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DEPARTMENT OF THE ARMY TECHNICAL MANUAL

GENERAL SUPPORT AND DEPOT MAINTENANCE MANUAL

TEST SET, TELETYPEWRITER TS-800/UGM-1

This copy is a reprint which includes current
Pages from Changes 1 and 2

HEADQUARTERS, DEPARTMENT OF THE ARMY

14 MARCH 1968

WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working on or near the 115 or 230—volt ac line connections. Serious injury or DEATH may result from contact with these terminals.

DON'T TAKE CHANCES!

Change

No. 2

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 1 August 1986

**General Support and Depot Maintenance Manual
TEST SET, TELETYPEWRITER TS-800/UGM- 1
(NSN 6625-00-965-0197)**

TM 11-6625-620-45-2, 14 March 1968, is changed as follows:

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WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working on or near the 115- or 230-volt ac line connections. Serious injury or DEATH may result from contact with these terminals.

WARNING

When troubleshooting or making repairs on this equipment be extremely careful. Voltages as high as 230V are present in the test set. Use insulated test probes when making voltage measurements. Always disconnect the power cords before touching any internal parts.

CAUTION

Use extreme care when performing maintenance of the printed circuit boards.

CAUTION

Make sure that the power cable is never connected to a 230 volt ac source with the POWER switch locking guard permitting the POWER switch to be set to the 115 volt position. Setting the POWER switch to the 115 volt position with equipment connected to a 230 volt source can damage the equipment.

CAUTION

Do not make resistance measurements on the distortion analyzer unless specifically directed to do so. The battery voltage of an ohmmeter can damage the transistors.

TECHNICAL MANUAL }
 No. 11-6625-620-45-2 }

HEADQUARTERS
 DEPARTMENT OF THE ARMY
 WASHINGTON, D. C., 14 March 1968

General Support and Depot Maintenance Manual

TEST SET, TELETYPEWRITER TS-800/UGM-1

(NSN 6625-00-965-0197)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter or DA Form 2028 (Recommended Changes to Publications and Blank Forms) direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, NJ 07703-5007.

In either case, a reply will be furnished direct to you.

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*This manual supersedes TM 11-6625-620-45-2, 6 December 1966.

CHAPTER 1 INTRODUCTION

Section I. GENERAL

1-1. Scope

a. This manual contains general support and depot maintenance instructions for Test Set, Teletypewriter TS-800/UGM-1. It includes instructions appropriate to general support and depot maintenance personnel for troubleshooting, testing and repairing the equipment. It also lists tools, materials, and test equipment required for general support and depot maintenance. Functional analysis of the equipment is also covered.

b. The complete technical manual for this equipment includes TM 11-6625-620-12 and TM 11-6625-620-25P-2.

1-2. Consolidated Index of Army Publications and Blank Forms

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

1-2.1. Maintenance Forms, Records and Reports

a. *Reports of Maintenance and Unsatisfactory Equipment.* Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750 as contained in Maintenance Management Update.

b. *Report of Packaging and Handling Deficiencies.* Fill out and forward SF 364 (Report of

Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73A/AFR 400-54/MCO 4430.3H.

c. *Discrepancy in Shipment Report (DISREP) (SF 361).* Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D DLAR 4500.15.

1-2.2. Destruction of Army Materiel To Prevent Enemy Use

Refer to TM 750-244-2 for procedures to be used for this equipment.

1-2.3. Administrative Storage

Refer to TM 760-90-1 for procedures to be used when equipment is to be placed in administrative storage.

1-2.4. Reporting Equipment Improvement Recommendations (EIR)

If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-PA-MA-D, Fort Monmouth, New Jersey 07703-5023. We'll send you a reply.

Section II. UNIT FUNCTIONING

1-3. General

Test Set, Teletypewriter TS-800/UGM-1 (distortion analyzer) provides a direct-reading, panel-meter indication of the amount of distortion present in a start-stop telegraph signal. It compares the position of the input signal transitions to an accurate time-base signal that is generated in the time-base circuits, and indicates whether the signal transitions are occurring at the correct time, early, or late. The EARLY lamp lights to indicate when the transitions are early; the LATE lamp lights to indicate when the transitions are late. The time-base circuits synchronize the time-base signal (reference) with the mark-to-space transition of the stop-mark and start-space. The distortion analyzer also compares the succeeding mark-to-space or space-to-mark transitions of the

input signal to this reference. The displacement of the telegraph-signal transitions with respect to the reference is directly indicated as a percent distortion indication on the PERCENT DISTORTION meter.

1-4. Block Diagram Analysis

(fig. 6-2)

a. *Signal-Input Circuits.* The signal-input circuits accept either neutral or polar telegraph signals for distortion analysis.

(1) Neutral or polar telegraph signals are applied to neutral and polar marking tone keyer No. 1 or to polar spacing tone keyer No. 2, as applicable, through POLARITY switch 1A1S2, CURRENT SELECT switch 1A1S3, and a noise- and interference-rejecting filter assembly. The

output from the tone keyers is applied to the first Schmitt trigger. When the FILTER switch is set to IN, an internal filter is connected to the input of the first Schmitt trigger which filters out any noise, spikes, or holes in the input signal that could cause erratic indications on the PERCENT DISTORTION meter.

(2) The output of the first Schmitt trigger is applied to the SIGNAL indicator lamp through two inverting amplifiers and also to a second Schmitt trigger. If the input signal to the distortion analyzer is in a marking state, the SIGNAL lamp lights.

(3) The output of the second Schmitt trigger is applied to the baud counter (i below) through the stop-mark and start-space transition gates. The second Schmitt trigger output is also applied to the synchronizing bistable through the mark-space and space-mark gates in the transition sampler circuits (f below).

b. Time-Base Circuits. A timing input signal from one of the four oscillators is selected by the RATE switch. The timing input signal is then shaped by the first monostable multivibrator and is applied to the frequency divider. The output of the frequency divider, which is 126 times the baud frequency, is applied to the timing input gate in order to control the timing signal applied to the digital time base counter (c below). A signal from the reset monostable is also applied to the digital time-base counter during the stop-mark as a set pulse.

c. Digital Time-Base Circuits. The digital time-base circuits include the digital time-base counter, reversing gates, inverting OR gates, and an inverting amplifier.

(1) An output from the timing input gate in the time-base circuits is applied to the digital time-base counter to produce four signals as follows:

(a) A seven-digit running binary that counts from 0 to 127 for the length of a character, during each ideal bit, except during a stop-mark when it counts from 0 to 63 (only 1/2 bit of the stop-mark).

(b) A six-digit reversible running binary that counts from 0 to 63 and 63 to 0 during each ideal bit except during a stop-mark.

(c) An early pulse during the 1/2-bit period (63 to 0 count) preceding each ideal transition time (except for the stop-mark/start-space transition), and a late pulse during the 1/2-bit period (0 to 63 count) following each ideal transition time.

(d) A pulse 1/2-bit after the stop-mark/stop-space transition, and a pulse every 128 counts for the length of the character which advances the baud counter.

(2) An output from the last stage in the digital time-base counter is applied to the baud counter advance (i below). Other outputs are applied to the early transition gate and the late transition gate of the transition control circuits (g below), and to the early selection gate and late selection gate of the early-late circuits (h below). The first six stages of the seven-stage binary digital time-base counter provide a 0 to 63 and 63 to 0 count through the reversing gates, inverting OR gates, and inverting amplifier, to the distortion comparator gates of the magnitude comparator circuits (d below), and the read-in gates of the digital-to-analog converter circuits (e below). The direction of the count (0 to 63 and 63 to 0) is controlled by the reversing gates.

d. Magnitude Comparator Circuits. The magnitude comparator circuits compare the instantaneous output of the first six stages of the digital time-base counter with the number stored in the storage register of the digital-to-analog converter circuits (e below).

- (1) After the distortion comparator gates compare the number with the one stored in the storage register, it is transferred to the transition control gate through the comparison gate. When DISTORTION SELECT switch 1A1S7 is set to one of the PEAK positions, and the count in the first six stages of the digital time-base counter is less than the number held in the storage register, the comparison gate is inhibited. This inhibits the transition control gate and the output of the inverting amplifier, and prevents the digital time-base output number from being read into the storage register. In this way, only the highest distortion measurement is held in the storage register when measuring peak distortion.
- (2) Momentarily depressing the RESET switch will reset the storage register to binary 000000. When the RESET switch is released, the number present in the digital time-base counter will be read into the storage register. If the number held in the storage register is less than the number in the digital time-base counter, when measuring peak distortion, an enabling pulse is applied to the transition control gate through the comparison gate.
- (3) The inverting amplifier output now permits the number from the digital time-base counter to be read into the storage register. When DISTORTION SELECT switch 1A1S7 is set to AVERAGE, the comparison gate is inhibited and each new number in the digital time-base counter can be read into the storage register.

e. Digital-to-Analog Converter Circuits. The digital-to-analog converter circuits consist of read-in gates, a storage register, meter drive circuits, and the PERCENT DISTORTION meter. The number held in the storage register is in digital form. It is converted to analog form by the meter drive circuits and is displayed on the PERCENT DISTORTION meter. The storage register is reset to a new number by the read-in gates when it is enabled by the transition control gate (*d* above). The output of the storage register is applied to both the meter drive circuits and to the distortion comparator gates.

f. Transition-Sampler Circuits. The transition-sampler circuits include the space mark and mark-space gates, reset gate, synchronizing bistable, transition inhibit gate (trigger gate), and transition monitor monostable. The transition-sampler circuits determine the type of transition to be monitored.

- (1) The output pulse from the transition monitor monostable is synchronized with the input signal transition by the synchronizing bistable. When a transition is received by the synchronizing bistable, an output is applied through the trigger gate to the transition monitor monostable. Another output of the synchronizing bistable, applied through a reset gate, immediately resets the synchronizing bistable to prepare it for the next transition.
- (2) When DISTORTION SELECT switch 1A1S7 is at TOTAL PEAK, both the space-mark and mark-space gates are enabled and all transitions are monitored. With DISTORTION SELECT switch 1A1S7 set at either EARLY PEAK or LATE PEAK, space-mark or mark-space transitions may be selected by the other DISTORTION SELECT switch, 1A1S6, and the corresponding early or late peak distortion will be monitored.
- (3) With DISTORTION SELECT switch 1A1S7 set at AVERAGE, space-mark or mark-space transitions

may again be selected by DISTORTION SELECT switch 1A1S6, and the corresponding average distortion of the selected transition will be monitored.

g. Transition-Control Circuits. The transition-control circuits include the transition-control gate, the early and late transition gates, the comparison gate, the inverting amplifier, and DISTORTION SELECT switches 1A1S6 and 1A1S7.

- (1) Six inputs are applied to the transition-control gate to determine exactly when a new number from the digital time-base counter should be read into the storage register.
 - (a) The first input, applied through the comparison gate, is produced by the distortion comparator gates in the digital-to-analog converter circuits, which compare the six-digit binary number in the storage register to the reversible running output from the inverting OR gates and to the inverting amplifier of the digital time-base circuits.
 - (b) Starting at each ideal transition time, the reversible running binary increases its count until the midpoint of a bit and then decreases its count until the next ideal transition time. The instantaneous value of the reversible running binary is always proportional to the displacement of a transition.
 - (c) When the distortion analyzer is set to measure peak distortion and the reversible running binary count in the distortion comparator gates is less than the stored binary number in the storage register, the comparison gate will inhibit the transition control gate. In this way, it precludes the possibility of reading into the storage register any numbers that would indicate a level of distortion less than that already displayed on the PERCENT DIS-

TORTION meter. The transition-control gate is not inhibited by the comparison gate during average distortion measurements.

- (d) The second and third inputs, early and late pulses from the early and late transition gates in the transition-control circuits, inhibit the transition-control gate during the 1/2-bit period after each ideal transition time. This will prevent measurements of early distortion during late peak distortion measurements, and before each ideal transition time to prevent measurements of late distortion during early peak distortion measurements.
- (e) The fourth input, from the transition gate of the baud distributor circuits (i below), enables the transition-control gate from a 1/2-bit period preceding to a 1/2-bit period following the ideal time of the transition as selected by TRANSITION SELECT switch 1A1 S9. When TRANSITION SELECT switch 1A1S9 is set at ALL, the transition gate enables the transition-control gate for all transitions.
- (f) The fifth input, from the transition selection gating circuits (stop-mark/start-space transition inhibit gate), inhibits the transition-control gate during the first 1/2-bit period of each start-stop character, and thus establishes the stop-mark/start-space transition as the reference transition.
- (g) The sixth input, produced by the transition monitor monostable of the transition-sampler circuits, is a short enabling pulse produced at the time of each mark/space or space/mark transition (as determined by DISTORTION SELECT switches 1A1S6 and 1A1S7). During total peak distortion measurements, both monitored transitions

produce an enabling signal to the transition-control gate.

- (2) The output of the transition-control gate (a short pulse at the time of a selected transition) is inverted and applied to the read-in gates of the digital-to-analog converter circuits. During measurements of average distortion, the transition-control gate also enables the early and late selection gates through an inverting amplifier. To summarize, the function of the transition-control gate is to produce an enabling-pulse output for the read-in gates at the time of an input signal transition if the following is true:
 - (a) The transition is of the polarity selected by DISTORTION SELECT switch 1A1S6 (both transitions during total peak distortion measurements).
 - (b) The time is within the 1/2-bit period of the ideal time of the transition selected by TRANSITION SELECT switch 1A1S9.
 - (c) The time is before the ideal transition time (early peak only).
 - (d) The time is after the ideal transition time (late peak only).
 - (e) The count in the digital time-base counter is greater than that stored in the storage register at the time of the transition (except during average distortion measurements).

h. Early-Late Circuits. The early-late circuits consist of the early and late selection gates, a holding bistable, early and late driver gates, and EARLY and LATE indicators.

- (1) During measurements of average distortion, the digital time-base counter supplies a condition pulse of 1/2-bit duration to the early selection gate (63 to 0 count) and a condition pulse of 1/2-bit duration to the late selection gate (0 to 63 count).
- (2) The transition-control gate applies an enabling pulse, through an inverting amplifier, during an early

or late transition to control the EARLY and LATE indicators. The EARLY and LATE indicators are inhibited during peak distortion measurements by the application of -15 volts through DISTORTION SELECT switch 1A1S7 to the early and late driver gates.

i. Baud Distributor Circuits. The baud distributor circuits include the stop-mark/start-space transition gate, the baud counter, transition selection gating circuits, inverting amplifiers, the transition gate, and the CHARACTER SYNC jack.

- (1) The digital time-base counter advances the baud counter one count for each ideal bit of any character (0 to 127 count) except the stop-mark.
- (2) The baud counter, which is, in effect, a continuation of the digital time-base counter, produces a three-digit binary number proportional to the bit positions (start-space, first bit, second bit, third bit, fourth bit, fifth bit, stop-mark, and stop-mark/start-space transition). The first six digits are compared to the setting of TRANSITION SELECT switch 1A1S9, and cause the appropriate output to be selected from transition selection gating circuits.
- (3) One-half bit after the stop-mark transition, count-6 gate is enabled. The output of the count-6 gate is applied to the met monoatable of the time-base circuits (which resets the digital time-base counter to 127 or 1111111), and inhibits the timing input gate of the time-base circuits to insure that no timing pulses occur between characters.
- (4) The output of count-6 gate is also applied to the stop-mark/start-space transition gate through an inverting amplifier. It conditions the gate so that the stop-mark/start-space transition advances the baud counter one full count and enables the count-7 gate as described in (6) below.

- (5) The inverting amplifier output is also applied to the CHARACTER SYNC jack through a second inverting amplifier to provide a negative-going transition that coincides with the end of each character. A positive-going transition is also available to coincide with the start of each character. The output of the inverting amplifier also inhibits the transition inhibit (trigger) gate in the transition sampler circuits.
- (6) TRANSITION SELECT switch 1A1S9 conditions the selected transition gating circuits. The selected gates (count 0 through count 7) are enabled by an output from the baud counter. When a selected gate is enabled, its output triggers the transition gate. The transition gate conditions the transition-control gate of the transition-control circuits during the time of the transition to be monitored.
- (7) The output of the transition gate is a 1-bit pulse, centered about the ideal time of the selected transition. This is accomplished by comparing the output of the baud counter with the setting of TRANSITION SELECT switch 1A1S9. At the start of each character, the stop-mark/start-space transition of the baud counter enables the count-7 gate and inhibits the count-6 gate in the transition selection gating circuit.
- (8) The output of the count-7 gate inhibits the transition-control gate for 1/2 bit, and the stop-mark/start-space transition is not monitored. The number stored in the storage register of the digital-to-analog converter circuits does not change. The output of the inhibited count-6 gate enables the timing input gate in the time-base circuit, and the digital time-base counter is activated. The output of the count-6 gate also inhibits the stop-mark/start-space transition gate. At the count of 63, the

baud counter is advanced 1/2-bit after the stop-mark/start-space transition, and the count-0 gate is enabled.

j. Power Supply Block Diagram (fig. 6-2). Output voltages are + 15, -15, -120 volts direct current (dc). These voltages are developed from a 115- or 230-volt alternating current (ac) power source. The input is applied through line filter 1A1FL1 and switch 1A1S1. The ac power is applied to the primary of transformer T1 from switch 1A1S1.

- (1) *Regulated + 15-volt dc circuit.* The ac voltage from transformer T1 is converted to dc by bridge rectifier diodes CR1 through CR4, and regulated by 15-volt regulator transistor Q1 and Zener diode CR5.
- (2) *Regulated -15-volt dc circuits.* Bridge rectifier diodes CR6 and CR7 convert the ac to a -15-volt dc voltage that is regulated by transistor Q2 and Zener diode CR10.
- (3) *Regulated -10-volt dc circuit.* Zener diode CR11 regulates the -10 volts dc.
- (4) *Unregulated -120-volt dc circuits.* The ac voltage from transformer T1 is converted to dc by half-wave rectifier CR12.

k. Power Supply Circuit Analysis (fig. 6-10).

- (1) *Line voltage.* The line voltage (115 or 230 volts ac 50-60 Hertz (Hz)) is applied through line fuses 1A1F1 and 1A1F2 to line filter 1A1FL1 and to power switch 1A1S1, and then to the primary of transformer 1A3T1 and POWER lamp 1A1DS1. Transformer 1A3T1 has three step-down secondary windings.
- (2) *Regulated + 15-volt dc circuit.* Bridge rectifier diodes CR1 through CR4 convert the ac from transformer 1A3T1 secondary (terminals 5 and 6) to dc and is filtered by capacitor C1. Resistor R1 provides a discharge path for capacitor C1. Fuse F1 protects the + 15-volt dc circuit from

overload. Resistor R2 provides current limiting. When the output voltage developed across resistor R4 drops, Zener diode CR5 forward-biases transistor Q1, and allows more current to flow through transistor Q1 to provide the regulated +15 volts to associated assemblies. Resistor R3 provides current limiting for CR5 and the base of transistor Q1. If the output voltage developed across resistor R4 increases, CR5 reverse-biases the emitter-base junction of transistor Q1 and reduces the current through it. This reduces the voltage developed across resistor R4 to the regulated +15 volts. Resistor R5 provides isolation for test equipment connected to jack J1.

- (3) *Regulated -15-volt dc circuit.* Bridge rectifier diodes CR6 through CR9 convert the ac from transformer 1A3T1 secondary (terminals 7 and 8) to dc, and is filtered by capacitor C2. Resistor R6 provides a discharge path for capacitor C2. Fuse F2 protects the -15-volt dc circuit from overload. Resistor R7 provides current limiting. When the output voltage developed across resistor

R9 and Zener diode CR11 drops, CR10, forward-biases transistor Q2 and allows more current to be drawn through Q2 to provide a regulated -15 volts to associated assemblies. Resistor R8 provides current limiting for CR10 and the base of Q2. If the output voltage developed across CR11 and R9 increases, CR10 reverse-biases the emitter-base junction of Q2. This reduces the voltage developed across R9 and CR11 to the regulated -15 volts. Resistor R10 provides isolation for test equipment connected to jack J3.

- (4) *Regulated -10 volts dc.* Zener diode CR11 provides -10 volts regulation with voltage-dropping resistor R9. Resistor R11 provides isolation for test equipment connected to jack J4.
- (5) *Unregulated -120-volt dc circuit.* The output of transformer 1A3T1 (secondary terminals 9 and 10) is half-wave rectified by CR12 and filtered by R12 and capacitor C3. Resistor R14 provides isolation for test equipment connected to jack J5. Resistor R13 is the bleeder resistor that provides a discharge path for capacitor C3.

Section III. CIRCUIT ANALYSIS AND LOGIC SYMBOLS

1-5. General

a. Many of the stages in the distortion analyzer are identical except for the parts values and the reference designations used. *For example*, the seven bistable multivibrator stages (FFC-8 through FFC-14) which make up the digital time-base counter contain identical circuits. Therefore, the circuit analysis of the distortion analyzer provided in this manual is of each type, rather than of each individual stage. The circuit analyses of the different types of stages are contained in paragraphs 1-6 through 1-14. All referenced symbols are shown on the logic diagram (fig. 6-3).

b. Reference designations, such as Ca, Rc, and Qa (figs. 1-1 through 1-10) are arbitrarily assigned to assist in making the circuit analyses (paras 1-6 through 1-14). To determine the correct reference designation for a specific part within a particular stage, refer to the applicable schematic diagram.

c. Designations such as 0 and 1 are the logic symbols used to define voltage levels. A 0 represents a high-level potential very near ground (0 volt), and a 1 represents a low-level potential (approximately -15 volts). Because of the potential differences between 0 and 1, a transition from 0 to 1 produces a negative pulse, and a transition from

1 to 0 produces a positive pulse. The more negative of two given logic levels (1) is represented by the presence of a small circle at the input or output points of the logic symbol; conversely, the more positive level (0) is represented by the absence of the circle. The logic levels shown at the inputs and outputs of gate and amplifier logic symbols are those present when the logic element is active (i.e., when it is performing its principal function). For example, if the symbol is that of an AND function, the logic levels shown include the required inputs and resultant output level developed when the AND stage is operating.

1-6. Bistable Multivibrator Stages

(fig. 1-1)

a. *General.* Three variations of a bistable multivibrator stage are used in the distortion analyzer, two of which are illustrated in figure 1-1. The logic symbol, used with the logic diagram (fig. 8-3) and shown directly below each bistable multivibrator stage, is the same for each bistable multivibrator, because their functions are the same.

- (1) The reference designations for the logic symbols of the bistable multivibrator stages differ, and indicate the manner in which they are triggered. The lines on the left side of the logic symbols represent inputs (including the reset provisions). The lines on the right side of the logic symbols represent outputs. The upper lines (left and right) of the logic symbol are associated with one of the transistors in the stage, and the lower lines (left and right) are associated with the other transistor.
- (2) Bistable multivibrators are set by applying a positive-going transition (logical-1 to logical-0) to the set (S) input, thereby producing a logical-1 at the 1 output and a logical-0 at the 0 output. An identical input transition applied to the clear (C) input resets the flip-flop, pro-

ducing a logical-0 at the 1 output and a logical-1 at the 0 output. When a logical-1 is present at the 1 output, the flip-flop is defined as being in its 1-state; a logical-0 at the 1 output defines the 0-state.

b. *Circuit Analysis.* Resistors R_e and R_f establish the initial bias for transistors Q_a and Q_b , respectively. Resistors R_a and R_b are the collector load resistors. Resistors R_c and R_d and capacitors C_a and C_b determine the switching time required for the stage to change state. The outputs, which are 180° out of phase with each other, are developed across the collector and emitter of transistors Q_a and Q_b .

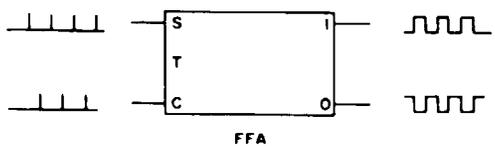
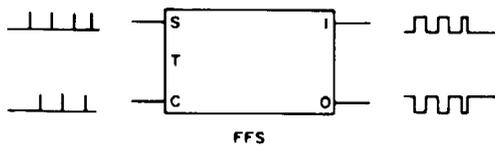
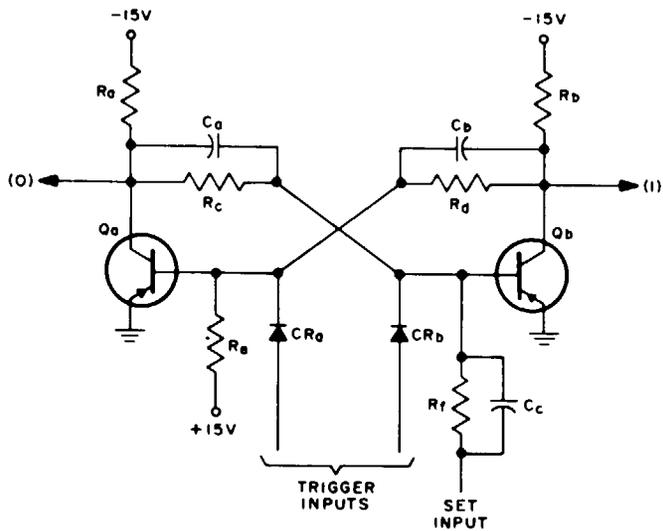
c. *Triggering.* The stages shown in figure 1-1 require positive pulses at the inputs. If the transistor associated with a given input is conducting when the positive pulse is applied through steering diode CR_a or CR_b (B, fig. 1-1), the transistor will cut off. A second positive input pulse through the opposite steering diode will return the stage to its original state. The state shown in B, figure 1-1 will change each time a positive pulse is applied through differentiating network C_d and R_3 and steering diodes CR_a and CR_b .

d. *Set.* The set input triggers (A and B, fig. 1-1) are employed to place the bistable multivibrators FFS stages into predetermined states. Bistable multivibrator FFA is the same as the FFS type (B, fig. 1-1), except that it does not have a set trigger.

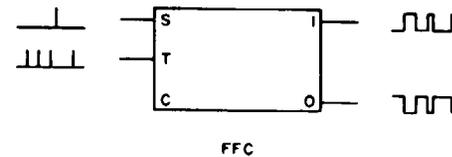
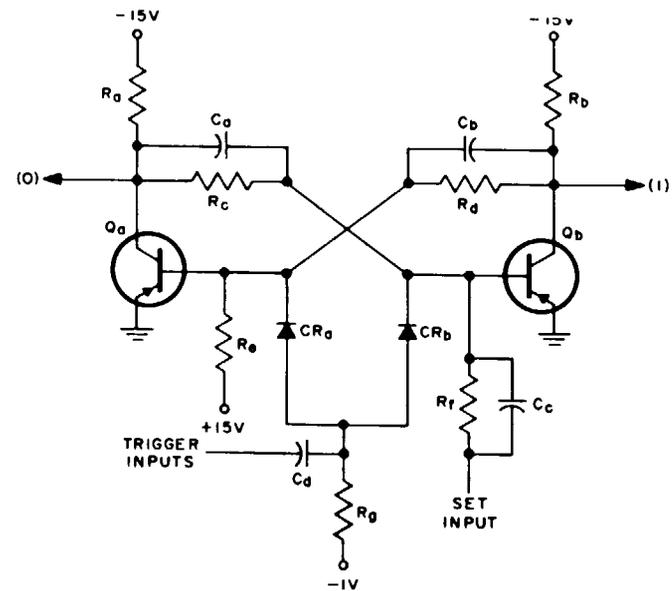
1-7. Monostable Multivibrator Stages

(fig. 1-2)

a. *General.* Three variations of a monostable multivibrator stage are used in the distortion analyzer, two of which are shown in figure 1-2. The logic symbol, used with the logic diagram (fig. 6-3) and shown directly below each monostable multivibrator stage, is the same for each monostable multivibrator, because their functions are the same. The reference designations for the logic symbols of the monostable multivibrator stages differ, and indicate the manner in which they are triggered. The lines on the left side of the logic symbols represent the inputs, and the lines on the right side represent the outputs.



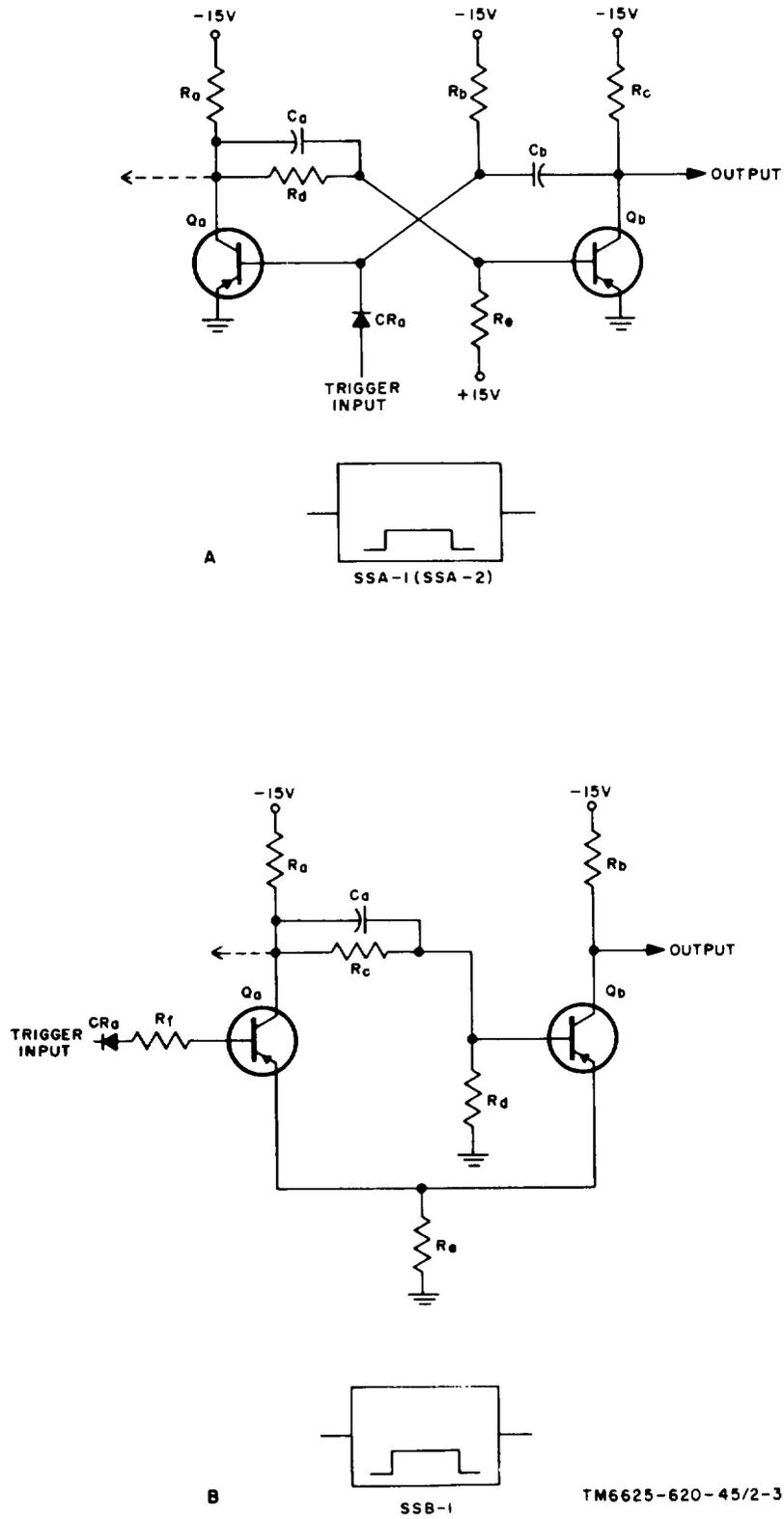
A.



B.

TM6625-620-45/2-2

Figure 1-1. Bistable multivibrator stage.



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Figure 1-2. Monostable multivibrator stage.

b. Circuit Analysis.

- (1) The set-input trigger is applied through steering diode CRa to transistor Qa, which is normally conducting. A positive input pulse is then required to trigger the stage (A, fig. 1-2) (SSA-1). For SSA-2, the steering diode is reversed and the set-input trigger is applied to transistor Qb, which is normally cut off. In this case, a negative pulse is required to trigger the stage. Resistors Ra and Rc, (A, fig. 1-2) are collector load resistors; resistors Rb and Re establish the initial bias; and resistor Rd, with capacitors Ca and Cb, determines the switching time required to return the stage to its original state.
- (2) In B, figure 1-2 the set-input trigger is applied through steering diode CRa and limiting resistor Rf to the base of transistor Qa, which is normally cut off. A negative input pulse is then required to trigger the stage. Resistors Ra and Rb are collector load resistors; resistors Rd and Rc establish the initial bias; and resistor Rc, with capacitor Ca, determines the switching time required to return the stage to its original state.

1-8. Schmitt Trigger Stages

(fig. 1-3)

a. General. The two Schmitt Trigger Stages are of the same type. The logic symbol shown directly below each stage is used with the logic diagram (fig. 6-3). The line on the left side of the logic symbol represents the input, and the lines on the right side represent the output. The 0 output is in phase with the input, and the 1 output is 18° out of phase with the input.

b. Circuit Analysis. Transistor Qa and resistor Ra provide the stage with a relatively constant input resistance. Resistors Rb and Rc are collector load resistors, resistors, Rg and Rh are common emitter resistors, and Re and

Rf compensate for hysteresis loss in the circuit. Voltage-dividing network resistors Rb, Rd, and Ri provide bias for transistor Qc; and capacitor Ca, with resistor Rd, provides coupling from the collector of transistor Qb to the base of transistor Qc.

1-9. AND Gate Stages

(fig. 1-4)

a. General. Four types of AND gate stages are used. The function of each AND gate is the same; therefore, the logic symbol shown directly below each stage and used with the logic diagram (fig. 6-3) is the same for each stage, except for the number of inputs available. The lines on the left side of the logic symbols represent inputs. A circle on an input line indicates that the signal is applied through a switch, and whenever the switch is in the open position, an inhibit voltage is applied to the gate. Typical input and output waveforms are shown for normal operation.

b. Circuit Analysis. An AND gate stage will develop an output when coincident input pulses are present on the input lines.

- (1) The AND gate stage shown in A, figure 1-4, uses capacitor Ca and resistor Ra in the inputs, and diode CRa in the output. The waveforms shown with the logic symbol indicate that the leading pulse of two positive coincident pulses is required to provide a positive output spike.
- (2) The AND gate shown in B, figure 1-4, uses diode CRa with forward-biasing resistor Ra, and capacitor Ca for the inputs. The waveforms shown with the logic symbol indicate that, with a negative level applied to CRa, the leveling edge of a positive pulse will provide a positive output spike and the trailing edge of a positive pulse will provide a negative output spike.
- (3) The AND logic function shown in C, figure 1-4, is performed with input diodes CRa and CRb and load resistor Ra. The waveforms shown indicate that two negative coincident

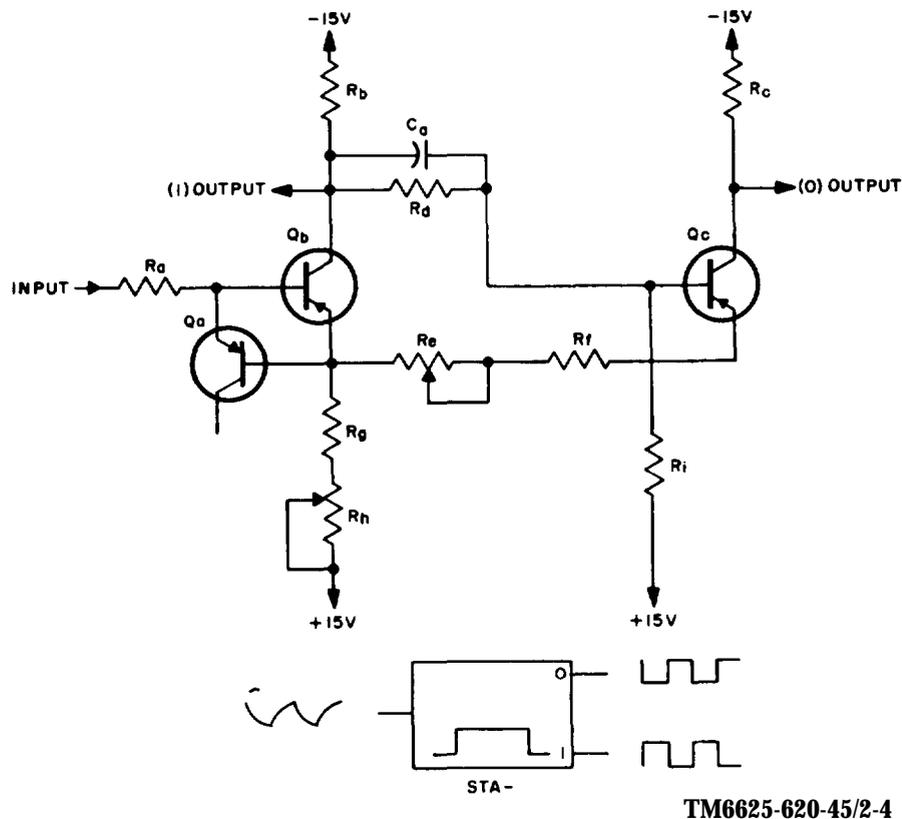


Figure 1-3. Schmitt trigger stage.

- pulses are required to provide a negative output pulse.
- (4) Resistors Ra, Rb, and Rc are input coupling resistors for the AND gate stage shown in D, figure 1-4. Resistor Rf is the collector load resistor and resistor Re establishes reverse bias for transistor Qa. Resistor Rd is the inhibit load resistor when the input is open. The waveforms shown with the logic symbol indicate that three positive coincident pulses are required to provide a negative output pulse.

1-10. OR Gate Stages
(fig. 1-5)

Two variations of OR gate stages are used. The function of each OR gate stage is the

same; therefore, the logic symbol shown directly below each stage and used with the logic diagram (fig. 6-3) is the same for each stage. Typical input and output waveforms are shown for normal operation.

a. Input diodes CRa and CRb and load resistor Ra make up the OR gate stage shown in A, figure 1-5. The waveforms shown with the logic symbol indicate that a positive output pulse occurs when a positive input pulse is present on either input line.

b. Resistors Ra and Rb are input coupling resistors for the OR gate stage shown in B, figure 1-5. Resistor Rc establishes reverse bias, and resistor Rd is the collector load resistor for transistor Qa. The waveforms shown with the logic symbol indicate that negative pulses on any one of the input lines provide a positive output pulse.

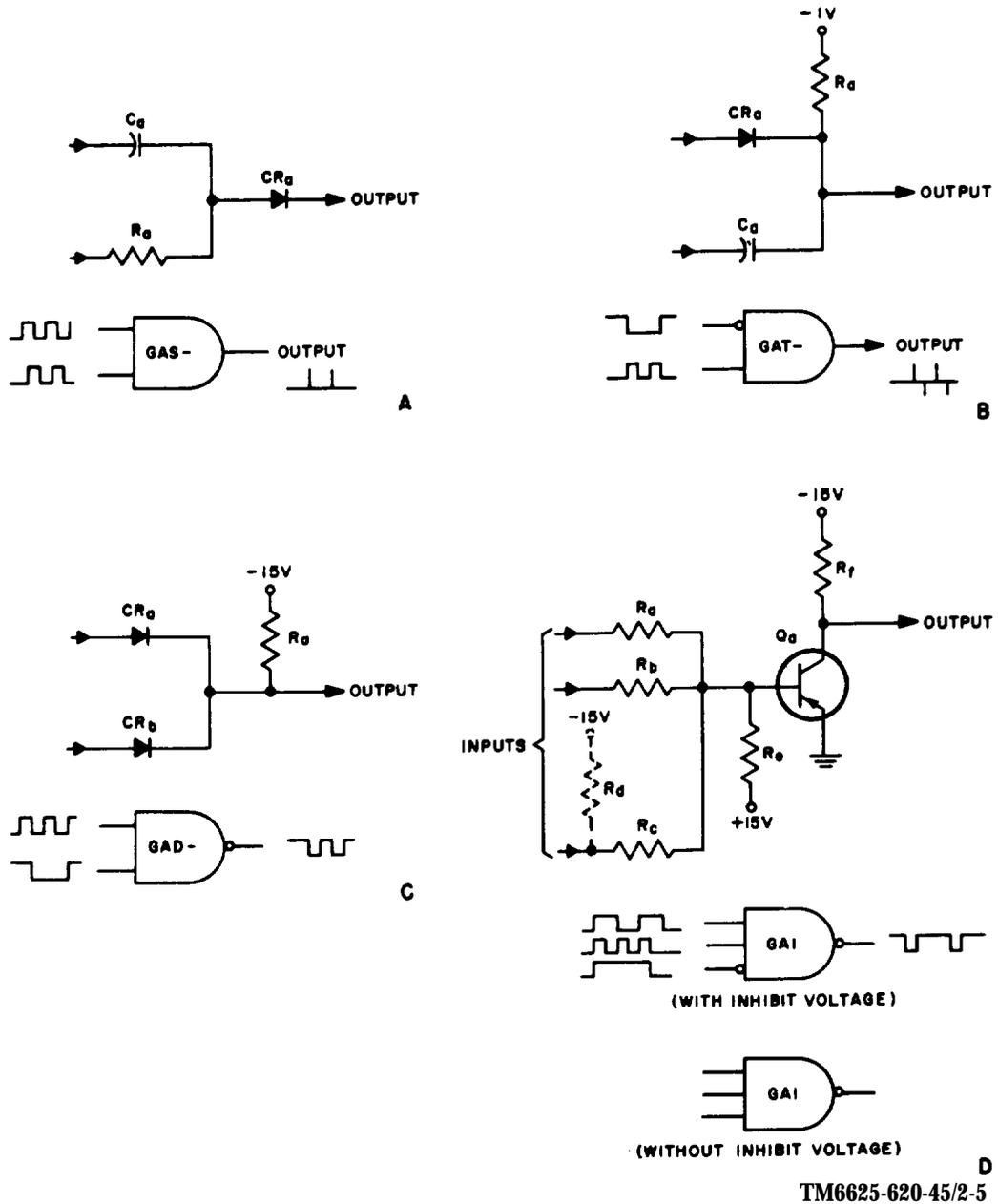


Figure 1-4. AND gate stage.

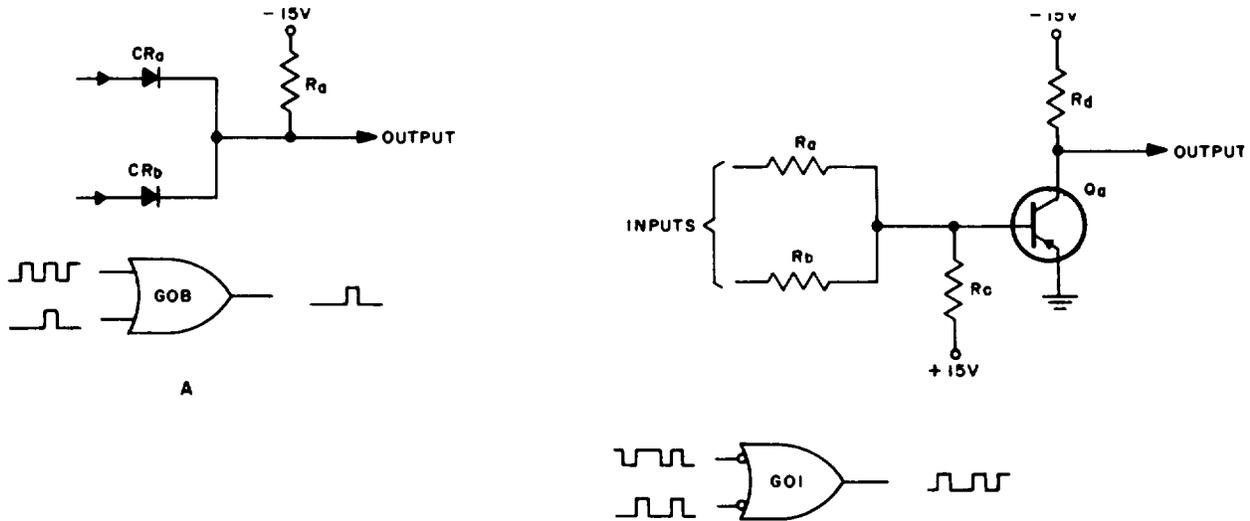
1-11. Amplifier Stages
(fig.1-6)

a. *General.* The inverting amplifier stage shown in A, figure 1-6 and the emitter follower shown in B, figure 1-6 are used. The lines on the left side of the logic symbol are input lines, and the lines shown on the right

side are output lines. Typical input and output waveforms representing normal operation are shown with the logic symbols (A and B, fig. 1-0).

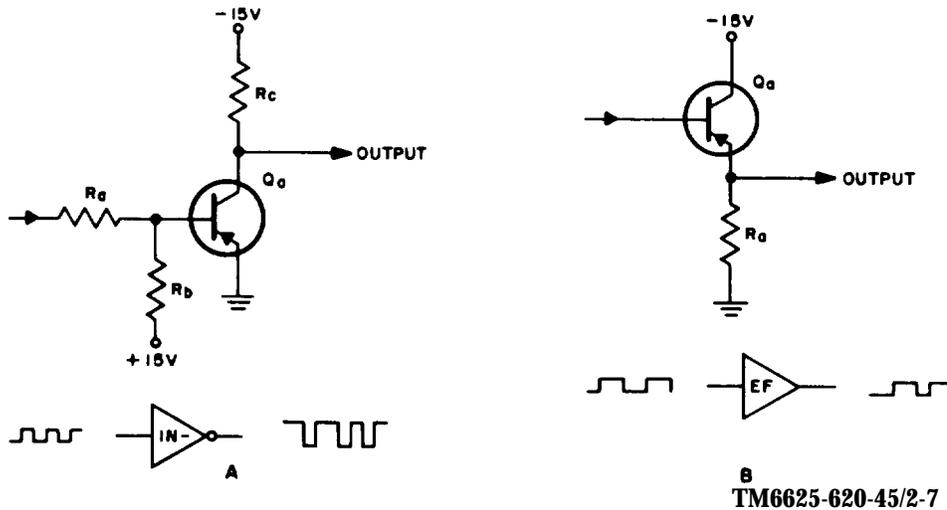
b. *Circuit Analysis.*

- (1) Resistor Ra is the input coupling resistor for the inverter stage shown



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Figure 1-5. OR gate stage.



TM6625-620-45/2-7

Figure 1-6. Amplifier stage.

in A, figure 1-6. Resistor Rb establishes reverse bias and resistor Rc is the collector load resistor for transistor Qa. The waveforms shown with the logic symbol indicate that the input waveform is amplified and inverted by the stage.

(2) Resistor Ra is the emitter load resistor for the emitter follower stage shown in B, figure 1-6. The waveforms shown with the logic symbol indicate that no amplification takes place because the emitter follower stage is primarily used for impedance matching.

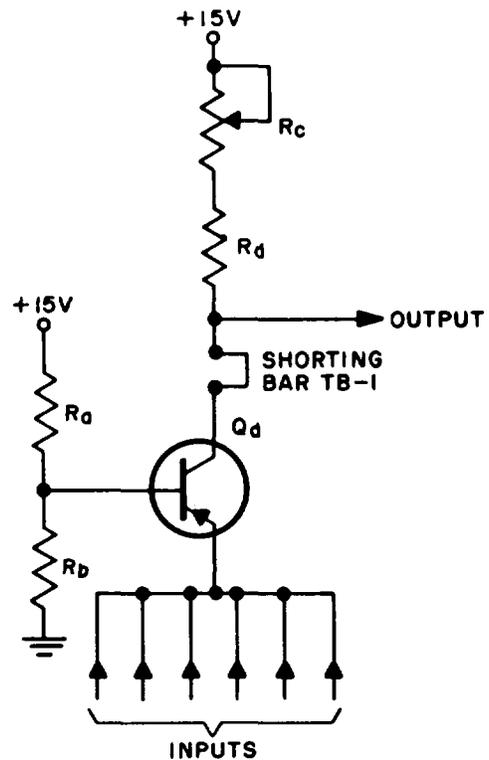
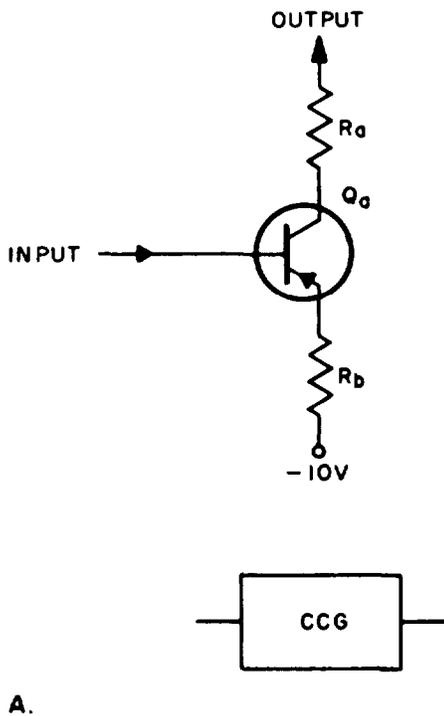
1-12. Constant-Current Generator and Current Summary Circuits

(fig. 1-7).

a. *General.* The constant-current generator stage used with its logic symbol is shown in A, figure 1-7. The type of summing stage used with its logic symbol is shown in B, figure 1-7. The lines on the left side of the logic symbols represent input lines, and the lines on the right side represent output lines. The logic symbols are used with the logic diagram (fig. 6-3). No input or output waveforms are shown with these logic symbols (fig. 1-7) because both stages produce a current level in the output.

b. *Circuit Analysis*

- (1) The constant-current generator stage shown in A, figure 1-7 is a digital-to-analog converter. Resistor R_b establishes the direct current (dc) voltage level applied to the emitter of transistor Q_a . Resistor R_a is the collector load. With the input voltage, either 0 or -15 volts dc, transistor Q_a is reverse-biased, and no current is produced in the output.
- (2) Voltage-dividing resistors R_a and R_b shown in B, figure 1-7, bias transistor Q_a in the active region.



B.

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Figure 1-7. Constant-current generator and summing stages.

Variable resistor r_c and resistor R_d make up the collector load. Shorting bar SB-1 is removable to permit measurement of the collector current. The input current to the summing stage is supplied by the constant-current generator stage ((1) above). The sum of the currents applied to the inputs of the summing stage provides the necessary current to operate the PERCENT DISTORTION meter (not shown), which is paralle-connected with variable resistor R_c and resistor R_d .

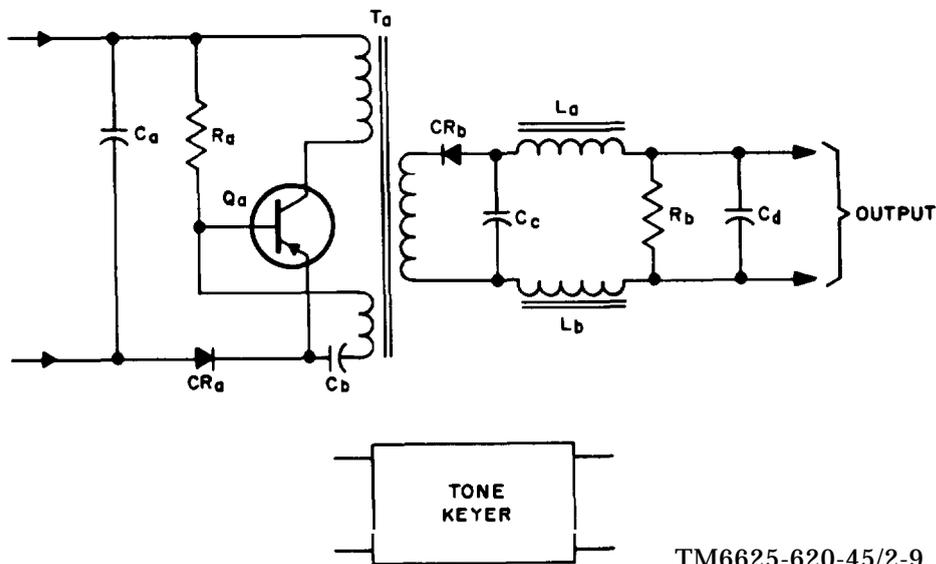
b. Circuit Analysis. Transistor Q_a , resistor R_a , the primary of transformer T_a and the inherent capacitance of the circuit make up an oscillator circuit which is triggered by the input signal, Capacitor C_a isolates the oscillator from the signal input. Diode CR_a isolates tone keyer No. 1 from tone keyer No. 2. Capacitor C_b prevents the base-emitter circuit of transistor Q_a from shorting through the primary winding of transformer T_a . The output signal is applied through half-wave rectifier CR_b , filter capacitors C_c and C_d , filter chokes L_a and L_b , and is developed across load resistor R_b .

1-13. Tone-Keyer Stages
(fig. 1-8)

a. General. Two tone-keyer stages are used in the signal input circuit, and the type used is shown in the figure. The logic symbol shown directly below the stage is used with the logic diagram (fig. 6-3). The lines on the left side of the logic symbol represent inputs, and the lines on the right side represent the output. The waveforms shown with the logic symbol indicate that the tone-keyer stage will produce an output for a neutral signal and for positive or negative polar signals.

1-14. Time Base Frequency-Divider Network
(fig. 1-9)

a. General. Four bistable multivibrator stages are used in the time-base circuits in a frequency-divider network, which divides the oscillator circuit output to a frequency which is equal to 128 times the baud rate. Stages FFC-1, FFC-2, and FFC-3 are the same as that shown in A, figure 1-1, except that the latter has no set input and the 0 output line is not used. Fourth bistable multivibrator



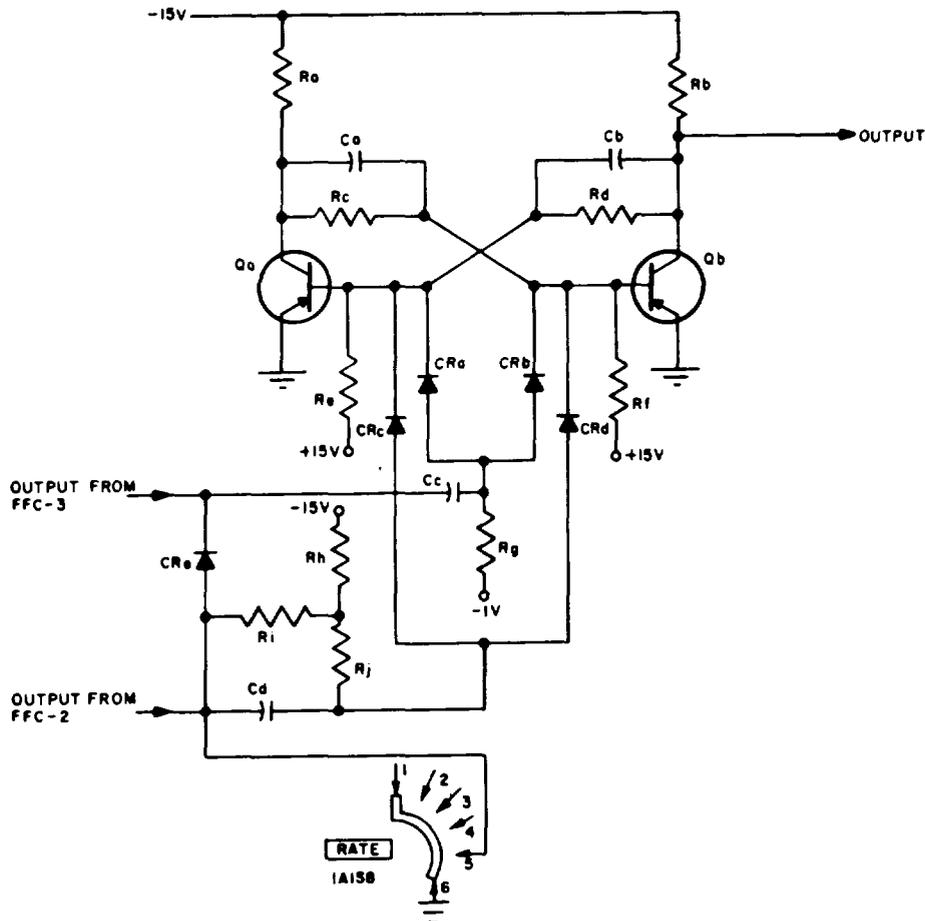
TM6625-620-45/2-9

Figure 1-8. Tone-keyer stage.

FFC-4, of the time-base frequency-divider network, is shown in figure 1-9.

b. Circuit Analysis. Resistors R_e and R_f establish the initial bias for transistors Q_a and Q_b , respectively; resistors R_a and R_b are the collector load resistors; and resistors R_c and R_d , with capacitors C_a and C_b , determine the switching time required for the stage to change state. Resistors R_h and R_j reverse-bias diodes CR_c and CR_d in all RATE switch 1A1S8 positions except for 150 BAUDS (position 5). When the RATE switch is set to position 5, resistors R_h and R_i are used to forward-bias diodes CR_c and CR_d . Diode CR_e clamps FFC-3 at ground when the RATE switch is set to position 5.

c. Triggering. Bistable multivibrator stage FFC-4 requires a positive pulse at the inputs.. Because there are two sets of steering diodes (CR_a and CR_b , and CR_c and CR_d), this stage may be controlled by two separate inputs. When RATE switch 1A1S8 is set to 150 BAUDS (position 5), steering diodes CR_c and CR_d are forward-biased. Because a ground is also applied through diode CR_e to the 1 output of FFC-3, the output from bistable multivibrator stage FFC-2 controls the stage. When RATE switch 1A1S8 is set to any other position, steering diodes CR_c and CR_d , as well as diode CR_e , are reverse-biased and cause the output from FFC-3 to control the stage.



FFC-4

TM6625-620-45/2-10

Figure 1-9. Time-base frequency-divider network

Section IV. LOGIC ANALYSIS

1-15. Signal Input Circuit

(fig. 6-3)

a. Neutral or polar telegraph signals are applied through SIGNAL INPUT jack 1A1J1, and then to POLARITY switch 1A1S2. The telegraph signal is converted from a current level signal to a voltage level signal by the converter to provide for operation of the tone keyers. Tone keyers No. 1 and No. 2 isolate all received telegraph signals from ground, thus providing an output equivalent to a polar-type telegraph signal. When POLARITY switch 1A1S2 is in the appropriate position for a particular type of input signal, tone keyer No. 1 is activated by either neutral or polar marking signals, and tone keyer No. 2 is activated by only polar spacing signals.

b. The output from the tone keyers is selected by CURRENT SELECT switch 1A1S3 and is applied to Schmitt trigger STA-1. Schmitt trigger STA-1 shapes the signal and drives Schmitt trigger STA-2. The output of STA-2 is applied through inverting amplifiers IN-1 and IN-2 to SIGNAL indicator lamp 1A1DS1, which lights when the input signal is in a marking condition. Spikes or holes in the signal, which could cause erroneous indications on PERCENT DISTORTION meter 1A1M1, are eliminated when FILTER switch 1A1S4 is set to IN.

c. Schmitt trigger STA-2 provides additional shaping of the signal, which is applied to inverting AND gate GAI-1. AND gate GAI-1 provides an output which is used to reset bistable FFC-5 (para 1-24) during the stop-mark/start-space transitions only, to initiate each character cycle. The output of STA-2 is also applied to GAS-1 in the transition-sampler circuits (para 1-21).

1-16. Time-Base Circuits

(fig. 6-3)

a. The timing signal to be used for the distortion measurements is generated by one of four crystal oscillators. The oscillator circuit to be used is selected by RATE switch 1A1S8. The output of the selected oscillator is a sine wave and is shaped into a square wave by mon-

ostable SSB-1. It is then applied to four-stage frequency divider FFC-1 through FFC-4. The oscillator frequency is such that, after division by the four-stage divider, a timing signal of 128 times the baud frequency of the input signal is obtained.

b. The output of the four-stage divider is applied to inverting AND gate GAI-4 together with an input from the inverting AND gate GAI-2 in the baud distributor circuits. AND gate GAI-2 supplies a high-level signal to GAI-4 from the start of a character through 1/2-bit of the stop-mark bit. This high-level signal from GAI-2 enables GAI-4 so that a timing signal from the frequency divider may be applied to the digital time-base circuits (para 1-17). The low-level signal from GAI-2 (from 1/2-bit into the stop-mark bit until the stop-mark/start-space transition of the next character) inhibits GAI-4, and the timing signal is not applied to the digital time-base circuits.

c. When a low-level signal from GAI-2 is applied to monostable SSA-2, the negative low-level output of SSA-2 is applied to the digital time-base circuit as a set pulse for the digital time-base counter.

d. The output of GAI-4 is also applied to inverting AND gate GAI-3 in the transition-sampler circuits (para 1-21).

1-17. Digital Time-Base Circuits

(fig. 6-3)

a. *General.* The digital time-base counter (FFC-8 through FFC-14) is controlled by AND gate GAI-4 in the time-base circuits. Because the signal from the time-base circuits is 128 times the baud frequency of the input signal, it enables the digital time-base counter to count from zero to 127 during each bit of the input signal, except during the stop mark (para 1-16b). The count from the digital time-base counter is taken from bistables FFC-8 through FFC-13, and only the zero to 63 count is used. The outputs from the 0 output lines of bistables FFC-8 through FFC-13 (complementary count) are applied to odd-numbered AND gates GAD-1 through GAD-

11, and the outputs from the 1 output lines of bistables FFC-8 through FFC-13 (true count) are applied to even-numbered AND gate GAD-2 through GAD-12.

- (1) The output from the 0 output line of bistable FFC-14 is applied to the remaining input line of odd-numbered AND gates GAD-1 through GAD-11 through emitter follower EF-1, and the output from the 1 output line of bistable FFC-14 is applied to the remaining input line of even-numbered AND gates GAD-2 through GAD-12 through emitter follower EF-2. AND gates GAD-1 through GAD-12 are therefore controlled by bistable FFC-14, which can change its state only once during the entire zero to 127 count (the 0 output line of FFC-14 is at 1 from the 64 to 127 count). A true count (zero to 63 from the 1 output lines of bistable FFC-8 through FFC-13) is obtained at the output of the even-numbered AND gates (GAD-2 through GAD-12) as the digital time-base counter counts from zero to 63.
- (2) A complimentary count (63 to zero, from the 0 output lines of bistables FFC-8 through FFC-13) is obtained at the output of odd-numbered AND gates GAD-1 through GAD-11 as the digital time-base counter counts from 64 to 127. The outputs of AND gates GAD-1 through GAD-12 are applied, through inverting OR gates GOI-1 through GOI-6, to the X1 through X6 lines, respectively. The outputs on the X1 through X6 lines therefore provide a zero to 63 and 63 to zero count. The outputs from gates GOI-1 through GOI-6 are also applied, through inverters IN-5 through IN-10, to the $\overline{X1}$ through $\overline{X6}$ lines, respectively. The outputs on the \overline{X} through $\overline{X6}$ lines therefore provide a 63 to zero and zero to 63 count.

b. Operating Sequence. The digital time-base counter counts from zero to 127 for each bit of a character except the stop mark. For

the stop mark, the digital time-base counter counts from zero to 63 and stops until the stop-mark/start-space transition of the next character. The digital time-base counter is initially set to 127 (a 1 on each 1 output line of bistables FFC-8 through FFC-14 or 64 counts into the stop-mark bit) by monostable SSA-2. Monostable SSA-2 is triggered by count six AND gate GAI-2 in the baud distributor circuits, and monostable SSA-2, in turn, applies a set pulse to bistables FFC-8 through FFC-14.

- (1) The first pulse received from AND gate GAI-4 thus causes each bistable (FFC-8 through FFC-14) to change state. That is, the digital time-base counter advances one count from 127 (1111111) to zero (0000000). The resulting transition from 1 to 0 on the 1 output line of bistable FFC-8 triggers each succeeding bistable. The 1 output on the 0 output line of bistable FFC-14 is applied to one input of odd-numbered AND gates GAD-1 through GAD-11. The other input to each of these gates is a 1 from the 0 output line of bistables FFC-8 through FFC-13. When two low-level inputs are applied to each odd-numbered AND gate GAD-1 through GAD-11, the output of these gates will be a 1.
- (2) The 1 output is then inverted by OR gates GOI-1 through GOI-6 and appears on each X1 through X6 line as a 0 (000000). Another output from OR gates GOI-1 through GOI-6 is also inverted by inverters IN-5 through IN-10 and appears on each $\overline{X1}$ through $\overline{X6}$ line as a 1 (111111). The second pulse received from GAI-4 changes the state of bistable FFC-8, but has no effect on bistable FFC-9. When this occurs, the count is changed to 100000 on the X lines and to 011111 on the \overline{X} lines. The third input pulse changes the state of FFC-8 again, and it, in turn, changes the state of bistable FFC-9.

- (3) When the sequence of counting reaches 64, a 1 from the 1 output line of bistable FFC-14 is applied to even-numbered AND gates GAD-2 through GAD-12. The other input to each of these AND gates is a 0 from the 1 output line of bistables FFC-8 through FFC-13. Because only one input to each of the even-numbered AND gates is a high-level signal, the output of even-numbered AND gates GAD-2 through GAD-12 is a 0. Because the output from the odd-numbered gates is also a 0 (high-level input from each 1 output line), OR gates GOI-1 through GOI-6 are inhibited and the low-level output appears on the X1 through X6 lines as a 1 (111111).
- (4) The outputs of OR gates GOI-1 through GOI-6 are also inverted by inverters IN-5 through IN-10 and appear on the $\overline{X1}$ through $\overline{X6}$ lines as a 0 (000000). Thus, the outputs on the X lines are counts from zero to 63 and 63 to zero, and the outputs on the \overline{X} lines are counts from 63 to zero and zero to 63 for each series of 128 pulses received from the time-base circuit. In addition to its use in complementing the outputs from bistables FFC-8 through FFC-13, bistable is used to trigger the early-late circuits (para 1-23), and the early-late transition gates of the transition-control circuits (para 1-22), as well as to advance the baud counter in the baud distributor circuits (para 1-24).

1-18. Read-In Gates and Storage Register

(fig. 6-3)

a. Read-in gates GAS-3 through GAS-14, when enabled, apply input triggers to storage register bistables FFS-1 through FFS-6. The storage register bistables are thus set, or reset, depending on the condition of the X1 through X6 lines and the $\overline{X1}$ through $\overline{X6}$ lines in the digital time-base circuits. In order for the read-in gates to be enabled, two positive (high-level)

inputs must be applied. One of the inputs to the gates is from the digital time-base circuits; the other input is from transition-control AND gate GAI-15, through inverter IN-11 in the transition-control circuits.

b. AND gates GAS-3 through GAS-14 determine the number contained in the storage register. The X lines from the outputs of OR gates GOI-1 through GOI-6 provide one input to odd-numbered AND gates GAS-3 through GAS-13, and the \overline{X} lines from inverters IN-5 through IN-10 provide an input to even-numbered AND gates GAS-4 through GAS-14. The other input, common to all AND gates GAS-3 through GAS-1, is received from transition-control gate GAI-15, through inverter IN-11 in the transition-control circuits (para 1-22). The X outputs of the AND gates are connected to the C (reset) input lines of bistables FFS-1 through FFS-6.

c. The \overline{X} outputs of the AND gates are connected to the S (set) input line of bistables FFS-1 through FFS-6. When a positive transition is applied to the common input line of AND gates GAS-3 through GAS-14, the AND gates that have a 0 on their X or \overline{X} line place a 0 on the input to the storage register bistable to which they connect.

d. Thus, a 0 appearing on the X line causes a 0 to be stored in the associated storage register bistable, and a 0 appearing on the \overline{X} line causes a 1 to be stored in the associated storage register bistable. Therefore, the number placed in the storage register bistable is the output of the digital time-base counter as it appears on the X lines.

e. When RESET switch 1A1S5 is momentarily depressed, a ground potential is applied to the C (reset) input of each storage register bistable, which then resets the storage register to binary number 000000.

1-19. Magnitude Comparator Circuits

(fig. 6-3)

a. The magnitude comparator circuits compare the binary number stored at the \overline{Y} lines of the storage registers with the binary number present at the X output lines of the digital time-base counter for each transition during peak distortion measurement-s. When

the binary number held in the storage registers (Y lines) is larger than the binary number present at the output of the digital time-base counter (X lines), the magnitude comparator circuits prevent a new read-in from entering the storage registers. This insures an indication of maximum distortion on PERCENT DISTORTION meter 1A1M1 when measuring peak distortion.

b. When DISTORTION SELECT switch 1A1S7A is set to AVERAGE, a 1 is applied to comparison AND gate GAI-18. However, AND gate GAI-18 requires a 0 on each input line in order to apply a 1 to transition-control gate GAI-15. Therefore, with a 1 always applied to one input line, AND gate GAI-18 always applies a 0 to transition-control gate GAI-15 during average distortion measurement. Assuming each input of transition-control gate GAI-15 to be 0, the resultant 1 output will be inverted by inverter IN-11 and applied as a 0 to read-in AND gates GAS-3 through GAS-14. This will cause those read-in gates with a 0 on the other input line to trigger the storage register.

c. When DISTORTION SELECT switch 1A1S7 is set to any other position, a 0 is applied to one input of AND gate GAI-18. The other input to AND gate GAI-18 is obtained from AND gate GAI-28 in the magnitude comparator circuits. When a 0 is received at the input of AND gate GAI-18 from AND gate GAI-28 (the binary number held in the storage register is greater than the binary number present at the output of the digital time-base counter), AND gate GAI-18 applies a 1 to transfer control gate GAI-15. Each input of transition-control gate GAI-15 must be a 0; therefore, the resulting output from inverter IN-11 will inhibit a read-in from the digital time-base counter to the storage register.

d. Thus, when a 1 output is present at AND gate GAI-28 (binary number held in the storage register is less than the binary number present at the output of the digital time-base counter), AND gate GAI-18 applies a 0 to transition-control gate GAI-15. When each input of transfer control gate GAI-15 is at 0, the output from inverter IN-11 enables a new

read-in from the digital time-base counter to the storage register.

e. When the binary number stored at the \bar{Y} lines of the storage register is smaller than the binary number present at the X lines of the digital time-base counter, the magnitude comparator circuits apply the 0 from the output of AND gate GAI-18 to transition-control gate GAI-15. Assume that the output on the X lines of the digital time-base counter is the binary number 20 (010100), and the binary number stored on the Y lines of the storage register is 13 (001101); then the binary number present on the \bar{X} lines of the digital time-base counter would be 43 (101011) and the binary number stored on the Y lines of the storage register would be 50 (110010).

f. Reading from right to left in each of these binary numbers, the 0's and 1's would correspond to the 0's and 1's present on the X1 through X6, $\bar{Y}1$ through $\bar{Y}6$, through $\bar{X}6$, and Y1 through Y6 lines, respectively. The X1 and Y1 inputs to AND gate GAD-13 would be 0 and 0, respectively, and the 0 output would be applied to the upper input of inverting AND gate GAI-19. The X2 and Y2 inputs to OR gate GOB-1 would be 0 and 1, respectively, and the 0 output would be applied to the lower input of inverting AND gate GAI-19.

g. The two 0 inputs produce a 1 in inverting AND gate GAI-19 output, which is then applied to the upper input of inverting AND gate GAI-20. The $\bar{X}2$ and $\bar{Y}2$ inputs to OR gate GOB-2 would be a 1 and 0, respectively, producing a 0 which would be applied to the other input of inverting AND gate GAI-20. With a 0 and a 1 present at the inputs of inverting AND gate GAI-20, a 0 would be produced and applied to the lower input of inverting AND gate GAI-21. The X3 and Y3 inputs of OR gate GOB-3 would be a 1 and 0, respectively, and the 0 output produced would be applied to inverting AND gate GAI-21.

h. With two 0 inputs, inverting AND gate GAI-21 would produce a 1 which would be applied to the upper input line of inverting AND gate GAI-22. The $\bar{X}3$ and $\bar{Y}3$ inputs of

OR gate GOB-4 would be 0 and 1, respectively, and the 0 output produced would be applied to inverting AND gate GAI-22. With a 1 and a 0 present at the inputs of inverting AND gate GAI-22, a 0 would be produced and applied to the lower input of inverting AND gate GAI-23. The X4 and Y4 inputs of OR gate GOB-5 would each be 0 and the resulting 0 output would be applied to the other input of inverting AND gate GAI-23.

i. With two 0 inputs, inverting AND gate GAI-23 would produce and apply to a 1 to the upper input of GAI-24. The $\overline{X4}$ and $\overline{Y4}$ inputs of OR gate GOB-6 would each be 1 and would apply the 1 produced in the output to the other input of inverting AND gate GAI-24. With two 1 inputs, inverting AND gate GAI-24 would apply a 0 to the lower input of inverting AND gate GAI-25. The X5 and Y5 inputs to OR gate GOB-7 would each be 1; therefore, a 1 would be applied to the other input of inverting AND gate GAI-25. With a 0 and a 1 present on the inputs of inverting AND gate GAI-25, a 0 would be produced and applied to the upper input of inverting AND gate GAI-26.

j. The $\overline{X5}$ and $\overline{Y5}$ inputs of OR gate GOB-8 would each be 0, and a 0 would be produced and applied to the other input of GAI-26. With two 0 inputs, inverting AND gate GAI-26 would apply a 1 to the lower input of inverting AND gate GAI-27. The X6 and Y6 inputs of OR gate GOB-9 would be 0 and 1, respectively; therefore, a 0 would be produced and applied to the other input of inverting AND gate GAI-27.

k. With a 0 and a 1 present on the inputs of inverting AND gate GAI-27, a 0 would be produced and applied to the upper input of AND gate GAI-28. The $\overline{X6}$ and $\overline{Y6}$ inputs of OR gate GOB-10 would be 1 and 0, respectively, and a 0 output produced would be applied to the other input of inverting AND gate GAI-28. With two 0 inputs, inverting AND gate GAI-28 would produce and apply a 1 to inverting AND gate GAI-18. Inverting AND gate GAI-18 would therefore apply a 0 to transition-control AND gate GAI-15. The output of transition-control AND gate GAI-15, which is inverted by inverter IN-11, triggers

AND gates GAS-3 through GAS-14 to provide a new read-in from the digital time-base counter to the storage register.

l. When the binary number stored in the \overline{Y} lines of the storage register is larger than the binary number present at the X lines of the digital time-base counter, the magnitude comparator circuits apply a 1 from the output of inverting AND gate GAI-18 to transition-control gate GAI-15. In this condition, transition-control gate GAI-15 cannot enable AND gates GAS-3 through GAS-14. Therefore, no read-in from the digital time-base counter to the storage register is possible.

m. Assume that the output on the X lines of the digital time-base counter is the binary 13 (001101) and the binary number stored on the \overline{Y} lines of the storage register is 20 (010100); then the binary number present on the \overline{X} lines of the digital time-base counter would be 50 (110010) and the binary number stored on the Y lines of the storage register would be 43 (101011).

n. When RESET switch 1A1S5 is momentarily depressed, a 0 is applied to the C input lines of the storage register (bistables FFS-1 through FFS-6). This resets the storage register to binary 000000, and PERCENT DISTORTION meter 1A1M1 will indicate zero. When RESET switch 1A1S5 is released, the number in the digital time-base counter will be read into the storage register, since the binary number stored at the \overline{Y} lines of the storage register is smaller than the binary number present at the X lines of the digital time-base circuits (c above).

1-20. Digital-to-Analog Converter Circuits (fig. 6-3)

a. The meter-drive circuits in the digital-to-analog converter circuits contain constant-current generators CCG-1 through CCG-6. These constant-current generators convert the digital number (states of FFS-1 through FFS-6) stored in the storage-register bistables to an analog form (current level signals). Current summing network CSN-1 adds up the current levels and then attenuates the sum by a factor of 1/32 before applying the result to PER-

CENT DISTORTION meter 1A1M1. PERCENT DISTORTION meter 1A1M1 requires 1 milliamperes to provide a full-scale deflection (50-PERCENT DISTORTION indication).

b. The binary number stored in the storage-register bistables (FFS-1 through FFS-6) on the Y1 through Y6 lines is applied direct to constant-current generators CCG-1 through CCG6, respectively. A 1 stored on the Y line in a particular storage register turns on the associated constant-current generator, and a 0 stored on the Y line turns it off. The largest number that can be held in the storage register is 63 (111111), which represents 49.2-percent distortion. When a 1 is present on each Y line of the storage register, a total current of 31.5 milliamperes is applied to current summing network CSN-1. Current summing network CSN-1 then attenuates the current to 0.984 milliamperes ($31.5 \times 1/32$). This causes a deflection of 98.4 percent of full scale, or a reading of 49.2 PERCENT DISTORTION on meter 1A1M1.

1-21. Transition-Sampler Circuits

(fig. 6-3)

a. The transition-sampler circuits are controlled by DISTORTION SELECT switch 1A1S7 and DISTORTION SELECT switch 1A1S6. The transition-sampler circuits determine whether the distortion measurements involve all transitions, the space-to-mark transitions, or the mark-to-space transitions. When DISTORTION SELECT switch 1A1S7 is at TOTAL PEAK, a high-level 0 is applied to the lower inputs of AND gates GAS-1 and GAS-2. The other input to AND gate GAS-1 is obtained from the 1 output line of Schmitt trigger STA-2 (C, fig. 1-10), and the other input to AND gate GAS-2 is obtained from the 0 output line of Schmitt trigger STA-2(D, fig. 1-10). Thus, the 0 output line from STA-2, which is positive-going for a space-to-mark transition (D, fig. 1-10), will enable AND gate GAS-2.

b. The 1 output line from STA-2, which is positive-going for a mark-to-space transition (C, fig. 1-10), will enable AND gate GAS-1. Thus, each AND gate, GAS-1 and GAS-2 (E and F, fig. 1-10), passes a transition, and both types of transitions are applied to bistable

FFA-1 as positive triggers. The positive signal transitions from AND gates GAS-1 and GAS-2 are applied to the S input of synchronizing bistable FFA-1.

c. Bistable FFA-1 and inverting AND gate GAI-3 then synchronize the transitions to be measured with the timing pulses from AND gate GAI-4 in the time-base circuits (para 1-7). The 0 output from bistable FFA-1 (G, fig. 1-10) is applied through AND gate GAT-1 to the input of monostable SSA-1. The output from monostable SSA-1 (J, fig. 1-10) is applied to transition-control gate GAI-15 to provide the proper read-in to the storage register bistables.

d. When a positive transition is applied to the C input of bistable FFA-1, the 1 output line provides a high level to AND gate GAI-3 and the 0 output line provides a low level to AND gate GAT-1. When the next positive timing pulse (timing pulses are 128 times the baud frequency), from AND gate GAI-4 is applied to AND gate GAI-3, GAI-3 is enabled and provides a low level, which has no effect, to FFA-1. When the timing pulse is removed, GAI-3 is inhibited and a high level is applied to the S input of bistable FFA-1. The 1 output line provides a low level to AND gate GAI-3 and the 0 output line provides a high level to AND gate GAT-1. AND gate GAT-1 is thus enabled and applies a low level to monostable SSA-1.

e. When the next positive transition is applied to the C input of bistable FFA-1, the 1 output line again provides a high level to AND gate GAI-3, and the 0 output line provides a low level to AND gate GAI-1. The next timing pulse will again set bistable FFA-1. Thus, when left-hand DISTORTION SELECT switch 1A1S7 is set to TOTAL PEAK, each transition of the input signal (A, fig. 1-10) is applied to monostable SSA-1 from AND gate GAT-1 (J, fig. 1-10),

f. When DISTORTION SELECT switch 1A1S7 is in any position other than TOTAL PEAK, DISTORTION SELECT switch 1A1S6A determines whether a mark/space or space/mark transition is applied to transition-control gate GAI-15. When DISTORTION SELECT switch 1A1S6A is set to MARK/SPACE, AND gate GAS-1 is enabled (E, fig.

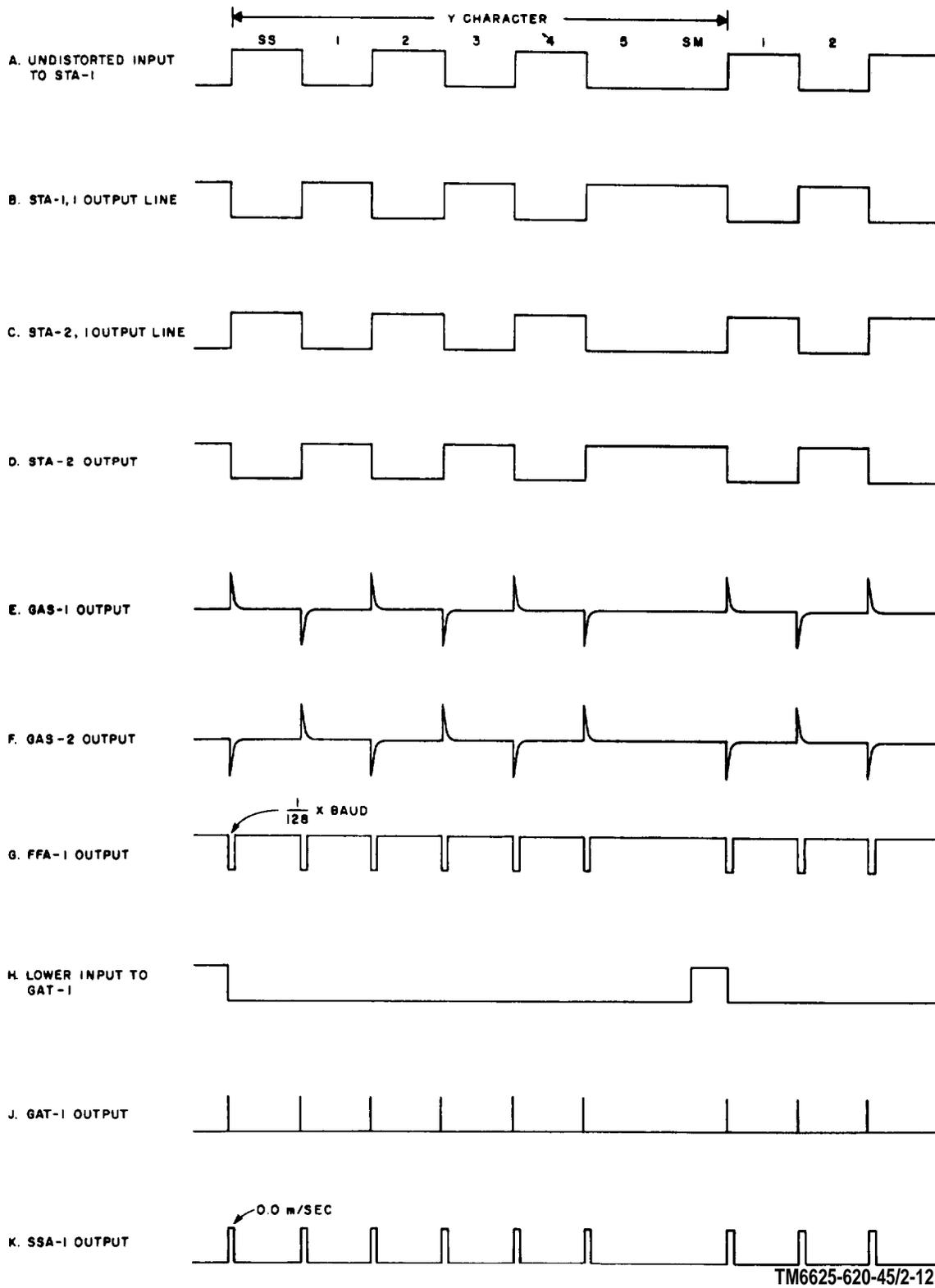


Figure 1-10. Transition sampler circuits, timing diagram.

1-10) and AND gate GAS-2 is inhibited. Thus, the output from monostable SSA-1 will occur only during the mark-to-space transitions. When right-hand DISTORTION SELECT switch 1A1S6 is set to SPACE/MARK, AND gate GAS-1 is inhibited and AND gate GAS-2 is enabled (F, fig. 1-10). Thus, the output from monostable SSA-1 will occur during the space-to-mark transition.

1-22. Transition-Control Circuits (fig. 6-3)

a. When DISTORTION SELECT switch 1A1S7A is set to AVERAGE, a low-level inhibit signal is applied to comparison AND gate GAI-18. Thus, AND gate GAI-18 applies a constant high-level enable signal to transition-control gate GAI-15 during average distortion measurements. When DISTORTION SELECT switch 1A1S7A is set to any other position, a high-level signal is applied through the switch to one input line of AND gate GAI-18.

b. The other input to comparison AND gate GAI-18 is obtained from AND gate GAI-28 in the magnitude comparator circuits (para 1-19). When the binary number held in the storage register is greater than the binary number present at the output of the digital time-base counter, AND gate GAI-28 provides a high-level output to AND gate GAI-18, which then applies a low-level enable signal to transition-control gate GAI-15. When the binary number held in the storage register is less than the binary number present at the output of the digital time-base counter, AND gate GAI-28 provides a low-level output to AND gate GAI-18, which then applies a high-level inhibit signal to transition-control gate GAI-15.

c. When DISTORTION SELECT switch 1A1S7B is set to AVERAGE or TOTAL PEAK, a low-level signal is applied to early transition AND gate GAI-14 and to late transition AND gate GAI-13 (no switch connection provides -15 volts to the open lead). Early transition AND gate GAI-14 and late transition AND gate GAI-13 require high-level inputs at the input lines in order to apply a low-level signal to transition-control gate

GAI-15. Therefore, early transition AND gate GAI-14 and late transition AND gate GAI-13 apply a constant high-level signal to transition-control gate GAI-15 during average and total peak distortion measurements.

d. When DISTORTION SELECT switch 1A1S7A is set to EARLY PEAK, a high-level signal is applied to one input line of early transition AND gate GAI-14, and a low-level signal is applied to one input of late transition AND gate GAI-13. The other input to early transition AND gate GAI-14 is from the 1 output line of bistable FFC-14 in the digital time-base circuits (para 1-17). When a high-level signal is present at the 1 output line of bistable FFC-14 in the digital time-base circuits (the digital time-base counter is counting from zero to 63), AND gate GAI-14 applies a low-level signal to transition-control gate GAI-15.

e. When a low-level signal is applied to the input of early transition AND gate GAI-14 from the digital time-base counter (digital time-base counter is counting from 63 to zero), AND gate GAI-14 applies a high-level signal to transition-control gate GAI-15. Thus, a high-level signal is present at the output of late transition AND gate GAI-13 at all times during early peak-distortion measurements, and a high-level signal is present at the output of early transition AND gate GAI-14 for only the 1/2 bit preceding each ideal transition time (early transitions), except during the stop-mark/start-space transition. When DISTORTION SELECT switch 1A1S7 is set to LATE peak, a high-level signal is applied to one input line of late transition AND gate GAI-13, and a low-level signal is applied to one input line of early transition AND gate GAI-14.

j. The other input to late transition AND gate GAI-13 is from the 0 output line of bistable FFC-14 in the digital time-base circuits. When a high-level signal is present at the 0 output line of bistable FFC-14 (the digital time-base counter is counting from 64 to 127), AND gate GAI-13 applies to a low-level signal to transition-control gate GAI-15.

g. When a low-level signal is present on the 0 output line of bistable FFC-14 (the digital time-base counter is counting from zero

to 63), AND gate GAI-13 applies a high-level signal to transition-control gate GAI-15. Thus, a high-level signal is present at the output of early transition AND gate GAI-14 at all times during late peak-distortion measurements, and a high-level signal is present at the output of late transition AND GATE GAI-13 for only the 1/2 bit following each ideal transition time (late transitions),

h. Transition-control gate GAI-15 controls the read-in gates to insure that the storage register will provide the proper output, through the meter drive circuits, to PERCENT DISTORTION meter 1A1M1, for the type of distortion measurement being made. The output transition-control AND gate GAI-15 is applied through inverter IN-11 to read-in gates GAS-3 through GAS-14 (para 1-18) and to early selection AND gate GAD-3 and late selection AND gate GAD-4 in the early-late circuits (para 1-23).

i. When a high-level signal is applied to the read-in gates, the gates are enabled, and when a low-level signal is applied to the read-in gates, the gates are inhibited. To enable the read-in gates, all high-level inputs must be present at transition-control gate GAI-15.

j. Because transition-control gate GAI-15 is controlled by the outputs of six other circuits, the read-in gates will be enabled only when the proper timing waveforms are present on the input lines of transition-control gate GAI-15. The relationship between the various input and output waveforms at transition-control gate GAI-15, when various distortion measurements are made with the distortion analyzer, is discussed in (1) through (4) below.

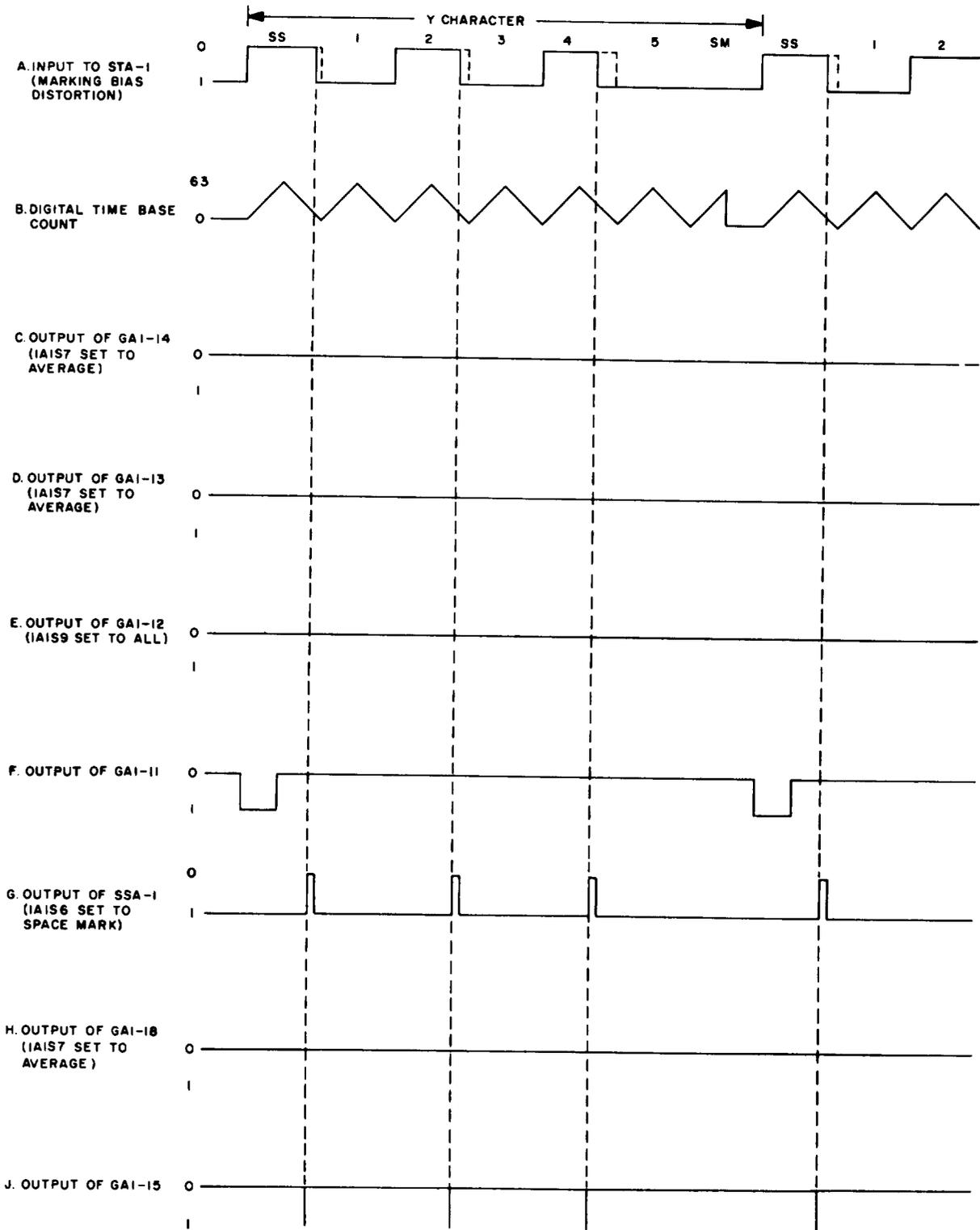
k. The six inputs to transition-control gate GAI-15 are as follows: Two inputs are from AND gates GAI-14 and GAI-13 (c above); two inputs are from AND gates GAI-11 AND GAI-12 in the baud distributor circuits (para 1-24); one., input is from monostable SSA-1 in the transition-sampler circuits (para 1-21); and the last input is from AND gate GAI-18 (a above).

(1) *Average distortion measurements.* Waveforms C through H in figure 1-11 at the input to transition-control gate GAI-15 are representative of

the waveforms present during the analysis of a character, with DISTORTION SELECT switch 1A1S7 set to AVERAGE and DISTORTION SELECT switch 1A1S6 set to SPACE/MARK. Waveform J, figure 1-11 represents the waveform present at the output of GAI-15. Other waveforms shown are A, which represents a distorted Y-character signal present at the input of STA-1, and waveform B, which shows the time relationships of the count in the digital time-base counter with respect to the other waveforms.

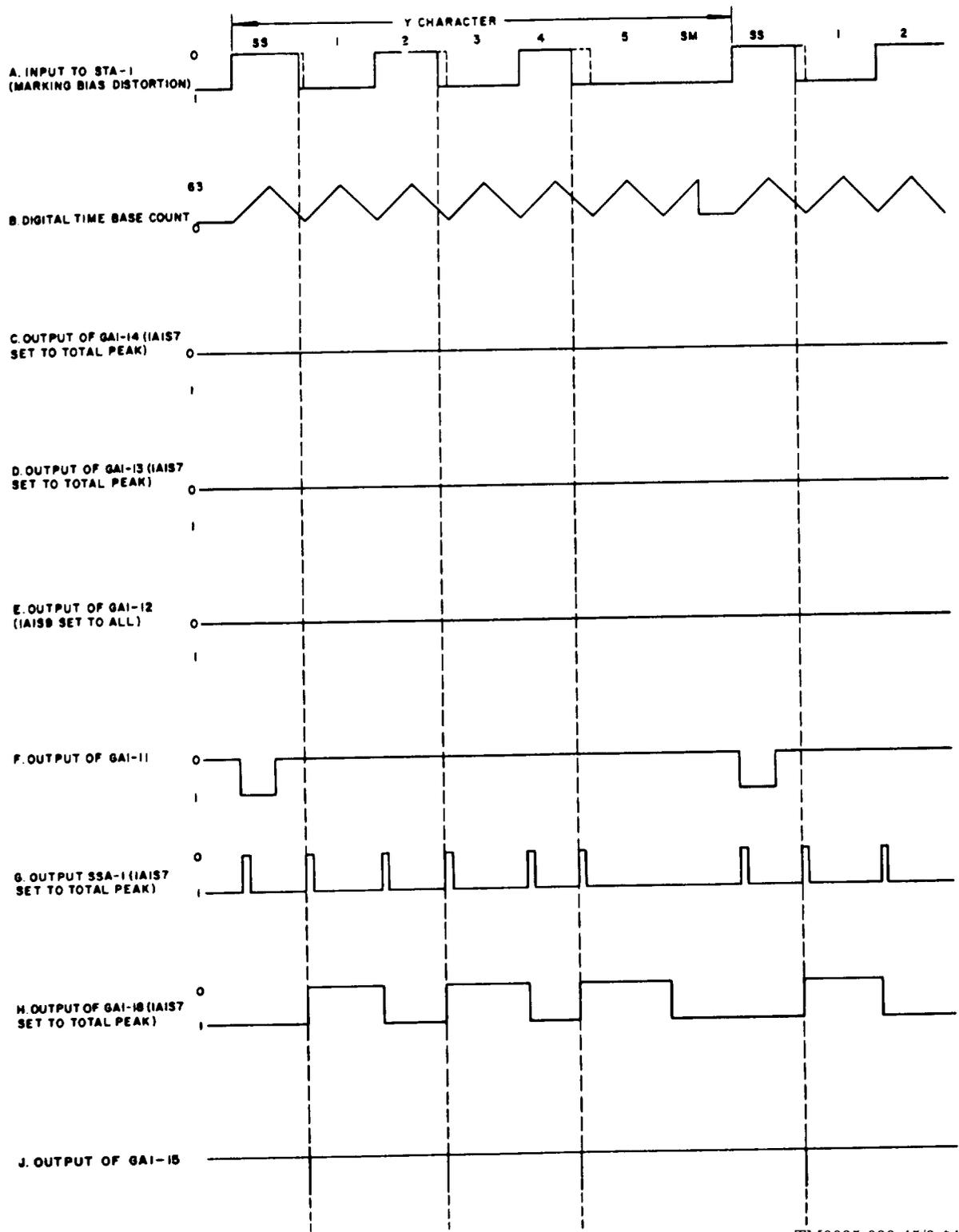
- (a) The zero points on waveform B correspond to the time when transitions would occur in an ideal character waveform. Waveforms C and D, figure 1-11 indicate that a 0 is present at all times at the early transition AND gate GAI-14 and at late transition AND gate GAI-13. When TRANSITION SELECT switch 1A1S9 is set to ALL, a high-level signal is present at all times at the transition gate GAI-12 output (waveform E).
- (b) A high-level input is also present from the count seven AND gate GAI-11 in the baud distribution circuits (para 1-23), except during the first 1/2-bit period of the character (waveform F), thus inhibiting transition-control gate GAI-15 (fig. 5-4) during the stop-mark/start-space transition. Because a high-level signal is present at all times from comparison AND gate GAI-18 (waveform H, fig. 1-11), and because a high-level input from the monostable SSA-1 in the transition-sampler circuits (para 1-8) is present only during the space/mark transition (waveform G) of the character, transition-control gate GAI-15 is enabled only during the space/mark transitions of the character (waveform J).

- (c) When DISTORTION SELECT switch 1A1S7 is set to AVERAGE and DISTORTION SELECT switch 1A1S6 is set to MARK/SPACE, the waveforms shown in A through F and H of fig. 1-11 would be the same. The output of monostable SSA-1 (waveform G) would enable transition-control gate GAI-15 only during the mark/space transitions (except for the stop-mark/start-space transition).
- (2) *Total peak-distortion measurements.* The waveforms shown in figure 1-12 are typical of those present during the analysis of a Y-character when left-hand DISTORTION SELECT switch 1A1S7 is set to TOTAL PEAK. Waveforms A through F of figure 1-12 are the same as those in figure 1-11 and have been described in (1) above.
- (a) A high-level input from monostable SSA-1 in the transition-sampler circuits is present at the input of GAI-15 for each mark/space and space/mark transition (waveform G, fig. 1-11). The output from the comparison AND gate GAI-18 will be a high level only when the count in the storage register is smaller than the count in the digital time-base counter.
- (b) The duration of the high-level output from comparison AND gate GAI-18 (waveform H) therefore, depends on the amount of distortion present in the input signal (waveform A). Thus, transition-control gate GAI-15 will be enabled only when the high-level inputs of monostable SSA-1 (waveform G) and comparison AND gate GAI-18 are in coincidence (waveform J).
- (3) *Early peak-distortion measurement.* The waveforms shown in figure 1-13 are typical of those presented during the analysis of a Y-character when DISTORTION SELECT switch 1A1S7 is set to EARLY PEAK and DISTORTION SELECT switch 1A1S6 is set to MARK/SPACE.
- (a) Waveforms B and D through F are the same as those in figure 1-11 and have been described in (1) above. A high-level input from early transition AND gate GAI-14 (waveform C, fig. 1-13) will be present only at the input of GAI-15 during the 1/2-bit period preceding each ideal transition. The output from comparison AND gate GAI-18 (waveform H) will be a high level only when the count in the storage register is smaller than the count in the digital time-base counter.
- (b) The duration of the high-level output from comparison AND gate GAI-18 (waveform H), therefore, depends on the amount of distortion present in the input signal (waveform A). Because a high-level signal is present from monostable SSA-1 (waveform G) for each mark/space transition, transition-control gate GAI-15 will be enabled (waveform I) only when the high-level inputs from early transition AND gate GAI-14 (waveform C), comparison AND gate GAI-18 (waveform H), and monostable SSA-1 (waveform G) are in coincidence.
- (4) *Late peak-distortion measurements.* The waveforms shown in figure 1-14 are typical of those present during the analysis of a Y-character when DISTORTION SELECT switch 1A1S7 is set to LATE PEAK and DISTORTION SELECT switch 1A1S6 is set to SPACE/MARK.
- (a) Waveforms B, C, E, and F are the same as those in figure 1-11 and have been described in (1) above. A high-level input from late transition AND gate GAI-13 (waveform D) will be present at the input of GAI-15 only during the 1/2-bit period following each ideal transition. The output from comparison



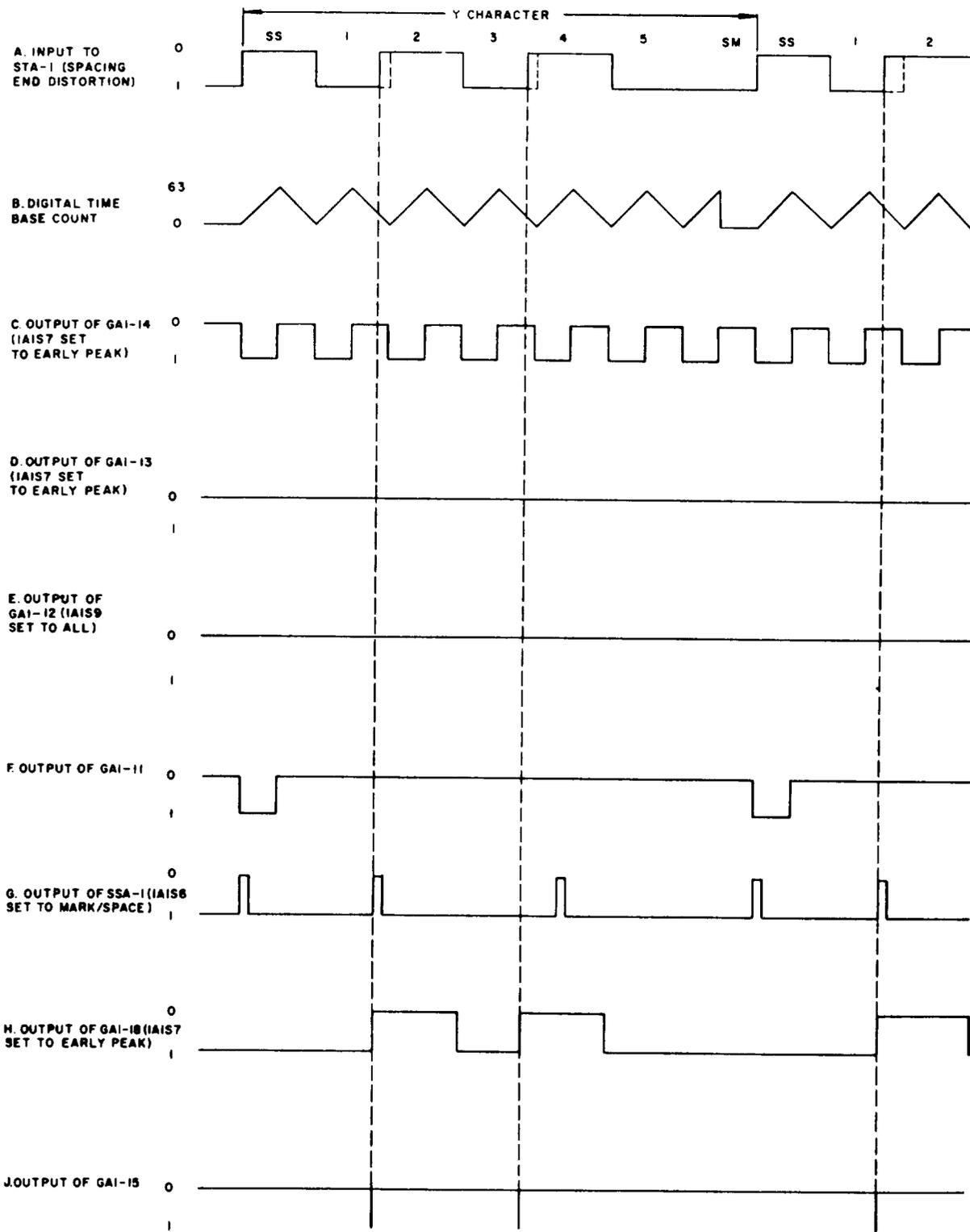
TM6625-620-45/2-13

Figure 1-11. Average distortion, timing diagram.



TM6625-620-45/2-14

Figure 1-13. Early peak distortion, timing diagram.



TM6625-620-45/2-15

Figure 1-13. Early peak distortion timing diagram.

AND gate GAI-18 (waveform H) will be at a high level only when the count in the storage register is smaller than the count in the digital time-base counter.

- (b) The duration of the high-level output from comparison AND gate GAI-18 (waveform H), therefore, depends on the amount of distortion present in the input signal (waveform A). Because high-level signal is present from monostable SSA-1 (waveform G) for each space/mark transition, transition-control gate GAI-15 will be enabled (waveform I) only when the high-level inputs from late transition AND gate GAI-13, (waveform D) comparison AND gate GAI-18 (waveform H), and monostable SSA-1 (waveform G) are in coincidence.

1-23. Early-late Circuits

a. The early-late circuits are controlled by DISTORTION SELECT switch 1A1S7 (fig. 6-3) and transition-control gate GAI-15 in the distortion select circuits (para 1-9). When DISTORTION SELECT switch 1A1S7 is set to AVERAGE, a high-level signal is applied to one input of AND gates GAI-16 and GAI-17. The state of bistable FFA-2 determines whether EARLY indicator lamp 1A1DS3 or LATE indicator lamp 1A1DS2 will light. When DISTORTION SELECT switch 1A1S7 is set to any position other than AVERAGE, a low-level signal is applied to one input of AND gates GAI-16 and GAI-17, and neither indicator lamp will light.

b. When the digital time-base counter is counting from zero to 63, AND gate GAD-14 receives a high-level signal on one input from bistable FFC-14 in the digital time-base circuits, and another high-level signal at the other input through inverter IN-11 from transition-control gate GAI-15. The output from GAD-14, which is set at a high level during the 1/2 bit following each ideal transition, triggers bistable FFA-2 to provide a low level signal on the 0 input line and a high-level signal on the 1 output line.

c. With a high-level signal at each input line of AND gate GAI-16, a low-level signal is applied to LATE indicator lamp 1A1DS2. Thus, LATE indicator lamp 1A1DS2 lights during the 1/2-bit period succeeding each ideal transition of the telegraph signal, except for the stop-mark/start-space transition, during which time transition-control gate GAI-15 is inhibited by AND gate GAI-11 in the baud distributor circuits (para 1-24).

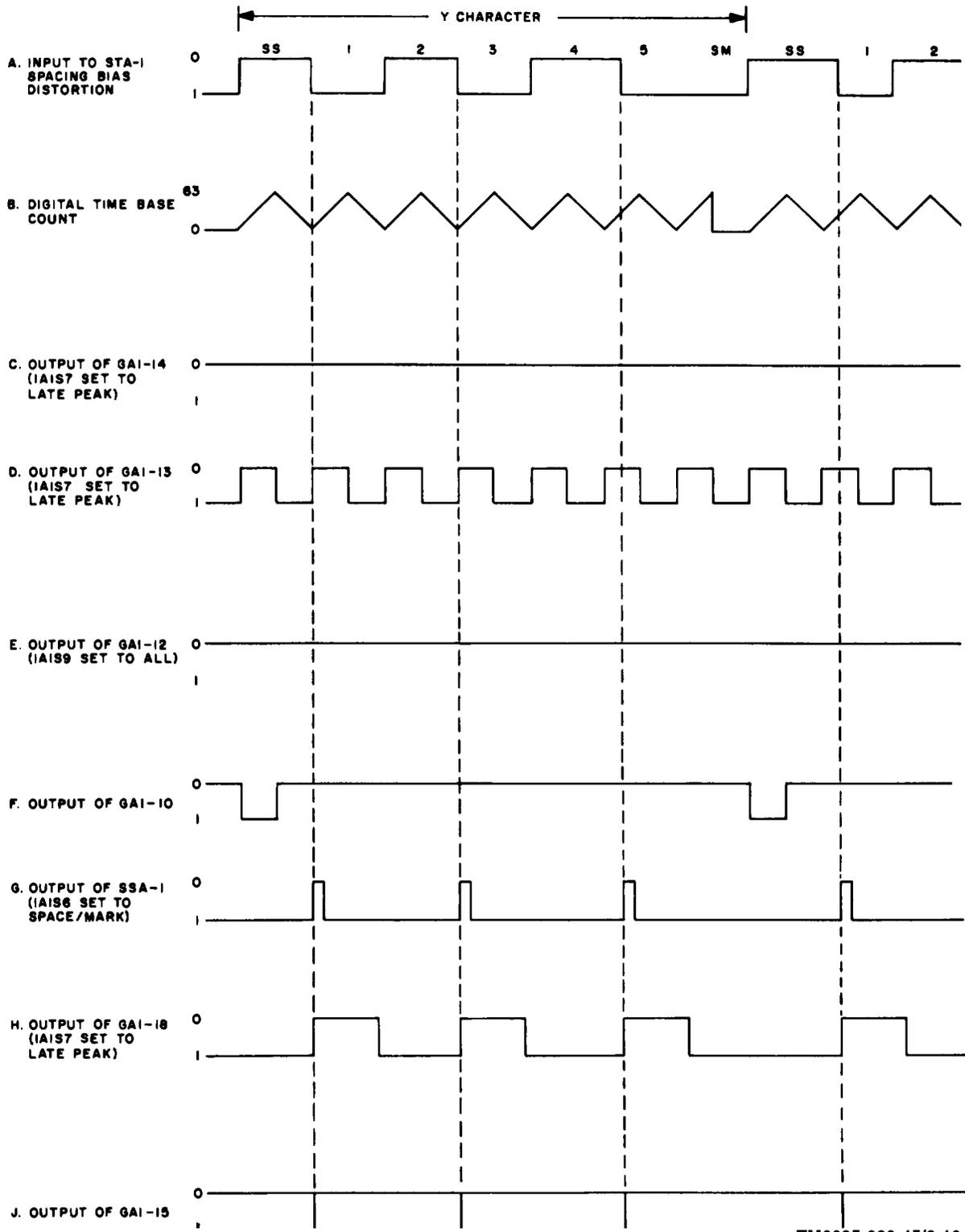
d. When the digital time-base counter is counting from 64 to 127, AND gate GAD-13 receives a high-level signal on one input from bistable FFC-14 in the digital base circuits, and a high-level signal on the other input through inverter IN-11 from transition-control gate GAI-15. When both inputs to AND gate GAD-13 are high levels, the output from GAD-13, which is at a level during the 1/2 bit following each ideal transition, triggers bistable FFA-2 provide a low level on the 0 output line.

e. With a high-level signal at each input line of AND gate GAI-17, a low-level signal is applied to EARLY indicator lamp 1A1S3. Thus, EARLY indicator lamp 1A1DS3 lights during the 1/2 bit preceding each ideal transition of the telegraph signal except the stop-mark/start-space transition.

1-24. Baud Distributor Circuits

a. The baud distributor circuits insure that the digital time-base counter in the digital time-base circuits (para 1-17) is set 1/2 bit into the stop/mark bit and that the count in the digital time-base counter is synchronized with the stop-mark/start-space transition of each character. The baud distributor circuits also determine whether all of the transitions or a specific transition of the input signal will be selected for analysis.

b. The waveforms shown in figure 1-15 are typical of those present during the analysis of Y-character with TRANSITION SELECT switch 1A1S9 set to 1. The waveform shown in A represents an undistorted Y-character input signal present at the 0 output of STA-2. The waveform shown in B shows the time relationships of the count in the digital time-base counter with respect to the other waveforms. The 0 points on waveform B correspond to the time



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Figure 1-14. Late peak distortion timing diagram.

when a transition should occur in an ideal character waveform. The 0 output line of bistable FFC-14 (fig. 6-3) in the digital time-base counter is used to advance baud counter bistables FFC-5 through FFC-7.

c. When the count in the digital time-base counter changes from 63 (1111110) to 64 (0000001), the transition from 1 to 0 on the 0 output line of bistable FFC-14 (waveform C fig. 1-15) triggers bistable FFC-5 in the baud counter (bistables FFC-5, FFC-6, and FFC-7). Thus, every 128 pulses, the baud counter is advanced one count (waveforms D, E and F). The baud counter counts from zero to seven for each character and the outputs are applied to AND gates GAI-2, and GAI-5 through GAI-11 (count zero through count six gates).

d. The count stored in the baud counter during each bit is shown in waveform G. Thus, depending upon the position of TRANSITION SELECT switch 1A1S9, the count-one through count-five gates (GAI-5 through GAI-10) are enabled consecutively 1/2 bit before the ideal transition time, and remain enabled until 1/2 bit after the ideal transition time, for each transition after the occurrence of the stop-mark/start-space transition of each character. Count-six gate GAI-2 is enabled 1/2 bit into the stop/mark (waveform H). The low-level output of GAI-2 then inhibits the timing pulse (waveform B) through AND gate GAI-4.

e. The low-level output from GAI-2 is also applied through inverter IN-3 as a high level to enable AND gate GAI-1 for the length of the stop/mark bit. The negative-going stop-mark/start-space transition (waveform A) inhibits AND gate GAI-1. The 1 to 0 transition at the output of GAI-1 is applied to the C input of bistable FFC-5 in the baud counter, resetting the baud counter. At this time, the count-six gate is inhibited and the 1 to 0 transition at the output of GAI-2 starts the timing (waveform H). Thus, the time in the digital time-base counter is synchronized with the stop-mark/start-space transition and a positive

transition is provided through inverting amplifiers IN-3 and IN-4.

j. The transition time is applied to CHARACTER SYNC jack 1A1S2, where it is used to synchronize the external equipment to the stop-mark/start-space transition of each character. Count-seven gate GAI-11 is also enabled. The low-level output from GAI-11 (waveform K) inhibits transition-control gate GAI-15 for 1/2 bit following the stop-mark/start-space transition.

g. The count-zero through count-five gates (GAI-5 through GAI-10) provide the required low-level inputs to transition gate GAI-12 in order to insure a proper analysis of the desired transition (fig. 6-3). When a low-level signal is applied to any of the input lines of transition gate GAI-12, the required high-level input is applied to transition-control gate GAI-15 in the distortion select circuits (para 1-15).

h. When TRANSITION SELECT switch 1A1S9 is set to 1, a high-level signal is applied to one input of GAI-5; thus, the count-two through count-five gates (GAI-6 through GAI-10) are inhibited by the open-switch position. The count-zero gate will be enabled when the count in the baud counter (FFC-5 through FFC-7) is a 0 (\overline{ABC}) and will apply a low-level signal (waveform L, fig. 1-15) to transmission gate GAI-12 for 1/2 bit before and after the ideal transition time of the first bit. Transition gate GAI-12 (fig. 6-3) will apply a high-level signal to one input of GAI-15 for the same period of time as above.

i. When TRANSITION SELECT switch 1A1S9 is set to 2, count-one gate GAI-6 will be enabled, and transition gate GAI-12 will enable transition-control gate GAI-15 during the 1/2 bit before and the 1/2 bit after the ideal transition time of the second bit of a character, in the same manner as that described above. When TRANSITION SELECT switch 1A1S9 is set at ALL, a low-level signal is applied to transition gate GAI-12, which then applies a constant high-level signal to transition-control gate GAI-15.

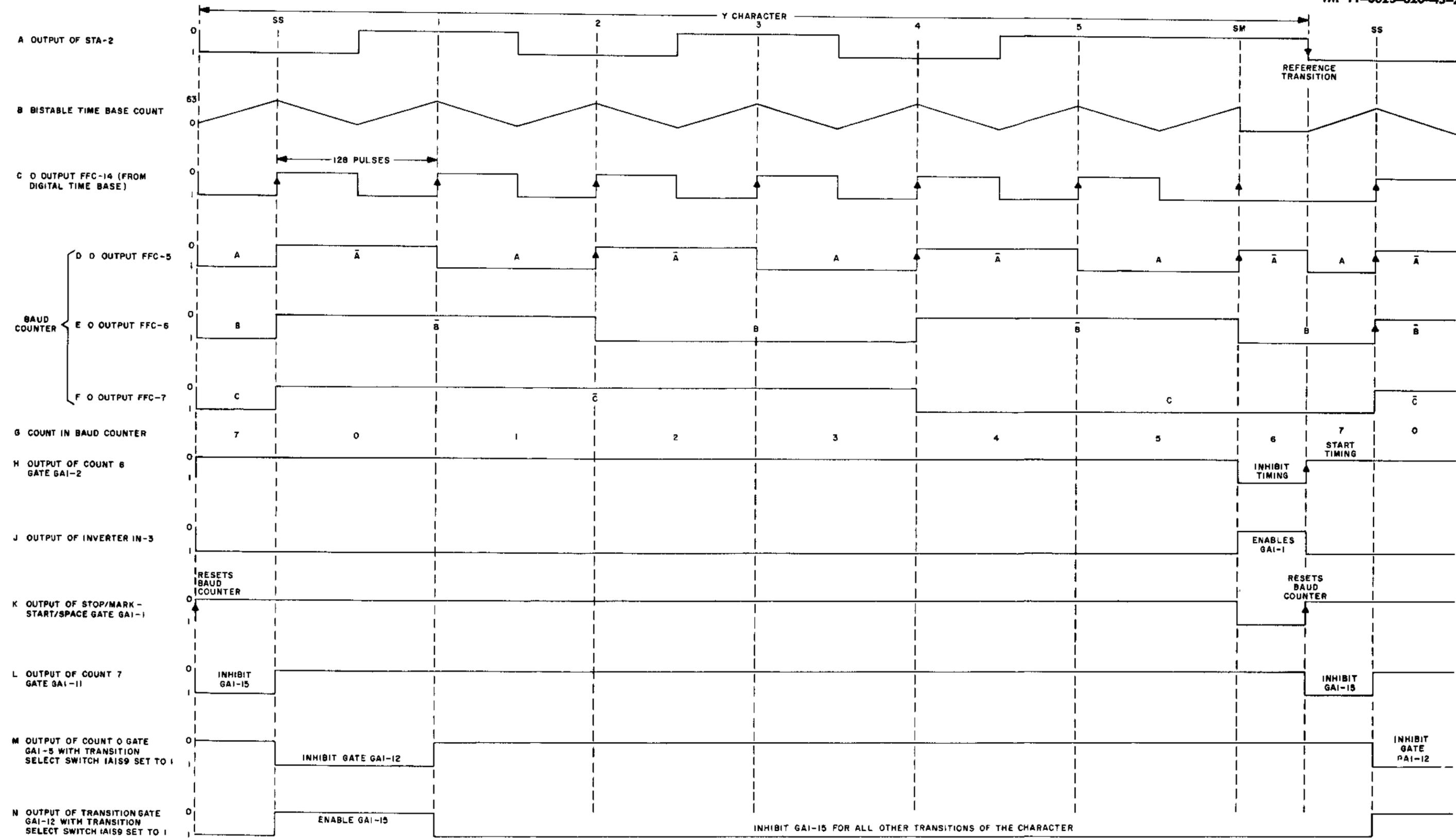


Figure 1-15. Baud distributor circuits, timing diagram.

CHAPTER 2

TROUBLESHOOTING

Section I. GENERAL TROUBLESHOOTING INFORMATION

Warning: When troubleshooting or making repairs in this equipment, be extremely careful. Voltages as high as 230 are present internally. Use insulated test probes when making the required voltage measurements. Always disconnect the power cord from the equipment before touching any of the internal parts.

2-1. General Instructions

a. Troubleshooting at general support and depot maintenance levels includes all techniques outlined for organizational maintenance and any special or additional techniques required to isolate a defective part. The general support and depot maintenance procedures are not complete in themselves but supplement the procedures described in the organizational maintenance manual (TM 11-6625-620-12). The systematic troubleshooting procedure, which begins with the operational and sectionalization checks performed at an organizational level, must be completed by further localizing and isolating techniques.

b. Troubleshooting may be performed while the equipment is operating as part of a system or, if necessary, after the equipment (or parts of it) has been removed from service. When trouble occurs, certain observations and measurements can be made which will help in determining whether the trouble is in the local equipment or exists elsewhere in the system. Usually, when troubleshooting is performed while the equipment is operating as part of a system, it is done at the organizational level (TM 11-6625-620-12). Troubleshooting at the general support level is usually done with the component removed from the equipment with which it is normally associated. Paragraphs 2-2 through 2-9 describe the systematic procedures to be followed which will enable the repairman to isolate the cause of the trouble and correct the fault.

2-2. Organization of Troubleshooting Procedures

The first step in servicing a defective equipment is to sectionalize the fault. Sectionalization means tracing the fault to the major equipment component. Refer to TM 11-6625-620-12 for sectionalization procedures. The second step is to localize the fault. Localization means tracing the fault to the defective stage. The third step, isolation, means tracing the fault to the defective part. Some faults, such as burned-out resistors, arcing, or shorted transformers, can often be isolated by sight, smell, or hearing. The majority of faults, however, must be isolated by checking voltages, resistance, and signal levels.

a. *Localization.* Follow the troubleshooting procedure described in paragraph 2-4, using the equipment specified below. If correct results are not obtained, refer to the troubleshooting chart in paragraph 2-5 to localize the trouble to a specific circuit, and to paragraph 2-6 to localize the trouble to a specific stage.

b. *Isolation.* When the trouble has been localized to a stage, isolate the trouble to the defective part by using the procedures described in paragraph 2-8.

2-3. Test Equipment Required

The following chart lists the test equipment required for troubleshooting Test Set, Teletypewriter TS-800/UGM-1. The associated technical manuals and the assigned common names are also listed.

Test equipment, tools, and materials	Technical manual	Common name
Multimeter TS-M2B/U- - - - -	TM 11-6625-366-15	Multimeter.
Oscilloscope OS-8/U- - - - -	TM 11-1214	Oscilloscope.
Test Set, Teletypewriter TS-799/UGM-1.	TM 11-6625-620-12	Pattern generator.
Test Set, Transistor TS-1836/U.	TM 11-6625-539-15	Transistor tester.
Tool Kit, Electronic Equipment TK-105/G.	-----	Toolkit,
Frequency Meter AN/USM-26.	TM 11-5057	Frequency meter.

Cautions: Use extreme care when performing procedures in a through l below.

- a. This equipment contains transistor circuits; therefore, be very careful when using test equipment.
- b. Never connect test equipment (other than multimeters) directly to a transistor circuit; use a coupling capacitor.
- c. Make test equipment connections with care so that short circuits will not be caused by exposed test equipment connectors. Use tape or sleeving (spaghetti) on test prods or clips as necessary to leave as little exposed metal as needed to make contact to the circuit under test.
- d. The equipment internal power supply is servicing this transistorized equipment. However when external power sources are used, observe polarity. Polarity reversal may damage the transistors or electrolytic capacitors in the circuit. If an external source is used in place of the internal source, it must have good voltage regulation and low ac ripple. Good regulation is important because the output voltage of an external power supply that has poor regulation may exceed the maximum voltage rating of the transistors in the equipment being tested.

- e. When the unit chassis is exposed, high-voltage terminals are also exposed.
- f. Replace parts carefully; the careless replacement of parts can create new problems.
- g. Before a part is unsoldered, note the positions of its leads. If a part such as a transformer has a number of connections, tag each lead.
- h. Be careful not to damage other leads when pulling or pushing them out of the way.
- i. Do not allow drops of solder to fall into the equipment; they may cause short circuits.
- j. A carelessly soldered connection may create a new fault. It is important to make well-soldered joints; a poorly soldered joint is one of the most difficult faults to find.
- k. When repairs are to be made on a printed circuit card, use a small iron such as a 35-watt iron. Access to the component or printed circuit may be obtained by gently melting away the epoxy coating. However, to avoid destroying the bond between the printed circuit conductor and the printed card, heat the printed circuit foil as little as possible.
- l. Semiconductor devices may be damaged by excessive heat on their leads. Therefore, when replacing a transition or crystal diode, use heat-conducting clips between the point of soldering and the component. Long-nose pliers may be used as a heat sink.

Section II. TROUBLESHOOTING PROCEDURES

2-4. Test Setup

- a. General. To test the distortion analyzer, make connections to the pattern generator, a loop power supply (60 volts, 60 milliamperes (ma)), and a multimeter, and the distortion

analyzer. Power connections are given in b below, control settings in c below, loop and signal connections in d below, and loop current adjustments in e below.

- b. *Power Connections.* Connect the equipment to primary power as follows:

- (1) If the distortion analyzer and pattern generator are placed on a bench, connect the ac power cables to their respective AC POWER input connectors.
- (2) If the units are to be rack-mounted, connect the ac power cable to AC POWER connector jack J2 on the pattern generator and to AC POWER connector jack J4 on the distortion analyzer.
- (3) Connect the other end of the power cable to the voltage indicated by the POWER switch locking guard.

Caution: Make certain that the power cable is never connected to a 230-volt ac source with the POWER switch locking guard permitting the POWER toggle switch to be set to the 115-volt position. Setting the POWER switch to the 115-volt position with equipment connected to a 230-volt ac source can damage the unit.

c. *Test Equipment Control setting.* Set the controls on the distortion analyzer, pattern generator, loop power supply, and multimeter as described below.

Equipment	Control	Position	
Pattern generator	MESSAGE SELECT switch	DOT CY	
	RATE control	75 DOT CYCLES	
	DISTORT SELECT switch	SPACE/BIAS	
	% DISTORT control	0	
	MESSAGE TRANSMIT SWITCH.	OFF	
	CURRENT SELECT switch	30 POLAR	
	POWER switch	OFF	
	Distortion analyzer	TRANSITION SELECT switch.	ALL
		R A T E s w i t c h	76 BAUDS
		Left-hand DISTORTION SELECT switch.	AVERAGE
Right-hand DISTORTION SELECT switch.		SPACE/MARK	
FILTER switch		OUT	
POLARITY switch		(minus)	
POWER switch		OFF	
Loop power supply	CURRENT SELECT switch	30 POLAR	
	ON-OFF switch	OFF	
	FUNCTION switch	DC CURRENT	
multimeter.	RANGE switch	5 0 M A	

d. *Connection.*

- (1) Connect the polar loop as shown in A, figure 2-1.
- (2) Connect the TS-800/UGM-1 and the TS-799/UGM-1 as shown in B, figure 2-1.

e. *Loop Current Adjustment.* Before operating the equipment, adjust the output loop current to 30 ma as follows:

- (1) Set the multimeter to measure 100 ma, and set the POWER switch on each equipment to 115V ON or ON 230V.
- (2) Adjust the loop current rheostat until the multimeter indicates the required loop current (30 ma).
- (3) Set the POWER switch to OFF.

2-5. Localizing Troubles

a. *General.* Localizing trouble in the distortion analyzer consists of performing an operational test (b below) and noting any abnormal results.. Refer to the troubleshooting chart (c below) and locate the symptom. The chart lists the probable cause of the trouble and the corrective action to be taken.

b. *Operational Test.* Set up the equipment as described in paragraph 2-4. Perform the following tests:

- (1) Set the pattern generator, distortion analyzer, and the loop power supply power switches to ON.
- (2) Observe the visual indications on the distortion analyzer; the POWER, SIGNAL, and LATE indicator lamps should light and the PERCENT DISTORTION meter should indicate 0.
- (3) Set the pattern generator % DISTORT control to 10, 20, 30, and 40 in that order. The distortion analyzer PERCENT DISTORTION meter should indicate 10, 20, 30, and 40.
- (4) Rotate the pattern generator % DISTORT control from 1 through 49 for each position of the % DISTORT SELECT SWITCH. The distortion analyzer PERCENT DISTORTION meter should indicate 1 through 49 for each setting.
- (5) Set the pattern generator % DISTORT control to 40, and DISTORT SELECT switch to MARK BIAS. The distortion analyzer PERCENT DISTORTION meter should indicate 40 and the EARLY indicator lamp should light.
- (6) Turn the pattern generator and the distortion analyzer RATE switches from 45,5 through 150. for each matched setting of the RATE switches, the distortion analyzer EARLY indicator lamp should light and the PERCENT DISTORTION meter should indicate 40.
- (7) Set the pattern generator DISTORT SELECT switch to SPACE BIAS. The distortion analyzer PERCENT DISTORTION meter should indicate

40 and the LATE indicator lamp should light.

- (8) Set the distortion analyzer left-hand DISTORT SELECT switch to TOTAL PEAK and depress the RESET switch. The PERCENT DISTORTION meter should indicate zero, and then immediately reset to 40, and the EARLY and LATE indicator lamps should go out,
- (9) Set the pattern generator % DISTORT control to 30 and depress the distortion analyzer RESET switch. The distortion analyzer PERCENT DISTORTION meter should indicate 30 and hold.
- (10) Repeat the procedure given in (9) above for the 20, 10, and 0 positions of the pattern generator % DISTORT control. The distortion analyzer PERCENT DISTORTION meter should reset to each new lower distortion level and hold.
- (11) Set the pattern generator % DISTORT control to 40 and set the distortion analyzer left-hand DISTORTION SELECT switch to LATE PEAK. The distortion analyzer PERCENT DISTORTION meter should indicate 40.
- (12) Set the distortion analyzer left-hand DISTORTION SELECT switch to EARLY PEAK and depress the RESET switch, The PERCENT DISTORTION meter should indicate 0.
- (13) Set the pattern generator DISTORT SELECT switch to MARK BIAS, The distortion analyzer PERCENT DISTORTION meter should indicate 40.
- (14) Depress the distortion analyzer RESET switch and set the left-hand DISTORTION SELECT switch to EARLY PEAK and then to TOTAL PEAK. The PERCENT DISTORTION meter should indicate 40 for each position.
- (15) Set the pattern generator DISTORT SELECT switch to SPACE BIAS and depress the distortion analyzer RESET switch, The distortion analyzer PERCENT DISTORTION meter should indicate 40.

- (16) Depress the distortion analyzer RESET switch and set the left-hand DISTORTION SELECT switch to LATE PEAK and then to EARLY PEAK. The PERCENT DISTORTION meter should indicate 0 and 40, respectively.
- (17) Set the pattern generator DISTORT SELECT switch to MARK END. The distortion analyzer PERCENT DISTORTION meter should indicate 40.
- (18) Set the distortion analyzer right-hand DISTORTION SELECT switch to MARK/SPACE and depress the RESET switch. The PERCENT DISTORTION meter should indicate 40.
- (19) Depress the distortion analyzer RESET switch and set the left-hand DISTORTION SELECT switch to LATE PEAK and then to EARLY PEAK.
- (20) Set the pattern generator DISTORT SELECT switch to SPACE END. The distortion analyzer PERCENT DISTORTION meter should indicate 40.
- (21) Depress the distortion analyzer RESET switch and set the left-hand DISTORTION SELECT switch to EARLY PEAK and then to LATE PEAK. The PERCENT DISTORTION meter should indicate 0 and 40, respectively.
- (22) Set the distortion analyzer left-hand DISTORTION SELECT switch to AVERAGE and the pattern generator % DISTORT control to 0.
- (23) Set the pattern generator and distortion analyzer switches and controls to the positions specified below:

Equipment	Control or switch	Position
Pattern generator-----	MESSAGE SELECT switch--	SELECTED PULSES
	RATE control-----	75 BAUDS
	DISTORT SELECT switch-----	MARK/BIAS
	% DISTORT control-----	20
	MESSAGE TRANSMIT switch.	ON
Distortion analyzer-----	SELECTED PULSES 1 switch	MARK
	SELECTED PULSES 2 through 5 switches.	SPACE
	TRANSITION SELECT switch.	1
	Left-hand DISTORTION SELECT switch.	TOTAL PEAK
	Right-hand DISTORTION SELECT switch.	SPACE/PARK

- (24) Depress the distortion analyzer RESET switch. The PERCENT DISTORTION meter should indicate 20.
- (25) Set the pattern generator SELECTED PULSES 1 switch to SPACE and SELECTED PULSES 2 switch to MARK.
- (26) Set the distortion analyzer TRANSITION SELECT switch to 2 and depress the RESET switch. The PERCENT DISTORTION meter should indicate 20.
- (27) Set the pattern generator SELECTED PULSES 2 switch to SPACE and SELECTED PULSES 3 switch to MARK.
- (28) Set the distortion analyzer TRANSITION SELECT switch to 3 and depress the RESET switch. The PERCENT DISTORTION meter should indicate 20.
- (29) Set the pattern generator SELECTED PULSES 3 switch to SPACE and SELECTED PULSES 4 switch to MARK.

- (30) Set the distortion analyzer TRANSITION SELECT switch to 4 and depress the RESET switch. The PERCENT DISTORTION meter should indicate 20.
- (31) Set the pattern generator SELECTED PULSES 4 switch to SPACE and SELECTED pulses 6 switch to MARK.
- (32) Set the distortion analyzer TRANSITION SELECT switch to 6 and depress the RESET switch. The PERCENT DISTORTION meter should indicate 20.
- (33) Set the pattern generator SELECTED PULSES 6 switch to SPACE.
- (34) Set the distortion analyzer TRANSITION SELECT switch to 6 and depress the RESET switch. The PERCENT DISTORTION meter should indicate 20.
- (35) Set the distortion analyzer POLARITY switch to + and depress the RESET switch. The PERCENT DISTORTION meter should indicate 0.
- (36) Set the pattern generator, distortion analyzer, and the loop power supply

power switches to OFF, and disconnect the equipment,

c. Troubleshooting Chart. The symptoms listed in the troubleshooting chart may be observed during the operational test (b above). The possible troubles listed in the chart indicate defective circuits, stages, or parts that can cause each symptom to appear. The corrective measures listed in the chart may be used to localize the trouble to a defective circuit or stage, or to isolate the trouble to a defective part. When the corrective measures localize the trouble to a defective circuit, use the procedures given in paragraph 2-6 to localize the trouble to a stage. When the trouble is localized to a stage, use the procedures given in paragraph 2-7 to isolate the trouble to a defective part. When the corrective measures isolate the trouble to a defective part, refer to paragraph 2-6.

Note. The possible troubles and corrective measures indicated below do not include the possibility of defective wiring. When the trouble cannot be repaired using the corrective measures given, check the wiring associated with the particular circuit and repair any defective wiring.

Item No.	Symptom	Probable cause	Corrective measures
1	POWER indicator does not light when POWER switch on distortion analyzer is set to ON.	<ul style="list-style-type: none"> a. Defective lampholder 1A1XDS1. b. Defective line filter 1A1FL1. c. Defective POWER switch 1A1S1. d. Defective power supply ----- 	<ul style="list-style-type: none"> a. Check lampholder (fig. 2-15); replace if defective. b. Check line filter (fig. 2-16); replace if defective. o. Check switch (fig. 2-16); replace if defective. d. Take voltage and resistance measurements of the power supply (para 2-8); replace defective components.
2	SIGNAL indicator does not light but all other indications are normal when signal is applied to distortion analyser.	<ul style="list-style-type: none"> a. Defective resistor 1A1R1. b. Defective polarity switch 1A1S2. c. Defective varistor R5- ----- d. Defective lampholder 1A1XDS2. e. Defective inverter IN-1 or IN-2 on 1A2A6 (fig. 6-4). 	<ul style="list-style-type: none"> a. Check resistor (fig. 2-14); replace if defective. b. Check switch (fig. 2-15); replace if defective. c. Check varistor (fig. 2-15); replace if defective. d. Check lampholder; replace if defective. . . Check inverter (para 2-8a); replace defective component.

Item No.	Symptom	Probable cause	Corrective measures
3	LATE indicator does not light when making average distortion measurements of signal with spacing bias or marking end distortion, but all other indications are normal.	<ul style="list-style-type: none"> a. Defective lampholder 1A1XDS3. b. Defective resistor 1A2A14R37. c. Defective AND gate GAI-16 on 1A2A6 or GAD-13 on 1A2A14 (fig. 6-8). 	<ul style="list-style-type: none"> a. Check lampholder (fig. 2-14); replace if defective. b. Check resistor (fig. 2-12); replace if defective. c. Check AND gate (para 2-8e); replace defective components.
4	EARLY indicator does not light when making average distortion measurements of signal with making bias or spacing end distortion, but all other indications are normal.	<ul style="list-style-type: none"> a. Defective lampholder 1A1XDS4. b. Defective resistor 1A2A14R37. c. Defective AND gate GAI-17, on 1A2A66, or GAD-14 on 1A2A14 (fig. 6-8). 	<ul style="list-style-type: none"> a. Check lampholder (fig. 2-14); replace if defective. b. Check resistor (fig. 2-12); replace if defective. c. Check AND gate (para 2-8e); replace defective components.
5	Neither EARLY <i>nor</i> LATE indicator lights when making average distortion measurements regardless of type of distortion on signal, but all other indications are normal.	Defective A (rear) section of DISTORTION SELECT switch 1A1S7.	Check switch (fig. 2-15); replace if defective.
6	Either EARLY or LATE indicator is lighted at all times when making average distortion measurements regardless of type of distortion on signal, but all other indications are normal.	Defective bistable multivibrator FFA-2 on 1A2A14 (fig. 6-8).	Check bistable multivibrator (para 2-8c); replace defective components.
7	PERCENT DISTORTION meter always indicates below 25 regardless of type or amount of distortion on input signal, but all other indications are normal.	<ul style="list-style-type: none"> a. Defective digital-to-analog converter CCG-6 on 1A2A15 (fig. 6-12). b. Defective OR gate GOI-6 on 1A2A13 (fig. 6-6). c. Defective bistable multivibrator FFS-6 on 1A2A13 (fig. 6-9). 	<ul style="list-style-type: none"> a. Check digital-to-analog converter (para 2-8h); replace defective components. b. Check OR gate (para 2-8f); replace defective components. c. Check bistable multivibrator (para 2-8c); replace defective components.
8	PERCENT DISTORTION meter never indicates between 11.7 to 25 and 36.7 to 60 regardless of type or amount of distortion on input signal, but all other indications are normal.	<ul style="list-style-type: none"> u. Defective digital-to-analog converter CCG-5 on 1A2A15 (fig. 6-12). b. Defective OR gate GOI-5 on 1A2A12 (fig. 6-6). c. Defective bistable multivibrator FFS-5 on 1A2A12 (fig. 6-12). 	<ul style="list-style-type: none"> a. Check digital-to-analog converter (para 2-8h); replace defective components. b. Check OR gate (para 2-8f); replace defective components. c. Check bistable multivibrator (para 2-8c); replace defective components.

Item No.	Symptom	Probable cause	Corrective measures
9	PERCENT DISTORTION meter never indicates between 5.5 to 12.5, 18 to 25, 30.5 to 37.5, and 43 to 50 regardless of type or amount of distortion on input signal, but all other indications are normal.	<ul style="list-style-type: none"> a. Defective digital-to-analog converter CCG4 on 1A2A15 (fig. 6-12). b. Defective OR gate GOI-4 on 1A2A11 (fig. 6-6). c. Defective bistable multivibrator FFS-4 on 1A2A11 (fig. 6-9). 	<ul style="list-style-type: none"> a. Check digital-to-analog converter (para 2-8h); replace defective components b. Check OR gate (para 2-8f); replace defective components. c. Check bistable multivibrator (para 2-8c); replace defective components.
10	PERCENT DISTORTION meter never indicates between 2.3 to 6.2, 8.6 to 12.5, 14.8 to 18.8, 2.1 to 25, 27.8 to 31.2, 33.6, to 37.5, 39.8 to 43.6, and 46 to 50 regardless of type or amount of distortion on input signal, but all other indications are normal.	<ul style="list-style-type: none"> a. Defective digital-to-analog converter CCG3 on 1A2A15 (fig. 6-12). b. Defective OR gate GOI-3 on 1A2A10 (fig. 6-6). c. Defective bistable multivibrator FFS-3 on 1A2A10 (fig. 6-9). 	<ul style="list-style-type: none"> a. Check digital-to-analog converter (para 2-8h); replace defective component. b. Check OR gate (para 2-8f); replace defective components. c. Check bistable multivibrator (para 2-8c); replace defective components.
11	PERCENT distortion meter never indicates between 0.8 to 3.1, 3.9 to 6.3, 7 to 9.4 10.2 to 12.5, 13.3 to 15.6, 16.4 to 18.8, 19.5 to 21.9, 22.7 to 25.1, 25.9 to 28.2, 28.9 to 31.3, 32 to 34.4, 35.2 to 37.5, 38.3 to 40.6, 41.4 to 43.8, 44.6 to 46.9, and 47.6 to 50 regardless of type or amount of distortion on input signal, but all other indications are normal.	<ul style="list-style-type: none"> a. Defective digital-to-analog converter CCG-2 on 1A2A15 (fig. 6-12). b. Defective OR gate GOI-2 on 1A2A9 (fig. 6-6). c. Defective bistable multivibrator FFS-2 on 1A2A9 (fig. 6-9). 	<ul style="list-style-type: none"> u. Check digital-to-analog converter (para 2-8h); replace defective components. b. Check OR gate (para 2-8f); replace defective components. c. Check bistable multivibrator (para 2-8c); replace defective components.
12	PERCENT DISTORTION meter never indicates 0.8, 2.3, 3.9, 5.5, 7.0, 8.6, 10.2 11.7,13.3 14.8, 16.4, 18.0, 19.5, 21.1, 22.7, 24.2, 25..8, 27.3, 28.9, 30.5, 32.0 33.6, 35.2, 36.7, 38.3, 39.8, 41.4, 43.0, 44.6, 46.1, 47.7, and 43.2 regardless of type or amount of distortion on input signal, but all other indications are normal.	<ul style="list-style-type: none"> a. Defective digital-to-analog converter CCG-1 on 1A2A15 (fig. 6-9). b. Defective OR gate GOI-1 on 1A2A8 (fig. 6-6). c. Defective bistable multivibrator FFS-1 on 1A2A8 (fig. 6-9). 	<ul style="list-style-type: none"> a. Check digital-to-analog converter (para 2-8h); replace defective components. b. Check OR gate (para 2-8f); replace defective components. c. Check bistable multivibration (para 2-8c); replace defective components.

Item No.	Symptom	Probable cause	Corrective measures
13	PERCENT DISTORTION meter always indicates below 26 for input signal with any amount of spacing bias or marking end distortion, but indications are normal for signal with marking bias and spacing end distortion.	<ul style="list-style-type: none"> a Defective AND gate GAS-14 on 1A2A13 (fig. 6-9) or GAD-12 on 1A2A18 (fig. 6-6). b. Defective inverter IN-10 on 1A2A13 (fig. 6-6). 	<ul style="list-style-type: none"> a Check AND gate (para 2-8e); replace defective components. b. Check inverter (para 2-8g); replace defective components.
14	PERCENT DISTORTION meter never indicates between 11.7 and 26 36.7 to 50 for input signal with any amount of spacing and marking end bias distortion, but indications are normal for signal with marking bias or spacing end distortion.	<ul style="list-style-type: none"> a Defective AND gate GAS-12 on 1A2A12 (fig. 6-9) or GAD-10 on 1A2A12 (fig. 6-6). b. Defective inverter IN-9 on 1A2A12 (fig. 6-6). 	<ul style="list-style-type: none"> a Check AND gate (para 2-8e); replace defective components b. Check inverter (para 2-8g); replace defective components.
15	PERCENT DISTORTION meter never indicates between 5.5 to 12.5, 18 to 25, 30.5 to 37.5, and 43.8 to 50 for input signal with any amount of spacing bias and marking end distortion, but indication are normal for signal with marking or spacing end distortion.	<ul style="list-style-type: none"> a Defective AND gate GAS-10 on 1A2A11 (fig. 6-9) or GAD-18 on 1A2A11 (fig. 6-6). b. Defective inverter IN-8 on 1A2A11 (fig. 6-6). 	<ul style="list-style-type: none"> a. Check AND gate (para 2-8e); replace defective components. b. Check inverter (para 2-8g); replace defective components.
16	PERCENT DISTORTION meter never indicates between 2.3 to 6.2, 8.6 to 12.5, 14.8 to 18.7, 21.1 to 25, 27.8 to 31.2, 33.6 to 37.5, 39.8 to 43.6, and 46 to 50 for input signal with any amount of spacing bias or marking end bias distortion, but indications are normal for signal with marking bias or spacing end distortion.	<ul style="list-style-type: none"> a Defective AND gate GAS-8 on 1A2A10 (fig. 6-9) or GAD-6 on 1A2A10 (fig. 6-6). b. Defective inverter IN-7 on 1A2A10 (fig. 6-6). 	<ul style="list-style-type: none"> a Check AND gate (para 2-8e); replace defective component. b. Check inverter (para 2-8g); replace defective components.

Item No.	Symptoms	Probable cause	Corrective measures
17	PERCENT DISTORTION meter never indicates between 0.8 to 3.1, 3.9 to 6.3, 7.0 to 9.4, 10.2 to 12.5, 13.3 to 15.6, 16.4 to 18.8, 19.5 to 21.9, 22.7 to 25.1, 25.9 to 28.2, 28.9 to 31.3, 32.0 to 34.4, 35.2 to 37.5, 68.3 to 40.6, 41.4 to 43.8, 44.6 to 46.9, and 47.6 to 50 for input signal with any amount of spacing bias distortion, but indications are normal for signal with marking bias distortion.	a. Defective AND gate GAS-6 on 1A2A9 (fig. 6-9) or GAD-4 on 1A2A9 (fig. 6-6). b. Defective inverter IN-6 on 1A2A9 (fig. 6-6).	a. Check AND gate (para 2-8e); replace defective components. b. Check inverter (2-8g); replace defective components.
18	PERCENT DISTORTION meter never indicates 0.8, 2.3, 3.9, 5.5, 7.0, 8.6, 10.2, 11.7, 13.3, 14.8, 16.4, 18.0, 19.5, 21.0, 22.7, 24.2, 25.8, 27.3, 28.9, 30.5, 32.0, 33.6, 35.2, 36.7, 38.3, 39.8, 41.4, 43.0, 44.6, 46.1, 47.7, and 49.2 for input signal with any amount of spacing bias or marking end distortion, but indications are normal for signal with marking bias or spacing end distortion.	a. Defective AND gate GA S-4 on 1A2A8 (fig. 6-9) or GA D-2 on 1A2A8 (fig. 6-6). b. Defective inverter IN-5 on 1A2A8 (fig. 6-6).	a. Check AND gate (para 2-8e); replace defective components. b. Check inverter (para 2-8g); replace defective components.
19	PERCENT DISTORTION meter always indicates below 25 for input signal with any amount of marking bias or spacing end distortion, but indication are normal for signal with spacing bias or marking end distortion.	Defective AND gate GAD-11 on 1A2A13 (fig. 6-6) or GAS-13 on 1A2A13 (fig. 6-9).	Check AND gate (para 2-8e); replace defective components.
20	PERCENT DISTORTION meter never indicates between 5.5 to 12.5, 18 to 25, 30.5 to 37.5, and 43 to 50 for input signal with any amount of marking bias distortion, but indications are normal for signal with spacing bias distortion.	Defective AND gate GAD-9 on 1A2A12 (fig. 6-6) or GAS-11 on 1A2A12 (fig. 6-9).	Check AND gate (para 2-8e); replace defective components.

Item No.	Symptom	Probable cause	Corrective measures
21	PERCENT DISTORTION meter never indicates between 5.5 to 12.5, 18 to 25, 30.5 to 37.6, and 43 to 50 for input signal with any amount of marking bias distortion, but indications are normal for signal with spacing bias distortion.	Defective AND gate GAD-7 on 1A2A11 (fig. 6-6) or GAS-9 on 1A2A11 (fig. 6-9).	Check AND gate (para 2-8 e); replace defective components.
22	PERCENT DISTORTION meter never indicates between 2.3 to 6.2, 8.6 to 12.5, 14.8 to 18.8, 21.1 to 25, 27.3 to 31.2, 33.6 to 37.5, 39.8 to 43.6, and 46 to 50 for input signal with any amount of marking bias distortion but indications are normal for signal with spacing bias distortion.	Defective AND gate GAD-5 on 1A2A10 (fig. 6-6) or GAS-7 on 1A2A10 (fig. 6-9).	Check AND gate (para 2-8 e); replace defective components.
23	PERCENT DISTORTION meter never indicates between 0.8 to 3.1, 3.9 to 6.3, 7.0 to 9.4, 10.2 to 12.5, 13.3 to 15.6, 16.4, to 18.8, 19.5 to 21.9, 22.7 to 25.1, 25.9 to 28.2, 28.9 to 31.3, 32.0 to 34.4, 35.2 to 37.5, 38.3 to 40.6, 41.4 to 43.8, 44.6 to 46.9, and 47.6 to 50 for input signal with any amount of marking bias distortion, but indications are normal for signal with spacing bias distortion.	Defective AND gate GAD-3 on 1A2A9 (fig. 6-6) or GAS-5 on 1A2A9 (fig. 6-9).	Check AND gate (para 2-8e); replace defective component.
24	PERCENT DISTORTION meter never indicates 0.8, 2.3, 3.9, 5.5, 7, 8.6, 10.2, 11.7, 13.3, 14.8, 16.4, 18.0, 19.5, 21.0, 22.7, 24.2, 25.0, 27.3, 28.9, 30.5, 32.0, 33.6, 35.2, 36.7, 38.3, 39.8, 41.4, 43.0, 44.6, 46.0, 47.7, and 49.2 for input signal with any amount of marking bias distortion, but indications are normal for signal with spacing bias distortion.	Defective AND gate GAD-1 on 1A2A8 (fig. 6-6) or GAS-3 on 1A2A8 (fig. 6-6).	Check AND gate (para 2-8 e); replace defective components.

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Item No.	Symptom	Probable cause	(Corrective measures
25	PERCENT DISTORTION meter indicates zero at all times for input signal with any amount of spacing bias distortion and LATE indicator does not light, but indications are normal for signal marking bias distortion.	Defective emitter follower EF-1 on 1A2A14 (fig. 6-8).	Check emitter follower (para 2-8g); replace defective components.
26	PERCENT DISTORTION meter indicates zero at all times for input signal with any amount of marking bias distortion and EARLY indicator does not light, but indications are normal for signal with spacing bias distortion.	Defective emitter follower EF-2 on 1A2A14 (fig.6-8).	Check emitter follower (para 2-8g); replace defective components.
27	Distortion measurements cannot be made for 45.5 BAUDS position of RATE switch; at all other positions, operation is normal.	a. Defective RATE switch 1A1S8. b. Defective oscillator OSC-1 on 1A2A2 (fig. 6-5).	a. Check switch (fig. 2-15); replace if defective. b. Check oscillator (para 2-8k); replace if defective.
28	Distortion measurements cannot be made for 50 BAUDS position of RATE switch, at all other positions, operation is normal.	a. Defective RATE switch 1A1S8. b. Defective oscillator OSC-2 on 1A2A2 (fig. 6-5).	a. Check switch (fig. 2-15); replace if defective. b. Check oscillator (para 2-8k); replace if defective.
29	Distortion measurements cannot be made for 74.2 BAUDS position of RATE switch, at all other positions, operation is normal.	a. Defective RATE switch 1A1S8. b. Defective oscillator OSC-3 on 1A2A2 (fig. 6-5).	a. Check switch (fig. 2-15); replace if defective. b. Check oscillator (para 2-8k); replace if defective.
30	Distortion measurements cannot be made for 75 BAUDS position of RATE switch; at all other positions, operation is normal.	Defective RATE switch 1A1S8.	Check switch (fig. 2-15); replace if defective.
31	Distortion measurement cannot be made for 150 BAUDS position of RATE switch; at all other positions, operation is normal.	Defective RATE switch 1A1S8,	Check switch (fig. 2-15); replace if defective.
32	Distortion measurements cannot be made for 75 BAUDS and 150 BAUDS positions of RATE switch; at all other positions, operation is normal.	Defective oscillator OSC-4 on 1A2A2 (fig. 6-5).	Check oscillator (para 2-8k); replace if defective.

Item No.	Symptom	Probable cause	Corrective measures
33	Distortion measurements cannot be made for any position of RATE switch.	<ul style="list-style-type: none"> a. Defective switch 1A1S8----- b. Defective monostable multivibrator SSB-1 on 1A2A1 (fig. 6-5). c. Defective frequency divider (bistable multivibrator FFC-1 through FFC-4) on 1A2A1 (fig. 6-5). d. Defective AND gate GAI-4 on 1A2A8 (fig. 6-5). 	<ul style="list-style-type: none"> a. Check switch (fig. 2-15) ; replace if defective. b. Check multivibrator (para 2-8b) ; replace defective components. c. Check multivibrator (para 2-8c) ; replace defective component. d. Check AND gate (para 2-8e) ; replace defective components.
34	PERCENT DISTORTION meter indicates zero at all times for any type of distortion measurements, but EARLY and LATE indications operate normally.	<ul style="list-style-type: none"> a. Defective EXT M resistor 1A1R1 on terminal board 1A1TB1. b. Defective resistors 1A15R17, 1A15R18 or 1A15RT1. c. Defective current summer CSN-1 on 1A2A15 (fig. 6-2). d. Defective PERCENT DISTORTION meter 1A1M1. 	<ul style="list-style-type: none"> a. Check resistor (fig. 2-18) ; replace if defective. b. Check resistor (fig. 2-9); replace if defective. c. Check current summer (para 2-8i) ; replace defective components. d. Check meter (fig. 2-15); replace if defective.
35	SIGNAL indicator does not blink off and on with test message applied to distortion analyzer, and PERCENT DISTORTION meter indicates zero at all times.	Defective Schmitt trigger STA-1 on 1A2A6 (fig. 6-4).	Check Schmitt trigger (para 2-8d) ; replace defective components.
36	SYNC pulse indication is not present at J2 (fig. 2-14) at the end of each character; all other indications are normal.	Defective inverter IN-4 on 1A2A4 (fig. 6-4).	Check inverter (para 2-8g) ; replace defective components.
37	SYNC pulse indication is present at end of first character, but after that, appears at random.	Defective AND gate GAI-1 on 1A2A4 (fig. 6-4).	Check AND gate (para 2-8e); replace defective components.
38	SYNC pulse indication is not present at the end of each character, and PERCENT DISTORTION meter indicates zero regardless of distortion.	<ul style="list-style-type: none"> a. Defective inverter IN-3 or IN-4 on 1A2A4 (fig. 6-4). b. Defective AND gate GAI-2 on 1A2A3 (fig. 6-11). 	<ul style="list-style-type: none"> a. Check inverter (para 2-8e) ; replace defective components. b. Check AND gate (para 2-8e); replace defective components
39	Distortions measurements cannot be made with TRANSITION SELECT switch set to 1; at all other positions, operation is normal.	Defective TRANSITION SELECT switch 1A1S9.	Check switch (fig. 2-15); replace if defective.

Item No.	Symptom	Probable cause	Corrective measures
40	Distortion measurements cannot be made with TRANSITION SELECT switch set to 2; at all other positions, operation is normal.	a. Defective TRANSITION SELECT switch 1A1S9. b. Defective AND gate GAI-6 on 1A2A3 (fig. 6-11).	a. Check switch (fig. 2-15); replace if defective. b. Check AND gate (para 2-8e); replace defective components.
41	Distortion measurements cannot be made with TRANSITION SELECT switch set to 3; at all other positions, operation is normal.	a. Defective TRANSITION SELECT switch 1A1S9. b. Defective AND gate GAI-7 on 1A2A3 (fig. 6-11).	a. Check switch (fig. 2-15); replace if defective. b. Check AND gate (para 2-8e); replace defective components.
42	Distortion measurements cannot be made with TRANSITION SELECT switch set to 4; at all other positions, operation is normal.	a. Defective TRANSITION SELECT switch 1A1S9. b. Defective AND gate GAI-8 on 1A2A3 (fig. 6-11).	a. Check switch (fig. 2-15); replace if defective. b. Check AND gate (para 2-8e); replace defective component.
43	Distortion measurements cannot be made with TRANSITION SELECT switch set to 5; at all other positions, operation is normal.	a. Defective TRANSITION SELECT switch 1A1S9. b. Defective AND gate GAI-9 on 1A2A3 (fig. 6-11).	a. Check switch (fig. 2-15); replace if defective. b. Check AND gate (para 2-8e); replace defective components.
44	Distortion measurement cannot be made with TRANSITION SELECT switch set to 6; at all other positions, operation is normal.	a. Defective TRANSITION SELECT switch 1A1S9. b. Defective AND gate GAI-10 on 1A2A3 (fig. 6-11).	a. Check switch (fig. 2-15); replace if defective. b. Check AND gate (para 2-8e); replace defective components.
45	Distortion measurements cannot be made with TRANSITION SELECT switch set to ALL; at all other position, operation is normal.	Defective TRANSITION select switch 1A1S9.	Check switch (fig. 2-15); replace if defective.
46	PERCENT DISTORTION meter reading erratic with fixed amount of distortion applied when making average distortion measurements. EARLY and LATE indicator will also switch off and on.	Defective digital time-base counter (fig. 6-6).	Check digital time-base counter (para 2-6 b); replace defective components
47	PERCENT DISTORTION meter indicates zero at all times when DISTORTION SELECT switch is set at EARLY PEAK, but indication are normal for all other positions,.	Defective AND gate GAI-14 on 1A2A14 (fig. 6-8).	Check AND gate (para 2-8e); replace defective components.

Item No.	Symptom	Probable cause	Corrective measures
48	PERCENT DISTORTION meter indicates zero at all times when DISTORTION SELECT switch is set at LATE PEAK, but indications are normal for all other positions.	Defective AND gate GAI-13 on 1A2A14 (fig. 6-8).	Check AND gate (para 2-8e); replace defective components.
49	PERCENT DISTORTION meter indicates zero at all times when TRANSITION SELECT switch is set at MARK/SPACE and DISTORTION SELECT switch is set at any position other than TOTAL PEAK, but all other indications are normal.	Defective AND gate GAS-1 on 1A2A5 (fig. 6-4).	Check AND gate (para 2-8e); replace defective components.
50	PERCENT DISTORTION meter indicates zero at all times when TRANSITION SELECT switch is set at SPACE/MARK and DISTORTION SELECT switch is set in any position other than TOTAL PEAK, but all other indications are normal.	Defective AND gate GAS-2 on 1A2A5 (fig. 6-4).	Check AND gate (para 2-8e); replace defective components.
51	PERCENT DISTORTION meter indication does not drop to zero when RESET switch is depressed.	a. Defective RESET switch 1A1S5. b. Defective resistor 1A2A8R37 or 1A2A8R38.	a. Check switch (fig. 2-15) ; replace if defective. b. Check resistor (fig. 2-10); replace if defective.
52	No indications on distortion analyzer for any type of input signal and no SYNC pulse indication.	a. Defective INPUT POLARITY switch A1S6. b. Defective INPUT SELECT switch 1A1S4.	a. Check switch (fig. 2-15) ; replace if defective. b. Check switch (fig. 2-15) ; replace if defective.
53	PERCENT DISTORTION meter indicates zero for input signal with no distortion when FILTER switch is set at OUT, but does indicate distortion when FILTER switch is set at IN when input signal has no distortion.	FILTER ADJ resistor 1A2A5R4 out of adjustment.	Adjust resistor (para 3-2).
54	PERCENT DISTORTION meter indication automatically resets while making peak distortion measurements.	Defective inverter IN-1 on 1A2A6 (fig. 6-4).	Check inverter (para 2-8g) ; replace defective components.

Item No.	Symptom	Probable cause	Corrective measures
55	When measuring peak distortion, PERCENT DISTORTION meter indications do not correspond to distortion on input signal, but all indications are normal when measuring average distortion.	Defective AND gate GAI-15 or GAI-18 on 1A2A14 (fig. 6-8). Defective magnitude comparator circuit (fig. 6-7).	Check AND gate (para 2-8e); replace defective components. Check magnitude comparator circuit (para 2-6d); replace defective component.
56	No indication on distortion analyzer for any type of input signal.	Defective baud counter circuit (fig. 6-11).	Check baud counter circuit (para 2-6c); replace defective components.
57	PERCENT DISTORTION meter indication does not correspond to distortion applied by pattern generator when making average distortion measurements.	a. Schmitt trigger circuits out of adjustment. b. Meter drive circuits out of adjustment. c. Defective digital time-base counter circuits (fig. 6-6).	a. Adjust Schmitt trigger circuits (para 3-2). b. Adjust meter drive (para 3-2) c. Check digital time-base counter circuits (para 2-6b); replace defective components.

2-6. Signal Tracing

Note. Refer to paragraph 2-17 for location of printed circuit assemblies.

a. General. When trouble has been localized to a specific circuit (para 2-5), the oscilloscope may be used to localize the trouble to a stage within the circuit.

- (1) Prepare the equipment by following the procedures given in paragraph 2-4.
- (2) Position the distortion analyzer so as to provide access to the harness board at the bottom of the chassis, and the printed circuit card assemblies at the top.
- (3) When the trouble has been localized to a stage, refer to paragraph 2-8.

b. Digital Time-Base Counter Circuits.

- (1) Set the MESSAGE SELECT switch on the pattern generator to DOT CY and the MESSAGE TRANSMIT switch to ON.
- (2) Set the distortion analyzer and pattern generator power switches to ON.

- (3) Remove the printed circuit card assembly to be tested, and install extender card 1A2A7 (fig. 2-13) in its place. Plug the printed circuit card assembly into the extender card.
- (4) Use the oscilloscope to check for a square wave at the output of each bi-stable multivibrator stage (FFC-8 through FFC-14) (fig. 2-17). The following chart indicates the printed circuit card assembly and pins to check to localize the trouble to one or more stages in the digital time-base counter circuits

Assembly	Pin	Associated stage
1A2A8	P	FFC8
1A2A9	X	FFC9
1A2A10	X	FFC-10
1A2A11	X	FFC11
1A2A12	X	FFC-12
1A2A13	X	FFC-13
1A2A14	D	FFC14
1A2A14	J	EF-1
1A2A14	K	EF-2

- (5) When the square wave output is not present at a given terminal, troubleshoot the associated stage or stages by

following the procedures given in paragraph 2-8.

c. *Baud Counter Circuits* (fig. 6-11).

- (1) Set the pattern generator MESSAGE SELECT switch to DOT CY and the MESSAGE TRANSMIT switch to ON.
- (2) Set the distortion analyzer and the pattern generator power switches to ON.
- (3) Remove the printed circuit card to be tested, and install extender card 1A2-A7 in its place. Plug the printed circuit card assembly into the extender card.
- (4) Use the oscilloscope to check for a square wave at the output of each bistable multivibrator stage FFC-5 through FFC-7 (fig. 2-17). The following chart indicates the assembly and pins to check to localize the troubles to the stages in the baud counter circuits.

Assembly	Pin	Associated stage
1A2A4-----	Z	FFC-5
1A2A4-----	Y	FFC-6
1A2A4-----	X	FTC-7

- (5) When the square wave output is not present at a given terminal, troubleshoot the associated stages by following the appropriate procedures given in paragraph 2-8.

d. *Magnitude Comparator Circuits.*

- (1) Connect a black test lead between the -DC and ±AC OHMS jack of the multimeter and terminal A of connector XA9 (fig. 2-14).
- (2) Connect a red test lead between the 50V (20,000 OHMS PER VOLT DC) jack of the multimeter and terminal S of connector XA9.
- (3) Set the multimeter FUNCTION switch to REV.
- (4) Remove printed circuit card assembly 1A1A2 (fig. 2-17) from the distortion analyzer.
- (5) Set the distortion analyzer POWER switch to ON.
- (6) Depress distortion analyzer RESET switch.
- (7) Connect a test lead to terminal N of connector XA2, and momentarily

touch the free end of the test lead to terminal H of connector XA2. The multimeter should indicate approximately 0 volt.

- (8) Disconnect the test lead from terminal N of connector XA2 and reconnect the test lead to terminal B of connector XA2.
- (9) Momentarily touch the free end of the test lead to terminal H of connector XA2. The multimeter should indicate approximately -15 volts.
- (10) Momentarily touch the free end of the test lead to terminal A of connector XA2. The multimeter should indicate approximately 0 volt. If the correct indication is not obtained, check AND gate GAD-13 (para 2-8e).
- (11) Disconnect the test lead from terminal B of connector XA2 and reconnect the test lead to terminal U of connector XA8.
- (12) Momentarily touch the free end of the test lead to terminal H of connector XA8. The multimeter should indicate approximately -15 volts. If the correct indication is not obtained, check OR gate GOB-9 (para 2-8f) or AND gate GAT-25 (para 2-8e).
- (13) Depress the distortion analyzer RESET switch. The multimeter should indicate approximately 0 volt.
- (14) Disconnect the test lead from terminal U of connector XA8 and reconnect the test lead to terminal U of connector XA7.
- (15) Momentarily touch the free end of the test lead to terminal H of connector XA7. The multimeter should indicate approximately -15 volts. If the correct indication is not obtained, check OR gate GOB-7 (para 2-8f) or AND gate GAI-25 (para 2-8e).
- (16) Depress the distortion analyzer RESET switch. The multimeter should indicate approximately 0 volt.
- (17) Disconnect the test lead from terminal U of connector XA7 and reconnect the test lead to terminal U of connector XA6.
- (18) Momentarily touch the free end of the test lead to terminal H of connector

- XA6. The multimeter should indicate approximately -15 volts. If the correct indication is not obtained, check OR gate GOB-5 (para 2-8f) or AND gate GAI-23 (para 2-8e).
- (19) Depress the distortion analyzer RESET switch. The multimeter should indicate approximately 0 volt.
 - (20) Disconnect the test lead from terminal U of connector XA6 and reconnect the test lead to terminal U of connector XA4.
 - (21) Momentarily touch the free end of the test lead to terminal H of connector XA4. The multimeter should indicate approximately -15 volts. If the correct indication is not obtained, check OR gate GOB-3 (para 2-8f) or AND gate GAI-21 (para 2-8e).
 - (22) Depress the distortion analyzer RESET switch. The multimeter should indicate approximately 0 volt.
 - (23) Disconnect the test lead from terminal U of connector XA4 and reconnect the test lead to terminal U of connector XA3.
 - (24) Momentarily touch the free end of the test lead to terminal H of connector XA3. The multimeter should indicate approximately -15 volts. If the correct indication is not obtained, check OR gate GOB-1 (para 2-8f) or AND gate GAI-19 (para 2-8e).
 - (25) Depress the distortion analyzer RESET switch.
 - (26) Disconnect the test lead from terminal U of connector XA3 and reconnect the test lead to terminal N of connector XA2.
 - (27) Momentarily touch the free end of the test lead to terminal H of connector XA2. The multimeter should indicate approximately 0 volt.
 - (28) Disconnect the test lead from terminal N of connector XA2 and reconnect the test lead to terminal U of connector XA2.
 - (29) Disconnect the test lead from terminal U of connector XA2 and reconnect the test lead to terminal U of connector XA8.
 - (30) Momentarily touch the free end of the test lead to terminal H of connector XA8. The multimeter should indicate approximately -15 volts. If the correct indication is not obtained, check OR gate GOB-10 (para 2-8f) or AND gate GAI-28 (para 2-8e).
 - (31) Momentarily touch the free end of the test lead to terminal A of connector XA8. The multimeter should indicate approximately 0 volt.
 - (32) Disconnect the test lead from terminal U of connector XA8 and reconnect the test lead to terminal U of connector XA7.
 - (33) Momentarily touch the free end of the test lead to terminal H of connector XA7. The multimeter should indicate approximate}} -15 volts. If the correct indication is not obtained, check OR gate GOB-8 (para 2-8f) or AND gate GAA-26 (para 2-8e).
 - (34) Momentarily touch the free end of the test lead to terminal A of connector XA7. The multimeter should indicate approximately 0 volt.
 - (35) Disconnect the test lead from terminal U of connector XA7 and reconnect the test lead to terminal U of connector XA6.
 - (36) Momentarily touch the free end of the test lead to terminal H of connector XA6. The multimeter should indicate approximately -15 volts. If the correct indication is not obtained, check OR gate GOB-6 (para 2-8f) or AND gate GAI-24 (para 2-8e).
 - (37) Momentarily touch the free end of the test lead to terminal A of connector XA6. The multimeter should indicate approximately 0 volt.
 - (38) Disconnect the test lead from terminal U of connector XA6 and reconnect the test lead to terminal U of connector XA4.
 - (39) Momentarily touch the free end of the test lead to terminal H of connector XA4. The multimeter should indicate

approximately 0 volt. If the correct indication is not obtained, check OR gate GOB-4 (para 2-8f) or AND gate GAA-22 (para 2-8e).

- (40) Momentarily touch the free end of the test lead to terminal A of connector XA4. The multimeter should indicate approximately 0 volt.
- (41) Disconnect the test lead from terminal U of connector XA4 and reconnect the test lead to terminal U of connector XA3.
- (42) Momentarily touch the free end of the test lead to terminal H of connector XA3. The multimeter should indicate approximately -15 volts. If the correct indication is not obtained, check OR gate GOB-2 (para 2-8f) or AND gate GAA-20 (para 2-8e).
- (43) Set the distortion analyzer POWER switch to OFF, and disconnect the multimeter and the test leads.

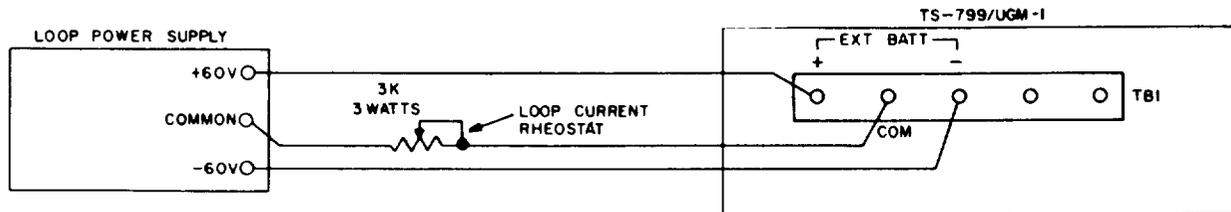
2-7. Location of Logic Circuits

The following chart list the logic gates and the printed circuit cards on which they are located. To determine reference designations, locations, and other data concerning individual components associated with the specific logic circuits, refer to the schematic diagrams (figs. 6-4 through 6-12), component location diagram (figs. 2-1 through 2-17), and voltage and resistance diagrams (figs. 2-18 and 2-19).

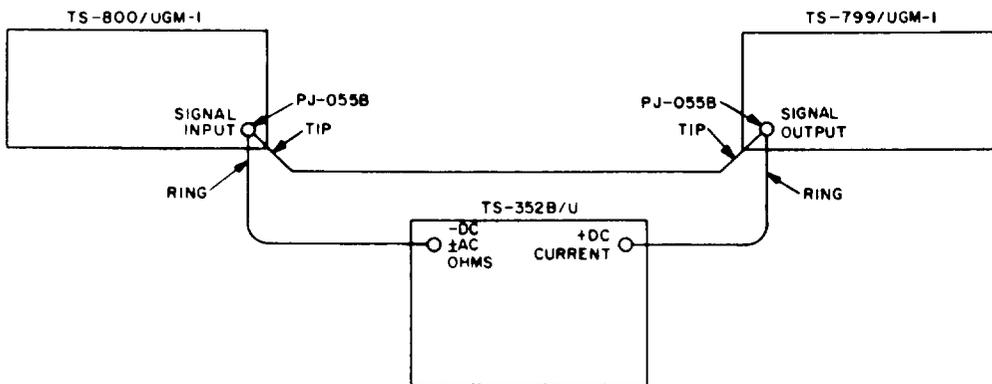
Circuit designation	Located on assembly (fig. 2-17)
CCG-1-----	1A2A15
CCG-2-----	1A2A15
CCG-3-----	1A2A15
CCG-4-----	1A2A15
CCG-5-----	1A2A15
CCG-6-----	1A2A15
CSN-1-----	1A2A15
EF-1-----	1A2A14
EF-2-----	1A2A14
FFA-1-----	1A2A5
FFA-2-----	1AA14
FFC-1-----	1A2A1
FFC-2-----	1A2A1
FFC-3-----	1A2A1
FFC-4-----	1A2A1
FFC-5-----	1A2A4

Circuit designation	Located on assembly (fig. 2-17)
FFC-6-----	1A2A4
FFC-7-----	1A2A4
FFC-8-----	1A2A8
FFC-9-----	1A2A9
FFC-10-----	1A2A10
FFC-11-----	1A2A11
FFC-12-----	1A2A12
FFC-13-----	1AA213
FFC-14-----	1A2A14
FFS-1-----	1A2A8
FFS-2-----	1A2A9
FFS-3-----	1A2A10
FFS-4-----	1A2A11
FFS-5-----	1A2A12
FFS-6-----	1A2A13
GAD-1-----	1A2A8
GAD-2-----	1A2A8
GAD-3-----	1A2A9
GAD-4-----	1A2A9
GAD-5-----	1A2A10
GAD-6-----	1A2A10
GAD-7-----	1A2A11
GAD-8-----	1A2A11
GAD-9-----	1A2A12
GAD-10-----	1A2A12
GAD-11-----	1AA13
GAD-12-----	1A2A13
GAD-13-----	1A2A8, 1A2A14
GAD-14-----	1A2A14
GAI-1-----	1A2A4
GAI-2-----	1A2A3
GAI-3-----	1A2A5
GAI-4-----	1A2A8
GAI-5-----	1A2A3
GAI-6-----	1A2A3
GAI-7-----	1A2A3
GAI-8-----	1A2A3
GAI-9-----	1A2A3
GAI-10-----	1A2A3
GAI-11-----	1A2A3
GAI-12-----	1A2A3
GAI-13-----	1A2A14
GAI-14-----	1A2A14
GAI-15-----	1A2A14
GAI-16-----	1A2A6
GAI-17-----	1A2A6
GAI-18-----	1A2A14
GAI-19-----	1A2A9
GAI-20-----	1A2A9
GAI-21-----	1A2A10
GAI-22-----	1A2A10
GAI-23-----	1A2A11
GAI-24-----	1A2A11
GAI-25-----	1A2A12
GAI-26-----	1A2A12
GAI-27-----	1A2A13
GAI-28-----	1A2A12
GAS-1-----	1A2A5

Circuit designation	Located on assembly (fig. 2-17)	Circuit designation	Located on assembly (fig. 2-17)
GAS-2	1A2A5	GOI-3	1A2A10
GAS-3	1A2A8	GOI-4	1A2A11
GAS-4	1A2A8	GOI-5	1A2A12
GAS-5	1A2A9	GOI-6	1A2A13
GAS-6	1A2A9	IN-1	1A2A6
GAS-7	1A2A10	IN-2	1A2A7
GAS-8	1A2A10	IN-3	1A2A6
GAS-9	1A2A11	IN-4	1A2A7
GAS-10	1A2A11	IN-5	1A2A8
GAS-11	1A2A12	IN-6	1A2A9
GAS-12	1A2A12	IN-7	1A2A10
GAS-13	1A2A13	IN-8	1A2A11
GAS-14	1A2A13	IN-9	1A2A12
GAT-1	1A2A5	IN-10	1A2A13
GOB-1	1A2A9	IN-11	1A2A14
GOB-2	1A2A9	OSC-1	1A2A2
GOB-3	1A2410	OSC-2	1A2A2
GOB-4	1A2A10	OSC-3	1A2A2
GOB-5	1A2A11	OSC-4	1A2A2
GOB-6	1A2A11	SSA-1	1A2A5
GOB-7	1A2A12	SSA-2	1A2A8
GOB-8	1A2A12	SSB-1	1A2A1
GOB-9	1A2A13	STA-1	1A2A6
GOB-10	1A2A13	STA-2	1A2A5
GOI-1	1A2A8	Tonekeyer	1A2A6
GOI-2	1A2A9	Tonekeyer	1A2A6



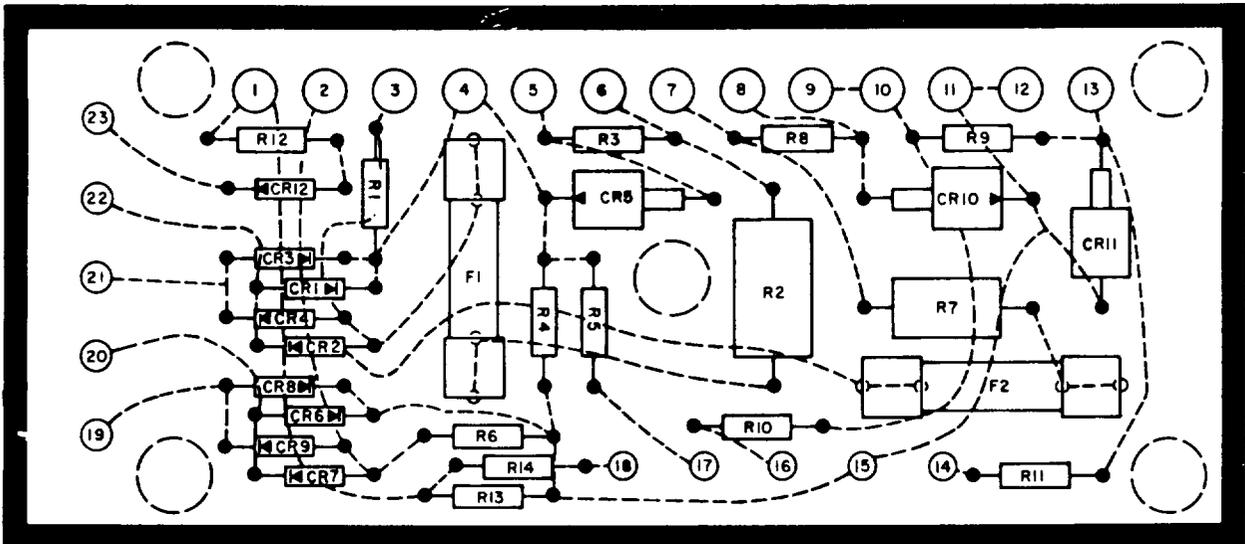
A. LOOP CONNECTIONS



B. SIGNAL CONNECTIONS

TM6625-620-45/2-4

Figure 2-1. Test setup connections.



TM6625-620-45/2-21

Figure 2-2. Printed circuit card assembly 1A3A1 (80047110), component locations.

2-8. Isolating Troubles

Note. For location of logic circuits, refer to paragraph 2-7, and for location of printed circuit boards, refer to figure 2-17.

Caution: Do not make resistance measurements in the distortion analyzer unless specifically directed to do so. The battery voltage in an ohmmeter can damage the transistors.

a. *General.* When trouble has been localized to a stage on a printed circuit card, locate the stage and follow the procedures given in (1) below. When making voltage measurements, use the procedures given in (2) below. If an intermittent trouble is suspected, use the procedures given in (3) below. When the trouble is isolated to a defective pint, refer to paragraph 2-9.

(1) Isolation procedures.

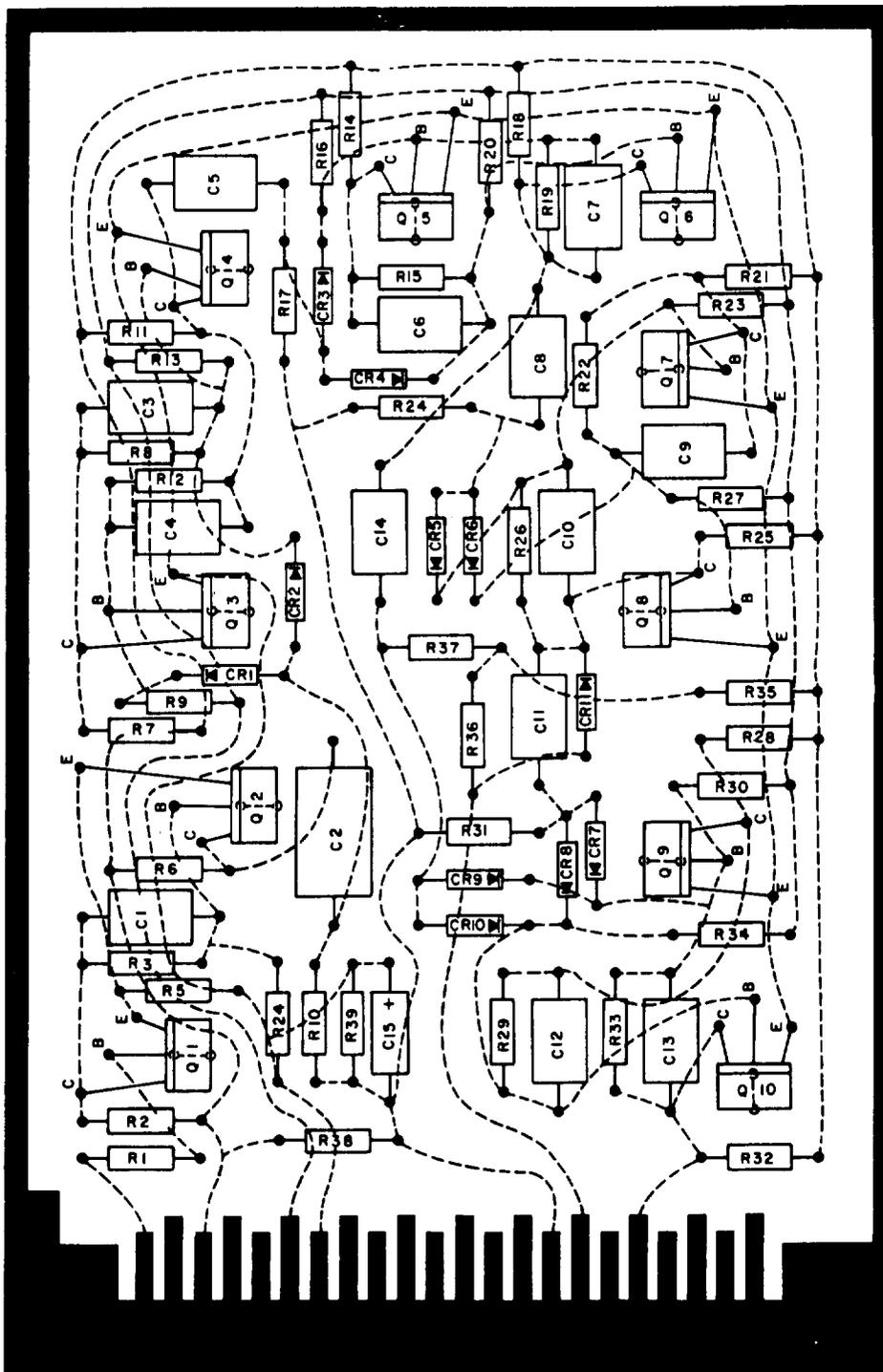
- (a) Set the distortion analyzer POWER switch to OFF.
- (b) Remove the printed circuit card containing the stage to be checked and install extender card assembly 1A2 in its place.
- (c) Plug the connector on the printed circuit card into the connector on extender card assembly 1A2A7.

(d) Set the distortion analyzer POWER switch to ON.

(e) Troubleshoot the stage; follow the applicable procedures given in b, c, d, e, f, g, h, i, j, or k, below.

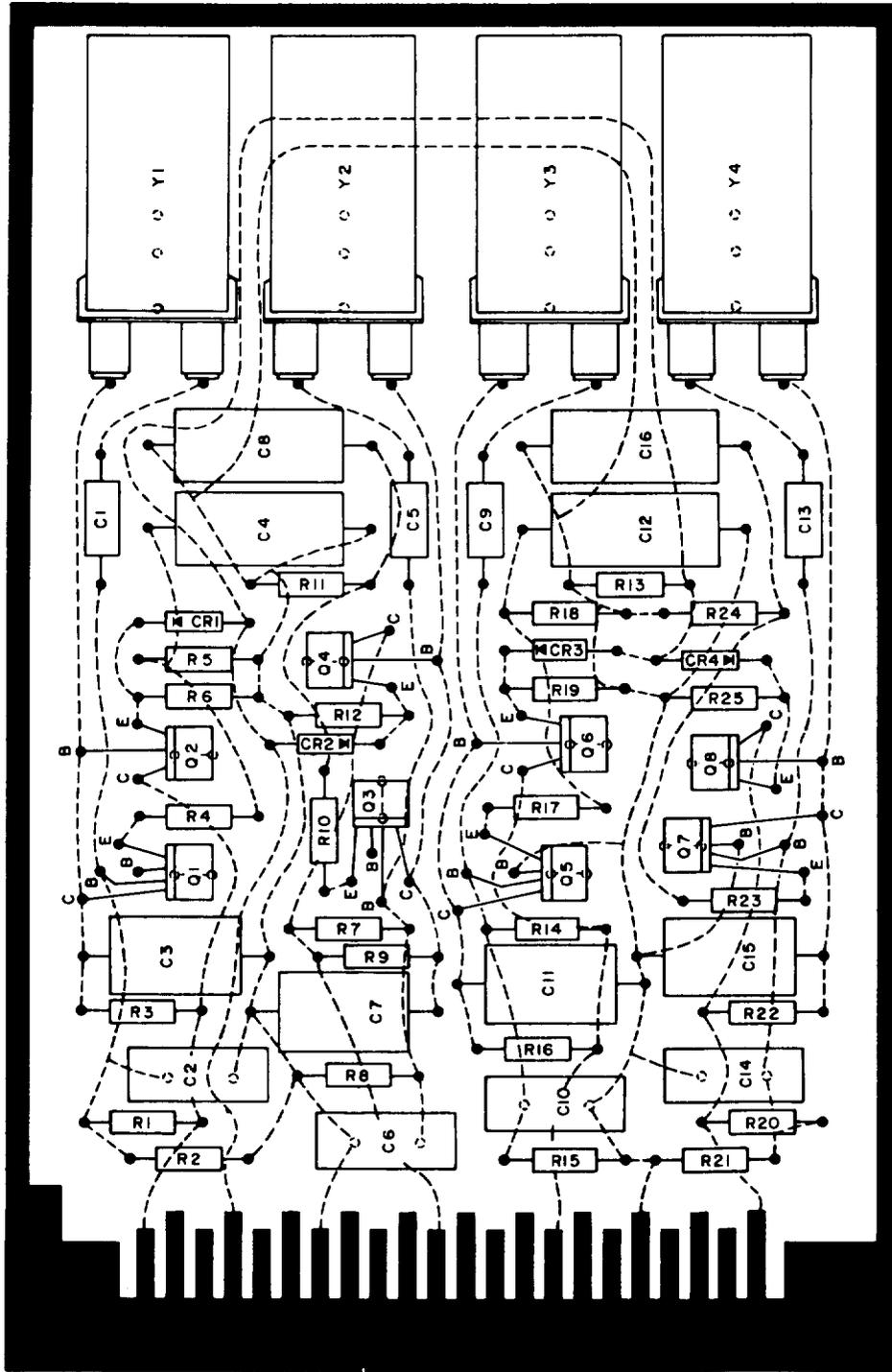
Note. The isolation procedures given in b through j below reference figures 2-1 through 2-19. To determine the actual reference designation for a specific part, compare the circuit with the applicable schematic diagram (figs. 6-4 through 6-12) and obtain the correct reference designations.

- (2) *Voltage measurements.* This equipment is transistorized. Observe all precautions given, to prevent transistor damage. Make voltage measurements in this equipment only as specified. When measuring voltages, use tape or sleeving to insulate the entire probe, except the extreme tip. A momentary short circuit can ruin a transistor. *For example,* if the bias is shorted out, excessive emitter-base current would bum out the transistor. Use the resistor and capacitor color codes (figs. 5-1 and 6-1) to determine part values.



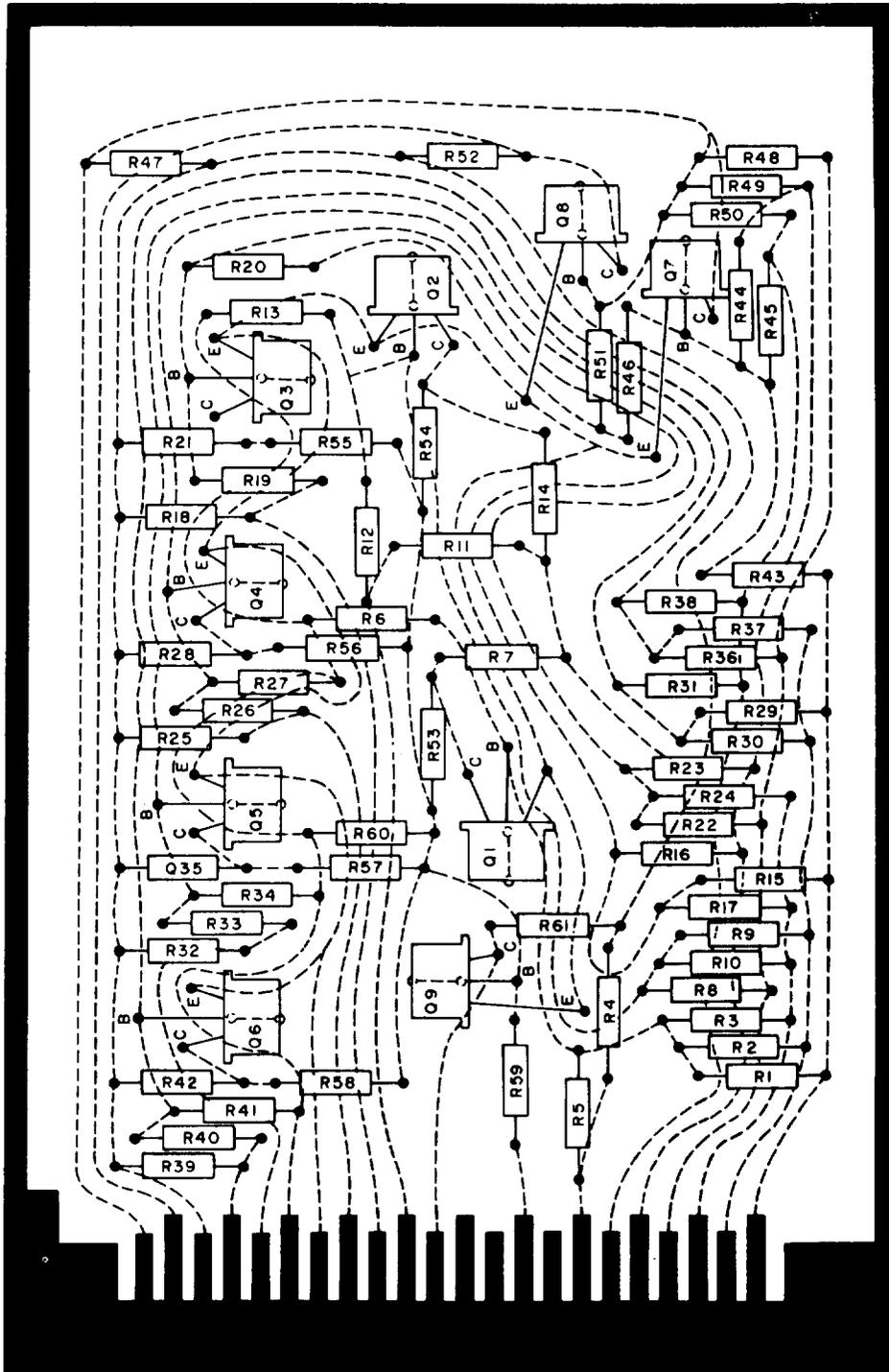
TM6625-620-45/2-22

Figure 2-3. Printed circuit card assembly 1A2A1 (80047060), component locations.



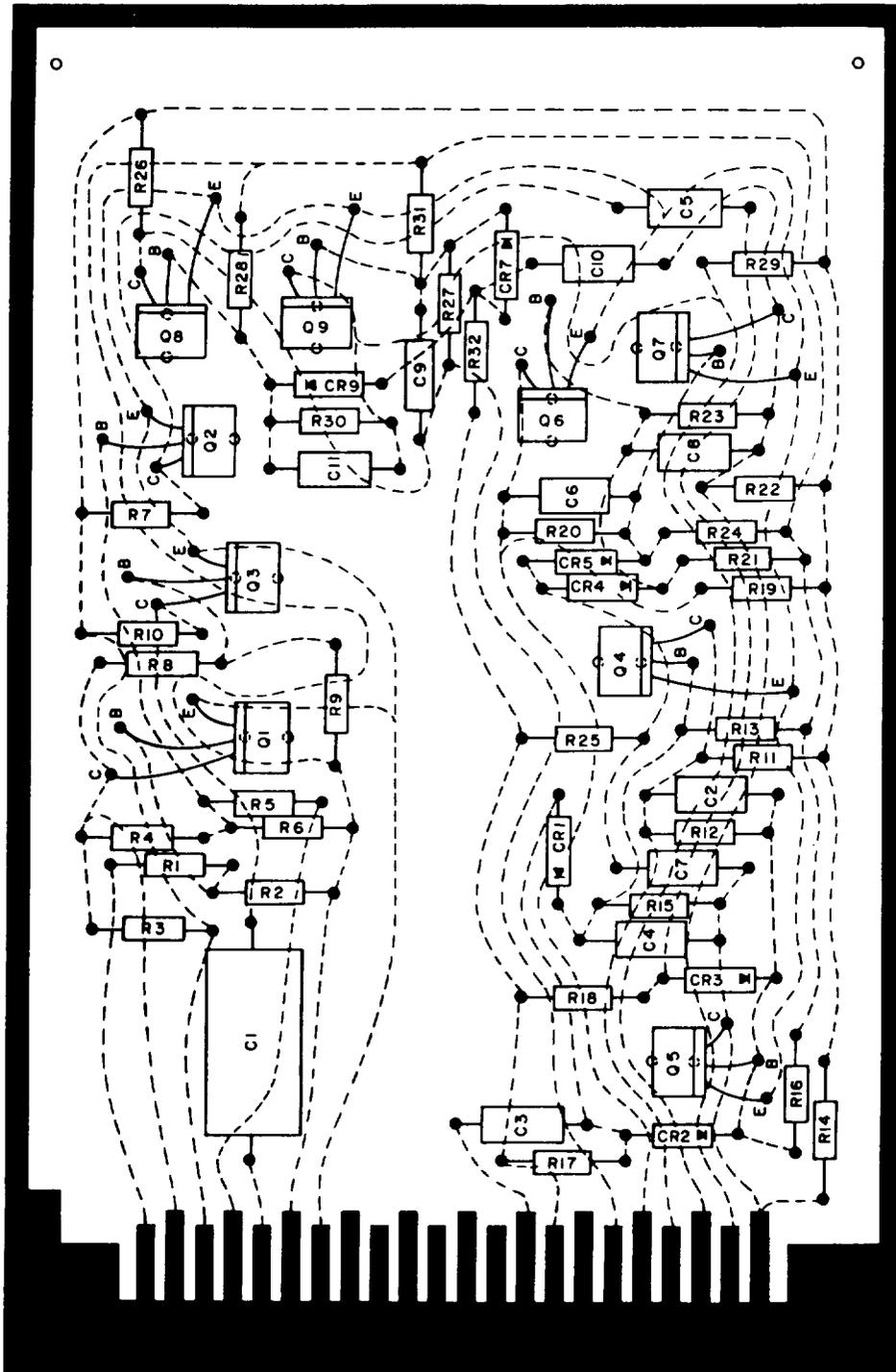
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Figure 2-4. Printed circuit card assembly 1A2A (80047050), component locations.



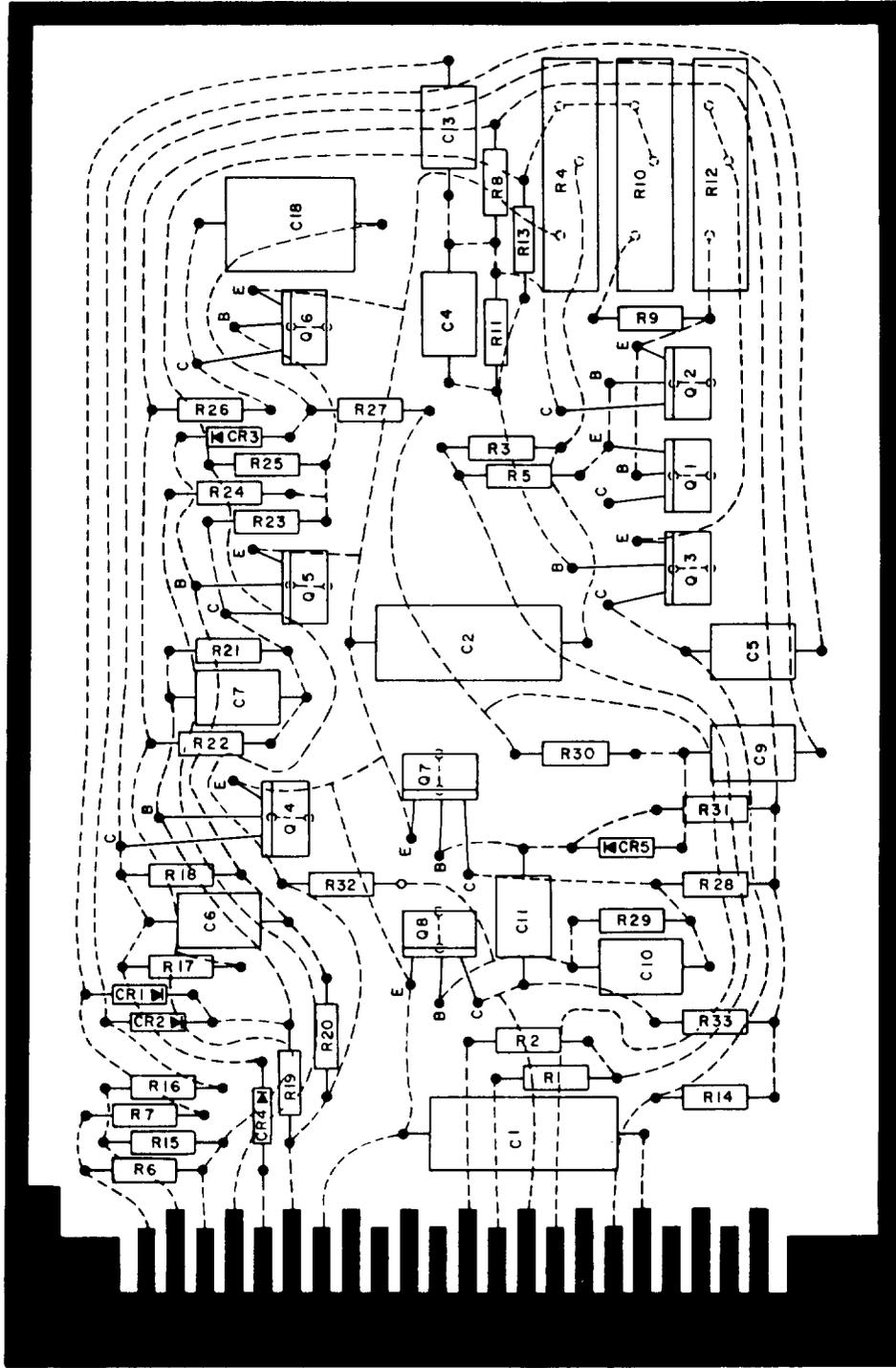
TM6625-620-45/2-24

Figure 2-5. Printed circuit card assembly 1A2A3(80047090), component locations.



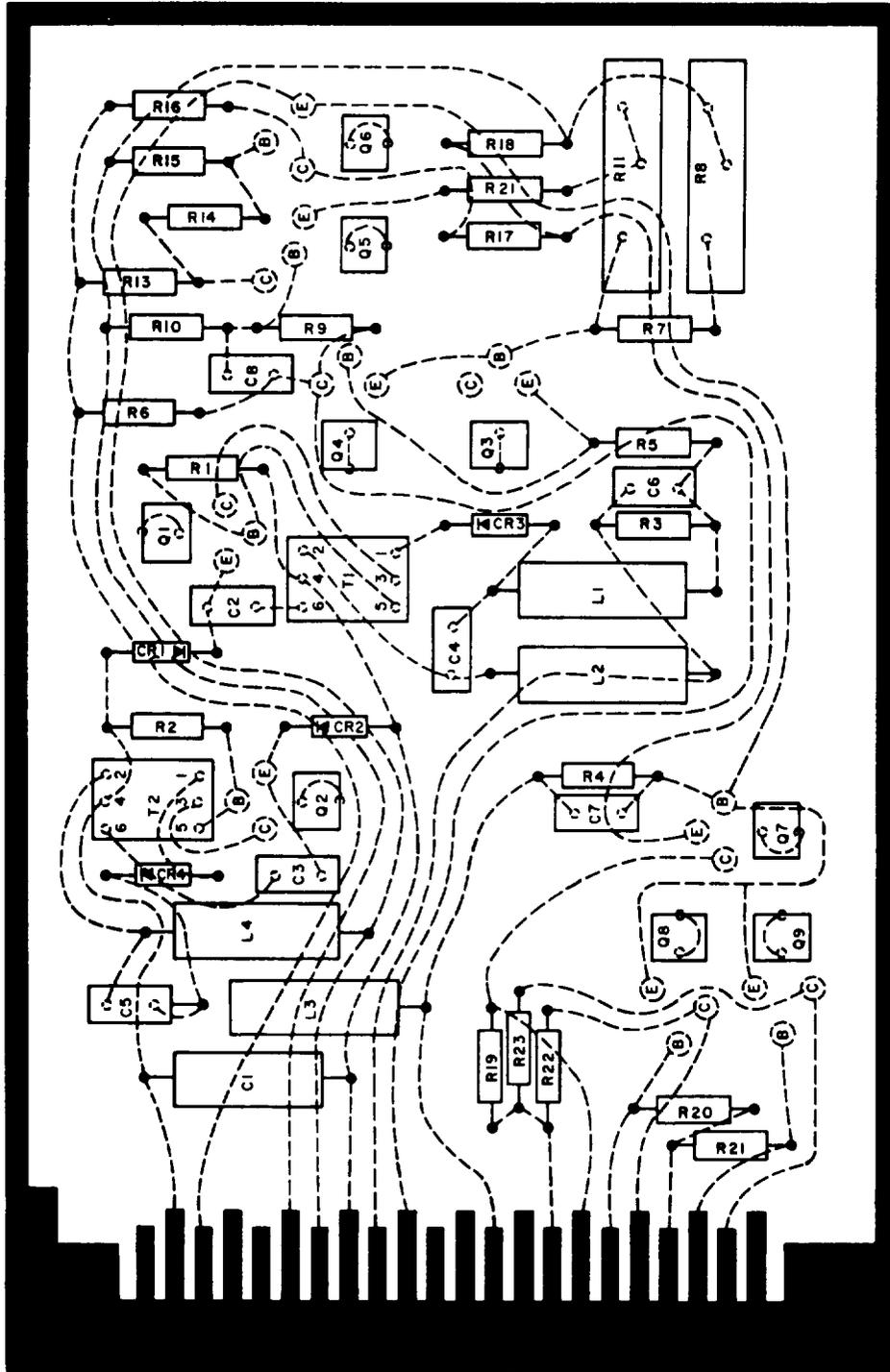
TM6625-620-45/2-25

Figure 2-6. Printed circuit card assembly 1A2A4 (80047100), component locations.



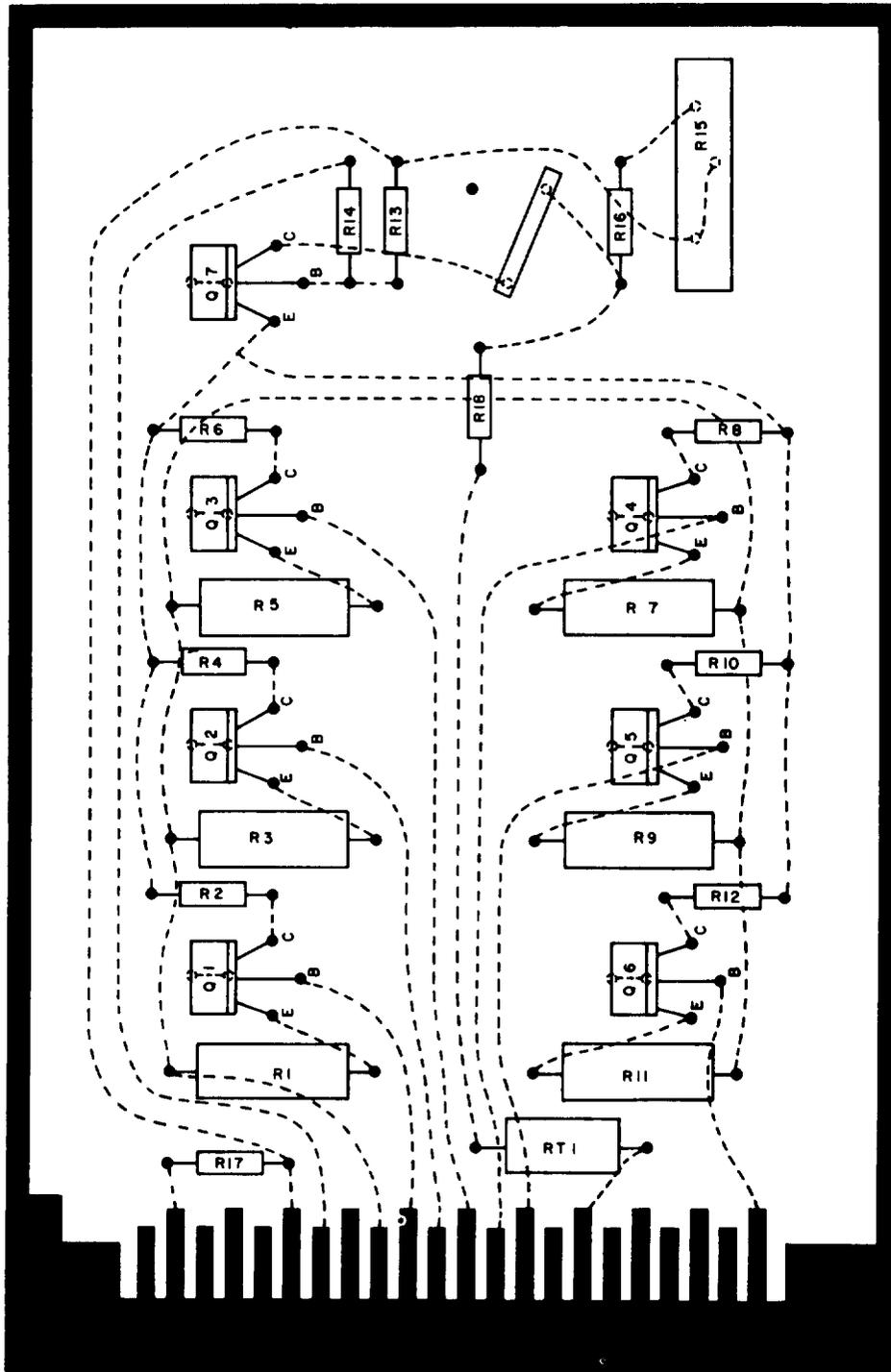
TM6625-620-45/2-26

Figure 2-7. Printed circuit card assembly 1A2A5 (80047020), component locations.



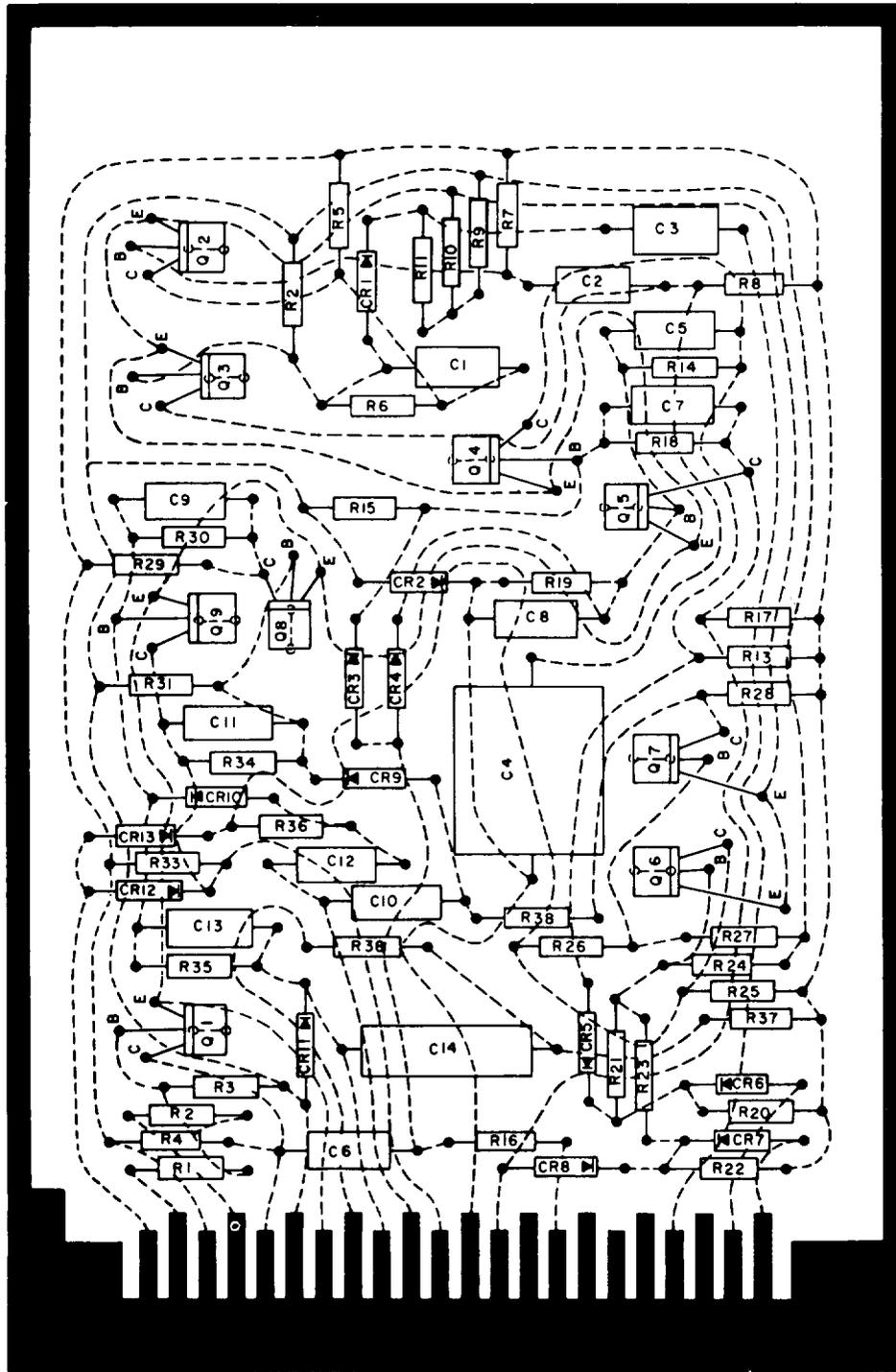
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Figure 2-8. Printed circuit card assembly 1A2A6 (80047010), component locations.



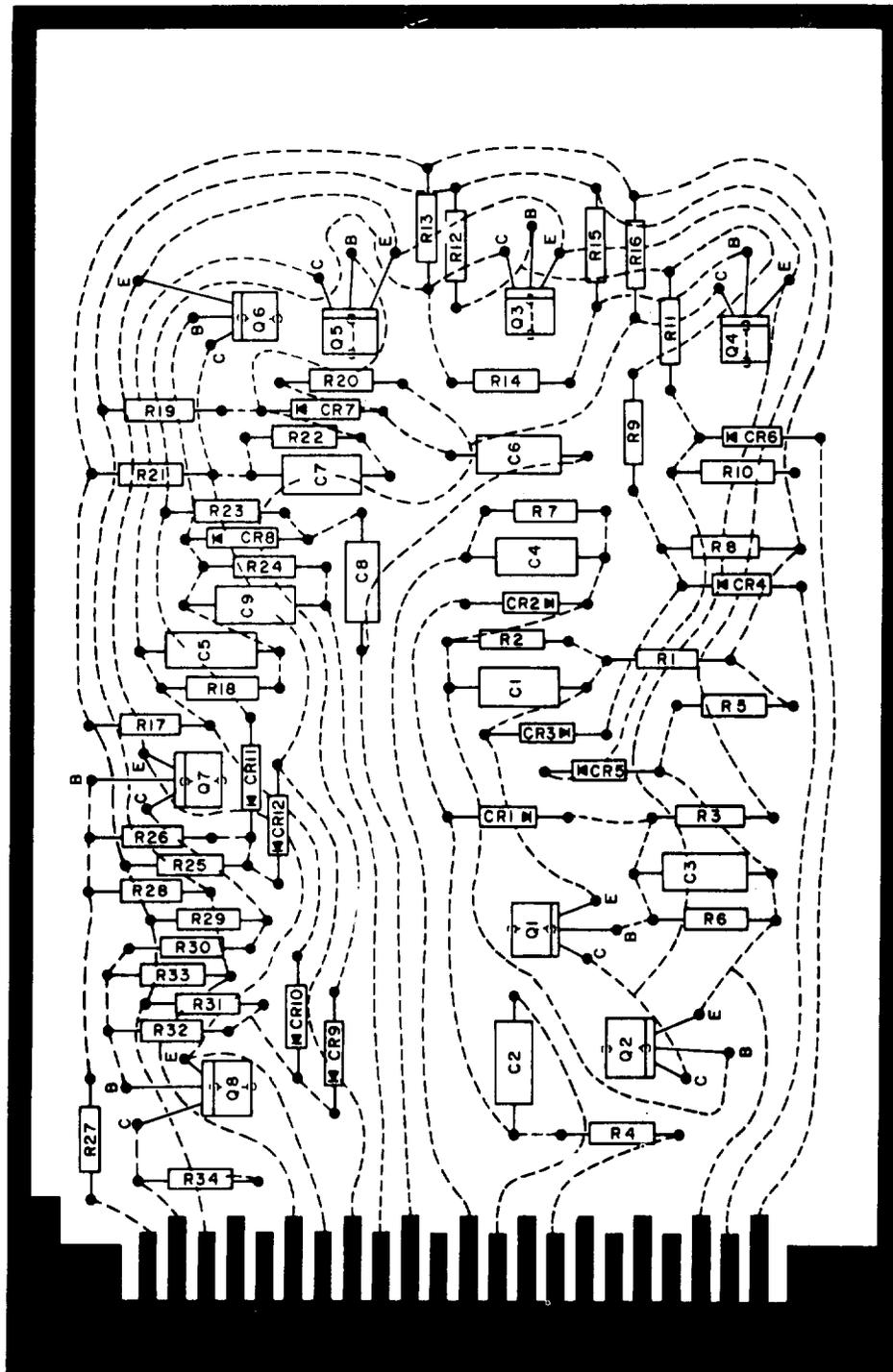
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Figure 2-9. Printed circuit card assembly 1A2A15 (80047080), component locations.



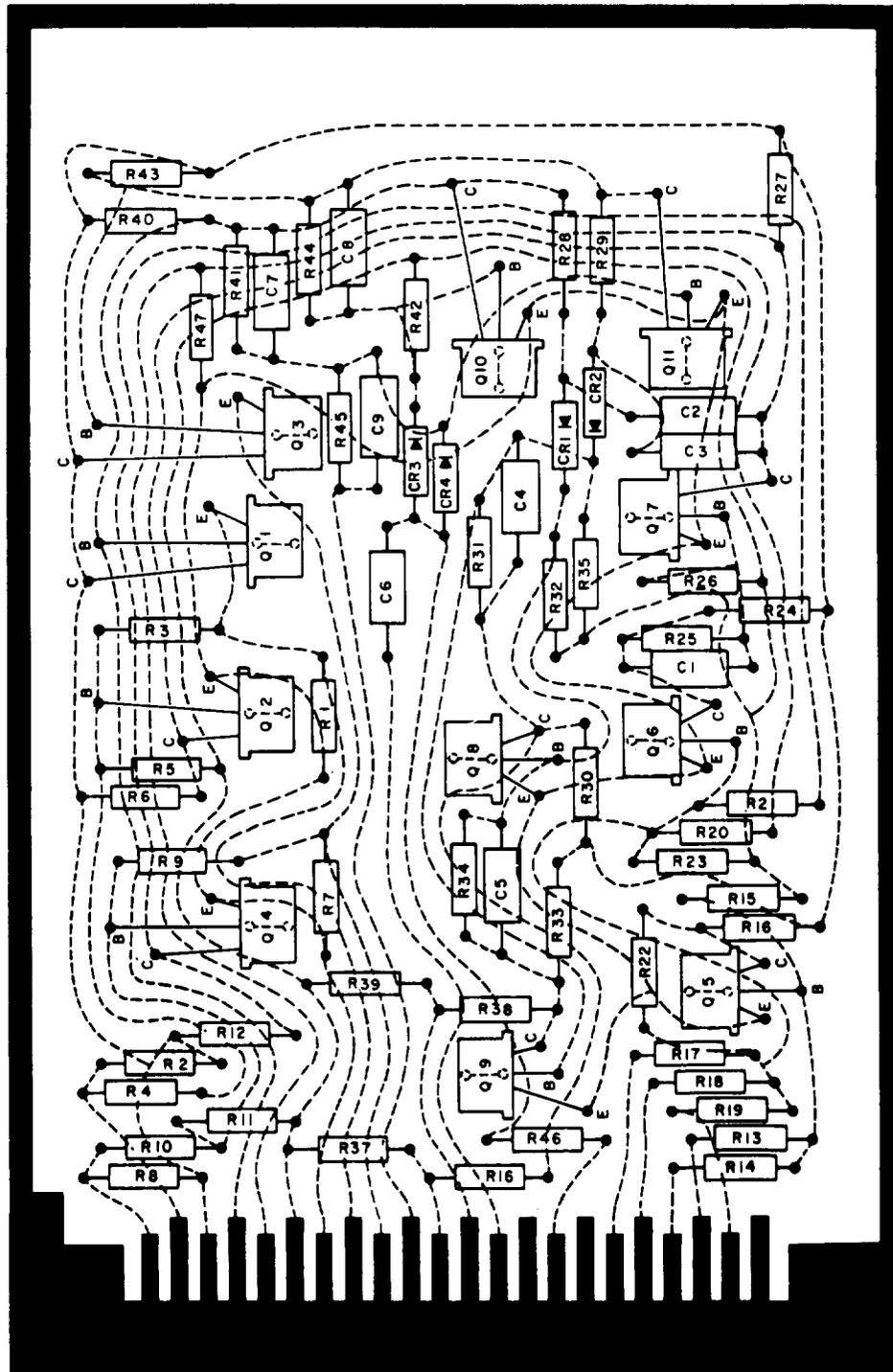
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Figure 2-10. Printed circuit card assembly 1A2A8 (80047040), component locations.



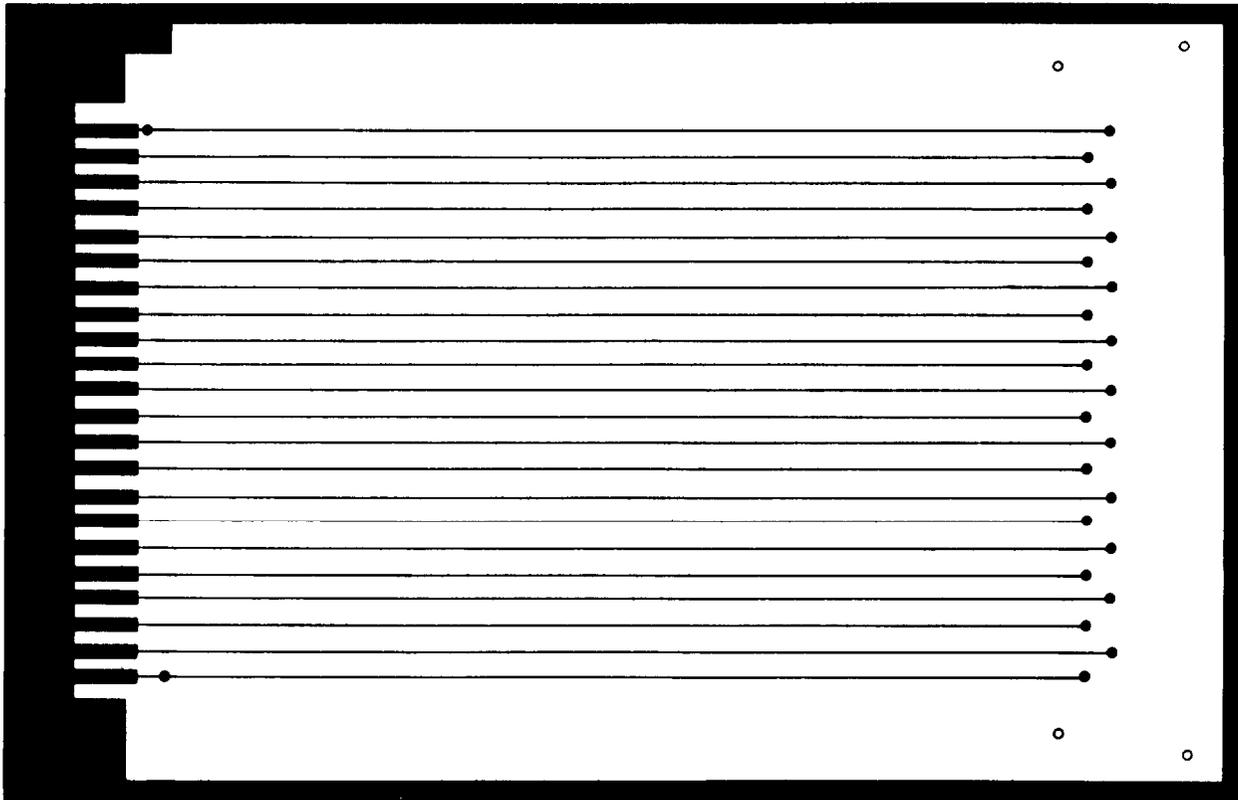
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Figure 2-11. Printed circuit card assembly 1A2A9-1A2A13 (80047030), component locations.



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Figure 2-12. Printed circuit card assembly 1A2A14 (80047070), component locations.



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Figure 2-13. Printed circuit card assembly 1A2A7 (80047130), component locations.

- (3) Intermittent troubles. If intermittent troubles exist, the trouble may often be made to reappear by gently tapping or jarring the equipment. Also check all wiring (fig. 6-13) and connections to the equipment.

b. Monostable Multivibrator Stages SSA- and SSB-.

- (1) *SSA-* (A, figs. 1-2, 2-7, and 6-4).

(a) Short the base to the emitter of Qa, and then measure the collector voltage of Qa. The indication should be approximately -12.5 volts.

1. If the indication is +15 volts, check for an open Ra.
2. If the indication is -15 volts, check for an open Rd or Re.
3. If the indication is zero, check for a shorted Qa.

(b) Measure the collector voltage of Qb. If the indication is -15 volts, check for an open Qb or Rd.

(c) Remove the short between the base and emitter of Qa and short the base to emitter of Qb.

(d) Measure the collector voltage of Qb. If the indication is zero, check for a shorted Qb.

(e) Remove the short between the base and emitter of Qb, and short the collector to base of Qa.

(f) Measure the base voltage of Qb. If a positive indication is not obtained, check for a shorted Ca or open Re.

(g) Remove the short between the collector and base of Qa and short the collector to base of Qb.

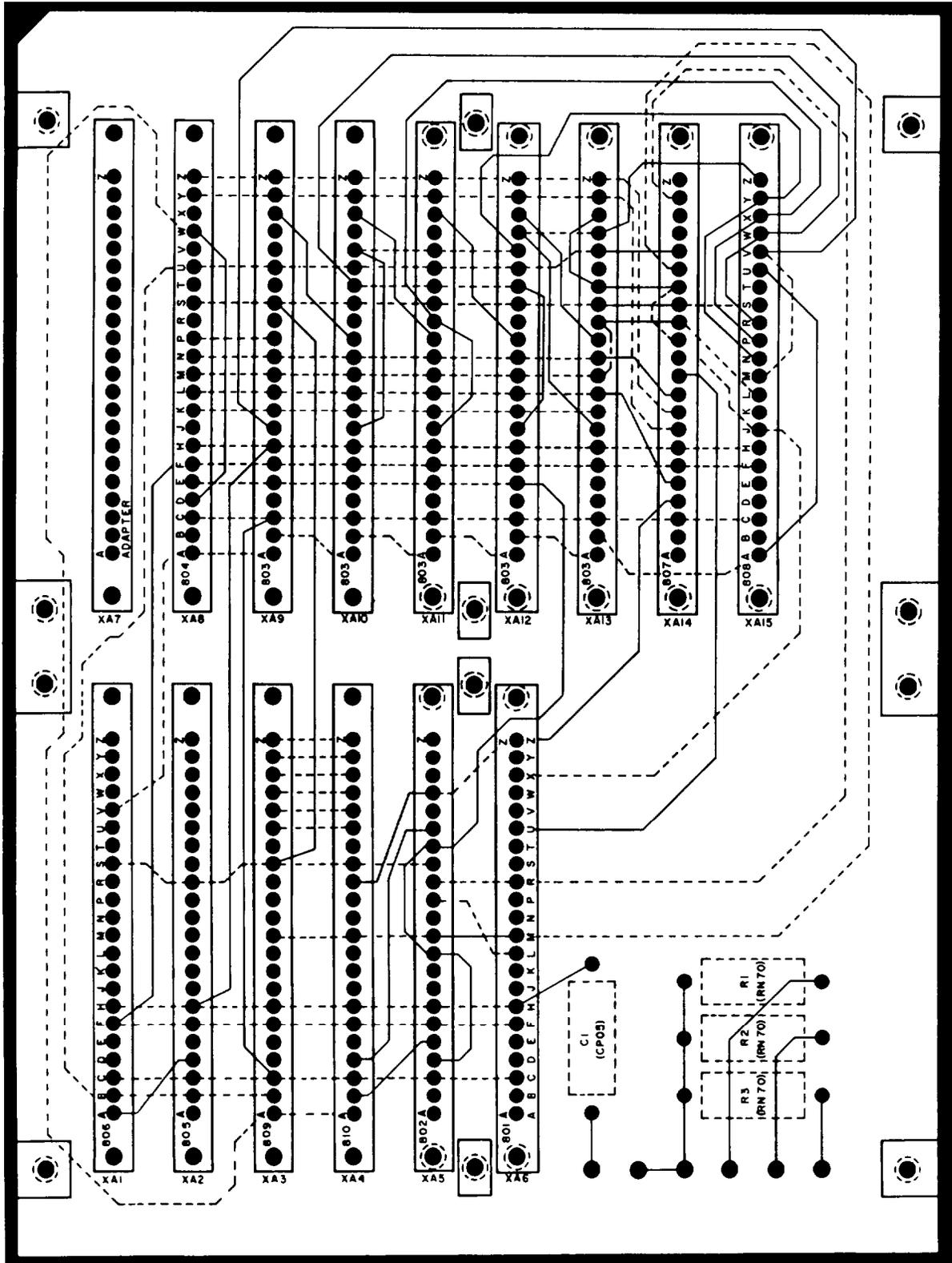
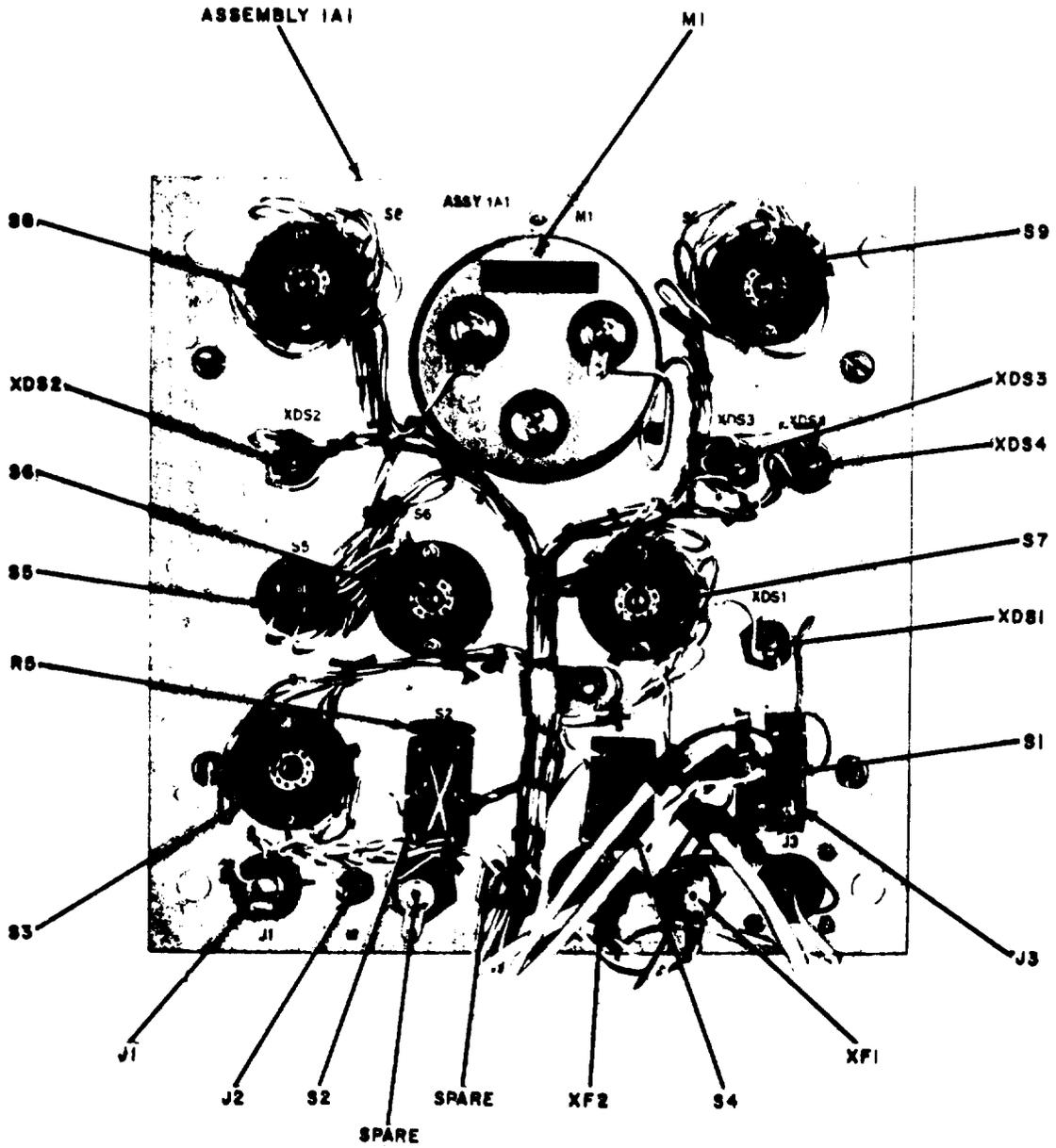


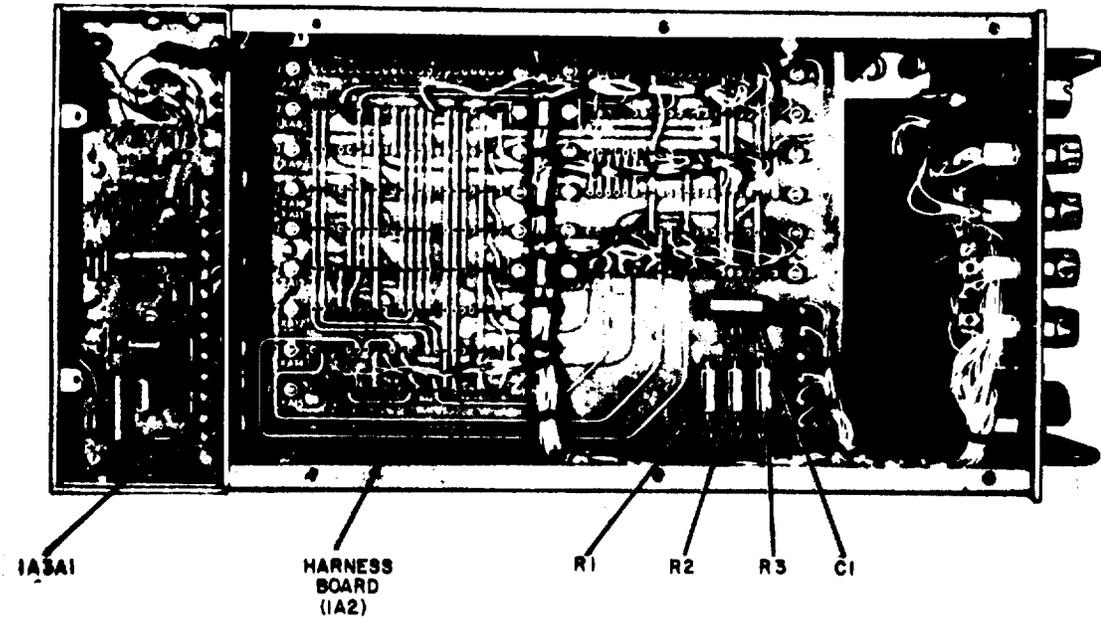
Figure 2-14. Harness board, component locations.

TM6625-620-45/2-50



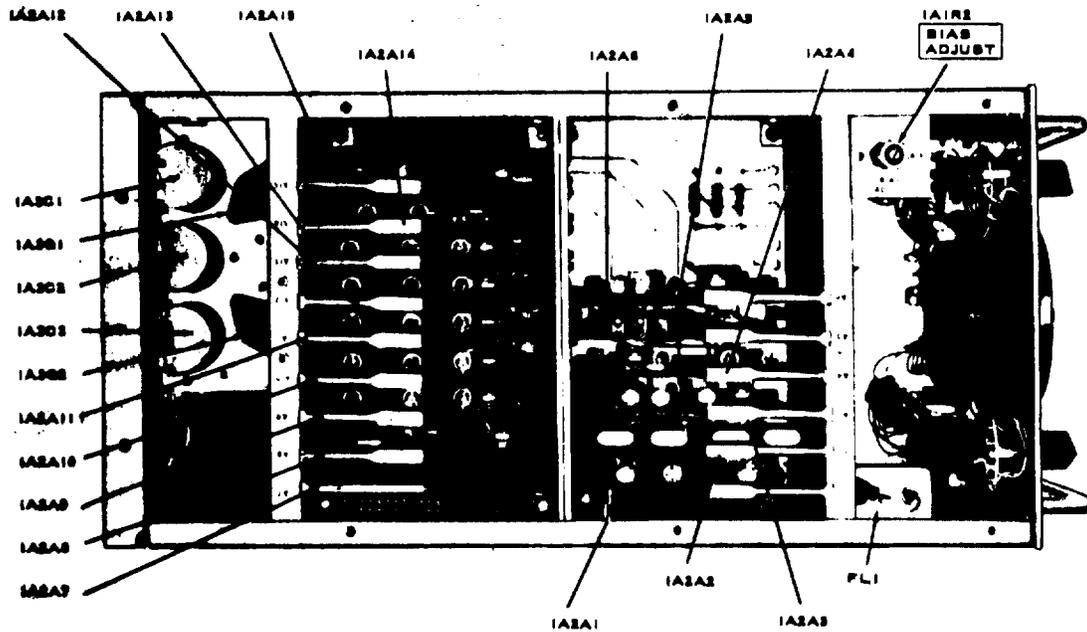
TM6625-620-45/2-48

Figure 2-15. Rear of front panel, component locations.



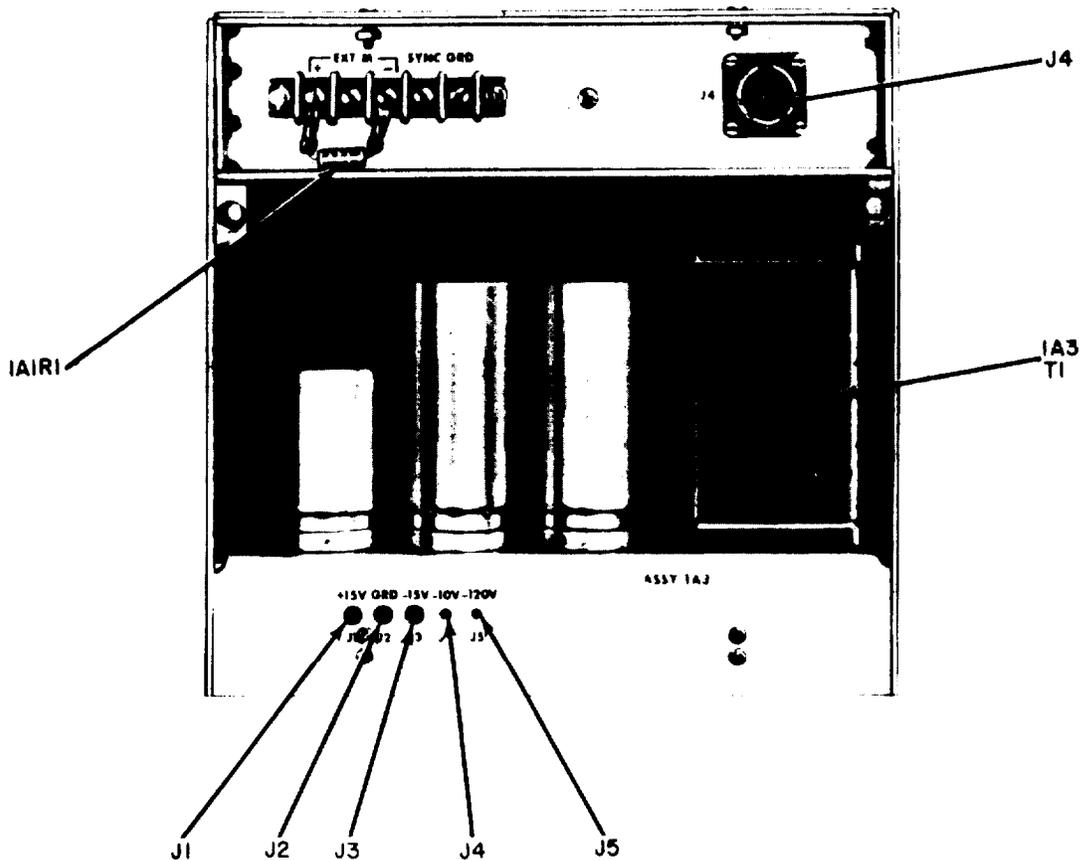
TM6625-620-45/2-44

Figure 2-16. Bottom view, component locations.



TM6625-620-45/2-45

Figure 2-17. Top view, component locations.



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Figure 2-18. Rear view, component locations.

- (h) Measure the base voltage of Qa. If a negative indication is not obtained, check for a shorted Cb.
- (i) Remove the short between the collector and base of Qb.
- (2) SSB- (B, figs. 1-2, 2-3, and 6-5).
 - (a) Short the base to the emitter of Qa, and then measure the collector voltage of Qa. The indication should be approximately -12.5 volts.
 - 1. If the indication is 0 volt, check for an open Rc or Rd or shorted Qa.
 - 2. If the indication is -15 volts, check for an open Ra.
 - (b) Measure the collector voltage of Qb. If the indication is -15 volts, check for an open Qb or Rb.
 - (c) Remove the short between the base and emitter of Qa and short the base to emitter of Qb.
 - (d) Measure the collector voltage of Qb. If the indication is zero, check for a shorted Qb or open Re.
 - (e) Remove the short between the base and emitter of Qb.
 - (f) Measure the base voltage of Qb. If the indication is not positive, check for an open Rd.
 - (g) Measure the base voltage of Qb. If the indication is not negative, check

for an open resistor RD or defective Ca

c. *Bistable Multivibrator Stages FFA-* (fig. 6-4), *FFC-* (figs. 6-5 and 6-6), and *FFS-* (figs. 1-2 and 6-9). The bistable multivibrator stages shown in A and B, figure 1-1, are identical except for the arrangement of the steering and triggering circuits. Only the stage shown in A is discussed below, because the procedures apply to each type of stage.

- (1) Remove printed circuit card assembly 1A2A2 (fig. 2-17) (80047050) to remove input timing signal.
- (2) Short the base to the emitter of Qa, and then measure the collector voltage. The indication should be approximately 7 volts.
 - (a) If the indication is +15 volts, check for an open Ra.
 - (b) If the indication is -15 volts, check for an open Rc or Rf.
 - (c) If the indication is zero, check for shorted Qa or Ca.
- (3) Remove the short between the base and emitter of Qa, short the base to emitter of Qb, and measure the collector voltage of Qb. The indication should be 7 volts.
 - (a) If the indication is +15 volts, check for an open Rb.

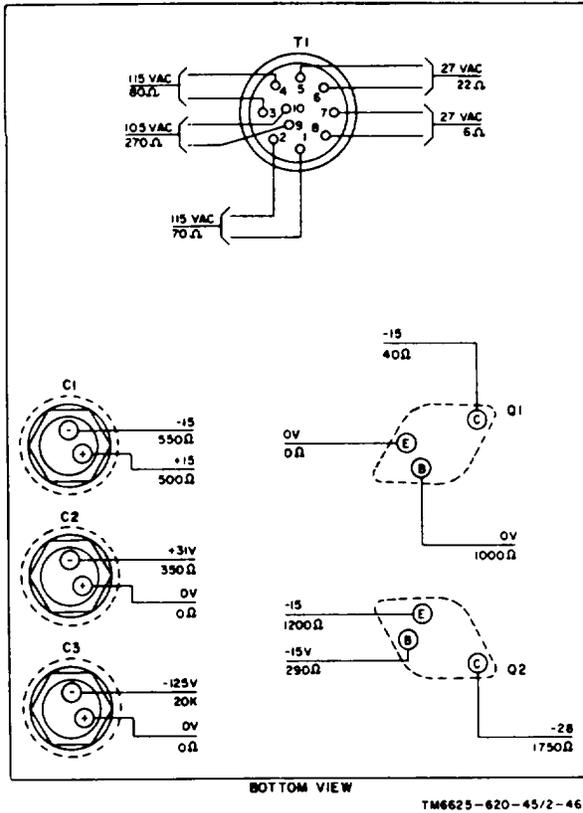


Figure 2-19. Power supply assembly 1A3, voltage and resistance diagram.

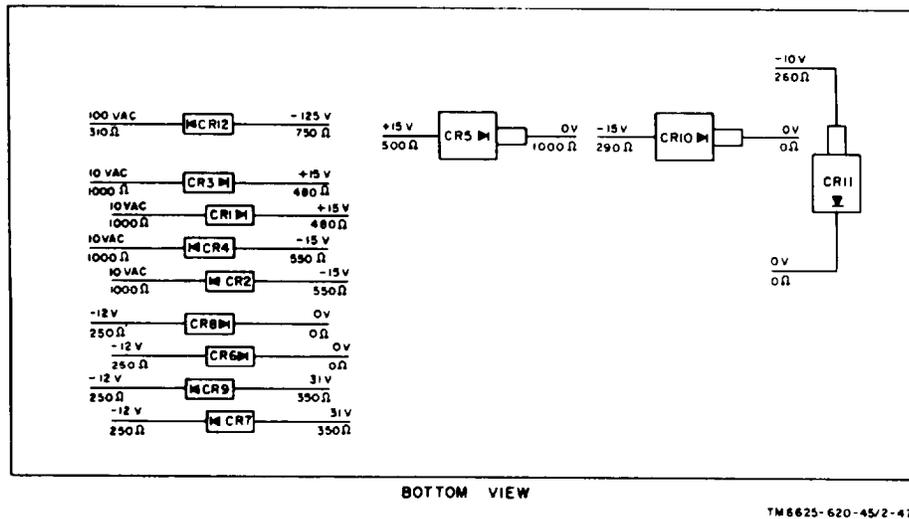


Figure 2-20. Printed circuit card assembly 1A3A1, voltage and resistance diagram.

- (b) If the indication is -15 volts, check for an open Rd or Re.
 - (c) If the indication is zero, check for a shorted Qb or Cb.
 - (4) Remove the short between the base and emitter of Qb and short the collector to emitter of Qa.
 - (5) Measure the base voltage of Qb. If a positive indication is not obtained, check for an open Rf.
 - (6) Remove the short between the collector and emitter of Qa and short the collector to emitter of Qb.
 - (7) Measure the base voltage of Qa. If a positive indication is not obtained, check for an open Re.
 - (8) Remove the short between the collector and emitter of Qb.
 - (9) If the indications given in (1) through (8) above are correct, but the bistable multivibrator stage does not function properly, set the distortion analyzer POWER switch to OFF and check the steering diodes as follows:
 - (a) Disconnect one side of the steering diode to be checked (CRa or CRb).
 - (b) Measure the forward and reverse resistance of the steering diode. The forward resistance should be from 1 to 10 ohms. The reverse resistance should be approximately 100 times the forward resistance,
- d. Schmitt Trigger STA-* (figs. 1-2, 2-7, 2-8, 2-18, and 6-4).
- (1) Set the pattern generator POWER switch to OFF,
 - (2) Measure the Qc collector voltage, If the indication is not approximately zero, check for an open Qc, Re, Rf, or Rg.
 - (3) Measure the Qb collector voltage, If the indication is not slightly positive, check for an open Rb, shorted Qb, or shorted Ca.
 - (4) Connect a test lead from the input side of Ra to -15V jack J3 on the distortion analyzer power supply.
 - (5) Measure the Qb collector voltage, If the indication is not approximately zero, check for an open Ra or Rd, defective Qa, or shorted Ca.
 - (6) Measure the Qc base voltage, If a positive indication is not obtained, check for an open Rh.
 - (7) Measure the Qc collector voltage. If a positive indication is not obtained, check for an open Rc.
 - (8) Disconnect the test lead from the input side of Ra and -15V jack J3.
- e. AND Gate GAS-, GAT-, GAD-, or GAI-* (fig. 1-4). Before troubleshooting AND gate stages, remove printed circuit card assembly 1A2A2 (fig. 2-17).
- (1) *AND gate GAS-* (A, fig. 1-4).
 - (a) Use the oscilloscope to check the waveform at the junction of Ra, Ca, and CRa. If a differentiated waveform is not observed, check for a shorted Ca or an open Ra.
 - (b) Check the waveform present at the output side of CRa. If a differentiated waveform with negative spikes is present, check for a shorted CRa. If no waveform is present, check for an open CRa.
 - (2) *AND gate GAT-* (B, figs. 1-4 and 2-7).
 - (a) Connect a test lead between the input side of CRa and GRD jack J2 on the distortion analyzer power supply,
 - (b) Connect a test lead between the input side of Ca and -15V jack J3 on the distortion analyzer power supply.
 - (c) Measure the voltages at the junction of CRa, Ra, and Ca. If a 0-volt indication is not obtained, check for an open CRa.
 - (d) Disconnect the test lead from -15V jack J3 on the distortion analyzer power supply. Disconnect the test lead from GRD jack J2 and connect it to -15V jack J3 on the distortion analyzer power supply.
 - (e) Use the oscilloscope to check the waveform present at the junction of Ra, Ca, and CRa, while alternately connecting the test lead from the

- input side of Ca to -15V jack J3 and the GRD jack J2 on the distortion analyzer power supply.
- (f) If a differentiated waveform is not observed, check for a shorted Ca or an open Ra. If a -15-volt indication is observed, check for a shorted CRa.
- (g) Disconnect the test leads from the input sides of CRa and Ca, and from -15V jack J3 and GRD jack J2 on the distortion analyzer power supply.
- (8) *AND gate GAD-* (C, figs. 1-4 and 6-6).
- (a) Connect a test lead between the input side of CRa and GRD jack J2 on the distortion analyzer power supply.
- (b) Short the input sides of CRa and CRb and measure the voltage on the output sides (junction of CRa and CRb). The indication should be approximately zero.
- (c) Remove the short from the input sides of CRa and CRb and connect a test lead between the input side of CRb and -15V jack J3 on the distortion analyzer power supply.
- (d) Measure the voltage at the junction of diodes CRa and CRb. If a -15-volt indication is obtained, check for an open CRa or shorted CRb.
- (e) Reverse the test lead connections on the GRD J2 and -15V J3 jacks on the distortion analyzer power supply.
- (f) Measure the voltage at the junction of CRa and CRb. If a -15-volt indication is obtained, check for an open CRb or a shorted CRa.
- (g) Disconnect the lead from GRD jack J2 on the distortion analyzer power supply.
- (h) Short the input sides of CRa and CRb and measure the voltage at the output sides (junction of CRa and CRb). If the indication is not -15 volts, check for an open Ra.
- (i) Disconnect the short from the input sides of CRa and CRb and the test lead from -15V jack J3 on the distortion analyzer power supply.
- (4) *AND gate GAI- with inhibit voltage* (D, fig. 1-4).
- (a) Short the input sides of Ra and Rb and connect a test lead between the input side of Ra and GRD jack J2 on the distortion analyzer power supply,
- (b) Measure the Qa collector voltage. If a zero indication is not obtained, check for an open Re, Rd, or Rc.
- (c) Disconnect the test lead from GRD jack J2 on the distortion analyzer power supply.
- (d) Connect a test lead between the input side of Ra or Rb and -15V jack J3 on the distortion analyzer power supply, and connect a test lead between the input side of Rc and the GRD jack.
- (e) Measure the Qa collector voltage. If a *zero* indication is not obtained, check for an open Ra, Rb, or Qa.
- (f) Disconnect the test lead from -15V jack J3 on the distortion analyzer power supply, and short Ra and Rb to Rc.
- (g) Measure the Qa collector voltage. If a -15-volt indication is not obtained, check for an open Rf or shorted Qa.
- (h) Remove the short between the input sides of Ra through Rc and disconnect the test lead from GRD jack J2.
- f. OR Gates GOB- and GOI-* (fig. 1-5). Before troubleshooting OR gate stages GOB- and GOI- ((1) and (2) below), remove printed circuit card assembly 1A2A2 (fig. 2-16).
- (1) *OR gate GOB-* (A, fig. 1-5 and 6-7).
- (a) Short the input sides of CRa and CRb, and connect a test lead between the input side of CRa and -15V jack J3 on the distortion analyzer power supply.
- (b) Measure the voltage at the junction of CRa, CRb, and Ra. If a -15-volt indication is not obtained, check for an open Ra.

- (c) Disconnect the test lead from -15V jack J3 on the distortion analyzer power supply and connect it to GRD jack J2, and then remove the short from the input sides of CRa and CRb.
 - (d) Connect a test lead from the input side of CRb and -15V jack J3 on the distortion analyzer power supply.
 - (e) Measure the voltage at the junction of CRa, CRb, and Ra. If a zero indication is not obtained, check for an open CRa or shorted CRb.
 - (f) Reverse the test lead connections at the GRD J2 and -15V J3 jacks on the distortion analyzer power supply.
 - (g) Measure the voltage at the junction of CRa, CRb, and Ra. If a zero indication is not obtained, check for an open CRb or shorted CRa.
 - (h) Disconnect the test leads from the input sides of CRa and CRb, and from the GRD J2 and -15V J3 jacks on the distortion analyzer power supply.
- (2) *OR gate GOI-* (B, figs. 1-5 and 6-6).
- (a) Short the input sides of Ra and Rb, and connect a test lead from the input side of Ra to the GRD jack on the distortion analyzer power supply.
 - (b) Measure the Qa collector voltage. If a -15-volt indication is not obtained, check for an open Rd or shorted Qa.
 - (c) Remove the short from the input sides of Ra and Rb.
 - (d) Disconnect the test lead from the GRD jack on the distortion analyzer power supply and connect it to -15V jack J3.
 - (e) Measure the collector voltage of Qa. If a zero indication is not obtained, check for an open Ra or Rc.
 - (f) Disconnect the test lead from the input side of Ra and connect it to the input side of Rb.
 - (g) Measure the Qa collector voltage. If a zero indication is not obtained, check for an open Rb.
- (h) Disconnect the test lead from the input side of Rb and -15V jack J3 on the distortion analyzer power supply.
- g. *Inverter Stage IN- and Emitter Follower EF-* (figs. 1-7 and 6-6).
- (1) *Inverter IN-* (A, fig. 1-6).
- (a) Remove printed circuit card 1A2A2 (fig. 2-17) from the distortion analyzer.
 - (b) Short the base to emitter of Qa, and then measure the collector voltage. If a -15-volt indication is not obtained, check for an open Rc or shorted Qa.
 - (c) Remove the short between the base and emitter of Qa and connect a test lead between the input side of Ra and -15V jack J3 on the distortion analyzer power supply.
 - (d) Measure the Qa collector voltage. If a zero indication is not obtained, check for an open Ra or a shorted Rb.
 - (e) Disconnect the test lead from the input side of Ra and -15V jack J3 on the distortion analyzer power supply.
- (2) *Emitter follower EF-* (B, fig. 1-6).
- (a) Connect a test lead between the base of Qa and GRD jack J2 on the distortion analyzer power supply.
 - (b) Measure the Qa emitter voltage. If a zero indication is not obtained, check for a shorted transistor Qa.
 - (c) Disconnect the test lead from GRD jack J2 on the distortion analyzer power supply, and connect it to -15V jack J3.
 - (d) Measure the Qa emitter voltage. If a -15-volt indication is not obtained, check for an open Ra.
 - (e) Disconnect the test lead from the base of Qa and -15V jack J3 on the distortion analyzer power supply.
- h. *Digital-to-Analog Converter Stage CCG-* (A, fig. 1-7). When trouble is localized to a digital-to-analog converter stage, check Ra or Rb and Qa.

i. Current Summer CSN- (B, fig. 1-7).

- (1) Before troubleshooting current summer, remove printed circuit assembly 1A2A2 (fig. 2-16) from the distortion analyzer.
- (2) Measure the Qa base voltage, If a + 10-volt indication is not obtained, check for an open Ra or Rb.
- (3) Connect a test lead to GRD jack J2 on the distortion analyzer power supply and touch the other end of the test lead to the bases of 1A2A15Q1 through 1A2A15Q6, one at a time.
- (4) Measure the Qa collector voltage. A positive indication should be obtained. If a zero indication is obtained, check for an open Rc or Rd.
- (5) Disconnect the test lead from GRD jack J2 on the distortion analyzer power supply.

j. Power Supply (figs. 2-19, 2-20, and 6-0).

0). Troubleshoot the power supply as follows:

- (1) Check for +15 volts at + 15V jack J1 (fig. 2-18). If voltage is correct, proceed to (2) below. If voltage is incorrect, proceed as follows:
 - (a) Check continuity of secondary winding of transformer T1 at terminals 5 and 6 (fig. 2-19); replace if defective.
 - (b) Take voltage and resistance measurements of CR1, CR2, CR3, and CR4 (fig. 2-2); replace if defective.
 - (c) Take voltage and resistance measurements (fig. 6-10) of + 15-volt regulator circuit. Check C1 and Q1 on the chassis (fig. 2-19).
 - (d) Check resistance of R5 (fig. 2-2); replace if defective.
- (2) Check for -15 volts at test jack J3 (fig 2-17). If voltage is correct, proceed to (3) below. If voltage is incorrect, proceed as follows:
 - (a) Check continuity of secondary winding of T1 at terminals 7 and 8 (fig. 2-19); replace if defective.
 - (b) Take resistance measurements of surements of CR5, CR6, CR7, and CR8 (fig. 2-2); replace if defective.

(c) Take voltage and resistance measurements of -15-volt regulator circuit (fig. 6-10). Check C2 and Q2 on the chassis (fig. 2-2).

(d) Take resistance measurements of R10 (fig. 2-2); replace if defective.

(3) Check for -10 volts at -10V jack J4 (fig. 2-18). If voltage is correct, proceed to (4) below. If voltage is incorrect, proceed as follows:

(a) Take resistance measurements of CR11 (fig. 2-2); replace if defective.

(b) Take resistance measurements of R9 R9 and R11 (fig. 2-2); replace if defective.

(4) Check for -120 volts at -120V jack J5 (fig. 2-18). If voltage is incorrect, proceed as follows:

(a) Check continuity of secondary winding of T1 at terminals 9 and 10 (fig. 2-18); replace if defective.

(b) Take resistance measurements of CR12 (fig. 2-2); replace if defective.

(c) Take resistance measurements of R12 (fig. 2-2); replace if defective.

(d) Take resistance measurements of C3 (fig. 2-19) on the chassis.

(e) Take resistance measurements of R13 (fig. 2-2); replace if defective.

(f) Take resistance measurements of R14 (fig. 2-2); replace if defective.

k. Oscillator Stage OSC- (figs. 2-4 and 6-5). When trouble is localized to an oscillator stage, check the crystal, transistors, and other associated components (fig. 2-4).

2-9. General Parts Replacement Techniques

All the parts in the distortion analyzer can be reached and replaced without special procedures. However, the following precautions apply to all printed circuit cards:

a. The distortion analyzer is transistorized. Use a pencil-type soldering iron with a 25-watt maximum capacity. If the soldering iron must be used with alternating current, use an isolating transformer between the soldering iron and the line. Do *not* use a soldering gun; damaging voltages can be induced in components.

b. When soldering transistor or diode leads, solder quickly; wherever wiring permits, use a heat sink (such as long-nose pliers) between the joint to be soldered (or unsoldered) and the transistor or diode. Use approximately the same length and dress of transistor and component leads as used originally.

c. Before making repairs on printed cards, refer to TB SIG 222.

d. If the settings of variable resistors are disturbed, or if variable resistors are replaced, perform the adjustment procedures described in chapter 3.

CHAPTER 3

ADJUSTMENT PROCEDURES

3-1. Tools, Materials, and Test Equipment Required

- a. Tool Kit, Electronic Equipment TK-105/G.
- b. Multimeter TS-352B/U.
- c. Test Set, Teletypewriter TS-799/UGM-1.
- d. Oscilloscope AN/USM-81.
- e. 0.2-microfarad (μf) capacitor (2 each).

3-2. Adjustment of Schmitt Triggers STA-1 and STA-2
(figs. 3-1 and 4-5)

Adjust the Schmitt trigger circuits as follows:

- a. Connect the pattern generator signal output to the distortion analyzer input. Connect a 0.2- μf capacitor across the distortion analyzer input. Connect the oscilloscope to the collector of Q6 on 1A2A6 (fig. 2-8). Connect another 0.2- μf capacitor from the collector of Q6 to power supply ground. Adjust the oscilloscope for a crossover pattern.

Note. A crossover pattern is obtained by setting the oscilloscope sweep generator to twice the frequency of the input signal. Expand the sweep as required to observe the crossover.

- b. Set the pattern generator controls as follows:

Control	Position
CURRENT SELECT switch	30 POLAR
MESSAGE SELECT switch	DOT CY
RATE switch	75
DISTORT SELECT switch	OFF
POWER switch	115V ON
% DISTORT control	N/A
MESSAGE TRANSMIT switch	ON

- c. Set the distortion analyzer controls as follows:

Control	Position
RATE switch	75
CURRENT SELECT switch	30 POLAR

Control	Position
F I L T E R	OUT
DISTORTION SELECT switch	N/A
TRANSITION SELECT switch	N/A
POWER switch	ON 115V

- d. Adjust 1A2A6R8 (fig. 3-1) to control the dc level of the trigger point and 1A2A6R11 to control the hysteresis of the output of the Schmitt trigger. Adjust the two resistors until the crossover occurs at the 0-volt level.

- e. Set the FILTER switch to IN. Connect the oscilloscope to the junction of R1 and R5 on 1A2A6 (fig. 2-8). Adjust 1A2A5R4 (fig. 3-1) to center the signal on the 0-volt (ground) level.

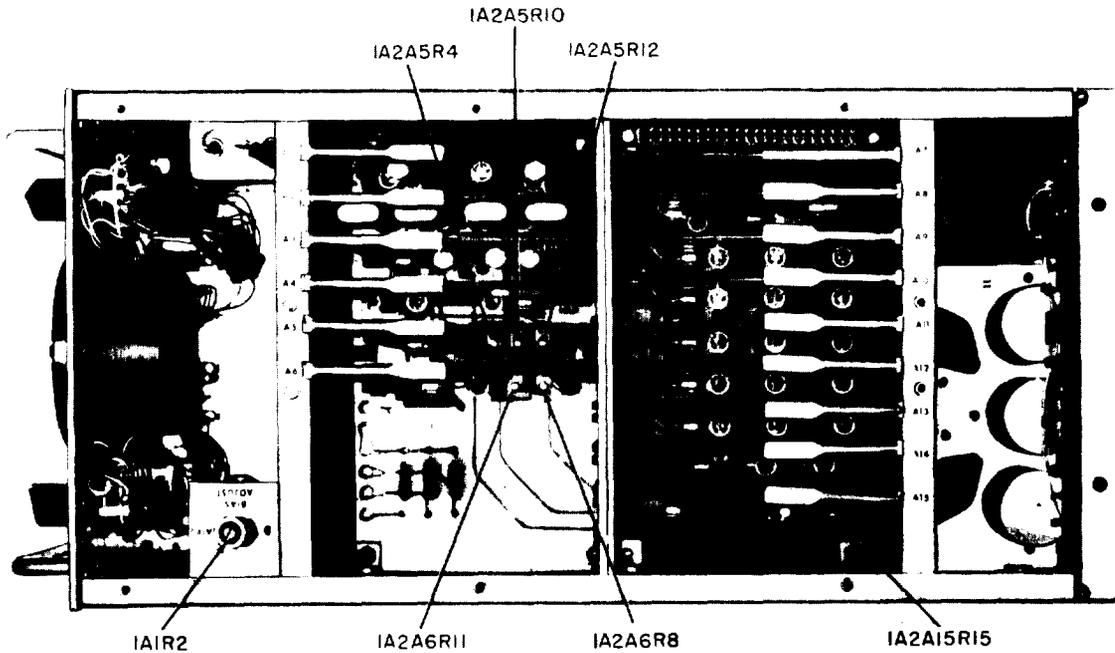
- f. Connect the oscilloscope to the collector of Q3 on 1A2A6 (fig. 2-8). Disconnect the 0.2- μf capacitor from the collector of Q6 and connect it between the collector of Q3 and chassis. Adjust 1A2A5R10 and 1A2A5R12 (fig. 3-1) as described in d above.

3-3. Adjustment of BIAS ADJUST control 1A1R2

(fig. 2-17)

Note. The following procedure assumes that the Schmitt triggers (STA-1 and STA-2, para 3-2) have been adjusted.

Set up the pattern generator and distortion analyzer as directed in paragraph 3-2. Set the pattern generator CURRENT SELECT switch to 20. Set the distortion analyzer DISTORTION SELECT switch to PEAK TOTAL. Adjust BIAS ADJUST control 1A1R2 (fig. 3-1) for zero indication on the PERCENT DISTORTION meter.



TM6625-620-45/2-43

Figure 3-1. Adjustment locations.

**3 - 4 Adjustment of Meter Adjust Screw
1A2A15R15**

a. Connect the distortion analyzer to an ac power source and set the controls as indicated in paragraphs 3-2 and 3-3. (Do not apply an input signal.) Remove assembly 1A2A15 and insert extender card assembly 1A2A7 into its place. Insert assembly 1A2A15 into the extender card.

b. Depress the distortion analyzer RESET switch, and then momentarily connect a lead between power supply ground and the base of transistor 1A2A15Q6 (fig. 2-9). Adjust 1A2A15R15 for a 25-percent indication on the PERCENT DISTORTION meter. Momentarily connect a lead from power supply ground to the base of each transistor 1A2A15Q1 through 1A2A15Q5. Note the meter indication (49.2 percent nominal). Adjust 1A2A15R 15 to halve the error between the 25-percent and 49.2-percent indications.

CHAPTER 4

GENERAL SUPPORT TESTING PROCEDURES

4-1. General

a. These testing procedures are prepared for use by Signal Field Maintenance Shops and Signal Service Organizations responsible for general support maintenance of electronic equipment to determine the acceptability of repaired equipment. These procedures set forth specific requirements that repaired electronic equipment must meet before it is returned to the using organization. A summary of the performance standards is given in paragraph 4-9.

b. Each test depends on the preceding one for certain operating procedures and, where applicable, for test equipment calibration. Comply with the instructions preceding the body of each chart before proceeding to the chart. Perform each step and each test in sequence. Do not vary the sequence. For each step in a test, perform all actions required in the *Control settings* columns, and then perform each specific test and verify the results against the appropriate performance standard.

Warning: Voltages up to 230 volts exist on some terminals of this equipment. Serious injury or death may result from contact with these terminals.

c. When performing tests, do not set the TS-799/UGM-1 and TS-800/UGM-1 POWER switches to ON until after all connections have been made. Set the POWER switches to OFF before disconnecting or changing any connections. Return switches to ON when ready to make measurement.

d. When directions for setting controls are not given in either *Control settings* column, the controls may be set to any position. However, if the control had been set to a particular position in a previous step, do not change the control setting.

4-2. Test Equipment, Tools, and Materials

Test equipment, tools, materials, and other equipments required for the general support testing procedures (listed in the following paragraphs) are authorized under TA 11-17 and TA 11-100 (11-17).

Note. Specific models and types of test equipment were used to perform the general support testing procedures. If these testing procedures are followed using other models or types of test equipment, test results may differ from those given in the procedures.

a. *Test Equipment.* The following is a list of the test equipment required for general support testing procedures:

Nomenclature	National stock number	Technical manual
Multimeter TS-352B/U	6625-00-553-0142	TM 11-6625-366-15
Test Set, Teletypewriter TS-799/UGM-1.	6625-00-965-0196	TM 11-6625-620-45-1

b. *Tools and Materials.*

Tools and Materials	National Stock No.
Tool Kit, Electronic Equipment TK-105G	5180-00-610-8177
Wire, hookup, insulated, No. 18 AWG (30 ft.)	—
Plug, Phone PJ-055B, (2)	—
Cable, Power C5471079	5995-00-941-2359

depot maintenance activity according to current BILI directions. Use this cable instead of the one supplied. During the procedures that follow, this will serve as a suitable electrical check of this cable. If not furnished, use the cable supplied with the equipment.

b. An ac power-source is required that will provide 115 or 230 volts at 50-400 Hz. There are no special procedures for connecting the unit to the power source.

4-3. Test Facilities

a. IF power cable C5471079 is furnished by the

4-4. Fabrication of Test Cable

Fabricate the test cable required for the distortion generation test as follows:

- a.* Cut two pieces of No. 18 AWG hookup wire, each 4 feet long.
- b.* Strip 1/2 inch of insulation from each end of each cable.
- c.* Connect the 4-foot wires to the two type PJ-055B plugs.

4-5. Modification Work Orders

The performance standards in the tests assume that no modification work orders (MWO's) have been performed on the equipment. If a modification work order is performed on the equipment an allowance must be made for any test connections or test results that may differ from those given in these test procedures.

4-6. Physical Tests and Inspection

- a. *Test Equipment and Materials.* None required.
- b. *Test Connections and Conditions.*
 - (1) No connections necessary.
 - (2) Remove TS-800/UGM-1 chassis from its transit case.
- c. *Procedure.*

Step No.	Test equipment	Control setting	Equipment under test	Test procedure	Performance standard
1	N/A		Controls may be in any position.	<p>a. Inspect front panel. Look for damaged, loose, or missing screw, knobs, or other parts.</p> <p>b. Inspect front panel and chassis (top and bottom). Look for cleanliness, signs of excessive wear or damage, loose or missing components and hardware.</p> <p>c. Inspect condition of finish. Look for rust, corrosion, and spots where bare metal is exposed.</p> <p><i>Note.</i> Touchup painting is recommended instead of refinishing. Screwheads and receptacles will not be polished with abrasives.</p> <p>d. Operate each switch and control on front panel. Look for smooth and positive operation.</p> <p>e. Inspect condition of jack and lamps. Look for cracks, broken parts, and condition of jack spring contacts.</p> <p>f. Inspect chassis; be sure printed circuit boards are in proper places.</p>	<p>a. No evidence of damaged, loose, or missing screws, knobs, or parts.</p> <p>b. Front panel and chassis are clean. No evidence of excessive wear, damage, or loose components or hardware.</p> <p>c. External surfaces intended to be painted do not show bare metal. Panel lettering is legible.</p> <p>d. Switches and controls operate smoothly with positive action to indicated positions.</p> <p>e. No evidence of cracks or broken parts. Jack contact springs are straight and show positive action in opening and closing.</p> <p>f. Printed circuit boards are in proper places and firmly seated.</p>

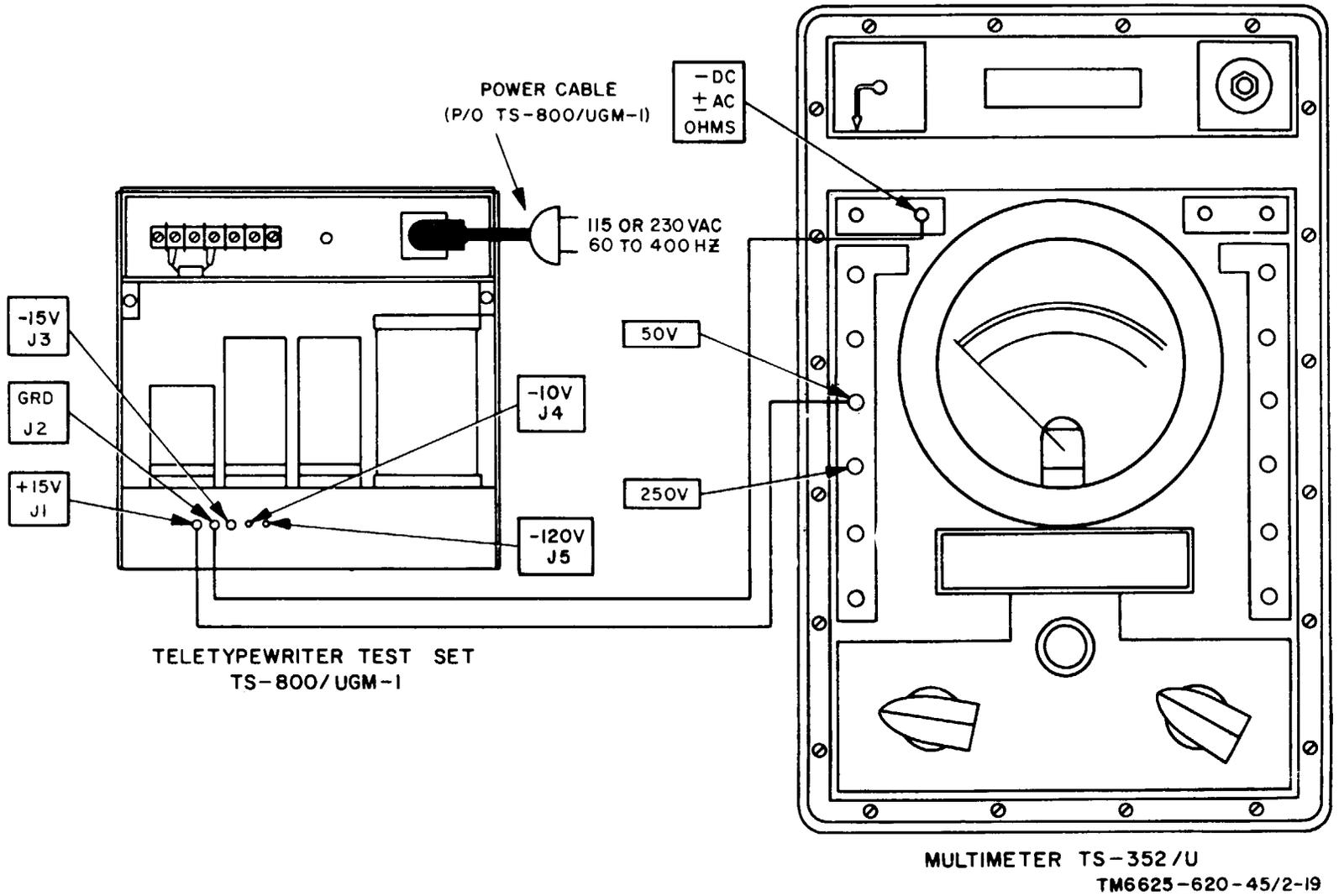


Figure 4-1. Power supply test setup.

4-7. Power Supply Test
(fig. 4-1)

a. Test Equipment. Multimeter TS-352B/U.

b. Test Connections and Conditions. Connect the equipment as shown in figure 4-1, and as indicated in the *c* below.

Step No.	Test equipment	Control setting	Equipment under test	Test procedure	Performance standard
1	TS-352/U				
	a. FUNCTION: DIRECT.		a. POWER: ON (115V or 230V, depending on the power source). All other controls may be in any position.	a. Observe the meter indication on the TS-352B/U; disconnect the red test lead from jack J1 on the TS-800/UGM-1.	a. The TS-352B/U should indicate 15 volts \pm 5%.
	b. FUNCTION: REV			b. Connect the red test lead to jack J3. Read negative voltage on the TS-352B/U; disconnect the red test lead from J3 and from 50V on the TS-352B/U.	b. The TS-352B/U should indicate 15 volts \pm 5%.
				c. Connect the red test lead to jack J5 on the TS-800/UGM-1, and to the 250V jack on the TS-352B/U. Observe meter indication on the TS-352B/U.	c. The TS-352/U should indicate 120 volts \pm 10%.
				d. Connect the red test lead to jack J4 on the TS-800/UGM-1 and to the 50V jack on the TS-352B/U. Observe the meter indication on the TS-352B/U.	d. The TS-352B/U should indicate 10 volts \pm 8%.

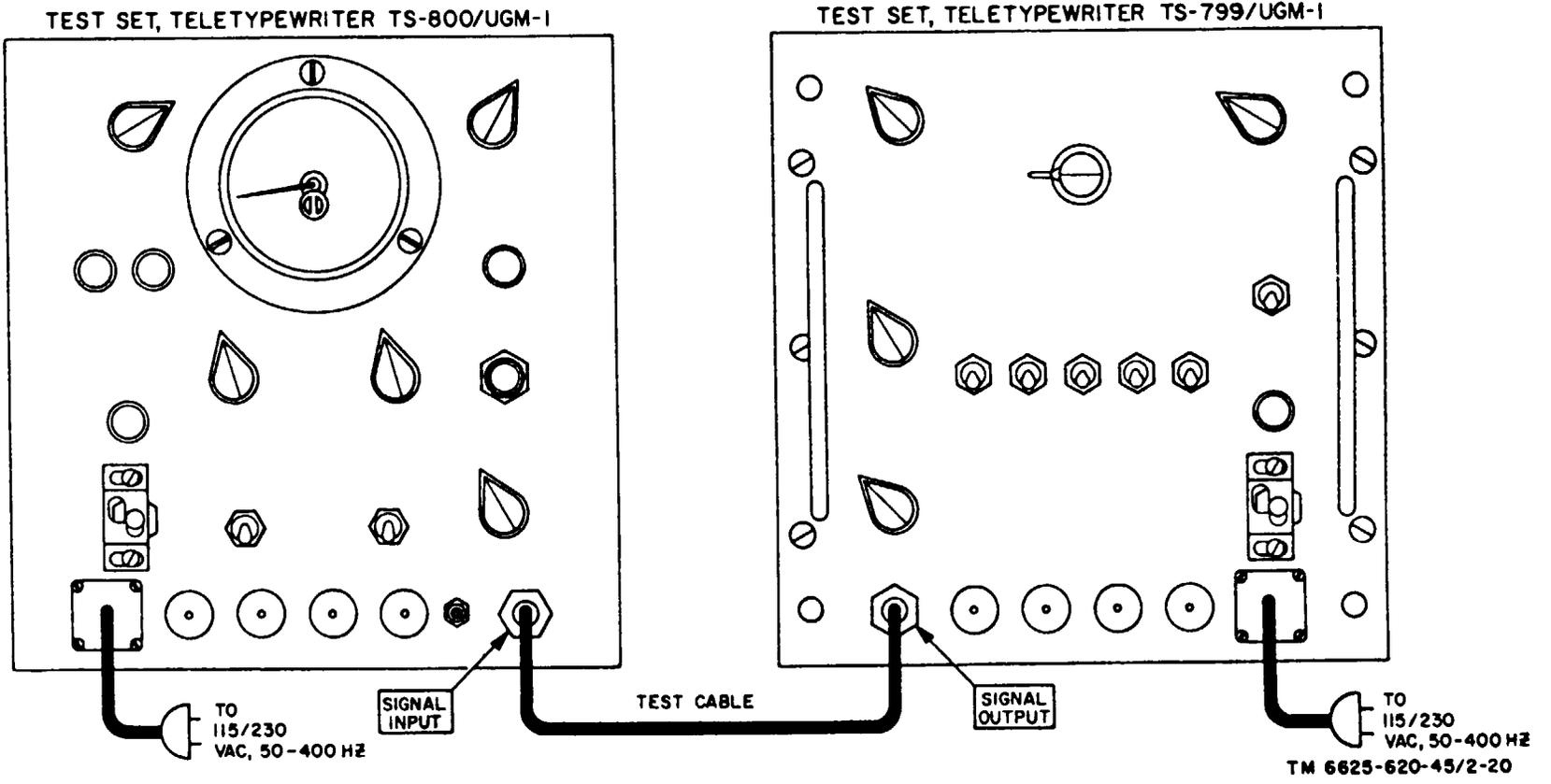


Figure 4-8. Distortion measurement test setup.

4-9. Summary of Performance Standards

Arrange a checklist similar to that shown below. In the *Test indication* column, record the actual indications obtained during the tests. These data can be used as checks against the performance standards the next time the test are performed.

a. Power Supply Test

Step	Performance standard	Test indication
1a	15 volts $\pm 5\%$	----volts
1b	15 volts $\pm 5\%$	----volts
1c	130 volts $\pm 5\%$	----volts

b. Distortion Measurement Test

Step	Performance standard	Test indication
1	SIGNAL lamp flasher	----yes----no
	LATE lamp lights.	----yes----no
	PERCENT DISTORTION meter follows control ($\pm 1\%$)	\pm ---- %
2	PERCENT DISTORTION meter indicates 0 distortion	----
3	EARLY lamp lights.	----yes----no
	PERCENT DISTORTION meter follows control ($\pm 1\%$)	+ ---- %
4	PERCENT DISTORTION meter indicates 0 distortion	----
5	EARLY lamp lights.	----yes----no
	PERCENT DISTORTION meter follows control ($\pm 1\%$)	\pm ---- %
6	PERCENT DISTORTION meter indicates 0	----
7	LATE lamp lights	----yes----no
	PERCENT DISTORTION meter follows control ($\pm 1\%$)	\pm ---- %

Step	Performance standard	Test indication
8	PERCENT DISTORTION meter indicates 0 distortion	----
9	PERCENT DISTORTION meter indicates 40 when control is dropped to 0	----
10	PERCENT DISTORTION meter follows control ($\pm 1\%$)	\pm ---- %
11	PERCENT DISTORTION meter follows control ($\pm 1\%$)	\pm ---- %
12a	PERCENT DISTORTION meter indicates 25.	----
12b	PERCENT DISTORTION meter indicates minimum (or maximum)	----
12c	PERCENT DISTORTION meter indication follows control	----yes----no
12d	PERCENT DISTORTION meter indication follows control	----yes----no
12e	PERCENT DISTORTION meter indication follows control	----yes----no
12f	PERCENT DISTORTION meter indication follows control	----yes----no
12g	PERCENT DISTORTION meter indication follows control	----yes----no
13	PERCENT DISTORTION meter indicates 0	----
14	PERCENT DISTORTION meter indicates 25 for each substep.	----yes----no ----yes----no ----yes----no ----yes----no

4-9. Summary of Performance Standards

Arrange a checklist similar to that shown below In the *Test indication* column, record the actual indications obtained during the tests These data can be used as checks against the performance standards the next time the test are performed

a. Power Supply Test

Step	Performance standard	Test indication
1a	15 volts $\pm 5\%$	----volts
1b	15 volts $\pm 5\%$	----volts
1c	130 volts $\pm 5\%$	----volts

b. Distortion Measurement Test

Step	Performance standard	Test indication
1	SIGNAL lamp flasher	----yes----no
	LATE lamp lights.	----yes----no
	PERCENT DISTORTION meter follows control ($\pm 1\%$)	\pm ---- %
2	PERCENT DISTORTION meter indicates 0 distortion	----
3	EARLY lamp lights.	----yes----no
	PERCENT DISTORTION meter follows control ($\pm 1\%$)	+ ---- %
4	PERCENT DISTORTION meter indicates 0 distortion	----
5	EARLY lamp lights.	----yes----no
	PERCENT DISTORTION meter follows control ($\pm 1\%$)	\pm ---- %
6	PERCENT DISTORTION meter indicates 0	----
7	LATE lamp lights	----yes----no
	PERCENT DISTORTION meter follows control ($\pm 1\%$)	\pm ---- %

Step	Performance standard	Test indication
8	PERCENT DISTORTION meter indicates 0 distortion	----
9	PERCENT DISTORTION meter indicates 40 when control is dropped to 0	----
10	PERCENT DISTORTION meter follows control ($\pm 1\%$)	\pm ---- %
11	PERCENT DISTORTION meter follows control ($\pm 1\%$)	\pm ---- %
12a	PERCENT DISTORTION meter indicates 25.	----
12b	PERCENT DISTORTION meter indicates minimum (or maximum)	----
12c	PERCENT DISTORTION meter indication follows control	----yes----no
12d	PERCENT DISTORTION meter indication follows control	----yes----no
12e	PERCENT DISTORTION meter indication follows control	----yes----no
12f	PERCENT DISTORTION meter indication follows control	----yes----no
12g	PERCENT DISTORTION meter indication follows control	----yes----no
13	PERCENT DISTORTION meter indicates 0	----
14	PERCENT DISTORTION meter indicates 25 for each substep.	----yes----no ----yes----no ----yes----no ----yes----no

CHAPTER 5

DEPOT MAINTENANCE

5-1. General

Depot maintenance consists of rebuilding the TS-800/UGM-1. Final tests for a rebuilt TS-800/UGM-1 are the same as those for general support (ch. 4). The tools and test equipment required for depot testing are the same as those for general support.

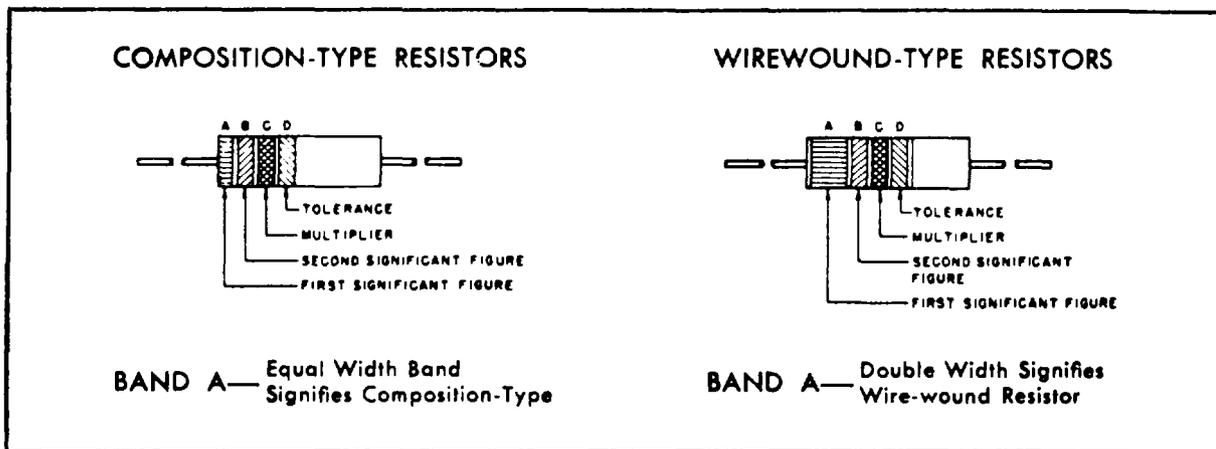
5-2. Maintenance Procedures

Restore the appearance, performance, and life expectancy of the TS-800/UGM-1 to a

standard comparable to that of new equipment by performing the following procedures.

- a. Disassemble the TS-800/UGM-1 as required.
- b. Inspect all parts.
- c. Repair or replace any worn, unserviceable part with a part that conforms to the original manufacturing tolerances and specifications.
- d. Reassemble the TS-800/UGM-1.
- e. Perform the general support testing procedures (paras 4-6, 4-7, and 4-8).

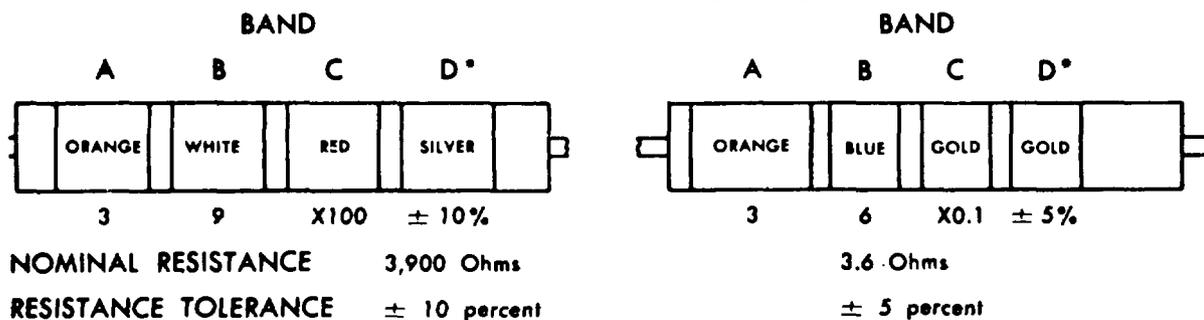
COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS



COLOR CODE TABLE

BAND A		BAND B		BAND C		BAND D*	
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)
BLACK	0	BLACK	0	BLACK	1		
BROWN	1	BROWN	1	BROWN	10		
RED	2	RED	2	RED	100		
ORANGE	3	ORANGE	3	ORANGE	1,000		
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	± 10
GREEN	5	GREEN	5	GREEN	100,000	GOLD	± 5
BLUE	6	BLUE	6	BLUE	1,000,000		
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7				
GRAY	8	GRAY	8	SILVER	0.01		
WHITE	9	WHITE	9	GOLD	0.1		

EXAMPLES OF COLOR CODING



*If Band D is omitted, the resistor tolerance is ± 20%, and the resistor is not Mil-Std.

STD-R2

Figure 5-1. MIL-STD resistor color code markings.

CHAPTER 6

DEPOT OVERHAUL STANDARDS

6-1. Applicability of Depot Overhaul Standards

The tests outlined in this chapter are designed to measure the performance capability of a repaired distortion analyzer. Equipment that is to be returned to stock should meet the standards given in these tests.

6-2. Applicable References

a. Repair Standards. Applicable procedures of the depot performing these tests and the general standards for repaired electronic equipment given in TB SIG 355-1, TB SIG 355-2, and TB SIG 355-3 form a part of the requirements for testing the distortion analyzer.

b. Technical Publications. The technical" publications applicable to the equipment to be tested are indicated below.

Equipment and subject Test Set, Teletypewriter AN/UGM-1,	Publication TM 11-6625-620-12
--	----------------------------------

Equipment and subject Organizational Maintenance. Organizational, Direct Support, General Support, and Depot Maintenance Repair Parts and Special Tools List, Test Set, Teletypewriter TS-800/UGM-1 (P/O Test Set, Teletypewriter AN/UGM-1).	Publication TM 11-6625-620-25P-2
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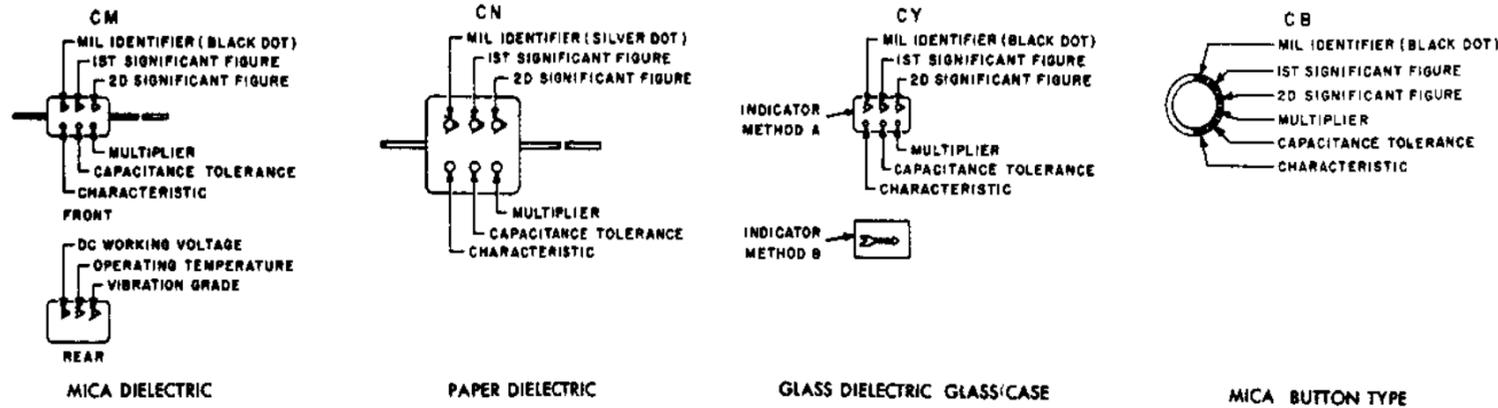
c. Modification Work Orders. Perform all modification work orders applicable to this equipment before making the tests specified. DA Pam 310-7 lists all available MWO's.

6-3. Depot Overhaul Standards

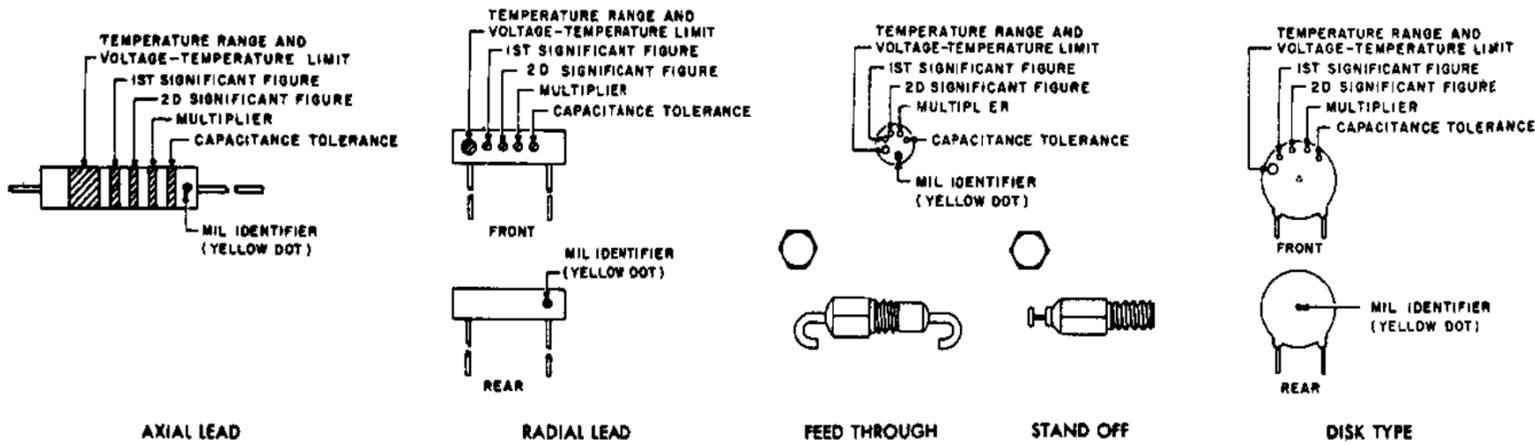
Perform the tests listed in chapter 4 to check the operation of the distortion analyzer. If meter indications are not within tolerance given, make necessary adjustments (ch. 3) correct the trouble before attempting any repair procedures.

COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

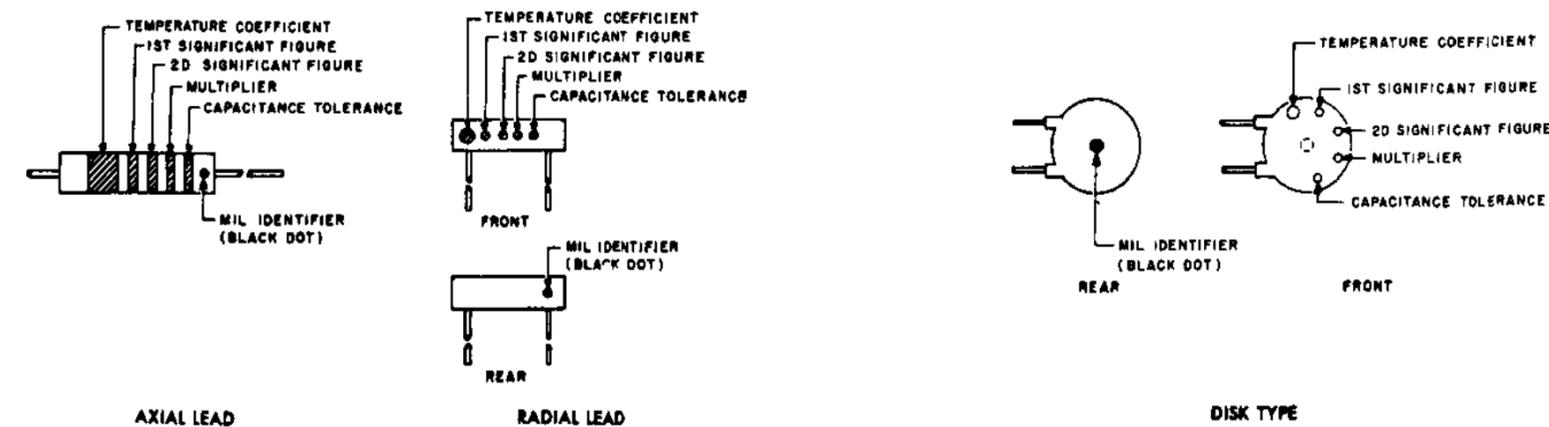
GROUP I Capacitors, Fixed, Various-Dielectrics, Styles CM, CN, CY, and CB



GROUP II Capacitors, Fixed Ceramic-Dielectric (General Purpose) Style CK



GROUP III Capacitors, Fixed, Ceramic Dielectric (Temperature Compensating) Style CC



COLOR CODE TABLES

TABLE I - For use with Group I, Styles CM, CN, CY and CB

COLOR	MIL ID	1st SIG FIG	2nd SIG FIG	MULTIPLIER ¹	CAPACITANCE TOLERANCE				CHARACTERISTIC ²				DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CY	CB			
BLACK	CM, CY, CB	0	0	1			± 20%	± 20%		A				-55 to +70 C	10-55 cps
BROWN		1	1	10					B	E					
RED		2	2	100	± 2%		± 2%	± 2%	C		C			-55 to +85 C	
ORANGE		3	3	1 000		± 30%			D			D	300		
YELLOW		4	4	10 000					E					-55 to +125 C	10-2 000 cps
GREEN		5	5				± 5%		F				500		
BLUE		6	6											-55 to +150 C	
PURPLE (VIOLET)		7	7												
GREY		8	8												
WHITE		9	9												
GOLD				0.1			± 5%	± 5%							
SILVER	CN				± 10%	± 10%	± 10%	± 10%							

TABLE II - For use with Group II, General Purpose, Style CK

COLOR	TEMP RANGE AND VOLTAGE - TEMP LIMITS ²	1st SIG FIG	2nd SIG FIG	MULTIPLIER ¹	CAPACITANCE TOLERANCE	MIL ID
BLACK		0	0	1	± 20%	
BROWN	AW	1	1	10	± 10%	
RED	AX	2	2	100		
ORANGE	BX	3	3	1 000		
YELLOW	AV	4	4	10 000		CK
GREEN	CZ	5	5			
BLUE	BY	6	6			
PURPLE (VIOLET)		7	7			
GREY		8	8			
WHITE		9	9			
GOLD						
SILVER						

TABLE III - For use with Group III, Temperature Compensating, Style CC

COLOR	TEMPERATURE COEFFICIENT ⁴	1st SIG FIG	2nd SIG FIG	MULTIPLIER ¹	CAPACITANCE TOLERANCE		MIL ID
					Capacitance over 10uuf	Capacitance 10uuf or less	
BLACK	0	0	0	1		± 20uuf	CC
BROWN	-30	1	1	10	± 1%		
RED	-60	2	2	100	± 2%	± 0.25uuf	
ORANGE	-150	3	3	1 000			
YELLOW	-220	4	4				
GREEN	-330	5	5		± 5%	± 0.5uuf	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	± 10%		
GOLD	+100					± 1.0uuf	
SILVER							

- The multiplier is the number by which the two significant (SIG) figures are multiplied to obtain the capacitance in uuf
- Letters indicate the Characteristics designated in applicable specifications MIL-C-5 MIL-C-91 MIL-C-11272 and MIL-C-10950 respectively
- Letters indicate the temperature range and voltage temperature limits designated in MIL-C-11015
- Temperature coefficient in parts per million per degree centigrade

Figure 6-1. MIL-STD capacitor color code markings.

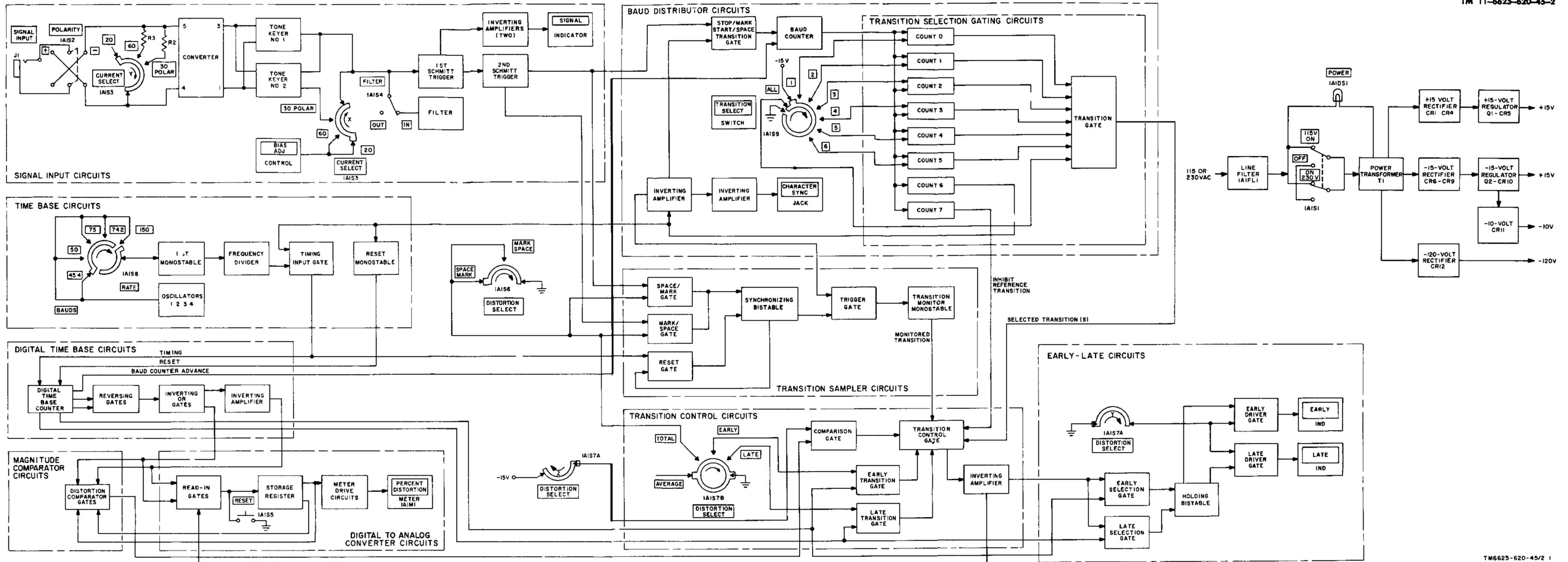


Figure 6-2. Teletypewriter Test Set TS-800/UGM-1, block diagram

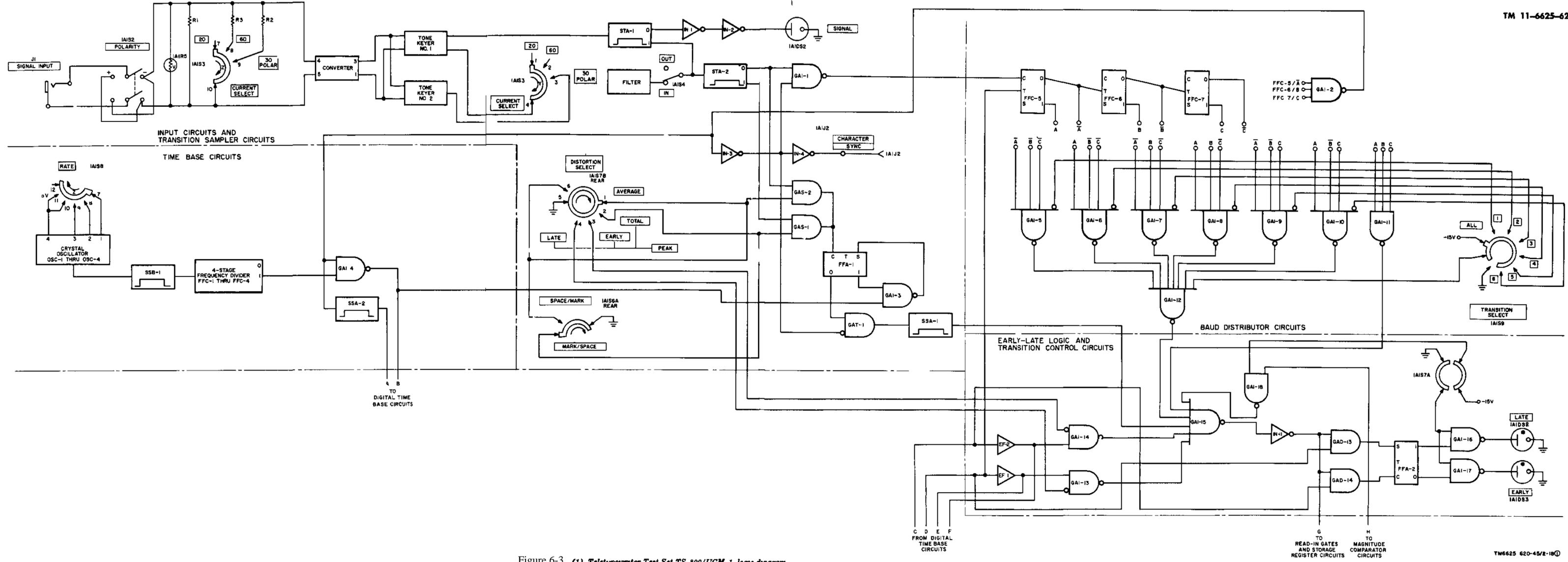
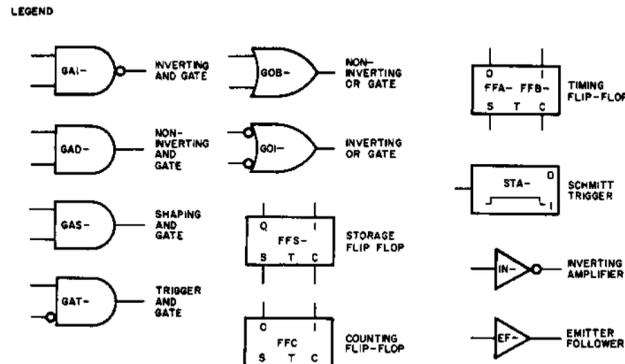


Figure 6-3. (1) Teletypewriter Test Set TS-800/UGM-1, logic diagram.

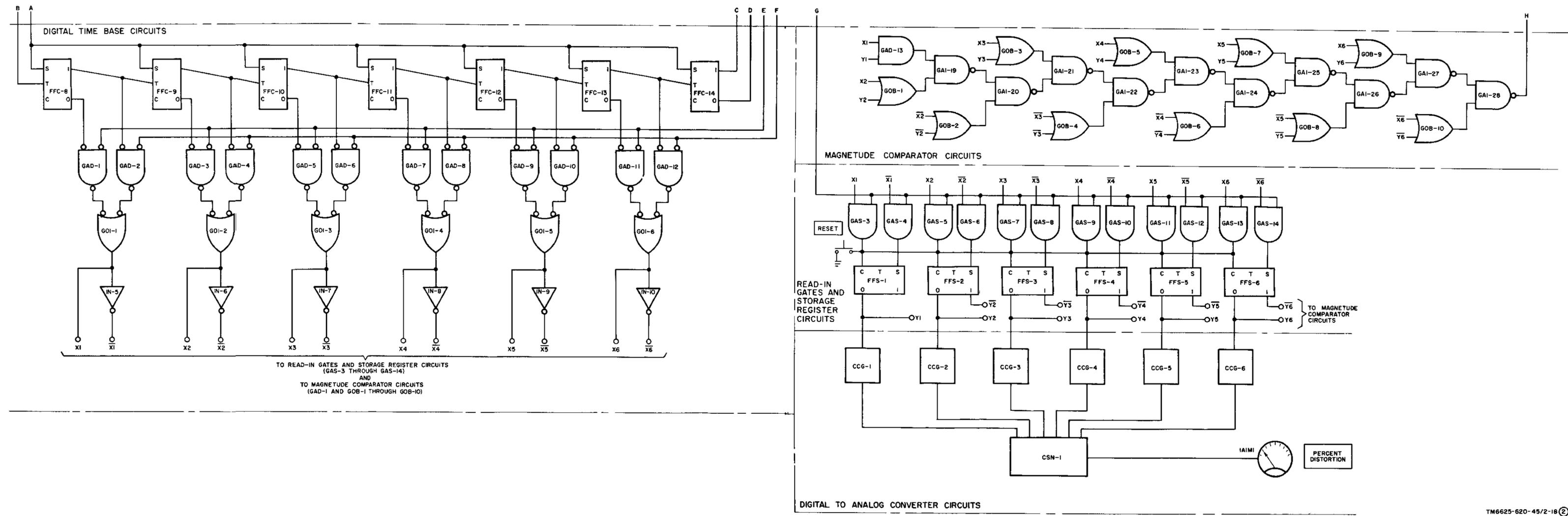
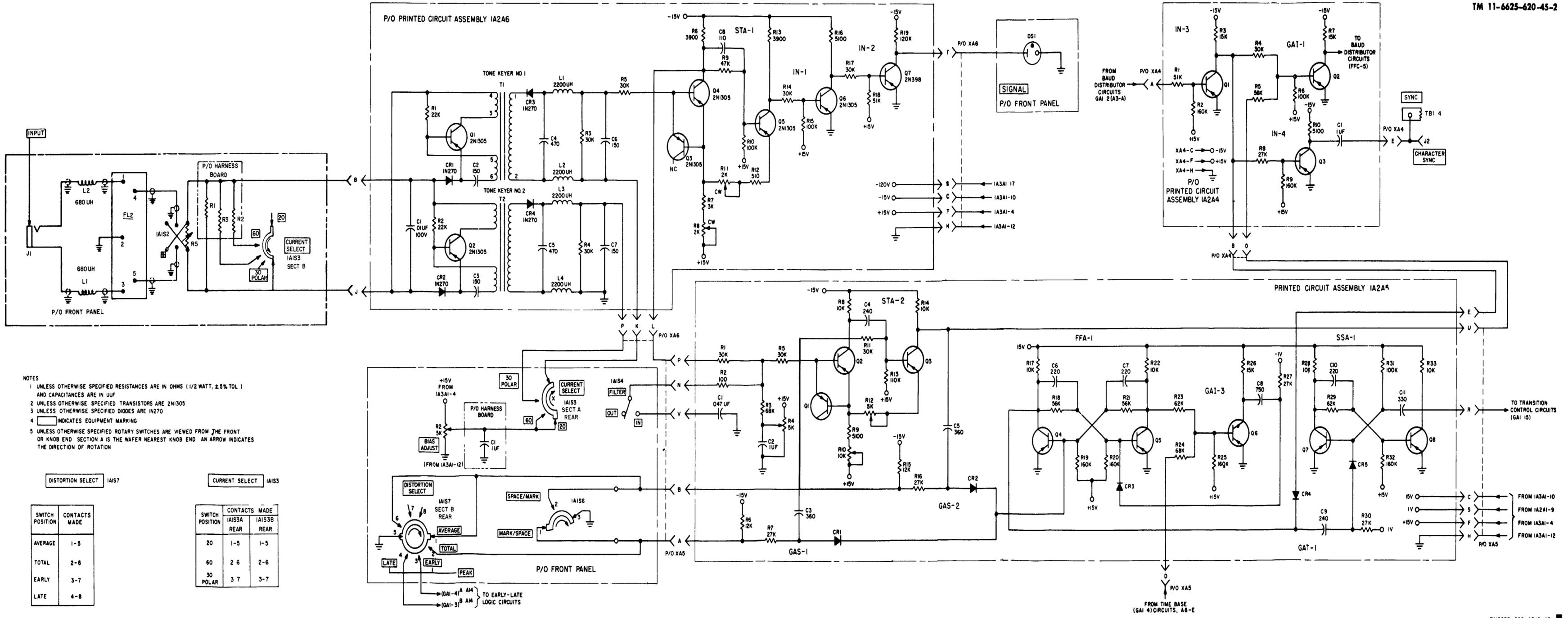


Figure 6-3. (2) Teletypewriter Test Set TS-800/UGM-1, logic diagram.



- NOTES
- UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS (1/2 WATT, ±5% TOL) AND CAPACITANCES ARE IN UUF
 - UNLESS OTHERWISE SPECIFIED TRANSISTORS ARE 2N1305
 - UNLESS OTHERWISE SPECIFIED DIODES ARE IN270
 - INDICATES EQUIPMENT MARKING
 - UNLESS OTHERWISE SPECIFIED ROTARY SWITCHES ARE VIEWED FROM THE FRONT OR KNOB END SECTION A IS THE WAFER NEAREST KNOB END AN ARROW INDICATES THE DIRECTION OF ROTATION

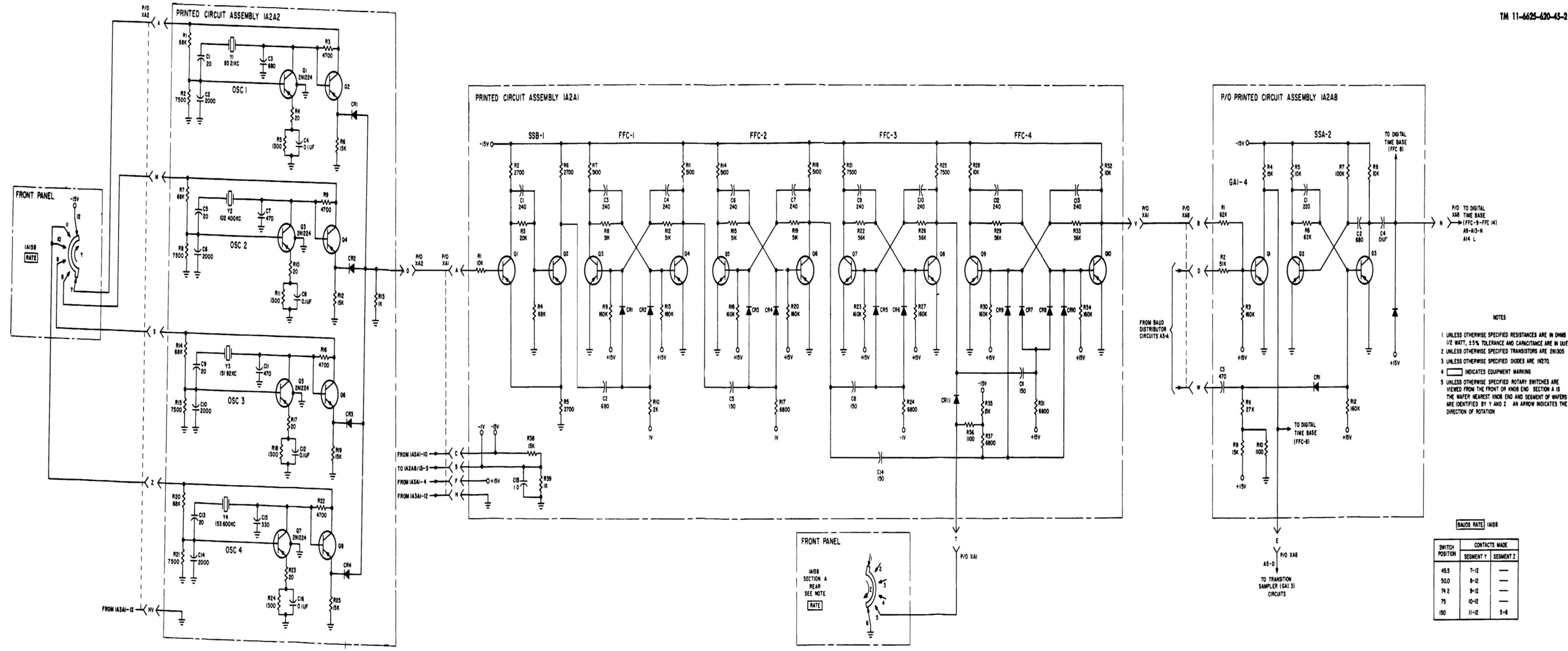
DISTORTION SELECT IAIS7

CURRENT SELECT IAIS3

SWITCH POSITION	CONTACTS MADE
AVERAGE	1-5
TOTAL	2-6
EARLY	3-7
LATE	4-8

SWITCH POSITION	CONTACTS MADE IAIS3A REAR	CONTACTS MADE IAIS3B REAR
20	1-5	1-5
60	2-6	2-6
30 POLAR	3-7	3-7

Figure 6-4. Input circuits and transition-sampling circuits, schematic diagram.

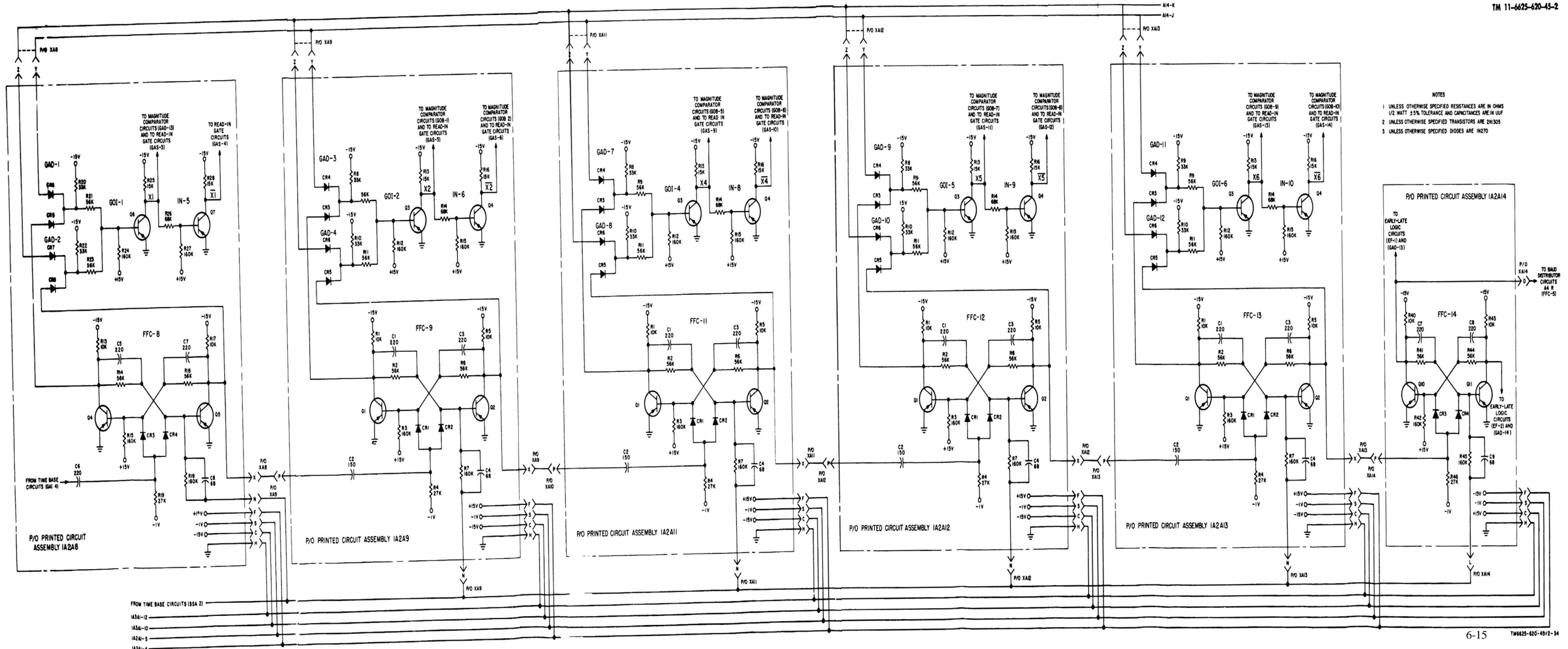


- NOTES
- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS 1/2 WATT, ±5% TOLERANCE AND CAPACITANCE ARE IN UUF
 - 2 UNLESS OTHERWISE SPECIFIED TRANSISTORS ARE 2N1305
 - 3 UNLESS OTHERWISE SPECIFIED DIODES ARE 1N270.
 - 4 INDICATES EQUIPMENT MARKING
 - 5 UNLESS OTHERWISE SPECIFIED ROTARY SWITCHES ARE VIEWED FROM THE FRONT OR KNOB END SECTION A IS THE WAFER NEAREST KNOB END AND SEGMENT OF WAFERS ARE IDENTIFIED BY Y AND Z. AN ARROW INDICATES THE DIRECTION OF ROTATION

BAUDS RATE IA158

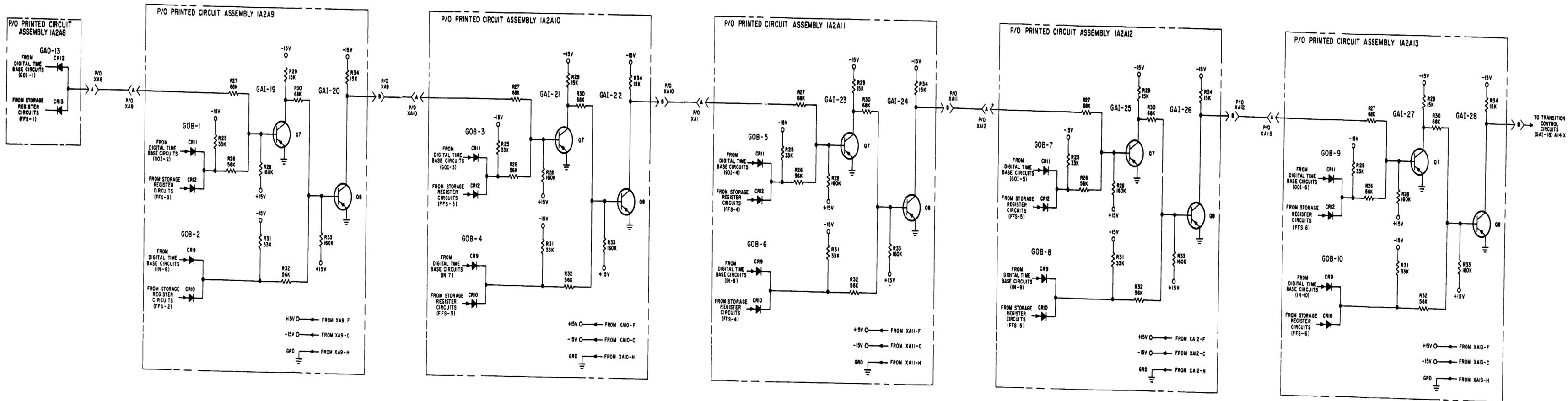
SWITCH POSITION	CONTACTS MADE	
	SEGMENT Y	SEGMENT Z
45.5	7-12	---
50.0	8-12	---
74.2	9-12	---
75	10-12	---
150	11-12	5-6

Figure 6-5. Time-base circuits, schematic diagram.



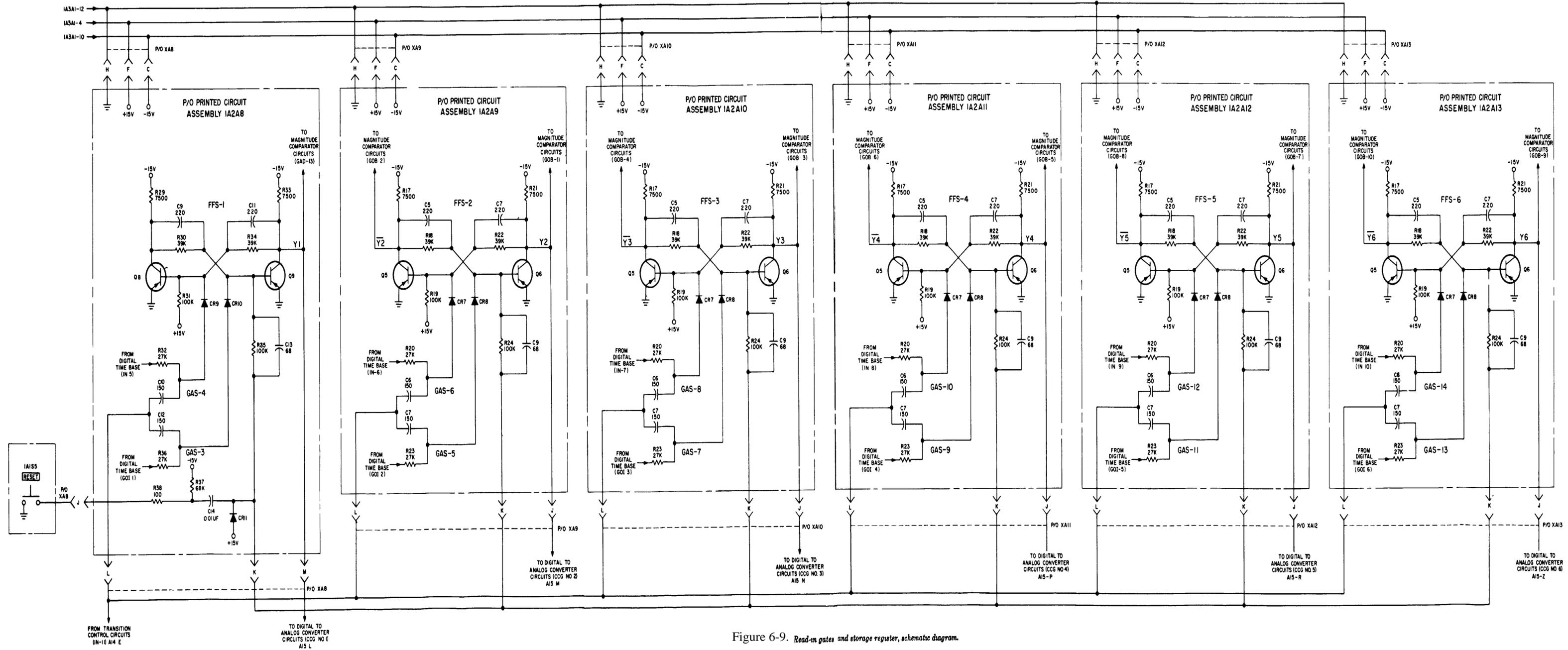
- NOTES
- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS
 - 2 UNLESS OTHERWISE SPECIFIED TOLERANCE AND CAPACITANCES ARE IN UUF
 - 3 UNLESS OTHERWISE SPECIFIED DIODES ARE IN270

Figure 6-6. Digital timebase circuits, schematic diagram.



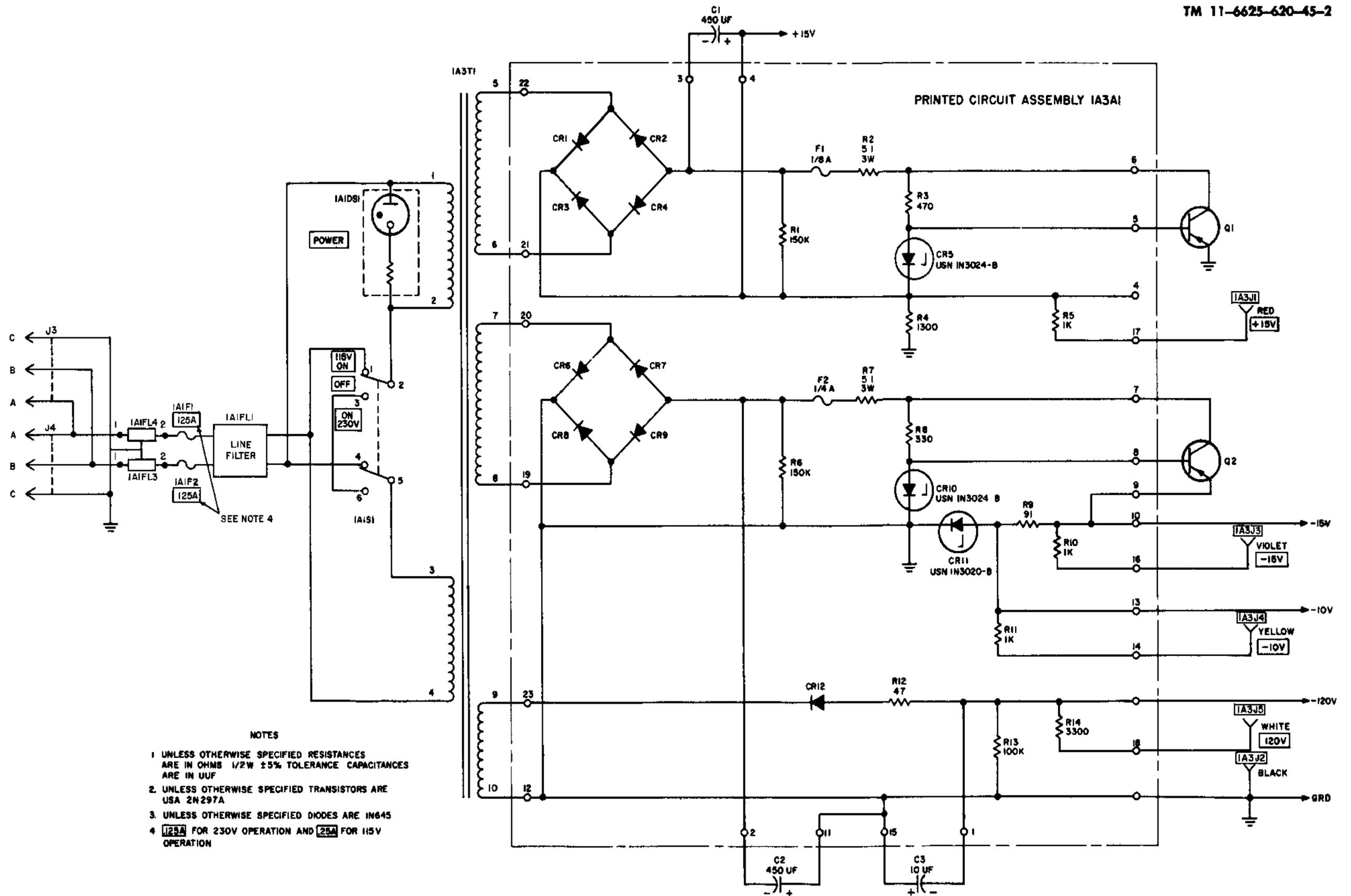
- NOTES
- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS
1/2 WATT, ± 5% TOLERANCE CAPACITANCES ARE IN UUF
 - 2 UNLESS OTHERWISE SPECIFIED TRANSISTORS ARE 2N1305
 - 3 UNLESS OTHERWISE SPECIFIED DIODES ARE IN270
 - 4 FOR INPUT POWER CONNECTIONS, REFER TO DIGITAL TIME BASE CIRCUITS SCHEMATIC

Figure 6-7. Magnitude comparator circuits, schematic diagram.



- NOTES
- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS 1/2 WATT, 5% TOLERANCE AND CAPACITANCES ARE IN UF
 - 2 UNLESS OTHERWISE SPECIFIED TRANSISTORS ARE 2N1305
 - 3 UNLESS OTHERWISE SPECIFIED DIODES ARE IN270
 - 4 INDICATES EQUIPMENT MARKING

Figure 6-9. Read-in gates and storage register, schematic diagram.



- NOTES
- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS 1/2W ±5% TOLERANCE CAPACITANCES ARE IN UUF
 - 2 UNLESS OTHERWISE SPECIFIED TRANSISTORS ARE USA 2N297A
 - 3 UNLESS OTHERWISE SPECIFIED DIODES ARE IN645
 - 4 **125A** FOR 230V OPERATION AND **25A** FOR 115V OPERATION

Figure 6-10. Power supply, schematic diagram.

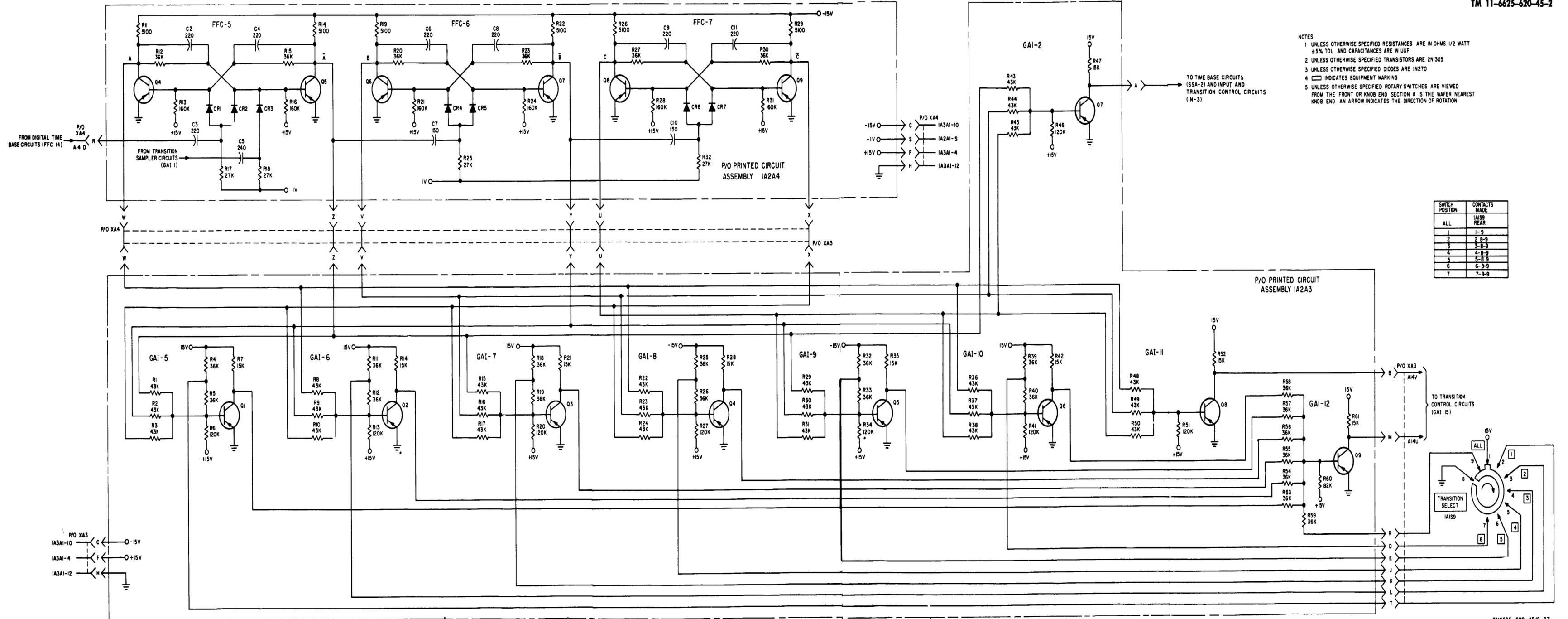


Figure 6-11. Baud distributor circuits, schematic diagram.

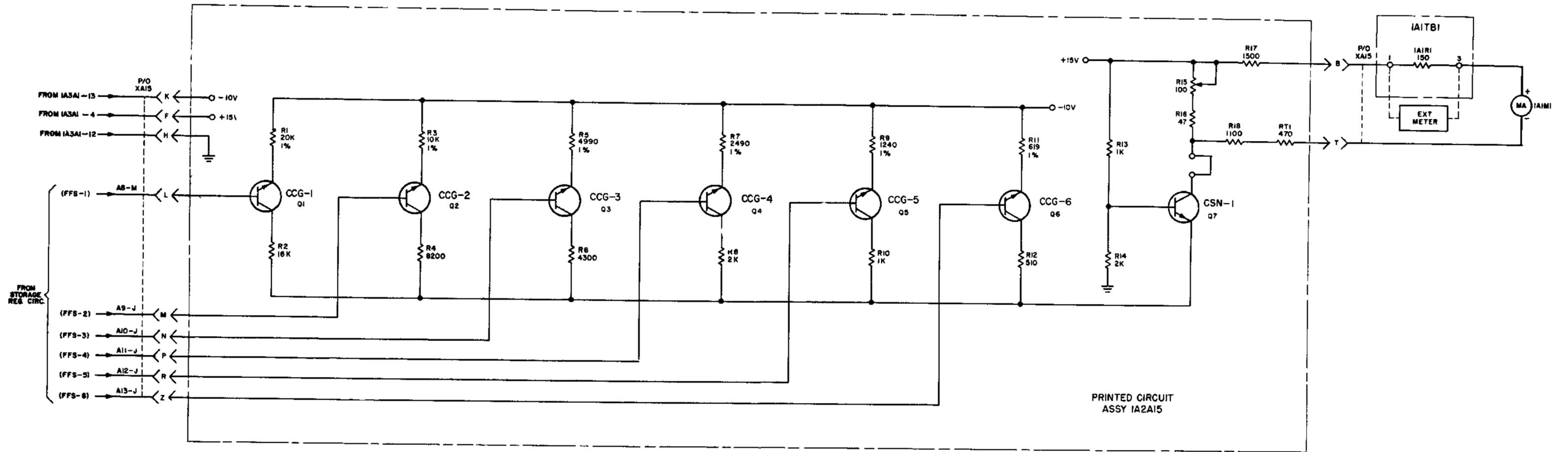
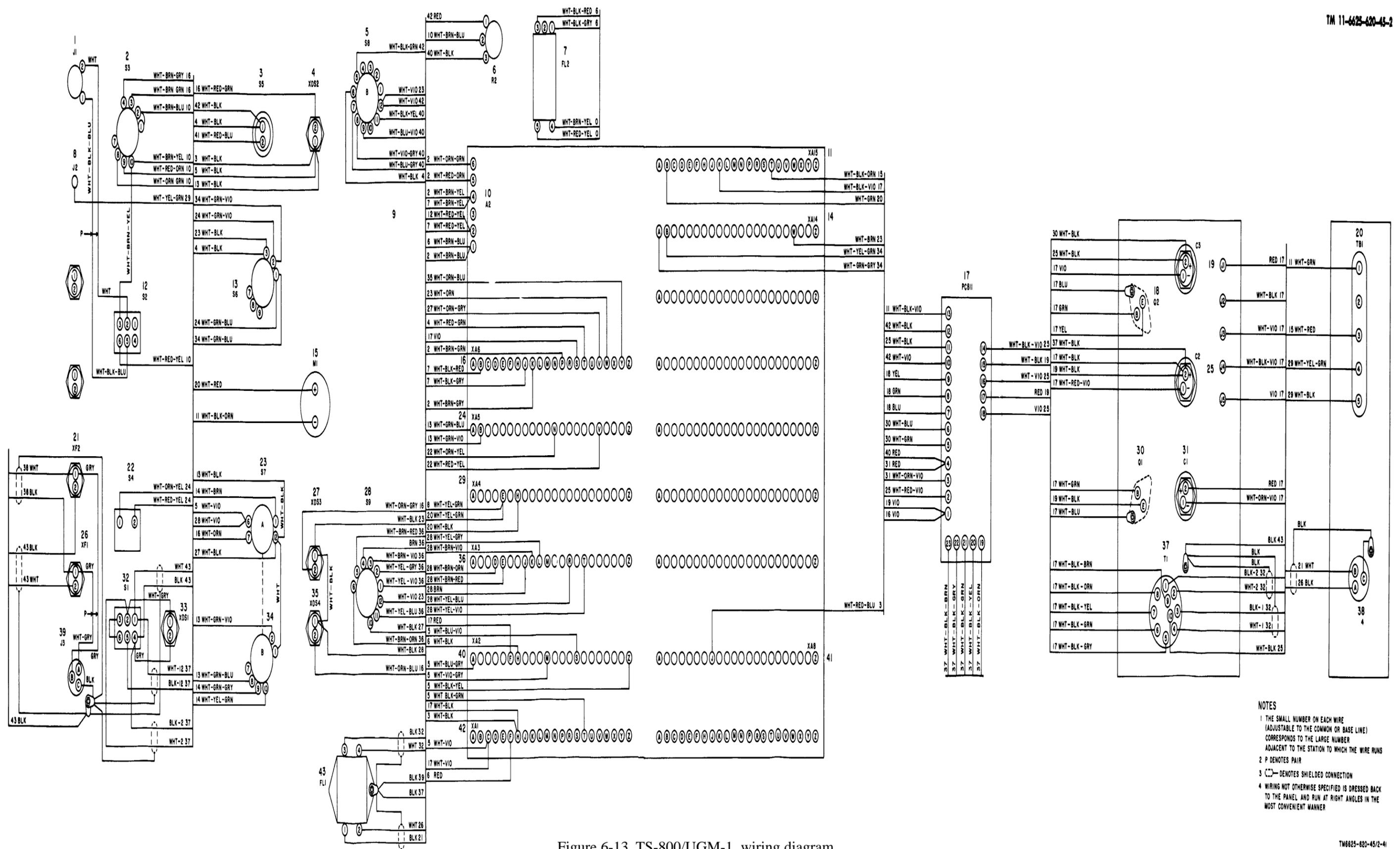


Figure 6-12. Digital-to-analog converter, schematic diagram.

- NOTES
- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE 1% OHMS
1/2 WATT ±5% TOLERANCE CAPACITANCES ARE 1% UUF
 - 2 UNLESS OTHERWISE SPECIFIED ALL TRANSISTORS ARE
2N1308
 - 3 ○ DENOTES COMMON TIE POINT



- NOTES**
- 1 THE SMALL NUMBER ON EACH WIRE (ADJUSTABLE TO THE COMMON OR BASE LINE) CORRESPONDS TO THE LARGE NUMBER ADJACENT TO THE STATION TO WHICH THE WIRE RUNS
 - 2 P DENOTES PAIR
 - 3 DENOTES SHIELDED CONNECTION
 - 4 WIRING NOT OTHERWISE SPECIFIED IS DRESSED BACK TO THE PANEL AND RUN AT RIGHT ANGLES IN THE MOST CONVENIENT MANNER

Figure 6-13. TS-800/UGM-1, wiring diagram.

APPENDIX
REFERENCES

Following a list of applicable references available to the general support and depot maintenance repairman of Test Set, Teletypewriter TS-800/UGM- 1.

DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms
DA Pam 738-750	The Army Maintenance Management System (TAMMS)
FM 11-62	Communications, Electronics Fundamentals: Solid State Devices and Solid State Power Supplies
TA 11-101 (11-158)	Allowances for Signal Corps Expendable Supplies for Signal Depot Company
TB SIG 222	Solder and Soldering
TB SIG 355-1	Depot Inspection Standard for Repaired Signal Equipment
TB SIG 355-2	Depot Inspection Standard for Refinishing Repaired Signal Equipment
TB SIG 355-3	Depot Inspection Standard for Moisture and Fungus Resistant Treatment
TM 11-1214	Instruction Book for: Oscilloscope OS-8/U
TM 11-6625-366-10	Operator's Manual for Multimeter TS-352B/U (NSN 6625-00-553-0142)
TM 11-6625-366-15	Operator's, Organizational, Direct Support, General Support and Depot Maintenance Manual: Multimeter TS-352B/U
TM 11-6625-539-15	Operator, Organizational, Field, and Depot Maintenance Manual: Transistor Set, TS-1836/U (NSN 6625-00-168-0954)
TM 11-6625-620-12	Organizational Maintenance Manual: Test Set, Teletypewriter AN/UGM-1 (NSN 6625-00-965-0195)
TM 11-6625-620-40P-2	General Support Repair Parts and Special Tools Lists for Test Set, Teletypewriter, TS-800/UGM-1 and TS-800A/UGM-1 (NSN 6625-00-965-0197)
TM 11-6625-620-45-1	Limited Coverage, General Support and Depot Maintenance Manual: Test Set, Teletypewriter TS-799/UGM-1

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NG: None.

USAR: None.

For explanation of abbreviations used see AR 320-50.

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 1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
 1 Kilometer = 1000 Meters = 0.621 Miles

WEIGHTS

1 Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
 1 Kilogram = 1000 Grams = 2.2 lb.
 1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
 1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
 1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
 1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
 1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

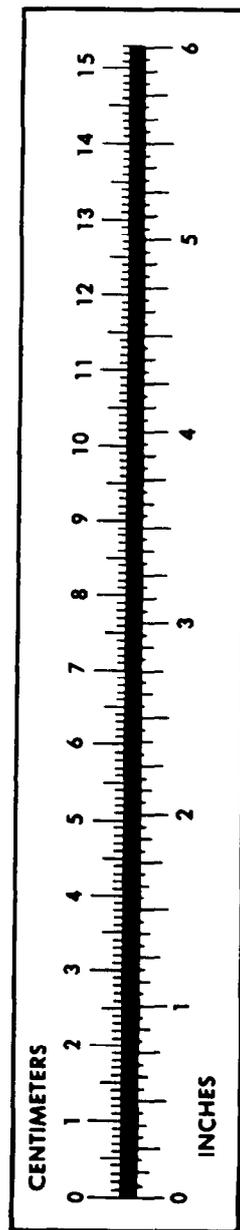
TEMPERATURE

$5/9(^{\circ}\text{F} - 32) = ^{\circ}\text{C}$
 212° Fahrenheit is equivalent to 100° Celsius
 90° Fahrenheit is equivalent to 32.2° Celsius
 32° Fahrenheit is equivalent to 0° Celsius
 $9/5^{\circ}\text{C} + 32 = ^{\circ}\text{F}$

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
its	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
ometers per Liter	Miles per Gallon	2.354
ometers per Hour	Miles per Hour	0.621



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