

TECHNICAL MANUAL

DIRECT SUPPORT AND
GENERAL SUPPORT
MAINTENANCE MANUAL

FOR

MULTIPLEXER TD-754/G
(NSN 5820-00-930-8078)

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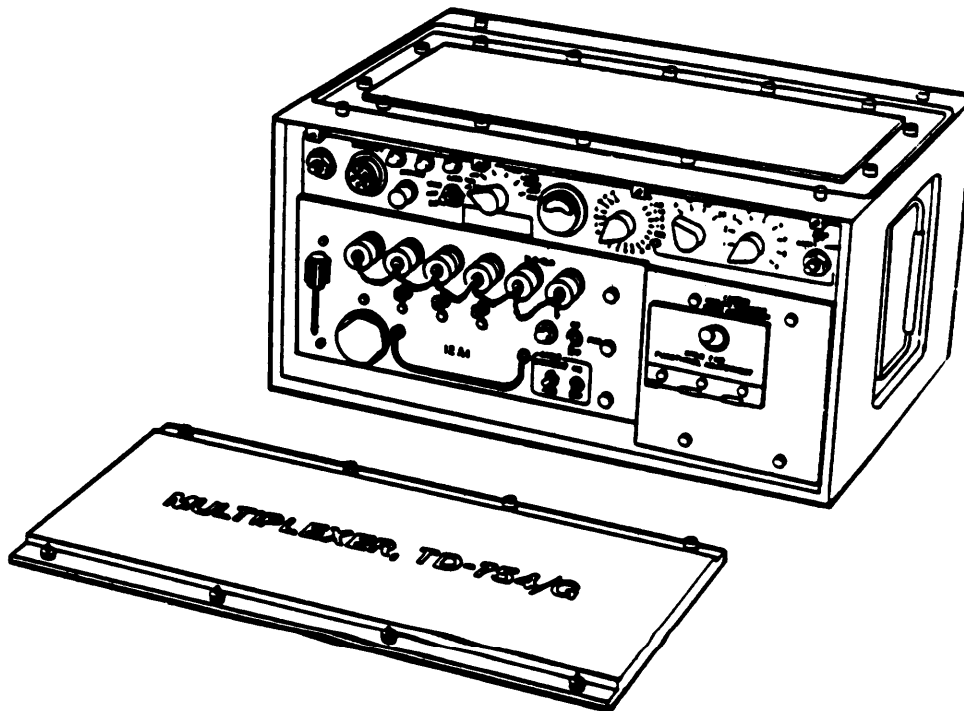
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SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1

DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

2

IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

3

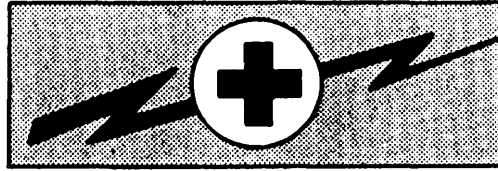
IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL

4

SEND FOR HELP AS SOON AS POSSIBLE

5

AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION



WARNING

HIGH VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections of 115/230-volt ac input connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through vital organs of the body.

WARNING

Do not be misled by the term "low voltage". Potentials as low as 50 volts may cause death under adverse conditions.

For Artificial Respiration, refer to FM 21-11.

WARNING

Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

When compressed air is used for cleaning, the following warning applies;

Compressed air shall not be used for cleaning purposes except where reduced to less than 29 pounds per square inch (psi) and then only with effective chip guarding and personnel protective equipment. Do not use compressed air to dry parts when TRICHLOROTRIFLUOROETHANE has been used. Compressed air is dangerous and can cause serious bodily harm if protective means or methods are not observed to prevent chip or particle (of whatever size) from being blown into the eyes or unbroken skin of the operator or other personnel.

Assure that the input voltage to the TD-754/G is 115 \pm 6 vac. Higher voltages will damage the equipment or possibly cause an explosion resulting in injury to personnel.

**DANGEROUS VOLTAGES ARE PRESENT
DON'T TAKE CHANCES!**

WARNING

Dangerous voltages exist in the TD-754/G that may cause death or injury to personnel. 115 volts ac are present in the equipment when PWR switch is operated to ON, and a dc voltage of up to 1,000 volts may be present in the equipment when CABLE CURRENT switch is operated to ON. When troubleshooting or repairing the TD-754/G, be careful not to contact ac or dc high voltage connections in the equipment. Use insulated test probes when making measurements or waveform checks. Always operate PWR and CABLE CURRENT switches to OFF before connecting test probes to the TD-754/G.

Always be sure your equipment is properly grounded. Death from electric shock can result from handling ungrounded or improperly grounded equipment.

CAUTION

This equipment is transistorized. Do not make indiscriminate resistance measurements.

**Direct Support and General Support Maintenance Manual
for
MULTIPLEXER TD-754/G
(NSN 5820-00-930-8078)**

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-LM-LT, Fort Monmouth, New Jersey 07703-5007. In either case, a reply will be furnished direct to you.

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NOTE: CECOM DMWR 11-5805-383 (1 Aug 1988) replaces Depot portion of TM 11-5805-383-35. (This notice does not appear on DMWR.) This TM 11-5805-383-34 replaces balance of (Jan 1971) and all changes.

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CHAPTER 1

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Section 1. GENERAL

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1-1. Scope

This manual contains instructions for direct support and general support maintenance including troubleshooting, testing, alignment and repair for Multiplexer TD-754/G and includes a functional description of the equipment. References are provided in Appendix A.

1-2. Consolidated Index of Army Publications and Blank Forms

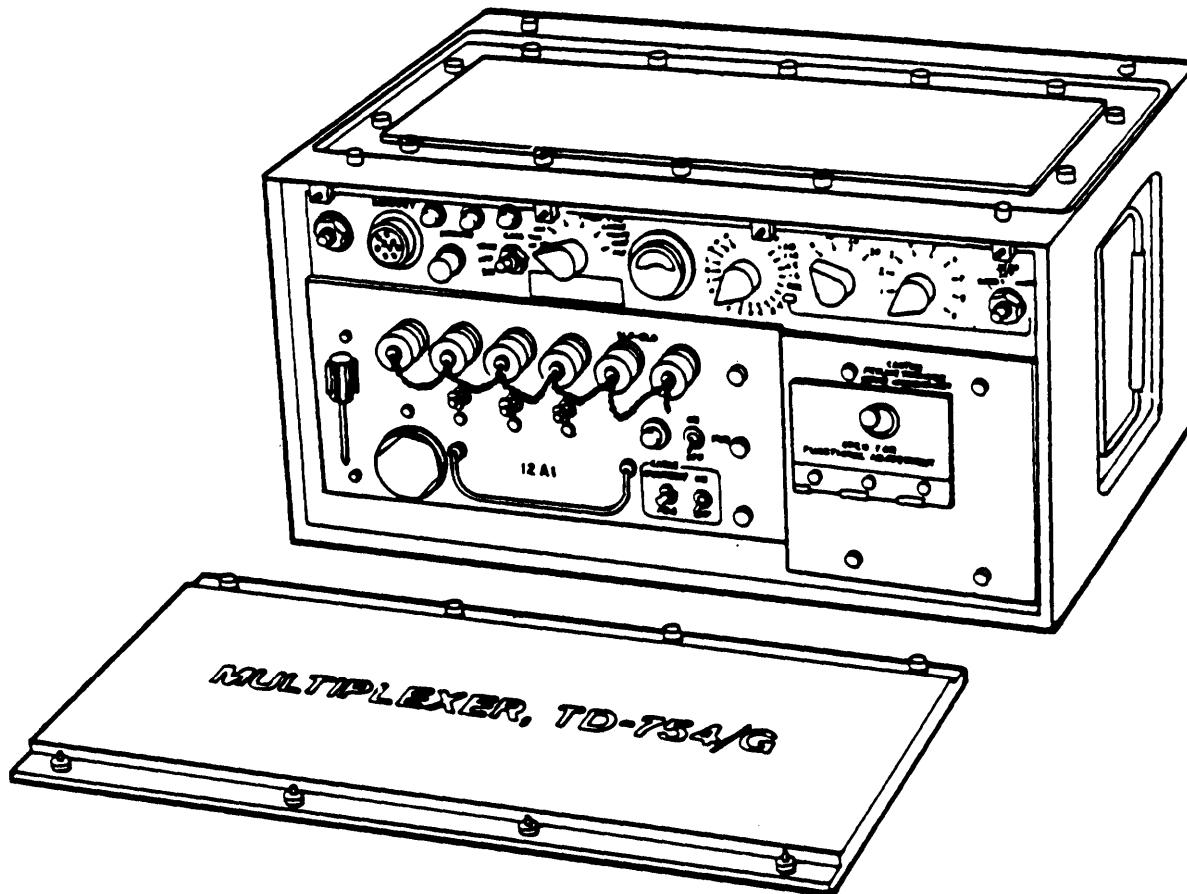
Refer to the latest issue of DA PAM 25-30 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

1-3. Maintenance Forms, Records, and Reports

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750, as contained in Maintenance Management Update.

b. Reporting of Item and Packaging Discrepancies. Fill out and forward SF364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/SECNAVINST 4355.18/AFR 400-54/MCO 4430.3J.

c. Transportation Discrepancy Report (TDR) (SF 361). Fill out and forward Transportation Discrepancy Report (TDR) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.



4858-002

Figure 1-1. Multiplexer TD-754/G.

1-4. Reporting Equipment Improvement Recommendations (EIR)

If your Multiplexer TD-754/G need improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about the equipment. Let us know why you don't like the design or performance. Put it on a SF 368 (Product Quality Deficiency Report). Mail it to: Commander US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ED-PH, Fort Monmouth, New Jersey 07703-5000. We'll send you a reply.

1-5. Administrative Storage

Administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS charts before storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness. (Refer to TM 11-5805-383-12.)

1-6. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

1-7. List of Abbreviations

VF	Voice Frequency
TMDE	Test, Measurement, and Diagnostic Equipment
PCM	Pulse-code Modulation
KHz	Kilohertz
RZ	Return-to-Zero
NRZ	Nonreturn-to-zero
SF	Service Facilities

Section II. Equipment Description and Data

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1-8. Equipment Characteristics, Capabilities and Features

The TD-754/G enables voice frequency (VF) communication through cable transmission systems composed of pulse-code modulations (pcm) equipment, such as Multiplexer TD-660/G. Typically, a TD-660/G or similar equipment sends a pcm pulse to a TD-754/G. The TD-754/G receives and encodes the pulse and transmits the altered pulse to a second TD-754/G which decodes the pulse (returning it to its original format) and transmits the pulse to another TD-660/G or similar equipment. The TD-754/G has 6-, 12-, 24-, or 48- channel capacity.

The two TD-754/G's can be up to 40 miles apart, with Pulse Form Restorers TD-206/G installed at 1-mile intervals along the cable link. The TD-206/G's are powered by the TD-754/G.

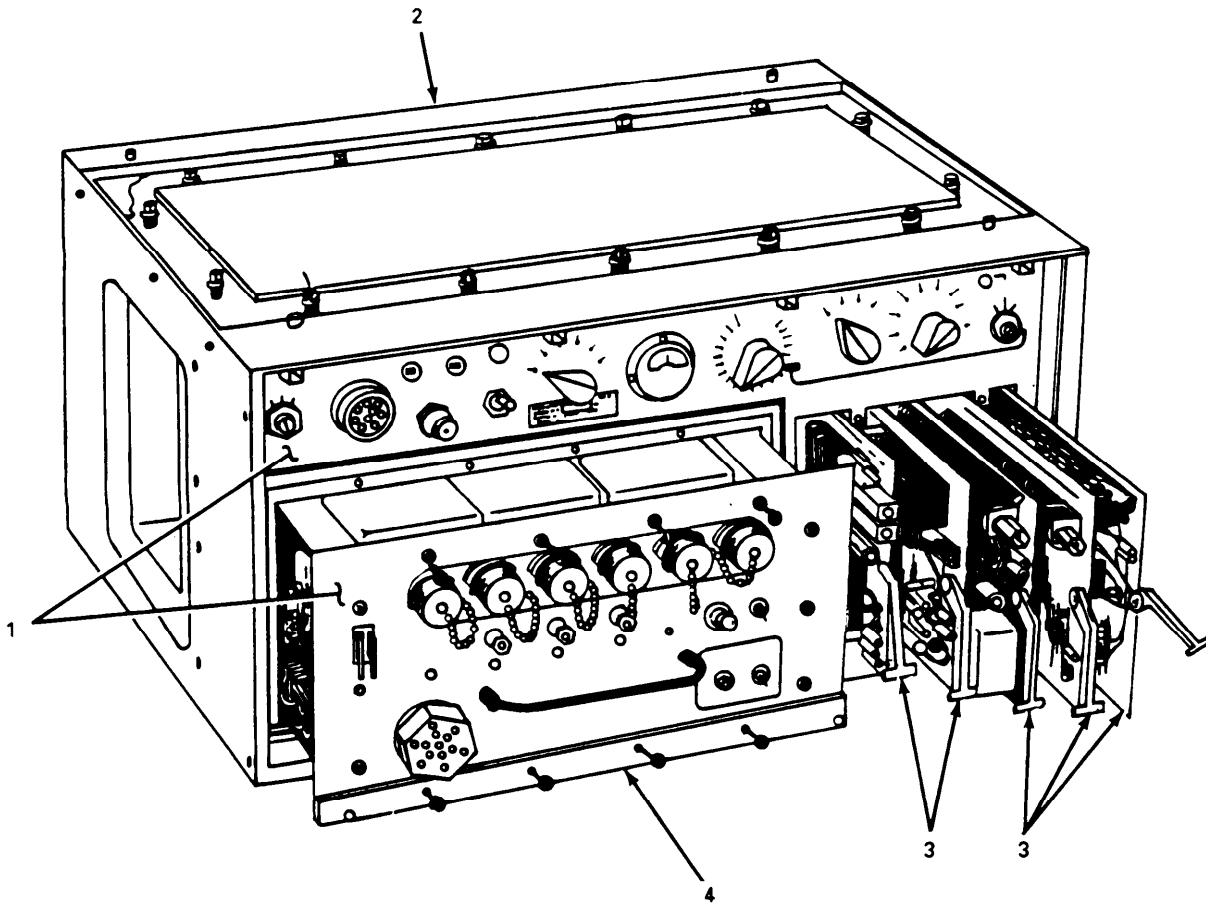
Order wire facilities in the TD-754/G permit voice communication between the two TD-754/G operators when Headset H-91/U is connected to the headset receptacle. When operating as an attended repeater, incoming order wire signals can be retransmitted. Although transmitted along the same cable link as the pcm pulses, order wire audio voltage signals are not affected by traffic failure or TD-206/G failure.

The TD-754/G has a monitor circuit that performs self-testing, and a cable fault locator circuit to detect and isolate faulty TD-206/G's in the cable link.

The TD-754/G can also be used in radio transmission systems. For a listing of compatible radio sets, multiplexer and cables refer to TM 11-5805-383-12.

1-9. Location and Description of Major Components (figure 1-2)

Item	Description
1. Front panel	Contains all operator controls and indicators and the protective cover over plug-in panels.
2. Rear panel	Contains all coaxial cable, multipin power and patch-through receptacles.
3. Plug-in panels (12A2 through 12A6)	Contain the transmit, receive, cable input and order wire circuits, and test jacks for monitoring major test points. The boards are keyed at the connector end to assure that each board is plugged into the correct TD-754/G receptacle.
4. Power supply 12A1	Provides dc power required to operate the TD-754/G and the TD-206/G's along the cable link. The power supply plugs into two multipin connectors located inside the rear panel of the TD-754/G case.



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Figure 1-2. Location of Major Components.

1-10. Differences Between Models

There are no differences between models applicable to the equipment covered by this technical manual.

1-11. Equipment Data

Refer to TM 11-5805-383-12 for pertinent technical data and equipment specifications.

1-12. Safety, Care and Handling

Throughout this manual are warnings, cautions and notes designed to protect personnel and equipment when handling the multiplexer. Learn the warnings on the warning page before attempting to perform maintenance, and observe all warnings, cautions and notes as you come upon them in the text.

Always be sure your equipment is properly grounded before turning on the power. If the multiplexer is removed from its rack mounting for operation, testing, service or maintenance, the equipment must be grounded to the work bench before the power is turned on, using a jumper wire of equal or larger gage than the power input wire.

The multiplexer weighs 45 pounds. Do not attempt to lift it without assistance.

Section III. PRINCIPLES OF OPERATION

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1-13. General

Principles of operation is divided into block level discussions and theory of operation. The block level discussions (paragraphs 1-14 through 1-16) provide an understanding of the purpose and function of the system and its component circuits, and the way in which the component circuits interact. Theory of operation (paragraphs 1-17 through 1-23) provides a detailed circuit analysis of each individual circuit that comprises the system.

1-14. Block Level Discussion General Information

The TD-754/G provides interface between pcm equipment, such as two Multiplexer TD-660(*)/G, connected in a cable link configuration. The TD-754/G also provides cable current to power Restorers, Pulse Form TD-206/G connected in the cable link. Order wire facilities for entering and monitoring order wire data on the cable link are also contained in the TD-754/G. The service facilities in the TD-754/G contain a monitor circuit and a cable fault

locator circuit. The monitor circuit is used to monitor input and output signals of key circuits in the TD-754/G to confirm normal equipment operation and/or to locate faulty circuits for maintenance purposes. The cable fault locator circuit is used to locate a faulty TD-206/G in the cable link.

Electrically, the TD-754/G accepts pulse code modulation (pcm) pulses from one external source, such as a TD-660(*)/G, when used in the 6- or 12-channel mode of operation. When used in the 24-channel mode of operation, the TD-754/G receives pcm pulses from two external sources and interleaves the pulses together to form one pcm pulse output to the cable link. In the 48-channel mode of operation, the TD-754/G operates as an attended repeater. The bit rate of the applied pcm pulses to the TD-754/G is 288 kilohertz (kHz) for 6-channel, 576 kHz for 12-channel and 24-channel, and 2304 kHz for 48-channel modes of operation. In all modes of operation, the pcm output from the TD-754/G to the cable link is half-width RZ (return to zero) pulses at a bit rate of 2304 kHz. The receiving TD-754/G at the opposite end of the cable link restores the half-width pcm pulses to full width pcm pulses, and provides two identical pcm outputs at a bit rate of 576 kHz for 6-, 12-, or 24- channel mode of operation, or at a bit rate of 2304 kHz for 48-channel mode of operation, that can be applied to one or two TD-660(*)/G's, or similar equipment, connected to the TD-754/G.

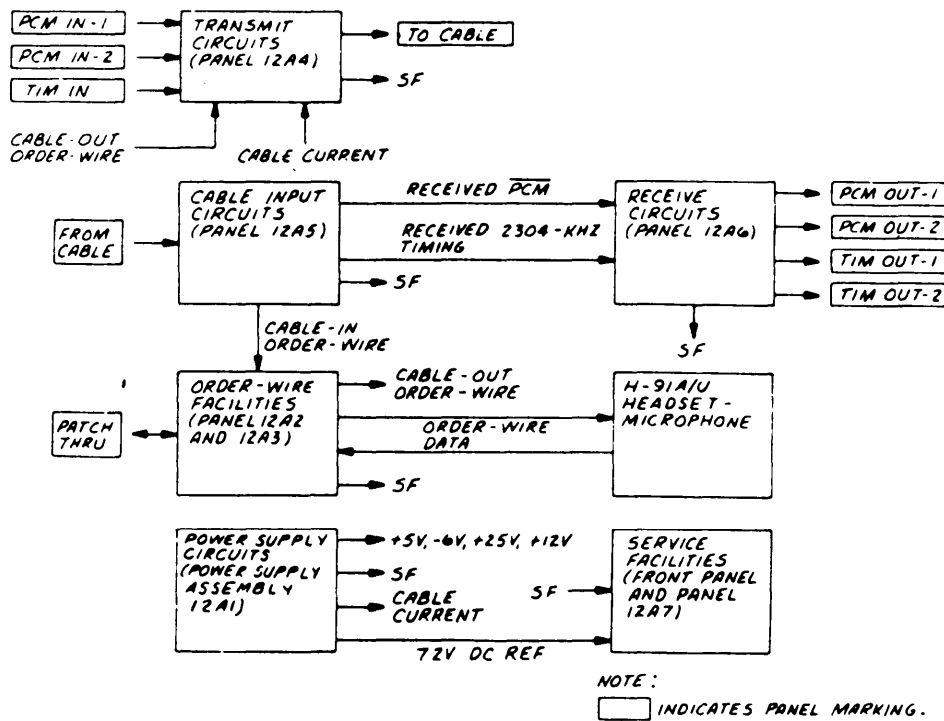
1-15. Overall Block Diagram Discussion

Figure 1-3 is a simplified overall block diagram of the TD-754/G. The block diagram shows the TD-754/G divided into six functional circuits. Each of these circuits is described in a through f below. The power supply circuits are mounted on power supply assembly 12A1 and the service facilities utilize the controls and indicators mounted on the front panel and components mounted on panel 12A7. The other functional circuits are mounted on one or more panels 12A2 through 12A6.

a. Transmit Circuit. The pcm pulses from a TD-660(*)/G, or similar equipment, are applied through the PCM IN-1 receptacle to the transmit circuits, where the pulses are conditioned and processed into half-width RZ pulses. The processed pcm pulses are applied at a 2304-kHz bit rate through the TO CABLE connector to the cable link. Cable-out order wire signals from the order wire facilities are superimposed on the pcm output pulses in the transmit circuits. The cable current from the power supply circuits to power the TD-206/G's in the cable is routed through the transmit circuits. In the 24-channel mode of operation, pcm-2 pulses from a second multiplexer are applied through the PCM IN-2 receptacle to the transmit circuits, where they are processed and interleaved with the pcm-1 pulses to provide a combined pcm output to the cable link. Timing pulses from the TD-660(*)/G are applied through TIM IN receptacle to the transmit circuits, where they are used for synchronization purposes.

b. Cable Input Circuits. The incoming pcm pulses from the cable link are applied through the FROM CABLE receptacle to the cable input circuits. The pcm pulses are conditioned and applied as received pcm pulses to the receive circuits. The circuits also generate received 2304-kHz timing pulses that are applied to the receive circuits. The timing pulses are synchronized to the incoming pcm pulses. The order wire signals imposed on the incoming pcm pulses are removed and routed to the order wire facilities as cable-in order wire signals.

c. Receive Circuits. The receive circuits process the incoming half-width RZ pulses into full-width nonreturn-to-zero (NRZ) pulses. The restored pcm pulses are applied to PCM OUT-1 and PCM OUT-2 receptacles. The output pcm pulses applied to both receptacles are identical. The 2304-kHz timing pulses applied to the receive circuits are used to generate 576-kHz timing pulses or 2304-kHz timing pulses that are synchronized to the output pcm pulses. The timing pulse outputs, which are either 576-kHz or 2304-kHz timing pulses, applied to TIM OUT-1 and TIM OUT-2 receptacles are identical. The dual pcm and timing pulse outputs can be applied to two TD-660(*)/G's, or similar equipment, connected to the TD-754/G.



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Figure 1-3. TD-754/G, Overall Block Diagram.

d Order Wire Facilities. The order wire facilities condition the audio output signals from a Headset Microphone H-91A/U connected to the TD-754/G and apply the signals to the transmit circuits for transmission. Incoming order wire signals from the receive circuits are conditioned and applied through the order wire facilities to the attached H-91A/U. A patch-through capability is contained in the order wire facilities. When two TD-754/G's are connected in the attended-repeater configuration, order wire signals from the incoming cable link are conditioned, applied to the attached H-91A/U, and applied to the outgoing cable link via the transmit circuits.

e. Power Supply Circuits. The power supply circuits generate the +25v, +12v, +5v, and -6v dc power for internal power distribution in the TD-754/G. The circuits also generate a 7.2v dc reference voltage that is used in the service facilities and generates the cable current that is applied to the cable link via the transmit circuits.

f. Service Facilities. The service facilities contain a monitor circuit and a cable fault locator circuit. The monitor circuit receives dc sample voltages (designated SF) from key circuit inputs and outputs in the TD-754/G. These SF voltages are used to develop an indication on the TEST ALIGN meter that shows the presence or absence of the selected signal. The cable fault locator circuit is used to isolate a faulty TD-206/G in the cable link.

1-16. Detailed Block Diagram Discussion

Figures 1-4 through 1-10 are the detailed block diagrams of the six functional circuits that make up the TD-754/G. Each of the functional circuits is described below.

a. Transmit Circuits (figure 1-4). In 6-, 12-, 24-, and 48-channel modes of operation, pcm-1 pulses from one external source are applied through PCM IN-1 receptacle on the rear panel to the pcm-1 input circuits on panel 12A4. In the 24-channel mode of operation, in addition to the pcm-1 pulse inputs, pcm-2 pulses from a second external source are applied through PCM IN-2 receptacle to the pcm-2 input circuits on panel 12A4.

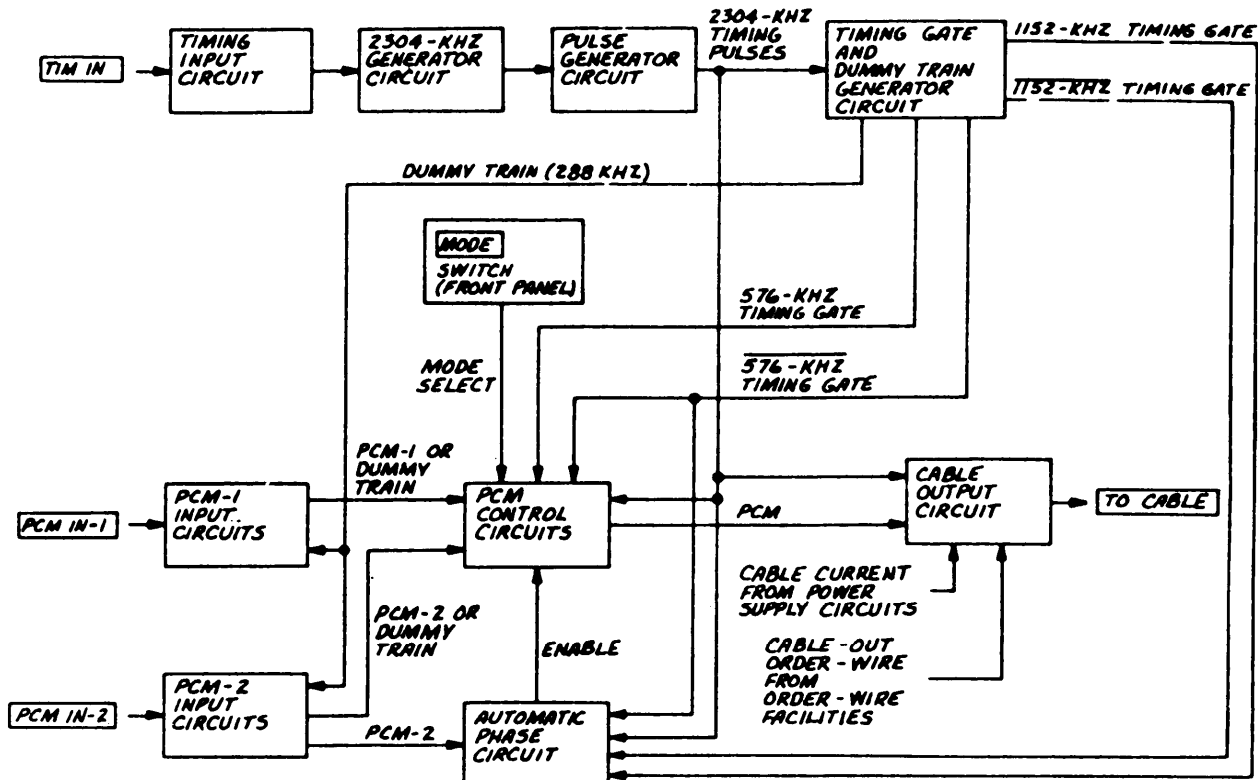
(1) In the pcm-1 input circuits, the pcm-1 pulses are conditioned and applied to the pcm control circuits. Dummy train pulses from the timing gate and dummy train generator circuits are continuously applied to the pcm-1 and pcm-2 input circuits. The dummy train pulses are automatically accepted and processed through the pcm-1 input circuit in place of the pcm-1 pulses when the pcm-1 pulse input to the TD-754/G is interrupted or missing.

(2) In 6- and 12-channel modes of operation, there is no pcm-2 pulse input to the pcm-2 input circuits. In these two modes of operation, the dummy train pulses are accepted and processed through the pcm-2 input circuits and applied to the pcm control circuits. In the 24-channel mode of operation, the pcm-2 pulse input is processed through the pcm-2 input circuits and applied to the pcm control circuits. If the pcm-2 pulse input is interrupted or missing, the dummy train pulses are accepted and processed through the pcm-2 input circuits. In the 24-channel mode of operation, pcm-2 pulses from the pcm-2 input circuits are also applied to the automatic phase circuit. The automatic phase circuit compares the phase relationship of the leading edge of the pcm-2 pulses with the timing gates to insure that the pcm-2 pulses are not sampled during pulse transition time in the pcm control circuits. When the proper phase is detected, an enable signal (1152- or 1152-kHz timing pulse) is applied to the pcm control circuits that permits the pcm-2 pulses to be correctly sampled in the pcm control circuits.

(3) In 6-, 12-, and 24-channel modes of operation, the pcm control circuits interleave the pulse outputs from the pcm-1 and pcm-2 input circuits at a 576-kHz rate and apply the mixed pcm pulses to the cable output circuit. In the 48-channel mode of operation, the pcm-1 pulses are gated through the pcm control circuits at a 2304-kHz rate and applied to the cable output circuits. The MODE switch on the front panel applies a mode select signal that inhibits the pcm-2 pulse input to the pcm control circuits in the 48-channel mode of operation. In the cable output circuit, the pcm pulses are converted into half-width RZ pulses at a 2304-kHz bit rate and then applied through the TO CABLE receptacle on the rear panel to the cable link.

(4) The cable-out order wire signals from the order wire facilities and the cable current from the power supply circuits are mixed with the pcm output from the cable output circuit.

(5) Timing pulses from the equipment supplying the pcm-1 pulses are applied through TIM IN receptacle on the rear panel to the timing input circuit. The timing pulses are conditioned in the timing input circuit and applied to the 2304-kHz generator circuit. A constant 2304-kHz sine wave is generated from the 2304-kHz generator circuit when 288-kHz, 576-kHz, 1152-kHz, or 2304-kHz timing pulses are applied to the generator circuit. The 2304-kHz sine wave is applied to the pulse generator circuit that produces the 2304-kHz timing pulses used in the transmit logic circuits. The 2304-kHz timing pulses applied to the timing gate and dummy train generator circuit are used to generate the dummy train pulses (288 kHz), the 576-kHz and 576-kHz timing gates, and the 1152- and 1152-kHz timing gates used in the transmit circuits. The 2304-kHz timing pulses are also applied to the pcm control circuits, the cable output circuit, and the automatic phase circuit.



NOTE :
 INDICATES PANEL MARKING.

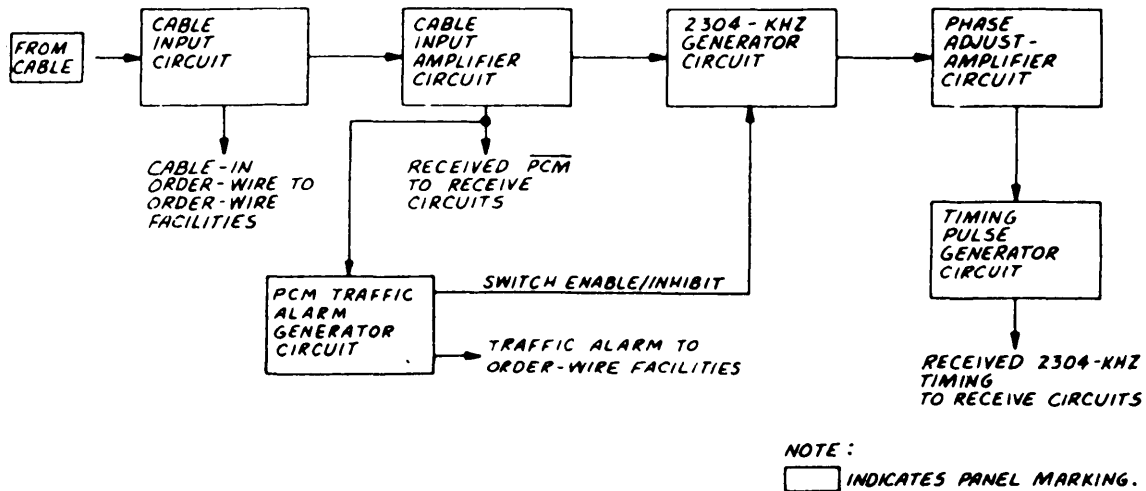
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Figure 1-4. Transmit Circuits, Block Diagram.

b. Cable Input Circuits (figure 1-5). The incoming pcm pulses from the cable link are applied through the FROM CABLE receptacle on the rear panel to the cable input circuit on panel 12A5. In the cable input circuit, the cable current is separated from the pcm pulses and routed to ground.

(1) In the cable input circuit, the cable-in order wire signals are separated from incoming pcm pulses and routed to the order wire facilities. The pcm pulses from the cable input circuit are amplified through the cable input amplifier circuit and applied to the 2304-kHz generator circuit. The received pcm pulses generated in the cable input amplifier circuit are applied to the pcm traffic alarm circuit and to the receive circuits on panel 12A6.

(2) The pcm pulses applied to the 2304-kHz generator circuit initiate a 2304-kHz sine wave output that is synchronized with the applied pcm pulses. The 2304-kHz sine wave output is applied to the phase adjust-amplifier circuit. The phase-adjust amplifier circuit contains a phase adjustment that properly positions the 2304-kHz sine wave input to the timing pulse generator to insure that the received 2304-kHz timing pulses from the timing pulse generator circuit are properly phased to the received pcm pulses for subsequent use in the receive circuits on panel 12A6.



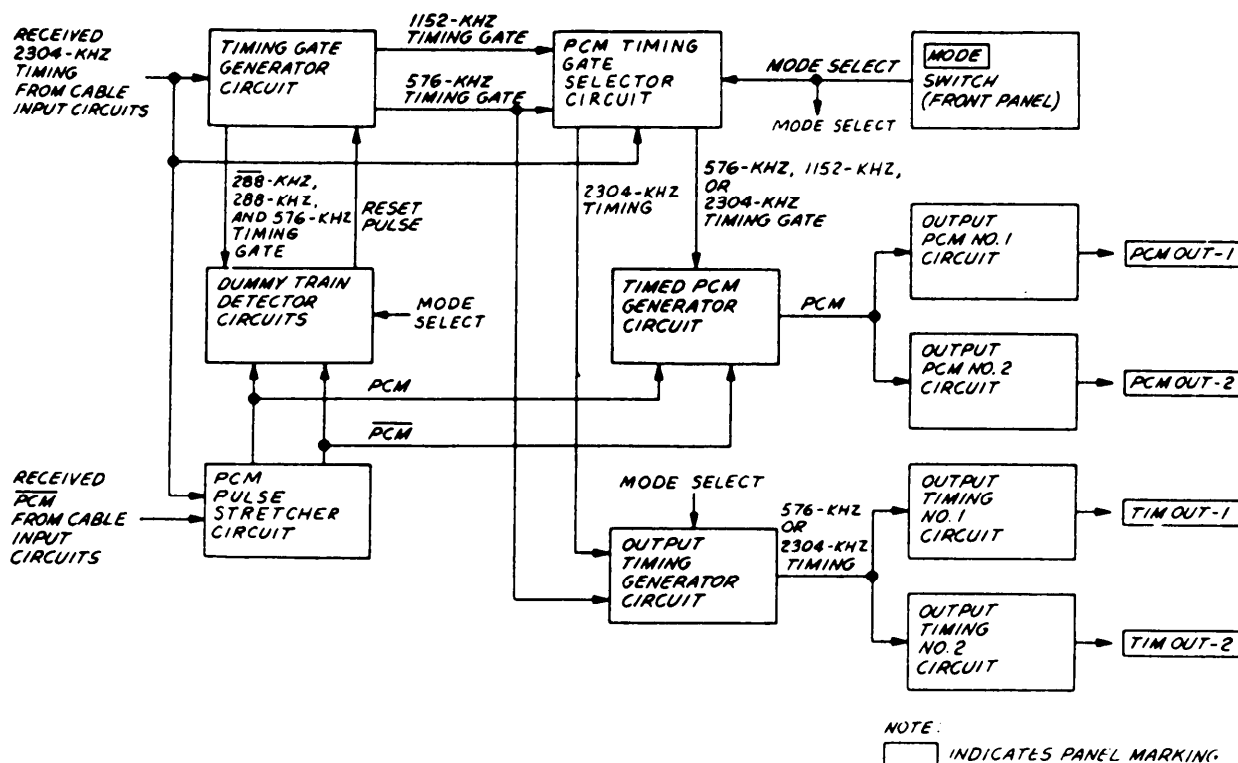
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Figure 1-5. Cable Input Circuits, Block Diagram.

(3) The pcm traffic alarm generator receives the traffic sample signal from the receive circuits. The traffic sample signal is present when pcm pulses are being received and processed through the cable input circuits and the receive circuits. When the traffic sample signal is removed, the pcm traffic alarm generator applies a low-level traffic alarm signal to the order wire facilities that initiates the audible and visual traffic alarm circuit. The pcm traffic alarm generator also generates a switch enable signal that covers the 2304-kHz generator circuit from a synchronous to an asynchronous circuit so that 2304-kHz generator circuit continues generating a 2304-kHz sine wave (free-running) output during the time the pcm pulses from the cable link are missing. When the traffic sample signal is reapplied to the pcm traffic alarm generator, a switch inhibit signal is applied to the 2304-kHz generator circuit that reverses the oscillator function and permits the incoming pcm pulses to again synchronize the 2304-kHz generator circuit.

c. *Receive Circuits* (figure 1-6). The receive circuits produce the timing pulses and full-width pcm pulses that are applied to the one or two TD-660(*)/G's, or similar equipment, connected to the TD-754/G.

(1) The received 2304-kHz timing pulses from the cable input circuits applied to the timing gate generator circuit are used to initiate and synchronize the 1152-kHz, 576-kHz, 288-kHz, and 288-kHz timing gates from the timing gate generator circuit. The 288-kHz, 288-kHz, and 576-kHz timing gates are applied to the dummy train detector circuits; the 576-kHz and 1152-kHz timing gates are applied to the pcm timing gate selector circuit; and the 576-kHz timing gate is also applied to the output timing generator circuit.



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Figure 1-6. Receive Circuits, Block Diagram.

(2) The received pcm pulses and received 2304-kHz timing pulses are applied to the pcm pulse stretcher circuit from the cable input circuits. The pcm pulse stretcher circuit converts the half-width pcm pulses to full-width (stretched) pcm and pcm pulses that are applied to the dummy train detector circuits and the timed pcm generator circuit. The dummy train detector circuits sample the pcm and pcm pulses for the presence and position of dummy train pulses when the MODE switch is in the 6/12 position. When dummy train pulses are detected and properly phased to the timing gates, there is no output from the circuits. When the dummy train pulses are detected and they have the wrong phase relationship to the timing gates, a reset pulse is generated and applied to the timing gate generator circuit. The reset pulse causes the timing gates to shift in phase with respect to the pcm pulses. The reset pulse is applied until the proper phase relationship is obtained between the timing gates and the dummy train pulses. When the proper phase relationship is obtained, dummy train pulses are automatically removed from the pcm pulse output from the timed pcm generator circuit. In the 24- or 48-channel mode of operation, the mode select signal from the MODE switch inhibits the dummy train detector circuits.

(3) The timed pcm generator circuit produces output pcm pulses at a bit rate of 576-kHz, 1152-kHz, or 2304-kHz as controlled by the timing gate input from the pcm timing gate selection circuit. The 576-kHz, 1152-kHz, or 2304-kHz timing gates from the pcm timing gate selector circuit are selected by the MODE switch on the front panel of the TD-754/G. When the MODE switch is in the 6/12 position, the 576-kHz timing gates are applied to the timed pcm generator circuit; in the 24 position, 1152-kHz timing gates are applied; and in the 48AR position, the 2304-kHz timing gates are applied. The output pulses from the timed pcm generator circuit are applied to the output pcm No. 1 and No. 2 circuits. The pcm outputs from the two circuits are identical. The pcm outputs are routed to the PCM OUT-1 and PCM OUT-2 receptacles on the rear panel of the TD-754/G for application to the one or two TD-660(*)/G's, or similar equipment, connected to the TD-754/G.

(4) The output timing generator circuit generates either 576-kHz or 2304-kHz timing pulses to the output timing No. 1 and No. 2 circuits. The timing output is selected by the MODE switch on the front panel. The MODE switch in the 6/12 and 24 positions causes 576-kHz timing gates to be generated and applied to the TIM OUT-1 and TIM OUT-2 receptacles on the rear panel for application to one or two TD-660(*)/G's, or similar equipment, connected to the TD-754/G. The MODE switch in the 48AR position causes 2304-kHz timing gates to be generated from the output timing generator circuit

d. Order Wire Facilities (figure 1-7). The order wire facilities on panels 12A2 and 12A3 process the incoming and outgoing order wire signals between the H-91A/U connected to the TD-754/G and the cable link. Order wire signals applied to one of two TD-754/G's connected as attended repeaters are processed and patched through to the other TD-754/G, where the order wire signals are further processed and transmitted to the adjacent cable link.

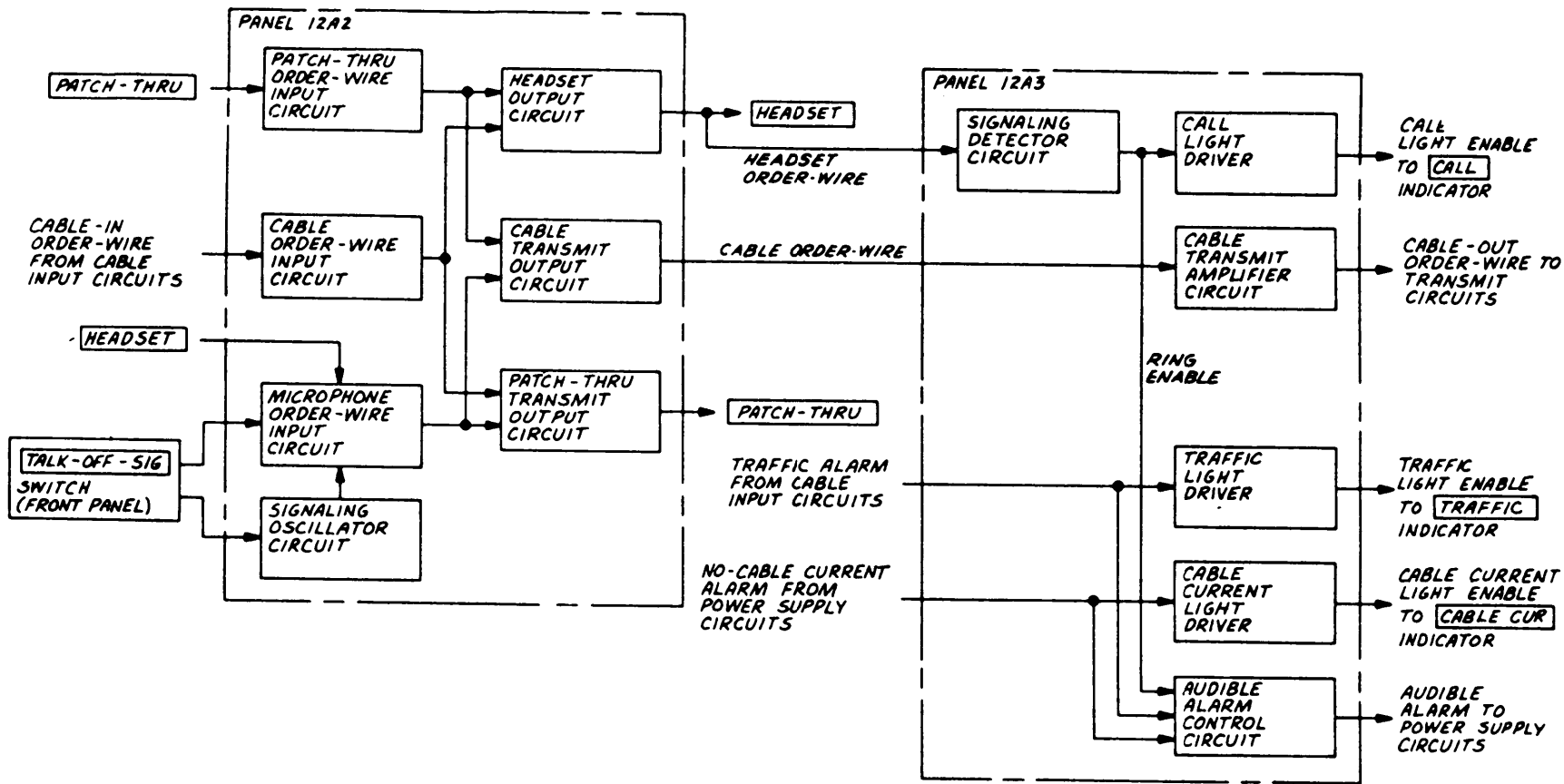
(1) Microphone order wire signals from an attached H-91A/U are applied through the HEADSET receptacle on the front panel of the TD-754/G to the microphone order wire input circuit when the TALK-OFF-SIG switch on the front panel is placed in the TALK position. When the TALK-OFF-SIG switch is placed in the SIG position, a ring signal from the signaling oscillator circuit is applied to the microphone order wire input circuit. The ring signal or microphone order wire signals from the microphone order wire input circuit are amplified in the patch-thru transmit output circuit and applied to the PATCH-THRU receptacle on the rear panel. When the TD-754/G is used in the attended-repeater configuration, the output signals at the PATCH-THRU receptacle are routed through the PATCH-THRU receptacle on the adjacent TD-754/G and applied to the patch-thru order wire input circuit. The output of the microphone order wire input circuit is also routed to the cable transmit output circuit. The amplified output of the cable transmit output circuit is applied to the cable transmit amplifier on panel 12A3. In the cable transmit amplifier, the signals are amplified and applied to the transmit circuits on panel 12A4, where the order wire signals are superimposed on the outgoing pcm pulses to the cable link.

(2) Incoming cable order wire signals from the cable link are applied from the cable input circuits on panel 12A5 to the cable order wire input circuit. The output of the cable order wire input circuit is applied to the patch-thru transmit circuit and processed as described in (1) above. The order wire output from the cable order wire input circuit is also applied to the headset output circuit. The amplified output of the headset output circuit is applied through the HEADSET receptacle on the front panel to the attached H-91A/U. The output of the headset output circuit is also applied to the signaling detector circuit on panel 12A3. When the ring signal (1600 Hz) is present in the order wire signals, the signaling detector circuit detects the 1600-Hz component and generates the ring enable signal that causes the call light driver to initiate the call light enable signal that lights the CALL indicator on the front panel. The ring enable signal is also applied to the audible alarm control circuit. The audible alarm control circuit, in turn, generates the audible alarm signal that causes the audible alarm horn on power supply assembly 12A1 to energize and produce the audible alarm.

(3) Order wire signals from an adjacent TD-754/G are applied through the PATCH-THRU receptacle on the rear panel to the patch-thru order wire input circuit when two TD-754/G's are connected as an attended repeater or when two TD-754/G's are connected as a remote multiplex terminal with drop and insert (D/I) facilities. The order wire signals from the patch-thru order wire input circuit are processed through the headset output circuit and cable transmit output circuit to the attached H-91A/U and to the outgoing cable link as described in (1) and (2) above.

(4) The traffic light driver generates a traffic light enable signal that lights the TRAFFIC indicator on the front panel when the traffic alarm signal is applied from the cable input circuits. The traffic alarm signal is also applied to the audible alarm control circuit to enable the audible alarm horn on power supply assembly 12A1.

Figure 1-7. Order Wire Facilities, Block Diagram.



NOTE :
 INDICATES PANEL MARKING.

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(5) The cable current light driver generates a cable current light enable signal that lights the CABLE CUR indicator on the front panel when the no-cable current alarm signal is applied from the power supply circuits on power supply assembly 12A1. The no-cable current alarm signal is also applied to the audible alarm control circuit to enable the audible horn on power supply assembly 12A1.

e. *Power Supply Circuits* (figure 1-8). The power supply circuits on power supply assembly 12A1 produce the dc voltages required to power the circuits in the TD-754/G. The cable constant current supply circuit that produces the cable current to power the TD-206/G's in the cable link, and a reference power supply circuit that produces a 7.2v dc reference voltage are also a part of the power supply circuits. The audible alarm horn mounted on power supply assembly 12A1 is also discussed below.

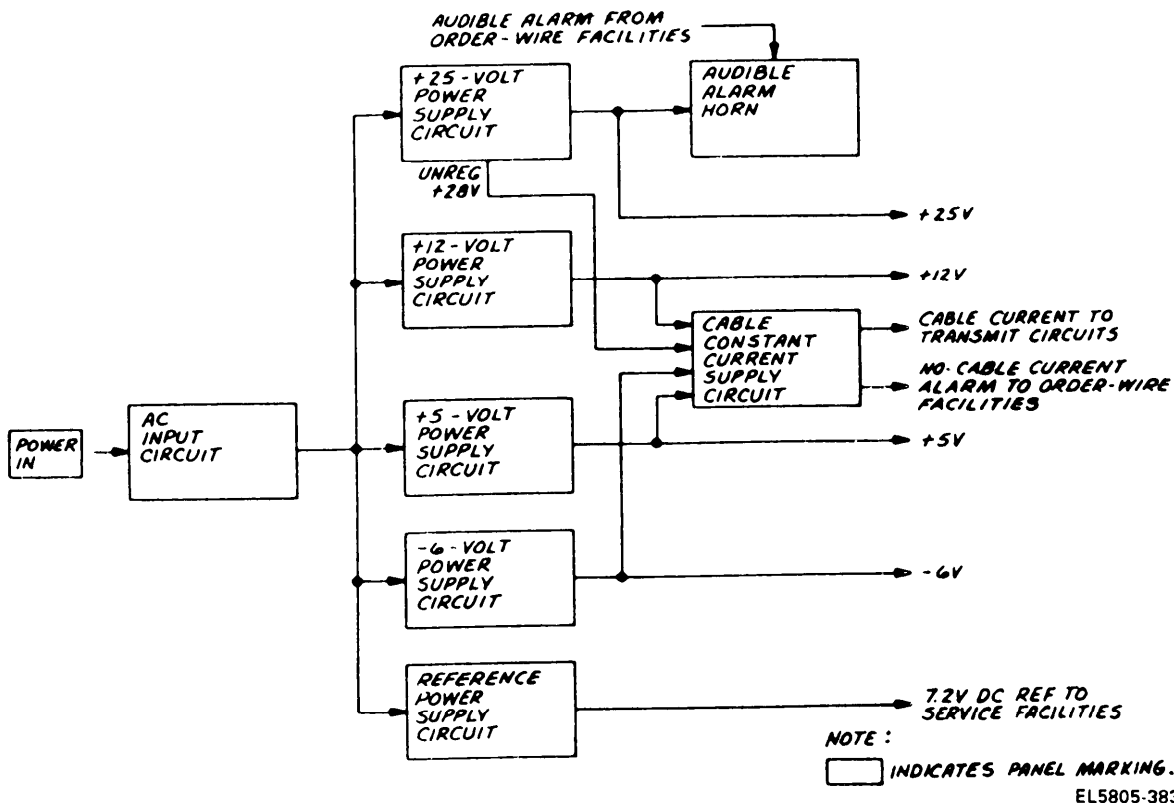


Figure 1-8. Power Supply Circuits, Block Diagram.

(1) The +28-volt power supply circuit produces unregulated +28 volts and regulated +25 volts. The unregulated +28 volts are applied to the cable constant current supply circuit. The regulated +25 volts are applied to the audible alarm horn and to circuits in the TD-754/G.

(2) The +12-volt power supply circuit generates regulated +12v dc that is applied as a power source to circuits in the TD-754/G. The +12v dc is also applied to the cable constant current supply circuit.

(3) The +5-volt power supply circuit generates regulated +5v dc that is applied as a power source to circuits in the TD-754/G. The +5v dc is also applied to the cable constant current supply circuit.

(4) The -6-volt power supply circuit generates regulated -6v dc that is applied as a power source to circuits in the TD-754/G. The -6v dc is also applied to the cable constant current supply circuit.

(5) The dc reference power supply circuit generates 7.2v dc (nominal voltage) that is applied to panel 12A7 in the service facilities for use as a dc reference voltage source.

(6) The cable constant current supply circuit provides regulated dc cable current that is applied through the transmit circuits on panel 12A4 to the cable link. The cable current provides the power to operate the TD-206/G in the cable link. A no-cable current alarm signal is generated and applied to the order wire facilities on panel 12A3 when the cable current output is interrupted.

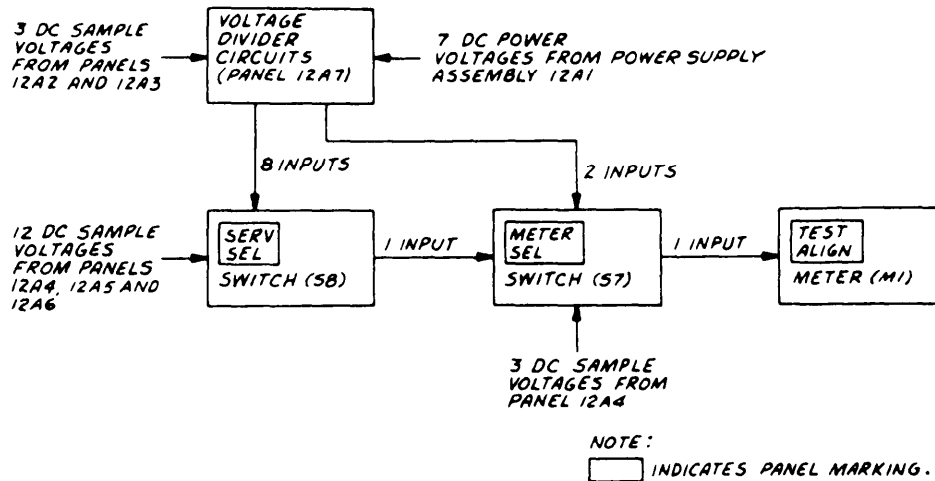
(7) The audible alarm horn sounds when the audible alarm signal is applied from the order wire facilities on panel 12A3.

f. Service Facilities. The service facilities contain the monitor circuit and the cable fault locator circuit. The monitor circuit uses the TEST ALIGN meter and controls on the front panel to provide a visual indication of the presence or absence of signal and power voltages at major test points throughout the TD-754/G. The cable fault locator circuit uses the TEST ALIGN meter and controls on the front panel to isolate a defective TD-206/G in the cable link.

(1) *Monitor circuit* (figure 1-9). The monitor circuit can check any one of eighteen dc sample voltages representing key signal points throughout the TD-754/G, or any one of seven dc power voltages in the TD-754/G. The three dc sample voltages from panels 12A2 and 12A3 and the seven dc power voltages from power supply assembly 12A1 are applied to voltage divider circuits on panel 12A7. Each of the dc voltages is divided down so that a low-level dc representative voltage is applied to contacts on SERV SEL switch S8 or to contacts on METER SEL switch S7. Any one of the 20 inputs to SERV SEL switch S8 can be selected and applied to TEST ALIGN meter M1 when METER SEL switch S7 is placed in the SERV FAC position. Five inputs can be selected directly by METER SEL switch S7 and applied to TEST ALIGN meter M1. When the amplitude of the dc sample voltage or power voltage is not proper or is missing, a faulty indication is obtained (out of the green band) on TEST ALIGN meter M1. When the proper dc sample voltage or dc voltage is present, a good indication (in the green band) is obtained on TEST ALIGN meter M1. To identify the dc sample signal and dc voltage inputs to the monitor circuit on the overall schematics, the letters "SF" and the switch position on SERV SEL switch S8 are listed after the signal name.

(2) *Cable fault locator circuit* (figure 1-10). Each TD-206/G has a built-in fault locator circuit that provides a fixed resistance in series with the cable link when the TD-206/G is faulty or deenergized. When the TD-206/G is operating normally, the resistance is shorted out. Once a TD-206/G fails, the TD-206G's that follow it in the cable link are deenergized, since their pcm pulse input is removed. Since the cable current is held constant, the high voltage output from the high voltage circuit must increase by an amount that is proportional to the number of TD-206/G's in the cable length that are deenergized. Therefore, by measuring the high voltage and substituting increments of the fixed resistance in series with the cable link, the defective TD-206/G can be isolated as explained in (a) through (c) below.

(a) The READ-ZERO SET-NORM OPR switch is placed in the ZERO SET position. This inhibits the pcm pulse output from the transmit circuits to the cable link. With no pcm pulses on the cable link, all the TD-206/G's are deenergized and their fixed resistances are in series with the cable link. Since the maximum resistance is in series with the cable link, the high voltage output from the high voltage circuit is maximum to maintain the constant cable current. At this time, the ZERO SET potentiometer is adjusted so that the input from the zero set circuit to TEST ALIGN meter M1 causes a midscale indication on the meter.



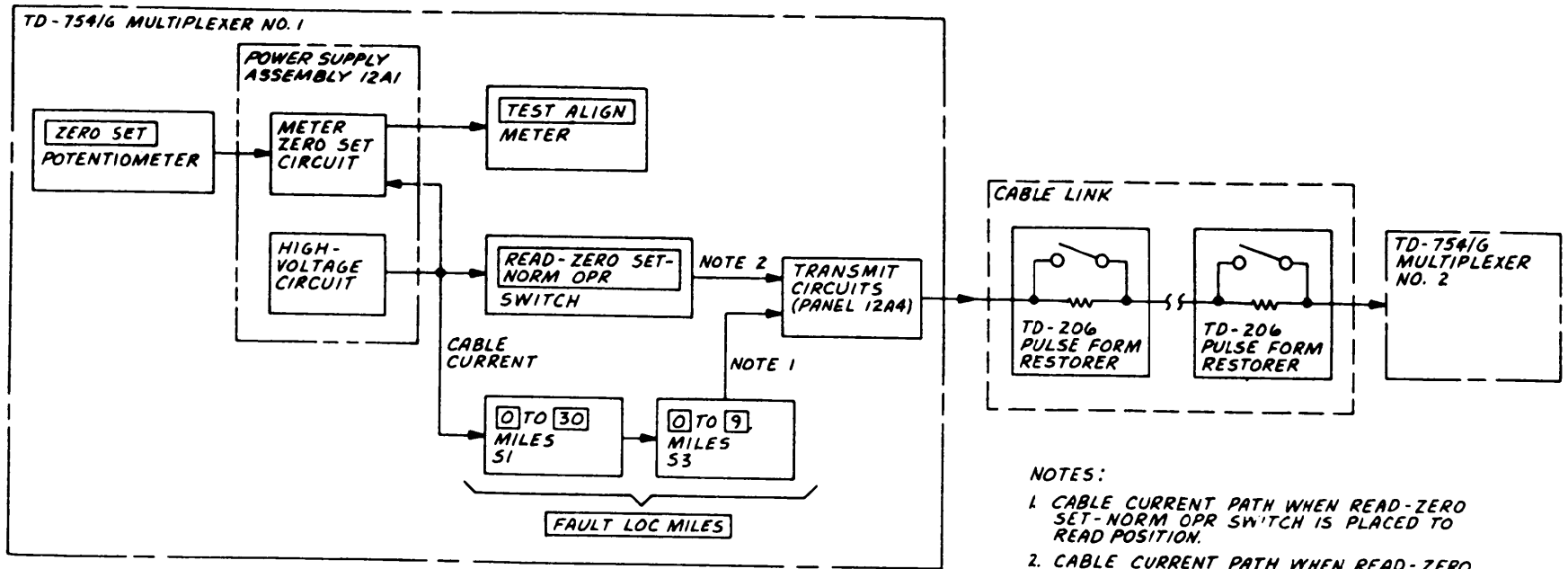
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Figure 1-9. Monitor Circuit, Block Diagram.

(b) Next, the READ-ZERO SET-NORM OPR switch is placed in the READ position. At this time, the traffic control signal is removed from the transmit circuits and pcm pulses are applied to the cable link. Also, the cable current applied to the transmit circuits is routed through FAULT LOC MILES switches S1 and S3. Each step of switch S3 adds a resistance in series with the cable current that represents the series fixed resistance of one deenergized or defective TD-206/G. Each step of switch S1 represents the series fixed resistance of 10 restorers.

(c) With pcm pulses being applied to the cable link, the TD-206/G's in front of the defective TD-206/G are energized and their series resistance in the cable link is shorted out. With FAULT LOC MILES switches S1 and S3 placed in their 0 positions, the amount of high voltage required to maintain the constant cable current decreases. Switches S1 and S3 are operated through their positions until a midscale indication is obtained on TEST ALIGN meter M1. When the proper indication on TEST ALIGN meter M1 is obtained, the resistance of the deenergized TD-206/G's in the cable link equals the total resistance in the cable length when all the TD-206/G's have been deenergized and the maximum high voltage is present. Therefore, the resistance added by switches S1 and S3 represents the number of TD-2-06/G's that are operating in front of the defective TD-206/G. Therefore, noting the position of switches S1 and S3 provides a visual indication of which TD-206/G in the cable link is defective.

Figure 1-10. Cable Fault Locator Circuit, Block Diagram.



NOTES:

1. CABLE CURRENT PATH WHEN READ-ZERO SET-NORM OPR SWITCH IS PLACED TO READ POSITION.
2. CABLE CURRENT PATH WHEN READ-ZERO SET-NORM OPR SWITCH IS PLACED TO NORM OPR AND ZERO SET POSITION.
3. INDICATES PANEL MARKING.

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1-17. Theory of Operation General Information

The detailed theory of operation is divided into the six functional circuits described in the block diagram discussions. To assist in the presentation and understanding of the theory of operation, the detailed circuits and stage names discussed in the following paragraphs are identified on their respective schematic diagrams.

Functional Circuit	Paragraph No.	Fig. No. Schematic Diagram
Transmit circuits	1-18	FO-5
Cable input circuits	1-19	FO-6
Receive circuits	1-20	FO-7
Order wire facilities	1-21	FO-3, FO-4
Power supply circuits	1-22	FO-2
Service facilities	1-23	FO-8

1-18. Transmit Circuits

a. General. The transmit circuits (figure FO-5) receive full-width pcm pulses and a master timing signal from a TD-660(*)/G, or similar equipment. In all modes of operation, the incoming pcm pulses are processed into positive half-width pulses and applied to the cable link at a 2304-kHz bit rate. The transmit circuits are mounted on panel 12A4. Figure 1-11 shows a typical timing diagram for the transmit circuits.

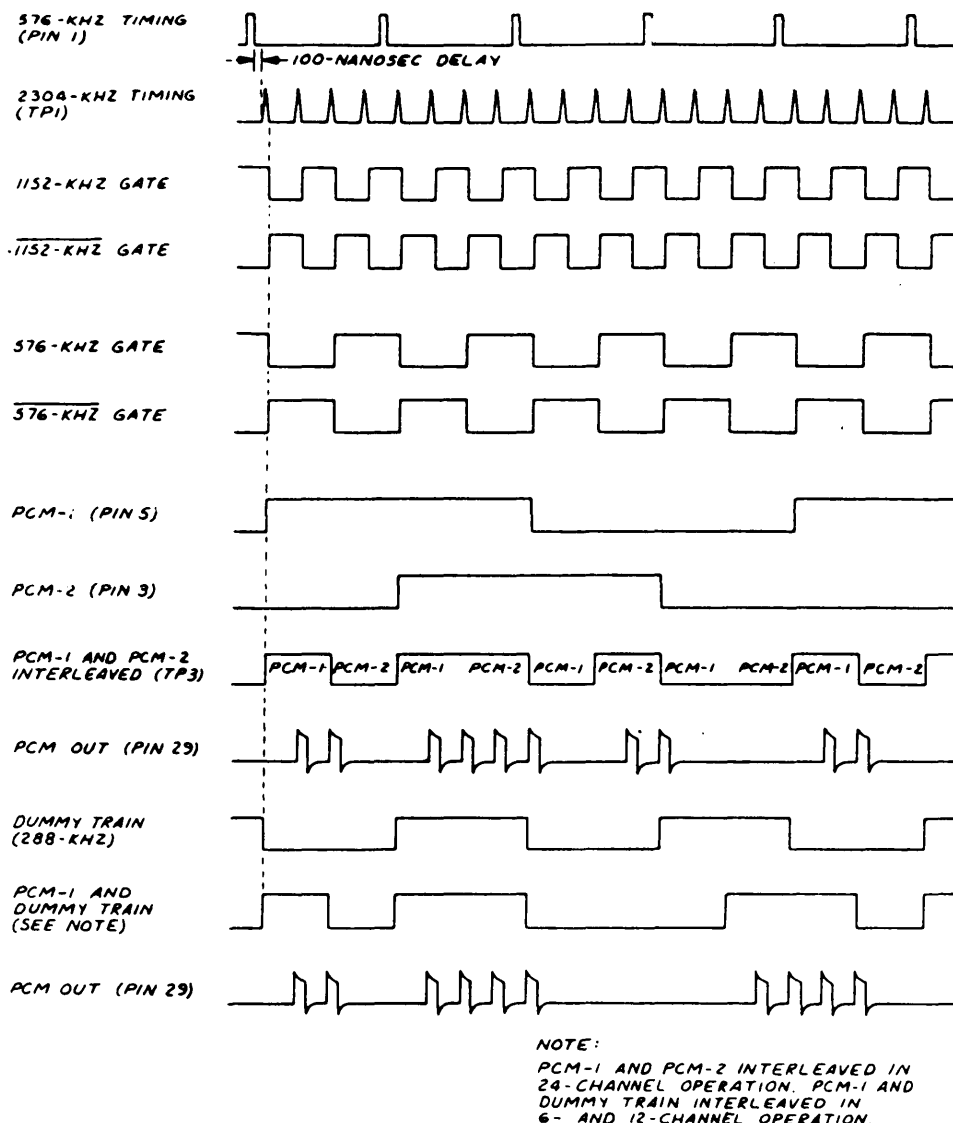
(1) In 6- and 12-channel modes of operation, one channel (pcm-1) of full-width pcm pulses is applied to the TD-754/G. The pcm pulses are converted to half-width pulses, interleaved with dummy train pcm pulses, and applied to the cable link.

(2) In the 24-channel mode of operation, two channels (pcm-1 and pcm-2) of full-width pcm pulses are applied to the TD-754/G. The pcm-1 and pcm-2 pulses are converted to half-width pulses, interleaved together, and then applied to the cable link.

(3) In the 48-channel mode of operation, one channel (pcm-1) of pcm pulses is applied to the TD-754/G. The pcm pulses are converted to half-width pulses, and then applied to the cable link.

(4) If the incoming pcm pulses are lost, the transmit circuits automatically generate dummy train pcm pulses to the cable link in all modes of operation. In all operations, the dummy train pcm pulses are a continuous series of logic 1's and 0's (1010. . .) generated at a 576-kHz bit rate.

(5) Cable-out order wire signals from panel 12A3 are applied to the transmit circuits, where they are superimposed on the pcm pulses for transmittal over the cable link.



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Figure 1-11. Transmit Circuits, Timing Diagram.

b. *Timing Input Circuit.* The applied timing pulses are applied from an external source to the TD-754/G through TIM IN receptacle J2 on the rear panel. The timing pulses from J2 are applied through contacts on READ-ZERO SET-NORM OPR switch S2 on the front panel to pin 1 on panel 12A4 when the switch is in the NORM OPR position. The positive-going timing pulses have an amplitude of approximately 2 volts. They have a base voltage of approximately -2 volts and a peak voltage of approximately 0 volt.

(1) *Differential amplifier Q1, Q2.* The positive-going timing pulses are applied through pin 1 to differential amplifier Q1, Q2. Each timing pulse biases Q1 into conduction and Q2 into cutoff. The negative-going pulse output from Q1 is applied to Z2A and Z2B in the timing gate and dummy train generator circuit, and to FL1 in the 2304-kHz generator circuit, The positive-going pulse from Q2 is applied to timing peak detector Q14.

(2) *Timing peak detector Q14.* Timing peak detector Q14 produces a dc sample voltage (timing sample) that is applied to the TIM IN contact on METER SEL switch S7 on the front panel when timing pulses are being received. When the dc sample voltage is developed, an indication in the green band is obtained on TEST ALIGN meter M1 when METER SEL switch S7 is placed in the TIM IN position.

c. *2304-Hz Generator Circuit.* A constant 2304-kHz sine wave is generated from 2304-kHz filter FL1 when 2304-kHz, 1152-kHz, 576-kHz, or 288-kHz timing pulses are applied. The 2304-kHz signal from FL1 is applied through emitter follower Q3 and 100-nanosecond delay line DL1 to amplifier Q4. The 100-nanosecond delay insures that the incoming pcm-1 pulses are received and have obtained a stabilized condition when the timing gates are applied to the pcm sample circuits. The amplified 2304-kHz signal from Q4 is applied through emitter follower Q5 to Q6 in the pulse generator circuit.

d. *Pulse Generator Circuit.* The 2304-kHz sine wave from Q5 in the 2304-kHz generator circuit changed into 2304-kHz positive-going timing pulses in the pulse generator circuit. Pulse shaper Q6, Q7 produces a positive pulse output each time the positive-going portion of the incoming sine wave signal crosses the zero potential level. This results in a positive-going pulse every 0.434 microsecond. The positive-going timing pulses, which are approximately 0.1 microsecond wide, are applied through emitter follower Q8 to Z2A in the timing gate and dummy train generator circuit, to Z5 in the cable output circuits, to Z6B in the automatic phase circuit, and to Z6A in the pcm control circuits.

e. *Timing Gate and Dummy Train Generator Circuit.* The 1152-kHz generator Z2A produces 1152-kHz and 1152-kHz timing gates. The 1152-kHz timing gates are applied to Z8A in the automatic phase circuit. The 1152-kHz timing gates are applied to 576-kHz generator Z2B and to Z8B in the automatic phase circuit. The 576-kHz generator Z2B produces 576-kHz and 576-kHz timing gates. The 576-kHz timing gates are applied to Z6A and Z4D in the pcm control circuits and to Z6B in the automatic phase circuit. The 576-kHz timing gates are applied to dummy train generator Z3A and to Z4B and Z7 in the pcm control circuits. Dummy train generator Z3 produces a 288-kHz pulse output from which the dummy train pulses are decoded. The dummy train pulses are a continuous series of 1010 generated by sampling the 288-kHz pulses at a 576-kHz rate. Z2A and Z2B are initially placed to their set condition by the first negative-going pulse from Q1 in the timing input circuit. This insures that the timing gates from Z2A and Z2B are properly synchronized with the applied reference timing signals. Each generator changes state on the negative-going portion of each applied pulse.

f. *PCM-1 Input Circuits.* A pcm-1 pulse input is applied from a TD-660(*)/G, or similar equipment, to PCM IN-1 receptacle J1 on the rear panel of the TD-754/G. The pcm-1 pulses are routed from J1 to pin 5 on panel 12A4.

(1) *Differential/amplifier Q9, Q10.* The positive-going pulses applied to differential amplifier Q9, Q10 have an amplitude of approximately 2 volts. The pcm pulses have a base voltage of approximately -2 volts and a peak voltage of approximately 0 volt. Each incoming pulse biases Q9 into conduction and Q10 into cutoff. The negative-going pulses from Q9 are applied to pcm-1 traffic detector Q11, Q12, and the positive-going pulses from Q10 are applied to pcm-1 traffic detector Q11, Q12, and the positive-going pulses from Q10 area applied to pcm-1/dummy train control gate Z1A. The pulse output from Q10 is level shifted so that a logic 0 is 0 volt and a logic 1 is approximately +5 volts dc.

(2) *Traffic detector Q11, Q12.* The negative-going pcm pulses from differential amplifier Q9, Q10 cause C10 to charge and remain negatively charged as long as pcm pulses are being applied. A negative voltage across C10 biases Q11 into cutoff and Q12 and into conduction. This condition applies a constant logic 1 (enable) from Q11 to Z1A and a logic 0 (inhibit) from Q12 to Z1B as long as pcm pulses are present. When pcm pulses are missing, C10 is discharged, Q11 is biased into conduction, and Q12 is biased into cutoff. This condition applies a constant logic 0 to Z1A and a logic 1 to Z1B as long as pcm pulses are missing. When cable

fault isolation procedures are being performed and READ-ZERO SET-NORM OPR switch S2 on the front panel is placed in the READ position, a ground signal (logic 0) is applied through pin 2 on panel 12A4 to CR8 in the base circuit of Q11. The logic 0 (0 volt) prevents C10 from charging and driving Q11 into cutoff when pcm pulses are being applied to the circuit. Therefore, placing switch S2 in the READ position inhibits the incoming pcm-1 pulses and enables the dummy train pulses in the TD-754/G. When pcm pulses are being applied and Q11 is cut off, the logic 1 voltage level is also applied as a dc sample voltage (pcm-1 sample) to the PCM IN-1 input on METER SEL switch S7 on the front panel. When pcm pulses are being applied to the transmit circuits, an indication in the green band is obtained on TEST ALIGN meter M1 when METER SEL switch S7 is placed in the PCM IN-1 position.

(3) Pcm-1/dummy train control gate Z1A, Z1B. Gate Z1A passes pcm-1 pulses when a logic 1 from traffic detector Q11, Q12 is applied to Z1A-2. The pcm-1 negative-going pulses from Z1A are applied to pcm-1/dummy train mix peak detector Q13 and to Z4A in the pcm control circuits. When pcm-1 pulses are not being applied to the TD-754/G, a logic 0 from traffic detector Q11, Q12 inhibits Z1A and a logic 1 is applied to Z1B-5. The logic 1 to Z1B permits the 288-kHz pulses (dummy train) to pass through Z1B and be applied to pcm-1/dummy train mix peak detector Q13 and to Z4A in the pcm control circuits.

(4) *Pcm-1/dummy train mix peak detector Q13.* Pcm-1/dummy train mix peak detector Q13 produces a dc sample voltage (mix in) that is applied to the A input on SERV SEL switch S8 on the front panel when pcm-1 or dummy train data pulses are present. When the dc voltage is developed, an indication in the green band is obtained on TEST ALIGN meter M1 when SERV SEL switch S8 is placed in the A position and METER SEL switch S7 is placed in the SERV FAC position.

g. PCM-2 Input Circuits. The pcm-2 input circuits consist of differential amplifier Q15, Q16, traffic detector Q17, Q18, and pcm-2/dummy train control gate Z1C, Z1D. The operation of these circuits is similar to the operation of the pcm-1 input circuits described in f above. The pcm-2 pulses are applied only to the circuits in the 24-channel mode of operation. In 6-, 12- and 48-channel modes of operation, only dummy train pulses are developed from pcm-2/dummy train control gate Z1C, Z1D and applied to Z6A in the pcm control circuits.

h. PCM Control Circuits. The pcm control circuits receive pcm-1 and pcm-2 pulses and interleave the pulses at a 576-kHz bit rate in the 6-, 12-, and 24-channel modes of operation. In the 48-channel mode of operation, the pcm-2 pulse input is inhibited and the pcm-1 pulses are processed through the circuits at their 2304-kHz bit rate.

(1) *Pcm-1 sampler Z4A, Z4B.* In 6-, 12- and 24-channel modes of operation, Z4A produces a logic 1 or a logic 0 output to Z5 in the cable output circuit during 576-kHz gate time. In the 48-channel mode of operation, Z4A processes logic data at the 2304-kHz rate, independent of internal timing gates. Placing MODE switch S4 on the front panel in the 6/12 or 24 position applies a logic 1 (+5 volts) through pin 14 on panel 12A4 to Z4B-5. This causes Z4B to produce a logic 1 (enable) to Z4A during 576-kHz gate time, and a logic 0 (inhibit) to Z4A during 576-kHz gate time. Placing MODE switch S4 in the 48 position applies a logic 0 (ground) through pin 14 to Z4B, which causes Z4B to produce a constant logic 1 to Z4A. A logic 1 from Z1A, Z1B in the pcm-1 input circuits applied to Z4A-1 simultaneously with a logic 1 applied to Z4A-2 causes a logic 0 output to Z5 in the cable output circuit.

(2) *Pcm-2 phase control Z6A*. In the 48-channel mode of operation, a logic 0 is applied to pcm-2 phase control Z6A-3 that inhibits the pcm-2 circuits. In 6-, 12-, and 24-channel modes of operation, a logic 1 is applied to Z6A-3. When incoming pcm-2 pulses are properly phased to the timing gates, an enable (logic 1) signal is applied to Z6A-5 during 1152-kHz or 1152-kHz gate time from the automatic phase circuit. The 576-kHz and 2304-kHz timing gates are applied to Z6A-2 and Z6A-4. These conditions permit logic 0 pulses from Z1C, Z1D in the pcm-2 input circuits to generate logic 1 pcm-2 pulses from Z6A to pcm-2 pulse generator Z7 during 576-kHz gate time in the 6-, 12-, and 24-channel modes of operation. In the 48-channel mode of operation, Z6A produces a continuous logic 1 output to Z7. The output from Z6A during 576-kHz gate time is always a logic 1.

(3) *Pcm-2 pulse generator Z7*. A logic 1 applied to pcm-2 pulse generator Z7 has no effect on Z7. A logic 0 pulse from Z6A during 576-kHz gate time sets Z7. Once Z7 is set, it remains set and produces a logic 1 output to Z4C until the trailing edge of the 576-kHz timing gate is applied to Z7-2. When the negative-going trailing edge of the 576-kHz timing gate occurs, Z7 is reset and the output from Z7 becomes a logic 0 and remains a logic 0 until the next logic 0 is applied from Z6A to Z7.

(4) *Pcm-2 mix peak detector Q24*. Pcm-2 mix peak detector Q24 produces a dc sample voltage (pcm-2 mix in) that is applied to the B input on SERV SEL switch S8 on the front panel when pcm-2 output pulses from Z7 are present. When the dc sample voltage is developed, an indication in the green band on TEST ALIGN meter MI is obtained when SERV SEL switch S8 is placed in the B position and METER SEL switch S7 is placed in the SERV FAC position.

(5) *PCM-2 sampler Z4C, Z4D*. In 6-, 12-, and 24-channel modes of operation, Z4C produces a logic 1 or a logic 0 output to Z5 in the cable output circuit during 576-kHz gate time. The 576-kHz timing gate applied to Z4D causes a logic 1 (enable) to be applied to Z4C during 576-kHz gate time, and a logic 0 (inhibit) to be applied during 576-kHz gate time. The logic output from Z4C remains a logic 1, except when a logic 1 is applied to Z4C from Z7 during 576-kHz gate time. At this time, a logic 0 is applied from Z4C to Z7. In the 48-channel mode of operation, a constant logic 0 applied to Z4C from Z7 inhibits the stage and causes a constant logic 1 to be applied to Z5 in the cable output circuit from Z4C.

(6) *Pcm mix out peak detector Q23*. Pcm mix out peak detector Q23 produces a dc sample voltage (pcm mix out) that is applied to the C input on SERV SEL switch S8 on the front panel when pcm-1, pcm-2, and/or dummy train pulses are present at the output of Z4A or Z4C. When the dc sample voltage is developed, an indication in the green band is obtained on TEST ALIGN meter M1 when SERV SEL switch S8 is placed in the C position and METER SEL switch S7 is placed in the SERV FAC position.

i. Cable Output Circuit. The cable output circuit changes all pcm pulses into half-width pulses at the 2304-kHz bit rate, conditions the pulses, and then applies them to the output cable link.

(1) *Pulse generator Z5*. Pulse generator Z5 is a one-shot multivibrator that produces negative going half-width (200 ±30-nanosecond) pulses from the applied pcm-1 and/or pcm-2 pulses. In the 48-channel mode of operation, one negative-going pulse is generated for each pcm-1 logic 1 pulse applied from Z4A. In 6-, 12-, and 24-channel modes of operation, Z5 generates two pulses each time a logic 1 is applied during 576-kHz or 576-kHz gate time. Pulse generator Z5 is triggered into conduction when the negative-going trailing edge of the 2304-kHz timing pulse occurs and a logic 1 pcm-1 or pcm-2 pulse is applied simultaneously to Z5-4.

(2) *Emitter follower Q20 and amplifier Q21*. Each applied half-width pulse biases emitter follower Q20 into cutoff for the duration of the pulse. When Q20 cuts off, amplifier Q21 conducts and current flows through the building-out network and the primary winding of T1 to develop the pcm pulse output to the cable link. The output from Q1 is also applied to cable pcm output peak detector Q22.

(3) *Building-out network.* The building-out network attenuates the output pulses when the adjacent output cable in the cable link is less than 1 mile in length. This prevents overdriving the TD-206/G's in the cable link. CABLE MILES switch S1 is used to switch in one of three resistances when the cable length to the TD-206/G is less than 1 mile, or to switch in a direct connection between Q21 and T1 when the cable length is 1 mile. Resistor R48 is the equivalent resistance of a 3/4-mile length of cable and is switched into the circuit (switch position 1/4) when the cable length to the TD-206/G is 1/4 mile. Resistor R47 is the equivalent resistance of 1/2 mile length of cable and is switched into the circuit (switch position 1/2) when the cable length is 1/2 mile. Resistor R46 is the equivalent resistance of a 1/4-mile length of cable and is switched into the circuit (switch position 3/4) when the cable length is 3/4 mile. The cable current from power supply assembly 12A1 and the order wire signals from panel 12A3 are combined on the rear of the front panel and applied through pin 28 on panel 12A4 to T1-6. The order wire signals and cable current are added to the pcm pulses and applied through pin 29 on panel 12A4 to TO CABLE receptacle J9 on the rear panel. The pcm output pulses have a pulse width of 180 to 230 nanoseconds at their 50-percent points. The pulse amplitude is dependent on the position of switch S1 in the building-out network. In switch position 1, the pcm pulses have an amplitude of approximately 3.7 volts peak to peak. In switch position 3/4, the pcm pulses have an amplitude of approximately 1.5 volt peak to peak. In switch position 3/4, the pcm pulses have an amplitude of approximately 1.5 volt peak to peak. In switch position 1/2, the pcm pulses have an amplitude of approximately 0.7 volt peak to peak. In switch position 1/4, the pcm pulses have an amplitude of approximately 0.45 volt peak to peak.

(4) *Cable pcm output peak detector Q22.* Cable pcm output peak detector Q22 produces a dc sample voltage (output pcm) that is applied to the D input on SERV SEL switch S8 on the front panel when pcm pulses are present at the output of amplifier Q21. When the dc voltage is developed, an indication in the green band is obtained on TEST ALIGN M1 when SERV SEL switch S8 is placed in the D position and METER SEL switch S7 is placed in the SERV FAC position.

j. Automatic Phase Circuit. The incoming pcm-1 data pulses from an external source and the timing gates generated in the TD-754/G are synchronized, since both are synchronized to the external timing input to the TD-754/G. Because of the different system configurations in which the TD-754/G can be connected, it is possible that the phase relationship between the timing gates and pcm-2 pulses may not be properly synchronized. The automatic phase circuit checks for proper phase relationship between pcm-2 pulses and the timing gates by looking for pulse transition of the pulses occurring during a sample time. If pulse transition during a sample time is detected, the sampling time is automatically shifted by 0.434 microsecond. This insures that pulse transition is complete prior to sampling the pcm-2 pulses.

(1) *Transition pulse amplifier Q19.* Transition pulse amplifier Q19 produces a positive 200-nanosecond pulse whose leading edge is in coincidence with the leading edge of the negative-going pcm-2 pulses applied from differential amplifier Q15, Q16. The positive pulses from Q19 are applied to comparison gate Z6B.

(2) *Comparison gate Z6B.* Comparison gate Z6B produces a logic 0 pulse to flip-flop Z3B when all inputs to it are in coincidence. When the pcm-2 pulses are in the proper phase relationship with the timing gates, comparison gate Z6B-13 receives a logic 0 from combination output gate Z8A, Z8B during pulse transition time that keeps Z6B inhibited. When the pcm-2 pulses are out of phase with the internal timing gates, comparison gate Z6B receives a logic 1 from Z8A, Z8B during pulse transition time. This permits Z6B to produce a logic 0 to the input of flip-flop Z3B when all four input signals are in coincidence.

(3) *Flip-flop Z3B.* Flip-flop Z3B has a logic 1 output from pin 6 and a logic 0 output from pin 5, or a logic 0 output from pin 6 and a logic 1 output from pin 5. The logic outputs from pins 5 and 6 to combination output gate Z8A, Z8B switch each time a logic 0 pulse is applied to Z3B and Z6B.

(4) *Combination output gate Z8A, Z8B.* Combination output gate Z8A, Z8B generates a 1152-kHz or 1152-kHz gate that is applied to comparison gate Z6B and to Z6A in the pcm control circuits. If the 1152-kHz or 1152-kHz gate applied to comparison gate Z6B is in coincidence with a transition pulse applied to Z6B during 2304-kHz and 576-kHz gate time, the logic 1 and 0 outputs to Z8A-2 and Z8B-4 switch as described in (2) and (3) above. Switching the logic inputs to Z8A and Z8B from Z3B also switches the gate input to Z6B. For example, if a 1152-kHz gate from Z8A, Z8B is applied to Z6B in coincidence with a transition pulse, the output from Z8A, Z8B is switched so that the 1152-kHz gate is applied to Z6B. This switch now applies a logic 0 to Z6B in coincidence with the transition pulse to hold Z6B inhibited. The switch in outputs from Q8A, Q8B also selects the gate time (1152-kHz or 1152-kHz) that Z6A can be enabled. This ensures that a pcm-2 pulse applied to Z6A is not sampled during its transition time.

1-19. Cable Input Circuits

a. *General.* The cable input circuits (figure FO-6) on the TD-754/G receive incoming pcm pulses from the cable link. In the cable input circuits, the pcm pulses are amplified, reshaped, and then applied as received pcm pulses to the receive circuits on panel 12A6. Received 2304-kHz timing pulses are also generated in the cable input circuits and applied to the receive circuits. Cable-in order wire signals are separated from the pcm pulses and the signals are applied to the order wire circuits on panel 12A2. The cable input circuits are mounted on panel 12A5.

b. *Cable Input Circuit.* The pcm pulses from the cable link are applied through FROM CABLE receptacle J8 on the rear panel and filter FL8 mounted on the TD-754/G chassis to pin 28 on panel 12A5. The cable-in order wire signals and the dc cable current are routed through chokes L1, L2, and L3 to pin 10 on panel 12A5. From pin 10, the order wire signals are routed to the order wire facilities on panel 12A2. The high frequency pcm pulses are routed through capacitor C1 to the building-out network consisting of CABLE MILES switch S1 and resistors R1, R2, and R3. CABLE MILES switch S1 is used to switch in one of three resistances when the cable length to the TD-206/G is less than 1 mile, or to switch in a direct connection when the cable length is 1 mile. Resistor R1 is the equivalent resistance of a 1/4 -mile length of cable and is switched into the circuit (switch position 3/4) when the cable length to the TD-206/G is 3/4 mile. Resistor R2 is the equivalent resistance of 1/2-mile length of cable and is switched into the circuit (switch position 1/2) when the cable length is 1/2 mile. Resistor R3 is the equivalent resistance of a 3/4-mile length of cable and is switched into the circuit (switch position 1/4) when the cable length is 1/4 mile. Cable input amplifier Z1 can function properly with incoming pulse amplitudes of 20 to 50 millivolts. Choke L5 and capacitor C2 form a resonant circuit at 2304 kHz that permits the desired pcm pulses to develop a voltage across resistor R4, and also provides a path to ground for any undesired ac noise voltages.

c. *Cable Input Amplifier Circuit.* The pcm pulses are routed through C3 to cable input amplifier Z1. In Z1, the pcm pulses are amplified and reshaped. The negative-going pcm pulses from Z1 have a pulse width of 260 \pm 40 nanoseconds at their 50-percent points. The pulse amplitude is approximately 2.5 volts, starting from a base voltage of approximately +2.5 volts to a negative peak voltage of approximately 0 volt. The received pcm pulses from Z1 are applied to the 2304-kHz generator circuit, to the pcm traffic alarm circuit, and they are also applied through pin 22 on panel 12A5 to the receive circuits on panel 12A6.

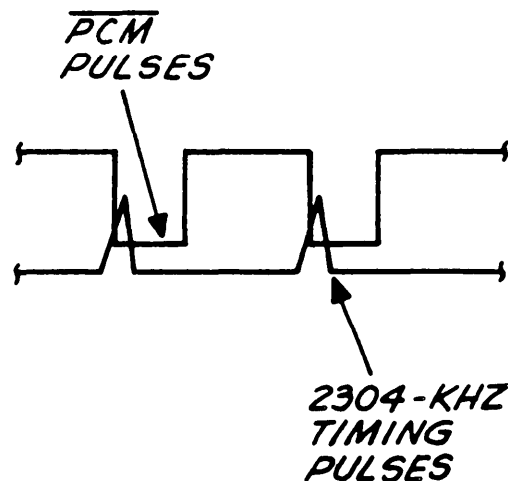
d. 1304-kHz Generator Circuit.

(1) The 2304-kHz generator circuit produces 2304-kHz timing pulses that are synchronized by the pcm pulses that have a 2304-kHz bit rate. The negative-going pcm pulses from Z1 are applied through emitter follower Q3 to drive 2304-kHz crystal filter FL1. The 2304-kHz sine wave output from FL1, which is synchronized with the pcm pulses, is applied through emitter follower Q4 to T1 in the phase adjust-amplifier circuit.

(2) Oscillator Q11 is enabled and generates a 2304-kHz output (free-running) in conjunction with 2304-kHz crystal filter FL1 and emitter follower Q4 when incoming pcm pulses are missing. Oscillator Q11 is cut off when pcm pulses are applied to the circuits, since switch Q12 is also cut off. Switch Q12 is held in cut off by Q14 in the pcm traffic alarm generator circuit. When pcm pulses are missing, Q14 goes into cutoff and the bias voltage to the base of Q12 goes negative, driving Q12 into conduction. When Q12 conducts, the bias voltage to the base of oscillator Q11 goes positive, permitting Q11 to conduct, and thus enabling the oscillator function.

e. Phase Adjust-Amplifier Circuit.

(1) *Phase adjust circuit.* The 2304-kHz sine wave from the 2304-kHz generator circuit is applied to the primary winding of transformer T1. The sine wave output from the secondary winding of T1 is applied through capacitor C13 and phase-adjust potentiometer R20 to the base of emitter follower Q5 in the amplifier circuit. Potentiometer R20 is adjusted while the negative-going pcm pulses at TP1 and the received 2304-kHz timing pulses at TP3 are monitored, so that the trailing edge of the timing pulse occurs slightly after the leading edge of the pcm pulse (figure 1-12). This adjustment insures that the pcm pulses applied to the receive circuits are properly synchronized with the timing pulses and the timing gates generated in the receive circuits.



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Figure 1-12. Phase Adjustment, Simplified Waveform Diagram.

(2) *Amplifier circuit.* The 2304-kHz sine wave is applied through emitter follower Q5 to amplifier Q6. The amplified 2304-kHz sine wave from Q6 is applied through emitter follower Q7 to the pulse generator circuit. Choke L6 and capacitor C15 in the emitter circuit of Q7 form a series resonant circuit that passes the desired 2304-kHz sine wave and appears as a high impedance to block undesired spurious noise voltages.

f. Timing Pulse Generator Circuit.

(1) *Pulse generator.* The 2304-kHz sine wave from emitter follower Q7 is applied to pulse generator Q8, Q9. Pulse generator Q8, Q9 produces the positive-going received 2304-kHz timing pulses that are applied through emitter follower Q10 to peak detector Q1, Q2. The received 2304-kHz timing pulses from Q10 are also applied through pin 2 on panel 12A5 to the receive circuits on panel 12A6. The received 2304-kHz timing pulses have a pulse width of 60 ± 20 nanoseconds at the 50-percent points. The positive-going pulses rise from a base voltage of approximately -1.2 volts to a peak voltage of approximately +6 volts.

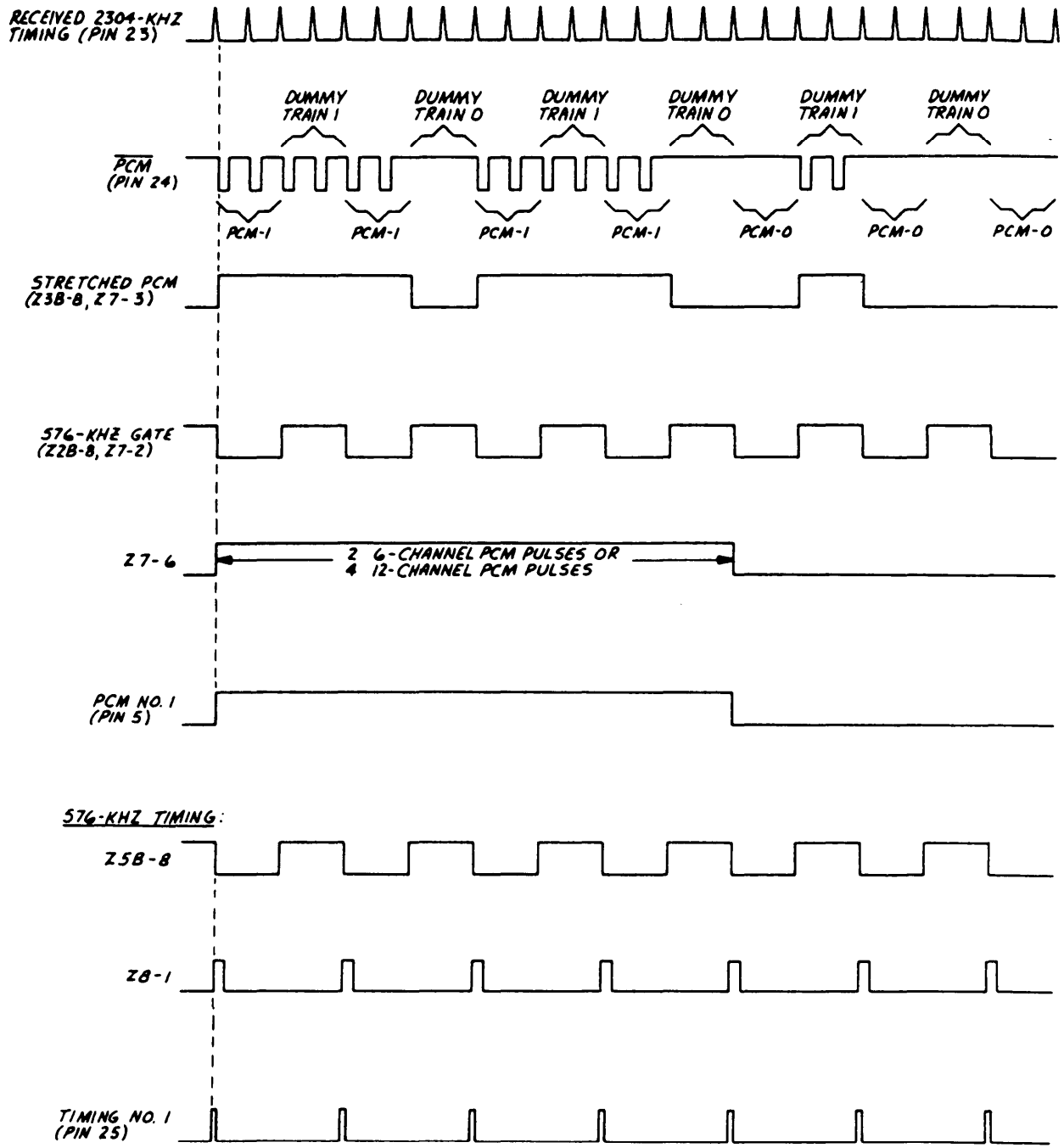
(2) *Peak detector.* Peak detector Q1, Q2 produces a dc sample voltage (received 2304-kHz timing) that is applied to the E input on SERV SEL switch S8 on the front panel when the received 2304-kHz timing pulses are present. When the dc sample voltage is developed, an indication in the green band is obtained on TEST ALIGN meter MI when SERV SEL switch S8 is placed in the E position and METER SEL switch S7 is placed in the SERV FAC position.

g. *PCM Traffic Alarm Generator Circuit.* The pcm traffic alarm generator circuit receives pcm pulses from the cable input amplifier circuit when pcm pulses are being processed through the cable input circuits. When no pcm pulses are being processed, Q13 is conducting and Q14 is cut off. When the negative-going pcm pulses are applied to Q13, the stage is driven into cutoff for the duration of each pulse. When Q13 cuts off, C13 quickly discharges through CR8, R37, and R36 to -6 volts. When the pulse passes, Q13 is biased back into conduction and C19 charges through R38 and CR9. The positive voltage developed across R38 charges C20 and biases Q14 into conduction. Although Q13 is continually being biased on and off, the time constant of C20 and R38 is long enough to hold Q14 in conduction as long as pcm pulses are being processed. The time constant is also long enough to hold Q14 in conduction if the incoming pcm pulses are momentarily interrupted. Once the incoming pulses are removed, Q13 remains in conduction and C19 becomes fully charged. When C19 is charged, Q14 is biased into cutoff when the current flow through R38 ceases and C20 discharges through R38 to ground. When Q14 conducts, a positive dc sample voltage (received pcm) is developed and applied to the F input on SERV SEL switch S8 on the front panel. When the dc voltage is developed, an indication is obtained on TEST ALIGN meter M1 when SERV SEL switch S8 is placed in the F position and METER SEL switch S7 is placed in the SERV FAC position. The traffic alarm signal from Q14 is a positive dc voltage (logic 1) when pcm pulses are present, or a negative dc (logic 0) when pcm pulses are missing. The traffic alarm signal applied to the alarm circuits on panel 12A3 causes a visual and audible alarm when the traffic alarm signal is a logic 0. When Q14 is conducting, the positive voltage at the junction of R36 and R37 is applied as an inhibit signal to switch Q12 in the 2304-kHz generator circuit. When pcm pulses are missing in the circuits and Q14 goes into cutoff, a negative voltage is developed at the junction of R36 and R37 and applied as an enable voltage to switch Q12.

1-20. Receive Circuits

a. *General.* The receive circuits (figure FO-7) process the negative-going received pcm pulses from the cable input circuits on panel 12A5 into full-width pcm pulses. The receive circuits generate 2304-kHz timing pulses when the TD-754/G is used in the 48-channel mode of operation. In 6-, 12-, and 24-channel modes of operation, the receive circuits generate 576-kHz timing pulses. In 6- and 12-channel modes of operation, the dummy train pcm pulses are automatically removed from the desired data pcm pulses. The decoded pcm pulses and timing pulses from the receive circuits are applied to one or two TD-660(*)/G's, or similar equipment, connected to the TD-754/G. Figure 1-13 shows a typical timing diagram for the receive circuits.

b. *Timing Gate Generator Circuit.* The timing gate generator circuit produces 1152-kHz, 576-kHz, and 288-kHz timing gates that are synchronized to, and generated from, the positive-going 2304-kHz timing pulses applied through pin 23 to Z2A. Multivibrator Z2A generates 1152-kHz timing gates that are applied to Z2B and to Z6A in the pcm timing gate selector circuit. Multivibrator Z2B generates 576-kHz timing gates that are applied to Z3A, to Z5A in the pcm timing gate selector circuit, to Z5C in the output timing generator circuit, and to Z4A and Z4B in the dummy train detector circuits. The 288-kHz and 288-kHz timing gates from Z3A are applied to Z4A and Z4B in the dummy train detector circuits. Negative-going reset (logic 0) pulses are applied to Z2A-4, Z2B-10, and Z3A-4 from Z10D in the dummy train detector circuits to shift the phase of the timing gates with respect to the incoming pcm pulses as described in h below. When a reset pulse is applied, a logic 1 is present at the outputs of Z2A, Z2B, and Z3A. The three stages remain in the set condition until the negative-going reset pulses are removed.



NOTE:
PCM PULSES SHOWN FOR TYPICAL
6- OR 12-CHANNEL OPERATION.

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Figure 1-13. Receive Circuits, Timing Diagram.

c. *PCM Pulse Stretcher Z3B.* Pcm pulse stretcher Z3B produces a full-width (stretched) pcm pulse and a full-width pcm pulse each time a half-width pcm pulse from panel 12A5 is applied. The full-width pcm and pcm pulses have a pulse width of 434 nanoseconds. The received pcm pulses are applied through pin 24 on panel 12A5 to Z3B-10 and the received 2304-kHz timing pulses are applied through pin 23 to Z3B-13. When one or more pcm pulses are applied to Z3B-10, a logic 1 (pcm) is generated from Z3B-8 and a logic 0 (pcm) is generated from Z3B-9. The logic outputs remain in this condition until the pcm pulses applied to Z3B-10 are removed and the trailing edge of the next 2304-kHz timing pulse occurs. For example, a series of four 2304-kHz timing pulses with pcm pulses being applied, followed by a series of four 2304-kHz timing pulses without pcm being applied, produces a logic 1 followed by a logic 0 from Z3B; the pulse width of the logic 1 and the logic 0 is 1,736 nanoseconds each (434 nanoseconds multiplied by 4). The stretched pcm pulses from pin 8 are applied to flip-flop Z7 in the timed pcm generator circuit and to Z4A in the dummy train detector circuits. The stretched pcm pulses from pin 9 are applied to flip-flop Z7 and to Z4B.

d. *PCM Timing Gate Selector Circuit.* The 576-kHz, 1152-kHz, or 2304-kHz timing gate applied through Z6B to Z7 in the timed pcm generator circuit is controlled by MODE switch S4 on the front panel.

(1) Placing MODE switch S4 in the 6/12 position applies +5 volts (logic 1) to pins 21 (mode select 2) and 22 (mode select 1) on panel 12A6. The logic 1 to Z1B produces a logic 0 output from Z1B that inhibits Z6A. The logic to Z1A produces a logic 0 output from Z1A that inhibits Z5B. Inhibiting Z6A and Z5B removes the 1152-kHz and 2304-kHz timing gates to Z6B. The logic 1 from pin 22 to Z5A enables the 576-kHz timing gate to Z6B.

(2) Placing MODE switch S4 in the 24 position applies +5 volts (logic 1) to pin 21 and ground (logic 0) to pin 22. This condition inhibits Z5A and Z5B, thus removing the 576-kHz and 2304-kHz timing gates to Z6B. The logic 1 from Z1B and pin 21 to Z6A enables the 1152-kHz timing gate to Z6B.

(3) Placing MODE switch S4 in the 48AR position applies ground (logic 0) to pins 21 and 22. This condition inhibits Z5A and Z6A, thus removing the 576-kHz and 1152-kHz timing gates to Z6B. The logic 1 from Z1A to Z5B enables the 2304-kHz timing gate to Z6B.

e. *Output Timing Generator Circuit.* In 6-, 12-, and 24-channel modes of operation, the circuit produces 576-kHz timing pulses. In the 48-channel mode of operation, the circuit produces 2304-kHz timing pulses.

(1) In 6-, 12-, and 24-channel modes of operation, MODE switch S4 is placed in the 6/12 or 24 position. In either position, +5 volts (logic 1) are applied through pin 21 to Z1A. The logic 0 from Z1A inhibits Z5B so that a constant logic 1 is applied from Z5B to Z5D. The logic 1 from pin 21 is also applied to Z5C. Therefore, Z5C produces a logic 1 output to Z5D during 576-kHz time. The leading edge of the logic 0 from Z5D to Z8 during 576-kHz time triggers Z8 to produce a negative-going pulse whose width is approximately 150 nanoseconds. Therefore, Z8 generates negative-going pulses at the 576-kHz rate.

(2) In the 48-channel mode of operation, MODE switch S4 is placed in the 48AR position. This applies a ground (logic 0) through pin 21 on panel 12A6 that inhibits Z5C so that a constant logic 1 is applied from Z5C to Z5D. The logic 0 from pin 21 is applied to Z1A so that a constant logic 1 is applied to Z5B. This enables Z5B to generate a logic 0 output to Z5D each time a 2304-kHz timing pulse is applied to Z5B. Gate Z5D, in turn, produces a logic 1 whose trailing edge triggers Z8 to produce a negative-going pulse whose width is approximately 125 nanoseconds. The negative-going pulses from Z8 are generated at the 2304-kHz rate.

f. Timing No. 1 Output Circuit.

(1) *Emitter follower Q3, switch Q4.* Emitter follower Q3 is cut off during the time each 576-kHz or 2304-kHz timing gate is applied from Z8 in the output timing generator circuit. Switch Q4 is biased into conduction during the time that Q3 is cut off. When Q4 conducts, the voltage at the junction of R13 and Q4 changes from a base voltage of approximately -2 volts to 0 volt. The positive-going 2-volt timing pulses, which have a pulse width of 100 ± 20 nanoseconds, are routed through pin 25 on panel 12A6 to TIM OUT-1 receptacle on the rear panel. The timing pulses are also applied to peak detector Q5.

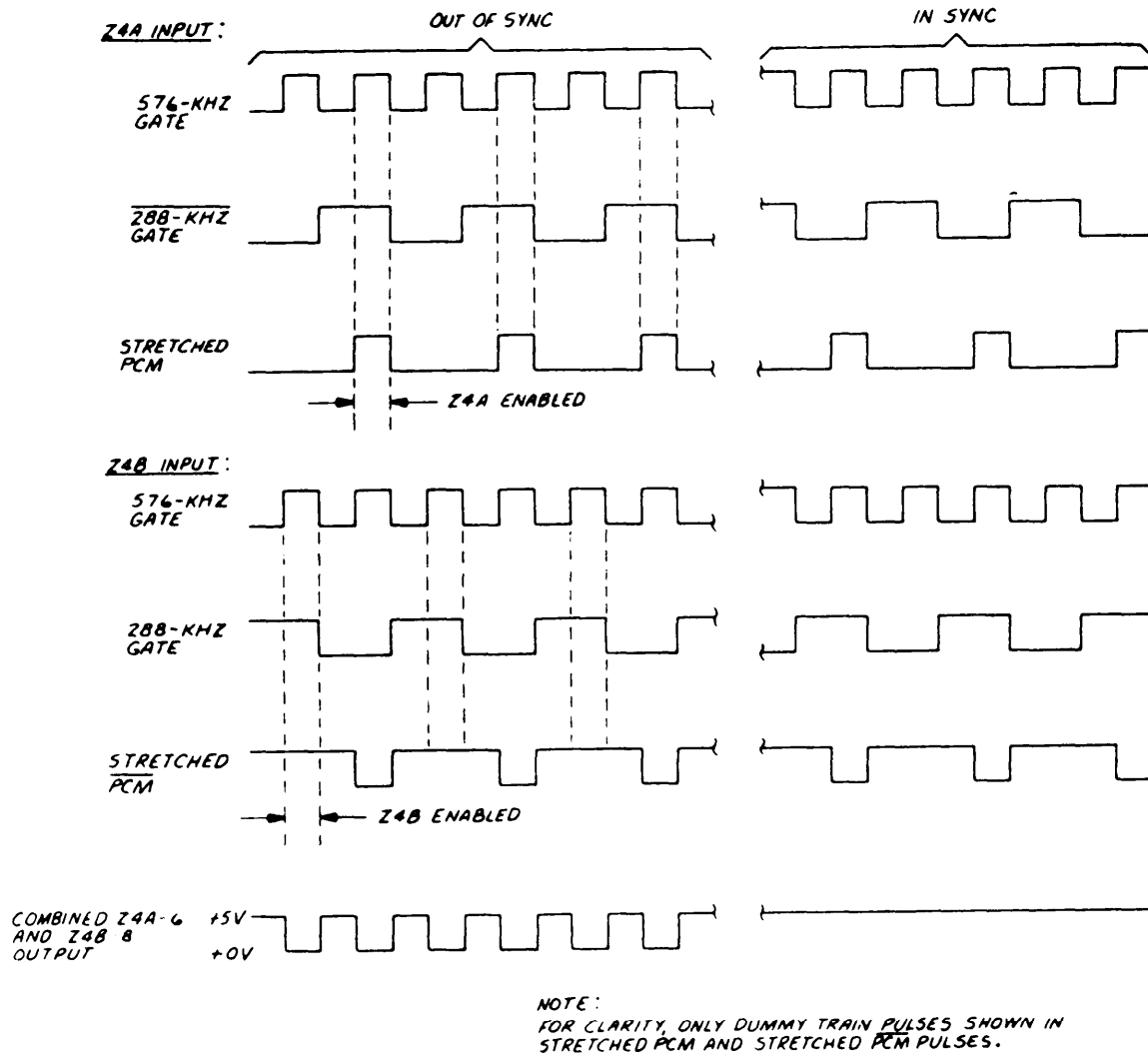
(2) *Peak detector Q5.* The output from Q5 is a positive dc voltage to pin 27 on panel 12A6 when timing pulses are being generated, or a 0-volt output from Q5 when timing pulses are not being generated. When the positive-going pulses are applied to Q5 from Q4, C11 and C13 change to a positive value that biases Q5 towards cutoff. As long as timing pulses are generated, C13 will retain a positive charge that is sufficient to bias Q5 towards cutoff. When Q5 is biased towards cutoff, the dc sample voltage developed at the junction of R15 and Q5 goes to some positive value between +2 and +5 volts. When Q5 conducts, the dc sample voltage (timing No. 1) decreases to approximately 0 volt. When timing pulses are generated, the positive dc sample voltage is applied through pin 29 on panel 12A6 to the H input on SERV SEL switch S8 on the front panel. When the dc voltage is present, an indication in the green band is obtained on TEST ALIGN meter M1 when SERV SEL switch S8 is placed in the H position and METER SEL switch S7 is placed in the SERV FAC position.

g. Output Timing No. 2 Circuit. The operation of this circuit is similar to the operation of the circuit described in f(1) above. The timing No. 2 pulses are applied through pin 27 on the panel 12A6 to READ-ZERO SET-NORM OPR switch S2 on the front panel, and through the NORM OPR position of S2 to TIM OUT-2 receptacle J7 on the rear panel. The operation of peak detector Q8 is similar to the operation of peak detector Q5 described in f(2) above. The dc sample voltage (timing No. 2) is applied through pin 28 on panel 12A6 to input J on SERV SEL switch S8 on the front panel. When the dc voltage is present, an indication in the green band is obtained on TEST ALIGN meter M1 when SERV SEL switch S8 is placed in the J position and METER SEL switch S7 is placed in the SERV FAC position.

h. Dummy Train Detector Circuits. In 6- and 12-channel modes of operation, the dummy train detector circuits sample the stretched pcm pulses for the presence and position of dummy train pulses with respect to the timing gates. When the dummy train pulses are not properly positioned, a reset signal is applied to the timing gate multivibrators in the timing gate generator circuit from the dummy train detector circuits. The reset signal remains until timing gates and dummy train pulses are properly positioned. Once the dummy train pulses are properly positioned, the receive circuits process the desired pcm pulses and remove the dummy train pulses from the pulse train. In 24- and 48-channel modes of operation, the dummy train detector circuits are disabled.

(1) *Detector Z4A, Z4B.* Operating MODE switch S4 in the 24 or 48AR position applies a logic 0 level to Z4A-9 and Z4B-5 to inhibit the detector. In the 6/12 position, MODE switch S4 applies a logic 1 level to Z4A and Z4B that enables the detector. When properly positioned, the dummy train pulses are generated from Z3B and applied to Z4A and Z4B during the 576-kHz gate time as shown in figure 1-14. In this sequence, Z4A and Z4B remain inhibited and generate a constant logic 1 level to Z10A. When the dummy train pulses are not properly positioned, the constant dummy train logic 1 applied to either Z4A or Z4B causes a logic 0 to be applied to Z10A. In the data pcm pulses that are applied to Z4A and Z4B, the logic 1's and 0's are randomly distributed throughout the pulse train. Therefore, the probability of a prolonged series of logic 1's being applied to Z4A or Z4B to cause a reset signal is slight. An indication of whether pcm or dummy train pulses are being sampled can be monitored at TP5. If the output is static, the dummy train pulses are being sampled; if the output is constantly changing at a random rate, pcm pulses are being sampled. A logic 0 input to Z10A produces a logic 1 from Z10A to Z10D. If

the second input to Z10D is also a logic 1, then Z10D produces the logic 0 (reset signal) level to the timing gate multivibrators in the timing gate generator circuit.



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Figure 1-14. Dummy Train Detector, Timing Diagram.

(2) *Holding circuit.* The holding circuit prevents a reset pulse (logic 0) output from Z10D to be generated by a temporary loss of synchronization or a temporary false pcm pulse input. When the dummy train detector circuits are initially energized, Q2A is cut off and Q2B is conducting. The output from Z9 is a logic 0 at this time. The logic 0 applied to Z10C from Z9 causes Z10C to produce a logic 1 input to Z10A and Z10D. When a logic 1 is generated from detector Z4A, Z4B, capacitor C8 charges through CR3 and R9 towards +5 volts. The logic 0 output from Z10A to Z10B causes the Z10B output to be a logic 1; therefore, R10 and CR4 provide a parallel charge path for C8. When the charge across C8 is approximately 3.8 volts, Q2A is biased into conduction and a voltage is developed across R19 that causes the output of Z9 to switch from a logic 0 to a logic 1. The logic 1 causes Z10C to develop a logic 0 output that inhibits Z10A and Z10D from generating logic 0 outputs. When the output from detector Z4A, Z4B changes from a logic 1 to a logic 0, the holding circuit continues to produce a logic 0 from Z9 for 200 ±100 milliseconds. This prevents Z10D from generating a logic 0 (reset) output for approximately 200 milliseconds after the logic 0 output is generated from detector Z4A, Z4B. The 200-millisecond delay is provided by the time it requires C8 to discharge to a voltage that biases Q2A into cutoff.

The discharge path for C8 is through CR2 and R8. When Q2 is cut off, Z9 generates a logic 0 that causes Z10C to generate a logic 1 to Z10A and Z10D. The logic 0 output of detector Z4A, Z4B causes Z10A to generate a logic 1 to Z10D. Therefore, the two logic 1's applied to Z10D cause Z10D to generate a logic 0 (reset) output to Z2A, Z2B, and Z3A in the timing gate generator circuit. Z10D continues to generate the logic 0 output until the dummy train pulses are properly positioned with the 576-kHz, 288-kHz, and 288-kHz timing gates.

i. PCM Timing Gate Selector Circuit. The pcm timing gate selector circuit selects either 576-kHz, 1152-kHz, or 2304-kHz timing gates to generate the pcm output pulses at the proper pulse rate. The proper pcm pulse rate is selected and controlled by MODE switch S4 on the front panel.

(1) *6- and 12-channel modes of operation.* When MODE switch S4 is placed in the 6/12 position, a logic 1 is effectively applied to pins 21 and 22 on panel 12A6. The logic 1 input to Z1A and Z1B produces a logic 0 output from Z1A and Z1B that inhibits Z5B and Z6A. The logic 1 input from pin 22 is applied to Z5A so that Z5A produces a 576-kHz gate output when the 576-kHz timing gate from Z2B is applied. The 576-kHz gating pulses from Z5A are applied through Z6B to Z7 in the timed pcm output circuit.

(2) *24-channel mode of operation.* When MODE switch S4 is placed in the 24 position, a logic 1 is applied to pin 21 and a logic 0 is applied to pin 22. The logic 1 input to Z1A produces a logic 0 output from Z1A that inhibits Z5B. The logic 0 input from pin 22 inhibits Z5A. The logic 0 applied to Z1B produces a logic 1 output from Z1B to Z6A. The logic 1 from pin 21 is also applied to Z6A so that Z6A produces a 1152-kHz gate output when the 1152-kHz timing gate from Z2A is applied. The 1152-kHz gating pulses from Z6A are applied through Z6B to Z7 in the timed pcm output circuit.

(3) *48-channel mode of operation.* When MODE switch S4 is placed in the 48AR position, a logic 0 is applied to pins 21 and 22. The logic 0 at pins 21 and 22 inhibits Z5A and Z6A. The logic 0 applied to Z1A produces a logic 1 output from Z1A to Z5B. Therefore, Z5B produces a 2304-kHz gate output when the 2304-kHz timing signal from pin 23 is applied. The 2304-kHz gating pulses from Z5B are applied through Z6B to Z7 in the timed pcm output circuit.

j. Timed PCM Generator Circuit.

(1) *Generator Z7.* The stretched pcm pulses from the pcm pulse stretcher circuit are applied to Z7-3 and the stretched pcm pulses are applied to Z7-11. Generator Z7 is a j-k flip-flop that produces outputs on pins 6 and 9, which correspond to the inputs on pins 3 and 11, when the negative-going trailing edge of the timing gate from Z6B is applied to A7-2. For example, a high-level signal applied to pin 3 and a low-level signal applied to pin 11 produce a high-level output at pin 6 and a low-level output at pin 9. In 6- and 12-channel modes of operation, the 576-kHz timing gates are applied to Z7-2. In 6- and 12-channel modes of operation, the dummy train pulses are applied to Z7-3 and Z7-11 during 576-kHz gate time and the desired pcm pulses are applied during 576-kHz gate time. Therefore, the dummy train pulses are effectively inhibited and the desired pcm pulses control the outputs from Z7-6 and Z7-9. In the 24-channel model of operation, 1152-kHz timing gates are applied to Z7-2. In the 48-channel model of operation, 2304-kHz timing gates are applied to Z7-2. The pcm pulses from Z7-6 are applied through Z10C to emitter followers Q9 and Q13 in the output pcm No. 1 and No. 2 circuits. The pcm pulses from Z7-9 are applied to peak detector Q1.

(2) *Peak detector Q1.* Peak detector Q1 produces a dc sample voltage (pcm activity) that is applied to the G input on SERV SEL switch S8 on the front panel when pcm pulses are generated from Z7. When the proper dc sample voltage is developed, an indication in the green band is obtained on TEST ALIGN meter M1 when SERV SEL switch S8 is placed in the G position and METER SEL switch S7 is placed in the SERV FAC position.

k. Output PCM No. 1 Circuit.

(1) *Emitter follower Q9, switch Q10.* Emitter follower Q9 is cut off and switch Q10 conducts during the time negative-going pcm pulses are applied from Z1C. When Q10 goes into conduction, the voltage at the junction of Q10 and R28 changes from a base voltage of approximately -2 volts to 0 volt, thereby generating a positive-going 2-volt pcm pulse that is applied to pin 5 on panel 12A6. The positive-going pcm No. 1 pulses at pin 5 are routed to PCM OUT-1 receptacle J4 on the rear panel. In 6- and 12-channel modes of operation, the pulse width of each pcm pulse is 3.57 microseconds; in a 24-channel mode of operation, the pulse width is 1.736 microseconds; and in 48-channel mode of operation, the pulse width is 0.434 microsecond. The pcm pulses from Q10 are also applied to peak detector Q11, Q12.

(2) *Peak detector Q11, Q12.* Peak detector Q11, Q12 produces a dc sample voltage (pcm No. 1) that is applied to the K input on SERV SEL switch S8 when pcm pulses are generated from switch Q10. When the dc voltage is developed, an indication in the green band is obtained on TEST ALIGN meter M1 when SERV SEL switch is placed in the K position and METER SEL switch S7 is placed in the SERV FAC position.

l. Output PCM No. 2 Circuit. The operation of this circuit is identical to the operation of the circuit described in k above. The pcm pulses from switch Q14 are applied through pin 2 on panel 12A6 to PCM OUT-2 receptacle J6 on the rear panel. The dc sample voltage (pcm No. 2) from peak detector Q15, Q16 is applied through pin 1 on panel 12A6 to the L input on SERV SEL switch S8 on the front panel. When the dc voltage is present, an indication in the green band is obtained on TEST ALIGN meter M1 when SERV SEL switch S8 is placed in the L position and METER SEL switch S7 is placed in the SERV FAC position.

1-21. Order Wire Facilities

a. General.

(1) The order wire facilities provide single-channel, direct audio communications between terminal and attended-repeater stations in a cable- or radio-pcm system. Provision is made to patch the order wire capability in radio-to-cable, cable-to-radio, and cable-to-cable system configurations. The order wire transmitting and receiving circuits are mounted on panel 12A2 (figure FO-3), except for the final cable transmit amplifier circuit, which is mounted on panel 12A3 (figure FO-4).

(2) Panel 12A3 also contains the circuits that generate the audible and visual call signals when an incoming ring signal is detected in the cable-in or patch-in order wire signals. These circuits are also used to generate the audible and visual alarm signals when the cable current generated in the TD-754/G is removed, or to generate the audible and visual alarm signals when incoming pcm traffic is missing.

(3) The TD-754/G processes the three types of input order wire signals listed below.

(a) *Cable-in order wire.* The order wire signals that are applied to the TD-754/G from the TD-754/G terminal at the opposite end of the cable link.

(b) *Mike-in order wire.* The order wire signals that are applied to the TD-754/G from an attached H-91A/U.

(c) *Patch-in order wire.* The order wire signals that are applied to the TD-755/G from an adjacent TD-754/G when two TD-754/G's are connected as attended repeaters.

b. Signaling Oscillator Circuit. The signaling oscillator circuit generates the initial 1600 ± 32 -Hz ring signal when another TD-754/G is called. The circuit also generates a 1100 ± 100 -Hz test tone signal that is used for test and alignment purposes. The circuit is controlled by TALK-OFF-SIG switch S5 on the front panel. Operating switch S5 to the SIG position electrically connects J1-6 to J1-9 and J1-7 to J1-8. Connecting J1-6 to J1-9 energizes the oscillator by applying -6 volts to the emitter circuit of Q2. Connecting J1-7 to J1-8 applies the 1600-Hz ring signal to the input of amplifiers Z1 and Z3. Placing TONE switch S1 on panel 12A2 in the ON position energizes the oscillator and connects C3 parallel with C4 to change the oscillator frequency to 1100 Hz. TTL potentiometer R37 is adjusted for the desired test tone level of 150 millivolts ac at TP4.

c. Cable Order Wire Input Circuit. The cable-in order wire signals from the cable link are applied through panel 12A5 to pin 2 on panel 12A2. The dc cable current is routed through the primary winding of T4 and R44 to ground. The low frequency order wire signals are coupled through T4 and applied through CRL potentiometer R45 to amplifiers Z1 and Z2. CRL potentiometer R45 is an in-system adjustment that controls the signal level of the incoming order wire signals from the cable link. The dc voltage developed across R44 and C24 is applied through pin 3 on panel 12A2 as the dc sample voltage (received cable current) to the RCC input on SERV SEL switch S8. When the dc voltage is present, an indication in the green band on TEST ALIGN meter M1 is obtained when SERV SEL switch S8 is placed in the RCC position and METER SEL switch S7 is placed to the SERV FAC position. Breakdown diode VR1 prevents the voltage drop across R44 from exceeding 6.2 volts dc.

d. Headset Output Circuit.

(1) *Amplifier Z2.* Amplifier Z2 is a linear operational amplifier that has a voltage gain of 10. The cable-in order wire signals from the cable order wire input circuit or the patch-in order wire signals from the patch-thru order wire input circuit are amplified in Z2 and applied through pin 14 on panel 12A2 to the signaling detector circuit on panel 12A3. The amplified signals from Z2 are also applied through pin 13 on panel 12A2 to an H-91A/U attached to the HEADSET receptacle on the front panel.

(2) *Detector Q3.* Detector Q3 produces a dc sample voltage (earphone rec level) that is applied to the 0 input on SERV SEL switch S8 when order wire signals are amplified through Z2. When the dc voltage is developed, an indication in the green band is obtained on TEST ALIGN meter M1 when SERV SEL switch S8 is placed to the 0 position and METER SEL switch S7 is placed in the SERV FAC position.

e. Patch-Thru Transmit Output Circuit.

(1) *Amplifier Z1.* Amplifier Z1 is a linear operation amplifier that has a voltage gain of 10. The cable-in order wire signals from the cable order wire input circuit or the mike-in order wire signals from the microphone order wire input circuit are amplified in Z1 and applied through pins 20 and 21 on panel 12A2 to PATCH-THRU receptacle J11 on the rear panel. The signals applied to PATCH-THRU receptacle J11 are used when the TD-754/G is connected to another TD-754/G in the attended-repeater configuration. When two TD-754/G's are used in the attended-repeater configuration, a special patch-thru cable is connected between the two PATCH-THRU receptacles. The patch thru circuits permit order wire signals from the west terminal to be received in TD-754/G No. 1, patched through to TD-754/G No. 2, and retransmitted to the east terminal. Order wire signals from the east terminal, in turn, are received by TD-754/G No. 2, patched through to TD-754/G No. 1, and retransmitted to the west terminal. Order wire signals can be monitored or inserted at either TD-754/G in the attended repeater configuration.

(2) *Detector Q1.* Detector Q1 produces a dc sample voltage (order wire xmit) that is applied to the N input on SERV SEL switch S8 when order wire signals are amplified through Z1. When the dc voltage is developed, an indication in the green band is obtained on TEST ALIGN meter M1 when SERV SEL switch S8 is placed in the N position and METER SEL switch S7 is placed in the SERV FAC position.

f. Microphone Order Wire Input Circuit. Operating TALK-OFF-SIG switch S5 to the TALK position allows mike-in order wire signals from the attached H-91A/U to be applied to pin 7 on panel 12A2. The incoming signals are applied through C22 to amplifiers Z1 and Z3. The -6 volts to R32 are applied as mike bias through pin 5 on panel 12A2 to the attached H-91A/U.

g. Cable Transmit Output Circuit. The cable transmit output circuit contains linear operational amplifier Z3 that has a voltage gain of 10. The mike-in order wire signals from the microphone order wire input circuit and the patch-in order wire signals from the patch-thru order wire input circuit are applied to Z3. The order wire signals amplified in Z3 are applied through pin 12 on panel 12A2 as cable order wire signals to the cable input circuit on panel 12A3.

h. patch-Thru Order Wire Input Circuit. The patch-out order wire signals from the patch-thru transmit output circuit on the adjacent TD-754/G in the attended-repeater configuration are applied as patch-in order wire signals to the patch-thru order wire input circuit. Resistors R1 through R6 form an attenuation pad to prevent the incoming signals from overloading amplifiers Z2 and Z3. The signals are coupled through T1 and applied through PRL potentiometer R7 to amplifiers Z2 and Z3. PRL potentiometer R7 is an in-system adjustment that controls the signal level of the incoming order wire signals from the adjacent TD-754/G.

i. Cable Transmit Amplifier Circuit (figure FO-4). The cable order wire signals from panel 12A2 are applied through pin 28 on panel 12A3 to amplifier Q8. The cable transmit amplifier circuit has a voltage gain of 10. The signal voltages developed across the primary winding of T2 in the collector circuit of Q8 are coupled through the secondary windings of T2 and applied to the bases of push-pull amplifiers Q9 and Q10. The amplified signal voltages developed across the primary winding of T3 in the collector circuits of Q9 and Q10 are coupled through the secondary winding of T3 and applied to filter FL1. The filtered order wire signals from FL1 are applied through pin 22 on panel 12A3 to the transmit circuits on panel 12A4. When order wire signals are present at the output of FL1, a dc sample voltage (cable order wire) is developed at the junction of CR5 and R30. The dc sample voltage is applied through pin 24 on panel 12A3 to the M input on SERV SEL switch S8. When the dc voltage is present, an indication in the green band is obtained on TEST ALIGN meter M1 when SERV SEL switch S8 is placed in the M position and METER SEL switch S7 is placed in the SERV FAC position.

j. Signaling Detector Circuit. The signaling detector circuit generates a ring enable signal when the 1600-Hz ring signal is detected in the headset order wire signals. The headset order wire signals from panel 12A2 are applied through pin 2 on panel 12A3 to amplifier Q1. The amplified signal voltage developed across the primary winding of T1 in the collector circuit of Q1 is coupled through the secondary winding of T1 and applied to emitter follower Q2. The output signals from the secondary winding of T1 are applied across tank circuit C3, L1 connected in series with R5. Capacitor C3 and L1 form a parallel resonant circuit that is resonant at 1600 Hz. The Q of the tank circuit is high enough so that the resonant impedance decreases rapidly at frequencies other than 1600 Hz. This causes most of the signal voltage to be developed across C3, L1 at 1600 Hz; at frequencies other than 1600 Hz, most of the signal voltage is developed across R5. Diode CR1 permits C4 to charge positive with respect to ground and diode CR2 permits C5 to charge negative with respect to ground. At 1600 Hz, the voltage developed across C3, L1 is greater than the voltage across R5. This results in a greater positive charge across C4 than the negative charge across C5. The summing effect is a positive potential that drives Q2 into conduction. At frequencies other than 1600 Hz, the voltage developed across R5 is greater than the voltage developed across C3, L1. In this condition, the summing effect is a negative potential that holds Q2 in cutoff. The

time constant of the charge and discharge paths for C4 and C5 is long enough so that spurious 1600-Hz components in the order-wire signals cannot charge C4 sufficiently to bias Q2 into conduction. When Q2 conducts, the voltage at the junction of Q2 and R9 changes from approximately -4 volts to +5 volts. The positive voltage is applied as the ring enable signal to call light driver Q3 and as a logic 1 to Z2A in the audible alarm control circuit.

k. Call Light Driver Q3. Call light driver Q3 conducts when the positive enable voltage is applied from Q2 in the signaling detector circuit. When Q3 conducts, the call light enable signal (ground) is applied to CALL indicator DS1. The ground signal causes CALL indicator DS1 to light during the time that a 1600-Hz call signal is being applied to the TD-754/G.

l. Traffic Light Driver Q4. Traffic light driver Q4 conducts when the traffic alarm signal from panel 12A5 changes from approximately +5 volts (logic 1) to a slightly negative (logic 0) voltage. The logic 0 level applied to Z2C changes its output from 0 volt to +5 volts, thus driving Q4 into conduction. The traffic light enable signal (ground) is applied to TRAFFIC indicator DS2 when Q4 conducts, causing the indicator to light.

m. Cable Current Light Driver Q5. Cable current light driver Q5 conducts when no-cable current signal from power supply assembly 12A1 changes from approximately +5 volts (logic 1) to 0 volt (logic 0). The logic 0 level applied to Z2B changes its output from 0 volt to +5 volt, thus driving Q5 into conduction. The cable current light enable signal (ground) is applied to CABLE CUR indicator DS3 when Q5 conducts, causing the indicator to light.

n. Audible Alarm Control Circuit. The audible alarm control circuit activates horn Z1 on power supply assembly 12A1 when a no-traffic condition is detected on panel 12A5 or a no-cable current condition is detected on power supply assembly 12A1. Horn Z1 is also activated by the audible alarm control circuit when the signaling detector circuit detects the 1600-Hz call signal in the incoming order wire signals.

(1) Under normal operating conditions, the traffic alarm and no-cable current alarm signals applied through pins 14 and 20 on panel 12A3 to Z1A are logic 1's (+5 volts). Loss of traffic and/or cable current places a logic 0 (ground) to one or both inputs of Z1A. The output from Z1A to Z1B and Z1C switches from a logic 0 to a logic 1. This causes a logic 1 output from Z1B to Z1D and a logic 0 output from Z1A to Z1C.

(2) When the equipment is operating normally and the audible alarm is silent, BUZZER OFF switch S6 on the front panel is operated so that a logic 1 is applied through pin 27 to Z1C and a logic 0 is applied through pin 29 to Z1D. This condition results in a logic 1 output from Z1C and Z1D. If BUZZER OFF switch S6 is pressed, the logic inputs through pins 27 and 29 switch levels and Z1D has logic 1's applied to both inputs. The logic output from Z1D to Z2D switches from a logic 1 to a logic 0. The logic 0 output from Z2D switches from a logic 0 to a logic 1 to 6.25-Hz pulse generator Q6, Q7. The logic 1 enables 6.25-Hz pulse generator Q6, Q7 and the audible alarm output is applied through pin 10 on panel 12A3 to horn Z1 on power supply assembly 12A1. The audible alarm output is a logic 0 (enable) signal for 50 milliseconds and a logic 1 (inhibit) for 110 milliseconds. Pressing BUZZER OFF switch S6 again switches the logic levels to pins 27 and 29 and Z1D generates a logic 1 output to Z2D. The logic 1 applied to Z2D results in a logic 0 output from Z2D that inhibits 6.25-Hz pulse generator Q6, Q7.

(3) When the equipment is operating normally and the audible alarm is silent, the loss of traffic and/or cable current places a logic 0 to one or both of the inputs to Z1A. This condition causes the output from Z1A to Z1B and Z1C to switch from a logic 0 to a logic 1. The logic 1 to Z1B switches the output from Z1B to Z1D from a logic 1 to a logic 0. The logic 1 applied to Z1C switches the output from Z1C to Z2D from a logic 1 to a logic 0. This enables 6.25-Hz pulse generator Q6, Q7 as described in (2) above. The 6.25-Hz pulse generator remains enabled until the faulty condition is corrected and the traffic alarm and/or cable current alarm inputs through pins 14 and 20 change from a logic 0 to a logic 1, or BUZZER OFF switch S6 is pressed. Pressing BUZZER OFF switch S6

applies a logic 1 to Z1D and a logic 0 to Z1C, causing a logic 1 output from Z1D or Z1C. This causes an inhibit (logic 0) signal from Z2D to be applied to 6.25-Hz pulse generator Q6, Q7.

(4) When a defective condition is corrected (traffic alarm and no-cable current inputs to pins 27 and 29 return to a logic 1 level) after the BUZZER OFF switch has been pressed to silence the audible alarm, the audible alarm is again enabled. The inputs to Z1D become logic 1's, since the buzzer-off input to Z1D-13 is a logic 1 and the output from Z1B to Z1D-12 switches from a logic 0 to a logic 1. The output from Z1D to Z2D becomes a logic 0 and 6.25-Hz pulse generator Q6, Q7 is enabled.

(5) A 1600-Hz call signal detected in the signaling detector circuit results in a ring enable (logic 1) signal to Z2A. The logic 0 output from Z2A to Z2D enables 6.25-Hz pulse generator Q6, Q7. The 6.25-Hz pulse generator is enabled only during the time that the 1600-Hz call signal is being detected in the signaling detector circuit. The BUZZER OFF switch cannot silence the audible alarm when the alarm is enabled by the ring enable signal.

1-22. Power Supply Circuits

a. General. The power supply circuits mounted on power supply assembly 12A1 (figure FO-2) consist of +28-volt, +12-volt, +5 volt, and -6-volt power supply circuits and a reference power supply circuit. The assembly also contains a cable constant current power supply circuit, a meter zero set circuit for the cable fault locator circuit, and horn Z1 for the audible alarm function. The majority of the components for the dc power supply circuits and reference power supply are mounted on panel 12A1-A2. The majority of components for the cable constant current power supply circuit and the meter zero set circuit are mounted on panel 12A1-A1. Several components that are electrically part of the power supplies are mounted on heat sink assembly 12A1-A3, which is external to power supply assembly 12A1. Panel 12A1-A3 is mounted on the rear panel of the TD-754/G chassis.

b. Ac Input Circuit. Placing PWR switch S1 to the ON position applies a 115-volt, single-phase, 50-to-400-Hz input through fuses F1 and F2 to the primary winding of stepdown transformer T1 and to power on indicator DS1. Transformer T1 has five secondary windings that produce the voltages discussed in c below.

c. Dc Voltage Power Supplies.

(1) *+28-volt power supply circuit.* The secondary winding between T1-3 and T1-4 develops approximately 33.5 volts rms. The ac voltage is rectified by full-wave diode bridge rectifier CR1, CR2, CR3, and CR4. The dc output from the rectifier is filtered through choke input filter network L2, C4, C5, and C6. The unregulated +28 volts are applied through 2A+28V fuse F6 to voltage regulator Q10, Q11. The voltage is also applied to the +12-volt power supply circuit and the cable constant current supply circuit. The unregulated voltage applied through fuse F6 can increase to as much as +44 volts when the current requirements of the cable constant current supply circuit are minimum. Breakdown diode VR3 holds the base of Q10 at approximately +27 volts so that the output voltage from Q11 is regulated at +25 volts ± 10 percent. The +25-volt output at pin 5 can be monitored by placing METER SEL switch S7 in the SERV FAC position and SERV SEL switch S8 in the +28 position, and then observing TEST ALIGN meter M1 for an indication in the green band.

(2) *+12-volt power supply circuit.* The secondary winding between T1-5 and T1-6 develops approximately 23.3 volts rms. The ac voltage is rectified by full-wave diode bridge rectifier CR1, CR2, CR3, and CR4. The dc output of the rectifier is filtered through choke input filter L1A and C1. The unregulated +12 volts are applied through 1/4A+12V fuse F3 to an electronic voltage regulator consisting of Q1 on heat sink 12A1-A3 and Q1, Q2, and Q3. Transistor Q1 on the heat sink is a series regulator. Transistors Q1, Q2, and Q3 sample the +12-volt output and generate a control bias to Q1 on the heat sink to regulate the output voltage at +12 volts ± 2 percent. Potentiometer R1 (+12V) on the front panel is adjusted for a +12-volt output. Potentiometer R1 is adjusted by

placing METER SEL switch S7 in the SERV FAC position and SERV SEL switch S8 in the +12 position, and then adjusting R1 for a hairline indication on TEST ALIGN meter M1.

(3) *+5-volt power supply circuit.* The secondary winding between T1-7 and T1-8 develops approximately 11.5 volts rms. The ac voltage is rectified by full-wave diode bridge rectifier CR5, CR6, CR7, and CR8. The dc output of the rectifier is filtered through choke input filter L1B and C2. The unregulated +5 volts are applied through 1/2A+5V fuse F4 to an electronic voltage regulator consisting of Q2 on heat sink 12A1-A3, and Q4, Q5, and Q6. Transistor Q2 on the heat sink is a series regulator. Transistors Q4, Q5, and Q6 sample the +5-volt output and generate a control bias to Q2 on the heat sink to regulate the output voltage at +5 volts ± 2 percent. Potentiometer R2 (+5V) on the front panel is adjusted for a +5-volt output. Potentiometer R2 is adjusted by placing METER SEL switch S7 in SERV FAC position and SERV SEL switch S8 in the +5 position, and then adjusting R2 for a hairline indication on TEST ALIGN meter M1.

(4) *-6-volt power supply circuit.* The secondary winding between T1-9 and T1-10 develops approximately 15.5 volts rms. The ac voltage is rectified by full-wave bridge diode rectifier CR9, CR10, CR11, and CR12. The dc output from the rectifier is filtered through choke input filter L1C and C3. The unregulated -6 volts are applied through 1A-6V fuse F5 to an electronic voltage regulator consisting of Q3 on heat sink 12A1-A3, and Q7, Q8, and Q9. Transistor Q3 on the heat sink is a series regulator. Transistors Q7, Q8, and Q9 sample the -6-volt output and generate a control bias to Q3 to regulate the output voltage at -6 volts ± 2 percent. Potentiometer R3 (-6V) on the front panel is adjusted for a -6-volt output. Potentiometer R3 is adjusted by placing METER SEL switch S7 in the SERV FAC position and SERV SEL switch S8 in the -6 position, and then adjusting R3 for a hairline indication on TEST ALIGN meter M1.

(5) *Reference power supply circuit.* The secondary winding between T1-11 and T1-13 develops approximately 16.5 volts rms. The ac voltage is rectified by full-wave rectifier CR13 and CR14. The dc output from the rectifier is filtered through capacitor input filter C4, R20, and C5. The dc reference voltage from the circuit is applied to the service facilities function on panel 12A7. The reference voltage is a nominal value of 7.2v dc and is floating, rather than referenced to ground.

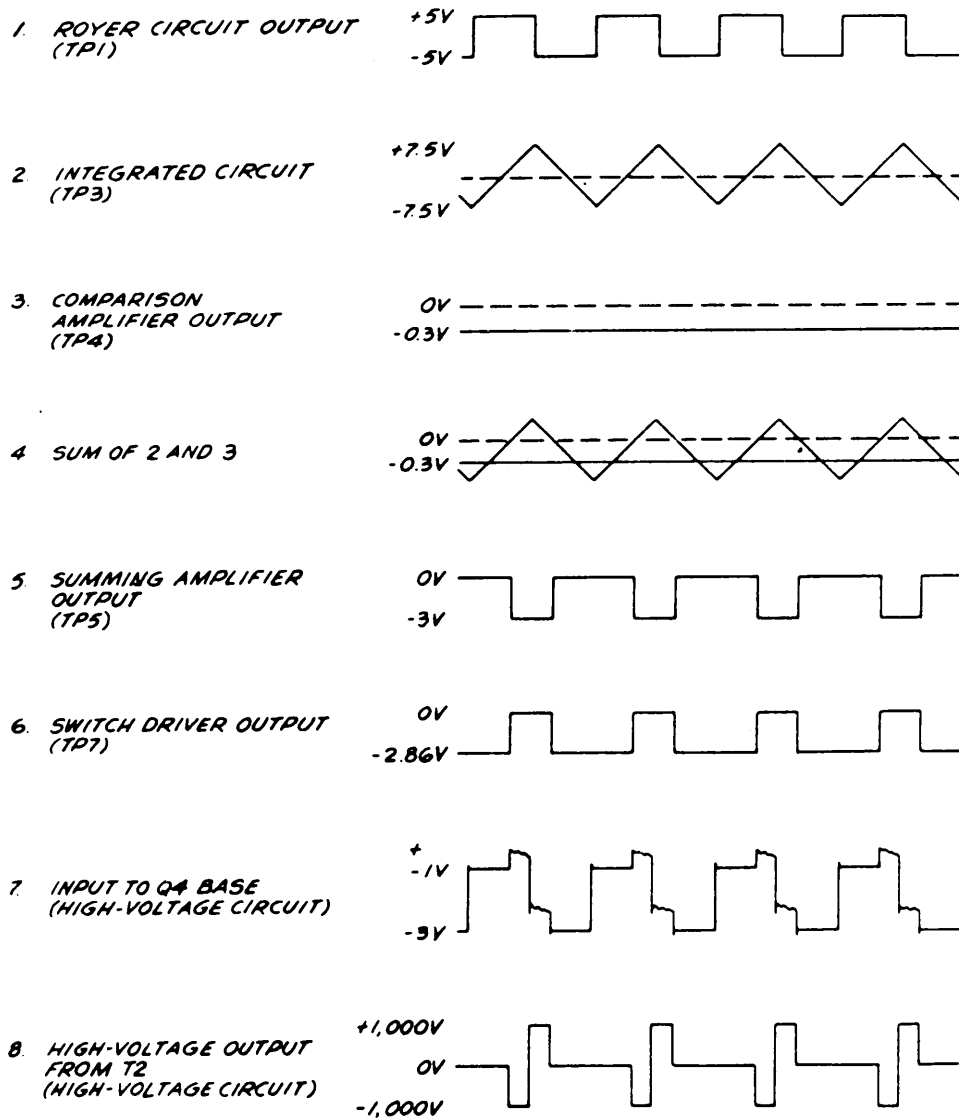
d. Horn Z1. Horn Z1 is energized by a ground signal from the order wire facilities on panel 12A3. When applied, the ground signal is on for 50 milliseconds and off for 110 milliseconds so that the horn generates a fluctuating audible tone.

e. Cable Constant Current Supply Circuits.

(1) *General* The cable constant current supply circuits generate a constant cable current of 38 milliamperes ± 3 percent to TD-206/G's in the cable link. The power supply produces a constant current for any combination of TD-206/G's up to a maximum of 39. To maintain a constant current, the voltage generated into the cable link varies from approximately 600 volts under maximum resistance conditions to approximately 0 volt when the cable link is effectively a short circuit. The circuits that makeup the cable constant current supply circuits are described in (2) through (10) below.

(2) *Royer circuit.* The Royer circuit generates two 3-kHz pulse outputs when the TD-754/G is initially turned on. The Royer circuit is energized when -6 volts are applied to the emitter circuits of Q2 and Q3. The 3-kHz pulse output across secondary winding T3-10 and T3-11 is applied to the integrator circuit and the 3-kHz pulse output across secondary winding T3-7 and T3-9 is applied to push-pull amplifiers Q4 and Q5 in the high voltage circuit. The typical waveform developed at the collector of Q2 and applied to the base of Q4 in the high voltage circuit is shown in (1), figure 1-15. The waveform developed at the collector of Q3 and applied to Q5 in the high voltage circuit is similar to the voltage input to Q4, but 180 degrees out of phase.

(3) *Integrator circuit.* The pulsed output from the secondary winding T3-10 and T3-11 of transformer T3 in the Royer circuit is applied to the integrator circuit consisting of R11, C6, and R12. The output of the circuit is a 3-kHz sawtooth voltage as shown in (2), figure 1-15. The sawtooth voltage is combined with the dc voltage from Z3 and applied to the inverting input of summing amplifier Z4 as described in (7) below.



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Figure 1-15. Cable Constant Current Supply Circuit, Waveform Diagram.

(4) *Start circuit.* The start circuit is energized when CABLE CUR switch S2 on the front panel is placed to the ON position. The +5 volts through S2 charge C7 in the base circuit of amplifier Q4. The charging action of C7 develops a positive voltage across R14 that drives Q4 into conduction while C7 is charging. While Q4 conducts, a logic 0 is applied to Z1A and Z1B in the current detection circuit. The output from Z1A is a logic 1 that drives switch Q5 into cutoff. When switch Q5 is cut off, a positive clamp voltage is removed from the junction of R34 and R35 in the base circuit of switch driver Q6 to enable the current regulating function. The charge time of C7 holds the logic 1 input to switch Q5 for approximately 1 second. After 1 second, Q5 is then continued to be held in cutoff

by Z1A, which has a logic 0 applied from Z1C in the current detection circuit. Switch Q5 remains cut off until a fault occurs or the power supply is deenergized.

(5) *Current detection circuit.* The current detection circuit turns off the cable current when the current exceeds 45 ± 3 milliamperes or the current decreases to less than 16 ± 1.4 milliamperes. Differential comparator Z2A, Z2B applies a logic 0 to Z1B when the cable current is within tolerance. The return path for the cable current from ground is through R23 and R22 to the junction of CR1 and CR3 in the high voltage circuit. When the cable current is 38 milliamperes, the voltage at the junction of R22 and R23 is approximately -3.2 volts and the voltage at the junction of CR1 and CR3 is approximately -6 volts. The voltage at the junction of R22 and R23 drives either Z2A or Z2B into conduction when the cable current increases or decreases to a level that is out of tolerance. When Z2A or Z2B conducts, the logic input to Z1B changes to a logic 1. During normal operation, the second input to Z1B from amplifier Q4 is a logic 1 and the three inputs to Z1C are logic 1's. Therefore, when Z2A or Z2B conducts, the logic 1 applied to Z1B switches the output from Z1B to Z1C to a logic 0. The logic 0 applied to Z1C switches the output from Z1C to Z1A in the start circuit to a logic 1. The output from Z1A switches to a logic 0 that drives switch Q5 into conduction. The logic 0 output from Z1A is also applied back to an input on Z1C so that Z1C continues to apply a logic 1 input to Z1A. Therefore, a continuous logic 0 is generated from Z1A that holds Q5 in conduction until CABLE CUR switch S2 is placed to the OFF position and then back to the ON position and the start circuit is reenergized. While Q5 is held in conduction, a positive voltage is applied to the junction of R34 and R35 in the base circuit of switch driver Q6. The positive voltage applied to the base circuit of Q6 clamps the stage in cutoff, thus inhibiting the cable current output. Capacitor C8 in the output circuit of Z1C prevents the current detection circuit from reacting to spurious change in cable current by preventing the output of Z1A from changing states for approximately 1 microsecond after Z1A switches from a logic 0 to a logic 1 output. The input to Z1B from amplifier Q4 in the start circuit is a logic 0 while the start circuit is energized to insure that a logic 1 is generated from Z1B while the cable constant current supply circuit is being energized.

(6) *Current sensing circuit.* The current sensing circuit is made up of comparison amplifier Z3 and a voltage divider circuit consisting of R9, CABLE CURRENT ADJ potentiometer R4 and R25. The voltage applied to one end (R9) of the voltage divider, at the junction of CR1 and CR3, is approximately -6 volts when the cable current is regulated at 38 milliamperes. The voltage at the opposite end (R25) of the voltage divider is held at approximately +6 volts at the junction of R25 and R26 by breakdown diode VR3. When CABLE CURRENT ADJ potentiometer R4 is adjusted to regulate the cable current at 38 milliamperes, the voltage applied from R4 to Z3 is approximately 0 volt. During normal operation, the output voltage from Z3-11, -12 is approximately -0.3 volt. An increase or decrease in cable current results in a change in the -6 volts at the junction of CR1 and CR3. Therefore, the increase or decrease in cable current causes a change in voltage across the voltage divider, and a bias voltage developed across R4 is applied to the noninverting input of Z3. If the cable current increases, the -6 volts become more negative and a negative-going bias voltage is applied to Z3. The negative bias voltage results in a more negative dc voltage level from Z3-11, -12. If the cable current decreases, the -6 volts become less negative and a positive-going bias voltage is applied to Z3 to develop a less negative dc output from Z3-11, -12. The dc voltage from Z3 is mixed with the output from the integrator circuit and applied to summing amplifier Z4. The -6 volts at the junction of CR1 and CR3 are also applied through pin 11 as the cable current sample voltage to the CABLE CUR output on METER SEL switch S7. When the cable current is within tolerance, an indication in the green band is obtained on TEST ALIGN meter M1 when METER SEL switch S7 is placed in the CABLE CUR position.

(7) *Summing amplifier Z4.* The negative dc voltage from comparison amplifier Z3, combined with the sawtooth voltage from the integrator circuit, is applied to the inverting input of summing amplifier Z4. Diode CR9, which is connected between the inverting input and the output of Z4, maintains the output voltage from Z4 at approximately 0 volt when the input voltage to Z4 is slightly negative or at 0 volt. When a positive voltage applied to the input of Z4 exceeds 0 volt, diode CR9 is back biased out of the circuit and the voltage gain of the amplifier increases to an open loop gain of 60 db. When the positive-going voltage applied to Z4 exceeds 0 volt, Z4 is

quickly biased into heavy conduction and when the input voltage starts decreasing in amplitude and approaches 0 volt, 24 is quickly biased into cutoff. The resultant output from 24 is a squared negative-going pulse each time the positive portion of the sawtooth voltage is applied to Z4 as shown in (5), figure 1-15. The amount of time that 24 conducts is proportional to the level of the dc voltage applied from Z3 to Z4; i.e., the more positive the dc voltage is, the longer Z4 is held in conduction. Therefore, the resultant output from Z4 to switch driver Q6 is negative pulses applied at a 3-kHz rate. When the cable current increases, the width of the output pulses decreases and when the cable current decreases, the width of the output pulses increases.

(8) *Switch drivers Q6 and Q7.* Switch drivers Q6 and Q7 are biased into conduction each time a negative pulse is applied to Q6 from summing amplifier Z4. The period of time that Q6 and Q7 conduct is determined by the width of the negative pulse output from Z4. When Q7 is cut off, -2.86 volts from the junction of R39 and R40 are applied as an inhibit voltage to T3-8 in the Royer circuit to disable the high voltage circuit as described in (9) below. When Q7 conducts, R40 is effectively bypassed to ground and a 0-volt enable potential is applied to T3-8. Therefore, during normal operation, the output from Q7 is a 3-kHz pulsed output that rises from a base voltage of -2.86 volts to a peak of 0 volt as shown in (6), figure 1-15. When switch Q5 in the start circuit conducts, a positive potential is applied to the junction of R34 and R35 in the base circuit of switch Q6. This condition prevents the negative pulses from summing amplifier Z4 from biasing Q6 into conduction. When Q6 is held in cutoff, the output from Q7 is a constant -3 volts, which bias Q4 and Q5 into cutoff, therefore inhibiting the high voltage circuits.

(9) *High voltage circuit.* The 3-kHz squared pulses from the secondary of T3-7 and T3-9 in the Royer circuit are applied to the bases of push-pull amplifiers Q4 and Q5. Push-pull amplifiers Q4 and Q5 alternately conduct only during the time that a 0-volt pulse is applied to T3-8 in the Royer circuit. A 3-kHz pulsating voltage is developed across the primary windings of step-up transformer T2 when Q4 and Q5 conduct. The 0-volt pulse applied to T3-8 is centered on the crossover time of the 3-kHz pulses applied to Q4 and Q5. This time relationship of the pulses insures that Q4 and Q5 have equal conduction time as shown in (7 and 8), figure 1-15. The high voltage output from T2 is rectified through full-wave diode bridge rectifier CR1, CR2, CR3, and CR4. The dc voltage from the rectifiers is filtered by choke input circuit L3, L4, and C8. The dc voltage at the output of high voltage circuit varies from approximately +10 volts (minimum loading) to +600 volts (maximum loading).

(10) *Bleeder circuit.* In normal operation, relay K1 is deenergized. Relay K1 is energized by a logic 0 (cable current light enable signal) from panel 12A3. The logic 0 signal is applied to K1 when the current detection circuit detects an out-of-tolerance condition and Z1B applies the no-current alarm signal (logic 0) to panel 12A3 through pin 4 on panel 12A1. When K1 energizes, R5 is connected through the closed contacts of K1 of ground. When grounded, R5 and R6 provide a bleeder path to ground to quickly discharge high voltage capacitors C1 and C8.

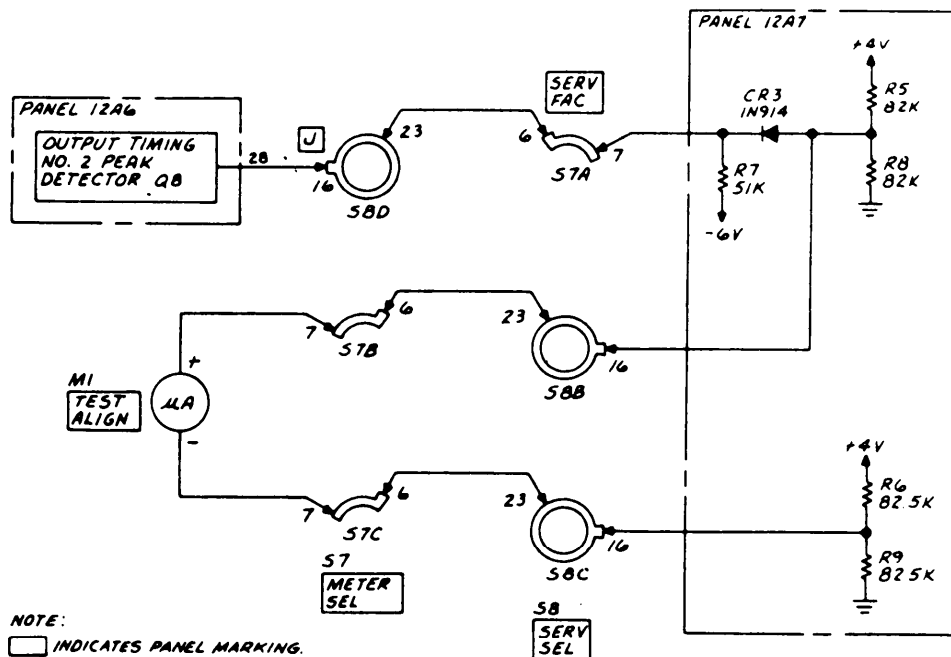
f. Meter Zero Set Circuit. The meter zero set circuit output is a reference voltage to TEST ALIGN meter M1 that causes a midscale (hairline) indication when the initial adjustment procedures of the cable fault locator function are performed. Amplifier Q1 is connected in series with resistors R4 and R5 to form a voltage divider circuit between -6 volts and the high voltage output from L4. ZERO SET potentiometer R2 on the front panel, which controls the bias voltage to amplifier Q1, is adjusted so that a 0-volt potential is present at the junction of Q1 and R4. A 0-volt potential at this point causes a midscale indication on TEST ALIGN meter M1. Breakdown diode VR1 functions as a meter protection circuit by conducting when the voltage at the junction of R4 and Q1 attempts to exceed +6.2 volts.

1-23. Service Facilities

a. *General.* The monitor circuit can be operated while the TD-754/G is operational without disturbing the overall operation. The TD-754/G is disabled when the cable fault locator circuit is used. The monitor circuit and the cable fault locator circuit use the controls and TEST ALIGN meter on the front panel of the TD-754/G.

b. *Monitor Circuit.* To monitor a specific test point in the TD-754/G, SERV SEL switch S8 and/or METER SEL switch S7 is used to select the input. The signal routing and monitoring functions for the timing No. 2 (SF-J) dc sample voltage from panel 12A6 are described in (1) below. The signal routing and monitoring functions for the +12v dc output from power supply assembly 12A1 are described in (2) below.

(1) When the output timing No. 2 pulses (figure 1-16) are proper, output timing No. 2 peak detector Q8 produces a +2v to +5v dc output that is routed to pin 16 on SERV SEL switch S8D. Placing SERV SEL switch S8 to the J position applies the dc voltage to pin 6 of METER SEL switch S7A. Placing METER SEL switch S7 in the SERV FAC position routes the dc voltage to the junction of CR3 and R7 on panel 12A7. The +dc voltage applied to the cathode of CR3 biases the diode into cutoff. When CR3 is cut off, the voltage at the junction of R5 and R8 goes to +2v dc. The +2v dc applied through S8B and S7B to the + input of TEST ALIGN meter M1 and the +2v dc applied from the junction of R6 and R9 to the - input of TEST ALIGN meter M1 through S8C and S7C cause an indication in the green band on the meter. If the output from output timing No. 2 peak detector Q8 is missing or less than +2v dc, then a faulty indication (out of the green band) is obtained, since diode CR3 conducts and a less positive voltage is applied to the + input of TEST ALIGN meter M1.

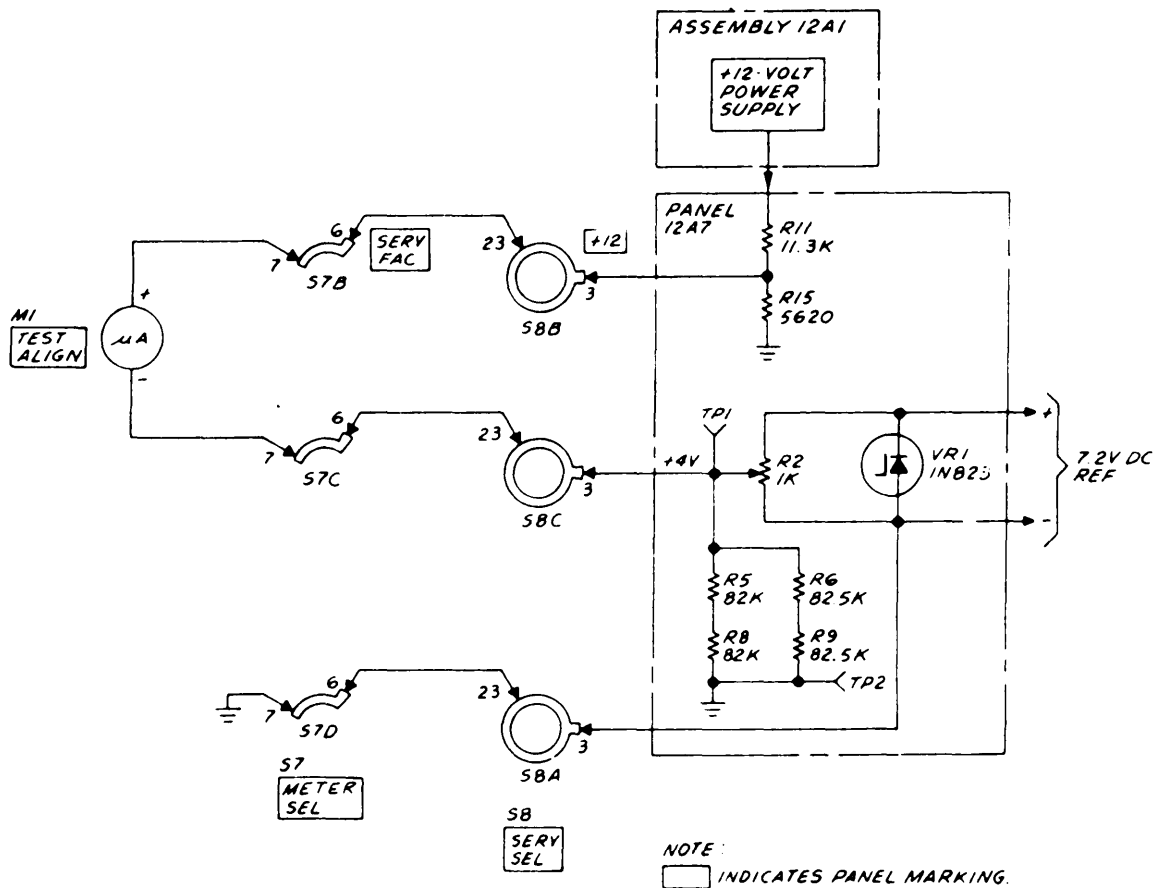


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Figure 1-16. Monitor Circuit, Typical DC Sample Voltage Test, Simplified Schematic Diagram.

(2) The output from the +12-volt power supply circuit (figure 1-17) is applied to voltage divider R11, R15 on panel 12A7. The +4v dc at the junction of R11 and R15 is applied to pin 3 of SERV SEL switch S8B. When SERV SEL switch S8 is placed to the +12 position and METER SEL switch S7 is placed to the SERV FAC position, the +4v dc is applied to the + input of TEST ALIGN meter M1. The +4v dc at the junction of R2 and R5 is applied through S8C and S7C to the - input of TEST ALIGN meter M1. Therefore, when the +12V dc output is proper, +4v dc is applied to both inputs on TEST ALIGN meter M1, causing an indication in the green band on the meter.

(3) Potentiometer R2 on panel 12A7 is adjusted for +4 volts as measured between TP1 and TP2. Breakdown diode VR1 provides a constant 6.2v dc across potentiometer R2. Breakdown diode VR1 is referenced to ground through the closed contacts of S8A and S7D when potentiometer R2 is adjusted and when most dc sample and dc power voltages are being monitored. The +4 volts across TP1 and TP2 is monitored by placing SERV SEL switch S8 to the REF position, placing METER SEL switch S7 in the SERV FAC position, and observing the indication on TEST ALIGN meter M1. An indication in the yellow band is obtained when the reference voltage is within tolerance.



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Figure 1-17. Monitor Circuit, Typical Dc Power Voltage Test, Simplified Schematic Diagram.

c. *Cable Fault Locator Circuit* (figure 1-18). The high voltage circuit on power supply assembly 12A1 provides a regulated cable current of 38 milliamperes into the cable link to power the TD-206/G's. Each TD-206/G contains a cable fault locator circuit that consists of transistor Q6 and precision resistor R16. When the TD-206/G is operating and producing a pulse output to the cable link, transistor Q6 conducts and effectively shorts out R16. When no pulses are applied to the TD-206/G, transistor Q6 is cut off and R16 appears in series with the cable link.

(1) Initially, METER SEL switch S7 is placed in the SERV FAC position, SERV SEL switch S8 is placed to FL position, FAULT LOC MILES switches S1 and S2 are placed in their 0 positions, and READ-ZERO SET-NORM OPR switch S2 is placed to ZERO SET. Placing switch S2 in the ZERO SET position removes the timing input to the cable output circuits. This disables the pulse outputs from the transmit circuits to the cable link. With no pulses on the cable link, all the TD-206/G's in the cable link are disabled and their resistors R16 are in series with the cable current.

(2) ZERO SET potentiometer R1 is adjusted until a 0-volt potential is present at the junction of Q1 and R4. This causes a midscale deflection on TEST ALIGN meter M1. Therefore, a midscale indication on TEST ALIGN meter M1 is produced with all resistors R16 are in series with the cable link.

(3) READ-ZERO SET-NORM OPR switch S2 is placed to the READ position. This applies the traffic control (ground) signal to the transmit circuits to disable the pcm-1 and pcm-2 input circuits. The 576-kHz or 2304-kHz timing pulses from panel 12A6 are applied to the cable output circuits in the transmit circuits. This causes pcm pulses to be applied to the cable link at the 576-kHz or 2304-kHz bit rate. MODE switch S4 in the 6/12 or 24 position causes the pcm pulses at the 576-kHz bit rate to be generated. MODE switch S4 in the 48AR position causes the pcm pulses at the 2304-kHz bit rate to be generated. The selected pulse frequency does not affect the operation of the cable fault locator function.

(4) With READ-ZERO SET-NORM OPR switch S2 in the READ position, the cable current path from the high voltage circuit is routed through FAULT LOC MILES switches S1 and S3 to transform T1 in the cable output circuits. Switches S1 and S3 are operated until a midscale indication is obtained on TEST ALIGN meter M1. Each position of switch S3 represents the series resistance of one TD-206/G. Each position of switch S1 represents the series resistance of 10 TD-206/G's. Therefore, a total of 39 TD-206/G's can be simulated by switches S1 and S3. Once the midscale indication of TEST ALIGN meter M1 is obtained, the defective restorer is determined by noting the positions of FAULT LOC MILES switches S1 and S3. For example, S1 in the 10 position and S3 in the 5 position indicates that the first 15 TD-206/G's are operational and the 16th TD-206/G is defective.

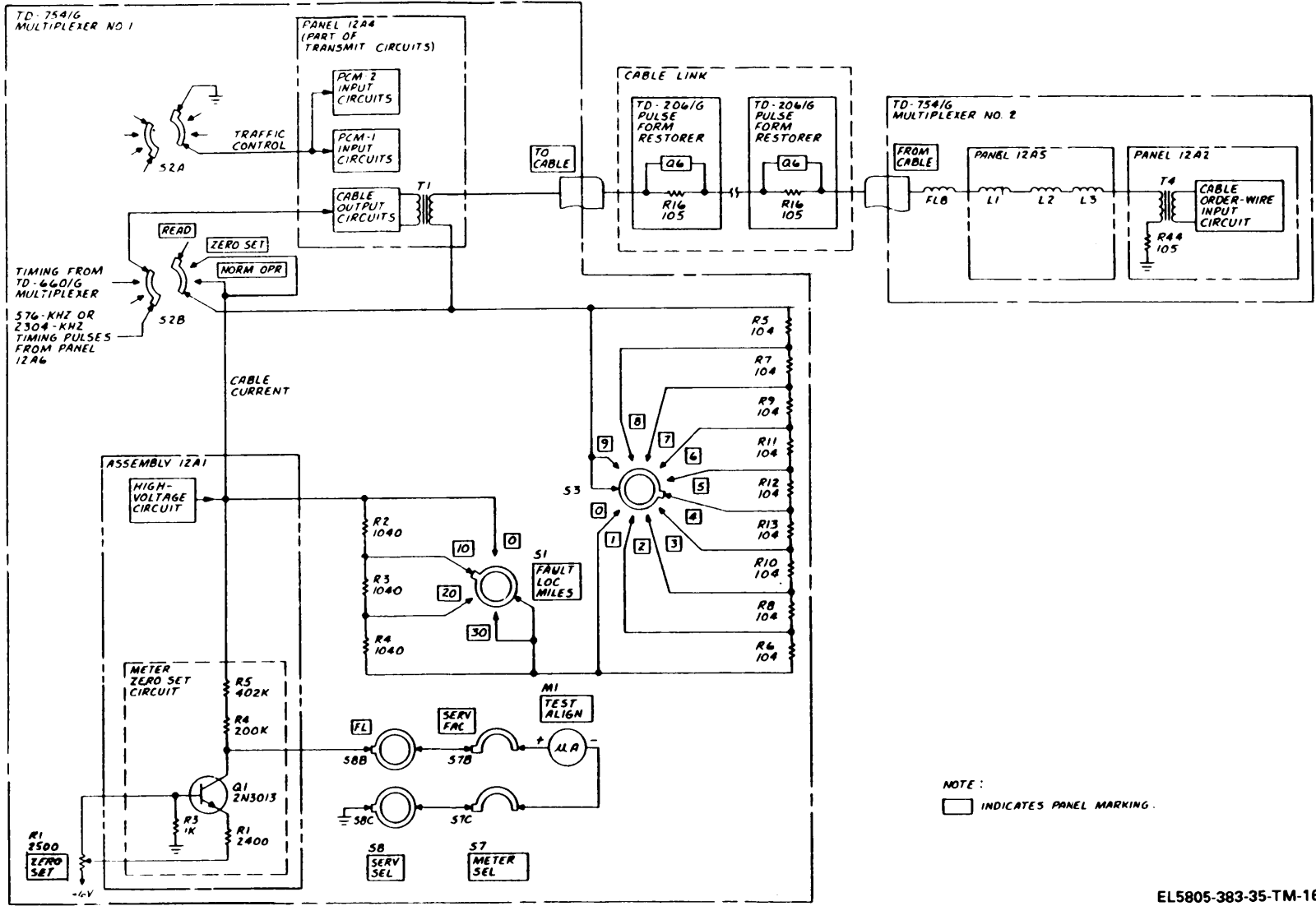


Figure 1-18. Cable Fault Locator Circuit.

NOTE: INDICATES PANEL MARKING.

CHAPTER 2

DIRECT SUPPORT MAINTENANCE

	Page
Section I Repair Parts, Special Tools, TMDE and Support Equipment	2-1
Section II Direct Support Troubleshooting	2-4
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Section I. REPAIR PARTS, SPECIAL TOOLS, TMDE AND SUPPORT EQUIPMENT

Para.		Page
2-1	Common Tools and Equipment	2-1
2-2	Special Tools, TMDE and Support Equipment	2-1
2-3	Repair Parts	2-4

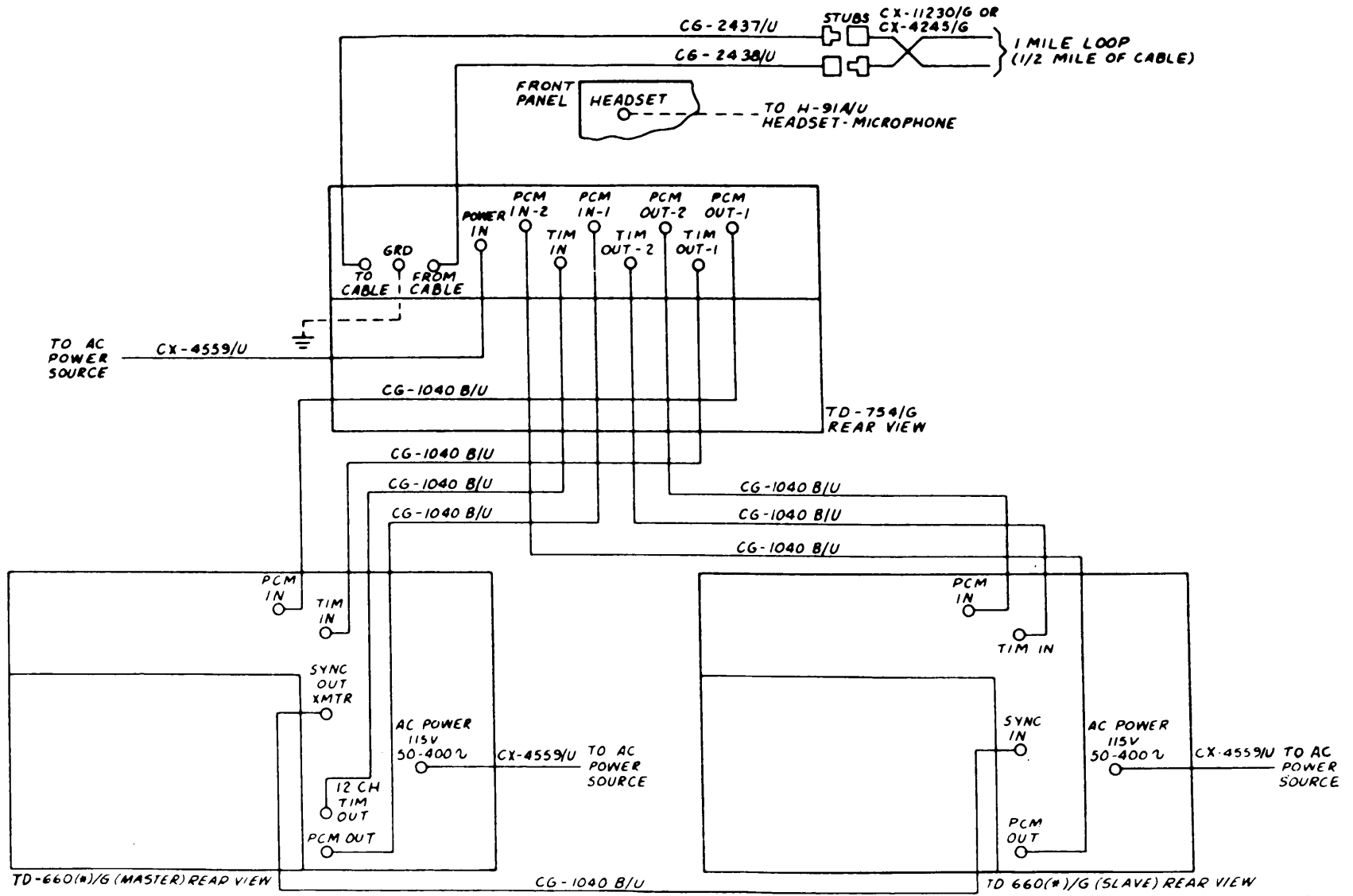
2-1. Common Tools and Equipment

A complete list of common tools and tool kits required for direct support maintenance and testing of the multiplexer is given in Appendix B of TM11-5805-383-12. In addition, each maintenance paragraph in this chapter lists the specific tools and equipment required for the procedure outlined in that paragraph.

2-2. Special Tools, TMDE and Support Equipment

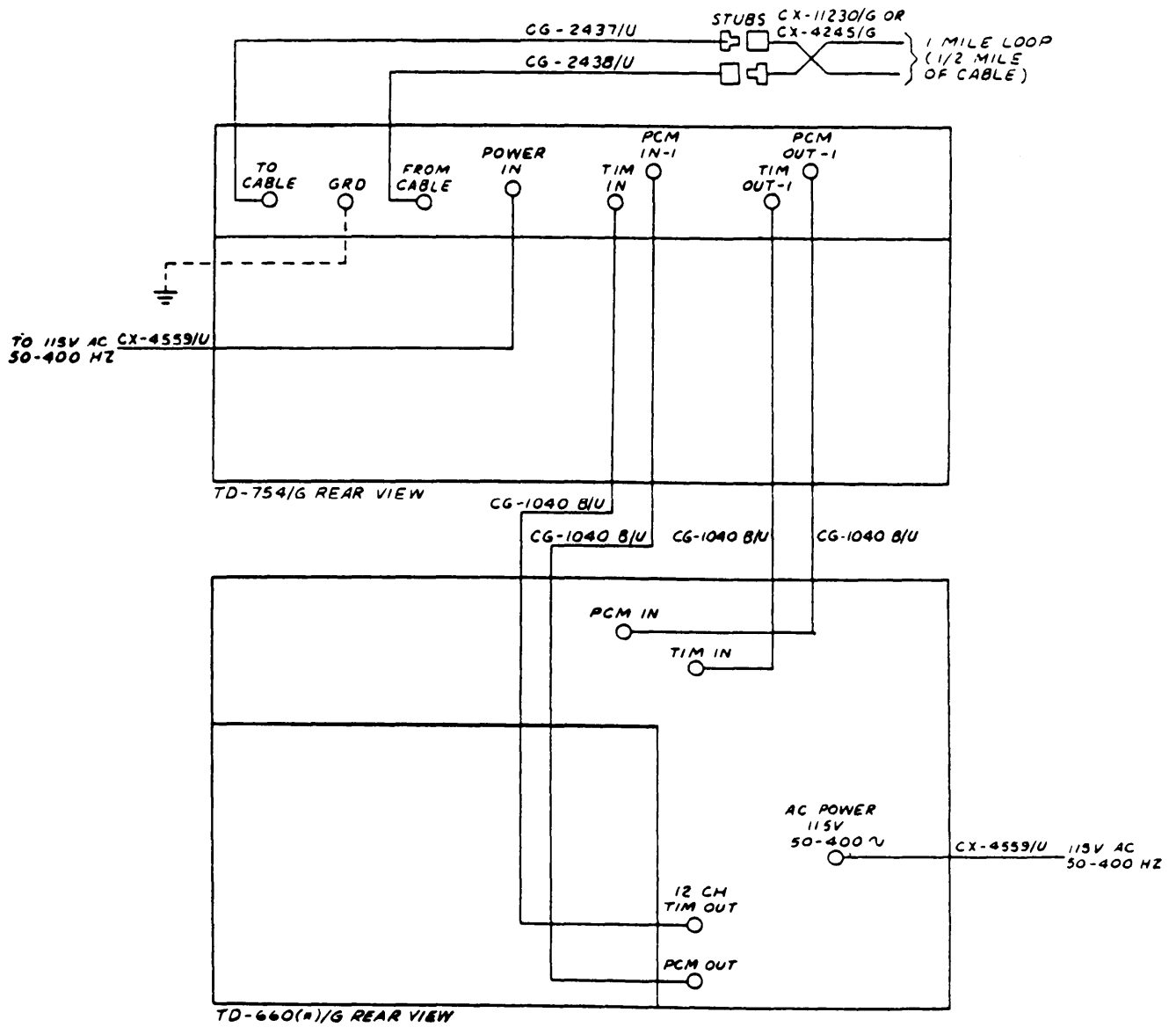
Two extension test cables are required for testing and troubleshooting power supply assembly 12A1. These cables are fabricated at direct support level. Fabrication data can be found in appendix C, List of Manufactured Items. In addition to the extension test cables, the following equipment is required for direct support maintenance. Items a. through h. are required if troubleshooting, testing and alignment are to be performed with the TD-754/G in a feedback loop test setup (figures 2-1 and 2-2). Item "i" is required for plug-in panel alignment.

- a. Amphenol connector, PN 57-10240-1 (NSN 5935-00-687-2204) (2 required)
- b. Amphenol connector, PN 57-20240-1 (NSN 5935-00-921-3450)(2 required)
- c. Cable Assembly CG-2437/U
- d. Cable Assembly CG-2438/U
- e. Cable Assembly CX-1040B/U (8 required)
- f. Cable Assembly CX-4559/U (3 required)
- g. Cable Assembly CX-11230/G or CX-4245/G (2 quarter-mile spools required)
- h. Adapter, Cable Assembly CX-10734/G (2 required)
- i Extender Panel MX-8898/G
- j. Multiplexer TD-660(*)/G (2 required)



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Figure 2-1. TD-754/G Performance Test Setup.



EL5805-383-35-TM-26

Figure 2-2. Troubleshooting and Alignment Test Setup.

2-3. Repair Parts

Repair parts for direct support maintenance of the multiplexer are listed and illustrated in TM 11-5808-383-20P and -34P.

Section II. DIRECT SUPPORT TROUBLESHOOTING

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2-4	General2-4
2-5	Preliminary Procedures 2-5
2-6	Overall System Troubleshooting. 2-6
2-7	Power Supply Assembly Troubleshooting 2-10
2-8	Power Supply Component Voltage Testing2-20
2-9	Continuity Testing2-22

2-4. General

The first step in troubleshooting is to trace the fault to a specific system or subsystem. The next step is to localize the fault to a particular assembly, such as a plug-in panel or control panel. The final step is to isolate the fault. Isolating is tracing the fault to a defective component, such as a resistor, capacitor, diode, relay or switch. Fault isolation is limited to those components which maybe repaired or replaced at direct support level.

Troubleshooting procedures to localize a fault to panel A3 in power supply assembly 12A1 and to isolate a defective component on 12A1A3 are authorized at direct support level. Isolation of a defective component on 12A1A1 or 12A1A2 is not authorized. Troubleshooting to isolate a faulty part that is not mounted on a plug-in panel (12A2 through 12A6) or panel 12A7 is authorized at direct support. Continuity testing may also be done at direct support to supplement troubleshooting procedures, and to locate wiring defects.

A faulty panel or individual component can be isolated by making voltage measurements or waveform checks. The troubleshooting methods selected should be based on directions in the appropriate troubleshooting section and by analysis of circuits on the applicable schematic and wiring diagrams.

Troubleshooting procedures may be performed while the TD-754/G is operating in the system configuration, connected in the feedback loop configuration (figure 2-2), or after the TD-754/G has been removed from service. When trouble occurs, make as many observations and applicable measurements as possible to determine if the fault is in the TD-754/G or is elsewhere in the system.

This section has two troubleshooting tables. Table 2-1 pertains to the overall system, and table 2-2 pertains to the power supply assembly. Each table lists common malfunctions that may occur during operation and maintenance of the multiplexer after unit maintenance has been performed. Each malfunction is followed by a list of tests or inspections and corrective actions. These tests or inspections and corrective actions should be performed in the order listed. This manual cannot list all malfunctions that may occur. If you encounter a problem that is not listed or cannot be corrected by the listed corrective actions, notify your supervisor.

WARNING

Dangerous voltages exist in the TD-754/G that may cause death or injury to personnel. 115 volts ac are present in the equipment when PWR switch is operated to ON, and a dc voltage of up to 1,000 volts may be present in the equipment when CABLE CURRENT switch is operated to ON. When troubleshooting or repairing the TD-754/G, be careful not to contact ac or dc high voltage connections in the equipment. Use insulated test probes when making measurements or waveform checks. Always operate PWR and CABLE CURRENT switches to OFF before connecting test probes to the TD-754/G.

Whenever the TD-754/G is removed from its rack mounting and powered up for operation, bench testing, service or maintenance, an external ground must be applied, by connecting a jumper wire from TD-754/G ground stud (or case) to bench ground stud, before turning power on. Jumper wire must be of equal or larger gauge than power input wire.

CAUTION

Always operate CABLE CURRENT and PWR switches to OFF before removing power supply assembly 12A1. Failure to turn off power may result in damage to equipment.

NOTE

After trouble has been corrected, appropriate unit level alignment and checkout procedures should be performed, as described in TM 11-5805-383-12, to make sure the TD-754/G is serviceable.

2-5. Preliminary Procedures

Before using the troubleshooting charts, perform the following procedures:

- a. If the +12-volt, +5-volt, or -6-volt indications on TEST ALIGN meter M1 are marginal, adjust the appropriate potentiometer on power supply assembly 12A1 for a hairline indication on TEST ALIGN meter M1 as authorized at the unit maintenance level. (Refer to TM 11-5805-383-12.)
- b. If operation of the order wire facilities is marginal, check the adjustments authorized at the unit maintenance level. (Refer to TM 11-5805 -383-12.)
- c. Insure that the correct plug-in panel (12A2 through 12A6) was substituted for a specific trouble symptom and that the identical trouble symptom still exists after substitution of a known good panel. Ensure that each plug-in panel is properly seated in its respective receptacle.
- d. Visually check equipment for physical damage to wiring, panel switches, receptacles, etc., in the TD-754/G.

2-6. Overall System Troubleshooting

Troubleshooting is performed with the TD-754/G connected in a system, or connected in a loopback test setup as described in TM 11-5805-383-12. Either configuration produces the required pcm inputs and outputs. Refer to figure FO-8, the overall TD-754/G schematic diagram, for applicable voltages and resistances of components under test. The components itemized in the chart below are mounted on the TD-754/G chassis and shown in figure 2-3.

Table 2-1. Direct Support System Troubleshooting.

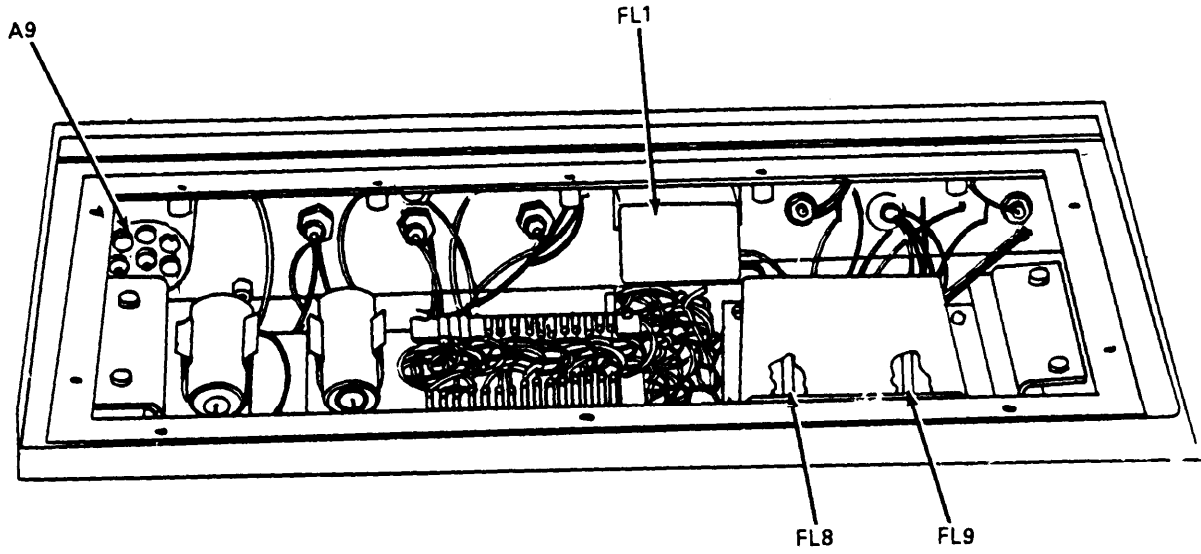
Malfunction	Test or Inspection	Corrective Action
1. PWR INDICATOR ON FRONT PANEL REMAINS OFF WHEN PWR SWITCH IS OPERATED TO ON.	Step 1. Check POWER IN receptacle/fitter FL1 on rear panel.	Replace FL1 if defective.
	Step 2. Check PWR switch on power supply 12A1.	Replace power supply 12A1.
2. TEST ALIGN METER FAILS TO INDICATE IN GREEN BAND WHEN METER SEL SWITCH IS OPERATED TO TIM-IN AND READ-ZERO SET-NORM OPR SWITCH IS OPERATED TO NORM OPR.	Check READ-ZERO SET-NORM OPR switch S2 on front panel.	Replace S2 if defective.
3. TEST ALIGN METER FAILS TO INDICATE IN GREEN BAND WHEN SERV-SEL SWITCH IS OPERATED TO F (AND PCM IS APPLIED TO TD-754/G) AND METER SEL SWITCH IS OPERATED TO SERV FAC.	Check filter FL8 in top of multiplexer.	Replace FL8 if defective.
4. OUTPUT PCM PULSES TO CABLE LINK ARE WEAK, DISTORTED OR MISSING.	Check filter FL9 in top of multiplexer.	Replace FL9 if defective.

Table 2-1. Direct Support System Troubleshooting (cont).

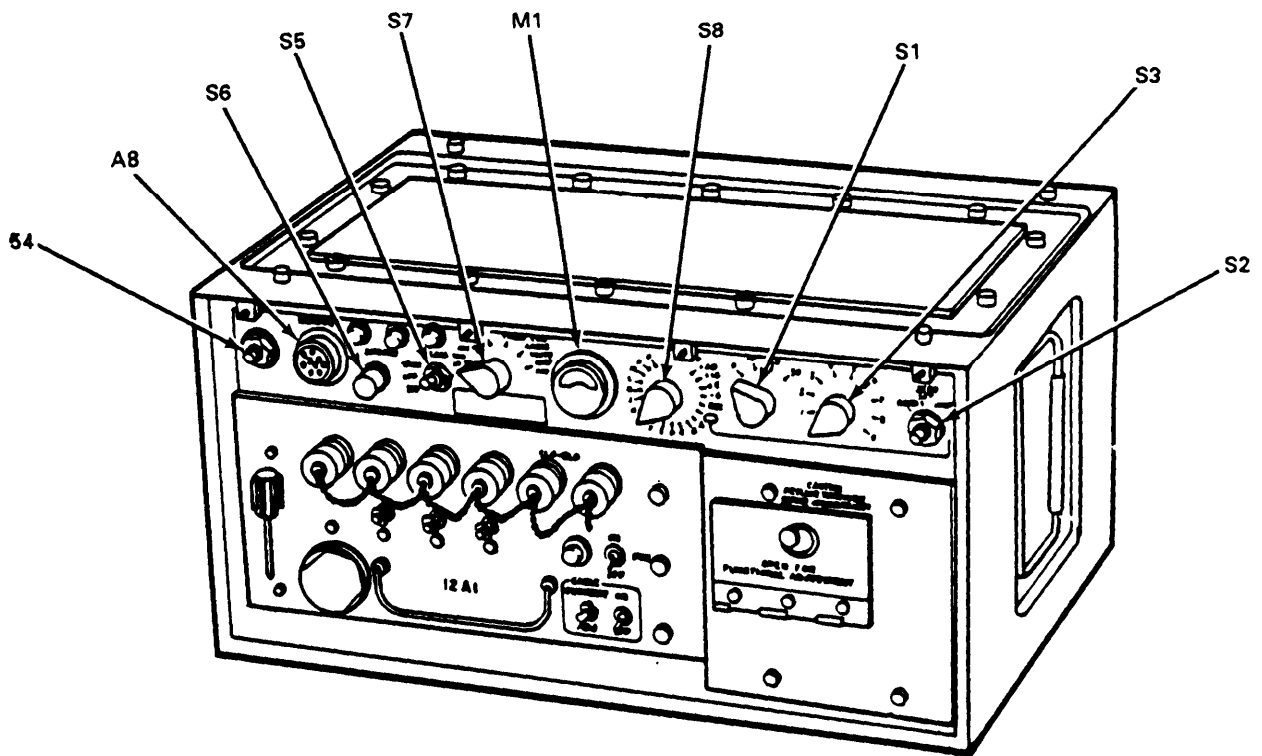
Malfunction	Test or Inspection	Corrective Action
5. RING SIGNAL NOT GENERATED WHEN TALK-OFF-SIG SWITCH IS OPERATED TO SIG.	Check switch S5 on front panel.	Replace S5 if defective.
6. AUDIO FROM ATTACHED H-91A/U NOT APPLIED TO PANEL 12A2.	Step 1. Check switch S5 on front panel.	Replace S5 if defective.
	Step 2. Check filter assembly 12A8 on front panel.	Replace 12A8 if defective (para. 2-13).
7. ORDER WIRE AUDIO TO ATTACHED H-91A/U IS FAULTY OR MISSING.	Step 1. Check switch S5 on front panel.	Replace S5 if defective.
	Step 2. Check filter assembly 12A8 on front panel.	Replace 12A8 if defective (para. 2-13).
8. AUDIBLE ALARM FAILS TO TURN ON OR OFF WHEN BUZZER OFF SWITCH IS PRESSED.	Check BUZZER OFF switch S6 on front panel.	Replace S6 if defective.
9. MODE OF OPERATION CANNOT BE SELECTED.	Check MODE switch S4 on front panel.	Replace S4 if defective.
10. PATCH-THRU INPUT AND OUTPUT SIGNALS MISSING OR FAULTY.	Check filter assembly 12A9 on rear panel.	Replace 12A9 if defective (para. 2-14),

Table 2-1. Direct Support System Troubleshooting (cont).

Malfunction	Test or Inspection	Corrective Action
<hr/>		
11. CABLE FAULT LOCATOR CIRCUIT IS FAULTY.		
	Step 1. Check READ-ZERO SET-NORM OPR switch S2.	Replace S2 if defective.
	Step 2. Check FAULT LOC MILES switch S1.	Replace S1 if defective.
	Step 3. Check FAULT LOC MILES switch S3.	Replace S3 if defective.
	Step 4. Check ZERO SET potentiometer R1.	Replace R1 if defective.
12. MONITOR CIRCUIT IS FAULTY..		
	Step 1. Check METER SEL switch S7.	Replace S7 if defective.
	Step 2. Check SERV SEL switch S8.	Replace S8 if defective.
	Step 3. Check TEST ALIGN meter M1.	Replace M1 if defective.



A. TOP VIEW WITH COVER REMOVED



B. FRONT VIEW

4858-004

Figure 2-3. TD-754/G Component Locations.

2-7. Power Supply Assembly 12A1 Troubleshooting

To troubleshoot the power supply, the power supply must be removed from the TD-754/G and electrically connected back to the TD-754/G using two extension test cables. (Refer to appendix C for test cable fabrication data.) One test cable shall be connected from receptacle J1 on power supply 12A1 to receptacle J17 on the TD-754/G. The second test cable shall be connected from receptacle J2 on power supply 12A1 to receptacle 12A1-J2 on the TD-754/G.

When the TO CABLE and FROM CABLE receptacles are not terminated into a cable configuration, a pair of cables, CG-2437/U and CG-2438/U, shall be connected in a shorted configuration between the two receptacles. This is necessary to complete a current path for the output of the cable constant current circuit in the power supply.

Heat sink assembly 12A1A3, a component of the power supply, is mounted to the rear panel of the TD-754/G. The heat sink assembly must be removed from the TD-754/G case (paragraph 2-12) in order to be tested. If necessary, the heat sink assembly can be removed from the TD-754/G case and then connected directly to the power supply by connecting one of the extension test cables from the heat sink assembly receptacle directly to J2 on power supply 12A1.

Locations of the components itemized in the troubleshooting chart are shown in figure 2-4. The schematic for the power supply, including head sink assembly 12A1A3, is given in figure FO-2. Voltages for components under test are given in paragraph 2-8, and shown in figure FO-2.

WARNING

Dangerous voltages exist in the TD-754/G that may cause death or injury to personnel. 115 volts ac are present in the equipment when PWR switch is operated to ON, and a dc voltage of up to 1,000 volts may be present in the equipment when CABLE CURRENT switch is operated to ON. When troubleshooting the TD-754/G, be careful not to contact ac or dc high voltage connections in the equipment. Use insulated test probes when making measurements or waveform checks. Always operate PWR and CABLE CURRENT switches to OFF before connecting test probes to the TD-754/G.

CAUTION

Always operate the CABLE CURRENT and PWR switches to OFF before removing power supply assembly 12A1. Failure to turn off power may result in damage to equipment.

NOTE

If trouble with your equipment is not corrected by procedures in troubleshooting chart, perform a continuity check (para. 2-9).

Panels 12A1A1 and 12A1A2 are removed from power supply 12A1 by depot only. If it is determined that either board is faulty, return 12A1 with both boards attached. It is not necessary to return heat sink assembly 12A1A3 with power supply.

Table 2-2. Direct Support Power Supply Troubleshooting.

Malfunction	Test or Inspection	Corrective Action
1. ALL DC VOLTAGES ARE MISSING.		<p>Check for defective power switch S1 or transformer T1 on 12A1.</p> <p>Return power supply to depot for repair.</p>
2. +12-VOLT OUTPUT AT TP1 ON 12A1 IS MISSING OR CANNOT BE REGULATED.		<p>a. Check for defective +12V potentiometer R1, transformer T1, capacitor C1 or choke L1A on 12A1.</p> <p>Return power supply to depot for repairs.</p> <p>b. Check for defective transistor Q1 on heat sink panel 12A1A3.</p> <p>Replace Q1 (para. 2-12).</p> <p>c. Check for defective components on panel 12A1A2.</p> <p>Return power supply to depot for repairs.</p>
3. RIPPLE IS EXCESSIVE ON +12-VOLT OUTPUT.		<p>Check for defective capacitor C1 or choke L1A on 12A1.</p> <p>Return power supply to depot for repairs.</p>
4. +28-VOLT OUTPUT IS MISSING OR OUT OF TOLERANCE.		<p>a. Check for defective transformer T1, choke L2, or capacitor C4, C5 or C6 on 12A1.</p> <p>Return power supply to depot for repair.</p> <p>b. Check for defective diode CR1, CR2, CR3 or CR4 on heat sink panel 12A1A3.</p> <p>Replace defective diode(s) (para. 2-12).</p> <p>c. Check for defective components on panel 12A1A2.</p> <p>Return power supply to depot for repair.</p>

Table 2-2. Direct Supped Power Supply Troubleshooting (cont).

Malfunction

Test or Inspection

Corrective Action

5. RIPPLE IS EXCESSIVE ON +28-VOLT OUTPUT.

Check for defective choke L2 or capacitor C4, C5 or C6 on 12A1.

Return power supply to depot for repair.

6. +5-VOLT OUTPUT IS MISSING OR CANNOT BE REGULATED.

a. Check for defective +5V potentiometer R2, transformer T1, capacitor C2 or choke L1B on 12A1.

Return power supply to depot for repair.

b. Check for defective transistor Q2 on heat sink panel 12A1A3.

Replace transistor Q2 (para. 2-12).

c. Check for defective components on panel 12A1A2.

Return power supply to depot for repair.

7. RIPPLE IS EXCESSIVE ON +5-VOLT OUTPUT.

Check for defective capacitor C2 or choke L1B on 12A1.

Return power supply to depot for repair.

8. -6-VOLT OUTPUT IS MISSING OR CANNOT BE REGULATED.

a. Check for defective -6V potentiometer R3, transformer T1, capacitor C3, or choke L1C on 12A1.

Return power supply to depot for repair.

b. Check for defective transistor Q3 on heat sink panel 12A1A3.

Replace transistor Q3 (para. 2-12).

c. Check for defective components on panel 12A1A2.

Return power supply to depot for repair.

Table 2-2. Direct Support Power Supply Troubleshooting (cont).

Malfunction	Test or Inspection	Corrective Action
9. RIPPLE IS EXCESSIVE ON -6-VOLT OUTPUT.		<p>Check for defective capacitor C3 or choke L1C on 12A1.</p> <p>Return power supply to depot for repair.</p>
10. REFERENCE POWER SUPPLY CIRCUIT OUTPUT IS MISSING OR INCORRECT (NOMINAL 7.2 VDC ACROSS E40 AND E41 ON PANEL 12A1A2).		<p>a. Check for defective transformer T1 on 12A1.</p> <p>Return power supply to depot for repair.</p> <p>b. Check for defective components on 12A1A2.</p> <p>Return power supply to depot for repair.</p>
11. CABLE CURRENT REMAINS OFF WHEN CABLE CURRENT SWITCH S2 IS OPERATED TO ON (CABLE CURRENT ADJ POTENTIOMETER R4 PROPERLY ADJUSTED OR SET TO MIDSCALE).		<p>a. Check for defective CABLE CURRENT switch S2, CABLE CURRENT ADJ potentiometer R4, transformer T2 or T3, choke L3 or L4, or capacitor C8 on 12A1.</p> <p>Return power supply to depot for repair.</p> <p>b. Check for defective transistor Q4 or Q5 on heat sink panel 12A1A3</p> <p>Replace transistor(s) (para. 2-12).</p> <p>c. Check for defective components on panel 12A1A1.</p> <p>Return power supply to depot for repair.</p>
12. CABLE CURRENT IS PRESENT BUT CANNOT BE ADJUSTED TO REMAIN WITHIN TOLERANCE USING CABLE CURRENT ADJ POTENTIOMETER R4.		<p>a. Check for defective CABLE CURRENT ADJ potentiometer R4 on 12A1.</p> <p>Return power supply to depot for repair,</p> <p>b. Check for defective components on panel 12A1A1.</p> <p>Return power supply to depot for repair.</p>

Table 2-2. Direct Supped Power Supply Troubleshooting (cont).

Malfunction

Test or Inspection

Corrective Action

13. E13 IN BLEEDER CIRCUIT IS NOT CONNECTED TO GROUND WHEN CABLE CURRENT SWITCH S2 IS OPERATED TO OFF.

Check for defective relay K1 on 12A1.

Return power supply to depot for repair.

14. LOW CABLE CURRENT OUTPUT FROM POWER SUPPLY ASSEMBLY 12A1.

- a. Check for defective relay K1 on 12A1.

Return power supply to depot for repair.

- b. Check for defective components on panel 12A1A1.

Return power supply to depot for repair.

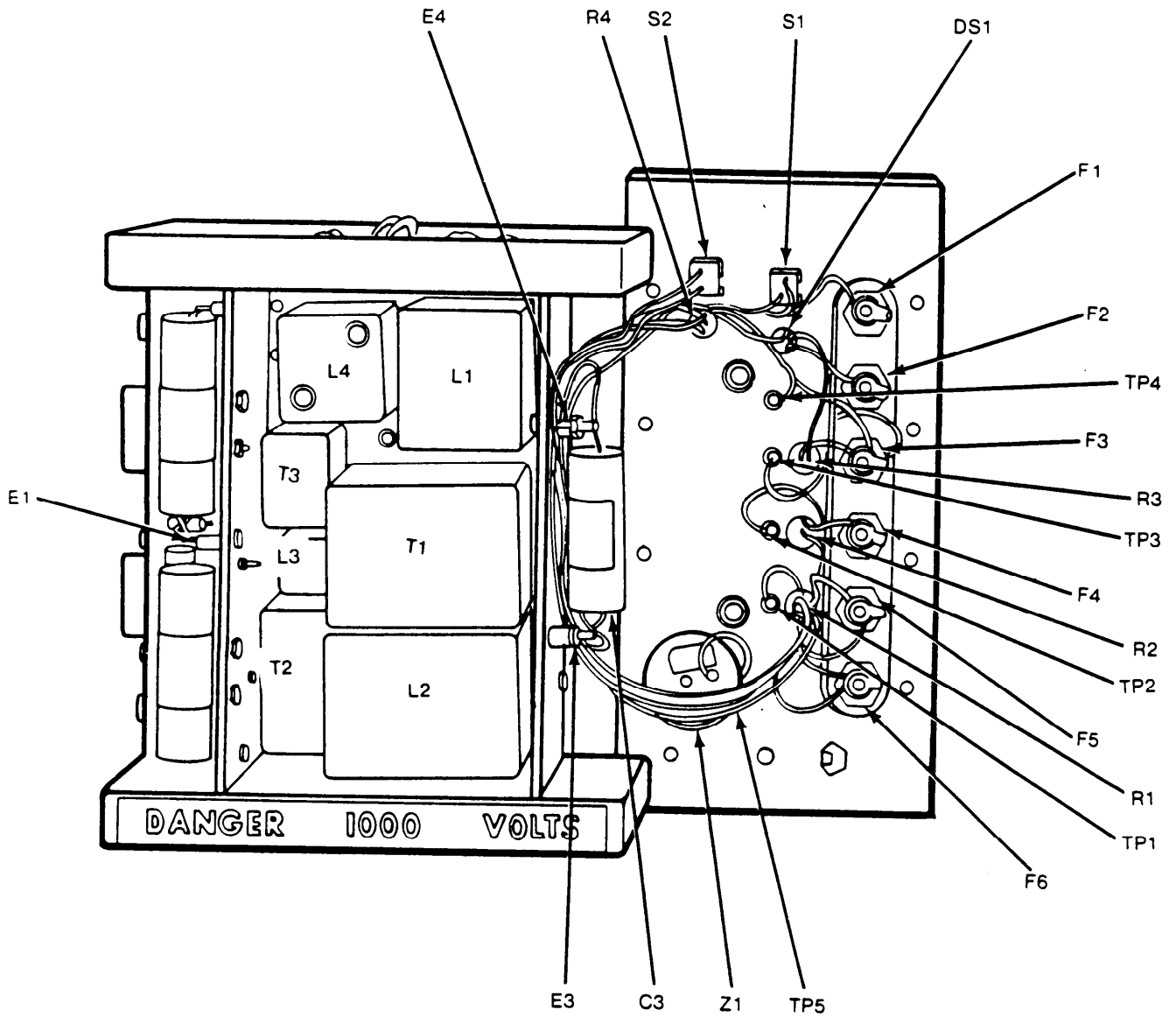
15. INDICATION ON TEST ALIGN METER M1 CANNOT BE CENTERED BY USING ZERO SET POTENTIOMETER R1

- a. Check for defective ZERO SET potentiometer R1 on TD-754/G front panel.

Replace R1,

- b. Check for defective meter zero set circuit on panel 12A1A1.

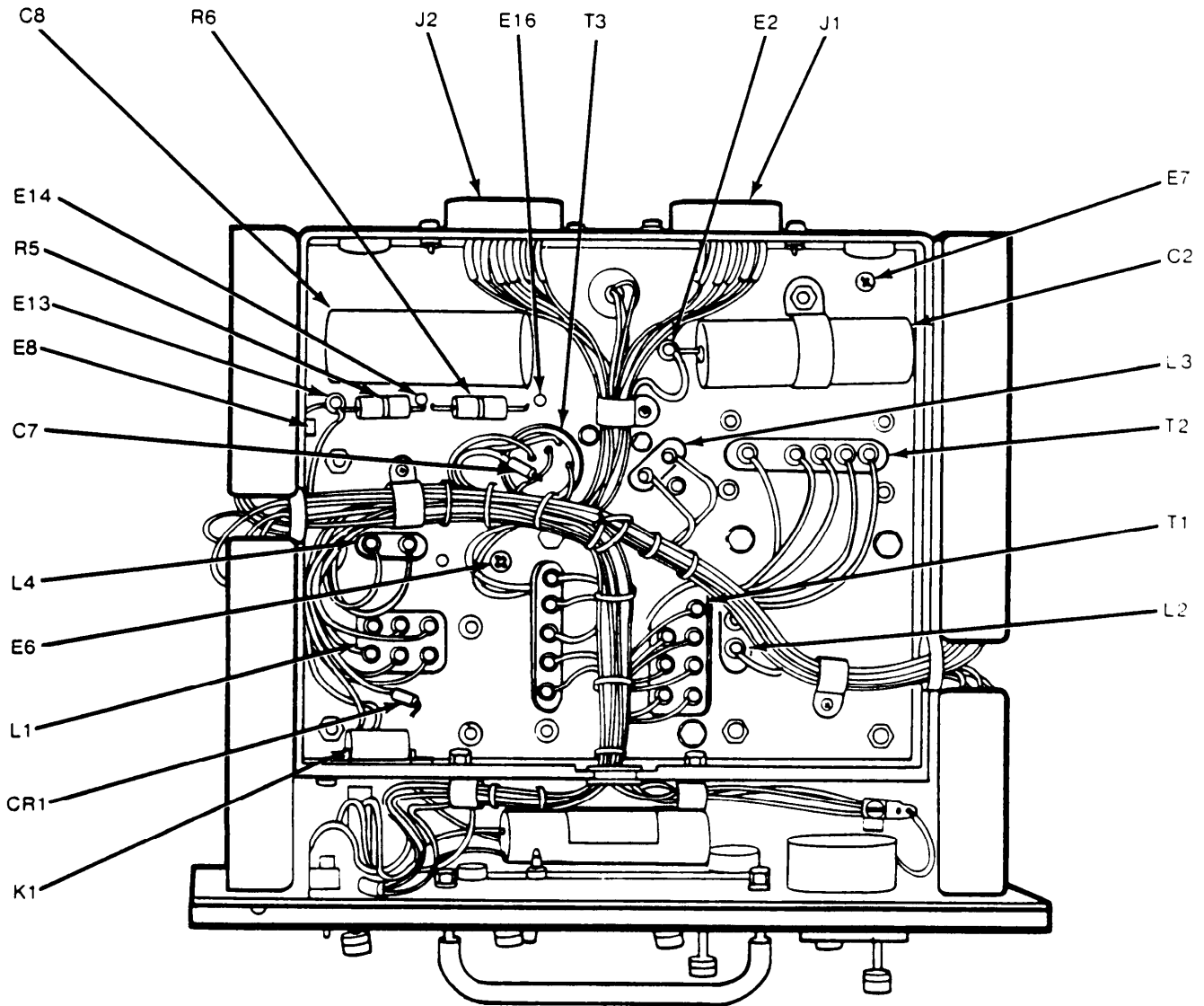
Return power supply to depot for repair.



A. POWER SUPPLY REAR VIEW OF FRONT PANEL

4858-005.1

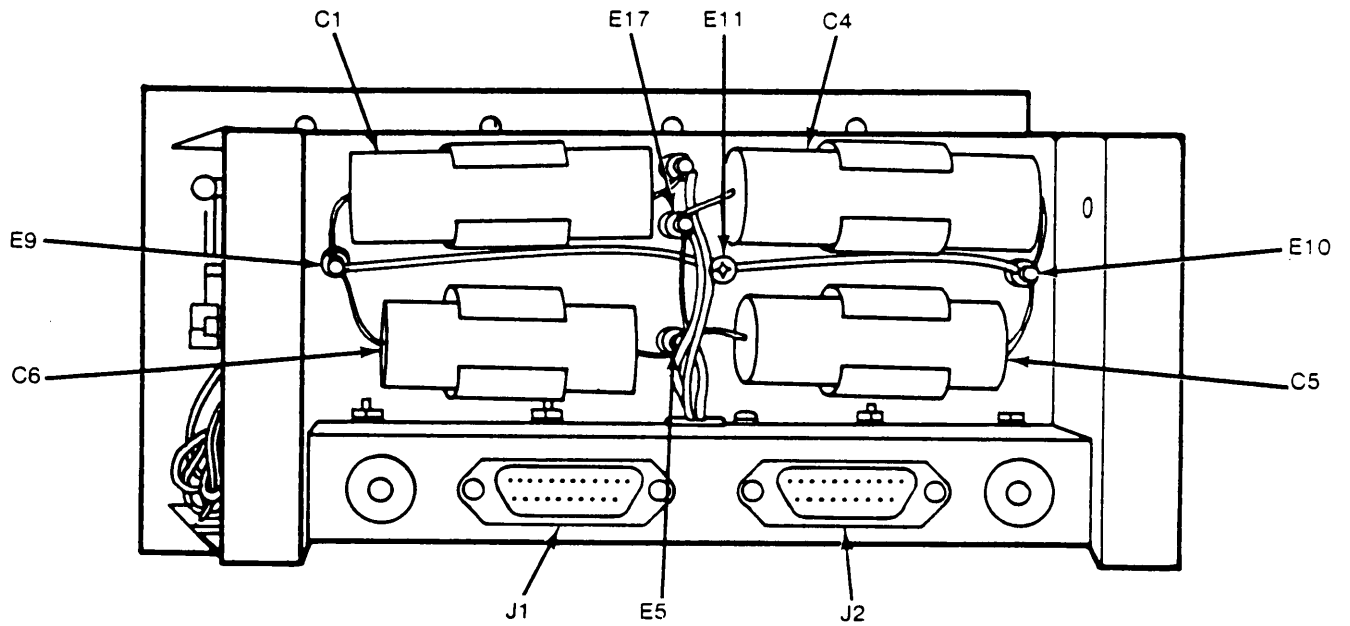
Figure 2-4. Power Supply Component Locations (Sheet 1 of 5).



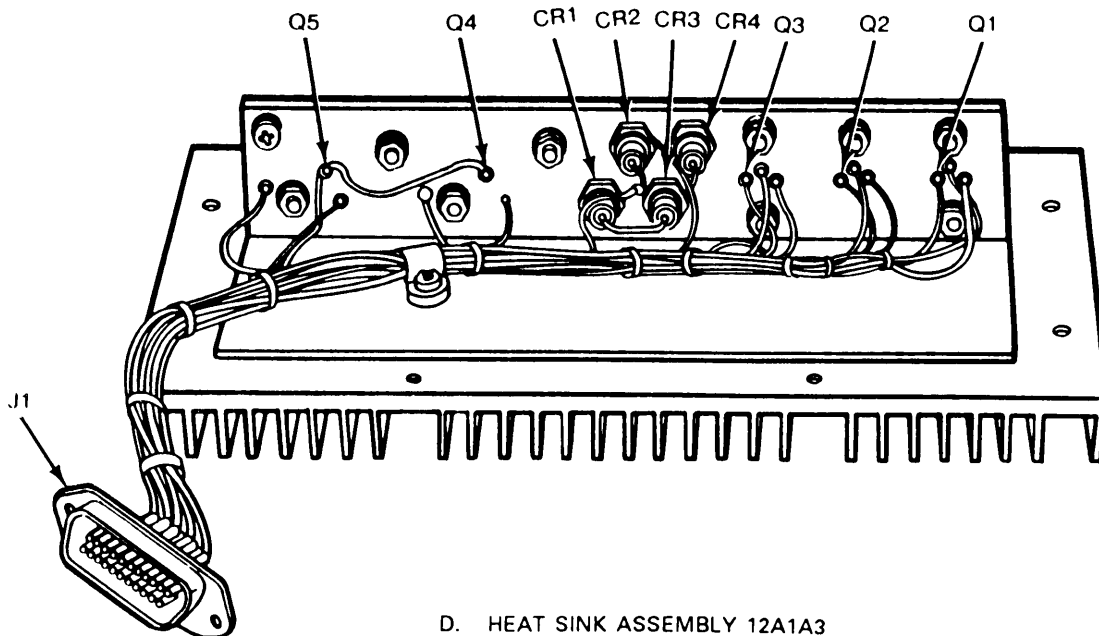
B. POWER SUPPLY BOTTOM VIEW

4858-005.2

Figure 2-4. Power Supply Component Locations (Sheet 2 of 5).

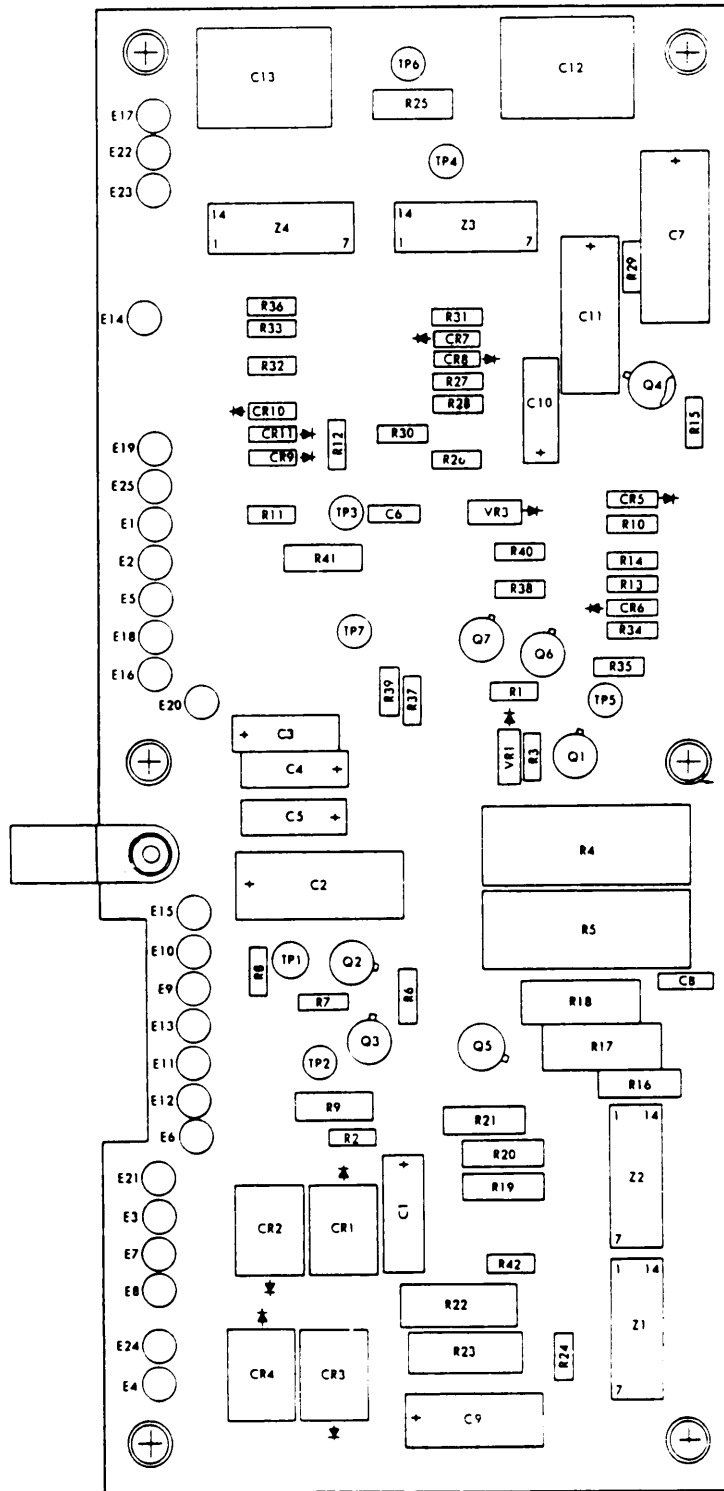


C. POWER SUPPLY REAR VIEW



D. HEAT SINK ASSEMBLY 12A1A3

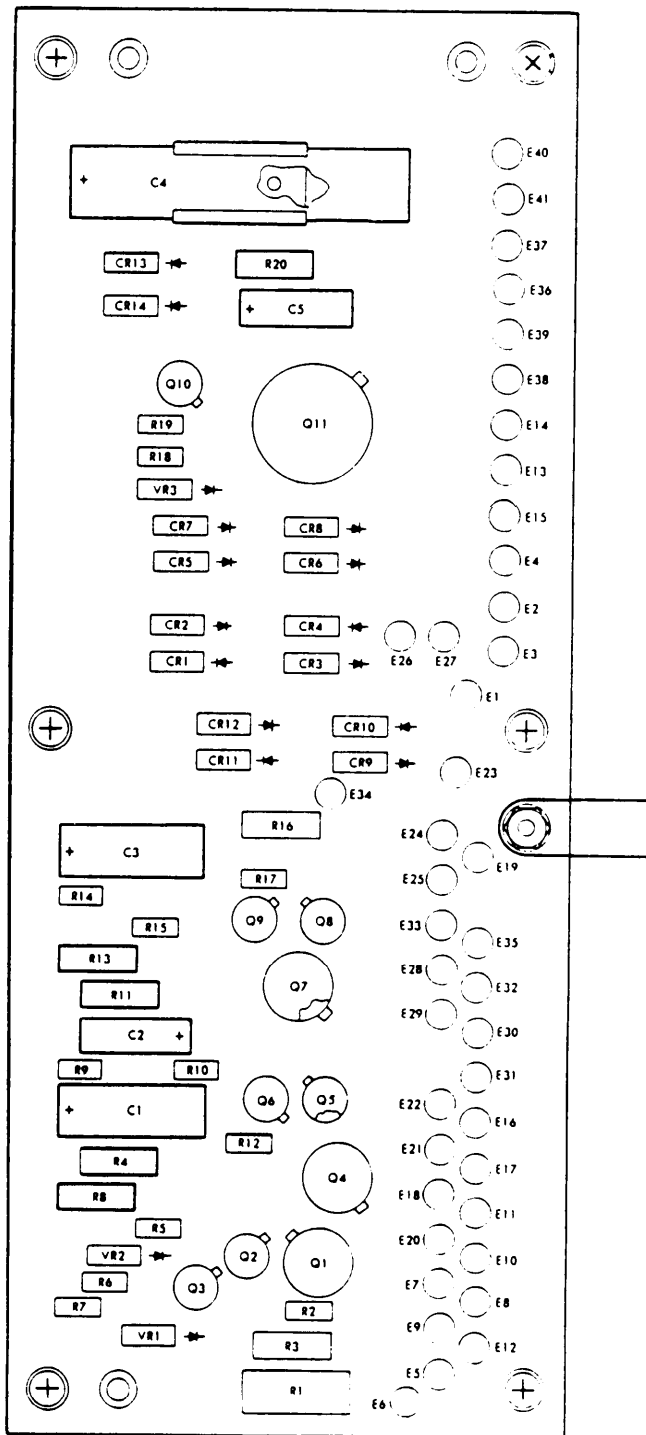
Figure 2-4. Power Supply Component Locations (Sheet 3 of 5).



E. PANEL ASSEMBLY 12A1A1

4858-005.4

Figure 2-4. Power Supply Component Locations (Sheet 4 of 5).



F. PANEL ASSEMBLY 12A1A2

4858-005.5

Figure 2-4. Power Supply Component Locations (Sheet 5 of 5).

2-8. Power Supply Component Voltage and Resistance Testing

The measurements below apply to the components shown on the power supply schematic (figure FO-2). When making checks, connect the common test lead to the GRD receptacle on the front panel. The locations of the components listed below are shown in figure 2-3. Measure voltages using Multimeter AN/GSM-64D. Measure resistances using Multimeter AN/PSM-45.

NOTE

Component variations and exact control settings may cause the measured voltages to differ slightly between equipments from the values given below:

a. DC Power Supply Circuit.

(1) Panel 12A1A2 terminal voltage measurements.

Item	Voltage	Item	Voltage
E1	+10.1	E22	+4.4
E2	0	E23	+0.5
E3	+10.1	E24	+0.5
E4	+20.2	E25	+7.1
E5	+30.2	E26	0
E6	+12.1	E27	0
E7	+12.6	E28	0
E8	+18.5	E29	+0.8
E9	+6.7	E30	+6.0
E10	+6.4	E31	+0.5
E11	+5.5	E32	0
E12	+12.1	E33	-0.6
E13	+4.5	E34	-0.6
E14	+4.5	E35	-0.6
E15	+9.0	E36	0
E16	+5.0	E37	0
E17	+5.8	E38	+30.2
E18	+8.0	E39	+26.0
E19	+5.0	E40	+6.4
E20	+5.5	E41	0
E21	+5.0		

(2) Panel 12A1A2 TRANSISTOR voltage measurements.

Item	Base	Collector	Emitter
Q1	+13.3V	+18.5V	+12.6V
Q2	+6.4V	+13.3V	+5.7V
Q3	+6.4V	+12.1V	+5.7V
Q4	+6.4V	+8.0V	+5.8V
Q5	+5.0V	+5.0V	+4.3V
Q6	+5.0V	+6.4V	+4.3V
Q7	+1.4V	+6.0V	+0.8V
Q8	0V	0V	+0.7V
Q9	0V	+1.4V	+0.7V
Q10	+26.2V	+30.2V	+25.8V
Q11	+25.8V	+30.2V	+26.0V

(3) Panel 12A1A2 breakdown diode voltage measurements.

Item	Voltage	Item	Voltage
VR1	+6.3	VR3	+26.0
VR2	+6.3		

(4) Panel 12A1A2 resistance measurements.

Item	Resistance (ohms)
L1-1 to L1-2	14.0
L1-3 to L1-4	1.5
L1-5 to L1-6	1.5
L2-1 to L2-2	0.9
T1-1 to T1-2	6.0
T1-3 to T1-4	1.0
T1-5 to T1-6	4.5
T1-7 to T1-8	1.0
T1-9 to T1-10	1.0
T1-11 to T1-12	6.7
T1-12 to T1-13	6.7

b. Cable Current Power Supply.

(1) Panel 12A1A3 transistor voltage measurements.

item	Base	Collector	Emitter
Q4	-2.7V	+30.0V	0V
Q5	-2.7V	+30.0V	0V

(2) Panel 12A1A1 terminal voltage measurements.

Item	Voltage	Item	Voltage
E1	+1.7 ²	E14	0
E2	-1.7 ²	E15	0
E3	+14.5 ¹	E16	-6.0
E4	+13.2 ¹	E17	+5.0
E5	+2.7 ²	E18	+12.0
E6	+18.4 ¹	E19	0
E7	+34.0 ¹	E20	+5.0
E8	-6.0	E21	-0.9
E9	0	E22	0
E10	-5.3	E23	+1.1
E11	-5.3	E24	+5.0
E12	0	E25	-2.7
E13	-5.3		

NOTES:

1. Dangerous voltages may be present. Voltages shown are with a short circuit connected across TO CABLE and FROM CABLE receptacles. If the cable current loading is increased, the dc voltage at E3, E4, E6, and E7 can be increased as high as 1,000 volts dc.
2. Voltages at E1, E2, and E5 vary as ZERO SET potentiometer R1 in the front panel is varied.

(3) Panel 12A1A1 resistance measurements.

Item	Resistance (ohms)
L3-1 to L3-2	135.0
L4-1 to L4-2	260.0
T2-1 to T2-2	0.5
T2-1 to T2-3	1.0
T2-4 to T2-5	120.0
T3-1 to T3-3	16.5
T3-4 to T3-6	95.0
T3-7 to T3-9	200.0
T3-10 to T3-11	155.0

2-9. Continuity Testing

WARNING

Dangerous voltages exist in the TD-754/G that may cause death or injury to personnel and damage to transistorized circuits in the equipment. Be careful not to contact ac or dc high voltage connections in the equipment. Make sure PWR switch is in OFF position, before connecting test probes. Use insulated test probes.

If the trouble with your equipment is not corrected by the procedures in the troubleshooting charts, the wiring continuity must be checked. To do this systematically, the operating principles of the TD-754/G must be thoroughly understood. Generally, the trouble symptoms can be localized to specific functions, and in turn, to specific components. Otherwise, each lead in the chassis will have to be checked, even though most connections may not apply to the trouble concerned.

As an aid to performing continuity checks, the overall TD-754/G wiring diagram is shown in figure FO-15, and the overall wiring diagram for power supply assembly 12A1 is shown in figure FO-16.

Section III. DIRECT SUPPORT MAINTENANCE PROCEDURES

Para.		Page
2-10	General	2-23
2-11	Multiplexer Test Procedures	2-23
2-12	Heat Sink Assembly 12A1A3	2-26
2-13	Filter Assembly 12A8	2-28
2-14	Filter Assembly 12A9	2-30
2-15	Wiring Harness	2-32

2-10. General

Repair of the TD-754/G at direct support level is limited to replacement of filter assemblies 12A8 and 12A9, replacement of power supply heat sink assembly 12A1A3, repair of heat sink assembly 12A1A3 by replacement of components, wiring harness repair, and system testing. No other repairs to the power supply are permitted. There are no alignment or adjustment procedures authorized at direct support level.

WARNING

Dangerous voltages exist in the TD-754/G that may cause death or injury to personnel. 115 volts ac are present in the equipment when PWR switch is operated to ON, and a dc voltage of up to 1,000 volts may be present in the equipment when CABLE CURRENT switch is operated to ON. When repairing the TD-754/G, be careful not to contact ac or dc high voltage connections in the equipment. Always operate PWR and CABLE CURRENT switches to OFF before attempting to make any repairs.

2-11. Multiplexer Test Procedures

a. *General.*

(1) The monitor circuit, one of the multiplexer's two SF circuits, provides built-in system testing capability. The monitor circuit consists of TEST ALIGN meter M1, METER SEL switch S7, SERV SEL switch S8, and components on panel 12A7. The monitor circuit monitors key circuit voltages and signal functions in the TD-754/G. The test procedures are performed with TD-754/G connected in a feedback loop test configuration with a known good TD-660()/G,

NOTE

Maintenance of panel 12A7 is not authorized at direct support.

(2) When a hairline indication cannot be obtained on TEST ALIGN meter M1 while the appropriate dc voltage is within acceptable tolerance, the dc voltage between TP1 and TP2 on panel 12A7 must be measured. If the voltage measured is not 4.00 volts dc, the TD-754/G must be returned to general support maintenance for adjustment and/or repair.

(3) If the dc voltage measured between TP1 and TP2 on panel 12A7 is 4.00 volts dc, then the appropriate wiring and components on the TD-754/G case must be checked to isolate the faulty component.

b. Test Procedures.

NOTE

The following procedures require Multimeter AN/GSM-64D.

- (1) Operate PWR and CABLE CURRENT switches to ON.
- (2) Connect common (ground) lead of voltmeter to GRD receptacle on front panel.
- (3) Operate METER SEL switch to SERV FAC.
- (4) Operate SERV SEL switch to +28 and connect test lead of voltmeter to +28V receptacle on front panel.
- (5) Observe that indication on TEST ALIGN meter is in green band and indication on voltmeter is $+25 \pm 2.5$ volts.
- (6) Operate SERV SEL switch to +12 and connect test lead of voltmeter to +12V receptacle on front panel.
- (7) If necessary, adjust +12V potentiometer for hairline indication on TEST ALIGN meter. Observe that indication on voltmeter is $+12 \pm 0.24$ volts.
- (8) Operate SERV SEL switch to +5 and connect test lead of voltmeter to +5V receptacle on front panel.
- (9) If necessary, adjust +5V potentiometer for hairline indication on TEST ALIGN meter. Observe that indication on voltmeter is $+5 \pm 0.1$ volts dc.
- (10) Operate SERV SEL switch to -6 and connect test lead of voltmeter to -6V receptacle on front panel.
- (11) If necessary, adjust -6V potentiometer for hairline indication on TEST ALIGN meter. Observe that indication on voltmeter is -6 ± 0.12 volts dc.

2-12. Heat Sink Assembly 12A1A3

This task covers: a. Removal b. Repair c. Installation

INITIAL SETUP

Tools

Electronic Equipment Tool Kit TK-105/G
Tool Equipment TE-123

Materials/Parts

Solder (Item 1, Appendix B)

a. Removal. (figure 2-5)

- (1) Loosen 14 sets of hardware and take top cover off multiplexer.
- (2) Disconnect heat sink assembly connector 12A1A3J1 (1) from power supply connector 12A1J2.
- (3) Unscrew eight screws (2) mounting heat sink assembly (3) to rear of multiplexer chassis (4) and remove heat sink assembly.

b. Repair. (figure 2-5)

NOTE

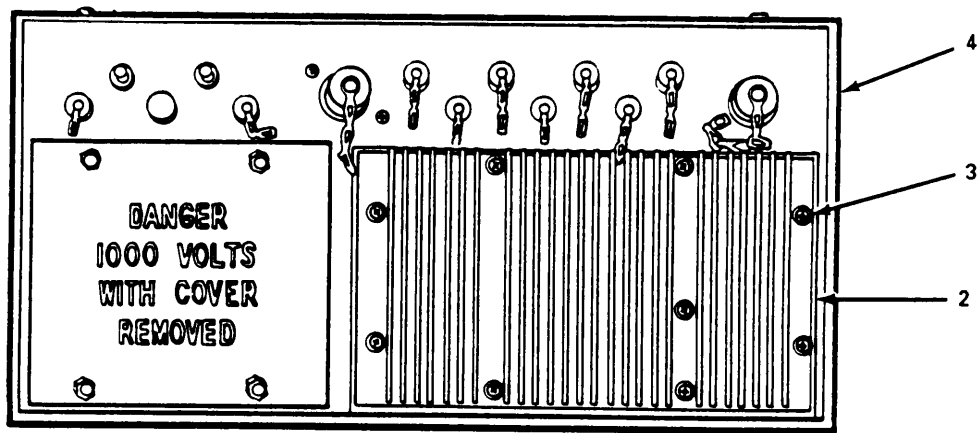
Heat sink assembly may be repaired by replacing defective transistors and diodes, and by repairing wiring harness. For wiring harness repair, refer to paragraph 2-15.

If more than one component is being replaced, make sure each lead is tagged for identification before removal.

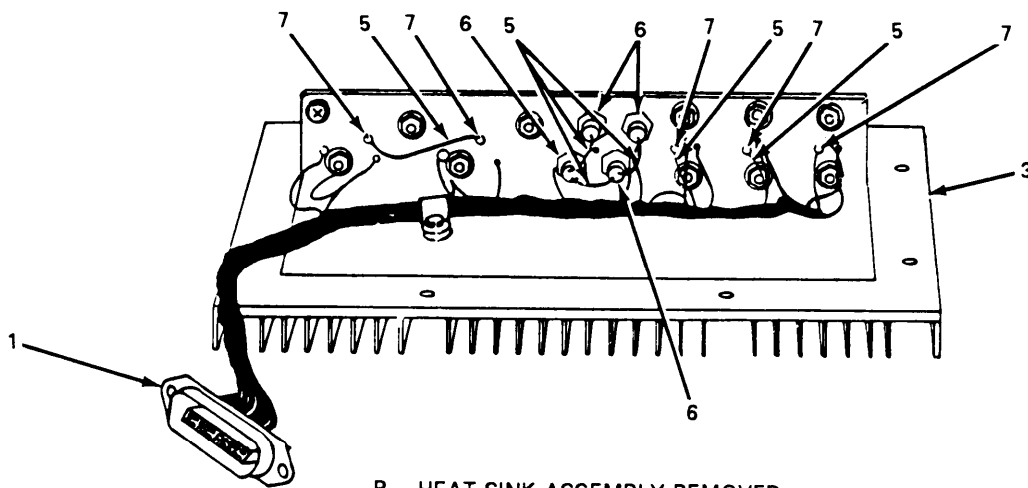
- (1) Unsolder electrical lead (5) from contact on diode (6) or transistor (7).
- (2) Remove defective diode (6) or transistor (7) from heat sink assembly (3).
- (3) Install new diode (6) or transistor (7) on heat sink assembly (3). Make sure contact end of component is on wiring side of board.
- (4) Solder electrical lead (5) onto contact of diode (6) or transistor (7). If more than one component was replaced, make sure correct lead is soldered to each component. (Refer to figure FO-2, Power Supply Assembly 12A1 Schematic Diagram.)

c. Installation. (figure 2-4)

- (1) Position heat sink assembly (3) in rear of multiplexer chassis (4) and fasten with eight screws (2).
- (2) Plug heat sink assembly connector 12A1A3J1 (1) into power supply connector 12A1J2.
- (3) Position top cover on multiplexer chassis (4) and fasten with 14 sets of hardware.



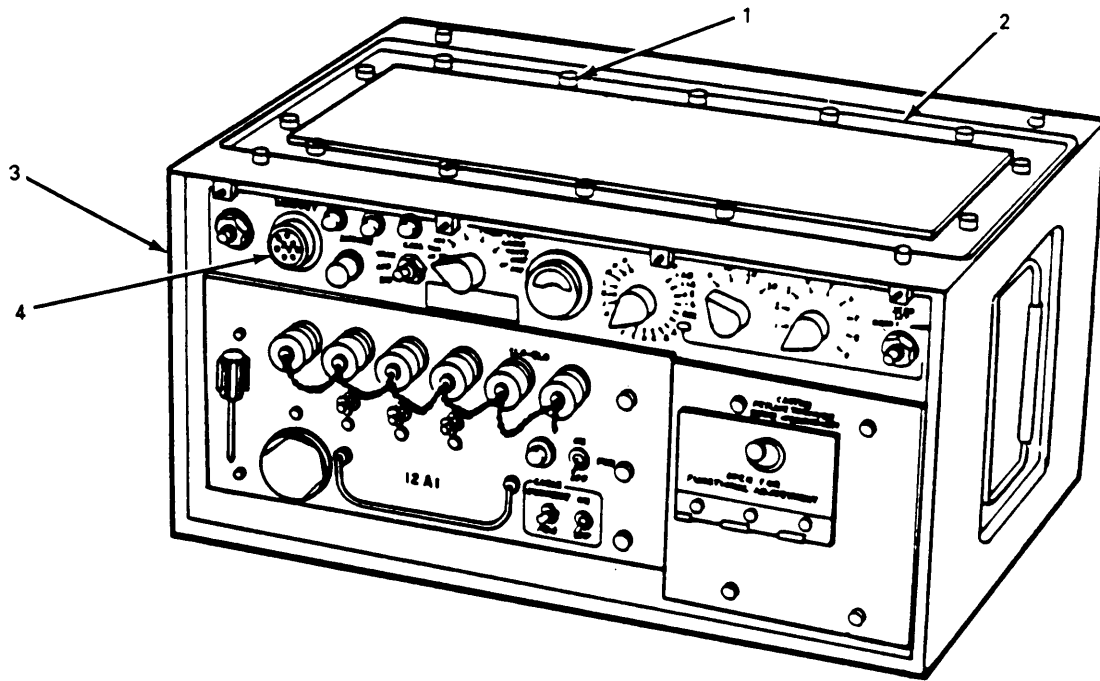
A. MULTIPLEXER REAR VIEW



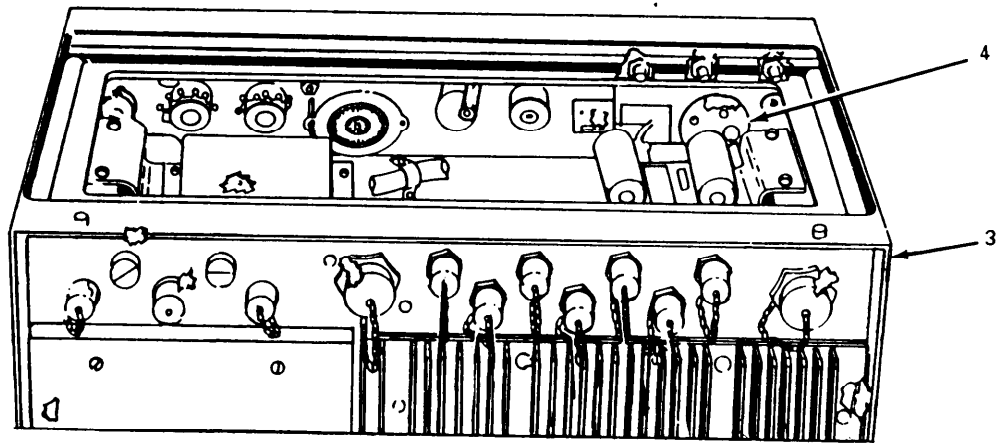
B. HEAT SINK ASSEMBLY REMOVED

4858-006

Figure 2-5. Heat Sink Assembly 12A1A3 Repair and Replacement.



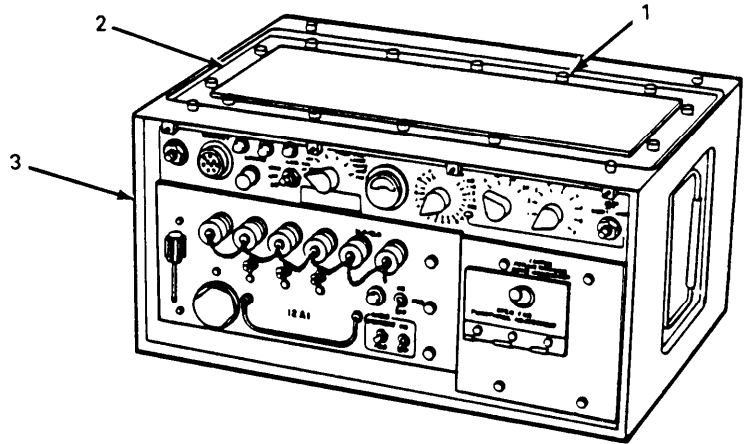
A. FRONT VIEW



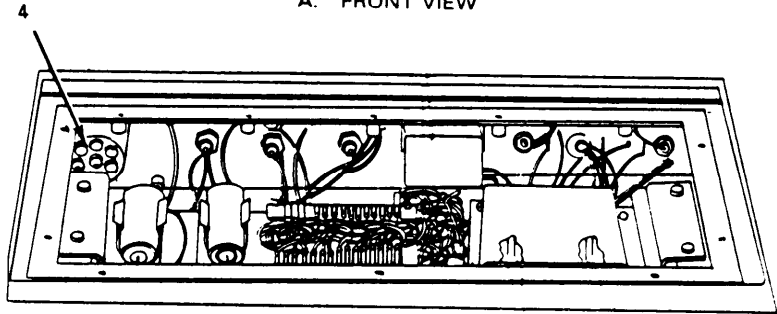
B. REAR VIEW WITH COVER REMOVED

4858-007

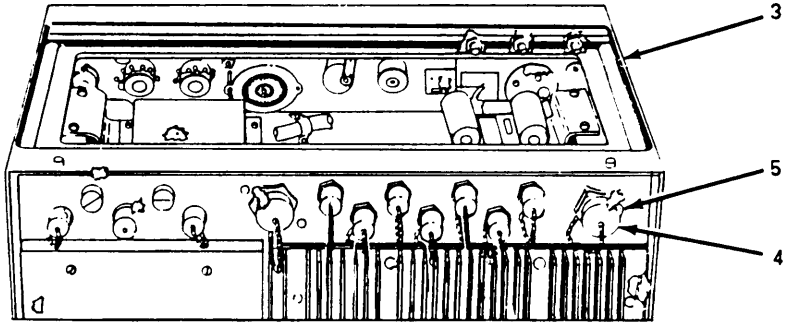
Figure 2-6. Filter Assembly 12A8 Replacement.



A. FRONT VIEW



B. TOP VIEW WITH COVER REMOVED



C. REAR VIEW WITH COVER REMOVED

Figure 2-7. Filter Assembly 12A9 Replacement.

2-15. Wiring Harness

This task covers: Repair

INITIAL SETUP

Tools

Electronic Equipment Tool Kit TK-105/G

Materials/Parts

Solder (Item 1, Appendix B)
Wire (Item 2, Appendix B)

Repair.

NOTE

A wiring harness will require repair if an individual lead is open, cut, burned, or too short to be resoldered when broken from the connection point.

When replacing an individual lead in a wiring harness, use wire of same gauge as wire being replaced.

- (1) Cut a length of wire a few inches longer than wire being replaced.
- (2) Route new wire the same way original lead is routed, and lace it to top of existing wiring harness.
- (3) If either end of old lead is still connected, unsolder it.
- (4) Trim new wire to desired length.
- (5) Strip insulation off each end of new wire and solder them to contacts from which old lead was removed.
- (6) Cut old lead short and snub ends into harness so that it cannot cause a short circuit or be mistaken for an active lead.

NOTE

Do not attempt to remove defective lead from harness. Do not unlace existing harness, since this can cause additional breaks in wiring, and pulling of wires from soldered connections.

CHAPTER 3

GENERAL SUPPORT MAINTENANCE

	Page
Section I Repair Parts, Special Tools, TMDE and Support Equipment	3-1
Section II General Support Troubleshooting	3-2
Section III General Support Maintenance Procedures	3-5

Section I. REPAIR PARTS, SPECIAL TOOLS, TMDE AND SUPPORT EQUIPMENT

Para.		Page
3-1	Common Tools	3-1
3-2	Special Tools, TMDE and Support Equipment	3-1
3-3	Repair Parts	3-1

3-1. Common Tools

A complete list of common tools and tool kits required for general support maintenance and testing of the multiplexer is given in appendix B of TM 11-5805-383-12. In addition, each maintenance paragraph in this chapter lists the specific tools and equipment required for the procedure outlined in that paragraph.

3-2. Special Tools, TMDE and Support Equipment

Refer to paragraph 2-2 for a list of equipment required when troubleshooting and testing are to be performed with the TD-754/G in a feedback loop test setup.

3-3. Repair Parts

Repair parts for general support maintenance of the multiplexer are listed and illustrated in TM 11-5805-383-20P and -34P.

Section II. GENERAL SUPPORT TROUBLESHOOTING

Para.	Page
3-4 General	3-2
3-5 Panel 12A7 Troubleshooting Procedure	3-2

3-4. General

In addition to the troubleshooting and testing performed at the unit and direct support levels, troubleshooting for malfunction of panel 12A7 is authorized at the general support level. These malfunctions are listed in table 3-1.

Troubleshooting procedures are performed while the TD-754/G is operating in the system configuration, connected in the feedback loop test setup (figure 2-2) ,or after theTD-754/G has been removed from service. Refer to paragraph 2-2 and figure 2-2 for feedback loop test setup information.

Troubles that are not corrected through plug-in panel substitution require detailed continuity checks of case-mounted parts and associated wiring. To use the test jacks and input-output pins on a plug-in panel for system troubleshooting, the panel should be placed in extender panel MX8898/U.

WARNING

Dangerous voltages exist in the TD-754/G that may cause death or injury to personnel. 115 volts ac are present in the equipment when PWR switch is operated to ON, and a dc voltage of up to 1,000 volts may be present in the equipment when CABLE CURRENT switch is operated to ON. When troubleshooting or repairing the TD-754/G, be careful not to contact ac or dc high voltage connections in the equipment. Use insulated test probes when making measurements or waveform checks. Always operate PWR and CABLE CURRENT switches to OFF before connecting test probes to the TD-754/G.

Make sure your equipment is properly grounded before turning on the power.

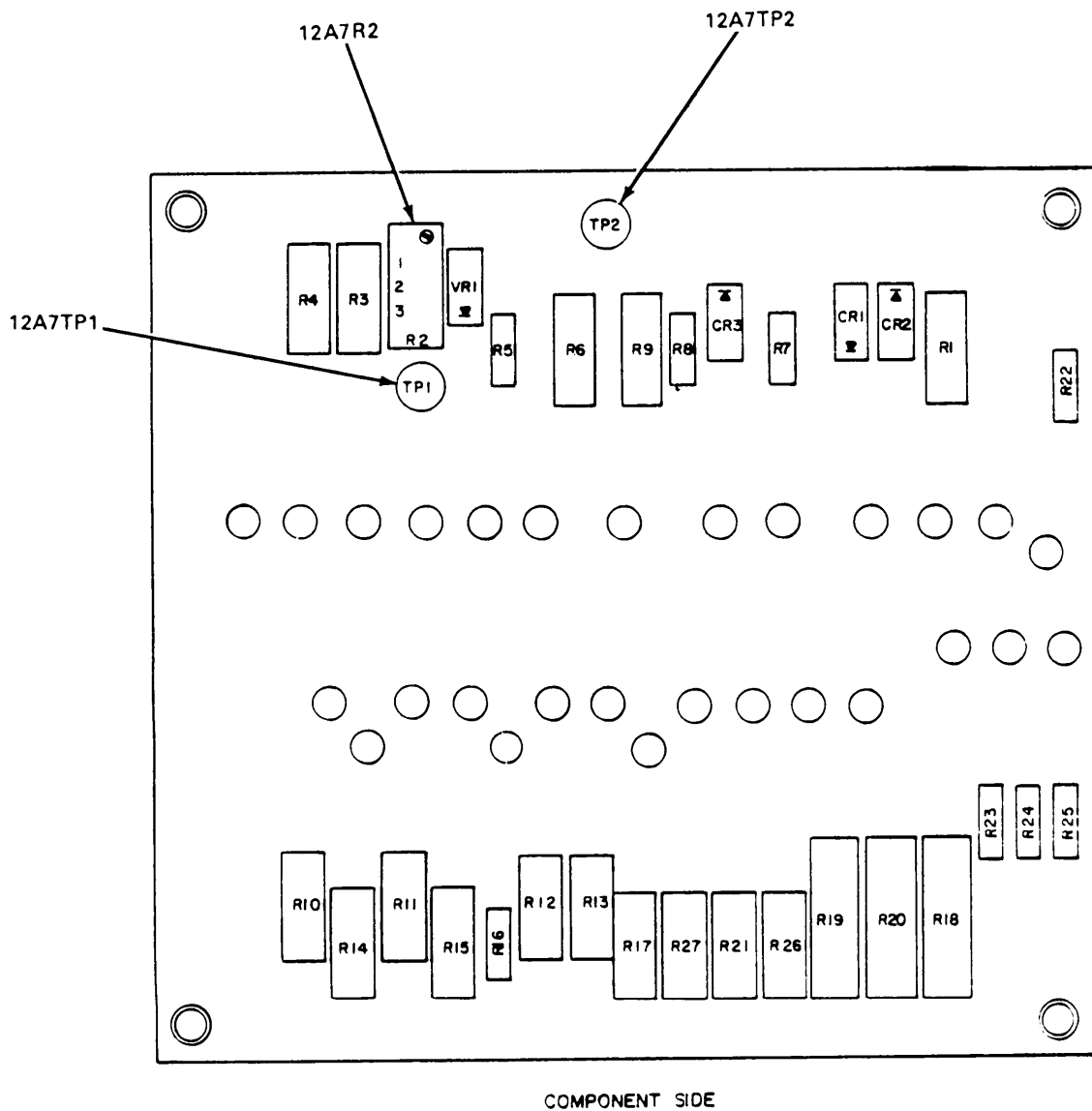
Whenever the TD-754/G is removed from its rack mounting and powered up for operation, bench testing, service or maintenance, an external ground must be applied, by connecting a jumper wire from TD-754/G ground stud (or case) to bench ground stud, before turning power on. Jumper wire must be of equal or larger gauge than power input wire.

3-5. Panel 12A7 Troubleshooting Procedure

Panel 12A7 is a component of the monitor circuit. The schematic information for panel 12A7 is found in the overall schematic diagram (figure FO-8). Panel 12A7 component locations are shown in figure 3-1.

Table 3-1. General Support Troubleshooting.

Malfunction	Test or Inspection	Corrective Action
1. MONITOR CIRCUIT IS FAULTY. (INDICATION ON TEST ALIGN METER IS OUT OF YELLOW BAND WHEN METER SEL SWITCH IS OPERATED TO SERV FAC AND SERV SEL SWITCH IS OPERATED TO REF)	Check voltage between TP1 and TP2 on panel 12A7 for 4.00 VDC.	<ul style="list-style-type: none"> a. Adjust potentiometer R2 (para. 3-10). b. If R2 cannot be adjusted, return TD-754/G to depot for repair.
2. HAIRLINE INDICATION CANNOT BE OBTAINED ON TEST ALIGN METER FOR ANY OR ALL DC VOLTAGE CHECKS WHEN TESTING MONITOR CIRCUIT.	Check voltage between TP1 and TP2 on panel 12A7 for 4.00 VDC.	<ul style="list-style-type: none"> a. Adjust potentiometer R2 (para. 3-10). b. If R2 cannot be adjusted, return TD-754/G to depot.
3. TEST ALIGN METER M1 DOES NOT FUNCTION PROPERLY.	Check for defective resistor R1 or diode CR1 or CR2.	Return TD-754/G to depot for repair.



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Figure 3-1. Panel Assembly 12A7 Component Locations.

Section III. GENERAL SUPPORT MAINTENANCE PROCEDURES

Para.		Page
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3-6. General

Maintenance of the TD-754/G at general support level consists of system alignment, alignment of plug-in panel assemblies 12A2 and 12A5, alignment of panel assembly 12A7, and repair of filter assemblies 12A8 and 12A9. Once the alignment procedures are performed on plug-in panels 12A2 and 12A5, the plug-in panels can be interchanged in different TD-754/G's. This permits one TD-754/G to be used for aligning groups of plug-in panels 12A2 and 12A5.

After all repair and alignment procedures have been performed, physical inspection and performance testing shall be done to verify operational readiness of the multiplexer. (Refer to paragraphs 3-11 and 3-12.)

WARNING

Dangerous voltages exist in the TD-754/G that may cause death or injury to personnel. 115 volts ac are present in the equipment when PWR switch is operated to ON, and a dc voltage of up to 1,000 volts maybe present in the equipment when CABLE CURRENT switch is operated to ON. When repairing the TD-754/G, be careful not to contact ac or dc high voltage connections in the equipment. Use insulated test probes when making measurements or waveform checks. Always operate PWR and CABLE CURRENT switches to OFF before connecting test probes to the TD-754/G.

Make sure your equipment is properly grounded before turning on the power.

Whenever the TD-754/G is removed from its rack mounting and powered up for operation, bench testing, service or maintenance, an external ground must be applied, by connecting a jumper wire from TD-754/G ground stud (or case) to bench ground stud, before turning power on. Jumper wire must be of equal or larger gauge than power input wire.

3-7. Multiplexer Alignment Procedures

There are three alignment procedures that may be performed by general support personnel. Alignment procedures for panel 12A7 are given in paragraph 3-10. Panel 12A7 is wired in place on the TD-754/G. Alignment procedures for plug-in panels 12A2 and 12A5 are given in paragraphs 3-8 and 3-9, respectively. Once panels 12A2 and 12A5 have been aligned, they can be switched with panels 12A2 and 12A5 in other TD-754/G's. This permits one TD-754/G to be used for aligning groups of plug-in panels.

3-8. Panel Assembly 12A2

This task covers: Alignment

INITIAL SETUP

Tools and Test Equipment

Multimeter AN/GSM-64D
Electronic Digital Readout Counter AN/USM-459
Cable Assembly CX-4559/U

Tools and Test Equipment (cont)

Extender Panel MX-8898/U
Screwdriver (mounted on TD-754/G)

Alignment. (figure 3-2)

- (1) Operate multiplexer PWR switch (1) to OFF.
- (2) Connect cable assembly CX-4559/U between POWER IN receptacle on TD-754/G and 115-volt ac power source.
- (3) Remove four flat head screws (2) and remove protective cover (3) from front panel.
- (4) Remove panel assembly 12A2 (4) from multiplexer chassis (5).
- (5) Place panel 12A2 (4) to be aligned in extender panel MX-8898/U and then install extender panel in multiplexer.
- (6) Connect test leads of digital voltmeter AN/GSM-64D between GRD receptacle (6) on front panel of power supply and test jack TP4 (7) on panel 12A2 (4).
- (7) Operate multiplexer PWR switch (1) to ON.
- (8) Operate TONE switch S1 (8) on panel 12A2 (4) to ON.
- (9) Adjust TTL potentiometer R37 (9) on panel 12A2 (4) for an indication of 150 ± 1.0 mv ac on digital voltmeter.
- (10) Operate multiplexer PWR switch (1) to OFF and disconnect digital voltmeter test leads from multiplexer.
- (11) Connect digital readout counter AN/USM-459 input to TP10 (10).
- (12) Operate multiplexer PWR switch (1) to ON.

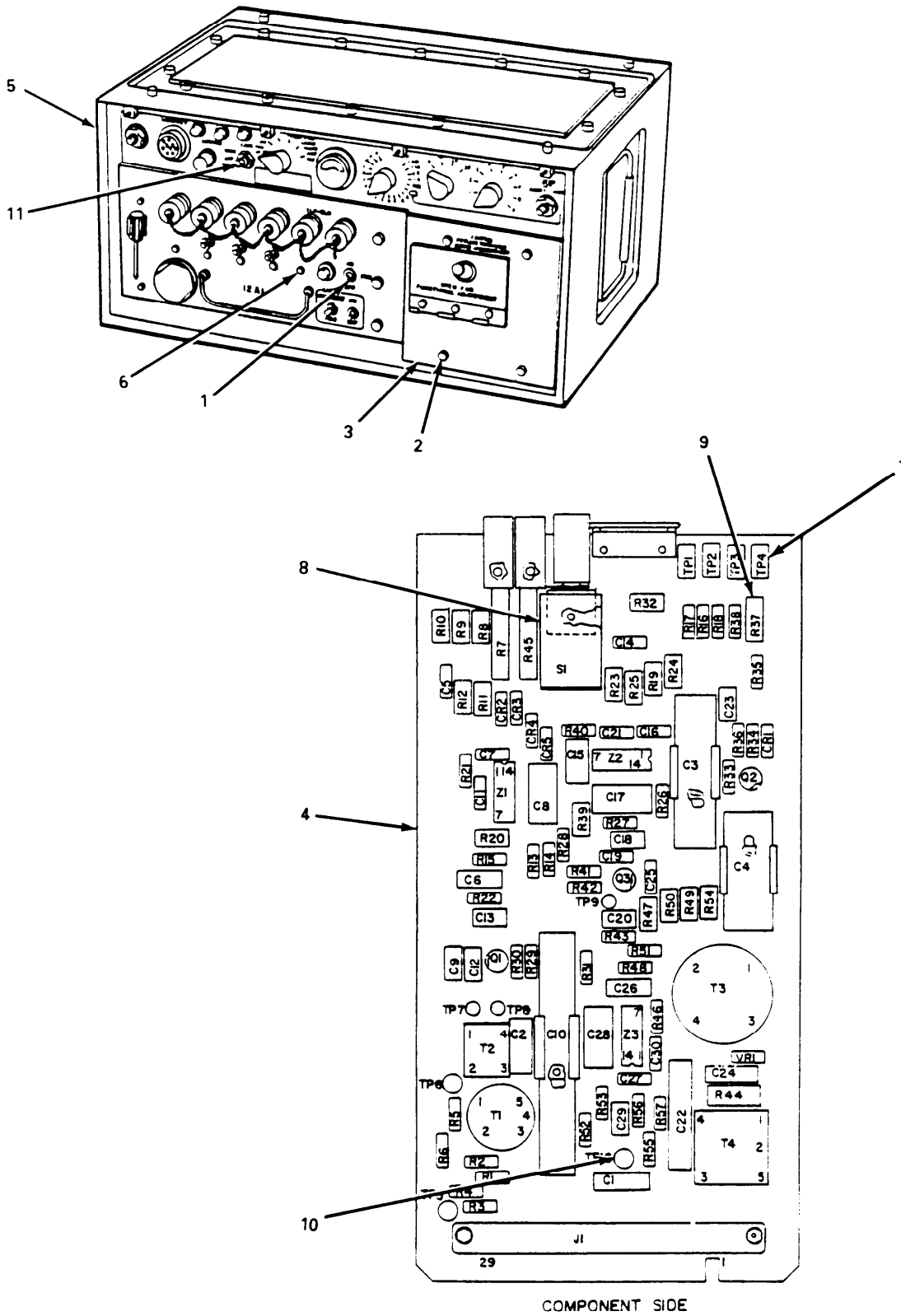


Figure 3-2. Panel Assembly 12A2 Alignment.

3-8. Panel Assembly 12A2 (cont)**NOTE**

If frequency in step (13) or (15) is out of tolerance, panel must be forwarded to a depot maintenance facility for repair.

(13) Check for a frequency reading of 1100 ± 100 Hz on digital readout counter.

(14) Operate TONE switch S1 (8) on panel 12A2 (4) to OFF.

(15) Operate TALK-OFF-SIG switch (11) on multiplexer front panel to SIG and hold in SIG position for several seconds. Check for a frequency reading of 1600 ± 32 Hz on digital readout counter.

(16) Operate multiplexer PWR switch (1) to OFF and disconnect digital readout counter test leads from multiplexer.

(17) Remove panel assembly 12A2 (4) from extender panel.

(18) Remove extender panel from multiplexer.

(19) If another panel assembly 12A2 is to be aligned, install panel to be aligned in extender panel and then install extender panel in multiplexer. Repeat steps (6) through (18).

NOTE

PRL potentiometer R7 and CRL potentiometer R45 are in-system adjustments that are performed at unit level maintenance.

3-9. Panel Assembly 12A5

This task covers: Alignment

INITIAL SETUP

Tools and Test Equipment

Oscilloscope AN/USM-488
Extender Panel MX-8898/U
Screwdriver (attached to TD-754/G)
TD-660()/G
Cable Assembly CG-1040B/U (4 required)
Cable Assembly CX-4559/U (2 required)
Cable Assembly CG-2437/U
Cable Assembly CG-2438/U

Tools and Test Equipment (cont)

Cable Assembly CX-11230/G or CX-4245/G
(2 quarter-mile spools) (optional)

Equipment Condition

TD-754/G connected in a feedback loop test setup (figure 2-2).

NOTE

As an alternative to the half-mile cable loop (CX-11230/G or CX-4245/G) shown in figure 2-2, cable assemblies CG-2437/U and CG-2438/U may be connected in a short circuit configuration between TO CABLE and FROM CABLE receptacles.

Alignment. (figures 3-3 and 3-4)

- (1) Operate TD-754/G PWR switch (1) to OFF.
- (2) Operate TD-660()/G POWER switch to OFF.
- (3) Remove four flat head screws (2) and remove protective cover (3) from front panel of TD-754/G.
- (4) Remove panel assembly 12A5 (4) from TD-754/G.
- (5) Place panel 12A5 (4) to be aligned in extender panel MX-8898/U and then install extender panel in TD-754/G.
- (6) Connect one input (A) on oscilloscope to test jack TP1 (5) on panel 12A5 (4).
- (7) Connect one input (B) on oscilloscope to test jack TP3 (6) on panel 12A5 (4).
- (8) Connect external trigger on oscilloscope to SCOPE SYNC receptacle on TD-660()/G.
- (9) If one mile of cable CX-11230/G or CX-4245/G is connected between TO CABLE and FROM CABLE receptacles, operate CABLE MILES switch S1 on panels 12A4 and 12A5 to its 1 position. If cables CG-2437/U and CG-2438/U are connected directly between TO CABLE and FROM CABLE receptacles, operate each CABLE MILES switch to its 1/2 position.

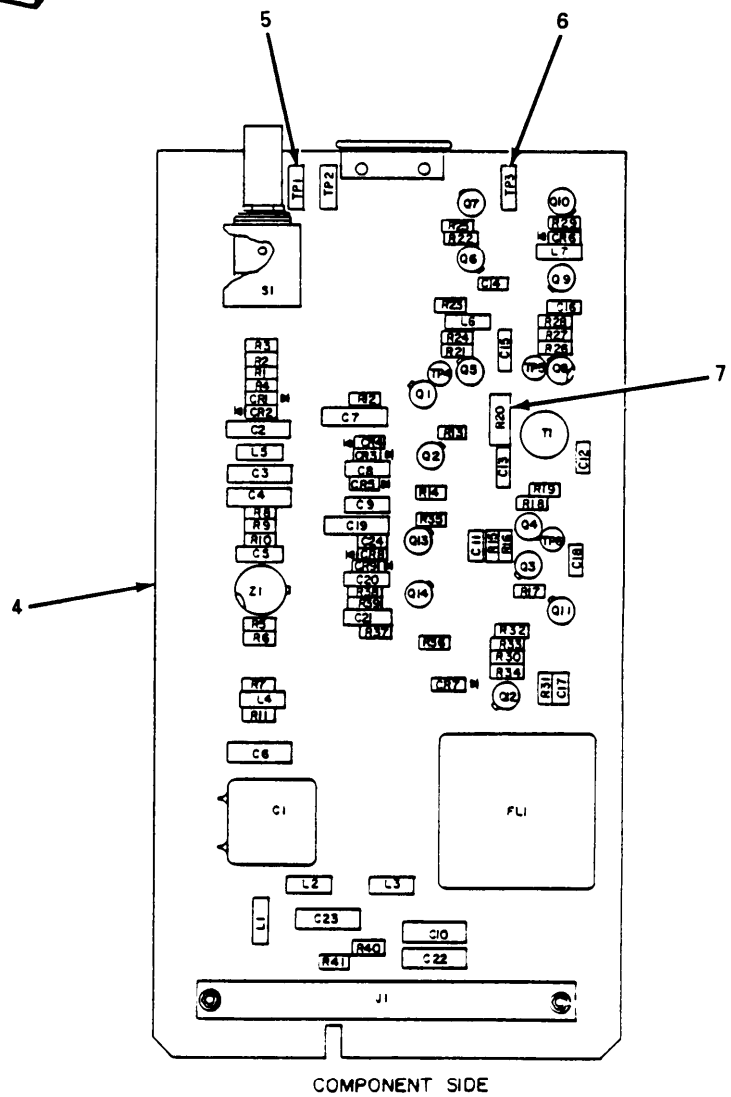
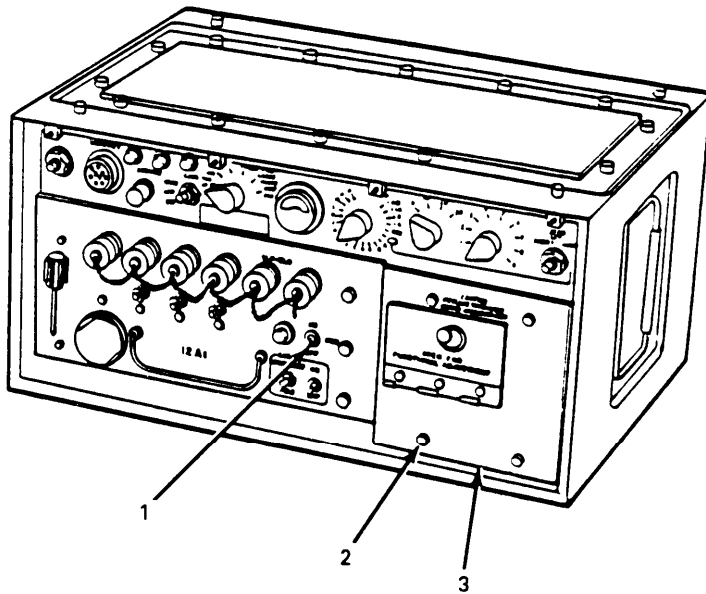


Figure 3-3. Panel Assembly 12A5 Alignment.

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3-9. Panel Assembly 12A5 (cont)

(1 O) Operate switches on TD-754/G and TD-660()/G as shown in table below.

Equipment	Switch	Position/Setting
TD-754/G	CABLE CURRENT MODE READ-ZERO SET-NORM OPR METER SEL SERV SEL	OFF 6/1 2 NORM OPR SERV FAC REF
TD-660()/G	MODE 2 WIRE -4 WIRE AUX I II III MASTER-SLAVE	12 CH 4 WIRE OUT SW III OFF MEAS MASTER

(11) Operate TD-754/G PWR switch (1) to ON.

(12) Operate TD-660()/G POWER switch to ON.

(13) Operate oscilloscope input A (TP1) controls for 0.5 usec/cm and 1.0 v/cm. Operate input B (TP3) controls for 0.5 usec/cm and 5.0 v/cm.

(14) On panel 12A5 (4) adjust potentiometer R20 (7) until trailing edge of timing pulse (input B) occurs slightly after leading edge of pcm pulse (input A), as shown in figure 3-4.

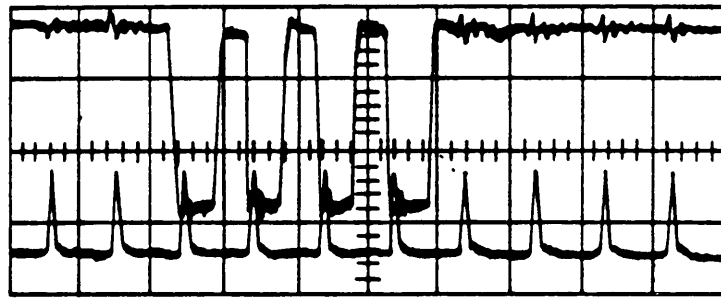
(15) Operate TD-754/G PWR switch (1) to OFF.

(16) Operate TD-660()/G POWER switch to OFF.

(17) Remove panel 12A5 (4) from extender panel.

(18) Remove extender panel from TD-754/G.

(19) If another panel assembly 12A5 is to be aligned, install panel to be aligned in extender panel and then install extender panel in TD-754/G. Repeat steps (6) through (18).



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Figure 3-4. Phase Adjustment, Waveform Diagram.

NOTE

FOLLOW-ON MAINTENANCE: Remove TD-754/G from feedback loop test setup.

3-10. Panel Assembly 12A7

This task covers: Alignment

INITIAL SETUP

Tools and Test Equipment

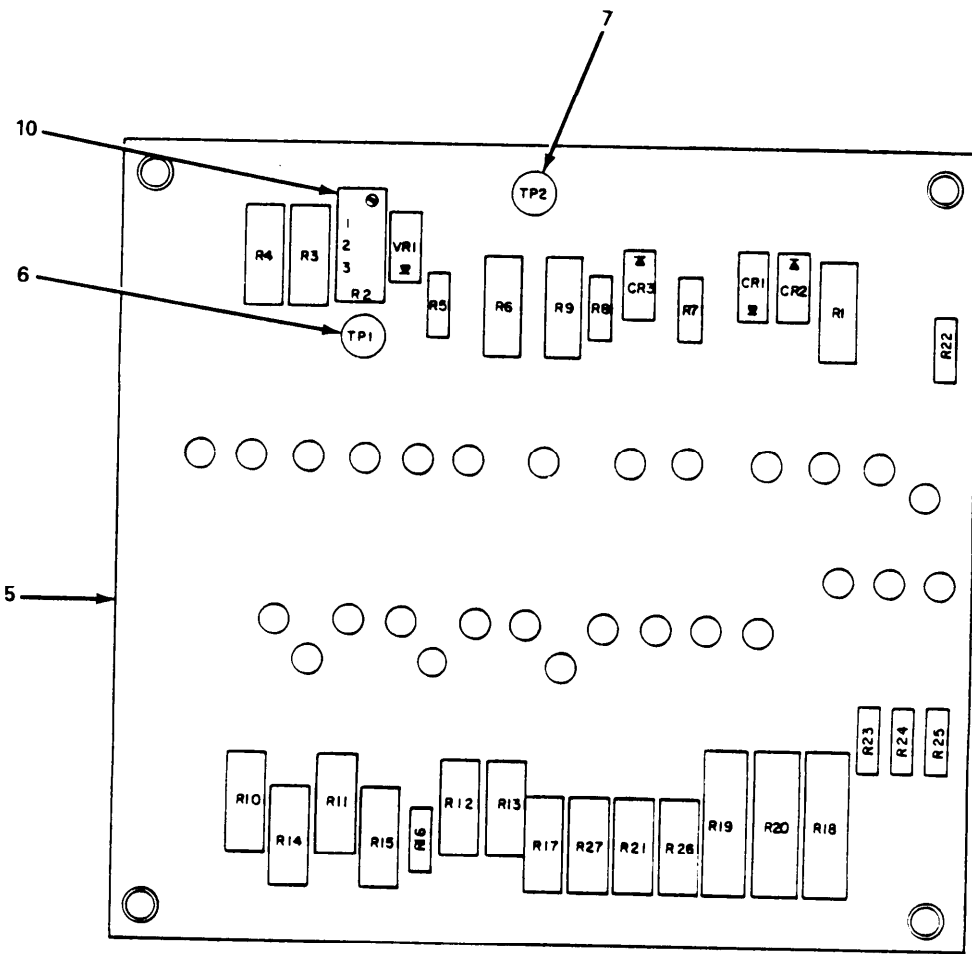
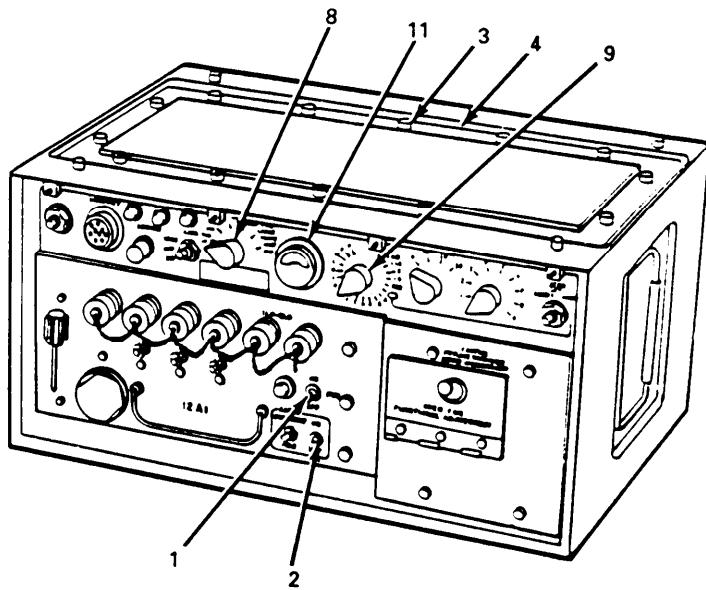
Multimeter AN/GSM-64D

Cable Assembly CX-4559/U

Screwdriver (mounted on TD-754/G)

Alignment. (figure 3-5)

- (1) Operate multiplexer PWR (1) and CABLE CURRENT (2) switches to OFF.
- (2) Remove 14 flat head screws (3) and remove top cover (4) from multiplexer.
- (3) Connect cable assembly CX-4559/U between multiplexer POWER IN receptacle and 115-volt ac power source.
- (4) Connect test leads of digital voltmeter AN/GSM-64D between test jacks TP1 (+) (6) and TP2 (common) (7) on panel 12A7 (5).
- (5) Operate METER SEL switch (8) to SERV FAC.
- (6) Operate SERV SEL switch (9) to REF.
- (7) Operate multiplexer PWR switch (1) to ON.
- (8) Adjust potentiometer R2 (10) on panel 12A7 (5) for an indication of 4.00 volts dc on digital voltmeter.
- (9) Verify that indication on TEST ALIGN meter (11) is in yellow band when digital voltmeter indicates 4.00 volts.
- (10) Operate PWR switch (1) to OFF.
- (11) Remove digital voltmeter test leads from TP1 and TP2.
- (12) Replace top cover (4) on multiplexer.



COMPONENT SIDE

Figure 3-5. Panel Assembly 12A7 Alignment.

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3-11. **Physical Inspection**

a. *Purpose.* Before the TD-754/G is returned to service, the physical checks listed below should be performed. Particular attention should be paid to items that have been repaired or replaced. The inspections listed in table 3-2, together with the performance tests listed in paragraph 3-12, are designed to verify serviceability of the TD-754/G.

b. *Test Equipment and Materials.* No special test equipment or materials are required for inspection.

c. *Setup.* The TD-754/G should not be connected to any other equipment or power source while physical inspections are being performed.

NOTE

When inspections are completed, reinstall power supply assembly and all plug-in panels.

Table 3-2. *Physical Inspections.*

Item	Action	Normal Indication
1	Inspect front panel for evidence of damage.	Front panel is complete, clean and undamaged.
2	Inspect rear panel for evidence of damage.	Rear panel is complete, clean and undamaged.
3	Remove all fuses and check each fuse for proper amperage rating.	All fuses are good and have proper amperage rating.
4	Remove power supply assembly 12A1 and plug-in panels 12A2 through 12A6. Inspect components for evidence of overheating or damage.	Capacitors and resistors show no discoloration or charring from overheating; no components are damaged.
5	Check wiring and interior of multiplexer chassis for damage.	No wires are loose or broken. Components are clean. No damage is evident.
6	Inspect all metal surfaces for condition of finish.	No bare metal is showing on any painted surface. panel lettering is legible.
7	Check covers and gaskets for damage.	Covers and gaskets are in good condition, with no rough or worn edges.
8	Inspect all connector pins on plug-in panels for excessive wear, dirt, and damage.	Connector pins are clean and have no evidence of excessive wear or damage.
9	Inspect all receptacles and plugs for dirt and damage.	Receptacles and plugs are clean and have no evidence of excessive wear or damage.

3-12. Performance Tests

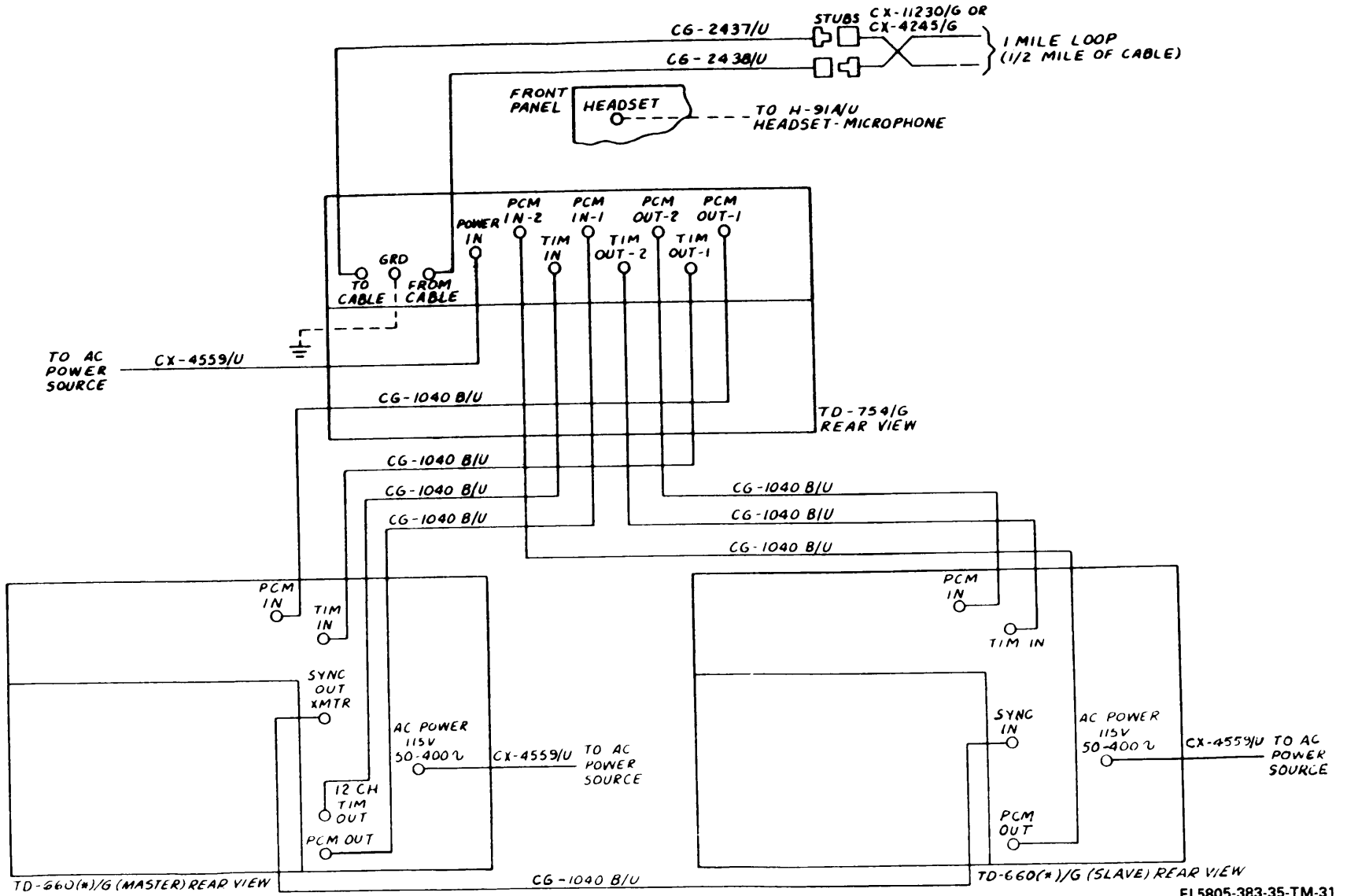
a. Purpose. The purpose of the performance tests is to verify operational readiness of the TD-754/G after repair and alignment procedures have been performed. These procedures can also be used to test a repaired power supply 12A1 or repaired or aligned plug-in panels 12A2 through 12A6 by installing the panel or power supply in a known good TD-754/G and performing normal system operation. The monitor circuit is tested to assure reliability of the multiplexer's built-in test capability. If the TD-754/G fails to meet the specified standards in any of the tests, refer to the applicable troubleshooting chart,

b. Test Equipment and Materials. The following equipment is required for performance testing.

- (1) Headset-Microphone H-91A/U
- (2) Digital Voltmeter AN/GSM-64D
- (3) Multiplexer TD-660()/G (2 required)
- (4) Fault locate circuit tester (see paragraph 3-13n.)
- (5) Cable Assembly CG-1040B/U (8 required)
- (6) Cable Assembly CG-2437/U
- (7) Cable Assembly CG-2438/U
- (8) Cable Assembly CX-4559/U (3 required)
- (9) Cable Assembly CX-11230/G or CX-4245/G (2 quarter-mile spools required)

c. Setup. The TD-754/G under test is connected to two TD-660()/G's as shown in figure 3-6. The tests are conducted by performing normal system operations while the TD-754/G is connected in this test setup. Do not operate the controls on the equipment until directed to do so in the instructions below.

Figure 3-6. TD-754/G Performance Test Setup.



d. *Initial Equipment Control Settings.* The table below gives the control settings for the TD-754/G under test and for each TD-660()/G. Do not set the controls until directed to do so in the procedures.

Equipment	Control or Switch	Position/Setting
TD-754/G (equipment under test)	PWR CABLE CURRENT MODE READ-ZERO SET-NORM OPR TALK-OFF-SIG METER SEL SERV SEL CABLE MILES switch S1 on panels 12A4 and 12A5	OFF OFF 24 NORM OPR OFF SERV FAC REF 1
TD-660()/G (master) (test equipment)	MODE 2 WIRE -4 WIRE I II III IV MASTER-SLAVE AUX POWER	12 CH 4 WIRE SW III OFF MEAS 12 CH-1 MASTER OUT OFF
TD-660()/G (slave) (test equipment)	MODE 2 WIRE -4 WIRE I II III IV MASTER-SLAVE AUX POWER	12 CH 4 WIRE SW III OFF MEAS 12 CH-1 SLAVE OUT OFF

WARNING

Dangerous voltages exist in the TD-754/G that may cause death or injury to personnel. 115 volts ac are present in the equipment when PWR switch is operated to ON, and a dc voltage of up to 1,000 volts may be present in the equipment when CABLE CURRENT switch is operated to ON. When testing the TD-754/G, be careful not to contact ac or dc high voltage connections in the equipment. Use insulated test probes when making measurements. Always operate PWR and CABLE CURRENT switches to OFF before connecting test probes to the TD-754/G.

Make sure your equipment is properly grounded before turning on the power.

e. Cable Current and Alarm Circuit Tests. (table 3-3)

Table 3-3. Cable Current and Alarm Circuit Tests.

Item	Action	Normal Indication
1	Operate controls on test equipment and equipment under test to settings as directed in equipment control settings table above, and turn both TD-660()/G POWER switches to ON.	On both TD-660()/G's, audible alarms sound and FRAME ALARM indicators light. If audible alarm does not sound, press BUZZER OFF switch to activate audible alarm.
2	Operate TD-754/G PWR switch to ON.	Audible alarms on both TD-660()/G's are silenced and FRAME ALARM indicators are off. TD-754/G power and CABLE CUR indicators light and audible alarm sounds. If TD-754/G audible alarm does not sound, press BUZZER OFF switch to activate audible alarm.
3	Operate TD-754/G CABLE CURRENT switch to ON.	Audible alarm on TD-754/G is silenced and CABLE CUR indicator is out.
4	Operate TD-754/G SERV SEL switch to RCC. Observe TEST ALIGN METER.	TEST ALIGN meter indication is in green band.
5	Operate TD-754/G METER SEL switch to CABLE CURRENT. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
6	Operate TD-754/G METER SEL switch to CABLE VOLTS. Observe TEST ALIGN meter.	TEST ALIGN meter indication is near extreme left (out of green band) of meter face.

f. TD-754/G Power Circuit Tests. (table 3-4)

Table 3-4. TD-754/G Power Circuit Tests.

Item	Action	Normal Indication
1	Operate METER SEL switch to SERV FAC and SERV SEL switch to REF. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in yellow band.
2	Operate SERV SEL switch to +28. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
3	Operate SERV SEL switch to +12. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
4	Operate SERV SEL switch to +5. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
5	Operate SERV SEL switch to -6. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.

g. Traffic Alarm and Input Monitor Circuit Tests. (table 3-5)

Table 3-5. Traffic Alarm and Input Monitor Circuit Tests.

Item	Action	Normal Indication
1	On master TD-660()/G, operate POWER switch to OFF.	On TD-754/G, audible alarm sounds and TRAFFIC indicator lights.
2	On master TD-660()/G, operate POWER switch to ON.	On TD-754/G, audible alarm is silenced and TRAFFIC indicator is off.
3	Operate TD-754/G METER SEL switch to TIM IN. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
4	Operate TD-754/G METER SEL switch to PCM IN-1. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
5	Operate TD-754/G METER SEL switch to PCM IN-2. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.

h. Order Wire Circuit Monitor Tests. (table 3-6)

NOTE

These tests monitor panel assemblies 12A2 and 12A3.

Table 3-6. Order Wire Circuit Monitor Tests.

Item	Action	Normal Indication
1	Turn R45 (CRL) control on panel assembly 12A2 to its maximum counter-clockwise position.	None
2	Operate TD-754/G TALK-OFF-SIG switch to SIG and hold for approximately two seconds.	Audible alarm sounds and CALL indicator lights while switch is held to SIG.
3	Operate TONE switch on panel 12A2 to ON.	None
4	Operate TD-754/G METER SEL switch to SERV FAC, and SERV SEL switch to M. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
5	Operate TD-754/G SERV SEL switch to N. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
6	Operate TD-754/G SERV SEL switch to 0. Adjust R45 on panel 12A2 clockwise and observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
7	Attach Headset-Microphone H-91A/U to TD-754/G HEADSET receptacle, and listen in headset for test tone.	Test tone is audible and free from spurious noise.
8	Operate TONE switch on panel 12A2 to OFF.	None
9	Operate TD-754/G TALK-OFF-SIG switch to TALK and speak into microphone.	Operator should hear himself in earphone.
10	Operate TD-754/G SERV SEL switch to M. Speak into microphone and observe TEST ALIGN meter.	Indication on meter face should fluctuate as operate speaks.
11	Operate TD-754/G SERV SEL switch to N. Speak into microphone and observe TEST ALIGN meter.	Indication on meter face should fluctuate as operator speaks.
12	Operate TD-754/G TALK-OFF-SIG switch to OFF.	None

i. TD-754/G Transmit Circuit Monitor Tests. (table 3-7)

NOTE

These tests monitor panel assembly 12A4.

Table 3-7. Transmit Circuit Monitor Tests.

Item	Action	Normal Indication
1	Operate TD-754/G SERV SEL switch to A. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
2	Operate TD-754/G SERV SEL switch to B. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
3	Operate TD-754/G SERV SEL switch to C. Observe TEST ALIGN meter.	TEST ALIGN indication is in green band.
4	Operate TD-754/G SERV SEL switch to D. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.

j. TD-754/G Cable Input Circuit Monitor Tests. (table 3-8)

NOTE

These tests monitor panel assembly 12A5.

Table 3-8. Cable Input Circuit Monitor Tests.

Item	Action	Normal Indication
1	Operate TD-754/G SERV SEL switch to E. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
2	Operate TD-754/G SERV SEL switch to F. Observe TEST ALIGN meter.	None.

k. TD-754/G Receive Circuits Monitor Tests. (table 3-9)

NOTE

These tests monitor panel assembly 12A6.

Table 3-9. Receive Circuits Monitor Tests.

Item	Action	Normal Indication
1	Operate TD-754/G SERV SEL switch to G. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
2	Operate TD-754/G SERV SEL switch to H. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
3	Operate TD-754/G SERV SEL switch to J. Observe TEST ALIGN meter.	TEST ALIGN indication is in green band.
4	Operate TD-754/G SERV SEL switch to K. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.
5	Operate TD-754/G SERV SEL switch to L. Observe TEST ALIGN meter.	TEST ALIGN meter indication is in green band.

l. Monitor Circuit Tests. (table 3-10)

NOTE

These tests verify operation of the monitor circuit, which consists of TEST ALIGN meter M1, METER SEL switch S7, SERV SEL switch S8 and components on panel 12A7.

Table 3-10. Monitor Circuit Test.

Item	Action	Normal Indication
1	Connect common (ground) lead of Digital Voltmeter AN/GSM-64D to GRD receptacle on front of TD-754/G.	None
2	Operate TD-7541G METER SEL switch to SERV FAC.	None
3	Operate TD-754/G SERV SEL switch to +28 and connect test lead of voltmeter to +28V receptacle on front panel. Observe TEST ALIGN meter and voltmeter.	TEST ALIGN meter indication is in green band and voltmeter indicates +25 ±2.5 volts.
4	Operate TD-754/G SERV SEL switch to +12 and connect test lead of voltmeter to +12V receptacle on front panel. Observe TEST ALIGN meter and voltmeter. NOTE If necessary, adjust +12V potentiometer for hairline indication on TEST ALIGN meter.	Hairline indication on TEST ALIGN meter, and voltmeter indicates +12 ±0.24 volts.
5	Operate TD-754/G SERV SEL switch to +5 and connect test lead of voltmeter to +5V receptacle on front panel. Observe TEST ALIGN meter and voltmeter. NOTE If necessary, adjust +5V potentiometer for hairline indication on TEST ALIGN meter.	Hairline indication on TEST ALIGN meter, and voltmeter indicates +5 ±0.1 volts.
6	Operate TD-754/G SERV SEL switch to -6 and connect test lead of voltmeter to -6V receptacle on front panel. Observe TEST ALIGN meter and voltmeter. NOTE If necessary, adjust -6V potentiometer for hairline indication on TEST ALIGN meter.	Hairline indication on TEST ALIGN meter and voltmeter indicates -6 ±0.12 volts.
7	Disconnect voltmeter from TD-754/G.	None

m. Patch Through Order Wire Test. (table 3-11)

Table 3-11. Patch Through Order Wire Test.

Item	Action	Normal Indication
1	a. Connect Patch Cord CX-7874/TCC from PATCH THRU connector on Test Set TD-754/G to PATCH THRU connector on TD-754/G under test. b. Connect Headset-Microphone H-91A/U to headset receptacle on each unit.	None
2	Operate METER SEL switch on both units to SERV FAC.	None
3	Operate POWER switch on both units to ON position.	None
4	SET SERV SEL switch on test set to any position except 0.	None
5	Turn TONE switch on test set 12A2 card to ON position.	None
6	Set SERV SEL switch on unit under test to 0.	None
7	Operate TONE switch on unit under test to OFF position.	None
8	Adjust patch receiver level, PRL located on 12A1 card, for green band indication on test align meter of unit under test.	Indication is in green band.
9	Operate TONE switch on test set to OFF.	None
10	Operate TALK-OFF-SIGNAL switch on both sets to TALK position.	None
11	Speak into microphone of unit under test.	A clear and undistorted voice should be heard on opposite headset.

n. *Fault Locator and Meter Zero Set Circuit Test.* (table 3-12). (See figures 3-7 and 3-8 for test setup and schematic data.)

CAUTION

Failure to follow test procedure sequence may result in damage to test fixture and/or TD-754/G.

NOTE

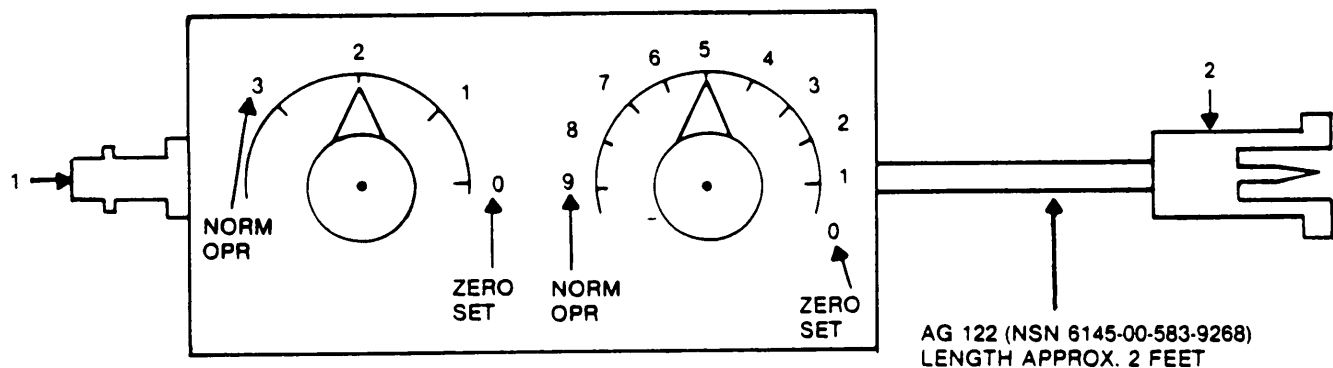
TD-660()/G test sets do not have to be on for this test.

Table 3-12. Fault Locator and Meter Zero Set Circuit Test.

Item	Action	Normal Indication
1	Disconnect cable from TO CABLE connector on TD-754/G rear panel and connect it to fault locate circuit tester (4, figure 3-7).	None
2	Connect fault locate circuit tester cable (2, figure 3-7) to TO CABLE connector on TD-754/G.	None
3	Operate TD-754/G PWR and CABLE CURRENT switches to OFF.	None
4	Operate TD-754/G NORM OPR-ZERO SET-READ switch to NORM OPR.	None
5	Operate TD-754/G SERV SEL switch to FL.	None
6	Operate all test fixture switches to NORM OPR.	None
7	Operate TD-754/G PWR and CABLE CURRENT switches to ON.	None
8	Operate TD-754/G NORM OPR-ZERO SET-READ switch to ZERO SET.	None
9	Operate TD-754/G FAULT LOCATE MILES switches to 0.	None
10	Operate test fixture switches to ZERO SET.	None
11	Adjust ZERO SET potentiometer on TD-754/G to give a center line indication on the TEST ALIGN meter.	TEST ALIGN meter gives center line indication.

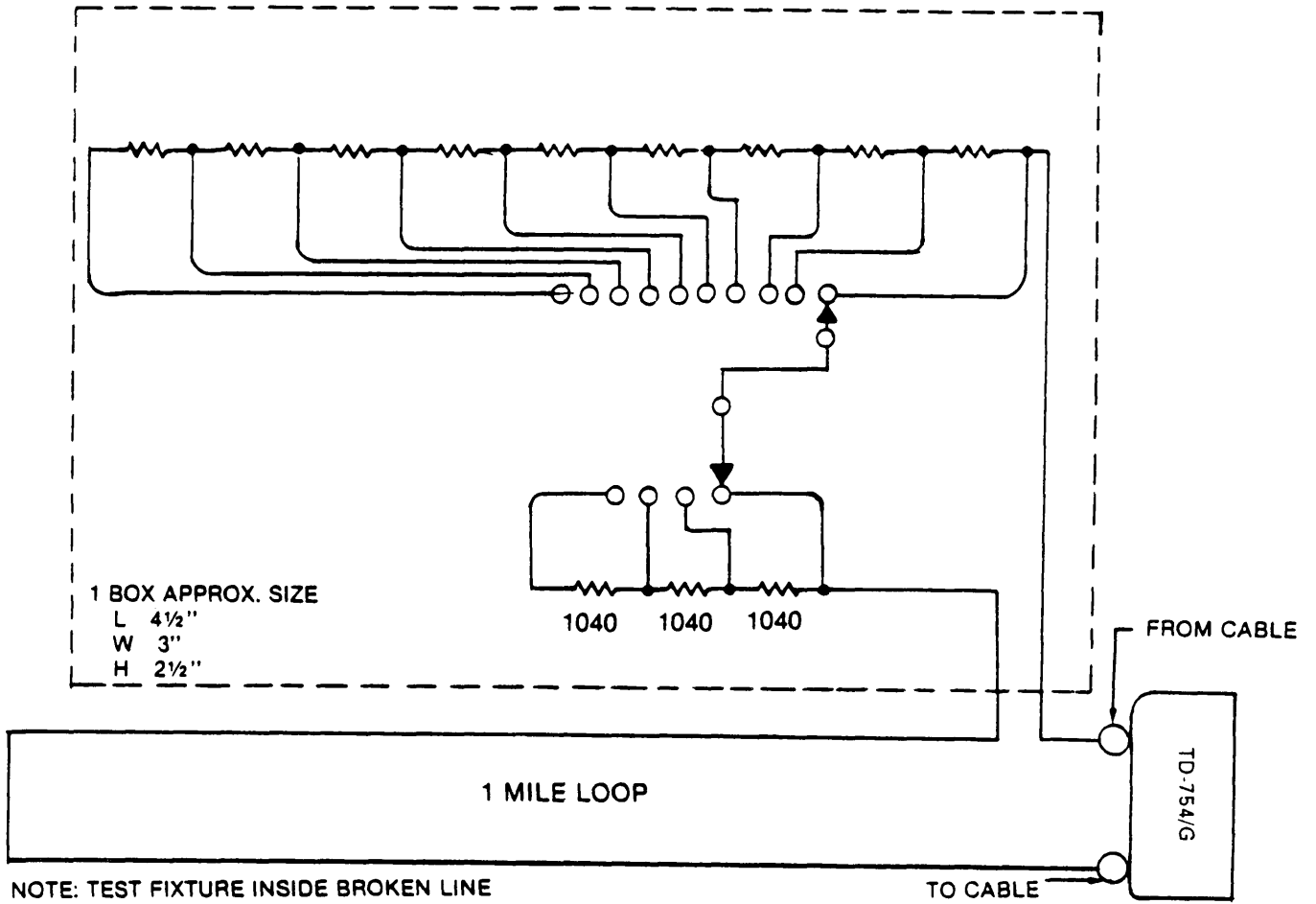
Table 3-12. Fault Locator and Meter Zero Set Circuit Test (cont).

Item	Action	Normal Indication
12	Operate TD-754/G NORM OPR-ZERO SET-READ switch to READ.	None
13	Operate test fixture to any number from 1 to 39. This simulates a bad pulse restorer. Operate FAULT LOC MILES switches on TD-754/G until TEST ALIGN meter gives a center line indication.	Number of miles indicated on FAULT LOC MILES switches are the same as number set on test fixture.
14	Operate TD-754/G PWR and CABLE CURRENT switches to OFF.	None
15	Operate test fixture switches to NORM OPR.	None
16	Operate TD-754/G FAULT LOC MILES switches TO 0.	None
17	Operate TD-754/G NORM OPR-ZERO SET-READ switch to NORM OPR.	None.



4858-014

Figure 3-7. Fault Locate Circuit Tester.



4858-015

Figure 3-8. Fault Locate Circuit Tester Schematic.

APPENDIX A

REFERENCES

A-1 . **Scope**

This appendix lists all forms, military specifications, technical manuals and miscellaneous publications referenced in this manual.

A-2. **Forms and Records**

Recommended Changes to Publications and Blank Forms	DA Form 2028
Recommended Changes to Equipment Technical Manuals	DA Form 2028-2
Transportation Discrepancy Report (TDR)	SF 361
Report of Discrepancy (ROD)	SF 364
Product Quality Deficiency Report	SF 368
Consolidated Index of Army Publications and Blank Forms	DA Pam 25-30
The Army Maintenance Management System (TAMMS)	DA Pam 738-750

A-3. **Technical Manuals and Bulletins**

Depot Maintenance Work Requirement for Multiplexer TD-754/G (NSN 5820-00-930-8078)	DMWR 11-5805-383
Field Instructions for Painting and Preserving Communications-Electronic Equipment	TB 43-0118
Operator and Organizational Maintenance Manual, Including Repair Parts and Special Tools Lists: Multiplexer TD-660/G and TD-660A/G	TM 11-5805-382-12
Operator's and Organizational Maintenance Manual, Including Repair Parts and Special Tools List: Multiplexer TD-754/G	TM 11-5805-383-12
Organizational Maintenance Repair Parts and Special Tools Lists for Multiplexer TD-754/G (NSN 5820-00-930-8078)	TM 11-5805-383-20P
Direct Support and General Support Maintenance Repair Parts and Special Tools Lists (Including Depot Maintenance Repair Parts and Special Tools) for Multiplexer TD-754/G (NSN 5820-00-930-8078)	TM 11-5805-383-34P

TM 11-5805-383-34

Operator, Organizational, Field and Depot maintenance Repair Parts and
Special Tool Lists: Headset-Microphone H-91/U, H-91A/U; Handset-Headset
H-144/U, H-144A/U, H-144B/U, H-144C/U, and Headset-Microphone H-210/G TM 11-5965-206-15P

Organizational Maintenance Manual: Multimeters ME-26A/U, ME-26B/U,
ME-26C/U, and ME-26D/U TM 11-6625-200-15

Operator, Organizational, Field and Depot Maintenance Manual: Digital
Voltmeters AN/GSM-64 and V-34A.... . TM 11-6625-444-15

Operator's Manual: Digital Readout, Electronic Counter AN/USM-207 TM 11-6625-700-10

Procedures for Destruction of Electronics Materiel to Prevent Enemy Use
(Electronics Command) TM 750-244-2

APPENDIX B

EXPENDABLE/DURABLE SUPPLIES AND MATERIALS LIST

Section 1. INTRODUCTIONS

B-1 . Scope

This appendix lists expendable supplies and materials you will need to operate and maintain the multiplexer. These items are authorized to you by CTA 50-970, Expendable Items (Except Medical, Class V, Repair Part, and Heraldic Items).

B-2. Explanation of Columns.

a. Column (1) – Item Number. This number is assigned to the entry in the listing.

b. Column (2) – Level. This column identifies the lowest level of maintenance that requires the listed item.

- F – Direct Support
- H – General Support

c. Column (3) – National Stock Number. This is the National stock number assigned to the item; use it to request or requisition the item.

d. Column (4) – Description. Indicates the Federal item name, and, if required, a description to identify the item. The last line for each item indicates the Federal Supply Code for Manufacturer (FSCM) in parentheses followed by the part number.

e. Column (5) – Unit of Measure (U/M). Indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea, in, pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy your requirements.

Section II. EXPENDABLE/DURABLE SUPPLIES AND MATERIALS

(1) Item Number	(2) Level	(3) National Stock Number	(4) Description	(5) U/M
1	F	3439-00-922-4555	Solder SN60WRMAP3	
2	F		Wire, 16-Gauge Stranded Copper	

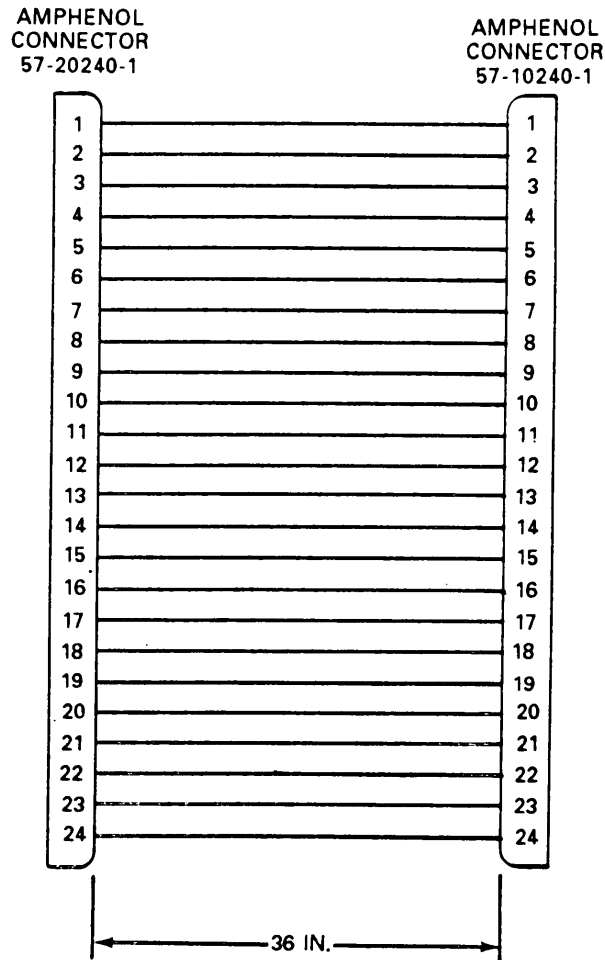
APPENDIX C

ILLUSTRATED LIST OF MANUFACTURED ITEMS

C-1. Introduction.

This appendix includes complete instructions for making items authorized to be manufactured or fabricated at direct support or general support maintenance.

All bulk materials needed for manufacturer of an item are listed by part number or specification number in a tabular list on the illustration.



NOTES:

1. JOIN CONNECTORS USING 16-GAUGE STRANDED COPPER WIRE.
2. AFTER EACH CABLE IS WIRED, TIE WIRES INTO A HARNESS AND WRAP WIRES WITH INSULATION MATERIAL TO PREVENT POSSIBLE SHOCK HAZARD.

4858-013

Figure C-1. Extension Test Cable Fabrication Wiring Diagram

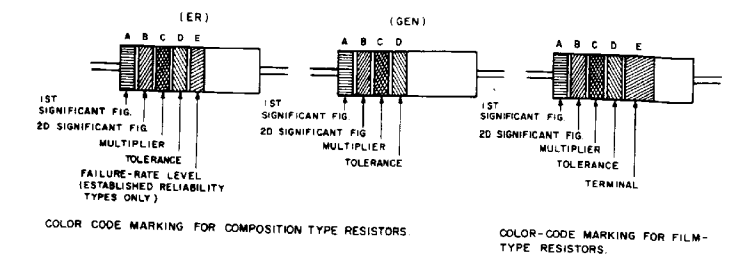


TABLE 1
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E	
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL
BLACK	0	BLACK	0	BLACK	1			BROWN	M=10
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1
RED	2	RED	2	RED	100			ORANGE	R=0.01
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE	
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5		SOLD-ERABLE
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)		
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7						
GRAY	8	GRAY	8	SILVER	101				
WHITE	9	WHITE	9	GOLD	0.1				

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

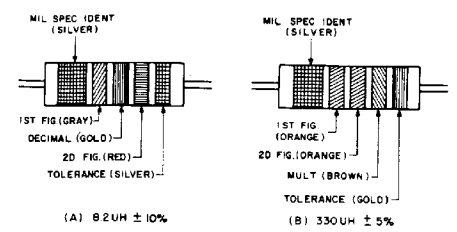
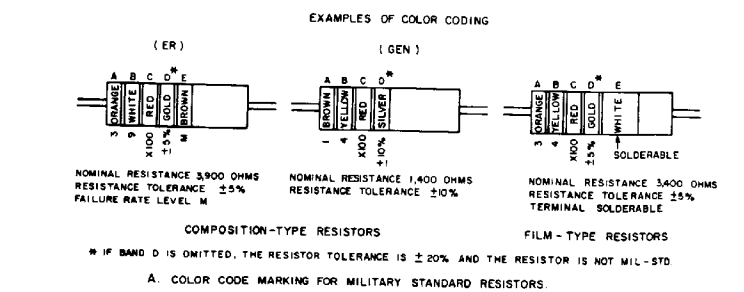
BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS) ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS



COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF THE CODING FOR AN 82UH CHOKER IS GIVEN AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD			5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

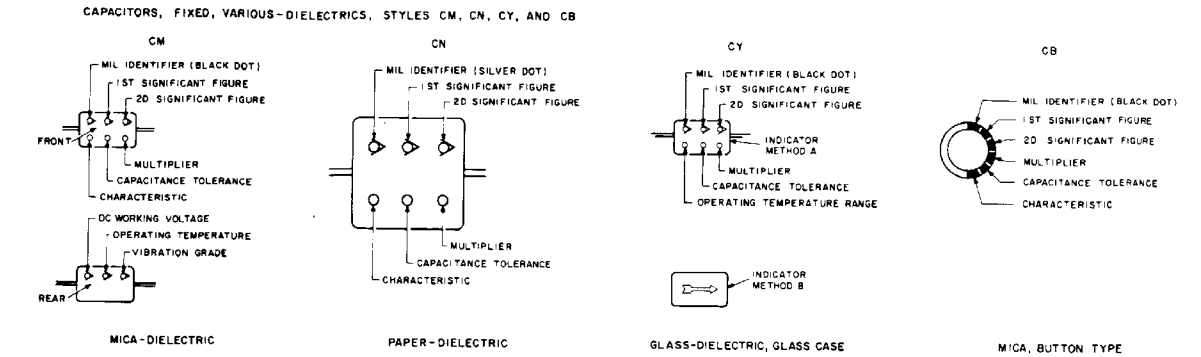


TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB

COLOR	MIL ID	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE				CHARACTERISTIC	DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB				
BLACK	CM, CY, CB	0	0	1			±20%	±20%			-55° to +70°C	10-93+2
BROWN		1	1	10					B	E	B	
RED		2	2	100	±2%		±2%	±2%	C			-55° to +85°C
ORANGE		3	3	1,000	±30%		±30%		D	O	300	
YELLOW		4	4	10,000					E			-55° to +25°C
GREEN		5	5		±5%				F		300	10-2,000H
BLUE		6	6									-55° to +50°C
PURPLE (VIOLET)		7	7									
GRAY		8	8									
WHITE		9	9									
GOLD				0.1			±5%	±5%				
SILVER	CN				±10%	±10%	±10%	±10%				

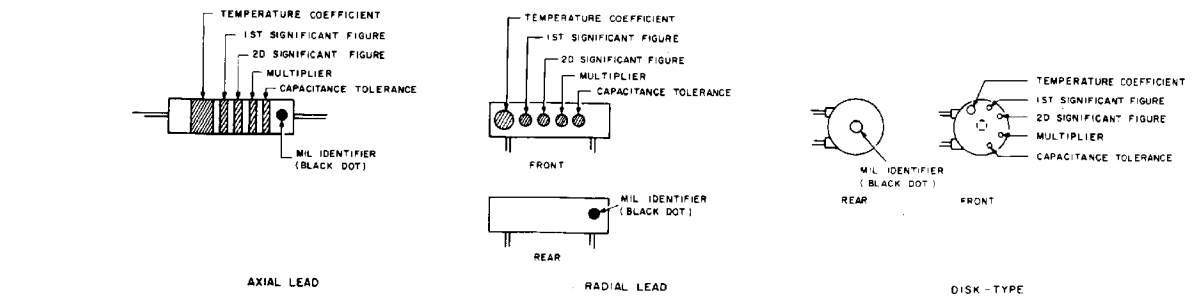


TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC

COLOR	TEMPERATURE COEFFICIENT*	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±20 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01			
WHITE		9	9	0.1	±10%		
GOLD	+100					±10 UUF	
SILVER							

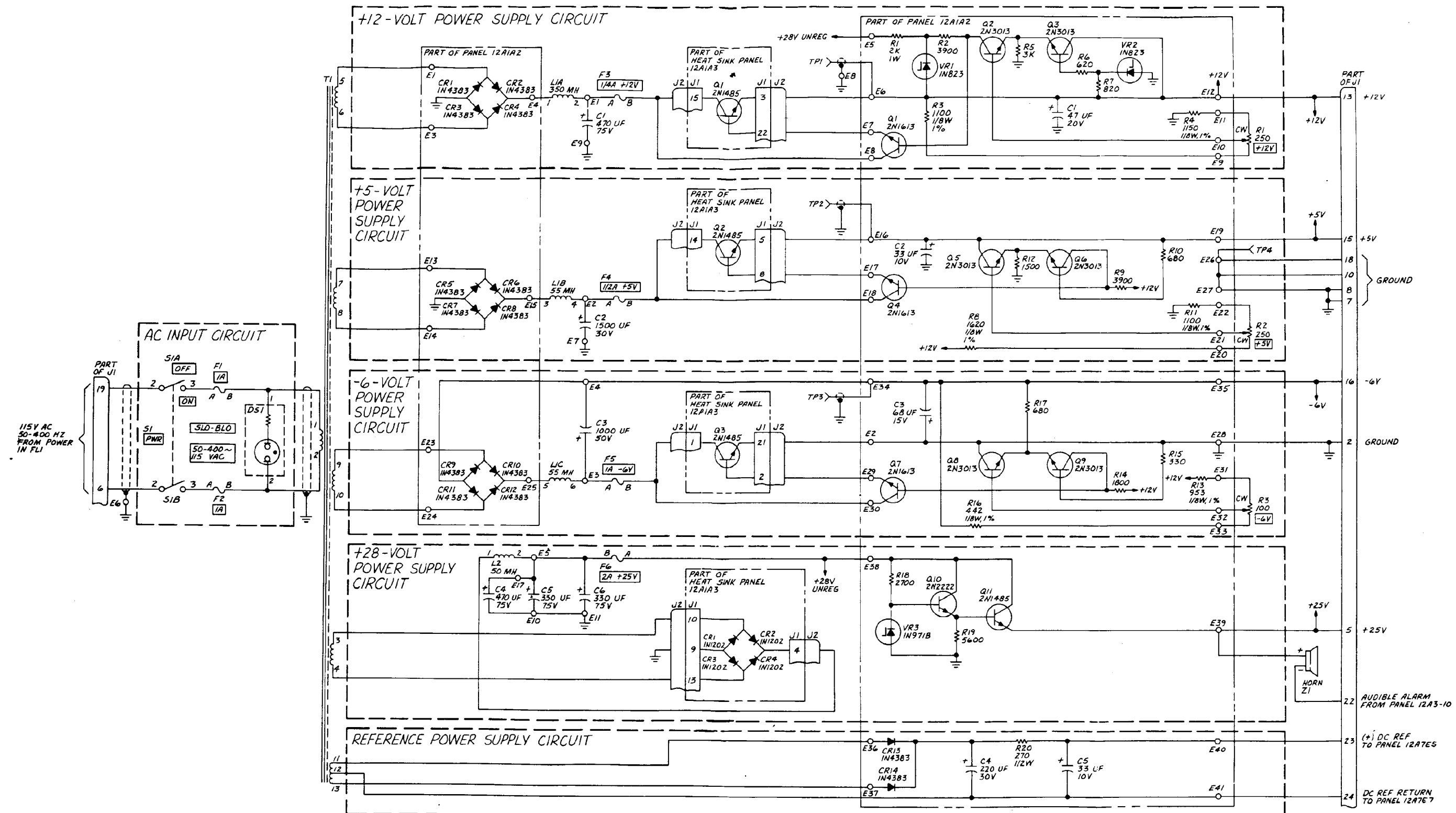
1 THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF

2 LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY

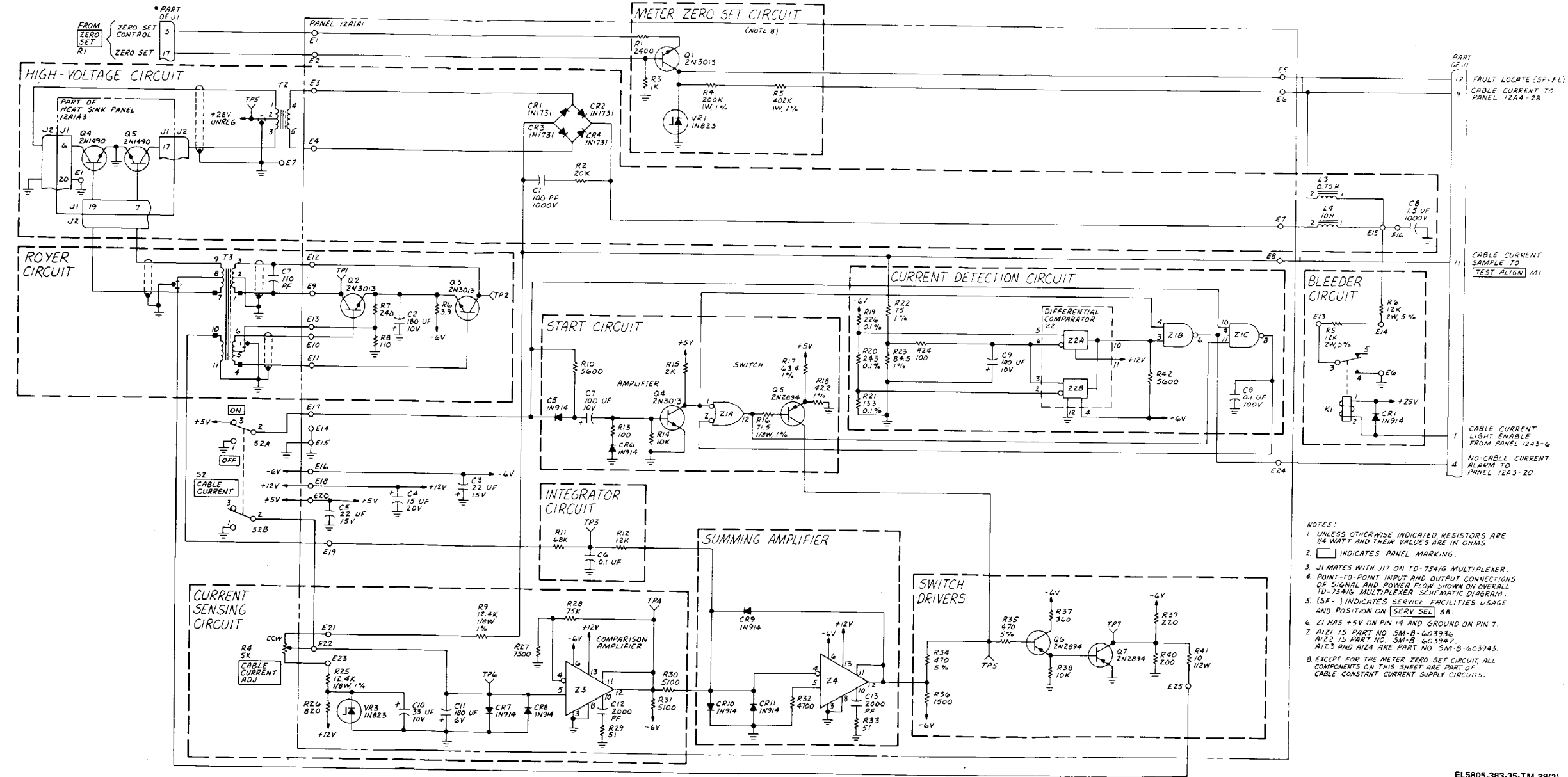
3 LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D

4 TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS



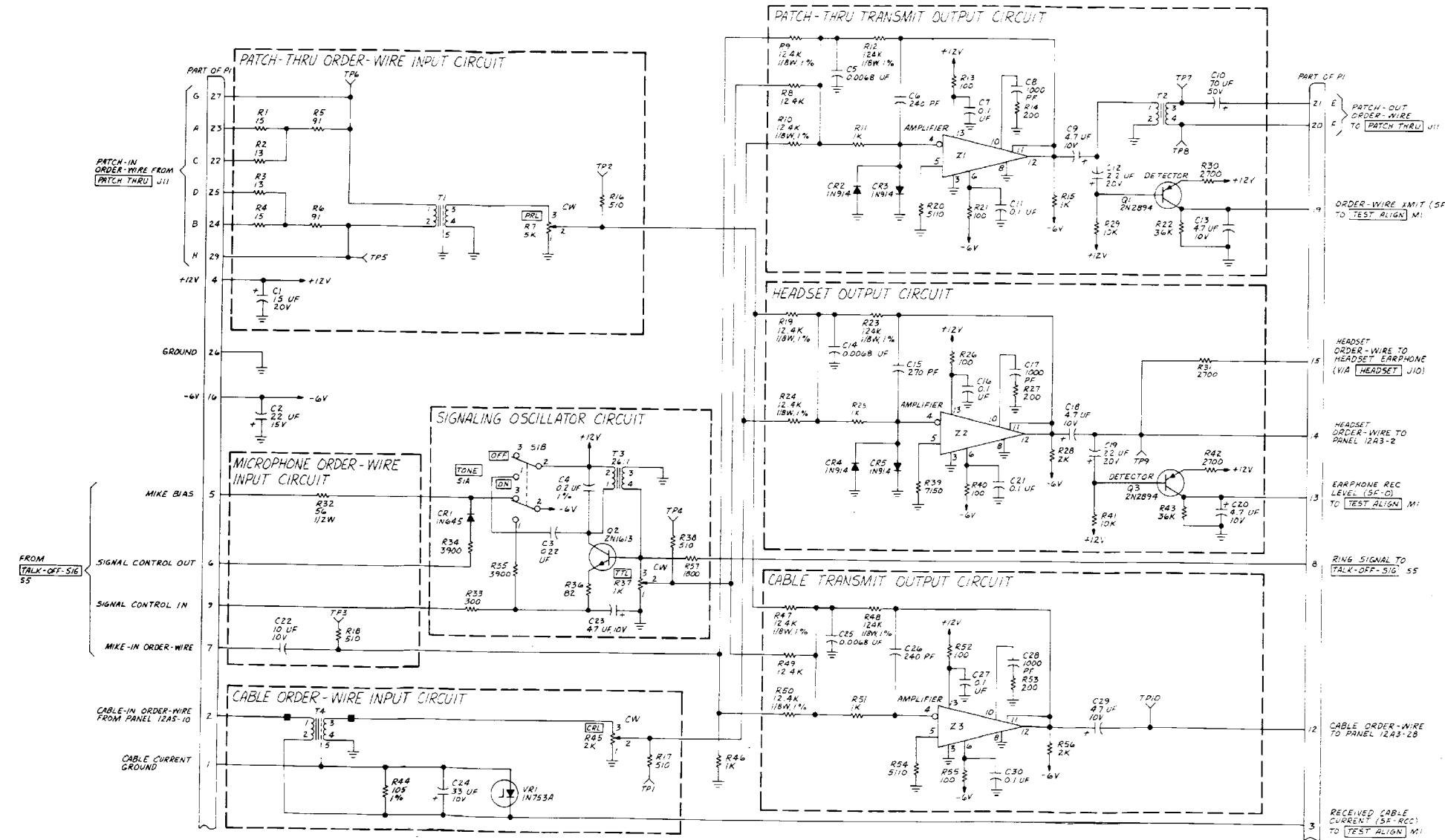
FO-2. Power Supply Assembly 12A1, Schematic Diagram (Sheet 1 of 2).



- NOTES:
- 1 UNLESS OTHERWISE INDICATED RESISTORS ARE 1/4 WATT AND THEIR VALUES ARE IN OHMS
 - 2 [] INDICATES PANEL MARKING.
 - 3 J1 MATES WITH J17 ON TD-75416 MULTIPLEXER.
 - 4 POINT-TO-POINT INPUT AND OUTPUT CONNECTIONS OF SIGNAL AND POWER FLOW SHOWN ON OVERALL TD-75416 MULTIPLEXER SCHEMATIC DIAGRAM.
 - 5 (SF-) INDICATES SERVICE FACILITIES USAGE AND POSITION ON [SERV SEL] 5B.
 - 6 Z1 HAS +5V ON PIN 14 AND GROUND ON PIN 7.
 - 7 A1Z1 IS PART NO. 5M-B-603936. A1Z2 IS PART NO. 5M-B-603942. A1Z3 AND A1Z4 ARE PART NO. 5M-B-603943.
 - 8 EXCEPT FOR THE METER ZERO SET CIRCUIT, ALL COMPONENTS ON THIS SHEET ARE PART OF CABLE CONSTANT CURRENT SUPPLY CIRCUITS.

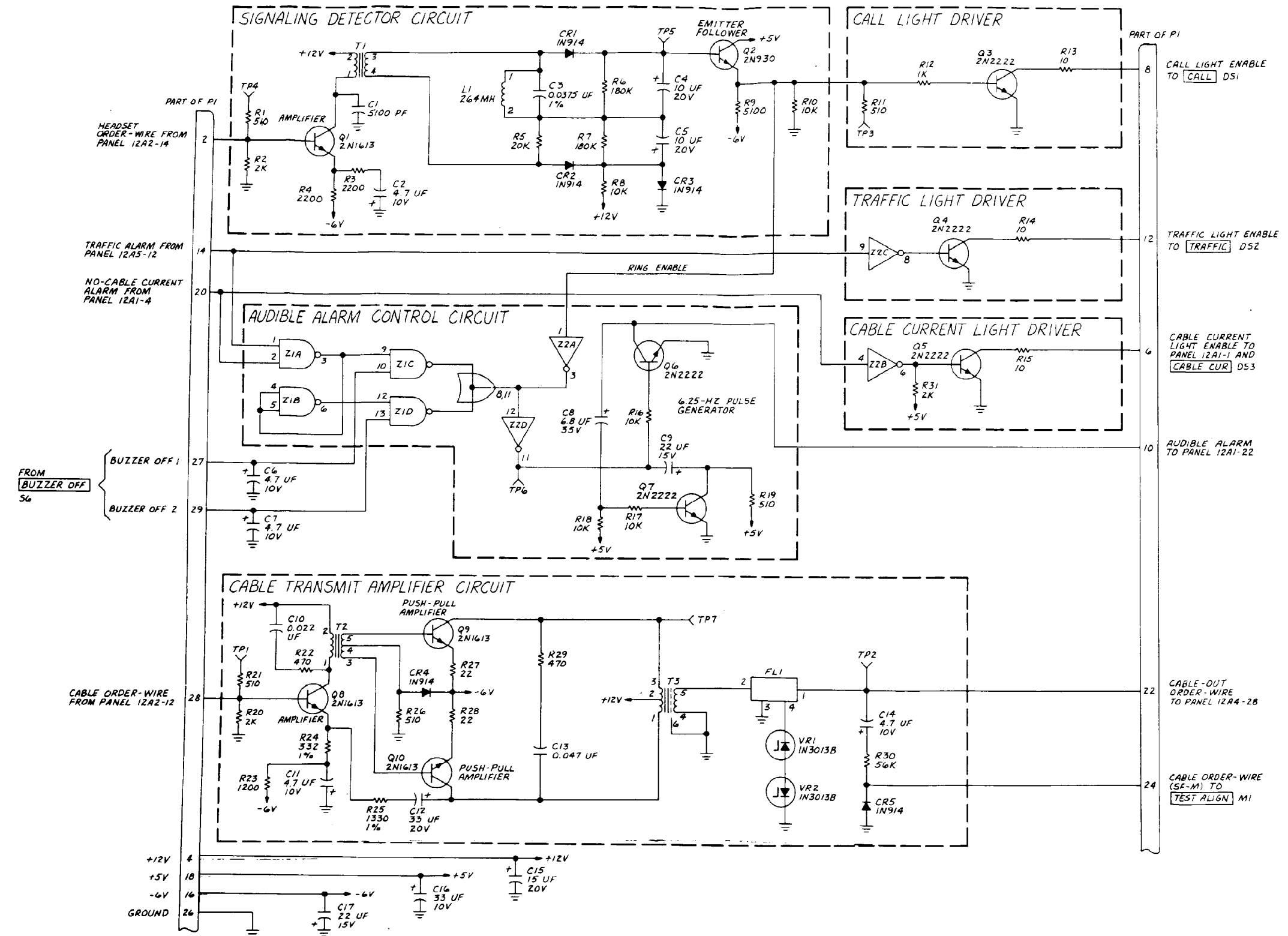
FO-2. Power Supply Assembly 12A1, Schematic Diagram (Sheet 2 of 2).

EL5805-383-35-TM-38(2)

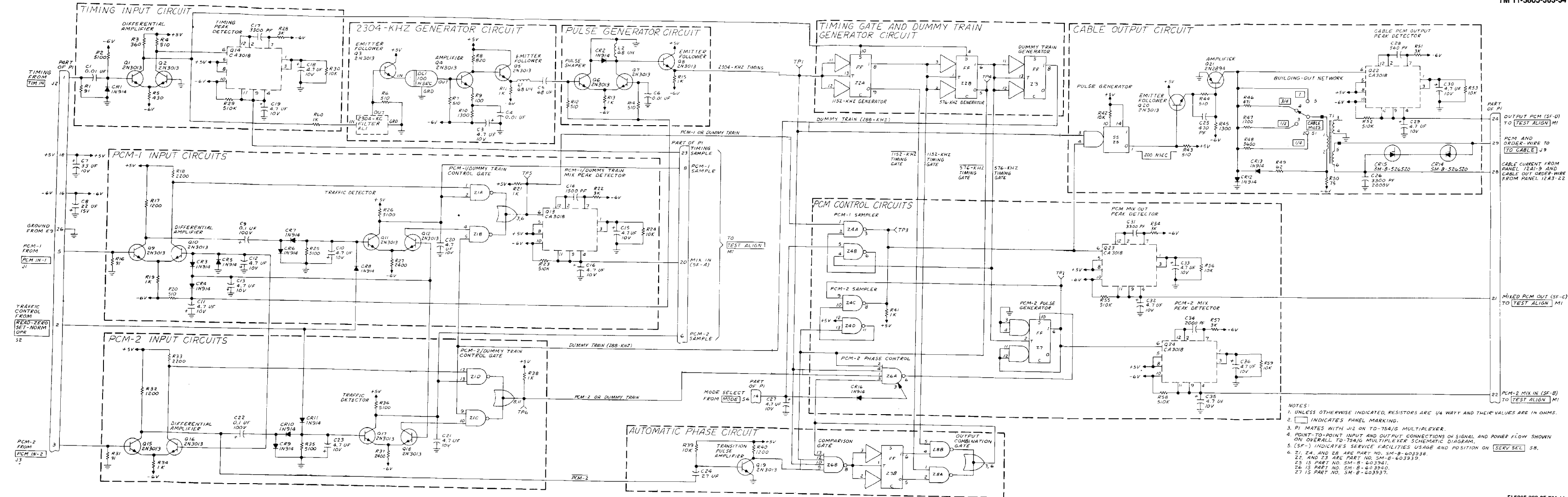


- NOTES:
- UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/4 WATT AND THEIR VALUES ARE IN OHMS.
 - INDICATES PANEL MARKING.
 - PI MATES WITH J15 ON TD-75A16 MULTIPLEXER.
 - POINT-TO-POINT INPUT AND OUTPUT CONNECTIONS OF SIGNAL AND POWER FLOW SHOWN ON OVERALL TD-75A16 MULTIPLEXER SCHEMATIC DIAGRAM.
 - (SF-1) INDICATES SERVICE FACILITIES USAGE AND POSITION ON [SERV SE] SB.
 - Z1, Z2 AND Z3 ARE PART NO. 5M-B-603943.

FO-3. Panel Assembly 12A2, Schematic Diagram.

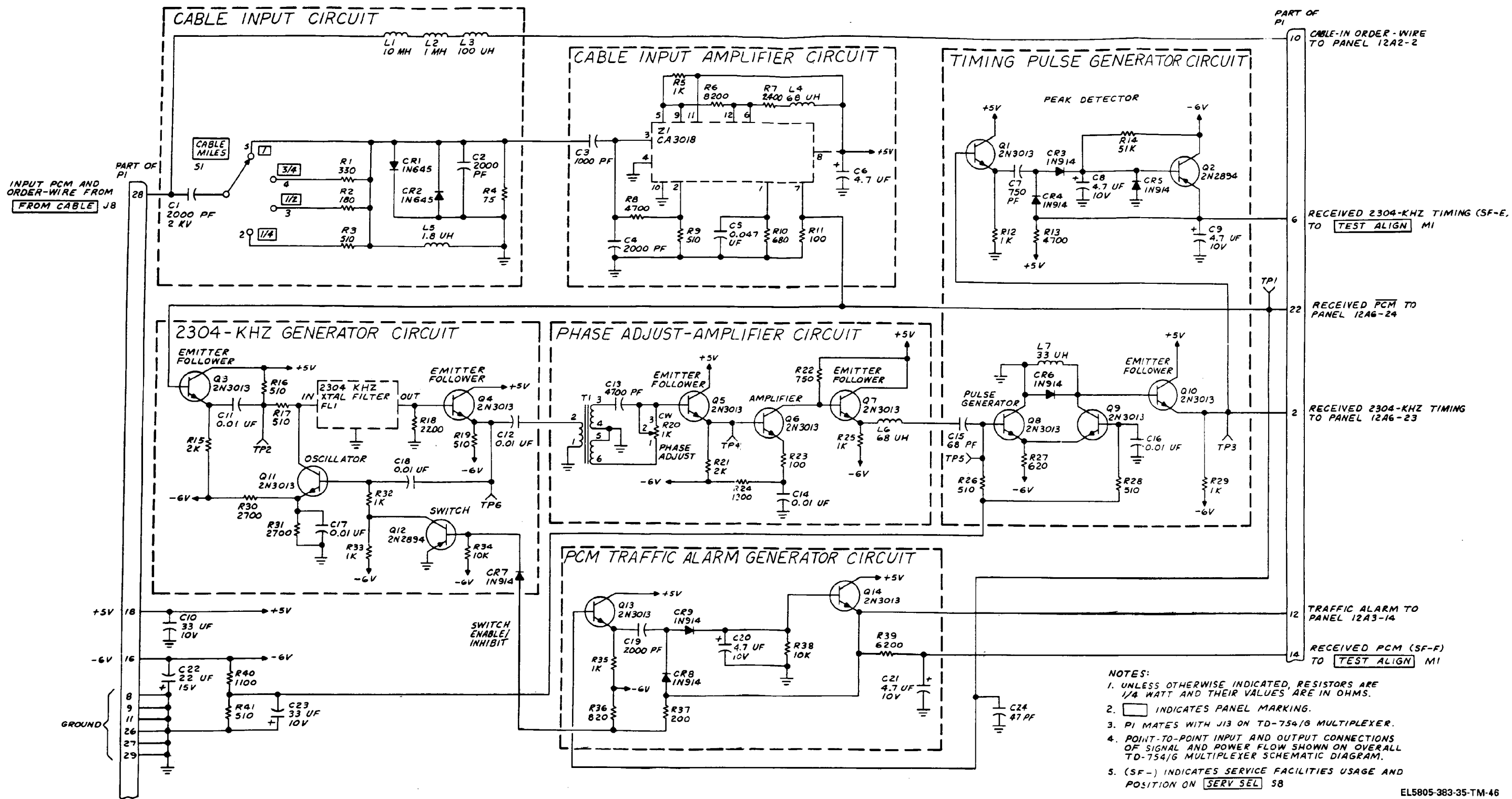


- NOTES:
- UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/4 WATT AND THEIR VALUES ARE IN OHMS.
 - INDICATES PANEL MARKING.
 - PI MATES WITH J16 ON TD-754/G MULTIPLEXER.
 - POINT-TO-POINT INPUT AND OUTPUT CONNECTIONS OF SIGNAL AND POWER FLOW SHOWN ON OVERALL TD-754/G MULTIPLEXER SCHEMATIC DIAGRAM.
 - (SF-1) INDICATES SERVICE FACILITIES USAGE AND POSITION ON **SERV SEL** 5B.
 - Z1 AND Z2 HAS +5V ON PIN 14 AND GROUND ON PIN 7.
 - Z1 AND Z2 ARE PART NO. SM-B-60393B.

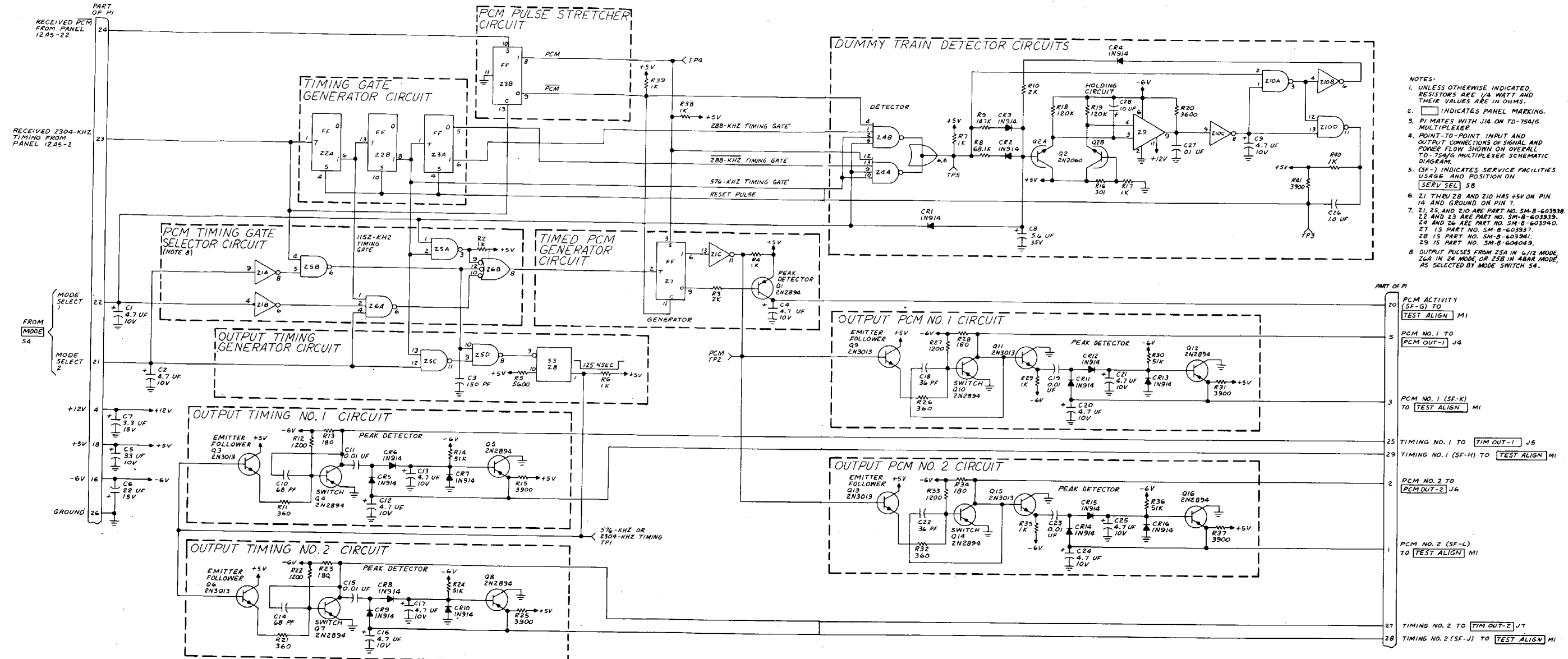


- NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/4 WATT AND THEIR VALUES ARE IN OHMS.
 2. [Symbol] INDICATES PANEL MARKING.
 3. PI MATES WITH J12 ON TD-754/G MULTIPLEXER.
 4. POINT-TO-POINT INPUT AND OUTPUT CONNECTIONS OF SIGNAL AND POWER FLOW SHOWN ON OVERALL TD-754/G MULTIPLEXER SCHEMATIC DIAGRAM.
 5. (SF-) INDICATES SERVICE FACILITIES USAGE AND POSITION ON [SERV SEL] SB.
 6. Z1, Z4, AND Z8 ARE PART NO. SM-B-60338.
 7. Z2 AND Z3 ARE PART NO. SM-B-60339.
 8. Z5 IS PART NO. SM-B-60394.
 9. Z6 IS PART NO. SM-B-60390.
 10. Z7 IS PART NO. SM-B-60397.

FO-5. Panel Assembly 12A4, Schematic Diagram.

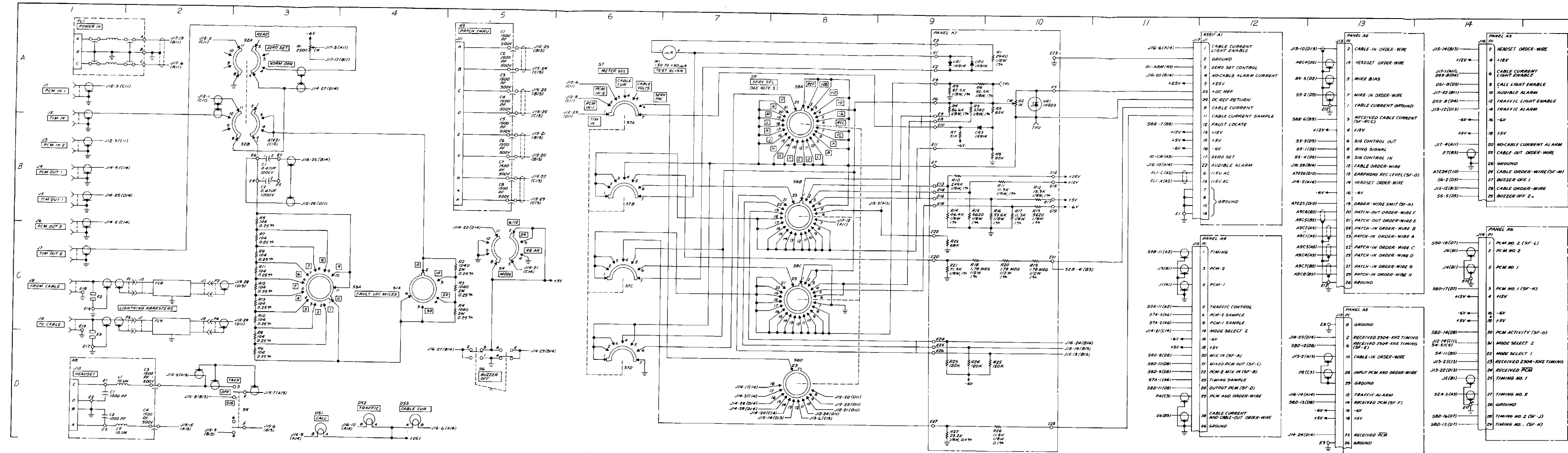


FO-6. Panel Assembly 12A5, Schematic Diagram.



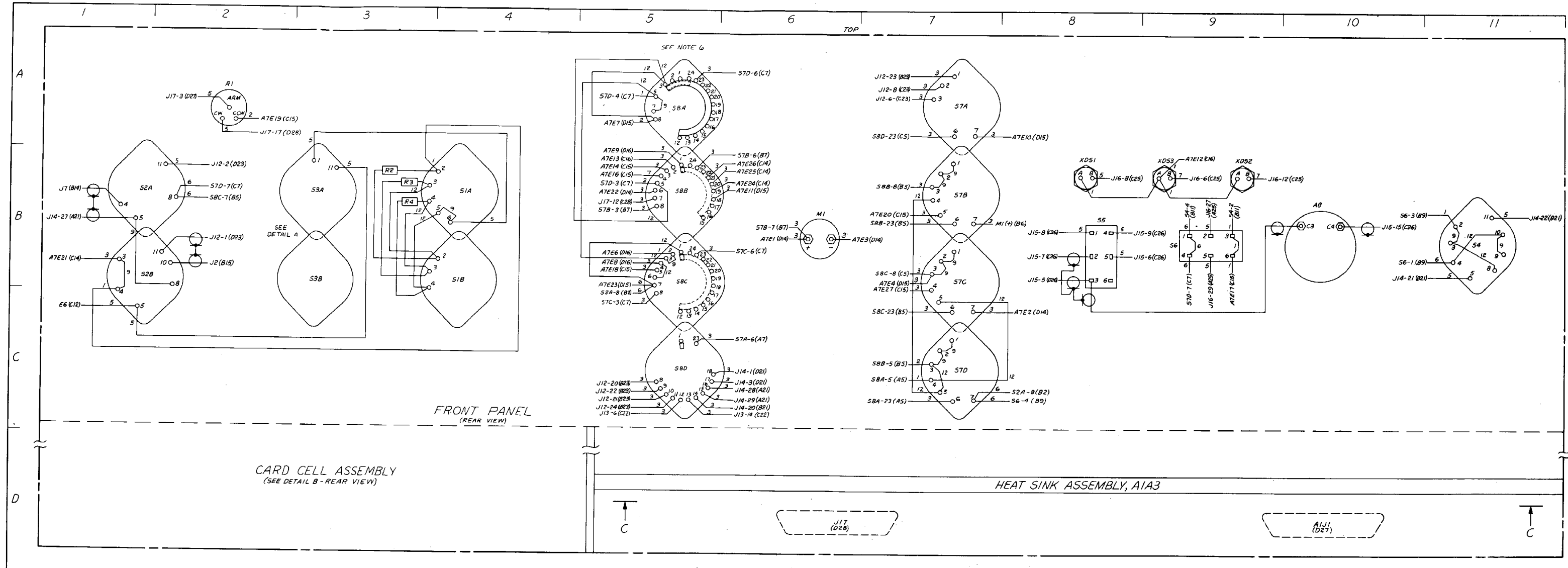
- NOTES:
- UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/4 WATT AND THEIR VALUES ARE IN OHMS.
 - INDICATES PANEL MARKING.
 - PI MATES WITH J14 ON TD-75A/G MULTIPLEXER.
 - POINT-TO-POINT INPUT AND OUTPUT CONNECTIONS OF SIGNAL AND POWER FLOW SHOWN ON OVERALL TD-75A/G MULTIPLEXER SCHEMATIC DIAGRAM.
 - GF-1 INDICATES SERVICE FACILITIES USAGE AND POSITION ON [SERV SEL] 5B
 - Z1 THRU Z8 AND Z10 HAS +5V ON PIN 14 AND GROUND ON PIN 7.
 - Z1, Z5, AND Z10 ARE PART NO. SM-B-60393B. Z2 AND Z3 ARE PART NO. SM-B-60393C. Z4 AND Z6 ARE PART NO. SM-B-60394D. Z7 IS PART NO. SM-B-60393F. Z8 IS PART NO. SM-B-60394E. Z9 IS PART NO. SM-B-604049.
 - OUTPUT PULSES FROM Z5A IN 4/12 MODE, Z6A IN 24 MODE, OR Z5B IN 48AR MODE, AS SELECTED BY MODE SWITCH 54.

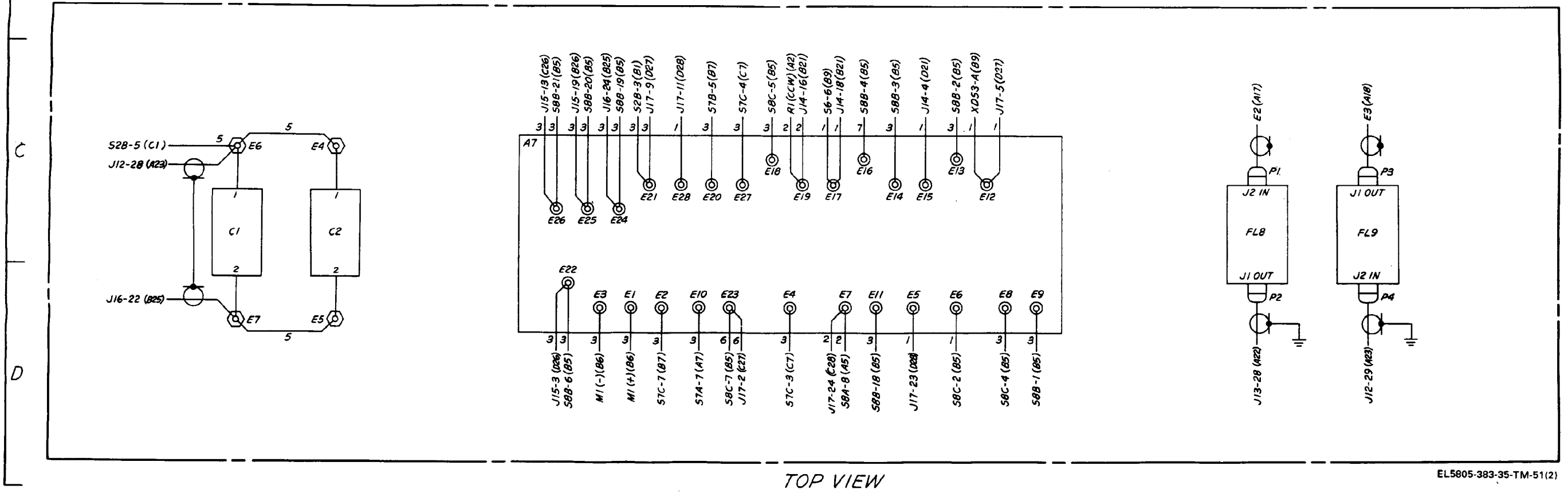
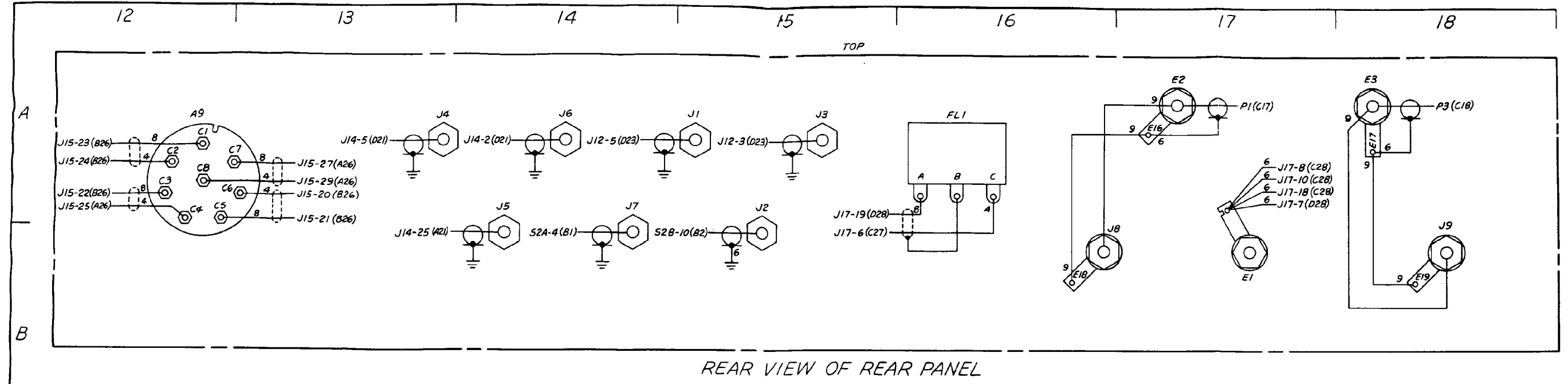
- PART OF PI
- 20 PCM ACTIVITY (SF-G) TO [TEST ALIGN] M1
 - 5 PCM NO. 1 TO [PCM OUT-1] J4
 - 3 PCM NO. 1 (SF-K) TO [TEST ALIGN] M1
 - 25 TIMING NO. 1 TO [TIM OUT-1] J5
 - 29 TIMING NO. 1 (SF-H) TO [TEST ALIGN] M1
 - 2 PCM NO. 2 TO [PCM OUT-2] J6
 - 1 PCM NO. 2 (SF-L) TO [TEST ALIGN] M1
 - 27 TIMING NO. 2 TO [TIM OUT-2] J7
 - 28 TIMING NO. 2 (SF-J) TO [TEST ALIGN] M1

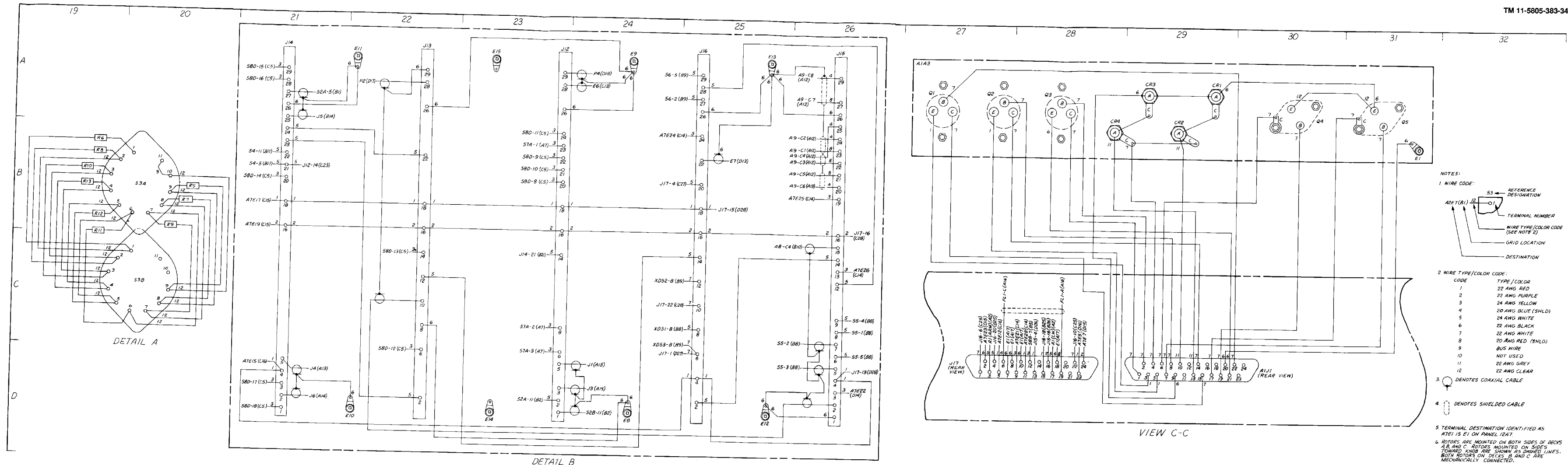


NOTES:
 1. REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX DESIGNATION WITH IE.
 2. [Symbol] INDICATES PANEL MARKING.
 3. UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/4 WATT AND THEIR VALUES ARE IN OHMS.
 4. (SF-) INDICATES SERVICE FACILITIES USAGE AND POSITION ON [SERV SEC] SB.
 5. PHYSICAL VIEW OF DECS 30000 ON TD-754G OVERALL WIRING DIAGRAM.

FO-8. TD-754/G, Overall Schematic Diagram.

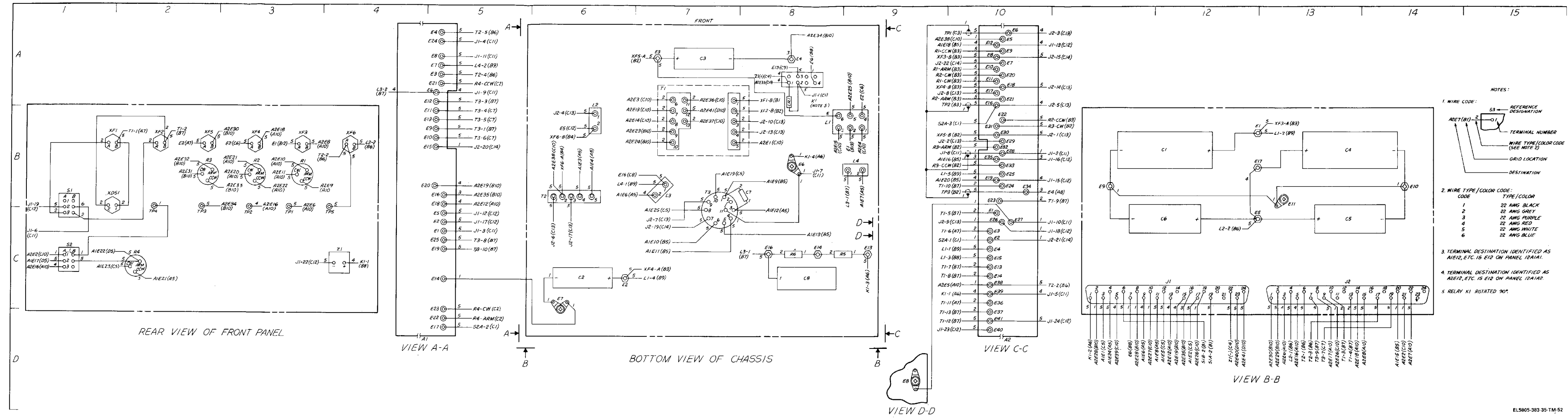






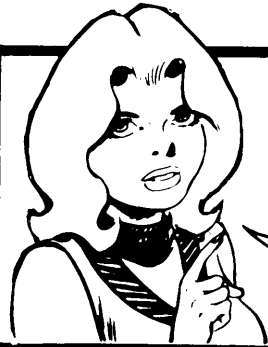
- NOTES:
- WIRE CODE:
 - S3 → REFERENCE DESIGNATION
 - 01 → TERMINAL NUMBER
 - 12 → WIRE TYPE/COLOR CODE (SEE NOTE 2)
 - 19 → GRID LOCATION
 - 10 → DESTINATION
 - WIRE TYPE/COLOR CODE:

CODE	TYPE / COLOR
1	22 AWG RED
2	22 AWG PURPLE
3	24 AWG YELLOW
4	20 AWG BLUE (SHLD.)
5	24 AWG WHITE
6	22 AWG BLACK
7	22 AWG WHITE
8	20 AWG RED (SHLO.)
9	BUS WIRE
10	NOT USED
11	22 AWG GREY
12	22 AWG CLEAR
 - ⊙ DENOTES COAXIAL CABLE
 - ⊞ DENOTES SHIELDED CABLE
 - TERMINAL DESTINATION IDENTIFIED AS A7E15 IS E1 ON PANEL 12A7.
 - ROTORs ARE MOUNTED ON BOTH SIDES OF DECKS A, B, AND C. ROTORs MOUNTED ON SIDES TOWARD KNOB ARE SHOWN AS DASHED LINES. BOTH ROTORs ON DECKs B AND C ARE MECHANICALLY CONNECTED.



FO-10. Power Supply Assembly 12A1, Overall Wiring Diagram.

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS



THEN... JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT. FOLD IT AND DROP IT IN THE MAIL!

SOMETHING WRONG WITH THIS PUBLICATION?

FROM (PRINT YOUR UNIT'S COMPLETE ADDRESS)
 Commander
 Stateside Army Depot
 ATTN: AMSTA-US
 Stateside, N.J. 07703-5007

DATE SENT
 10 July 1975

PUBLICATION NUMBER
 TM 11-5840-340-12

PUBLICATION DATE
 23 Jan 74

PUBLICATION TITLE
 Radar Set AN/PRC-76

BE EXACT PIN-POINT WHERE IT IS

PAGE NO	PARA-GRAPH	FIGURE NO	TABLE NO
2-25	2-28		
3-10	3-3		3-1
5-6	5-8		
		FO3	

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°.

REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.

Item 5, Function column. Change "2 db" to "3db."

REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.

Add new step f.1 to read, "Replace cover plate removed in step e.1, above."

REASON: To replace the cover plate.

Zone C 3. On J1-2, change "+24 VDC to "+5 VDC."

REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

TEAR ALONG PERFORATED LINE

PRINTED NAME, GRADE OR TITLE AND TELEPHONE NUMBER
 SSG I. M. DeSpiritof 999-1776

SIGN HERE

FILL IN YOUR
UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS

Commander
US Army Communications-Electronics Command
and Fort Monmouth
ATTN: AMSEL-LC-LM-LT
Fort Monmouth, New Jersey 07703-9988

SAMPLE



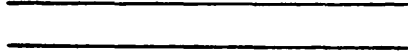
FOLD BACK

TEAR ALONG PERFORATED LINE

FILL IN YOUR
UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY



OFFICIAL BUSINESS

Commander
US Army Communications-Electronics Command
and Fort Monmouth
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