TM 11-5805-367-35/1

DEPARTMENT OF THE ARMY TECHNICAL MANUAL

DS, GS, AND DEPOT MAINTENANCE MANUAL

MULTIPLEXERS

TD-202/U

AND TD-203/U

This copy is a reprint which includes current pages from Changes 1 through 3.

HEADQUARTERS, DEPARTMENT OF THE ARMY
24 JANUARY 1967

WARNING

Be careful not to contact the 115-volt ac line connections when using this equipment. Serious injury or death may result.

DON'T TAKE CHANCES!

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL

4. SEND FOR HELP AS SOON AS POSSIBLE

5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

WARNINGS

TD-202 and TD-203/U weigh 50 pounds. Be careful when moving. Two person lift required.

Prevent injury when applying or removing steel strapping by wearing heavy gloves and a face shield or goggles (NSN 4240-00-542-2048). Do not handle packing cartons by the steel strapping.

Compressed air shall not be used for cleaning purposes except where reduced to less than 29 pounds per square inch (psi) and then only with effective chip guarding and personnel protective equipment. Do not use compressed air to dry parts when TRICHLOROTRIFLUOROETHANE has been used. Compressed air is dangerous and can cause serious bodily harm if protective means or methods are not observed to prevent chip or particle (of whatever size) from being blown into the eyes or unbroken skin of the operator or other personnel.

Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

TECHNICAL MANUAL

No. 11-5805-367-35/1

HEADQU ARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D. C. 24 January 1967

DS, GS, AND DEPOT MAINTENANCE MANUAL MULTIPLEXERS TD 202/U (NSN 5805-00-884-2176) AND TD-203/U (NSN 5805-00-884-2177)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter or DA Form 2028 (Recommended Changes to Publications and Blank Forms), direct to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, NJ 07703-5000 In either case, a reply will be furnished direct to you.

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (CONT)

LIST OF ILLUSTRATIONS (CONT)

*Foldouts located in back of manual

CHAPTER 1
INTRODUCTION

1-1. Scope

This manual covers direct support (DS), general support (GS), and depot maintenance for Multiplexer TD-202/U and Multiplexer TD-203/U. It includes troubleshooting, testing aligning, and repairing the equipment; replacing maintenance parts. It also lists material and test equipment required for DS and GS maintenance. Detailed functioning of the equipment is covered in chapter 2. Refer to TM 11-5805-367-12 for applicable forms and records.

1-2. Consolidated Index of Army Publications and Blank Forms

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

1-3. Maintenance Forms, Records and Reports

a. *Reports of Maintenance and Unsatisfactory Equipment.* Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750 as contained in Army Maintenance Management Update.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 73511-2/DLAR 4140.55/NAVMATINST 4355.73B/ AFR 400-54/MCO 4430.3H.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR)

If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-PA-MA-D, Fort Monmouth, New Jersey 07703-5000. We'll send you a reply.

1-5. Administrative Storage

administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance Title the PMCS charts before storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness. Disassembly and repacking of equipment for shipment or limited storage are covered in TM 740-90-1.

1-6. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

1-7. Differences Between Models/Silicon Versions

This paragraph contains information covering redesigned multiplexer subassemblies used in the TD-202/U and TD-203/U Multiplexers. These redesigned subassemblies use silicon semiconductors in lieu of germanium devices. Subassemblies equipped with silicon semiconductors are identified by the suffix letter "A". For example, 5A5A denotes a silicon version and 5A5 denotes a germanium version of the same multiplexer subassembly. It is possible, that multiplexers in the field might be equipped with a combination of germanium and silicon subassemblies. The germanium subassemblies and the silicon subassemblies can be used interchangeably. The following subassemblies contain silicon subassemblies.

Panels 5A2A through 5A8A ..... Multiplexer TD-202/U

Panels 4A7A and 4A8A ..... Multiplexer TD-203/U

Note

- Unless otherwise noted in this manual, data relating to the subassemblies containing germanium semiconductors apply to the subassemblies containing the silicon semiconductors.
- Silicon subassemblies are considered to be nonrepairable items and should be returned to depot for final disposition.

CHAPTER 2

FUNCTIONING

Section I. BLOCK DIAGRAM ANALYSIS

Note. This manual describes Muitiplexers TD-202/U and TD-203/U. Because the function of the multiplexers is similar, differing mainly in the channel capacity, the manual serves the dual purpose of describing both multiplexers. When functions or descriptions apply to both the TD-202/U and the TD-203/U, only the TD-203/U is described, and a parenthetical reference is made to the TD-202/U. For example: TD-203/U (TD-202/U); 96- (24-) channel; 48 (12-) channel.

2-1. General

Multiplexer TD202/U (12 or 24 channels) or Multiplexer TD-203/U (48 or 96 channels) functions as a combiner in a radio-terminal or radio repeater facility. Familiarity with the equipment, how it works, and why it works that way are valuable tools for troubleshooting the equipment rapidly and effectively

a. 48- (12-) Channel Operation. For transmission, a binary pulse-train signal with an associated timing signal is combined to form a radio baseband signal. For reception, the baseband signal is regenerated to form a binary pulse train with an associated timing signal.

b. 96- (24-) Channel Operation. Interleaved (I), separated (S), or repeater (R) optional modes may be selected by the TRAFFIC SEL switch; the switch position is determined by the application requirement (TM 11-5805-367-12). Two binary pulse-train signals, with one associated timing signal, are combined into a radio baseband signal for transmission. The received radio baseband signal is converted into two binary pulse train signals, each with an associated timing signal.

2-2. T-202/U Transmit Circuit (fig. 6-19)

a. 12- Channel Operation. The binary pulse-train signal (PCM IN-1) is applied to the sampler 1 and the detector inhibitor. The signal applied to the detector inhibitor prevents the operation of the gate, when no signal is present. With an input signal present, the detector inhibitor activates the gate. The timing input signal is applied through the delay circuits to insure that the timing pulse transitions do not occur in coincidence with the transitions of the pulses in the binary pulse-train signal. The binary pulse train is regenerated and reshaped in the flip-flop, and applied through the radio drivers to the radio (TO RADIO XMTR) as the baseband signal.

b. 24- Channel Operation Two binary pulse-train signals (PCM IN-1 and PCM IN-2) are applied to the TD-202/U. The PCM IN-1 binary pulse-train signal operates as in *a* above. The PCM IN-2 binary pulse train signal is applied to the automatic phase control and the detector inhibitor. The automatic phase control, with the timing signal, insures that the PCM IN-2 binary pulse-train signal is properly timed for interleaving with the PCM IN-1 binary pulse train signal. The detector inhibitor, the gate, and the sampler 2 function as in a above. The two signals are applied to the flip-flop; its output is an interleaved signal consisting of PCM IN-1 and PCM IN-2, properly timed by the timing signal. The combined signal is applied through the radio drivers to the radio (TO RADIO XMTR) as the baseband signal.

2-2.1. TD-203/U Transmit Circuit (fig. 6-19)

a. 48-Channel Operation. The binary pulse train signal (PCM IN-1) is applied to the differential amplifier. The outputs of this amplifier are applied to output control gates, and the peak detector. With an input signal present, the peak detector activates the output flip-flop control gates on the signal is not present, the peak detector inhibits the output flip-flop control gates. The timing input

signal (TIM IN-1) is applied to a differential amplifier. The output of this amplifier is applied to the inhibit and delay gate and a delay circuit. The inhibit and delay gate is not used in 48-channel operation. The timing input signal is applied through the delay circuit to the output flip-flop control gates to insure that the timing pulse transitions do not occur in coincidence with the transitions of the pulses in the binary pulse train signal. The binary pulse train is regenerated in the flip-flop, with the outputs from the flip-flop control gates. The output of the flip-flop is fed through the radio driver to the radio (TO RADIO XMTR) as the baseband signal.

b. 96-Channel Operation. Two binary pulse train signals (PCM IN-1 and PCM IN-2) are applied to the TD-203/U. The PCM lN-1 binary pulse train operates as in a above. The PCM IN-2 pulse train is applied to another differential amplifier. The output of the differential amplifier is applied to the read-in gates and storage, and the peak detector. The TIM IN-2 signal is applied to the delay circuit and a differential amplifier. The output of this differential amplifier is fed to a peak detector, a divide-by-6 circuit, and to the read-in gates and storage. The peak-detected PCM IN-2 and TIM IN-2 trains are applied to a gate. Failure of either train will produce an output from the gate to the inhibit and delay circuit in the TIM IN-1 line. PCM IN-2 is sequentially read into the storage elements with the associated timing derived from the divide-by-6 circuit at one-sixth the bit rate. In this manner, each PCM IN-2 bit is stored for six bits with no loss of pcm information. Each storage element is read out sequentially at one-sixth the bit rate with the TIM IN-1 train which may have jitter relative to PCM IN-2. In this manner, the original pcm train is reconstructed and synchronized with the PCM IN-1 timing (TIM IN-1). The readout timing is derived from the TIM IN-1 signal output from the differential amplifier through the inhibit and delay gate, through another gate, and the divide-by-6 circuit. Since both pcm trains are now synchronized, with the same Liming signal, they are easily interleaved into one signal in the output flip-flop control gates. To avoid occurrence of the read out pulse at read-in time, the read-in and readout pulses for the first storage element are compared in a gate. The readout pulses derived from readout gate Z8B are compared with the read-in bracket pulse in gate Z8A. If a coincidence is detected, the flip-flop is set with the output of gate Z8A. The output of the flip-flop is applied to gate Z5A and inhibits the next timing pulse. This pulse also resets the flip-flop to enable subsequent timing pulses to pass through the gate. In this manner, one pulse is deleted from the timing train and ail readout pulses are shifted one bit. This process continues until no coincidence exists between the read-in and readout pulses. This allows as much as four bits peak-to-peak jitter between the PCM IN-1 and PCM IN-2 signals with no transmission errors. The interleaved pcm signal is regenerated in the output flip-flop and passed to the radio driver and output level adjust as the baseband signal.

2-3. Receiving Circuits (fig. 6-19).

a. 48- (12-) Channel Operation. The composite signal received from the radio (FROM RADIO RCVR is applied to the video amplifier and clamp where the pcm and orderwire signals are separated. The order wire is applied through an order-wire detector, where it is processed and applied to the order-wire circuits (ORDER WIRE). The pcm is applied to the differentiator and slicer, the positive and negative peak detectors, and the decision circuits. The output of the differentiator and slicer is applied to a 2,304-kc (576-kc) crystal filter that extracts the timing signal, which is applied to a pulse generator. The TRAFFIC SEL switch divides the pulse generator output into two branches. One branch is applied through an amplifier to the decision circuits as a timing signal. The outputs of the positive and negative peak detectors are applied to the decision circuits, which compare them with the pcm signal. The resulting output is applied to the flip-flop to regenerate the pcm signal. The regenerated pcm signal is applied to a differential pulse amplifier. The TRAFFIC SEL switch applies the other branch of the pulse generator output to the inhibitor

and timing-selection circuit. The output of the inhibitor and timing-selector circuit is the *timing out-l* signal which is applied to the differential pulse amplifier. The differential pulse amplifiers sample the pcm train with the timing signal. The resulting output is applied to flip-flops which regenerate the pcm binary train (PCM OUT-1 and PCM OUT-2).

b. 96- (24-) Channel Operation. Operation in 96- (24-) channels mode is the same as described in a above except that the timing signal is extracted by the 4,608-kc (1,152-kc) crystal filter. This is applied to the pulse generator and fed through the TRAFFIC SEL switch to the amplifier, and to the inhibitor and timing selection. The output of the inhibitor and timing selection consists of two timing signals (TIMING OUT-1 and TIMING OUT-2) that are applied to two differential pulse amplifiers. The outputs of the two differential pulse amplifiers are applied to flip-flops whose outputs are PCM OUT-1 and PCM OUT-2. A third amplifier provides the pcm address signal which is applied to the error-checking circuits. In separate operation, the address signal in the pcm is compared for error with a local address signal, derived from a countdown driver. With an error, the error checking circuit develops a skip pulse to synchronize the local address with the incoming pcm signal. To insure that the correct binary train is selected from the interleaved pair, skip pulses are permitted to escape the error-checking circuit to the inhibitor and timing selection, where the timing is skipped by one bit to shift the 8-kc output of the countdown divider to the next pulse in the pcm train. The skip pulses are continued until the local address signal coincides with the address signal in the pcm train. The pcm signals (PCM OUT-1 and PCM OUT-2) are then separated with correct identification.

2-4. Power and Alarm Circuits

The power and alarm circuits are conventional. Since the function of the power and alarm circuits is standard, no block diagram analysis is provided. For additional information, refer to paragraphs 2-9 through 2-18.

Section II. MODULE SCHEMATIC ANALYSIS

2-5. General

Timing generator No. 3, panel 4A6/5A6 contains eight set-reset flip-flop modules (module 09), one complement flip-flop module (module 18), and three pulse-shaper modules (two modules 44 and one module 30) . The circuit analysis of each module is covered in paragraphs 2-6, 2-7, and 2-8. Unless otherwise specified, a positive-going pulse is one switching from -4. 5 volts to 0 volt (ground), and a negative-going pulse is one switching from 0 volt to -4. 5 volts. Some of the TD-203/U circuits employ diode transistor logic (DTL) integrated circuit modules. Transmit No. 1, panel 4A10, contains nine RS/T flip-flop modules (SE124K), seven dual high fanout NAND/NOR gate modules (SE113K), and one dual NAND/NOR gate (buffer) module (SE157K). Transmit No. 2, panel 4A2, contains four SE124K modules, one SE157K module, nine SE113K modules, and one monostable multivibrator module (SE161K). The function of each module is covered in paragraphs 2-8. 1 through 2-8. 4. Unless otherwise specified, positive logic is assumed with -4 . 5 volts representing logic 0 and ground representing logic one (1) .

2-6 Flip-Flop Module 09 (fig. 2-1)

a. Function. Flip-flop module 09 is a highspeed, bistable multivibrator, capable of switching states at a 2.3-megacycle (mc) rate. The flip-flop switches states in response to 4.5-volt positive-going trigger pulses applied to the collector of the cutoff transistor. These pulses are routed to the collector through input triggering circuits from pins 3 and 9. Outputs are taken from the collector of either transistor and are available through pins 2 and 10. The output at one of these pins

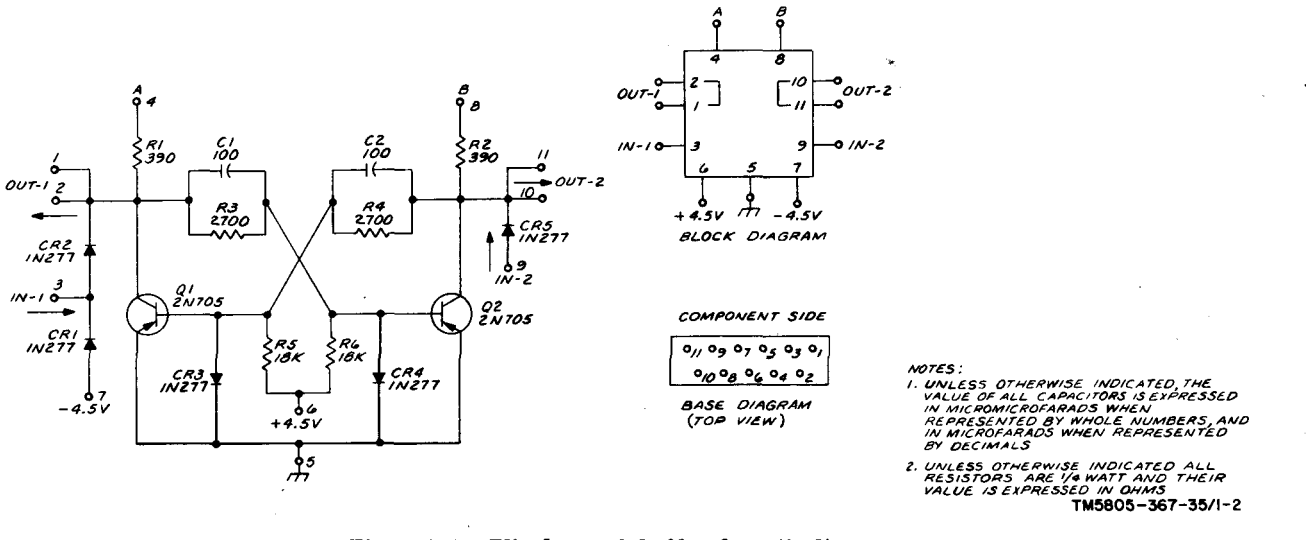


Figure 2-1. Flip-pop module 09, schematic diagram.

is -0.2 volt, while at the other pin, it is -4.3 volts.

b. Circuit Description. Flip-flop module 09 consists of multi-vibrator transistors Q1 and Q2, steering diodes CR2 and CR5, and trigger-loading diode CR1. The bases of transistors Q1 and Q2 are clamped slightly positive by diodes CR3 and CR4, respectively. Either set-reset input triggering or complemented input triggering is used for switching.

2-7. Flip-Flop Module 18

a. Function. Flip-flop module 18 is a bistable multivibrator which uses set-reset or complemented input triggering. The multivibrator changes stable states in response to pulses varying between 0. 0 and -4.5 volts. These pulses are applied to the base of either transistor, through external input triggering circuits on pin 5 or 8. In addition, a -4.5-volt positive-going pulse applied to pin 3 switches the flip-flop when pins 1 and 11 are tied to pins 2 and 10, respectively. Outputs are taken from either collector and are applied to external circuits through pins 2 and 10. The output from one of the pins is 0.0 volt, and the output of the other is -4.5 volts.

b. Circuit Description. Flip-flop module 18 consists of multivibrator transistors Q1 and Q2, and a complemented input triggering circuit con

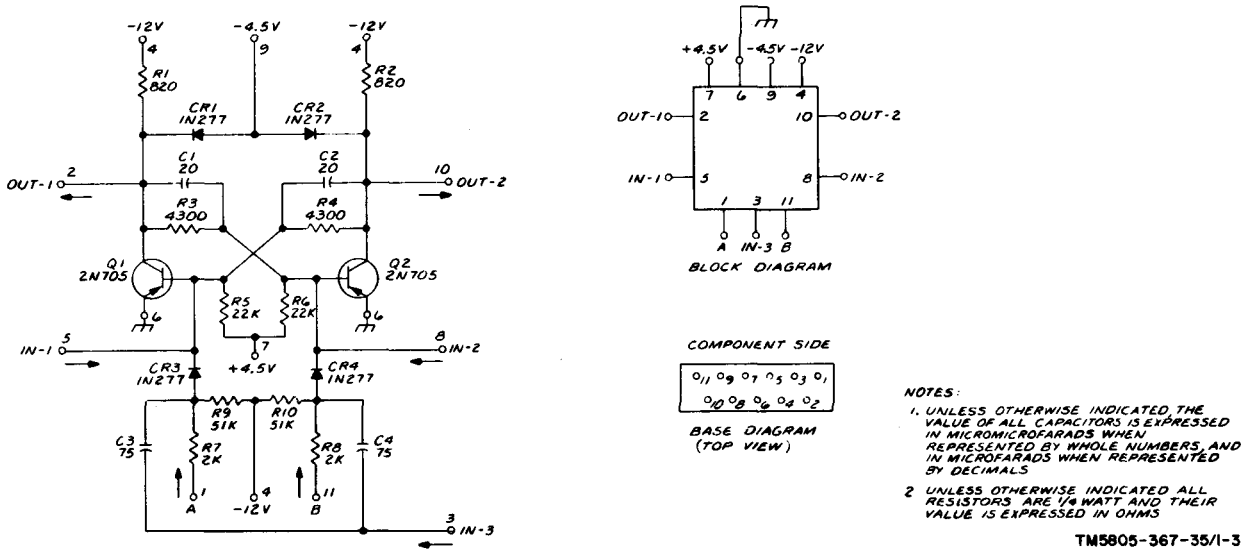


Figure 2-2 Flip-Flop module 18, schematic diagram.

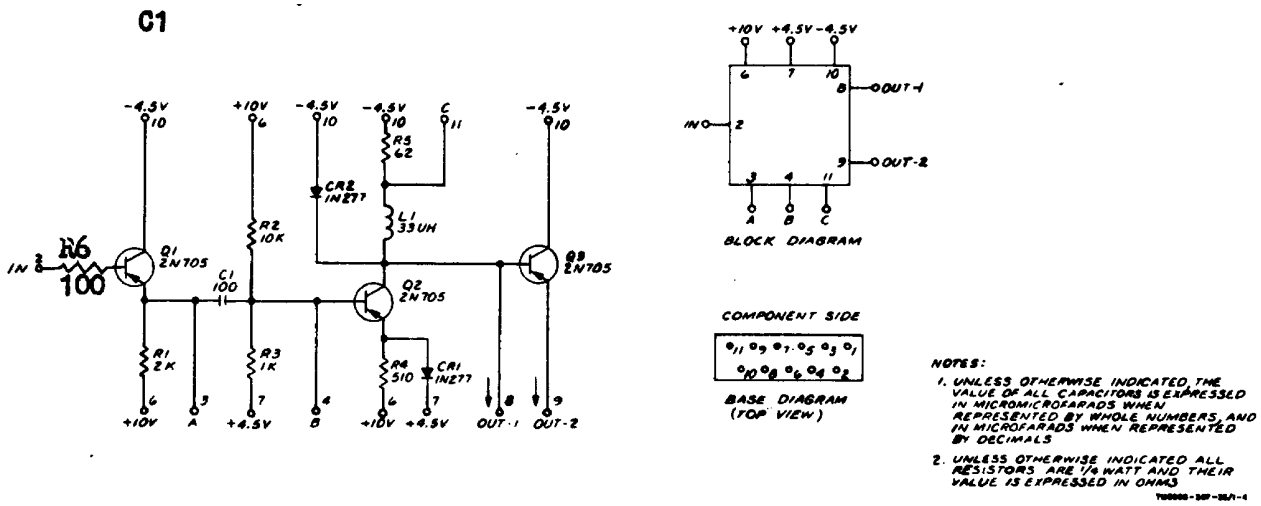


Figure 2-3. Pulse-shaper module 30, schematic diagram.

sisting of two biased steering gates. The input to both steering gates is applied through pin 3. The collectors of transistors Q1 and Q2 are clamped at -4.5 volts by diodes CR1 and CR2, respectively.

2-8. Pulse-Shaper Modules 30 and 44 (fig. 2-3 and 2-4)

a. Function. The input to pulse-shaper module 30 or 44 is a negative square-pulse signal with a frequency range between 8 kc and 2.3 mc and with an approximate 4.5-volt amplitude. The output of the pulse shaper is a sharp, positive output pulse of fixed duration, in phase with the negative edge of the input signal. The output pulse continues for 100 nanoseconds (nsec), with an amplitude varying between 4.5 and 9.0 volts.

b. Circuit Description. Pulse-shaper modules 30 and 44 consist of emitter-follower transistor Q1, differentiator-capacitor C1, resistors R2 and R3, pulse-amplifier transistor Q2, and output driver transistor Q3. The output is applied to external circuitry either from the collector of transistor Q2 or the emitter of transistor Q3.

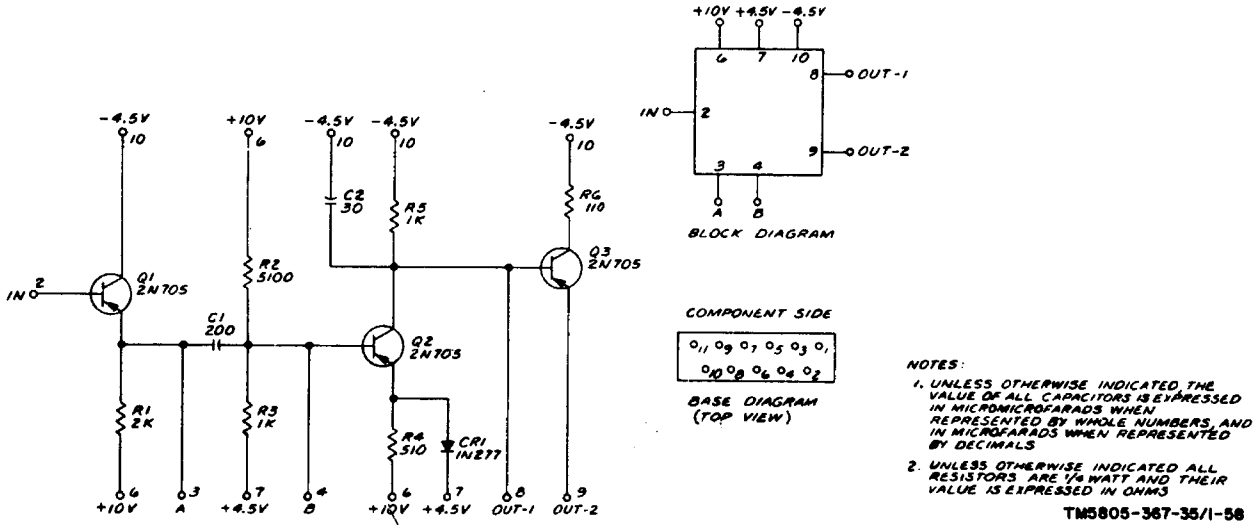


Figure 2-4. Pulse-shaper module 44, schematic diagram.

2-8.1. NAND/NOR Gate Module SE113K (fig. 2-4.1)

a. Function. Module SE113K is a dual high fanout NAND/NOR gate with three inputs to each gate.

b. Theory. When all inputs to pins 3, 4, and 5 are simultaneously at logic 1, the inverted output at pin 2 will be at logic 0. The associated gate operates in the same manner with inputs at pins 7, 8, and 9 and the output at pin 10. Therefore, the logic gates are NAND gates. When any one of the three inputs to a gate is at logic 0 the inverted output will be a logic 1. Additional logic is obtained by tying the outputs at pins 2 and 10 together. In this case the resultant output will be a 0 if the output of one gate is at logic 0. If the outputs of both gates are at logic 1 the resultant output, from the tie point, is a logic 1. Therefore, the tie point connection is basically an AND gate.

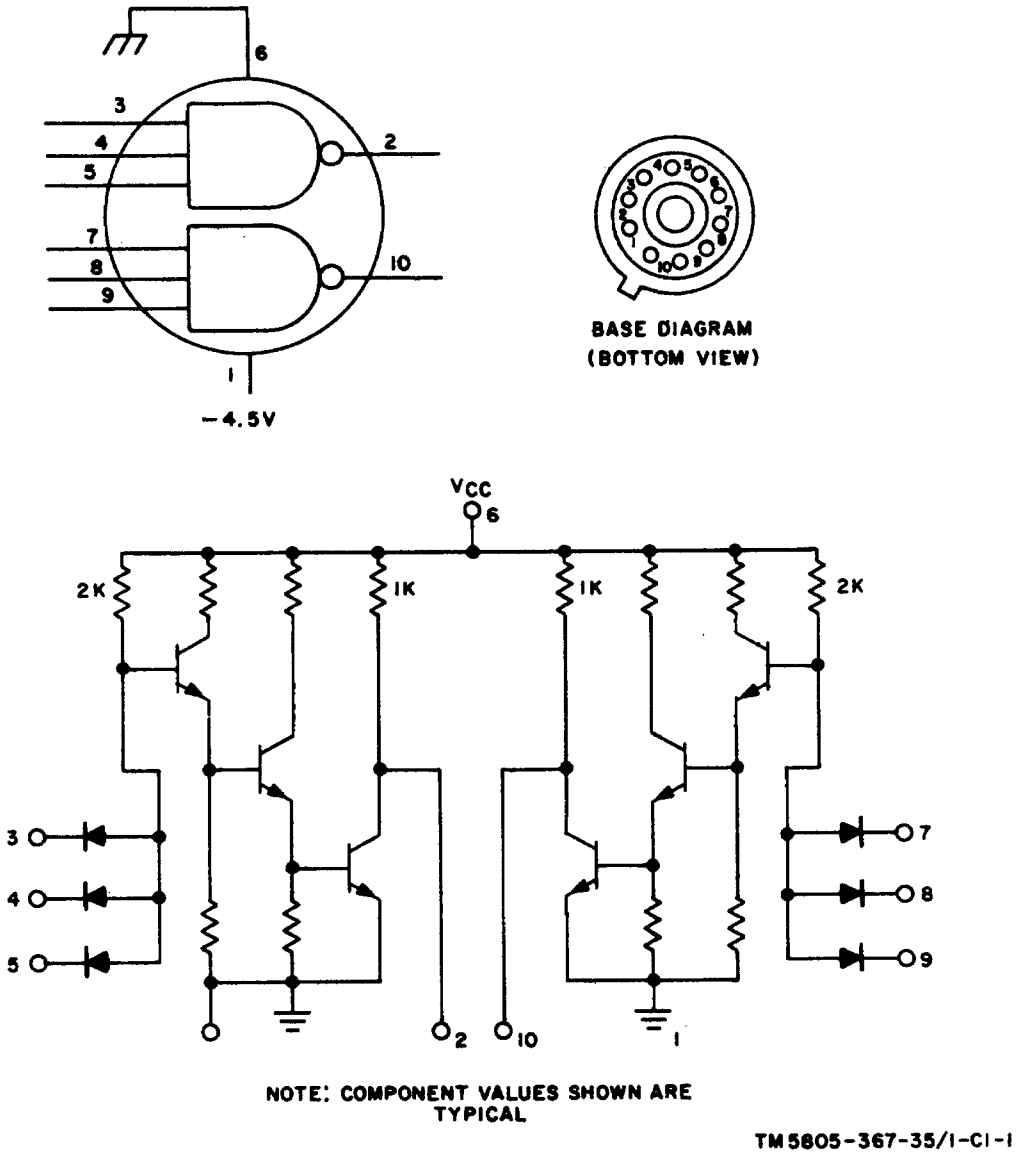


Figure 2-4.1. High fanout NAND/NOR gate integrated circuit module (SE113K), basic application and schematic diagram.

2-8.2. Flip-Flop Module SE124K (fig. 2-4.2)

a. Function. Module SE124K is an RS/T binary element used for ripple counting, storage, and control circuits. This device has input provisions for both synchronous (clocked) and asynchronous operation.

b. Theory. When connected as shown in figure 2-4.2A, the module is used as a binary storage device or counter. When a clock pulse is applied to the T input the output state will be controlled by the levels present at the S and C inputs. Truth table 1 shows the output state for all input levels in synchronous operation. When no clock pulse is present at the T input, the output state of the binary element can be controlled asynchronously by the SD and CD inputs. The truth table in figure 2-4.2B shows the output state, for all SD and CD inputs. Various logic functions can be implemented using both basic modes of operation.

2-8.3. NAND/NOR Gate (Buffer) Module SE157K (fig. 2-4.3)

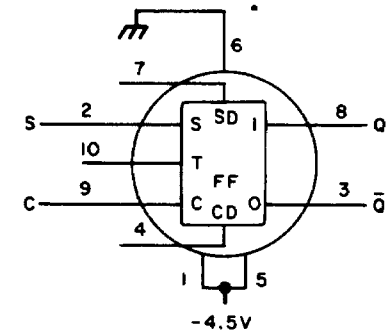
a. Function. The SE157K is a NAND/NOR gate consisting of dual diode transistor logic buffers. This device is intended for clock and capacitive line driving applications.

b. Theory. When all inputs to pins 3, 4, and 5 are simultaneously at logic 1, the inverted output at pin 2 will be at logic 0. The associated gate operates in the same manner with inputs at pins 7, 8, and 9 and the output at pin 10. Therefore, the logic gates are NAND gates. When any one of the three inputs to a gate is at logic 0 the inverted output will be a logic 1.

2-8.4. Monostable Multivibrator Module SE161K (fig. 2-4.4)

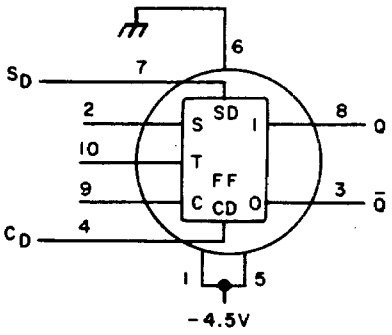
a. Function. The SE161K is a general purpose monostable multivibrator (single-shot) device with a gasted clock input and complementary outputs. The output pulse duration may be increased by adding external capacity across pins 7 and 8.

b. Theory. The nominal outputs at pins 10 and 4 are 0 and 1, respectively. This device is activated when input pin 2 is at logic 0 and a clock pulse is applied to pin 3. This causes pin 10 to go to logic 1 and pin 4 to logic 0 for the active time duration of the device. The outputs then revert to their normal state. If the gate input (pin 2) is at logic 1 the single shot is inhibited and no change occurs with the clock pulse.



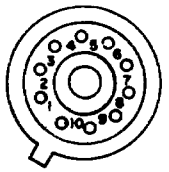
TRUTH TABLE		
S	C	Q
0	0	(NOTE 1)
0	1	0
1	0	1
1	1	NO CHANGE

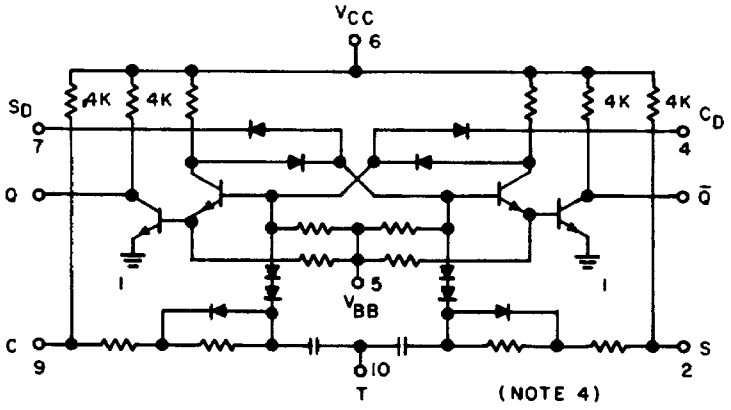
A. COUNTER OR STORE APPLICATION (NOTE 2)



TRUTH TABLE		
S_D	C_D	Q
0	0	(NOTE 3)
1	0	1
0	1	0
1	1	NO CHANGE

B. FLIP-FLOP APPLICATION





NOTES:

1. INDETERMINATE.
2. BOTH S_D AND C_D INPUTS AT LOGIC 1.
3. BOTH Q AND $\bar{Q}$ AT LOGIC 1.
4. COMPONENT VALUES SHOWN ARE TYPICAL.

TM5805-367-35/1-C1-2

Figure 2-4.2. Flip-flop integrated circuit module SE124K), basic application and schematic diagram

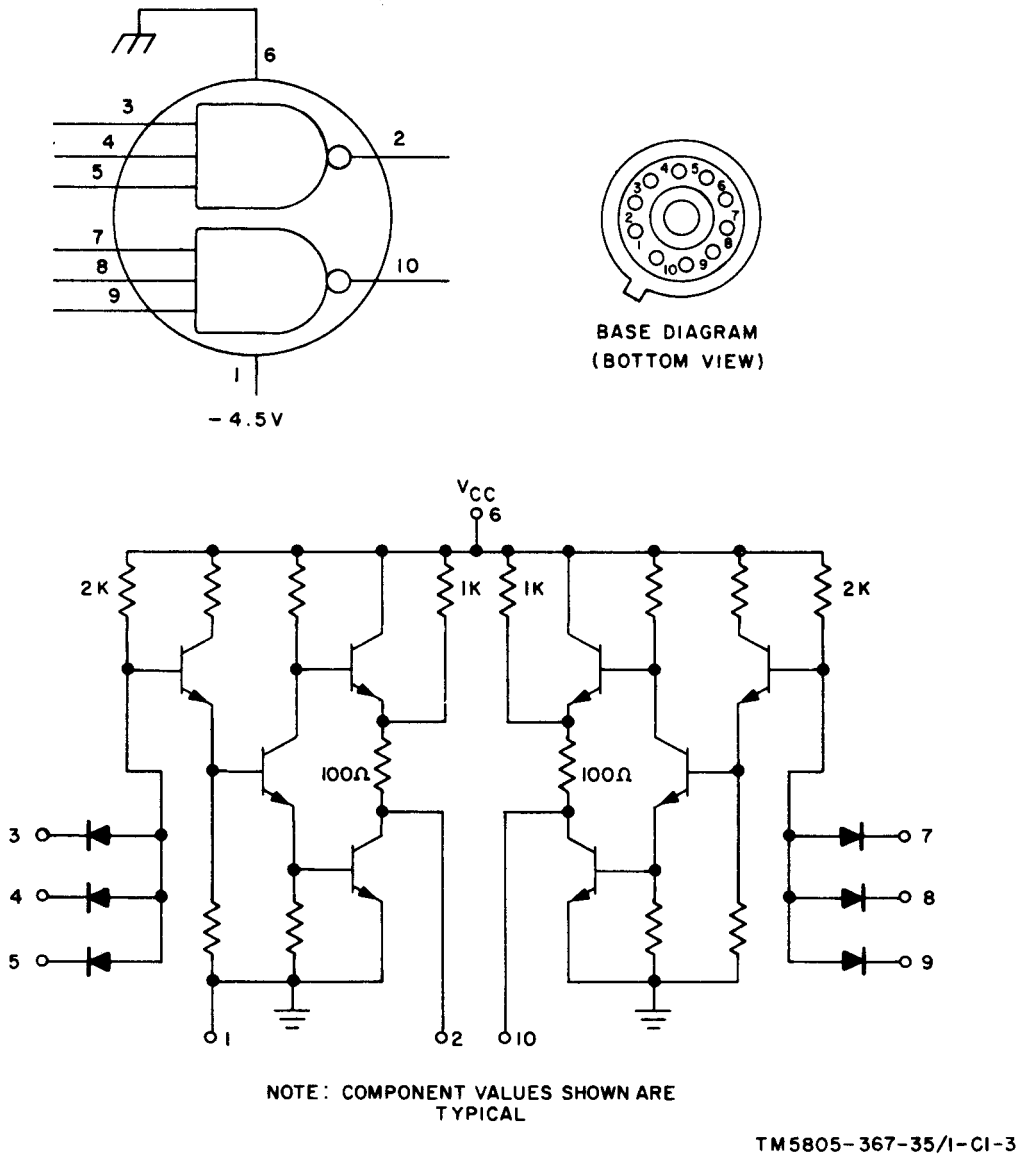


Figure 2-4.3. NAND/NOR gate (buffer) integrated circuit module (SE157K), basic application and schematic diagram.

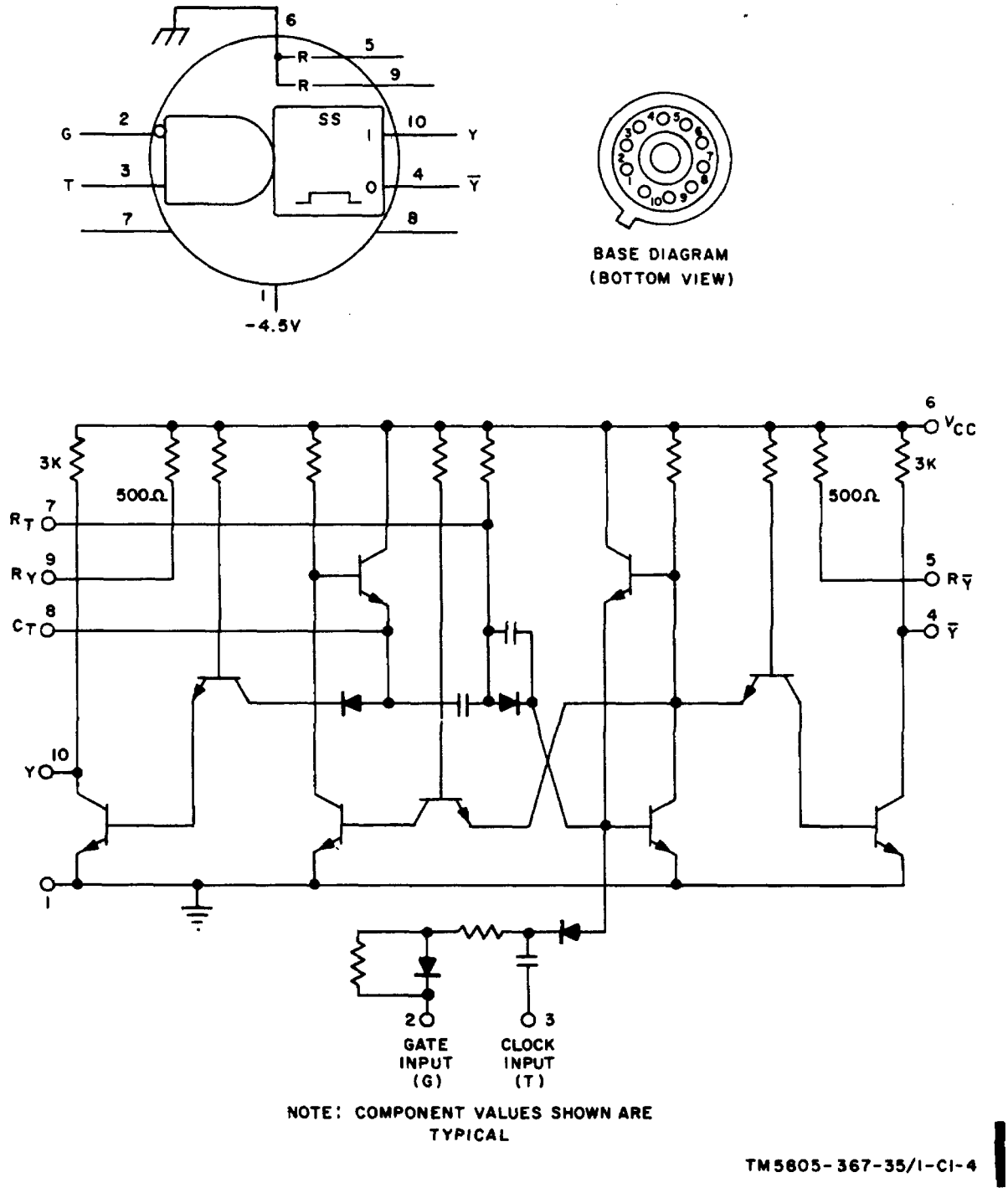


Figure 2-4.4. Monostable multivibrator integrated circuit module (SE161K), basic application and schematic diagram"

Section III. PANEL SCHEMATIC ANALYSIS

2-9. General

a. In 48- (12-) channel operation, the TD-203/U (TD-202/U) accepts a pcm signal with timing from a transmitting multiplexer or another multiplexer, samples and reshapes the pcm signal, and provides a full-width, binary video signal to modulate a radio transmitter. The multiplexers also accept a band-limited binary video signal from the radio receiver, regenerate the pcm signal, and recover the timing.

b. In 96- (24-) channel operation, the TD203/U (TD-202/U) accepts two pcm signals from two transmitting multiplexers, or other multiplexers, and interleaves them, bit by bit, to provide a video channel signal to the radio transmitter. The interleaved pcm signal contains full-width binary pulses at twice the original bit rate. In addition, the TD-203/U (TD-202/U) accepts a band-limited biternary video signal from the radio receiver, regenerates the pcm signal, and recovers the timing. The multiplexers, through the address-detection process, separate the regenerated binary signal into two pcm signals, identify them, and recover the radio order-wire from the video signal.

c. The chart below indicates the plug-in panels used in the TD-202/U and TD-203/U and also provides a brief functional description of each panel.

	Panel number		
Panel	TD-203/U	TD-202/U	Function
Power supply	4A1 /5A1	4A1/6A1	Receives 115 vac; rectifies and produces regulated-4.5-vdc, +4.5-vdc, +10-vdc, -12-vdc, and 28-vac unregulated output for the plug-in panels.
Transmit No.1	4A10		Panels 4A10 and 4A2 operate together to process one or two pcm input trains from multiplexers. Automatically phases and synchronizes two inputs for interleaving. Supplies binary output for radio operation. Panel 5A2 provides the same function for TD-202/U.
Transmit No.2	4A2		
Transmitter		5A2	
Receiver	4A3	5A3	Recovers radio signal; reshapes and retimes pcm input. Converts biternary 96-or 24-channel operation to binary.
Timing No 1	4A4	5A4	These panels operate together to provide timing signals for binary and biternary operation.
Timing No.2	4A5	5A5	
Timing No. 3	4A6/5A6	4A6/5A6	Provides 8-kc address signals to operate panel 4A8/5A8; also provides output timing signals.
Timing No. 4	4A9		Provides timing signal to operate panel 4A8/5A8.
Order wire	4A7/5A7	4A7/5A7	Recovers order wire for use with radio equipment.
Detector framing	4A8/5A8	4A8/5A8	Locates 4-kc framing pulse; divides 96 channel output into two 48-channel outputs or 24-channel output into two 12-channel outputs.
Extender panel			Used for DS and GS maintenance troubleshooting purposes.

2-10. Power Supply Panel 4A1/5A1 (fig. 6-20)

a. General. Power supply panel 4A1/5A1 contains four regulated rectifier power supplies which provide dc outputs of +10 volts, +4.5 volts, -4.5 volts, and -12 volts. An unregulated ac output of 28 volts is also provided for use in the alarm circuits. Each of the dc outputs is regulated by a series regulator transistor, controlled by an electronic sensing and feedback circuit located on subassembly A1. With the exception of the -12-volt supply, the feedback circuit consists of a breakdown diode regulator, differential amplifier, and an emitter-follower driver. The -12-volt regulator consists only of series regulator transistor Q13 with a controlled base bias determined by the breakdown diodes.

b. +10-Volt Supply The +10-volt supply is connected to secondary winding 3, 4, 5 of transformer T1. Full-wave rectifier CR1, CR2 is connected across the secondary and provides a dc output which is filtered through inductor L1A and capacitor C1. The filtered output is applied through fuse F1 and series regulator Q1 to the load. Transistor Q1 acts as a variable resistance in series with the load, which maintains the load voltage at 10 volts. The 10-volt output is monitored across potentiometer R1 and applied to the base of transistor Q3. Transistor Q3 is one-half of a differential amplifier which also includes transistor Q4. The differential amplifier compares the monitored output voltage with the regulated output of breakdown diode VR1. Any variations in the load voltage, caused by variations in the load voltage, caused by variations in the input or in the load, are detected in the differential amplifier, amplified and inverted, and are applied through emitter-follower driver Q2 to the base of series regulator Q1. This causes the series resistance of Q1 to change, keeping the output voltage constant.

c. +4.5-Volt Supply. The +4.5-volt supply is identical with the +10-volt supply except for part values and the breakdown diode circuit. In the +4.5-volt supply, the breakdown voltage of the diode is divided across voltage divider R14, R15 to supply the reference voltage to differential amplifier Q7, Q8.

d. -4.5-Volt Supply. Since the -4.5-volt supply operates into a heavier load than the other supplies, power rectifiers CR5 and CR6 are mounted on chassis heat sinks. In addition, the collector supply for the differential amplifier and driver stages is provided by a separate rectifier-filter consisting of diodes CR7 and CR8, and capacitor C11.

2-11. Transmitter Panel 5A2 (fig. 6-28)

a. General. Transmitter panel 5A2 combines two single binary 12-channel trains into one binary train during 24-channel interleaved (24I) or separated (24S) operation. When used as a radio repeater (24R), the incoming binary train from a companion TD-202/U is regenerated and applied to the next radio. During 12-channel operation, the incoming single binary train is regenerated and applied to the next radio.

b. PCM IN-1 Signal. The PCM IN-1 signal enters panel 5A2 at terminal 30 of jack J6. Wave forms of the incoming PCM IN-1 signal are shown in figure 2-5 and 2-6. The duration of each pulse is 1.736 usec, During 12-channel operation, the PCM IN-1 signal consists of a single binary train of pulses (A, fig. 2-5) .

During 24-channel operation, the PCM IN-1 signal consists of a single interleaved binary or double binary train of pulses (C, fig. 2-6). The pulse excursion is between 0 volt and -2 volts. An amplitude of 0 volt represents a logic 1, and -2 volts represents logic 0. In the panel, the PCM IN-1 signal enters the sampler PCM 1N-1 circuit ((1) below), where the logic 1 pulses are separated from the

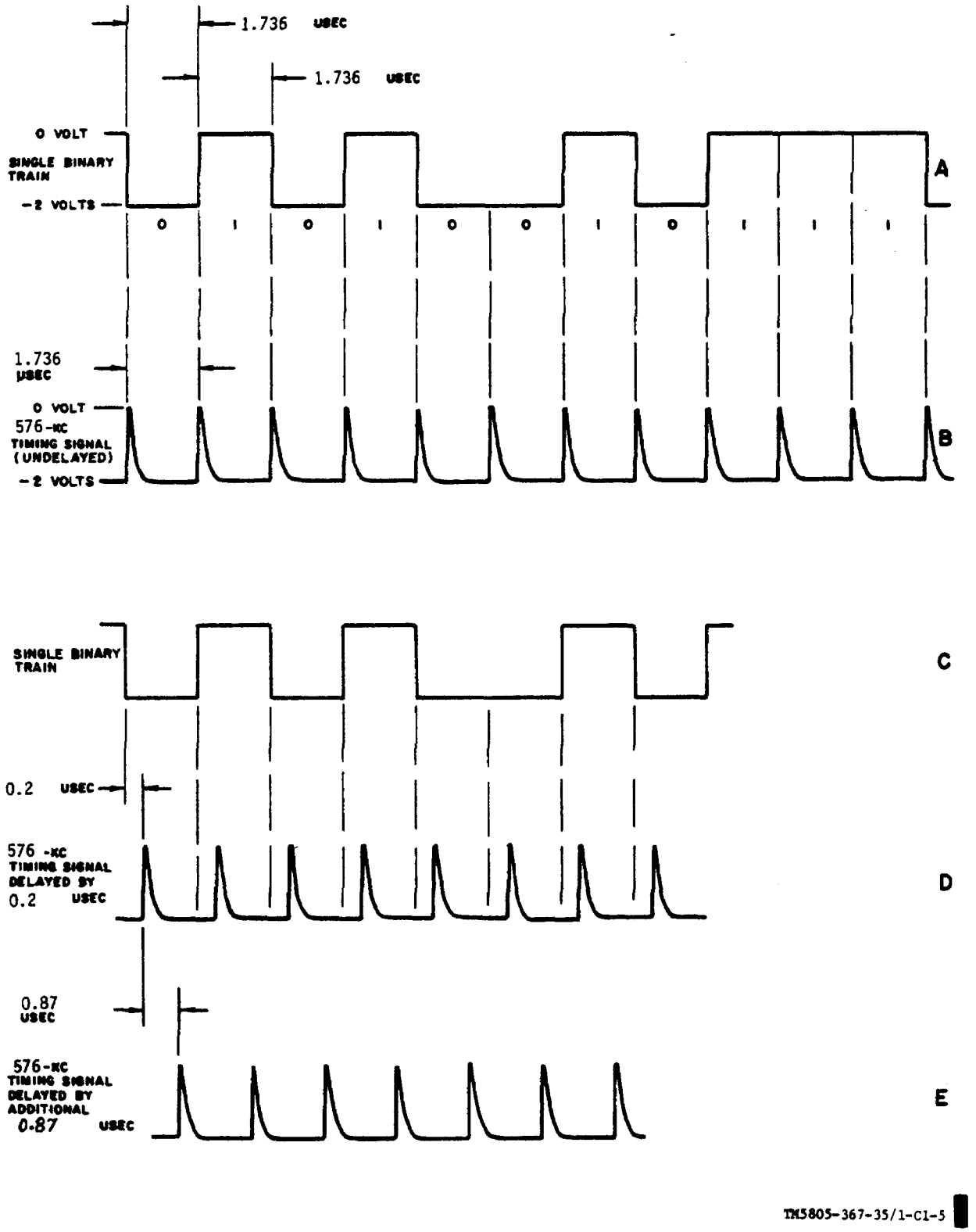


Figure 2-5. Panel 5A2 12- channel operation, waveforms.

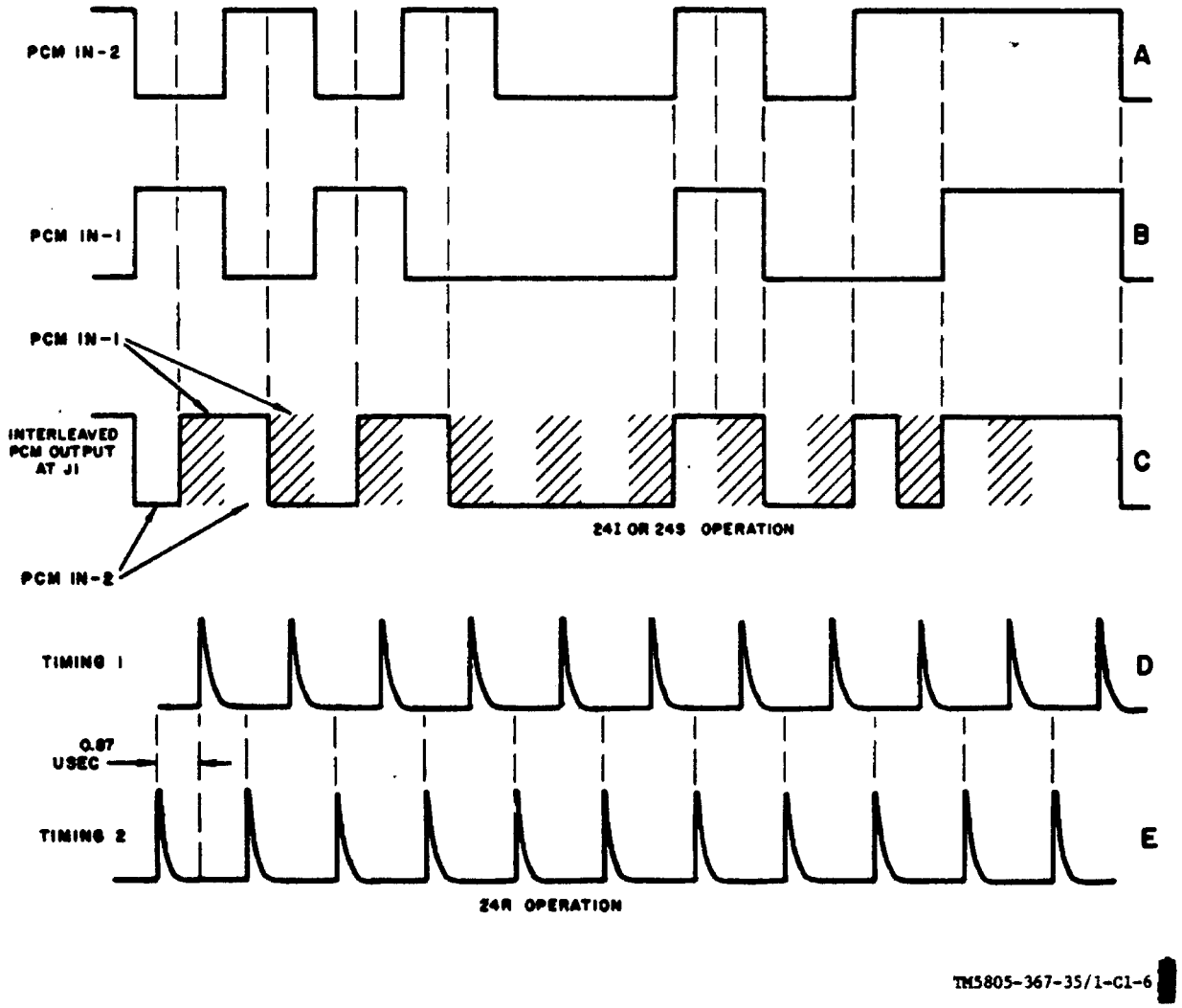


Figure 2-6. Panel 5A2 24- channel operation, waveforms

logic 0 pulses and applied on separate lines to set and reset the PCM pulse reshaper (*e* below which reconstitutes the original PCM IN-1 signal.

(1) *Pcm in-1 circuit*. The pcm in-1 circuit consists of a sampler, detector-inhibitor, and gate. Two signal inputs, PCM IN-1 and TIM IN, are required for the operation of the pcm in-1 circuit.

(a) Pcm in-1. The PCM IN-1 signal from terminal 30 of jack J6 is applied to the base of transistor Q1 of the sampler pcm in-1 circuit ((3) below), and via peak detector capacitor C2 and diode CR4 to capacitor C4. The charge on capacitor C4 is applied to the base of transistor Q5 of the pcm in-1 detector inhibitor circuit ((b) below), and to terminal 29 of jack J6 (PCM IN-1 meter); this signal is used for monitoring.

(b) Timing in. The TIM IN signal at terminal 31 of jack J6 (B, fig. 2-5) is a train of negative-going trigger pulses applied to the base of inhibitor transistor Q3. This signal is derived from the emitter of buffer transistor Q17 of the timing-in circuit (e below).

(2) *Pcm in-1 inhibitor*. The pcm in-1 inhibitor circuit prevents the timing signal input to the sampler pcm in-1 circuit

when there is no PCM IN-1 signal input. This circuit consists of a peak detector (transistors Q3, Q4, and Q5) whose output controls the sampler pcm in-1 circuit.

(a) Normal operation. Transistor Q3 conducts whenever a negative-going pulse enters the base. The biasing for the base of transistor Q4 is developed from the PCM IN-1 signal applied to capacitor C2. The signal passes through capacitor C2, and the upper level of the signal is clamped to ground potential by diode CR2. When the peaks of the negative-going pcm pulses exceed the potential at the anode of diode CR4, diode CR4 conducts and charges capacitor C4 with a negative potential equal to the peak voltage of the pcm pulses. The negative voltage is applied to the base of transistor Q5, cutting it off. With transistor Q5 off, the base of transistor Q4 assumes a + 4. 5-volt potential. The negative-going trigger pulses at the base of transistor Q3 are more negative than the potential at the base of transistor Q4, and transistor Q3 conducts.

(b) Inhibiting operation. When there is no pcm input at capacitor C2, capacitor C4 loses its negative charge and transistor Q5 conducts. The collector of transistor Q5 goes to approximately 0 volt, which is applied to the base of transistor Q4. The base of transistor Q4 become" more negative than the peak negative voltage at the base of transistor Q3; consequently, transistor Q4 conducts and transistor Q3 shuts off, inhibiting any output at the collector of transistor Q3.

(3) *Sampler pcm in-1 circuit*. The sampler pcm in-1 circuit consists of transistors Q1 and Q2 which operate as a differential amplifier. The input for the base of transistor Q1 is a voltage-type b as provided by the PCM IN-1 signal from terminal 30 of jack J6. The input for the base of transistor Q2 is a voltage-type bias of approximately -1 volt provided by voltage divider R7 and R8. The current input to the emitters of transistors Q1 and Q2 is a 576-kc timing signal (E, fig. 2-5) from the collector of transistor Q3. The sampler circuit separates the logic 1 pulses from the logic 0 pulses and applies the pulses on separate lines to set and reset a pcm pulse reshaper that reconstitutes the original PCM IN-1 signal. The logic 1 and 0 pulses are applied to the bases of driver transistors Q9 and Q10, respectively, of the pcm pulse reshaper (e below).

c. Pcm In-2 Signal. The PCM IN-2 signal, enters panel 5A2 at terminal 2 of jack J6. Waveforms of the incoming PCM IN-2 signal are shown in figure 2-6. The duration of each pulse is 1.736 μsec. During 24-channel interleaved 24I or separated 24S operation, the PCM IN-2 signal is A single binary train of pulses (A, fig. 2-6) . During 24-channel repeater (24R) operation of the TD-202/U, the PCM IN-2 signal consists of a single interleaved binary or double binary train of pulses (C, fig. 2-6).

(1) *Pcm in-2 circuit*. The pcm in-2 circuit consists of the inhibitor, sampler pcm in-2, automatic phase control, and inverter. The operation of the inhibitor, sampler pcm in-2, and inverter circuits is described below; the automatic phase control is described in f below. Two inputs, PCM IN-2 and TIM IN, are required for the operation of the pcm in-2 circuit.

(a) Pcm in -2. The incoming PCM IN-2 signal from terminal 2 of jack J6 is divided into two branches. One branch of the signal is applied through capacitor C22 to diodes CR27 and CR26. The signal is clamped to ground by diode CR 27, peak-detected by diode CR 26, and a negative charge is stored on capacitor C24 . One branch of

the charge on capacitor C24 is applied to the base of transistor Q20 of the pcm in-2 inhibitor circuit ((2) below). The other branch of the charge on capacitor C24 is applied to terminal 8 and 9 of jack J6 (PCM IN-2 meter); this signal is used for monitoring. The other branch of the PCM IN-2 signal is applied to the automatic phase control circuit (f below). In the automatic phase control, the PCM IN-2 signal follows one of two branches, depending on the phasing. One branch is via diodes CR17 and CR15 to the bass of transistor Q21. The other branch passes through delay circuit DL3, where the signal is delayed 0.4 μsec, and diodes CR18 and R20 to the base of transistor Q21.

(b) Timing in. The incoming TIM IN signal is delayed 0.2 μsec for use as a timing signal in the sampler pcm in-2 circuit. This timing signal is derived from the emitter of buffer transistor Q17 of the timing-in circuit (d below) and is divided into two branches. One branch, *24-channel timing*, is applied to terminal 5 of jack J6. The signal re-enters the panel via the front panel TRAFFIC SEL switch at terminal 7 of jack J6, where it is designated as *24-channel sample timing*, and is applied to the base of transistor Q18 of the pcm in-2 inhibitor circuit ((2) below). The other branch is from the emitter of transistor Q17 applied to coincidence circuit CR22 and CR23 of the automatic phase control circuit (*f* below).

(2) *Pcm in-2 inhibitor*. The pcm in-2 inhibitor circuit disables the sampler pcm in-2 circuit when there is no PCM IN-2 signal. This circuit consists of a peak-detector (transistors Q18, Q19, and Q20) whose output controls the sampler pcm in-2 circuit. Two inputs, pcm in-2 and 24-channel sample timing, are required for the operation of this circuit. The negative voltage proportional to the negative peaks of the PCM IN-2 signal from capacitor C24 is applied to the base of transistor Q20. The incoming 24-channel sample timing signal from terminal 7 of jack J6 is applied to the base of transistor Q18. The pcm in-2 inhibitor circuit operates in the same manner as the pcm in-1 inhibitor circuit (b (2) above).

(3) *Sampler pcm in -2 circuit*. The sampler pcm in-2 circuit consists of transistor Q7 and Q8. The PCM IN-2 signal input for the sampler pcm in-2 circuit is taken from the collector of transistor Q21 of the automatic phase control (f below). The PCM IN-2 signal is inverted in transistor Q21 and inverted again in transistor Q7. The 24-channel sample timing signal for the sampler pcm in-2 circuit is taken from the collector of pcm in-2 inhibitor transistor Q18 and applied to the emitters of transistors Q7 and Q8. The signal is derived from one of the output branches of the emitter of buffer transistor Q17 of the timing-in circuit (d below). Another branch of the emitter of transistor Q17 is delayed 0.87 μsec for use as a 24-channel timing signal, in the sampler pcm in-1 circuit. The delay places the timing pulse for pcm in-1 for one-half bit apart from the pcm pulses of pcm in-2, so that the pulses of the PCM IN-1 signal occur midway between those of the PCM IN-2 signal. The sampler pcm in-2 circuit operates in the same manner as the pcm in-1 circuit (b (8) above). Logic 0 pulses are produced at the collector of transistor Q7 which is connected to the line carrying the pcm in-1 logic 0 pulses. The logic 0 pulses of both signal trains, with equal spacing, enter the base of driver transistor Q10 of the pcm pulse reshaper circuit (d below). The logic 1 pulses are produced at the collector of transistor Q8, which is connected to the line carrying the pcm in-1 logic pulses.

The pulses of both signal trains enter the base of driver transistor Q9 of the pcm pulse reshaper circuit. However, before the pcm in-1 pulses enter the pcm pulse reshaper, the pcm in-2 pulses are injected into the circuits carrying the pcm in-1 pulses. The pcm in-2 pulses are phased to fall between the pulses of pcm in-1. The interleaved combination enters the pcm pulse reshaper as one train to produce one binary pcm train (C, fig. 2-6).

d. Timing-In Circuit. The timing signal is derived from the TIM IN signal which enters the panel at terminal 31 of jack J6. In the panel, the TIM IN signal is applied to timing-in circuit DL2, Q16, and Q17. The signal passes through delay line DL2 where it is delayed 0.2 μsec (D, fig. 2-5) . The purpose of the delay is to shift the timing pulse so that it does not coincide with the edges of the pcm wavetrain (C, fig. 2-5) during the sampling process. If the timing pulse should occur at a sloping (leading or trailing) edge, it is possible that the timing pulse would not be able to reach its full amplitude to trigger the circuit. To avert such a possibility, the timing pulse is shifted away from the edge toward the center of the pcm wavetrain. The delayed timing signal passes through capacitor C9 to the base of amplifier transistor Q16, where the pulses are reshaped and inverted. The negative-going trigger pulses are applied through buffer transistor Q17 and are divided into four branches. One of the branches of the timing signal is applied to the anode of diode CR23 in the coincidence circuit of the automatic phase control (f below). Another branch is applied to terminal 5 of jack J6 *(24-channel timing)* for application to sampler pcm in-2 via TRAFFIC SEL switch S5 and terminal 7 of jack J6. These two signal branches are used during 24- channel operation; the third branch is applied through delay line DL1 and capacitor C1 to the based of transistor Q3. The fourth branch of the emitter output of transistor Q17 is applied to diode CR12 where the signal is detected and a negative charge is stored on capacitor C10 . This direct-current (dc) voltage is applied through resistor R43 to terminal 4 of jack J6 (TIMING IN meter); this signal is used for monitoring. The timing signal is delayed 0.87 μsec by line DL1 (E, fig. 2-5). This delay, which shifts the timing pulses by one-half bit, is not actually required for 12- channel operation. However, it is necessary to keep the timing pulses for sampler pcm in-1 one-half bit apart from those for sampler pcm in-2 during 24-channel operation.

e. Pcm Pulse Reshaper. The pcm pulse reshaper circuit converts the logic 1 and 0 pulses of the sampler circuit or circuits to square-wave pcm. The circuit consists of flip-flop Q11, Q12, Q13, and Q14.

(1) *Inputs.* The logic 1 and 0 pulses from the sampler circuit (or circuits) are applied to the base of driver transistors Q9 and Q10, respectively. The logic 1 pulses from the emitter of transistor Q9 are applied through diode CR6 to the collector of flip-flop transistor Q12. The logic 0 pulses from the emitter of transistor Q10 are applied to the collector of flip-flop transistor Q13.

(2) *Flip-flop*. The flip-flop consists essentially of transistors Q12 and Q13. Each of these two transistors operates in conjunction with another transistor as a differential amplifier. Transistors Q11 and Q12 act as one differential amplifier; transistors Q13 and Q14 act as another differential amplifier.

(a) Initial status It is assumed that transistor Q12 of the flip-flop is off. With transistor Q12 off, transistor Q13 conducts, as in a conventional flip-flop, and transistor Q11 conducts, as in a differential amplifier. When transistor Q13 is on, transistor Q14 is off. Because of this, the potential at the collector assumes the -4.5-volt value of the upper end of collector resistor R29. This -4.5volt potential is applied to the base of buffer transistor Q15 as a logic 0 representation.

(b) Application of logic 1 pulse. When a logic 1 pulse is applied to the collector of transistor Q12, it conducts, and transistor Q13 shuts off; transistor Q11 shuts off and transistor Q14 conducts. Because transistor Q14 conducts, the collector of transistor Q14 assumes a ground or 0-volt potential. This potential is applied to the base of transistor Q15 as a logic 1.

(c) Application of logic 0 pulse. When a logic 0 pulse is applied to the collector of transistor Q13, it conducts, and transistor Q12 shuts off. The circuit assumes the same conditions that existed during the initial status. Because transistor Q14 is off, the collector of transistor Q14 assumes a -4.5-volt potential, which is applied to the base of transistor Q15 as a logic 0.

(d) Consecutive application of Similar pulses. If a logic 0 pulse causes transistor Q13 to conduct, application of a second logic 0 pulse has no effect on transistor Q13. The output voltage of transistor Q14 also remains the same for the second pulse.

(3) *Output*. The output of the pcm pulse reshaper is taken from the collector of transistor Q14 and applied to the base of buffer transistor Q15. The signal, with unchanged polarity, is applied across a voltage-dividing network which includes output level (OL) potentiometer R33. Potentiometer R33 is screwdriver adjustable and is used to vary the output level of the pcm signal. The potentiometer output is taken from the arm and applied via terminal 1 of jack J6 to the TO RADIO XMTR connector on the front panel. Another branch of the potentiometer output is converted to a dc voltage by a peak detector and applied to terminal 6 of jack J6 (to radio xmtr meter); this signal is used for monitoring.

f. Automatic Phase Control (apc). The apc (fig. 2-7) shifts the PCM IN-2 signal 0.4 μsec whenever the timing pulses coincide with the transitions of the pcm square-wave pulses. The apc is used during 24I and 24S (disabled during 24R) operation; during 12-channel operation, the apc is disconnected. When the PCM IN-2 signal is suitably phased, it passes through the apc and enters the sampler pcm in-2 circuit where the logic 1's and 0's are separated (c (3) above). Whenever the PCM IN-2 signal is not suitably phased for sampling, a signal is developed in the apc to reroute the PCM IN-2 signal either through the delay line or direct to the sampler, depending on the phase of the signal. To accomplish this delay, the 24-channel timing pulses are compared with pulses representing the negative transitions of the PCM IN-2 signal. If coincidence occurs, the resulting signal is used to change the state of flip-flop Q25 and Q26. This change in state disables the route taken by the PCM IN-2 signal and presents the alternate route which may be direct or delayed (0.4 μsec) in delay line DL3. The apc consists of the differential amplifier, buffer, driver, flip-flop, undelayed and delayed.

(1) *Inputs*. The apc circuit requires two signal inputs for operation: PCM IN-2 and 24-channel timing . The incoming PCM IN-2 signal from terminal 2 of jack J6 is applied to diode CR15 and through 0.4 μsec delay circuit DL3 to the anode of diode CR18. Depending on the phasing, the PCM IN-2 signal connects via one of the two branches to the base of differential amplifier transistor Q21. One branch of the 24-channel timing signal from the emitter of timing-in buffer transistor Q17 is applied to coincidence circuit CR22 and CR23, and R60, where the timing-in pulses are compared with the pulses representing the negative transitions of the PCM IN-2 signal.

(2) *Apc differential amplifier*. The signal (B, fig. 2-7) representing the transitions from pcm in-2 (A, fig. 2-7) is developed in differential amplifier circuit Q21 and Q22. Whenever the pcm signal at the base of transistor Q21 goes from positive to negative, transistor Q21 conducts and transistor Q22 shuts off. The signal at the collector of transistor Q21 passes on to the sampler as the principal signal.

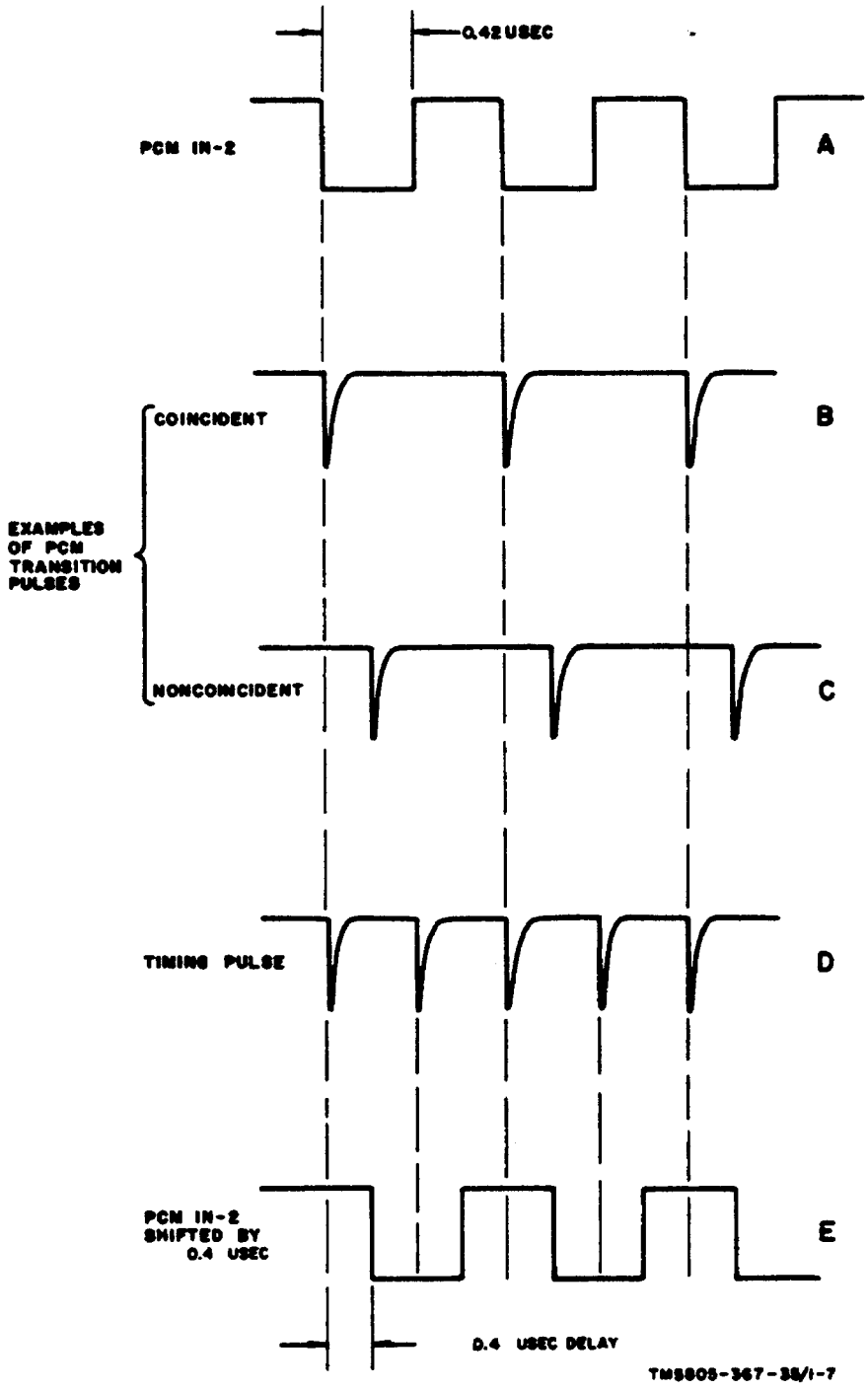


Figure 2-7. Panel 5A2 automatic phase control, waveforms.

When transistor Q22 shuts off, B spiked pulse is developed across coil L2; diode CR21 dampens the oscillation. The negative-going pulses pass through capacitor C20 and are applied to the base of buffer transistor Q23. The negative signal at the emitter of transistor Q23 is applied to diode CR22 of the coincidence circuit ((3) below).

(3) *Apc coincidence circuit*. The coincidence circuit consists of diodes CR22 and CR23 and resistor R60. The timing signal for the coincidence circuit, a train of negative-going pulses at a 576-kc rate, is taken from the emitter of buffer transistor Q17 and applied to diode CR23 . The coincidence circuit is energized by the -4.5-volt source applied to one end of resistor R60. The other end of resistor R60 is connected to the junction of diodes CR22 and CR23 and the base of transistor Q24. When there are no incoming signals, current flows in resistor R60 and the potential at the common point is approximately 0 volt. When a negative pulse arrives at either one of the diode anodes, the diodes receiving the negative pulse tends to shut off, to restrict current flow in this diode branch. Current flow continues in the other diode branch, and the voltage at the common point remains at approximately 0 volt. When each diode receives a negative pulse simultaneously, both diodes shut off to halt current flow in resistor R60 . Since there is practically no voltage drop across resistor R60, the common point assumes a negative potential which causes transistor Q24 to conduct. A positive-going pulse produced at the collector of transistor Q24 is applied to bath sides of flip-flop transistors Q25 and Q26 via diodes CR24 and CR25 . The flip-flop changes state.

(4) *Apc flip-flop*. The flip-flop determines whether the undelayed PCM IN-2 signal or the delayed PCM IN-2 signal is applied to the base of transistor Q21 for eventual application to the sampler pcm in-2 circuit.

(a) Undelayed pcm in-2 signal. Transistor Q25 of the automatic phase control flip-flop is off and transistor Q26 conducts. With transistor Q25 off, gate CR15 and CR 16, and R 54 is able to pass the pcm in-2 signal. The output of the gate is applied to diode CR17 of another gate consisting of diodes CR17 and CR20 and resistor R55. The signal passes through this gate and is applied to the base of transistor Q21. Transistors Q21 and Q22 act as a differential amplifier; when the pcm signal goes negative, transistor Q21 conducts and transistor Q22 cuts off. The PCM IN-2 signal appears at the collector of transistor Q21 with inverted polarity and is applied through resistor R11 to the base of inverter transistor Q6. The signal is inverted again in transistor Q6. The output of transistor Q6 is applied to transistor Q7 of the sampler pcm in-2 circuit.

(b) Delayed pcm in-2 signal. Transistor Q25 of the automatic phase control flip-flop conducts and transistor Q26 is off. The collector of transistor Q25 assumes a potential of approximately 0 volt which is applied to the anode of gate diode CR16. As a result, the pcm at the anode of diode CR15 cannot pass through the gate circuit. With transistor Q26 off, the anode of gate diode CR19 assumes a -4.5-volt potential, permitting the delayed pcm output of delay circuit DL3 (E, fig. 2-7) to pass through gate diode CR18. The signal passes through gate diode CR20 to the base of transistor Q21. However, if the pcm signal phase should drift so that its negative transition coincides with the timing pulse, a pulse is developed in the coincidence circuit to change the state of the flip-flop.

The change in state causes the gates to reverse their status, and the undelayed pcm is connected to the base of transistor Q21. The coincidence circuit changes the state of the flip-flop whenever the pcm signal transitions coincide with the timing pulses.

g. 24-Channel Repeater Operation. When the TRAFFIC SEL switch is operated to 24R, the incoming train is applied, via the front panel PCM IN-1 and PCM IN-2 connectors, to terminals 30 and 2 of jack J6. The binary train enters both samplers, but only a single train is sampled in each sampler. Since the timing signal (D, fig. 2-6) for sampler pcm in-1 is spaced 0.87 μsec from the timing (E, fig. 2-6) for sampler pcm in-2, one timing signal selects the pulses of one of the binary trains and the other timing signal selects the pulses of the other binary train. In the 24R position, the automatic phase control circuit is grounded. This prevents the delayed PCM IN-2 signal from passing through the gate to the base of transistor Q21. The 24 -channel timing signal at terminal 5 of jack 6 is fed back into the panel, via terminal 7 of jack J6, as the 24 -channel sample timing signal. The signal passes through capacitor C12 and transistor Q18 for application to the emitters of transistors Q7 and Q8 of the sampler pcm in-2 circuit.

2-11.1 Transmit No. 1 Panel 4A10

(fig. 6-20.1)

a. General. Transmit No. 1 panel 4A10 sequentially stores the 48-channel (PCM IN-2) binary train for six bits, with no loss of pcm information, during 96-channel interleaved (96I) or separated (96S) operation. Each output from the panel 4A10 storage elements is applied to panel 4A2, where it is read out sequentially at one-sixth of the bit rate. In this manner, the original pcm train is reconstructed and synchronized with the same timing signal. During 96-channel repeater (96R) operation, the PCM IN-2 binary train from a companion TD-203/U bypasses the storage circuits in panel 4A10 and is applied to panel 4A2 for regeneration and application to the next radio. During 48-channel operation, the 4A10 panel elements are inactive.

b. PCM IN-2 Signal. The PCM IN-2 signal enters panel 4A10 at terminal 29 of jack J10; wave forms of a typical incoming PCM IN-2 signal are shown in A of figure 2-7.1. The duration of each pulse is 0.43 μsec. During 96-channel interleaved (96I) or separated (96S) operation, the PCM IN-2 signal is a single binary train of pulses with a duration of 0.22 μsec. During 96-channel repeater (96R) operation, the PCM IN-2 signal consists of a single interleaved binary or double binary train of pulses. The pulse excursion Is between 0 and -2 volts. An amplitude of 0 volt represents a logic 1; an amplitude of -2 volts represents a logic 0. In the panel, the PCM IN-2 signal is separated into 1's and 0's and applied on separate lines as inputs to the reading gates and associated storage elements. Each PCM IN-2 bit is sequentially read in at one sixth of the bit rate, and stored for six bits. Each storage element is read out, at one-sixth of the bit rate, on panel 4A2 where it is combined and synchronized with the PCM IN-1 signal.

(1) *Pcm in-2 circuit*. This circuit consists of the pcm input and timing elements that process, control, and store the pcm-2 signal. The storage circuits are described in c below. Two inputs, PCM IN-2 and TIM IN-2, are required for operation of the pcm in-2 circuit.

(a) Pcm in-2. The incoming PCM IN- signal from terminal 29 of jack J10 is applied to a differential amplifier consisting of transistors Q1 and Q2. The outputs of the differential amplifier are fed to driver transistors Q3 and Q4, respectively. This provides both phases of the pcm signal at the necessary logic levels to operate the integrated circuits. The output of transistor Q3 is applied to the peak detector circuit consisting of transistors Q5 and Q6, capacitors C2 and C3, diodes CR2 thru CR4 and resistor R11. The outputs of driver transistors Q3 and Q4 are coupled to pins 9 and 3, respectively, on read-in gates Z1, Z4, Z7, Z9, Z14, and Z16; and to terminals 11 (PCM-2) and 7 (PCM-2) of jack J10.

(b) Tim in-2. The 2304-kc TIM IN-signal is applied to terminal 31 of J10 through delay line DL1, where it is delayed 0.2 μsec. The purpose of this delay is to shift the timing pulse so that it does not coincide with the edges of the pcm wavetrain during the sampling process.

The delayed timing signal is applied to differential amplifier transistors Q9 and Q10. The output of transistor Q10 is applied to driver transistor Q11 and a peak detector consisting of transistors Q7 and Q8, diodes CR6 and CR7, capacitor C9, and resistor R16. The output of transistor Q11 is applied to one-half of driver Z6 to provide a basic timing pulse train for panel 4A10. The output of driver Z6 branches into two outputs. One branch is applied to a counter comprising flip-flops Z11, Z12, and Z13. The other branch is applied to the toggle inputs of flip-flops Z2, Z5, Z8, Z10, Z15, and Z17. Outputs from pin 8 of flip-flops Z12 and Z13 are applied to pins 3 and 4 of gate Z3. The output of this gate is coupled back to pin 2 of counter flip-flop Z11. This results in a divide-by-6 counter.

(2) *Pcm-2 inhibitor*. The pcm-2 inhibit pulse is derived when either of the peak detected pcm-2 or tim-2 outputs from transistors Q6 and Q8 fail to appear at pins 7 and 8 of gate Z3. This causes a high dc level at terminal 18 of jack J10 (pcm-2 inhibit). This signal is used in 96-channel operation to inhibit the C2 timing pulse (pare 2-11. 2b (2)), if there is a failure of the pcm-2 or tim-2 pulse trains. This essentially causes panel 4A2 to operate in a 48-channel mode. The output of transistor Q6 is also coupled via resistor R13 to output terminal 21 of jack J10 (PCM IN-2 meter); this signal is used for monitoring. The output of peak detector transistor Q8 is also coupled, via resistor R19, to terminal 19 of jack J10 (TIM IN-2 meter); this signal is used for monitoring.

c. Read-in and Storage Circuits. The output from pin 8 of flip-flop Z11 is applied to pins 5 and 8 of gate Z7 and pins 4 and 7 of gate Z1. The output from pin 3 of flip-flop Z11 is applied to pins 5 and 8 of gate Z16 and pins 4 and 7 of gate Z9. The output from pin 8 of flip-flop Z12 is applied to pins 4 and 7 of gate Z4 and pins 5 and 8 of gate Z9. The output from pin 3 of flip-flop Z12 is applied to pins 4 and 7 of gate Z14 and to pins 6 and 8 of gate Z1. The output from pin 3 is also applied to a pulse shaper consisting of transistor Q12, resistors R27 and R28, and capacitor C13. This pulse shaper forms a positive pulse at the collector of transistor Q12 when the Wave form at pin 3 of flip-flop Z12 makes a transition from ground to-4.5 volts. The output of transistor Q12 is applied to terminal 20 of jack J10 (read-in bracket pulse). The output from pin 8 of flip-flop Z13 is applied to pins 5 and 8 of gate Z14 and pins 4 and 7 of gate Z7. This signal is also applied to pin 9 of flip-flop Z11. The output from pin 3 of flip-flop Z13 is applied to pins 4 and 7 of gate Z16 and 5 and 8 of gate Z4. Gate Z1 is normally inhibited by the inputs from the counter. This produces logic 1's at pins 2 and 10. These are applied to pins 2 and 9 of storage flip-flop Z2. When the outputs are at logic 1, the 2,304-kc timing pulse will have no effect on the state of flip-flop Z2. When the inputs from the counter are simultaneously at logic 1, the read-in gate is enabled. The outputs applied to pin 2 and pin 10 of flip-flop Z1 will be the inverse of the complementary pcm inputs, at pins 3 and 9, respectively, for the duration of one clock period (0.43 μsec). The toggle pulse (H, fig. 2-7.1) will then set flip-flop Z2 according to the state of the pcm inputs. The output from pin 8 of flip-flop Z2 is applied to terminal 4 of jack J10 (S1). When gate Z1 has been enabled for the one period it will be disabled by the counter pulses for five clock periods. Therefore, flip-flop Z2 will change state at a maximum of once every six clock pulses. Read-in gates Z4, Z7, Z9, Z14, and Z16 and the associated storage flip-flops Z5, Z8, Z10, Z15, and Z17, respectively, operate in a similar manner, except the gates are enabled in a sequential fashion. In this manner, each pcm bit is stretched for a duration of six clock bits (B through G. fig. 2-7.1) and no pcm information is lost. The read-in bracket pulse is coincident with the time the pcm input is read into storage flip-flop Z2.

2-11.2. Transmit No. 2 Panel 4A2 (fig. 6-21)

a. General. Transmit No. 2 panel 4A2 provides the readout pulses to reconstruct the 48-channel pcm-2 binary train from the storage elements on panel 4A10, and combines this pcm train with the 48-channel pcm-1 train in

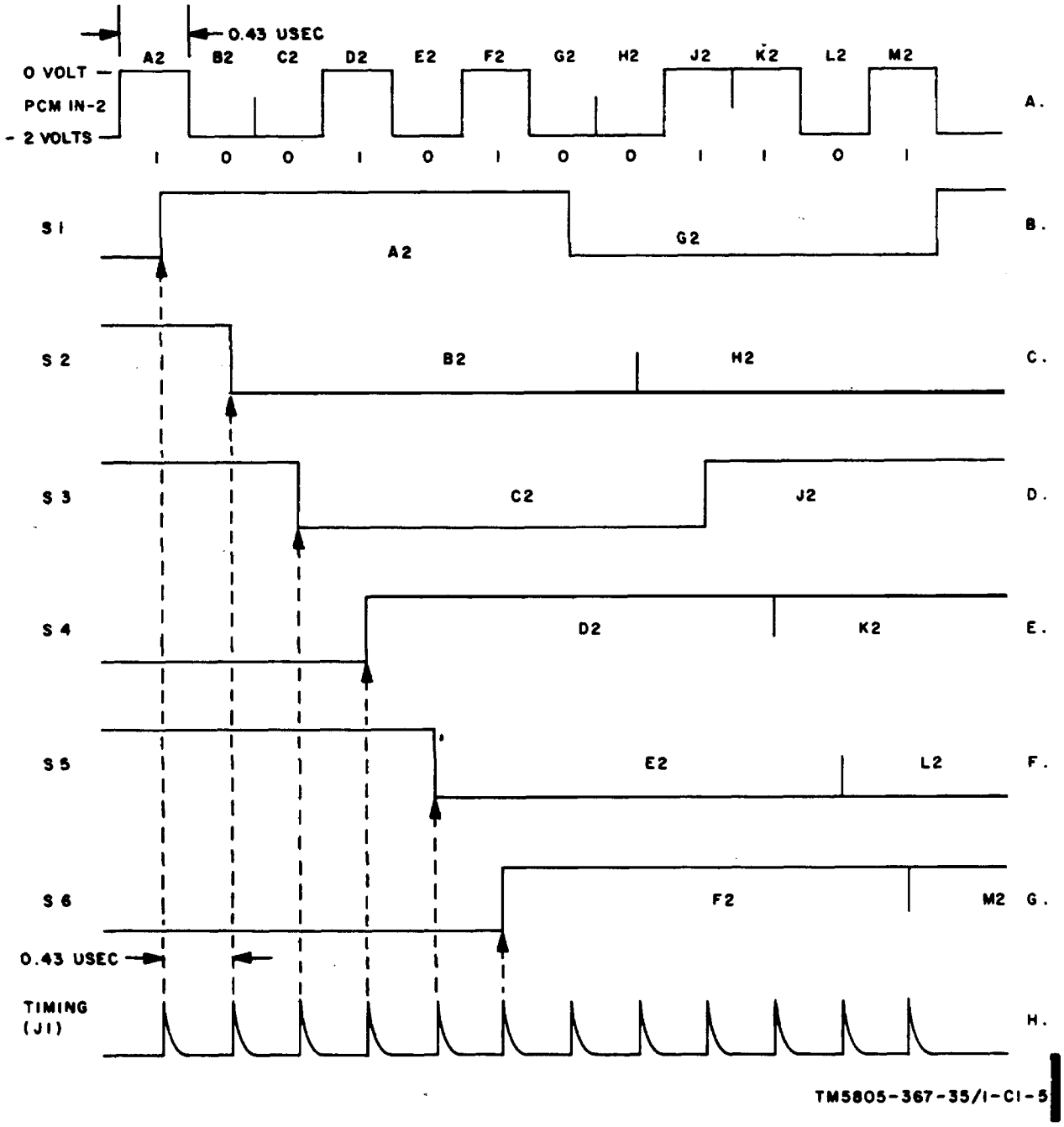


Figure 2-7.1. Panel 4A10 storage of idealized pcm 2 waveforms during 96I-or 96S -channel operation.

96-channel interleaved (961) or separated (96S) operation. This signal is then applied to the next radio.

b. Pcm In-1 Signal. The PCM IN-1 signal enters panel 4A2 at terminal 16 of J15; waveforms of the incoming PCM IN-1 signal are shown in A of figure 2-7.2. During 96-channel interleaved (961) or separated (96S) operation, the PCM IN-1 signal is a single binary train of pulses (A, fig. 2-7.2). The duration of each pulse is 0.43 μsec. During 96-channel repeater (96R) operation, the PCM IN-1 signal consists of a single interleaved binary or double-binary train of pulses

(B, fig.2-7.2) with a duration of 0.22μsec. The pulse excursion is between 0 and -2 volts. An amplitude of 0 volt represents a logic 1; an amplitude of -2 volts represents a logic 0. In the panel, the PCM IN-1 signal is separated into 1's and 0's and applied on separate lines as inputs to the output flip-flop control gates. The output from these gates reconstitutes the original PCM IN-1 signal.

(1) *Pcm in-1 circuit*. The pcm in-1 circuit consists of the pcm input and timing elements that process and control the pcm-1 signal up to the output control circuits. The output control circuits are described in *c* below. Two inputs, PCM IN-1 and TIM IN-1, are required for operation of the pcm in-1 circuit.

(a) Pcm in-1. The incoming PCM IN- signal from terminal 16 of J15 is applied to a differential amplifier consisting of transistors Q9 and Q10. The outputs of the differential amplifiers are fed to driver transistors Q11 and Q12, respectively. This provides the necessary logic levels for use with the integrated circuits. The output of transistor Q11 is applied to pin 7 of gate Z15. The output of transistor Q12 is applied to pin 3 of gate Z7 and to the base of transistor Q13, which acts as a buffer emitter follower. The output from the emitter is coupled through capacitors C11 and C16 and diodes CR8 and CR9 to constitute a peak detector circuit which activates transistor Q15. The output of transistor Q15 is also applied to pin 9 of gate Z15 and to pin 5 of gate Z7. This output is also fed through resistor R24 to terminal 17 of jack J15 (PCM IN-1 meter); this signal is used for monitoring. When failure of the PCM IN- occurs, the dc output from transistor Q15 inhibits the output flip-flop control gates processing the PCM IN-1 signal.

(b) Tim in-l. The 2,304-kc TIM IN-1 signal from terminal 29 of jack J15 is applied to differential amplifier transistors Q1 and Q2. The output from transistor Q1 is used to produce the C1 clock pulse (*b*(2) below). The output from transistor Q2 is coupled to transistor Q3. The output from transistor Q3 is coupled through buffer emitter follower transistor Q4. One output from the emitter of this 2-16.2 transistor branches to a peak detector consisting of capacitors C2 and C3 and diodes CR2 and CR3. The dc voltage from this peak detector is applied to transistor Q6. The collector of transistor Q6 is coupled through resistor R12 to terminal 20 of jack J15 (TIM IN-1 meter); this signal is used for monitoring. The other branch from the emitter of transistor Q4 is used to produce the C2 clock pulse (*b* (2) below) .

(2) *Timing pulses C1 and C2*. Timing pulses C1 and C2 (fig. 2-7. 2) are derived from the TIM IN-1 signal (*b*(1) (*b*) above). These signals are used for sampling the pcm-1 and *pcm-2* signals from output flip-flop control gates Z7 and Z15, respectively. Timing pulse C2 also controls the sampling of the *pcm-2* signals from read-out gates Z10, Z12, and Z14. The TIM IN-1 output from differential amplifier transistor Q1 is fed through 0. 1-usec delay line DL1 to the base of transistor Q5. The output from transistor Q5 is the clock pulse designated as C1. The TIM IN-1 output, from the emitter of buffer transistor Q4, is applied to pin 3 of single-shot multivibrator Z4 which is used as a timing delay circuit. The delay is adjustable with variable capacitor C7. The output from single-shot multivibrator Z4 is applied via a differentiating pulse shaper network, consisting of capacitor C5 and resistor R18, to the base of transistor Q7. The output from transistor Q7 is a positive pulse at the dc levels necessary for operation of the integrated circuits. This signal is applied to pin 5 of gate Z5 and to pin 10 of flip-flop Z9. The output from pin 2 of gate Z5 is coupled to pin 7 of gate Z5. This half of gate Z5 acts as an inverter driver for the clock pulse designated as C2. This pulse, at the 2,304-kc rate, is adjustable by capacitor C7 to fall midway between the C1 clock pulses. From pin 10 of gate Z5, this pulse is applied to pin 10 of counter flip-flops Z1, Z2, and Z3. This signal is also applied to pin 7 of gate Z8.

c. Readout and Output Control Circuits. The divide-by-6 counter comprises flip-flops Z1, Z2, and Z3 and provides the necessary waveforms for the readout gates. The feedback output from pin 2 of gate Z6 forces the

shift register type counter to count by six. The outputs from pin 8 of flip-flops Z2 and Z3 are fed to pins 3 and 4, respectively, on gate Z6. The output from pin 2 of gate Z6 is fed back to pin 2 of flip-flop Z1. The output from pin 8 of Z3 is also coupled to pin 9 of Z1. This provides the necessary feedback for the divide-by-6 counter. Gates Z10, Z12, and Z14 are the readout gates for the storage elements located on panel 4A10. The six stored outputs (S1 through S6) from panel 4A10 are applied to terminals 4, 2, 8, 5, 9, and 3, respectively, on jack J15. The S1, S2, and S3 are applied to pin 3 of gates Z10, Z12, and Z14, respectively. The S2, S4 and S6 signals are applied to pin 7 of gates Z10, Z12, and Z14, respectively. Therefore, there is one readout gate for each storage element on the 4A10 panel. The proper gating waveforms are supplied from the panel 4A2 counter stage. The gating waveforms for the S1 signal are applied from pin 8 of flip-flop Z1 and pin 3 of flip-flop Z2 to pins 4 and 5, respectively, on gate Z10. The gating waveforms for the S2 signal are applied from pin 8 of flip-flop Z2 and pin 3 of flip-flop Z3 to pins 8 and 9, respectively, on gate Z10. The gating waveforms for the S3 signal are applied from pin 8 of flip-flops Z3 and Z1 to pins 4 and 5, respectively, on gate Z12. The gating waveforms for the S4 signal are applied from pin 3 of flip-flop Z1 and pin 8 of flip-flop Z2 to pins 8 and 9, respectively, on gate Z12. The gating waveforms for the S5 signal are applied from pin 3 of flip-flop Z2 and pin 8 of flip-flop Z3 to pins 4 and 5, respectively, on gate Z14. The gating waveforms for the S6 signal are applied from pin 3 of flip-flops Z3 and Z1 to pins 8 and 9, respectively, on gate Z14. The outputs of all the readout gates, pins 2 and 10, are connected. Therefore, each gate is sequentially sampled for the duration of one clock pulse (0. 43 μsec) in a manner similar to the reading pulses. One common output of the readout gates is connected to pin 7 of gate Z13; the other is applied to pin 7 of gate Z6 which acts as an inverter. The output at pin 10 of gate Z6 is applied to pin 3 of gate Z11. Gates Z7; Z11A, Z13B, and Z15 are the output flip-flop control gates that process the pcm from the storage elements. Gates Z11B and Z13A make up the output flip-flop.

d. 48-channel Operation. The low level signal applied from the TRAFFIC SEL switch to terminal 1 of jack J15 (961 and 96S) inhibits gates Z11A and Z13B at pins 5 and 9. Therefore, the C1 pulses sample the pcm-1 signal in gate Z7A and the pcm-1 signal in gate Z15B. The output from pin 2 of gate Z7 is connected to pin 7 of gate Z11B. The output from pin 10 of gate Z15B is connected to pin 5 of gate Z13A. When the pcm-1 signal is at logic 1, and the clock pulse C1 is present, the output at pin 10 of Z7 is a negative going pulse. This is applied to pin 7 of flip-flop Z11 and forces pin 10 to a level 1. The output at pin 10 of Z15 remains a logic 1 because the pcm-1 is now at level 0; therefore, the input to Z13 pin 5 is a logic 1. The logic 1 level at pin 3 of Z11 and the logic 1 input at pin 5 of Z15 causes the output from pin 2 of gate Z13 to be at logic 0. When the pcm-1 signal is at logic 0 and the pcm-1 signal is at logic 1, this action is reversed and the output flip-flop changes state. The output from the flip-flop is taken from pin 10 of Z11 and applied to buffer output driver transistor Q14. The output from the emitter of transistor Q14 is connected through resistor R43 and the output level adjust potentiometer R44 to a peak detector consisting of capacitors C19 and C20 and diodes CR11 and CR12. The signal is applied to terminal S1 of jack J15 (TO RADIO XMTR meter) for monitoring. The center tap of the potentiometer is connected to terminal 30 of jack J15 (TO RADIO XMTR).

e. 961- or 96S-Channel Operation. In these modes of operation the *pcm-2* output flip-flop control gates are enabled by the dc level from the TRAFFIC SEL switch applied to terminal 1 of jack J15 (961 and 96S). This is now a high level. Readout gates Z10, Z12, and Z14 are sequentially sampled and the outputs are tied together to form a serial signal similar to output at jack J14 (A, fig. 2-7. 2). The complement of this signal is derived by inverting the signal in gate Z6B. The *pcm-2* and *pcm-2* signals from terminals 11 and 7 of jack J15 are applied to gates Z7B and Z15A, respectively. These are sampled by the C2 clock

pulse. The outputs of these gates are tied to the respective pcm-1 gates and to the output flip-flop. Therefore, a coincidence of the timing pulse C2 and a pcm signal that is at level 1 produces a negative pulse and sets the output flip-flop in a manner similar to that described for 48-channel operation. To avoid the possibility of reading out from the storage element when a pcm bit is being read in, the *read-in bracket pulse*, discussed in paragraph 2. 11. 1c is compared with the readout pulse for the storage of signal S1. The *read-in bracket pulse* is applied through terminal 13 of jack ,J15 to pin . 5 of gate Z8. To derive the readout pulse for the S1 signal storage element in gate Z10, pin 8 of Z1 is connected to pin 8 of Z8. Pin 3 of Z2 is connected to pin 9 of Z8 and the clock pulse C2 is connected to pin 7 of Z8. The output from pin 10 of Z8 is connected to driver transistor Q8. Therefore, the output at the collector of transistor Q8 is a positive pulse occurring at the time when the storage element S2 signal is being read into the flip-flop with clock pulse C1. This output is applied to pin 4 of gate Z8. When a coincidence occurs between the *read-in bracket pulse* and the readout pulse for storage signal S1, a negative-going pulse is formed at the output of gate Z8, pin 2. This pulse is applied to the clear-direct input, pin 4, of flip-flop Z9. This places the output at pin 3 of flip-flop Z9 into a level 0 state and inhibits gate Z5A. This output is also applied to pin 2 of Z9, the set level input. When the next clock pulse from the collector of transistor Q7 appears, there is no output at pin 2 of gate Z5 and the gate is inhibited by the 0 level at pin 4. However, this output is also applied to pin 10 of flip-flop Z9, the toggle input, and the state of the Z9 flip-flop is inverted. Therefore, pin 4 will go to its normal 1 state, the next clock input to gate Z5A will enable it, and the next clock pulse will pass through unaffected. However, if there still is a coincidence of the *read-in bracket pulse* and the readout pulse, this action will be repeated until no coincidence exists between these pulses. If there should be a failure of the PCM IN-2 or TIM IN-2 train in 96-channel operation, a high dc level is applied to terminal 19 of jack J15 (*pcm-2 inhibit*). This signal is applied to pin 2 of single-shot multivibrator Z4. This high level essentially inhibits the C2 timing pulse, and the operation of panel 4A2 becomes similar to that for 48 channels.

f. 96R-Channel Operation. For 96R operation the inputs to the panels are at the interleaved rate, 4,608 kc, and there is no need to use the storage scheme employed in 96I and 96S operation. A low dc level at terminal 1 of jack J15 (961 and 96S), from the TRAFFIC SEL switch, is applied to pin 9 of gate Z13 and pin 5 of gate Z11. This inhibits the readout flip-flop control gates of the storage elements. A high level at terminal 12 of jack J15 (96R sel) is applied to pin 5 of gate Z15 and pin 9 of gate Z7. Another input to pin 7 of gate Z7 is the *pcm-2* signal from terminal 11 of jack J15. The pcm in-1 signal via terminal 16 of jack J15 is applied to pin 7 of gate Z15. The PCM IN-1 and Pcm IN-2 inputs are identical (B, fig. 2-7. 2), since they are derived from a single source outside the TD-203/U. The pcm-1 signal is sampled by the C1 clock pulses, while the *pcm-2* signal is sampled by the C2 clock pulses. Since these pulses occur at the 2,304 kc rate, and are interleaved when combined, they effectively sample the pcm at the 4,608 kc interleaved rate. The output flip-flop is set and reset at this rate as in interleaved operation, except that the Acme signal is derived directly from panel 4A10, instead of via the storage elements.

2-12. Receiver, Panel 4A3 (5A3) (figs. 6-22 or 6-29)

a. General. Receiver panel 4A3 (5A3) receives and processes the pcm and order-wire signals. The receiver panel performs the actual regeneration of the pcm signal and aids in recovering the order wire from the composite radio signal. Panel 4A3 (5A3) essentially consists of the following circuits: video amplifier, clamp, peak detector, and decision circuit.

(1) *48- (12-) channel operation*. During 48- (12-) channel operation, the principal input signal is a filtered binary signal at a 2,304-kc (576-kc)

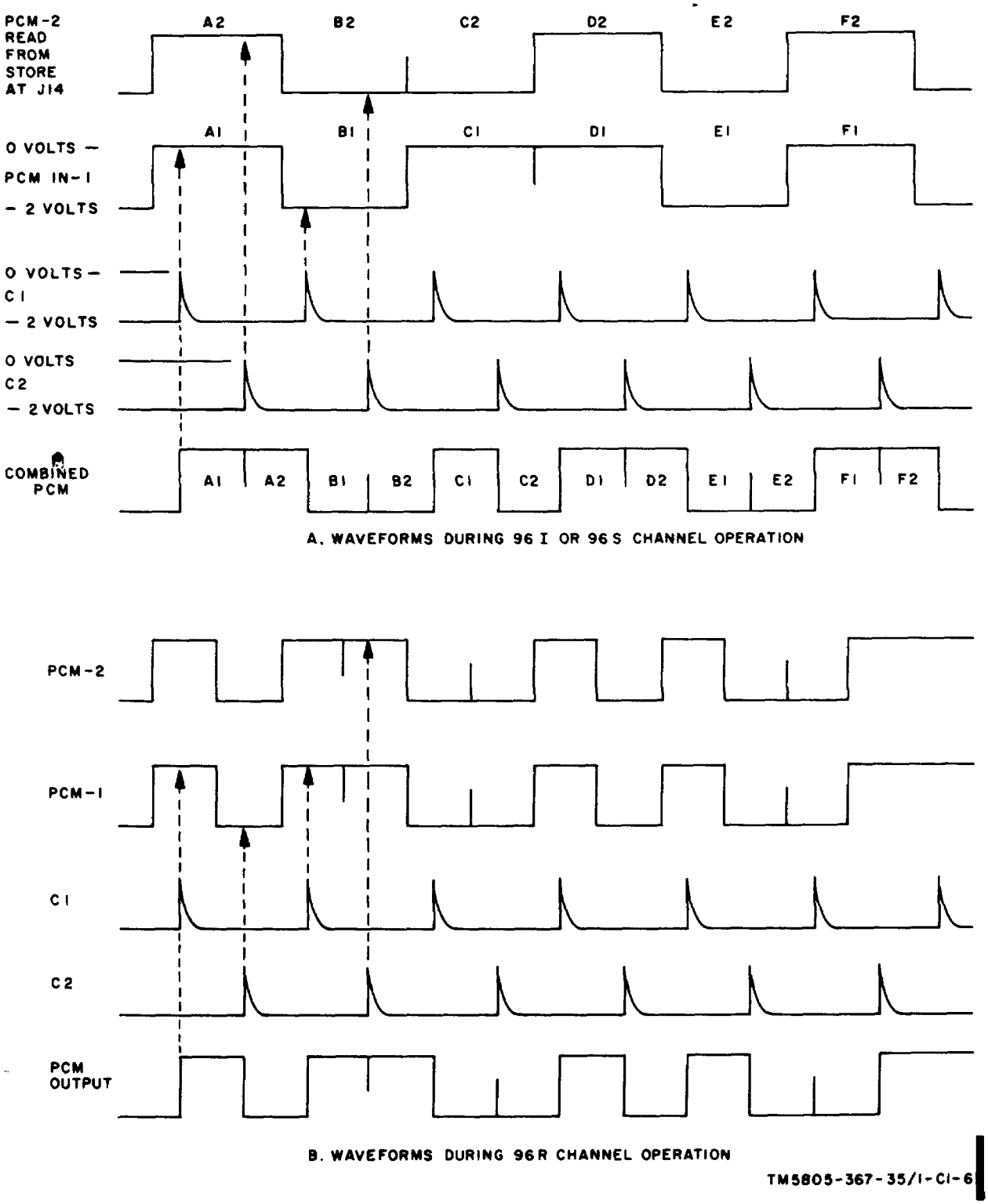


Figure 2-7.2. Panel 4A2 idealized waveforms during 96I- or 96S-, and 96R-channel operation

rate. The *from radio rcvr* signal enters the panel at terminal 2 of jack J8 and is applied to the video amplifier circuit (b below) and to terminal 8 of jack J8 (*rcvd radio signal*). In addition, two dc input signals of the same level (*decision level No. 1I* and *decision level No. 2*) and a 2,304-kc (576-kc) timing signal (*decision timing*) enter the panel at terminals 11, 12, and 24, respectively. These signals are applied to the decision circuits (*e* below).

(2) *96- (21-) channel operation*. During 96- (24-) channel operation, panel 4A3 (5A3) operates in the same manner as for 48-channel operation. However, the principal signal input is a filtered binary signal and the frequency of both the *from radio rcvr* and decision timing signals is 4,608 kc (1,152 kc). Also, the do levels of the *decision level No. 2* signal inputs to the decision circuits are not the same.

b. Video Amplifier Circuit. The video amplifier consists of transistors Q1 through Q4. The incoming from radio rcvr signal from terminal 2 of jack J8 is applied through RL potentiometer R2, which is used to adjust the level of the incoming signal, to the base of transistor Q4. The collector output of transistor Q4 is coupled back through a low-frequency compensation network (capacitor C5 and transistor Q3) to the emitter of transistor Q4. The emitter output of transistor Q4 is divided into two branches. One branch is applied through a high-frequency compensation network to the emitter of transistor Q1. The high-frequency compensation network, consisting of capacitor C4, resistors R7 and R8, and inductor L1, shapes and stabilizes the frequency response and gain of the video amplifier. The other branch of the emitter output of transistor Q4 is applied through capacitor C36 (C6) as a low-impedance driver input to the clamp circuit (c below).

c. Clamp Circuit. The clamp removes the order-wire signal from the composite signal. The pcm remaining after the order wire has been removed is applied to the stages that follow. The order-wire signal (A, fig. 2-8)is originally added to the pcm (B, fig. 2-8) at the distant radio set to produce the composite signal (C, fig. 2-8). The clamp circuit consists of diodes CR1 and CR2 and transistors Q5,Q6, and Q7.

(1) *Operation*. When the amplitude of the composite signal attempts to rise above the positive voltage at the junction of diode CR1 and capacitor C6(C7), diode CR1 conducts to prevent the rise. When the composite signal attempts to fall below the negative voltage at the junction of diode CR2 and capacitor C7 (C8), diode CR2 conducts to limit the negative excursion. The upper and lower limits are established by the potential across resistor R18. When the diodes are not conducting, a voltage drop is developed across resistor R18.

(2) *Outputs*. The *from radio rcvr* signal without the order wire is applied to the base of transistor Q5. Transistors Q5, Q6, and Q7 minimize loading of the clamp circuit by the stages that follow. The pcm signal is taken from the emitter of transistor Q7 and divided into five branches: one branch is peak-detected and applied as a monitoring output (*from radio rcvr meter*) to terminal 7 of jack J8; another branch (*clamped radio*) is applied as an output to terminal 9 of jack J8. The remaining branches of the clamped circuit output are applied to the bases of transistors Q30 and Q34 of the peak-detector circuits (d below) and to the bases of transistors Q8 (Q10) and Q28 of the decision circuits (*e* below).

d. Peak-Detector Circuits. Transistor Q30 is the initial stage for the positive peak detector; transistor Q34 is the initial stage of the negative peak detector. In these circuits, the upper and lower limits of the pcm signal are used to establish a single dc signal (binary level) during 48- (12-) channel operation, or two dc levels (*ternary pos level and ternary neg level*) during 96-(24-) channel operation. The positive peak detector establishes an upper voltage level to represent an amplitude average of the positive-going peaks of the pcm signal waveform. The negative peak detector establishes a lower voltage level to represent an amplitude average of the negative-going pulses. The two circuits are similar; however, the negative peak detector basically differs from the positive peak detector in that diodes CR19 (CR20) and

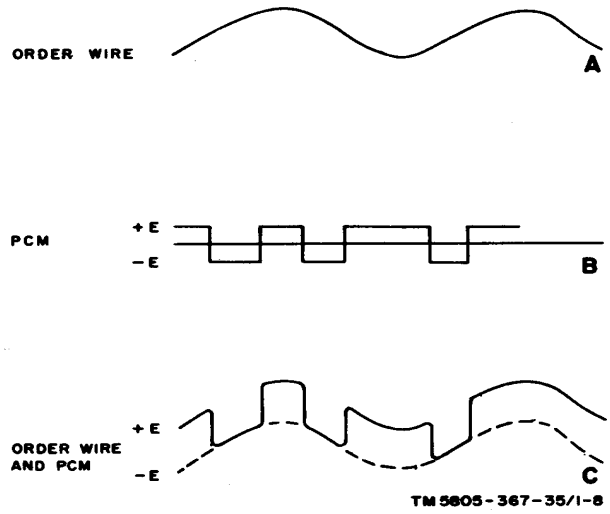


Figure 2-8. Composite signal (pcm and order-wire) waveforms

CR20(CR21) are reversed and, in some cases, resistance values and biasing points also differ.

(1) *Positive peak detector*. The positive peak detector consists of transistors Q30 through Q33. Transistors Q30 and Q32 act as a differential amplifier that constantly compares the incoming pcm signal with its positive peak voltage. The input for the base of transistor Q30 is the pcm signal. Normally, the base of transistor Q30 is more negative than that of transistor Q32; as a result. transistor Q30 conducts and its collector is positive. If the peak of the pcm signal goes more positive than the base of transistor Q32, the emitter current is switched to the emitter of transistor Q32. This causes the collector of transistor Q30 to go negative, thus permitting transistor Q31 to conduct. The collector of transistor Q31 goes to 0 volt. When the pcm returns to a more negative level than the base of transistor Q32, transistor Q30 again conducts and drives transistor Q31 to cutoff. The collector of transistor Q31, in turn, goes from 0 volt to -4. 5 volts.

(2) *Peak-detector outputs*. The dc output of the positive peak detector is taken from the emitter of transistor Q33 and applied to voltage-dividing network R83(R82), R85(R84), and R87(R86); to voltage dividing network R84 (R83) and R86 (R85) . and through resist A" R82 (R81) to terminal 31 of jack J8 as a monitoring signal, designated ternary positive level meter (SF(A)). The dc output of the negative peak detector is taken from the emitter of transistor Q37 and applied to the opposite ends of the two voltage dividing networks, and to terminal 30 of jack J8 as a monitoring signal, designated *ternary neg level meter* (SF(A)).

(3) Voltage divider outputs. The voltage divider outputs leave panel 4A3 (SA3), but are eventually returned for use in the decision circuits. The center level signal at the arm of CL potentiometer R85 (R84) is applied to terminal 26 of jack J8 (center level). The output of PL potentiometer R84(R83)is applied to terminal 27 of jack J8 (*ternary pos level*). The output of NL potentiometer R86 (R85)is applied to terminal 28 of jack J8 (*ternary neg level*). A dc signal is taken from a point between PL potentiometer R84 (R83) and NL potentiometer R86 (R85) and applied to terminal 29 of jack J8 (*binary level*).

e. Decision circuits. The decision circuits restore the pcm to the condition that existed when the signal was initially transmitted. An idealized waveshape is shown in A, figure 2-9. When the pcm is transmitted over the radio, the higher frequencies are filtered and the corners rounded off (B, fig. 2-9). This waveshape is designated as filtered pcm, because the higher frequencies have been effectively filtered by the radio. Also, as the signal passes through the transmission media and the receiver, noise is picked up on the pcm (C, fig. 2-9). To restore the pcm signal to its original condition, the two decision circuits sample the signal and produce pulses which are applied to a flip-flop to reproduce the transmitted signal. One decision circuit produces the logic 1 pulses and applies them to one side of the flip-flop; the other decision circuit produces the logic 0 pulses and applies them to the other side of the flip-flop. The decision circuit which produces logic 1 pulses consists of transistors Q8 through Q13, as shown in figure 2-10. The pcm signal output of the clamp circuit is applied to the base of transistor Q8 (Q10). The decision timing signal from terminal 24 of jack J8 (*decision timing*) is applied

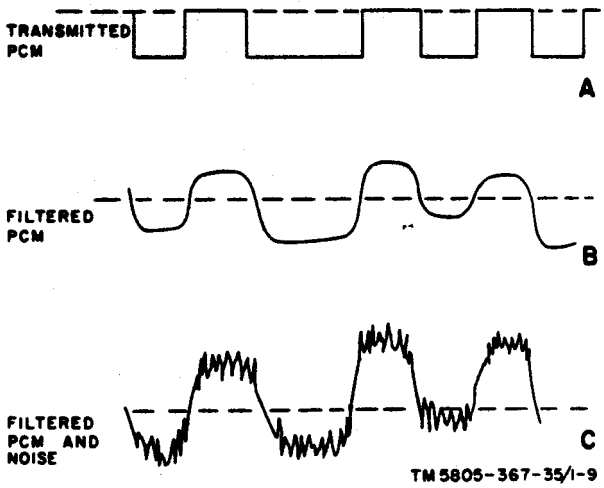


Figure 2-9. Typical pcm waveforms.

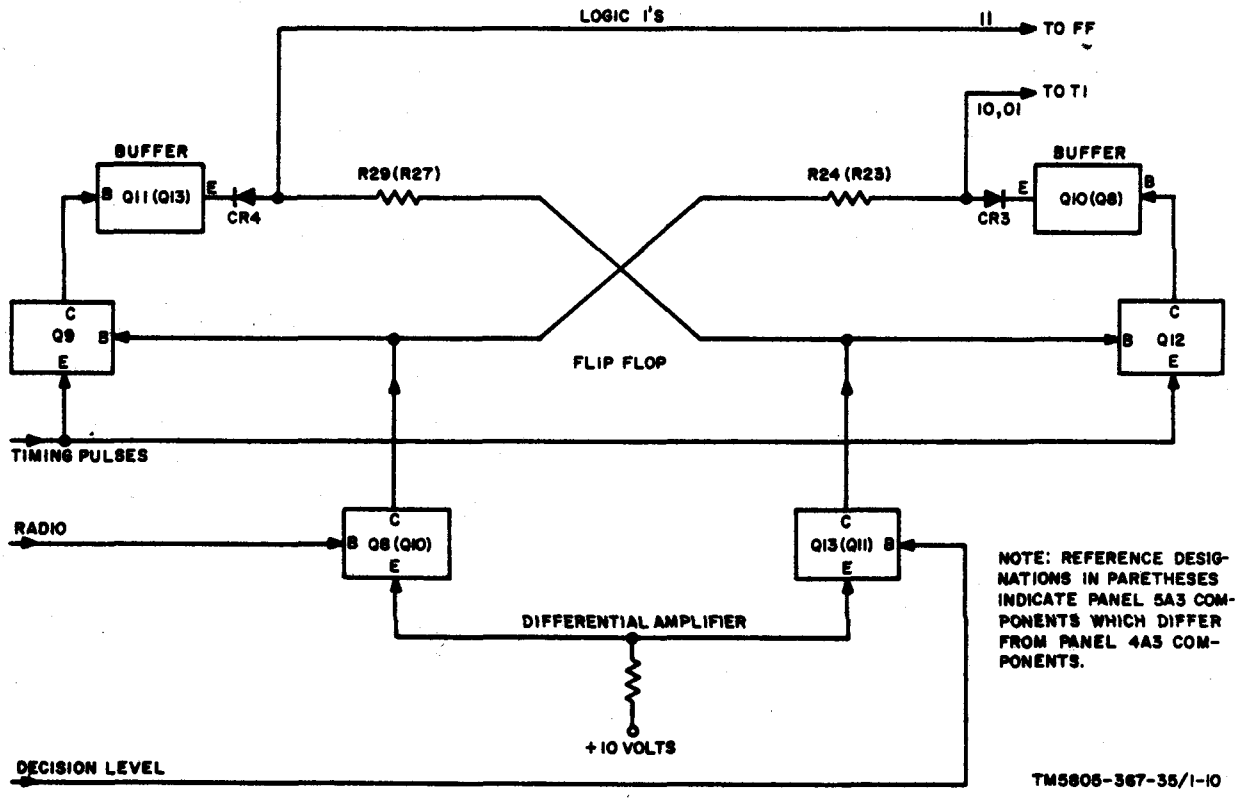


Figure 2-10. Pane! 413 (543) decision circuit, block diagram.

through amplifier transistor Q14 (Q20) to the emitter of transistors Q9 and Q12. The decision level No.1 signal from terminal 11 of jack J8 is applied to the base of transistor Q13 (Q11). During 48-(12-) channel operation, the same signal is fed to the other decision circuit via terminal 12 of jack J8 as decision level No.2. During 96- channel operation, however, two different decision levels are used. The circuit that produces logic 0's operates in a similar manner.

(1) *Operation*. Transistors Q8 (Q10) and Q13 (Q11) operate as a modified differential amplifier; the voltage at the base of transistor Q13(Q11) is constant, and the voltage at the base of transistor Q8 (Q10) varies with the pcm signal. This circuit compares the pcm signal with the decision level signal. When the amplitude of the pcm signal is more positive than the decision level, transistor Q13 (Q11) conducts; when less positive, transistor Q8 (Q10) conducts. As a result, the pcm signal is sliced; the upper half of the waveform appears at one collector, and the lower half appears at the other collector. The signal is sliced to assure that the pulses are definitely of one polarity or the other before they are sampled in the succeeding stages. Any pulses of dubious polarity could upset the operation of transistors Q9 and Q12, which operate as a flip-flop. The outputs of transistors Q8 (Q10) and Q13 (Q11) are applied to each side of flip-flop transistors Q9 and Q12. To prevent loading, transistors Q1O (Q8) and Q11 (Q13) are inserted in the feedback circuits to act as buffers (fig. 2-lo). The states of the flip-flop are governed by the inputs to the flip-flop bases from the collectors of transistors Q8 (Q10) and Q13 (Q11). The timing pulses at the emitters of transistors Q9 and Q12 appear at the collectors of Q9 or Q12 and pass through buffer transistor Q10 (Q8) or Q11 (Q13) as feedback signals and as outputs. A conventional flip-flop produces

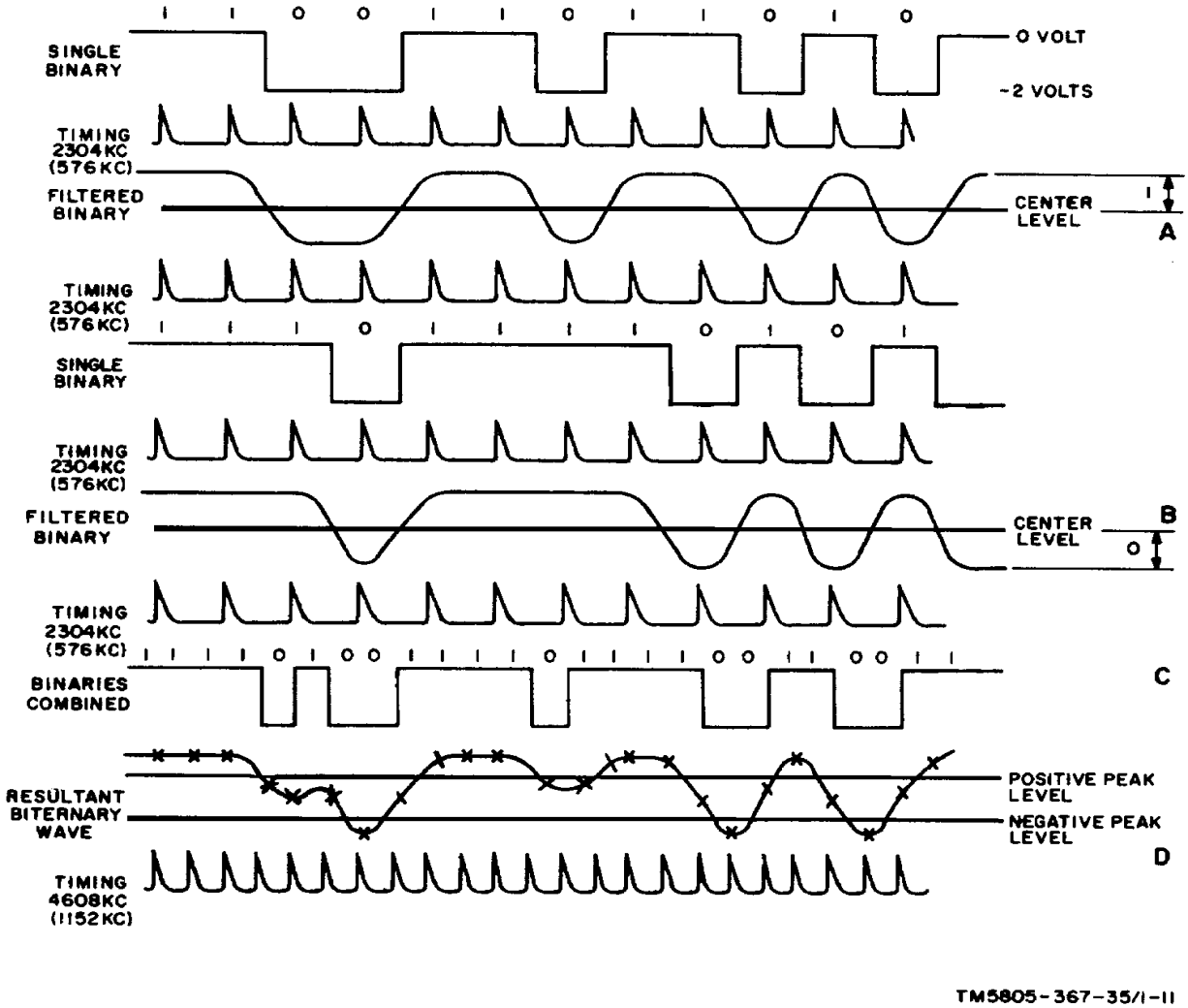
square-wave outputs, but the decision circuit produces pulsed outputs.

(2) *Outputs*. The logic 1 pulses are produced at the emitter of transistor Q11 (Q13) when the pcm signal is positive With respect to the decision level at transistor Q8 (Q10). They are clamped to ground by diode CR5 (CR8), and applied through amplifier transistor Q15 (Q16) to one side of flip-flop Q18 (Q17) and Q20 (Q19). The logic 0 pulses are furnished by the second decision circuit. The logic 0 pulses are developed at the emitter of transistor Q24, when the pcm signal is negative with respect to the decision level at transistor Q27. They are clamped to ground by diode CR9 (CR12) and applied through amplifier transistor Q21 to the other side of the flip-flop.

f. Flip-Flop Circuit. Transistors Q15, Q18, Q20, and Q21 (Q16, Q17, Q19, and Q21) form a modified flip-flop circuit, which operates in a manner similar to that of a pcm pulse reshaper (pare 2-11). This flip-flop circuit converts the logic 1 and O pulses to square-wave pcm. The restored pcm signal (recovered pcm-1) is taken from the collector of amplifier transistor Q15 (Q16) and applied to the base of buffer transistor Q22. The emitter output of transistor Q22 is divided into two branches: one branch, designated *recovered pcm-1*, is applied through dc shifting network R49 (R47) and C17 (C18) to terminal 22 of jack J8; the other branch, designated *recovered pcm-1 meter* (SF(G)), is converted to a dc voltage in a peak-detector circuit and applied as a monitoring output to terminal 25 of jack J8. An inverted restored pcm signal, designated as recovered pcm -2, is taken from the collector of transistor Q21 and applied to terminal 20 of jack J8.

g. Analysis of Biternary Waveform. An example of a single binary wavetrain with its filtered counterpart is shown in A, figure 2-11. The wave excursions, although rounded off, just reach one level or the other during a timing period and dwell long enough above or below the center level for the timing pulses to perform their functions. During the 48- (12-) channel sampling process, the waveform need only be divided into two regions to reproduce the signal. In 96- (24-) channel operation, two binary trains (A and B, fig. 2-11) are interleaved to produce a double binary train (C, fig. 2-11) at twice the rate of the 48- (12-) channel waveform. Therefore, due to the filtering, two consecutive digits (either 11 or 00) are required so that the filtered signal can reach the amplitude extremes. When the porn signal consists of alternate digits (1, 0), the filtered signal falls midway between the extremes, and does not reach the extremes until two consecutive digits occur. Thus, it is the filtering of the binary waveform that produces the biternary, or 3-level, signal in 96- (24-) channel operation. Since the mid region signals occur so close to the center of the extremes, a center-level voltage is insufficient to separate the indefinite pulses. Consequently, in 96- (24-) channel operation, it is necessary to divide the waveform into three regions to reconstruct the original pcm. This is accomplished with the outputs from the positive and negative peak detectors, designated as decision level No. 1 and decision level No. 2. In the decision circuits, biternary waveform excursions (A, fig. 2-12) that rise above decision level No. 1 are separated as logic 1 pulses. The excursions that fall below decision level No. 2 are separated as logic 0's. When the biternary waveform is the center region, the pcm is in transition from its previous state. To separate a mid-region pulse, simultaneous complement pulse outputs of the decision circuits develop a single complement pulse in transistors Q10 (Q8) and Q23. This pulse is applied through transformer T1 to the flip-flop to change it from its previous state. Figure 2-12 shows five possible conditions of the relationship of the input to the output of the two decision circuits. If the pcm contains a row of logic 1 pulses (11), the waveform peak remains in the upper region and can be readily sampled to produce set pulses (A, fig. 2-12). The indefinite complement pulse output of transistor Q23 can perform no action while acting alone. If the pcm signal contains a row of logic 0 pulses (0 0), the waveform peak remains in the lower region and can readily produce reset pulses (E, fig. 2-12). If the waveform (B, fig. 2-12) goes from a logic 1 pulse to a logic 0 pulse (1 0, 0 1), the waveform excursion does not reach the opposite extreme, but falls midway between the extremes. Since the pulse has not fallen in the upper region, it cannot be sampled as a logic 1 pulse, and there is no output at the emitter of transistor Q11 (Q13).

The indefinite complement output of the first decision circuit, however, drives the base of transistor Q10 (Q8) more positive. Since the pulse has not fallen in the lower region, the pulse cannot be sampled as a logic 0 pulse. In addition, there is no output at transistor Q24 of the second decision circuit, but the complement action drives the base of transistor Q23 positive. The emitters of transistors Q10 (Q8) and Q23 are tied together and act in a manner similar to that of the differential amplifier. In this case, however, both transistors must tend to go toward shutoff simultaneously before any useful output is produced. This is accomplished when the two indefinite outputs simultaneously arrive at the bases of the transistors Q10 (Q8) and Q23. The transistors shut of f and the voltage drop across resistor R56 (R54) is reduced, so that a positive pulse is produced. This complement pulse, after passing through transformer T1 and a stage of amplification, is applied to both sides of flip-flop transistors Q18 (Q17) and Q20 (Ql9). The complement pulse changes the flip-flop to its alternate state. If the next pulse is a logic l pulse, the waveform falls again in the mid region (C, fig. 2-12) and the process is repeated. The complement output changes the flip-flop to its alternate state to set the flip-flop. If the next pulse is a logic 0 pulse, the waveform excursion still remains in the mid region (D, fig. 2-12) and the process is repeated. The complement pulse resets the flip-flop. If the next pulse is a logic 0 pulse, the waveform excursion reaches the lower region (E, fig. 2-12) because two logic 0 pulses have occurred in sequence. In this case, a definite logic 0 pulse appears at the output of transistor Q24 and is applied to the flip-flop. The pulse is ineffective, however, because the flip-flop has already been reset by the previous pulse. In this manner, the biternary signal



NOTE: PARENTHESES INDICATE FREQUENCIES USED IN PANEL 5A3 WHICH DIFFER FROM THOSE USED IN PANEL 4A3.

Figure 2-11. Panel 4A3 (5A3) biternary waveforms.

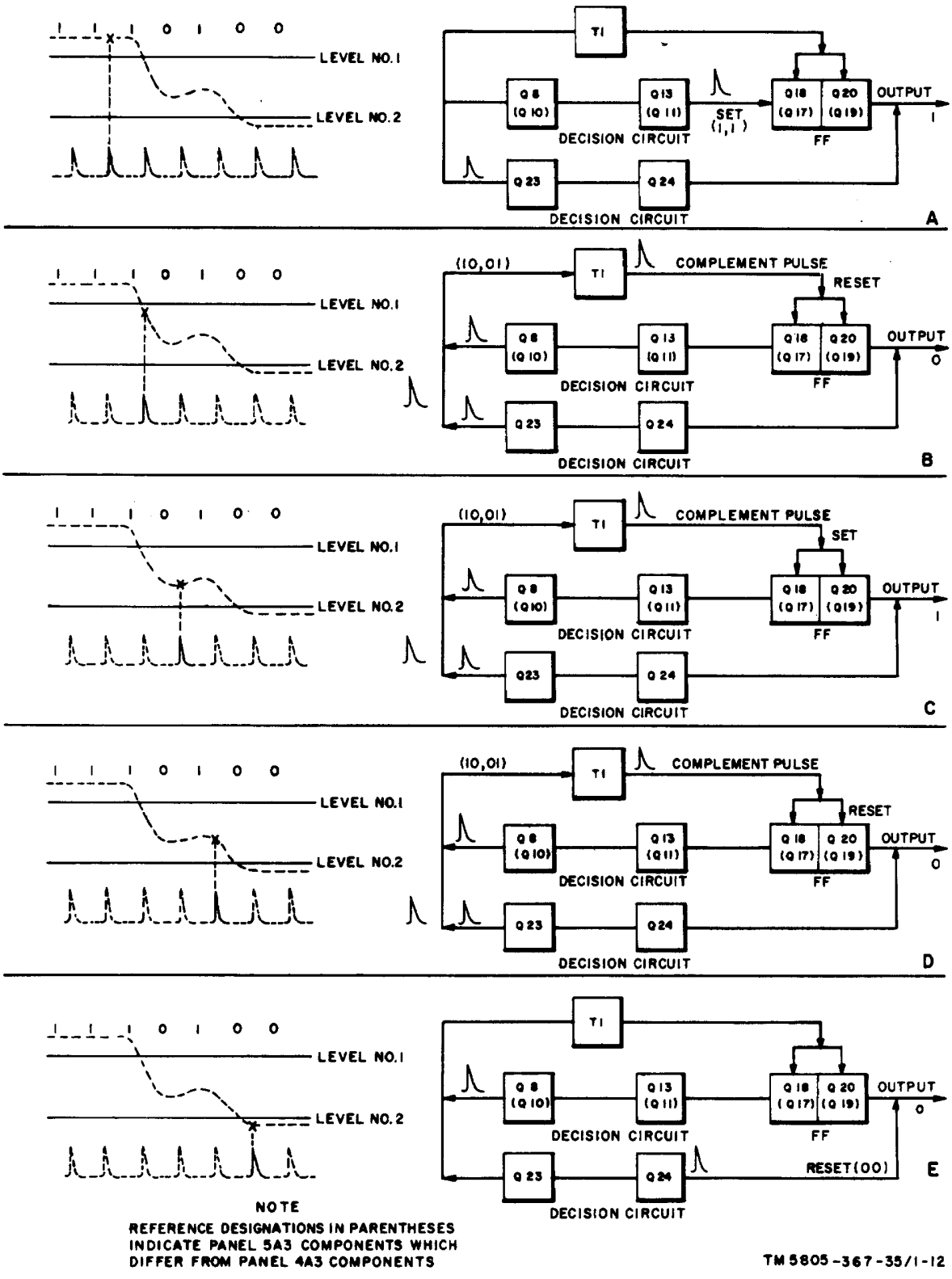


Figure 2-12. Panel 4A3 (5A3) decision circuit, input-output relationships.

converted back to the original interleaved binary waveform.

2-13. Timing Generator No. 1, Panel 4A4 (5A4) (fig. 6-23 (6-30))

a. General. Timing generator No. 1, panel 4A4 (5A4), develops timing signals for use in the receive circuits. The timing signals aid in sampling, regeneration, signal operation, and frequency division in the panels that comprise the receive circuits. To develop the timing signals, a radio signal input is compared with a dc level signal input; the signals are sliced, differentiated, and rectified; shell the resulting timing signals are buffered, amplified, inverted, and delayed before they are applied as outputs from the panel. Panel 4A4 (5A4) consists of the crystal-filter drive, 48(12-) channel timing, traffic-alarm control, and radio signal detector.

(1) *48- (12-) channel operation*. A 2,304-kc (576-kc) single binary pcm train, designated *clamped radio* signal, and a dc *center-level signal*, designated center level, enter panel 4A4 (5A4) at terminals 27 arid 25 of jack J6 (J3), respectively. The incoming clamped radio signal is divided into two branches: one branch is applied through tile crystal-filter drive circuit (*b* below) to the 48- (12-) channel timing circuit (*c* below), and to the traffic-alarm control circuit (*d* below); the other branch is applied to the radio signal detector circuit (*e* below). The incoming center-level signal is also applied to the crystal-filter drive circuit.

(2) *96- (24-) charnel operation*. During 96- (24-) channel operation, the Timing circuits operate in the same manner as for 48- (12-) channel operation. However, the incoming *clamped radio signal* at terminal 27 of jack J6 (J3) consists of a 4,6G8-kc (1,159-kc) single biternary pcm train. In addition, the Outputs at terminals 7 and 13 of jack J6 (J3) are not used during 96- (24-) channel operation. The output at terminal 31 of jack J6 (J3) is used only during the 96- (24-) channel mode of operation.

b. Crystal-Filter Drive Circuit. The crystal filter drive circuit converts the incoming clamped radio signal to spiked pulses for application as a drive signal to the 48- (12-) channel timing circuit. The crystal-filter drive circuit consists of the slicer and differentiation/full-wave rectifier.

(1) *Slicer circuit*. The slicer circuit consists of transistors Q1 through Q I; transistors Q1 and Q2 and transistors Q3 and Q4 operate in pairs, and each pair acts as a differential amplifier. The incoming *clamped radio* signal from terminal 27 of jack J6 (J3) and the incoming *center level* signal from terminal 25 of jack J6 (J3) are applied to the bases of transistors Q1 and Q2, respectively. When the pcm signal level rises above the value of the *center level* signal, transistor Q2 conducts and produces an amplified, clipped, rectangular pulse. When the pcm signal level falls below the value of the *center level* signal, transistor Q1 Conducts and produces an inverted version of the signal out of transistor Q2. The rectangular output pulses from transistors Q1 and Q2 are direct-coupled to slicer transistors Q3 and Q4, respectively. When either transistor Q3 or Q4 conducts, the rectangular pulse output is fed to the differentiator/full-wave rectifier circuit ((2) below)

(2) *Differentiator/full-wave rectifier circuit*. The differentiator/full-wave rectifier circuit consists of coils L1 and L2, resistors R5 and R6, and diodes CR1 and CR2. The differentiator portion of the circuit converts the square-wave pulses to spiked pulses; the rectifier portion of the circuit passes only the negative portions of the spiked inputs. The resulting output is a random train of 2,304-kc (576-kc) timing pulses that are applied to buffer transistor Q5 and then to amplifier transistor Q6. The output pulses of transistor Q6 are delayed 0. 025 μsec (0. 2 μsec) in delay line DL1 and coupled to buffer transistor Q7. The output from the emitter of transistor Q7 is applied through capacitor C12 (C9) to the filter FL1 of the 48- (12-) channel timing circuit (*c*

below) and to the base of buffer transistor Q8. The output at the emitter of transistor Q8 is divided into two parts: one part, designated *xtal filter drive,* is applied to terminal 31 of jack J6 (J3), which is only used during 96- (24-) channel operation. The other part of the transistor Q8 output, designated *xtal filter drive meter* (SF (B)), is peak-detected by diode CR5 and capacitor C8, and applied to terminal 17 of jack J6 (J3) as a monitoring output.

c. 48- (12-) Channel Timing Circuit. . The 48(12-) channel timing circuit provides timing to the transmit and receive circuits during 48-(12-) channel operation. The timing circuits consist of a filter, phase shifter, and pulse generator.

(1) *Filter network.* The filter network consists of crystal filter FL1, buffer transistor Q12 (Q9), and amplifier transistor Q13 (Q10). The output of buffer transistor Q7 is a random train of spiked pulses that are filtered by filter FL1, producing a 2,305-kc (576-kc) sine wave at the input of buffer transistor Q12 (Q9). The signal is amplified and inverted by transistor Q13 (Q10). In panel 4A4, the output of transistor Q13 passes through a resonant parallel-tuned circuit before being applied to the phase-shifter network; however, in panel 5A4, the output of transistor Q10 is applied direct to the phase-shifter network. Tuned circuit L4, C22, and R28 amplifies only the selected bandwidth and further suppresses unwanted frequencies.

(2) *Phase-shifter network*. The phase-shifter network consists of buffer transistor Q14 (Q11), transformer T1, capacitor C16 (C13), and adjustable resistor R32 (R25). The inverted sine-wave output of transistor Q13 (Q10) is applied to the base of buffer transistor Q14 (Q11). The output is taken from the emitter and applied to the primary winding of transformer T1. One phase of the output of transformer T1 is connected to terminals 2 and 3 of PA resistor R32 (R25) through capacitor C16 (C13); the other phase is connected to terminal 1 of resistor R32 (R2B). Adjustment of PA resistor R32 (R25) varies the phase of the signal at the base of transistor Q15 (Q12), with respect to the signal at the base of transistor Q14 (Q11), from approximately -180° to approximately -60°. The output of the phase shifter is applied to the base of transistor Q15 (Q12).

(3) *Pulse generator*. The pulse generator is a pulse amplifier consisting of transistors Q16 (Q13) and Q17 (Q14), inductor L3, and diode CR9 (CR6); this circuit acts as a differential amplifier. The buffered output of transistor Q15 (Q12) is applied to the base of transistor Q16 (Q13) . The output from the collector of transistor Q16 (Q14) is differentiated by coil L3, and diode CR9 (CR6) removes the positive spikes. The resulting negative pulses are buffered by transistor Q18 (Q15) and Q19 (Q17). The output of transistor Q18 (Q15) is applied to delay DL1, in which the negative pulses are delayed 0. 1 ,μsec(0. 2 μsec). The delayed signal, designated *48-channel timing-2* (12-channel timing-2), is buffered by transistor Q20 (Q16) and applied as an output signal to terminal 13 of jack J6 (J3). The undelayed signal, designated 48-channel timing-1 (12-channel tinming-1), is taken from the emitter of transistor Q19 (Q17) and applied as an output signal to terminal 7 of jack J6 (J3). The timing-1 and timing-2 signal outputs are phased 180° apart.

d. Traffic-Alarm Control Circuit. The traffic alarm control circuit provides an alarm signal if the incoming radio signal fails or a failure occurs in the 48- (12-) channel timing circuit. The output of amplifier transistor Q13 (Q10), in addition to providing the input signal to the phase-adjust network, aids in energizing traffic-alarm relay K1 during 48- (12-) channel operation (pare 2-20 b). The traffic-alarm control circuit consists of buffer transistor Q9 (Q18), a detector, and driver transistor Q11 (Q19). The output of transistor Q13 (Q10) is applied through buffer transistor Q9 (Q18) to positive peak detector CR6 (CR8), CR8 (CR7), C11 (C17), C19 (C20), R21 (R35), and

R22 (R36). The positive charge developed on capacitor C11 provides the positive bias for driver transistor Q11 (Q19) which conducts and provides an output signal, designated *traffic alarm control*. at terminal 1 of jack J6 (J3). When the incoming radio signal is lost or a failure occurs in the 48- (12-) channel timing circuit, capacitor C11 (C17) discharges and the positive bias at the base of transistor Q11 (Q19) is shut off, thereby inhibiting the traffic-alarm control signal output.

e. Radio Signal Detector Circuit. The radio signal detector circuit provides a dc signal which aids in energizing the traffic-alarm relay during normal 48- (19-) channel operation (pare 2-20b). The detector circuit consists of buffer transistor Q10 (Q20), diodes CR10 and CR11, and driver transistor Q21. The incoming *clamped radio signal* from terminal 27 of jack J6 (J3) is applied to buffer transistor Q10 (Q20). The output from transistor Q10 (Q20) is applied to a negative peak detector which operates the same as the positive peak detector (d above). The output of the negative peak detector is applied to the base of drive transistor Q21. The dc signal output from transistor Q21 (designated *radio signal detector*) is applied as an output signal to terminal 15 of jack J6 (J3)

2-14. Timing Generator No. 2, Panel 4A5(5A5) (fig-6-24(6-31))

a. General. Timing generator No. 2, panel 4A5 (5A5), develops and amplifies timing signals for use in the receive circuits. In addition, the panel contains a relay which deenergizes to give an alarm if the radio signal fails or a failure occurs in the 96- (24-) channel timing circuit. Panel 4A5 (5A5) consists of the 96- (24-) channel timing, decision timing, countdown timing, and traffic alarm.

(1) *48- (12-) channel operation*. The *crystal-filter drive* signal at terminal 31 of jack J6 (J4) is not used during this mode of operation. Two 9,304-kc (576-kc) negative-going pulse inputs and two dc signal inputs are used during 48- (12-) channel operation. The pulse trains enter the panel at terminals 2 (1) and 19 of jack J6 (J4). The input designated *48/96 channel timing-1 (12/24 channel timing-1)* from terminal 19 is applied to the decision timing circuit (*c* below). The input, designated 48/96-channel timing (12/24-channel timing-1) from terminal 2 (1), is applied to the countdown timing circuit (*d* below). The dc signal inputs, designated *radio signal detector* signal and *traffic-alarm control.* enter the panel at terminals 21 and 24 of jack J6 (J4), respectively. Both of these inputs are applied to the traffic alarm circuit (e below).

(2) *96- (24-) channel operation*. The *crystal-filter drive* signal at terminal 31 of jack J6 (J4) is used only during 96- (24-) channel operation. This signal train consists of 4,608-kc (1,152-kc) random positive-going pulses and is applied to the 96- (24-) channel timing circuit (*b* below). In this mode, the decision timing, countdown timing, and traffic-alarm circuits operate in the same manner as for 48-(12-) channel operation. However, the frequency of both the 48/96channel timing-1 and timing-2, and 12/ 24-channel timing-1 and timing-2 signal inputs is 4,608 kc and 1,152 kc, respectively.

b. 96- (24-) Channel Timing Circuit. The 96(24-) channel timing circuit develops and provides timing signals for use in the receive circuits during 96- (24-) channel operation. The timing circuit consists of a filter, phase shifter, and pulse generator.

(1) *Filter network*. The filter network consists of crystal filter FL1, buffer transistor Q1, and amplifier transistor Q2. This network operates in the same manner as the 48- (12-) channel filter network (pare 2-13 c (1)). During 96-channel (24-channel) operation, however, this filter network produces a 4,608-kc (1,152-) sine wave.

(2) *Phase-shifter network*. The phase shifter network consists of buffer transistor Q3, transformer T1, capacitor C5, and PA potentiometer R8 (R9). which is mounted on the panel edge and is used to shift the phase of the signal. This network operates in the same manner as

the 48- (12-) channel phase-shifter network (pare 2-13c(2)). During 96(24-) channel operation, however, output of this phase-shifter network appears at the emitter of buffer transistor Q4. The output is applied to the traffic alarm circuit (e below), buffer transistor Q11, and through capacitor C6 to the pulse generator circuit ((3) below).

(3) *Pulse amplifier circuit*. The pulse amplifier circuit consists of transistors Q6 and Q8, diode CR2, and inductor L2 (transistors Q7 and Q8, diodes CR1 and CR2, and inductors L1 and L2). The output of buffer transistor Q4 is applied to the base of transistor Q6 (Q7) which operates in conjunction with transistor Q8 as a differential amplifier. The output of transistor Q8 is a negative-going spike pulse which is connected to driver transistors Q7 (Q6) and Q9. Diode CR2 (CRT and CR2) clips the positive overshoot. The output at the emitter of transistor Q7 (Q6) is designated 98-channel timing-1 (24-channel timing-1) and the output at the emitter of transistor Q9 is designated 96-channel timing-£ (24-channel timing-2). The outputs are connected to terminals 27 and 29, respectively, of jack J4. Since the output pulses are derived from opposite polarities of the sine wave, the pulse trains are 180° out of phase.

c. Decision Timing Circuit Decision timing circuit Q14 (Q12), Q15 (Q13), and Q16 (Q14), amplifies the 48/96-channel timing-1 (12/24channel timing-1) signal. The 48/96 channel timing-] (12/24-channel tirning-1) signal, consisting of negative-going pulses, enters panel 4A5 (5A5) at terminal 19 of jack J6 (J4). This signal is amplified by transistors Q14 (Q12) and Q15 (Q13), and applied to the base of buffer transistor Q16 (Q14). The output from the emitter of transistor Q14 (Q16) is applied to terminal 6 of jack J6 (J4) (decision timing) and to terminal 7 of jack J6 (J4) (decision timing meter (SFCF)).

d. Countdown Timing circuit. Countdown timing circuit Q17 and Q18 amplifies the 48/96 channel timing-£ (12/24-channel timing-2 signal, which enters panel 4A5 (5A5) at terminal 2 (1) of jack J6 (J4) and is divided into two branches: one branch, designated countdown timing, is applied through transistors Q17 and Q18 to terminal 3 of jack J6 (J4); the other branch is applied through buffer transistor Q20 and a negative peak detector to the base of amplifier transistor Q19. The output of transistor Q19, designated countdown timing meter (SF(E)), is applied as a monitoring output to terminal 1 (2) of jack J6 (J4).

e. Traffic-Alarm, Circuit. The traffic-alarm circuit provides an alarm signal if the incoming radio signal fails or a failure occurs in the 96(24-) channel timing circuit. This circuit consists of relay K1, a positive peak detector, and a delay network. A-12-volt dc bias from terminal 26 of jack J6 (J4) is applied to terminal 3 of relay K1. The incoming radio signal detector signal from terminal 21 of jack J6 (J4) is applied to terminal 4 of the relay coil. The incoming traffic alarm control signal from terminal 24 of jack J6 (J4) and the output of the collector of transistor Q10 are applied to terminal 2 of the relay coil. The output of transistor Q4, in addition to providing the input signal to the pulse generator circuit, aids in energizing relay K1 during normal 96 or 24-channel operation (para 2-20b). The timing alarm control circuit, consisting of a detector and transistors Q5 and Q10, operates in the same manner as the traffic-alarm control circuit (pare 2-13d). When relay K1 energizes, contacts 1 and 5 open and contacts 1 and 3 close. When contacts 1 and 3 are closed, a 12-volt bias is applied to delay network R25 (R36) and C13 (C27). The charge on capacitor C13 (C27) biases the base of transistor Q13 (Q16) into cutoff approximately 1 second after relay K1 deenergizes. With transistor Q13 (Q16) cut off, transistor Q12 (Q15) is cut off. Simultaneously, a-12-volt dc bias is also applied to resistors R34 (R32) and R40 (R41), causing transistors Q13 (Q16) and Q18 to cut off, thereby inhibiting the decision timing and countdown timing outputs. When normal operation returns, relay K1 is energized, closing contacts 1 and 5 and opening contacts 1 and 3. Capacitor C13 (C27) rapidly discharges through resistor R24 (R35), diode CR12 (CR15) and pins 1 and 5 of relay K1 to ground. Transistors Q13 (Q16) and Q12 (Q15) conduct with a ground potential at the base of transistor Q13 (Q16). The out put of transistors Q12 (Q15) is applied to terminal 20

of jack J6 (J4) where it is designated delayed traffic alarm. The ground potential at contacts 1 and 5 of relay K1 is also applied to resistors R34 (R32) and R40 (R41) enabling the decision circuit and countdown timing outputs, and to terminal 28 of jack J6 (J4) where it is designated traffic meter (SF(P)).

2-15. Timing Generator No. 3, TD-202/U Panel 4A6/SA6 (fig. 6-25)

a. General. Timing generator No. 3 panel 4A6/5A6 provides timing signals for sampling the recovered pcm and the address detection circuit. Panel 4A6/5A6 also provides the external timing out signals. It contains a countdown timing circuit (b below), timing-1 control circuit (c below), timing-2 control circuit (d below), and 8-kc control circuit (e below). The 8-kc control circuit is used during 24S operation only.

b. Countdown Timing Circuit. The countdown timing circuit converts a countdown timing signal and a medium-traffic, skip-pulse signal to a *medium-traffic, 8-kc control* signal.

(1) The *countdown timing* signal, a 576-kc positive pulse train, is applied through capacitor C1 and resistor R1 to a frequency-doubler stage. Each positive spike applied to the base of transistor Q1 appears as a negative spike at the collector. The negative spikes are coupled through capacitor C2 and applied to the base of the transistor Q2. The positive spikes (1. 74 μsec apart) appearing at the collector of transistor Q2 are applied to diode CR1 and delay line DL1. A positive spike applied to delay line DL1 is reflected back to diode CR1 as a negative spike with a 0. 44-usec delay. Since diode CR1 appears as an open circuit to the negative spike, it is reflected back into delay line DL1, which then reflects back to positive spike delayed an additional 0. 44 μsec Since the total delay is 0. 88 μsec, the delayed spikes combined with the original spikes provide a 1,152-kc output frequency. For detailed functioning of delay lines, refer to TM 11-672.

(2) The 1,152-kc positive-going spikes are coupled through capacitor C3 to the base of amplifier Q3. The amplified and inverted signal is applied to terminal 2 of pulse shaper Z1. The medium-traffic 8-control signal (1,152-kc positive pulses), developed by pulse shaper Z1, is coupled through capacitor C5.

(3) During 24S operation, skip pulses are developed by the address signals to shift the timing until the trains are properly separated. The medium-traffic, skip- pulse signal is coupled through capacitor C4 and diode CR3 to flip-flop Z2. When no skip pulse is present, inhibitor Q4 is cut off. When a skip pulse is present, flip-flop Z2 changes state and inhibitor Q4 conducts, eliminating an output pulse from the medium-traffic 8-kc control signal. The next pulse from terminal 8 of pulse shaper Z1 is coupled through capacitor C6 and diode CR4 to reset flip-flop Z2, and transistor Q4 is again cut off. This deletes one pulse to the countdown chain and shifts the 8-kc address signal 0. 87 μsec The address signals generate skip pulses until correct separation is established.

c. Timing-1 Control Circuit. The timing-1 control circuit converts a high/medium-traffic timing-1 control signal (576-kc square wave) to the timing out-1 signal, a timing A signal, and timing out-1 meter monitoring voltages for high and medium traffic. The H/M traffic timing-1 control signal is coupled through capacitor C7 to pulse shaper Q5. Coil L1 and diode CR6 make up a pulse-shaping network. Buffer Q6 isolates the timing A output from pulse shaper Q5; the output from pulse shaper Q5 is applied to terminal 2 of pulse shaper Z3. The 576 kc pulse generated by pulse shaper Z3 is applied to terminal 21 of jack J7 as the timing out-1 signal. Capacitors C8 and C9, diodes CR8 and CR9, and resistors R21 and R22, comprise a meter voltage peak detector.

d. Timing-2 Control Circuits. The operation of the timing-2 control circuit is identical with that of the timing-1 control circuit (c above) except that their corresponding input signals are 180° out of phase.

e. 8-Kc Control Circuit. The 8-kc control circuit converts the high/medium-traffic 8-kc control

signal to a medium-traffic timing-1 control signal, a medium-traffic timing-2 control signal, an 8-kc address-1 signal, an 8-kc address-1 meter signal, an 8-kc address-2 signal, and an 8-kc address-2 meter signal. In the TD-202/U, the 8-kc control signal is a train of square pulses at a pulse repetition rate of 1,152 kc

(1) 1,152-kc signal (A, fig. 2-13) applied to terminals 3 and 9 of flip-flop Z4 is converted to two 576-kc square-wave complementary signals at terminals 2 and 10 (B, fig. 2-13). These outputs become the medium-traffic timing-1 control and the medium-traffic timing-2 control signals.

(2) The 576-kc square-wave signal is coupled through capacitor C18 to pins 3 and 9 of flip-flop Z5, and through differentiating circuit C25 and R24, to the base of feedback gate Q8 (C, fig. 2-13). The terminal 2 output of flip-flop Z5 (D, fig. 2-13) is applied through capacitor C19 to terminals 3 and 9 of flip-flop Z6, and through register R23 to the base of feedback gate Q7. The output from terminal 10 of flip-flop Z6 (E, fig. 2-13) is applied to the base of feedback gate Q9. When simultaneous negative pulses appear at the bases of feedback gates Q7, Q8, and Q9, a positive spike (G. fig. 2-13), is applied through diode CR10 to change the state of flip-flop Z5. Comparing the terminal 2 output of flip-flop Z6 (F. fig. 2-13) with the input to flip-flop Z4 (A, fig. 2-13) shows that flip-flop Z4, Z5, and Z6, and feedback gates Q7, Q8, and Q9 make up a divide-by-six function. The output applied through capacitor C20 to terminals 3 and 9 of flip-flop Z7 is therefore 192 kc.

(3) Flip-flops Z7 and Z8 perform divide-by-2 functions: the output applied through capacitor C22 to terminals 3 and 9 of flip-flop Z9 is 48 kc.

(4) Flip-flops Z9, Z10, and Z11, and feedback gates Q12, Q13, and Q14 form a divide by 6 function, with a resultant complementary output of 8 kc at terminals 2 and 10 of flip-flop Z11. Buffers Q15 and Q16 provide isolation for the 8-kc address-2 and 8-kc address-1 signals, respectively. Resistors R42 and R45 couple the 8-kc address-1 and 8-kc address-2 metering signals to the meter circuit.

2-15.1. Timing Generator No. 3, TD-203/U Panel 4A11 (fig. 6-25. 1)

a. General. Timing generator No. 3 panel 4A11 provides the high traffic timing signals for sampling the recovered pcm and the address detection circuit in the receive section of the TD- 203/U. It contains tim out 1/ timing A generator, tim out-2/ Timing B generator, and the B-kc address generator. The 8-kc address circuit is used during 96S operation only.

b. Tim Out-1/Timing A Generator. This circuit develops the 2,304-ko tim out-1 and 2,304-kc timing A pulse signals as follows. The timing-1 control signal, a continuous train of 2,304-kc positive going pulses, is coupled through capacitor C5 to pulse shaper transistor Q1. Pulse shaper transistor Q1, with coil L1 and diode CR1 in the collector circuit, shapes and inverts the timing-1 control signal, forming a 2,304-kc pulse train of negative pulses. This signal is applied to two circuit branches; one branch feeds through buffer Q2 to terminal 20 of jack J7, where it becomes the timing A signal; the second branch is applied to terminal 2 of pulse shaper Z1. Pulse shaper Z1 converts the negative pulses to sharp positive spikes and applies the signal to two branches one branch la applied through terminal 21 of Jack J7 as the tim out-1 signal; the second branch passes through capacitor C6 to voltage doubler diodes CR4 and CR5 and resistor R5, producing a dc voltage at terminal 15 of Jack J7, which is the tim out-1 monitoring signal.

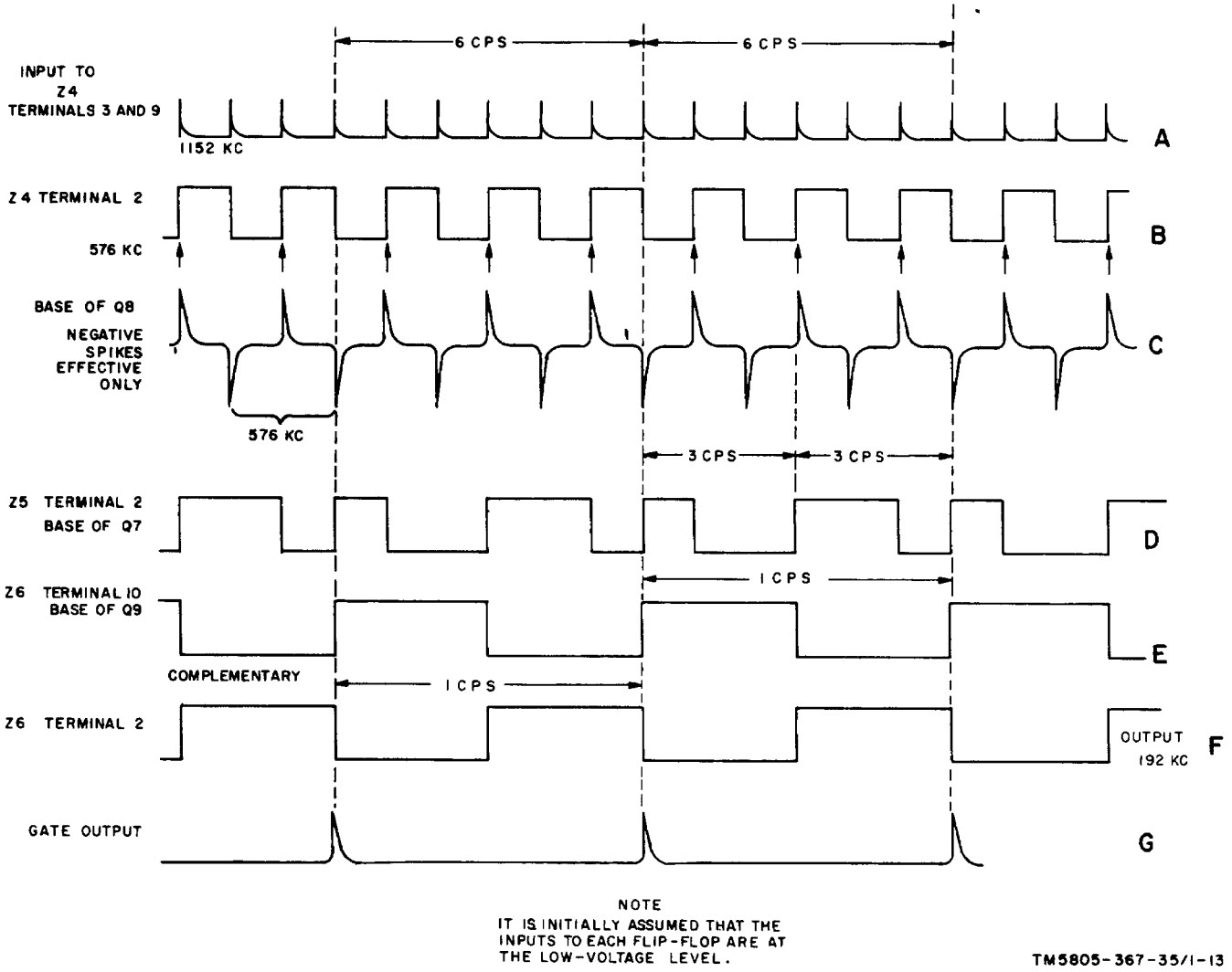


Figure 2-13. Panel 4A6/5A6, divide by 6 function relationship.

c. Tim out-2/timing B Generator. The operation of the tim out-2/timing B generator circuit is identical with that of the tim out-1/ timing A generator circuit (b above), except that the pulses in the timing-2 control input signal are delayed 0. 2 microseconds with respect to those in the timing-l control input signal.

d. 8 kc Address Generator. This generator develops the 8 kc address-1 and -2 framing signals. It consists of a countdown chain, retiming, and output circuit.

(1) *Countdown chain*. This circuit performs a divide by 144 function in eight steps as follows.

(a) The 8 kc control signal, a continuous train of 1,152-kc square pulses ((B, fig 6-19.1) is fed from terminal 4 of jack J7 to terminals 3 and 9 of flip-flop Z3. Flip-flop Z3 converts the 1,152-kc signal to a 576-kc square pulse signal which appears at terminal 2 of Z3 (C, fig 6-19.1). The 576-kc signal is fed from terminal 2 of Z3 to three branches; one branch feeds to buffer transistor Q5; a second branch is applied to feedback gate Q10; the third branch is fed through capacitor C14 to terminals 3 and 9 of the second countdown element flip-flop Z4. If this were the only input to flip-flop Z4, it would divide by 2 producing a 288-kc signal. However, a second input to Z4, a 192-kc pulse signal applied at terminal 2 causes Z4, in effect, to divide by 1. 6 producing a complex pulse sequence (D, fig. 6-19. 1) which contains positive-going trigger edges at a 384-kc regular rate. This signal feeds through capacitor C15 to terminals 3 and 9 of the third countdown element flip-flopping trigger edges producing complement 192Z4 which counts down the 384 kc positive-go kc square pulse signals at terminals 2 (E, fig. 6-19.1) and 10 of Z5.

(b) The 192 kc pulse signal applied to terminal 2 of Z4 is generated in feedback gate transistors Q8, Q9, and Q10. Gate input signals to the base of transistors Q8, Q9, and Q10 are as shown in figure 2-13.1. When simultaneous negative pulses appear at the bases, a sharp positive pulse (4, fig 2-13.1) is generated and fed through diode CR11 to change the state of flip-flop Z4, thus producing waveform D, figure 6-19.1.

(c) Flip-flops Z6 and Z7, the fourth and fifth countdown elements each perform a divide by 2 function. The terminal 2 output of each is shown as waveforms E, and F respectively, in figure 6-19.1.

(d) Flip-flop Z8, the sixth countdown element and feedback gates Q11, Q12, and Q13 combine to perform a divide by 1.5 function producing waveform G. figure 6-19.1. Flip-flop Z9 the seventh countdown element, performs a divide by 2 function waveform J. figure 6-19.1. The operation of flip-flops Z8 and Z9 and feedback gates Q11, Q12, and Q13 is similar to that described for flip-flops Z4, Z5 and feedback gates Q8, Q9, and Q1Q in (a) and (b) above.

(e) The output of flip-flop Z9, a complex pulse sequence containing positive-going trigger edges at a 16-kc regular rate, drives the eighth countdown element flip-flop Z10 producing an 8 kc square pulse signal at terminals 2 and 10 of Z10 (J. K, fig 6-19.1).

(2) *Timing and output circuits*. These circuits operate to accurately retime and condition the output of flip-flop Z10.

(a) Timing-1 control signal (5, fig 2-13.1) feeds through buffer Q5 to the base of gate transistor Q6; the 576-kc signal from terminal 2 of Z3 feeds through buffer Q7 to the cathode of diode CR8. The 2,304-kc pulses are gated through diode CR8 under control of gate transistor Q6 driven by 576-kc square pulse signal. The gated pulses (7, fig 2-13.1) are fed to the trigger input of flip-flop Z11. The level set inputs of flip-flop Z11, terminals 1 and 11, are driven by the output from terminals 10 and 2, respectively (K, L, fig 6-19.1), of Z10. As indicated in M, figure 6-19. 1, sampling flip-flop Z11 is triggered only by the first pulse after the level inputs change state, generating complementary 8-kc square pulse output at terminals 2 and 10 of Z11 (O, N. fig 6-19.1). All other input pulses have no effect on the output of Z11.

(b) Delay line DL 1 inserts a slight delay in the 8-kc address-1 signal to insure proper operation of the recovered pcm sampling circuit in panel 4A8/5A8. Buffer Q15 isolates the delay line and Z11. Buffers Q14 and Q16 provide isolation for the 8-kc address-2 and 8-kc address-1 signals, respectively. Resistors R32 and R39 couple the 8-kc address-1 and 8 kc address-2 metering signals to the meter circuit.

2-16. Order-Wire Panel 4A7/5A7 (fig. 6-26)

a. *General*. Order-wire panel 4A7/5A7 provides facilities for recovering the radio orderwire signal. The radio order wire is an auxiliary communications link used by maintenance and supervisory personnel to communicate between stations during maintenance, alignment, and troubleshooting. The order-wire signal (A, fig. 2-8) is transmitted by adding it linearly to the outgoing pcm (B, fig. 2-8) in

the transmitter section to produce a composite (C, fig, 2-8) of the two signals. In the receiving station, the composite signal is passed by the radio, to the TD-202/U or TD-203/U, where the order-wire signal is separated from the composite signal and is returned to the radio receiver section.

b. Circuit Analysis. The order-wire signal is recovered in the subtractor circuit, where the pcm portion of the received radio signal (*recd rad sig*) and the *recovered pcm-2* signal cancel out, leaving the order-wire signal. The *recd rad sig* enters the panel at terminal 7 of jack J5. The *recovered pcm-2* signal enters the panel at terminal 31 of jack J5.

(1) *Received radio signal*. The incoming *recd rad sig* is applied to transistor Q15 and then to filter network L3, R32, and C21. The filter network removes the higher frequencies of the signal to match it with the recovered *pcm-2* signal entering the other side of the subtractor. The *recd rad sig* is applied to the

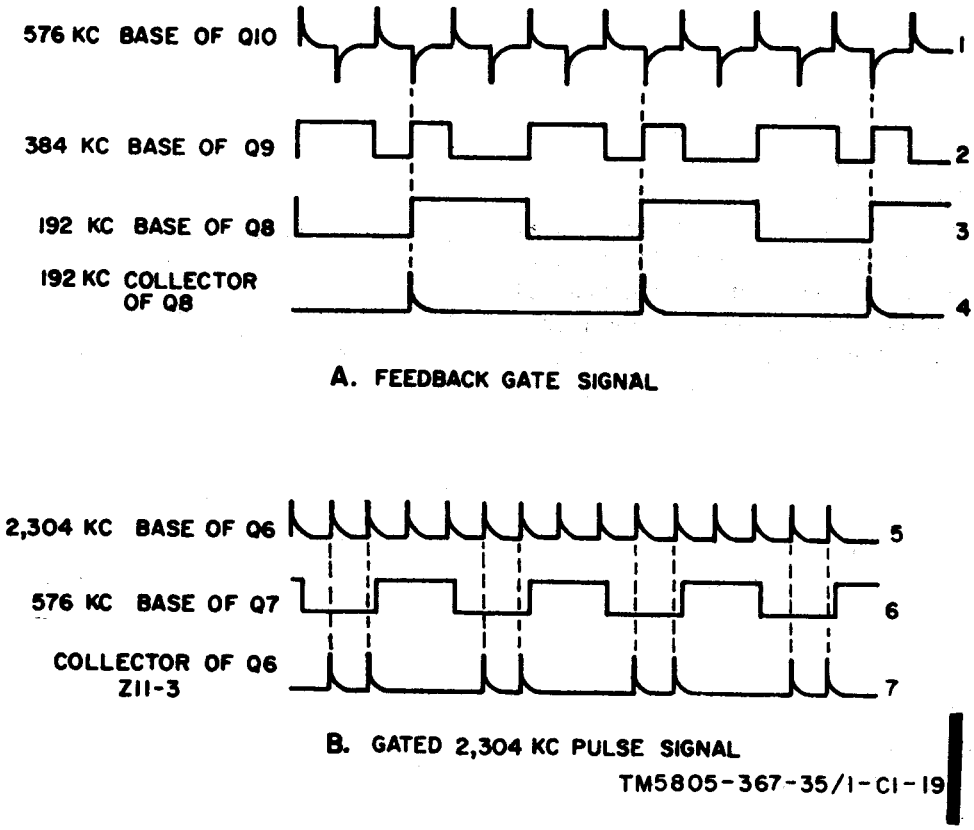


Figure 2-13.1. 8-kc address generator, timing signals.

base of transistor Q16. The emitter output of Q16 is applied, through rc network R35, C22, to the emitter of transistor Q17. The composite signal (pcm plus order wire) is then compared with the recovered *pcm-2* signal which has been similarly filtered. The difference appears at the collector of Q17 as the order-wire signal.

(2) *Recovered pcm signal*. The incoming recovered *pcm-2* signal at terminal 31 of jack J5, is divided into two branches: one branch is applied to the base of buffer transistor Q2 for application to the product detector; the other branch is applied to the base of gain-controlled amplifier transistor Q1. In the gain-controlled amplifier, the signal amplitude is matched to that of the composite signal to make the pulling in the subtractor more nearly complete. The signal at the emitter of transistor Q1 is applied to buffer transistor Q10, and then to filter network L2, R18, and C14. The filter network removes the higher frequencies to match the signal with the pcm in the *recd rad sig*. The recovered *pcm-2* signal is then applied to subtractor transistor Q17 for comparison with the *recd rad sig*.

(3) *Order-wire output*. The order-wire output of the subtractor at the collector of transistor. Q17 is applied to the product detector and the order-wire amplifier. If the order wire is devoid of pcm, the signal is applied to the base of transistor Q11. The signal is taken from the emitter of transistor Q11 and applied to filter FL1, which removes the high frequencies. The order-wire signal is amplified by transistors Q12 and Q13 and applied via terminal 15 of jack J5 (order wire level adjust) to order-wire level adjust potentiometer R2 on the service facility panel. The signal is picked off by the potentiometer arm and returned to terminal 6 of jack J5. The order-wire signal is then applied to the base of transistor Q14, and the output at the collector is applied to the primary winding of impedance matching transformer T2. The output of the secondary winding is applied to terminals 3 and 5 of jack J5, designated order-wire out-B and order-wire out-A, respectively. Another branch of the output of the collector of transistor Q14 is converted to a negative dc voltage in a peak-detector circuit and applied to terminal 1 of jack J5 (order-wire meter [SF (o)]); this signal is used for monitoring.

(4) *Product detector*. If the level of the recovered *pcm-2* signal into the subtractor is not equal to the level of the pcm portion of the *recd rad sig* into the other side of the subtractor, pcm appears at the collector of transistor Q17, together with the order-wire signal. If this occurs, the product detector automatically adjusts the gain of the gain-controlled amplifier to eliminate the pcm. The secondary branch of the subtractor output is applied to the base of buffer transistor Q5; the output at the emitter is applied to the primary winding of transformer T1. The recovered *pcm-2* signal (b above) from receiver panel 4A3 (5A3) (pare 2-12) is divided into two branches, with one branch going to the base of buffer transistor Q2. This signal is taken from the emitter of transistor Q2 and applied to filter network L1, R2, and C1, which removes the higher frequencies. The output of the filter is applied to driver transistor Q4, and then to a junction between the two secondary windings of transformer T1 in the product detector. The product detector multiplies the composite signal with the order-wire output of the subtractor and averages the product. If there is any unbalanced pcm in the subtractor output, an unbalanced signal results at the output of the product detector. This unbalanced signal is applied to the differential amplifier, which develops a control signal at the collector of transistor Q9. The dc control signal at the collector of transistor Q9 is applied to the base of transistor Q3 of the gain controlled amplifier. This circuit operates as a differential amplifier. The recovered *pcm-2* signal at the base of transistor Q1 is compared with the control signal at the base of transistor Q3. When the voltage at the base of transistor Q1 goes more negative than that of transistor Q3, transistor Q1 conducts and permits the signal to enter the subtractor. This action tends to equalize the signal with

that entering the other side of the subtractor, so that the pcm can be completely nulled out.

2-17. Output and Framing, Panel 4A8/5A8 (fig. 6-27)

a. General. Output and framing panel 4A8/5A8 is the last panel of the receiving chain through which the principal signal passes before it leaves the TD-203/U (TD-202/U). During 48- (12-) channel operation, the panel regenerates the single binary signal. When the TRAFFIC SEL switch is set for 96R or 96I (24R or 241) biternary repeater or interleaved operation, the panel regenerates the interleaved 96- (24-) channel train. During 96S (24S) biternary separated operation, the 96- (24-) channel interleaved binary train is separated into its two 48- (12-) channel single binary trains and sent out on separate lines to the radio.

b. Pcm Signal. The recovered pcm-1 signal enters the panel at terminal 19 of jack J9 and is divided into three branches. The first branch, together with the timing A signal from terminal 14 of jack J9, is applied to the differential pulse amplifier of the pcm-1 circuit ((1) below) . The second branch, together with the timing B signal from terminal 9 of jack J9, is applied to the differential pulse amplifier of the *pcm-2* circuit. This circuit operates in the same manner as the pcm-1 circuit. The third branch, together with the 8-kc address-1 signal, is applied to the differential pulse amplifier of the 8-kc address-1 circuit (c (1) below). This circuit is only required for biternary separated operation.

(1) *Pcm-1 circuit*. The pcm-1 circuit is used during binary and biternary operation. During binary operation, this circuit samples the incoming pcm single binary train with the timing A signal and regenerates the pcm-1 signal. During biternary operation, this circuit operates in the same manner as for binary operation. During biternary repeater or interleaved operation, however, the pcm input and output consist of a single interleaved binary train. In this mode, the frequency of the timing signal is 4,608 kc (1,152 kc), twice that of the binary train, since timing A and timing B are connected together by the TRAFFIC SEL switch. During biternary separated operation, the pcm-1 circuit samples the incoming interleaved binary train with the 2,304-kc (576-kc) timing A signal and separates the pcm-1. The pcm-1 circuit consists of a differential pulse amplifier, a flip-flop, a driver, and a peak detector.

(a) Pcm-1 signal inputs. One branch of the incoming recovered pcm-1 signal from terminal 19 of jack J9, along with the timing A signal from terminal 14 of jack J9, is applied to the pcm-1 differential pulse amplifier.

(b) Pcm-1 differential pulse amplifier The differential pulse amplifier consists of transistors Q1, Q2, and Q3. The incoming recovered pcm-1 signal is applied to the base of transistor Q1; the incoming 2,304-kc (576-kc) negative spike timing A signal is applied to the base of transistor Q3. The differential pulse amplifier operates as a sampler circuit in which the pcm single binary train is sampled by the timing A signal. The pulses representing logic 0's appear at the collector of transistor Q1 and are applied to the left side of the pcm-1 flip-flop (transistors Q4 and Q5). The pulses representing logic 1's appear at the collector of transistor Q2 and are applied to the right side of the pcm-1 flip-flop.

(c) Pcm-1 flip-flop. The pcm-1 flip-flop regenerates the pcm-1 signal and the output appears at the emitter of transistor Q5, which operates in conjunction with transistor Q6 as a differential amplifier. The pcm-1 signal developed at the collector of transistor Q6 is applied to the base of driver transistor Q7.

(d) Pcm-1 output. The output at the emitter of driver transistor Q7 is applied to terminal 31 of jack J9 (PCM OUT-1) and, via a peak-detector network, to terminal 11 of jack J9, designated as pcm out-1 meter (SF(M)).

(2) *Pcm-2 circuit*. The *pcm-2* circuit is used only during biternary separated operation,

and operates in the same manner as the pcm-1 circuit. In repeater and interleaved operation, the pcm input and output is an interleaved binary train. In this mode, the frequency of the timing signal is 4,608 kc (1,152 kc) twice that of

|the binary train, since timing A and timing B are connected together by the TRAFFIC SEL switch. In separate operation, the incoming pcm is sampled with the *timing B* signal and separates the pcm-2 only. The frequency of the *timing B* signal is the same as the *timing A* frequency, but the signals are 180° out of phase.

c. Address Signals. To assure that the timing for the separation process is synchronized with that of the unit originating the pcm signal, two address signals *(8-kc address-1* and *8-kc address*-are employed.

(1) 8-kc address-1 circuit. The *8-kc address*1 signal enters the panel at terminal 3 of jack J9 and is divided into two branches: 4-kc reference and 4-kc address.

(a) 4-kc reference. One branch of the *8kc address-l* signal is applied as a complement pulse to both sides of the 4-kc reference flip-flop (transistors Q24 and Q25). The flip-flop output is used as a 4-kc constant reference signal which is compared with the 4-kc address signal in the pcm.

(b) 4-kc address. The other branch of the *8-kc address-1* signal is applied to the 4-kc address circuit, which consists of a pulse amplifier, a louder, a differential pulse amplifier, and a flip-flop.

1.4-kc address parse amplifier. The incoming *8-ke address-1* signal is applied to the base of pulse amplifier transistor Q35 which is normally on. The signal is differentiated by capacitor C25; the positive portion of the differentiated signal causes transistor Q35 to shut off forming a negative pulse at the collector. A wave train of negative-going 8-ke spike pulses is developed at the collector of transistor Q35, and applied through buffer transistor Q36 as a timing pulse to the 4-kc address differential pulse amplifier.

2. 4-kc address differential pulse amplifier. The differential pulse amplifier consists of transistors Q26, Q27, and Q37. The incoming binary interleaved pcm is applied to the base of transistor Q26. The 8-kc timing signal from the emitter of buffer transistor Q36 is applied to the base of transistor Q37. Assuming that the unit is locked-in-frame, the 8-kc timing pulses at the base of transistor Q37 coincide with the logic l's and logic 0's (C, fig. 2-14) of the 4-kc address signal (in the pcm) at the base of transistor Q26. When a timing pulse coincides with a logic 0, transistor Q26 conducts to set 4-kc address flip-flop transistors Q28 and Q29. When the next timing pulse coincides with a logic 1, transistor Q27 conducts to reset the 4-kc address flip-flop.

3. 4-kc address flip-flop. The 4-kc address flip-flop produces a 4-kc square wave that is applied through transistor Q30 to the exclusive-OR circuit, where it is compared with the 4-kc reference signal. Since it is assumed that the unit is locked-in frame, the two signals produce a 0-volt output at the collector of transistors Q32 and Q33.

(2) *8-ke address-2 circuit.* The 8-kc address2 circuit consists of a pulse amplifier and three buffers. The *8-ke address-2* signal enters the panel at terminal 2 of jack j9 and is applied to buffer transistor Q15 and then to a differentiating network. The positive-going portions of the differential signal cause normally on transistor Q17 to shut off, forming a negative pulse at the collector. A wave train of negative-going 8-kc spike pulses from the collector of transistor Q17 is applied through louder transistor Q18 to diode CR13 in the skip-pulse circuit (d(2) below).

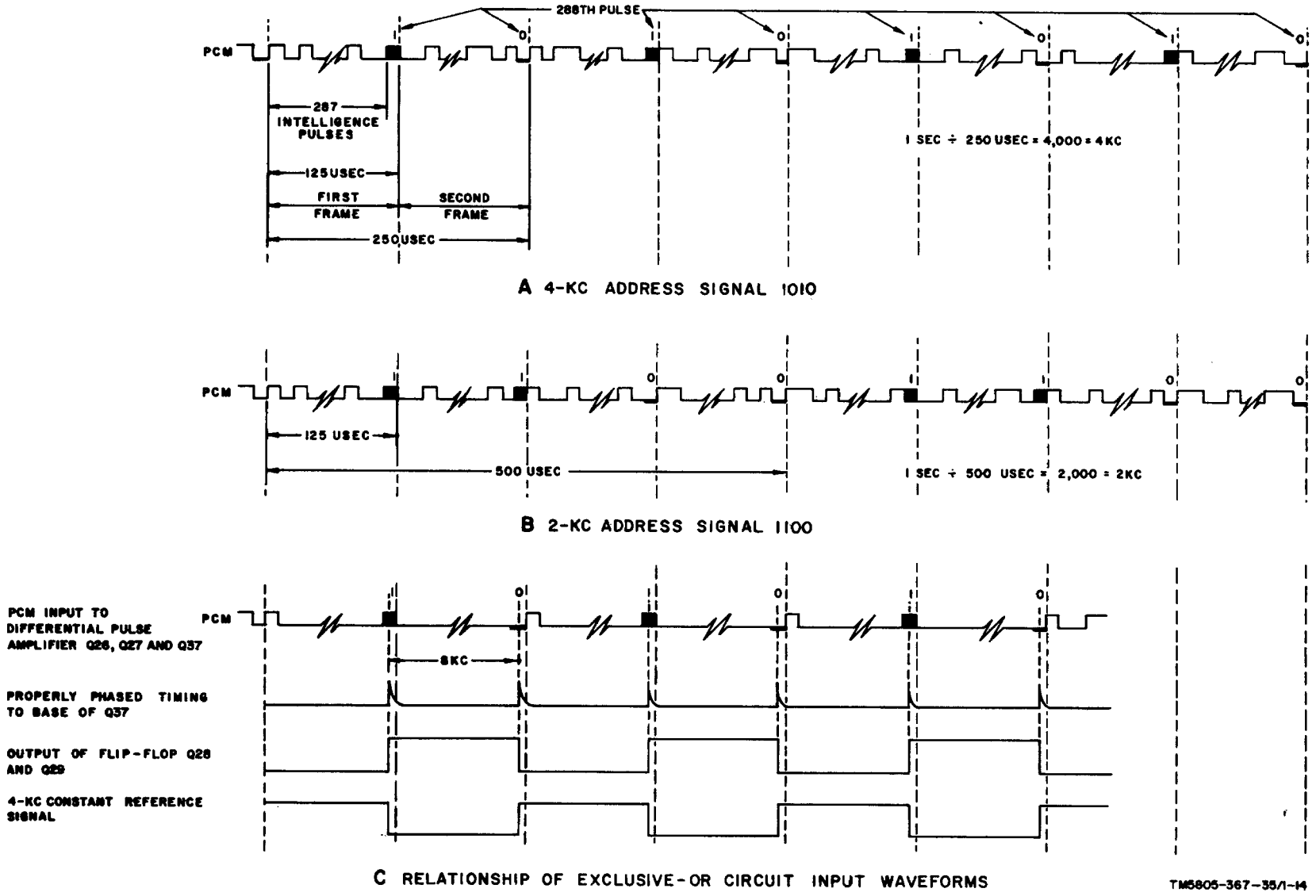


Figure 2-14. Address signal patterns

d. Skip-Pulse Signal. To assure that the pcm1 circuit is selecting tile correct binary train of the interleaved pair, a skip pulse is used to synchronize the locally generated address with the incoming pcm address. The skip pulse is developed by comparing a constant reference signal with tile address signal in the pcm; if the reference signal is of opposite phase to the address signal, the operation is normal. If this phasing does not exist, the skip pulses are generated to shift the timing until the correct address digits are found. This signal is sent out of the unit on terminal 31 of jack J9 and is designated as pcm out-1. The skip-pulse circuit consists of the following stages: exclusive-OR, storage, amplifier, and two gates.

(1) *Exclusive-OR circuit*. The exclusive OR circuit compares the 4-kc address signal with the 4-kc reference signal. The exclusive-OR circuit consists of two differential amplifiers that operate in conjunction with each other: transistors Q31 and Q33 comprise one differential amplifier; transistors Q32 and Q34 comprise the other. If the 4-kc input at the base of transistor Q31 is 180° out of phase with the signal at the base of transistor Q34, transistor Q32 or transistor Q. -33 conducts to produce a zero potential at its collectors. If both inputs to the circuit are in phase, transistors Q32 and Q33 are cut off to produce a -4. 5-volt potential at the collectors. This negative e potential is impressed at the base of louder transistor Q19. The emitter output of transistor Q19 aids in tile skipping operation.

(2) *Skipping operation*. The skipping operation automatically begins a searching process to shift the timing whenever the exclusive-OR circuit develops sufficient negative e error signals. Single isolated errors in the pcm address signal, however, do not initiate tile search process; approximately 10 errors in a row are required before the search process begins. The search process operates by permitting a pulse of an 8-kc wavetrain to escape as a skip pulse to eliminate a pulse from the timing. A wavetrain of negative-going 8-kc pulses is taken from the emitter of buffer transistor Q18 and applied to gate diode CR13 of tile skip-pulse circuit.

(a) Normal operation. During normal operation, gate transistor Q20 is off and gate transistor Q23 is on. Buffer transistor Q19 acts as an emitter follower; hence, the 0-volt potential at the base of transistor Q19 is impressed on the emitter of transistor Q19. The 0-volt potential is also impressed at the anode of gate diode CR14. The baseline of the negative pulses at the emitter of transistor Q18 is 0 volt; hence, a 0-volt potential exists at the junction of diodes CR13 and CR14 when no pulse is present. When a pulse is present, the voltage at the anode of diode CR13 goes negative. However, since tile cathode of diode CR13 is at zero potential, the diode cannot conduct to pass tile 8-kc pulses.

(b) Single isolated error. When the exclusive-OR circuit produces a negative error signal, it is applied to tile base of buffer transistor Q19. The -4. 5-volt potential at the base of transistor Q19 is impressed upon the anode of gate diode CR14, which cannot conduct, since the anode is mole negative shall tile 0-volt potential at the cathode. However, when a negative-going pulse is present at the emitter of buffer transistor Q18, the output at the junction of diodes CR13 and CR14 follows the voltage at the anode of diode CR13. The voltage at this junction goes negative for the duration of the pulse. I his negative pulse passes through capacitor C18 to the base of transistor Q21. Since gate transistor Q20 is not conducting gate transistor Q21 cannot conduct consequently, the pulse at the base of transistor Q21 cannot pass to the output of the circuit. The negative pulse also causes capacitor C19 to charge negatively. If the negative output of the exclusive-OR circuit is the result of a single isolated error tile negative error pulse is only momentary, and the base of transistor Q19 resumes

its 0-volt potential, which on to the anode of diode CR14. The negative-going charge on capacitor C19 leaks off, and normal operation is resumed.

(c) Negative error signal. When the timing actually requires correction, the process described in c (1) (b) 2 above occurs. However, in this case, the number of negative error pulses is large enough to charge capacitor C19 sufficiently negative to drive gate transistor Q20 into conduction. With gate transistor Q20 conducting, the other gate transistor Q21 is able to conduct when a negative pulse is applied to its base. Therefore, the negative-going pulses reaching the base of transistor Q21 under present conditions are able to pass through the gate. The pulse output is produced at the collector of gate transistor Q21, where the signal is designated as skip pulse.

(d) Termination of search process . When the skipping operation has corrected tile timing, any continuation of the skip pulse will only upset the timing again, and the search process will have to be repeated. When the timing is corrected, there is no longer an error signal; the base and the emitter of louder transistor Q19 assume a zero potential. Diode CR14 clamps the gate diode outputs to 0 volt and prevents passage of the 8-kc pulses beyond diode CR13. The charge on capacitor C19 leaks oaf; gate transistor Q20 goes of I, and normal operation is resumed.

2-18. Timing Generator No. 4, Panel 4A9 (fig. 6-32)

a. General. Timing generator No. 4, panel 4A9, aids in phasing the timing for the receive functions of the TD-203/U. Panel 4A9 consists of the high-traffic timing control, high-traffic 8-kc control, and 96-channel timing-2 drive.

(1) *48-channel operation*. The only input signal to the panel is a 2,304-kc pulse train which is derived direct from the countdown timing signal output of panel 4A5. This signal (2. 3-mc timing) enters the panel at terminal 31 of jack J8 and is processed by the high-traffic timing control circuit (b below) and the high-traffic 8-kc control circuit (c below), to develop two 2,304-kc timing control signals (h.t. tim-1 cont and h.t. tim-2 eons) and a 1,152kc control signal (h.t. 8-kc. eons).

(2) *96-channel operation*. In addition to the 2. 3--mc timing signal input, panel 4A9 receives a 4,608-kc spiked pulse train (96 chan-timing-2) and high-traffic skip pulse. The 9G-chan timing-2 signal input is derived directly from the 96-chan timing-2 signal output of panel 4A5. The spiked pulse enters the panel at terminal 2 of jack J8 and is applied to the 96-channel timing-2 drive circuit (d below), which develops a 2,304-kc timing drive signal (96-chan timing-2 drive). The skip-pulse input is an isolated pulse that occurs during the framing operation and is inserted into the high-traffic timing control circuit (b below) only during the 96S mode of operation. This pulse is derived from panel 4A8/5A8 via the TRAFFIC SEL switch. During 96-channel operation, the high-traffic timing control circuit operates in the same manner as for 48-channel operation. However, the 2. 3-me timing signal input is derived from the 96-channel timing-2 drive signal output of panel 4A9 via the TRAFFIC SKI, switch

b. High-Traffic Timing Control Circuit. The high-traffic timing control circuit receives a 2,304kc square-wave pulse training signal and develops two 2,304-kc timing control signals. During 96S Operation, this circuit also receives a skip-pulse signal to assure that the timing signals are coincident with their related pcm signals. The high-traffic timing control circuit consists of the undelayed pulse amplifier, delayed pulse amplifier, skip-pulse flip-flop, and switching gate.

(1). *Inputs*. During 48-channel operation, the incoming 2. 3-mc timing signal from terminal 31 of jack J8 consists of a 2,304kc pulse train (in 96-channel operation, a 2,304-kc square wave) which is amplified by transistors Q1, Q2, and Q3. The signal

at the emitter of transistor Q3 is applied to the undelayed pulse amplifier ((2) below) and the delayed pulse amplifier ((3) below). During 96S operation a skip pulse, generated in panel 4A8/5A8 whenever the phasing of the timing signal is incorrect, is applied to the skip-pulse flip-flop circuit ((4) below) via the TRAFFIC SEL switch and terminal 21 of jack J8.

(2) *Undelayed pulse amplifier*. One branch of the emitter output of transistor Q3 is the undelayed signal, which is applied to the base of undelayed pulse-amplifier transistor Q6. The signal appears at the collector of transistor Q6 with the original positive-going polarity. The network (diode CR3, resistor R13, inductor L2) at the collector sharpens the pulses to produce the required narrow spike pulses, which are applied to gate transistors Q7 and Q14 of the switching gate (c below).

(3) *Delayed pulse amplifier*. The other branch of the emitter output of transistor Q3 is the delayed signal which is applied to 2-usec delay DL1. The pulses of the delayed signal fall midway between the pulses of the undelayed signal. The delayed signal is amplified by buffer transistor Q4 and delayed pulse-amplifier transistor Q5. In transistor Q5, the signal is inverted to its original polarity and is sharpened by the network (diode CR1 resistor R8, inductor L1) at the collector. The positive-going pulses are then applied to gate transistors Q10 and Q11 of the switching gate (c below).

(4) *Skip- pulse flip-flop*. The skip-pulse flip-flop circuit governs the states of the transistors in the switching gate circuit (c below). The flip-flop operates as a conventional bistable multi vibrator which changes state each time a positive-going skip pulse from terminal 21 of jack J8 is applied to capacitors C17 or C18.

c. Switching Gate Circuit. The switching gate circuit acts like a double-pole, double-throw (dpdt) switch which automatically shifts the timing one-half bit (0. 2 μsec) each time the circuit receives a skip pulse; this occurs during the framing operation. By shifting the timing by one-half bit, the square-wave address signal that is developed by the timing pulses is shifted one-half bit along its base. The process repeats until the local address signal coincides with that of the pcm train. Undelayed and delayed timing signals are applied to the switching gate circuit which routes each of the two inputs to an output circuit. Whenever a skip pulse is generated, the switching gate interchanges the timing outputs. The specific purpose of the gate is to switch the positive-going pulsed output of undelayed pulse-amplifier transistor Q6 to buffer transistor Q15 or Q16. Further, the gate delivers the positive-going spiked output of delayed pulse-amplifier transistor Q5 to buffer transistor Q15 or Q16, whichever does not receive the signal from the undelayed pulse amplifier. The gate circuit consists of gate transistors Q7 through Q14, which operate in pairs as differential amplifiers. Diodes CR5 through CR6 are reverse bias protection diodes. Transistors Q7 and Q8 make up the first pair; transistors Q9 and Q10, the second pair; etc. Whenever one transistor of a pair is in the off state, the other is on. The states of the transistors are governed by the state of the skip-pulse flip-flop (b(4) above).

(1) *Operation*. Assume that the output of transistor Q20 is positive and the output of transistor Q21 is negative (A, fig. 215). The positive voltage is applied to the bases of transistors Q8 and Q9 to shut off these two transistors, and turns on transistors Q7 and Q10. The negative voltage of the skip-pulse flip-flop is applied to the bases of transistors Q12 and Q13 to drive them on and, consequently, to drive transistors Q11 and Q14 off. When the delayed or undelayed signal is applied to bases of transistors in the on state, the signals are able to pass and reach louder transistor Q15 or Q16. When the skip-pulse flip-flop changes state, the output of transistor Q20 is negative, and the output of transistor Q21 is positive (B, fig. 2-15). Transistors Q8 and Q9 are driven on, and transistors Q12 and Q13 are driven off reversing the delayed and undelayed signals.

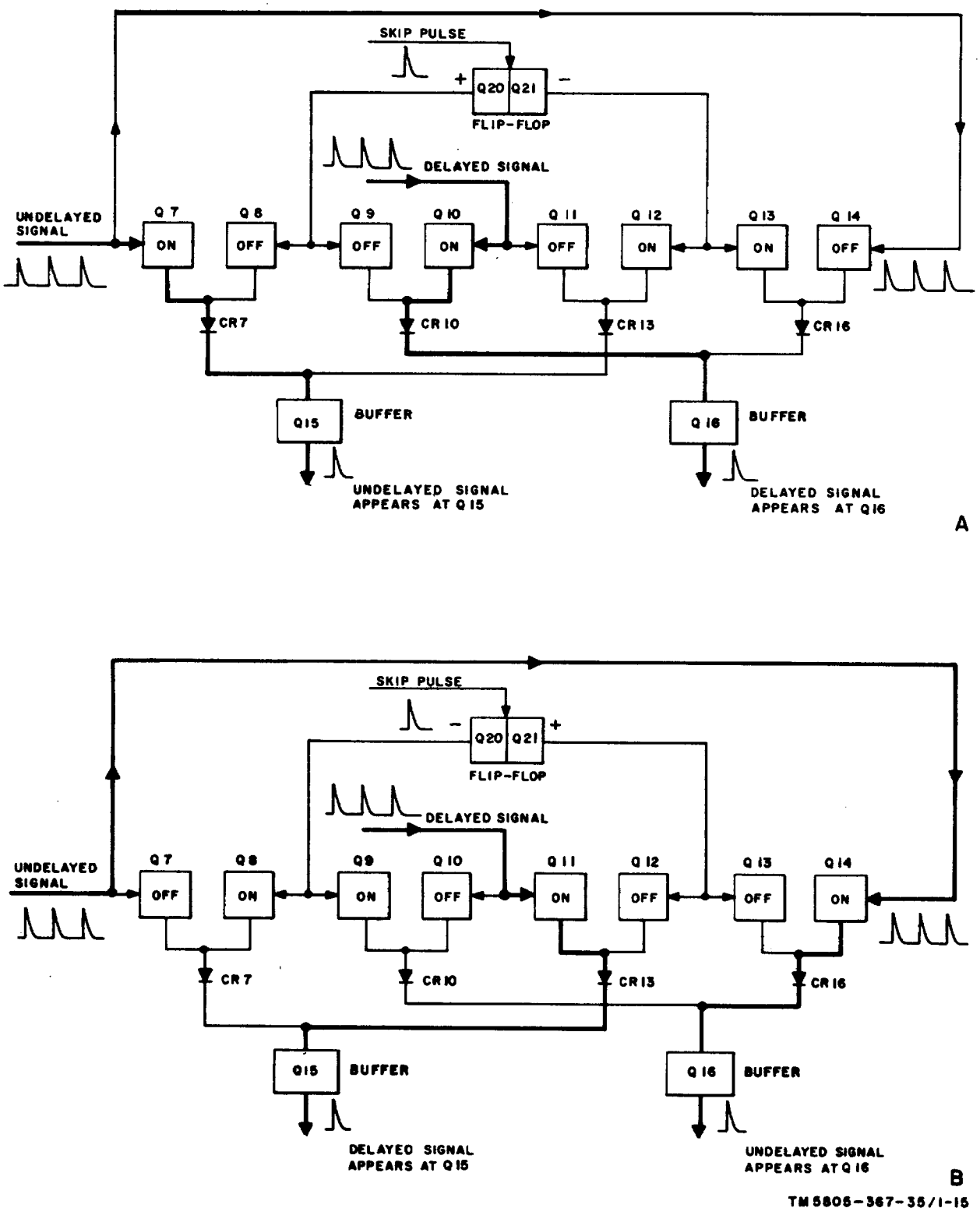


Figure 2-15. Double-pole, double-throw gate circuit.

(2) *Outputs*. The outputs of the switching gate appear at the bases of buffer transistors Q15 and Q16. The output signal from the emitter of transistor Q15 is a 2,304-kc wavetrain of positive-going spike pulses that is divided into two branches: one branch is applied to terminal 16 of jack J8 (*h.t. tim-2 cons*); the other branch is applied through capacitor C4 to both sides of the multivibrator of the high-traffic 8-kc control circuit (*d* below). The output signal from the emitter of transistor Q16 is a 2,304-kc wavetrain of positive-going spike pulses that is applied to terminal 17 of jack J8 *(h.t. I tim-1 cons)*. The pulses are spaced 180° apart from those of the *h. t. tim-1 cont* signal output.

d. High-Traffic 8-Kc Control Circuit. The high traffic 8-kc control circuit is a high-speed bistable multivibrator capable of switching states at a 2.3-mc rate. The control circuit receives a 2,304-kc positive-going spike pulse train from the emitter of buffer transistor Q15 and develops a 1,152-kc square-wave control signal. The multivibrator consists of transistors Q17 and Q18, steering diodes CR17 and CR21, and trigger loading diode CR18. The output is taken from the collector of transistor Q17 or Q18 and applied to the base of buffer transistor Q19. The output at the emitter of transistor Q 19 is a 1,152-kc square-wave pulse train *(h. t. 8-kc cons)* that is applied to terminal 7 of jack J8.

e. 96-Channel Timing-2 Drive Circuit. The 96-channel timing-2 drive circuit receives a 4,608-kc spike pulse train and develops a 2,304-kc square-wave pulse train. This circuit is used only during 96-channel operation of the TD-203/U. The timing-2 drive circuit consists of driver transistor Q22, flip-flop transistors Q23 and Q24, and buffer transistor Q25. The incoming 4,608-kc spike pulse train (96-channel timing-2) from terminal 2 of jack J8 is applied to driver transistor Q22 which inverts the signal and supplies drive to the flip-flop. The flip-flop is a bistable multivibrator that divides the 4,608 kc to 2,304 kc. The output is taken from transistor Q23 or Q24 and applied to the base of buffer transistor Q25. The output at the emitter of transistor Q25 is a 2,304-kc square-wave pulse train (96-channel timing-2 drive) that is applied to terminal 3 of jack J8.

Section IV. MISCELLANEOUS CIRCUITS

2 19. General

This section describes external controls and essential circuits not covered by the panel descriptions in sections, I, II, and III of this chapter. These controls and circuits are generally mounted on the front or side panels and include such components as potentiometers, fuses, meters, and switches. Because the circuits of the TD-202/U and TD-203/U are similar, one example of each typical circuit is described to avoid duplication.

2-20. Alarm System (fig. 2-16)

a. General. The audio and visual alarm system indicates faulty operating conditions. The alarm system consists of an ALARMS BUZZER OFF switch, TRAFFIC red indicating lamp, and an ALARMS CHANGE AIR FILTER red indicating lamp.

b.. Traffic Failure Alarm. The traffic failure alarm network gives an alarm whenever traffic fails either in panel 4A4 (5A4) or 4A5 (5A5) (fig. 2-16). During normal operation, relay K1 located on panel 4A5 (5A5) is energized by amplifier transistor Q10 on panel 4A5 ((5A5)) or driver transistor Q1 1(Q19) on panel 4A4 (5A5). Transistor Q10 and Q11 (Q19) are wired in series with coil of relay K1, traffic failure interrupts current flow in either transistor Q10 or Q1 1 (Q19), and relay K1 then deenergizes to close contacts 1 and 3. This applies a 12-volt dc bias to transistor Q12 (Q15) on panel 4A5 (5A5), which deenergizes relay K1 on the front panel. When this relay deenergizes, contacts 5 and 7 close, which applies 28-volts ac to TRAFFIC indicator DS1 and terminal B of buzzer DS4. Buzzer DS4 sounds (if OFF contacts of ALARMS BUZZER OFF switch S2 are closed) and TRAFFIC indicator DS1 lights. The operator presses ALARMS BUZZER OFF switch S2 (ON contacts close) and the buzzer deenergizes, TRAFFIC indicator DS1 remains lighted. When the fault is corrected, current flows in transistor Q10 or Q1 l (Q19), and relay K1 energizes to switch its contacts to the alternate position. This causes transistor Q12 (Q15) on panel 4A5 (5A5) to conduct, energizing relay K1, which opens 28-volt ac power input to TRAFFIC indicator DS1 and extinguishes DS1. Buzzer DS4 energizes via terminal 18 of jack J1 on panel 4A1 (5A1) and the arm of ALARMS BUZZER OFF switch S2. When the operator presses ALARMS BUZZER OFF switch S2, the buzzer is de-energized and normal operation is resumed.

c. Overheat Alarm. The TD-203/U (TD-202/U) is cooled by blower B1 that operates from the 115-volt ac line. The blower is energized by the AC POWER switch. Air enters the cabinet through a series of perforations on the right-hand side of the front panel; an air filter is fastened to the inside of the front panel over the perforations. The cooling air is baffled to circulate through the power supply, and it is exhausted by the blower through perforations on the left-hand side of the front

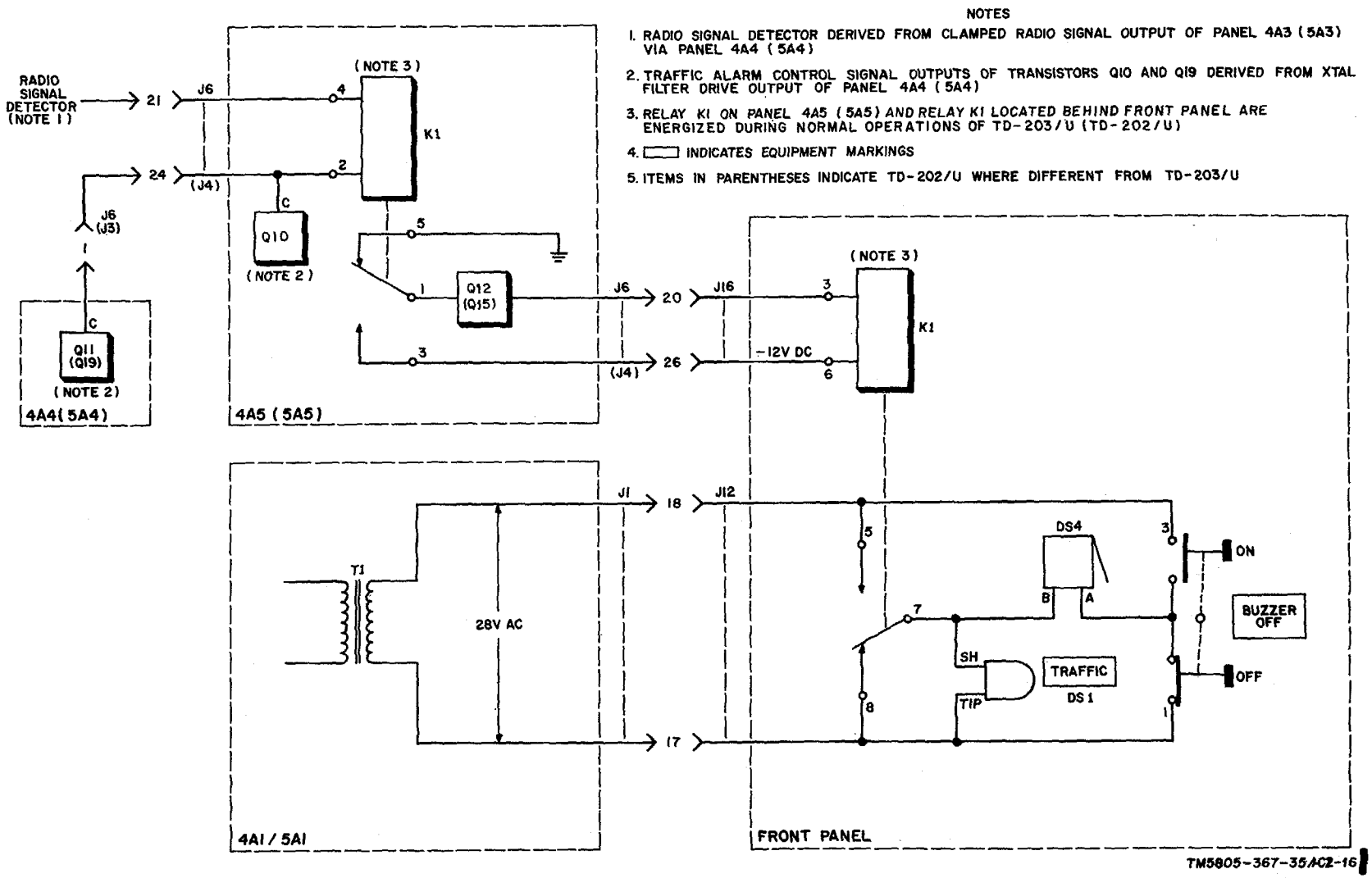


Figure 2-16. Traffic failure alarm network, simplified schematic diagram.

panel. A thermostat is mounted on the inside of the power supply; if the temperature rises above 158 °F., the thermostat closes its contacts to energize ALARMS CHANGE AIR FILTER indicator lamp DS3. In most cases, cleaning or replacing the air filter will restore normal operation.

2-21. Test Circuit (fig. 6-1 or 6-2)

a. General. The test circuit is used to monitor signals and voltage, to locate faulty panels, and to test and align the unit. This circuit consists of monitoring, fault locating, testing, and alignment networks.

b. Monitoring Network. TEST ALIGN meter M1 on the front panel monitors the values of the various signals and supply voltages. The meter has three ranges marked on its scale: a green band, a smaller yellow band, and a black hairline. The application of the signals and voltages to be monitored by the meter are controlled by METER SELECT switch S1.

c. Fault-Locating Network. When METER SELECT switch S1 is at SERV FAC, SERV SEL switch S4 may be operated to check circuits on specific panels. The position letter designations on the SERV SEL switch correspond to monitoring circuits on specific panels. Therefore, an incorrect indication on the TEST ALIGN meter indicates that the circuit on the panel corresponding to the letter designation is defective; for example, when SERV SEL switch S4 is at 0 and METER SELECT switch S1 is at SERV FAC, the order-wire circuit on panel 4A7/5A7 is monitored. An incorrect indication on the TEST ALIGN meter, therefore would indicate that the order-wire circuit on panel 4A7/5A7 is defective.

d. Test-Align Network. The test-align network develops a filtered signal which simulates an input from the radio set. The simulated signal is produced by rerouting the pcm output of the TD-203/U (TD-202/U) via the OPR-TEST switch and through filter FL2, which attenuates the higher frequencies to make the waveshape appear like that of an actual transmitted, dissipated signal. The signal is looped back to FROM RADIO RCVR jack J8, and tests are made to determine if the simulated signal is properly regenerated. The pcm output (to radio xmtr) of terminal 30 (1) or jack J15 (J6) of panel 4A2 (5A2) is applied to the arm of OPR-TEST switch S6, which is mounted on the service facility panel. For normal operation, the switch is in the OPR position, and the signal passes through filter FL3 to TO RADIO XMTR jack J7 for connection to the radio set. In the TEST position, switch S6 reroutes the pcm signal through filter FL2 to front panel TEST OUT jack J2. The simulated signal is then fed back to the TD-203/U (TD-202/U) by connecting an external jumper between TEST OUT jack J2 and FROM RADIO RCVR jack J8.

2-22. RF Filters

The 115-volt ac line voltage to each unit is filtered by filter FL I which reduces any radio frequency (rf) energy that tends to penetrate the leads carrying the line voltage. Filter networks are connected to both sides of the front-panel mounted fuses and to both sides of TEST ALIGN meter M 1. These filter networks are low pass circuits with a cutoff frequency of approximately 150 kc.

CHAPTER 3
DIRECT SUPPORT MAINTENANCE
Section I. TROUBLESHOOTING TD-202/U AND TD-203/U

3-1. General

a. Troubleshooting at direct support maintenance includes all the techniques outlined for organizational maintenance and any special or additional techniques required to isolate a defective part. The direct support maintenance procedures supplement those described in organizational maintenance. The systematic troubleshooting procedures, which begin with the operational and sectional checks performed at an organizational category, must be completed by further localizing and isolating techniques.

b. Troubleshooting at direct support is limited to localizing trouble to chassis or front panel mounted parts (i.e., switches, fuse holders, relays), and repairing or replacing of the defective parts.

c. Troubleshooting can be performed while the equipment is operating as part of a system or, if necessary, after the equipment (or parts of it) has been removed from service. When trouble occurs, certain observations and measurements can be made which will help determine whether the local equipment is at fault or if the trouble exists elsewhere in the system. Usually, when troubleshooting is performed while the equipment is operating as part of a system, it is done at the organizational level (TM 11-5805-367-12). Troubleshooting at direct support is usually performed with the defective unit removed from the equipment with which it is normally associated.

d. Voltage, resistance, or continuity measurements can be performed to localize the trouble to a component mounted on either the chassis or front panel. If the defective part is inaccessible and cannot be repaired or replaced, the chassis should be tagged and sent to higher category maintenance.

Caution: Do not attempt resistance measurements on the plug-in transistorized circuits unless specifically directed in this manual. Read the pertinent instructions before performing resistance and continuity measurements. When measuring resistance, make sure that power is off and all transistorized plug-in panels have been removed from the chassis.

3-2. Test Equipment and Tools Required for Troubleshooting

All the test equipment and tools required for the repair and replacement of parts mounted on the chassis or front panel are listed in the maintenance allocation chart in appendix C of TM 11-5805.367-12.

Section II. ALIGNMENT OF TD-202/U AND TD-203/U

3-3. Test Equipment and Special Tools Required for Alignment

Item	Technical manual
Multiplexer TD-353/U (2 ea.)	TM 11-5805-367-35/3.
Oscilloscope AN/USM-140 Screwdriver (mounted on chassis of TD-202/U and TD-203/U) .	TM 11-6625-535-15.

3-4. TD-203/U Alignment Procedure

a. Test Setup. To prepare the TD-203/U for alignment and adjustment, perform (1) through (5) below; this setup is used with each alignment. Before the TD-203/U is aligned, perform the less critical adjustments as described in chapter 2, section III, of TM 11-5805-367-12. During alignment, use multiplexer units that have passed their respective unit performance tests (para 5-7).

(1) Operate AC POWER switches on the master TD-353/U, slave TD-353/U, and

TD-203/U to OFF, and the OPR-TEST switch on the side panel of the TD-203/ U to TEST.

(2) Connect a 96-channel radio terminal (TM 11-5805-367-12) except for the following: connect the CG 409/U cable from the TEST OUT connector to the FROM RADIO RCVR connector on the TD-203/U front panel instead of to one of the CG-409/U cables going to Radio Set AN/GRC-50 or AN/GRC-66.

(3) Remove panel 4A3 and the extender panel from the TD-203/U.

(4) Attach panel 4A3 to the extender panel and reinsert the extender panel into the jack of the TD-203/U from which panel 4A3 was removed (fig. 3-1).

(5) Connect a cable from the INPUT connector of AN/USM-140 to the SCOPE SYNC connector on the side panel of the slave TD-353/U (fig. 3-1).

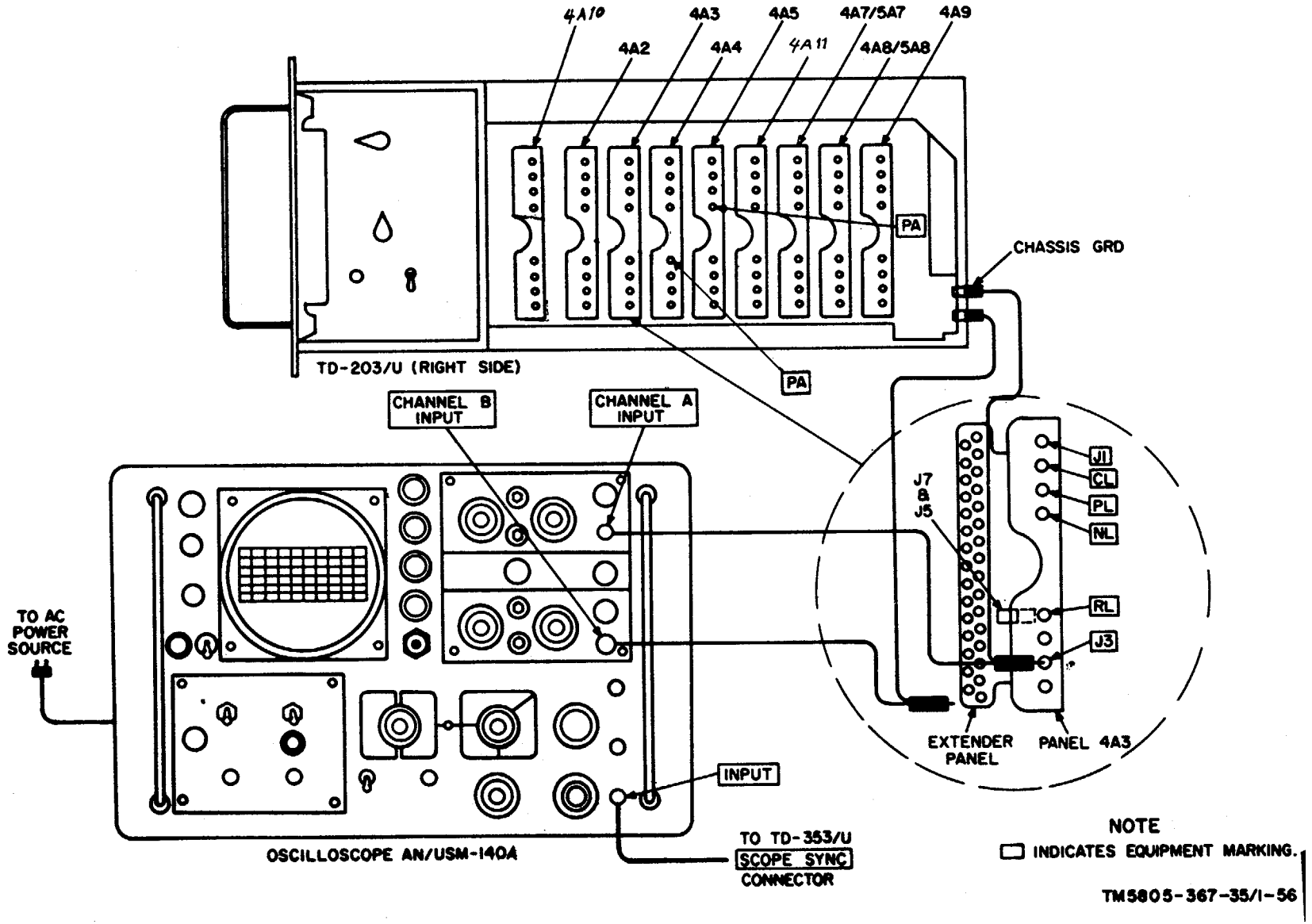


Figure 3-1. TD-203/U alignment procedure setup.

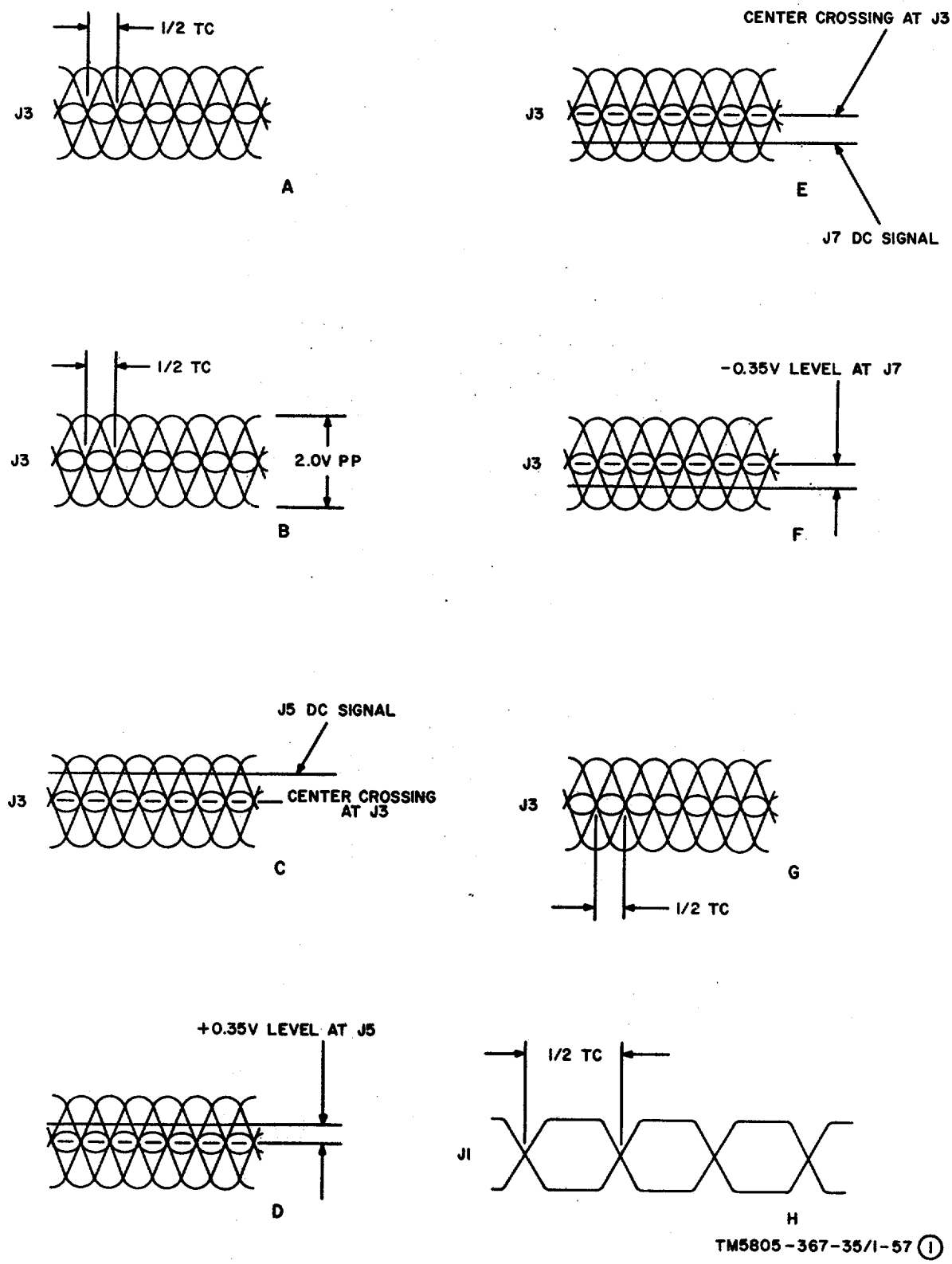
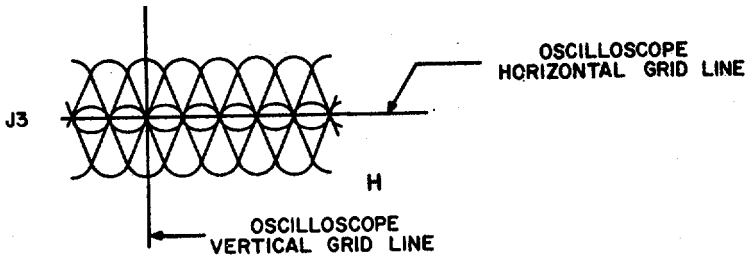
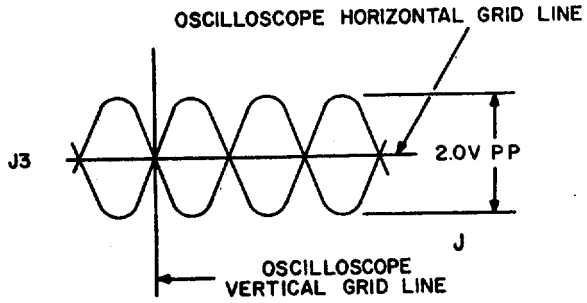
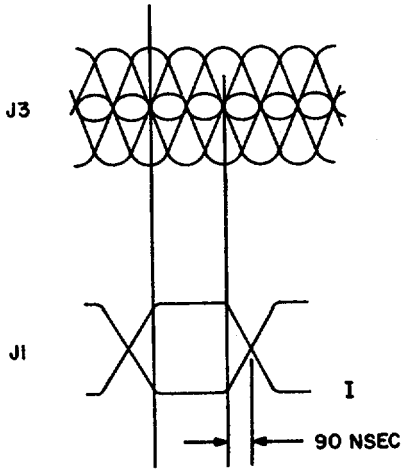
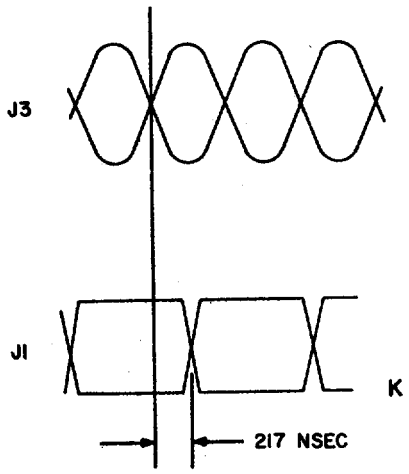


Figure 3-2. TD-203/U alignment procedure waveform indications.









NOTE

$$TC = \frac{1}{2.304\ MC} = 0.434\ USEC$$

TM5805-367-35/1-57 (2)

Figure 3-2.--Continued.

b. Alignment Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Alignment: Procedure	Alignment: Indication
1	Master TD-353/U ADDRESS: MASTER AC POWER: ON Slave TD-353/U ADDRESS: SLAVE AC POWER: ON	TD-203/U METER SELECT: SERV FAC SERV SEL: C TRAFFIC SEL: 96I OPR-TEST: TEST AC POWER. ON	Decision Levels (PL and NL) adjustments Note. If oscilloscope display is not bright enough, disconnect cables from SCOPE: SYNC and TIM OUT connectors on slave TD 353/U. Using a T connector, reconnect both cables from AN/USM-140 INPUT and TD-203/U PCM IN-2 connects) to TIM OUT connector on slave TD-353/U.	
	AN/USM-140 CHOPPED- A-B-ALTERNATE: A-B AC-DC (CHANNEL A and CHANNEL B): DC VERNIER SENSITIVITY (CHANNEL A and CHANNEL B) Outer: .5 VOLTS/CM Inner: max. cw		*a.* Connect CHANNEL A INPUT probe of AN/USM-140 to jack J3 on panel 4A3 and observe waveform on AN/USM-140.	*a.* AN/USM-140 indicates waveform as shown in A, figure 3-2.
			b. While observing J3 waveform on AN/ USM-140, adjust RL control on panel 4A3 for a peak-to-peak amplitude of 2 volts (4-cm deflection)	*b.* AN/USM-140 indicates waveform similar to that shown in B, figure 3-2.
			c. Adjust CL control on panel 4A3 for performance standard.	*c*. TEST ALIGN meter indicates maximum deflection to right.
	EXTERNAL VERNIER HORIZONTAL DISPLAY INTERNAL SWEEP- X1 VERNIER SWEEPTIME: .1 MICRO-SECON D/ CM SWEEP MODE TRIGGER SOURCE: EXT AC		*d.* Connect CHANNEL B INPUT probe of AN/USM-14o momentarily to jack J3 on panel 4A3 (fig. 3-1) and observe waveforms on AN/USM-140. Adjust AN/ USM-140 controls (VERTICAL POSITION and HORIZONTAL POSITION) for a superimposed oscilloscope pattern.	*d.* AN/USM-140 indicates identical waveforms on each channel similar to that shown in A, figure 3-2.
			e. Connect CHANNEL B INPUT probe of AN/USM-140 to jack J5 on panel 4A3 and observe waveforms on AN/USM-140.	*e.* AN/USM-140 indicates dual trace waveforms similar to those shown in C, figure 3-2.
			f. While observing dual trace waveforms on AN/USM-140, adjust PL control on panel 4A3 80 that the dc voltage level of J5 waveform is 0.35 volt above the dc level of center crossings of J3 waveform.	*f.* AN/USM-140 indicates dual trace waveforms similar to those shown in D, figure 3-2.
	POWER: ON		*g.* Disconnect CHANNEL B INPUT probe of AN/USM-140 from jack J5 on panel 4A3.	*g.* None.
			h. Connect CHANNEL B INPUT probe of AN/USM-140 to jack J7 on panel 4A3 and observe waveforms on AN/ USM-140.	*h*. AN/USM-140 indicates dual trace waveforms similar to those shown in E, figure 3-2.
			i. While observing dual trace waveforms	*i.* AN/USM-140 indicates dual

			on AN/USM-140, adjust NL control on panel 4A3 80 that the dc voltage level of J7 waveform is 0.35 volt below the dc level of center crossings of J3 waveform.	trace waveforms similar to those shown in F. figure 3-2
			j. Disconnect CHANNEL A and CHANNEL B INPUT probes of AN/USM-140 from jacks J3 and J7 on panel 4A3, respectively.	*j.* None.
			96-channel timing phase (PA) *adjustment*	
2	No change required.	*a.* No change required.	*a.* Connect CHANNEL A and CHANNEL B INPUT probes of AN/USM-140 to jacks J1 and J3 on panel 4A3, respectively, and observe waveforms on AN/ USM-140.	*a*. AN/USM-140 indicates two waveforms similar to those shown in G. Figure 3-2.
	.	*b*. No change required.	*b*. While observing waveforms on AN/ USM-140, vertically center J3 waveform and line up a center crossing on J3 waveform on a vertical grid line.	*b.* AN/USM-140 indicates waveform position similar to that shown in H. figure 3-2.
		c. Set OPR-TEST switch to OPR.	*c*. Terminate TD-203/D TO RADIO connector in 51 ohms Observe waveform at TO- RADIO and adjust capacitor 4A2C7 until periods equal each other and 1/2 TC	*c.* AN/USML140 indicates waveform position similar to that Shown in H, fig. 3-2.
			c. While observing waveforms on AN/ USM-140, adjust PA control on panel 4A5 so that center crossing point of J1 waveform lags center crossing point of J3 waveform by 90 ns	*c*. AN/USM-140 indicates two waveforms similar to those shown in I, figure 3-2.
3	No change required	No change required except: TD-203/U TRAFFIC SEL: 48	*48-channel timing phase* (PA) *adjustment*	
			a. While observing waveforms on AN/ USM-140, vertically center J3 waveform and line up center crossings on J3 waveform on a vertical grid line.	*a* AN/USM-140 indicates waveform position similar to that shown in J, figure 3-2.
			b. While observing waveforms on AN/ USM-140, adjust PA control on panel 4A4 so that center crossing point of J1 waveform lags center crossing point of J3 waveform by 217 ns	*b.* AN/USM-140 indicates two waveforms similar to those shown in K, figure 3-2
			c. Disconnect CHANNEL A and CHANNEL B INPUT probes of AN/USM-140 from jacks J1 and J3 on panel 4A3, respectively.	*c.* None.
			d. Operate AC POWER switch to OFF and remove panel 4A3 and extender panel. Separate the panels and reinsert them in their respective jacks in the TD-203/U.	*d.* None.

3-5. TD-202/U Alignment Procedure

a. Test Setup. To prepare the TD-202/U for alignment and adjustment, perform (1) through (5) below; this setup is used with each alignment. Before the TD-202/U is aligned, perform the less critical adjustments as described in chapter 2, section III, of TM 11-5805-367-12. During alignment, use multiplexer units that have passed their respective unit performance tests (para 5-5).

(1) Operate AC POWER switches on the master TD-352/U, slave TD-352/U, and TD-202/U to OFF, and the OPR-TEST switch on the side panel of the TD-202/U to TEST.

(2) Connect a 24-channel radio terminal (TM 11-5805-367-12) except for the following: connect the CG-409/U cable from the TEST OUT connector to the FROM RADIO RCVR connector on the TD202/U front panel instead of to one of the CG 409 /U cables going to Radio Set AN/GRC-50 or AN/GRC-66.

(3) Remove panel 5A3 and the extender panel from the TD-202/U.

(4) Attach panel 5A3 to the extender panel and reinsert the extender panel into the jack of the TD-202/U from which panel 5A3 was removed (fig.3-3).

(5) Connect a cable from the INPUT connector of AN/I SM-140 to the SCOPE SYNC connector on the side panel of the slave TD-352/U (fig. 3-3).

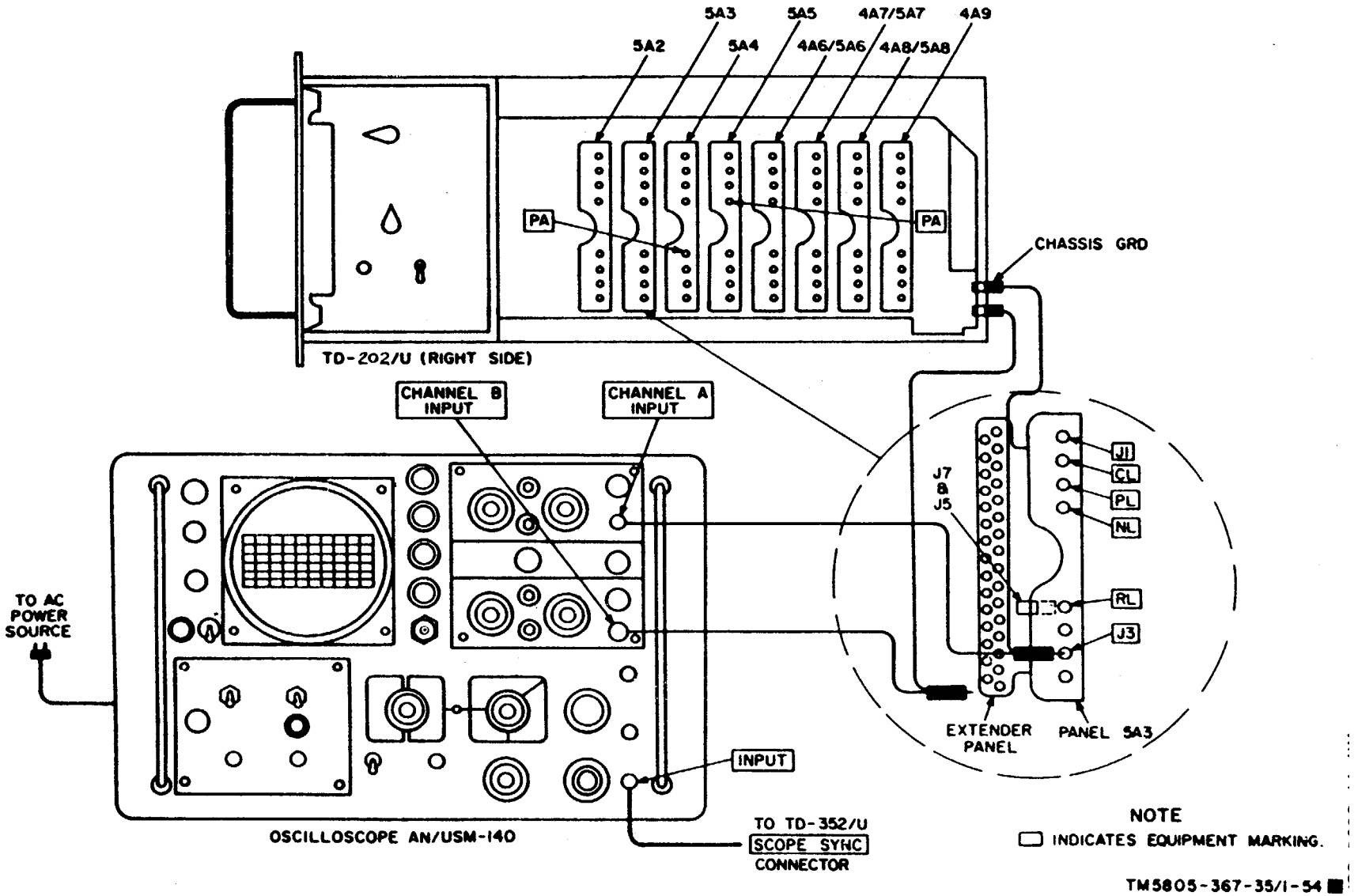


Figure 3-3. TD-202/U alignment procedure

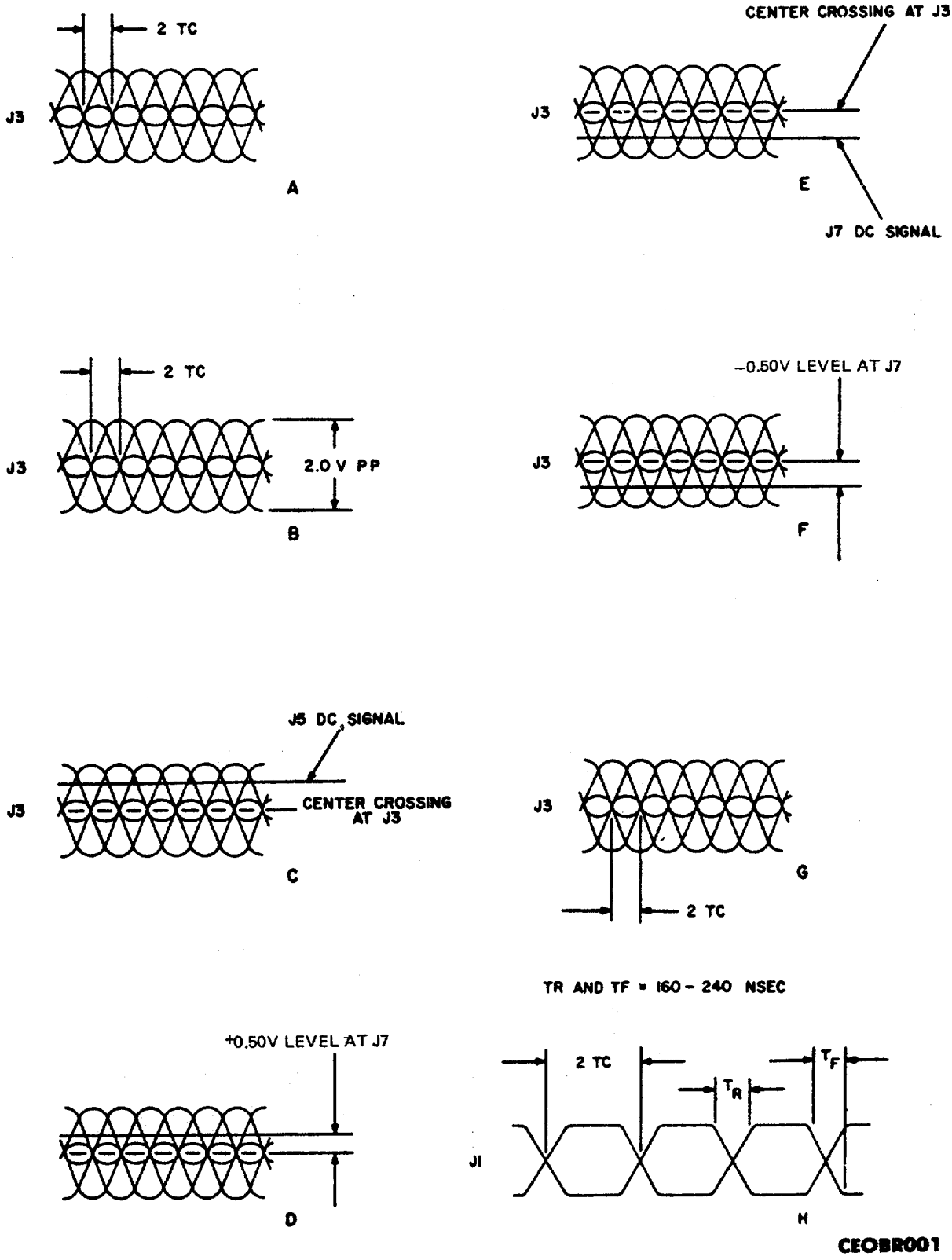


Figure 3-4. TD-202/U alignment procedure idealized waveforms

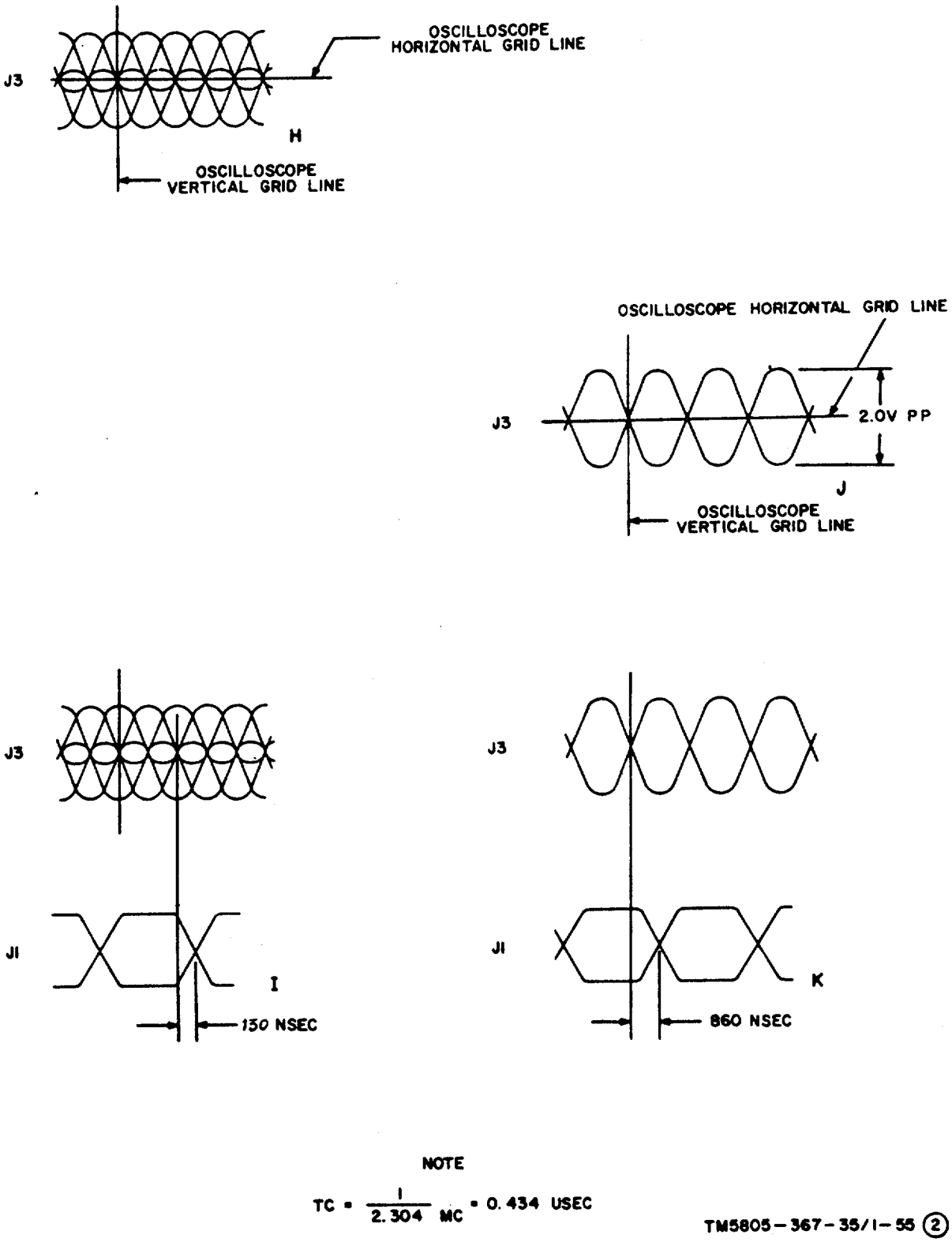


Figure 3-4. TD-202/U alignment procedure idealized waveforms (Continued)

b. Alignment Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Alignment: Procedure	Alignment: Indication
1	Master TD-352/U ADDRESS: MASTER AC POWER: ON Slave TD-352/U ADDRESS: SLAVE AC POWER: ON	TD-202/U METER SELECT: SERV FAC SERV SEL: C TRAFFIC SEL: 24I OPR-TEST: TEST AC POWER: ON	Decision levels (PL and NL) adjustments Note If oscilloscope display is not bright enough, disconnect cables from SCOPE SYNC and TIM OUT connectors on slave TD 352/U. Using a T-connector, reconnect both cables (from AN/USM-140 INPUT and TD-202/U TIM IN-2 connectors) to TIM OUT connector on slave TD-352/U.	
	AN/USM-140 CHOPPED A-B ALTERNATE: A-B AC-DC (CHANNEL A and CHANNEL B): DC VERNIER SENSITIVITY (CHANNEL A and CHANNEL B) Outer: .5 VOLTS/CM Inner: max cw EXTERNAL VERNIER HORIZONTAL DIS-PLAY INTERNAL SWEEP: X1 VERNIER SWEEP TIME : 0.5 MICROSECONDS/CM SWEEP MODE TRIGGER S0URCE: EXT AC POWER: ON		*a.* Connect CHANNEL A INPUT probe of AN/USM-140 to jack J3 on panel 5A3 and observe waveform on AN/USM-140. *b.* While observing J3 waveform on AN/ USM-140, adjust RL control on panel 5A3 for a peak-to-peak amplitude of 2 volts (4-cm deflection). c. Adjust CL control on panel 5A3 for performance standard. *d.* Connect CHANNEL B INPUT probe of AN/USM-140 momentarily to jack J3 on panel 5A3 (fig. 3-3) and observe waveforms on AN/USM-140. Adjust AN/USM-140controb (VERTICAL POSITION and HORIZONTAL POSITION) for a superimposed oscilloscope pattern. e. Connect CHANNEL B INPUT probe of AN/USM-140 to jack J5 on panel 5A3 and observe waveforms on AN/US M-140. *f.* While observing dual trace waveforms on AN/USM-140, adjust PL control on panel 5A3 NO that the dc voltage level of J5 waveform IN 0.50 volt above the dc level of center crossings of J3 waveform. *g.* Disconnect CHANNEL B INPUT UT probe of AN/USM-140 from jack J5 on panel 5A3. *h.* Connect CHANNEL B INPUT probe of AN/USM-140 to jack J7 on panel 5A3	*a.* AN/USM indicates waveform as shown in A, figure 3-4. *b.* AN/USM-140 indicates a waveform similar to that shown in B, figure 3-4. *c.* TEST ALIGN meter indicates maximum deflection to right. *d.* AN/USM-140 indicates identical waveforms on each channel similar to that shown in A, figure 3-4. *e.* AN/USM-140 indicates dual trace waveforms similar to those shown in C, figure 3-4. *f.* AN/USM-140 indicates dual trace waveforms similar to those shown in D. figure 3-4. *g.* None. *h.* AN/USM-140 indicates dual trace waveforms similar to those

			and observe waveforms on AN/USM 140. *i.* While observing dual trace waveforms on AN/USM-140, adjust NL, control on panel 5A3 so that the dc voltage level of J7 waveform is 0.50 volt below the dc level of center crossings of J3 waveform. *j.* Disconnect CHANNEL A an] CHANNEL B INPUT probes of AN/USM-140 from jacks J3 and J7 on panel 5A3, respectively.	shown in E, figure 3-4. *i.* AN/USM-140 indicates dual trace waveforms similar to those shown in F, figure 3-4. *j.* None.
2	Set EXTERNAL VERNIER HORIZONTAL DISPLAY INTERNAL SWEEP control to X5.	No change required.	24-channel timing phase (PA) adjustment *a*. Connect CHANNEL A and CHANNEL B INPUT probes of AN/USM-140 to jacks J1 and J3 on panel 5A3, respectively, and observe waveforms on AN/ USM- 140. *b.* While observing waveforms on AN/USM-140, vertically center J3 waveform and line up a center crossing on J3 waveform on a vertical grid line. *c*. While observing waveforms on AN/USM-140, adjust PA control on panel 5A5 so that center crossing point of J1 wave form lags center crossing point of J3 waveform by 130 ns.	*a*. AN/USM-140 indicates two waveforms similar to those shown in G, Figure 3-4. *b*. AN/USM-140 indicates waveform position similar to that shown in H, Figure 3-4. *c*. AN/USM-140 indicates two waveforms similar to those shown in I, figure 3-4.
3	No change required.	No change required except: TD-202/U TRAFFIC SEL: 12	12 channel timing phase (PA) adjustment *a*. While observing waveforms on AN/USM-140, vertically center J3 waveform and line up center crossing on J3 waveform on a vertical grid line. *b*. While observing waveforms on AN/USM-140, adjust PA control on panel 5A4 so that center crossing point of J1 waveform lags center crossing point of J3 waveform by 870 ns *c*. Disconnect CHANNEL A and CHANNEL B INPUT probes of AN/USM-140 from jacks J1 and J3 on panel 5A3, respectively. *d*. Operate AC POWER switch to OFF and remove panel 5A3 and extender panel. Separate the panels and reinsert them in their respective jacks in the TD-202/U.	*a*. AN/USM-140 indicates waveform position similar to that shown in J, figure 3-4. *b*. AN/USM-140 indicates two waveforms similar to those shown in K, figure 3-4. *c*. None. *d.* None.

CHAPTER 4
GENERAL SUPPORT MAINTENANCE

***Warning**:* When troubleshooting or making repairs in this equipment, be careful not to contact 115-volt ac connections. Use insulated test probes when making voltage measurements. Always disconnect the power cord from a unit before touching any of the internal parts.

4-1. Scope of General Support Maintenance Procedures

General support maintenance consists of troubleshooting, repairing and testing defective plug-in panels returned by organizational maintenance personnel. Troubleshooting procedures for each type of plug-in panel of the TD-202/U and TD903/U are provided in paragraphs 4-6 through 4-18. Repair procedures are covered in TB SIG-929. The testing of a repaired plug-in panel is accomplished by installing the plug-in panel in a TD-202/U or TD-203/U and performing the appropriate performance test (para 5-5 or 5-7).

4-2. Organization of Troubleshooting Procedures

a. Sectionalization. Sectionalizing faults in the TD-202/U or TD-203/U consists of tracing the source of the trouble to one or more plug-in panels, or to the unit chassis. This is normally done at the organizational category in accordance with the procedures contained in TM 11-5805-367-12. If panel substitution at the organizational category does not sectionalize the trouble, the unit chassis must undergo the direct support procedures given in chapter 3 of this manual. When a fault is sectionalized to a panel, either at the organizational category or, as a result of further checks, at direct support, that panel is sent to general support maintenance for localization of the trouble.

b. Localization. Localization of faults on the panels consists of tracing the source of trouble to the defective stage. This is done by using the troubleshooting charts (para 4-6 -4-18). A schematic diagram for each panel is included at the rear of this manual, accompanied by waveforms for all the points used to localize any fault listed in the corresponding troubleshooting chart. The general conditions for the use of the charts are given in paragraph 4-3, and information relative to the use of the waveform is included in paragraph 4-4.

c. Isolation. Isolation of a faulty part in a defective Stage is accomplished by making voltage and waveform measurements. A voltage and waveform chart is provided at the end of each panel troubleshooting chart.

***Note*.** To isolate short circuits, it may be necessary to remove wires from terminals.

4-3. Use of Troubleshooting Charts

a. To localize a fault to a defective stage, install the panel on an electrical test (extender) panel. Remove the corresponding panel in a TD-202/U or TD-203/U and insert the extender and faulty panel combination in place of the removed panel. The only exception to this procedure is the power supply panels, which require the use of extender cables. It is important that tile notes pertaining to troubleshooting dual-type panels (that is, panels used in either the TD-202/U or TD-203/U, or used for both transmit and receive functions) be strictly followed.

b. The probable cause and corrective action listed for any given symptom assumes that all previous symptoms are negative. This makes it unnecessary to list redundant information in each succeeding symptom. For example, if a panel exhibits a symptom given as item 10, the symptoms of items 1 through 9 must be proved negative by test before the corrective action recommended for item 10 is followed.

c. If a dual-unit panel is to be investigated for faults, it must be checked completely in both TD202/U and TD-203/U bench test units since differences exist in timing-signal frequencies, input and output connections, etc.

d. Only terminal numbers of panel connectors are listed in the charts. The connector designator is stipulated to be that shown on the corresponding schematic diagram included at the rear of this manual.

e. Reference to a transistor in a defective stage should be interpreted to include all parts of that stage.

f. Parts can be located by reference to the appropriate top panel view figure.

g. After replacement of any part, check to be sure that no other trouble exists.

h. After a panel is repaired proceed as follows:

(1) Insert the panel in the TD-202/U or TD203/U and check its alignment, using the procedures given in chapter 3.

(2) Perform the unit performance tests given in chapter 5.

4-4. Use of Waveforms

a. The principal factors that affect the waveforms are the oscilloscope grid values: sweep time and vertical sensitivity. Other conditions affecting the waveform obtained are given in the troubleshooting charts where applicable, and include the test requirements ((1) through (4) below) that must be met to obtain the expected waveform.

(1) Modulating frequencies used.
(2) TD-202/U or TD-203/U connections.
(3) Oscilloscope synchronization requirements.
(4) TD-202/U or TD-203/U control switch settings.

***Note*.** The signal voltage (amplitude) and period can be calculated from the vertical sensitivity and horizontal time information given with the waveform.

b. The waveforms obtained on the oscilloscope should be compared with the reference waveforms. When a waveform is incorrect or absent, make a detailed check of the appropriate stage, using the instructions given in the troubleshooting chart. Supplementary voltage and waveform data for the modules and transistors of the panel are also given after each chart for use in isolating faulty parts.

4-5. Test Equipment and Tools Required

The following test equipment and materials should be provided for troubleshooting the TD202/U and TD-203/U.

a. Frequency Meter AN/TSM-16.
b. Multimeter TS-352/U.
c. Multimeter ME-26B/U.
d. Multiplexers TD-352/U, TD-353/U, TD202/U, TD-203/U, and TD-204/U.
e. Oscilloscope AN/USM-140.
f. Signal Generator SG-71/FCC.
g. Spectrum Analyzer TS-723/U.
h. Test Set TS-140/PCM.
i. Test Set, Telephone TS-1323/PT.
j. Test Set, Transistor TS-1836/U.
k. Test Set, Transmission TS-762/U.
l. Voltmeter ME-30B/U.
m. Voltmeter TS-443/U.
n. Transformer, Variable Power TF-171/USM.
o. Screwdriver (mounted in TD-202/U and TD-203/U) .
p. Tool Kit, Radio Repairman TK-115/U.
q. Tool Kit, Electronic Equipment TK-105/G.

4-6. Panel 4A1 /5A1, Troubleshooting

a. Troubleshooting Chart (fig. 6-3, 6-4, 6-20).

Item No.	symptom	Probable trouble	Correction
	Caution: **Before making dc resistance measurements or continuity checks, make sure that power is turned off.**		
1	Primary power fuses on front panel of TD-202/U or TD203/U keep blowing.	a. Power supply input terminals 14 and 15 shorted.	a. Inspect terminals at jack J1 for lodged foreign material.
		b. Rectifier diode shorted in secondary.	b. Check rectifier diodes.
2	No power supply output with primary and secondary fuses intact.	Open primary winding on T1.	Using ohmmeter, check resistance across terminals 1 and 2 of T1. If reading exceeds approximately 20 ohms, winding is defective.

Item No.	symptom	Probable trouble	Correction
3	Fuses keep blowing in n single power supply.	a. Short to ground in associated regulator circuit.	a. Using transistor tester or ohmmeter, check associated series regulator from emitter to collector.
		b. Short to ground in associated driver and differential amplifier circuit.	b. Check for short to ground in associated driver and differential amplifier circuit.
		c. Short to ground across unregulated input.	c. Check for short to ground across unregulated input.
4	Fuses fail to blow in single power supply when output terminal is short circuited to ground or when output current drain is excessive.	a. Defective associated fuse.	a. Check fuse for continuity or wrong value.
		b. Defective fuseholder.	b. Check fuseholder.
5	High output ripple or abnormal | voltage regulation at single power supply output.	a. Defective filter capacitor, filter inductor, or rectifier diode in associated power supply.	a. Check rectifier diode, filter capacitor, and rectifier diodes.
		b. Defective reference diode in associated regulator circuit.	b. Using dc voltmeter, measure drop across reference diode in question. If reading is not 6.2 volts±0.3, diode is defective.
6	No output across a single power supply with associated secondary fuse intact.	a. Defective associated secondary winding on T1 or open filter inductor.	a. Using ohmmeter, check T1 secondary winding or filter inductor in question.
		b. Short or open in associated regulator circuit.	b. Starting at regulator input and working toward output, perform the following: check for open or short in transistors and associated wiring; check connections to series regulator transistors, driver transistors, and voltage potentiometers; check voltages, continuity, and resistance on transistors and potentiometers to various terminals.
7	Abnormal current at a single power supply meter output.	Defective associated resistor.	Check resistor in question for continuity or wrong value.

b. *Troubleshooting Incorrect Regulator-Outputs*. If a regulator circuit has an incorrect output voltage, check its respective reference zener diode first. If this fails to correct the output voltage, proceed with the measurements in (1), (2), and (3) below, depending on which supply is defective.

(1) *Troubleshooting +10-volt supply*. Measure the voltage at the base of transistor Q3. Compare this voltage with the voltages at the base of transistor Q4. If voltages are equal, try to adjust potentiometer R1 (+ 10V VOLTAGE ADJUSTMENTS). If transistor Q3 andQ4 base voltages remain equal, check for continuity and resistance in circuit from the base of transistor Q3, through potentiometer R1, to +10-volt and ground side of regulator. If the base signals are not equal, perform the voltage measurements in the chart below.

Note. When making use of the following charts, select row (positive, negative, or normal) based upon the condition found in the detective supply; then proceed across the row in the order given. All voltages listed in the charts are approximate.

Voltages with respect to + 10-volt bus

Base of Q3 with respect to Q4 base	Collector Q3	Emitter Q2	Emitter Q1
Positive	-12.5 to -15.	-12.2 to -14.7.	-11.9 to -14.4.
Negative	-6	-5.7	-5.4.
Normal	-10.6	-10.3	-10.0.

(2) *Troubleshooting +45-volt supply.* Measure the voltage at the base of transistor Q7. Compare this voltage with the voltage at the base of transistor Q8. If voltages are equal, try to adjust potentiometer R9 (+ 4.5V VOLTAGE ADJUSTMENTS). If transistors Q7 and Q8 base voltages remain equal, check for continuity and resistance in circuit from the base of transistor Q7, through potentiometer R9, to +4.5-volt and ground side of regulator! If the base signals are not equal, perform the voltage measurements in the chart below.

(3) *Troubleshooting -4.5-volt supply.* Measure the voltage at the base of transistor Q11. Compare this voltage with the voltage at the base of transistor Q10. If voltages are equal, try to adjust potentiometer R18 (-4.5V VOLTAGE ADJUSTMENTS). If transistor Q11 and Q12 base voltages remain equal, check for continuity and resistance in circuit from the base of transistor Q11, through potentiometer R18, to -4.5- volt and ground side of regulator. If the base signals are not equal, perform the voltage measurements in the chart below.

Voltages with respect to ±4.5-volt bus				*Voltage with respect to ground*			
Base of Q7 with respect to Q8 base	Collector Q7	Emitter Q6	Emitter Q5	Base of Q11 with respect to Q12 base	Collector Q11	Emitter Q10	Emitter Q9
Positive	-6 to -8	-5.7 to -7.7.	-5.4 to -7.4.	Positive	-6 to -8	-5.7 to -7.7.	-5.4 to -7.4.
Negative	-3	-2.7	-2.4.	Negative	-3	-2.7	-2.4.
Normal	-5.1	-4.8	-4.5.	Normal	-5.1	-4.8	-4.5.

4-7. Panel 5A2, Troubleshooting

a. Troubleshooting Chart (fig. 6-12, 6-28, 6-40**)**

Item No.	symptom	Probable trouble	Correction
1	No or incorrect wave form at J1 or terminal 1 (TO RADIO XMTR) with TRAFFIC SEL switch operated to 12 and OL control approximately midrange.	Q15 defective.	Check signal at base of Q15. If present, check Q15. If not present, proceed to step 2.
2	No signal at base of Q15.	Q11, Q12, Q13, Q14 defective.	Check signals at emitters of Q9 and Q10. If present at both emitters, check Q11, Q12, Q13, and Q14. If not present at one or both emitters, proceed to step 3.
3	No signal at emitter of either Q9 or Q10, or at both emitters.	Q9, Q10 defective.	Check signals at bases of Q9 and Q10. If present, check Q9 and Q10. If not present at one or both bases, proceed to step 4.
4	No signal at base of either Q9 or Q10, or at both bases.	Q1, Q2 defective.	Check signal at emitter of Q1. If present, check Q1 and Q2. If not present, proceed to step 5.
5	No signal at emitter of Q1.	Q3, Q4, Q5, CR4, CR2 defective.	Check signal at base of Q3. If present, check Q3, Q4, Q5, CR4, and CR2. If not present, proceed to step 6.
6	No signal at base of Q3.	DL1 defective.	Check waveform at J2 (terminal 5). If correct, check DL1. If incorrect or missing, proceed to step 7.

Item No.	symptom	Probable trouble	Correction
7	No signal or incorrect signal at J2 or terminal 5.	Q16, Q17, DL2 defective.	Check signal at base of Q16. If present, check Q16 and Q17. If not present, check DL2.
8	Incorrect waveform at terminal 1with TRAFFIC SEL switch at 24I (pcm-2 not interleaved with pcm-1).	Q18, Q19, Q20, CR26, CR27 defective.	Check signal at emitter of Q7. If not present, check Q18, Q19, Q20, CR26, and CR27. If present, proceed to step 9.
9	Incorrect waveform at terminal 1, but with signal present at emitter of Q7 (pcm-2 not interleaved with pcm-1).	Q7, Q8 defective.	Check signal at J3 (base of Q7). If present, check Q7 and Q8. If not present, proceed to step 10.
10	No signal at J3 (base of Q7).	Q6 defective.	Check signal at base of Q6. If present, check Q6. If not present, proceed to step 11.
11	No signal at base of Q6.	Q21, Q22 defective.	Check signal at base, of Q21. If present, check Q21 and Q22. If not present, proceed to step 12.
12	No signal at base of Q21.	CR15, CR16, CR17 defective or CR18, CRl9, CR20 defective.	Operation TRAFFIC SEL switch to 24R. If signal at base of Q21 is still not present, check CR15, CR16, and CR17. If signal at base of Q21 is present, check CR18, CR19, and CR20.
13	Incorrect waveform at terminal 1 with TRAFFIC SEL at 24I (faulty pcm-2 interleaved with pcm-1).	Q24, Q25, Q26, CR24, CR25, CR28, or CR29 defective.	Check waveform at emitter of Q23. If present, check Q24, Q25, Q26,CR24, CR25, CR28, and CR29.If not present, proceed to step 14.
14	No signal at emitter of Q23.	Q23 defective.	Check Q23.
15	Pcm in-1 meter (terminal 29) does not read in green area of TEST ALIGN meter.	CR2, CR4, C2, or C4 defective.	Check CR2, CR4, C2, and C4.
16	Pcm in-2 meter (terminals 8 and 9) does not read in green area on TEST ALIGN meter.	CR26, CR27, C22, or C4 defective.	Check CR26, CR27, C22, and C4.
17	TO RADIO XMTR meter (terminal 6) does not read in green area on TEST ALIGN meter.	CR8, CR9, C7, or C8 defective.	Check CR8, CR9, C7, and C8.
18	Timing in meter (terminal 4) does not read in green area on TEST ALIGN meter, with correct signal at J2	CR12 or C10 defective.	Check CR12 and C10.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector	Transistor	Base	Emitter	Collector
Q1	5, fig. 6-40	7, fig. 6-40	8, fig. 6-40.	Q14	0±0.1	21, fig. 6-40	24, fig. 6-40
Q2	-1.0±0.1	7, fig. 6-40	9, fig. 6-40.	Q15	24, fig. 6-40 .	25, fig. 6-40	26, fig. 6-40
Q3	10, fig. 6-40	11, fig. 6-40	7, fig. 6-40.	Q16	27, fig. 6-40 .	+0.2 ± 0.05	28, fig. 6-40.
Q4	+4.5±0.5 or +0.24 ±0. 1 [a]	11, fig. 6-40 .	0±0.1	Q17	28, fig. 6-40	29, fig. 6-40	
				Q18	31, fig. 6-40	30, fig. 6-40	15, fig. 6-40.
				Q19	+4.5±0.5 or +0.3 ±0.1 [b.]	30, fig. 6-40	0±0.1.
Q5	-1.08±0.1 or +0.38 ±0.1 [a]	-0.3±0.1 or +0.24 ±0.1 [a]	+4.5±0.5 or +0.24 ±0.1 [a]	Q20	-1.0±0.1 or +0.42 ± 0.1 [b]	-0.3± +0.31 ±0.1 [b]	+4.5±0.5 or +0.42 ±0.1 [b]
Q6	13, fig. 6-40	12, fig. 6-40	14, fig. 6-40				
Q7	4, fig. 6-40	15, fig. 6-40	8, fig. 6-40				
Q8	-1.0±0.1	15, fig. 6-40	9, fig. 6-40.	Q21	33, fig. 6-40	32, fig. 6-40	34, fig. 6-40.
Q9	9, fig. 6-40	16, fig. 6-40	-4.5±0.135.	Q22	-1.0± 0.1	32, fig. 6-40	40, fig. 6-40.
Q10	8, fig. 6-40	17, fig. 6-40	-4.5± 0.135.	Q23	36, fig. 6-40	35, fig. 6-40	-4.5±0.135
Q11	0±0.1	18, fig. 6-40	19, fig. 6-40	Q24	37, fig. 6-40	0.4±0.05	38, fig. 6-40
Q12	20, fig. 6-40	18, fig. 6-40	39, fig. 6-40	Q25	0 to -0 3 [c]	0±0.1	0 to-0.3 [c]
Q13	22, fig. 6-40	21, fig. 6-40	23, fig. 6-40.	Q26	+0.18 ± 0.05 [c]	0±0.1	-39±0.4 [c]

a Remove PCM-1 connector. Reconnect after making measurement.

b Remove PCM IN-2 connector. Reconnect after making measurement.

c Depending on the state of flip-flop Q25, Q26, voltage readings may be interchanged between bQ25 and bQ26, and between cQ25 and cQ26.

4-8. Panel 5A3, Troubleshooting

a. Troubleshooting Chart (fig. 6-13, 6-29, 6-41).

Item No.	symptom	Probable trouble	Correction
1	No waveform or incorrect waveform at J3 or terminal 9 (clamped radio signal).	Q5, Q6, Q7 defective	Check signal at base of Q5. If present, check Q5, Q6, and Q7. If not present, proceed to step 2.
2	No signal at base of Q5	Q3, Q4, CR1, CR2 defective	Check voltage at base of Q4. If present, check Q3, Q4, CR1 and CR2. If not present, proceed to step 3.
3	Incorrect voltage at base of Q4	Q1, Q2, C1, or C4 defective	Check voltage at base of Q1. If correct, check Q1 and Q2. If incorrect, check Q2, C1, and C4.
4	No signal or incorrect signal at terminal 26 (center level), terminal 27 (*ternary pos level*), and terminal 28 (*ternary neg level*) with correct signal present at J3.	Positive peak detector (Q30 through Q33) or negative peak detector (Q34 through Q37) defective	Check dc levels at J5, J7, and terminal 26 with TRAFFIC SEL switch first at 12 and then at 24 (I, S, or R), as described in the note below. If dc levels incorrect, adjust R83, R85, and R84. If correct dc level at J5, J7, or terminal 26 cannot be attained with R83, R85, and R84 adjustments, respectively, proceed to steps 5 and 6.

Item No.	Symptom	Probable trouble	Correction
5	Correct dc levels cannot be attained with adjustments.	Positive peak detector (Q30 through Q33) defective.	Check that dc level or signal at terminal 31 (emitter of Q33) is equal to positive peaks of signal at J3. If incorrect, check Q30 through Q33. If correct, proceed to step 6.
6	Correct dc levels cannot be attained with adjustment.	Negative peak detector (Q34 through Q37) defective.	Check that dc level of signal at terminal 30 (emitter of Q37)is equal to negative peaks of signal at J3. If incorrect, check Q34 through Q37. If correct, proceed to step 7.
7	Correct dc levels at terminals 31 and 30 (emitters of Q33 and Q37), but correct dc levels at J5 and J7 cannot be attained with R83 and R85 adjustments, or correct dc level at terminal 26 cannot be attained with R84 adjustment.	R83, R85,R84 defective.	Check R83, R85, and R84.
8	No waveform or incorrect wave-form at J1 or terminal 22 (recovered pcm-1) and/or terminal 20 (recovered pcm-2) with correct signals present at J3, J5, and J7.	Decision circuits or flip-flop defective	Check signals at J2,J4, and J6 as described in notes 1 and 2 below. If signals at J2 and J4 arc incorrect, proceed to step 9. If signals at J2 and J6 arc incorrect, proceed to step 10. If signals at J2,J4, and J6 are correct, proceed to step 11.

Note

1. With TRAFFIC SEL switch at 12, check for: no signal at J2; positive-going timing pulses at J4,and no pulses at J6 during the period that the waveform at J3 is undergoing a positive excursion; positive-going timing pulses at J6 and no pulses at J4 during the period that the waveform at J3 is undergoing a negative excursion.
2. With the TRAFFIC SEL switch at 24 (I, S. or R), cheek for: positive-going pulses when the waveform at J3 falls between the dc levels of J5 and J7; positive-going pulses at J4 only when the waveform at J3 is above the dc level of J5; positive-going pulses at J6 only when the waveform at J3 is below the dc level of J7.

9	Incorrect signal at J2 and/or J4	Decision circuit Q8 through Q13, Q20 defective	, Check Q8 through Q13 and Q20 as described in notes 1 through 3 below.

Note:

1. With TRAFFIC SEL switch at 12, perform the following checks during the period that the waveform at J3 is undergoing a positive excursion:

a. Check for a negative-going pulse (or pulses) at collator of Q10 and for a positive-going pulse (or pulses) at collector of Q11. If Incorrect indicators are obtained, check Q10 and Q11.

b. Check for a positive-going pulse (or pulses) at collector of Q9 and for no signal at collector of Q12. If a signal appears at collector of Q12, check Q9, Q12, and Q20. Check for pulses at J4 whenever pulses appear at collector of Q9. If pulses do not appear at J4, check Q13.

2. With TRAFFIC SEL switch at 12, check for a positive-going pulse (or pulses) at collector of Q12 during the period that the waveform at J3 is undergoing a negative excursion. If pulses do not appear, check Q8 and Q12.

3. With TRAFFIC SEL switch at 24 (I, S. or R), check signal at J2. If signal is incorrect, check Q8 and Q23.

10	Incorrect signal at J2 and/or J6	Decision circuit Q23 through Q28, Q29 defective	Check Q23 through Q29 as described in notes 1 through 3 below.

Notes.

1. With TRAFFIC SEL switch at 12, perform the following checks during the period that the waveform at J3 is undergoing a negative excursion:

a. Check for a negative-going pulse (or pulses) at collector of Q27 and for a positive-going pulse (or pulses) at collector of Q2 8. If incorrect indications are obtained, check Q27 and Q28.

b. Check for a positive-going pulse (or pulses) at collector of Q2s and for no signal at collector of Q26. If a signal appears at collector of Q20, check, Q25, Q26, and Q29. Check for pulses at J6 whenever pulses appear at collector of Q25. If pulses do not appear at J6, check Q24.

2. With TRAFFIC SEL switch at 12, check for a positive-going pulse (or pulses) at collector of Q26 during the period that the waveform at J3 is undergoing a positive excursion. If pulses do not appear, check Q23 and Q26.

3 With TRAFFIC SEL switch at 24 (I, S. or R), check signal at J2. If signal is incorrect, check Q8 and Q23.

Item No.	Symptom	Probable trouble	Correction
11.	No signal at terminal 22(J1) with signal present at J4,or no signal at terminal 20 with signal present at J6	Q16,Q17,Q19,Q21, Q22 defective.	With TRAFFIC SEL switch at 24 (I, S. or R), check that flip-flop (Q17,Q19) is set or reset whenever a signal appears at J4 and J6. If flip-flop fails to set and reset, check, Q16,Q17,Q19,Q21, and Q22.
12.	No signal at terminal 22(J1) or terminal 20 with signal present at J2 only	T1,Q14,Q15,Q18 defective	With TRAFFIC SEL switch at 24 (I, S. or R), check that flip-flop (Q17,Q19) changes state whenever a signal appears at J2. If flip-flop does not change state, check T1, Q14,Q15, and Q18.
13.	*From radio rcvr meter* (terminal 7) does not read in center green area on TEST ALIGN meter, with proper signal at J3	CRl9,CR20,C21, or C22 defective.	Check CR19,CR20,C21, and C22.
14	SERV SEL position 6 does not read in green area on TEST ALIGN meter.	CR13,CR14,Cl9, or C20 defective.	Check CR13,CR14,Cl9, and C20.
15.	SERV SEL position A does not read in green area on TEST ALIGN meter, with positive and negative peak detector working properly	R81 defective	Check continuity and value of R81.
16	No signal at terminal 8	R50 defective	Check continuity and value of R50.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector	Transistor	Base	Emitter	Collector
Q1	+9.1±0.9	+9.4±0.9	+4.4±0.4.	Q22	27, fig. 6-41	1,2,fig.6-41	-4.5±0.135.
Q2	+8.1±0.8	+8.4±0.8	+4.1±0.4	Q23	38, fig. 6-41	39,fig.6-41	-4.5± 0.135.
Q3	+9.3±0.9	+9.7±0.9	10, fig. 6-41.	Q24	40, fig. 6-41	41,fig.6-41	-4.5± 0.135.
Q4	+4.1±0.4	10, fig. 6-41	+0.33±0.1.	Q25	42, fig. 6-41	43,fig.6-41	40,fig.6-41.
Q5	11, fig. 6-41	12, fig. 6-41	-4.5±0.135.	Q26	44, fig. 6-41	43,fig.6-41	38,fig.6-41.
Q6	12, fig. 6-41	13, fig. 6-41	-4.5 ±0.135	Q27	+4.5± 0.5	45,fig.6-41	42,fig.6-41.
Q7	13, fig. 6-41	14, fig. 6-41	-4.5 ± 0.135	Q28	4, fig. 6-41	45,fig.6-41	44,fig.6-41.
Q8	15, fig. 6-41	16, fig. 6-41	-4.5±0.135.	Q29	35, fig. 6-41	46,fig.6-41	43,fig.6-41.
Q9	17, fig. 6-41	19, fig. 6-41	18, fig. 6-41.	Q30	5, fig. 6-41	+5±0.5	47,fig.6-41.
Q10	4, fig. 6-41	20, fig. 6-41	17, fig. 6-41.	Q31	47, fig. 6-41	+0.38±0.1	48,fig.6-41.
Q11	+5.2±0.5	20, fig. 6-41	21, fig. 6-41.	Q32	+5.7±0.6	+5.0±0.5	0±0.1
Q12	21, fig. 6-41	19, fig. 6-41	15, fig. 6-41.	Q33	+5.8±0.6	+5.0 ± 0.5	+10.0±0.3.
Q13	18, fig. 6-41	22, fig. 6-41	-4.5±0.135.	Q34	5,fig.5-41	+4.0±0.4	47,fig.6-41 or -0.07 ±0.02.
Q14	24, fig. 6-41	25, fig. 6-41	23, fig. 6-41.	Q35	47,fig.6-41 or -0.07 ±0.02.	+0.26±0.1	50,fig.6-41.
Q15	27, fig. 6-41	23, fig. 6-41	26, fig. 6-41.	Q36	+3.7±0.4	+4.0±0.4	0±0.1
Q16	29, fig. 6-41	30, fig. 6-41	28, fig. 6-41.	Q37	+3.4±0.4	+3.7 ± 0.4	0±0.1.
Q17	31, fig. 6-41	30, fig. 6-41	26, fig. 6-41.				
Q18	32, fig. 6-41	23, fig. 6-41	23, fig. 6-41.				
Q19	33, fig. 6-41	34, fig. 6-41	23, fig. 6-41.				
Q20	35, fig. 6-41	36, fig. 6-41	18, fig. 6-41.				
Q21	37, fig. 6-41	36, fig. 6-41	9, fig. 6-41.				

4-9. Panel 5A4, Troubleshooting

a. Troubleshooting Chart (fig. 6-14, 6-30, 6-42).

Item No.	Symptom	Probable trouble	Correction
1	No waveform or incorrect waveform at J1 or terminal 31(*xtal filter drive*).	Q8 defective	Check signal at base of Q8. If present, check Q8. If not present, proceed to step 2.
2	No signal at base of Q8	Q7, DL1 defective	Check signal at collector of Q6. If present, check Q7 and DL1. If not present, proceed to step 3.
3	No signal at collector of Q6	Q5, Q6, CR3, CR4 defective	Check signal at base of Q5. If present, check Q5, Q6, CR3, and CR4. If not present, proceed to step 4.
4	No signal at base of Q5	CRT, CR2 defective	Check signal at collectors of Q3 and Q4. If present, check CR1 and CR2. If not present, proceed to step 5.
5.	No signal at collectors of Q3 and Q4	Q1, Q2, Q3, Q4 defective	Check Q1, Q2, Q3, and Q4.
6	No waveform or incorrect waveform at terminal 7 (12-channel timing-1).	Q17 defective	Check signal at base of Q17. If present, check Q17. If not present, proceed to step 8.
7	No waveform or incorrect waveform at terminal 13 (12-channel timing-2).	Q15, Q16, DL2 defective	Check signal at base of Q15. If present, check Q15, Q16, and DL2. If not present, proceed to step 8.
8	No signal at bases of Q15 and Q17.	Q13, Q14, CR6 defective	Check signal at base of Q13. If present, check Q13, Q14 and CR6. If not present, proceed to step 9.
9	No signal at base of Q13	Q11, Q12, T1 defective	Check signal at base of Q11. If present, check Q11, Q12 and T1. If not present, proceed to step 10.
10	No signal at base of Q11	Q9, Q10, FL1 defective	Check signal at base of Q9. If present, check Q9 and Q10. If not present, check FL1.
11	Incorrect voltage (0.15 volt ±0.15) at terminal 1 (traffic alarm control).	Q18, Ql9, OR7, CR8, CR9 defective.	Check voltage at base of Q19. If presents check Q19. If not present, check Q18 and CR7 through CR9.
12	Incorrect voltage (9.9 volts +0.3) at terminal 15 (*radio signal detector*).	Q20, Q21, CR10, CR11 defective	Check signal at emitter of Q20. If present, check Q21, CR10, and CR11. If not present, check Q20.
13	SERV SEL position G does not read in green area on TEST ALIGN meter with correct signal at J1.	CR5 or C8 defective	Check CR5 and C8.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector		Transistor	Base	Emitter	Collector
Q1	1, fig. 6-42	3, fig. 6-42	2, fig. 6-42.		Q12	2, fig. 6-42.	23, fig. 6-42	-4.5± 0.135.
Q2	+4.8±0.5	3, fig. 6-42	4, fig. 6-42.		Q13	24, fig. 6-42	25, fig. 6-42	0± 0.1.
Q3	4, fig. 6-42	6, fig. 6-42	5, fig. 6-42.		Q14	+4.4:± 0.4	25, fig. 6-42	26, fig. 6-42.
Q4	2, fig. 6-42	6, fig. 6-42	7, fig. 6-42. -		Q15	26, fig. 6-42.	27, fig. 6-42	-4.5 ± 0.135.
Q5	8, fig. 6-42	9, fig. 6-42	4.5±0.135.		Q16	28, fig. 6-42	30, fig. 6-42	-4.5±0.135.
Q6	11, fig. 6-42	12, fig. 6-42	10, fig. 6-42.		Q17	26, fig. 6-42.	29, fig. 6-42	-4.5±0.135.
Q 7	13, fig. 6-42	14, fig. 6-42	-4.5±0.135.		Q18	18, fig. 6-42	31, fig. 6-42	-4.5±0.135.
Q8	14, fig. 6-42	15, fig. 6-42	-4.5±0.135.		Q19	+0.75:±:0.2	0 ± 0.1	+0.15±0.15.
Q9	16, fig. 6-42	17, fig. 6-42	4.5±0.135.		Q 20	3-2 fig. 6-42	32, fig. 6-42	0±0.1.
Q10	19, fig. 6-42	20, fig. 6-42	18, fig. 6-42.		Q21	± 9.6 ± 0.3	+ 10.0 ± 0.3	+9.9 ± 0.3.
Q11	18, fig. 6-42	21, fig. 6-42	-4.5±0.135					

4-10. Panel 5A5, Troubleshooting

a. Troubleshooting Chart (fig. 6-15, 6-31, 6-43).

Item No.	Symptom	Probable trouble	Correction
1	No waveform or incorrect waveform at terminal 27 (*24-channel timing-1*).	Q6 defective	Check signal at base of Q6. If present, check Q6. If not present, proceed to step 3.
2	No waveform or incorrect waveform at terminal 29 (*34-channel timing-2*).	Q9 defective	Check signal at base of Q9. If present, check Q9. If not present, proceed to step 3.
3	No signal at bases of Q6 and Q9	Q7, Q8, CRT, CR2 defective	Check signal at J1. If present, check Q7, Q8, CRT, and CR2. If not present, proceed to step 4.
4	No signal at J1	Q3, Q4, T1 defective	Check signal at base of Q3. If present, check Q3, Q4, and T1. If not present, proceed to step 5.
5	No signal at base of Q3	Q1, Q2, FL1 defective	Check signal at base of Q1. If present, check Q1 and Q2. If not present, check FL1.
6	No waveform or incorrect waveform at J2 or terminal 6 (*decision timing*).	Q14, CR11 CR12 defective	Check signal at base of Q14. If present, check Q14, CR11, and CR12. If not present, proceed to step 7.
7	No signal at base of Q14	Q12, Q13, CR8, CR9, CR10 defective.	Check signal at collector of Q12. If present, check Q13, CR9, and CR10. If not present, check Q12 and CR8.
8	No waveform or incorrect waveform at J3 or terminal 3 (*count-down timing*).	Q17, Q18, CR16, CR18 defective	Check signal at base of Q18. If present, check Q18 and CR18. If not present, check Q17 and CR16.
9.	Incorrect output (*traffic alarm present*) at terminal 14 (-1.4 volts ± 0.4); delayed traffic alarm with signal present at J1	Q15, Q16, or C27 defective; or Q5, Q10, CR3, CR4, CR5, or K1 defective.	Observe K1. If energized, check Q15, Q16, and C27. If de-energized, check Q5, Q10, CR3, CR4, CR5, and K1.

Item No.	Symptom	Probable trouble	Correction
10	Incorrect output (no traffic alarm present) at terminal 20(-12 volts ±+ 1) with TEST-OPR switch at OPR.	Q15,Q16, or C27 defective; or Q5,Q10,CR3,CR4,CR5, or B1 defective.	Observe E1. If de-energized, check Q15, Q16, and C27. If energized, check Q5,Q10,CR3,CR4,CR5, and K1.
11	SERV SEL position E (*countdown timing meter*, terminal 2) does not read in green area on TEST ALIGN meter with signal at terminal 6.	Ql9,CR17, or C26 defective	Check Q19,CR17, and C26.
12	SERV SEL position F (*decision timing meter*, terminal 7) does not read in green area on TEST ALIGN meter with proper signal at terminal 6.	CR13,CR14,C20, or C21 defective.	Check CR13,CR14,C20, and C21.
13	SERV SEL position C (*xtal fiber meter*, terminal 15) does not read within or to right of green area on TEST ALIGN meter, with signal present at J1. ALIGN meter, with signal present at J1.	Q11,CR6,CR7,C10, or C11 defective.	Check Q11,CR6,CR7,C10, and C11.
14	SERV SEL position D (*traffic meter*, terminal 28)does not read in green area on TEST ALIGN meter, with correct output at terminal 20(-1.4volts.±0.4).	R21 defective	Check R21 for continuity and correct value.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector		Transistor	Base	Emitter	Collector
Q1	14, fig. 6-43	15, fig. 6-43 .	-4.5±0.135.		Q11	1, fig. 6-43	24, fig. 6-43	-4.5±0.135.
Q2	16, fig. 6-43	17, fig. 6-43 .	18, fig. 6-43.		Q12	26, fig. 6-43	27, fig. 6-43	25, fig. 6-43.
Q3	18, fig. 6-43	18, fig. 6-43 .	-4.5±0.135.		Q13	29, fig. 6-43 .	30, fig. 6-43	28, fig. 6-43.
Q4	1, fig. 6-43	1, fig. 6-43	-4.5±0.135.		Q14	28, fig. 6-43	32, fig. 6-43	31, fig. 6-43.
Q5	1, fig. 6-43	19, fig. 6-43	-4.5±0.135.		Q15	-0.7±0.1	-1.4±0.4	0±0.1.
Q6	20, fig. 6-43	10, 11, fig. 6-43.	-4.5±4 0.135.		Q16	0±0.1 or -0.2.	-07 ± 0.4	0±0.1
Q7	22, fig. 6-43	23, fig. 6-43 .	21, fig. 6-43.		Q17	34, fig. 6-43	35, fig. 6-43	33, fig. 6-47.
Q8	23, fig. 6-43	23, fig. 6-43	20, fig. 6-43.		Q18	33, fig. 6-43	4,5, fig. 6-43.	-4.5±0.135.
Q9	21, fig. 6-43	12, fig. 6-43	-4.51± 0.135.		Q19b	-0.2±0.1	0±0.1	-0.1±0.1.
Q10	+0.73±0.1	0±0.1	+0.16± 0.1.					

4-11. Panel 4A6/5A6, Troubleshooting

a. *Troubleshooting Chart* (fig. 6-19, 6-24, 6-25).

Item No.	Symptom	Probable trouble	Correction
1	No waveform or incorrect waveform at J2 or terminal 21 (*tim out-1*).	3,Q5,CR5,CR6 defective.	Check signal at pin 2 of Z3. If present, check Z3. If not present, check Q5,CR5, and CR6.
2	No waveform or incorrect waveform at terminal 20 (*timing A*).	Q6 defective	Check Q6.
3	No waveform or incorrect waveform at J1 or terminal 31 (*tim out-2*).	Z12,Q10,CR11,CR12 defective	Check signal at pin 2 or Z12. If present, check Z12. If not present, check Q10,CR11, and CR12.
4	No waveform or incorrect waveform at J5 or terminal 26 (*timing B*).	Q11 defective	Check Q11.
5	No waveform or incorrect waveform at J4 or terminal 1 (*8-kc address-1*).	Q16 defective	Check signal at base of Q16. If present, check Q16. If not present, proceed to step 7.
6	No waveform or incorrect waveform at J3 or terminal 19 (*8-kc address-2*).	Q15 defective	Check signal at base of Q15. If present, check Q15. If not present, proceed to step 7.
7	No signal at base of Q15 or Q16, or at both bases.	One or more of modules Z4 through Z11; Q7, Q8, Q9, CR10;Q12,Q13,Q14, and CR14 defective.	Check signal at pin 3 of Z11. If present, check Z11. If not present, work backward checking pin 3 of Z10, Z9, Z8, Z7, Z6,Z5, and Z4 sequentially until signal is recovered. When signal is recovered, check the first module which has an input at pin 3. If signal at Z11 or Z10 is incorrect, check Q12,Q13,Q14, and CR14. If signal at Z5 to Z11 is incorrect, check A7, Q8,Q9, and CR10. If signal is incorrect at pin 3 of Z4, proceed to step 8.
8	No waveform or incorrect waveform at terminal 4 (medium traffic 8-kc control).	Q4, Z1 defective	Check signal at pin 2 of Z1. If present, check Q4 and Z1. If not present, proceed to step 9.
9	No signal at pin 2 of Z1	Q3,CR1 defective	Check signal at collector of Q2. If present, check Q3 and CRT. If not present, proceed to step 10.
10	No signal at collector of Q2	Q1,Q2,DL1,CR2 defective	Check signal at base of Q2. If present, check Q2,DL1, and CR2. If not present, check Q1.
11	No waveform or incorrect waveform at terminals 21 and 31 with TRAFFIC SEL switch at 24S (loss of skipping operation when unit is out of frame).	Q4,Z2,CR3,CR4 defective	With ADDRESS switches on both the master and slave TD-352/U units at SLAVE, check waveform at terminal 18. The timing pulses at this point should be blanked out whenever a skip pulse is presented at input terminal 30. If timing pulses at terminal 18 are not blanked out, check for pulses at pin 10 of Z2. If pulses at pin 10 of Z2 are present, check Q4. If not present, check Z2,CR3, and CR4.

Item No.	Symptom	Probable trouble	Correction
12	SERV SEL position H (*medium-traffic timing out-1* meter, terminal 14) does not read in green area on TEST ALIGN meter, with correct signal at J2.	CR8, CR9, C8, or C9 defective	Check CR8, CR9, C8, and C9.
13	SERV SEL position J (*medium traffic liming out-2 meter*, terminal 27) does not read in green area on TEST ALIGN meter, with correct signal at J1.	CR15, CR16, C31, or C33 defective.	Check CR15, CR16, C31, and C33.
14	SERV SEL position K (*8-kc address-1 meter*, terminal 2) does not read in green area on TEST ALIGN meter, with correct signal at J4.	R45 defective	Check R45.
15	SERV SEL position L (*8-kc address-2 meter*, terminal 17) does not read in green area on TEST ALIGN meter, with correct signal at J3. .	R42 defective	Check R42.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector		Transistor	Base	Emitter	Collector
Q1	10, fig. 6-44	0±0.1	11, fig. 6-44.		Q9	24, fig. 6-44	21, fig. 6-44	23, fig. 6-44.
Q2	12, fig. 6-44		13, fig. 6-44.		Q10	25, fig. 6-44	26, fig. 6-44	27, fig. 6-44.
Q3	14, fig. 6-44	0± 0.1	15, fig. 6-44.		Q11	27, fig. 6-44	5, fig. 6-44	-4.5± 0.135.
Q4	-6.5±0.6	-4.5± 0.135	8, fig. 6-44.		Q12	28, fig. 6-44	30, fig. 6-44	29, fig. 6-44.
Q5	16, fig. 6-44	17, fig. 6-44	18, fig. 6-44`		Q13	31, fig. 6-44	0±0.1	30, fig. 6-44.
Q6	18, fig. 6-44	9, fig. 6-44	-4.5±0.135.		Q14	32, fig. 6-44	29, fig. 6-44	33, fig. 6-44.
Q7	19, fig. 6-44	20, fig. 6-44	21, fig. 6-44.		Q15	34, fig. 6-44	3, fig. 6-44	-4.5±0.135.
Q8	22, fig. 6-44	0±0.1	20 fig., 6-44		Q16	35, fig. 6-44	4, fig. 6-44	-4.5±0.135.

c. Module Terminal Voltages. The module terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Module	1	2	3	4	5	6	7	8	9	10
Z1		15, fig.6-44						36, fig.6-44	8, fig.6-44	
Z2		-0.12 ± 0.05			-0.35 ± 0.05			+0.66 ± 0.1		
Z3		18, fig.6-44							2, fig.6-44	
Z4		7, fig.6-44	37, fig.6-44						37, fig.6-44	6, fig.6-44
Z5		38, fig.6-44	39, fig.6-44						39, fig.6-44	
Z6		40, fig.6-44	41, fig.6-44						41, fig.6-44	42, fig.6-44
Z7		43, fig.6-44	44, fig.6-44						44, fig.6-44	
Z8		45, fig.6-44	46, fig.6-44						46, fig.6-44	
Z9		47, fig.6-44	48, fig.6-44						48, fig.6-44	
Z10		49, fig.6-44	50, fig.6-44						50, fig.6-44	51, fig.6-44
Z11		35, fig.6-44	52, fig.6-44						52, fig.6-44	34, fig.6-44
Z12									1, fig.6-44	

4-11.1. Panel 4A11, Troubleshooting

a. Troubleshooting Chart (figs. 6-19.1. 6-24.1, 6-25.1)

Item No.	Symptom	Probable trouble	Correction
1	No waveform or incorrect waveform at J2 or terminal 21 (tim out-1).	Z1, Q1, CR1, or CR2 defective.	Check signal at Pin 2 of Z1. If present, check Z1. If not present, cheek Q1, CRT, and CR2.
2	No waveform or incorrect waveform at terminal 20 (timing A).	Q2 defective.	Check Q2.
3	No waveform or incorrect waveform at J1 or terminal 31 (tim out-23.	Z2, Q3, CR3, and CR6 defective.	Check signal at pin 2 of Z2. If present, check Z2. If not present, check Q3, CR3, and CR6.
4	No waveform or incorrect waveform at J5 or terminal 26 (timing B).	Q4 defective.	Check Q4.
5	No waveform or incorrect waveform at J4 or terminal 1 (8-kc address-1).	Q16 defective.	Check signal at base of Q16. If present, cheek Q16. If not present, proceed to step 6.
6	No waveform or incorrect waveform at base of Q16.	DLI defective.	Check signal at emitter Of Q15. If present, check DL1. If not present, proceed to step 7.
7	No waveform or an incorrect waveform at emitter of Q16	Q15 defective.	Check signal at base of Q15. If present, cheek Q15. If not present, proceed to step 9.
8	No waveform or an incorrect waveform at J3 or terminal 19 (8-kc address 2).	Q14 defective.	Check signal at base of Q14. If present, check Q14.If not present, proceed to step 9.
9	No signal at base of Q14 or Q15 or at both bases.	Z11 defective.	Check signal at Pins 1, 3, and 11 of Z11. If all signals are present, check Z11. If all signals are not present or incorrect, proceed to step 10. If signal is not present at pin 3, proceed to step 11. If signal is not present at pins 1 and 11, proceed to step 13.
10	No waveform or an incorrect waveform at pins 1, 3, and 11 of all.	Z3 defective.	Check Z3.
11	No waveform or an incorrect waveform at pin 3 of Z11.	Q6, Q7, CR7, or CR8 defective.	Check signal at emitter of Q7 and at base of Q6. If signal is present at emitter of Q7, check CR8. If not present at emitter of Q7, check Q7. If signal is present at base of Q6, check Q6 and CR7. If signal is not present at base of Q6, proceed to step 12.
12	No waveform organ incorrect waveform at base of Q6.	Q5, C13, R8, or R9 defective.	Check signal at emitter of Q5. If present, cheek C13, R8, and R9. If not present, check Q5.
13	No waveform or an incorrect waveform at pins 1 and Al of Z11.	One or more modules Z4 through Z10; Q8, Q9, Q10, CR11; Q11 Q12 Q13, or CR12 defective.	Check signal at pin 3 of Zl0. If 2 present, check Z10. If not present, work backward checking pin 3 of Z9, Z8, Z7, Z6, Z5, and Z4 sequentially until signal is recovered or appears correct. Where signal

Item No.	Symptom	Probable trouble	Correction
			first appears correct, check the module that has an input at pin 3. If signal at Z10 or Z9 is incorrect, check Q11, Q12, Q13, and CR12. If signal at Z4 to Z10 is incorrect, check Q8, Q9, Q10 and CR11.
14	SERV SEL position H *(timing out-1 meter, terminal 15)* does not read in green area on TEST ALIGN meter, with correct signal at J2.	CR4, CR5, C6, or C7 defective.	Check CR4, CR6, C6, and C7.
15	SERV SEL position J *(timing out-1 meter, terminal 28)* does not read in green area on TEST ALIGN meter, with correct signal at J1.	CR9, CR10, C8, or C9 defective.	Check CR9, CRIB, C8, and C9.
16	SERV SEL position K *(8-kc address-1 meter terminal 2)* does not read in green area on TEST ALIGN meter, with correct signal at J4.	R32 defective.	Check R32.
17	SERV SEL position L (*8-kc address-1 meter terminal* 17) does not read in green area on TEST ALIGN meter, with correct signal at J3	R29 defective.	Check R29.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure reference are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector
Q1	1, fig. 6-44. 1	2, fig. 6-44. 1	3, fig. 6-44.1
Q2	3, fig. 6-44. 1	4, fig. 6-44. 1	-4.5±0.135
Q3	1, fig. 6-44. 1	2, fig. 6-44. 1	3, fig. 6-44.1
Q4	3, fig. 6-44. 1	4, fig. 6-44. 1	-4.5 ±0.135
Q5	6, fig. 6-44. 1	6, fig. 6-44. 1	+4.5 ±0.135
Q6	7, fig. 6-44. 1	8, fig. 6-44. 1	9, fig. 6-44 .1
Q7	10, fig. 6-44. 1	11, fig. 6-44. 1	-4.5±0.135
Q8	24, fig. 6-44	21, fig. 6-44	23, fig. 6-44
Q9	19, fig. 6.44	20, fig 6-44	21, fig. 6-44.
Q10	22, fig. 6-44	0±0.1	20, fig. 6-44
Q11	32, fig. 6-44	29, fig. 6-44	33, fig. 6-44
Q12	28, fig. 6-44	30, fig. 6-44	29, fig. 6-44.
Q13	31, fig. 6-44	0±0.1	30, fig. 6-44
Q14	12, fig. 6-44 1	13, fig. 6-44. 1	+4.5 ±0.135
Q15	14, fig. 6-44.1	16, fig. 6-44. 1	-4.5 ±135
Q16	16, fig. 6-44.1	17, fig. 6-44. 1	+4.5 ± 0.135

c. Module Terminal Voltages. The module terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Z or Q NUMBER	1	2	3	4	5	6	7	8	9	10	11
Z1		6-44. 1 6-44.1				+10 ±0.3	+4.5 ±0.135		18, fig. 6-44.1	-4.5 ±0.135	
Z2		3, fig. 6-44 1				+10±0.3	+4.5 ±0.135		18, fig. 6-44.1	-4.5±0. 135	
Z3		5, fig. 6 44.1	19, fig. 6-44. 1	-4.5 ±0.135	0.0±0.1	+4.5 ±0.135	-4.5 ±0.135	-4.5 ±0.135	19, fig. 6-44.1		
Z4		38, fig. 6 44	39, fig. 6-44	-4.5 ±0.135	0.0±0.1	+4.5 ±0.135	-4.5 ±0.135	-4.5 ±0.135	39, fig. 6-44		
Z5		40, fig. 6-44.	41, fig. 6-44	-4.5 ±0.135	0.0±0.1	+4.5 ±0.135	-4.5 ±0.135	-4.5 ±0.135	41, fig 6-44.	42, fig. 6 44	
Z6		43, fig. 6-44.	44, fig. 6-44	-4.5 ±0.135	0.0±0.1	+4.5 ±0.135	-4.5 ± 0.135	-4.5 ±0.135	44, fig 6-44		
Z7		45, fig. 6-44	46, fig. 6-44	-4.5 ± 0.135	0.0±0.1	+4.5 ±0.135	-4.5 ±0.135	-4.5 ±0.135	46, fig 6-44.		
Z8		47, fig. 6-44	48, fig. 6-44	-4.5 ±0.135	0.0±0.1	+4.5 ±0.135	-4.5 ±0.135	-4.5 ±0.135	48, fig 6-44.		
Z9		49, fig. 6-44	50,-fig. 6-44	-4.5 ±0.135	0.0±0.1	+4.5 ±0.135	-4.5 ±0.135	-4.5 ±0.135	50, fig 6-44	51, fig. 6-44	
Z10		35, fig; 6-44.	52, fig. 6-44	-4.5 ±0.135	0.0±0.1	+4.5 ±0.135	-4.5 ±0.135	-4.5 ± 0.135	52, fig 6-44.	34, fig. 6-44	
Z11	35, fig. 6-44	12, fig. 6-44. 1	9, fig. 6-44. 1	-12 ± 0.36		0.0 ±0.1	+4.5 ±0.135		-4.5 ±0.135	14, fig. 6-44.1	34, fig. 6-44.

4-12. Panel 4A7/5A7,Troubelshooting

a. Troubleshooting Chart (fig. 6-10, 6-26, 6-45).

Item No.	Symptom	Probable trouble	Correction
	Note. Prior to troubleshooting panel 4A7/6A7, adjust the order-wire level of the TD-202/U test unit as follows: Connect the audio oscillator UNBAL. OUTPUT test lead prod through a 510 ohm resistor to the center conductor and the A test lead prod to the shield ground of the T-connector (FROM RADIO RCVR connector on the TD-202/U test unit). Adjust the audio oscillator output for 1,000 cps at 0.07 volt rms. Operate the SERV SEL switch to the O position and adjust the ORDER WIRE LEVEL control of the TD-202/U test unit for a center-scale hairline indication on the TEST ALIGN meter. After adjusting the order-wire level of the TD-202/U test unit, disconnect the audio oscillator test lead prods from the T-connector and remove the 4A7/5A7 and extender panels from the TD-202/U test unit. Using the panel extender, connect the 4A7/5A7 panel under test to the TD-202/U test unit		
1	No waveform or incorrect wave form at J1 or terminal 30 (J1 test).	Q1, Q3 defective	Check that voltage at base of Q3 varies as RL control on panel 5A3 is varied. If proper indication is obtained, check Al and Q3. If not, check Q3 and then proceed to step 2.
2	Amplitude of J1 or terminal 30 waveform does not vary with amplitude of terminal 7 wave-form when RL control on panel 5A3 is varied.	Q6, Q7, Q8, Q9 defective	Check voltage at bases of Q6 and Q7. If present at both bases, check Q6 through Q9. If not present at one or both bases, proceed to step 3.
3	Incorrect voltage at one or both bases of Q6 and Q7.	T1, CRT, CR3 defective	Check voltage at emitters of Q4 and Q5. If correct at both emitters, check T1, CRT, and CR2. If incorrect at emitter of Q4 only, proceed to step 4. If incorrect at emitter Q5 only, proceed to step 5.
4	Incorrect voltage at emitter of Q4	Q2, Q4 defective	Check Q2 and Q4.
5	Incorrect voltage at emitter of Q5	Q5 defective	Check voltage at collector of Q17. If correct, check Q5. If incorrect, proceed to step 6.
6	Incorrect voltage at collector of Q17.	Q17 defective	Check voltage at base and emitter of Q17. If correct at both base and emitter, check Q17. If incorrect at base only, proceed to step 7. If incorrect at emitter only, check Q17 and then proceed to step 8.
7	Incorrect voltage at base of Q17 .	Q10 defective	Check Q10.
8	Incorrect voltage at emitter of Q16	Q15 or Q16 defective	Check Q15 and Q16.
9	No indication or incorrect indication on TEST ALIGN meter with SERV SEL switch at 0, and 1,000-cps audio signal at 0.07 volt rms injected into FROM RADIO RCVR connector on TD-202/U front panel (no signal or incorrect signal at terminal 1).	CR3, CR4, C19, or C20 defective	Check signal at J4. If present, check CR3, CR4, C19, and C20. If not present, proceed to step 10.
10	No signal at J4 with proper voltage at collector of Q17	Q12, Q13, or Q14 defective	Check voltage at base of Q12. If correct, check Q12, Q13, and Q14, then proceed to step 11.
11	No signal at J4 with Q12, Q13, and Q14 normal.	Q11 of FL1 defective	Check voltage at emitter of Q11. If correct, check FL1. If incorrect, check Q11.
12	No waveform heroes terminals 5 and 3 with correct signal at J4	T2 defective	Check T2

b. Transistor Terminal Voltages. Tile transistor terminal voltages listed below were measured with a do vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector		Transistor	Base	Emitter	Collector
Q1	2, fig. 6-45	1, fig. 6-45	-4.5±0.135.		Q10	5, fig. 6-45	6, fig. 6-45	-4.5±0.135
Q2	2, fig. 6-45	4, fig. 6-45	-4.5±0.135.		Q11	-2.5±0.3	-2.2±0.3	-4.5±0.135
Q3	-4.5 to +1	1, fig. 6-45	-4.5±0.135.		Q12	+4.9±0.4	+ 5.3±0.4	-0.2±0.4
Q4	-1.9±0.3	1.71+0.3	-4.5±0.135.		Q13	-0.2±0.4	+0.1±0.4	-4.5±0.135
Q5	-2.5±0.3	-2.2+0.3	-4.5±0.135.		Q14 [a]	0±0.1	+0.3±0.2	-4.5±0.135
Q6	+5.1±0.8	+5.3±0.8	+3±3.		Q15	3, fig. 6-45	7, fig. 6-45	-4.5±0.135
Q7	+5.1±0.8	+5.3±0.8	+3±3.		Q16	-0.13±0.2	-0.08±0.2	-2.6±0.3
Q8	+3±3	+ 1.5±1.0	+1 to-4.5.		Q17	+0.3±0.2	+0.5±0.2	-2.5±0.3
Q9	+3±3	+1.5±1.0	-4.5to +1.					

[a] Order wire lever control operated fully counterclockwise

4-13. Panel 4A8/548, Troubleshooting

a. Troubleshooting Chart (fig.. 6-11, 6-27,6-46)

Item No.	Symptom	Probable trouble	Correction
1	No waveform or incorrect waveform at J1 or terminal 31 (PCM OUT-1).	Q7 defective	Check signal at collector of Q6. If present, check Q7. If not present, proceed to step 2.
2	No signal at collector of Q6	Q4, Q5, Q6, CR3 defective	Check signals at collectors of Q1 and Q2. If present at both collectors, check Q4, Q5, Q6, and CR3. If not present at one or both collectors, proceed to step 3.
3	No signal at collector of either Q1 or Q2, or at both collectors.	Q1, Q2, Q3, CR1, CR2 defective	Check signal at collector of Q3. If present, check Q1 and Q2. If not present, check Q3, CR1, and CR2.
4	No waveform or incorrect waveform at J2 or terminal 30 (PCM OUT-2).	Q14 defective	Check signal at collector of Q3. If present, check Q14. If not present, proceed to step 5.
5	No signal at collector of Q13	Q11, Q12, Q13, CR8 defective	Check signals at collectors of Q8 and Q9. If present at both collectors, check Q11, Q12, Q13, and CR8. If not present at one or both collectors, proceed to step 6.
6	No signal at collector of either Q8 or Q9, or at both collectors.	Q8, Q9, Q10, CR6, CR7 defective	Check signal at collector of Q10. If present, check Q8 and Q9. If not present, check Q10, CR6, and CR7.
7	No waveform or incorrect waveform at J7 or terminal 1 *(skip pulse)* when the unit is out of frame.	Q22 defective	Make necessary connections and set controls to obtain out-of-frame condition (see note below). Check signal at base of Q22. If present, check Q22. If not present, proceed to step 8.
	Note. Operate TRAFFIC SEL switch on TD-202/U to 24S. Operate ADDRESS switch on master TD-352/U to SLAVE.		

Item No.	Symptom	Probable trouble	Correction
8	No signal at base of Q22	Q20, Q21, Q23, or CR15 defective	Check for pulse signal at base of Q21. If not present, proceed to step 9. If present, check do voltage at base of Q20. If do voltage at base of Q20 is more negative than at base of Q23, check Q20, Q21, Q23, and CR15. If do voltage at base of Q20 is more positive than that at base of Q21, proceed to step 11.
9	No signal at base of Q21	CR13, CR14 defective	Check signal at J8. If not present, proceed to step 10. If present, check voltage at emitter of Q19. The signal should be a random square wave varying between O volt and-4.5 volt). If correct, check CR13 and CR14. If incorrect, proceed to step 11.
10	No signal at J8	Q15, Q16, Q17, Q18, CR11, CR12 defective.	Check signal at base of Q16. If present, check Q16, Q17, Q18, CR11, and CRIB. If not present, check Q15.
11	Incorrect voltage at base of Q20 and/or incorrect emitter voltage at Q19.	Q19 defective	Check for random square wave (0 volt to + 4.5 volts) at J4. If present, check Q19. If not present, proceed to step 12.
12	Incorrect signal at J4	Q31, Q32, Q33, Q34 defective	Check signal at base of Q34. If not present, proceed to step 13. If present, check signal at J3. If signal at J3 is present, check Q31, Q32, Q33, and Q34. If signal at J3 is not present, proceed to step 14.
13	No signal at base of Q34	Q24, Q25, CR16, CR17, CR18, CR19, CR20 defective.	Check signal at cathode of CR16. If present, check Q24, Q25, and CR17 through CR20. If not present, check CR16.
14	No signal at J3	Q28, Q29, Q30, CR21 defective	Check signals at collectors of Q26 and Q27. If present at both collectors, check Q28, Q29, Q30, and CR21. If not present at one or both collectors, proceed to step 15.
15	No signal at collector of either Q26 or Q27, or at both collectors.	Q26, Q27, Q37, CR24, CR25 defective.	Check signal at J5. If present, check Q26, Q27, Q37, CR24, and CR25. If not present, proceed to step 16.
16	No signal at J5 . .	Q35, Q36, CR22, CR23 defective	Check signal at collector of Q35. If present, check Q36 and CR23. If not present, check Q35 and CR22.
17	SERV SEL position 34 *(pcm out-1* meter, terminal 11) does not read in green area on TEST ALIGN meter with correct signal at J1.	CR4, CR5, C4, or C5 defective	Check CR4, CR5, C4, and C5.
18	SERV SEL position a *(pcm out-8* meter, terminal 8) does not read in green area on TEST ALIGN meter with correct signal at J2	CR9, CR10, C9, or C10 defective	Check CR9, CRIB, C9 and C10.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector	Transistor	Base	Emitter	Collector
Q1	8 fig. 6-46	10 fig. 6-46	11 fig. 6-46	Q21	37 fig. 6-46	+0.3±0.1 or +0.4±0.1 [a]	38 fig. 6-46.
Q2	0±0.1	10 fig. 6-46	12 fig. 6-46	Q22	38 fig. 6-46	6 fig. 6-4	-4.5±0.135
Q3	13 fig. 6-46	14 fig. 6-46	10 fig. 6-46	Q23	+1.7+0.17	+ 1.0 ±0.1 or +1.4±0.1 [a]	0±0.1
Q4	15 fig. 6-46	16 fig. 6-46	11 fig.6-46	Q24	39 fig. 6-46	0±0.1	40 fig. 6-46
Q5	17 fig. 6-46	18 fig. 6-46	12 fig. 6-46	Q25	41 fig. 6-46	0±0.1	42 fig. 6-46
Q6	0±0.1	18 fig. 6-46	19 fig. 6-46	Q26	43 fig.6-46	44 fig. 6-46	45 fig. 6 46
Q7	19 fig. 6-6	1 fig. 6-46	20 fig. 6-46	Q27	0±0.1	44 fig. 6-46	46 fig. 6-46
Q8	8 fig. 6-46	22 fig. 6-46	21 fig. 6-46	Q28	47 fig. 6-46	48 fig. 6 46	45 fig. 6-46
Q9	0±0.1	22 fig. 6-46	23 fig. 6-46	Q29	49 fig. 6-46	60 fig. 6-46	46 fig. 6-46
Q10	13 fig. 6-46	24 fig. 6-46	22 fig. 6-46	Q30	0±0.1	50 fig. 6-46	3 fig. 6-46
Q11	25 fig. 6-46	26 fig. 6-46	21 fig. 6-46	Q31	3 fig. 6-46	61 fig. 6-46	-4.5±0.135
Q12	27 fig. 6-46	28 fig. 6-46	23 fig. 6-46	Q32	52 fig. 6-46	53 fig. 6-46	4,fig.6 46
Q13	0±0.1	28 fig. 6-46	29 fig. 6-46	Q33	64 fig 6-46	51 fig. 6-46	4 fig. 6-46
Q14	29 fig. 6-46	2. fig. 6-46	30 fig. 6-46	Q34	55 fig. 6-46	53 fig. 6-46	-4.6±0.135
Q15	9 fig. 6-46	31 fig. 6-46	-4.5 + 0.135	Q35	56 fig. 6-46	57 fig. 6-46	58 fig. 6-46
Q16	31 fig. 6-46	32 fig. 6-46	-4.5 + 0.136	Q36	68 fig. 6-46	5 fig. 6-46	-4.5±0.135.
Q17	33 fig. 6-46	34 fig. 6-46	35 fig. 6-46	Q37	59 fig.6-46	+4.9±0.5	44 fig. 6-46.
Q18	35 fig. 6-46	7 fig. 6-46	-4.5 + 0.135				
Q19	4 fig. 6-46	36 fig. 6-46	-4.5 + o.i35				
Q20	+0.7±0.1or +1.2±0.1[a]	+1.0±0.1 or +1.4±0.1[a]	+0.3±0.1 or +0.4±0.1[a]				

[a] Operate master T-352/U ADDRESS switch to SLAVE (provides out-of-frame condition as required to generate skip pulse).

4-14. Panel 4A2, Troubleshooting

a. Troubleshooting Chart (fig.6-5, 6-21, 6-47).

Item No. Symptom Probable trouble Correction

Note. With TRAFFIC SEL switch in 96I position, perform the following checks:

1 Incorrect output at terminal 30. R44 or Q14 defective. Check signal at base of Q14. If incorrect, proceed to item 2. If correct, check Q14 and R44.

Note. If incorrect signal at terminal 30 in 48-channel operation but correct in 96I and 96S operation, check Z11 and Z13. If incorrect signal at terminal 30 in 96R operation but correct in 96I and 96S operation, check Z15 and Z7.

2 Incorrect signal at base of Q14. Z11 or Z13 defective. Check signals at pin 7 of Z11 and pin 5 of Z13. If signal at pin 7 of Z11 is incorrect, proceed to item 3. If signal at pin 5 of Z13 is incorrect, proceed to item 4. If both signals are correct, check Z11 and Z13.

3 Incorrect signal at pin 7 of Z11 Z7 or Z11 defective. Check signals at pins 3, 4, 5, and of Z11 8 of Z2 and pins 3 and 4 of Z11. If signal at pin 3 of Z7 is incorrect, proceed to item 5. If signal at pin 4 of Z7 is incorrect, proceed to item 8. If level at pin 5 of Z7 is incorrect, proceed to item 23. If signal at

No.			
			pin 8 of Z7 or pin 4 of Z11 is incorrect, proceed to item 10. If signal at pin 8 of Z11 is incorrect, proceed to item 20. If signals at pins 3, 4, 5, and 8 of Z7 and pins 3 and 7 of Z11 are correct, check Z7 and Z11.
4	Incorrect signal at pin 5 of Z13	Z13 or Z15 defective.	Check signals at pins 7 and 8 of Z13 and pins 4, 7, 8, and 9 of Z15. If signal at pin 7 of Z13 is incorrect, proceed to item 21. If signal at pin 8 of Z13 or pin 4 of Z15is incorrect, proceed to item ID. If signal at pin 7 of Z16 is incorrect, proceed to item 6. If signal at pin 8 of Z15is incorrect, proceed to item 8. If level at pin 9 of Z15is incorrect, proceed to item 23. If signals at pins 7 and 8 of Z13 and pins 4, 7, 8, and 9 of Z15 are all correct, check Z13 and Z15.
5	Incorrect signal at pin 3 of Z7 or at base of Q13	Q12 or Q13 defective.	Check signal at base of Q12. If incorrect, proceed to item 7. If correct, check Q12 and Q13.
6	Incorrect signal at pin 7 of Z16	Q11 or CR10 defective.	Check signal at base of Q11. If incorrect, proceed to item 7. If. correct, check Q11 and CR10.
7	Incorrect signal at bases of Q11 and Q12	Q9, Q10, or C10 defective.	Check dc level at base of Q10. If incorrect, check C10. If correct, check Q9 and Q10.
8	incorrect signal at pin 4 of Z7 or pin 8 of Z15	Q5 or CR4 defective.	Check signal at base of Q5. If incorrect, proceed to item 9. If correct, check Q5 and CR4.
9	Incorrect signal at base of Q5	DL1 defective.	Check signal at emitter of Q1. If incorrect, proceed to item 19. If correct, check DL1.
10	Incorrect signals at pin 8 of Z7, pin 4 of Z11, pin8 of Z13, pin 4 of Z15,pin 10 of Z1, and pin 7of Z8	Z5 defective.	Check signal at pins 4 and 5 of Z5. If signal at pin 4 is incorrect, proceed to Item 11. If signal at pin 5 is incorrect, proceed to item 15. If both signals are correct, check Z5.

Note. To check Z8 and Z9, in steps 11 and 12 below, remove panel 4A10 and connect terminal 19 to terminal 25 (-4.5V).

11	Incorrect signal at pin 4 of Z5.	Z9 defective.	Check signals at pins 4 and 10 of Z9. If signal at pin 4 is incorrect, proceed to item 12. If signal at pin 10 is incorrect, proceed to item 15. If both signals are correct, check Z9.
12	Incorrect signal at pin 4 of Z9	Z8 defective.	Check signal at pin 4 of Z8. If incorrect, proceed to item 13. If correct, check Z8.

Item No.	Symptom	Probable trouble	Correction
13	Incorrect signal at pin 4 of Z8.	Q8 or CR6 defective.	Check signal at base of Q8. If incorrect, proceed to item 14. If correct, check Q8 and CR6.
14	Incorrect signal at base of Q8.	Z8 defective.	Check signals at pins 7, 8, and 9 of Z8. If signal at pin 7 is incorrect, proceed to item 15. If signal at pins 8 and 9 is incorrect, proceed to item 22. If all signals are correct, check Z8.
15	Incorrect signal at pin 7 of Z8, pin 10 of Z9, or pin 5 of Z5.	Q7 or CR5 defective.	Check signal at base of Q7, If incorrect, proceed to item 16. If correct, check Q7 and CR5.
16	Incorrect signal at base of Q7.	Z4 and C7 defective.	Check signal at pin 3 of Z4. If incorrect, proceed to item 17. If correct, check Z4 and C7.
17	Incorrect signal at pin 3 of Z4.	Q4 or CR1 defective.	Check signal at base of Q4. If incorrect, proceed to item 18. If correct, check Q4 and CR1.
18	Incorrect signal at base of Q4.	Q3 defective.	Check signal at base of Q3. If incorrect, proceed to item 19. If correct, check Q3.
19	Incorrect signal at base of Q3 or emitter of Q1.	Q1 or Q2 defective.	Check Q1 and Q2.
20	Incorrect signal at pin 3 of Z11.	Z6 defective.	Check signal at pin 7 of Z6. If incorrect) proceed to item 21. If correct, check Z6.
21	Incorrect signal at pin 7 of Z13 and at pin 7 of Z6.	Z10, Z12, or Z14 defective.	Check signals at pins 4, 5, 8, and 9 of Z10, Z12, and Z14. If signals at pin 4, 5, 8, or 9 are incorrect, proceed to item 22. If all signals are correct, check Z10, Z12, and Z14.
22	Incorrect signals at pin 4, 5, 8, or 9 of Z10, Z12, Z14 or at pins 8 and 9 of Z8.	Z1, Z2, Z3, or Z6 defective.	Check signal at pin 10 of Z1. If incorrect, proceed to item 10. If correct, check Z1, Z2, Z8, and Z6.
23	Incorrect dc level at pin 9 of Z15 and pin 5 of Z7 and/or PCM IN-1 meter (terminal 17) does not indicate in green region of TEST ALIGN meter.	Q15, CR8, CR9, Cl6 or C21 defective.	Check signal at emitter of Q13. If incorrect, proceed to item 24. If correct, check Q15, CR8, CR9, C16, and C21.
24	Incorrect signal at emitter of Q13.	Q13 or CR7 defective.	Check signal at base of Q13. If incorrect, proceed to item 5. If correct, check Qi3 and CR7.
25	TIM IN- 1 meter (terminal 20) does not indicate in green region of TEST ALIGN meter.	Q6, CR2, CR3, or C3 defective.	Check signal at pin 3 of Z4. If incorrect, proceed to item 17. If correct, check Q6, CR2, CR3, and C3.
26	TO RADIO XMTR meter (terminal 31) does not indicate in green region of TEST ALIGN meter.	CR11, CR12, or C20 defective.	Check output of terminal 30. If incorrect, proceed to item 1. If correct, check CR11, CR12, and C20.

b. Transistor Terminal Voltages. The transistor voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Collector	Emitter
Q1	11, fig. 6 47	12, fig. 6-47	13, fig. 6-47
Q2	0 ±0.1	12, fig. 6-47	14, fig. 6-47
Q3	14, fig. 6-47	-4.5 ±0. 135	15, fig. 6-47
Q4	15, fig. 6-47	4, fig. 6-47	0 ±0. 1
Q5	16, fig. 6-47	-4.6 ±0. 135	1, fig. 6-47
Q6	-I. 2 ±2. 0	-4.5 ±0. 135	0 to -1. 5
Q6 [a]	-3. 8 ±0- 4	-4.5 ±0. 135	-4.5 ±0. 2
Q7	17, fig. 6-47	-4. 5 ±0. 135	18, fig. 6-47
Q8	39, fig. 6-47	-4. 5 ±0. 135	6, fig. 6-47
Q9	19, fig. 6-47	20, fig. 6-47	21, fig. 6-47
Q10	-1. 0 ±0.1	20, fig. 6-47	22, fig. 6-47
Q11	22, fig. 6-47	-4. 5 ±0. 135	10, fig. 6-47
Q12	21, fig. 6-47	-4. 5 ± 0. 135	7 fig. 6-47
Q13	7, fig. 6-47	23, fig. 6-47	0 ±0. 1
Q14	45, fig. 6-47	24, fig. 6-47	26, fig. 6-47
Q15 [b]	-7. 2 ±2. 0	-4. 5 ±0. 135	0 to -1.5
Q15 [c]	-3. 8 ±0. 4	-4. 6 ±0. 135	-4.5 ±0.2

[a] Remove TIM IN-1 connector. Reconnect after making measurement.

[b] Operate front panel meter switch to PCM IN-I when making measurement.

[c] Remove PCM IN-1 connector. Reconnect after making measurement.

c. Module Terminal Voltages. The module terminal voltages listed below were measured with a dc vtvm (Multimeter ME-6B/U or equivalent). This figure references are for waveform measurements with the AN/U:SM-140.

Module	1	2	3	4	5	6	7	8	9	10
Z1	-4 .5±0.135	33 fig 6-47	26 fig 6-47		-4.5±0.135	0±0.1		3 fig 6-47	3 fig 6-47	2 fig 6-47
Z2	-4.5±0.135	3 fig 6-47	26 fig 6-47		-4.5±0.135	0±0.1		3 fig 6-47		2 fig 6-47
Z3	-4.5±0.135	3 fig 6-47	3 fig 6-47		-4.5± 0.135	0±0.1		3 fig 6-47	26 fig 6-47	2 fig 6-47
Z4	-4.5±0.135	-4.5 ±0.2	4 fig 6-47		-4.5±0.135	0±0.1	27 fig 6-47	28 fig 6-47		29 fig 6-47
Z4[c]		0±0.2	4 fig 6-47							-4.5±0.2
Z5	-4.5±0.136	30 fig 6-47		42 fig 6-47	18 fig 6-47	0±0.1	30 fig 6-47			31 fig 6-47
Z5[d]		32 fig 6-47		41 fig 6-47						2 fig 6-47
Z6	-4.5±0.135	33 fig 6-47	3 fig 6-47	3 fig 6-47		0±0.1	43 fig 6-47			34 fig 6-47
Z7	-4.5±0.135	5 fig 6-47	7 fig 6 -47	1 fig 6-47	-4.5±0.2	0±0.1	35 fig 6-47	31 fig 6-47	-4.5±0.135	5 fig 6-47
Z7[a]		36 fig 6-47	0.7±0.3		-4.5±0.2					36 fig 6-47
Z7[b]		37 fig 6-47					35 fig 6-47		0±0.1	37 fig 6-47
Z8	-4.5 ± 0.135	0 ±0.2		6 fig 6-47	38 fig 6-47	0±0.1	2 fig 6-47	3 fig 6-47	26 fig 6-47	39 fig 6-47
Z8[d]		40 fig 6-47		6 fig 6-47	GND					
Z9[d]		41 fig 6-47	41 fig 6-47	40 fig 6-47						18 fig 6-47
Z9	-4.5 ±0.135	42 fig 6-47	42 fig 6-47	0±0.2	-4.5±0.135	0±0.1			0±0.1	18 fig 6-47
Z10	-4.5±0.135	43 fig 6-47	44 fig 6-47	3 fig 6-47	26 fig 6-47	0±0.1	44 fig 6-47	3 fig 6-47	3 fig 6-47	43 fig 6-47

Module	1	2	3	4	5	6	7	8	9	10
Z11	-4.5 ±0.135		34 fig 6-47	31 fig 6-47	0±0.1	0±0.1			47 fig 6-47	45 fig 6-47
Z11[e]					4.5 ±0.135					46 fig 6-47
Z12	-4.5±0.135	43 fig 6-47	44 fig 6-47	3 figs. 6-47	3 fig 6-47	0±0.1	44 fig 6-47	26 fig 6-47	3 fig 6-47	43 fig 6-47
Z13	-4.5±0.135	47 fig 6-47			8 fig 6-47	0±0.1	43 fig 6-47	31 fig 6-47	0±0.1	8 fig 6-47
Z13[e]			46 fig 6-47		8 fig 6-47			26 fig 6-47	-4.5 ±0.135	8 fig 6-47
Z14	-4.5±0.135	43 fig 6-47	44 fig 6-47	26 fig 6-47	3 fig 6-47	0±0.1	44. fig 6-47	1 fig 6-47	26 fig 6-47	43 fig 6-47
Z15	-4.5±0.135	8 fig 6-47	48 fig 6-47	31 fig 6-47	-4.5±0.135	0±0.1	10 fig 6-47		0 to 1.5	8 fig 6-47
Z15[b]		49 fig 6-47	48 fig 6-47		0±0.1					49 fig 6-47
Z15[a]		50 fig 6-47					-4.5±0.2		-4.5±0.2	50 fig 6 47

a. Remove PCM IN-1 connector. Reconnect after making measurements.
b. Operate TRAFFIC SEL switch to 96R.
c. Remove PCM IN-2 connector. Reconnect after making measurements.
d. Remove panel 4A10 and connect terminal 19 to -4.5V. Remove terminal connection (first) and replace panel 4A10 after making measurements. Operate TRAFFIC SEL switch to 48.

4-15. Panel 4A3, Troubleshooting

a. Troubleshooting Chart (fig. 6-6, 6-22, 6-48)

Item No.	Symptom	Probable trouble	Correction
1	No waveform or incorrect wave form at J3 or terminal 9 (*clamped radio signal).*	Q5, Q6, Q7 defective	Check signal at base of Q5. If present, cheek Q5, Q6, and Q7. If not present, proceed to step 2.
2	No signal at base of Q5	Q3, Q4, CR1, CR2 defective	Check signal at base of Q4. If present, check Q3, Q4, CRT, and CR2. If not present, proceed to step 3.
3	No signal at base of Q4	Q1, Q2, R2 defective	Check signal at base of Q1. If present, cheek Q1 and Q2. If not present, cheek continuity and value of R2.
4	No signal or incorrect signal at terminal 26 (*center lever*), terminal 27 (*ternary pos level),* and terminal 28 (*ternary neg level)* with correct signal present at J3.	Positive peak detector (Q30 through Q33) or negative peak detector (Q34 through Q37) defective.	Check de levels at J5, J7, and terminal 26 with TRAFFIC SEL switch first at 48 and then at 96 (I, S. or R), as described in the note below. If do levels are incorrect, adjust R84, R86, and R85 to attain correct do levels. If correct do levels at J5, J7, or terminal 26 cannot be attained with R84, R86, or R85 adjustments, respectively, proceed to steps 5and 6

Note To cheek do levels at Jacks J5 and J7, switch the test oscilloscope to DC and perform the following: Adjust RL control on panel A43 so the waveform at Jack J3 is 4 cm high (20 volts pn). The positive peak should be exactly 2 cm above the center grid line; the negative peak should be exactly 2 cm below the center grid line. Without changing the oscilloscope controls, Check the dc levels at jacks J5 and J7. In 48-channel operation, the two levels should be the same and should fall in the center of the signal at J3. In 96-channel operation, the level at J5 should be 0.7 cm (0.35 volt) above the centerline; the level at J7 should be 0.7 cm (0.35 volt) below the centerline. The dc level at terminal 26 should be In center of signal at J3 in both cases.

Item No.	Symptom	Probable trouble	Correction
5	Correct do levels cannot be attained with adjustment.	Positive peak detector (Q30 through Q33) defective.	Check that do level of signal terminal 31 (emitter of Q33) is equal to positive. peaks of signal at J3. If incorrect, check Q30 through Q33. If correct, proceed to step 6.
6	Correct do levels cannot be attained with adjustment.	Negative peak detector (Q34 through Q37) defective.	Check that do level of signal at terminal 30 (emitter of Q37) is equal to negative peaks of signal at J3. If incorrect, check Q34 through Q37. If correct, proceed to step 7
7	Correct do levels at terminals 31 and 30 (emitters of Q33 and Q37), but correct dc levels at J5 and J7 cannot be attained with R84 and R86 adjustments, or correct do level at terminal 26 cannot be attained with R85 adjustment.	R84, R86, R85 defective	Check R84, R86, and R85.
8	No waveform or incorrect wave-form at J1 or terminal 22 (recovered pcm-1) and/or terminal 20 (recovered pcm-2) with correct signals present at J3,J5, and J7.	Decision circuits or flip-flop defective	Check signals at J2,J4, and J6 as described in notes 1 and 2 below. If signals at J2 and J4 are incorrect, proceed to step 9. If signals at J2 J4 and J6 are incorrect, proceed to step 10. If signals at J2,J4, and J6 are correct, proceed to step 11.
	Note. 1. With TRAFFIC SEL switch at 48, check for: no signal at J2; positive-going timing pulses at J4 and no pulses at J6 during the period that the waveform at J3 is undergoing a positive excursion; positive-going timing pulses at J6 and no pulses at J4 during the period that the waveform at J3 is undergoing a negative excursion.2. With TRAFFIC SEL switch at 96 (I, S. or R), check for: positive-going pulses at J2 only when the waveform at J3 falls between the do levels of J5 and J7; positive-going pulses at J4 only when the waveform at J3 is above the dc level of J5; positive-going pulses at J6 only when the wavcforn1 at J3 is below the do level of J7.		
9	Incorrect signal at J2 and/or J4	Decision circuit Q8 through Q13, Q14 defective	Check Q8 through Q13 and Q14 as. described in notes 1 through 3 below.
	Notes. 1. With TRAFFIC SEL switch at 48, perform the following checks during the time that the waveform at J3 is undergoing a positive excursion. a. Check for a negative-going pulse (or pulses) at collector of Q8 and for a positive-going pulse (or pulses) at collector of Q13. If incorrect indications are obtained, check Q8 and Q13. b. Check for a positive-going pulse (or pulses) at collector of Q9 and for no signal at collector of Q12. If a signal appears at collector of Q12, check Q9, Q12, and Q20. Check for pulses at J4 whenever pulses appear at collector of Q9. If pulses do not appear at J4, Check Q11. 2. With TRAFFIC SEL switch at 48, check for a positive-going pulse or pulses at collector of Q12 during the period that the waveform at J3 is under-going a negative excursion. If pulses do not appear, check Q8 and Q12. 3. With TRAFFIC SEL switch at 96 (I, S. or R), check signal at J2. If signal is incorrect, check Q10 and Q23.		
10	Incorrect signal at J2 and/or J6	Decision circuit Q23 through Q28, Q29 defective	Check Q23 through Q29 as described in notes 1 through 3 below.
	Notes. 1. With TRAFFIC SEL switch at 48, perform the following checks during the period that the waveform at J3 is undergoing a negative excursion: a. Check for negative-going pulse (or pulses) at collector of Q27 and for a positive-going pulse (or pulses) at collector of Q28. If incorrect indications are obtained, check Q27 and Q28. b. check for a positive-going pulse (or pulses) at collector of Q25 and for no signal at collector of Q26. If a signal appears at collector Q26, check Q25, Q26 and Q29. Check for pulses at J6 whenever pulses appear at collector of Q25. If pulses do not appear at J6, check Q24, 2. With TRAFFIC SEL switch at 48, check for a positive-going pulse (or pulses) at collector of Q26 during the period that the waveform at.l3 is undergoing a positive excursion. If pulses do not appear, check Q23 and Q26. 3. With TRAFFIC SEL switch at 96 (I, S. or R), check signal at J2. If signal is incorrect, check Q10 and Q23.		
11	No signal at terminal 22 (J1) with signal present at J4, or no signal at terminal 20 with signal present at J6.	Q15' Q18, Q20, Q21, Q22 defective.	With TRAFFIC SEL switch at 96 (I, S. or R), check that flip-flop (Q18, Q20) is set or reset whenever a signal appears at J4 and J6. If flip-flop fails to set and reset, check Q15, Q18, Q20, Q21, and Q22.

Item No.	Symptom	Probable trouble	Correction
12	No signal at terminal 22 (J1)or terminal 20 with signal present at J2 only.	T1, Q16, Q17, Ql9 defective	With TRAFFIC SEL switch at 96 (I, S. or R), check that flip-flop (Q18, Q20) changes state, whenever a signal appears at J2. If flip-flop does not change state, check T1, Q16, Q17, and Q19.
13	*From radio rcvr meter* (terminal 7) does not read in green area on TEST ALIGN meter, with proper signal at J3.	CR12, CR13, Cl9, or C20 defective.	Check CR12, CR13, C19, and C20.
14	SERV SEL position G (*recovered pcm in-1 meter*, terminal 25) does not read in green area on TEST ALIGN meter.	CR10, CR11, C17, C34, or C18 defective.	Check CR10, CR11, C17, C34, and C18.
15	SERV SEL position A (*ternary positive level meter* and *ternary neg level meter*, terminals 31 and 30) does not read in green area on TEST ALIGN meter, with positive and negative peak detectors working properly.	R82 defective	Check R82.
16	No signal at terminal 8 *(rcvd radio signal).*	R52 defective	Check R52.

b. Transistor Terminal Voltages. Tile transistor terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector		Transistor	Base	Emitter	Collector
Q1	9 fig. 6-48	10, fig.6-48	+2.0±0.2.		Q20	36, fig.6-48	37,fig.6-48	35,fig.6-48
Q2	+8.1±0.8	+8.3±0.8	11, fig. 6-48.		Q21	38, fig.6-48	37,fig.6-48	8,fig.6-48.
Q3	+0.34±0.1	+9.5±0.9	12, fig. 6-48		Q22	27, fig.6-48	39,fig.6-48	-4.5±0.135
Q4	11 fig. 6-48	12, fig.6-48	0.34±0.1.		Q23	40, fig.6-48	53,fig.6-48	-4.5±0.135
Q5	13 fig. 6-48	14, fig.6-48	-4.5±0.135		Q24	41, fig.6-48	42,fig.6-48	-4.5±0.135.
Q6	14 fig. 6-48	15, fig.6-48	-4.5±0.135		Q25	43, fig.6-48	44,fig.6-48	41,fig.6-48.
Q7	15 fig. 6-48	16, fig.6-48	-4.5±0.135		Q26	45, fig.6-48	44,fig.6-48	40,fig.6-48.
Q8	4,5,fig.6-48	17, fig.6-48	18, fig. 6-48.		Q27	+ 4.8	46,fig.6-48	43,fig.6-48.
Q9	18, fig.6-48	19, fig.6-48	20, fig. 6-48		Q28	4,5,fig.6-48	46,fig.6-48	45,fig.6-48.
Q10	21, fig.6-48	51, fig.6-48	-4.5±0.135		Q29	24, fig.6-48	47,fig.6-48	44,fig.6-48.
Q11	20, fig.6 48	22, fig.6-48	-4.5±0.135		Q30	4,5,fig.6-48	48,fig.6-48	49,fig.6-48.
Q12	23, fig.6-48	19, fig.6-48	21, fig. 6-48		Q31	49, fig.6-48	+0.4	-4.2.
Q13	+5.5±0.5	17, fig.6-48	23, fig. 6-48		Q32	+ 6.2	48,fig.6-48	-4.5±0.135
Q14	24, fig.6-48	25, fig.6-48	19, fig. 6-48		Q33	+6.3	+6.2	+10±0.3
Q15	52, fig.6-48	26, fig 6-48	27, fig. 6-48		Q34	48, fig.6-48	+4.3	-0.11.
Q16	28, fig.6-48	29, fig.6-48	30, fig. 6-48		Q35	-0.11	+4.3	+0.02
Q17	31, fig.6-48	30, fig.6-48	32, fig. 6-48		Q36	+4.3	+4.3	0.
Q18	33, fig. 6-48	26, fig.6-48	32, fig. 6-48		Q37	+3.8	+4.3	0.
Q19	34, fig.6-48	30, fig 6-48	35, fig. 6-48					

4-16. Panel 4A4,Troubleshooting

a. Troubleshooting Chart (fig. 6-7, 6-23, 6-49).

Item No.	Symptom	Probable trouble	Correction
1	No waveform or incorrect waveform at J1 or terminal 31 (*xctal filter drive*) with TRAFFIC SEL switch at 48.	Q8 defective	Check signal at base of Q8. If present, check Q8. If not present, proceed to step 2.
2	No signal at base of Q8	Q7, DL1 defective	Check signal at collector of Q6. If present, check Q7 and DL1. If not present, proceed to step 3.
3	No signal at collector of Q6	Q5,Q6,CR3,CR4 defective	Check signal at base ofQ5. If present, check Q5,Q6,CR3, and CR4. If not present, proceed to step 4.
4	No signal at base of Q5	CR1,CR2 defective	Check signals at collectors of Q3 and Q4. If present, check CR1 and CR2. If not present, proceed to step 5.
5	No signals at collectors of Q3 and Q4.	Q1,Q2,Q3,Q4 defective .	Check Q1,Q2,Q3, and Q4.
6	No waveform or incorrect waveform at J4 or terminal 7(48channel timing-l).	Q19 defective	Check signal at base of Ql9. If present, check Ql9. If not present, proceed to step 8.
7	No waveform or incorrect waveform at J5 or terminal 13(48channel timing-2).	Q18,Q20,DL2 defective	Check signal at base of Q18. If present check Q18, Q20, and DL2. If not present, proceed to step 8.
8	No signal at bases of Q18 and Ql9	Q16,Q17,CR9 defective	Check signal at J3 (emitter of Q15). If present, check Q16, Q17, and CR9. If not present, proceed to step 9.
9	No Signs at J3 (emitter of Q15)	Q14,Q15, or T1 defective	Check signal at base of Q14. If present, check Q14, Q15, and T1. If not present, proceed to step 10.
10	No signal at base of Q14	Q12,Q14, or FL1 defective	Check signal at base of Q12. If present, check Q12 and Q13. If not present, check FL1.
11	Incorrect voltage (0.15 volt A 0.15) at terminal 1 (traffic alarm control).	Q9,Q11,CR6,CR7, or CR8 defective.	Check voltage (0.73 volt $\pm$0.2) at base of Q11. If present, check Q11. If not present, check Q9 and CR6 through CR8.
12	Incorrect voltage (9.6 volts +0.3) at terminal 15 (radio signal detector).	Q10,Q21,CR10,CR11 defective	Check signal at emitter of Q10. If present, check Q21,CR10, and CR11. If not present, check Q10.
13	SERV SEL position B *(xtal filter drive meter*, terminal 17) does not read in green area on TEST ALIGN meter.	CR5 or C8 defective	Check CR5 and C8.

b. Transistor Voltages. The transistor terminal voltages listed below were measured with a do vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector		Transistor	Base	Emitter	Collector
Q1	1, fig. 6-49	2, fig. 6-49	3, fig. 6-49.		Q12	19,fig.6-49	20, fig. 6-49	-4.5±0.135.
Q2	+5	2, fig. 6-49	4, fig. 6-49.		Q13	21,fig.6-49	22, fig. 6-49	16, fig. 6-49.
Q3	4, fig. 6-49	5, fig. 6-49	6, fig. 6-49.		Q14	16,fig.6-49	23, fig. 6-49	-4.5±0.135.
Q4	3, fig. 6-49	5, fig. 6-49	7, fig. 6-49		Q15	24,fig.6-49	25, fig. 6-49	-4.5±0.135.
Q5	8, fig. 6-49	9, fig. 6-49	-4.5±0.135.		Q16	26,fig.6-49	27, fig. 6-49	28, fig. 6-49.
Q6	10, fig. 6-49	11, fig. 6-49	12, fig. 6-49.		Q17	+4.4	27, fig. 6-49	0.
Q7	13, fig. 6-49	14, fig. 6-49	-4.5±0.135.		Q18	28,fig.6-49	29, fig. 6-49	-4.5±0.135.
Q8	14, fig. 6-49	15, fig. 6-49	-4.5±0.135.		Q19	28,fig.6-49	30, fig. 6-49	-4.5±0.135.
Q9	16, fig. 6-49	17, fig. 6-49	-4.5±0.135.		Q20	31,fig.6-49	32, fig. 6-49	-4.5±0.135.
Q10	0	18, fig. 6-49	1, fig. 6-49.		Q21	+9.2	+10	+9.6.
Q11	+0.73	0	+0.18.					

4-17. Panel 4A5, Troubleshooting

a. Troubleshooting Chart (fig 6-8, fig 6-24, fig 6-50).

Item No.	Symptom	Probable trouble	Correction
1	No waveform or incorrect waveform at J4 or terminal 27(96-channel timing-1).	Q7 defective	Check signal at base of Q7. If present, check Q7. If not present, proceed to step 3.
2	No waveform or incorrect waveform at J5 or terminal 29(96-channel timing-2).	Q9 defective	Check signal at base of Q9. If present, check Q9. If not present, proceed to step 3.
3	No signal at bases of Q7 and Q9	Q6,Q8,CR2 defective	Check signal at J1. If present, check Q6, Q8, and CR2. If not present, proceed to step 4.
4	No signal at J1	Q3,Q4, T1 defective	Check signal at base of Q3. If present, check Q3,Q4, and T1. If not present, proceed to step 5.
5	No signal at base of Q3	Q1,Q2, FL1 defective	Check signal at base of Q1. If present, check Q1 and Q2. If not present, check FL1.
6	No waveform or incorrect waveform at J2 or terminal 6 (decision timing).	Q16,CR11,CR13 defective	Check signal at base of Q16. If present, check Q16, CR11, and CR13. If not present, proceed to step 7.
7	No signal at base of Q16	Q14,Q15,CR8,CR9,CR10 defective.	Check signal at collector of Q 14. If present, check Q15, CR9, and CX10. If not present, check Q14 and CR8.
8	No waveform or incorrect waveform at J3 or terminal 3 (countdown timing).	Q17,Q18.CR1,CR16 defective	Check signal at base of Q18. If present, check Q18 and CRT. If not present, check Q17 and CR16.

Item No.	Symptom	Probable trouble	Correction
9	Incorrect output (traffic alarm present) at terminal 20 (-1.4 volts ±0.4, (*delayed traffic alarm)* with signal present at J1	Q12,Q13,C13 defective or Q5, Q10,CR3.CR4,CR5 of K1 defective.	Observe K1. If energized, check Q12 and Q13. If deenergized, check Q5, Q10,CR3,CR4,CR5, and K1.
10	Incorrect output (no traffic Warm present) at terminal 20 (12 volts + 1) with TE6T-OPR switch at OPR.	Q12,Q13 defective, or Q5,Q10, CR3,CR4,CR5, or K1 defective.	Observe K1. If deenergized, check Q12. Q13, and CR12. If energized, check Q5,Q10,CR3,CR4,CR5, and K1.
11	SERV SEL position E (decision timing meter, terminal 7) does not read in green area with correct signal at terminal 6.	CR14,CR15,C27, C26 defective	Check CR14,CR15,C27, and C26.
12	SERV SEL position F (*decision timing meter*, terminal 7) does not read in green area of TEST ALIGN meter with proper signal at terminal 6.	Q14,CR15,C27, or C26 defective	Check Q14,CR15,C27, and C26.
13	SERV SEL position C(*xtal filter meter* terminal 15) does not read 1/6 scale or above on TEST ALIGN meter, with signal present at J1.	Q11,CR6,CR7,C11, or C12 defective.	Check Q11.CR6,CR7,C11, and C12.
14	SERV SEL position D *(traffic meter*, terminal 28) does not read in green area on TEST ALIGN meter with correct output at terminal 20(-1.4volts ±0.4).	R18 defective	Check R18.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with a do vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector		Transistor	Base	Emitter	Collector
Q1	13, fig.6-50	14, fig.6-50	-4.5±0.135.		Q12	-0.65 or -1.5[a].	-1.38 or -12.3[a].	0±0.1 or 0±0.1[a]
Q2	15, fig.6-50	16, fig.6-50	17, fig. 6-50.		Q13	-0.05 or -12.1[a].	-11.5 [a]	0±0.1 or 0±0.1[a]
Q3	17, fig.6-50	18, fig.5-50	-4.5±0.135.		Q14	25, fig.6-50	26, fig.6-50	27, fig. 6-50.
Q4	19, fig.6-50	1, fig. 6-50	-4.5±0.135.		Q15	28, fig.6-50	29, fig.6-50	30, fig. 6-50.
Q5	1, fig. 6-50	20, fig.6-50	-4.54±0.135.		Q16	30, fig.6-50	31, fig.6-50	32, fig. 6-50.
Q6	21, fig.6-50	22, fig.6-50	0±0.1.		Q17	33, fig.6-50	34, fig.6-50	35, fig. 6-50.
Q7	23, fig.6-50	6, fig. 6-50	-4.54±0.135.		Q18	35, fig.6-50	4,5, fig. 6-50	-4.5±0.135
Q8	+4.5	22, fig.6-50	23, fig. 6-50.		Q19 [b]	-0.35	0±0.1	-0.05.
Q9	23, fig.6-50	7, fig. 6-50	-4.5±0.135.		Q20	8,9, fig. 6-50	36, fig.6-50	4.5±0.135.
Q10	+0.75	0±0.1	+0.17.					
Q11	1 fig. 6-50	24, fig.6-50	-4.5±0.135.					

[a]. Operate OPR-TEST switch to OPR.

[b]. Operate SERV SEL switch to E.

4-18. Panel 4A9, Troubleshooting

a. Troubleshooting Chart (fig. 6-19, 6-23, 6-51).

Item No.	Symptom	Probable trouble	Correction
1	No waveform or incorrect wave-form at J2 or terminal 7 (*h.t. 8-kc cont*).	Q19 defective	Check signal at base of Q19. If present, check Q19. If not present, proceed to step 4.
2	No waveform or incorrect wave-form at terminal 16 (*h.t. tim-1cont).*	Q15 defective	Check signal at J6 (base of Q15). If present, check Q15. If not present, proceed to step 5.
3	No waveform or incorrect wave-form at terminal 17 (*h.t. tim-2 cont).*	Q16 defective	Check signal at J6 (base of Q16). If present, check Q16. If not present, proceed to step 6.
4	No signal at base of Q19	Q15,Q17,Q18,CR17,CR18, CR19,CR20,CR21 defective.	Check signal at J6. If present, check Q15,Q17, and Q18 and CR18 through CR21. If not present, proceed to step 5.
5	No signal at base of either Q15 (J6) of Q16(J5), or at both bases.	Either gates circuits are defective or there are no inputs to gates circuits.	Check signals at collectors of Q5 and Q6. If signals are not present at both collectors, proceed to step 9. If signal is not present at collector of Q5 only, proceed to step 7. If signal is not present at collector of Q6 only, proceed to step 8. If signals are present at both collectors, check for approximately -4.5 volts at collector of Q20 and 0 volt at J4 (collector of Q21), or vice versa. If collector voltages are incorrect, check Q20,Q21,CR22, and CR24. If collector voltages are correct, proceed to step 6.
6	No output from gates circuits with all inputs present.	Gates circuits defective	If signal is not present at base of Q16 (J5), check Q9,Q10,Q13,Q14, CR8 through CR10, and CR14 through CR16. If signal is not present at base of Q15(J6), check Q7,Q8,Q11,Q12,CR5 through CR7, and CR11 through CR13.
7	No signal at collector of Q5	Q4,Q5, DL1,CR1,CR2 defective.	Check signal at emitter of Q3. If present, check Q4,Q5,DL1,CR1, and CR2. If not present, proceed to step 9.
8	No signal at collector of Q6	Q6,CR3,CR4 defective	Check signal at emitter of Q3. If present, check Q6,CR3, and CR4. If not present, proceed to step 9.
9	No signal at emitter of Q3	Q1,Q2,Q3,CR30 defective	Check signal at base of Q2. If present, check Q2 and Q3. If not present, check Q1 and CR30.
10	No waveform or incorrect waveform at J1 or terminal 3 (96-channel timing-2 drive).	Q25 defective	Check signal at base of Q25. If present, check Q25. If not present or incorrect, proceed to step 11.
11	No signal at base of Q25	Q22,Q23,Q24,CR26,CR27,CR 28,CR29 defective	Check signal at collector of Q22. If present, check Q23,Q24, and CR26 through CR29. If not present, check Q22.

Item No.	Symptom	Probable trouble	Correction
12	Incorrect dual trace waveform at terminals 16 and 17 with TRAFFIC SEL switch at 96S and unit out of frame (skip pulse fails to switch circuit when unit is out of frame).	Q20, Q21, CR22, CR23, CR24, CR25 defective	To effect an out-of-frame condition, set the ADDRESS switch of the master and slave TD-352/U to SLAVE. Then cheek signals at collector of Q21 and at J4. Signals should alternate at an irregular rate. If not, check Q21, Q22, and CR22 through CR25

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with a dc vtvm (Multimeter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector		Transistor	Base	Emitter	Collector
Q1	10, fig. 6-51		11, fig. 6-51.		Q14	21, fig.6-51	-4.4 or 29, fig. 6-51 [a].	-4.5.
Q2	11, fig. 6-51	12, fig. 6-51	-4.5.		Q15	6, fig. 6-51	8, fig. 6-51	-4.5.
Q3	12, fig. 6-51	13, fig. 6-51	-4.5.		Q16	5, fig. 6-51	9, fig. 6-51	-4.5.
Q4	14, fig. 6-51	15, fig. 6-51	-4.5.		Q17	30, fig.6-51	0	2, fig. 6-51.
Q5	16, fig. 6-51	17, fig. 6-51	18, fig. 6-51.		Q18	31, fig.6-51	0	2, fig. 6-51.
Q6	19, fig. 6-51	20, fig. 6-51	21, fig. 6-51.		Q19	2, fig. 6-51	2, fig. 6-51	-4.5.
Q7	21, fig. 6-51	22, fig. 6-51	-4.5.		Q20	-0.45 or + 0.15 [a]	0	-0.15 or -4.7 [a]
Q8	-0.15 or -4.7[a]	24, fig. 6-51 or -4 3[a]	-4.5.		Q21	+0.18 or -0.4 [a]	0	4, fig. 6-51 or -0.1[a].
Q9	-0.15 or -4.7 [a]	25, fig. 6-51 or -4.3[a]	-4.5.		Q22	7, fig. 6-51	0	32, fig.6-51
Q10	18, fig.6-51	23, fig.6-51	-4.5.		Q23	33, fig.6-51	0	34, fig.6-51
Q11	18, fig.6-51	28, fig.6-51	-4.5.		Q24	35, fig.6-51	0	36, fig.6-51
Q12	4, fig. 6-51 or -0.1[a].	26, fig. 6-51	-4.5.		Q25	36, fig.6-51	1, fig. 6-51	-4.5.
Q13	4, fig. 6-51 or -0.15 [a]	-4.4 or 27, fig 6-51 [a]	-4.5.					

[a] Measurement depends on state of flip-flop.

4-19. Panel 4A10, Troubleshooting

a. Troubleshooting Chart (figs. 6-51, 6-20.1, 6-47.1).

Note. Outputs *S1, S2, S3, S4, S5, and S6,* measured in item 1 below, are identical. The same procedure is used to troubleshoot any of these outputs and respective modules Z2, Z5, Z8, Z10 Z15, and Z17.

Item No.	Symptom	Probable trouble	Correction
1	Incorrect output at terminal 4(S1) [2(S2), 8(S3), 6(S4), 9(,S6), or3(S6)].	Z2 (Z5, Z8, RIO, Z15, or Z17) defective.	Check signals at pins 2, 9, and 10 of Z2 (Z5, Z8, Z10, Z15, or Z17). If signal at pins 2 and 9 is incorrect, proceed to item 2. If signal at pin 10 is incorrect, proceed to item 3. If all signals are correct, check Z2 (Z5, Z8,Z10, Z15, or Z17).
2	Incorrect signals at pins 2 or 9 of Z2 (Z5, Z8, Z10, Z15, or Z17).	Z1 (Z4, Z7, Z9, Z14, or Z16) defective.	Check signals at pins 8, 4, 5, 7, 8, and 9 of Z1 (Z4, Z7, Z9, Z14, or Z16). If signals at pins 4, 5, 7, or 8 are incorrect, proceed to item 6. If signal at pin 3 is incorrect, proceed to item 7. If signal at pin 9 is incorrect, proceed to item 8. If all signals are correct, check Z1 (Z4, Z7, Z9, Z14, or Z16).
3	Incorrect signal at pin 10 of Z2 (Z5, Z8, Z10, Z15, or Z17) or Z11.	Z6 defective.	Check signal at pin 3 of Z6. If incorrect, proceed to item 4. If correct, check Z6.
4	Incorrect signal at pin 3 of Z6.	Q7 or Q11 defective.	Check signal at base of Q11. If incorrect, proceed to item 5. If correct, check Q7 and Q11.
5	Incorrect signal at base of Q11.	Q9, Q10, or DL1 defective.	Check signal at base of Q9. If incorrect, check DL1. If correct, check Q9 and Q10.
6	Incorrect signal at pin 4, 5, 7, or 8 of Z1 (Z4, Z7, Z9, Z14, or Z16) or base of Q12.	Z3, Z11 Z12, or Z13 defective	Check signal at pin 10 of Z11. If incorrect, proceed to item 3. If correct, check Z3, Z11, Z12, and Z13.
7	Incorrect signal at pin 3 of Z1 (Z4, Z7, Z9, Z14, or Z;16) or terminal 7 (PCM-2).	Q4 or CR1 defective.	Check signal at base of Q4. If incorrect, proceed to item 9. If correct, check Q4 and CRT.
8	Incorrect signal at pin 9 of Z1 (Z4, Z7, Z9 Z14, or Z16) or terminal 11 (PCM-2).	Q3, Q6, or CR2 defective.	Check signal at base of Q3. If incorrect, proceed to item 9. If correct, check Q3, Q6, and CR2.
9	Incorrect signal at base of Q3 or Q4.	Q1 or Q2 defective.	Check Q1 and Q2.
10	Incorrect output at terminal 20 (READIN BRACKET PULSE).	Q12 or CR9 defective.	Check signal at base of Q12. If incorrect, proceed to item 6. If correct, check Q12 and CR9.
11	Meter terminal 19 (TIM IN-2) does not read in green region of TEST ALIGN meter or incorrect dc level at pin 8 of Z3.	Q7, Q8, CR6, CR6, or CR7 defective.	Check signal at emitter of Q7. If incorrect, check Q7 and CR6. If correct, check CR6, CR7, and Q8

Item No.	Symptom	Probable trouble	Correction
12	Meter terminal 21 (PCM IN-2) does not read in green region of TEST ALIGN meter or incorrect dc level at pin 7 of Z3.	Q5,Q6,CR2,CR3, or CR4 defective.	Check signal at emitter of Q5. If incorrect, check Q6 and CR2. If correct, check CR3,CR4, and Q6.
13	Incorrect dc level at terminal18 (*PCM-2 INHIBIT).*	Z3 defective.	Check dc levels at pins 7 and 8 of Z3. If level at pin 7 is incorrect, proceed to item 12. If level at pin 8 is incorrect, proceed to item 11. If both levels are correct' check Z3.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with a dc vtvm (multi-meter ME-26B/U or equivalent). The figure references are for waveform measurements with the AN/USM-140.

Transistor	Base	Emitter	Collector
Q1	8, fig. 6-47.1	9, fig. 6-47.1	10, fig. 6-47.1
Q2	-1.0 ±0.1	9, fig. 6-47.1	11, fig. 6-47.1
Q3	10, fig. 6-47.1	-4.5±0.136	3, fig. 6-47.1
Q4		-4.5±0.135	4, fig. 6-47.1
Q5	3, fig. 6-47.1	12, fig. 6-47.1	0±0.1
Q6	-7.3±2.0	-4.6±0.136	0 to -1.5
Q6[b]	-3.8±0.4	-4.5±0.136	-4.5±0.2
Q7	13, fig. 6-47.1	14, fig. 6-47.1	0±0.1
Q8[c]	-7.3±2.0	-4.5±0.135	0 to -1.5
Q8[d]	-3.8±0.4	-4.5±0.135	-4.5±0.2
Q9	15, fig. 6-47.1	16, fig. 6-47.1	-4.5±0.135
Q10	Gnd.	16, fig. 6-47.1	17, fig. 6-47.1
Q11		-4.5±0.135	13, fig. 6-47.1
Q12	18, fig. 6-47.1	-4.6+0.135	7, fig. 6-47.1

[a] Operate front panel meter switch to PCM IN-2 when making measurement.
[b] Remove PCM IN-2 connector. Reconnect after making measurement.
[c] Operate front panel meter switch to TIM IN position when making measurement.
[d] Remove TIM IN-2 connector. Reconnect after making measurement.

c. Module Terminal Voltages. The module terminal voltages listed below were measured with a dc vtvm (multi-meter ME-26B/U or equivalent). The figure REFERENCES are for waveform measurements with the AN/USM-140.

Module	1	2	3	4	5	6	7	8	9	10
Z1	-4.5 ±0.135	19 fig 6-47.1	4 fig 6-47.1	2 fig 6-47.1	21 fig 6-47.1	0±0.1	6 fig 6-47.1	21 fig 6-47.1	3 fig 6-47.1	5 fig 6-47.1
Z2	0±0.1	19 fig 6-47.1			0± 0.1	0± 0.1		6 fig 6-47.1	5 fig 6-47.1	1 fig 6-47.1
Z3	-4.5±0.135	20 fig 6-47.1	2 fig 6-47.1	2 fig 6-47.1		0± 0.1	0 to -1.5	0 to -1.5		-4.5± 0.2
Z3[a]							-4.5 ±0.2	0 to -1.5		0± 0.3
Z3[b]							0 to -1.5	-4.5± 0.2		0± 0.3
Z4	-4.5±0.135	19 fig 6-47.1	4 fig 6-47.1	2 fig 6-47.1	21 fig 6-47.1	0±0.1	2 fig 6-47.1	21 fig 6-47.1	3 fig 6-47.1	5 fig 6-47.1
Z5	-4.5± 0.135	19 fig 6-47.1			-4.5± 0.135	0±0.1		6 fig 6-47.1	5 fig 6-47.1	1 fig 6-47.1
Z6	-4.6± 0.135	1 fig 6-47.1	17 fig 6-47.1			0± 0.1	-4.5±0.135			
Z7	-4.5± 0.135	19 fig 6-47.1	4 figs 6-47.1	2 fig 6-47.1	2 fig 6-47.1	0±0.1	2 fig 6-47.1	2 fig 6-47.1	3 fig 6-47.1	5 fig 6-47.1
Z8	-4.5±0.135	19 fig 6-47.1			-4.5 ±0.135	0± 0.1			5 fig 6-47.1	1 fig 6-47.1
Z9	-4.5±0.135	19 fig 6-47.1	4 fig 6-47.1	21 fig 6-47.1	2 fig 6-47.1	0± 0.1	21 fig 6-47.1	2 fig 6-47.1	3 fig 6-47.1	5 fig 6-47.1
Z10	-4.5±0.135	19 fig 6-47.1				0± 0.1		6 fig 6-47.1	5 fig 6-47.1	1 fig 6-47.1
Z11	-4.5±0.135	20 fig 6-47.1	21 fig 6-47.1		-4.5 ± 0.135	0±0.1		2 fig 6-47.1	2 fig 6-47.1	1 fig 6-47.1
Z12	-4.5±0.135	2 fig 6-47.1	21 fig 6-47.1		-4.5 ± 0.135	0± 0.1		2 fig 6-47.1	21 fig 6-47.1	1 fig 6-47.1
Z13	-4.5± 0.135	2 fig 6-47.1	21 fig 6-47.1		-4.5 ± 0.135	0± 0.1		2 fig 6-47.1	21 fig 6-47.1	1 fig 6-47.1
Z14	-4.5±0.135	19 fig 6-47.1	4 fig 6-47.1	21fig 6-47.1	2 fig 6-47.1	0±0.1	21fig 6-47.1	2 fig 6-47.1	3 fig 6-47.1	5 fig 6-47.1

Module	1	2	3	4	5	6	7	8	9	10
Z15	-4.5± 0.135	19 fig 6-47.1			-4.5±0.135	0±0.1		6 fig 6-47.1	5 fig 6-47.1	1 fig 6-47.1
Z16	-4.5± 0.135	19 fig 6-47.1	4 fig 6-47.1	21 fig 6-47.1	4 fig 6-47.1	0± 0.1	21 fig6-47.1	4 fig 6-47.1	3 fig 6-47.1	5 fig 6-47.1
Z17	-4.5±0.135	19 fig 6-47.1			-4.5±0.135	0± 0.1		6 fig 6-47.1	5 fig 6-47.1	1 fig 6-47.1

[a]. Remove PCM IN-2 connector. Reconnect after making measurements on this circuit.
[b]. Remove TIM IN-2 connector. Reconnect after making measurement on this circuit.

CHAPTER 5
GENERAL SUPPORT TESTING PROCEDURES

5-1. General

a. These testing procedures are prepared for use by Electronics Field Maintenance Shops and Electronics Service Organizations responsible for general support maintenance of electronic equipment to determine the acceptability of repaired electronic equipment. These procedures set forth specific requirements that repaired electronic equipment must before it is returned to the using organization. The testing procedures may also be used as a guide for the testing of equipment that has been repaired at direct support if the proper tools and test equipment are available. Perform the physical test and inspection (para 5-4). Refer to paragraph 5-5 or 5-7 to perform the unit performance test on the TW202/U or TW203/U, respectively. A summary of performance standards is provided in paragraphs 5-6 and 5-8.

b. Each test depends on the preceding test for certain operating procedures. Comply with the instructions preceding the body of each chart before proceeding to the chart. Perform each test in sequence. Do not vary the sequence. For each step, perform all the actions required in the *control settings* columns, then perform each specific test procedure, and verify it against its performance standard.

5-2. Test Equipment, Materials, and Other Equipment

a. General. All test equipment, materials, and other equipment required to perform the testing procedures given in this section are listed in the following charts and are authorized under TA 11-17 (Signal Field Maintenance Shops) and TA 11-100(11-17) (Allowances of Signal Corps Expendable Supplies for Signal Field Maintenance Shop, Continental United States).

b. Test Equipment.

Nomenclature	Federal stock No.	Technical manual
Multiplexer TD-352/U (2 required).[a]	5805-900-8199	TM 11-5805-367-12.
Multiplexer TD-353/U (2 required).[b]	580-900-8200	TM 11-5805-367-12
Signal Generator SG-71/FCC	8625-669-0255.	TM 11-5088
Voltmeter, Electronic ME-30B/U.	6625-669-0742	TM 11-6625-320-12.
Headset-Microphone H-91A/U.	5965-699-6871	TM 11-580-367-12.

[a]. ·TD-202/U tests only.

[b]. TD-203/U tests only.

c. Materials.

Materials	Federal stock No.
Cable Assembly, Radio Frequency CG-1040B/U- (5 ft) (8 required)	6995-913-0509.
Resistor, fixed, 600-ohm 1/2-watt	5905-542-9532.

d. Other Equipment. Electric Light Assembly MX-1292/PAQ, FSN 6695-537-4470, TM 11-5540.

5-3. Modification Work Orders

The performance standards listed in the tests (para 5-6 and 5-8) assume that no modification work orders have been performed. A listing of current modification work orders will be found in DA Pam 310-4.

5-4. Physical Tests and Inspections

a. Test Equipment and Materials. Electric Light Assembly MX-12uA2/PAQ.

b. Test Connections and Conditions.

(1) Do not make any connection to the equipment.
(2) Perform the following check when repairs are completed, before reassembly of the equipment.
(3) Connect the MX-1292/PAQ to a 115-volt, 60-cps source, and install the wide band transmission filter.

c. Test Procedure

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	N/A	Controls may be in any position	a. Inspect front panel for evidence of physical damage loose or missing parts screws or panel fasteners. b. Inspect connectors and plugs for cleanliness and evidence of physical damage. c. Remove and check all fuses for proper size and amperage rating. d. Check all filter capacitors for evidence of overheating. e. Check all resistors for evidence of overheating. f. Inspect all wiring and cabling for worn or frayed insulation. g. Inspect all metal surfaces for condition of finish.	a. Front panel is complete and not damaged. b. Connectors and plugs are clean and not damaged. c. Fuses are proper size and rated As indicated on panel markings. d. Capacitors show no evidence of leakage. e. Resistors show no signs of discoloration due to overheating. f. Wiring and cabling are free of cuts and frays. g. All metal surfaces intended to be painted do not show bare metal. Panel lettering is legible.

Note. Touchup point Is recommended In lieu of refinishing whenever Practicable (TB 810 306).

2	N/A	Controls may be in any position	Check the equipment modification work orders (refer to DA Pam 310-4 for a list of MWO's).	If MWO is performed MWO number appears on equipment.
3	MX-1292/PAQ 245V FOR M. V. LAMP: ON.	Controls may be in any position	a. Expose equipment to direct rays of MX-1292/PAQ and inspect condition of moisture-fungi proofing epoxy. *Note.* Moisture-fungi proofing appears blue-green under rays of MX-1292/PAQ. Epoxy appears milky-white, but blue-gray if defective. b. Operate 245V FOR M.V. LAMP switch of MX-1292/PAQ to OFF.	a. All components wiring and chassis surfaces are completely covered with moisture-fungi proofing epoxy with no evidence of it on connectors or switch contacts. Note. Do not apply moisture-fungi proofing epoxy , to parts not originally treated with it. b. None

5-5. Performance Tests, TD-202/U

(fig. 5-1)

a. Test Equipment if and Materials

(1) Multiplexer TD-352/U (2 required).
(2) Signal Generator SG-71/FCC.
(3) Voltmeter, Electronic ME 3i0B/U.
(4) Headset-Microphone H-9lA/U.
(5) Cable assembly radio frequency, type CG-1040B/U (8 required).

b. Test Connections and Conditions. Connect the TD-202/17 and the TD-352/U master and slave units as shown in figure 5-1. Do not connect signal genera for, headset microphone or voltmeter until told to do so.

c. Test Procedures.

Note. Unless specifically stated otherwise, au procedural instructions and performance standards pertain to the TD-202/U test unit.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			Panel 5A2 Note. Audible and visual alarms should indicate traffic in this test.	
1	TD-202/U test unit AC POWER: ON OPR-TEST: TEST TRAFFIC SEL: 24I METER SELECT: SERV FAC TD-352/U master unit AC POWER: ON 2 WIRE-4 WIRE: 4 WIRE ADDRESS: MASTER AUX: OUT SERV SEL: CHAN 1-12 CHAN: 1 MEASURE-PHONE ODD, PHONE EVEN: MEASURE TD-352/U slave unit. AC POWER: ON 2 WIRE-4 WIRE: 4 WIRE ADDRESS: SLAVE AUX: OUT SERV SEL: CHAN 1-12 CHAN: 2 MEASURE PHONE ODD-PHONE EVEN: MEASURE		a. Set METER SELECT switch to TIMING IN. b. Set METER SELECT switch to PCM IN-1. c. Set METER SELECT switch to PCM IN-2. d. Set METER SELECT switch to RADIO XMTR e. Set TRAFFIC SEL switch to 12.	a. TEST ALIGN meter reads in green. b. TEST ALIGN meter reads in green. c. TEST ALIGN meter reads in green. d. None. e. Hairline, or near hairline reading in yellow area of TEST ALIGN meter.
			Panel 5A3 Note. Audible and visual alarms should indicate traffic in this test.	RL on 5A3 panel for
2	No change		a. Set METER SELECT switch to FROM RADIO RCVR and adjust b. Set METER SELECT switch to SERV FAC. c. Set SERV SEL switch to A d. Set SERV SEL switch to G e. Set TRAFFIC SEL switch to 12 f. Repeat stops 2a through 2d	a. Hairline, or near hairline reading in yellow area of TEST ALIGN meter b. None. c. TEST ALIGN meter reads in green d. TEST ALIGN meter reads in green e. None. f. Same as 2a through 2d.
			Panel 5A4 Note. Audible and visual alarms should indicate traffic in this test.	
3	No change required		a. Set TRAFFIC SEL switch to 12 b. Set SERV SEL switch to B c. Set SERV SEL switch to E d. Set SERV SEL switch to F e. Set TRAFFIC SEL switch to 24I f. Repeat step 3b	a. None. b. TEST ALIGN meter reads in green c. TEST ALIGN meter reads in green d. TEST ALIGN meter reads in green e. None. f. Same as 3b.
			Panel 5A5 Note. Audible and visual alarms should indicate traffic in this test	
4	No change required		a. Set SERV SEL switch to C b. Set SERV SEL switch to D c. Set SERV SEL switch to E d. Set SERV SKI, switch to F	a. TEST ALIGN meter reads in or to right of green. b. TEST ALIGN meter reads in green c. TEST ALIGN meter reads in green d. TEST ALIGN meter reads in green
			Panel 4A6/5A6	
5	No changes required		a. Set SERV SEL switch to H b. Set SERV SEL switch to J. c. Set SERV SEL switch to K d. Set SERV SEL switch to L e. Set TRAFFIC SEL switch to 12 f. Repeat steps 5a through 5d	a. TEST ALIGN meter reads in green b. TEST ALIGN meter reads in green c. TEST ALIGN meter reads in green d. TEST ALIGN meter reads in green e. None. f. Same as 5a through 5d.
			Panel 4A8/5A8	
6	No change required		a. Set SERV SEL switch to M b. Set SERV SEL switch to N c. Set TRAFFIC SEL switch to 12 d. Repeat steps 6a and 6b	a. TEST ALIGN meter reads in green b. TEST ALIGN meter reads in green c. None. d. Same as 6a and 6b.
			Panel 4A 7/5A 7	
7	TD-352/U's not required for this step. SC-71/FCC Power ON: ON RANGE: X 10 Tuning vernier: 100 AMPLITUDE: 0.020 rms MOD. BAL. BAL.-UNBAL.: BAL. - - M E-30B/ U- Power ON-OFF: ON Range 0.3	Connect a 600-ohm termination resistor across terminals A and B of TD-202/U ORDER WIRE connector	a. Disconnect master and slave TD-352/U units. b. Remove cable between TEST OUT and FROM RADIO RCVR. c. Connect BAL. OUTPUT of SG-71/ FCC to TD-202/U FROM RADIO RCVR connector. d. Set SERV SEL switch to 0. e. Adjust ORDER WIRE LEVEL control on side panel for performance standard. f. Connect voltmeter to pins A and B of ORDER WIRE connect g. Measure order wire output level.	a. None. b. None. c. None. d. None. e. TEST ALIGN meter reads on, or near, hairline in yellow area. f. None. g. 490mv 50.
			System test	
8	No change required.		a. Set TRAFFIC SEL switch to 12. b. Connect Headset - Microphone H-91A/U to TALK MONITOR jack of TD-352/U master unit. c. Listen to 1,100-cps test tone. d. Set master TD-352/U SERV SEL switch to PHONE and listen to channel 1. e. Set TRAFFIC SEL switch to 241. f. Repeat steps 8b through 8d. g. Connect Headset-Microphone H-91A/U to TALK MONITOR jack of TD-352/U slave unit. h. Listen to 1,100-cps test tone. i. Set slave TD-352/U SERV SEL switch to PHONE: and listen to channel 2. j. Set TRAFFIC SEL switch to 24S. k. Repeat steps 8f through 8i. l. Set TEST-OPR switch to OPR. m. Set TEST-OPR switch to TEST.	a. Audible and visual alarms indicate master TD-352/U is in frame and slave TD-352/U is out of frame. TD-202/U audible and visual alarms indicate traffic. b None. c. Test tone is clear and free of distortion. d. Channel is free of any random clicks. e. Audible and visual alarms indicate both master and slave TD-352/U units are in frame. TD-202/U audible and visual alarms indicate traffic. f. Same as in 8b through 8d. g. None. h. Test tone is clear and free of distortion. i. Channel is free of any random clicks. j. Same as in 8e. k. Same as in 8f through 8i. l. Visual and audible alarms indicate both TD-352/U units are out of frame. TD-202/U audible and visual alarms indicate no traffic.. m. Same as in 8e.

5-5.1 Power Supply and Metering Tests.

a. Set input voltage to 115 Vac and adjust the 5A1 + 10, + 4.5 and-4.5 supplies to their nominal voltage

b. Vary the input over the range of 109 to 121 Vac.
See TABLE 1, Column A.

c. Set the + 10, +4.5 and -4.5 supplies for Hairline(HL) on the Test ALIGN meter. See TABLE 1, Column B.

TABLE 1

Supply	Test Point	COLUMN A Regulation Limits (Vdc)	COLUMN B Meter at HL
+ 10.0	J2	to 10.25	9.70 to 10.30
+ 4.5	J3	4.38 to 4.62	4.36 to 4.64
-4.5	J4	-4.38 to -4.62	-4.36 to-4.64
-12.0*	J5	$\pm$10% 115 V Value	Within green area

*Not adjustable.

5-6. Summary of Performance Standards, TD-202/U

Test No.	Description	Performance standard	Test data
	Transmit timing, transmit timing-in monitor, pcm input and input monitor, sampler, reshaper, and output to radio transmitter tests		
1a	Panel 5A2, 24-channel timing delay and timing in monitor circuits (METER SELECT: TIMING IN).	TEST ALIGN meter reads in green	
1b	Panel 5A2 Pam in-1 monitoring (METER SELECT: PCM IN-1).	TEST ALIGN meter reads in green	
1c	Panel 5A2 pcm in-2 monitoring (METER SELECT: PCM IN-2).	TEST ALIGN meter reads in green	
1e	Panel 5A2 sampler, reshaper and output to radio transmitter (TRAFFIC SEL: 12).	Hairline, or near hairline, reading in yellow area of TEST ALIGN meter.	
	Video amplifier, peak detector, decision, and pcm regeneration tests		
2c	Panel 5A3 video amplifier and peak detectors (SERV SEL: A, TRAFFIC SEL: 241, 24R, 24S).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
2d	Panel 5A3 decision and pcm regeneration (SERV SEL: G. TRAFFIC SEL: 241, 24R, 24S).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
2f	Panel 5A3 video amplifier and peak detectors (SERV SEL: A, TRAFFIC SEL: 12); Panel 5A3 decision and pcm regeneration (SERV SEL: G. TRAFFIC SEL: 12).	TEST ALIGN meter reads in green for each position.	
	Receive timing generator and monitoring tests		
3b	Panel 5A4 crystal-filter drive (SERV SEL: B. TRAFFIC SEL: 12).	TEST ALIGN meter reads in green	
3c	Panel 5A4 12-channel timing-2 generator (SERV SEL: E, TRAFFIC SEL: 12).	TEST ALIGN meter reads in green	
3d	Panel 5A4 12-channel timing-1 generator (SERV SEL: F. TRAFFIC SEL: 12).	TEST ALIGN meter reads in green	
3f	Panel 5A4 crystal-filter drive (SERV SEL: B. TRAFFIC SEL: 24R, 24S, 24I),	TEST ALIGN meter reads in green for all positions of TRAFFIC SEL switch.	
	Receive timing and monitoring tests		
4a	Panel 5A5 crystal-filter output monitor (SERV SEL: C, TRAFFIC SEL: 24R, 24S, 24I).	TEST ALIGN meter reads maximum for (within or to right of green area) each position of TRAFFIC SEL switch.	
4b	Panel 5A5 traffic alarm monitoring (SERV SEL: D, TRAFFIC SEL: 24R, 24S, 24I).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
4c	Panel 5A6 countdown timing (SERV SEL: E, TRAFFIC SEL: 24R, 24S, 24I).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
4d	Panel 5A5 decision timing (SERV SEL: F. TRAFFIC SEL: 24R, 24S, 24I).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	

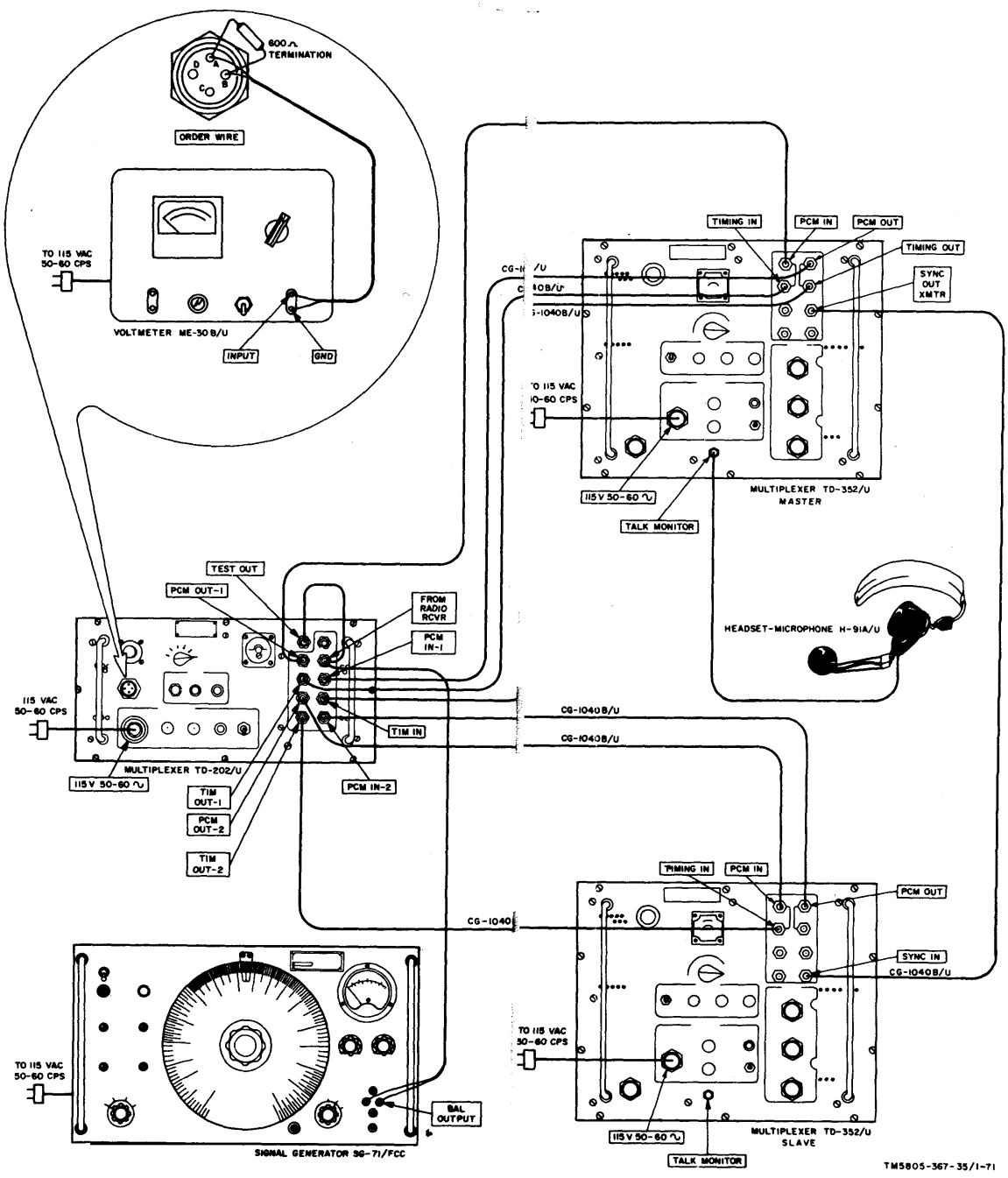


Figure 5-1. Multiplexer TD-202/U, Performance test setup.

Figure 5-1. Multiplexer TD-202/U, Performance test setup.

5-6. Summary of Performance Standards, TD-202/U-Continued

Test No.	Description	Performance standard	Test data
	Timing-A and timing-B generators, and 8-kc address-1 and address-2 generators		
5*a*	Panel 4A6/5A6 timing-A generator (SERV SEL: H. TRAFFIC SEL 24R, 24S, 24I).	TEST ALIGN meter reads in green.	
5*b*	Panel 4A6/5A6 timing-B generator (SERV SEL: J. TRAFFIC SEL: 24R, 24S, 24I).	TEST ALIGN meter reads in green.	
5*c*	Panel 4A6/5A6 8-kc address-1 generator (SERV SEL: K, TRAFFIC SEL 24R, 24S, 24I).	TEST ALIGN meter reads in green.	
5*d*	Panel 4A6/5A6 8-kc address-2 generator (SERV SEL: P. TRAFFIC SEL: 24R, 24S, 24I).	TEST ALIGN meter reads in green.	
5*f*	Panel 4A6/5A6 timing-A-generator (SERV SEL: H. TRAFFIC SEL: 24R, 24S, 24I); timing B generator (SERV SEL J. TRAFFIC SEL: 12); 8-kc address-1 generator (SERV SEL: K. TRAFFIC SEL: 12); 8-kc address-2 generator (SERV SEL: L, TRAFFIC SEL 12).	TEST ALIGN meter reads in green for each position of SERV SEL switch and TRAFFIC SEL switch.	
	Pcm-1 and pcm-2 output tests		
6*a*	Panel 4A8/5A8 pcm-1 output (SERV SEL: M, TRAFFIC SEL: 24R, 24S, 24I).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
6*b*	Panel 4A8/5A8 pcm-2 output (SERV SEL: N. TRAFFIC SEL: 24R, 24S, 24I).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
6*d*	Panel 4A8/5A8 pcm-1 output (SERV SEL: M, TRAFFIC SEL: 12); pcm-2 output (SERV SEL: N, TRAFFIC SEL: 12).	TEST ALIGN meter reads in green for each position of SERV SEL switch.	
	Orderwire tests		
7*e*	Panel 4A7/5A7 orderwire detector, amplifier and output (SERV SEL: 0).	TEST ALIGN meter reads on, or near, hairline in yellow area.	
7*g*	Panel 4A7/5A7 orderwire output level measured.	490 mv ± 50.	
	Traffic-alarm tests		
8*a*	12-channel traffic alarm (TRAFFIC SEL: 12)	Audible and visual alarms indicate master TD - 352/U is in frame, slave TD - 352/U is out of frame; TD-202/U audible and visual alarms indicate traffic.	
8*c*	Pcm-1 regeneration (modulated channel) (TRAFFIC SEL: 12).	Test tone is clear and free of distortion.	
8*d*	Pcm-1 regeneration (unmodulated channel) (TRAFFIC SEL: 12).	Channel is free of any random clicks.	
8*e*	24-channel interleaved traffic alarm (TRAFFIC SEL: 24I).	Audible and visual alarms indicate master and slave TD - 352/U's are in frame; TD-202/U alarms indicate traffic.	
8*f*	Pcm-1 regeneration (modulated channel) (TRAFFIC SEL: 24I);	Test tone in modulated channel is clear and free of distortion; unmodulated channel is free of any random clicks.	
	Pcm-1 regeneration (unmodulated channel) (TRAFFIC SEL: 24I).		
8*h*	Pcm-2 regeneration (modulated channel) (TRAFFIC SEL: 24I).	Test tone is clear and free of distortion.	
8*i*	Pcm-2 regeneration (unmodulated channel) (TRAFFIC SEL: 24I).	Channel is free of any random clicks.	

5-6. Summary of Performance Standards TD-202/U---Continued

Test No.	Description	Performance standard	Test data
8*j*	24-channel separated traffic alarm (TRAFFIC SEL: 24S).	Audible and visual alarms indicate master and slave TD-352/U's are in frame; TD-202/U audible and visual alarms indicate traffic.	
8*k*	Pcm-1 regeneration (modulated channel, unmodulated channel) (TRAFFIC SEL: 24S); Pcm-2 regeneration (modulated channel, unmodulated channel) (TRAFFIC SEL: 24S).	Test tone in modulated channels is clear and free of distortion; unmodulated channels are free of any random clicks.	
8*l*	Skip pulse generation (TEST-OPR: OPR)	Audible and visual alarms indicate both TD-352/U's are out of frame; TD-202/U alarms indicate no traffic.	
8*m*	Framing operation (TEST-OPR: TEST)	Audible and visual alarms indicate master and slave TD-352/U's are in frame; TD-202/U alarms indicate traffic.	

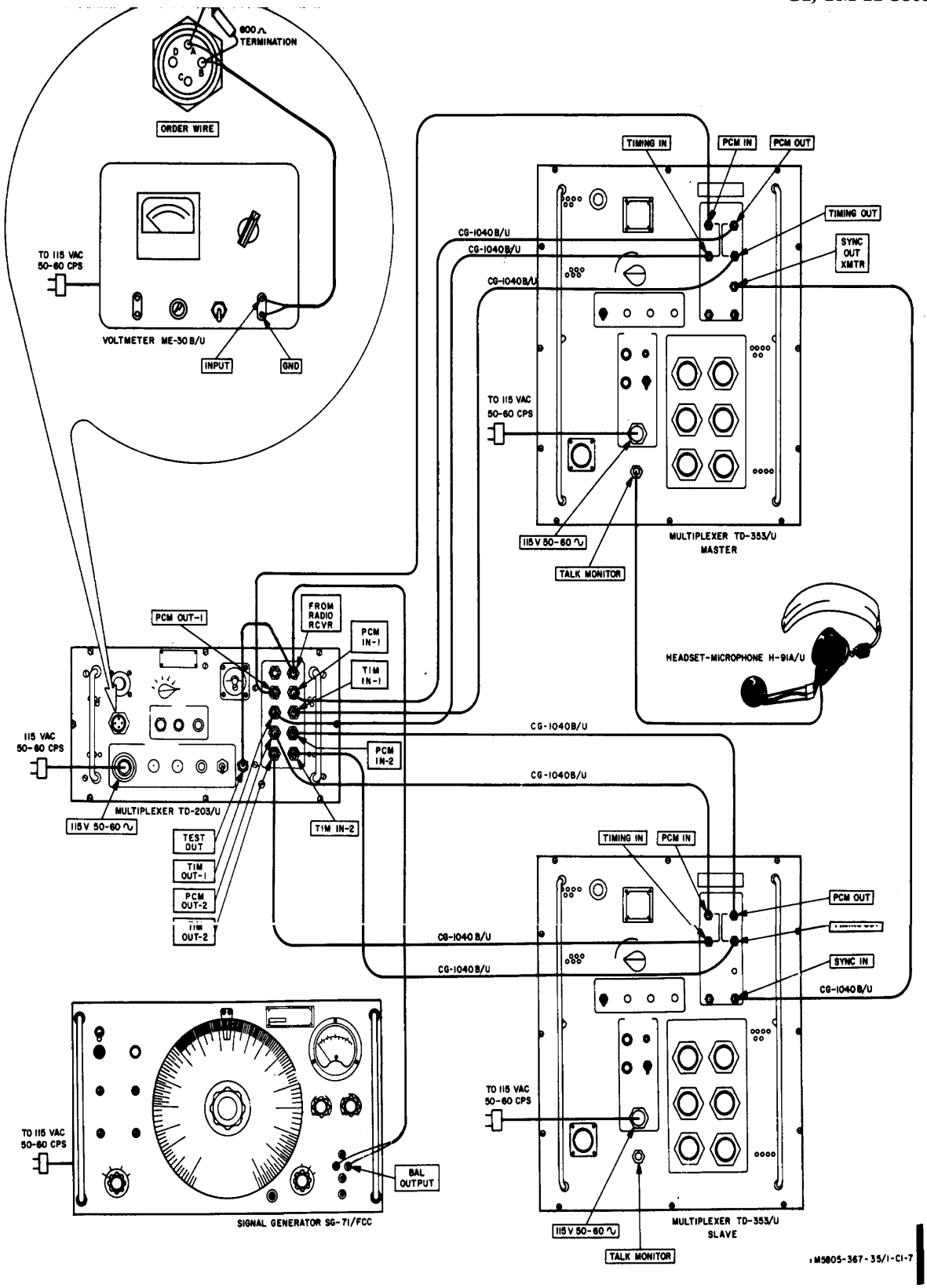


Figure 5-2. Multiplexer TD-203/U, performance test setup.

5-7 Performance Tests, TD-203/U

(fig.5 - 2)

a. Test Equipment and Materials

(1) Multiplexer TD-353/U (2 required).

(2) Signal Generator SG-71/FCC.

(3) Voltmeter, Electronic ME 30B/U.

(4) Headset-Microphone H-91A/U.

(5) Cable assembly, radiofrequency, type CG-1040B/U (8 required).

b. Test Connections and Conditions. Connect the TR - 203/U and the TD-353/U master and slave units as shown in figure 5.2. Do not connect signal generator, headset-microphone or voltmeter until told to do so.

c. Test Procedure.

Note. Unless specifically stated otherwise, all procedure instructions and performance standards pertain to the TD-203/U test unit.

Step No.	Control settings		Test procedures	Performance standard
	Test equipment	Equipment under test		
			Panel 4A2	
			Note. Audible and visual alarms should indicate traffic In this test.	
1	TD-203/U test unit AC POWER: ON OPR-TEST: TEST TRAFFIC SEL: 96I METER SELECT: SERV FAC TD-353/U master unit AC POWER: ON 2 WIRE-4 WIRE: 4 WIRE ADDRESS: MASTER AUX: OUT SERV SEL: E ODD CHAN: 1 MEASURE-PHONE ODD-PHONE EVEN: PHONE ODD TD-353/U slave unit. AC POWER: ON 2 WIRE-4 WIRE: 4 WIRE ADDRESS: SLAVE AUX: OUT SERV SEL: E EVEN CHAN: 2 MEASURE-PHONE ODD-PHONE EVEN: PHONE EVEN		*a.* Set METER SELECT switch to TIMING IN-1. *b.* Set METER SELECT switch to PCM IN-1. *c.* Set METER SELECT switch to TO RADIO XMTR. *d.* Set TRAFFIC SEL switch to 48 *Panel - 01 4A10* *e.* Set METER SELECT switch to TIMING IN-2 *f.* Set METER SELECT switch to PCM in-2. *Panel A43* Note Audible and visual alarms indicate traffic in this test	*a.* TEST A LIGN meter reads in green. *b.* TEST ALIGN meter reads in green. *c.* None. *d.* Hairline, or near hairline, reading in yellow area of TEST ASSIGN meter. *e.* TEST ALIGN meter reads in green. *f.* TEST ALIGN meter reads in green.
2	No change required		*a.* Set METER SELECT switch to FROM RADIO RCVR. *b.* Set METER SELECT switch to SERV FAC. *c.* Set SERV SEL switch to A *d.* Set SERV SEL switch to G *e.* Set TRAFFIC SEL switch to 48 *f.* Repeat steps *a* through *d* above *Panel 4A4* *Note.* Audible and visual alarms should indicate traffic in this test.	*a.* Hairline, or near hairline, reading in yellow area of TEST ALIGN meter. *b.* None. *c.* TEST ALIGN meter read., in green. *d.* TEST ALIGN meter reads in green. *e.* None. *f.* Same as *a* through *d* above.
3	No change required		*a.* Set TRAFFIC SEL switch to 48 . *b.* Set SERV SEL switch to B *c.* Set SERV SEL switch to E *d.* Set SERV SEL switch to F *e.* Set TRAFFIC SEL switch to 96I *f.* Repeat step *b* above *Panel 4A5* *Note*. Audible and visual alarms should indicate traffic in this test.	*a.* None. *b.* TEST ALIGN meter reads in green *c.* TEST ALIGN meter reads in green. *d.* TEST ALIGN meter reads in green. *e.* None. *f.* Same as *b* above.
4	No change required		*a.* Set SERV SEL switch to C and adjust CL on 4A3 panel for peak *b.* Set SERV SEL switch to D *c.* Set SERV SEL switch to E *d.* Set SERV SEL switch to F *e.* Set TRAFFIC SEL switch to 48 *f.* Repeat Steps *b* through *d* above *Panel 4A6/5A6*	*a.* *TEST* ALIGN meter indicates 1/6 scale or above *b.* TEST ALIGN meter reads in green. *c.* TEST ALIGN meter reads in green. *d.* TEST ALIGN meter reads in green. *e.* None. *f.* Same as *b* through *d* above
5	No change required		*a.* Set SERV SEL switch to H *b.* Set SERV SEL switch to J. *c.* Set SERV SEL switch to K *d.* Set SERV SEL switch to L *e.* Set TRAFFIC SEL switch to 48 *f.* Repeat steps *a* through *d* above *Panel 4A8l5A8*	*a.* TEST ALIGN meter reads in green. *b.* TEST ALIGN meter reads in green. *c.* TEST ALIGN meter reads in green. *d.* TEST ALIGN meter reads in green. *e.* None. *f.* Same as *a* through d above.
6	No change required		*a.* Set SERV SEL switch to M . *b.* Set SERV SEL switch to N *c.* Set TRAFFIC SEL switch to 48 *d.* Repeat Steps *a* and *b* above *Panel 4A9*	*a.* TEST ALIGN meter reads in green. *b.* TEST ALIGN meter reads in green. *c.* None. *d.* Same as *a* and *b* above.
7	No change required		*a.* Set TRAFFIC SEL switch to 96R, 96S, 96I. *b.* Set SERV SEL switch to E *c.* Set SERV SEL switch to H *d.* Set SERV SEL switch to J *e.* Set SERV SEL switch to K *f.* Set SERV SEL switch to L *g.* Set TRAFFIC SEL switch to 48 *h.* Repeat steps *c* through *f* above	*a.* None. *b.* TEST ALIGN meter reads in green. *c.* TEST ALIGN meter reads in green. d. TEST ALIGN meter reads in green. *e.* TEST ALIGN meter reads in green. *f.* TEST ALIGN meter reads in green. g. None. *h.* Same as *c* through *f* above.

			Panel 4A7/5A7	
8	TD-353/U's not required for this step. SG-71/FCC POWER ON: ON RANGE: X10 Tuning vernier: 100 AMPLITUDE:0.020 rms MOD. BAL.— BAL.-UNBAL BAL.. ME-30B/U Power ON-OFF: ON Range: 0.3 :	Connect a 600-ohm termination resistor across terminals A and B of TD-203/U ORDER WIRE connector.	*a*. Disconnect master and slave TD-353/U units. *b.* Remove cable between TEST OUT and FROM RADIO RCVR. *c*. Connect BAL. OUTPUT of SG-71/FCC to TD-203/U FROM RADIO RCVR connector. *d*. Set SERV SEL switch to 0. e. Adjust ORDER WIRE LEVEL control on side panel for performance standard. *f*. Connect voltmeter to pins A and B of ORDER WIRE connector. *g.* Measure order-wire output level *System Test*	*a*. None. *b.* None. *c*. None. *e*. TEST ALIGN meter reads on, or near, hairline in yellow area. *f*. None. *g* 490 mv ± 50.
9	Same as step 1 plus*:* SG-71/FCC Same as step 8		a. Set TEST-OPR switch to OPR b. Set TEST-OPR switch to TEST. c. Set TRAFFIC SEL switch to 48 d. Connect Headset-Microphone H-9lA /U to TALK MONITOR Jack of master TD-353 /U and listen to channel 1. e. Connect BAL output of SG-71 /FCC to master TD-353 CHAN 1-8 connector, pins A and B (channel 1). f. Adjust SG-71/FCC output level for performance standard. g. Listen to 1,000 Hz tone. h. Set TRAFFIC SEL switch to 96I. i. Repeat steps d through g above. j Set TRAFFIC SEL switch to 96S. k. Repeat steps d through g above. l. Connect Headset-Microphone H-91A/U to TALK MONITOR Jack of slave TD-353 /U and listen to channel 2. m. Connect BAL output of SG-71/FCC to slave TD-353/U CHAN 1-8 connector pins X and Y (channel 2). n. Repeat steps f and g above. o. Set TRAFFIC SEL switch to 96I. p. Repeat steps 1 through n above.	a. Visual and audible alarms indicate both TD-353/U units are out of frame. TD-203/U audible and visual alarms indicate no traffic. b. Audible and visual alarms indicate both TD-353/U units are in frame. TD-203/U audible and visual alarms indicate traffic. c. Audible and visual alarms indicate master TD-353 /U is in frame and slave TD-353 /U is out of frame. TD-203/U audible and visual alarms indicate traffic. d. Channel is free of any random clicks. e. None f. TEST ALIGN meter reads on hairline in yellow area (SERV SEL E). g. Tone is clear and free of distortion. h. Same as step b above i. Same as steps d through g above. J. Same as step b above k. Same as steps d through g above. l. Channel is free of any random clicks. m. None. n. Same as steps f and g above. o. Same as step b above. p. Same as steps l through n above.

5-8. Summary of Performance Standards, TD-203/U

Test No.	Description	Performance standard	Test data
	Transmit timing,, transmit timing-in monitor, pcm input and input monitor, sampler, reshaper and output to radio transmitter tests		
1a	Panel 4A2, 96-channel timing delay and timing in monitor circuits (METER SELECT: TIMING IN-1).	TEST ALIGN meter reads in green.	
1b	Panel 4A2 pcm in-1 monitoring (METER SELECT: PCM IN-1).	TEST ALIGN meter reads in green.	
1d	Panel 4A2 sampler, reshaper and output to radio transmitter (TRAFFIC SEL: 48).	Hairline or near hairline reading in yellow area of TEST align meter	
1e	Panel 4A10, 90-channel timing delay and timing - in-2 monitor circuits (METER SELECT: TIMING IN-2).	TEST ALIGN meter indicates green area.	
1f	Panel 410 pcm 4A2 monitoring (METER SELECT: PCM IN-2).	TEST ALIGN meter indicates in green area	
	Video amplifier, peak-a-detector decision and pcm regeneration tests		
2c	Panel 4A3 video amplifier and peak detectors (SERV SEL: A, TRAFFIC SEL: 96I, 96R, 96S).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
2d	Panel 4A3 decision and pcm regeneration (SERV SEL: G. TRAFFIC SEL: 96I, 96R, 96S).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
2f	Panel 4A3 video amplifier and peak detectors (SERV SEL: A, TRAFFIC SEL: 48).	TEST ALIGN meter reads in green for each position.	
	Panel 4A3 decision and pcm regeneration (SERV SEL: G. TRAFFIC SEL: 48).		
	Receive timing generator and monitoring tests		
3b	Panel 4A4 crystal-filter drive (SERV SEL: B, TRAFFIC SEL: 48).	TEST ALIGN meter reads in green.	
3c	Panel 4A4 48-channel timing-2 generator (SERV SEL: E, TRAFFIC SEL: 48).	TEST ALIGN meter reads in green.	
3d	Panel 4A4 48-channel timing-l generator (SERV SEL: F, TRAFFIC SEL: 48).	TEST ALIGN meter reads in green.	
3f	Panel 4A4 crystal-filter drive (SERV SEL: B, TRAFFIC SEL: 96R, 96S, 96I); 96-channel timing-2 generator (SERV SEL: E, TRAFFIC SEL: 96R, 96S, 96I); 96-channel timing-l generator (SERV SEL: F, TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green for all positions of TRAFFIC SEL switch.	
	Receive timing and monitoring tests	1/6 scale or above	
4a	Panel 4A5 crystal filter output monitor (SERV SEL: C, TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads ∧ for each position of TRAFFIC SEL switch.	
4b	Panel 4A5 traffic-alarm monitoring (SERV SEL: D, TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
4c	Panel 4A5 countdown timing (SERV SEL: E, TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
4d	Panel 4A5 decision timing (SERV SEL: F, TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	

5-8. Summary of Performance Standards, TD-203/U-Continued

Test No.	Description	Performance standard	Test data
4f	Panel 4A5 crystal-filter output monitor (SERV SEL: C, TRAFFIC SEL: 48); traffic-alarm monitoring (SERV SEL: D, TRAFFIC SEL: 48); countdown timing (SERV SEL: E, TRAFFIC SEL: 48); decision timing (SERV SEL: F. TRAFFIC SEL: 48).	TEST ALIGN meter reads in green for each | position of SERV SEL switch.	
	Timing-A and timing-B generators, *and 8-kc address-1* and *address-2 generators*		
5a	Panel 4A6/5A6 timing-A generator (SERV SEL: H. TRAFFIC SEL: 48).	TEST ALIGN meter reads in green	
5b	Panel 4A6/5A6 timing-B generator (SERV SEL: J. TRAFFIC SEL: 48).	TEST ALIGN meter reads in green	
5c	Panel 4A6/5A6 8-kc address-1 generator (SERV SEL: K TRAFFIC SEL: 48).	TEST ALIGN meter reads in green	
5d	Panel 4A6/5A6 8-kc address-2 generator (SERV SEL: L, TRAFFIC SEL: 48).	TEST ALIGN meter reads in green	
5f	Panel 4A6/5A6 timing-A generator (SERV SEL: H. TRAFFIC SEL: 96R, 96S, 96I); timing-B generator (SERV SEL: J. TRAFFIC SEL: 96R, 96S, 96I); 8-kc address-1 generator (SERV SEL: X, TRAFFIC SEL: 96R, 86S, 96I); 8-kc addressed generator (SERV SEL: L, TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green for each position of SERV SEL switch and TRAFFIC SEL switch.	
	Pcm-1 and pcm-2 output tests		
6a	Panel 4A8/5A8 pcm-1 output (SERV SEL: M, TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
6b	Panel 4A8/5A8 pcm-2 output (SERV SEL: N. TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green for each position of TRAFFIC SEL switch.	
6d	Panel 4A8/5A8 pcm-1 output (SERV SEL: M, TRAFFIC SEL: 48); pcm-2 output (SERV SEL: N. TRAFFIC SEL: 48).	TEST ALIGN meter reads in green for each position of SERV SEL switch.	
	High tragic timing *drive and timing control tests*		
7b	Panel 4A9 96-channel timing-2 drive (SERV SEL: E, TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green	
7c	Panel 4A9 ht timing-1 control (SERV SEL: H. TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green	
7d	Panel 4A9 ht timing-2 control (SERV SEL: J. TRAFFIC SEL**:** 96R, 96S, 96I).	TEST ALIGN meter reads in green	
7e	Panel 4A9 8-kc address-2 control (SERV SEL: X, TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green	
7f	Panel 4A9 8-kc address-2 control (SERV SEL: L, TRAFFIC SEL: 96R, 96S, 96I).	TEST ALIGN meter reads in green	
7h	Panel 4A9 96-channel timing-2 drive (SERV SEL: E, TRAFFIC SEL: 48); ht timing-1 control (SERV SEL: H. TRAFFIC SEL: 48); ht timing-2 control (SERV SEL: J. TRAFFIC SEL: 48); address-2 control (SERV SEL: X, TRAFFIC SEL: 48); addresa-2 control (SERV SEL: L, TRAFFIC SEL: 48).	TEST ALIGN meter reads in green for each position of SERV SEL switch.	

5 8. Summary of Performance Standards, TD-203/U-Continued

Test No.	Description	Performance standard	Test data
	Order-wire tests		
8e	Panel 4A7/5A7 order-wire detector, amplifier and output (SERV SEL: 0).	TEST ALIGN meter reads on or near hairline in yellow area.	
8g	Panel 4A7/5A7 order-wire output level measured.	490 mv ±50	
	Traffic -alarm tests		
9a	Skip pulse generation (TEST-OPR: OPR).	Audible and visual alarms indicate both TD-353/U's are out of frame; TD-203/U alarms indicate no traffic	
9b	Framing operation (TEST-OPR: TEST).	Audible and visual alarms indicate master and slave TD353/U's are in frame; TD-203/U alarms indicate traffic.	
9c	48-channel traffic alarm (TRAFFIC SEL: 48).	Audible and visual alarms indicate master TD-353/U is in frame, slave TD-353/U is out of frame; TD-203/U audible and visual alarms indicate traffic	
9d	Pcm-1 regeneration (unmodulated channel) (TRAFFIC SEL: 48).	Channel is free of any random clicks.	
9g	Pcm-1 regeneration (modulated channel) (TRAFFIC SEL: 48).	Test tone is clear and free of distortion.	
9h	96-channel interleaved traffic alarm (TRAFFIC SEL: 96I).	Audible and visual alarms indicate master and slave TD353/U's are in frame; TD-203/U alarms indicate traffic.	
9i	Pcm-1 regeneration (modulated channel) (TRAFFIC SEL: 96I). Pcm-l regeneration (unmodulated channel) (TRAFFIC SEL: 96I).	Test tone in modulated channel is clear and free of distortion; unmodulated channel is free of any random clicks.	
9j	96-channel separated traffic alarm (TRAFFIC SEL: 96S).	Audible and visual alarms indicate master and slave TD353/U's are in frame; TD-203/U audible and visual alarms indicate traffic.	
9k	Pcm-1 regeneration (modulated channel, unmodulated channel) (TRAFFIC SEL: 96S)	Test tone in modulated channels is clear and free of distortion; unmodulated channels are free of any random clicks.	
9l	Pcm-2 regeneration (unmodulated channel) (TRAFFIC SEL: 96S).	Channel is free of any random clicks.	
9n	Pcm-2 regeneration (modulated channel) (TRAFFIC SEL: 96S)	Test tone is clear and free of distortion.	
9p	Pcm-2 regeneration (modulated channel, unmodulated channel) (TRAFFIC SEL: 96I).	Test tone in modulated channels is clear and free of distortion; unmodulated channels are free of any random clicks.	

CHAPTER 6

DEPOT OVERHAUL STANDARDS

6-1 . Applicability of Depot Overhaul Standards

The depot overhaul standards are designed to measure the performance capability of a repaired equipment. Equipment that meets the minimum standards will have performance capabilities equivalent to that of new equipment.

6-2. Applicable References

a. *Repair Standards.* Applicable procedures of the depot performing these tests and the general standards for repaired electronic equipment given in TB SIG 355-1, TB SIG 355-2, and TB SIG 355-3 form a part of the requirements for testing this equipment.

b. *Modification Work* Orders. Perform all modification work orders applicable to this equipment before making the tests specified. DA Pam 310 -4 lists all available MWO's.

6-3. Depot Overhaul Standard

When depot repair and overhaul has been completed, perform the procedures in chapter 5. When the equipment has been tested, repackage it for stockage.

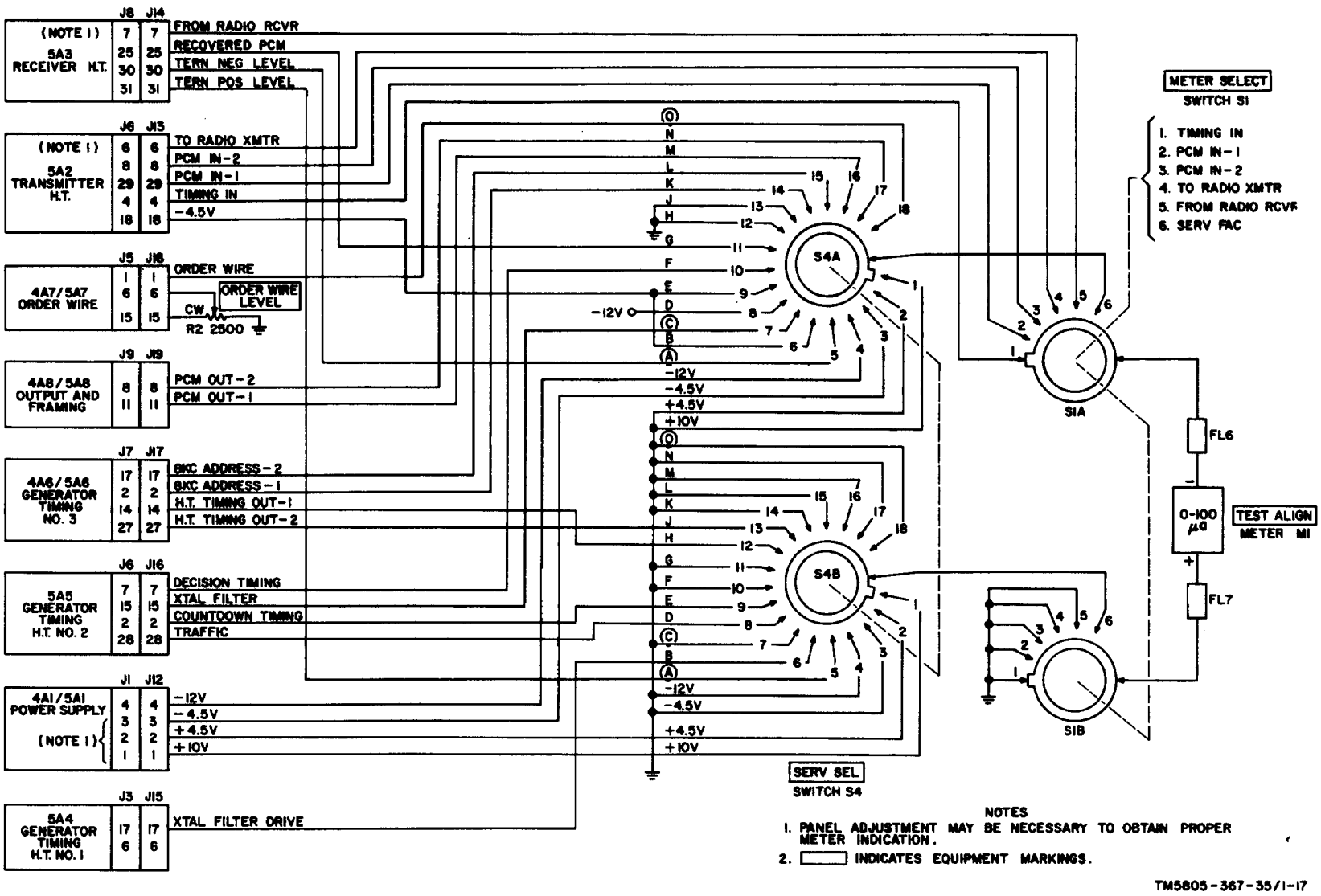


Figure 6-1. Multiplexer TD-202/U, test circuits, simplified schematic diagram.

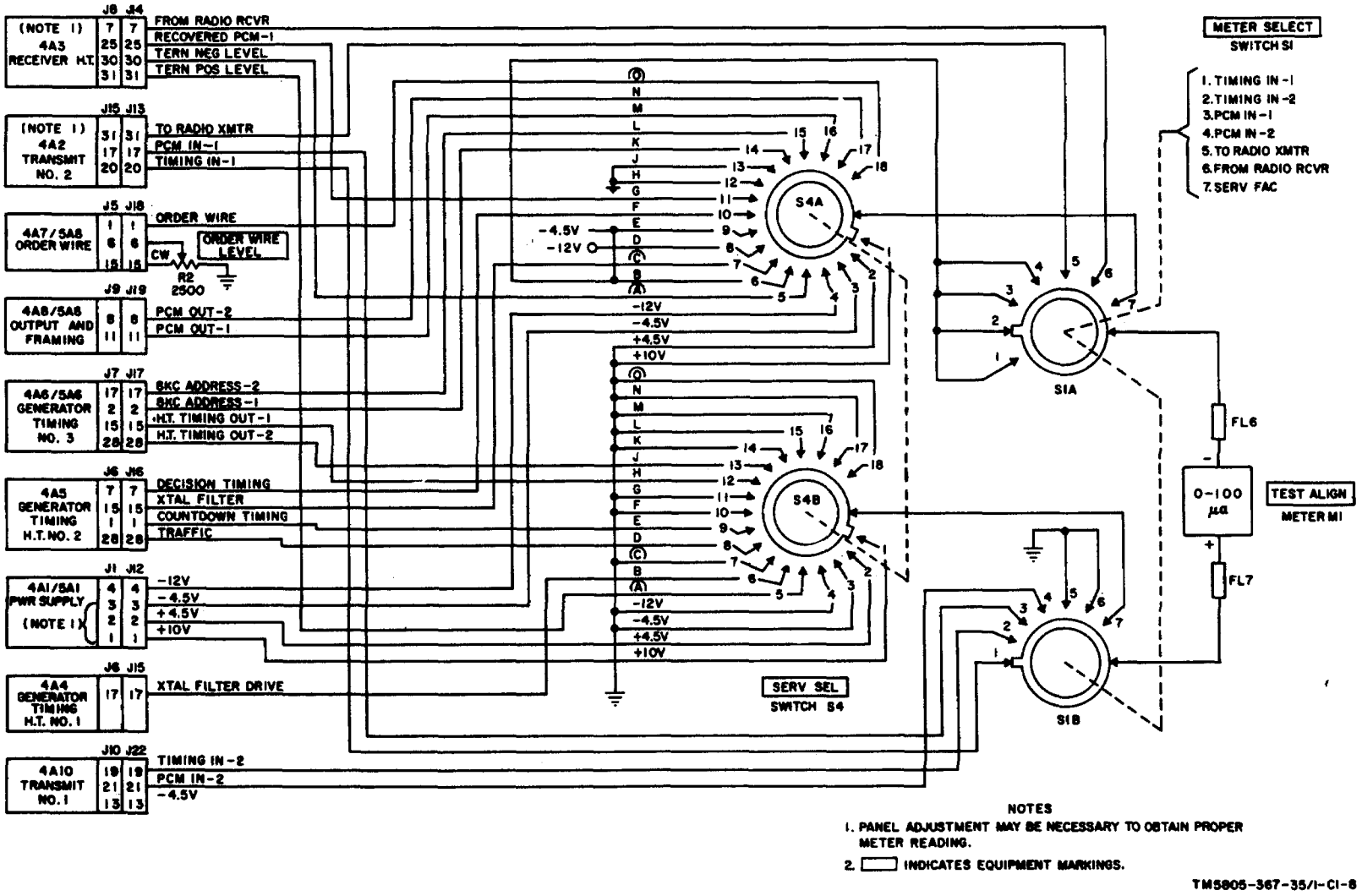


Figure 6-2. Multiplexer TD-203/U, test circuits, simplified schematic diagram.

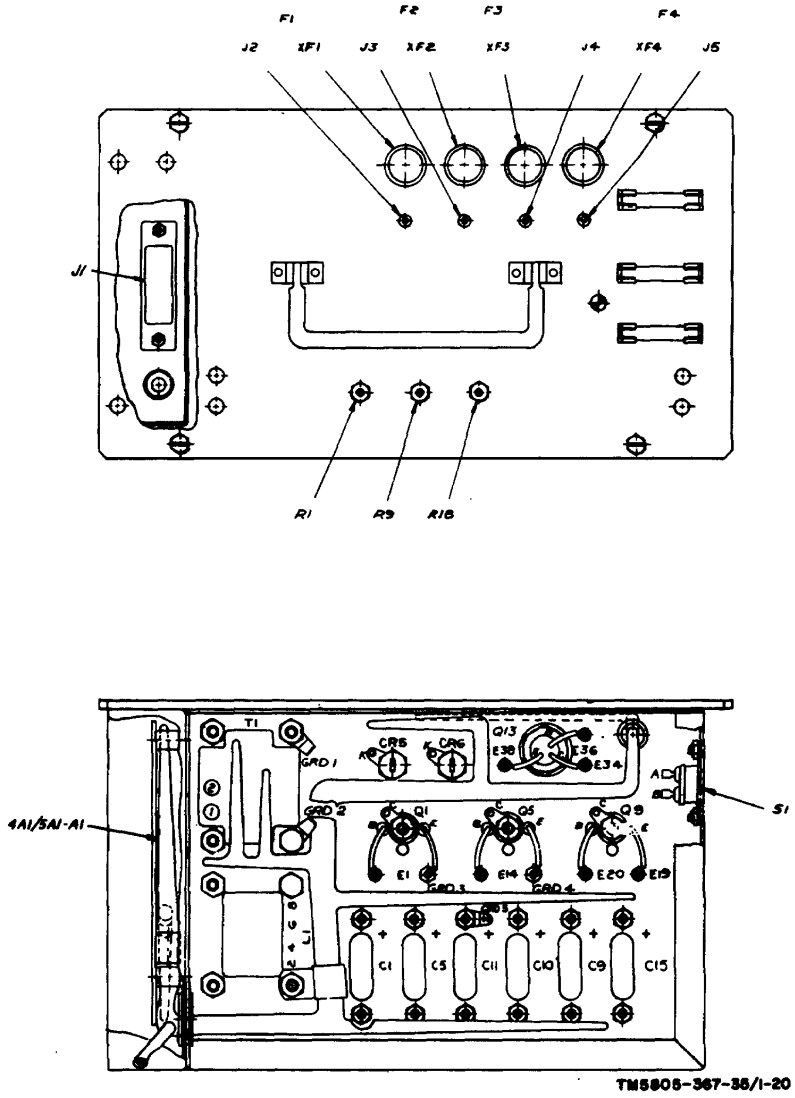


Figure 6-3. Power supply, panel 4A1/5A1, component location diagram.

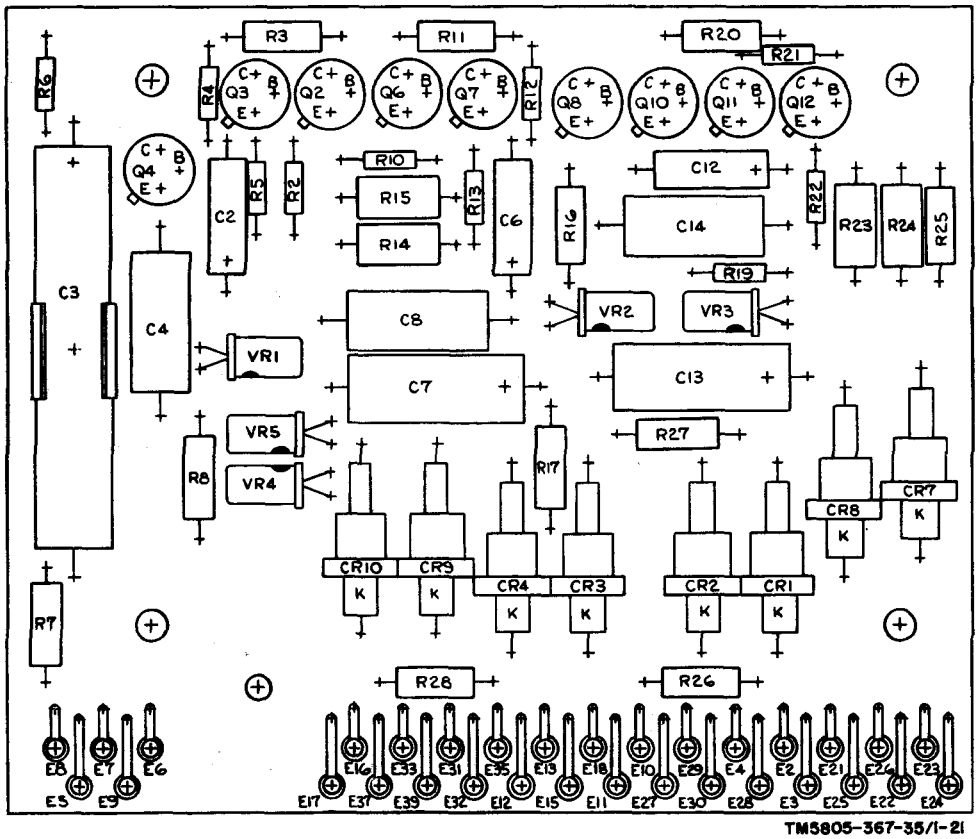


Figure 6-4. Power supply, panel 4A1/5A1-A1, top panel view.

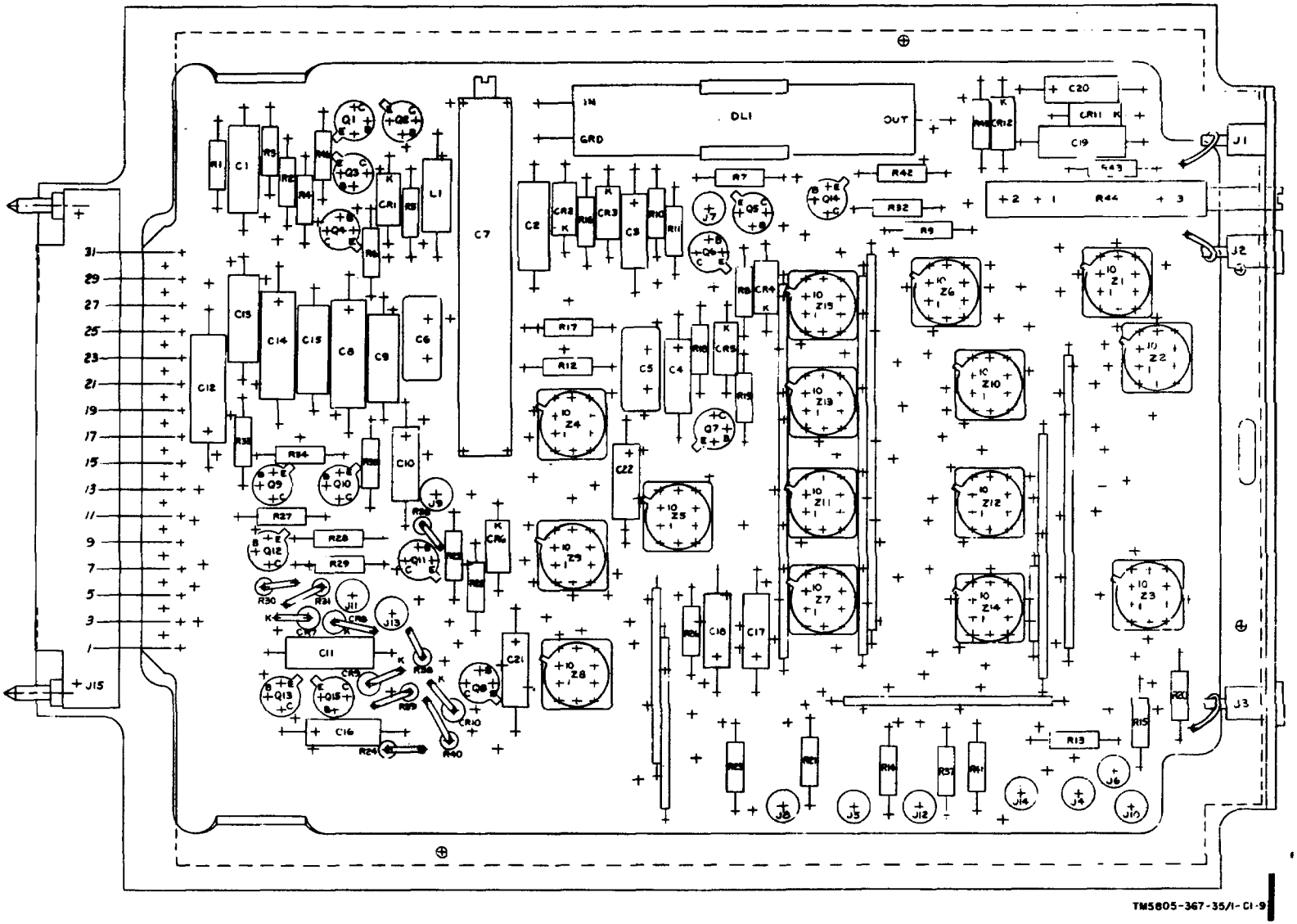


Figure 6-5. Transmit panel No. 2, panel 4A2, top panel view.

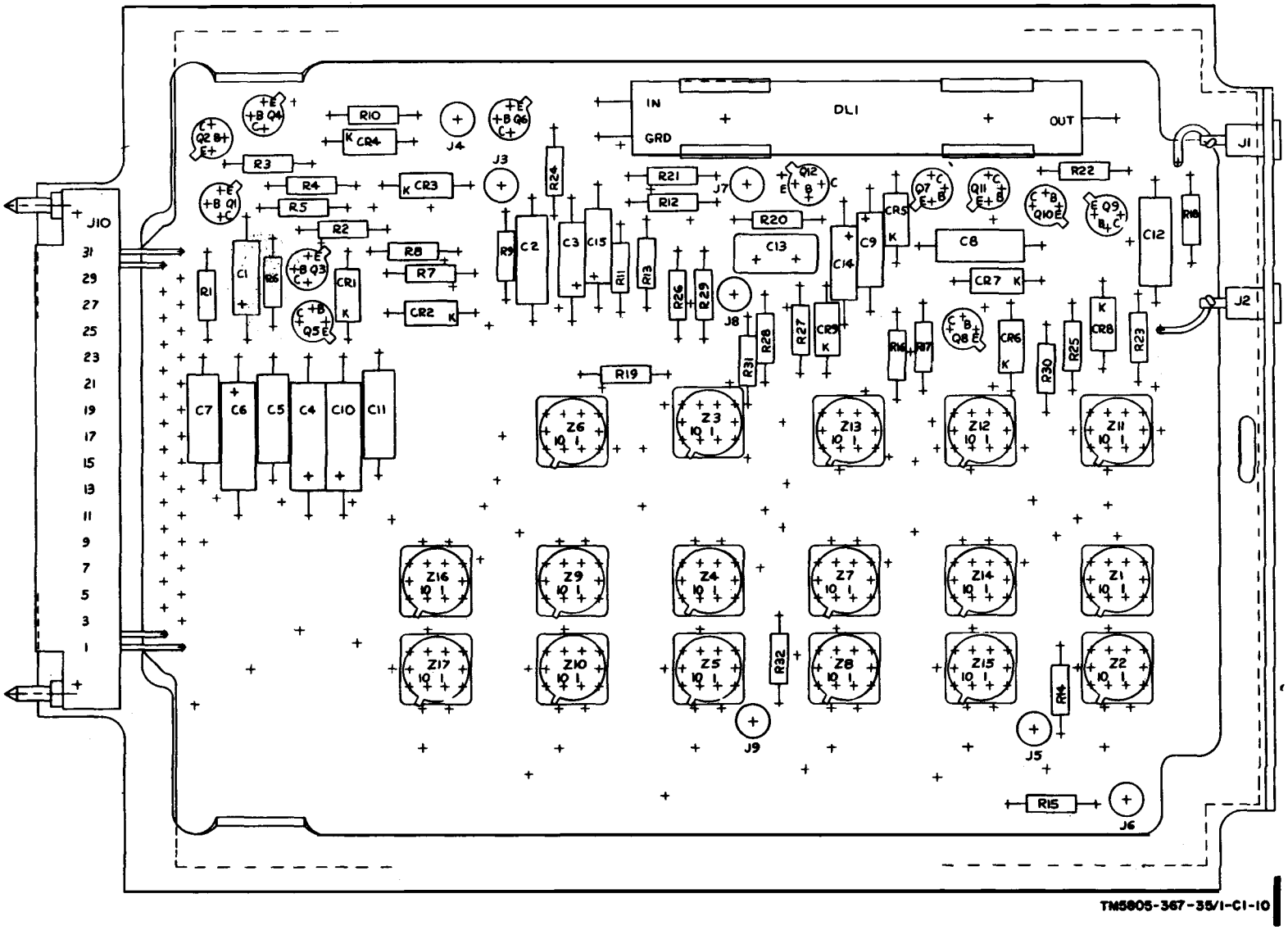


Figure 6-5.1. Transmit No.1, panel 4A10, top panel view.

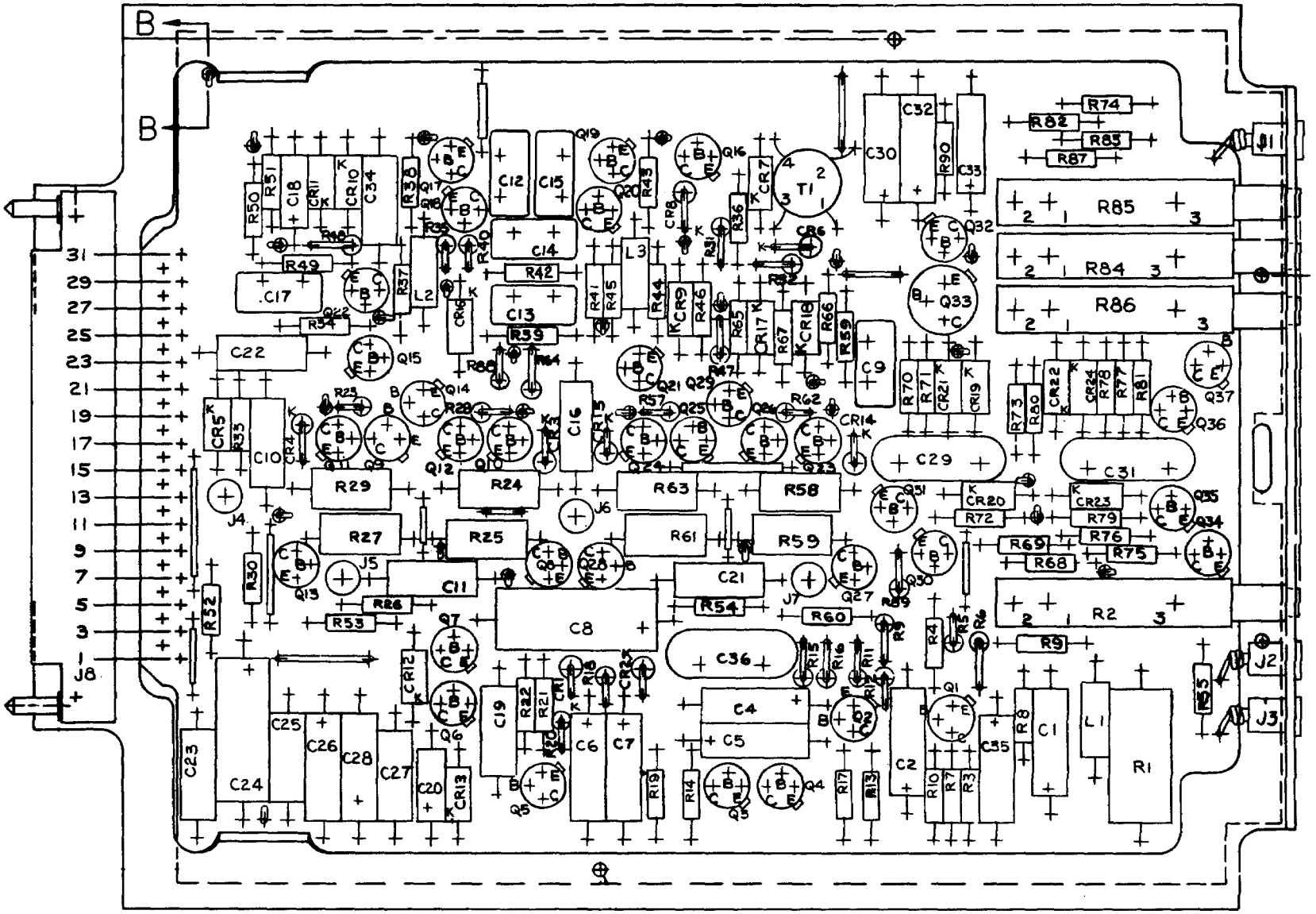


Figure 6-6. Receiver, panel 4A3, top panel view.

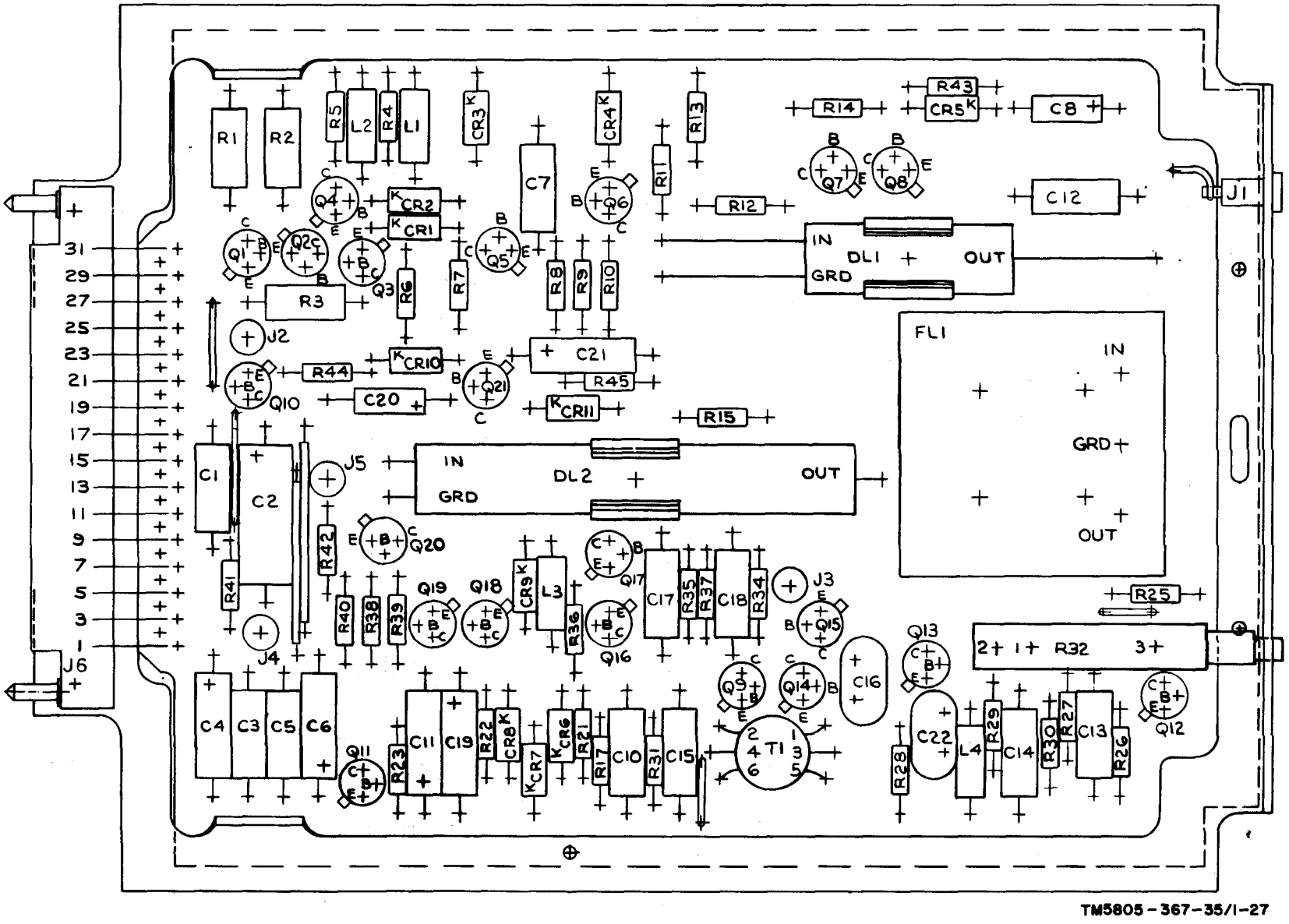


Figure 6-7. Timing generator No. 1, panel 4A4, top panel view.

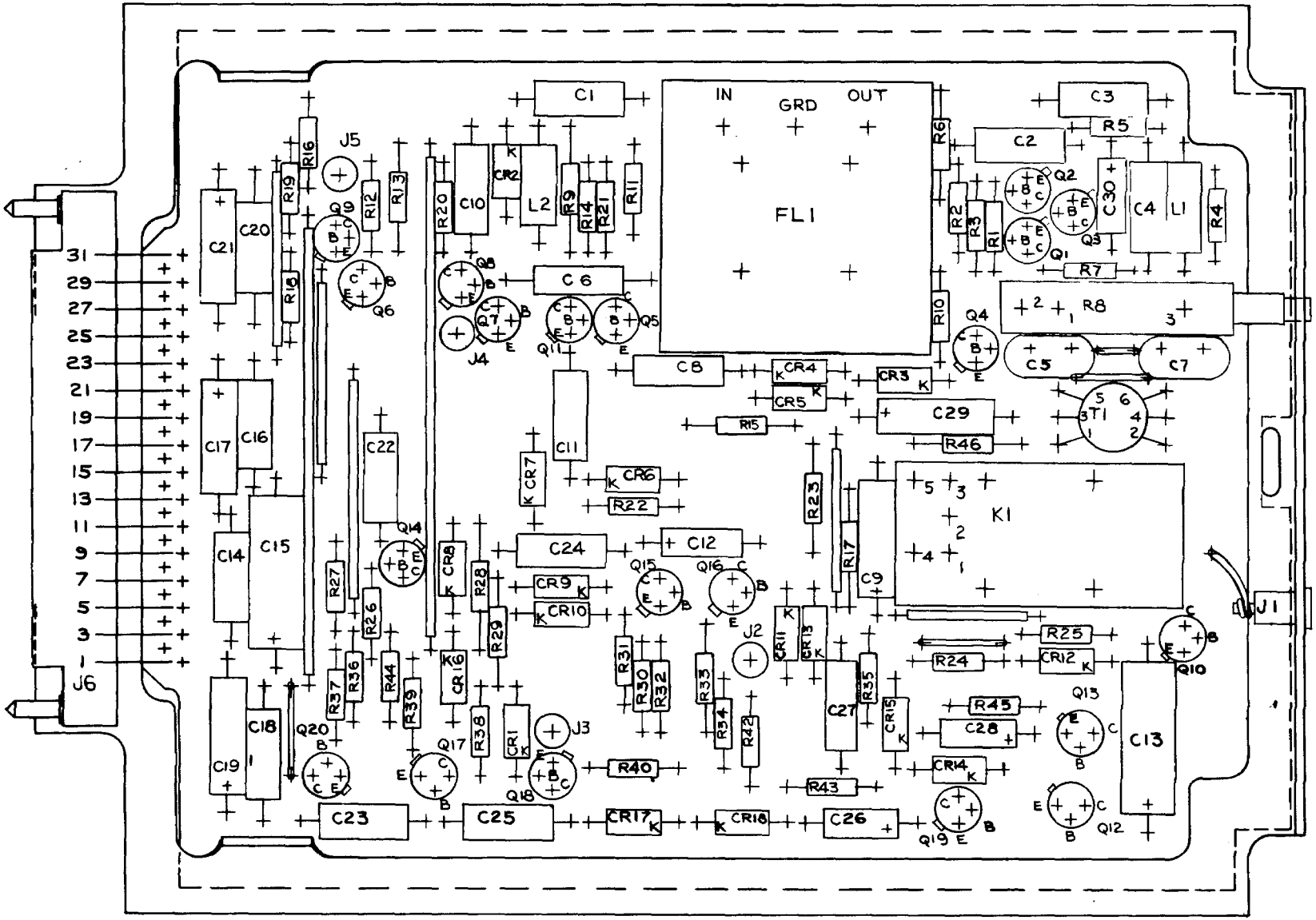


Figure 6-8. Timing generator No.2, panel 4A5, top panel view.

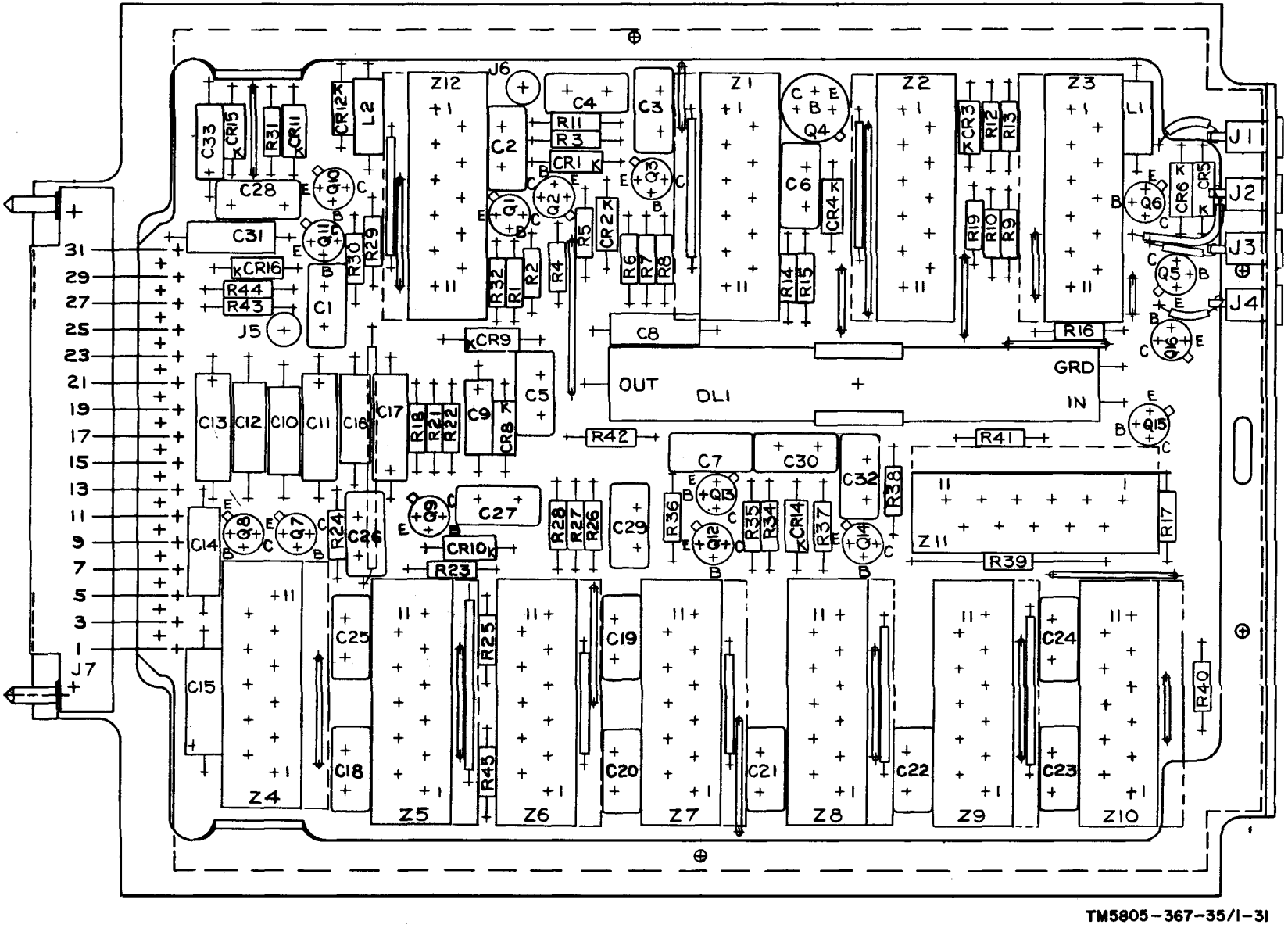


Figure 6-9. Timing generator No. 3, panel 4A6/5A6, top panel view.

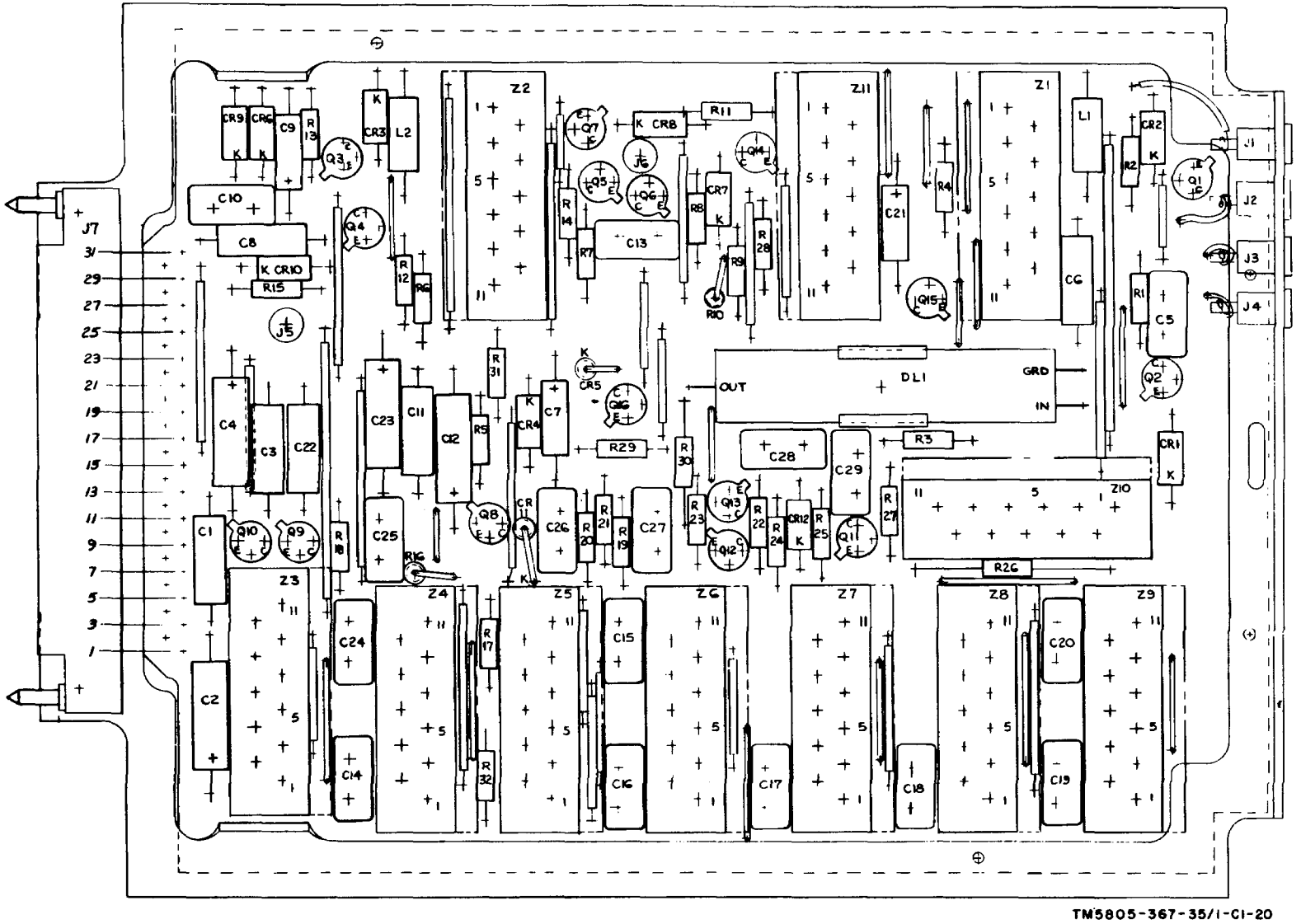


Figure 6-9.1. Timing generator No.3, panel 4A11, top view.

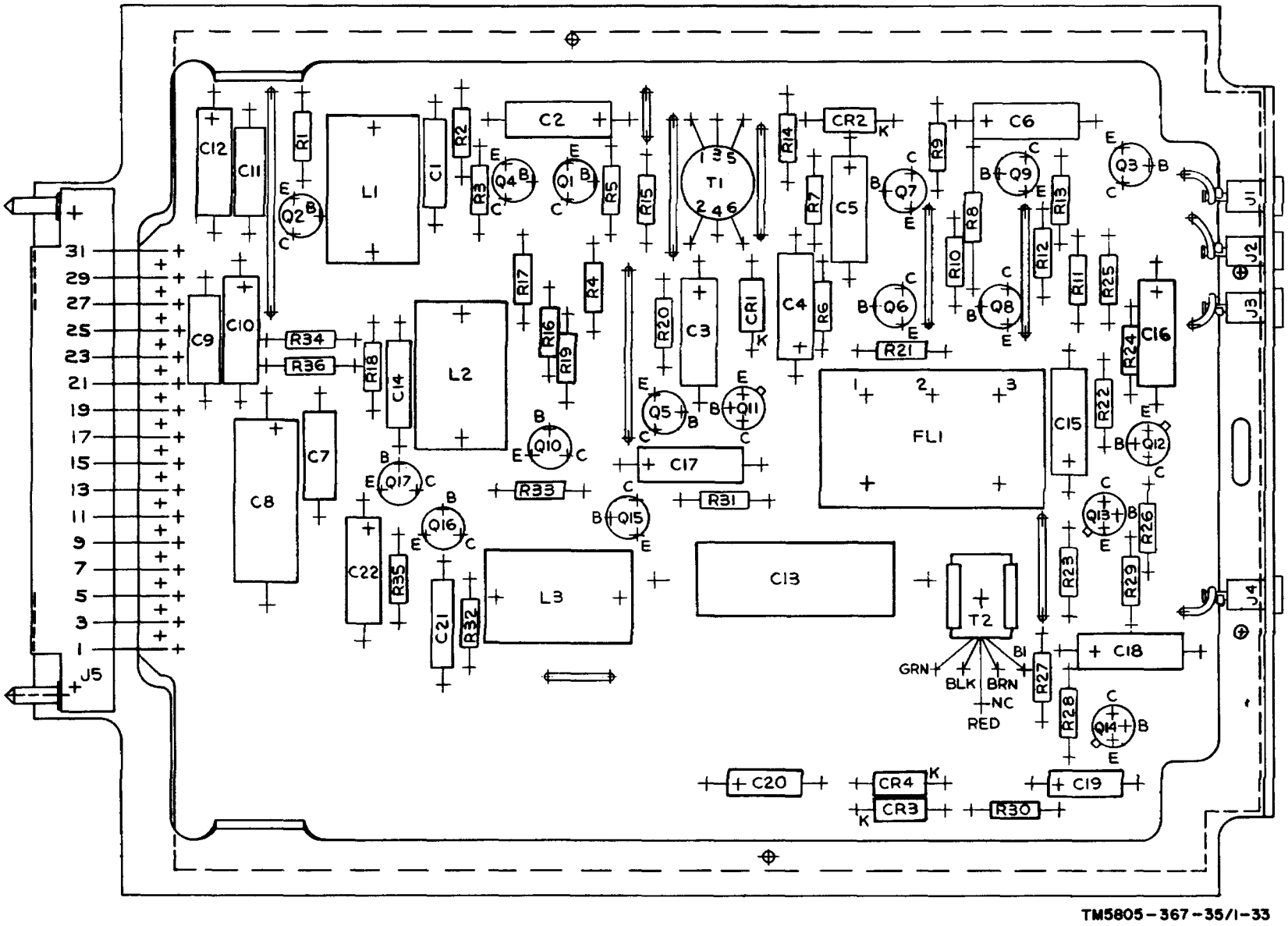


Figure 6-10. Order wire, panel 4A7/5A7, top panel view.

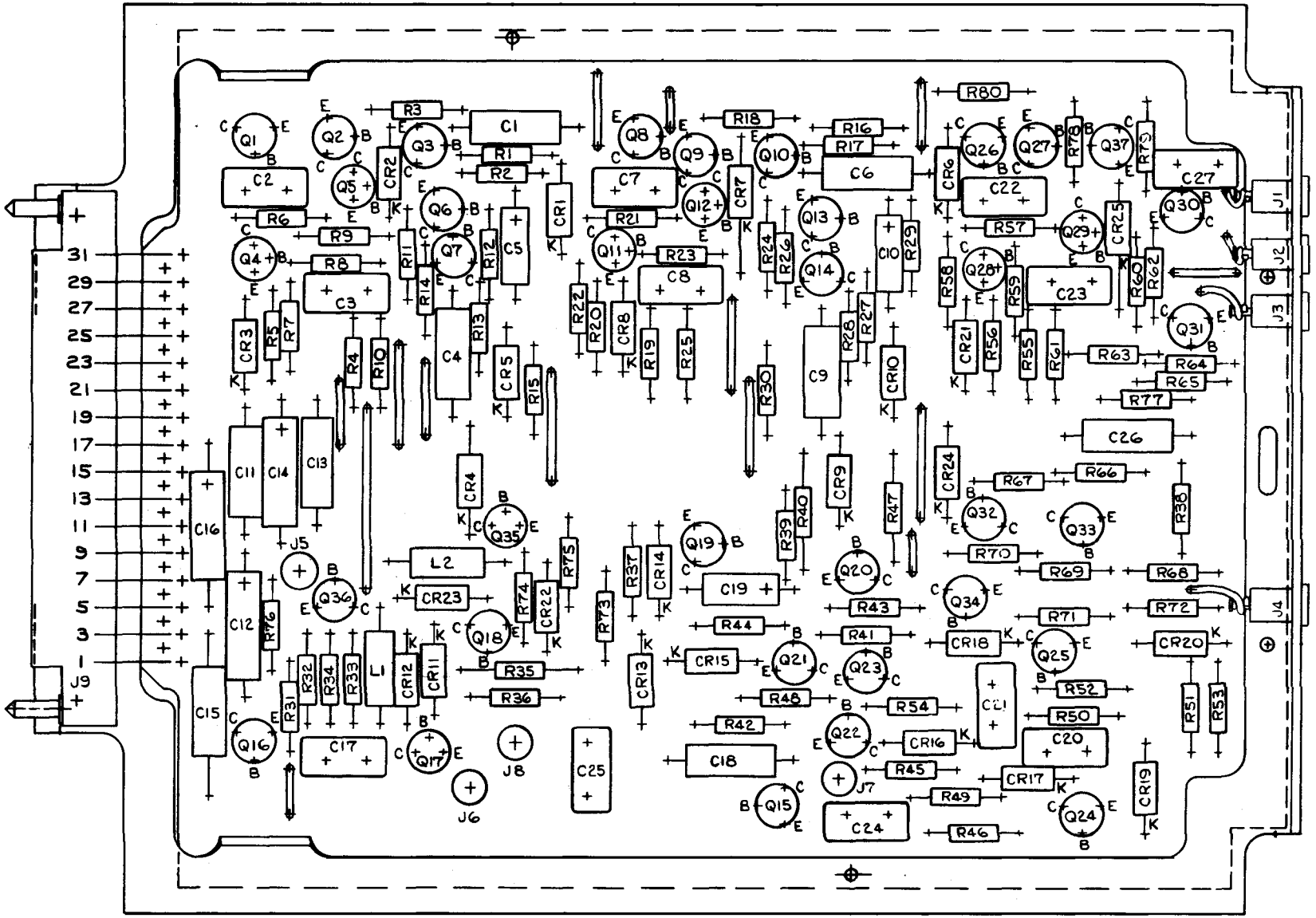


Figure 6-11. Detector framing, panel 4A8/5A8, top panel view

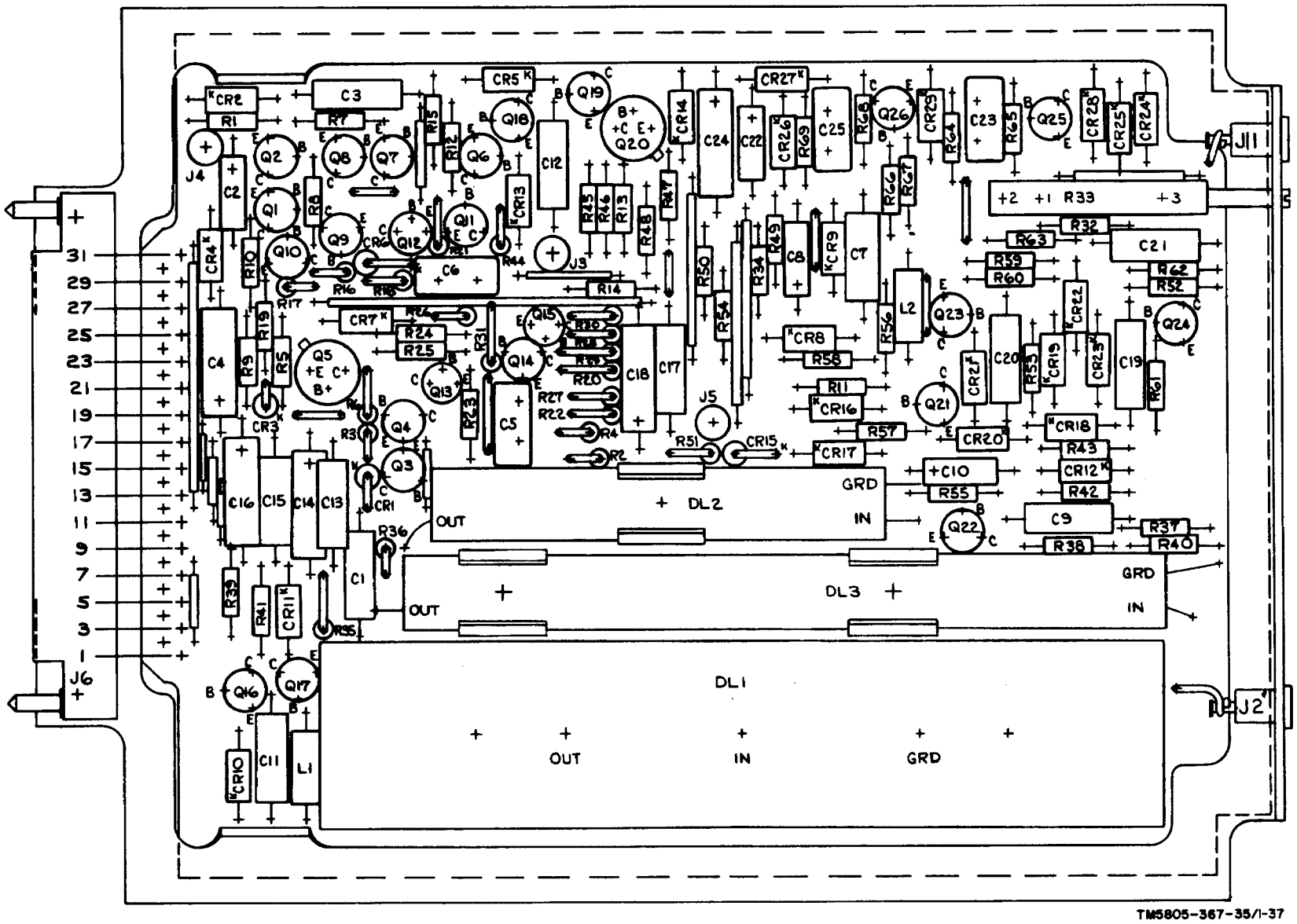


Figure 6-12. Transmitter, panel 5A2, top panel view.

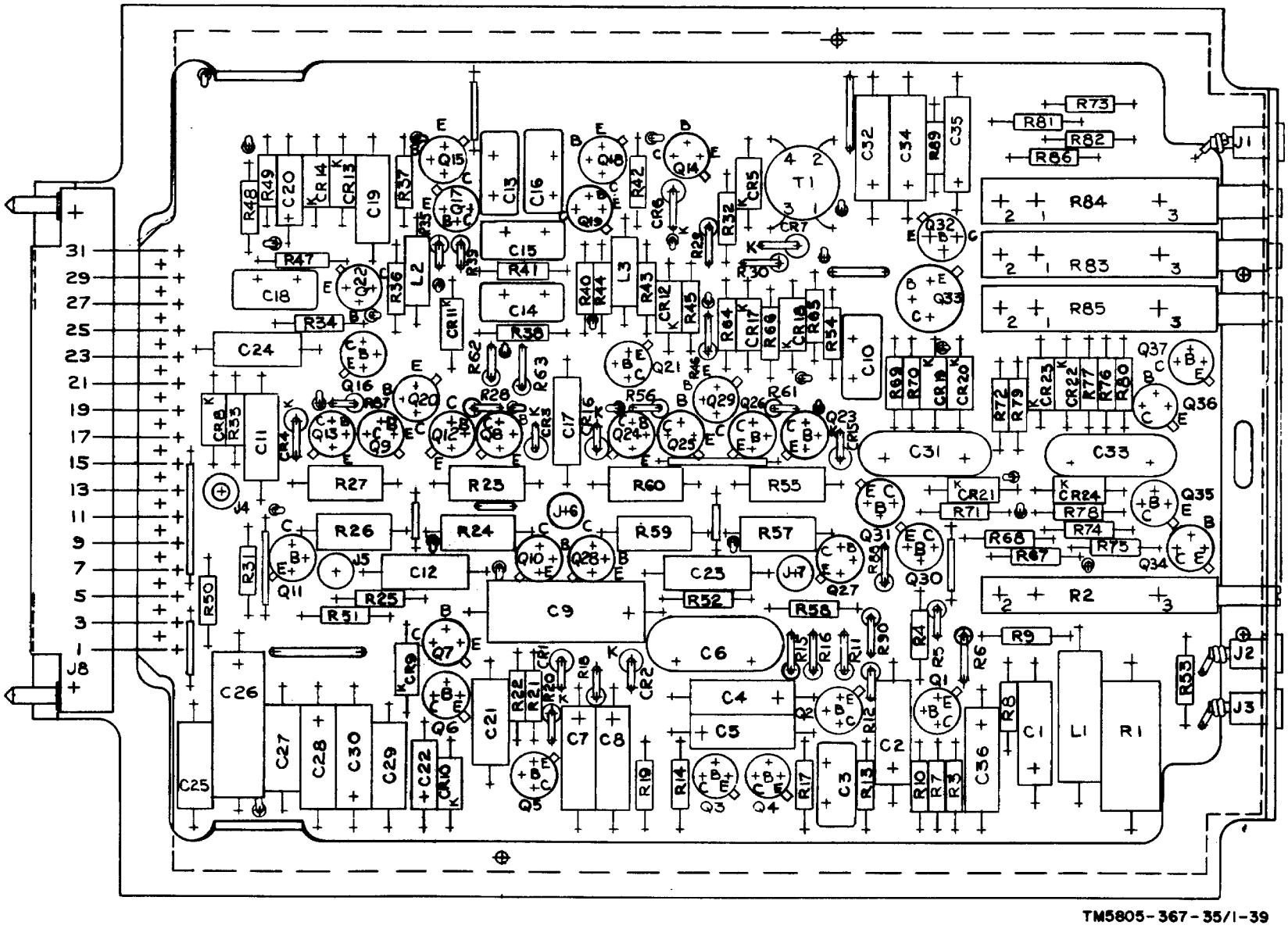


Figure 6-13. Receiver, panel 5A3, top panel view.

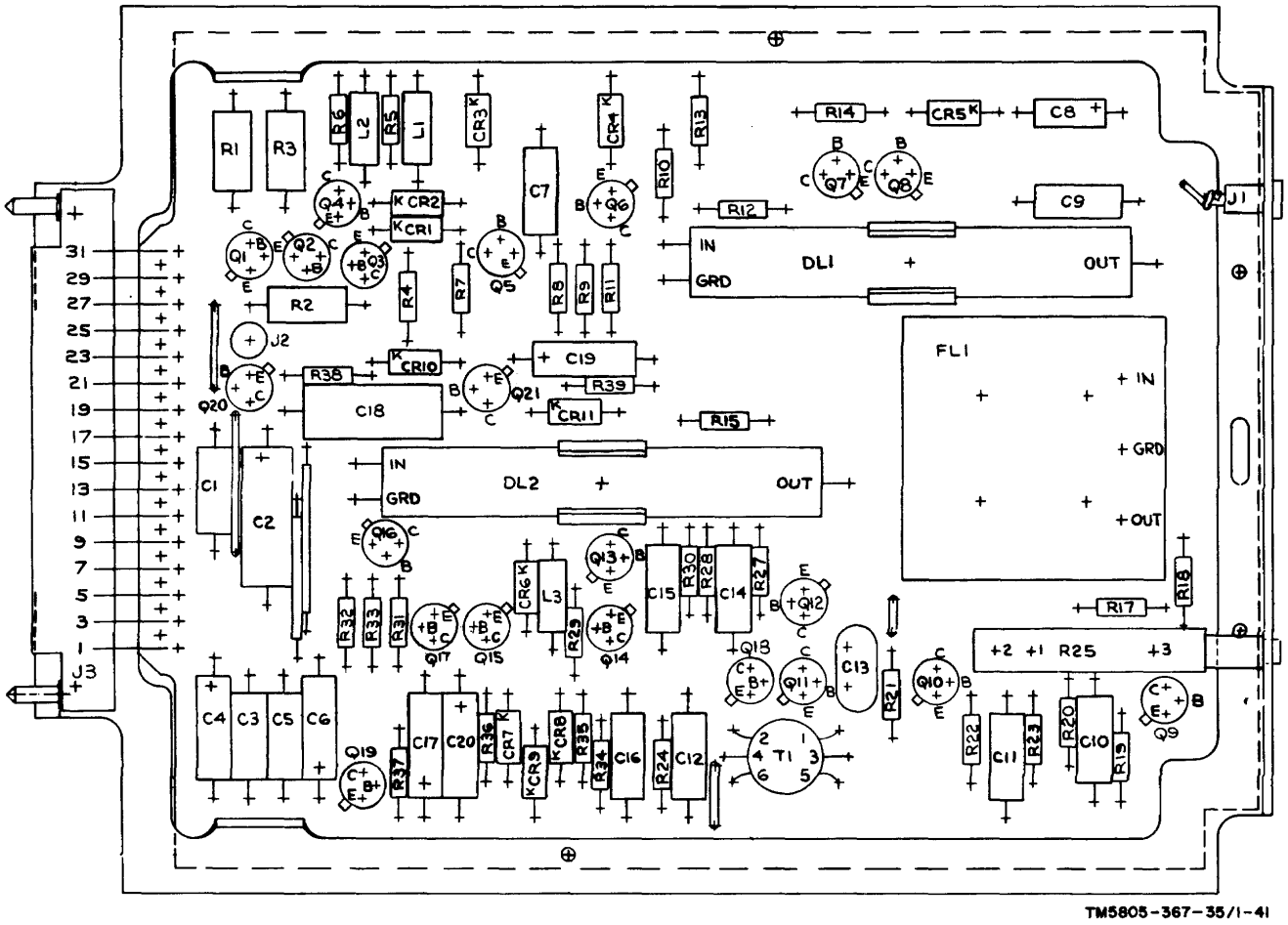


Figure 6-14. Timing generator No. 1, panel 5A4, top panel view.

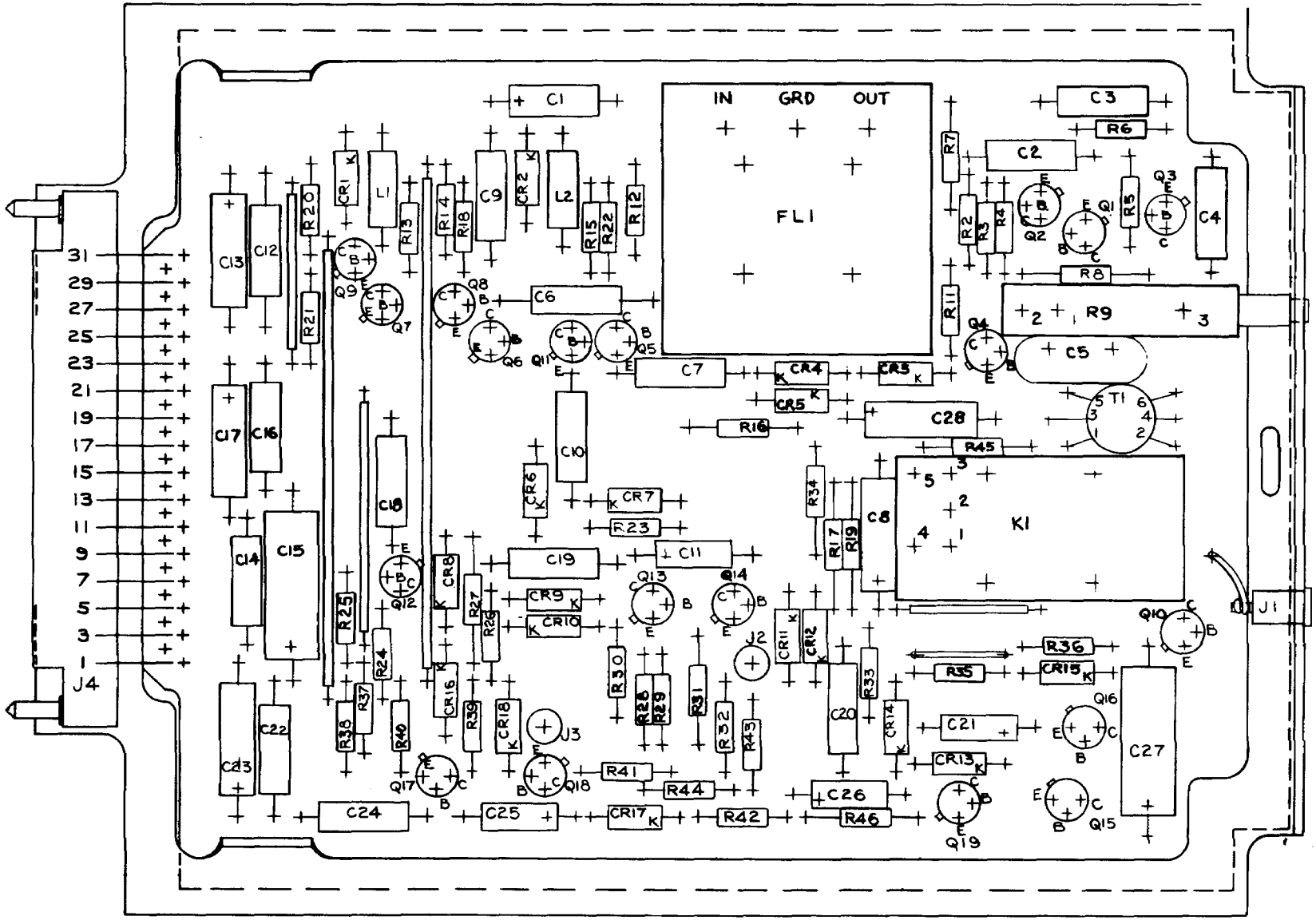


Figure 6-15. Timing generator No.2, panel 5A5, top panel view

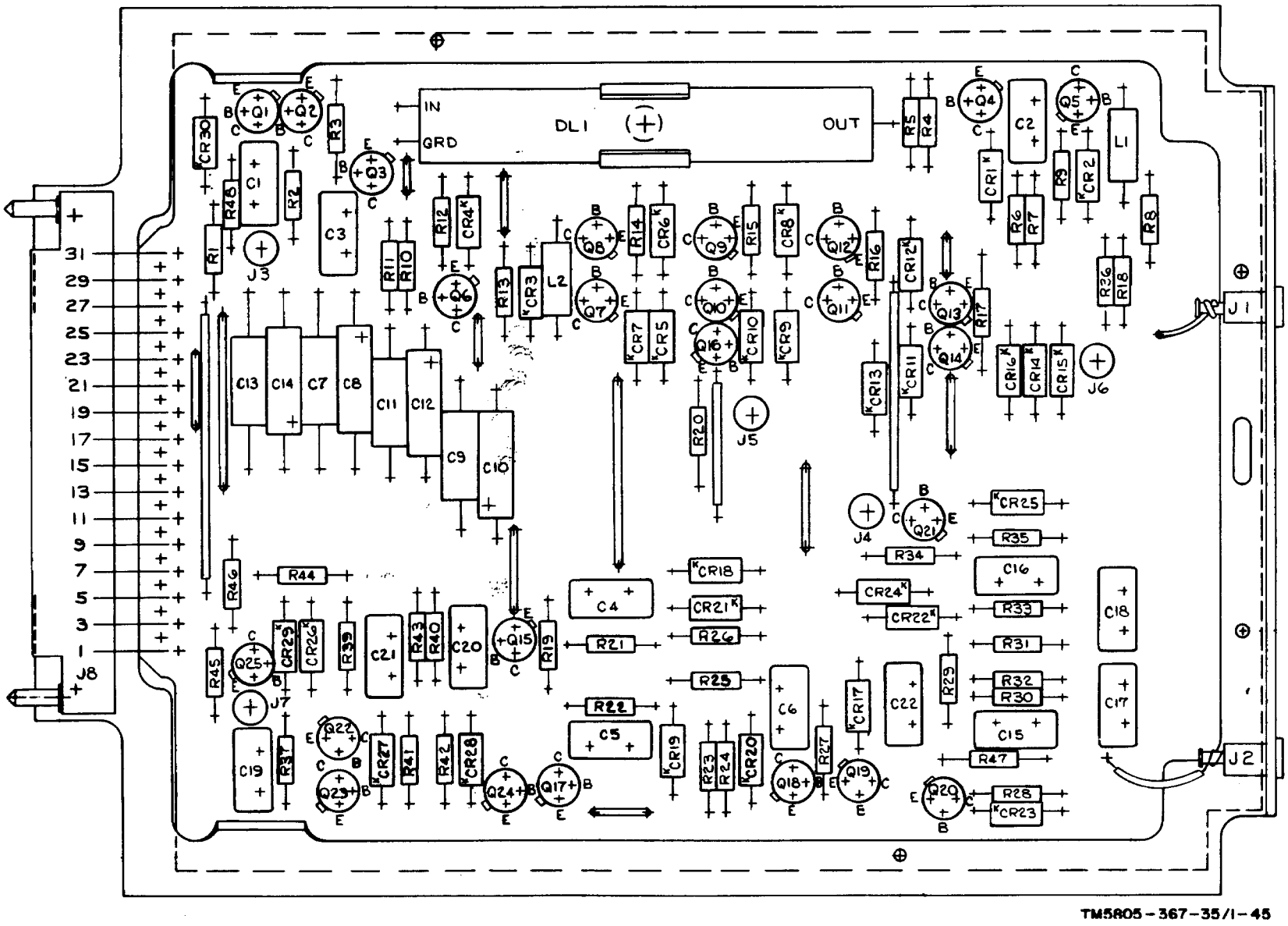


Figure 6-16. Timing generator No.4, panel 4A9, top panel view.

(6-18 blank)/ 6-17

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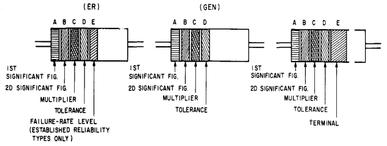


COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FO FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BA	E
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FA IRE E EL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M	
BROWN	1	BROWN	1	BROWN	10			RED	P	
RED	2	RED	2	RED	100			ORANGE	R	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE – RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1½ TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

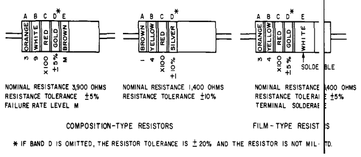
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED.)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

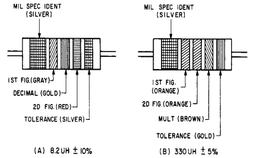
NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

NOMINAL RESISTANCE 4400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-TD.



COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED.

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.

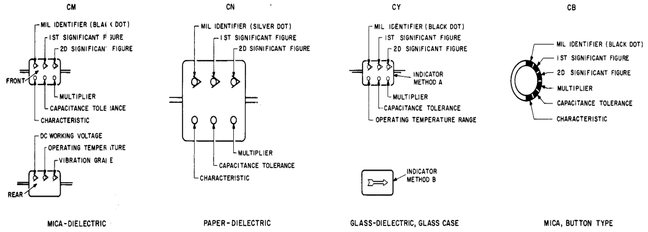


TABLE – FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER	CAPACITANCE TOLERANCE				CHARACTERISTIC			2 DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY, CB	0	0	1			±20%	±20%	A				-55°TO+70°C	10-55 Hz
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°TO+85°C	
ORANGE		3	3	1,000		±30%				O		O	300	
YELLOW		4	4	10,000					E				-55°TO+125°C	10-2,000Hz
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55°TO+150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±1%	±10%	±10%	±10%						

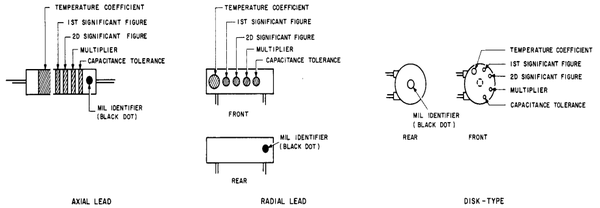


TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT*	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF.	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-250, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

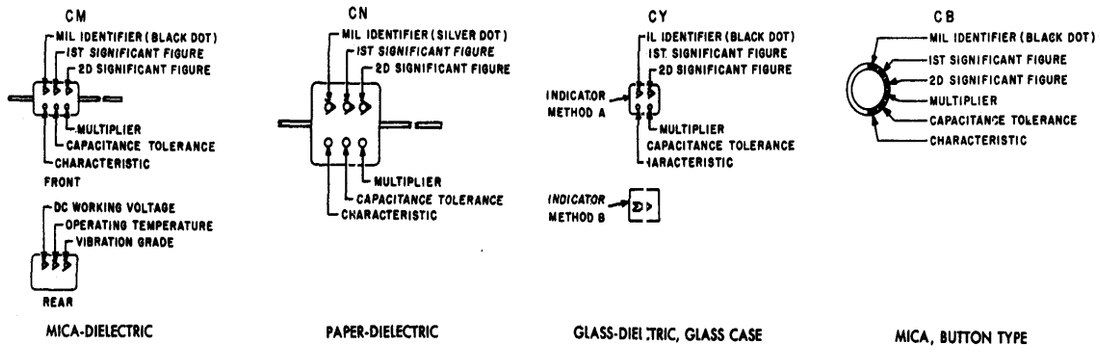
* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

ESC-FM 913-73

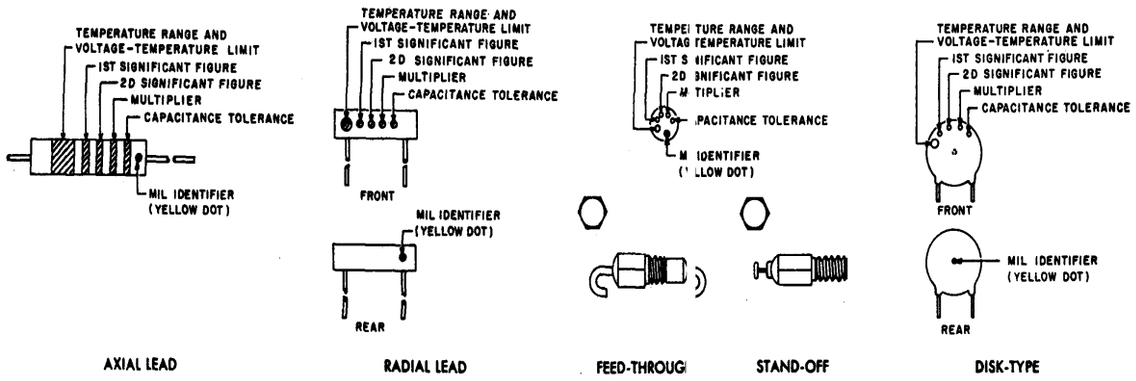
A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS. B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS. Figure 6-17. Resistor, Capacitor color coding. C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

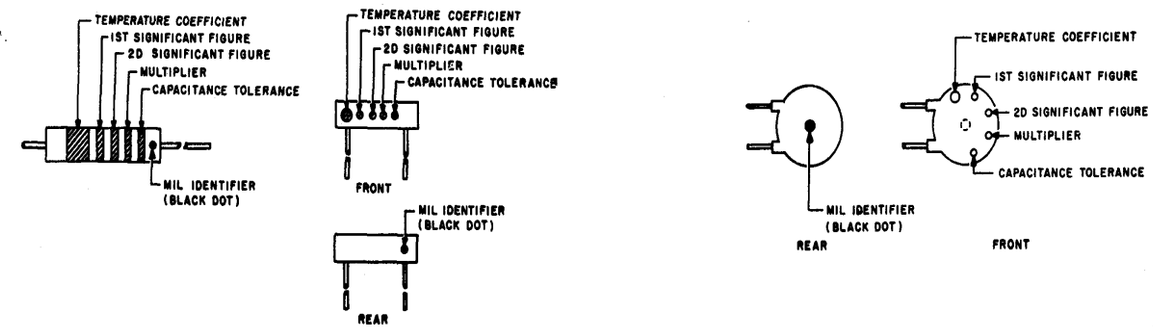
GROUP I Capacitors, Fixed, Various-Dielectrics, Styles CM, CN, CY, and CB



GROUP II Capacitors, Fixed Ceramic-Dielectric (General Purpose) Style CK



GROUP III Capacitors, Fixed, Ceramic-Dieletric (Temperature Compensating) Style CC



COLOR CODE TABLES

TABLE I – For use with Group I, Styles CM, CII, CY and CB

COLOR	MIL ID	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]				DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CY	CB	CM	CM	CM
BLACK	CM; CY CB	0	0	1			± 20%	± 20%		A				−55° to +70°C	10–55 cps
BROWN		1	1	10					B	E		B			
RED		2	2	100	± 2%		± 2%	± 2%	C		C			−55° to +85°C	
ORANGE		3	3	1,000		± 30%			D			D	300		
YELLOW		4	4	10,000					E					−55° to +125°C	10–2,000 cps
GREEN		5	5		± 5%				F				500		
BLUE		6	6											−55° to +150°C	
PURPLE (VIOLET)		7	7												
GREY[4]		8	8												
WHITE		9	9												
GOLD				0.1			± 5%	± 5%							
SILVER	CN				± 10%	± 10%	± 10%	± 10%							

TABLE II – For use with Group II, General Purpose, Style CK

COLOR	TEMP. RANGE AND VOLTAGE – TEMP. LIMITS[3]	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE	MIL ID
BLACK		0	0		± 20%	
BROWN	AW	1	1	1	± 10%	
RED	AX	2	2	10		
ORANGE	BX	3	3	1,00		
YELLOW	AV	4	4	10,00		CK
GREEN	CZ	5	5			
BLUE	BV	6	6			
PURPLE (VIOLET)		7	7			
GREY		8	8			
WHITE		9	9			
GOLD						
SILVER						

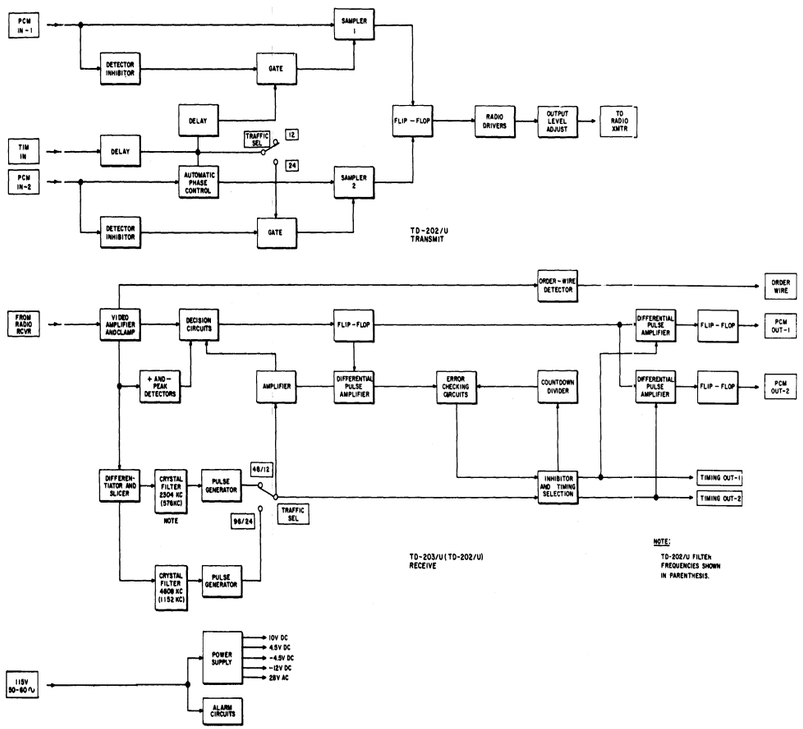
TABLE III – For use with Group III, Temperature Compensating, Style CC

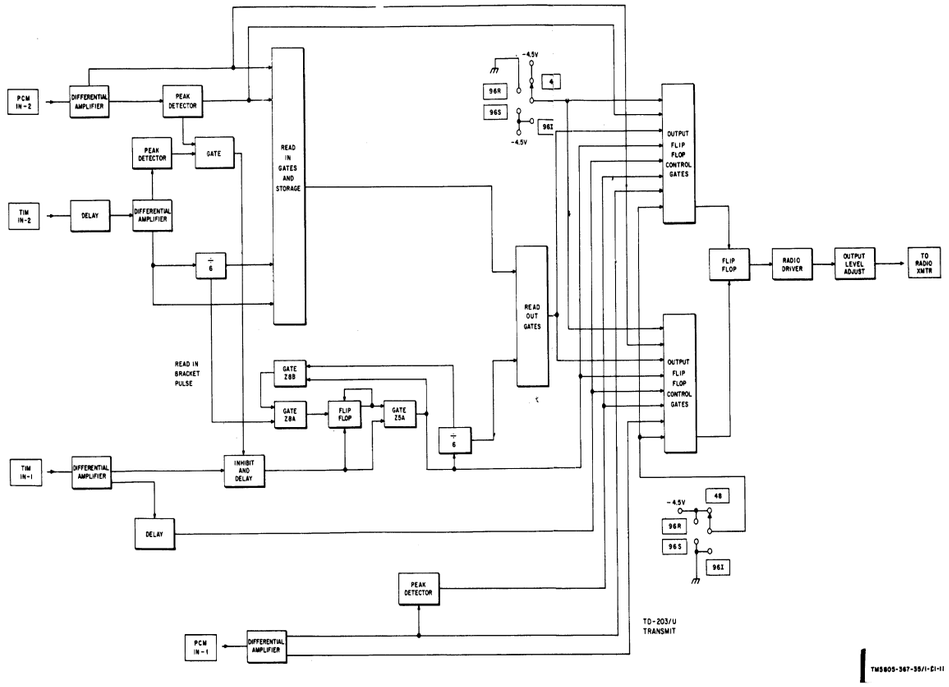
COLOR	TEMPERATURE COEFFICIENT[4]	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					Capacitances over 10uuf	Capacitances 10uuf or less	
BLACK	0	0	0	1		± 2.0uuf	CC
BROWN	−30	1	1	10	± 1%		
RED	−80	2	2	100	± 2%	± 0.25uuf	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		± 5%	± 0.5uuf	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	± 10%		
GOLD	+100					± 1.0uuf	
SILVER							

1. The multiplier is the number by which the two significant (SIG) figures are multiplied to obtain the capacitance in uuf.
2. Letters indicate the Characteristics designated in applicable specifications: MIL–C–5, MIL–C–91, MIL–C–11272, and MIL–C–10950 respectively.
3. Letters indicate the temperature range and voltage-temperature limits designated in MIL–C–11015.
4. Temperature coefficient in parts per million per degree centigrade.

STD–C2

Figure 6-18. Color code marking, MIL STD capacitors.





TM5805-367-35/1-01-11

Figure 6-19. TD-808/U (TD-802/U), block diagram.

Figure 6-19. TD-203/U (TD-202/U), block diagram

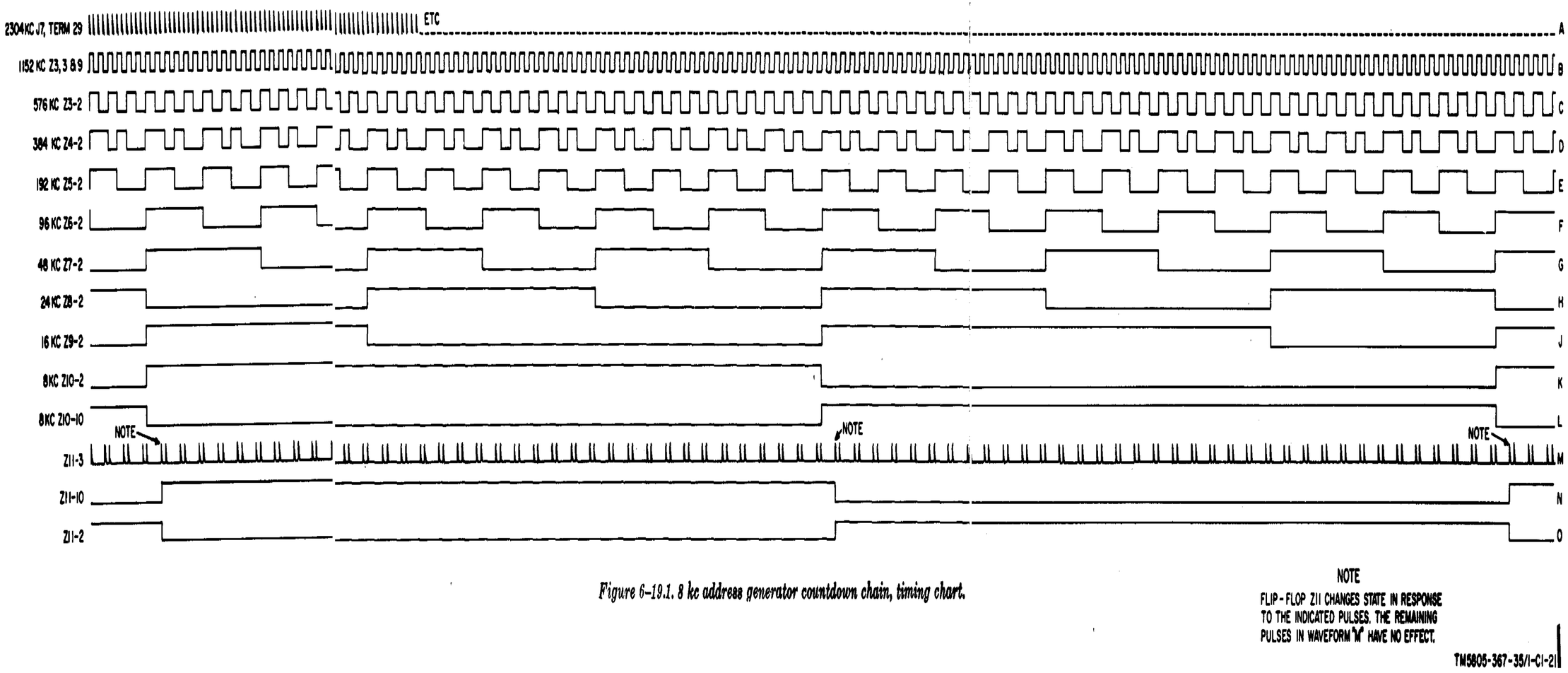
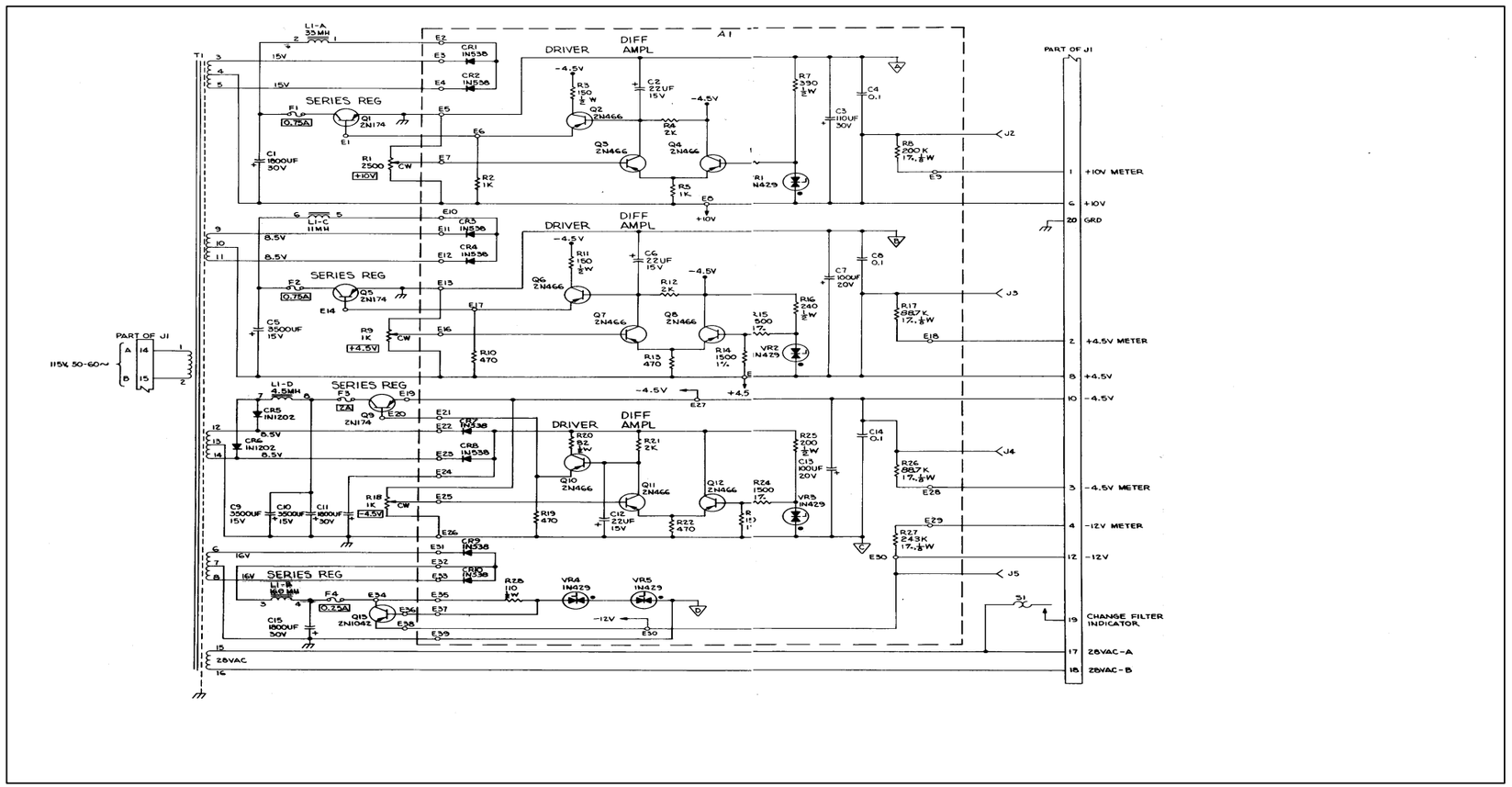


Figure 6-19.1. 8 kc address generator countdown chain, timing chart.

Figure 6-19.1. 8kc address generator countdown chain, timing chart.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ☐ INDICATES EQUIPMENT MARKING

Figure 6-20. Power supply, panel 4A1/5A1, schematic diagram.

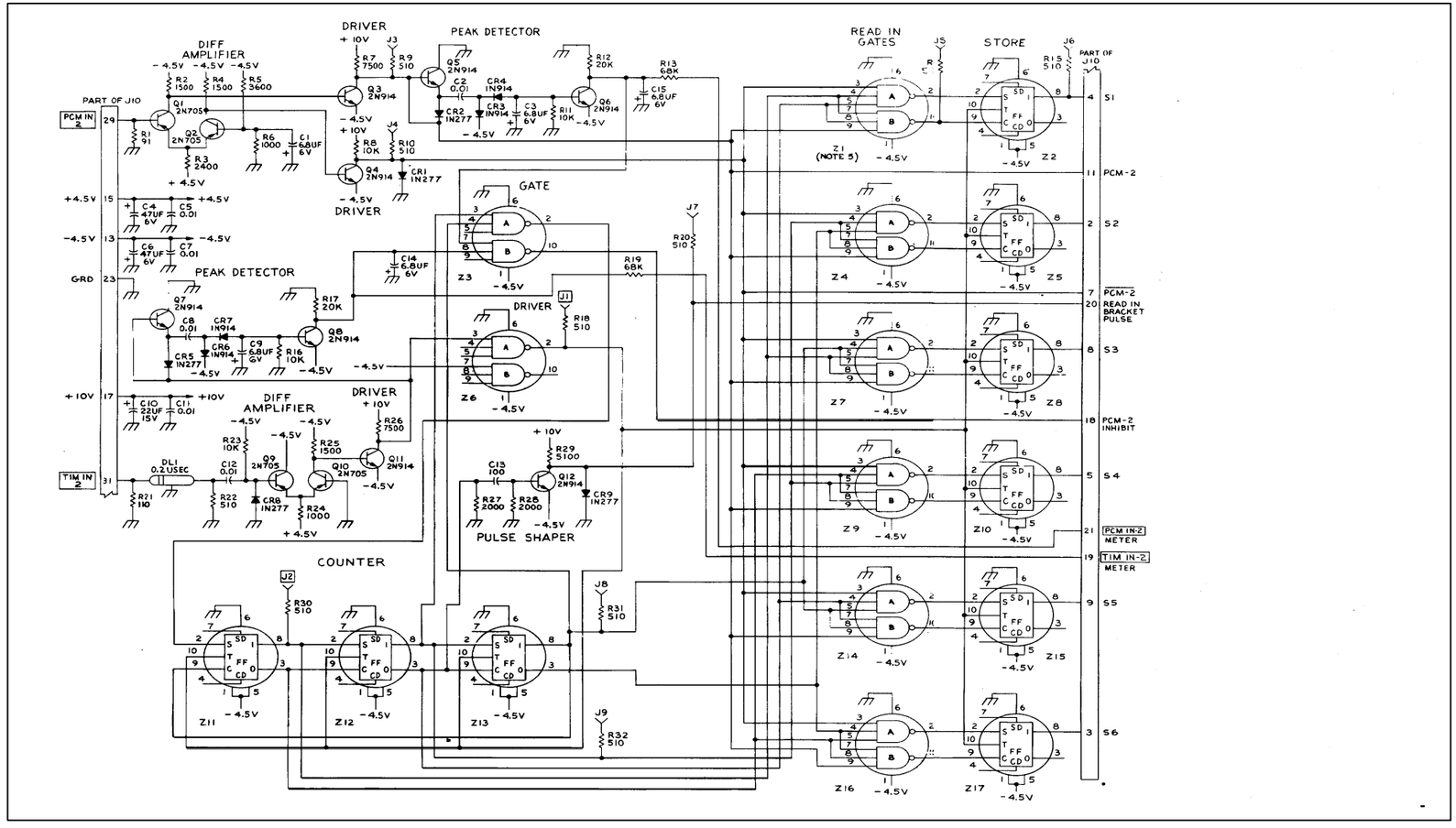


Figure 6-20.1. Transmit No. 1, panel 4A10, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE .25 WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ▭ INDICATES EQUIPMENT MARKING

5. Z1, Z3, Z4, Z7, Z9, Z14, Z16 SEE SM B-529556 (SE 113K). Z2, Z5, Z8, Z10, Z11, Z12, Z13, Z15, Z17, SEE SM B-523980 (SE 124K), Z6, SEE SM B-529557 (SE 157K)

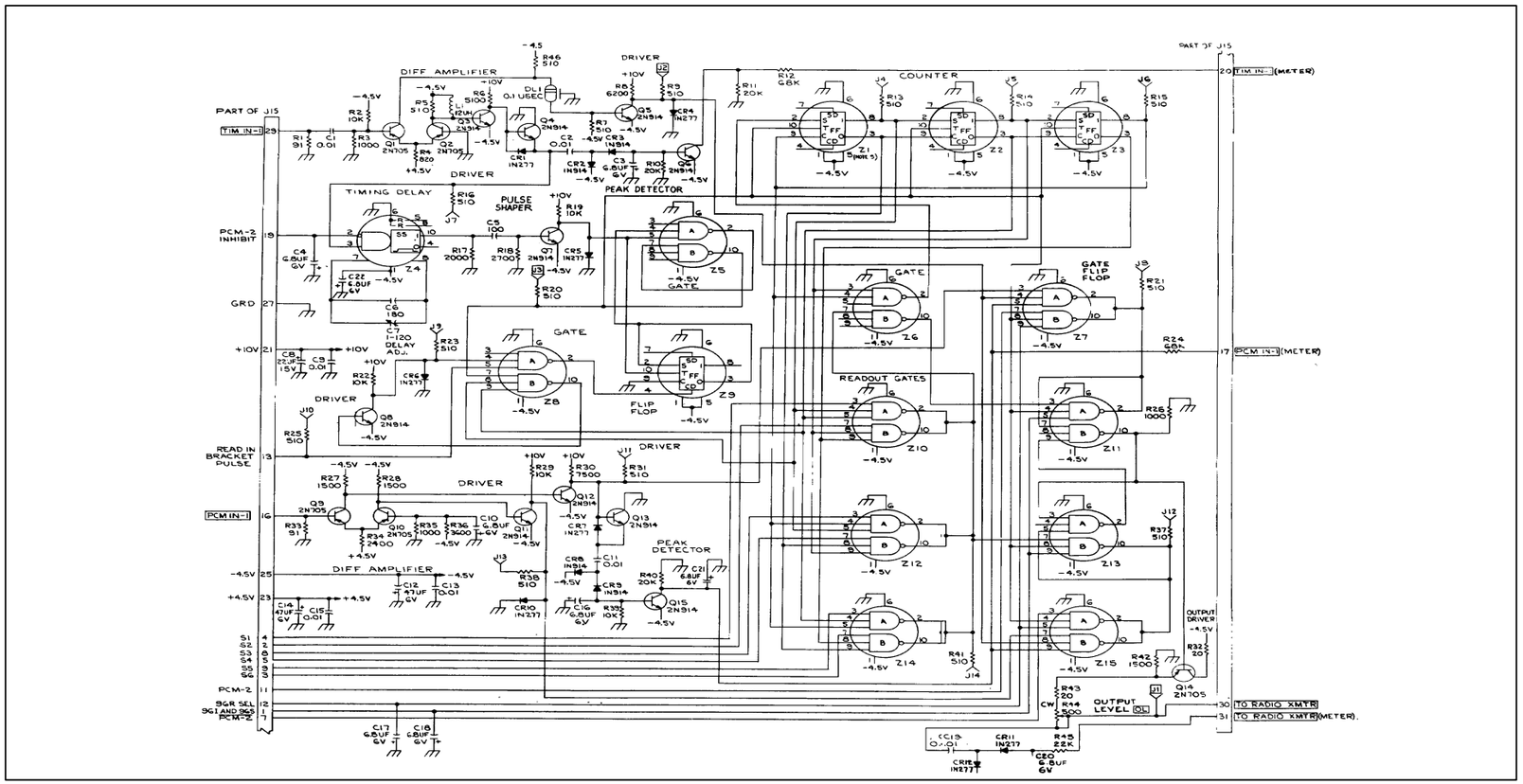


Figure 6-21. Transmit No. 2, panel 4A2, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE .25 WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ☐ INDICATES EQUIPMENT MARKING

5. Z1, Z2, Z3, Z9, SEE SM B-523980 (SE 124K). Z4, SEE SM B-524012 (SE 161K), Z5, SEE SM B-529557 (SE 157K). Z6, Z7, Z8, Z10 THRU Z15, SEE SM B-529556 (SE 113K)

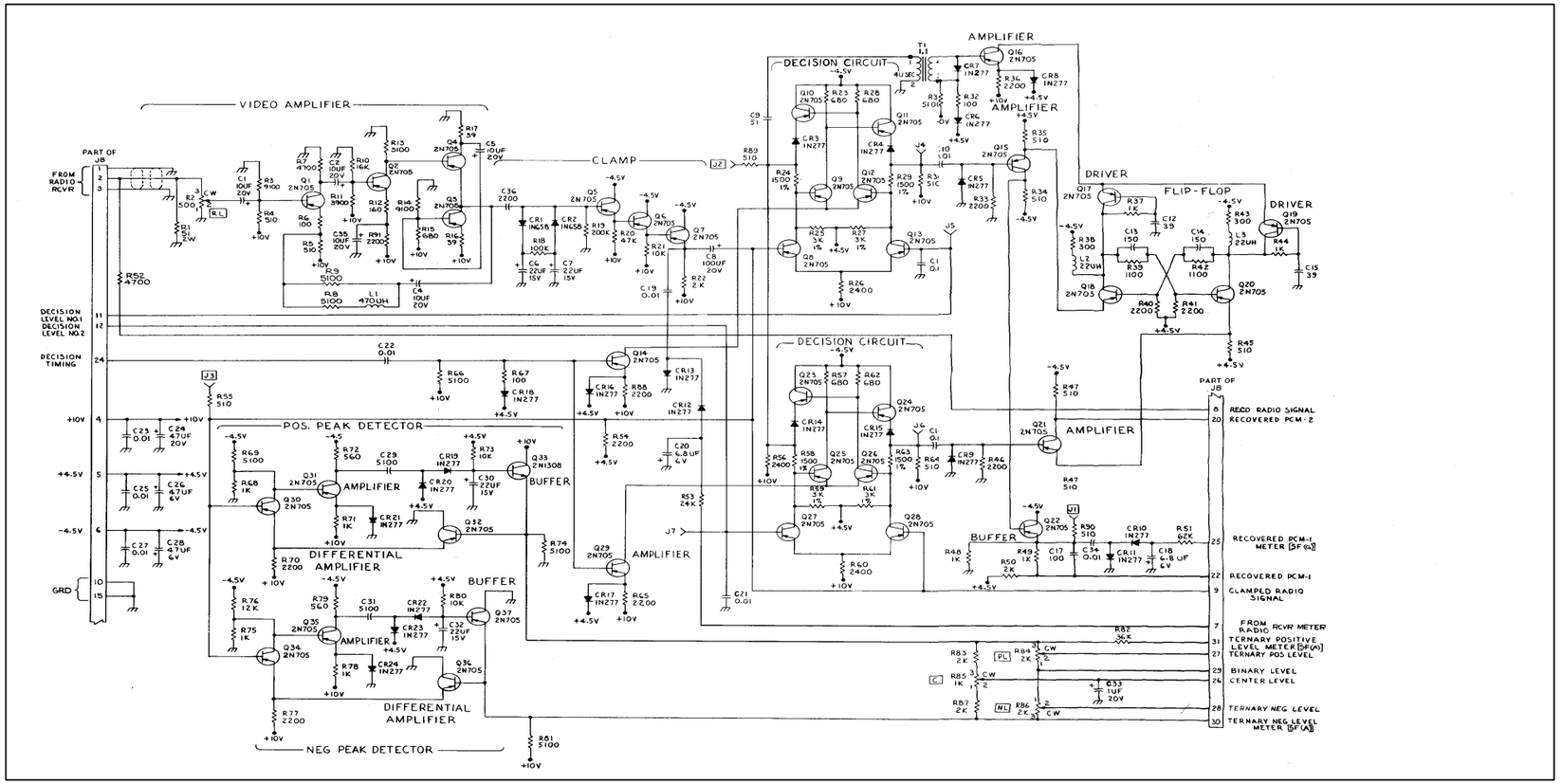


Figure 6-22. Receiver, panel 4A3, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE .25 WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ▭ INDICATES EQUIPMENT MARKING

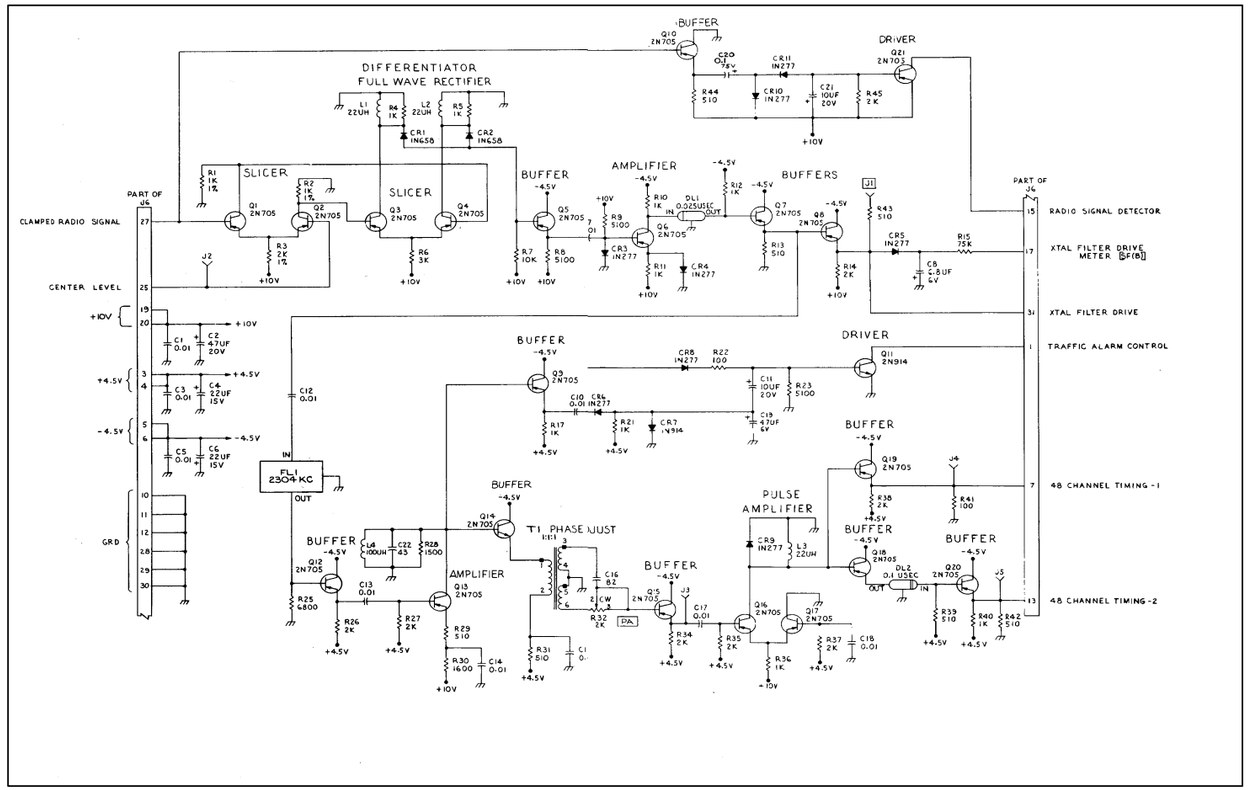


Figure 6-23. Timing generator No. 1, panel 4A4, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ▭ INDICATES EQUIPMENT MARKING

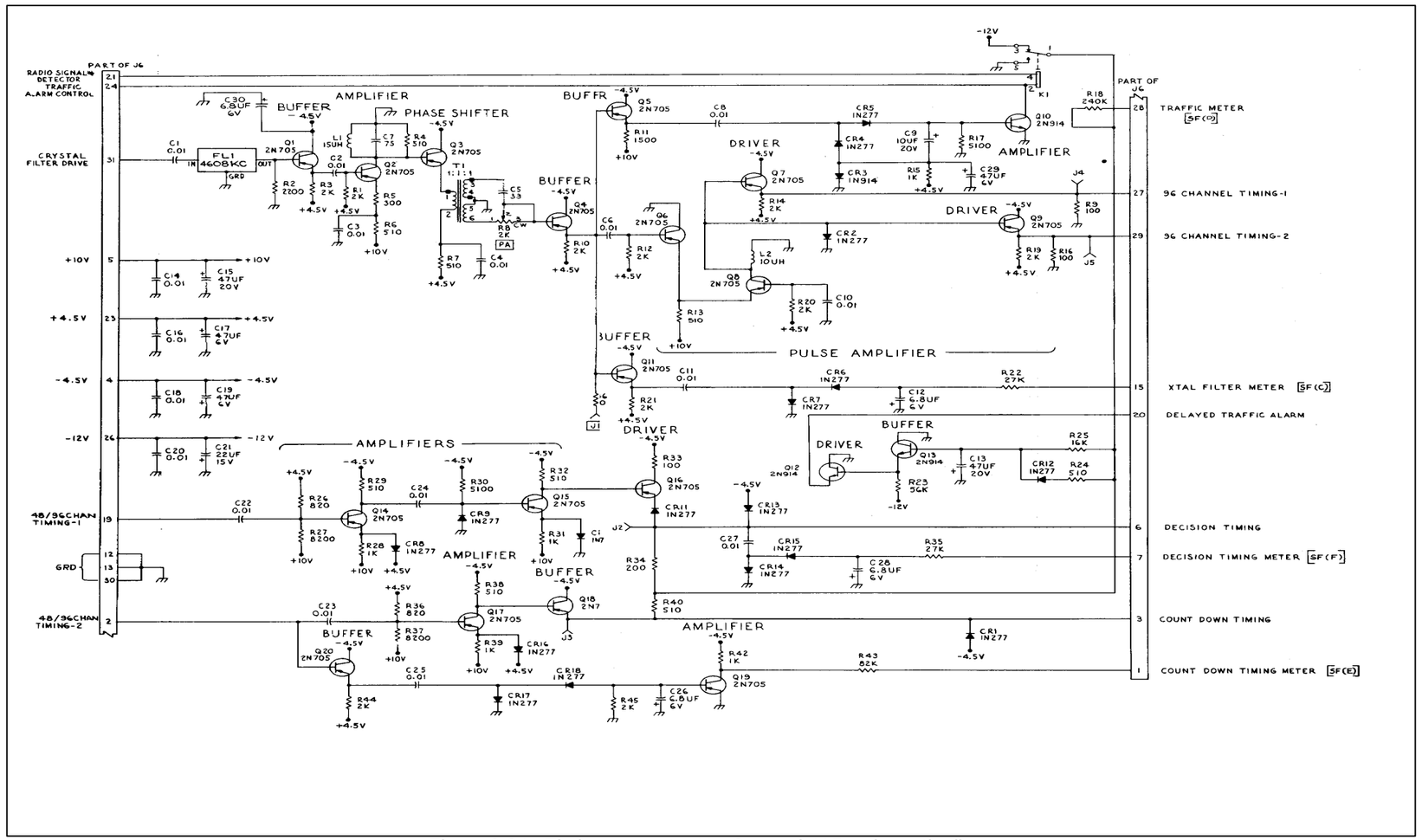


Figure 6-24. Timing generator No. 2, panel 4A5, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS
4. ☐ INDICATES EQUIPMENT MARKING

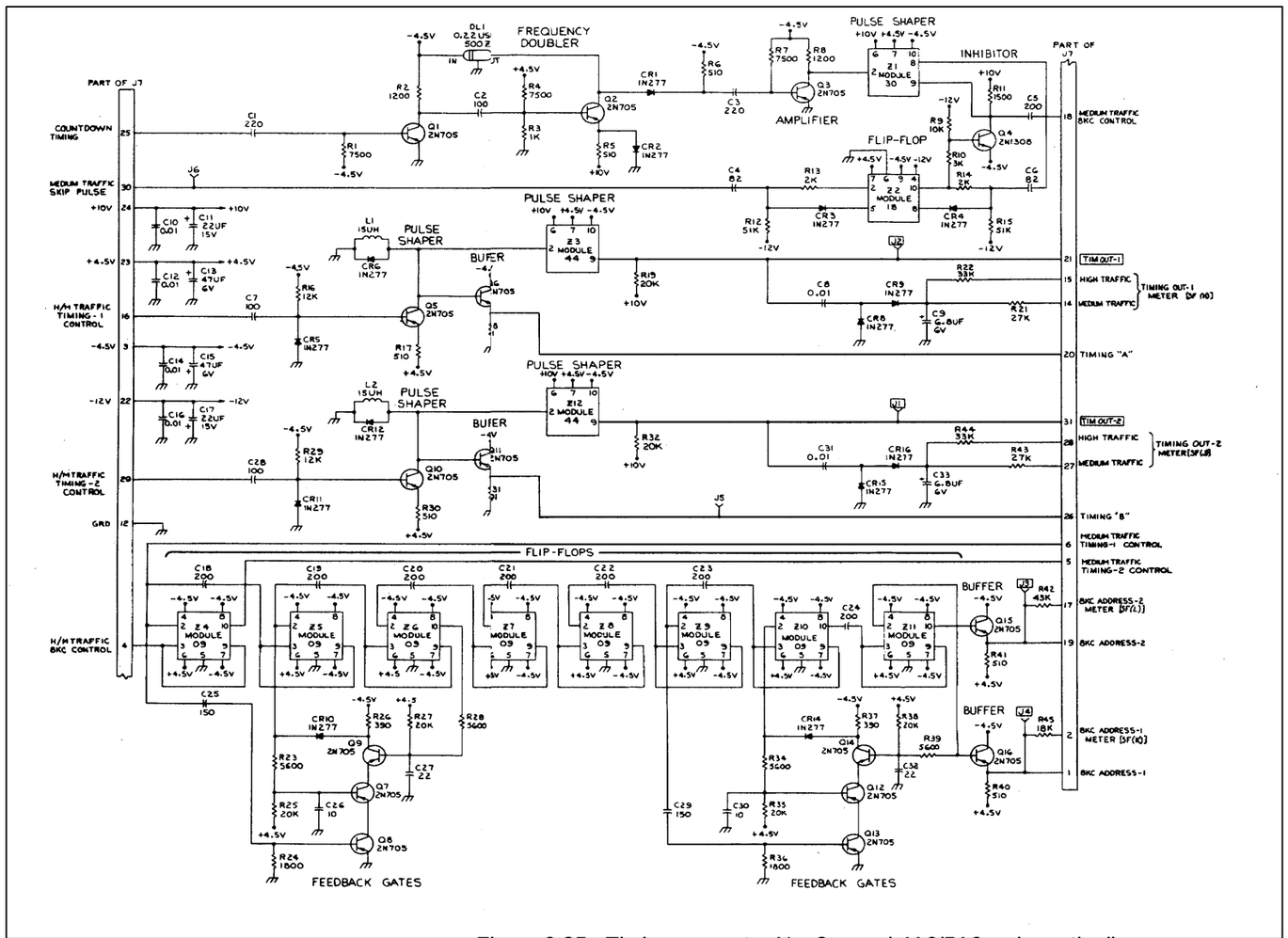


Figure 6-25. Timing generator No. 3, panel 4A6/5A6, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ☐ INDICATES EQUIPMENT MARKING

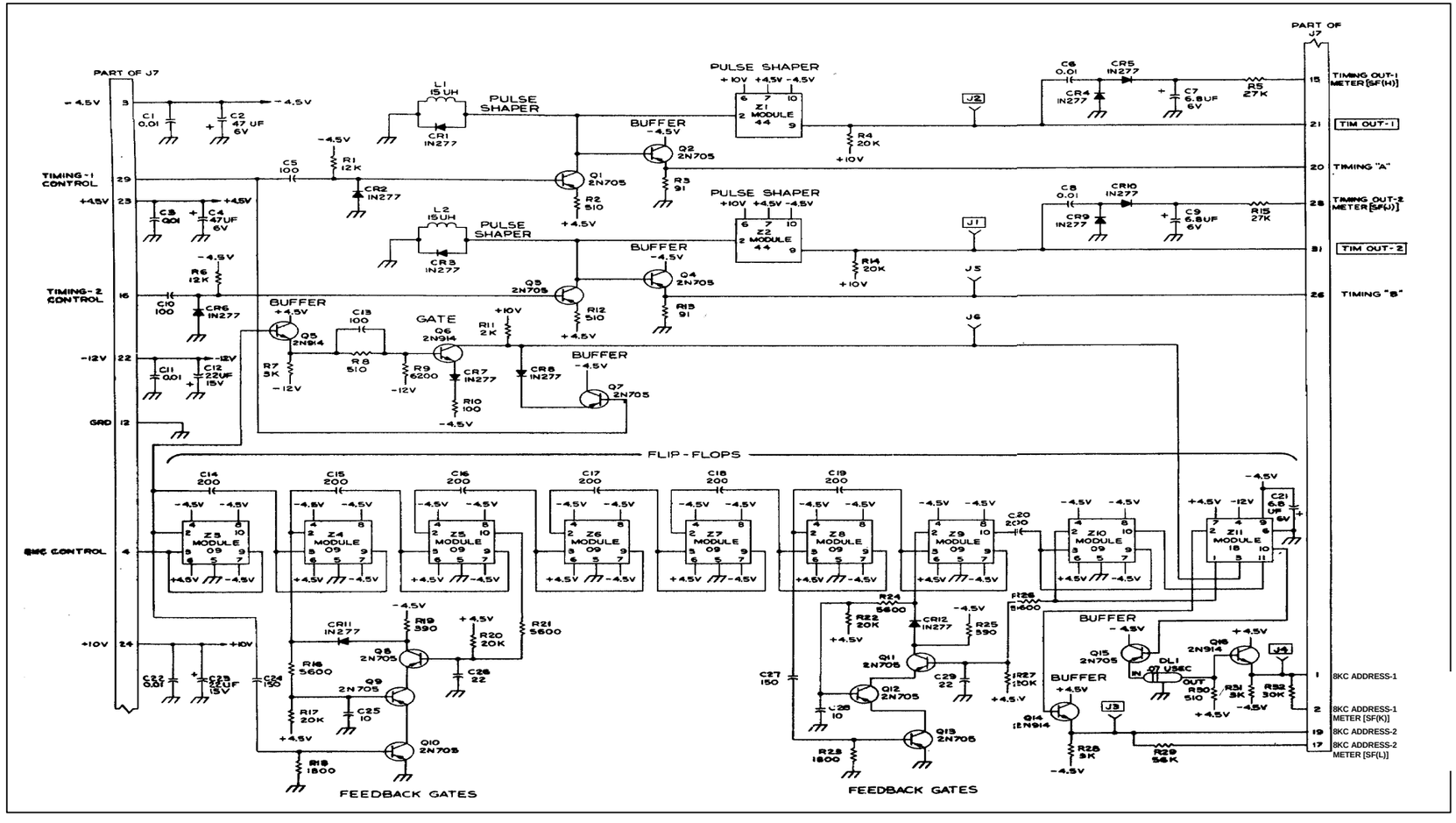


Figure 6-25.1. Timing generator No. 3, panel 4A11, schematic diagram.

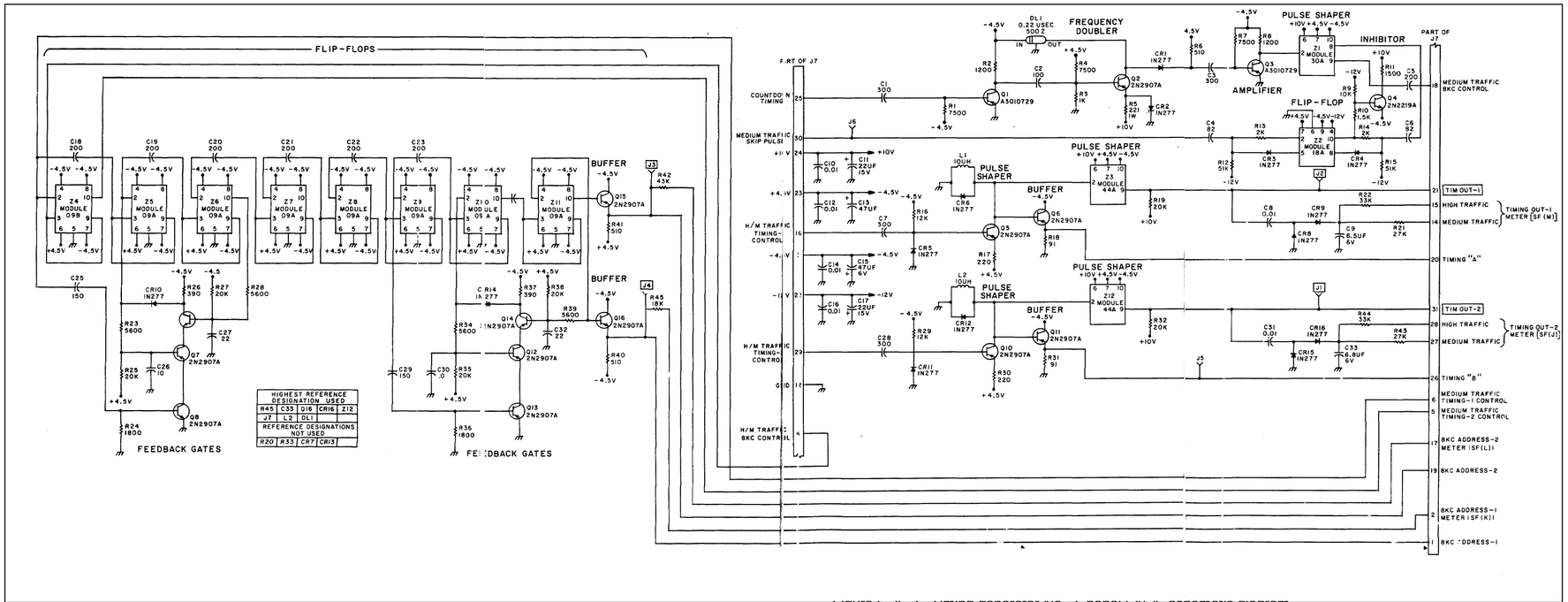
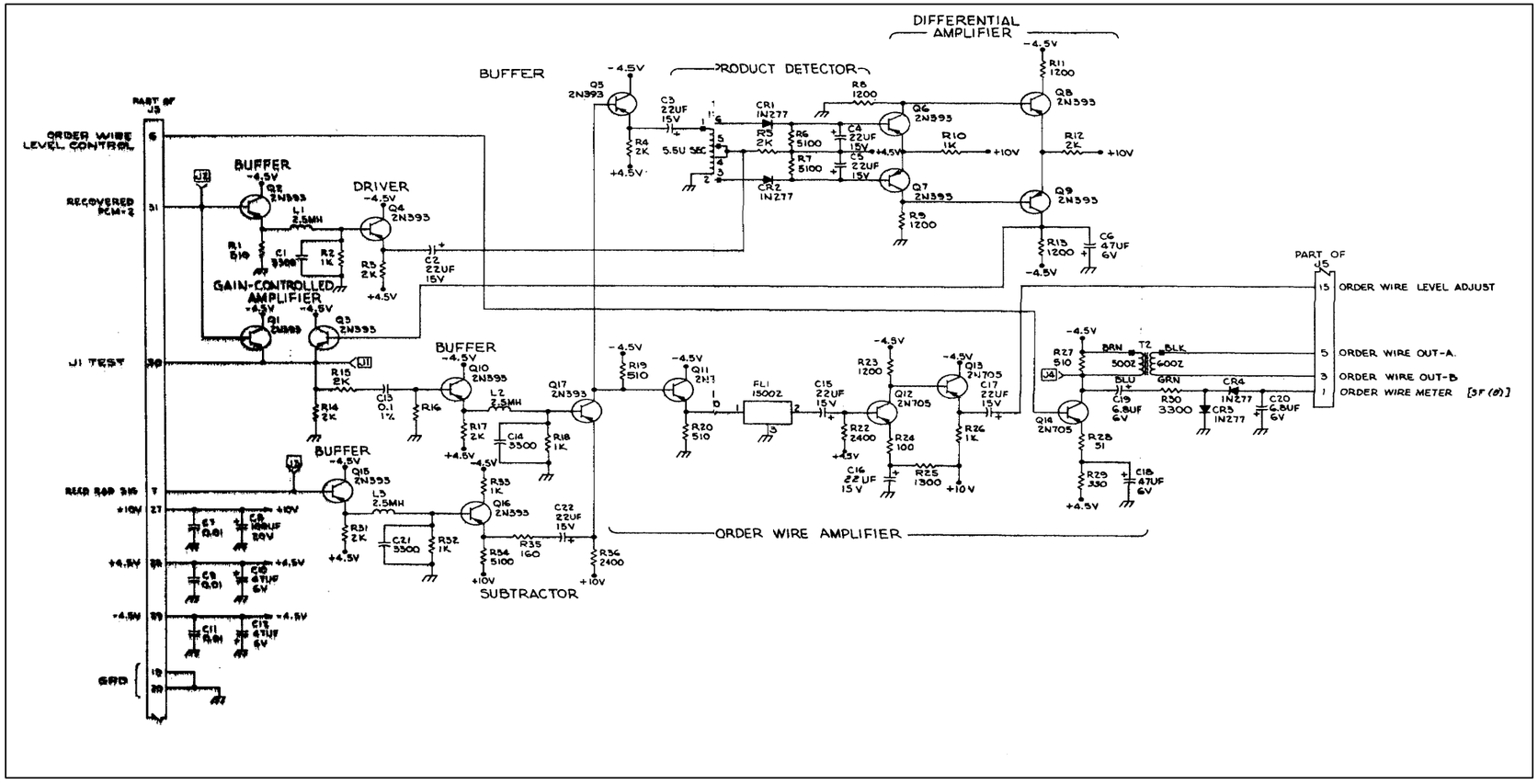


Figure 6-25-2. Timing generator No. 3, panel 5A6A, schematic diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS
4. ▭ INDICATES EQUIPMENT MARKING

CEOBR002



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ▭ INDICATES EQUIPMENT MARKING

Figure 6-26. Order wire, panel 4A7/5A7, schematic diagram.

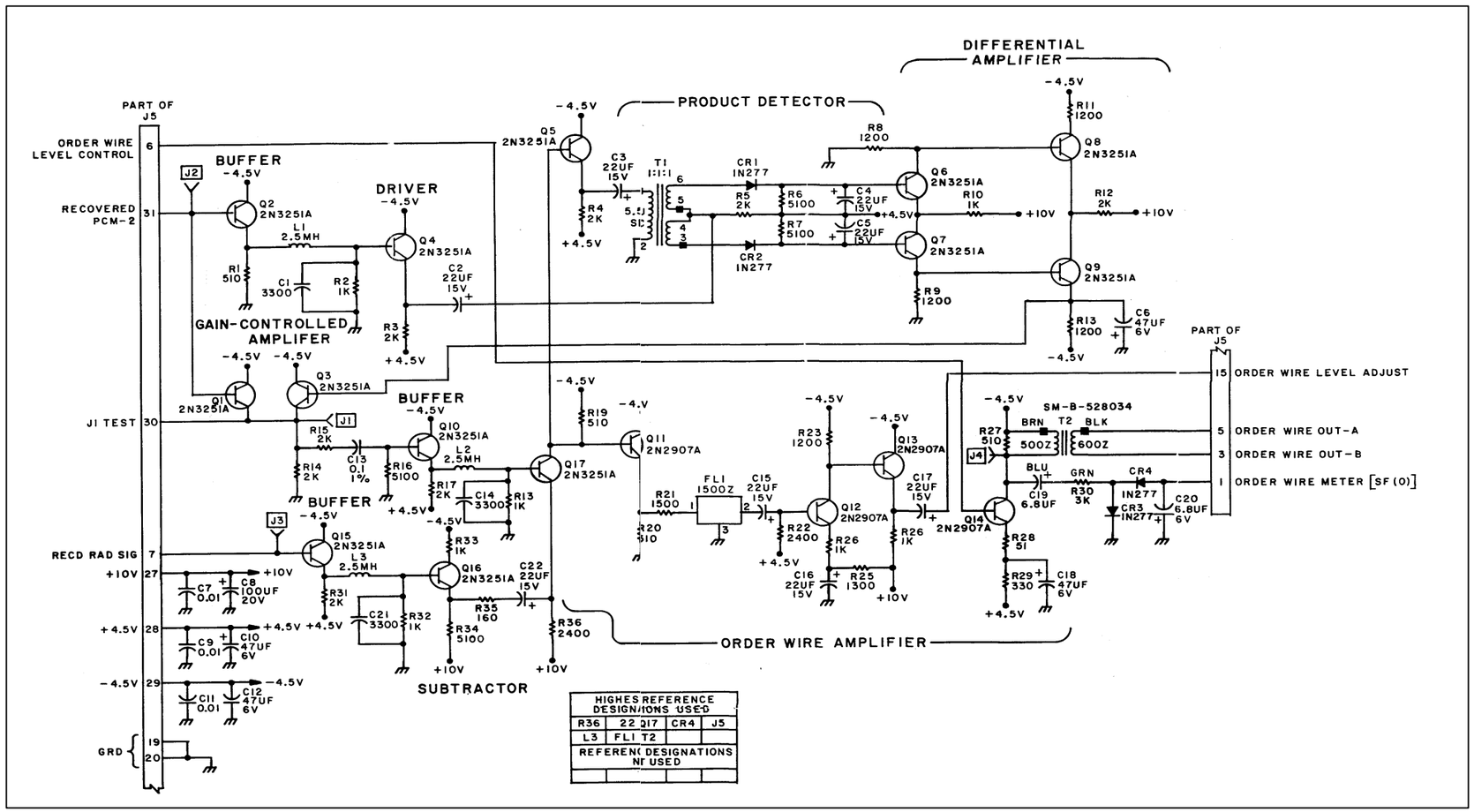


Figure 6-26-1. Order wire, panel 4A7A/5A7A, schematic diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN PICOFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS
4. ▭ INDICATES EQUIPMENT MARKING

CEOBR003

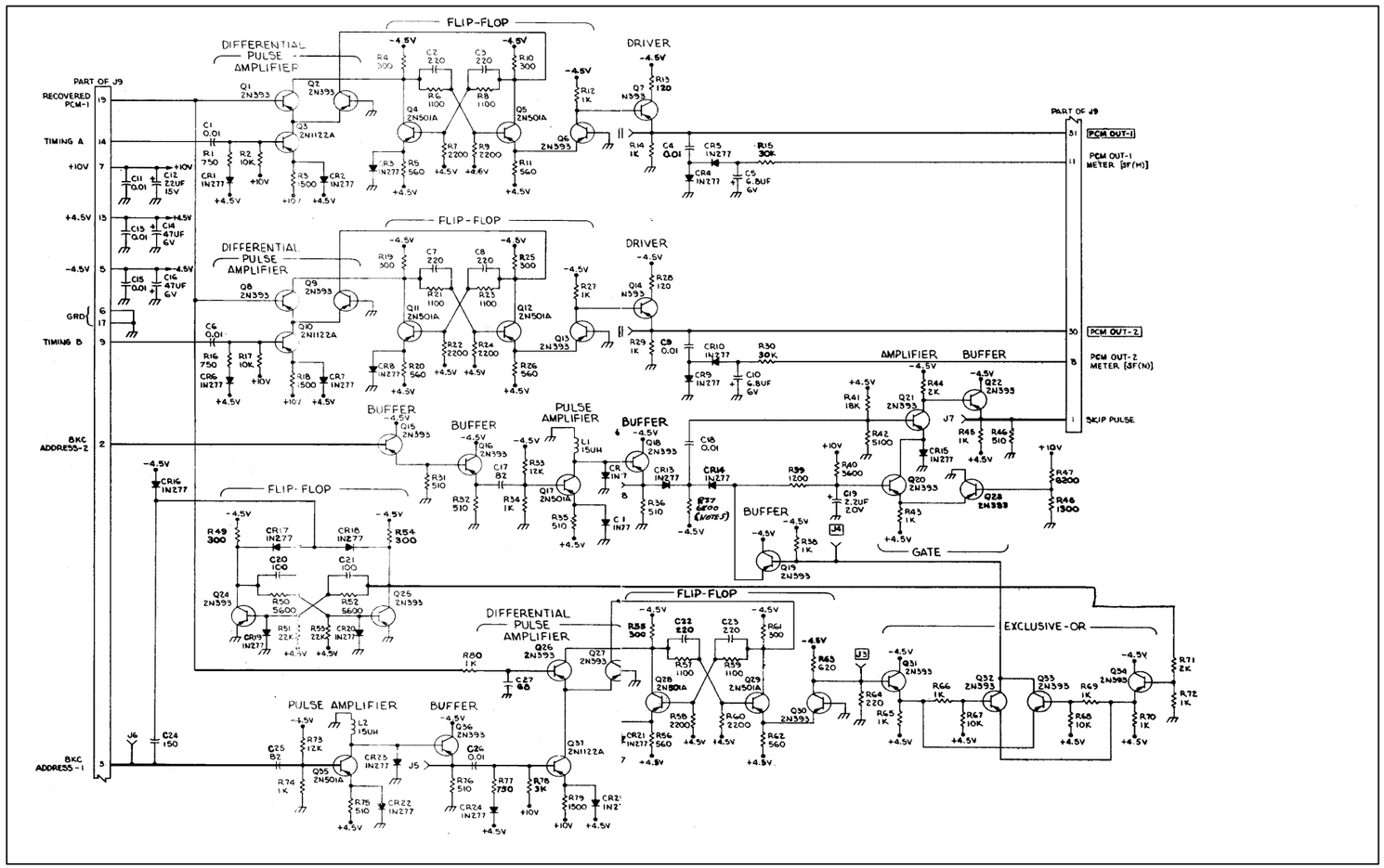


Figure 6-27. Output and framing, panel 4A8/5A8, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ☐ INDICATES EQUIPMENT MARKING

5. EARLY SERIAL NUMBER BOARDS MAY HAVE R37 4700 OHMS. IF R37 IS REPLACED, USE 6800 OHMS

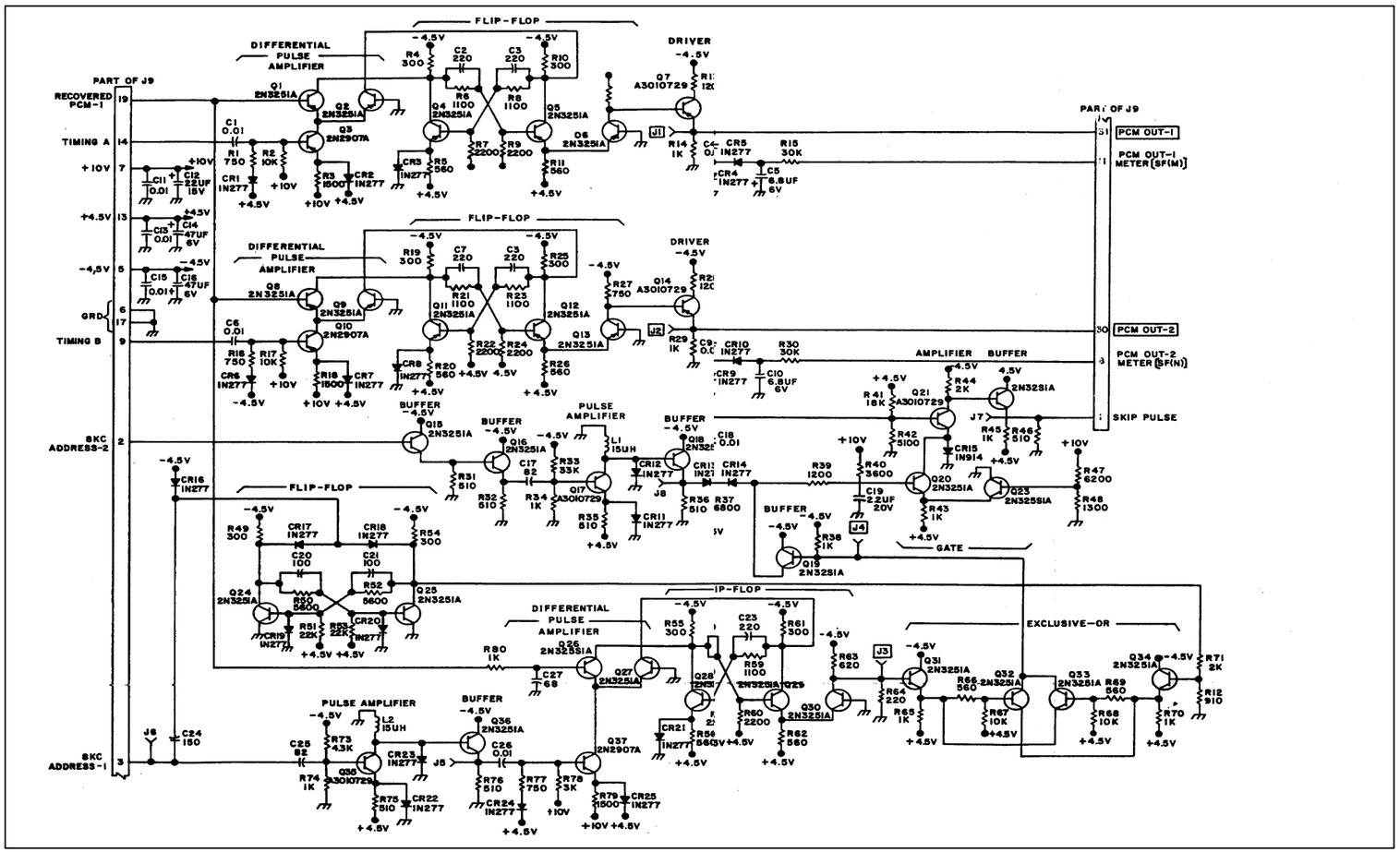


Figure 6-27-1. Output and Framing, panel 4A8A/5A8A, schematic diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN PICOFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS
4. ☐ INDICATES EQUIPMENT MARKING

CEOBR004

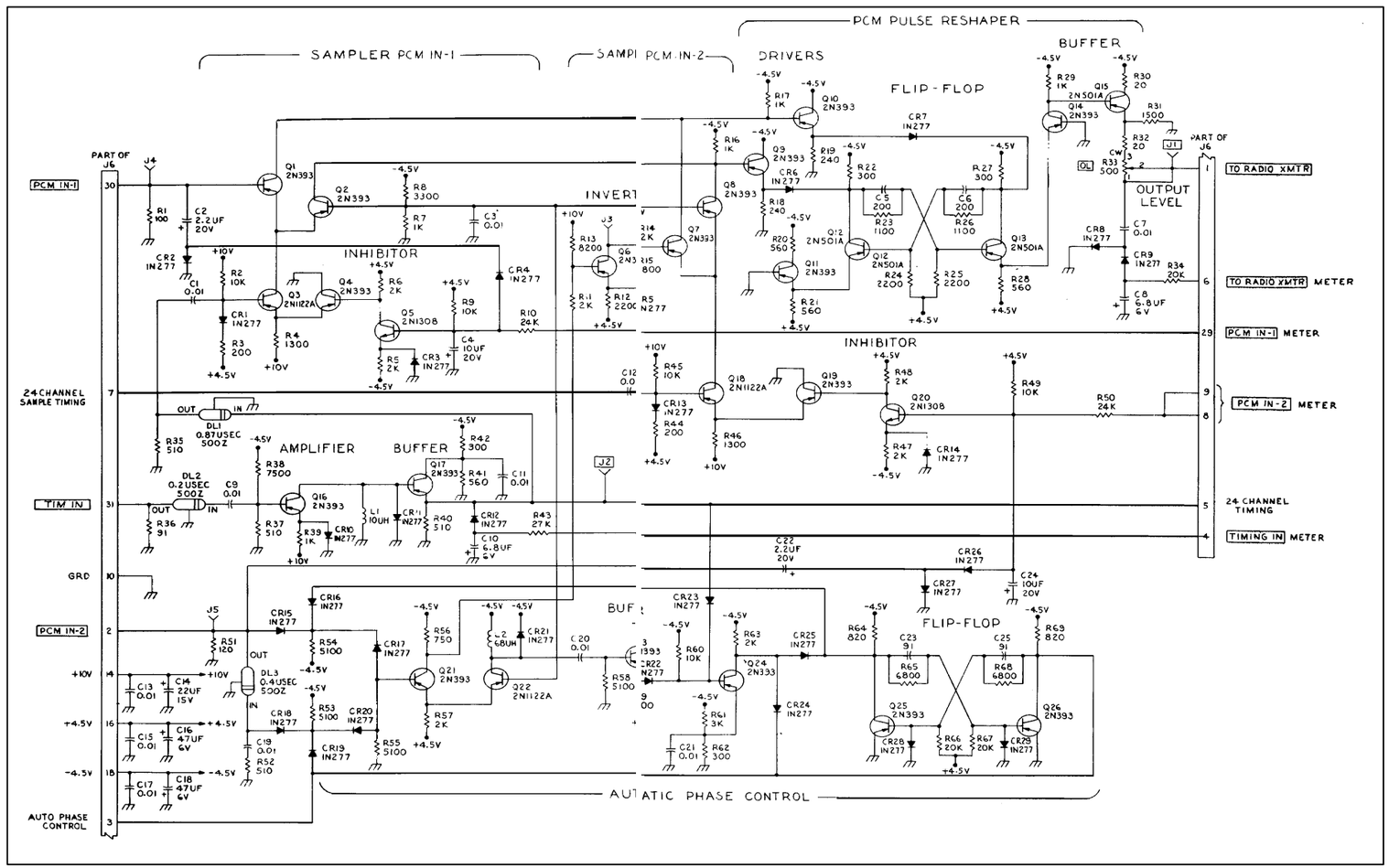


Figure 6-28. Transmitter, panel 5A2, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ☐ INDICATES EQUIPMENT MARKING

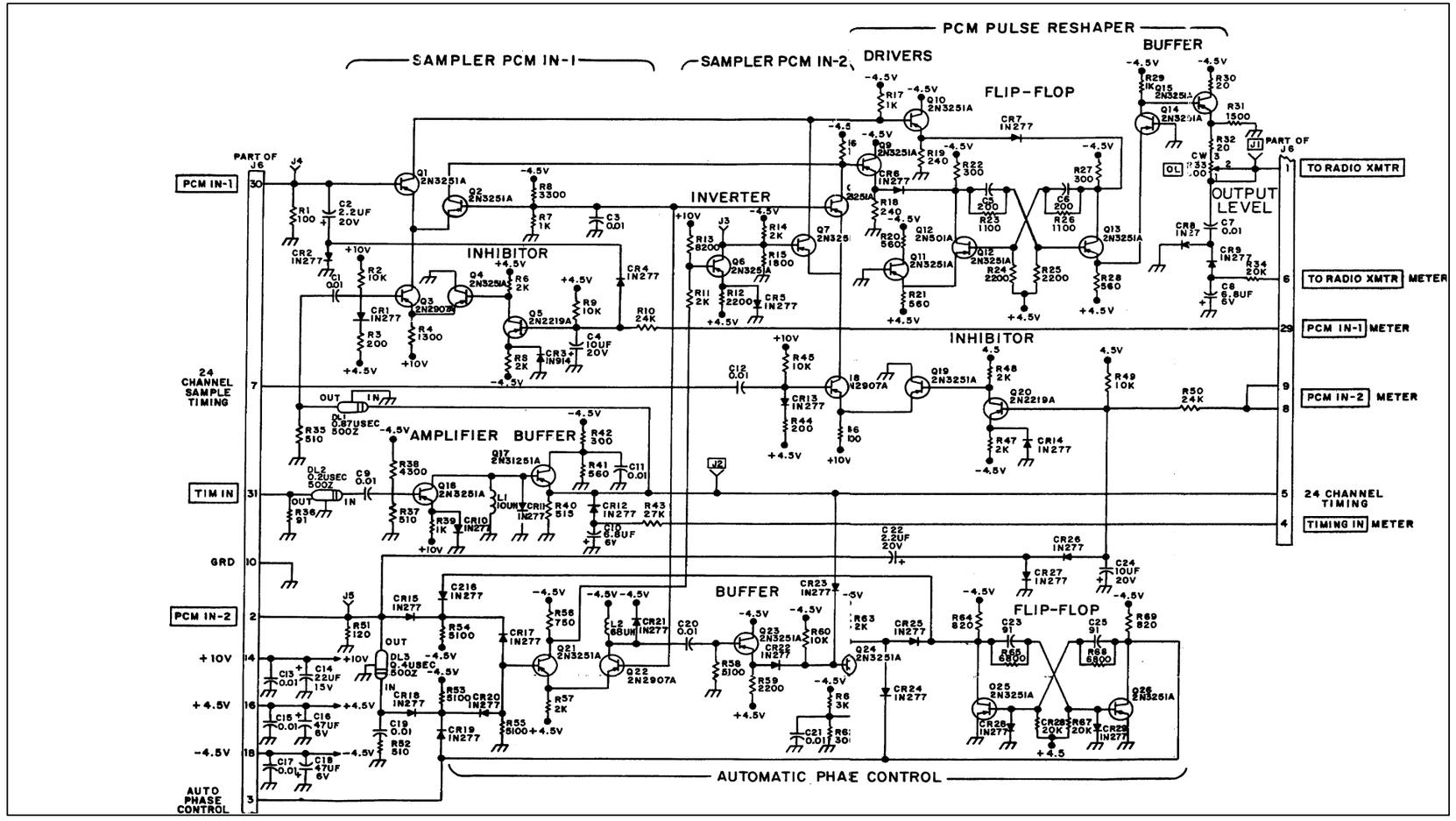


Figure 6-28-1. Transmitter, panel 5A2A, schematic diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN PICOFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ☐ INDICATES EQUIPMENT MARKING

CEOBR005

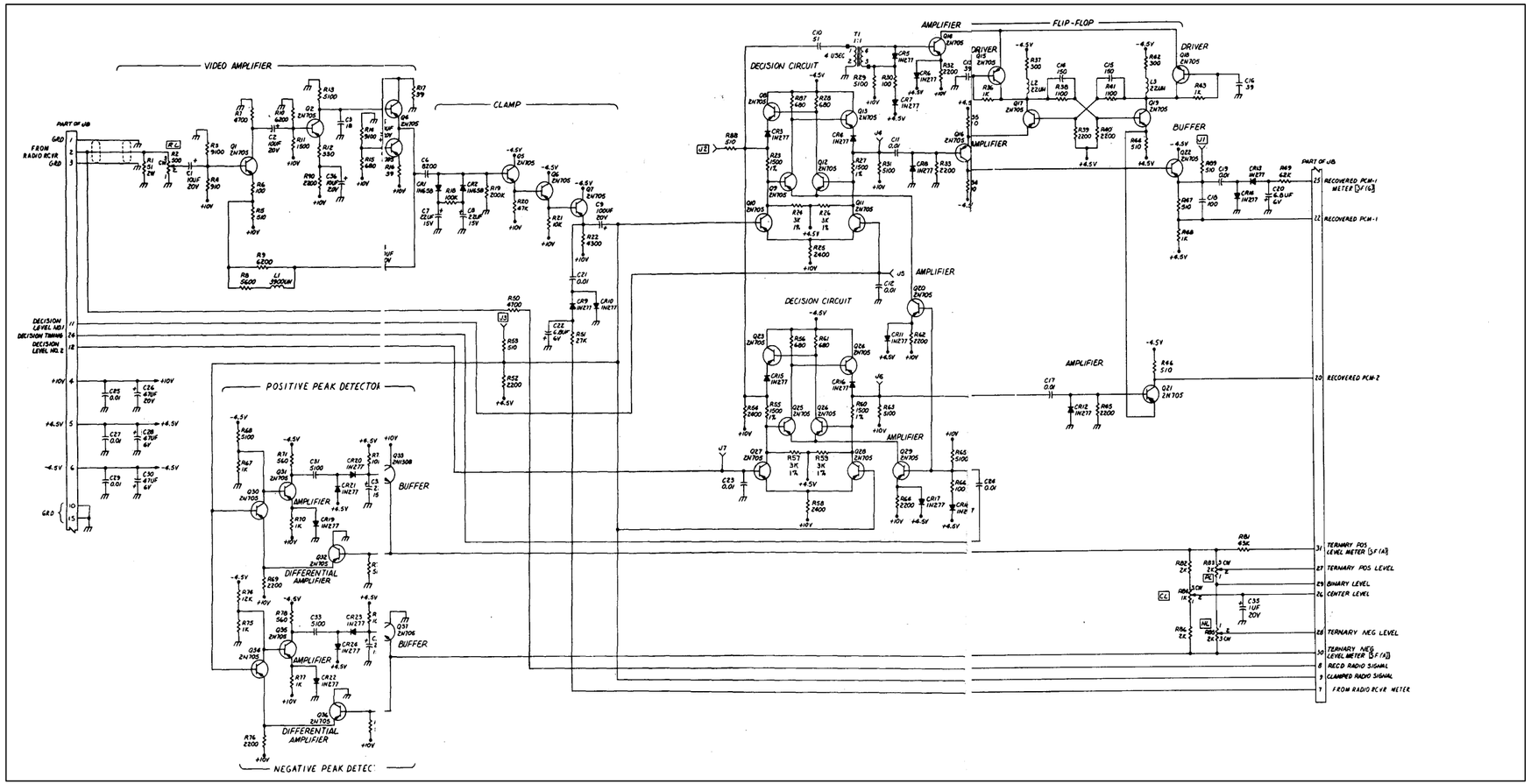


Figure 6-29. Receiver, panel 5A3, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ☐ INDICATES EQUIPMENT MARKING

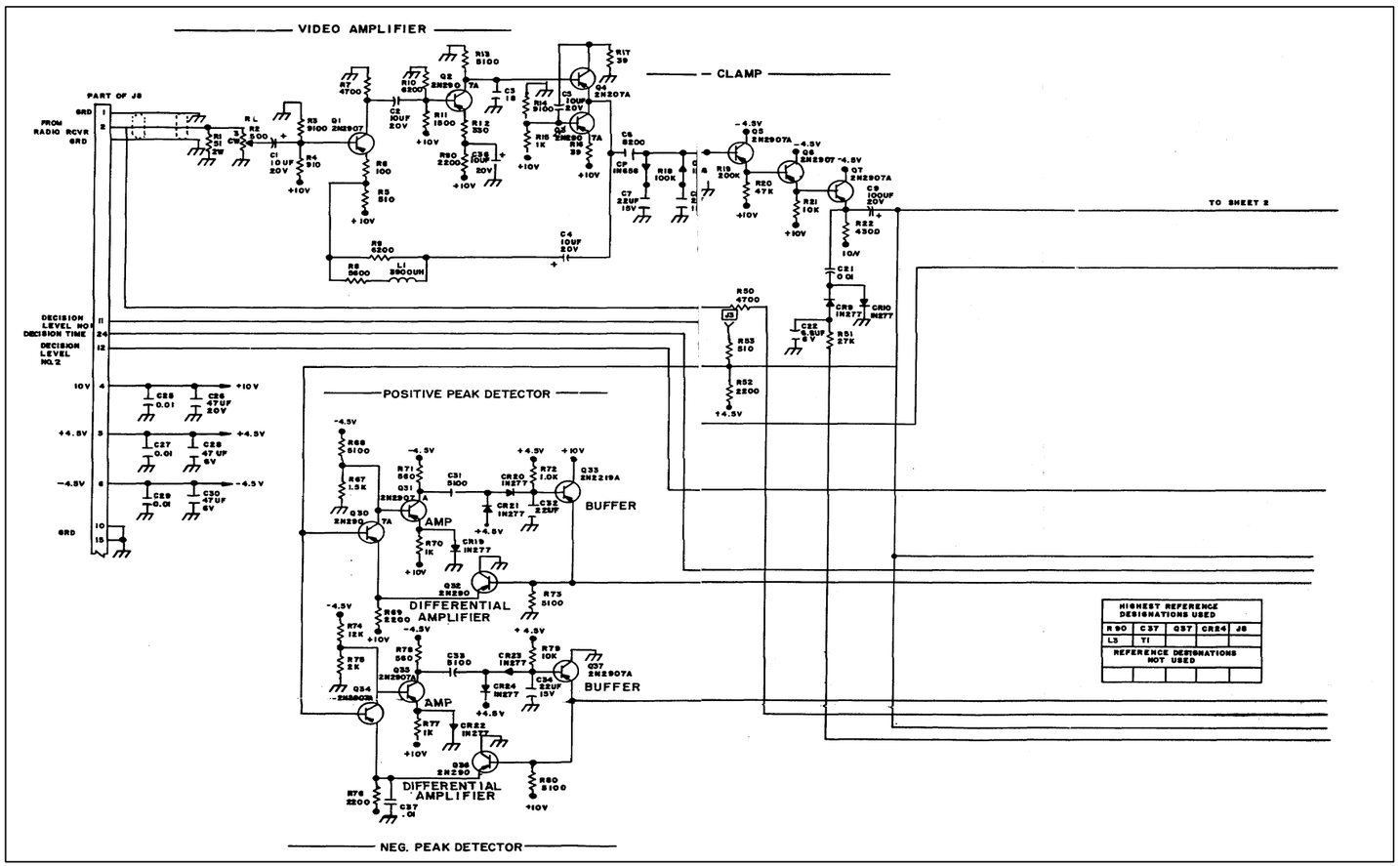


Figure 6-29.1. Receiver, panel 5A3A, schematic diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN PICOFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE 74 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
4. ☐ INDICATES EQUIPMENT MARKING

CEOBR006

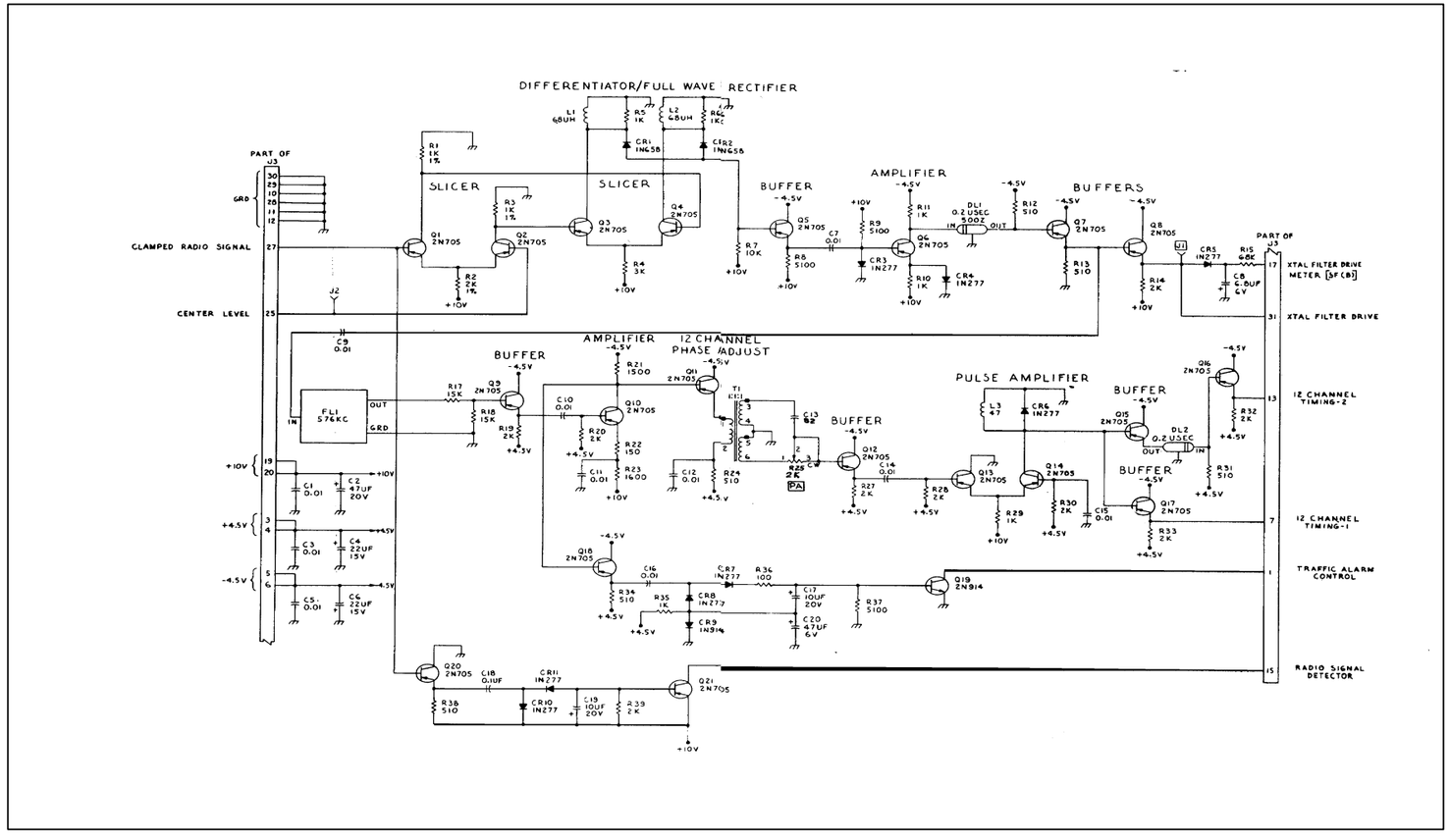


Figure 6-30. Timing generator No. 1, panel 5A4, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ☐ INDICATES EQUIPMENT MARKING

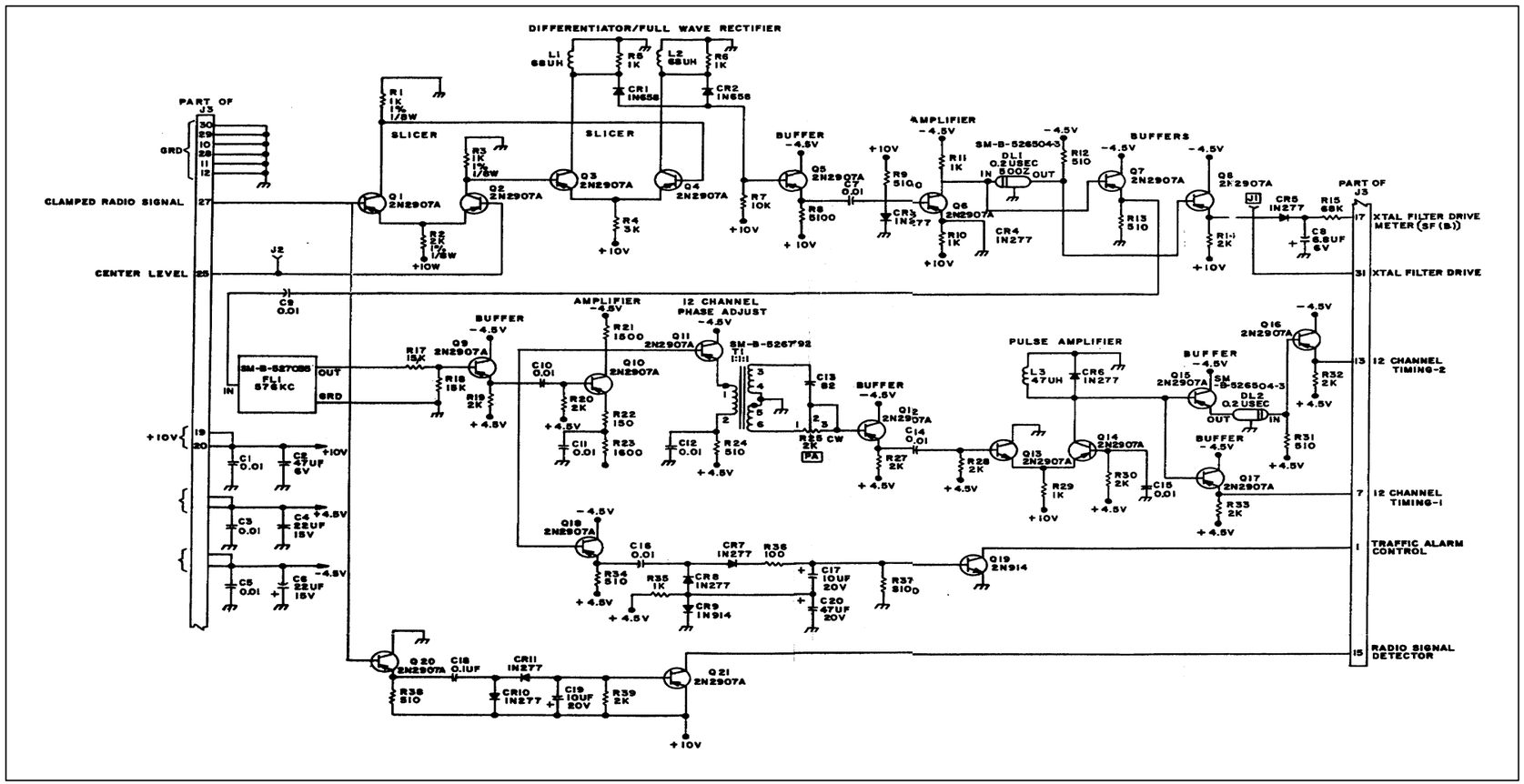


Figure 6-30.1. Timer generator No1., panel 5A4A, schematic diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN PICOFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS. ALL CAPACITORS ARE 100V.

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ☐ INDICATES EQUIPMENT MARKING

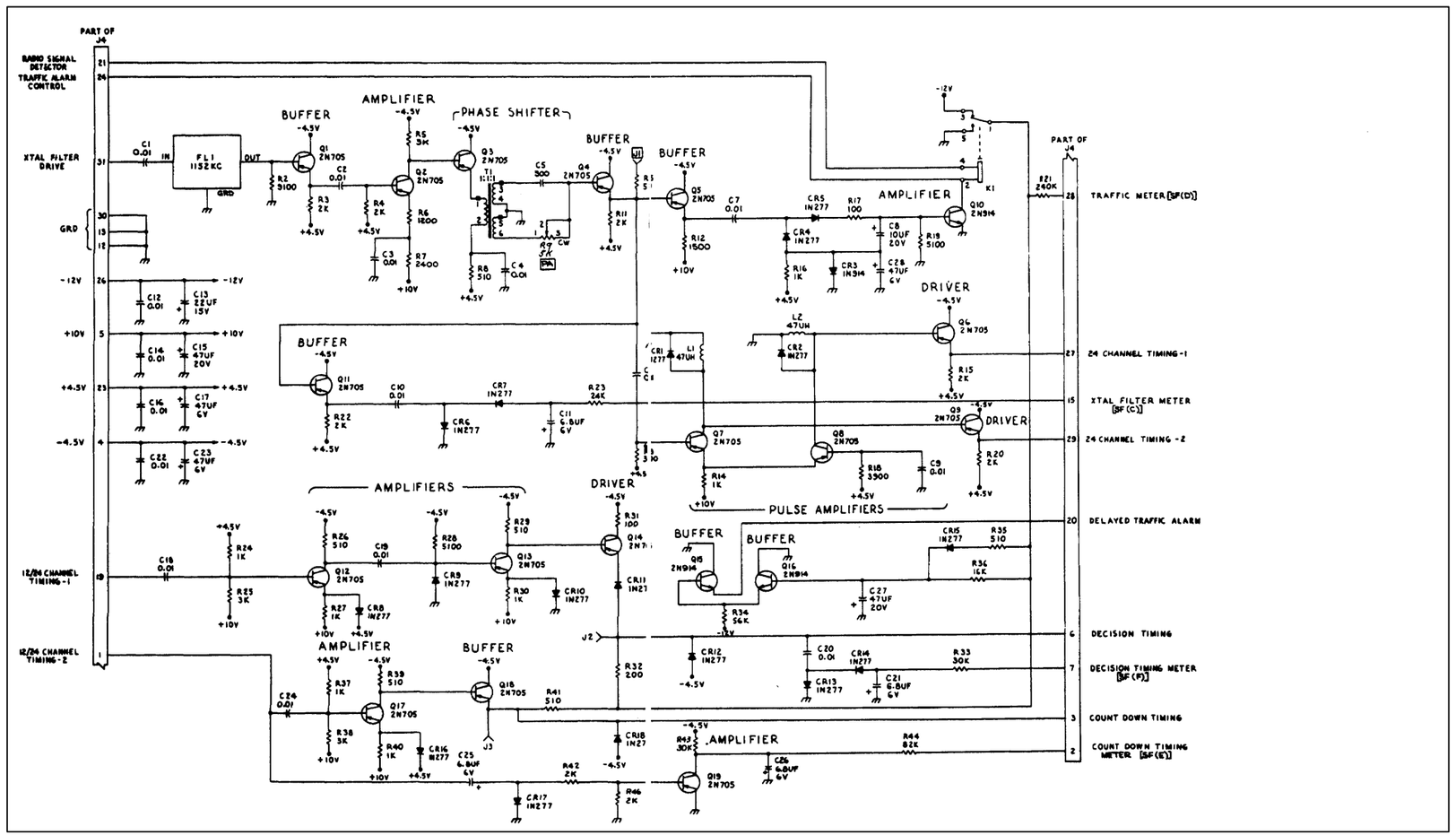


Figure 6-31. Timing generator No. 2, panel 5A5, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS
4. ☐ INDICATES EQUIPMENT MARKING

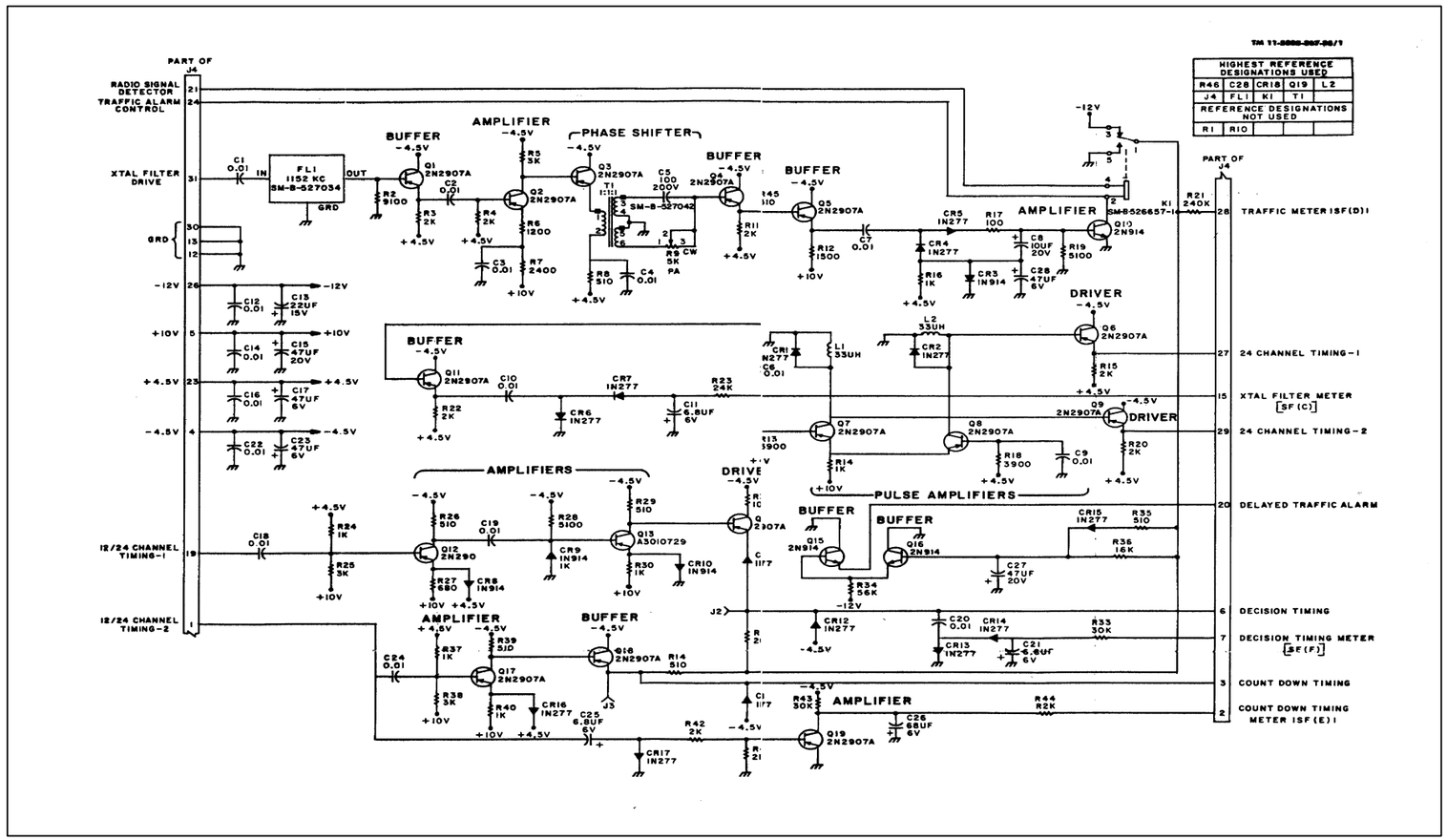


Figure 6-31.1. Timer generator No.2, panel 5A5A, schematic diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN PICOFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS. ALL CAPACITORS ARE 100V.

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ▭ INDICATES EQUIPMENT MARKING

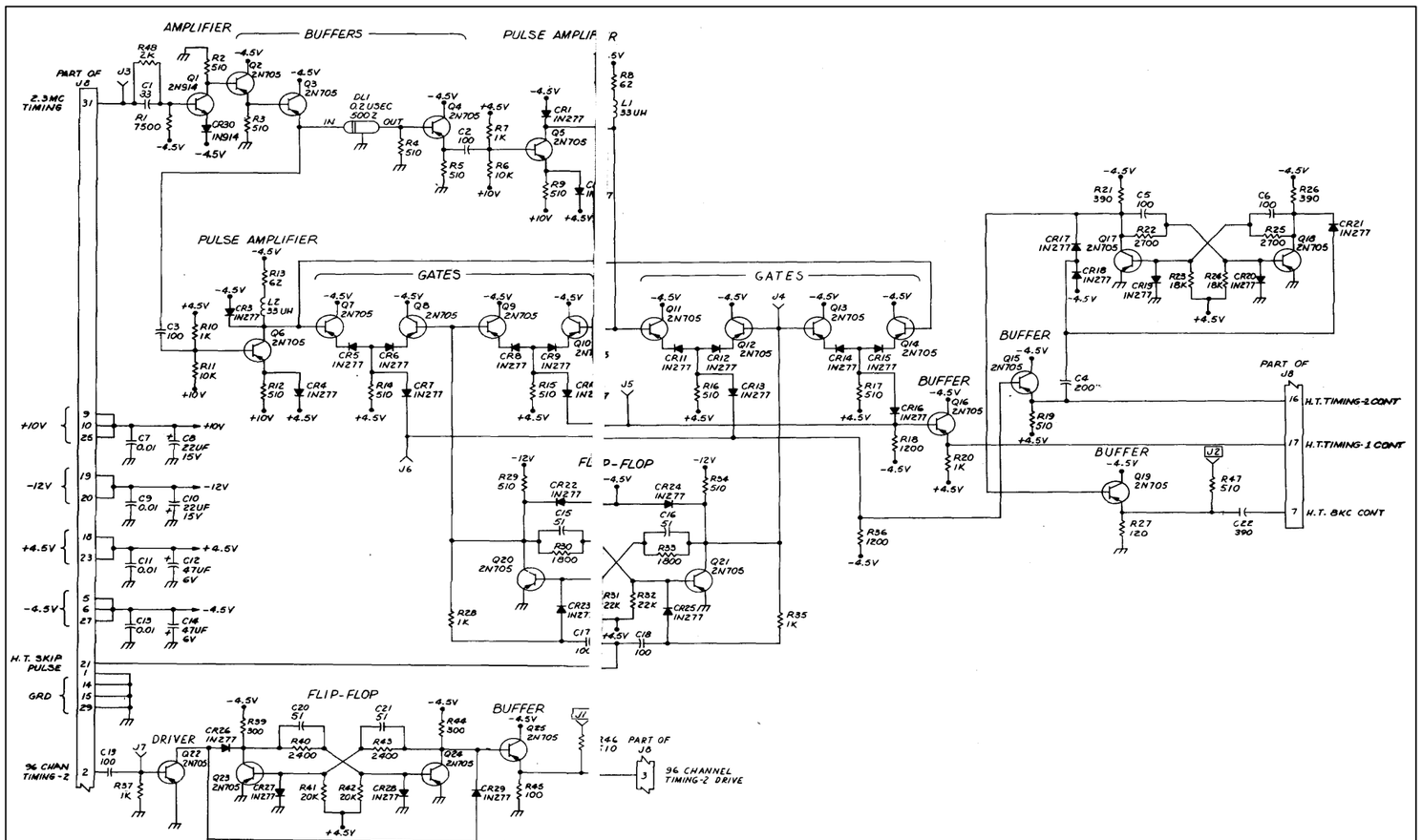


Figure 6-32. Timing generator No. 4, panel 4A9, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ▭ INDICATES EQUIPMENT MARKING

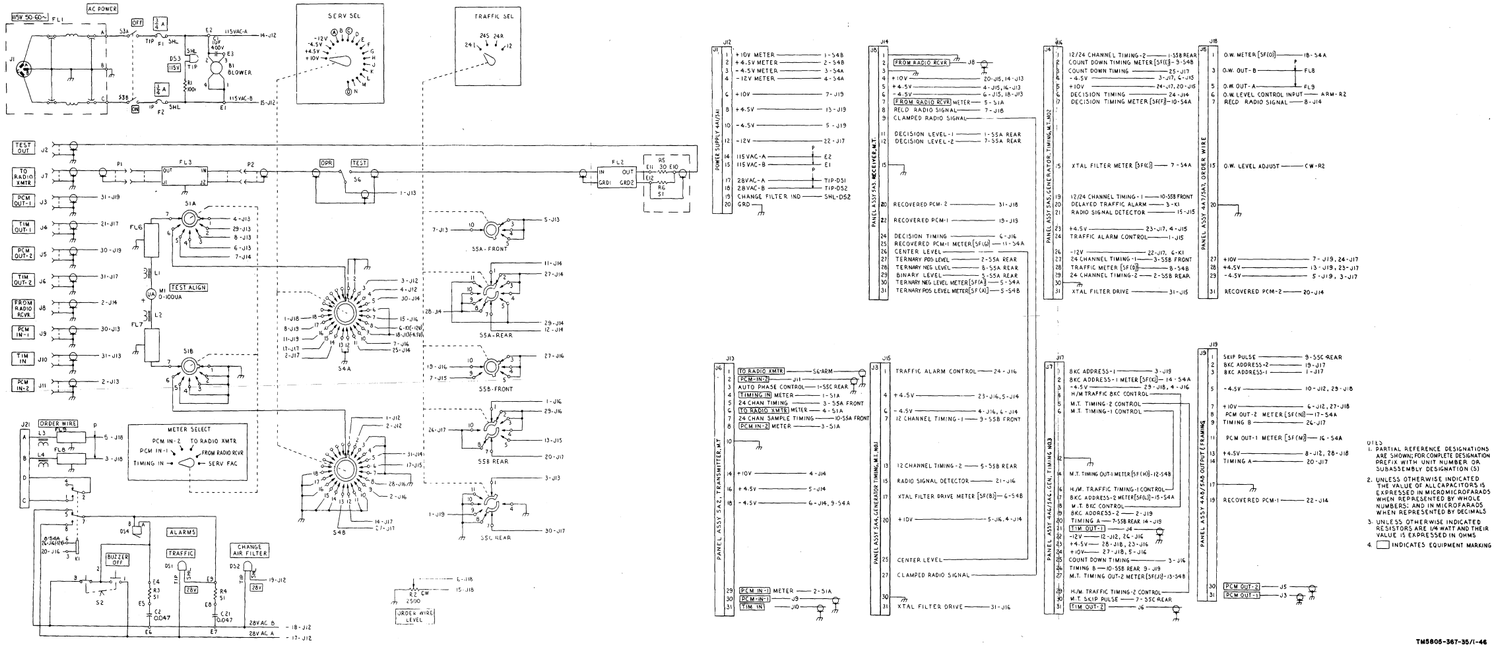


Figure 6-33. Multiplexer TD-202/U,, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS
4. ☐ INDICATES EQUIPMENT MARKING

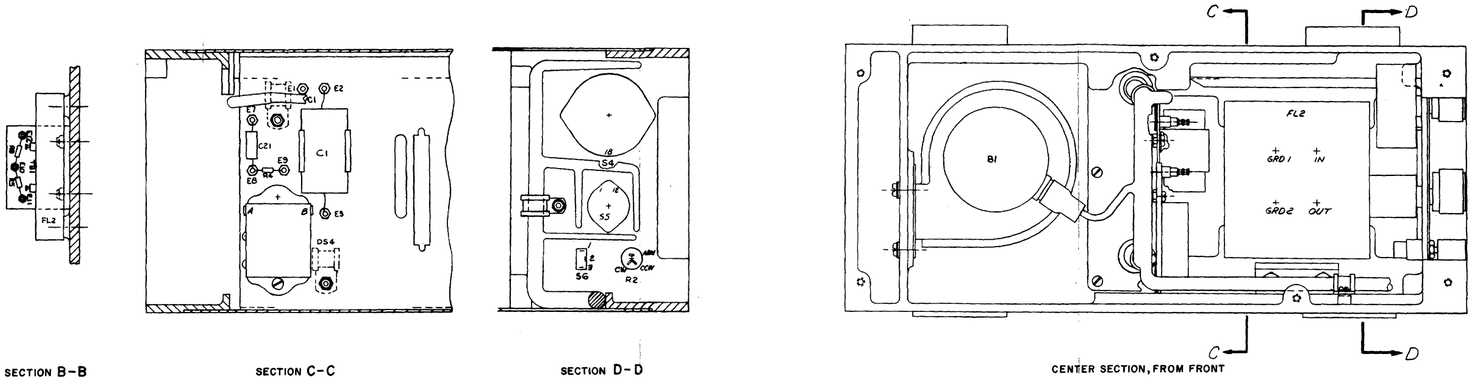


Figure 6-34. Multiplexer TD-202/U, component identification diagram

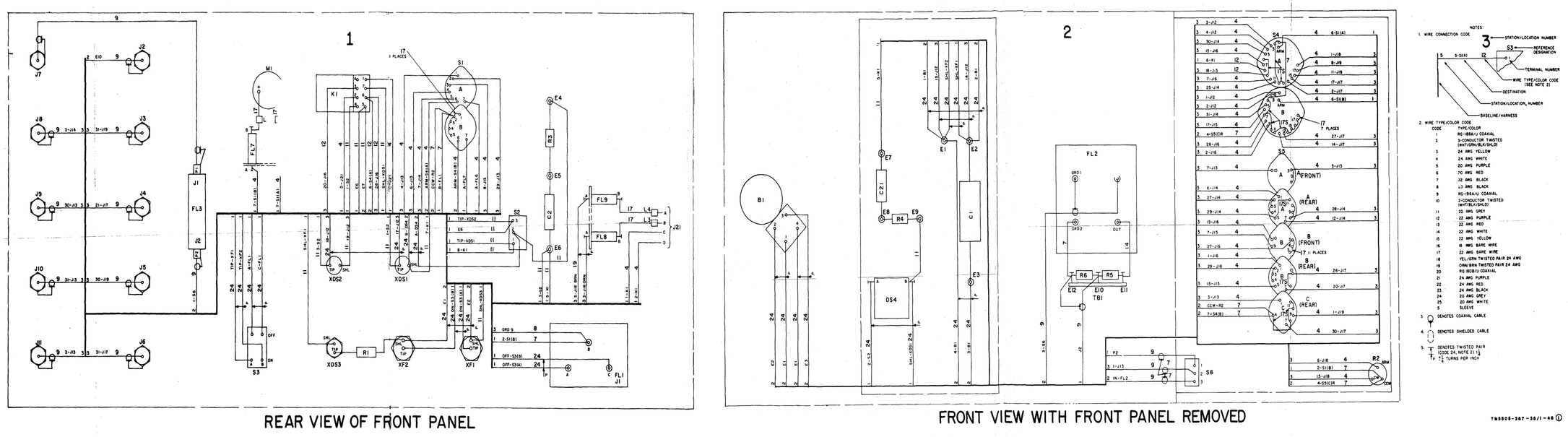


Figure 6-35. Multiplexer TD-202/U, unit wiring diagram (part 1of 2).

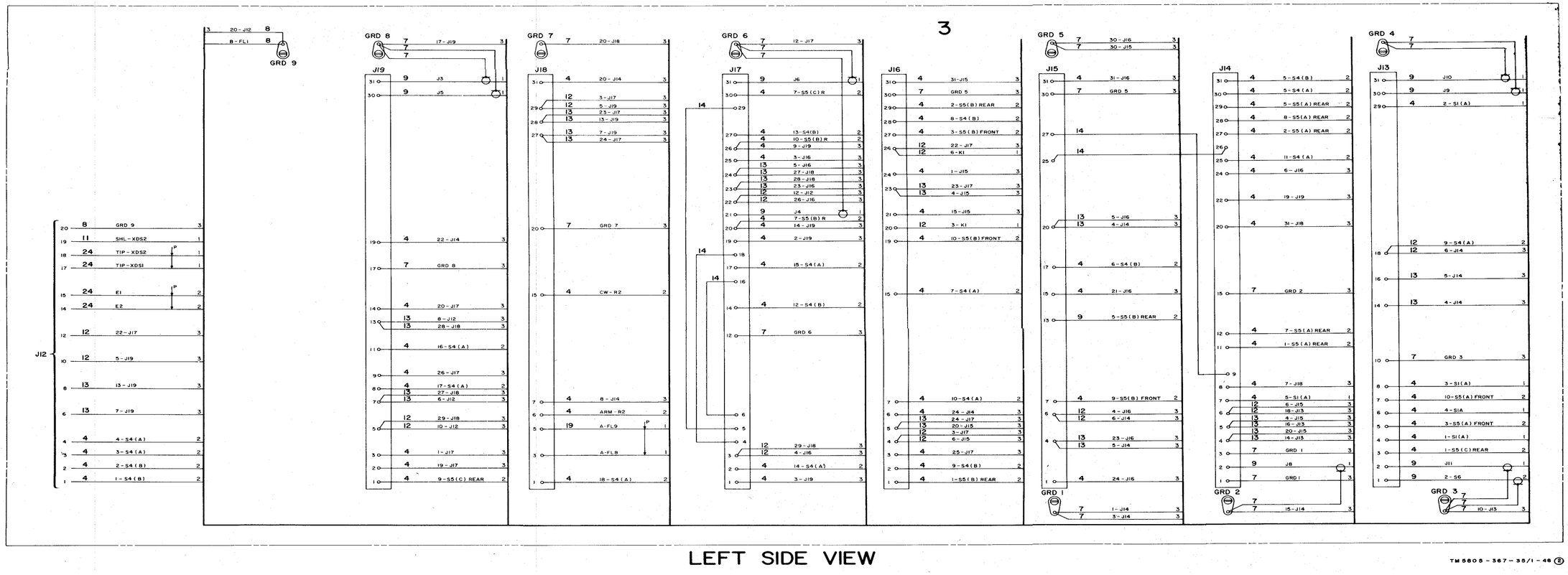


Figure 6-35. Multiplexer TD-202/U, unit wiring diagram (part 2 of 2).

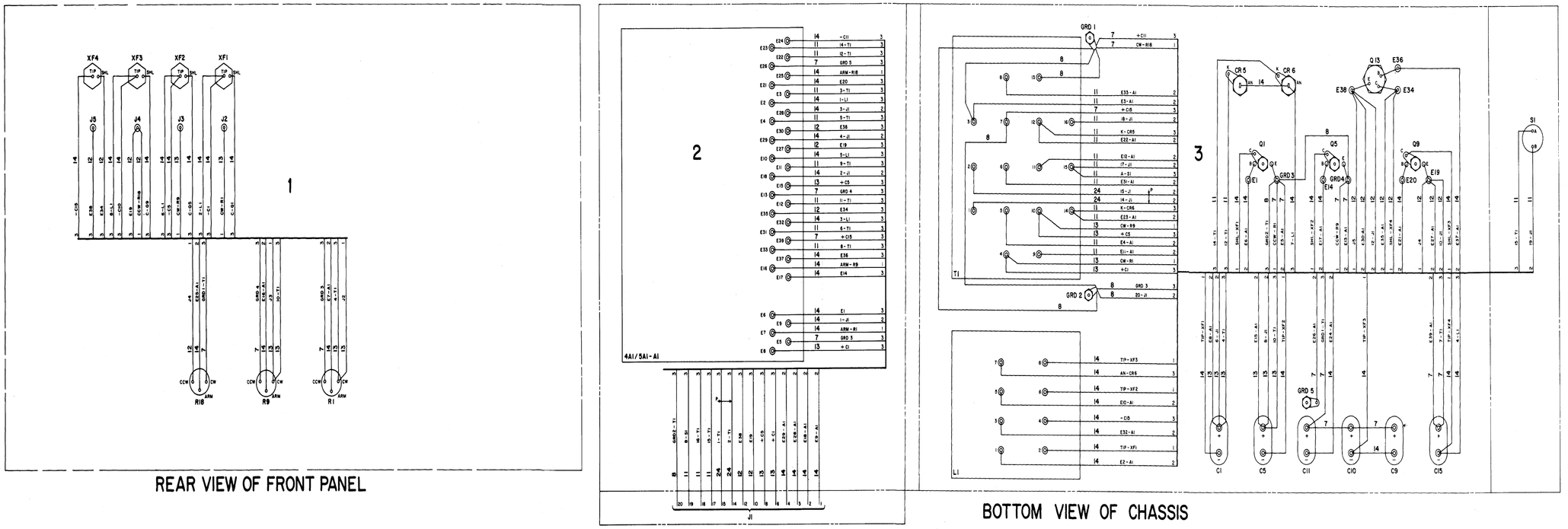


Figure 6-36. Power supply, panel 4A1/5A1, wiring diagram.

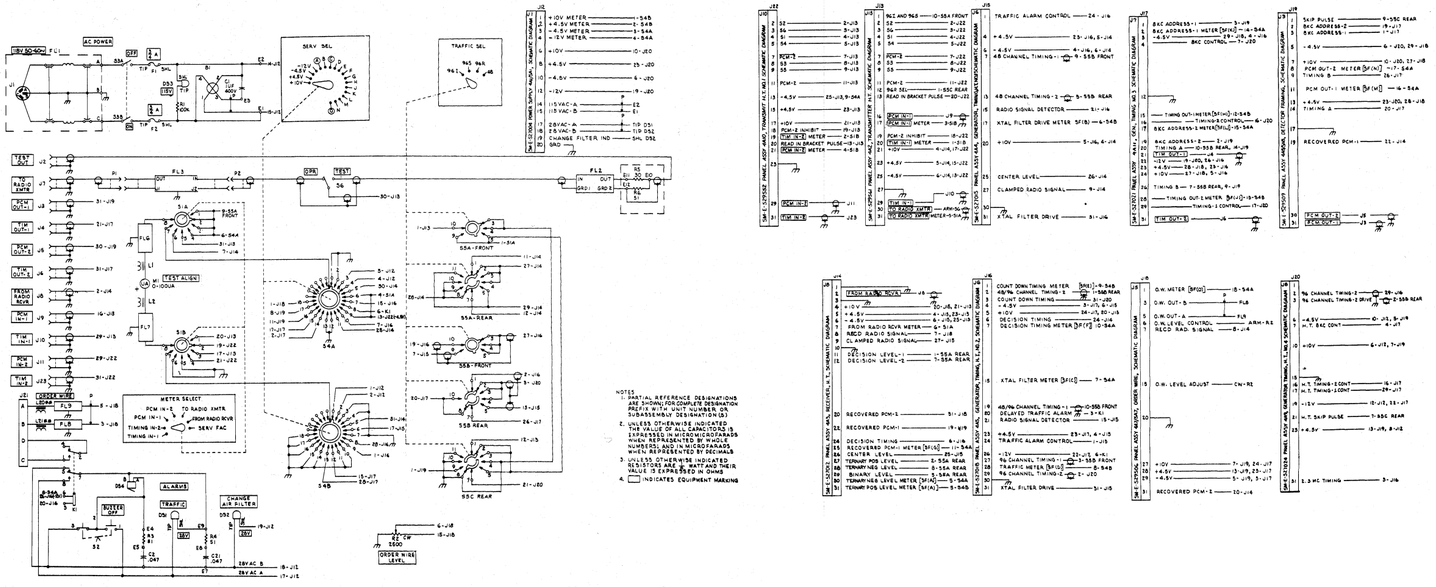


Figure 6-37. Multiplexer TD-203/U, schematic diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS

3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE ¼ WATT AND THEIR VALUE IS EXPRESSED IN OHMS

4. ☐ INDICATES EQUIPMENT MARKING

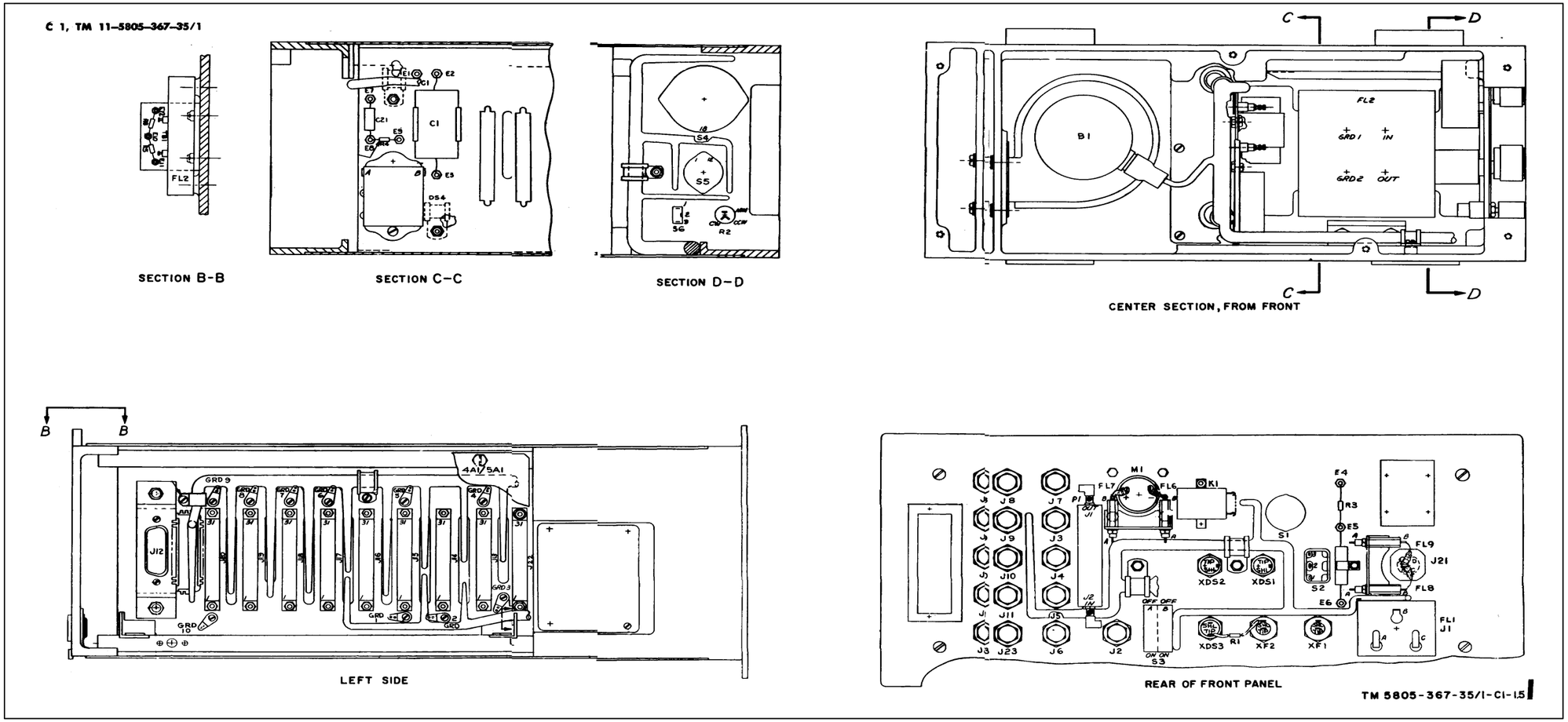


Figure 6-38. Multiplexer TD-203/U, component identification diagram.

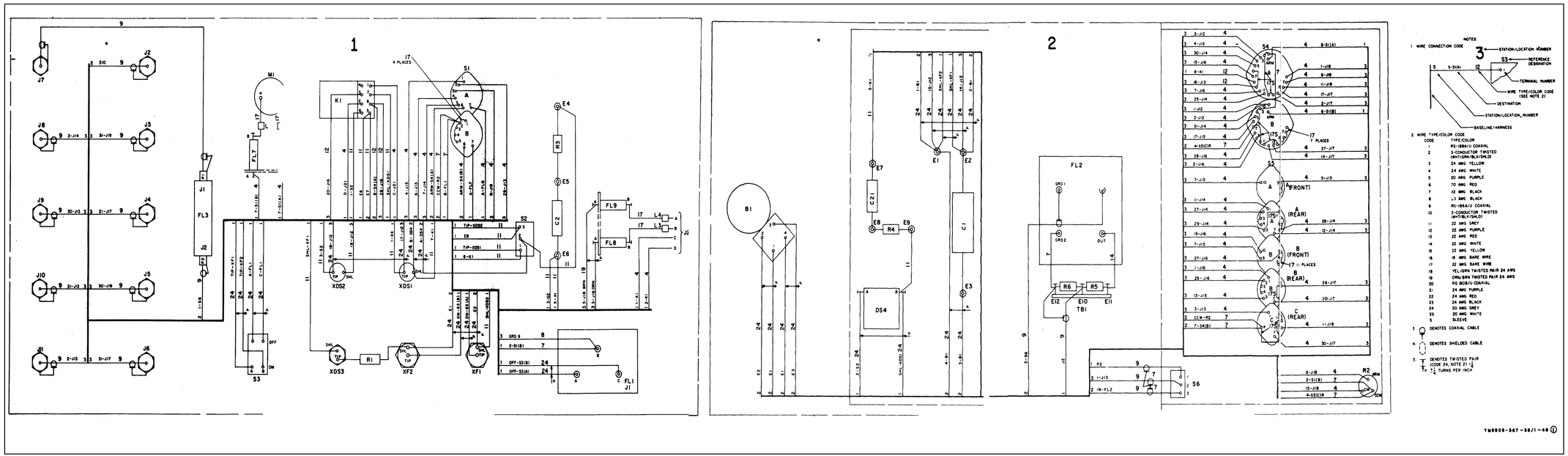
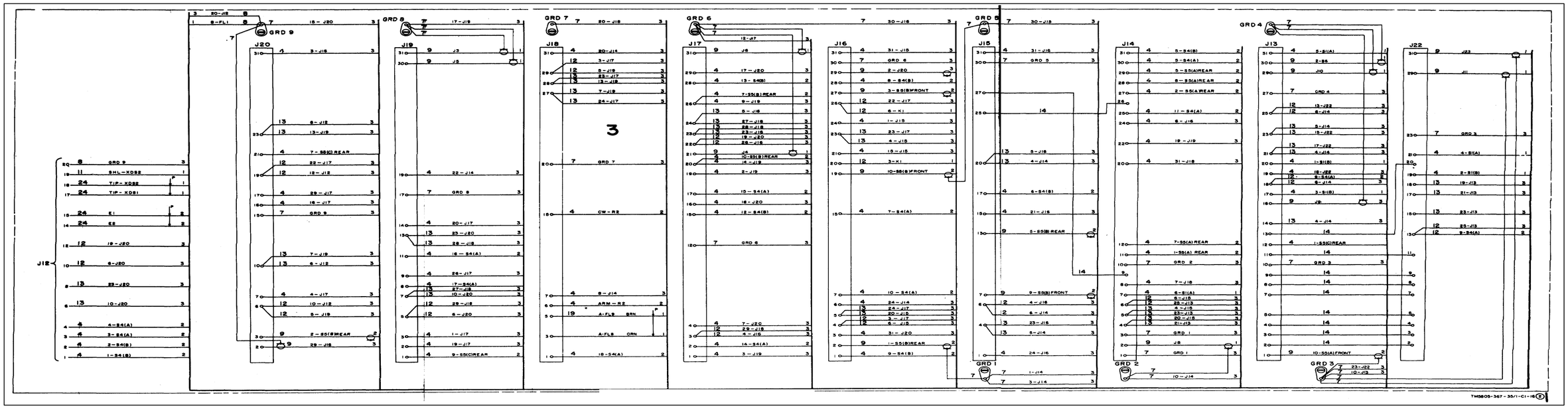


Figure 6-39. Multiplexer TD-203/U, unit wiring diagram (sheet 1 of 2).



LEFT SIDE VIEW

Figure 6-39. Multiplexer TD-203/U, unit wiring diagram (sheet 2 of 2).

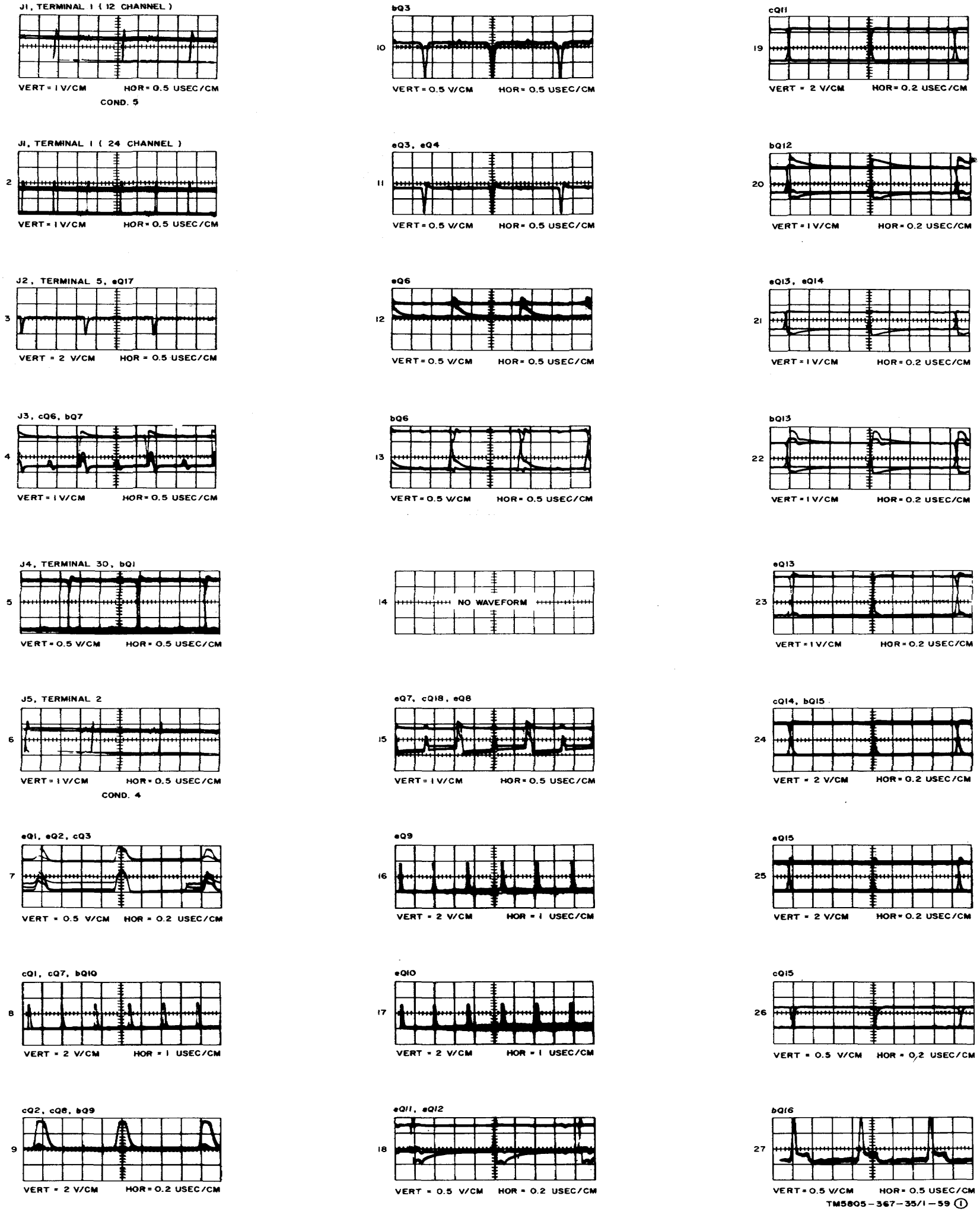
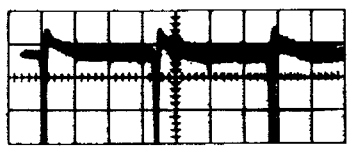
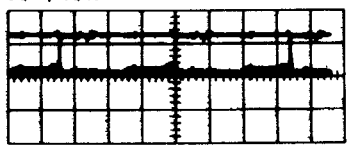


Figure 6-40. Panel 5A2, waveforms (part 1 of 2)

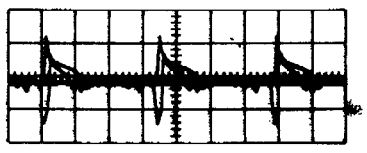
cQ16, bQ17



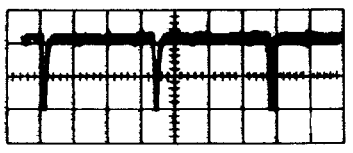
eQ21, eQ22



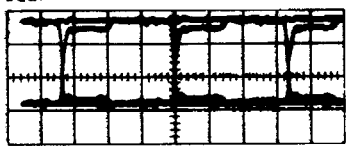
bQ24



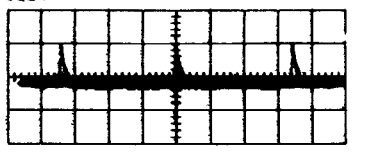
eQ17



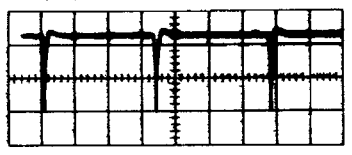
bQ21



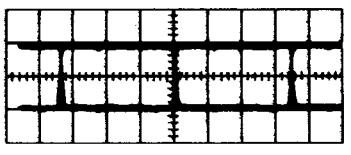
cQ24



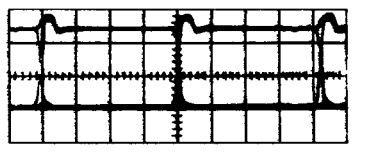
eQ18, eQ19



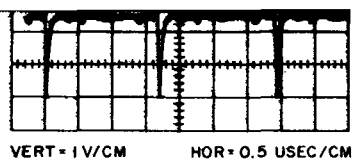
cQ21

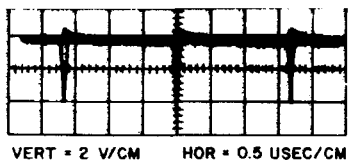


cQ12

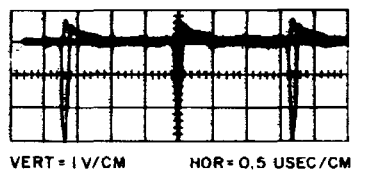


bQ18

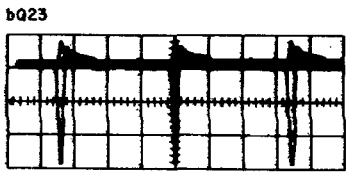




cQ22



bQ23



CONDITIONS FOR OBTAINING WAVEFORMS

NOTES 1, 2, AND 3 GIVEN BELOW ARE APPLICABLE TO ALL WAVEFORMS ON THIS ILLUSTRATION, NOTE-REFERENCES GIVEN WITH WAVEFORMS PERTAIN TO CONDITIONS LISTED BELOW WHICH ARE REQUIRED TO OBTAIN THAT WAVEFORM.

1. INTERCONNECT TWO TD-352/U's WITH THE TEST TD-202/U AS FOLLOWS USING CG-1040B/U CABLE ASSEMBLIES.

MASTER TD-352/U JACKS	TO	TD-202/U JACKS
PCM OUT		PCM IN-1
TIMING OUT		TIM IN (NOTE 2)
PCM IN		PCM OUT-1
TIMING IN		TIM OUT-1
SLAVE TD-352/U JACKS	**TO**	**TD-202/U JACKS**
PCM OUT		PCM IN-2
PCM IN		PCM OUT-2
TIMING IN		TIM OUT-2
MASTER TD-352/U JACK	**TO**	**SLAVE TD-352/U JACK**
SYNC IN		SYNC OUT XMTR

TD-202/U JACKS		
TEST OUT	TO	FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, SYNCHRONIZE AN/USM-140A WITH THE TD-202/U BY CONNECTING AN/USM-140A INPUT JACK TO TD-202/U TIM IN JACK. USE A T CONNECTOR AT TD-202/U TIM IN JACK.

3. UNLESS OTHERWISE NOTED SWITCHES ARE OPERATED AS FOLLOWS:

MASTER AND SLAVE TD-352/U

SWITCH	SETTING	
	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

TD-202/U	
AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	24I

4. DISCONNECT PCM IN-1 CONNECTOR. RECONNECT AFTER OBSERVING WAVEFORM.

5. DISCONNECT PCM IN-2 CONNECTOR. RECONNECT AFTER OBSERVING WAVEFORM.

TM5805-367-35/1-59②

Figure 6-40. Panel 5A2, waveforms (part 2 of 2).

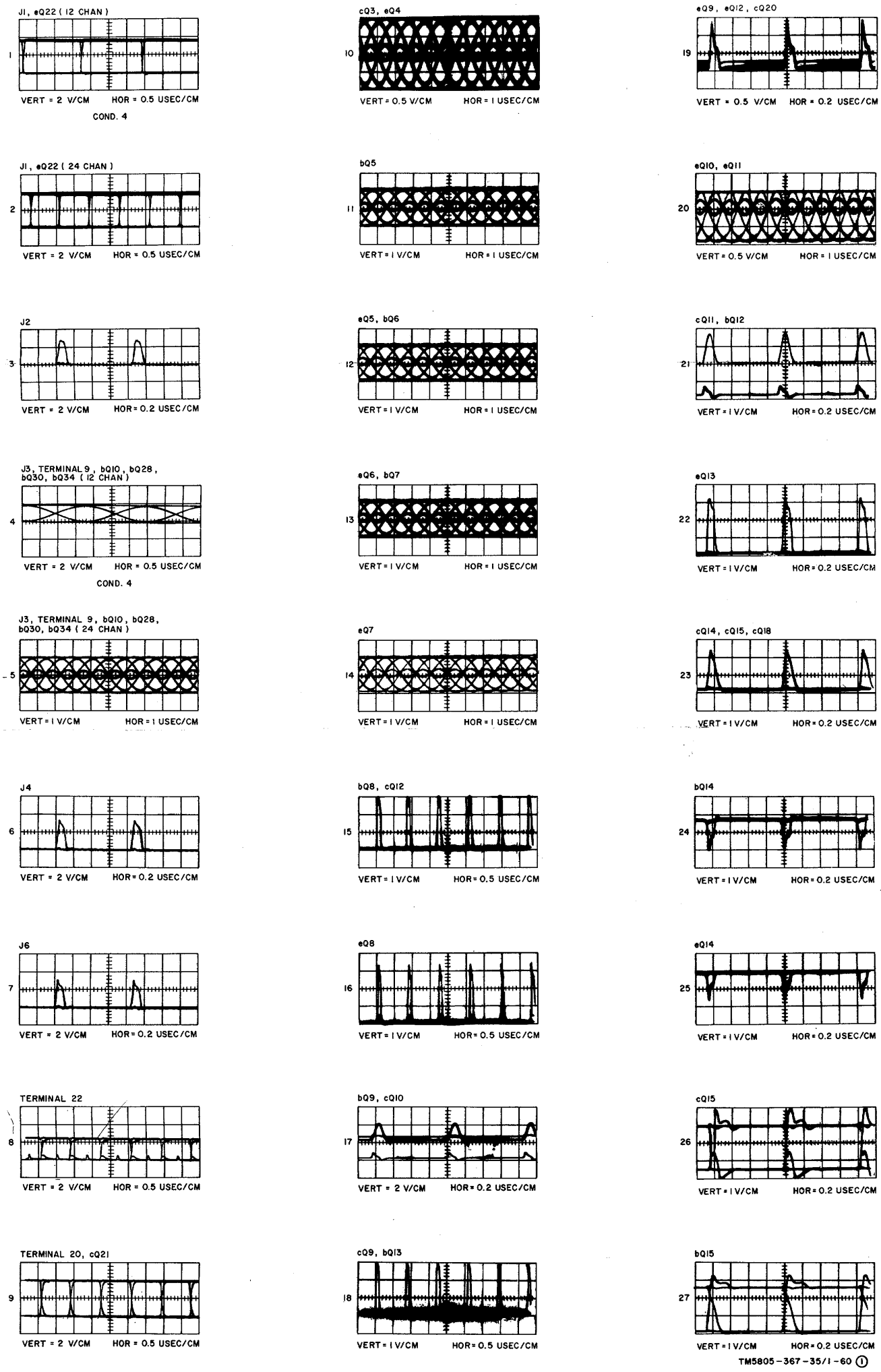
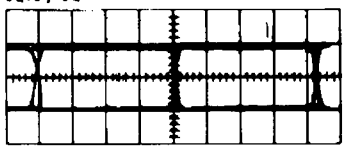


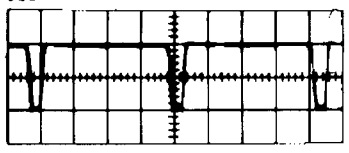
Figure 6-41. Panel, 5A3, waveforms (part 1 of 2).

cQ16, eQ17



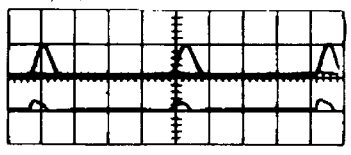
28 VERT = 2 V/CM HOR = 0.2 USEC/CM

eQ20



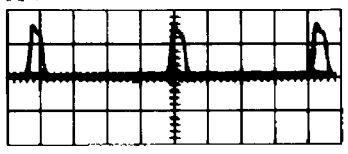
36 VERT = 1 V/CM HOR = 0.2 USEC/CM

bQ26, cQ28



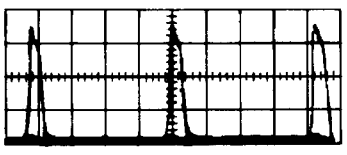
44 VERT = 2 V/CM HOR = 0.2 USEC/CM

bQ16



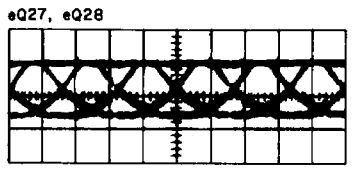
29 VERT = 2 V/CM HOR = 0.2 USEC/CM

bQ21



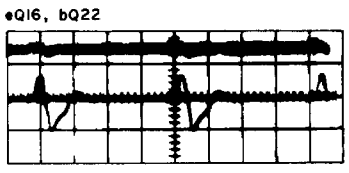
37 VERT = 1 V/CM HOR = 0.2 USEC/CM

eQ27, eQ28



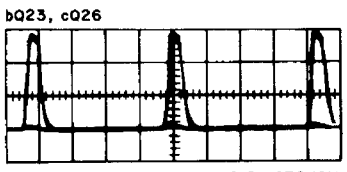
45 VERT = 0.5 V/CM HOR = 0.5 USEC/CM

eQ16, bQ22



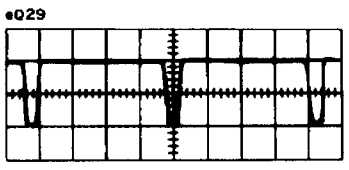
30 VERT = 0.5 V/CM HOR = 0.2 USEC/CM

bQ23, cQ26



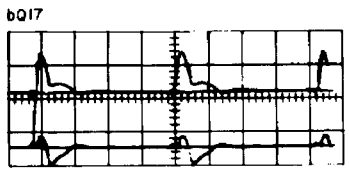
38 VERT = 2 V/CM HOR = 0.2 USEC/CM

eQ29



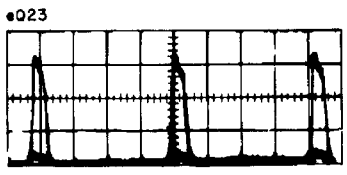
46 VERT = 1 V/CM HOR = 0.2 USEC/CM

bQ17



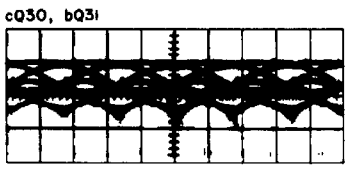
31 VERT = 1 V/CM HOR = 0.2 USEC/CM

eQ23



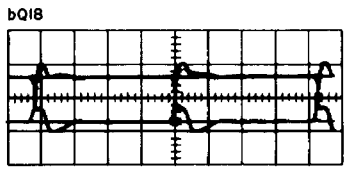
39 VERT = 1 V/CM HOR = 0.2 USEC/CM

cQ30, bQ31



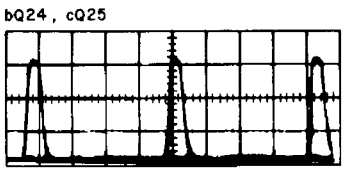
47 VERT = 0.5 V/CM HOR = 0.5 USEC/CM

bQ18



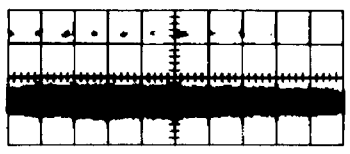
32 VERT = 2 V/CM HOR = 0.2 USEC/CM

bQ24, cQ25



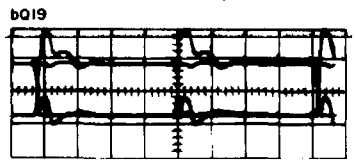
40 VERT = 1 V/CM HOR = 0.2 USEC/CM

cQ31



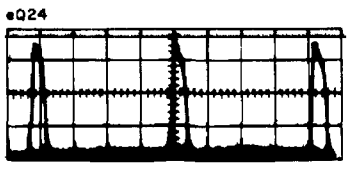
48 VERT = 1 V/CM HOR = 1 USEC/CM

bQ19



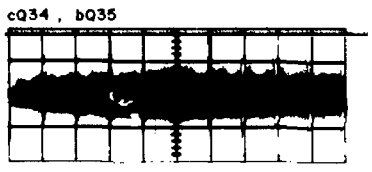
33 VERT = 1 V/CM HOR = 0.2 USEC/CM

eQ24



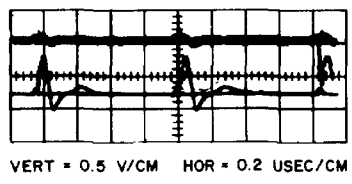
41 VERT = 1 V/CM HOR = 0.2 USEC/CM

cQ34, bQ35



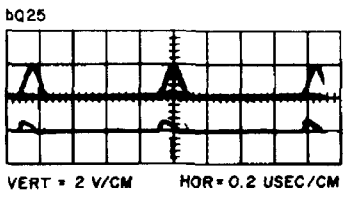
49 VERT = 0.5 V/CM HOR = 1 USEC/CM

eQ19



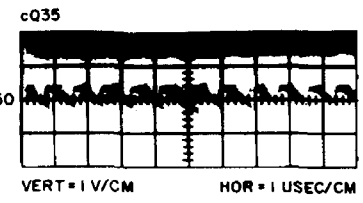
34 VERT = 0.5 V/CM HOR = 0.2 USEC/CM

bQ25



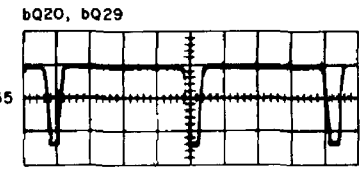
42 VERT = 2 V/CM HOR = 0.2 USEC/CM

cQ35



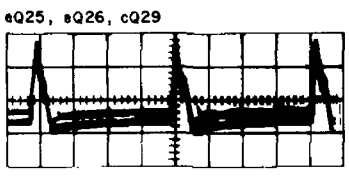
50 VERT = 1 V/CM HOR = 1 USEC/CM

bQ20, bQ29



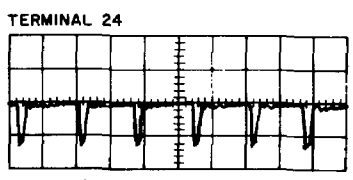
35 VERT = 1 V/CM HOR = 0.2 USEC/CM

eQ25, eQ26, cQ29



43 VERT = 0.5 V/CM HOR = 0.2 USEC/CM

TERMINAL 24



51 VERT = 2 V/CM HOR = 0.5 USEC/CM

CONDITIONS FOR OBTAINING WAVEFORMS

NOTES 1, 2, AND 3 GIVEN BELOW ARE APPLICABLE TO ALL WAVE FORMS ON THIS I
ILLUSTRATION, NOTE-REFERENCES GIVEN WITH WAVEFORMS PERTAIN TO

CONDITIONS LISTED BELOW WHICH ARE REQUIRED TO OBTAIN THAT

WAVEFORM.

1. INTERCONNECT TWO TD-352/U's WITH THE TEST TD-202/U AS FOLLOWS

USING CG-1040B/U CABLE ASSEMBLIES.

MASTER TD-352/U JACKS	TO	TD-202/U JACKS
PCM OUT		PCM IN-1
TIMING OUT		TIM IN (NOTE 2)
PCM IN		PCM OUT-1
TIMING IN		TIM OUT-1

SLAVE TD-352/U JACKS	TO	TD-202/U JACKS
PCM OUT		PCM IN-2
PCM IN		PCM OUT-2
TIMING IN		TIM OUT-2

MASTER TD-352/U JACK	TO	SLAVE TD-352/U JACK
SYNC IN		SYNC OUT XMTR

TD-202/U JACKS

TEST OUT TO FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, SYNCHRONIZE AN/USM-140A WITH THE TD-202/U

BY CONNECTING AN/USM-140A INPUT JACK TO TD-202/U TIM IN JACK. USE A T

CONNECTOR AT TD-202/U TIM IN JACK.

3. UNLESS OTHERWISE NOTED SWITCHES ARE OPERATED AS FOLLOWS:

MASTER AND SLAVE TD-352/U

SWITCH	SETTING	
	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

TD-202/U

AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	24I

4. OPERATE TRAFFIC SEL SWITCH TO 12. OPERATE BACK TO 24I AFTER

OBSERVING WAVEFORM.

TM5805-367-35/1-60②

Figure 6-41. Panel 5A3, waveforms (part 2 of 2).

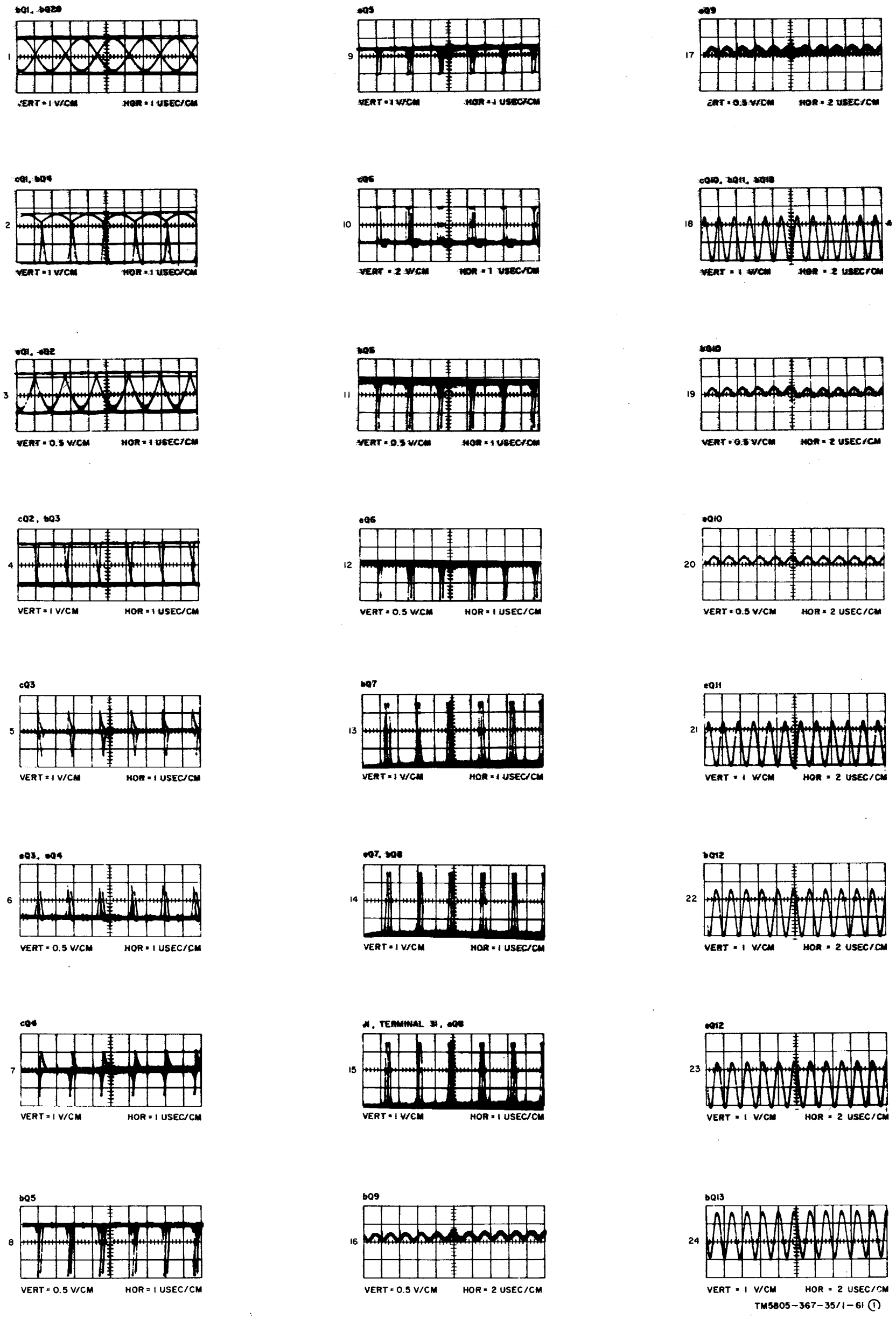
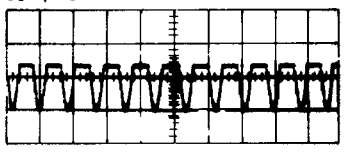


Figure 6-42. Panel 5A4, waveforms (part 1 of 2.)

eQ13, eQ14

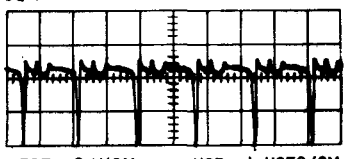
25



VERT = 1 V/CM HOR = 2 USEC/CM

bQ16

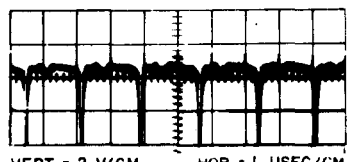
28



VERT = 2 V/CM HOR = 1 USEC/CM

TERMINAL 13, eQ16

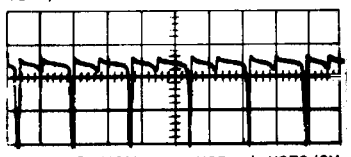
30



VERT = 2 V/CM HOR = 1 USEC/CM

cQ14, bQ15

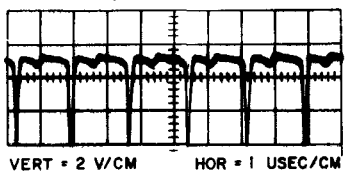
26



VERT = 2 V/CM HOR = 1 USEC/CM

TERMINAL 7, eQ17

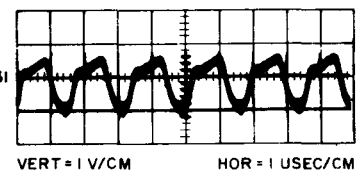
29



VERT = 2 V/CM HOR = 1 USEC/CM

eQ18

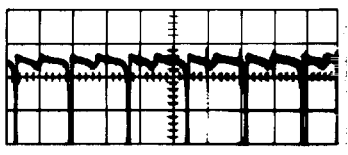
31



VERT = 1 V/CM HOR = 1 USEC/CM

eQ15

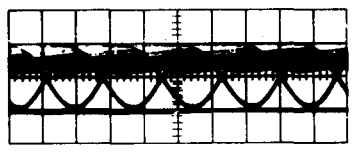
27



VERT = 2 V/CM HOR = 1 USEC/CM

eQ20

32



VERT = 1 V/CM HOR = 1 USEC/CM

CONDITIONS FOR OBTAINING WAVEFORMS

1. INTERCONNECT THE TEST TD-352/U WITH THE TEST TD-202/U AS FOLLOWS USING CG-1040B/U CABLE ASSEMBLES.

MASTER TD-352/U JACKS	TO	TD-202/U JACKS
PCM OUT		PCM IN-1
TIMING OUT		TIM IN (NOTE2)
PCM IN		PCM OUT-1
TIMING IN		TIM OUT-1

TD-202/U JACKS		
TEST OUT	TO	FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, SYNCHRONIZE AN/USM-140 WITH THE TD-202/U BY CONNECTING AN/USM-140A INPUT JACK TO TD-202/U TIM IN JACK. USE A T CONNECTOR AT TD-202/U TIM IN JACK.

3. UNLESS OTHERWISE NOTED SWITCHES ARE OPERATED AS FOLLOWS:

TD-352/U SWITCH	SETTING
AC POWER	ON
2 WIRE 4 WIRE	4 WIRE
AUX	OUT
ADDRESS	MASTER

TD-202/U	
AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	12

TM5805-367-35/1-61②

Figure 6-42. Panel 5A, waveforms (part 2 of 2).

1
J1, bQ5, eQ4, bQ11, bQ4
VERT = 1 V/CM HOR = 1 USEC/CM

9
TERMINAL 19
VERT = 2 V/CM HOR = 0.5 USEC/CM
SPEC. COND. 4

17
eQ2
VERT = 0.5 V/CM HOR = 1 USEC/CM

2
J2, TERMINAL 6
VERT = 2 V/CM HOR = 0.5 USEC/CM

10
TERMINAL 27, eQ6
VERT = 2 V/CM HOR = 0.5 USEC/CM

18
cQ2, bQ3, eQ3
VERT = 0.5 V/CM HOR = 1 USEC/CM

3
J2, TERMINAL 6
VERT = 2 V/CM HOR = 0.5 USEC/CM
SPEC. COND. 4

11
TERMINAL 27, eQ6
VERT = 2 V/CM HOR = 0.5 USEC/CM
SPEC. COND. 5

19
eQ5
VERT = 1 V/CM HOR = 1 USEC/CM

4
J3, TERMINAL 3, eQ18
VERT = 2 V/CM HOR = 0.5 USEC/CM

12
TERMINAL 29, eQ9
VERT = 2 V/CM HOR = 0.5 USEC/CM

20
bQ6, cQ8
VERT = 2 V/CM HOR = 1 USEC/CM

5
J3, TERMINAL 3, eQ18
VERT = 2 V/CM HOR = 0.5 USEC/CM
SPEC. COND. 4

13
TERMINAL 31
VERT = 2 V/CM HOR = 0.5 USEC/CM

21
cQ7, bQ9
VERT = 2 V/CM HOR = 1 USEC/CM

6
TERMINAL 1
VERT = 2 V/CM HOR = 0.5 USEC/CM

14
bQ1
VERT = 0.5 V/CM HOR = 1 USEC/CM

22
bQ7
VERT = 1 V/CM HOR = 1 USEC/CM

7
TERMINAL 1
VERT = 2 V/CM HOR = 0.5 USEC/CM
SPEC. COND. 4

15
eQ1
VERT = 0.5 V/CM HOR = 1 USEC/CM

23
eQ7, eQ8, bQ8
VERT = 1 V/CM HOR = 1 USEC/CM

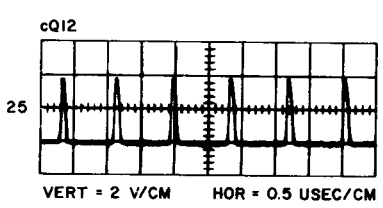
8
TERMINAL 19
VERT = 2 V/CM HOR = 0.5 USEC/CM

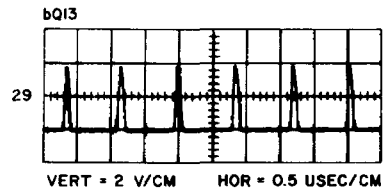
16
bQ2
VERT = 0.5 V/CM HOR = 1 USEC/CM

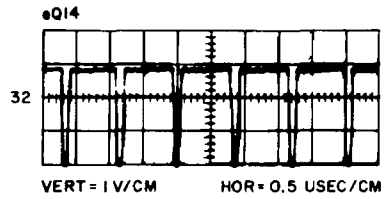
24
eQ11
VERT = 1 V/CM HOR = 1 USEC/CM

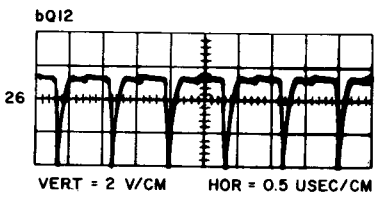
TM5805-367-35/1-62①

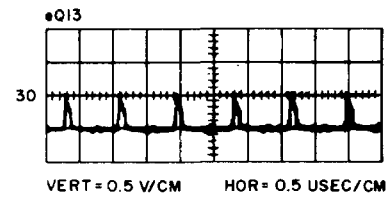
Figure 6-43. Panel 5A5, waveforms (part 1 of 2).

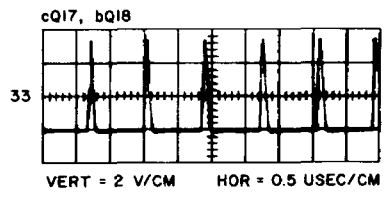


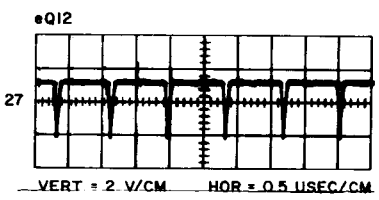


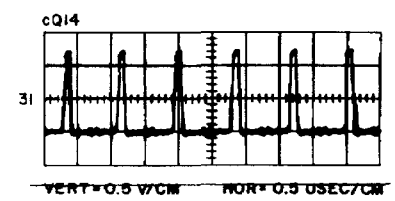


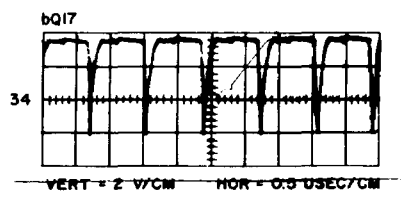


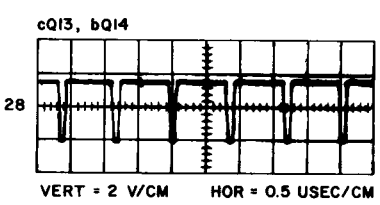


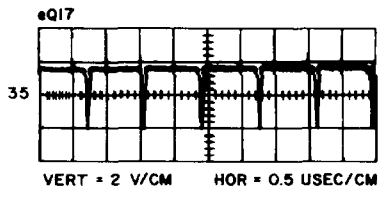












CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOW.

1. TWO TD-352/U MULTIPLEXERS CONNECTED FOR MASTER-SLAVE OPERATION AND INTERCONNECTED WITH TD-202/U AS FOLLOWS USING CG-1040B/U CABLES.

FROM MASTER TD-352/U	TO TD-202/U
PCM OUT	PCM IN-1
TIMING OUT	TIM IN (NOTE 2)
FROM SLAVE TD-352/U	TO TD-202/U
PCM OUT	PCM IN-2
FROM MASTER TD-352/U	TO SLAVE TD-352/U
SYNC OUT XMTR	SYNC IN
FROM TD-202/U	TO MASTER TD-352/U
PCM OUT-1	PCM IN
TIM OUT-1	TIMING IN
FROM TD-202/U	TO SLAVE TD-352/U
PCM OUT-2	PCM IN
TIM OUT-2	TIMING IN
FROM TD-202/U	TO TD-202/U
TEST OUT	FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, OSCILLOSCOPE SYNCHRONIZED FROM TIM IN SIGNAL INPUT TO TD-202/U. USE OF T CONNECTION ON TIM IN CONNECTOR PROVIDES ACCESS TO THIS 576-KC SIGNAL.

3. UNLESS OTHERWISE NOTED, SWITCHES OPERATED AS FOLLOWS:

TD-352/U

	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

TD-202/U

AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	24I

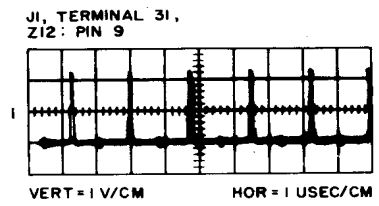
B. SPECIAL.

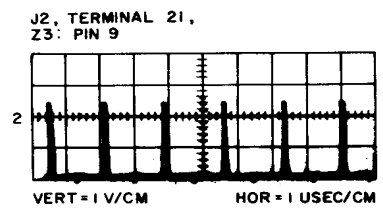
4. OPERATE TRAFFIC SEL SWITCH TO 12.

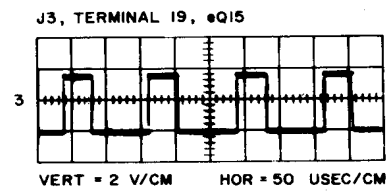
5. WAVEFORM AT TERMINAL 27 SHOULD LAG WAVEFORM AT TERMINAL 31 BY 0.4 USEC.

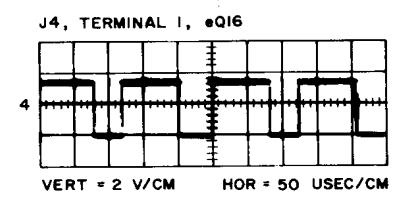
TM5805-367-35/1-62①

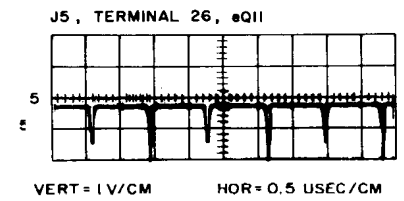
Figure 6-43. Panel 5A5, waveforms (part 2 of 2).

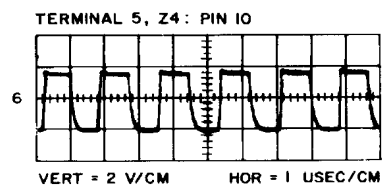


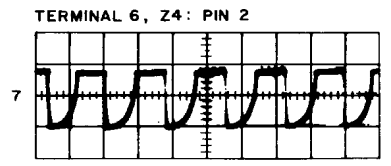


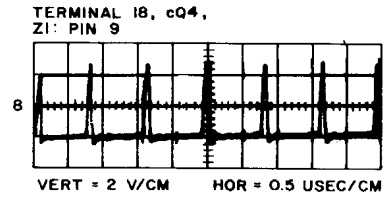


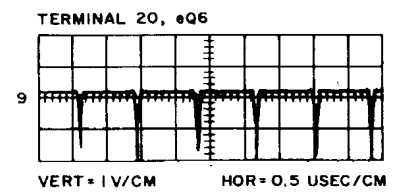


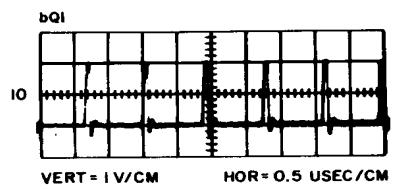


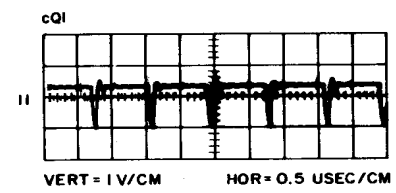


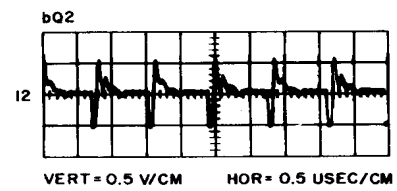


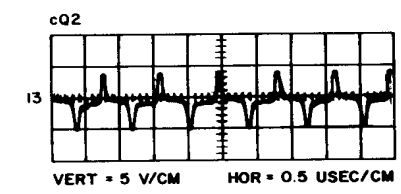


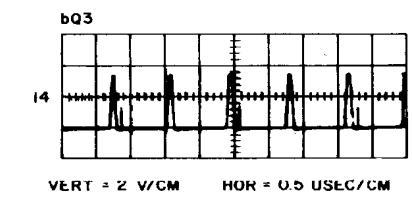


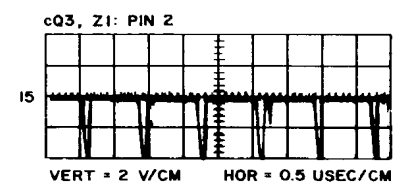


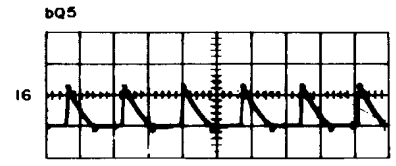


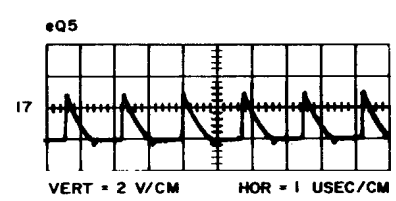


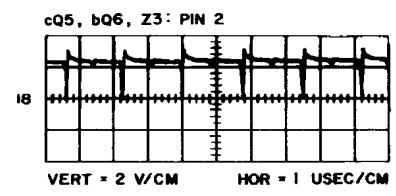


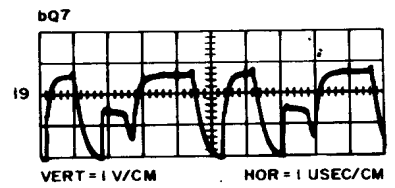


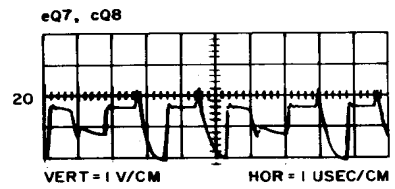


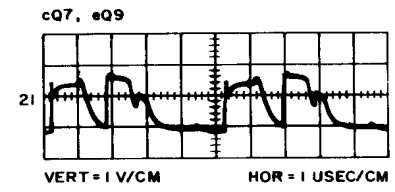


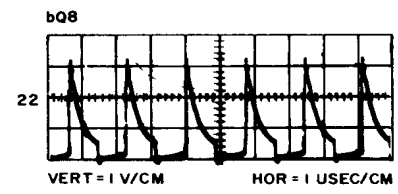


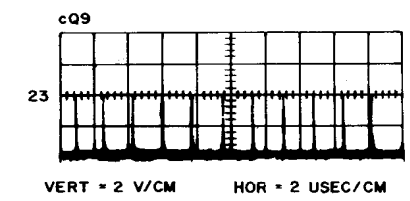


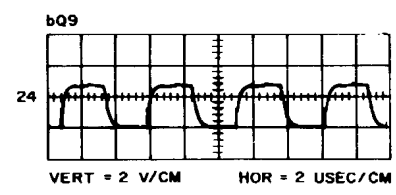


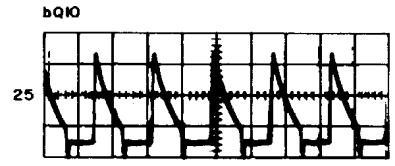


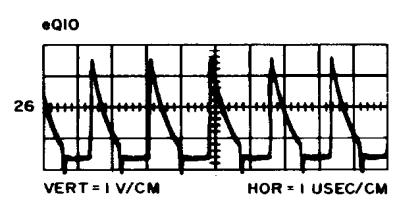


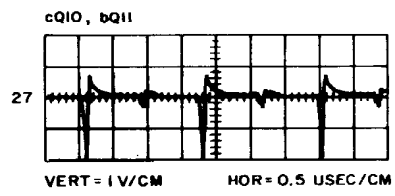






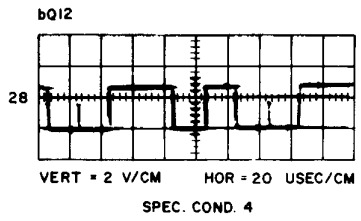


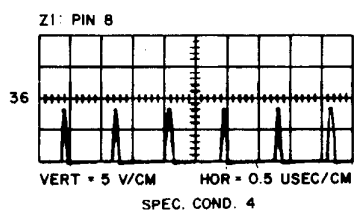


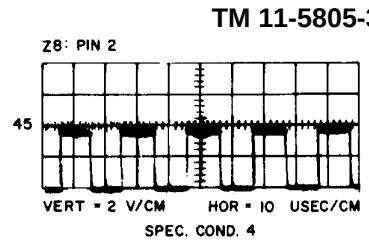


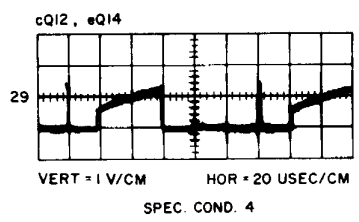
TM5805-367-35/1-63①

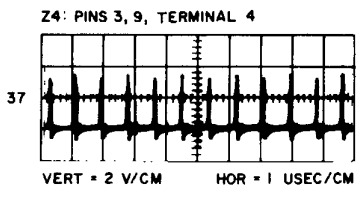
Figure 6-44. Panel 4A6/5A6, waveforms (part 1 of 2).

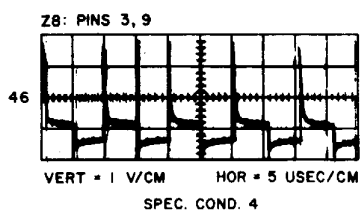


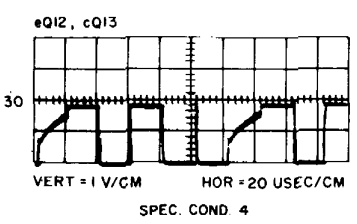


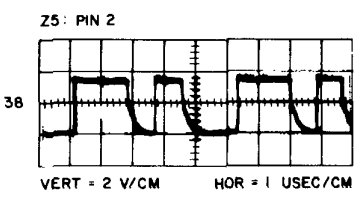


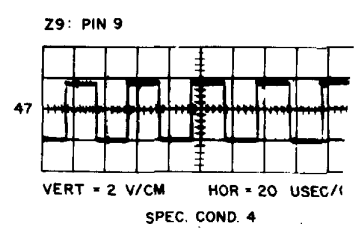


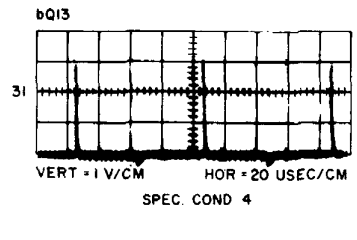


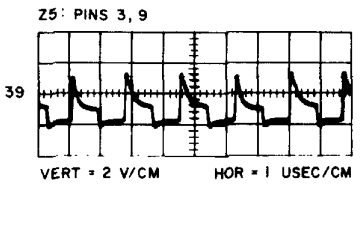


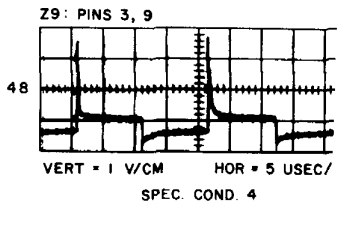


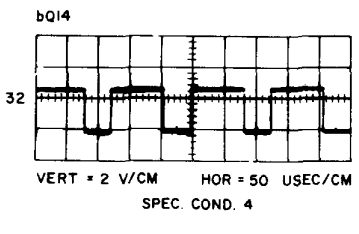


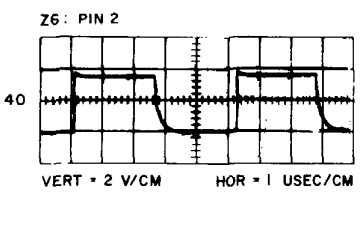


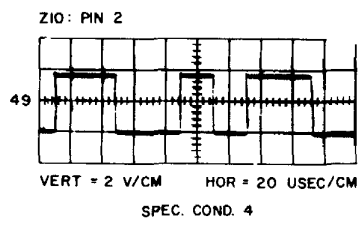


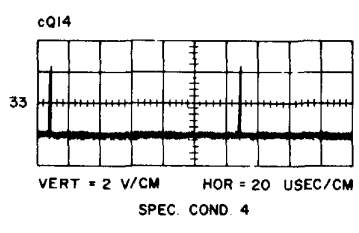


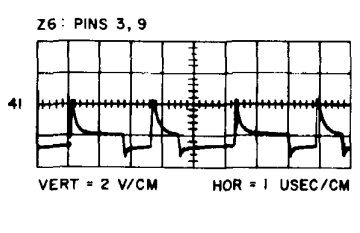


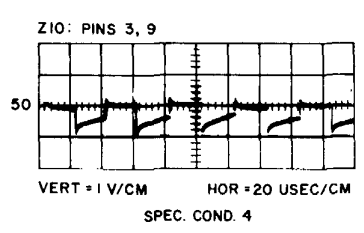


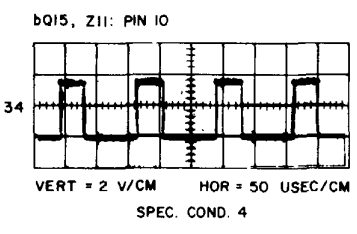


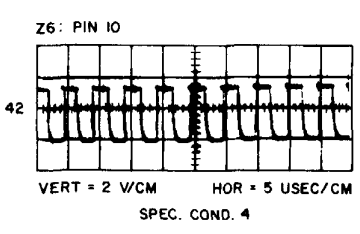


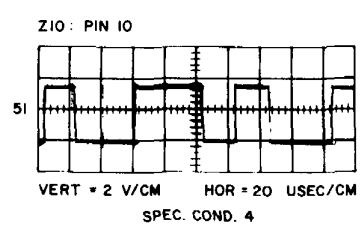


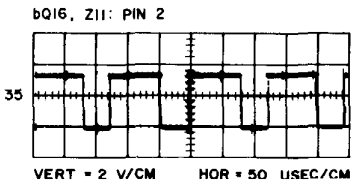


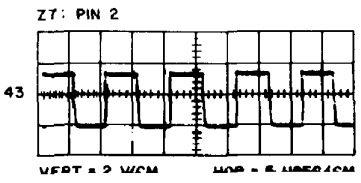


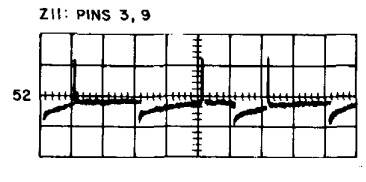






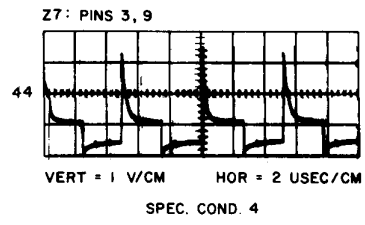






SPEC. COND. 4

SPEC. COND. 4



SPEC. COND. 4

CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOW.

1. TWO TD-352/U MULTIPLEXERS CONNECTED FOR MASTER-SLAVE OPERATION AND INTERCONNECTED WITH TD-202/U AS FOLLOWS USING CG-1040B/U CABLES.

FROM MASTER TD-352/U	TO TD-202/U
PCM OUT	PCM IN-1
TIMING OUT	TIM IN (NOTE 2)
FROM SLAVE TD-352/U	**TO TD-202/U**
PCM OUT	PCM IN-2
FROM MASTER TD-352/U	**TO SLAVE TD-352/U**
SYNC OUT XMTR	SYNC IN
FROM TD-202/U	**TO MASTER TD-352/U**
PCM OUT-1	PCM IN
TIM OUT-1	TIMING IN
FROM TD-202/U	**TO SLAVE TD-352/U**
PCM OUT-2	PCM IN
TIM OUT-2	TIMING IN
FROM TD-202/U	**TO TD-202/U**
TEST OUT	FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, OSCILLOSCOPE SYNCHRONIZED FROM TIM IN SIGNAL INPUT TO TD-202/U. USE OF T CONNECTION ON TIM IN CONNECTOR PROVIDES ACCESS TO THIS 576-KC SIGNAL.

3. UNLESS OTHERWISE NOTED, SWITCHES OPERATED AS FOLLOWS:

TD-352/U	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

TD-202/U	
AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	24I

B. SPECIAL.

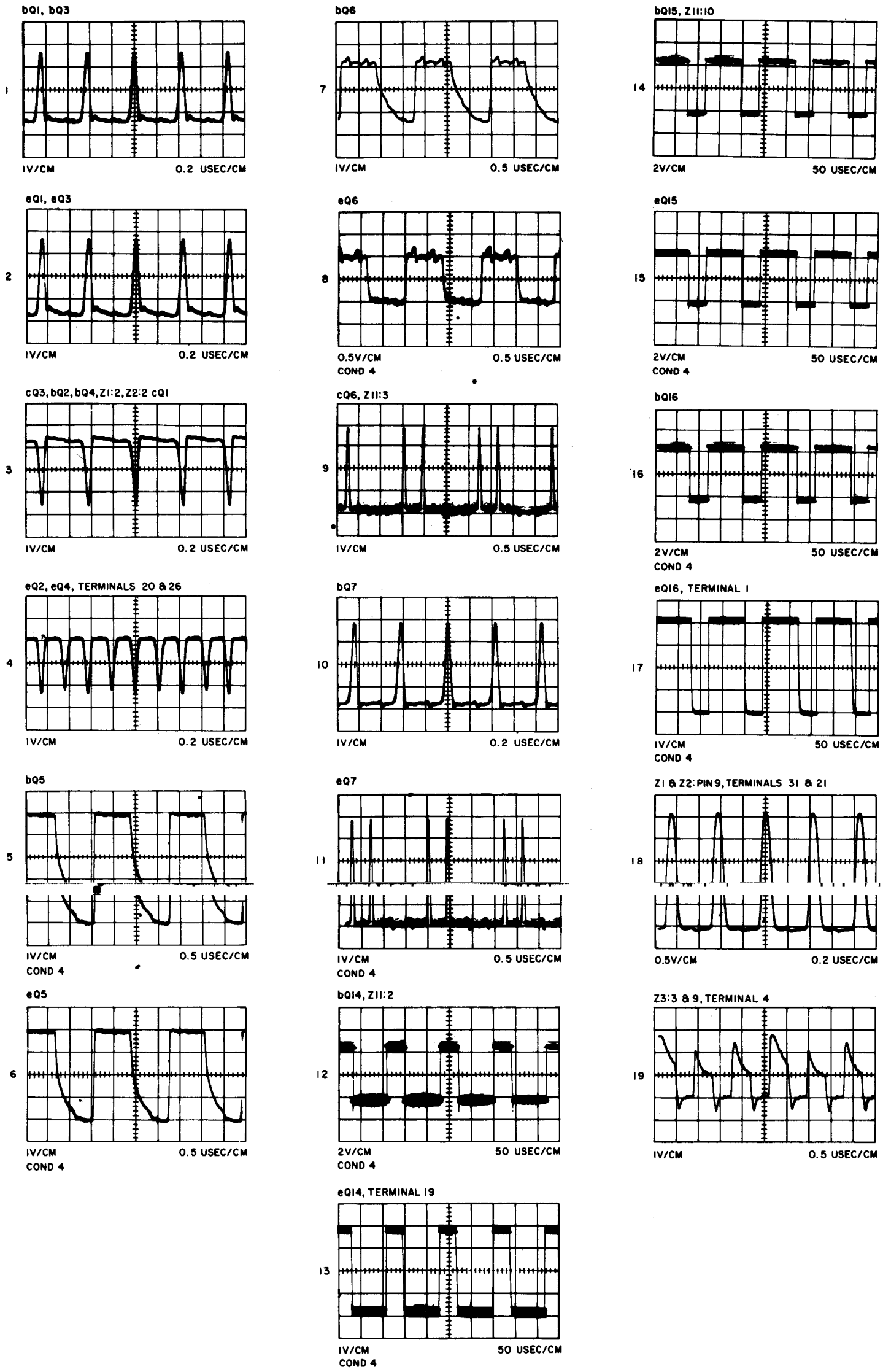
4. SYNCHRONIZE OSCILLOSCOPE FROM SCOPE SYNC OUTPUT OF MASTER TD-352/U.

NOTE

MEDIUM TRAFFIC WAVEFORMS ARE GIVEN FOR THIS PANEL BECAUSE ALL OF THE CIRCUITS ARE USED IN MEDIUM TRAFFIC OPERATION, WHEREAS IN HIGH TRAFFIC OPERATION NOT ALL CIRCUITS ARE USED. IF THE PANEL CHECKS GOOD IN MEDIUM TRAFFIC OPERATION, IT SHOULD OPERATE CORRECTLY IN HIGH TRAFFIC

TM5805-367-35/1-63②

Figure 6-44. Panel 4A6/5A6, waveforms (part 2 of 2).



CONDITIONS FOR OBTAINING WAVEFORMS

NOTES 1, THROUGH 3 GIVEN BELOW ARE APPLICABLE TO ALL WAVE FORMS ON THIS ILLUSTRATION, NOTE-REFERENCES GIVEN WITH WAVEFORMS PERTAIN TO CONDITIONS LISTED BELOW WHICH ARE REQUIRED TO OBTAIN THAT WAVEFORM.

1. INTERCONNECT TWO TD-353/U's WITH THE TEST TD-203/U AS FOLLOWS USING CG-1040B/U CABLE ASSEMBLIES.

MASTER TD-353/U JACKS	TO	TD-203/U JACKS
PCM OUT		PCM IN-1
TIMING OUT		TIM IN (NOTE 2)
PCM IN		PCM OUT-1
TIMING IN		TIM OUT-1
SLAVE TD-353/U JACKS	TO	TD-203/U JACKS
PCM OUT		PCM IN-2
PCM IN		PCM OUT-2
TIMING IN		TIM OUT-2
MASTER TD-353/U JACK	TO	SLAVE TD-353/U JACK
SYNC IN		SYNC OUT XMTR

TD-203/U JACKS

TEST OUT	TO	FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, SYNCHRONIZE AN/USM-140A WITH THE TD-203/U BY CONNECTING AN/USM-140A INPUT JACK TO TD-203/U TIM IN JACK. USE A T CONNECTOR AT TD-203/U TIM IN JACK.

3. UNLESS OTHERWISE NOTED SWITCHES ARE OPERATED AS FOLLOWS:

MASTER AND SLAVE TD-353/U

SWITCH	SETTING	
	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

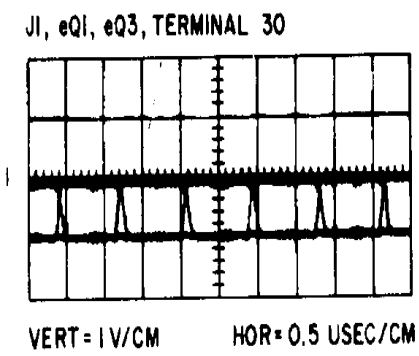
TD-203/U

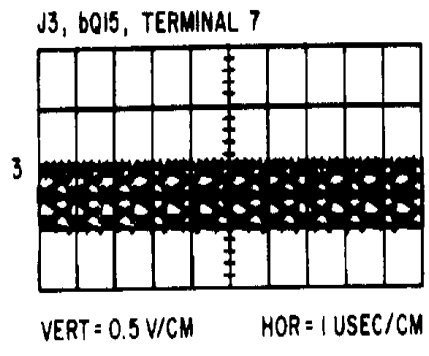
AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	96I

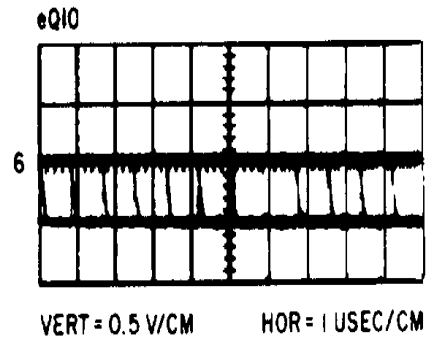
4. SYNCHRONIZE OSCILLOSCOPE FROM SCOPE SYNC OUTPUT OF MASTER TD-353/U.

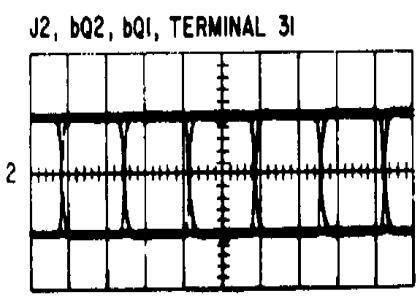
TM5805-367-35/1-C1-23

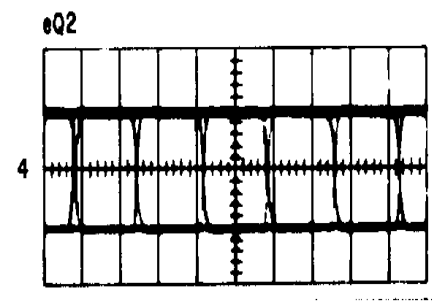
Figure 6-44.1. Panel 4A11, waveforms.

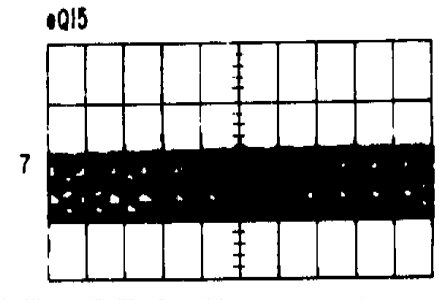


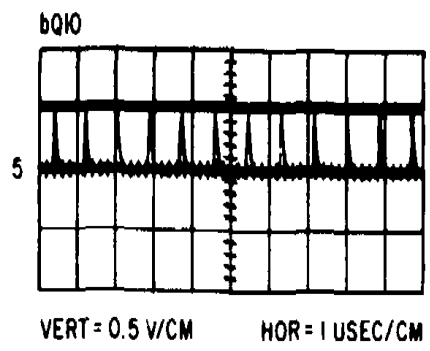












CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

1. TWO TD-352/U MULTIPLEXERS CONNECTED FOR MASTER-SLAVE OPERATION AND INTERCONNECTED WITH TD-202/U AS FOLLOWS USING CG-1040B/U CABLES.

FROM MASTER TD-352/U	TO TD-202/U
PCM OUT	PCM IN-1
TIMING OUT	TIM IN (NOTE 2)
FROM SLAVE TD-352/U	TO TD-202/U
PCM OUT	PCM IN-2
FROM MASTER TD-352/U	TO SLAVE TD-352/U
SYNC OUT XMTR	SYNC IN
FROM TD-202/U	TO MASTER TD-352/U
PCM OUT-1	PCM IN
TIM OUT-1	TIMING IN
FROM TD-202/U	TO SLAVE TD-352/U
PCM OUT-2	PCM IN
TIM OUT-2	TIMING IN
FROM TD-202/U	TO TD-202/U
TEST OUT	FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, OSCILLOSCOPE SYNCHRONIZED FROM TIM IN SIGNAL INPUT TO TD-202/U. USE OF T CONNECTION ON TIM IN CONNECTOR PROVIDES ACCESS TO THIS 576-KC SIGNAL.

3. UNLESS OTHERWISE NOTED, SWITCHES OPERATED AS FOLLOWS:

TD-352/U

	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

TD-202/U

AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	24I

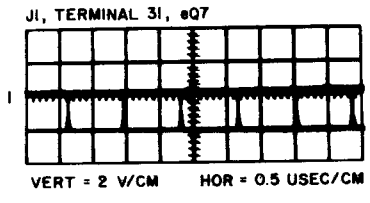
B. SPECIAL.

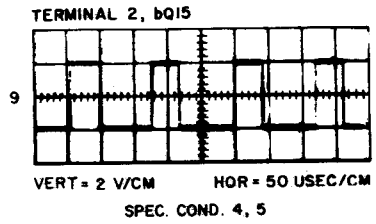
NOTE

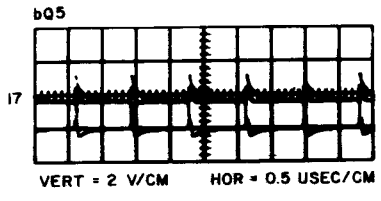
MEDIUM TRAFFIC WAVEFORMS ARE GIVEN FOR THIS PANEL. BECAUSE ALL OF THE CIRCUITS ARE USED IN MEDIUM TRAFFIC OPERATION, WHEREAS IN HIGH TRAFFIC OPERATION NOT ALL CIRCUITS ARE USED. IF THE PANEL CHECKS GOOD IN MEDIUM TRAFFIC OPERATION, IT SHOULD OPERATE CORRECTLY IN HIGH TRAFFIC.

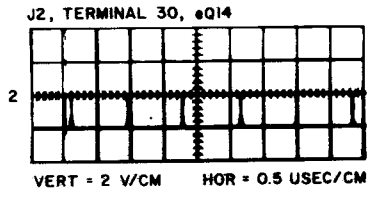
TM5805-367-35/1-64

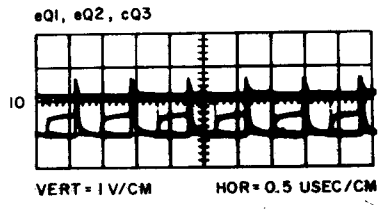
Figure 6-45. Panel 4A7/5A7, waveforms.

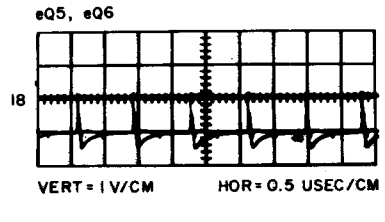


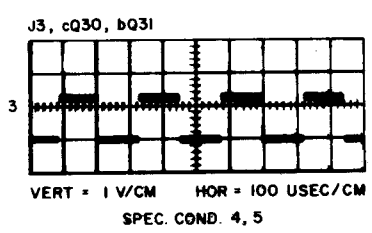


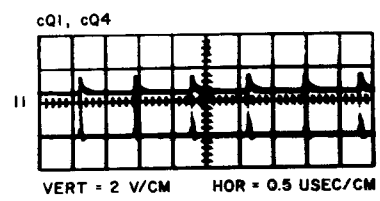


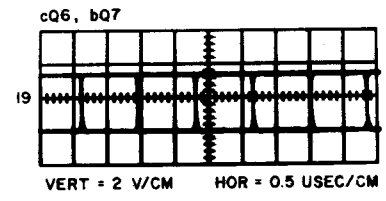


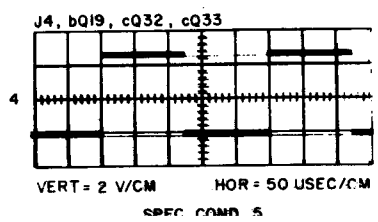


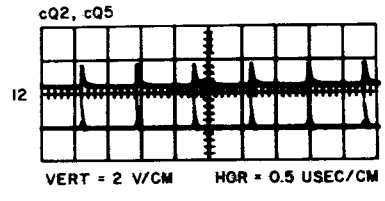


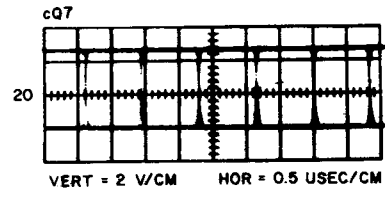


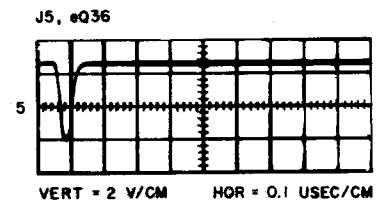


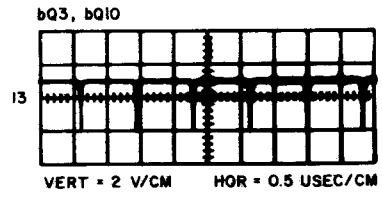


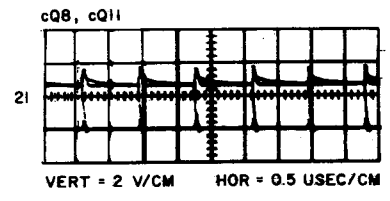


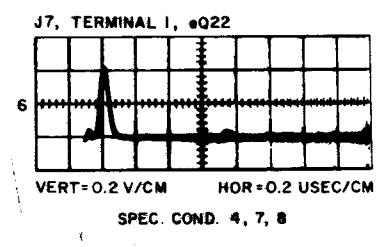


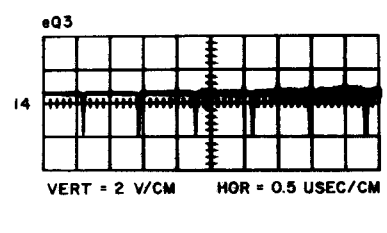


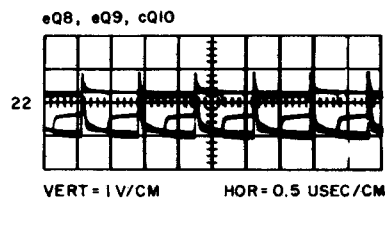


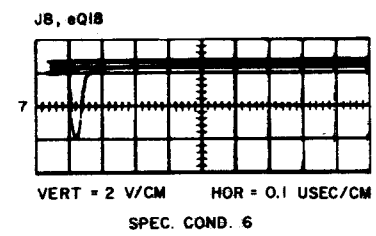


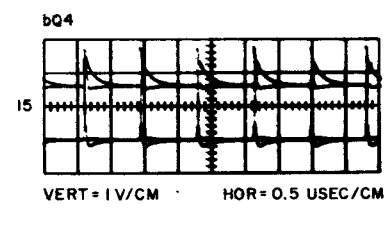


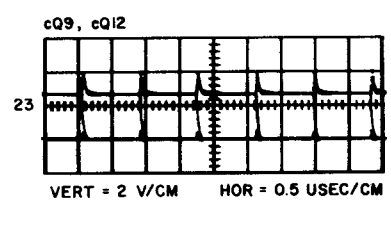


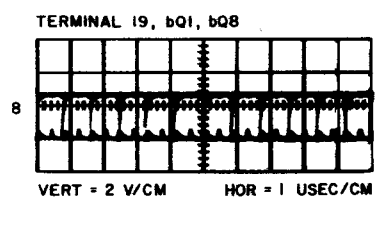


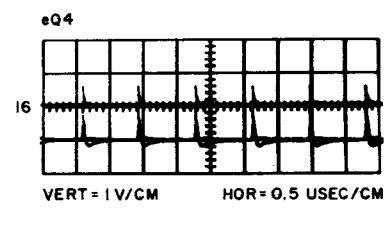












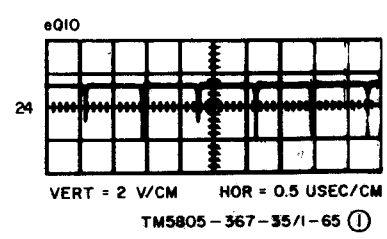
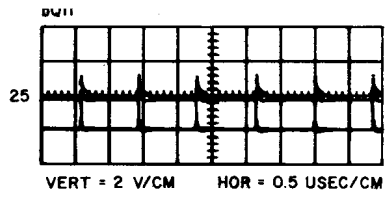
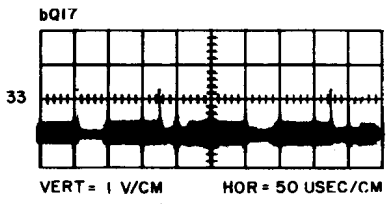
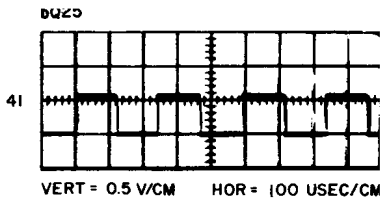
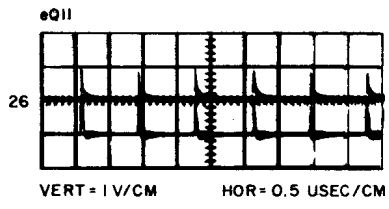


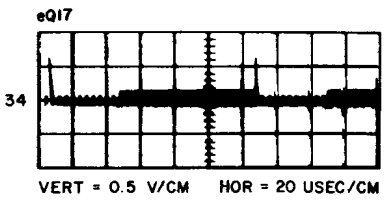
Figure 6-46. Panel 4A8/5A8, waveforms (part 1 of 3).

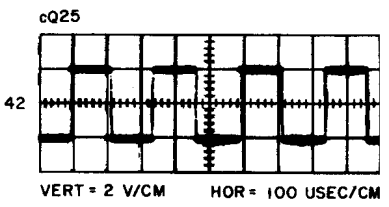


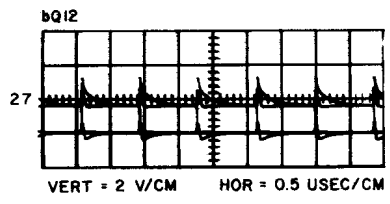


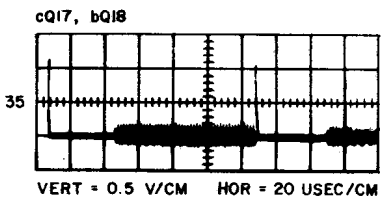


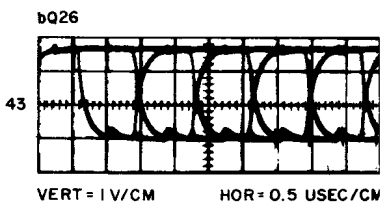


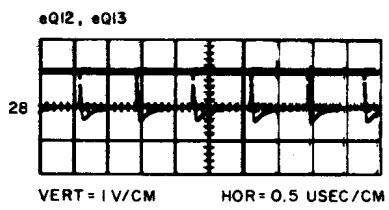


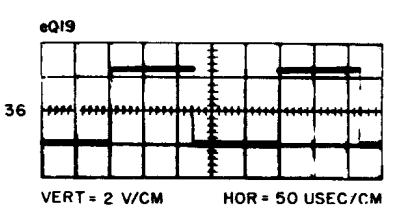


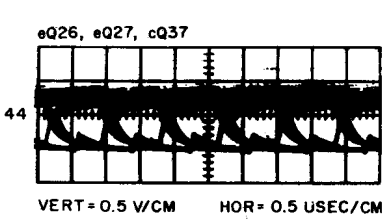


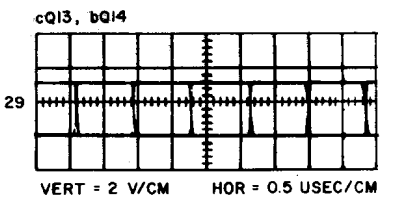


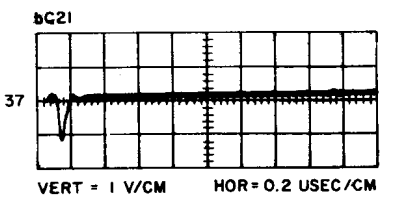


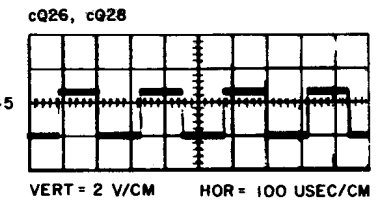


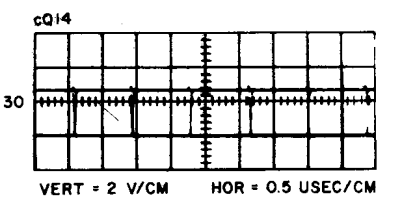


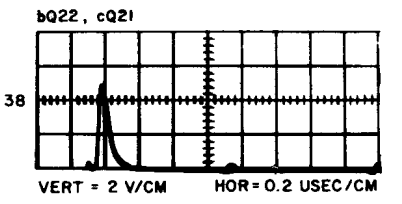


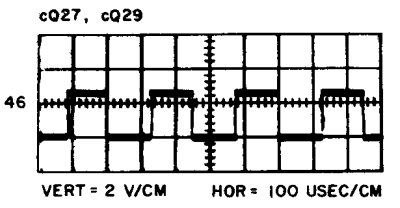


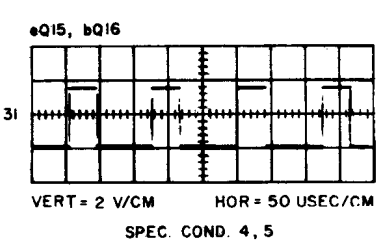


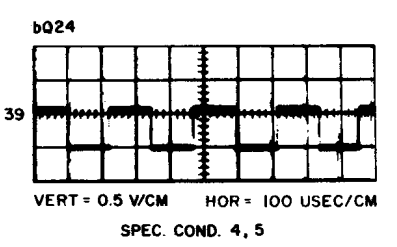


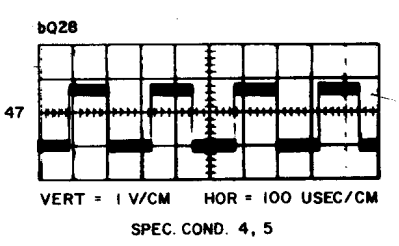


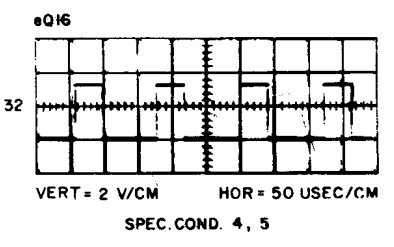


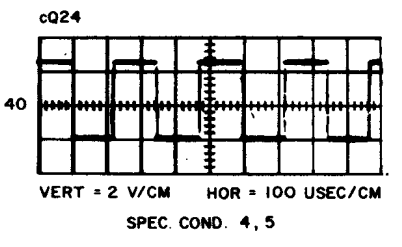












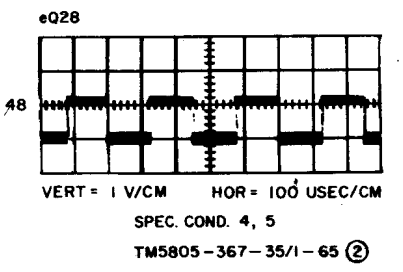
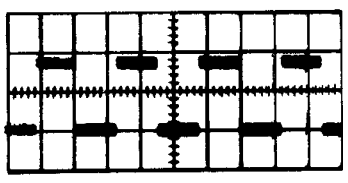


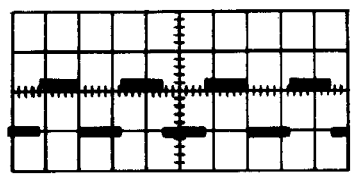
Figure 6-46. Panel 4A8/5A8, waveforms (part 2 of 3).

bQ29



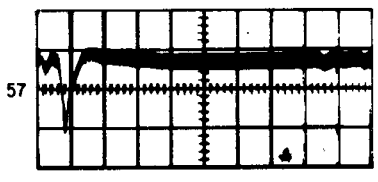
VERT = 1 V/CM HOR = 100 USEC/CM
SPEC. COND. 4, 5

eQ32, eQ34



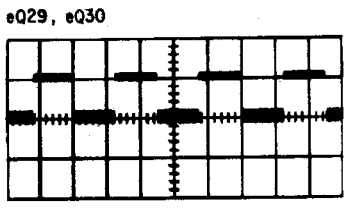
VERT = 1 V/CM HOR = 100 USEC/CM
SPEC. COND. 4, 5

eQ35



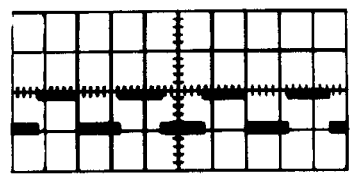
VERT = 0.5 V/CM HOR = 0.1 USEC/CM
SPEC. COND. 6

eQ29, eQ30



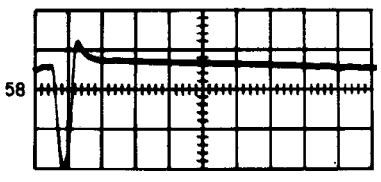
VERT = 1 V/CM HOR = 100 USEC/CM
SPEC. COND. 4, 5

bQ33



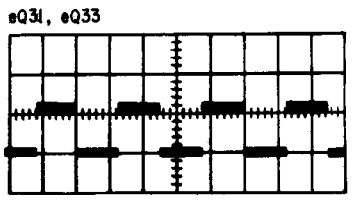
VERT = 1 V/CM HOR = 100 USEC/CM
SPEC. COND. 4, 5

cQ35, bQ36



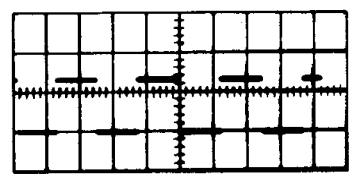
VERT = 1 V/CM HOR = 0.1 USEC/CM
SPEC. COND. 6

eQ31, eQ33



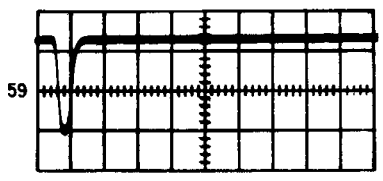
VERT = 1 V/CM HOR = 0.1 USEC/CM
SPEC. COND. 4, 5

bQ34



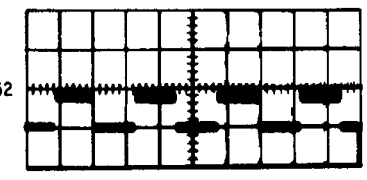
VERT = 1 V/CM HOR = 100 USEC/CM
SPEC. COND. 4, 5

bQ37



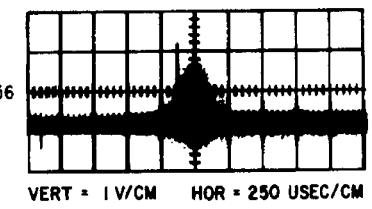
VERT = 2 V/CM HOR = 0.1 USEC/CM
SPEC. COND. 6

bQ33



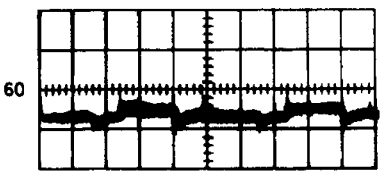
VERT = 1 V/CM HOR = 100 USEC/CM
SPEC. COND. 4, 5

bQ35



VERT = 1 V/CM HOR = 250 USEC/CM
SPEC. COND. 4, 5

CATHODE CR16



VERT = 2 V/CM HOR = 50 USEC/CM

CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TWO TD-352/U MULTIPLEXERS CONNECTED FOR MASTER-SLAVE OPERATION AND INTERCONNECTED WITH TD-202/U AS FOLLOWS USING CG-1040B/U CABLES.

FROM MASTER TD-352/U	TO TD-202/U
PCM OUT	PCM IN-1
TIMING OUT	TIM IN (NOTE 2)
FROM SLAVE TD-352/U	TO TD-202/U
PCM OUT	PCM IN-2
FROM MASTER TD-352/U	TO SLAVE TD-352/U
SYNC OUT XMTR	SYNC IN
FROM TD-202/U	TO MASTER TD-352/U
PCM OUT-1	PCM IN
TIM OUT-1	TIMING IN
FROM TD-202/U	TO SLAVE TD-352/U
PCM OUT-2	PCM IN
TIM OUT-2	TIMING IN
FROM TD-202/U	TO TD-202/U
TEST OUT	FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, OSCILLOSCOPE SYNCHRONIZED FROM TIM IN SIGNAL INPUT TO TD-202/U. USE OF T CONNECTION ON TIM IN CONNECTOR PROVIDES ACCESS TO THIS 576-KC SIGNAL.

3. UNLESS OTHERWISE NOTED, SWITCHES OPERATED AS FOLLOWS:

	TD-352/U	
	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

	TD-202/U
AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	24I

B. SPECIAL.

4. OPERATE TRAFFIC SEL SWITCH TO 24S.

5. SYNCHRONIZE OSCILLOSCOPE FROM SCOPE SYNC OUTPUT OF MASTER TD-352/U

6. OPERATE OSCILLOSCOPE ON NEGATIVE INTERNAL SYNCHRONIZATION.

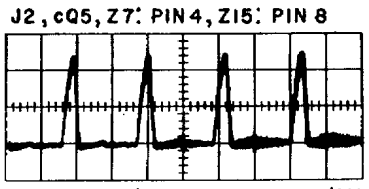
7. OPERATE OSCILLOSCOPE ON POSITIVE INTERNAL SYNCHRONIZATION.

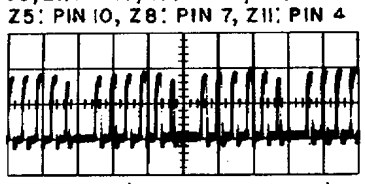
8. OPERATE MASTER TD-352/U ADDRESS SWITCH TO SLAVE (PROVIDES OUT-OF-FRAME CONDITION AS REQUIRED TO GENERATE SKIP PULSE IN TD-202/U).

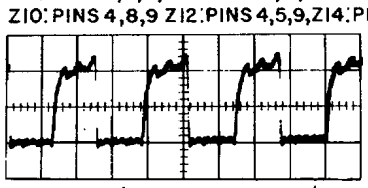
NOTE

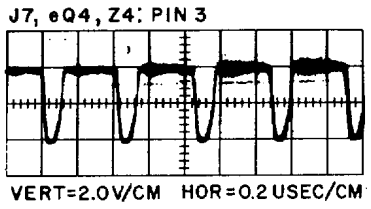
MEDIUM TRAFFIC WAVEFORMS ARE GIVEN FOR THIS PANEL BECAUSE ALL OF THE CIRCUITS ARE USED IN MEDIUM TRAFFIC OPERATION, WHEREAS IN HIGH TRAFFIC OPERATION NOT ALL CIRCUITS ARE USED. IF THE PANEL CHECKS GOOD IN MEDIUM TRAFFIC OPERATION, IT SHOULD OPERATE CORRECTLY IN HIGH TRAFFIC.

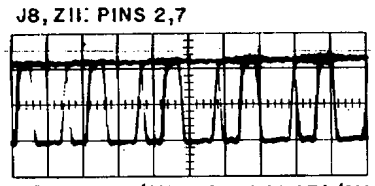
Figure 6-46. Panel 4A8/5A8, waveforms (part 3 of 3).

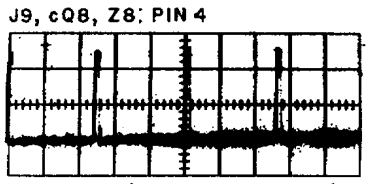
1 J2, cQ5, Z7: PIN 4, Z15: PIN 8

VERT=2.0V/CM HOR=0.2USEC/CM

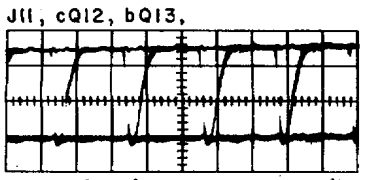
2 J3, Z1: PIN 10, Z2: PIN 10, Z3: PIN 10 Z5: PIN 10, Z8: PIN 7, Z11: PIN 4

VERT=2.0V/CM HOR=1.0USEC/CM
SPEC. COND. 9 AND 10

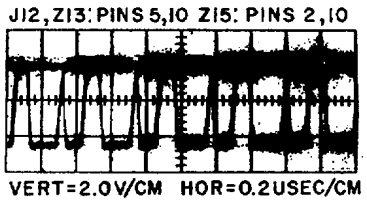
3 J4, J5, J6, Z1: PINS 8,9, Z2: PINS 2,8, Z3: PINS 2,3,8, Z6: PINS 3,4, Z8: PIN 8 Z10: PINS 4,8,9 Z12: PINS 4,5,9, Z14: PIN 5

VERT=2.0V/CM HOR=1.0USEC/CM
SPEC. COND. 4

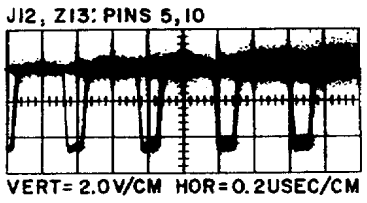
4 J7, eQ4, Z4: PIN 3

VERT=2.0V/CM HOR=0.2USEC/CM

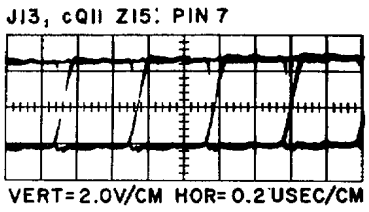
5 J8, Z11: PINS 2,7

VERT=2.0V/CM HOR=0.2USEC/CM

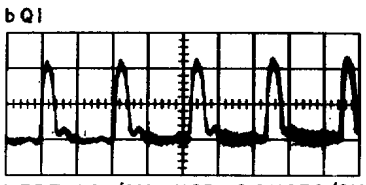
6 J9, cQ8, Z8: PIN 4

VERT=2.0V/CM HOR=0.2USEC/CM
SPEC. COND. 4

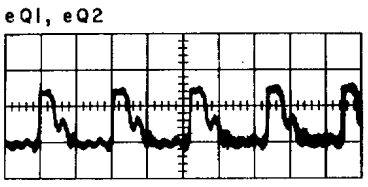
7 J11, cQ12, bQ13,

VERT 2.0V/CM HOR=0.2USEC/CM

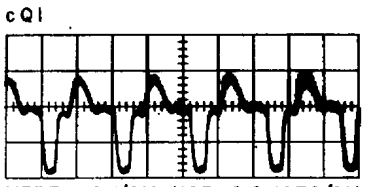
8 J12, Z13: PINS 5,10 Z15: PINS 2,10

VERT=2.0V/CM HOR=0.2USEC/CM

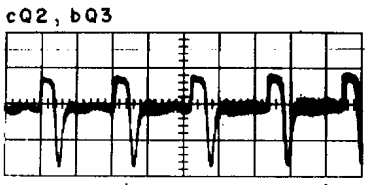
9 J12, Z13: PINS 5,10

VERT= 2.0V/CM HOR=0.2USEC/CM
SPEC. CON 8

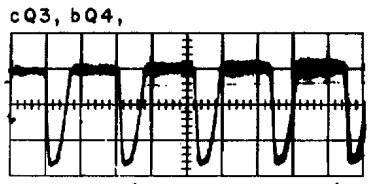
10 J13, cQ11 Z15: PIN 7

VERT=2.0V/CM HOR=0.2USEC/CM

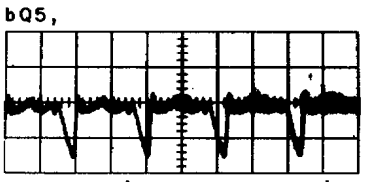
11 bQ1

VERT=1.0V/CM HOR=0.2USEC/CM

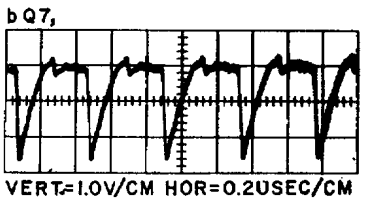
12 eQ1, eQ2

VERT=0.5V/CM HOR=0.2USEC/CM

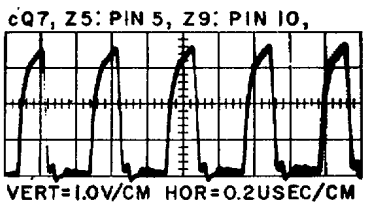
13 cQ1

VERT=1.0V/CM HOR=0.2USEC/CM

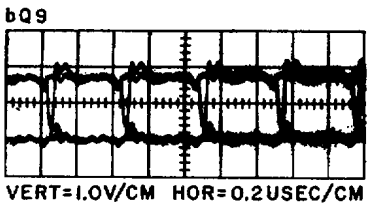
14 cQ2, bQ3

VERT=1.0V/CM HOR=0.2USEC/CM

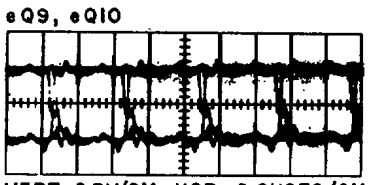
15 cQ3, bQ4,

VERT=2.0V/CM HOR=0.2USEC/CM

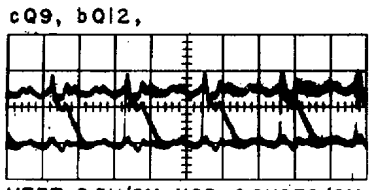
16 bQ5,

VERT=0.5V/CM HOR=0.2USEC/CM

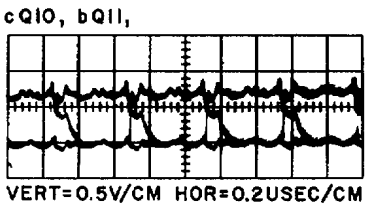
17 bQ7,

VERT=1.0V/CM HOR=0.2USEC/CM

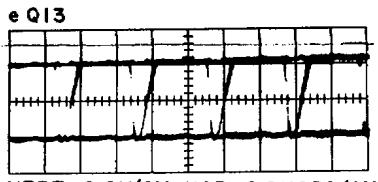
18 cQ7, Z5: PIN 5, Z9: PIN 10,

VERT=1.0V/CM HOR=0.2USEC/CM

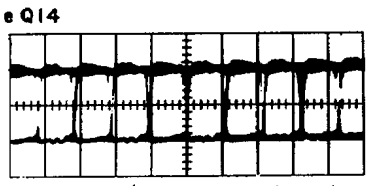
19 bQ9

VERT=1.0V/CM HOR=0.2USEC/CM

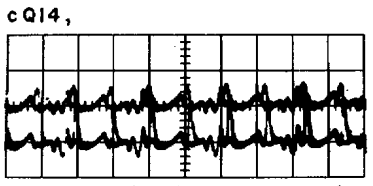
20 eQ9, eQ10

VERT=0.5V/CM HOR=0.2USEC/CM

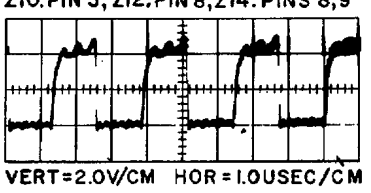
21 cQ9, bQ12,

VERT=0.5V/CM HOR=0.2USEC/CM

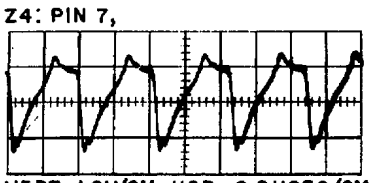
22 cQ10, bQ11,

VERT=0.5V/CM HOR=0.2USEC/CM

23 eQ13

VERT=2.0V/CM HOR=0.2USEC/CM

24 eQ14

VERT=2.0V/CM HOR=0.2USEC/CM
SPEC. COND. 5

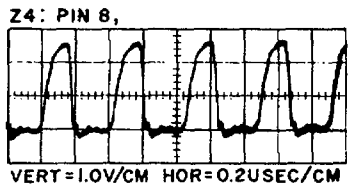
25 cQ14,

VERT=0.5V/CM HOR=0.2USEC/CM
SPEC. COND. 5

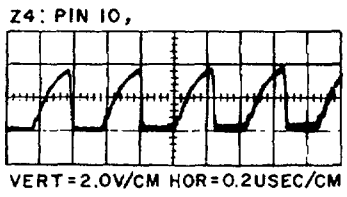
26 Z1: PIN 3, Z2: PIN 3, Z3: PIN 9, Z8: PIN 9, Z10: PIN 5, Z12: PIN 8, Z14: PINS 8,9

VERT=2.0V/CM HOR=1.0USEC/CM
SPEC. COND. 4

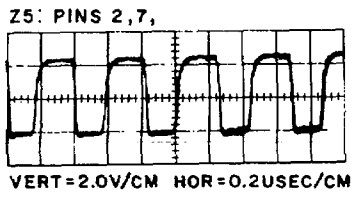
27 Z4: PIN 7,

VERT=1.0V/CM HOR=0.2USEC/CM

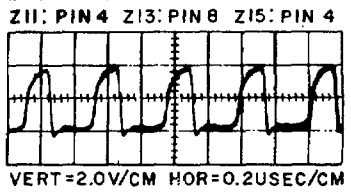
TM5805-367-35/1-C1-17①

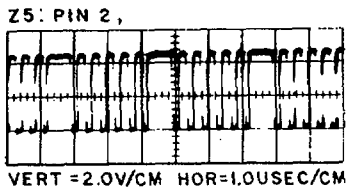
Figure 6-47. Panel 4A2, waveforms (pat 1 of 2).

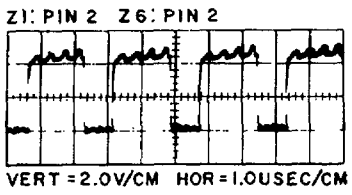
28 Z4: PIN 8,

VERT=1.0V/CM HOR=0.2USEC/CM

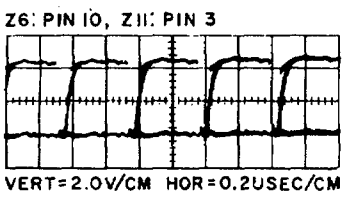
29 Z4: PIN 10,

VERT=2.0V/CM HOR=0.2USEC/CM

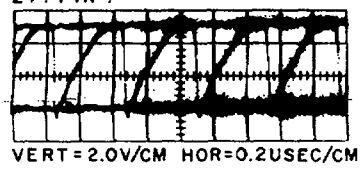
30 Z5: PINS 2,7,

VERT=2.0V/CM HOR=0.2USEC/CM

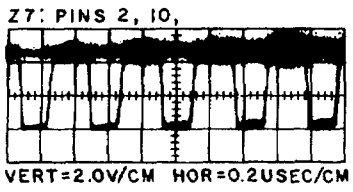
31 Z3: PIN 10 Z5: PIN 10 Z7: PIN 8
Z11: PIN 4 Z13: PIN 8 Z15: PIN 4

VERT=2.0V/CM HOR=0.2USEC/CM

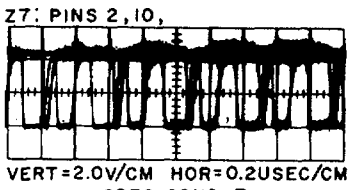
32 Z5: PIN 2,

VERT=2.0V/CM HOR=1.0USEC/CM
SPEC. COND. 9 AND 10

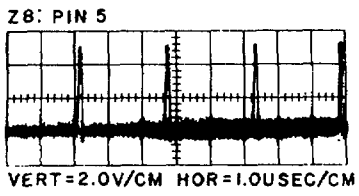
33 Z1: PIN 2 Z6: PIN 2

VERT=2.0V/CM HOR=1.0USEC/CM
SPEC. COND. 4

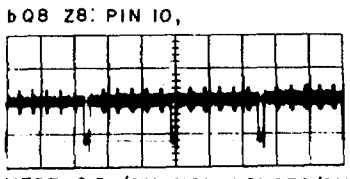
34 Z6: PIN 10, Z11: PIN 3

VERT=2.0V/CM HOR=0.2USEC/CM

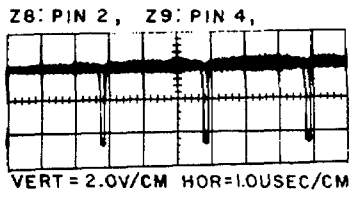
35 Z7: PIN 7

VERT=2.0V/CM HOR=0.2USEC/CM

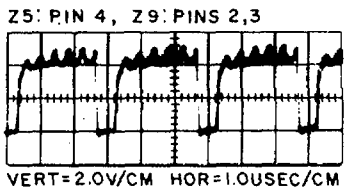
36 Z7: PINS 2, 10,

VERT=2.0V/CM HOR=0.2USEC/CM
SPEC. COND. 6

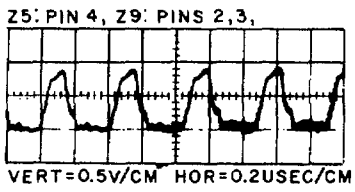
37 Z7: PINS 2,10,

VERT=2.0V/CM HOR=0.2USEC/CM
SPEC. COND. 7
(NOTE WAVEFORM 37 MAY BE SAME AS WAVEFORM 5)

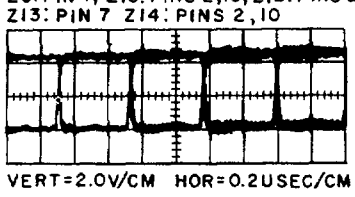
38 Z8: PIN 5

VERT=2.0V/CM HOR=1.0USEC/CM
SPEC. COND. 4

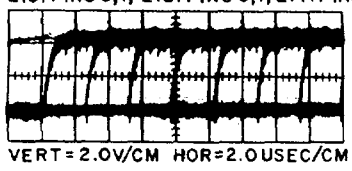
39 bQ8 Z8: PIN 10,

VERT=0.5V/CM HOR=1.0USEC/CM
SPEC. COND. 4

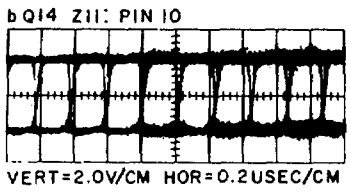
40 Z8: PIN 2, Z9: PIN 4,

VERT=2.0V/CM HOR=1.0USEC/CM
SPEC. COND. 9 AND 4

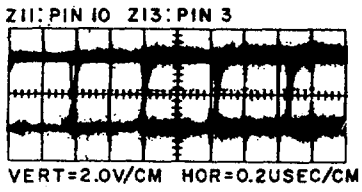
41 Z5: PIN 4, Z9: PINS 2,3

VERT=2.0V/CM HOR=1.0USEC/CM
SPEC. COND. 9 AND 4

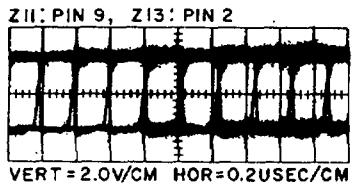
42 Z5: PIN 4, Z9: PINS 2,3,

VERT=0.5V/CM HOR=0.2USEC/CM

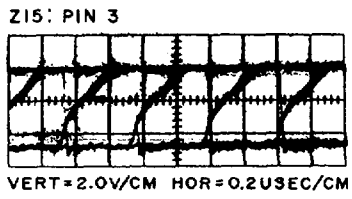
43 Z6: PIN 7, Z10: PINS 2,10, Z12: PINS 2,10
Z13: PIN 7 Z14: PINS 2,10

VERT=2.0V/CM HOR=0.2USEC/CM

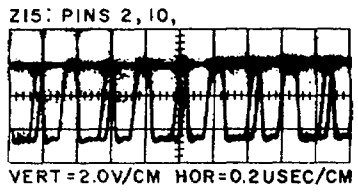
44 Z10: PINS 3,7, Z12: PINS 3,7, Z14: PINS 3,7

VERT=2.0V/CM HOR=2.0USEC/CM
SPEC. COND. 4

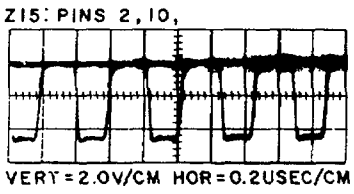
45 bQ14 Z11: PIN 10

VERT=2.0V/CM HOR=0.2USEC/CM

46 Z11: PIN 10 Z13: PIN 3

VERT=2.0V/CM HOR=0.2USEC/CM
SPEC. COND. 8

47 Z11: PIN 9, Z13: PIN 2

VERT=2.0V/CM HOR=0.2USEC/CM

48 Z15: PIN 3

VERT=2.0V/CM HOR=0.2USEC/CM

49 Z15: PINS 2,10,

VERT=2.0V/CM HOR=0.2USEC/CM
SPEC. COND. 7

50 Z15: PINS 2,10,

VERT=2.0V/CM HOR=0.2USEC/CM
SPEC. COND. 6

CONDITIONS FOR OBTAINING WAVEFORMS

NOTES 1, THROUGH 3 GIVEN BELOW ARE APPLICABLE TO ALL WAVE FORMS ON THIS ILLUSTRATION, NOTE-REFERENCES GIVEN WITH WAVEFORMS PERTAIN TO CONDITIONS LISTED BELOW WHICH ARE REQUIRED TO OBTAIN THAT WAVEFORM.

1. INTERCONNECT TWO TD-353/U's WITH THE TEST TD-203/U AS FOLLOWS USING CG-1040B/U CABLE ASSEMBLIES.

MASTER TD-353/U JACKS	TO	TD-203/U JACKS
PCM OUT		PCM IN-1
TIMING OUT		TIM IN (NOTE 2)
PCM IN		PCM OUT-1
TIMING IN		TIM OUT-1

SLAVE TD-353/U JACKS	TO	TD-203/U JACKS
PCM OUT		PCM IN-2
PCM IN		PCM OUT-2
TIMING IN		TIM OUT-2
TIMING OUT		TIM IN-2

MASTER TD-353/U JACK	TO	SLAVE TD-353/U JACK
SYNC IN		SYNC OUT XMTR

TD-203/U JACKS

TEST OUT TO FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, SYNCHRONIZE AN/USM-140A WITH THE TD-203/U BY CONNECTING AN/USM-140A INPUT JACK TO TD-203/U TIM IN-1 JACK. USE A T CONNECTOR AT TD-203/U TIM IN-1 JACK.

3. UNLESS OTHERWISE NOTED SWITCHES ARE OPERATED AS FOLLOWS:

MASTER AND SLAVE TD-353/U

SWITCH	SETTING	
	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

TD-203/U

AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	96I

4. USE INTERNAL SYNC.

5. OPERATE OPR-TEST SWITCH TO TEST.

6. REMOVE PCM IN-1 CONNECTOR. RECONNECT AFTER OBSERVING WAVEFORM.

7. OPERATE TRAFFIC SEL SWITCH TO 96R. OPERATE BACK TO 96I AFTER OBSERVING WAVEFORM.

8. OPERATE TRAFFIC SEL SWITCH TO 48. OPERATE BACK TO 96I AFTER OBSERVING WAVEFORM.

9. REMOVE PANEL 4A10. CONNECT PANEL 4A2 TERMINAL 19 TO 4.5V.

CAUTION

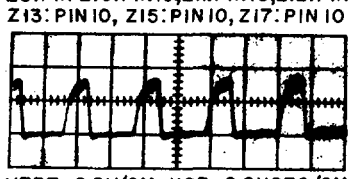
REMOVE TERMINAL 19 CONNECTION BEFORE REPLACING PANEL 4A10.

10. WAVEFORM SHOULD SHOW A DELETED PULSE - IF THIS IS NOT OBSERVED THE SCOPE SWEEP LENGTH MAY HAVE TO BE ADJUSTED.

TM5805-367-35/1-C1-17②

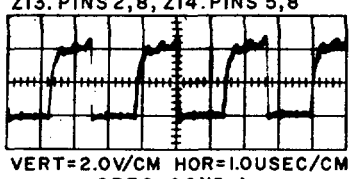
Figure 6-47. Panel 4A2, waveforms sheet 2 of 2).

1
J1, Z2: PIN 10, Z5: PIN 10, Z6: PIN 2, Z8: PIN Z10: PIN 10, Z11: PIN 10, Z12: PIN 10 Z13: PIN 10, Z15: PIN 10, Z17: PIN 10



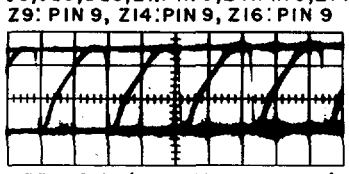
VERT = 0.2V/CM HOR = 0.2USEC/CM

2
J2, J8, J9, Z1: PINS 4,7, Z3: PINS 3,4, Z4: PINS 4,7, Z7: PINS (4,7), (5,8), Z9: PINS 5,8, Z11: PINS 8,9, Z12: PINS 2,8, Z13: PINS 2,8, Z14: PINS 5,8



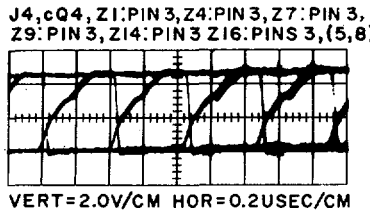
VERT = 2.0V/CM HOR = 1.0USEC/CM
SPEC. COND. 4

3
J3, cQ3, bQ5, Z1: PIN 9, Z4: PIN 9, Z7 PIN 9, Z9: PIN 9, Z14: PIN 9, Z16: PIN 9



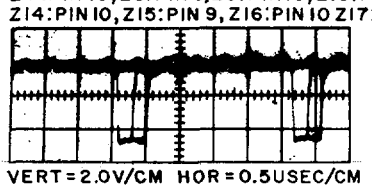
VERT = 2.0V/CM HOR = 0.2USEC/CM

4
J4, cQ4, Z1: PIN 3, Z4: PIN 3, Z7: PIN 3, Z9: PIN 3, Z14: PIN 3 Z16: PINS 3, (5,8)



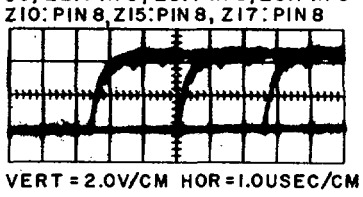
VERT = 2.0V/CM HOR = 0.2USEC/CM

5
J5, Z1: PIN 10, Z2: PIN 9, Z4: PIN 10, Z5: PIN 9, Z7: PIN 10, Z8: PIN 9, Z9: PIN 10, Z10: PIN 9, Z14: PIN 10, Z15: PIN 9, Z16: PIN 10 Z17: PIN 9.



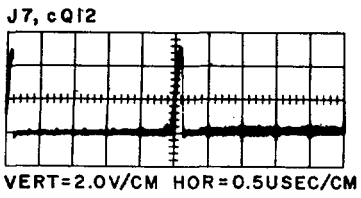
VERT = 2.0V/CM HOR = 0.5USEC/CM
SPEC. COND. 4

6
J6, Z2: PIN 8, Z5: PIN 8, Z8: PIN 8 Z10: PIN 8, Z15: PIN 8, Z17: PIN 8



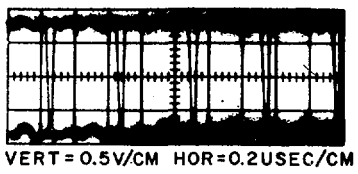
VERT = 2.0V/CM HOR = 1.0USEC/CM
SPEC. COND. 4

7
J7, cQ12



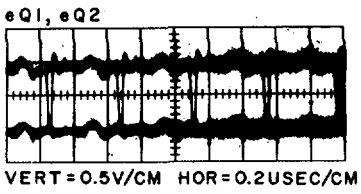
VERT = 2.0V/CM HOR = 0.5USEC/CM
SPEC. COND. 4

8
bQ1



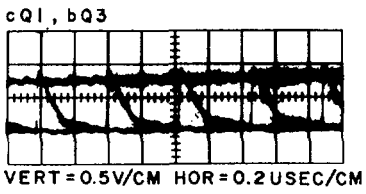
VERT = 0.5V/CM HOR = 0.2USEC/CM

9
eQ1, eQ2



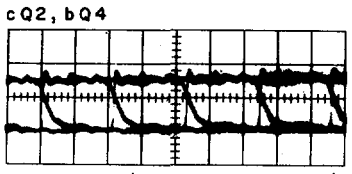
VERT = 0.5V/CM HOR = 0.2USEC/CM

10
cQ1, bQ3



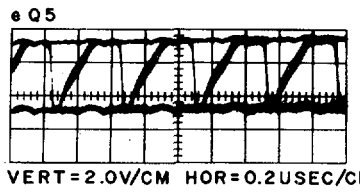
VERT = 0.5V/CM HOR = 0.2USEC/CM

11
cQ2, bQ4



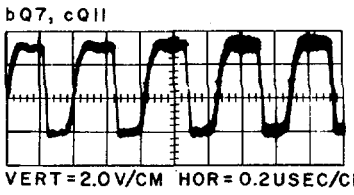
VERT = 0.5V/CM HOR = 0.2USEC/CM

12
eQ5



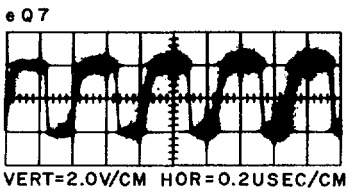
VERT = 2.0V/CM HOR = 0.2USEC/CM

13
bQ7, cQ11



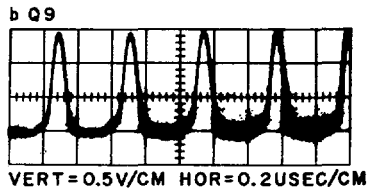
VERT = 2.0V/CM HOR = 0.2USEC/CM

14
eQ7



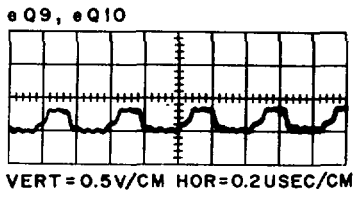
VERT = 2.0V/CM HOR = 0.2USEC/CM

15
bQ9



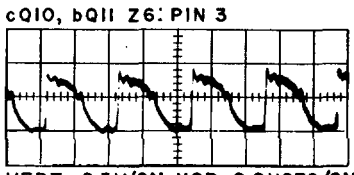
VERT = 0.5V/CM HOR = 0.2USEC/CM

16
eQ9, eQ10



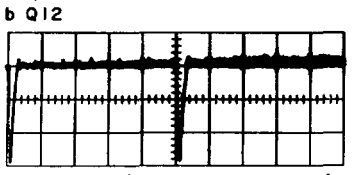
VERT = 0.5V/CM HOR = 0.2USEC/CM

17
cQ10, bQ11 Z6: PIN 3



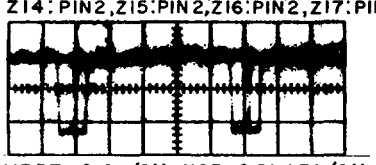
VERT = 0.5V/CM HOR = 0.2USEC/CM

18
bQ12



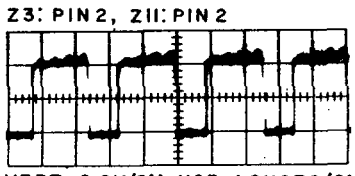
VERT = 1.0V/CM HOR = 0.5USEC/CM
SPEC. COND. 4

19
Z1: PIN 2, Z2: PIN 2, Z4: PIN 2, Z5: PIN 2 Z7: PIN 2, Z8: PIN 2, Z9: PIN 2, Z10: PIN 2 Z14: PIN 2, Z15: PIN 2, Z16: PIN 2, Z17: PIN 2



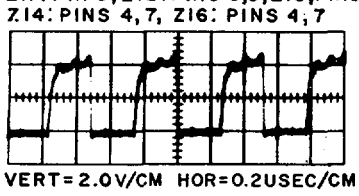
VERT = 2.0V/CM HOR = 0.5USEC/CM
SPEC. COND. 4

20
Z3: PIN 2, Z11: PIN 2



VERT = 2.0V/CM HOR = 1.0USEC/CM
SPEC. COND. 4

21
Z1: PINS 5,8, Z4: PINS 5,8, Z9: PINS 4,7, Z11: PIN 3, Z12: PINS 3,9, Z13, PINS 3,9, Z14: PINS 4,7, Z16: PINS 4,7



VERT = 2.0V/CM HOR = 0.2USEC/CM
SPEC. COND. 4

CONDITIONS FOR OBTAINING WAVEFORMS

NOTES 1, THROUGH 3 GIVEN BELOW ARE APPLICABLE TO ALL WAVE FORMS ON THIS ILLUSTRATION, NOTE-REFERENCES GIVEN WITH WAVEFORMS PERTAIN TO CONDITIONS LISTED BELOW WHICH ARE REQUIRED TO OBTAIN THAT WAVEFORM.

1. INTERCONNECT TWO TD-353/U's WITH THE TEST TD-203/U AS FOLLOWS USING CG-1040B/U CABLE ASSEMBLIES.

MASTER TD-353/U JACKS	TO	TD-203/U JACKS
PCM OUT		PCM IN-1
TIMING OUT		TIM IN (NOTE 2)
PCM IN		PCM OUT-1
TIMING IN		TIM OUT-1
SLAVE TD-353/U JACKS	**TO**	**TD-203/U JACKS**
PCM OUT		PCM IN-2
PCM IN		PCM OUT-2
TIMING IN		TIM OUT-2
TIMING OUT		TIM IN-2

MASTER TD-353/U JACK	TO	SLAVE TD-353/U JACK
SYNC IN		SYNC OUT XMTR

TD-203/U JACKS

TEST OUT TO FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, SYNCHRONIZE AN/USM-140A WITH THE TD-203/U BY CONNECTING AN/USM-140A INPUT JACK TO TD-203/U TIM IN-JACK. USE A T CONNECTOR AT TD-203/U TIM IN-JACK.

3. UNLESS OTHERWISE NOTED SWITCHES ARE OPERATED AS FOLLOWS:

MASTER AND SLAVE TD-353/U

SWITCH	SETTING	
	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

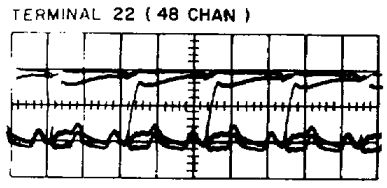
TD-203/U

AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	96I

4. USE INTERNAL SYNC.

Figure 6-47.1. Panel 4A10 waveforms.

TERMINAL 22 (48 CHAN)

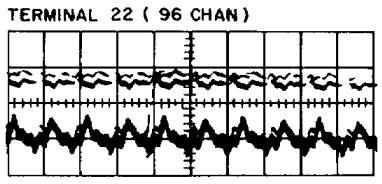


VERT = 1 V/CM HOR = 0.2 USEC/CM

COND. 4

TERMINAL 22 (96 CHAN)

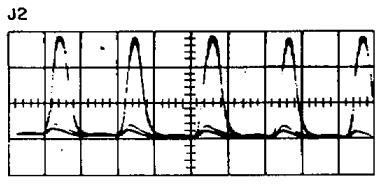
2



VERT = 1 V/CM HOR = 0.2 USEC/CM

J2

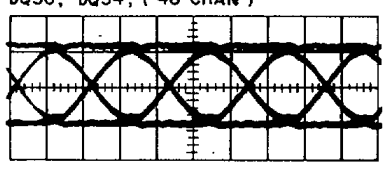
3



VERT = 1 V/CM HOR = 0.1 USEC/CM

J3, TERMINAL 9, bQ8, bQ28
bQ30, bQ34, (48 CHAN)

4

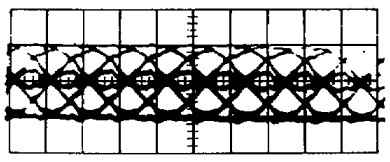


VERT = 1 V/CM HOR = 0.2 USEC/CM

COND. 4

J3, TERMINAL 9, bQ8, bQ28
bQ30, bQ34, (96 CHAN)

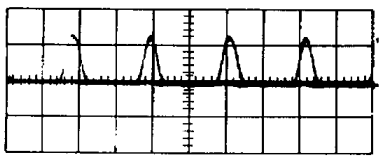
5



VERT = 1 V/CM HOR = 0.2 USEC/CM

J4

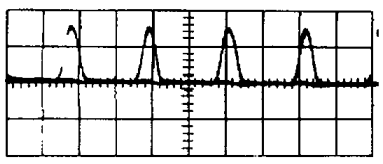
6



VERT = 1 V/CM HOR = 0.2 USEC/CM

J6

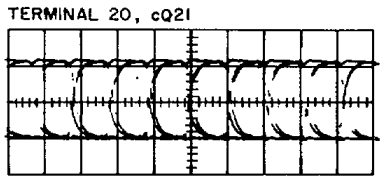
7



VERT = 2 V/CM HOR = 0.1 USEC/CM

TERMINAL 20, cQ21

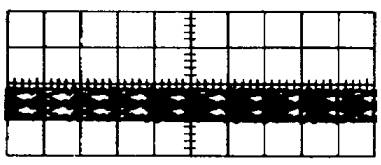
8



VERT = 2 V/CM HOR = 0.2 USEC/CM

bQ1

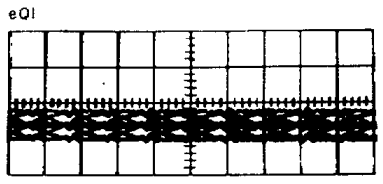
9



VERT = 0.5 V/CM HOR = 0.2 USEC/CM

eQ1

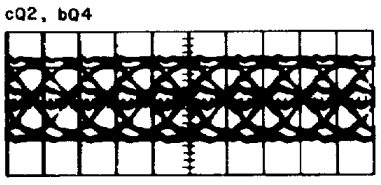
10



VERT = 0.5 V/CM HOR = 0.2 USEC/CM

cQ2, bQ4

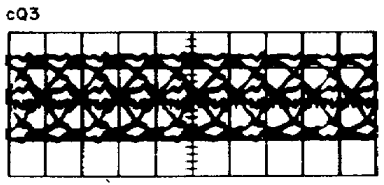
11



VERT = 1 V/CM HOR = 0.2 USEC/CM

cQ3

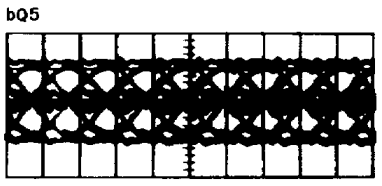
12



VERT = 1 V/CM HOR = 0.2 USEC/CM

bQ5

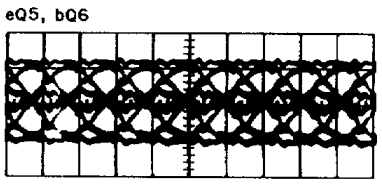
13



VERT = 1 V/CM HOR = 0.2 USEC/CM

eQ5, bQ6

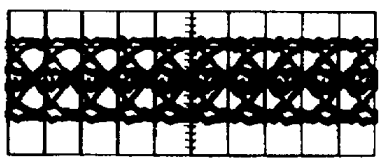
14



VERT = 1 V/CM HOR = 0.2 USEC/CM

eQ6, bQ7

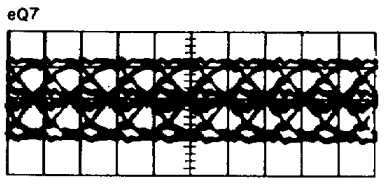
15



VERT = 1 V/CM HOR = 0.2 USEC/CM

eQ7

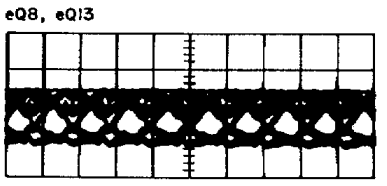
16



VERT = 1 V/CM HOR = 0.2 USEC/CM

eQ8, eQ13

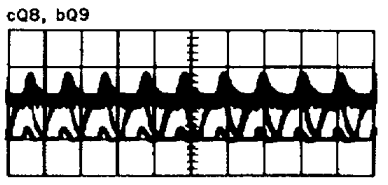
17



VERT = 1 V/CM HOR = 0.2 USEC/CM

cQ8, bQ9

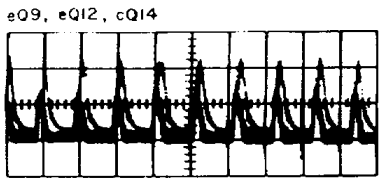
18



VERT = 2 V/CM HOR = 0.2 USEC/CM

eQ9, eQ12, cQ14

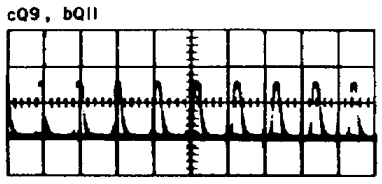
19



VERT = 1 V/CM HOR = 0.2 USEC/CM

cQ9, bQ11

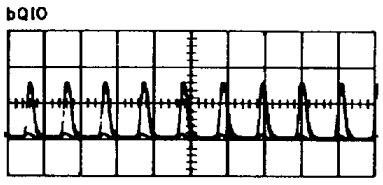
20



VERT = 2 V/CM HOR = 0.2 USEC/CM

bQ10

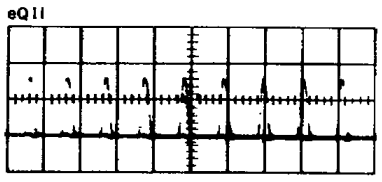
21



VERT = 2 V/CM HOR = 0.2 USEC/CM

eQ11

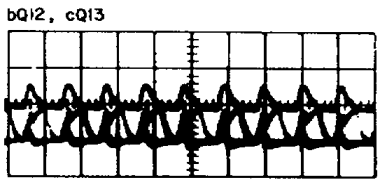
22



VERT = 2 V/CM HOR = 0.2 USEC/CM

bQ12, cQ13

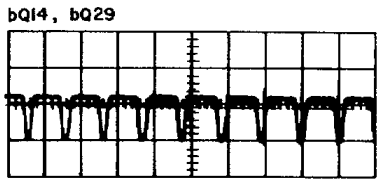
23



VERT = 2 V/CM HOR = 0.2 USEC/CM

bQ14, bQ29

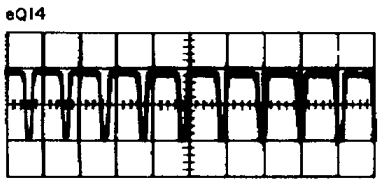
24



VERT = 2 V/CM HOR = 0.2 USEC/CM

eQ14

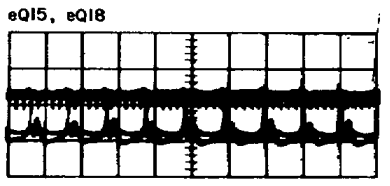
25



VERT = 1 V/CM HOR = 0.2 USEC/CM

eQ15, eQ18

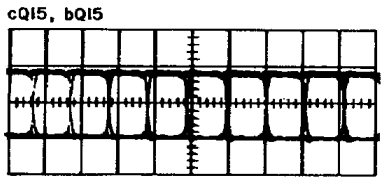
26



VERT = 1 V/CM HOR = 0.2 USEC/CM

cQ15, bQ15

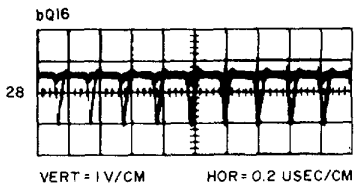
27

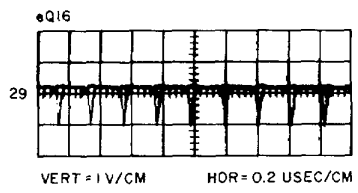


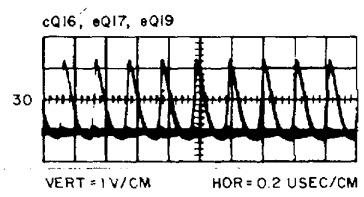
VERT = 2 V/CM HOR = 0.2 USEC/CM

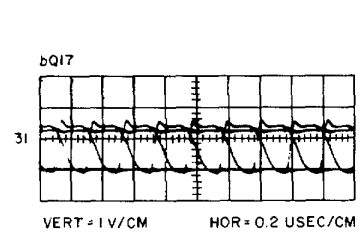
TM5805-367-35/1-67 (1)

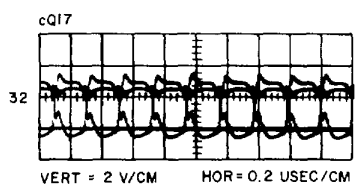
Figure 6-48. Panel 4A3, waveforms (part 1 of 2).

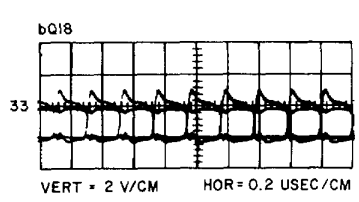


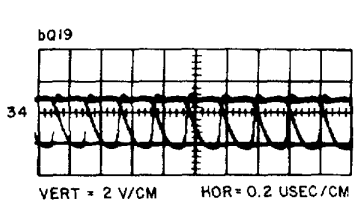


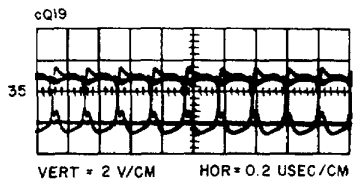


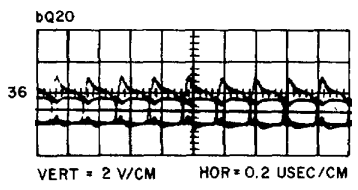


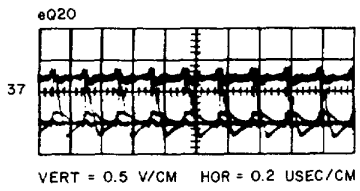


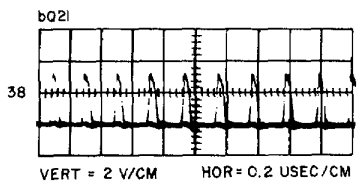


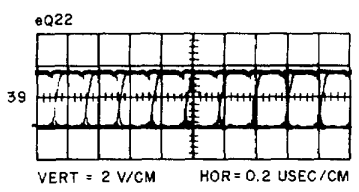


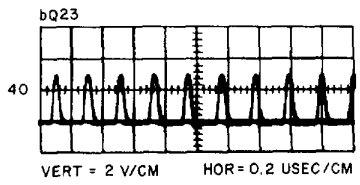


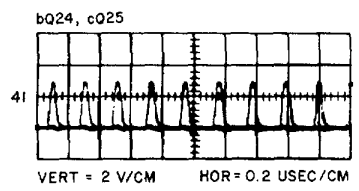


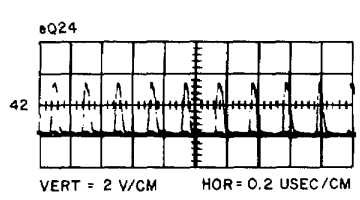


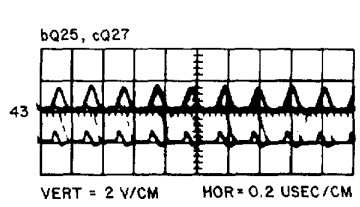


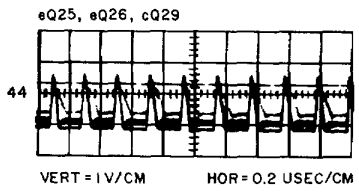


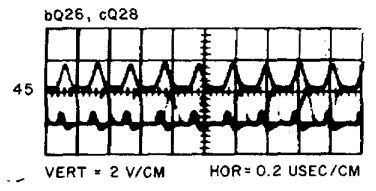


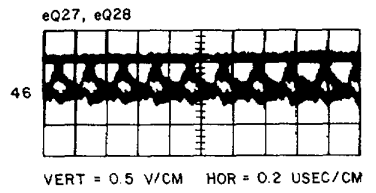


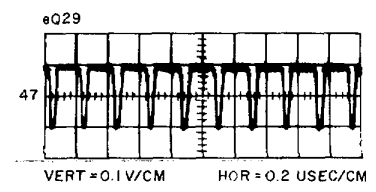


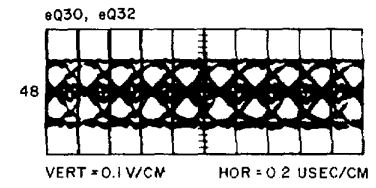


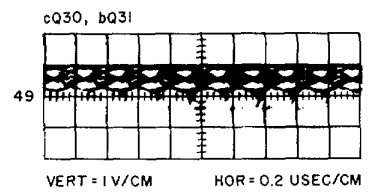


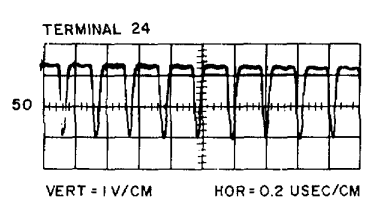


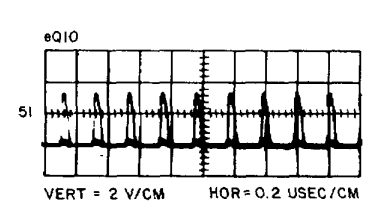


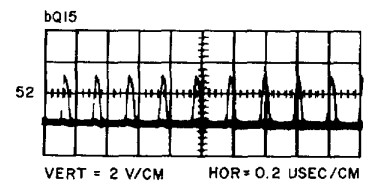


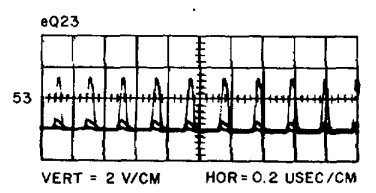












CONDITIONS FOR OBTAINING WAVEFORMS

NOTES 1, AND 3 GIVEN BELOW ARE APPLICABLE TO ALL WAVE FORMS ON THIS ILLUSTRATION, NOTE-REFERENCES GIVEN WITH WAVEFORMS PERTAIN TO CONDITIONS LISTED BELOW WHICH ARE REQUIRED TO OBTAIN THAT WAVEFORM.

1. INTERCONNECT TWO TD-353/U's WITH THE TEST TD-203/U AS FOLLOWS USING CG-1040B/U CABLE ASSEMBLIES.

MASTER TD-353/U JACKS	TO	TD-203/U JACKS
PCM OUT		PCM IN-1
TIMING OUT		TIM IN (NOTE 2)
PCM IN		PCM OUT-1
TIMING IN		TIM OUT-1

SLAVE TD-353/U JACKS	TO	TD-203/U JACKS
PCM OUT		PCM IN-2
PCM IN		PCM OUT-2
TIMING IN		TIM OUT-2

MASTER TD-353/U JACK	TO	SLAVE TD-353/U JACK
SYNC IN		SYNC OUT XMTR

	TO	TD-203/U JACKS
TEST OUT		FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, SYNCHRONIZE AN/USM-140A WITH THE TD-203/U BY CONNECTING AN/USM-140A INPUT JACK TO TD-203/U TIM IN JACK. USE A T CONNECTOR AT TD-203/U TIM IN JACK.

3. UNLESS OTHERWISE NOTED SWITCHES ARE OPERATED AS FOLLOWS:

MASTER AND SLAVE TD-353/U

SWITCH	SETTING	
	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

TD-203/U

AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	96I
OPERATE TRAFFIC SEL SWITCH TO 48. OPERATE BACK TO 96I AFTER OBSERVING WAVEFORM	

TM5805-367-35/1-67②

Figure 6-48. Panel 4A3 waveforms (part 2 of 2)..

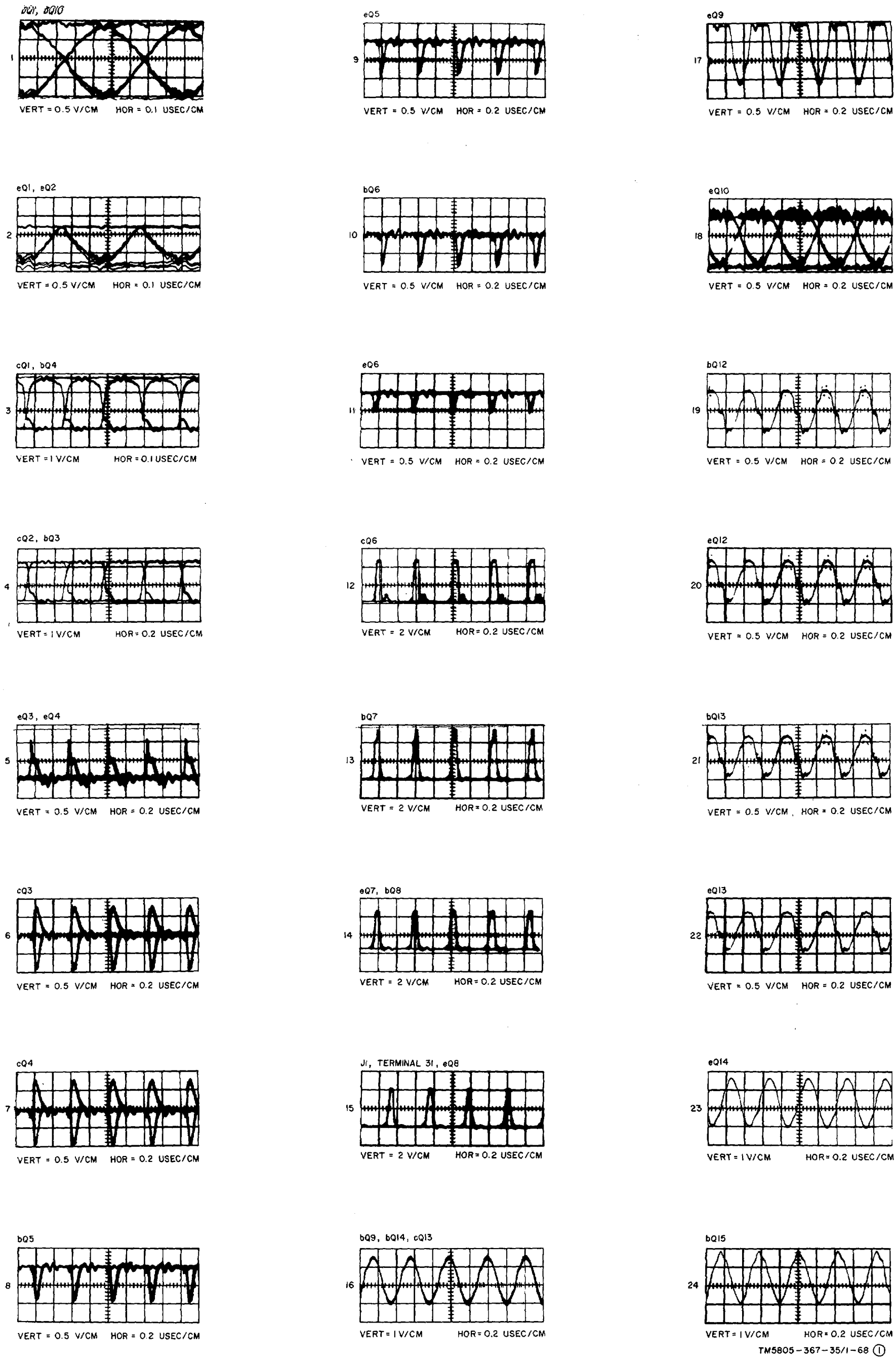
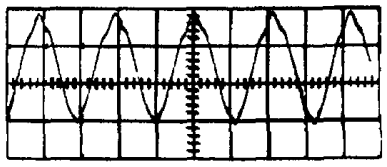


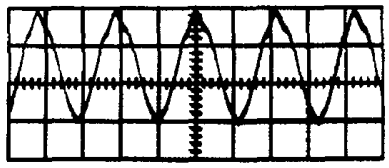
Figure 6-49. Panel 4A4, waveforms (part 1 of 2).

25 J3, eQ15



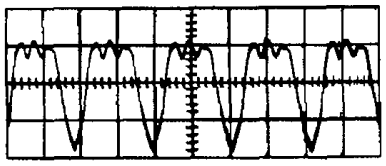
VERT = 1 V/CM HOR = 0.2 USEC/CM

26 bQ16



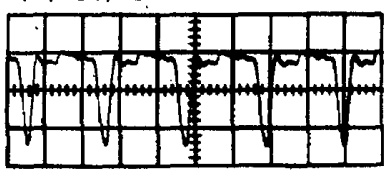
VERT = 1 V/CM HOR = 0.2 USEC/CM

27 eQ16, eQ17



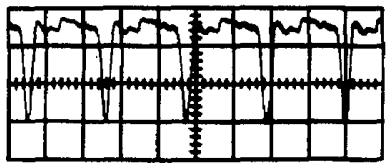
VERT = 0.5 V/CM HOR = 0.2 USEC/CM

28 cQ16, bQ18, bQ19



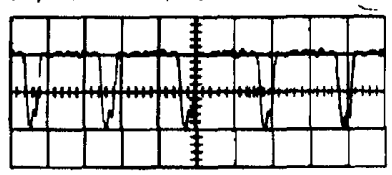
VERT = 1 V/CM HOR = 0.2 USEC/CM

29 eQ18



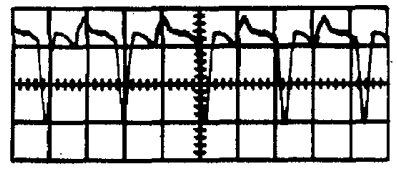
VERT = 0.5 V/CM HOR = 0.2 USEC/CM

30 J4, TERMINAL 7, eQ19



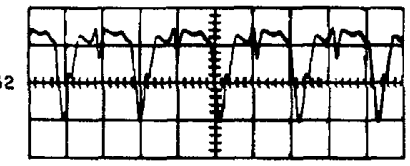
VERT = 1 V/CM HOR = 0.2 USEC/CM

31 bQ20



VERT = 1 V/CM HOR = 0.2 USEC/CM

32 J5, TERMINAL 13, eQ20



VERT = 1 V/CM HOR = 0.2 USEC/CM

CONDITIONS FOR OBTAINING WAVEFORMS

1. INTERCONNECT TWO TD-353/U's WITH THE TEST TD-203/U AS FOLLOWS USING CG-1040B/U CABLE ASSEMBLIES.

MASTER TD-353/U JACKS	TO	TD-203/U JACKS
PCM OUT		PCM IN-1
TIMING OUT		TIM IN (NOTE 2)
PCM IN		PCM OUT-1
TIMING IN		TIM OUT-1
SLAVE TD-353/U JACKS	TO	TD-203/U JACKS
PCM OUT		PCM IN-2
PCM IN		PCM OUT-2
TIMING IN		TIM OUT-2
MASTER TD-353/U JACK	TO	SLAVE TD-353/U JACK
SYNC IN		SYNC OUT XMTR
TD-203/U JACKS		
TEST OUT	TO	FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, SYNCHRONIZE AN/USM-140A WITH THE TD-203/U BY CONNECTING AN/USM-140A INPUT JACK TO TD-203/U TIM IN JACK. USE A T CONNECTOR AT TD-203/U TIM IN JACK.

3. UNLESS OTHERWISE NOTED SWITCHES ARE OPERATED AS FOLLOWS:

MASTER AND SLAVE TD-353/U

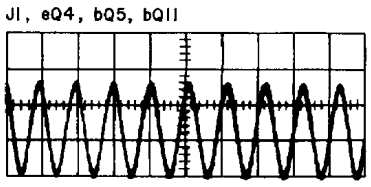
SWITCH	SETTING
AC POWER	ON
2 WIRE 4 WIRE	4 WIRE
AUX	OUT
ADDRESS	MASTER

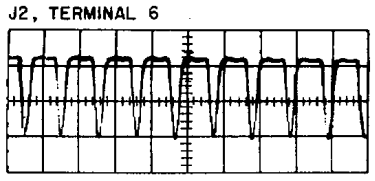
TD-203/U

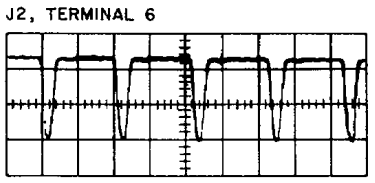
AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	48

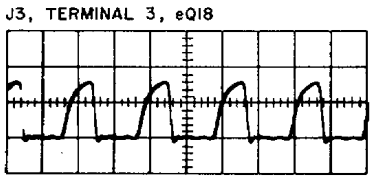
TM5805-367-35/1 -68②

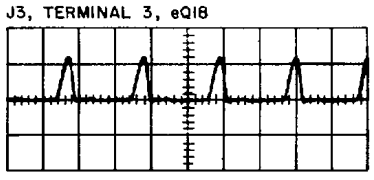
Figure 6-49. Panel 4A4 waveforms (part 2 of 2)..

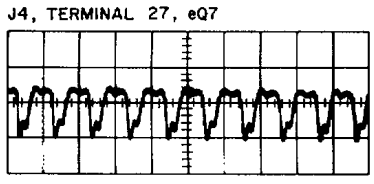
1 J1, eQ4, bQ5, bQ11

VERT = 1 V/CM HOR = 0.2 USEC/CM

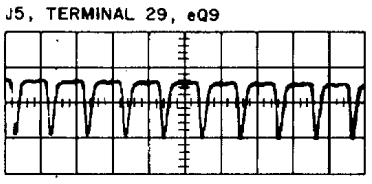
2 J2, TERMINAL 6

VERT = 1 V/CM HOR = 0.2 USEC/CM

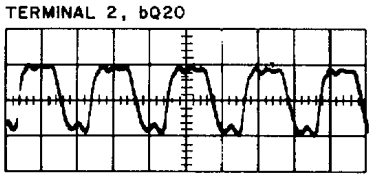
3 J2, TERMINAL 6

VERT = 1 V/CM HOR = 0.2 USEC/CM
SPEC. COND. 4

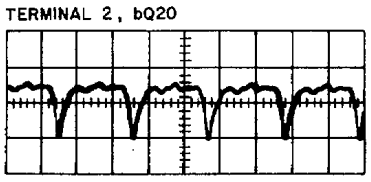
4 J3, TERMINAL 3, eQ18

VERT = 2 V/CM HOR = 0.2 USEC/CM

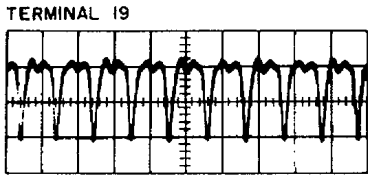
5 J3, TERMINAL 3, eQ18

VERT = 2 V/CM HOR = 0.2 USEC/CM
SPEC. COND. 4

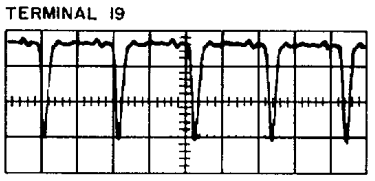
6 J4, TERMINAL 27, eQ7

VERT = 1 V/CM HOR = 0.2 USEC/CM
SPEC. COND. 5

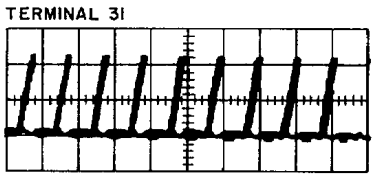
7 J5, TERMINAL 29, eQ9

VERT = 1 V/CM HOR = 0.2 USEC/CM

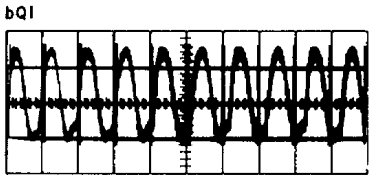
8 TERMINAL 2, bQ20

VERT = 2 V/CM HOR = 0.2 USEC/CM

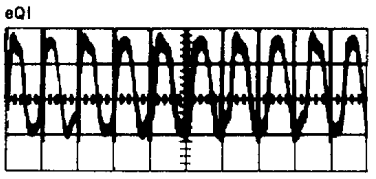
9 TERMINAL 2, bQ20

VERT = 2 V/CM HOR = 0.2 USEC/CM
SPEC. COND. 4

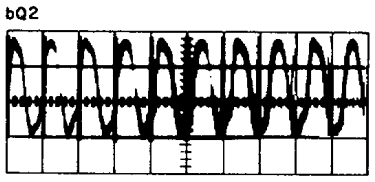
10 TERMINAL 19

VERT = 1 V/CM HOR = 0.2 USEC/CM

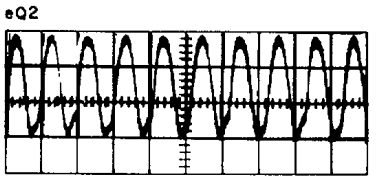
11 TERMINAL 19

VERT = 1 V/CM HOR = 0.2 USEC/CM
SPEC. COND. 4

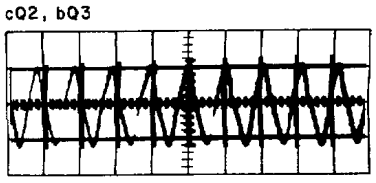
12 TERMINAL 31

VERT = 2 V/CM HOR = 0.2 USEC/CM

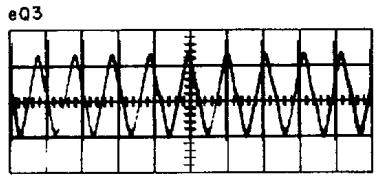
13 bQ1

VERT = 0.5 V/CM HOR = 0.2 USEC/CM

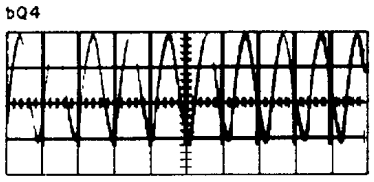
14 eQ1

VERT = 0.5 V/CM HOR = 0.2 USEC/CM

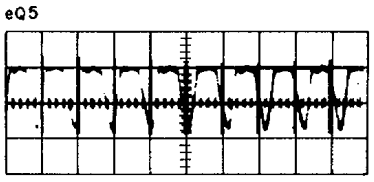
15 bQ2

VERT = 0.5 V/CM HOR = 0.2 USEC/CM

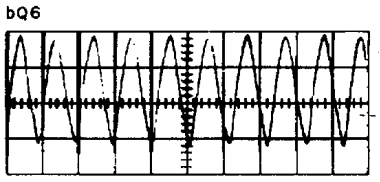
16 eQ2

VERT = 0.5 V/CM HOR = 0.2 USEC/CM

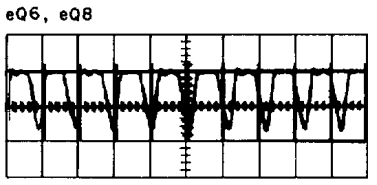
17 cQ2, bQ3

VERT = 1 V/CM HOR = 0.2 USEC/CM

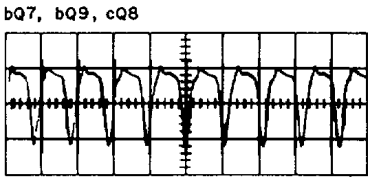
18 eQ3

VERT = 1 V/CM HOR = 0.2 USEC/CM

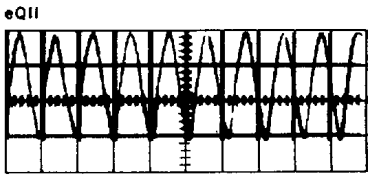
19 bQ4

VERT = 1 V/CM HOR = 0.2 USEC/CM

20 eQ5

VERT = 1 V/CM HOR = 0.2 USEC/CM

21 bQ6

VERT = 1 V/CM HOR = 0.2 USEC/CM

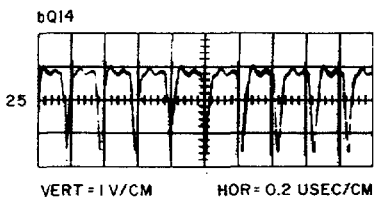
22 eQ6, eQ8

VERT = 1 V/CM HOR = 0.2 USEC/CM

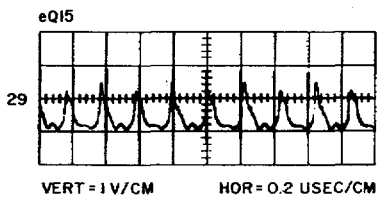
23 bQ7, bQ9, cQ8

VERT = 1 V/CM HOR = 0.2 USEC/CM

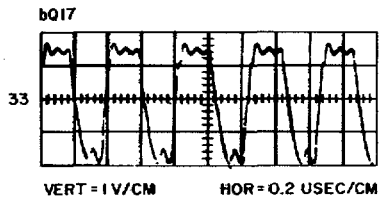
24 eQ11

VERT = 1 V/CM HOR = 0.2 USEC/CM

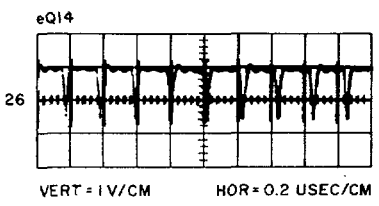
TM5805-367-35/1-69 (1)

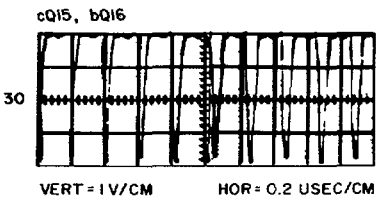
Figure 6-50. Panel 4A5, waveforms (part 1 of 2).

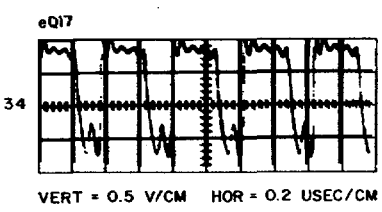


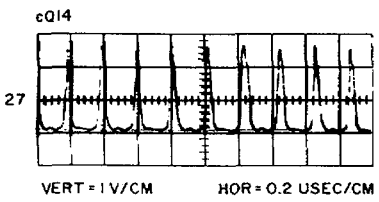


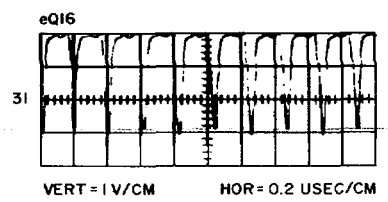


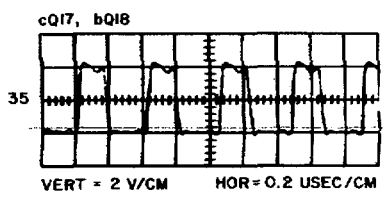


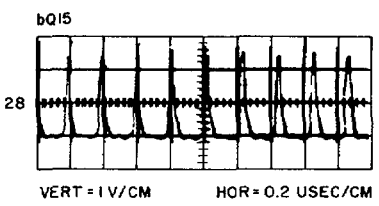


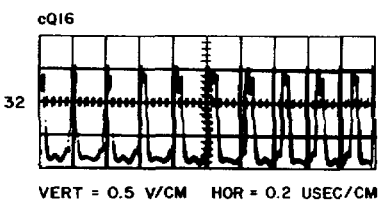


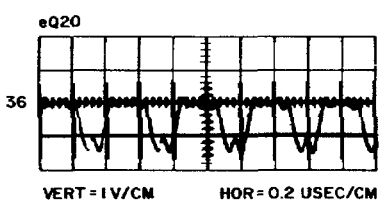












CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TWO TD-353/U MULTIPLEXERS CONNECTED FOR MASTER-SLAVE OPERATION AND INTERCONNECTED WITH TD-203/U AS FOLLOWS USING CG-1040B/U CABLES.

FROM	TO
MASTER TD-353/U	TD-203/U
PCM OUT	PCM IN-1
TIMING OUT	TIM IN (NOTE 2)
SLAVE TD-353/U	TD-203/U
PCM OUT	PCM IN-2
MASTER TD-353/U	SLAVE TD-353/U
SYNC OUT XMTR	SYNC IN
TD-203/U	MASTER TD-353/U
PCM OUT-1	PCM IN
TIM OUT-1	TIMING IN
TD-203/U	SLAVE TD-353/U
PCM OUT-2	PCM IN
TIM OUT-2	TIMING IN
TD-203/U	TD-203/U
TEST OUT	FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, OSCILLOSCOPE SYNCHRONIZED FROM TIM IN SIGNAL INPUT TO TD-203/U. USE OF T CONNECTION ON TIM IN CONNECTOR PROVIDES ACCESS TO THIS 2304-KC SIGNAL.

3. UNLESS OTHERWISE NOTED, SWITCHES OPERATED AS FOLLOWS:

TD-353/U	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

TD-203/U	
AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	96I

B. SPECIAL.

4. OPERATE TRAFFIC SEL SWITCH TO 48.

5. WAVEFORM AT J4 SHOULD LAG WAVEFORM AT TERMINAL 31 BY 1 USEC.

Figure 6-50. Panel 4A5, waveforms (part 2 of 2).

1
J1, eQ25
VERT = 2 V/CM HOR = 0.1 USEC/CM

2
J2, eQ19, cQ18, cQ17, bQ19
VERT = 2 V/CM HOR = 0.2 USEC/CM

3
J3, TERMINAL 31
VERT = 2 V/CM HOR = 0.2 USEC/CM

4
J4, bQ12, bQ13, cQ21
VERT = 2 V/CM HOR = 50 USEC/CM
SPEC. COND. 4, 5, 6

5
J5, bQ16
VERT = 2 V/CM HOR = 0.2 USEC/CM

6
J6, bQ15
VERT = 2 V/CM HOR = 0.2 USEC/CM

7
J7, bQ22
VERT = 2 V/CM HOR = 0.1 USEC/CM

8
TERMINAL 16, eQ15
VERT = 2 V/CM HOR = 0.2 USEC/CM

9
TERMINAL 17, eQ16
VERT = 2 V/CM HOR = 0.2 USEC/CM

10
bQ1
VERT = 1 V/CM HOR = 0.2 USEC/CM

11
cQ1, bQ2
VERT = 1 V/CM HOR = 0.2 USEC/CM

12
eQ2, bQ3
VERT = 1 V/CM HOR = 0.2 USEC/CM

13
eQ3
VERT = 1 V/CM HOR = 0.2 USEC/CM

14
bQ4
VERT = 1 V/CM HOR = 0.2 USEC/CM

15
eQ4
VERT = 1 V/CM HOR = 0.2 USEC/CM

16
bQ5
VERT = 1 V/CM HOR = 0.2 USEC/CM

17
eQ5
VERT = 0.5 V/CM HOR = 0.2 USEC/CM

18
cQ5, bQ10, bQ11
VERT = 2 V/CM HOR = 0.2 USEC/CM

19
bQ6
VERT = 1 V/CM HOR = 0.2 USEC/CM

20
eQ6
VERT = 1 V/CM HOR = 0.2 USEC/CM

21
cQ6, bQ7, bQ14
VERT = 2 V/CM HOR = 0.2 USEC/CM

22
eQ7
VERT = 0.5 V/CM HOR = 0.2 USEC/CM

23
eQ10
VERT = 0.5 V/CM HOR = 0.2 USEC/CM

24
eQ8
VERT = 2 V/CM HOR = 0.2 USEC/CM

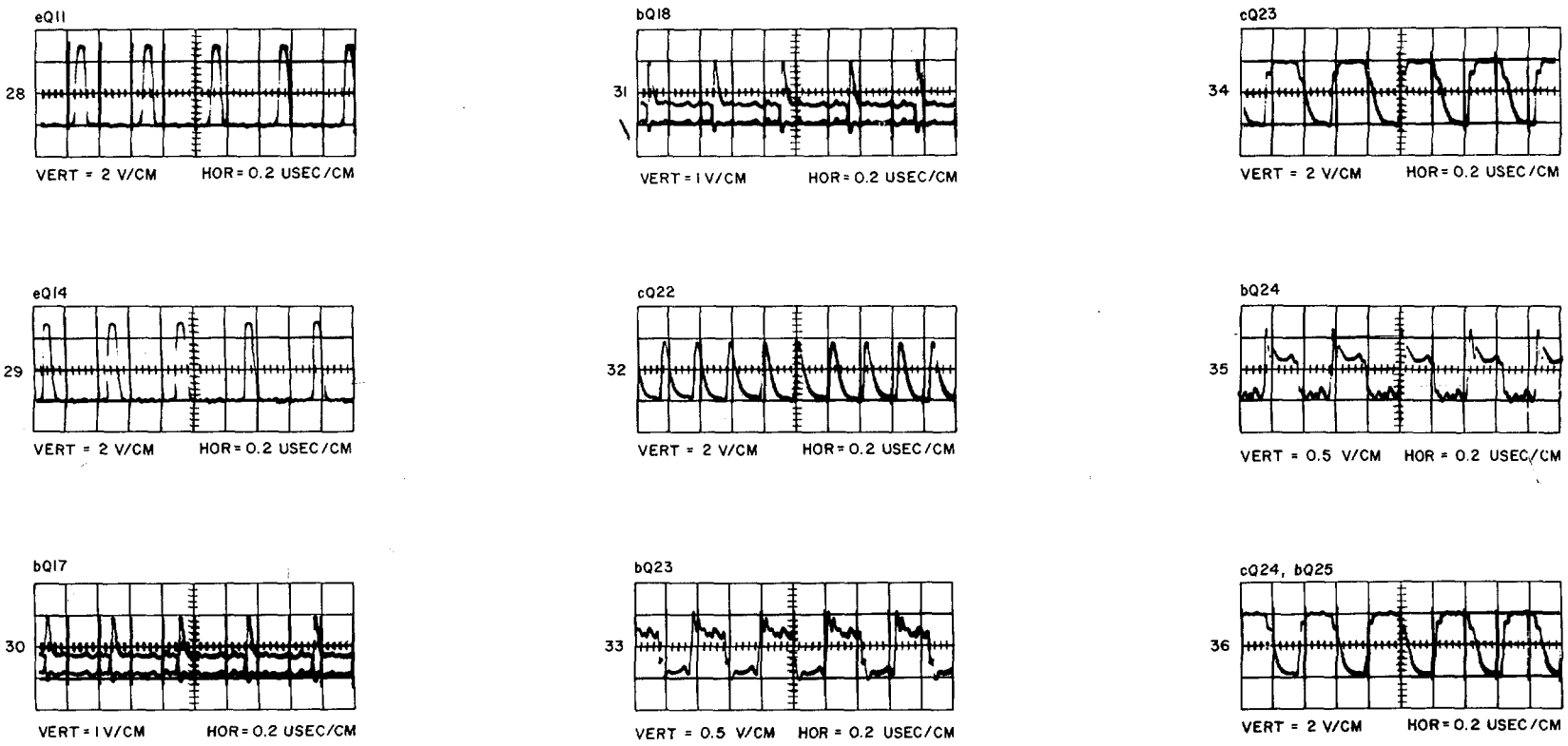
25
eQ9
VERT = 2 V/CM HOR = 0.2 USEC/CM

26
eQ12
VERT = 2 V/CM HOR = 0.2 USEC/CM

27
eQ13
VERT = 2 V/CM HOR = 0.2 USEC/CM

TM5805-367-35/1-70 (1)

Figure 6-51. Panel 4A9, waveforms (part 1 of 2).



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TWO TD-353/U MULTIPLEXERS CONNECTED FOR MASTER-SLAVE OPERATION AND INTERCONNECTED WITH TD-203/U AS FOLLOWS USING CG-1040B/U CABLES.

FROM MASTER TD-353/U	TO TD-203/U
PCM OUT	PCM IN-1
TIMING OUT	TIM IN (NOTE 2)
FROM SLAVE TD-353/U	TO TD-203/U
PCM OUT	PCM IN-2
FROM MASTER TD-353/U	TO SLAVE TD-353/U
SYNC OUT XMTR	SYNC IN
FROM TD-203/U	TO MASTER TD-353/U
PCM OUT-1	PCM IN
TIM OUT-1	TIMING IN
FROM TD-203/U	TO SLAVE TD-353/U
PCM OUT-2	PCM IN
TIM OUT-2	TIMING IN
FROM TD-203/U	TO TD-203/U
TEST OUT	FROM RADIO RCVR

2. UNLESS OTHERWISE NOTED, OSCILLOSCOPE SYNCHRONIZED FROM TIM IN SIGNAL INPUT TO TD-203/U. USE OF T CONNECTION ON TIM IN CONNECTOR PROVIDES ACCESS TO THIS 2304-KC SIGNAL.

3. UNLESS OTHERWISE NOTED, SWITCHES OPERATED AS FOLLOWS:

TD-353/U

	MASTER	SLAVE
AC POWER	ON	ON
2 WIRE 4 WIRE	4 WIRE	4 WIRE
AUX	OUT	OUT
ADDRESS	MASTER	SLAVE

TD-202/U

AC POWER	ON
OPR-TEST	TEST
TRAFFIC SEL	96I

B. SPECIAL.

4. OPERATE TRAFFIC SEL SWITCH TO 96S.
5. OPERATE OSCILLOSCOPE ON NEGATIVE INTERNAL SYNCHRONIZATION
6. OPERATE MASTER TD-353/U ADDRESS SWITCH TO SLAVE (PROVIDES OUT-OF-FRAME CONDITION AS REQUIRED TO GENERATE SKIP PULSE IN TD-203/U).

Figure 6-51. Panel 4A9, waveforms (part 2 of 2).

APPENDIX
REFERENCES

Following is a list of applicable references available to direct and general support and depot maintenance repairmen of Multiplexers TD-202/U and TD-203/U.

DA PAM 310-1	Consolidated Index of Army Publications and Blank Forms.
DA PAM 738-750	The Army Maintenance Management System (TAMMS).
AR 310-25	Dictionary of United States Army Terms.
AR 310-50	Catalog of Abbreviating and Brevity Codes (Microfiche).
AR 750-5	Organization, Policies, and Responsibilities for Maintenance Operations.
SB 11-573	Painting and Preservation of Supplies Available for Field Use for Electronics Command Equipment.
SB 38-100	Preservation, Packaging, and Packing Materials, Supplies, and Equipment used by the Army.
TA 11-17	Signal Field Maintenance Shops.
TA 11-100 (11-17)	Allowances of Signal Corps Expandable Supplies for Signal Field Maintenance Shops.
TB SIG 222	Solder and Soldering.
TB 43-0118	Field Instructions for Painting and Preserving Electronics Command Equipment, Including Camouflage Pattern Painting of Electrical Equipment Shelters.
TM 11-664	Theory and Use of Electronic Test Equipment.
TM 11-672	Pulse Techniques.
TM 11-690	Basic Theory and Application of Transistors.
TM 11-4000	Troubleshooting and Repair of Radio Equipment.
TM 11-6625-358-15	Operator, Organizational, DS, GS, and Depot Maintenance Manual: Signal Generators SG-71/FCC, SG-71A/FCC, and SG-71B/FCC, and SG-71C/FCC.
TM 11-5540	Electric Light Assembly MX-1292/PAQ.
TM 11-5805-367-12	Operator and Organizational Maintenance Manual: Multiplexers TD-202/U, TD-203/U, TD-204/U, TD-352/U, and TD-353/U, Restorer, Pulse Form TD-206/G, and Converter, Telephone Signal CV-1548/G.
TM 11-5965-206-15P	Operator, Organizational, Field and Depot Maintenance Repair Parts and Special Tool Lists: Headset-Microphone H-91/U, H-91A/U; Handset-Headset H-144/U, H-144A/U, H-144B/U, H-144C/U, and Headset-Microphone H-210/G.
TM 11-6625-200-15	Operator, Organizational, DS, GS, and Depot Maintenance Manual: Multimeters ME-26A/U, ME-26B/U, ME-26C/U, and ME-26D/U.
TM 11-6625-320-12	Operator and Organizational Maintenance Manual: Voltmeter, Meter, ME-30A/U and Voltmeters, Electronic ME-30B/U, ME-30C/U, and ME-30E/U.
TM 11-6625-366-15	Organizational, DS, GS, and Depot Maintenance Manual: Multi meters TS-352B/U.

TM 11-6625-366-25P	Organizational, DS, GS, and Depot Maintenance Repair Parts, Multimeter TS-352B/U.
TM 11-6625-535-15	Operator, Organizational, DS, GS, and Depot Maintenance Manual: Oscilloscope AN/USM-140A.
TM 11-6625-539-15	Operator, Organizational, Field and Depot Maintenance Manual: Transistor Test Set TS-1836/U.
TM 740-90-1	Administrative Storage Equipment.
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

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Ft Carson (21)
Ft Gordon (10)
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Ft Knox (12)
WSMR (5)
Army Dep (2) except
LBAD (14)
SAAD (30)
TOAD (14)
ATAD (10)
NAAD (5)
LEAD (7)
SVAD (5)
Gen Dep (2)
Sig Sec, Gen Dep (5)
Sig Dep (12)
SigFLDNS (2)
AMS (1)
USAERDAA (2)
USAERDAW (13)
USACRREL (2)
Units organized under following TOE's (2 each):

11-57	11-158
11-97	11-500
11-98	(AA-AC)
11-117	11-587
11-127	11-592
11-155	1597
11-157	

NG: State AG (3).

USAR: None.

For explanation of abbreviations used, see AR 320-50.

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1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

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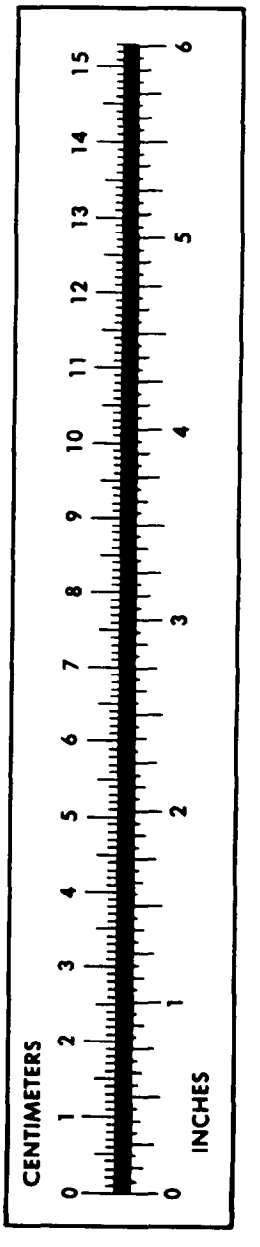
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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