

**TECHNICAL MANUAL**

**INTERMEDIATE DIRECT SUPPORT  
MAINTENANCE MANUAL**

**RADIO SETS**

**AN/GRC-103(V)1 (NSN 5820-00-935-4931),  
AN/GRC-103(V)2 (NSN 5820--00-116-6029),  
AN/GRC-103(V)3 (NSN 5820-00-116-6030),  
AN/GRC-103(V)4 (NSN 5820-01-081-8866)**

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**HEADQUARTERS, DEPARTMENT OF THE ARMY**

**1 OCTOBER 1987**



WARNING

Be careful when working on the 115 volt ac line connections. Serious injury or death may result from contact with these terminals.

## DON'T TAKE CHANCES!

EXTREMELY DANGEROUS VOLTAGES EXIST IN THE FOLLOWING UNITS

OF RADIO SET AN/GRC-103(V)1:

|   |              |
|---|--------------|
| TRANSMITTER, RADIO 5TR1   | 800 volts dc |
| AMPLIFIER-FREQUENCY MULTIPLIER<br>AM-4320/GRC-103(V),<br>AM-4320A/GRC-103(V)<br>AND AM-4320B/GRC-103(V) | 600 volts dc |

DANGEROUS RADIO FREQUENCY VOLTAGES EXIST AT THE  
ANTENNA TERMINALS

Be careful when working around the antenna or the antenna terminals. High voltages exist at these points.

WARNING

Operator and maintenance personnel should be familiar with the requirements of TB 43-0129 before attempting installation or operation of the equipment covered in this manual. Failure to follow requirements of TB 43-0129 could result in injury or DEATH.





Technical Manual  
 No. 11-5820-540-30

HEADQUARTERS  
 DEPARTMENT OF THE ARMY  
 Washington, DC, 1 October 1987

INTERMEDIATE DIRECT SUPPORT  
 MAINTENANCE MANUAL

RADIO SETS AN/GRC-103(V)1 (NSN 5820-00-935-4931),  
 AN/GRC-103(V)2 (NSN 5820-00-116-6029),  
 AN/GRC-103(V)3 (NSN 5820-00-116-6030),  
 AN/GRC-103(V)4 (NSN 5820-01-081-8866)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to: Commander, US Army Communications-Electronics Command, and Fort Monmouth ATTN : AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5000. In either case, a reply will be furnished direct to you.

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\*This manual supersedes so much of TM 11-5820-540-35, 21 August 1969, as pertains to direct support maintenance.

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CHAPTER 1  
INTRODUCTION

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NOTE

In this technical manual, some units or parts will be referenced by a CMC number or drawing number. These numbers will appear on the units or parts for identification purposes of the plain or "A" model. These units or parts are not to be interchanged, and replacement will be by like item.

1-1. Scope

a. This manual contains instructions for direct support maintenance of Radio Sets AN/GRC-103(V)1 (Band I), AN/GRC-103(V)2 (Band II), AN/GRC-103(V)3 (Band III), and AN/GRC-103(V)4 (Band IV). It includes instructions for troubleshooting, testing, aligning, and for repairing the equipment and replacing maintenance parts which are appropriate to the direct support maintenance category. Detailed theory of operation of the equipment is contained in chapter 2. Direct support maintenance instructions are contained in chapter 3. Chapter 4 contains the foldout schematic and block diagrams for the Radio Set.

b. The complete manual for this equipment includes TM 11-5820-540-12, TMs 11-5820-540-40-1, 40-2, 40-3, and DMWR 11-5820-540.

1-2. Index of Consolidated Publications and Blank Forms

a. DA Pam 25-30. Refer to the latest issue of DA Pam 25-30 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 750-10. Refer to DA Pam 750-10 to determine whether there are modification work orders (MWOS) pertaining to the equipment.

1-3. Maintenance Forms, Reports, and Reports

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750 as contained in Maintenance Management Update.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 [Report of Discrepancy (ROD)] as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73B/AFR 400-54/MCO 44300.3H.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1-4. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

1-5. Reporting Equipment Improvement Recommendations (EIR)

If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about the design. Put in on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-PA-MA-D, Fort Monmouth, New Jersey 07703-5000. In either case a reply will be furnished direct to you.

CHAPTER 2  
FUNCTIONING OF EQUIPMENT

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Section I. TRANSMITTER, RADIO T-983(P)/GRC-103(V), T-983A(P)/GRC-103(V)  
AND T-983B(P)/GRC-103(V)

NOTE

A functional block diagram analysis of the complete radio set is given in paragraph 6-1 of TM 11-5820-540-12. This chapter refers to all units, unless otherwise specified.

2-1. Block Diagram Analysis of Transmitter, Radio T-983(P)/GRC-103(V), T-983A(P)/GRC-103(V) and T-983B(P)/GRC-103(V) (Fig. 2-1).

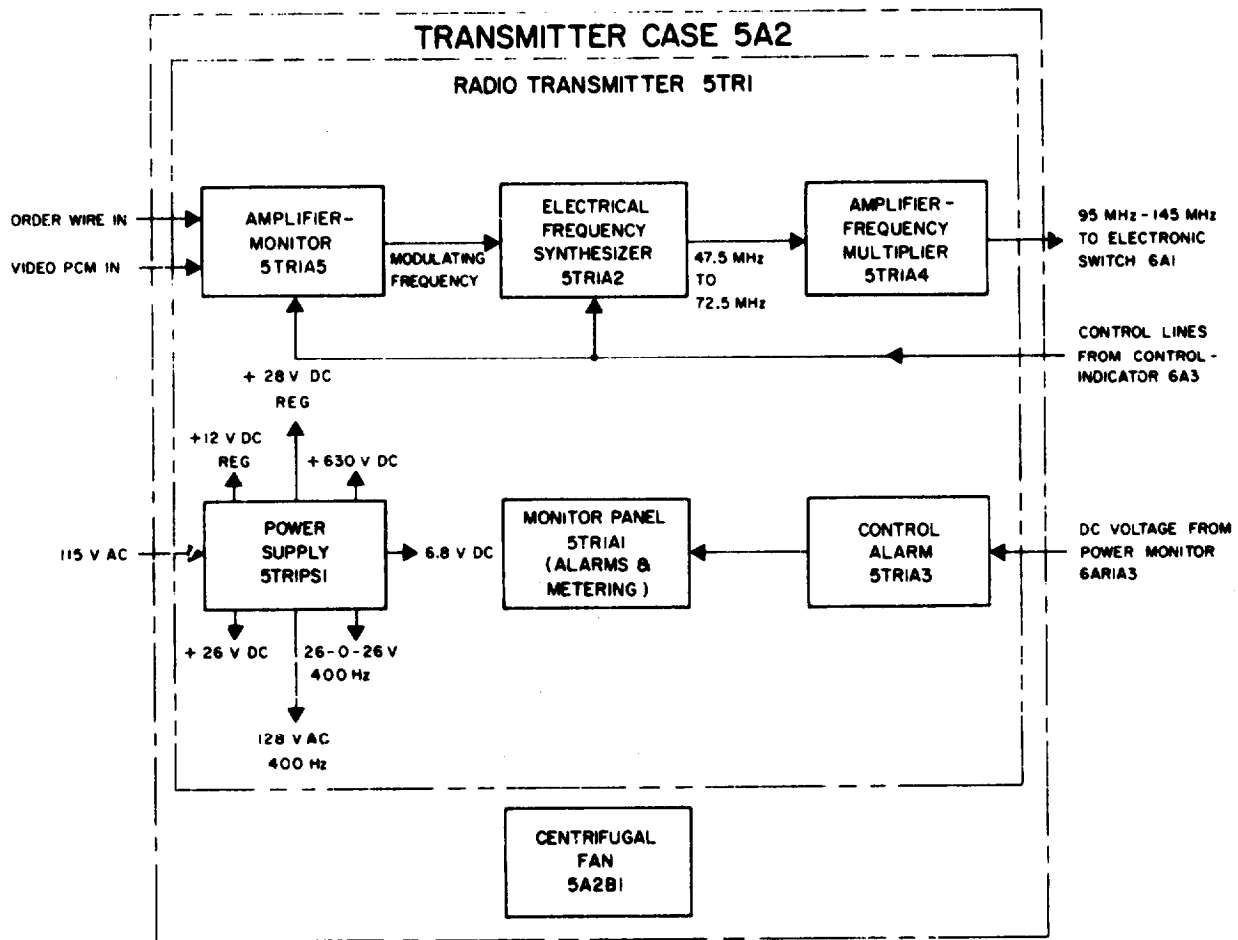
a. Transmitter, Radio T-983(P)/GRC-103(V), Transmitter, Radio T-983A(P)/GRC-103(V) and Transmitter, Radio T-983B(P)/GRC-103(V) (transmitter fixed head) accept baseband signals in the frequency range of 200 Hz to 1 MHz at the VIDEO connector and order wire signals from 200 Hz to 4 kHz at the OW connector, both connectors are located at the rear of Case, Transmitter CY-4637/GRC-103(V) or CY-4637A/GRC-103(V). The two input signals are combined and amplified in amplifier-monitor 5TR1A5, and then used to modulate the basic signal frequency generated in electrical frequency synthesizer 5TR1A2 (synthesizer). The level of the incoming video signal can be adjusted by the INPUT control on the front of the transmitter fixed head before it is fed into the amplifier-monitor. The amplifier-monitor attenuates the signal as required to insure that transmitter deviation remains constant as frequency multiplication factors are changed during transmitter tuning. This is accomplished through relays controlled by signals from Amplifier-Frequency Multiplier AM-4320/GRC-103(V), AM-4320A/GRC-103(V) or AN-4320B/GRC-103(V) (Transmitter Rf Head) which are initiated in control-indicator 6A3.

b. The crystal-controlled synthesizer generates the basic signal frequency in the range of 47.5 to 72.5 MHz in steps of 125.0 kHz or 83.333 kHz, depending on the frequency multiplication factor used (4 or 6 respectively). The synthesizer frequency is selected by the control-indicator and becomes, after appropriate multiplication, the final transmit frequency in the range of 220 to 405 MHz. The combined baseband and order wire signal from amplifier-monitor 5TR1A5 modulates the basic signal frequency to produce an fm signal in the range of 47.5 to 72.5 MHz at the output of the synthesizer. The output of the synthesizer is fed to amplifier-frequency multiplier 5TR1A4 where it is doubled in frequency and amplified to produce a 3 watt (nominal) output signal. The resulting 95 to 145 MHz rf signal is fed to the frequency multiplication circuits in the transmitter rf head.

c. A sample of the rf power at the output of the transmitter rf head is rectified and supplied to alarm control 5TR1A3 which provides a warning when the rf signal power falls about 8 db below the nominal output power.

Q. Power for all units in the transmitter fixed and rf heads is obtained from power supply 5TR1PS1 located in the transmitter fixed head. The power supply provides unregulated dc power at 26 volts for operating alarms and control circuits; regulated dc power at 12 volts to operate the general electronic circuits; 630 volts dc unregulated to operate radio frequency amplifier 6AR1 tubes; two supplies of 6.8 volts dc unregulated for the heaters of the radio frequency amplifier tubes; a 400 Hz, 128 volt, square wave output to operate centrifugal fan 5A2B1 in the transmitter case; and a 400 Hz, 26 volt square wave output for operation of alarm control 5TR1A3. The power supply includes two constant-current regulators for the cathodes of the rf amplifier tubes. It operates from a 115 volt, ac, 47 to 420 Hz source.

e. Metering facilities are provided in the transmitter for the 28 volt, 12 volt and 630 volt supplies; for the output levels of synthesizer 5TR1A2 (OSC), amplifier-frequency multiplier 5TR1A4 (DOUBLER), frequency-multiplier assembly 6A2 (MULT), driver stage (DRIVER) and output (PWR OUT) of radio frequency amplifier 6AR1; for the reflected rf power (REFL PWR); and for the frequency deviation in the three modes of operation (12 CH PCM, 24 CH PCM and FDM). Alarm circuits (audible and visible) are provided to indicate an out-of-lock condition of the afc loop used to control the output frequency of the synthesizer (SYNC), low rf output power (LOW POWER) and failure of the air cooling system (OVERHEAT).



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Figure 2-1. Transmitter, Radio T-983 (P)/GRC-103(V), T-983A (P)/GRC-103(V) and T-9838(P)/GRC-103(V), Block Diagram.



2-2. Amplifier-Monitor 5TR1A5

a. General. Amplifier-monitor 5TR1A5 consists of two separate printed circuit boards, video amplifier 5TR1A5AR1 and video monitor 5TR1A5A1, both of which are mounted in the same case. This signal path is shown in figure 2-2 and the overall circuit diagram is shown in F0-4-39.

b. Block Diagram Analysis (Fig. 2-1).

(1) Video amplifier 5TR1A5AR1. The video input signal (12-channel pcm, 24-channel pcm or fdm) from the INPUT level control is fed through a low-pass filter having a gaussian shaped response of 3 db down at 567 kHz and 11 db down at 960 kHz. The video output of the filter is added in a linear manner to the order wire signal through a simple resistive network. The pcm video is not modulated with the order wire signal; the peak voltage and the baseline vary simultaneously at the order wire signal frequency. The combined video and order wire signal is then fed to a three-stage video amplifier which has approximately 7 db gain. The output of the last stage of this amplifier, an emitter-follower, is fed through a series of relay-controlled attenuators to modulator-oscillator 5TR1A2A2 in the synthesizer. The relays switch the three pi-type attenuators into the circuit, as required to adjust the output signal in the proper proportion to the final signal multiplication factor; this is done to insure a constant transmitter deviation for the various multiplication factors. The attenuation, compared to the multiplication factor, is shown below:

| Multiplication factor | Attenuation            |
|-----------------------|------------------------|
| 4                     | 0 db Band I            |
| 6                     | 3.5 db Band I          |
| 8                     | 6.0 db Band II         |
| 12                    | 9.5 db Band II and III |
| 16                    | 12.0 db Band III       |
| 24                    | 15.5 db Band IV        |
| 32                    | 18.0 db Band IV        |

(2) Video monitor 5TR1A5A1. A portion of the video amplifier output is fed to video monitor 5TR1A5A1 for metering purposes. The input signal from video amplifier 5TR1A5AR1 is fed to two-stage amplifier Q1-Q2 of video monitor 5TR1A5A1. The output from the second amplifier stage is fed to a temperature-compensated rectifier circuit where it is peak detected and fed to three calibrated metering points, which have adjustable resistors for calibrating the meter indications at midscale for 24-channel or 12-channel pcm or fdm signal levels. The meter common point is connected to ground.

c. Circuit Diagram Analysis (F0-4-39).

(1) Video amplifier 5TR1A5AR1. The video or fdm signals are coupled through R1 to low-pass filter FL1. The filter attenuates the signals in a gaussian-shaped response (3 db down at 567 kHz and 11 db down at 960 kHz). This frequency limiting is required to reduce the transmitter rf bandwidth. The video signal at the output

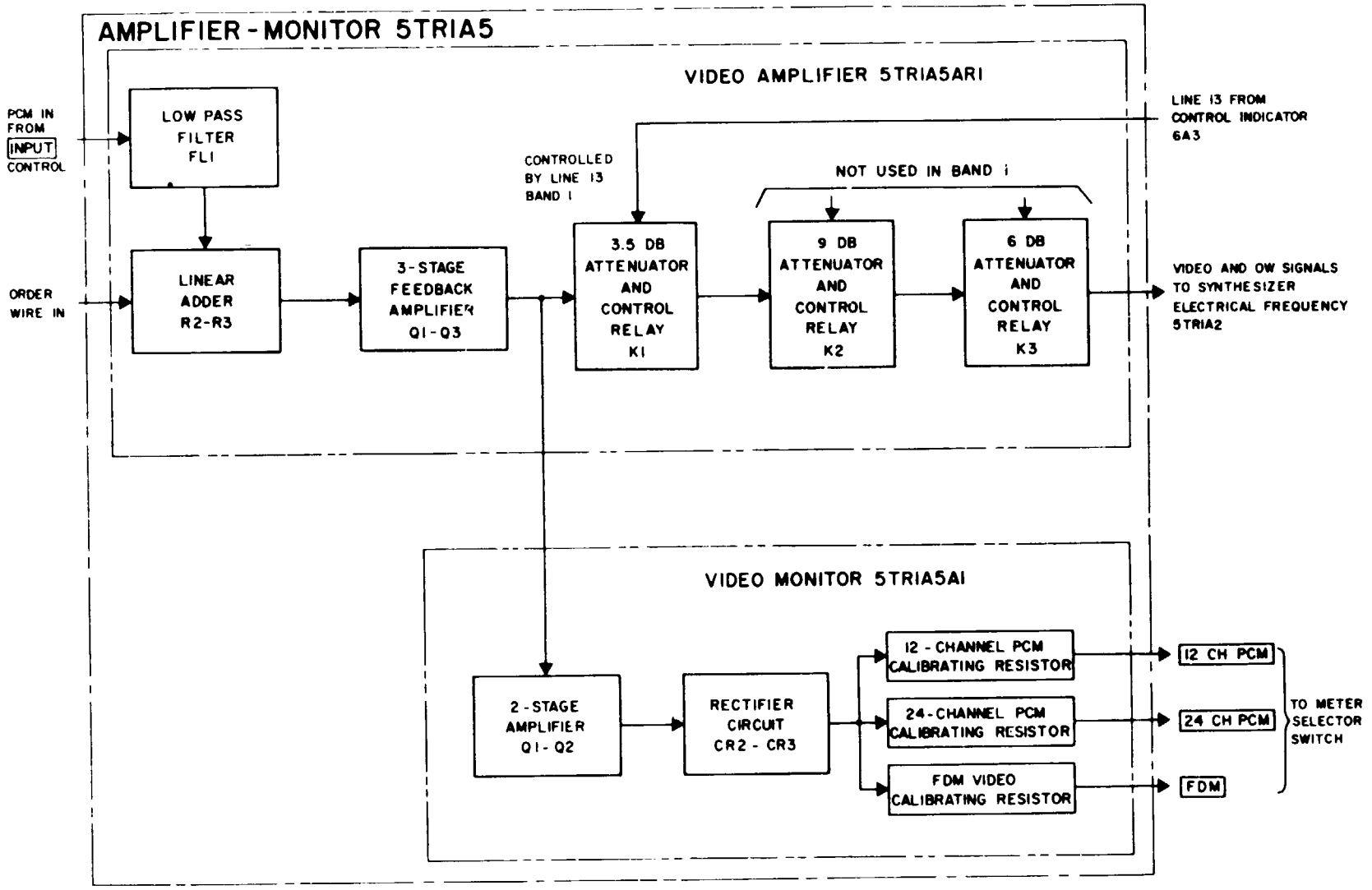


Figure 2-2. Amplifier-Monitor 5TRIA5, Block Diagram

of FL1 is fed through C1 to the base of Q1. Order wire signals are applied to the junction of R2 and R3. R2 provides termination for FL1 and R3 terminates the order wire input. The order wire signal is added to the video signal through R2 and then through C1 to the base of Q1. The combined signal at the Q1 collector is coupled through C3 to the base of Q2, and the amplified signal at the collector of Q2 is fed directly to the base of emitter-follower Q3. Q1, Q2 and Q3 form a three-stage amplifier which provides approximately 7 db gain. The signal at the Q3 emitter is fed through C6 and R26, the gain control, through feedback circuit C4 and R13 to the emitter of Q1. C4 extends the high frequency feedback; R26 adjusts the level of the feedback signal. The signal at the output of C6 is also coupled to video monitor 5TR1A5A1, and through R15 to the input attenuator. The three pi-type attenuators R16-R17-R18 (3.5 db), R19-R20-R21 (9 db) and R22-R23-R24 (6 db) are switched into the circuit by remotely-controlled relays K1 K2 and K3 respectively. The change of multiplication factor takes place with the interchange of transmitter rf heads. A further change within each band occurs as the frequency is changed past the middle of each band; this change is initiated by control line 13 from control-indicator 6A3 in the transmitter rf head. Relay operation is arranged to switch the attenuators into the circuit as the relays are de-energized. This is done to insure that the transmitter cannot be overmodulated in the event of a relay failure. The combined video and order wire signal at the output of the attenuators is fed directly into modulator-oscillator board 5TR1A2A2 of the synthesizer.

(2) Video monitor 5TR1A5A1. The second output of the emitter-follower Q3 of video amplifier 5TR1A5AR1 is coupled through C1 and Q1 to the base of emitter-follower Q2. L1, L2, L3 are parasitic oscillation suppressors. The Q2 emitter output is coupled through C3 to rectifier CR2, CR3. C3 attenuates order wire signals while passing video signals. CR1 provides temperature compensation for the rectifier. R7 and R10 are meter calibrating resistors in series with the 24-channel pcm metering line. Similarly, R8 and R11 are in series with the 12-channel pcm metering, and R9 and R12 are in series with the fdm metering. the Q1 emitter through voltage divider R4 and R5.

2-3. Electrical Frequency Synthesizer 5TR1A2 or 1RE1A2, Part No. SM-D-618945 (On Unlettered Model)

#### NOTE

The two models of modulator-oscillator 5TR1A2A2 or 1RE1A2A2 are distinguishable by part numbers CMC 456-260 and SM-D-865030. Except where specified otherwise, this paragraph refers to both units.

a. General. Synthesizer 5TR1A2 or 1RE1A2 consists of a voltage controlled oscillator (vco), whose output is fed through a variable divider (programmed counter) to a comparator circuit, and a fixed, crystal-controlled oscillator, whose output is fed through a fixed divider to the same comparator circuit. The comparator circuit then controls the automatic frequency control voltage which in turn controls the vco frequency. The counter is programmed by the code established within control-indicator 6A3 or 2A2. Thus, the synthesizer output frequency can be selected by a control-indicator 6A3 or 2A2 and referenced to a crystal oscillator at each selected frequency. The synthesizer consists of the following nine printed circuit boards and one interconnecting box (Part No. SM-D-618945):

|                      |                      |
|----------------------|----------------------|
| Modulator-oscillator | 5TR1A2A2 or 1RE1A2A2 |
|----------------------|----------------------|

|                                       |                      |
|---------------------------------------|----------------------|
| Amplifier-monitor                     | 5TR1A2A3 or 1RE1A2A3 |
| Frequency Divider                     | 5TR1A2A4 or 1RE1A2A4 |
| Digital Electronic<br>Divider-Counter | 5TR1A2A5 or 1RE1A2A5 |
| Digital Electronic Counter            | 5TR1A2A6 or 1RE1A2A6 |
| Electrical Synchronizer               | 5TR1A2A7 or 1RE1A2A7 |
| Signal Data Converter-<br>Storer      | 5TR1A2A8 or 1RE1A2A8 |
| Frequency Divider                     | 5TR1A2A9 or 1RE1A2A9 |
| Rf Oscillator                         | 5TR1A2Y1 or 1RE1A2Y1 |
| Interconnecting Box                   | 5TR1A2A1 or 1RE1A2A1 |

Synthesizer (Part No. SM-D-865030 A Model ) consists of the following eight circuit boards and one interconnecting box:

|  |                        |
|--|------------------------|
| Modulator-oscillator                   | 5TR1A2A2 or 1RE1A2A2   |
| Amplifier-monitor                      | 5TR1A2A3 or 1RE1A2A3   |
| Frequency divider                      | 5TR1A2A14 or 1RE1A2A14 |
| Digital electronic divider-<br>counter | 5TR1A2A15 or 1RE1A2A15 |
| Digital electronic counter             | 5TR1A2A16 or 1RE1A2A16 |
| Electrical synchronizer                | 5TR1A2A17 or 1RE1A2A17 |
| Signal data converter-storer           | 5TR1A2A18 or 1RE1A2A18 |
| Rf oscillator                          | 5TR1A2Y11 or 1RE1A2Y11 |
| Interconnecting Box                    | 5TR1A2A11 or 1RE1A2A11 |

NOTE

Electrical Frequency Synthesizer 5TR1A2 or 1RE1A2 will be distinguished by lettered and unlettered models, with different part numbers.

b. Block Diagram Analysis (FO-4-1, 4-2). Baseband signals from amplifier-monitor 5TR1A5 are applied through a sensitivity control to the modulation varactor in modulator-oscillator 5TR1A2A2. (This modulation facility is not used when the unit is mounted in a receiver.) The synthesizer output signal is the selected channel frequency in the range 47.5 to 72.5 MHz. Levels range from about +16 dbm at the lowest frequency to about +12 dbm at the highest frequency. Output level of synthesizer equipped with modulator-oscillator 1RE1A2A2 or 5TR1A2A2, part number CMC 220-800159-000, ranges between +12.5 and +15.5 dbm.

(1) The voltage controlled oscillator (vco) contained in modulator-oscillator 5TR1A2A2, operates in the frequency range of 47.5 to 72.5 MHz in frequency steps of 125.0 kHz or 83.333 kHz. Two varactors are used to provide precise, instantaneous frequency control. One of the varactors causes frequency modulation of the output signal in response to input baseband signals. The second varactor controls the vco frequency in steps by the automatic frequency control voltage. In modulator-oscillator 1RE1A2A2 or 5TR1A2A2, part number CMC 220-800159-000, two varactors are used to control the vco frequency. A third varactor causes frequency modulation of the rf signal. The output of the oscillator circuit is stabilized by capacitor C20, amplified in a wideband amplifier and coupled, through a transformer and a metering detector, directly to the output connector for connection to amplifier-frequency multiplier 5TR1A4. A portion of the output signal is coupled through bandpass fil-

ter FL1 to the high speed dividers, contained in frequency divider 5TR1A2A4, or 5TR1A2A14.

(2) The high-speed dividers are three stages of binary dividers, the first in a chain of dividers, which are required to reduce the frequency of the vco to a range of frequencies which can operate the programmed counters. The frequency at the output of the high-speed dividers is the vco frequency divided by 8, (rf divided by 8), in the range 5.94 to 9.06 MHz. The output of the high speed dividers is further divided in a second group of three integrated microcircuit binary dividers, contained in digital electronic divider-counter 5TR1A2A5. The output of this second group of binary dividers is 0.742 to 1.13 MHz, (rf divided by 64). The rf signal at this point is a 4 volt peak-to-peak square wave and is applied through gate A in electrical synchronizer 5TR1A2A7 to the input stages of the programmed counter or to the input stages of electrical synchronizer 5TR1A2A17.

(3) The reference oscillator crystal frequency is 2.0 MHz; the reference oscillator is part of rf oscillator 5TR1A2Y1 (part of unlettered model). This frequency is divided by 1.0 MHz before being applied to a NOR gate, which is used to control the further division of the reference frequency. The 1.0 MHz is further divided by 2 or 3 depending on the absence or presence of control line 13. The output frequency of the reference oscillator, effectively 500 kHz or 333 kHz is then divided by a factor of 2,048 in an n-stage reference binary divide frequency divider 5TR1A2A9. The output of the reference divider circuit, a 4 volt peak-to-peak square wave at 244.14 Hz (divide-by-2 operation) or 162.5 Hz (divide-by-3 operation), is fed to the clock pulse generator circuit of electrical synchronizer 5TR1A2A7.

(4) The reference oscillator, part of rf oscillator 5TR1A2Y11, (part of A model) provides a crystal-controlled frequency of 16 MHz. The output of the crystal oscillator is then applied to a group of four binary dividers. The resultant 1.0 MHz signal is then applied to a circuit which performs a divide-by-two or divide-by-three function depending on the presence or absence of a code on control line 13. The output frequency of the divider circuit, a 500 kHz or 333 kHz square wave is further divided by a factor of 64 (in a six-stage binary divider) before it is applied to electrical synchronizer board 5TR1A2A17. The signal at this point is either a 7.82 kHz (divide-by-two) or 5.16 kHz (divide-by-three) 4 volt, peak-to-peak square wave.

(5) The clock pulse generator circuit (unlettered model ) produces clock pulses A, B, C and D to control the counters and the error pulse generator. Clock pulse B establishes the start count and end count moments. The end count moment is the reference time to which the full count is compared to produce error pulses. Clock pulse A gates the divider rf signal to the counter through gate A, permitting it to start counting at the start count moment. Clock pulse C is a reset function clearing (set to zero state) all counters, including the full count store prior to the start count moment. Clock pulse D is the preset function occurring immediately after clock pulse C. It sets the selected counter stages to one prior to the start count moment.

(6) In the electrical synchronizer 5TR1A2A17 (A model), the output frequency of the reference oscillator is further divided in a nine-stage binary divider (divided by 512). The last four binary dividers are part of the clock pulse generator circuit. The clock pulse generator circuit produces the four pulses which control the counters and the error pulse generator circuits. Clock pulse A gates the divided rf signal to the counter through a NAND gate at the start count moment. Clock pulse B

establishes the start and end count moments. Clock pulse C is applied to the clear direct (CD) input of all counters, including the full count store. Clock pulses D, occurring immediately after clock pulse C, is applied, either directly or through an AND gate, to the set direct (SD) input of all counter stages and sets the selected (programmed) counter stages prior to the start count moment.

(7) The programmed counter (unlettered model) consists of 16 stages of binary dividers of which 10 are programmed by control lines 3 to 12 from control-indicator 6A3. The other six stages are not programmed and are always preset to one by clock pulse A (first binary stage) or clock pulse D (binaries 2 - 6 inclusive). The first binary divider (not programmed) is contained in electrical synchronizer 5TR1A2A7; digital electronic counter 5TR1A2A6 contains nine binary dividers (both programmed and not programmed) and the remaining six programmed dividers are in digital electronic divider-counter 5TR1A2A5. The counter counts the frequency of the incoming signal, indicating a full count when all 16 binary outputs are in the one state. This state is sensed by a 16-input gate which generates a full count (-1) pulse to be applied to the error pulse generator. The function of the error pulse generator is to sense the full-count pulse and compare it to the end-count moment, generating a low-count or high-count error pulse if out of synchronization. The low- or high-count error pulses are fed into an error pulse integrator circuit (signal data converter-storer 5TR1A2A8) where they are converted to a dc voltage. This dc voltage is then applied to the vco as an automatic frequency control voltage. This voltage varies from about 2 volts at the 47.5 MHz end of the range to about 9 volts at the 72.5 MHz end of the range. In synthesizers equipped with modulator-oscillator 5TR1A2A2 or 1RE1A2A2, part number CMC 220-800159-000, the automatic frequency control voltage ranges between 4 and 8 volts approximately. The SYNC alarm circuit of amplifier-monitor 5TR1A2A3 operates the alarm relay if this voltage drifts outside these limits. The alarm relay circuits also operate in the absence of clock pulse D.

(8) In electrical synchronizer 5TR1A2A17 (A model), the next seven binary stages are contained in digital electronic counter 5TR1A2A16 and the remaining eight stages are contained in digital electronic divider-counter 5TR1A2A15. The 16-stages counter counts the frequency of the incoming signal, indicating a full count when all 16 binary outputs are in the high state. This state is sensed by a gate which, in turn, generates a full count (-1) pulse. The error pulse generator in electrical synchronizer 5TR1A2A17 (A model) senses the full count (-1) pulses and compares it (in time) to the end count moment. If the full count moment occurs (in time) after or before the end count moment (as determined by clock pulse B), a low count or high count error pulse, respectively, is generated. The low or high count error pulses are fed into an error pulse integrator circuit (signal data converter-storer 5TR1A2A18), where they are converted to a dc voltage which, in turn, is applied to the vco as an automatic frequency control (afc) voltage. The afc voltage determines the output frequency of the vco. The afc voltage for a vco output of 47.5 MHz is approximately 4 volts; an afc voltage of approximately 8 volts is required for an output frequency of 72.5 MHz.

(9) The SYNC alarm circuit of amplifier monitor 5TR1A2A3 operates an alarm relay if the afc voltage drifts outside the 4 to 8 volt limit. The alarm relay circuits also operate in the absence of clock pulse D, 5TR1A2A7 or 1RE1A2A7 for gating further division.

2-4. Modulator-Oscillator 5TR1A2A2 or 1RE1A2A2

a. Part No. CMC 456-260.

(1) General. This unit is one of the printed circuit board components of synthesizer 1RE1A2 or 5TR1A2. It operates as a voltage controlled oscillator (vco) in the frequency range of 47.5 to 72.5 MHz. The main frequency control, the automatic frequency control (aft) voltage, controls the vco frequency in discrete steps through frequency controlling circuits on other printed circuit boards in the synthesizer. These frequency controlling circuits are in turn controlled by the frequency code in the channel selector, and are referenced to a crystal oscillator. A second frequency controlling voltage, the modulation signal, is used to frequency modulate the output signal when the synthesizer is mounted in a transmitter. This facility is not used when the synthesizer is mounted in a receiver.

(2) Block diagram analysis (Fig. 2-3).

(a) The basic oscillator is a modified Hartley circuit having two varactors acting as capacitors in the parallel resonant circuit. The automatic frequency control voltage from amplifier-monitor 5TR1A2A3, in the range of 2 to 9 volts, controls the capacity of one of the varactors over its required range. The ac modulating voltages from amplifier-monitor 5TR1A5 control the capacity of the second varactor over its required range, the modulating signal level depending upon the type of multiplex system in use. Modulation signals are attenuated within amplifier-monitor 5TR1A5 to maintain transmitter output frequency deviation constant as the multiplication factor is changed. The two varactor capacitors then resonate with a variable coil which is tapped to provide a feedback signal to the base of the oscillator transistor. The afc feedback loop can be open during set-up for test and adjustment purposes.

(b) The oscillator output is amplified in a two-stage amplifier which employs feedback to extend the frequency response over the frequency range. A broadband matching transformer at the amplifier output feeds the signal to bandpass filter 5TR1A2A1A1FL1 on the synthesizer interconnecting board, one portion going directly to the output connector, and the other portion going to the frequency comparison circuits to generate the afc voltage. A variable capacitor at the amplifier adjusts the level of the output signal over the frequency range. A portion of the output signal is rectified to provide metering of the output level. The output frequency, in the range of 47.5 to 72.5 MHz, is in steps of 1230.0 kHz over a portion of the

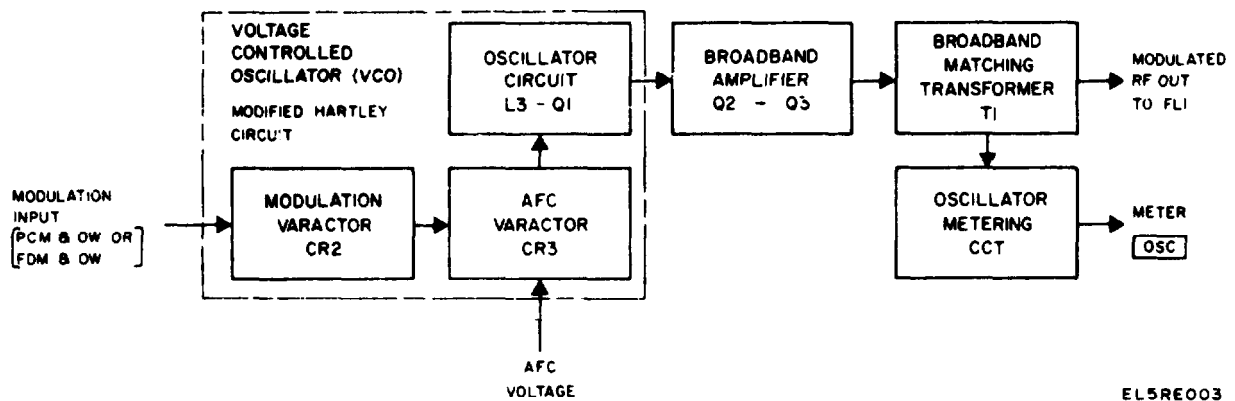


Figure 2-3. Modulator-Oscillator 5TR1A2A2 or 1RE1A2A2 (Part No. CMC 456-260), Block Diagram.

band and in steps of 83.333 kHz over the remainder. The frequency steps are related to multiplication factors of four and six respectively. The level of output level of the signal varies from +16 dbm at the 47.5 MHz end of the frequency range to +12 dbm at the 72.5 MHz end.

(3) Circuit diagram analysis (F0-4-5). Q1 is the oscillator transistor. The feed back signal is coupled from the collector through C8 and L2 to L3, and from a tap on L3 through C9 back to the base of Q1. The tuned circuit consists of L3, CR2 and CR3. C4 and C5 are dc blocking capacitors and L1 is an rf block to prevent loss of the modulator signal on the power supply line. CR2 is the modulation varactor and CR3 is the afc varactor. VARICAP TUNE coil L3 is adjusted during alinement to tune the circuit at each end of the range, with a test voltage applied to the afc varactor.

(a) Afc voltage is fed from pin 5 to J2 through TEST-NORMAL switch S1, R10, and L3 to CR3. TEST-NORMAL switch S1 is a maintenance provision to permit the afc feedback loop to be broken during alinement. Setting this switch to the TEST position applies a test voltage to the afc varactor in place of the normal afc voltage. The value of the test voltage can be varied by MANUAL FREQUENCY CONTROL resistor R4.

(b) Modulation is fed from pin 12 of J2 through MODULATION SENSITIVITY resistor R9 and then through C3 to L1 to CR2. Fixed bias for CR2 is established at the junction of R1 and R2, and applied to CR2 through MODULATION COMPENSATION control R6. The capacity of CR2, the modulation varactor, acts as a trimmer capacitor in parallel with CR3 capacity and provides a modulation frequency shift to the oscillator circuit which offsets the non-linear reaction of CR3 over the frequency range. As the frequency is increased across the rf range, the voltage on CR3 is increased, decreasing its capacity.

(c) Modulation varactor CR2, having fixed bias, and therefore fixed capacity across the range, assumes a larger percentage of the total tuned circuit capacity at the top end of the range. The capacity variation that results from the modulating signal then provides a fixed capacity swing over the entire range, resulting in a linear modulation sensitivity. The value of the fixed bias on the modulation varactor is adjusted by modulation compensation control R6, to insure correct modulation linearity over the tuning range. The level of the modulating signal applied to the varactor is adjusted by modulation sensitivity control R9.

(d) At the bottom end of the frequency range, the afc varactor CR3 capacity change per volt tends to become more sensitive, resulting in a non-linear frequency shift with afc voltage change. To counteract this effect, diode CR1 is connected between the afc input voltage and a fixed bias point. Thus, as the afc approaches the 2 volt end of the range, a small amount of voltage is fed through the diode to the afc line trying to pull the vco off frequency. This tendency is sensed in the normal afc loop as a frequency error and results in a more negative afc feedback voltage, resulting in a linear afc control at the low end of the frequency range. RT1 insures that this extra afc voltage is not bled off through CR1.

(e) The oscillator output signal is coupled through coupling capacitor C13 to the base of Q2. From the Q2 collector the signal is directly coupled to the Q3 base, and from the Q3 collector to matching transformer T1. Negative feedback is coupled from the Q3 emitter to the Q2 base to extend the frequency response of the amplifier. A portion of the output signal is fed through C17 to CR4, where it is rectified to produce a dc metering signal.



b. Part No. CMC 220-800159-000.

(1) General. This unit functions identically with that of modulator-oscillator 5TR1A2A2 or 1RE1A2A2, part No. CMC 456-260. This unit has been redesigned to give better modulation sensitivity linearity, a reduction in output level variation and improved interchangeability.

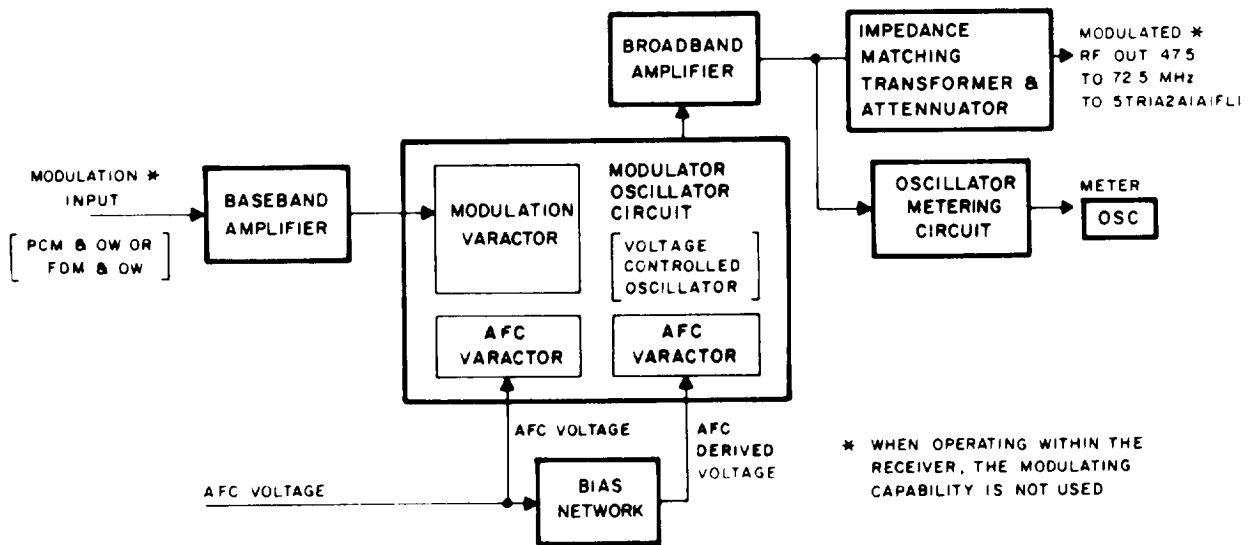
(2) Block diagram analysis (Fig. 2-4).

(a) The basic oscillator is a modified Hartley circuit. Two varactor diodes in the oscillator tuned circuit provide the rf changing function. An afc voltage, which is a function of the vco output frequency, is fed to the afc varactor from amplifier-monitor 5TR1A5. This dc voltage ranges from 4 to 8 volts and varies the capacity of the afc varactor to produce frequencies from 47.5 to 72.5 MHz. An ac modulating voltage from amplifier-monitor 5TR1A5 is amplified in the baseband amplifier and applied to the modulation varactor. The capacity of the modulation varactor varies with the modulating voltage and results in frequency modulation of the oscillator signal. The bias network is adjusted to provide linear modulation sensitivity across the operating frequency band.

(b) The oscillator output is amplified in a broadband amplifier having a high impedance input and push-pull output. The impedance matching transformer is required for proper matching of the modulator-oscillator to amplifier-frequency multiplier 5TR1A4. The output attenuator is also required for impedance matching and provides a load for the output transistors. A portion of the output rf signal is rectified to provide metering of the output level which varies from +12.5 dbm to +15.5 dbm.

(3) Circuit diagram analysis (F0-4-6).

(a) The oscillator transistor is Q1. The feedback signal is coupled from the collector through C5, L2 and C6 to Q1 emitter. The tuned circuit consists of CR2, CR4, L2 and C10. The capacitance of varactor diode CR2 changes as the afc voltage



EL5RE004

Figure 2-4. Modulator-Oscillator 5TR1A2A2 or 1RE1A2A2 (Part No. CMC 220-800159-000), Block Diagram.

changes. The oscillator operating frequency ranges from 47.5 to 72.5 MHz as the afc voltage changes from +4 to +8 volts. Capacitor C10 presents a low impedance to modulating signals and a high impedance to circulating rf signals. Biasing for CR2A and CR2B is designed to produce constant modulation sensitivity as rf is changed. Bias is applied to CR2A through R2, R3, R10 and R12. Bias for CR2B is applied through R2, R3, R4 and L4. Inductors L1, L3, L4 and L5 present a high impedance to the rf signal.

(b) Resistor R6 controls the level of modulating signals applied to the base of baseband amplifier Q2, thus setting the required peak fm deviation. Resistors R11 and R13 are bias resistors. Diode CR8 and resistor R32 provide a clamping voltage and spurious signal rejection for Q2 collector. Diode CR1 and resistor R9 perform a similar function for Q1 collector. Resistor R37 and diode CR10 limit the frequency of operation at the lower afc voltage range to 41 MHz. This action prevents the synthesizer from locking on to a false loop.

(c) Transistors Q3, Q4, Q5 and Q6 make up the broadband amplifier. Transistor Q3 is a N-channel field effect transistor (FET) which has a high input impedance to prevent loading the oscillator tuned circuit. Emitter follower Q4 provides a low source impedance to drive the low impedance output transistor. Transformer T1 phase inverts the input signal to output transistor Q6. Under large signal conditions, each output transistor conducts at different parts of an input cycle. Transistors Q5 and Q6 are arranged in a push-pull configuration to improve the broadband noise. Transformer T2 phase inverts the output signal from Q6. Transformer T3 presents the correct impedance to the input of the next subassembly 5TR1A4. Resistors R34, R35 and R36 form a 2 db, pi-type attenuator to improve the output vswr, reduce the effect of output impedance variation and decrease the absolute level of broadband noise at the output. It also provides a load for the output transistors when the synthesizer output is open-circuit. The output power level is adjustable by R25 which varies the base potential and consequently the collector voltage of Q5 and Q6. A portion of the output power is detected in CR6, R29, CR7, R30 and C30 to provide a meter indication of output power. All decoupling of transistor stages is provided by the 0.1 uf capacitors. Capacitors C4 and C33 prevent spurious signals from appearing on the power supply lines. Inductors L6, L7, L8 and L9 improve the output impedance from 47.5 to 60 MHz. Resistor R26 and diodes C21 and CR5 stabilize any power supply variations:

## 2-5. Rf Dividers, Functional Analysis

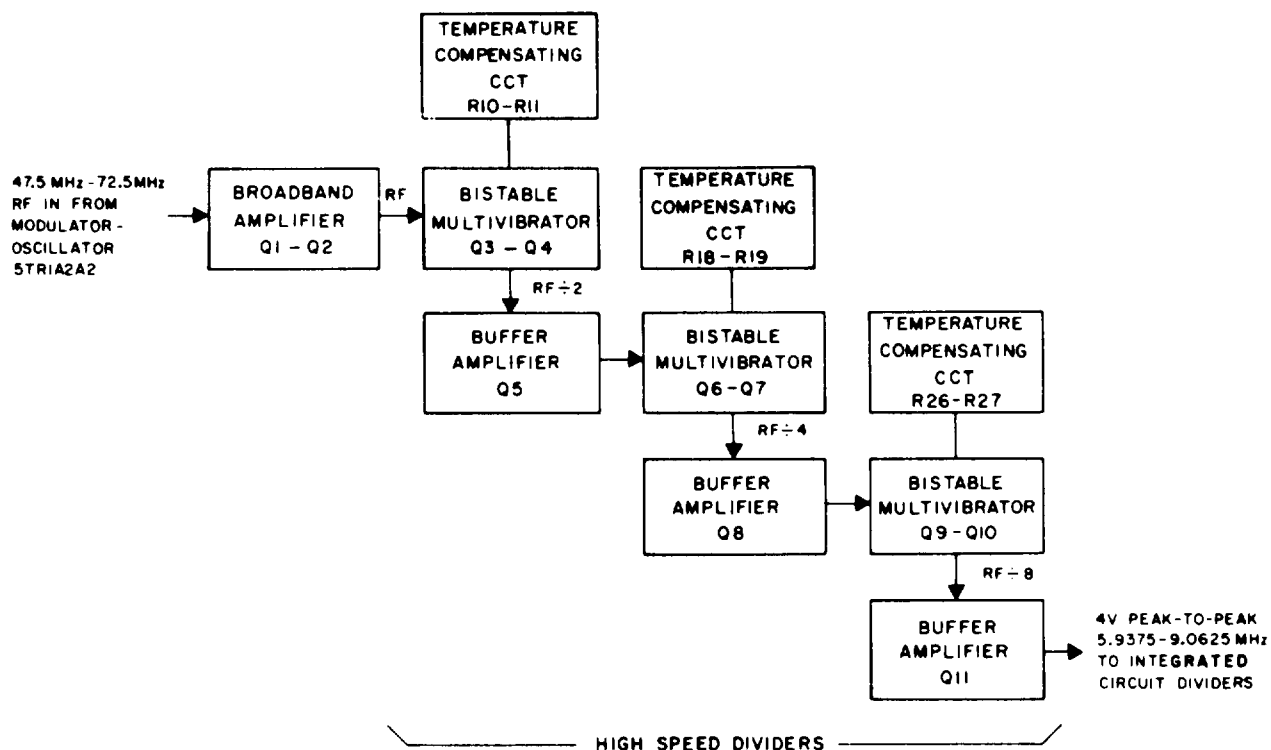
The frequency of the signal fed to the programmed counter must be approximately 1 MHz to provide the required frequency resolution with the counter. The signal fed to the programmed counter is derived from modulator-oscillator 5TR1A2A2 output frequency (rf output in the range of 47.5 to 72.5 MHz) by frequency division accomplished in six stages of binary dividers (F0-4-1). These high speed dividers are mounted, together with a two-stage broadband amplifier, on frequency divider 5TR1A-2A4 or 1RE1A2A4. The final three stages of division take place in microcircuit (integrated) binary dividers, which are mounted on digital electronic divider-counter 5TR1A2A5 or 1RE1A2A5. The output of the divider chain (rf divided by 64) is a square wave signal at 4 volts peak-to-peak in the frequency range of 0.7 to 1.13 MHz, which is then fed to electrical synthesizer 5TR1A2A7 or 1RE1A2A7 for gating and further division.

2-6. Frequency Divider

a. Model No. 5TR1A2A4 or 1RE1A2A4.

(1) General. Part of the output signal of the modulator-oscillator (rf output) is coupled through splitter filter 5TR1A2A1FL1 or 1RE1A2A1FL1 to the input of frequency divider 5TR1A2A4 or 1RE1A2A4. The filter prevents harmonics generated in the high speed dividers being fed back to amplifier-frequency multiplier 5TR1A4 or 1RE1A5.

(2) Block diagram analysis (Fig. 2-5). A low level sample of the rf output is first amplified in a two-stage broadband amplifier. The amplifier output is then coupled to the first bistable multivibrator. The negative-going transition of each cycle of input signal causes the multivibrator to switch to one side; the next negative-going transition of input signal causes the multivibrator to switch to the other side. Positive-going transitions cannot initiate the switching action since they are not high enough to override the negative voltage which is holding the transistor off. The multivibrator circuit is temperature-compensated to insure reliable switching over the temperature range of -40 degrees C to +80 degrees C. The output of the multi vibrator, a square wave at half the frequency of the input signal, is then fed through a single stage buffer amplifier to the next bistable multivibrator circuit. The second and third multivibrator circuits are identical to the first; a single stage buffer amplifier couples the signal between the second and third divider. The output of the third divider circuit is coupled to the output connector through a third single stage buffer amplifier. The output signal (rf divided by 8)



EL5RE005

Figure 2-5. Frequency Divider 5TR1A2A4 or 1RE1A2A4 (Unlettered Model), Block Diagram.

is then fed to the next three dividers of the divider chain which are located on digital electronic divider-counter 5TR1A2A5 or 1RE1A2A5.

(3) Circuit diagram analysis (F0-4-7). The input signal at J3 pin 15, in the range of 47.5 to 72.5 MHz is fed through a 5.6 pf capacitor to the base of Q1 the first stage of the broadband amplifier. The coupling capacitor has a small value to prevent loading of modulator-oscillator 5TR1A2A2 or 1RE1A2A2 output.

(a) Q1 output is coupled to Q2 base through C2. CR1 in the base circuit of Q2 provides base over-voltage protection by limiting the negative voltage swing. The amplifier output is then coupled from a common feed point to the bases of both sides of bistable multivibrator, Q3 and Q4.

(b) The signal at the Q2 collector is fed through C4, R8, L1 and C5 to the Q4 base, and through C4, R13, L2 and C6 to the Q3 base. The negative transition of the signal will tend to lower the base voltage of Q3 and Q4. If Q4 is conducting, the Q3 base will be near ground potential; the negative voltage will not affect it. The Q4 base, however, will drop, causing its collector and the Q3 base to rise, resulting in a reversal of the conducting states of Q3 and Q4. The next negative swing of input signal will then reverse the states again, resulting in an output signal at the Q4 collector at half the frequency of the input signal. L1 L2, C5 and C6 speed up the switching action of the multivibrator.

(c) As the surrounding temperature increases, the current of a transistor increases; therefore, less collector voltage is required to saturate a transistor at a higher temperature. Overdriving the transistors would cause a recovery delay, resulting in unreliable dividing action at high temperatures. To overcome this, the collector voltage of Q3 and Q4 is fed through thermistor R11, which has a positive temperature coefficient to increase resistance and lower the collector voltage at high temperatures. TEMP COMP control R10 is used to adjust the collector voltage at the temperature extremes to insure reliable counting.

(d) The output from the Q4 collector is fed through C7 to the base of buffer amplifier Q5. Output from Q5 is then fed through C8 to Q6 and Q7, the second divider. This divider operates exactly like the first divider, Q3 and Q4. Similarly, this divider is followed by buffer amplifier Q8, feeding the third divider Q9, and Q10. Q11 is a third buffer amplifier whose output is connected directly to pin 1 on J3.

(e) The output signal, a 4 v peak-to-peak square wave in the frequency range of 5.9375 to 9.0625 MHz, is then fed through J3 pin 1 and J5 pin 1 of the interconnecting box to digital electronic divider-counter 5TR1A2A5 or 1RE1A2A5 for further division (para 2-12a).

(f) Test points TP1 (ground) and TP2, TP3 and TP4 permit the monitoring of input signals to each of the high speed dividers.

b. Model No. 5TR1A2A14 or 1RE1A2A14 (A Model).

(1) General. Modulator-oscillator 5TR1A2A2 output frequency (in the range of 47.5 to 72.5 MHz) is divided in six stages of binary dividers to a frequency in the range of 0.742 to 1.133 MHz; this process provides the required frequency resolution within the programmed counter. The six binaries are mounted, together with a band-pass filter and harmonic rejection circuits, on frequency divider board 5TR1A2A12 or 1RE1A2A14.

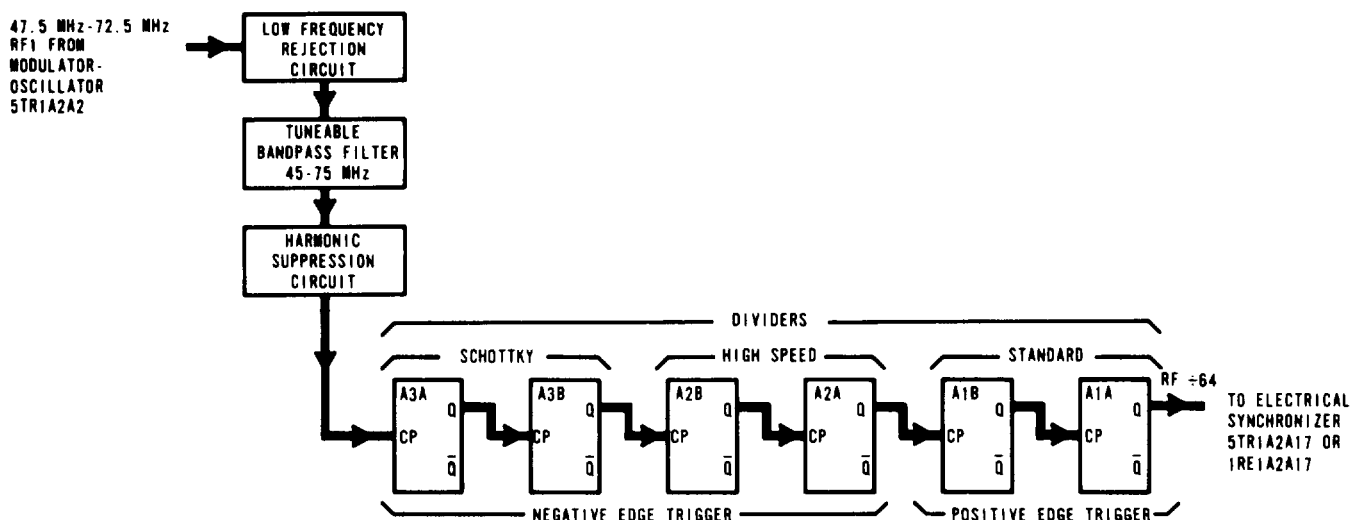
(2) Block diagram analysis (Fig. 2-6). A sample of the rf output from the modulator-oscillator is fed through a low-frequency rejection circuitry to a tunable bandpass filter section, then to a harmonic suppression section; these circuits provide a minimum of 90 db rejection at 30 MHz (if frequency). The output of the filter is fed into a string of six binary dividers and the output signal (rf divided by 64) is then fed to electrical synchronizer 5TR1A2A17 or 1RE1A2A17.

(3) Circuit diagram analysis (FO-4-8). The input signal at J3 pin 15, in the range of 47.5 to 72.5 MHz, is fed through C1 to the base of Q1. L1 matches input to output of the vco. The output of the Q1 is fed through a tunable bandpass filter to the emitter of Q2. L4 tunes the bandpass filter circuitry for amplifier frequency response from 45 - 75 MHz. R10 is a stabilizing resistor, preventing parasitic oscillations. Q2 and Q3 provide 55 db rejection of the 30 MHz signal. Q3 amplifies and squares the analog rf signal so as to drive the first divider. The overall rejection of the filter is in excess of 90 db. The filter output is fed into the CP input of binary A3A, one half of a dual pack Schottky J-K flipflop. The Q outputs of the first three binaries are fed to the CP input of the following binary. The Q outputs of A2A and A1B are fed to the CP input of the following binary. The Q output of A1A (rf divided by 64) is connected to J3 pin 4 and fed to electrical synchronizer boards. A2B and A2A are high power dual pack J-K flipflops. A1B and A1A are standard dual pack J-K flipflops. The first 4 binaries use negative-edge trigger, A1B and A1A positive-edge trigger. The J, SD and CD inputs of all binaries are connected to the +5 v line. The K inputs on the first 4 binaries are also connected to +5 v. The K inputs of A1B and A1A are connected to ground. L7, L9, R16, C11, C12 and C16 filter the 11.5 vdc line; L8, R17, C13, C14, C15 filter the +5 vdc line.

2-7. Rf Oscillator

a. Model No. 5TR1A2Y1 or 1RE1A2Y1.

(1) General . This unit provides the basic crystal-controlled frequency to which each selected synthesizer output frequency is referenced. Clock pulses that control the programmed counters in the synthesizer are derived from this basic crystal-controlled reference frequency by frequency division.



EL5RE006

Figure 2-6. Frequency Divider 5TR1A2A14 or 1RE1A2A14 (A Model), Block Diagram.

(a) It is necessary for the clock pulses to have a very low repetition rate, in order that the modulator-oscillator 5TR1A2A2 or 1RE1A2A2 rf output can be frequency modulated while still being controlled by the programmed counter. The first division in the clock pulse generating chain takes place within rf oscillator board 5TR1A2Y1 or 1RE1A2Y1.

(b) The output frequency steps of the synthesizer are changed as the overall frequency-multiplication factor is changed in the middle of the band. This is accomplished by changing the division factor (divide-by-2 or divide-by-3 function) within the reference oscillator unit, thus changing the widths of the clock pulses. The divide-by-2 to divide-by-3 change-over is initiated by control line 13 from control-indicator 6A3 or 2A2.

(2) Block diagram analysis (Fig. 2-7 and 2-8). The basic oscillator circuit consists of a three-transistor amplifier with a 2.0 MHz crystal feedback loop. An adjustable coil, in series with the crystal, provides adjustment of the crystal frequency over a narrow range. A temperature-compensating circuit consisting of a varactor in series with the crystal and two thermistors, keeps the basic crystal frequency free from drifting over a temperature range of -30°C to +75°C. The output of the oscillator section is a 2.0 MHz signal at about 4 volts peak-to-peak. This signal is fed to the toggle input of microcircuit binary divider A1; the binary divider outputs, 1 MHz square waves, 4 volts peak-to-peak each, are in antiphase. The two antiphase 1 MHz signals are fed one to each half of dual NOR gate microcircuit A2. One of the two NOR gates inverts the input signal, which is then applied to the toggle input of microcircuit binary divider A3. The other half of NOR gate A2 is held inactive during the divide-by-2 operation.

(a) Divide-by-2 operation (Fig. 2-7). The 1.0 MHz square wave signal applied to the toggle input of binary A3 is divided by a factor of two. The 500 kHz square wave output is then applied simultaneously to binary A4 (inactive during the divide-by-2 operation) and to one half of NOR gate A5; the second input to NOR gate A5 is inactive during the divide-by-2 operation. The output of NOR gate A5, during the divide-by-2 operation, is a 500 kHz square wave, 4 volts peak-to-peak.

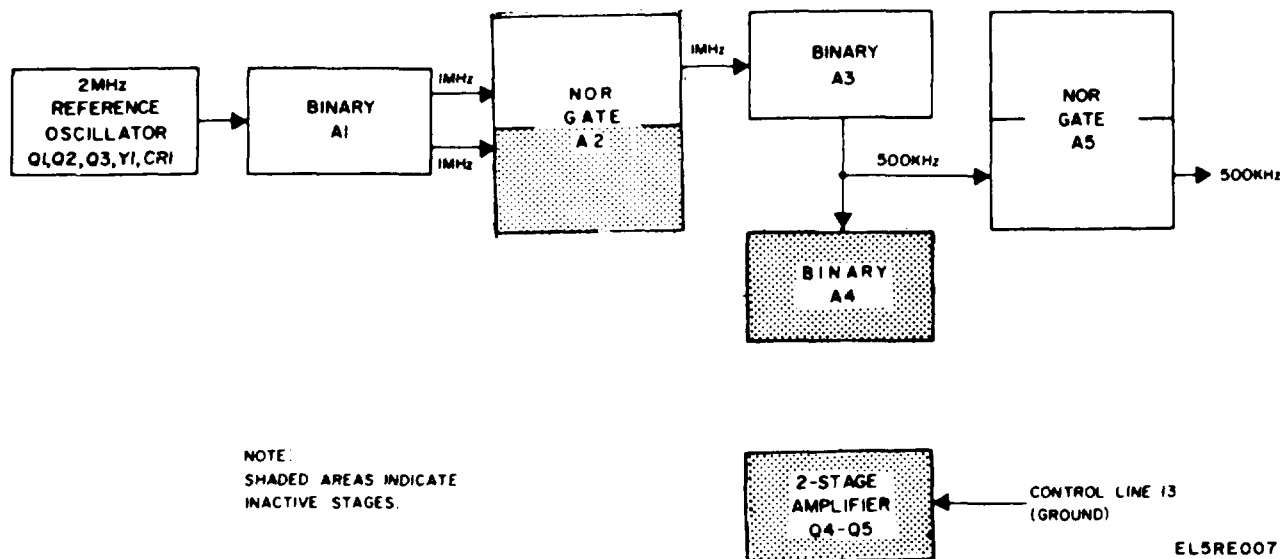


Figure 2-7. Rf Oscillator 5TR1A2Y1 or 1RE1A2Y1, Divide-By-Two Function, Block Diagram.

(b) Divide-by-3 operation (Fig. 2-8). The divide-by-3 operation is initiated by control line 13 of control-indicator 6A3 or 2A2 when set for channels 180 and above. For channels 180 and above, control line 13 is supplied with a positive voltage; for channels 179 and lower, control line 13 is grounded. The positive voltage supplied on control line 13 is first amplified in a two-stage amplifier after which it is applied to the input of binary divider A4, activating it. The toggle input to binary A4 is the 500 kHz output of binary divider A3 ((1) above). The output of binary A4 is a 250 kHz signal which is then fed as the other input to the second half of NOR gate A2; the first input being the 1.0 MHz output of the binary A1. The 1.0 MHz signal gated by 250 kHz at the output of NOR gate A2 is then applied to the reset input of binary A3. The output of binary A3 in the divide-by-3 operation is a 500 kHz signal gated by 1.0 MHz; this signal is fed simultaneously to the toggle input of binary A4 and to one half of dual NOR gate A5. The second output of binary A4 (activated in the divide-by-3 operation) is also fed to NOR gate A5, where it gates the output of binary A3. The output of NOR gate A5 is a positive pulse 2 microseconds long followed by a negative pulse 1 microsecond long, which is effectively a 333 kHz signal.

(3) Detailed circuit analysis (FO-4-18). Transistors Q1, Q2 and Q3 form a 2 MHz crystal-controlled oscillator. Feedback is coupled from the Q3 emitter through Y1, R6, L2, L1, CR1 and C1 to the base of Q1. The frequency adjustment control, L1, provides crystal frequency trimming at normal room temperature. Varactor CR1 is used to provide temperature compensation control of the crystal frequency over the operating temperature range of -30°C to +75°C, since the crystal frequency would tend to drift by about 40 Hz at the temperature extremes. The low temperature control, R2, is used to adjust the CR1 bias to provide an exact crystal frequency at -30°C. The high temperature control, R1, is used to adjust the bias applied through thermistor R3 to CR1 at +75°C, to pull the crystal frequency to exactly 2.0 MHz at that temperature.

(a) The oscillator output signal is coupled through C4 to pin 10 (toggle input) of binary divider A1. The outputs at pins 8 and 3 are two antiphase 1.0 MHz square wave signals at 4 volts peak-to-peak. The output at pin 8 of A1 is connected

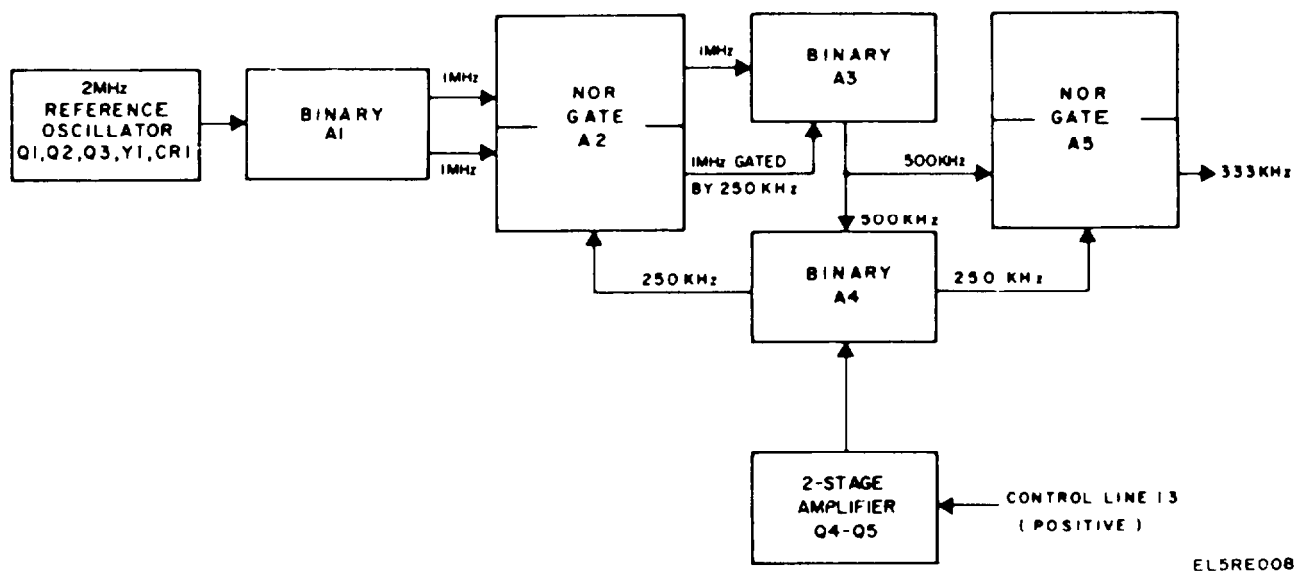


Figure 2-8. Rf Oscillator 5TR1A2Y1 or 1RE1A2Y1, Divide-By-Three Function, Block Diagram.

to pin 9 of dual NOR gate A2 and the signal at pin 3 of A1 is connected to pin 3 of A2, one of the inputs of the second NOR gate A2, which is cut off by a negative voltage on pin 5 during the divide-by-2 operation.

(b) The output from pin 10 of A2 is connected to the toggle input, pin 10, of binary divider A3. The output of divider A3 at pin 8 is a 500 kHz square wave signal at 4 volts peak-to-peak, which is then fed simultaneously to pin 3 of dual NOR gate A5 and to the toggle input of binary divider A4, held inactive during the divide-by-2 operation. The input at pin 4 of NOR gate A5 is a positive voltage (output of binary A4, pin 3). The output of NOR gate A5, a 500 MHz square wave from pin 2, is then connected directly to J10, pin 7, and on to the reference dividers on frequency divider 5TR1A2A9 or 1RE1A2A9.

(c) The divide-by-3 function is initiated when line 13 of control-indicator 6A3 or 2A2, connected to J10 pin 8, has a positive voltage on it. This voltage is connected through R18 to the base of Q5. The Q5 collector is connected to the base of Q4. The Q4 collector is connected to set input, pin 7 of binary divider A4, making it active.

(d) The output at pin 8 of binary A4 is fed into pin 5 of NOR gate A2 and is gating the 1.0 MHz square wave. The output at pin 2 of NOR gate A2 is a 0.5 microsecond pulse which is then fed into pin 4 of binary A3 and gates the 1.0 MHz trigger pulse arriving at pin 10 of A3. The result at pin 8 is a 1.0 MHz square wave followed by a 500 kHz square wave, giving the equivalent of a 3 microsecond square wave. This output is applied to pin 10 of binary A4, causing it to change state on the down clock. The binary A4 outputs at pins 3 and 8 are antiphase 333 kHz asymmetrical square waves. The output at pin 8 of A4 is fed into NOR gate A2 pin 5, where it is gated by the 1.0 MHz square wave arriving at pin 3. The output at pin 3 of binary A4 is fed to pin 4 of NOR gate A5, where it gates the 1.0 MHz square wave, followed by the 500 kHz square wave output fed into pin 8 of binary A3. The output at pin 2 of NOR gate A5 is an asymmetrical 333 kHz square wave. Binaries A3 and A4 as described above form a scale-of-three divider. The square wave is positive for 2 microseconds and negative for 1 microsecond. The output from pin 2 of A5 is connected through J10 pin 7 and J9 pin 7 to frequency divider 5TR1A2A9 or 1RE1A2A9.

b. Model No. 5TR1A2Y11 or 1RE1A2Y11 (A Model).

(1) General . This unit provides the basic crystal-controlled frequency to which each selected synthesizer output frequency is referenced. Clock pulses, that control the counter in the synthesizer, are derived from the basic crystal-controlled reference frequency by frequency division.

(a) It is necessary for the clock pulse to have a very low repetition rate so that modulator-oscillator 5TR1A2A2 or 1RE1A2A2 rf output can be frequency-modulated while still being controlled by the program counter. The first division in the clock pulse generating chain takes place within rf oscillator board 5TR1A2Y11 or 1RE1A2Y11.

(b) The output frequency-steps of the synthesizer are changed as the overall frequency multiplication factor is changed in the middle of the band. This is accomplished by changing the division factor (divide-by-2 or divide-by-3 function) within the reference oscillator unit, thus changing the widths (time) of the clock pulses. The divide-by-2 to divide-by-3 changeover is initiated by a code on control line 13 from control-indicator 6A3 or 2A2. The changeover point (transmitter) occurs between channels 179 (divide-by-two) and 180 (divide-by-three).



(2) Block diagram analysis (Fig. 2-9). The rf oscillator board consists of a crystal-controlled oscillator operating at 16 MHz, followed by a divider chain. The crystal is housed in a temperature-controlled oven, at a constant temperature of  $115^{\circ}\text{C} \pm 6^{\circ}\text{C}$ . Over this temperature range, the crystal stability is 4 parts per million (PPM). The crystal frequency itself can be adjusted over a narrow range (approximately 130 PPM) thus compensating for aging and differences between crystals. The 16 MHz square wave is then divided in a group of four binary dividers; the first two binaries of this divider chain, are high speed flipflops, the next two are low power flipflops. The resulting 1 MHz square wave, 2 volts peak-to-peak, is fed into the divide-by-2 or divide-by-3 circuits; the 500 kHz (channels below 179) or the 333 kHz (channels 180 and above) square wave output is further divided in a six-stage binary divider before it is fed into electrical synchronizer 5TR1A2A17 or 1RE1A2A17.

(3) Detailed circuit analysis (FO-4-19). Transistors Q1 and Q2, together with crystal Y1, form a 16 MHz crystal-controlled Butler oscillator. The Klixon oven which houses the crystal insures a constant operating temperature within  $6^{\circ}\text{C}$ , centered about  $115^{\circ}\text{C}$ . Series capacitor C5 compensates for the setting and aging tolerance of the crystal, and R7 insures correct drive to the crystal.

(a) The oscillator output is fed to the base of Q3, which converts the oscillator output into a square wave, approximately 4 volts peak-to-peak. Q3 output is connected through test link WT1-WT2 to the clock pulse (CP) input of binary divider A6A, A6A and A6B are high speed flipflops using negative-edge triggering. A4B and A4A binaries are low power flipflops and use positive edge triggering.

(b) The 1 MHz output of binary A4A is fed simultaneously to the CP inputs of binaries A2A and A2B, A2A and A2B, together with gate A7D, form the divide-by-two or divide-by-three circuit. In the divide-by-two mode, control line 13 at pin 9 is ground, switching transistor Q4 is cut off, and a High (H) is applied to the inputs of NAND gate A7C. The resulting Low (L) applied to NAND gate A7D insures that pin J of A2A is always H. The 1 MHz square wave applied to A2A is divided in the normal manner, and the 500 kHz output at the Q output of A2A is then divided by six binary dividers. The Q output of binary A5B is fed through A7A (for increased current-carrying capacity) and the 7.8125 kHz, 4 volt peak-to-peak square wave is applied through pin 13 to electrical synchronizer 5TR1A2A17 or 1RE1A2A17.

(c) The divide-by-3 function is initiated when line 13 from control indicator 6A3 or 2A2, at pin 9, has a positive voltage on it. This voltage is applied through R14 to the base of switching transistor Q4 which is now conducting. The collector

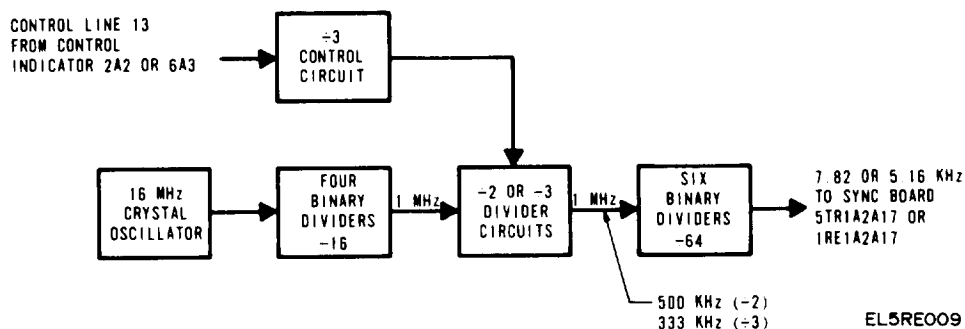


Figure 2-9. Rf Oscillator 5TR1A2Y11 or 1RE1A2Y11, Block Diagram.

output (L) is inverted in A7C which in turn holds one input of A7D at H. The other input to A7D is the Q output of binary A2B. The output of A7D, alternately H and L, now gates binary A2A. The Q output, an asymmetrical square wave with an up-clock occurring every 3 microseconds (333 kHz), is then fed to the same group of six binary dividers ((b) above). The output, this time a 5.2083 kHz, 4 volt peak-to-peak square wave is then inverted in A7A before being fed to electrical synchronizer 5TR1A2A17 or 1RE1A2A17.

## 2-8. Frequency Divider 5TR1A2A9 or 1RE1A2A9

### NOTE

Not used in A model.

a. General. The frequency divider board provides 11 stages of binary division of the 500 kHz or 333 kHz reference signal from rf oscillator 5TR1A2Y1 or 1RE1A2Y1. The signal at the output of the frequency divider is then applied to electrical synchronizer 5TR1A2A7 or 1RE1A2A7, where it is used to generate the clock pulses required for referencing, gating, set and reset operation.

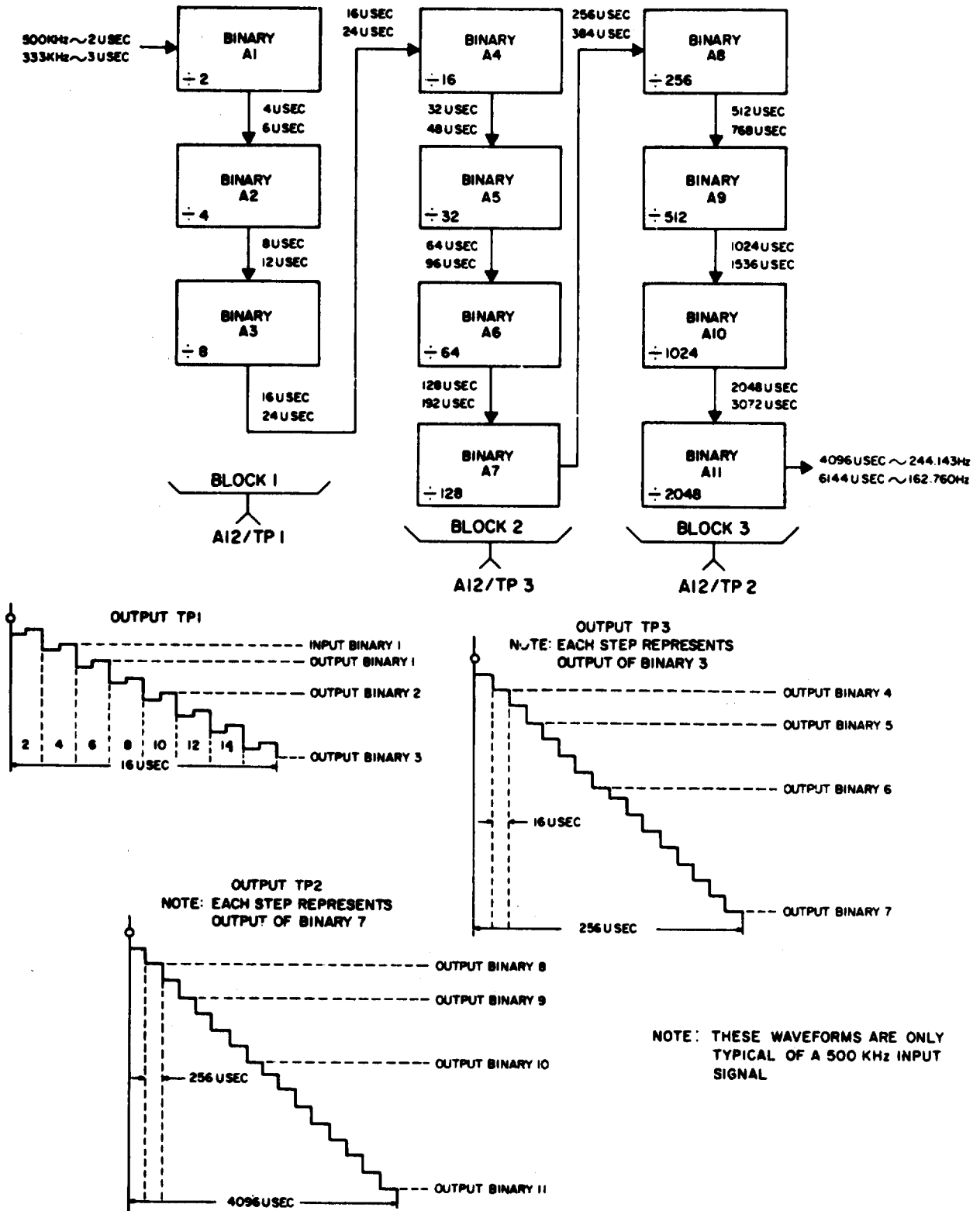
b. Block Diagram Analysis (Fig. 2-10). The input to the frequency divider is a 500 kHz square wave at 4 volts peak-to-peak over the times-4 portion of the band, and alternate half-cycles of 250 kHz and 500 kHz at 4 volts peak-to-peak over the times-6 portion of the band. The times-6 signal has negative-going transitions spaced 3 microseconds apart, which makes the signal look like 333 kHz to a binary divider. The 11 binaries are connected in a cascade to provide a total division of the input signal by 2,048. The output signal is a 244.14 Hz (times-4 portion of the band) or 162.75 Hz (times-6 portion of the band) square wave at 4 volts peak-to-peak. Three test points provide sources for displaying the signal, in three separate groups, as it is divided by each binary.

c. Circuit Diagram Analysis (F0-4-17). The 500 kHz or 333 kHz signal is fed through C1 to toggle input pin 10 of binary microcircuit divider A1. The binary divider is a bistable multivibrator which will flip from one state to the other when pin 10 input goes negative. The output at pin 8 of binary A1, a 4 volts peak-to-peak square wave at half the frequency of the input signal, is fed directly to the toggle input of binary A2, and so on. The output of binary A11 is coupled through C3 to pin 8 of J9 and on to electrical synchronizer 5TR1A2A7 or 1RE1A2A7. The input signal and the outputs of binaries A1, A2 and A3 are fed in parallel, through R1, R2, R3 and R4 respectively, to A12/TP1, a monitor point which provides a means of displaying the counting cycle on an oscilloscope. R1, R2, R3 and R4 are of different values to provide an oscilloscope presentation in the form of descending steps (fig 2-10); this facilitates identification of each signal. In a similar manner, the outputs of binary dividers A4 to A7 are connected to A12/TP3 and the outputs of binary dividers A8 to A11 are connected to A12/TP2.

## 2-9. Electrical Synchronizer

### a. Model No. 5TR1A2A7 or 1RE1A2A7.

(1) General. This unit performs two major functions within the synthesizer. The first function is the generation of clock pulses A, B, C and D. The second is the gating of the full count pulse, generated within the counter, to produce high count or low count error pulses. The error pulses then generate an afc voltage



EL5RE010

Figure 2-10. Frequency Divider 5TR1A2A9 or 1RE1A2A9, Block Diagram.

which locks the modulator-oscillator frequency to the selected channel frequency. This unit also gates the modulator-oscillator rf signal applied to the counter circuits; the first binary divider of the counter is also part of the electrical synchronizer board.

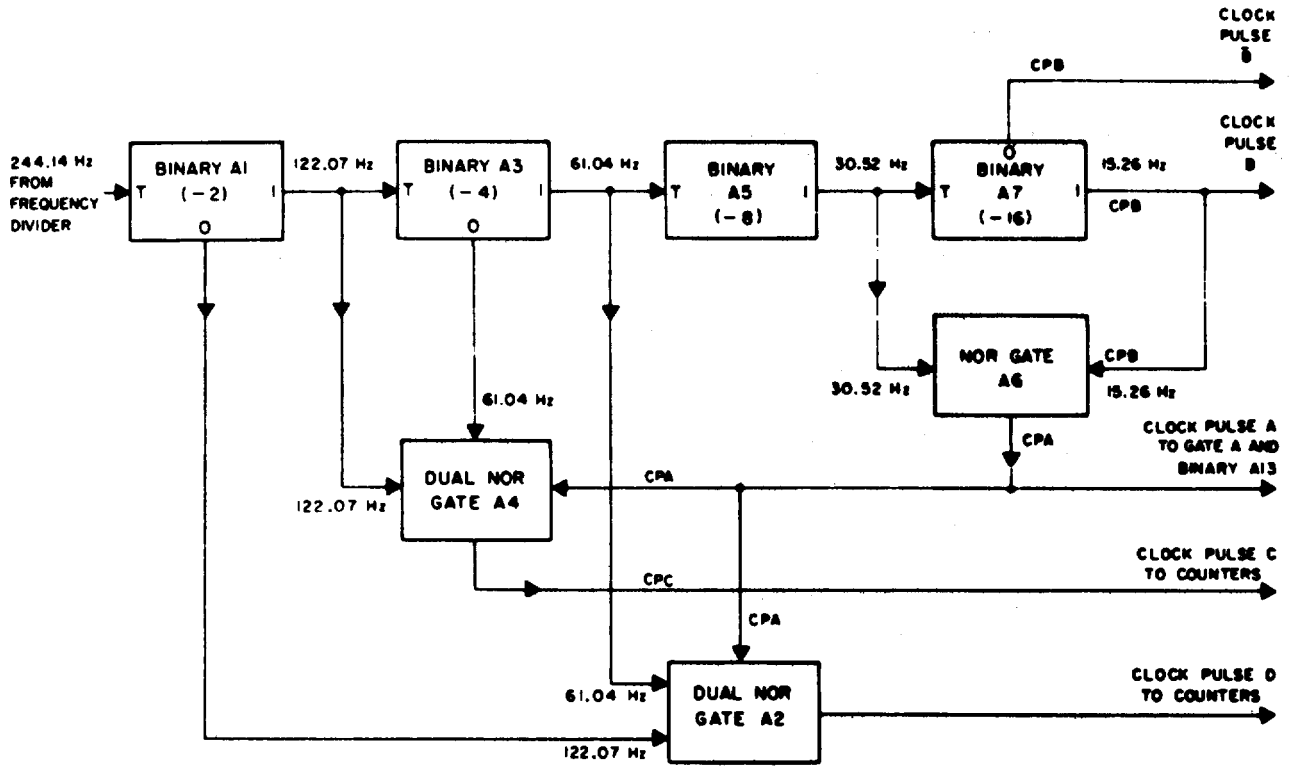
(a) The clock pulses are generated by dividing the signal from frequency divider 5TR1A2A9 or 1RE1A2A9 four-stage binary divider and gating the output signals from each divider with the outputs of succeeding dividers.

(b) The final referencing frequency of the programmed counter in the synthesizer must be low enough to allow several full cycles of the lowest modulating frequency to occur during each count cycle, in order to prevent the afc from drifting due to the modulating signal. The lowest modulating frequency is 200 Hz. The counter referencing frequency is 15.26 Hz over the portion of the band which includes a times-4 multiplication factor, and 10.15 Hz over the portion which includes a times-6 multiplication factor. The referencing rate is controlled by clock pulse B. Clock pulses A, C and D are required for gating, set and reset operation of the counter during the reference cycle. These pulses occur at the same rate as clock pulse B, but have a shorter time duration.

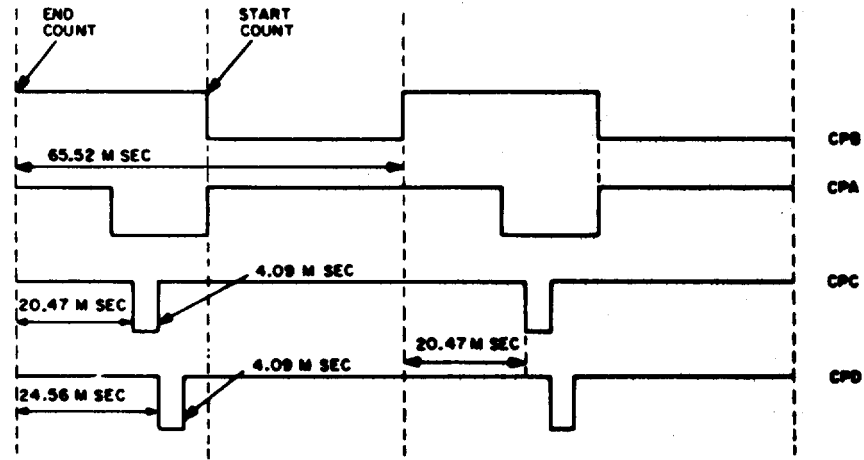
## (2) Block diagram analysis.

(a) Clock pulse generator circuits (Fig. 2-11). The input to the clock pulse generator section of the unit is a 244.14 Hz square wave at 4 volts peak-to-peak over the times-4 portion of the band, and a 162.75 Hz square wave at 4 volts peak-to-peak over the times-6 portion of the band. This signal is further divided by in a four-stage binary divider, A1, A3, A5 and A7. Clock pulse B is the inverted output of binary A7. Clock pulse B gates the non-inverted output of binary A5 in gate A6 to produce clock pulse A. Clock pulse C is the output of gate A4 and is derived by gating the non-inverted output of binary A1 with clock pulse A plus the inverted output of binary A3. Clock pulse D is produced in gate A2 by gating the inverted output of binary A1 with clock pulse A and the non-inverted output of binary A3. Clock pulse A is used to gate the rf signal applied to the programmed counter and to reset the first binary of the counter chain. Clock pulse B establishes the start count and end count moments as reference points for all other functions. Clock pulse C is the reset function; it occurs shortly after the end count moment and resets all binaries and the counters to zero state. Clock pulse D occurs immediately after clock pulse C ends and sets the programmed binaries to the one state.

(b) Error pulse generator circuits (Fig. 2-12). There are two main inputs to the error pulse generator section: the output of the sixth rf divider (digital electronic divider-counter 5TR1A2A5 or 1RE1A2A5) in the frequency range 742 kHz to 1.13 MHz, and the full count (-1) pulse from the programmed counter (digital electronic counter 5TR1A2A6 or 1RE1A2A6). The rf signal is gated by clock pulse A in dual NOR gate A8 (gate A) before clock pulse A is applied to the counter. Binary A13 is the first stage of the 16-stage counter and is reset by clock pulse A for convenience. The gated rf is also fed to the first count store (binary A9) and gate B (binary A10). The rf signal is then further divided by 5 non-programmed binary dividers contained in digital electronic counter 5TR1A2A6 or 1RE1A2A6 and digital electronic divider-counter 5TR1A2A5 or 1RE1A2A5. The full count (-1) pulse, generated when all 16 counter stages reach a one count simultaneously, is used to set the gate B (binary A10), which in turn, generates a full count pulse and an inverted full count pulse. These two pulses are then fed to the error pulse logic circuit which generates either a low count or a high count pulse. The lack of synchronization due to the delay between the opening of gate A (binary A8) and the passage of



CLOCK PULSE WAVEFORMS



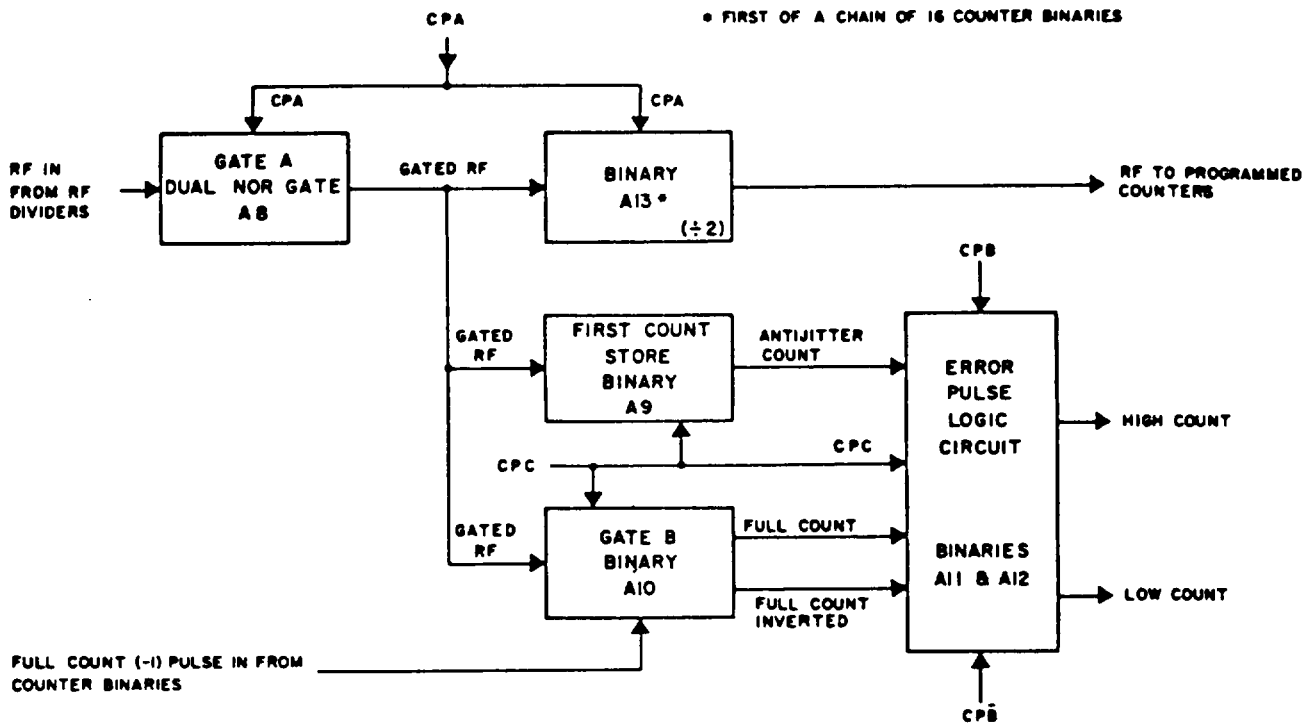
NOTES

ABOVE FREQUENCIES AND TIME COMPARISON ARE REPRESENTATIVE OF DIVIDE-BY-TWO FUNCTION. FOR DIVIDE-BY-THREE FUNCTION CONVERT AS FOLLOWS:

| FREQUENCIES  |              | TIME COMPARISON |              |
|--------------|--------------|-----------------|--------------|
| - 2 FUNCTION | - 3 FUNCTION | - 2 FUNCTION    | - 3 FUNCTION |
| 244.14 Hz    | 162.75 Hz    | 65.52 M SEC     | 98.28 M SEC  |
| 122.07 Hz    | 81.375 Hz    | 32.76 M SEC     | 49.14 M SEC  |
| 61.04 Hz     | 40.688 Hz    | 24.56 M SEC     | 36.84 M SEC  |
| 30.52 Hz     | 20.344 Hz    | 20.47 M SEC     | 30.70 M SEC  |
| 15.26 Hz     | 10.17 Hz     | 4.09 M SEC      | 6.13 M SEC   |

ELSRE011

Figure 2-11. Clock Pulse Generator 5TR1A2A7 or 1RE1A2A7, Functional Block Diagram.



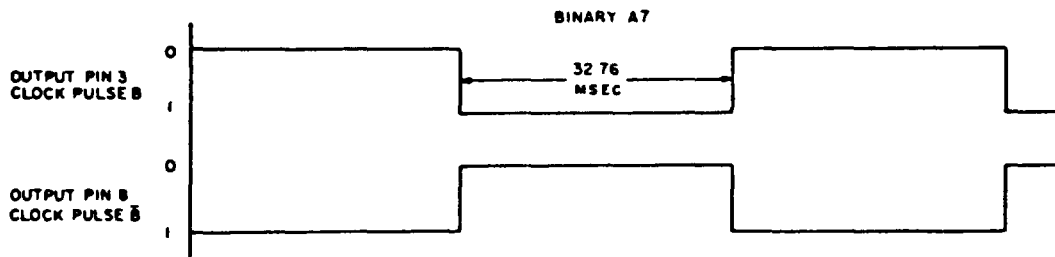
EL5RE012

Figure 2-12. Error Pulse Generator 5TR1A2A7 or 1RE1A2A7, Functional Block Diagram.

the first pulse through it, results in a random low count and causes a jitter on the afc line. This jitter is removed by the action of the first count store (binary A9) and gate A12 of the error pulse logic circuit, which produce high count pulses equal to the random low count pulses. The high count or the low count error pulses are a succession of negative-going pulses whose widths depend upon the frequency error of the modulator-oscillator rf signal. The high count or the low count error pulses are then fed to signal data converter-storer 5TR1A2A8 or 1RE1A2A8 where they are used in generating the afc voltage.

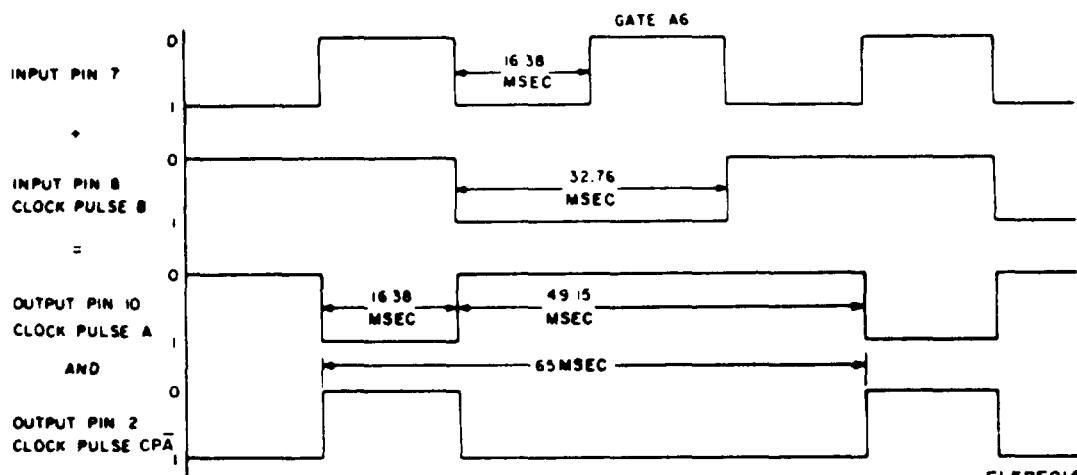
(3) Detailed circuit analysis (F0-4-13).

(a) Clock pulse generator. Clock pulse B establishes the counter start and stop times; the start count and end count moments. It is generated by dividing the 244.14 or 162.75 Hz signal a further 16 times through 4-stage binary divider A1 A3, A5 and A7. Clock pulse B is in the inverted output (pin 3) of binary A7 (fig. 2-13). The final frequency of clock pulse B is 15.26 Hz (or 10.17 Hz), depending on whether the transmitter multiplication factor is times-4 or times-6. These frequencies relate to referencing times of 65.53 milliseconds (or 98.3 milliseconds). The start count moment is initiated by the negative transition of clock pulse B; the end count moment is coincident with the next positive transition of clock pulse B. The pin 8 output of binary A5 is fed to pin 7 of dual NOR gate A6; clock pulse B applied at pin 8 gates the output of binary A5 to produce clock pulse A (CPA) at pin 10. Clock pulse A is 65.53 (or 98.33) milliseconds long, consisting of a negative pulse 16.38 (or 24.57) milliseconds long followed by a positive pulse 49.15 (or 73.76) milliseconds long (fig. 2-14). The output at pin 10 is fed into the second half of



EL5RE013

Figure 2-13. Clock Pulse B Generation, Waveforms.



EL5RE014

Figure 2-14. Clock Pulse A Generation, Waveforms.

NOR gate A6 (pin 4); the output at pin 2 is the inverted clock pulse A. CPA is fed to pins 3 and 9 of dual NOR gate A4 where it is used to gate the pin 3 output of binary A3 and the pin 8 output of binary A1 to generate clock pulse C (fig. 2-15). Clock pulse C (CPC) is a negative-going pulse 4.09 (or 6.14) milliseconds after CPA goes negative, or 12.27 (or 18.40) milliseconds before the start count moment. CPC is the clear or reset pulse fed to pin 4 of all programmed counters. Clock pulse D (CPD) is produced in NOR gate A2, by gating the pin 3 output of binary A1 and pin 8 output of binary A3 with CPA (fig. 2-16). CPD is a negative-going pulse 4.09 (or 6.14) milliseconds long starting 8.19 milliseconds after clock pulse A goes negative. CPD is the set pulse fed to pin 7 of all programmed counters.

(b) Error pulse generator circuits. The rf signal (rf divided by 64) at the output of the digital electronic divider-counter is fed through J7 pin 14 to pin 5 of gate A (dual NCR gate A8). Clock pulse A from pin 10 of NOR gate A6 is fed to pin 4 of gate A and gates the application of the rf signal to the counter. The gated rf from the first half of gate A is then fed through the second half of the gate to convert the rf signal before A is applied to pin 10 of the first counter stage, binary A13. Clock pulse A is fed to pin 4 of binary A13 to perform the reset function as a matter of convenience; all other counters are reset and set by clock

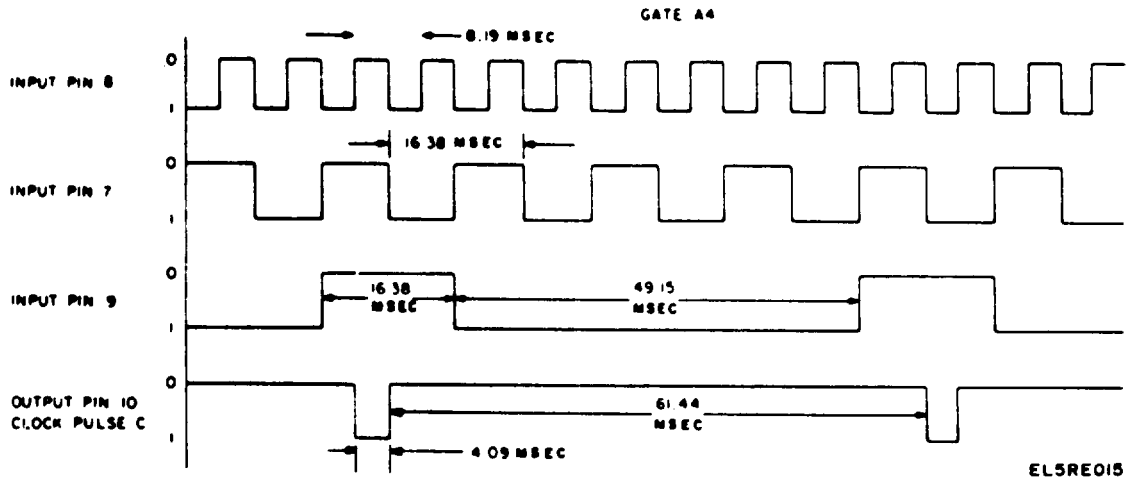


Figure 2-15. Clock Pulse C Generation, Waveforms.

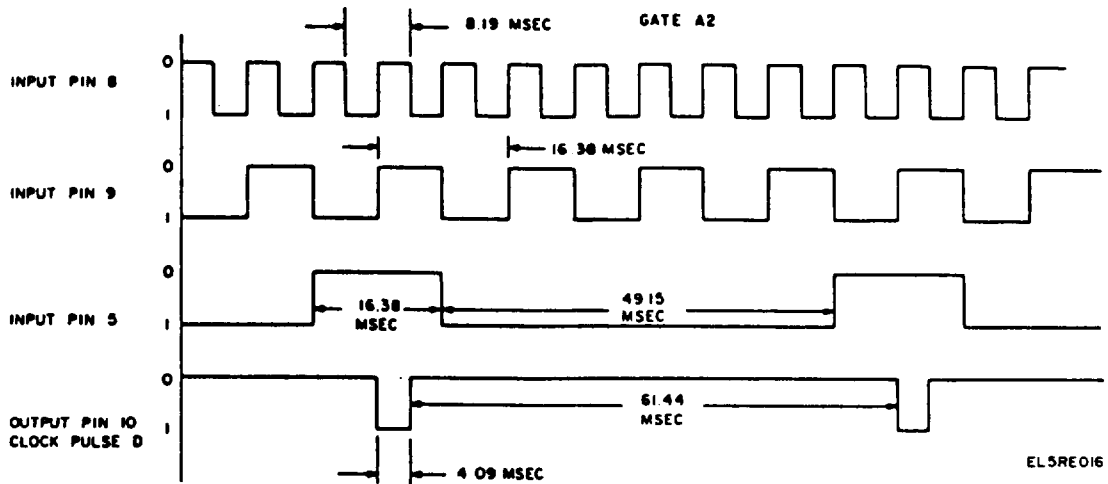


Figure 2-16. Clock Pulse D Generation, Waveforms,

pulses C and D respectively. The pin 8 output of binary A13 is fed through J7 pin 13 to digital electronic counter 5TR1A2A6 or 1RE1A2A6 for counting. The gated rf signal at the output of gate A is also fed to the toggle inputs of binary A9 (anti-jitter) and binary A10 (gate B). The full count (-1) pulse generated in digital electronic counter 5TR1A2A6 or 1RE1A2A6 (para 2-11a) is fed through J7 pin 12 to the gating input pin 2, of gate B (binary A10). (The full count (-1) pulse is generated when all counter stages reach a one count simultaneously.) The next negative transition of the rf signal through gate A (binary A8) arriving at pin 10 of gate B, causes gate B to change states, generating the full count pulse at pin 8 and the inverted full count pulse at pin 3. Gate B is then reset to zero state by clock pulse C.



1. The full count pulse at pin 8 of gate B is fed to pin 7 of NOR gate A12, while the inverted full count pulse at pin 3 of gate B is applied to NOR gate A11. NOR gates A11 and A12 form the error pulse logic circuit. The full count pulse fed to NOR gate A12 is referenced to clock pulse B applied to pin 8. Clock pulse A is fed to pin 9 of gate A12 to prevent any spurious low or high count pulses being generated during the counter resetting period. At the end count moment clock pulse B goes positive. The full count pulse goes negative at the time A10 is triggered. Thus, if the full count pulse occurs after the end count moment, the output at pin 10 of NOR gate A12 is a negative low count error pulse lasting from the end count moment to the moment the full count state has been reached. The inverted full count pulse at pin 3 of binary A10 is fed to pin 5 of NOR gate A11; the inverted full count pulse goes positive when A10 is triggered. Clock pulse B (CPB) (pin 8 output of binary A7) is applied to pin 4 of NOR gate A11 and is positive until the end count moment. If the full count moment occurs before the 'end count' moment, the output at pin 2 is a negative high count error pulse lasting from the moment the full count state has been reached to the end count moment. The negative high count error pulse is then fed into pin 8 of the second half of NOR gate A11. Input to pin 9 of A11 is the output (pin 3) of the anti-jitter binary which is negative at the start count moment, and pin 9 of A11 is held positive around the end count moment; the output at pin 10 of NOR gate A11 is a positive-going high count error pulse occurring near the end count moment if the modulator-oscillator frequency is high. This pulse is then fed into NOR gate A12 (pin 4) where it is inverted.

2. The gated rf at the output of gate A (binary A8) is also fed to the toggle input (pin 10) of binary A9. Binary A9 is set to state zero by clock pulse C applied at pin 4, and remains in this state until it is switched by the first rf pulse through gate A. The output at pin 3 of A9 is negative after the start count moment until the first pulse passes gate A; this pulse is fed to A11 (pin 9) where it is combined with the high count pulse generated at A11 pin 2. The output from A11 pin 10 thus carries the high count pulse and the anti-jitter pulse. This is equivalent to a high count error pulse produced at the start count moment and is equal in time to the delay in counting resulting from the lack of synchronization between clock pulse A and the first rf pulse through gate A. During the anti-jitter pulse generation, the input to A11 pin 5 is positive, since no full count pulses are produced near the start count moment. The output of A11 pin 10 is then fed into pin 4 of NOR gate A12 where it is inverted. The low count and/or high count error pulses are then fed into signal data converter-storer 5TR1A2A8 or 1RE1A2A8.

b. Model No. 5TR1A2A17 or 1RE1A2A17.

(1) General . This unit performs two major functions within the synthesizer. The first function is the generation of clock pulses A, B, C and D. The second is to produce high or low count error pulses. The board contains nine divider stages which are used to generate clock pulses A, B, C and D. The remaining circuitry forms the error pulse generator. The full count (-1) pulse, arriving at about the end-count moment, is used to generate an error pulse. The error pulse (high or low), proportional to the amount of frequency error in the vco frequency, is fed to the converter-storer where it is used to generate the afc voltage. Since the rf and the clock pulse B are not synchronized, the full-count pulse will jitter in a random manner and produce an average low count error of 1/2 bit. To eliminate this error (jitter) an anti-jitter pulse of the same width is generated in the high-count error

(2) Block diagram analysis, clock pulse generator circuits (Fig. 2-17). The 7.8125 kHz or 5.2083 kHz input to electrical synchronizer 5TR1A2A17 is divided in a group of nine binaries. Clock pulse B (CPB) is the Q output of the last binary and is a symmetrical square pulse 65.54 msec long. The Q output of binary A6A and CPB is fed to a NAND gate to produce clock pulse A (CPA). CPA is a negative-going pulse 16.36 msec long followed by a positive-going pulse 49.18 msec long. Similarly, the Q output of binary A6B, the Q output of binary A8A, and the inverted CPA (CPA) are fed to a NAND gate to produce clock pulse C (CPC). CPC is a negative-going pulse 4.09 msec long occurring once every 65.52 msec. The Q output of binary A6B, the Q output of binary A8A, and CPA are fed to a NAND gate. The inverted output, together with the Q output of binary A8B, are fed to a second NAND gate. The inverted output of the second NAND gate is clock pulse D (CPD), a positive-going pulse 2.05 msec long, occurring once every 65.52 msec. CPA, CPC and CPD coincide with the positive-going pulse of CPB. A timing chart of the time comparison for the divide-by-three function is included in figure 2-17.

(a) Error pulse generator circuits (Fig. 2-18). The error pulse generator section has two main inputs; the rf divided by 64 from frequency divider 5TR1A2A14 and the full count (-1) pulse from the digital electronic counter-divider 5TR1A2A16. CPA (high) opens NAND gate A1B to allow the rf signal to pass through to A2A, the first stage of the 16 stage counter. The gated rf is also fed to the first count store (binary A3A) and NAND gate A4A (part of error pulse logic circuit) and is used to generate the antijitter pulse. The full count (-1) pulse, fed into full count store A3B, and the rf divided by 64 applied through NAND gate A1C to the full count store, generate the full count pulse. The width of the full count pulse, as measured against the end count moment, depends on the magnitude of frequency error. A high count error will occur when the end count moment arrives, in time, after the full count (-1) pulse. This pulse is gated by CPB before it is fed to the NAND gate, together with the time delay registered by the first count store binary.

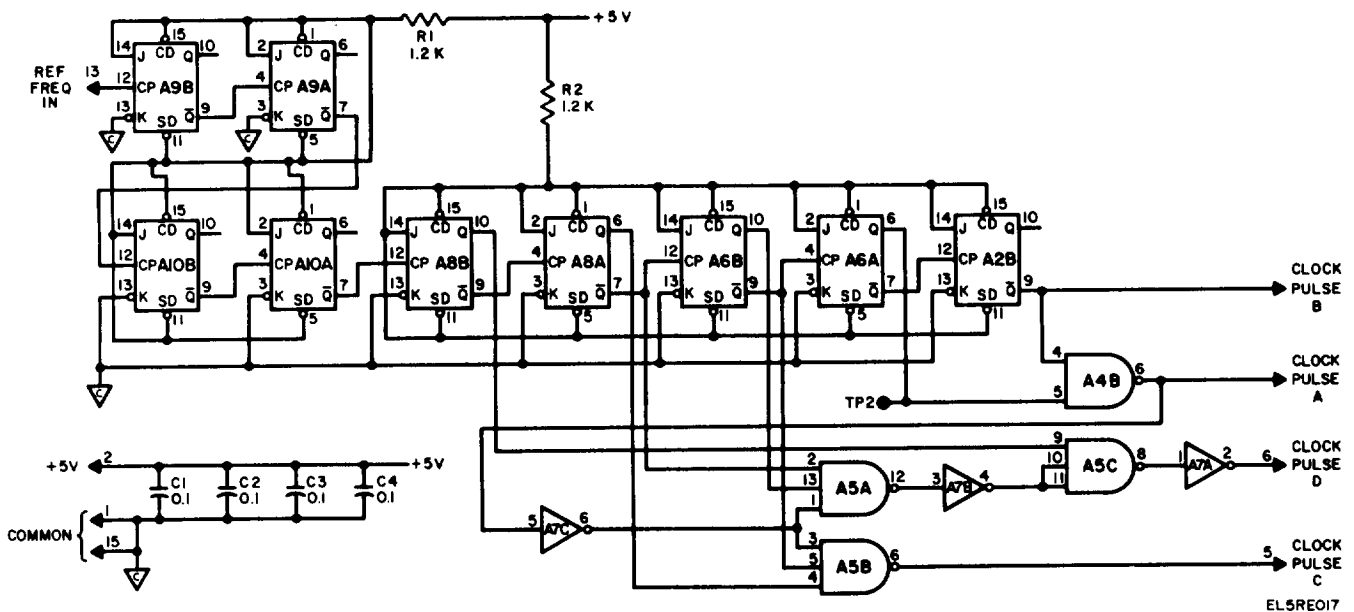


Figure 2-17. Clock Pulse Generator, 5TR1A2A17 or 1RE1A2A17, Functional Block Diagram.



(b) Delay of error pulse generator circuits. The lack of synchronization, due to delay between the opening of rf gate (A1B) and the passage of the first pulse through it (time delay of the first rf pulse), results in a random low count error and will cause a jitter on the afc line. This jitter is compensated for by combining the outputs of the first count store and the high count gate, which produce high count pulses equal to the random low count pulses. The high count or low count error pulses are negative going pulses whose widths are proportional to the frequency error of the modulator-oscillator. The high or low error count pulses are then fed to converter-storer 5TR1A2A18 or 1RE1A2A18 where they are converted to dc voltages, which increase or decrease the afc voltage to the modulator-oscillator. Figure 2-18 illustrates the effect of a full count (-1) pulse occurring before or after the end count moment.

(3) Detailed circuit analysis, low power dividers (F0-4-14). The incoming reference frequency from the rf oscillator 5TR1A2Y11 is further divided by a factor of 16 in dual flat packs A9B, A9A, A10B and A10A. The output frequency, 488.2 Hz or 325.5 Hz, is fed to the toggle (CP) input of A8B, the first stage of the clock pulse generator circuits.

(a) Clock pulse generator circuit. Clock pulse B, the Q output of A2B, establishes the reference time for the start count and end count moments. The start count moment is initiated by the negative transition of CPB, the end count moment is coincident with the next positive transition of CPB. The count time lasts for 32.76 msec (divide-by-2 function) or 49.15 msec (divide-by-3 function). The positive transition of the CPA is coincident with the negative transition of CPB (start count moment) and is used to gate the rf which is then fed to the 16-stage counter. CPC and CPD occur in time during the negative position of CPA (quiescence period). CPC, a negative-going pulse 4.09 msec long, occurs 12.27 msec before the start count moment. It is fed through J6 pin 5 to the program counters (CD input) to clear all counters. CPD is a positive-going pulse, 2.04 msec long, occurring 6.15 msec before the start count moment. CPD is fed through J6 pin 6 to the program counters (SD inputs) to set direct all programmed counters. Low power dual J-K flipflops are used in the binary stages. The J, CD and SD inputs are connected to the +5 volt dc line; the input is connected to ground. One half of the final binary A2B supplies the CPB and CPB outputs; the other half, A2A, is the first binary in the 16 stage, Triple-pack, three-input, NAND gates are used. These inverters A7A, A7B, A7C are hex type with three spares, A7D, A7E and A7F available. C1 C2, C3 and C4 filter the +5 dc line.

(b) Error pulse generator. The rf signal (rf divided by 64) at the output of the frequency divider is fed through J6, pin 4 to NAND gates A1B and A1C. The gate output of NAND gate A1B is fed to the CP input of the first binary of the 16-stage counter (A2A) and the CP input of the 1st Count store (A3A). CPA clears A2A so that the count starts simultaneously with the gated rf. The gated rf is fed through J6 pin 4 to the counters. A3A is cleared by CPC at the CD input. The Q output of A3A (time delay of the first rf pulse through the rf gate), is then fed to NAND gate A4A. NAND gate A1C has three inputs: the rf divided by 64, CPA, and the Q output of binary A3B. The output of A1C is applied to the CP input of full count store A3B; the full count (-1) pulse from electronic digital counter is fed through J6 pin 8 to the J and K inputs of A3B, and CPC is applied to the SD (set direct) input. The Q output of A3B, CPB, and CPA are fed into NAND gate A1A which generates the low count error pulses; A1A output is fed through J6 pin 11 to the signal data converter-storer board. The Q output of A3B is gated by CPB in NAND gate A4D; the high count pulses at the output of A4D are fed together with the Q output of A3A to

NAND gate A4A. By this process, the anti-jitter pulse is added to the high count pulse. The output of NAND gate A4D, which contains anti-jitter and high count error pulses, is further gated by CPA in NAND gate A4C. The A4C output, which now contains variable-width anti-jitter and high count pulses, is applied through J6 pin 10 to the signal data converter-storer board. A3A and A3B are low power dual J-K flip-flops. A1A, A1B, A1C are triple pack 3 input NAND gates. A4A, A4C, A4D are quadruple pack 2 input NAND gates. A4B is used in the clock pulse generator circuit to produce CPA.

## 2-10. Programmed Counters

### a. Unlettered Model (Fig. 2-19).

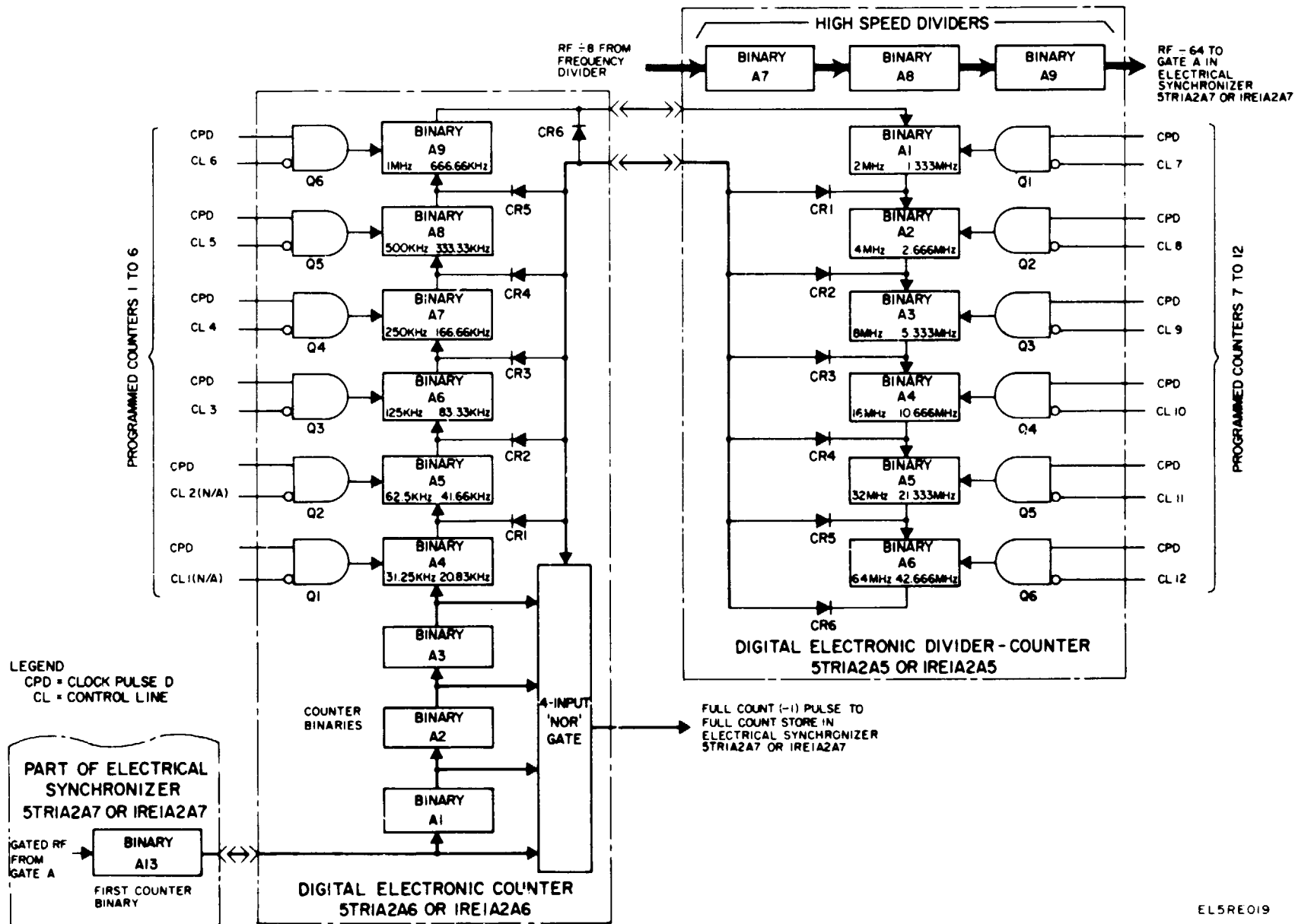
(1) The synthesizer frequency (any one of the 1,720 discrete output frequencies) is referenced to, and controlled by, the 2.0 MHz reference crystal oscillator (rf oscillator 5TR1A2Y1 or 1RE1A2Y1). The frequency referencing and control are done in a sampling manner to permit frequency deviation of the output signal. The sampling rate is related to the lowest modulating frequency, and is low enough to prevent the modulating signal from having an effect on the frequency controlling function. The lowest modulating frequency is 200 Hz; the frequency referencing rate has been established at 15.26 Hz (divide-by-2 function) or 10.17 Hz (divide-by-3 function).

(2) The frequency referencing rate is established by dividing the output of the 2.0 MHz crystal oscillator (rf oscillator 5TR1A2Y1 or 1RE1A2Y1) to 15.26 Hz (65.52 milliseconds) or 10.17 Hz (98.33 milliseconds). A sample of the modulator-oscillator output frequency is fed through the programmed ripple counter which should give a one count in every stage (full count) at precisely the same time as the sampling time interval ends (end count moment). If the one count is reached before or after the end moment, high or low count error pulses are produced; these in turn vary the afc voltage in the proper direction to bring the modulator-oscillator output frequency to the nominal value.

(3) To permit the selection of the synthesizer output frequencies (channel selection), certain stages of the programmed ripple counter are preset according to the frequency selection code. By changing the preset code, the time required for any particular frequency to establish full count condition also changes. This in turn causes the afc to change the modulator-oscillator output frequency to the point where the full count occurs at the end count moment. The preset code is established in control indicator 6A3 or 2A2 (para 2-28).

(4) The ripple counter consists of a total of 16 binary dividers connected in series, with the output of each binary feeding a 16-input NOR gate (fig. 2-19). The gate produces a full count output when all 16 stages reach the one state. In order to establish the correct counter working range (about 1 MHz), the sample of the synthesizer output frequency is first divided in six high speed dividers (para 2-3) to a frequency in the range of 0.742 MHz to 1.13 MHz. This signal is then fed into electrical synchronizer 5TR1A2A7 or 1RE1A2A7 and gated by clock pulse A in gate A. The gated rf is applied to the counter at the start of the counter referencing time (start count). The first binary of the 16-stage counter is contained in the electrical synchronizer. During the period the rf signal is gated-off (quiet period), all counter stages are set to zero state by clock pulse C, and immediately after, certain selected states are preset to the one state by clock pulse D, according to the information code arriving on control lines 3 - 12 from control-indicator 6A3 or

Figure 2-19. Programmed Counters (Unlettered Model), Functional Block Diagram.



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2A2 . The first six divider stages (one in the electrical synchronizer and five in digital electronic counter 5TR1A2A6 or 1RE1A2A6) are all preset to the one state by clock pulse A, clock pulse C or control lines 1 and 2. Their function is to provide fine frequency resolution and to reduce the amount of correction required of the anti-jitter circuit. The remaining 10 dividers are preset by control-indicator control lines 3 to 12 to produce the selected frequency.

(5) The frequency control information is in the form of a binary code (para 2-28). Each succeeding control line controls twice as much frequency change as the one preceding it. Thus control line 3 controls a frequency change of 125 kHz or 83.333 kHz; line 4 controls a frequency change of 250 kHz or 166.666 kHz; and line 12 controls a frequency change of 64 MHz or 42.666 MHz, depending whether the sampling interval is 32.76 milliseconds (channels up to 179) or 49.166 milliseconds (channels 180 and up).

(6) For example, to select a transmitter output frequency of 256 MHz, channel code 112 on the channel selector will preset line 12. Since the transmitter multiplication factor is times-4 at channel 112 the required synthesizer output frequency is 64.0 MHz. The six binary dividers that precede the counter reduce the modulator-oscillator output frequency to 1.0 MHz before it is applied to the counter. With line 12 preset it will take 32.76 milliseconds for the counter to generate the full count pulse. This signal equals the 32.76 millisecond counter reference time established by the reference rate of 15.26 Hz (clock pulse B). To increase transmitter output frequency by one channel, line 3 is preset with line 12 as the channel selector is set to channel 113. Presetting line 3 will initially decrease the time it takes to generate the full count pulse by 64 microseconds, causing low count error pulses which change the afc the correct amount to increase the vco frequency by 125 kHz to the point where the full count pulse again occurs at the end count moment. To decrease transmitter frequency by one channel to channel 111, the channel selector code removes line 12 preset and presets all other 9 stages in accordance with the binary counting code. This then increases the time to generate the full count pulse by 64 microseconds and causes the vco frequency to shift downward by 125 kHz.

b. A Model (Fig. 2-20).

(1) The synthesizer output frequency (any one in the range of 47.5 to 72.5 MHz) is referenced to, and controlled by, the 16 MHz reference crystal oscillator (rf oscillator 5TR1A2Y11 or 1RE1A2Y11). The frequency referencing and control are done in a sampling manner to permit frequency deviation of the output signal. The sampling rate is related to the lowest modulating frequency, and is low enough to prevent the modulating signal from having an effect on frequency controlling function. The lowest modulating frequency is 200 Hz; the frequency referencing rate has been established at 15.2 Hz (divide-by-2 function) or 10.17 Hz (divide-by-3 function). This is accomplished by dividing the output of the 16 MHz crystal oscillator (in a series of twenty binary dividers) to 15.26 Hz (65.53 milliseconds divided-by-2 mode) or 10.17 Hz (98.33 milliseconds, divided-by-3 mode).

(2) A sample of the modulating-oscillator (vco) 5TR1A2A2 output frequency is fed through a series of binary dividers (6) then through a programmed ripple counter (16 binaries). A full count state is reached when all the 16 binaries of the counter are in the H state. A logic circuit senses this state and produces a full count (-1) pulse which is then fed to the electrical synchronizer 5TR1A2A17. When the vco is on frequency, the full count (-1) pulse occurs at the end count moment. If the vco frequency is too high, then the full count state is reached before the end count moment and vice versa.

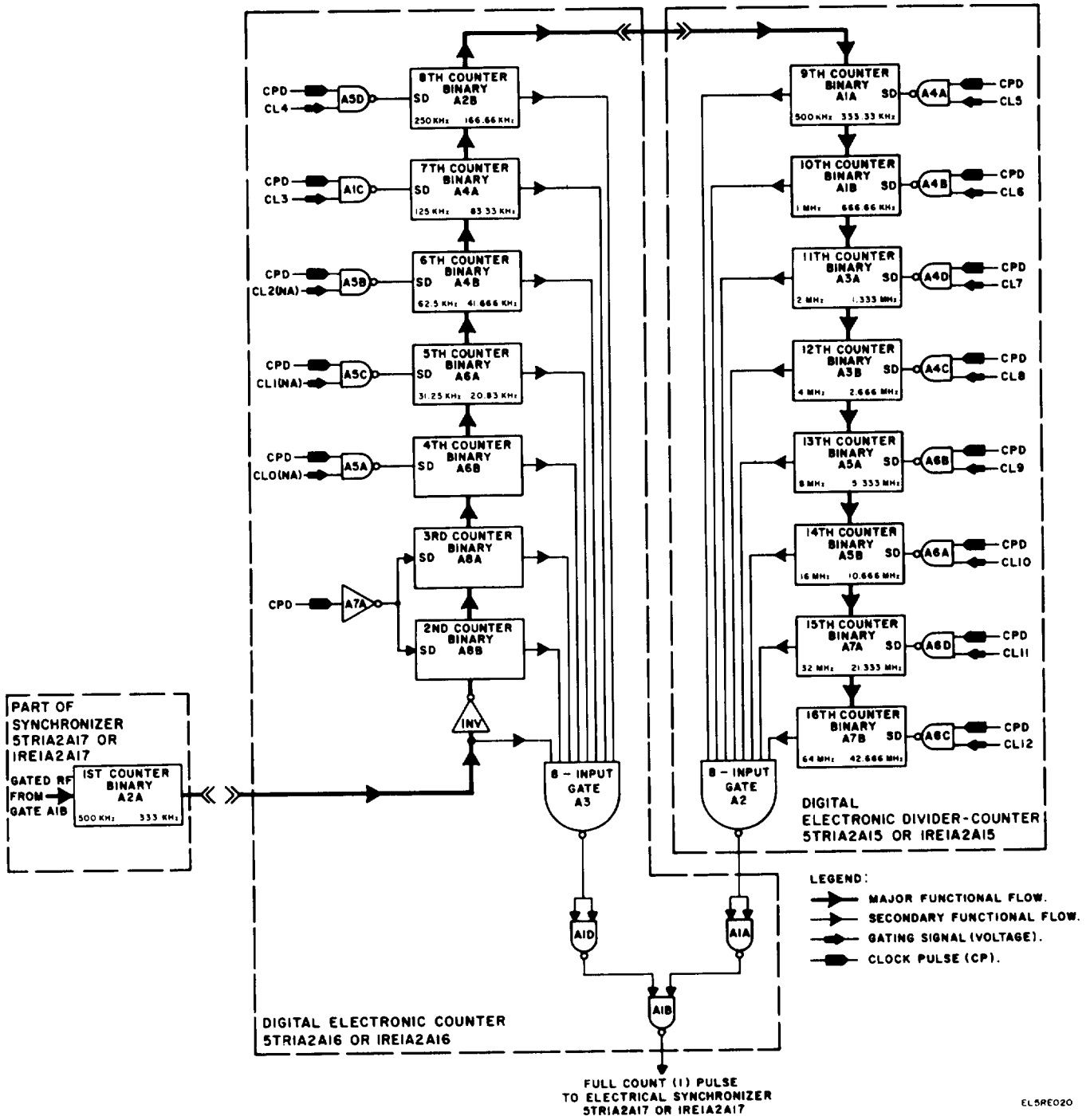


Figure 2-20. Programmed Counters, (A Model), Functional Block Diagram.

(3) To permit the selection of the synthesizer output frequencies (channel selection), certain stages of the programmed ripple counter are preset according to the frequency selection code. By changing the preset code, the time required for any particular frequency to establish full count condition also changes. This pro-



duces error pulses which, in turn, determines the afc voltage fed to the vco and changes the output frequency to the point where the full count occurs at the end count moment. The preset code is established in control indicator 6A3 or 2A2 (FO-4-33).

(4) The ripple counter consists of a total of 16 binary dividers connected in series, with the output of each binary feeding one of two 8-input NAND gates. The outputs of the two 8-input NAND gates are fed into another NAND gate to produce a full count output when all 16 stages reach a high state (fig. 2-20). In order to establish the correct counter working range (about 1 MHz), the sample of the synthesizer output frequency has been divided in six high speed dividers to a frequency in the range of 0.742 MHz to 1.13 MHz (para 2-6b). This signal is fed into electrical synchronizer 5TR1A2A17 or 1RE1A2A17 and gated by clock pulses A in the rf gate (para 2-9b) (start count). During the period the rf signal is gated off (quiet period, CPA negative), all counter stages are cleared direct by clock pulse C. Immediately afterwards, clock pulse D arrives at the SD input of all binaries. However, on each of binaries 4 through 16, CPD is applied through a NAND gate and can get through only if the other input is high. Binaries 7 through 16 are thus controlled by an H-L code present on control lines 3 through 12. The unprogrammed binaries 2 through 6 are always set direct by CPD. Their function is to provide fine frequency resolution and to reduce the amount of correction required of the anti-jitter circuit.

(5) The frequency control information is in the form of a binary code. Each control line controls twice as much frequency change as the one preceding it. Thus, control line 3 controls a frequency change of 125 kHz or 83.333 kHz; line 4 controls a frequency change of 250 kHz or 166.666 kHz, and line 12 controls a frequency change of 64 MHz or 42.666 MHz, depending on whether the sampling interval is 32.75 msec (channels up to 179) or 49.166 msec (channels 180 and up).

(6) For example, to select a transmitter output frequency of 256 MHz, channel code 112 on the channel selector will code line 12. Since the transmitter multiplication factor is times-4 at channel 112, the required synthesizer output frequency is 64.0 MHz. The six binary dividers that precede the counter reduce the modulator-oscillator frequency to 1.0 MHz before it is applied to the counter. With line 12 coded, it will take 32.76 msec for the counter to generate the full count pulse. This signal is equivalent to 32.76 msec counter reference time established by the reference rate of 15.25 Hz (clock pulse B). To increase transmitter output frequency by one channel, line 3 is coded with line 12 as the channel selector is set to channel 113. Coding line 3 will initially decrease the time it takes to generate the full count pulse by 64 microseconds, causing low count error pulses. These, in turn, change the afc by the correct amount to increase the vco frequency by 125 kHz, to the point where the full count pulse again occurs at the end count moment. To decrease transmitter frequency by one channel to channel 111, the channel selector code is removed from line 12; however, all other 9 lines are coded in accordance with the binaries counting code. This increases the time to generate the full count pulse by 64  $\mu$  sec and causes the vco frequency to shift downward by 125 kHz.

## 2-11. Digital Electronic Counter

### a. Model No. 5TR1A2A6 or 1RE1A2A6.

(1) General. The digital electronic counter contains three non-programmed binary counters (A1, A2 and A3), six programmed binary counters A4 through A9 and one 4-input NOR gate operating as a 16-input AND gate. All binaries are connected

in a counter-fashion with the rf signal at the zero output (pin 3) being connected to the toggle input (pin 10) of the next binary. The zero output of all binaries is used to originate the full count (-1) pulse.

(2) Detailed circuit analysis (F0-4-11). The output on binary A13 of electrical synchronizer 5TR1A2A7 (first binary counter), a 4 volt peak-to-peak square wave, is fed into the toggle input of binary A1 and to the full count gate (4-input NOR gate) A10, pin 10. Similarly, the outputs of binaries A1, A2 and A3 are also fed to the full count gate A10 (pins 7, 8 and 9 respectively). Binaries A1, A2 and A3 are preset to state one (zero state at pin 3) by clock pulse D fed to gating input pin 7 of each binary. Binaries A4 through A9 are programmed working in conjunction with control lines 1 through 6 of control-indicator 2A2 or 6A3. Control lines from the control-indicator are applied to the bases of transistors Q1 through Q6. Clock pulse D is applied to the emitters of transistors Q1 through Q6. Transistors Q1 through Q6 operate as AND gates with control lines gating clock pulse D application to the counter stage. The first two control lines (lines 1 and 2) are not used; the corresponding microswitches in the control-indicator are open. Clock pulse C applied to pin 4 of each binary sets it to state zero (pin 8). Clock pulse D arriving at binaries A4 and A5 through gates Q1 and Q2 presets them to state one (zero state at pin 3). The zero state at pin 3 is sensed by CR1 and CR2 respectively.

(a) Control lines 3 through 6 carry the control-indicator binary coding (para 2-28). When a control line is off (uncoded) the corresponding microswitch is closed, grounding the base of its corresponding transistor, thus preventing clock pulse D from getting through. The programmed binary remains at state zero (pin 8) and is switched to state one by the next negative transition. Diodes CR3 through CR6 sense state zero at pin 3 of each binary counter. CR1 through CR6 are part of a 12-input gate extender used to extend the inputs to the full count gate A10 from 4 to 16.

(b) The rf at the pin 3 output of binary A9 is fed through J6 pin 6 to the next six programmed counters contained in digital electronic divider-counter 5TR1A2A5 or 1RE1A2A5. The extender line from counter stages 7-12 is connected through J6 pin 8 to the extender line of the first six counter stages, and then fed to the gating input, pin 2, of the full count gate. The negative-going full count (-1) pulse is generated the instant all inputs sensed (2 and 7 through 10) become zero simultaneously. The full count pulse is then fed through J6 pin 1 to full count store, binary A10, in electrical synchronizer 5TR1A2A7 or 1RE1A2A7.

b. Model No. 5TR1A2A16 or 1RE1A2A16 (A Model).

(1) General. The digital electronic counter contains nine binaries, nine NAND gates and two inverters. All binaries are connected in a "counter" fashion, with the rf signal at the Q output being connected to the CP input of the next binary. The Q output of all binaries is sensed by an 8-input NAND gate.

(2) Detailed circuit analysis (F0-4-12). The output of the first binary counter A2A of electrical synchronizer 5TR1A2A17, a 4 volt, peak-to-peak square wave at pin 7 is fed through inverter A7B to the CP input of binary A8B. The Q output of binary A8B is fed to CP input of binary A8A, and so on. The Q output of the last binary A2B (count pulse out) is fed through pin 3 to the digital electronic divider-counter 5TR1A2A15, 8-input NAND gate A3 senses the Q outputs of binaries A8A, A6B, A6A, A4A and A2B and the input line (first counter binary), CPD at pin 6 is fed through inverter A7A to the SD input of binaries A8B and A8A. CPD is also fed to one input of NAND gates A5A, A5C, A5B, A1C and A5D. Control lines 0 through 4, at

pins 10 through 14 are also connected to NAND gates A5A, A5C, A5B, A1C and A5D, respectively. Depending on whether a control line is coded (+26 v, H) or not (0 v, L), the SD input to the binary will be L or H at CPD times, and the corresponding binary removed or added (time-wise). Control lines 0, 1 and 2 are always coded (H); at CPD time the low at SD input sets binaries A5A and A5C and A5B. Binaries A1C and A5D will set, or remain cleared, depending on whether control lines 3 and/or 4 were H or L.

(a) NAND gate A3 output remains H until such time all sensed Q outputs are simultaneously H; this occurs twice during a full count time. The L - the half count pulse lasts for the duration of the highest rf frequency fed into the counter. The waveform at the output of A3 is inverted in A1D and the resultant waveform applied to the input of A1B. The second input to A1B is a similar waveform, half count pulse, arriving at pin 4 from digital electronic divider-counter 5TR1A2A15. The output of the A1B is a negative-going pulse, approximately 1 usec wide, occurring at the moment both half inputs are high. This is the full count (-1) pulse, and is fed through pin 8 to the full count store binary in the electrical synchronizer 5TR1A2A17.

(b) All binaries are low-power dual pack J-K flip-flops. The J input is connected to the +5 vdc line. K input to ground, A3 is an 8-input NAND gate. All other NAND gates are of the quadruple-pack two-input type. A7A and A7B are "Hex" inverters with A7C, A7D, A7E and A7F available as spares. A2A is a spare binary. The +5 vdc line is filtered by C1 and C2.

## 2-12. Digital Electronic Divider-Counter

### a. Model No. 5TR1A2A5 or 1RE1A2A5.

(1) General. The digital electronic divider-counter contains six programmed binary counters A1 through A6 (stages 7 through 12) and the three last stages of the high speed dividers. Binaries A1 through A6 are connected in the same counter fashion as counter stages 1 through 6 in digital electronic counter 5TR1A2A6 or 1RE1A2A6 (para 2-11A).

(2) Detailed circuit analysis (FO-4-9).

(a) The operation of programmed counter binaries A1 through A6 is identical to that of counter binaries A4 through A9 in the digital electronic counter (para 2-11a). The counter input is available to the first binary from J5 to pin 5 and clock pulse C is fed through J5 to pin 7 to pins 4 of each binary. Clock pulse D is fed from J5 to pin 9 to the emitters of transistors Q1 through Q6, while control lines 7 through 12 are applied from J5 pins 10 through 15 and individual 22 k resistors to the bases of transistors Q1 through Q6 respectively. CR1 through CR6 sense the zero state at pin 3 of each binary and the extender line is fed through J5 pin 8 and J6 pin 8 to the full count (-1) gate in digital electronic counter 5TR1A2A6 or 1RE1A2A6.

(b) Binaries A7 through A9 are integrated micro-circuit binary dividers and have been mounted on this board for convenience. The rf input (rf divided by 8) is applied through J5 pin 1 and C2 to toggle input pin 10 of binary A7. The two anti-phase outputs at pins 3 and 8 are at half the input frequency. R7 and R13 lower the output impedance to speed up the switching action. The output at pin 3 is fed into toggle input pin 10 of the next binary A8, and similarly the A8 output at pin 3 is

fed into the toggle input of binary A9. R8 and R9 speed up the switching action of binaries A8 and A9 respectively. The output at pin 8 of binary A9, (rf divided by 64) is coupled through C1 to J5 pin 6 and then fed to electrical synchronizer 5TR1A-2A7 or 1RE1A2A7 for gating and counting.

b. Model No. 5TR1A2A15 or 1RE1A2A15 (A Model).

(1) General. The digital electronic divider-counter contains eight programmed binary counters and nine NAND gates. The eight binaries are connected in a similar way to the counter stages in digital electronic counter 5TR1A2A16 or 1RE1A2A16.

(2) Detailed circuit analysis (FO-4-10). The operation of the eight counter binaries, A1A through A7B, is identical to that of the counter binaries in the digital electronic counter (para 2-11b). The input signal available to the first binary from J8 pin 3 is the output signal of digital electronic counter 5TR1A2A16 or 1RE1A-2A16. CPC at pin 5 is fed to the CD input of all counter binaries. CPD at pin 6 is fed to one input of NAND gates A4A, A4B, A4D, A4C, A6B, A6A, A6D and A6C. Control lines 5 through 12, at pins 7 through 14 respectively, are also connected to NAND gates A4A, A4B, A4D, A4C, A6B, A6D and A6C. When one or more control lines are coded (+5 v, H) the corresponding binaries will be "set" (H at Q output) before the **start count moment**. The Q outputs of all eight binaries are fed to NAND gate A2; the output waveform of A2 remains a H until the full count is reached and all outputs are H. This L - the half count pulse - occurring once during the count time, at about the end count moment, is fed back to the digital electronic counter where it is inverted in A1A before being applied to the full count (-1) gate A1B. The eight counter binaries are low power dual pack J-K flipflops. The J inputs are connected to the +5 vdc line, the K inputs to ground. A2 is an 8-input NAND gate. All other NAND gates are quadruple pack, two-input types. C1 and C2 filter the +5 vdc line.

2-13. Signal Data Converter-Storer

a. Model No. 5TR1A2A8 or 1RE1A2A8.

(1) General. The only function of signal data converter-storer 5TR1A2A8 or 1RE1A2A8 is the conversion and integration of high count and low count error pulses to a dc automatic frequency control (afc) voltage. The afc voltage is then fed through amplifier-monitor 5TR1A2A3 or 1RE1A2A3 to modulator-oscillator 5TR1A2A2 or 1RE1A2A2 where it is used to control the synthesizer output frequency.

(2) Block diagram analysis (Fig. 2-21). The low count and high count error pulses fed into the signal data converter-storer are negative-going pulses at 4 volts peak-to-peak, whose width depends on the actual frequency error of the modulator-oscillator output frequency. The low count error pulses are fed through a two-stage amplifier (Q1-Q2) and a diode to a pair of low leakage capacitors in the gate circuit of a metal oxide semiconductor field effect transistor (FET), Q6. The two-stage amplifier is operated in saturation and acts as a switch which applies a constant amplitude voltage pulse to the capacitors. As the width of low count pulses indicates the frequency error, the length of time that the switch is open determines the amount of voltage charge built up on the capacitors. The high count error pulses and the anti-jitter pulses are fed through a three-stage amplifier and reversed diode to the same pair of capacitors. Thus the opposing error pulses operate in the same manner but in opposite directions. The voltage appearing at the drain output of Q6 is the afc voltage. High count error pulses (and anti-jitter

pulses) cause a decrease in the afc voltage while low count error pulses cause an increase in the afc voltage. The source voltage fed to Q6 is adjusted by a bias control to set the nominal afc working voltage. The afc voltage is then fed to amplifier-monitor 5TR1A2A3 or 1RE1A2A3.

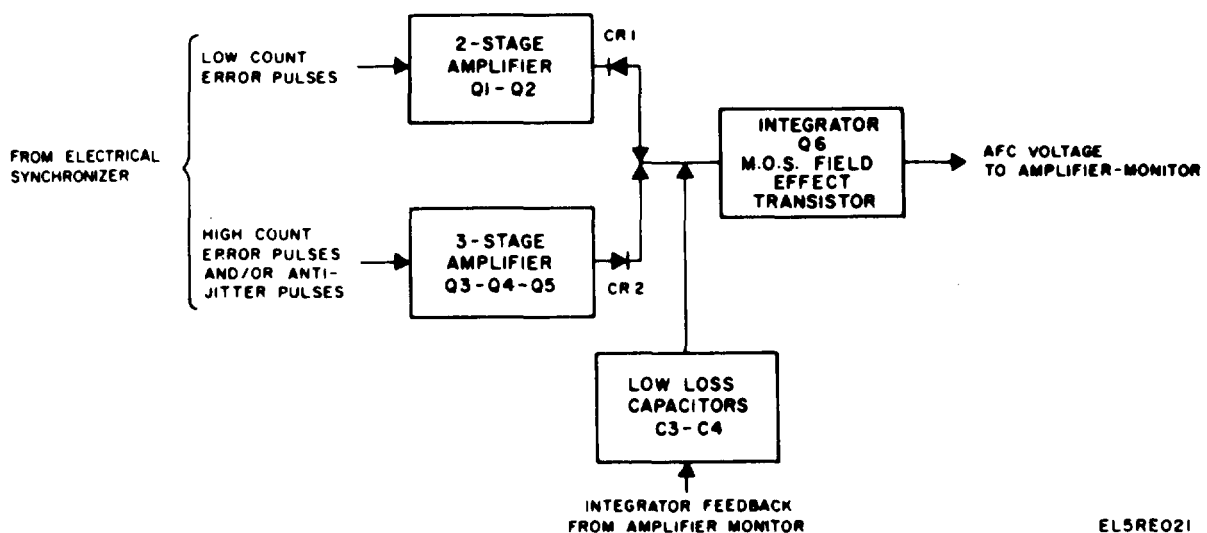
(3) Detailed circuit analysis (F0-4-15).

#### NOTE

The dynamic frequency store circuit, shown in the schematic diagram (F0-4-15), is not used at all; the circuit, however, has not been removed to date. The jumper between relay K1 contacts A1 and A3 insures continuity of the signal path, and the absence of an incoming signal at J8 pin 7 keeps the circuit inoperative.

(a) Low count error pulses from electrical synchronizer 5TR1A2A7 or 1RE1A2A7 are fed into the signal data converter-storer at J8 pin 11 and are coupled through C1 to the base of Q1. Transistor Q1 is normally conducting but upon receipt of a negative-going low count error pulse, Q1 cuts off, causing Q2 to conduct and 'draw 2 ma (0.6 ma. is drawn from the +12 v line (transmitter) through R4 and 1.4 ma is drawn from the integrating circuits C3 and C4 through diode CR1.) From Q1 collector the pulses are coupled through Q2, CR1, and a jumper between relay K1 contacts A2 and A3 to the low leakage capacitors C3 and C4.

(b) Similarly, high count error pulses are fed into the signal data converter storer from J8 pin 10 and coupled through C2 to the base of Q3. Transistor Q3 acts as a switch, normally conducting. When negative-going anti-jitter pulses (at the start count moment) or high count error pulses are received at the Q3 base, Q3 is cut off and the pulses are coupled through Q4 to PNP transistor Q5. Q5 inverts them and then CR2 passes them on to C2 and C3 through the K1 contact jumper. C3 and C4 are connected in the gate circuit of field effect transistor Q6. The source supply



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Figure 2-21. Signal Data Converter-Storer 5TR1A2A8 or 1RE1A2A8, Block Diagram.

to Q6 is adjusted by bias control R15 to establish the nominal afc voltage during setup. The output of Q6 at the drain is the afc drive to amplifier-monitor 5TR1A2A3 or 1RE1A2A3. The integrator feedback (J8 pin 9) is fed to the return side of low leakage capacitors C3 and C4 and is taken from the output of the feedback amplifier Q3 in the amplifier-monitor (para 2-14).

b. Model 5TR1A2A18 or 1RE1A2A18 (A Model).

(1) General. The function of signal data converter-storer 5TR1A2A18 or 1RE1A2A18 is the conversion and integration of high count and low count error pulses to a dc automatic frequency control (afc) voltage. The afc voltage is then fed through amplifier-monitor 5TR1A2A3 or 1RE1A2A3 to modulator-oscillator 5TR1A2A2 or 1RE1A2A2 (vco) where it is used to control the synthesizer output frequency.

(2) Block diagram analysis (Fig. 2-22). The low count and high count error pulses fed into the signal data converter-storer are negative-going pulses at approximately 4 volts peak-to-peak, whose widths are proportional to the actual frequency error of the vco output frequency. The low count error pulse (including the jitter pulse) is fed through a two-stage amplifier and a diode, to a pair of low-leakage capacitors in the gate circuit of a field effect transistor (FET). The two-stage amplifier is operated in saturation and acts as a switch which applies a constant amplitude voltage pulse to the capacitors. The width of low count pulses, proportional to the frequency error, determines the length of time that the switch is open and thus the amount of voltage change built up on the capacitors. The anti-jitter pulses and (if the vco frequency is too high) the high count error pulses are fed through a three-stage amplifier and a reverse diode to the same pair of capacitors; thus, the opposing error pulses operate in the same manner but in opposite directions. The voltage appearing at the drain output of the FET transistor is the afc voltage. High count error pulses (and anti-jitter pulses) cause a decrease in the afc voltage while low count error pulses cause an increase in the afc voltage. The source voltage fed to the FET is adjusted by a bias control to set the nominal afc working voltage.

(3) Detailed circuit analysis (FO-4-16). Low count error pulses from electrical synchronizer 5TR1A2A17 or 1RE1A2A17 pin 11 are coupled through C1 to the base of

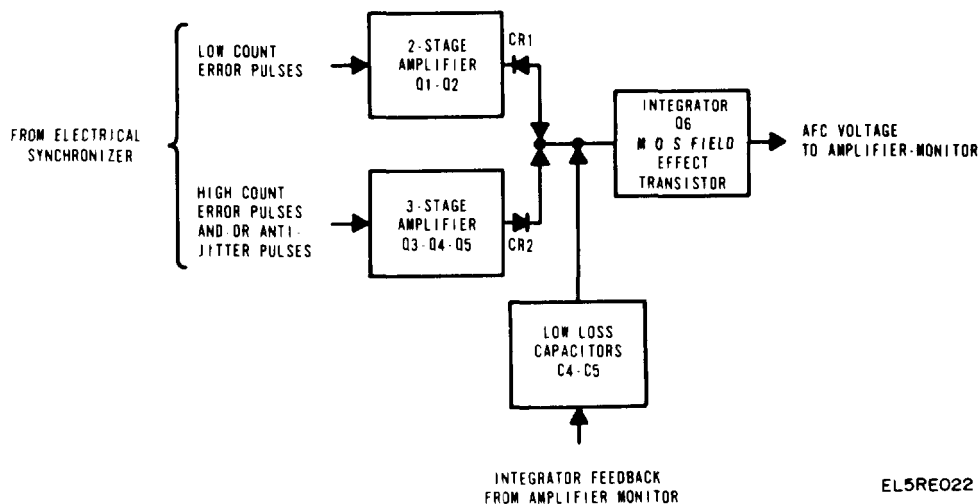


Figure 2-22. Signal Data Converter-Storer 5TR1A2A18 or 1RE1A2A18, Block Diagram.

Q1. Transistor Q1 is normally conducting, but upon receipt of a negative-going low count error pulse, it cuts off, causing Q2 to conduct and draw 2 ma (0.6 ma is drawn from the +12 volt line through R4 and 1.4 ma from the integrating circuit capacitors C4 and C5 through diode CR1). From Q1 collector, the pulses are coupled through Q2 and CR1 to the low-leakage capacitors C4 and C5.

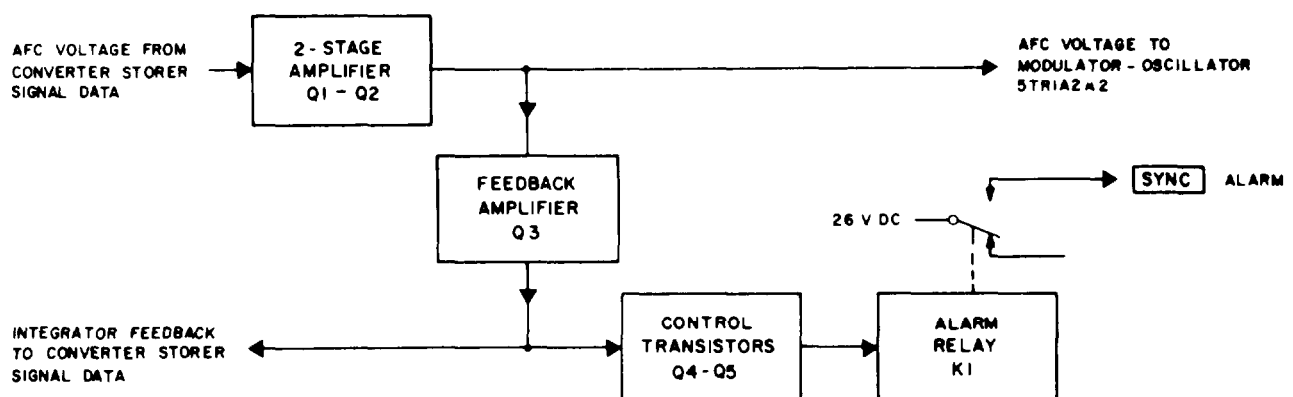
(a) Similarly, the high count error pulses at pin 10 are coupled through C3 to the base of Q3. Transistor Q3 acts as a switch, normally conducting. When the negative-going anti-jitter pulses (at the start count moment) and the high count error pulses are received at Q3 base, Q3 is cut off and the pulses are coupled through Q4 to PNP transistor Q5 which inverts them and passes them through CR2 to the low leakage capacitors C4 and C5.

(b) C4 and C5 are connected in the gate circuit of field effect transistor Q6. The source supply to Q6 is adjusted by bias control R16 to establish the nominal afc voltage during setup. The output of Q6 at the drain is the afc voltage drive, and is fed through pin 8 to amplifier-monitor 5TR1A2A3 or 1RE1A2A3. The integrator feedback at pin 9 is taken from the output of feedback amplifier Q3 in the amplifier-monitor (para 2-14) and is fed to the return side of the low leakage capacitors C4 and C5.

2-14. Amplifier-Monitor 5TR1A2A3 or 1RE1A2A3

a. General. Amplifier-monitor 5TR1A2A3 or 1RE1A2A3 amplifies the afc voltage to the required for frequency control, monitors the afc voltage and the presence of clock pulse D, and gives an alarm indication if frequency control is lost. This unit also provides the integrator feedback voltage to signal data converter-storer 5TR1A2A8 or 1RE1A2A8. (5TR1A2A18 or 1RE1A2A18 when radio is equipped with Electrical Frequency Synthesizer 5TR1A2 or 1RE1A2 Part No. SM-D-865030.)

b. Block Diagram Analysis (Fig. 2-23). The afc voltage at the output of the field effect transistor is fed to a two-stage cascade emitter follower, Q1, Q2, to adjust the afc voltage to the 2 to 9 volt range (4 to 8 volts when synthesizer equipped with modulator-oscillator 5TR1A2A2 or 1RE1A2A2, Part No. CMC 220-800159-000) required at modulator-oscillator 5TR1A2A2 or 1RE1A2A2. An inverted sample of the output afc is amplified in Q3 and fed back to the return side of the two low-leakage capacitors in the field effect transistor gate circuit in the signal data converter-storer as the integrator feedback circuit.



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Figure 2-23. Amplifier-Monitor 5TR1A2A3 or 1RE1A2A3, Block Diagram.

(1) The integrator feedback voltage is monitored and used to control the SYNC alarm relay K1. The SYNC alarm relay is normally operated by current through control transistors Q4-Q5, and drops out in the event of overvoltage or undervoltage. The normal current through the control transistor is preset by a SYNC alarm control.

(2) Clock pulse D is differentiated and fed to capacitor discharge transistor Q6. Loss of clock pulse D causes the capacitor to build up a voltage which overcomes the Zener diode bias and turns on control transistors Q4 and Q5, causing the SYNC alarm relay to drop out.

c. Detailed Circuit Analysis (Fig. 2-24).

NOTE

There are two versions of Amplifier-monitor 5TR1A2A3. Older models will contain semiconductors as shown in brackets in figure 2-24, new versions will have changes in semiconductors CR1, CR2, CR3 and CR4, and the value of resistor R8. Figure 2-24 shows both versions, the latter having the changed components identified by an asterisk. It is considered advisable that whenever a replacement of one, or more transistors (Q1 thru Q6) is made, that a simultaneous replacement of diodes CR3 and CR4 and resistor R8 be made. Changing CR1 and CR2 are not essential. Individual replacement of diodes CR1, 2 and 3 can be made with no impact on operation. In the event that CR4 is replaced, a similar change should be made to R8. The incorporation of these changes is considered necessary in order to prevent instability.

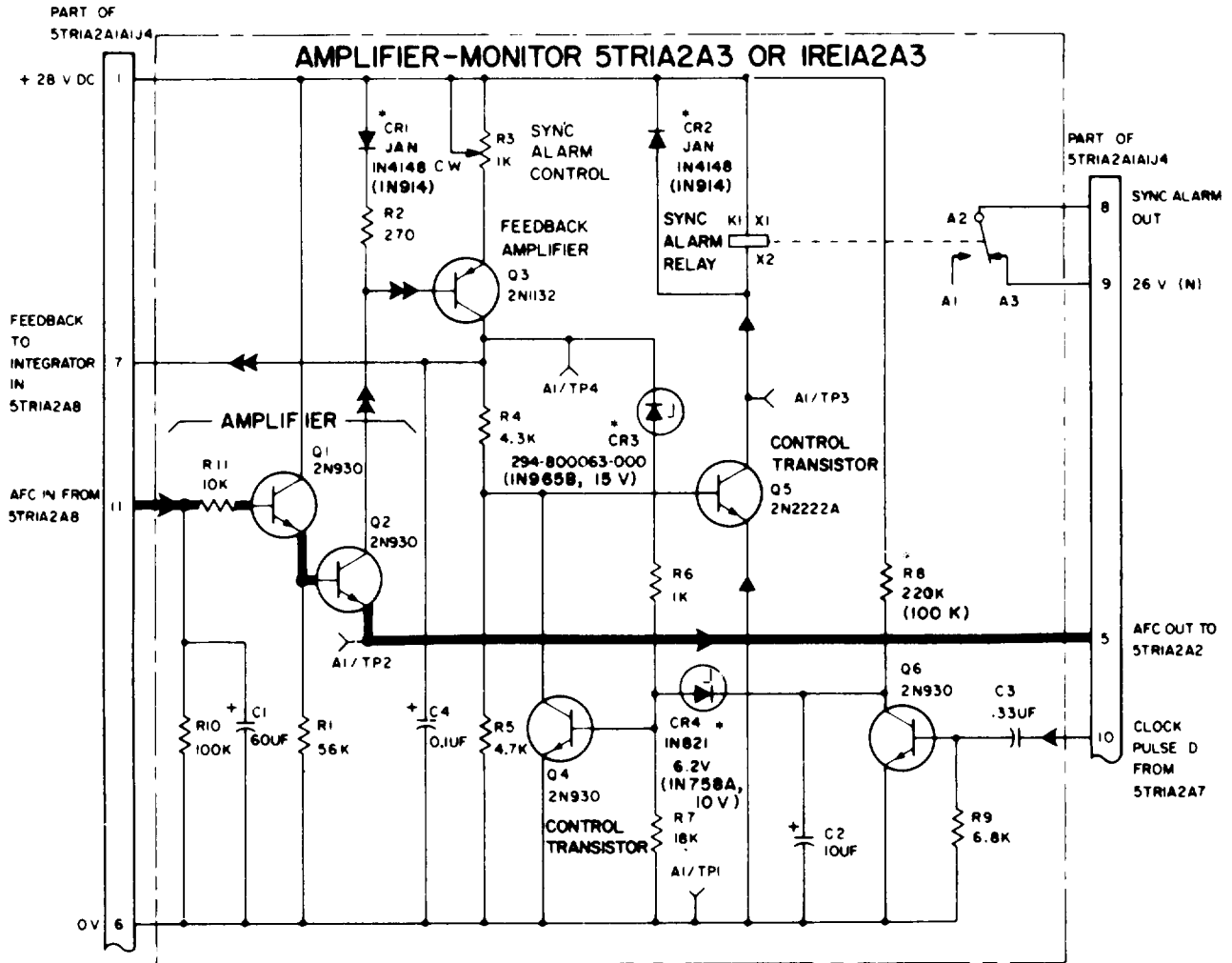
(1) Afc circuit. The afc drive at J4 pin 11 is fed through R11 to the base of Q1. The Q1 emitter is connected directly to the base of Q2, the output emitter follower; the afc signal at the Q2 emitter is then fed through J4 pin 5 to modulator-oscillator 5TR1A2A2 or 1RE1A2A2. The afc voltage in the range of 2 to 9 volts (4 to 8 volts when synthesizer equipped with modulator-oscillator 5TR1A2A2 or 1RE1A2A2, Part No. CMC 220-800159-000) is applied to the oscillator varactor in the modulator-oscillator board to generate output frequencies of 47.5 to 72.5 MHz (para 2-4).

(2) Integrator feedback. The voltage at the collector of Q2 is amplified in feedback amplifier Q3. The signal at the Q3 collector is fed through J4 pin 7 to the return side of the two low leakage capacitors, C3, and C4, of the integrator circuit in the signal data converter storer 5TR1A2A8 or 1RE1A2A8 (5TR1A2A18 or 1RE1A2A18 when radio is equipped with Electrical Frequency Synthesizer 5TR1A2 or 1RE1A2, Part No. SM-D865030).

(3) SYNC alarm operation. The SYNC alarm circuit operates when the afc voltage is either below or above set limits or when clock pulse D is absent. Normally, relay K1 is kept operated by current through control transistor Q5. The base of Q5 is connected in a voltage divider circuit and senses the current through control transistor Q4. The afc reference voltage is taken from the collector of Q3, the feedback amplifier. Since Q3 is a PNP transistor, a rising voltage at its base (equivalent to a drop in afc output voltage) will tend to cut it off. This will cause the voltage at the Q3 collector to fall, pulling down the Q5 base through R4. Q5 will



then cut off, letting K1 drop out. The SYNC alarm path through relay K1 contacts is open and the SYNC alarm is on. If the output afc increases above its reference value, the Q3 base will drop causing its collector to rise above 15 volts and fire Zener CR3. This will cause the Q4 base to rise, turning Q4 on. When Q4 conducts, its collector will fall, lowering the Q5 base. Q5 will then cut off, letting K1



NOTES:

1.

| SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEGOMM           |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

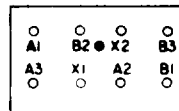
2. THE VOLTAGES SHOWN ARE THOSE USED IN THE TRANSMITTER. FOR RECEIVER CONVERT AS FOLLOWS:

| TRANSMITTER | RECEIVER |
|-------------|----------|
| +28 V DC    | +12 V DC |
| 0V          | -12 V DC |

\* SEE NOTE PARA 2-14C

- 3
- MAJOR FUNCTIONAL FLOW
  - FEEDBACK
  - SECONDARY FUNCTIONAL FLOW
  - SIGNAL PATH TO ENERGIZE RELAY

4. RELAY BASE PINS AS VIEWED FROM PIN END



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Figure 2-24. Amplifier-Monitor 5TR1A2A3 or 1RE1A2A3, Schematic Diagram.

drop out and indicate an alarm condition. Afc SYNC alarm operation is adjusted by control R3, which varies the current through Q3. Clock pulse D at J4 pin 10 is differentiated by C3 and R9 producing positive pips at the Q6 base. These positive pips cause Q6 to discharge C2. If clock pulse D fails, the discharge action stops and the C2 voltage builds up toward the supply voltage. When it reaches 10 volts (6.2 volts on later models with semiconductors CR1, CR2, CR3 and CR4 as shown with asterisk in figure 2-24), Zener CR4 fires, raising the Q4 base voltage, turning Q4 on and causing Q5 base voltage to fall. Q5 cuts off and lets relay K1 drop out, to indicate a SYNC alarm.

2-15. Interconnecting Box

a. Model No. 5TR1A2A1 or 1RE1A2A1.

(1) General. The interconnecting box 5TR1A2A1 or 1RE1A2A1 provides all the interconnecting facilities between the nine various printed circuit boards and to the two external connectors J11 and P2 of the synthesizer. J11 connects the synthesizer to the transmitter fixed head or receiver fixed head chassis. P2 connects the synthesizer to amplifier-frequency multiplier 5TR1A4 or 1RE1A4.

(2) Detailed circuit analysis (FO-4-3). A +28 vdc is applied through P2 pin 1 and resistors R2 through R13 to the AND gates of the programmed counters in digital electronic counter 5TR1A2A6 or 1RE1A2A6 and digital electronic divider-counter 5TR1A2A5 and 1RE1A2A5. +28 vdc is also applied through R14 to the divide-by-3 (line 13) circuits in rf oscillator 5TR1A2Y1 or 1RE1A2Y1. When a control line is coded, the corresponding microswitch in the control-indicator is open; +28 vdc is applied through a resistor in the base of the corresponding transistor gate and allows clock pulse D to preset the counter to one state (pin 8). When a control line is not coded, the corresponding microswitch in the control indicator is closed, grounding the base of the transistor and preventing clock pulse D from getting through the respective binary.

(a) Filter FL1 couples a portion of the rf output from modulator-oscillator 5TR1A2A2 or 1RE1A2A2 to the high speed divider in frequency divider 5TR1A2A4 or 1RE1A2A4. The purpose of FL1 is to prevent any harmonics of the output signal from being coupled from the high speed dividers back to the output line.

(b) The voltages available to operate the synthesizer are different in the transmitter from those in the receiver. The voltages available are:

|                   |                   |                  |
|-------------------|-------------------|------------------|
| Transmitter Duty: | 28 vdc regulated  | P2 pin 1         |
| (Supplied)        | +12 vdc regulated | P2 pin 2         |
|                   | 0 vdc             | P2 pin 3         |
|                   | 26 V (N)          | P2 pin 5         |
|                   | +28 vdc regulated | P2 pin 37        |
| Receiver Duty:    | +12 vdc regulated | P2 pin 1, 37, 88 |
| (Supplied)        | 0 vdc             | P2 pin 2         |
|                   | -12 vdc regulated | P2 pin 3         |
|                   | 26 V (N)          | P2 pin 5         |

(c) Two additional voltages are required by various circuits in the synthesizer:

|                   |         |     |
|-------------------|---------|-----|
| Transmitter Duty: | +20 vdc | E29 |
|                   | +16 vdc | E28 |

Receiver Duty:      +8 vdc      E29  
                          +4 vdc      E28

(d) These additional voltages are provided by a power supply divider circuit; CR1, CR3, R1 and R20. Zener diodes CR1 4.3 v and CR2 8.2 v provide regulation. The 4 volt discrepancy between the voltage available for transmitter duty as opposed to receiver duty is taken care of by dropping the extra voltage in a load resistor.

(e) In order that the synthesizer can be interchanged between the transmitter and receiver, the regulated dc return paths are connected to the respective power supply ground points rather than being grounded within the unit.

(f) C1 C2, C4, C5 and C6 are used to filter the +12 v, +28 v, +20 v, 0 v and +16 v supplies respectively. CR3, CR4, CR5 and R15 are part of the afc hold circuit which is not used. R19 provides a termination for the rf divided by 8 signal.

b. Model No. 5TR1A2A11 or 1RE1A2A11 (A Model).

(1) General. Interconnecting box 5TR1A2A11 or 1RE1A2A11 provides all the interconnecting facilities between the eight various printed circuit boards and to the two external connectors J11 and P2 of the synthesizer. P2 connects the synthesizer to chassis of the transmitter fixed head and the receiver fixed head. J11 connects the synthesizer to amplifier-frequency multiplier 5TR1A2 or 1RE1A2.

(2) Detailed circuit analysis (F0-4-4). A +28 vdc is applied through P2 pin 1 to the amplifier-monitor, signal data converter-storer, and rf oscillator boards. The +28 vdc is also applied through P2 pin 37 to J11 pin 1 for use with the respective amplifier-frequency multiplier. A +12 vdc is applied through P2 pin 2 to the modulator-oscillator and signal data converter-storer boards.

(a) Two additional voltages are required by various circuits in the synthesizer; +11.5 vdc for the bandpass filter in frequency divider board, and +5 vdc for all boards containing binaries and NAND gates. These voltages are provided by a regulated power supply comprising Q1, A2, zener diode CR2, and switching diode CR1. Resistors R3, R4, R5 and R6 supply bias and collector loads. Capacitors C1 C2, C3 and C4 filter the output voltage. The regulated +5 vdc is supplied to the rf oscillator, frequency divider, electrical synchronizer, digital electronic counter and digital electronic divider-counter boards.

(b) A portion of the rf output of the modulator-oscillator is fed through R1 , a 270 ohm resistor, to the frequency divider board. Control lines 0 to 12 inclusive are fed through P2 to the digital electronic counter and digital electronic divider-counter boards. The voltages mentioned above are those available from the transmitter; for receiver use convert as follows:

| Transmitter | Test point | Receiver |
|-------------|------------|----------|
| 0 v         | P2-Pin 3   | -12 v    |
| +12 v       | P2-Pin 2   | 0 v      |
| +28 v       | P2-Pin 37  | +12 v    |
| +5 v        | TP1        | +5 v     |
| NC          | P2-Pin 38  | +11.5 v  |

2-16. Amplifier-Frequency Multiplier 5TR1A4

a. General. Amplifier-frequency multiplier 5TR1A4 doubles the output frequency of synthesizer 5TR1A2, and amplifies the resulting signal to the level required by subsequent multipliers in the transmitter frequency generating chain.

b. Block Diagram Analysis (Fig. 2-25). The synthesizer modulated rf output in the range of 47.5 to 72 MHz, at a level of +13 dbm±1 db, is first fed to low pass filter FL1. The low pass filter attenuates all unwanted harmonics generated by the synthesizer, which would otherwise lower the efficiency of the doubler circuit. The rf signal at the output of the filter is applied to a 4 to 1 transformer T1, which converts the unbalanced input line to a balanced input to fullwave rectifier CR1. CR1 consists of a matched pair of hot-carrier diodes. Hot-carrier diodes provide efficient frequency doubling with low spurious outputs. The rectifier output circuits are balanced to remove the fundamental input frequency and all odd harmonics. Total conversion loss is about 8 db; the resulting signal, about +5 dbm, is applied to three-stage, stagger-tuned, medium-power amplifier Q1, Q2 and Q3. The first stage provides maximum gain at the low end of the output frequency range while the second stage provides maximum gain at the high end of the output frequency range. The third stage is a high power unit providing maximum gain at the middle of the output frequency range. The overall gain of the amplifier is about 32 db. The output of the amplifier is then coupled through a 1 db matching network to a tuned pi-type rf filter which attenuates all unwanted harmonic signals. The output signal is in the range of 95 to 145 MHz at 3 watts; output impedance is 50 ohms and fm deviation of the output signal is doubled during the frequency doubling process. A dc metering signal derived from the output signal provides an indication of the actual power delivered to the frequency multiplier chain (DOUBLER metering).

c. Detailed Circuit Analysis (F0-4-38). The synthesizer rf output is fed through P1-A1 to low pass filter FL1. FL1 is a conventional LC-type low pass filter mounted on a separate board. The unbalanced output of FL1 is coupled through C8 to terminals 1 and 2 of transformer T1. The output at pins 3 and 5 of T1 is balanced to ground and stepped up in voltage four times to increase the efficiency of full wave rectifier CR1. Balanced tuning circuits L6, C10, R1 and 15, C9 and R2 eliminate the fundamental frequency and all odd harmonics of the fundamental. Balance of the two sides of the rectifier output is achieved by adjusting R1 and R2, the harmonic reject potentiometers. The output of the rectifier at twice the input frequency is then coupled through C11, C12, C14, 18 and C19 to the base of Q1, the first stage amplifier. C14 is adjusted for optimum input matching to Q1. The output at the

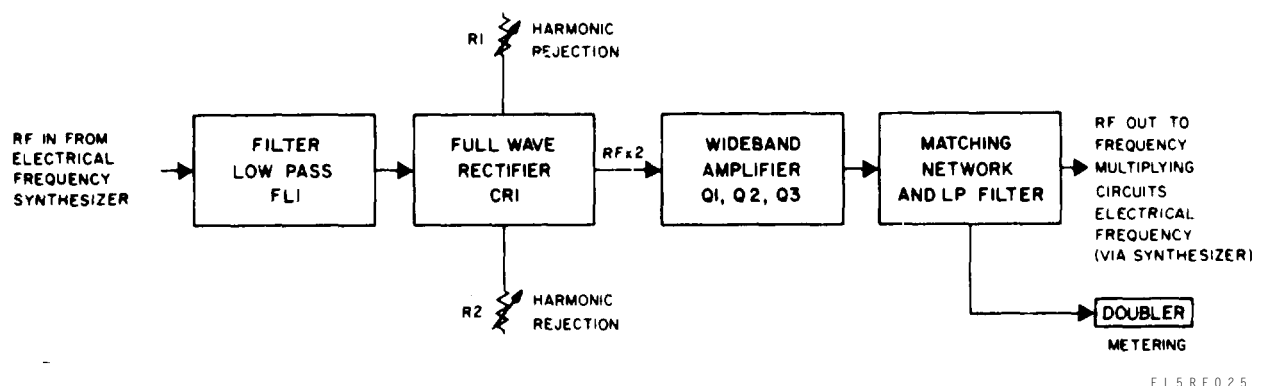


Figure 2-25. Amplifier-Frequency Multiplier 5TR1A4, Block Diagram.

collector of Q1 is coupled through C21 and L11 to the base of Q2. C22 adjusts the low-frequency portion (95 to 120 MHz) of the first amplifier stage response. The signal at the Q2 collector is then coupled through C26 and L13 to the base of Q3. The response of the second amplifier stage is tuned by C26 and C27 to favor the high frequency portion (120 to 145 MHz) of the input. The Q1 and Q2 base voltages are derived from the +28 vdc line through voltage dividers R8, and R5 for Q1, and R8 and R10 for Q2. The base voltage is filtered by C17 and C23 and kept constant at 6 v by Zener diode CR3. The first two stages of amplification provide a controlled gain of approximately 10 db each. Q3 is a high power wideband output amplifier. C31 adjusts the response of Q3 to the center portion of the input, and Q3 provides approximately 12 db gain from 95 to 145 MHz.

(1) The signal at the collector of Q3 is coupled through L16 and C32 to a 1 db resistive network, R13, R14, R15 and R16, for impedance matching before the signal is filtered in a pi-type low pass filter, L18, L19, C35, L20, C36 and L21. C35 and C36 adjust the response of the low pass filter. The filtered output at twice the synthesizer output frequency is then coupled through C37 to output connector P1 pin A2, for distribution to the frequency multiplying circuits in the transmitter rf head.

(2) The metering signal (DOUBLER) is derived from the voltage drop across L15 in the Q3 collector circuit, rf filtered by C33 and FL1, then made available at P1 pin 10. The metering return line at P1 pin 12 is decoupled to rf by L17, R17 and C34. Diode CR1 across the metering circuit provides scale expansion.

(3) The automatic level control (alc) circuit, pin diode CR2, is not used in the Band I configuration. The alc line at P1 pin 17 is grounded in the transmitter rf head. Resistor R18 is an additional load for the +12 vdc supply to the synthesizer (P2 pin 2 of 5TR1A2) and has been located in this unit for convenience. The +28 vdc supply to the amplifier-frequency multiplier is brought in directly through connector P2 pin 37 and J11 pin 1 of synthesizer 5TR1A2 to P1 pin 1.

## 2-17. Alarm Control 5TR1A3

a. General. Alarm control 5TR1A3 operates in conduction with power monitor 6AR1-A3 in the transmitter rf head to provide a warning in the form of both audible and visual alarms when the transmitter output power falls 8 db below its normal level. The alarm control operates from a center-tapped, 400 Hz supply.

b. Block Diagram Analysis (Fig. 2-26). Power monitor 6AR1A3 rectifies a sample of the rf output signal into a dc signal. This low level dc signal (0.25 v minimum) is used to keep one side of a low drift balanced dc amplifier (Q1-Q2) conducting and alarm relay K1 energized. If the dc signal falls below the required compensating

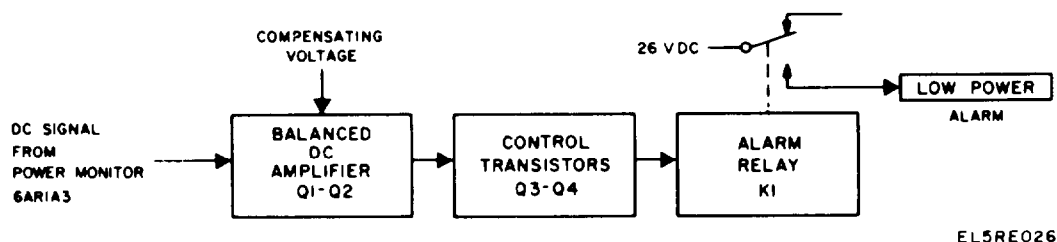


Figure 2-26. Alarm Control 5TR1A3, Block Diagram.

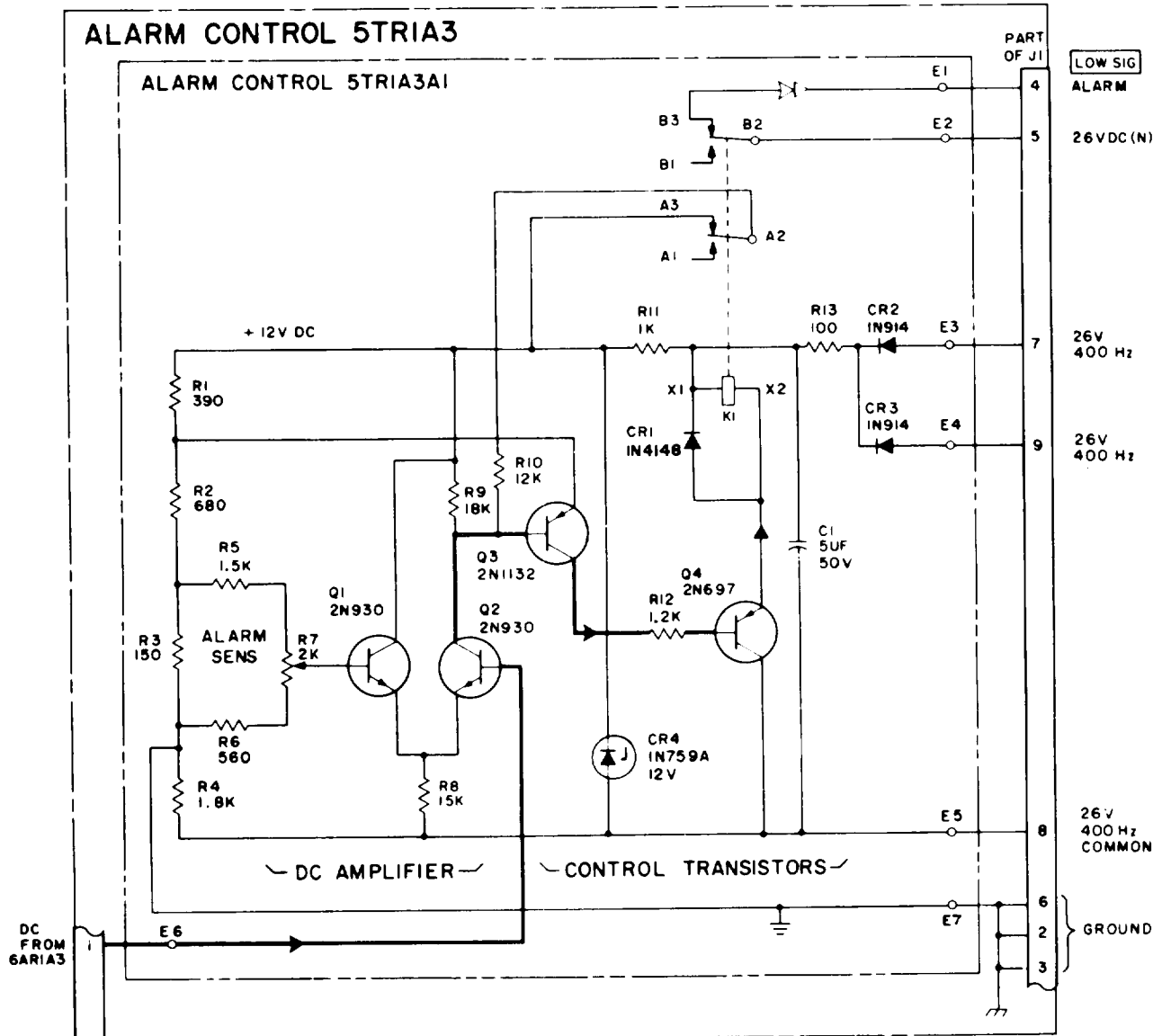
voltage, the dc amplifier is cut off and the relay drops out, causing the LOW POWER alarm light to go on and the buzzer to sound. The alarm condition comes on when the output level is 8 db below the nominal transmitter output level, and is cut off when the output level returns to about 6 db below nominal. The 2 db tolerance has been introduced to prevent the relay from chattering when the power level remains stable around the trip point.

c. Detailed Circuit Analysis (Fig. 2-27). The incoming dc signal derived from power monitor 6AR1A3 is applied to the base of Q2. Q1 and Q2 are part of a balanced dc amplifier of the long tail pair (R8) configuration. A compensating dc voltage is applied to the base of Q1 from bias voltage divider R1 through R7. The 52 v supply is derived from a center-tapped winding of the 400 Hz inverter transformer in power supply 5TR1PS1. This ac supply is rectified by CR2 and CR3 and the resulting 12 vdc is smoothed by R13 and C1 and stabilized by Zener diode CR4. R5, R6 and R7 in parallel with R3, allow for a very fine voltage adjustment of the Q1 base voltage by restricting the adjustment range of R7. R7 is adjusted so that the base of Q1 is somewhat positive with respect to ground. When no dc is available from the power monitor, Q2 is cut off, and so are Q3 and Q4; relay K1 is de-energized and the alarm condition is on, the buzzer sounds and the LOW POWER alarm light is on. As the output power of the transmitter increases, Q2 begins to conduct and Q1 is cut off; this action taking place at a sharply defined point of operation. At a certain point in the conduction of Q2, Q3 starts to conduct; this happens when the voltage drop across R9 is equal to the voltage drop across R1 plus an additional 0.5 v (Q3 emitter-base threshold). When Q3 conducts, Q4 also conducts and relay K1 becomes energized; this is the normal position. When K1 is energized, the LOW POWER alarm circuit is open. Resistor R10, switched into and out of the Q3 circuit by relay K1 contacts, provides some backlash to the circuit. CR1 protects Q4 against large inductive spikes which can occur when Q4 cuts off.

## 2-18. Power Supply 5TR1PS1

a. General. Power supply 5TR1PS1 provides all the regulated and unregulated dc and ac supplies used throughout the transmitter fixed and rf heads. It provides regulated supplies of 12 v and 28 vdc used in the active circuits, 26 vdc unregulated to relays and alarm circuits, 630 vdc unregulated plate supply to the power amplifier tubes in the transmitter rf head, two supplies of 7.2 vdc unregulated for the heaters of the power amplifier tubes, 128 vat, 400 Hz square wave for the blower motor, and a 52 vat, 400 Hz square wave output for the alarm control. It also contains current regulators for the cathode supply to power amplifier tubes in the transmitter rf head. A high voltage surge protector is connected at the line input to the unit. Further overvoltage protection is provided immediately following the choke-input filter. The regulators are current-limited for short circuit protection. The inverters are provided with starting circuits to provide immediate operation upon application of power. Power supply 5TR1PS1 consists of four subassemblies, interconnected by a wiring harness.

b. Block Diagram Analysis (Fig. 2-28). The 115 vat, 47 to 420 Hz, source supply is applied through a 5 ampere circuit breaker mounted on the front panel (AC POWER ON/RESET), a surge suppressor (lightning arrestor) and a current limiter circuit, to a full-wave bridge rectifier, CR1 and CR4. The current limiter circuit is by-passed by relay contacts once the inverters are operating and 26 vdc supply is available. The output of the rectifier is fed through a filter and a Zener diode to inverter starting relay K1. K1 produces a momentary bias surge (20 milliseconds) when the power supply is initially switched on. During the 20 milliseconds bias surge, the operation of both the 400 Hz and 5 kHz inverter circuits is initiated.



PART OF J1

NOTES

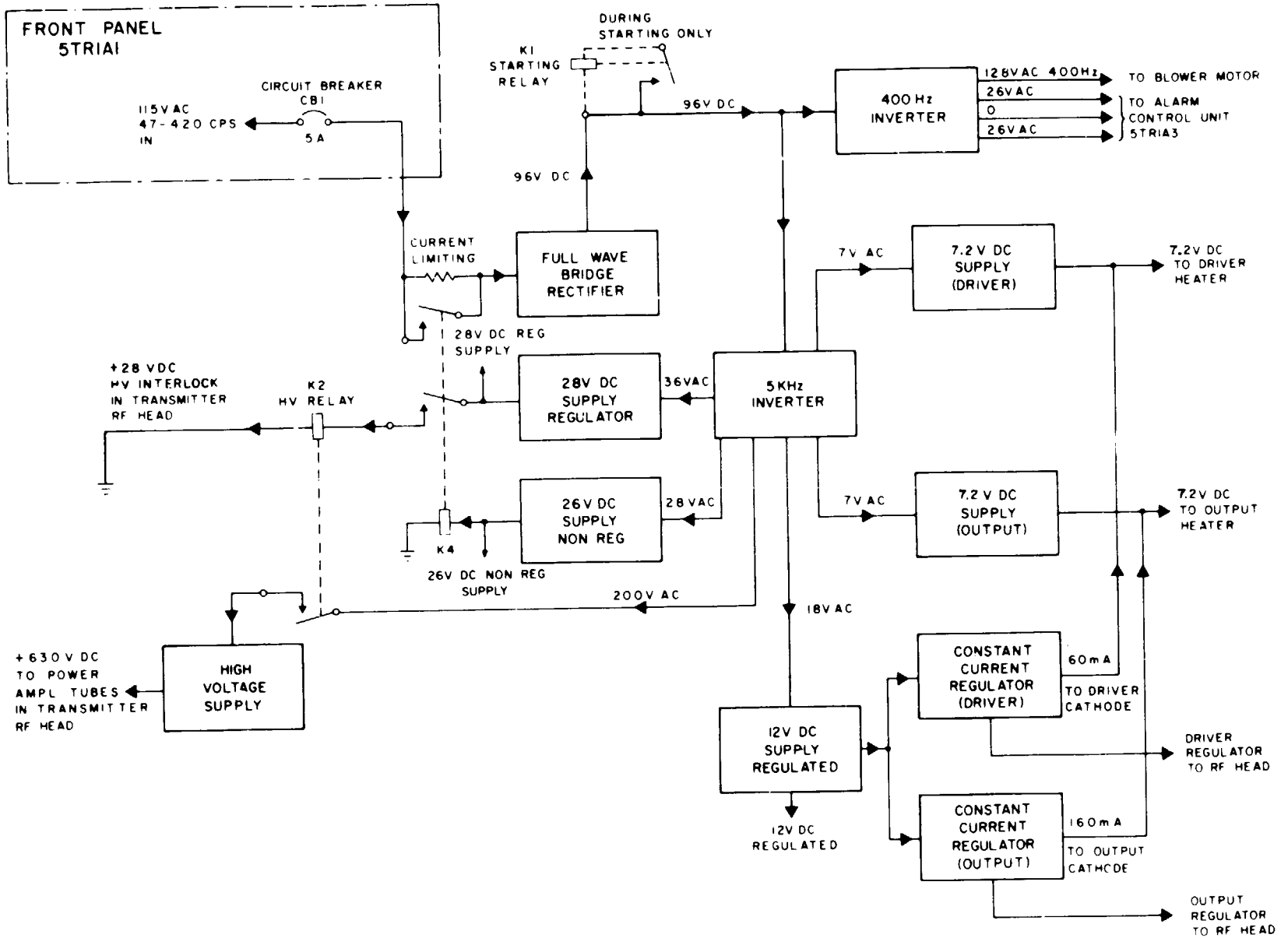
| SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEGOHM           |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

- 2- RELAY BASE PINS AS VIEWED FROM THE PIN END.
- 3- FAULT SIGNAL TO PROVIDE INDICATION.
- SIGNAL PATH TO ENERGIZE RELAY.
- SECONDARY FUNCTIONAL FLOW.

EL5RE027

Figure 2-27. Alarm Control 5TRIA3, Schematic Diagram.

Figure 2-28. Power Supply STRIPSI, Block Diagram.



EL5RE028



(1) The 400 Hz and the 5 kHz inverter circuits each consist of a multi-winding transformer and two switching transistors as part of an inverter-type power supply circuit. Each inverter circuit also contains spike suppressor base current limiters, switching speed-up diodes and short circuit protection devices.

(2) The 400 Hz inverter transformer, T1, provides a 128 v square wave at 400 Hz, to operate centrifugal fan 5A2B1. It also supplies a 26-0-26 v square wave at 400 Hz, to alarm control 5TR1A3; the transformer's center tap is returned to ground through a resistor in the 5TR1A3 unit.

(3) The secondary winding of 5 kHz inverter transformer T2 is tapped to provide 5 kHz square wave outputs from which the 26 v, 28 v, 12 v, 630 v and 7.2 vdc outputs are derived.

(4) The 26 vdc nonregulated supply is derived from a secondary winding of transformer T2, rectified and filtered before being fed to the output connector for distribution. The 26 vdc supply also energizes relay K4, which in turn switches out input surge limiting resistor R48. Relay K4 contacts also close the 28 vdc path through high voltage relay K2.

(5) The 28 v and the 12 vdc regulated supplies are derived from a center-tapped winding of T2 (36 vat), rectified and filtered to provide 36 vdc to the 28 v regulator and 18 vdc to the 12 v regulator circuit. A pre-regulator supply (44 vat) for the 28 v and 12 v regulators is taken across another center tapped winding of T2. The pre-regulator circuits increase regulation efficiency by providing a second feedback control voltage in parallel with the amplified feedback signal of the output voltage. Most of the transistors throughout the transmitter operate from the 12 vdc supply, while high power transistors require 28 vdc regulated supply. 28 vdc is also fed through relay K4 contacts to relay K2 and is grounded through the HV interlock circuit in the transmitter rf head. When K2 is energized, the 200 vac appearing across the primary winding of T2 is connected to the primary winding of step-up transformer T3. The voltage developed across the secondary winding of T3 is rectified and filtered to produce the 630 vdc plate supply for the power amplifier tubes.

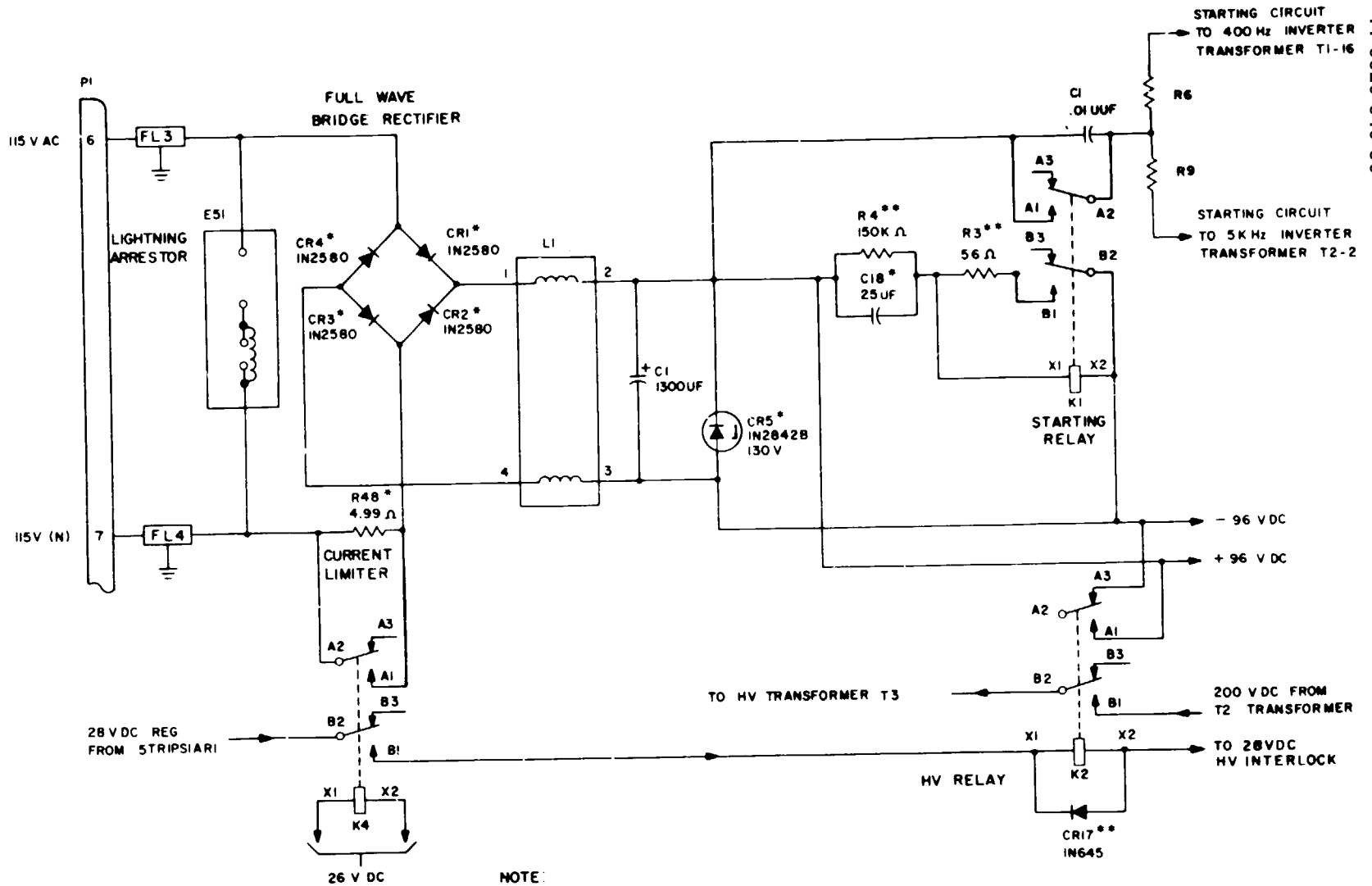
(6) The two 7.2 v filament (heater) supplies for the driver and output tubes of radio frequency amplifier 6AR1 are derived from another winding of T2. These voltages are separately rectified and filtered before being fed to the tubes.

(7) The two cathode current supplies to the power amplifier tubes are similarly derived from a T2 winding. The cathode current of the driver tube is regulated at 60 milliamperes, and the cathode current of the output tube is regulated at 160 milliamperes, to extend tube life. These current regulating circuits are returned to ground, through variable resistors mounted in the transmitter rf head. The variable resistors are used to set the currents to their nominal values.

### c. Detailed Circuit Analysis (F0-4-40).

(1) Input circuit (Fig. 2-29). The 115 volt ac, 47 to 420 Hz source is fed through a 5 amp circuit breaker (AC POWER ON/RESET), mounted on the front panel of the transmitter fixed head, to contacts 6 and 7 of P1 of 5TR1PS1. The 115 v supply is then fed through filters FL3, FL4, lightning arrestor E51 and current limiting resistor R48 (in power supply subassembly 5TR1PS1A2) to full-wave bridge rectifier CR1-CR4. The current limiting resistor R48 is by-passed by contacts A2 and A3 of

Figure 2-29. Power Supply, Output and Starting Circuits, Simplified Schematic Diagram.



NOTE:  
 ITEMS MARKED WITH \* ARE MOUNTED  
 ON THE POWER SUPPLY SUBASSEMBLY STRIPSI A2  
 ITEMS MARKED WITH \*\* ARE MOUNTED  
 ON THE POWER SUPPLY SUBASSEMBLY STRIPSI A1  
 ALL OTHERS ARE PART OF THE MAIN CHASSIS  
 ASSEMBLY STRIPSI.

relay K4, once the power supply is operating normally. Relay K4 is energized by the 26 v unregulated supply. The output of the bridge rectifier (96 v pulsed dc) is then fed through filter L1 and C1 to relay K1 which is part of the starting circuit, with Zener diode CR5 providing overvoltage protection.

(2) Starting circuit (Fig. 2-29). Starting relay K1, when initially energized (power supply just switched on), applies a start pulse to both inverter circuits simultaneously. A momentary forward bias is applied to the bases of all four inverter transistors, Q1 and Q2 (400 Hz inverter) to insure a positive start of oscillations. Charging current in C18 flows through the relay K1 coil to energize it. The time constant of C18 and R4 is such that relay K1 remains energized for approximately 20 milliseconds. The start pulse is then applied through K1 contacts A1 and A2, and R6 and R9 to the base windings of inverter transformers T1 and T2 respectively. K2 is the HV supply interlock circuit. 28 volt dc regulated is applied to one side of K2 coil through K4 contacts B1 and B2; the other side of the coil is connected to ground through the HV interlock circuit in the transmitter rf head. K2 contacts B1 and B2 apply the 200 v from 5 kHz inverter transformer T2 to the input of high-voltage transformer T3.

(3) 400 Hz inverter circuit (Fig. 2-30). Basically the inverter consists of two switching transistors and a transformer having a square hysteresis loop, the size and the shape of the hysteresis loop determining the oscillation frequency and output voltage waveform. Base input windings on the primary side of the transformer provide the feedback while the main primary winding provides the collector load. The operation of both the 400 Hz and 5 kHz inverter circuits is identical; only the 400 Hz one will be described in detail. When voltage is applied to the circuit, 96 vdc appears between terminal 5 of inverter transformer T1 and the emitters of Q1 and Q2 through resistor R5. Bias voltage is momentarily applied to Q1 and Q2 through resistor R5. Bias voltage is momentarily applied to Q1 and Q2 bases from pin 16 of transformer T1. When switching is initiated, voltages appearing at pins 15 and 17 of T1 are of opposite polarity, thus at any one time, the base of one transistor will be forward biased while the other will be reverse biased. Due to the forward bias, Q1 emitter-collector voltage will drop to about 1 volt. 96 v is developed across winding 1-5 of T1 and by mutual inductance 96 v series aiding is developed across winding 5-9 of T1; the resulting 192 v will appear at the collector of Q2, which is cut off due to the reverse bias on its base. These voltage conditions remain until transformer T1 saturates (a period of 1/500 second). As saturation is reached, the flux lines collapse, inducing voltages in the opposite direction in all windings. This causes a reversal of current and voltage relationships on Q1 and Q2; Q2 will conduct and Q1 will be cut off. Since transformer T1 has a square hysteresis loop, the changeover in the direction of the voltage occurs very sharply and the resulting output voltage is an ac square wave whose frequency is 400 Hz. When Q1 and Q2 are switching, CR2 and CR3 conduct the out-of-phase current which results from the inductive load presented by centrifugal fan 5A2B1. CR1 and CR4 are speedup diodes passing the negative-going collector voltages to the base of the transistor which is being cut off. R1, R2, R7 and R8 limit the base drive in Q1 and Q2; C3 and R6 form a surge-limiting circuit providing a load during the Q1 and Q2 switchover. Resistor R5 provides short circuit protection. If the load current on either of the two output lines becomes excessive, a higher than normal collector current will flow through the conducting transistor, causing a high voltage drop across R5. This will bias off both transistors, shutting down the inverter. The inverter cannot start again until the power supply has been turned off and then back on because it requires a start pulse to initiate the switching action. C2 helps to speed up the switching action by effectively shorting out R8 during switch-over. The 128 v

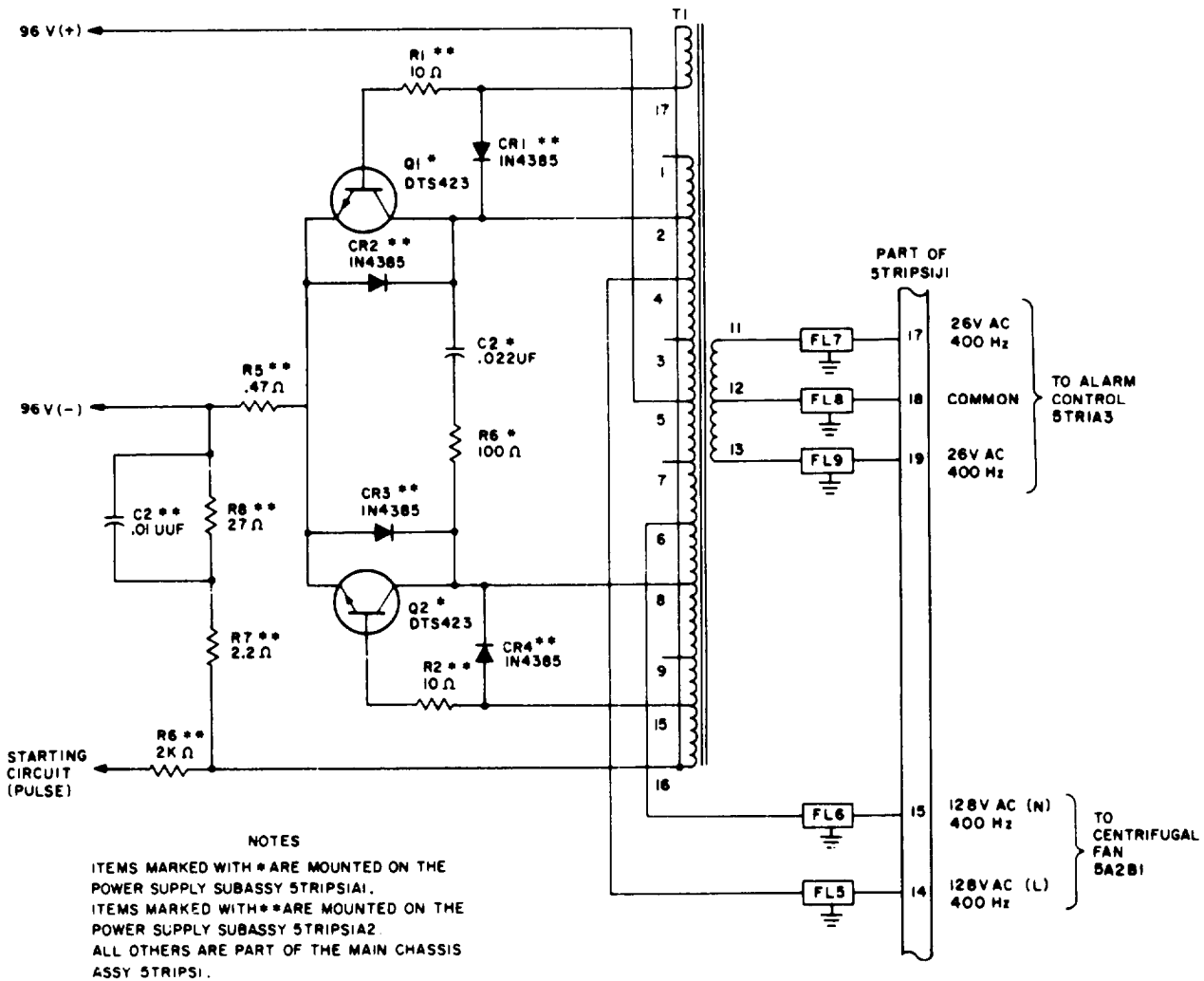


Figure 2-30. Power Supply, 400 Hz Inverter Circuit, Simplified Schematic Diagram.

ac, 400 Hz square wave for centrifugal fan operation is taken from terminals 4 and 6 of transformer T1, and fed through filter connectors FL5 and FL6 to the centrifugal fan. 26-0-26 vac for LOW POWER alarm operation is taken from secondary winding 11, 12 and 13 of T1 and fed through filter connectors FL7, FL8 and FL9 to alarm control 5TR1A3.

(4) 5 kHz inverter circuit (Fig. 2-31). The 5 kHz inverter circuit consists of switching transistors Q3 and Q4. A 96 vdc starting pulse is applied through R9 to pin 4 of inverter transformer T2. The operation of the 5 kHz inverter is identical to the operation of the 400 Hz inverter except that it requires additional protective components due to its greater load and higher frequency. Choke L2 speeds up the switching of the transistors. CR14 provides an additional protection against current flowing in the reverse direction through transistor Q3 or Q4. Zener diodes CR8 and CR9 limit the transient voltage spikes appearing at the collector of the cut off transistor. CR7 and CR10 direct the current through Zener diodes CR8 and CR9. CR6 and CR11, with CR5 and CR12, are also used to speed up switching in order to

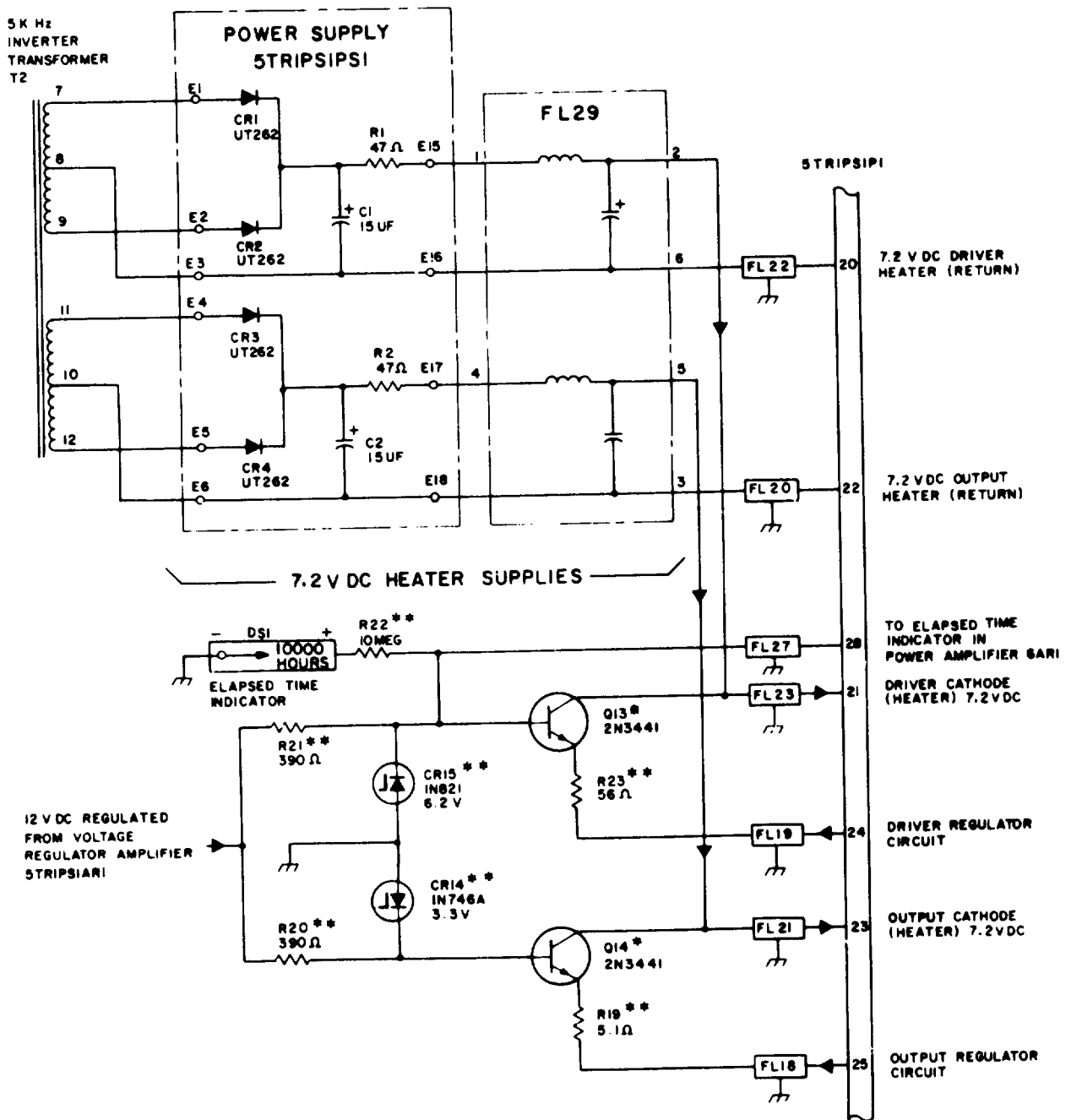


minimize heat dissipation. R12, a 0.332 ohm resistor, provides short circuit protection. If the load current on the 600 v line becomes excessive, a higher than normal current will flow through the conducting transistor, causing a high voltage drop across R12. This will bias both Q3 and Q4, shutting down the inverter. The inverter cannot start again until the power supply has been turned off and back on again. A 200 vat, 5 kHz square wave output is taken from across the primary winding 1-3 of inverter transformer T2 and fed through relay K2 contacts B1-B2 to the primary winding of high voltage (HV) step-up transformer T3. Voltage taken from across secondary winding 13-14 is rectified in CR26, smoothed by C20 (15 uf), and filtered by L1 and C4, to produce the 26 vdc unregulated supply for alarms, relays and indicator lamp operation. 26 vdc is fed directly to the relay K4 coil; K4 contacts close to bypass surge limiting resistor R48, when the power supply is operating normally (fig. 2-29). 26 vdc unregulated is also fed through filters FL16 and FL17 to P1 pins 4 and 5 for distribution. Two separate 16 vac peak, center-tapped, 5 kHz square wave outputs are taken across windings 7, 8, 9, and 10, 11, 12, of transformer T2 and fed into power supply 5TR1PS1PS1 ((5) below). The 36 vat, 5 kHz square wave output taken from pins 15, 16 and 17 of T2 is fed into full wave rectifier CR16 and supplies 36 v and 18 v to the 28 v and 12 v regulator circuits in voltage regulator amplifier 5TR1PS1AR1. A 44 vac output voltage taken across pins 18, 19 and 20 is rectified and is then used as the pre-regulator supply for the 28 vdc regulated supply.

(5) 7.2 vdc power supply. The 16 vac peak voltage across pins 7, 8 and 9 of transformer T2, center-tapped, is connected to terminals E1 E3 and E2 respectively (fig. 2-32) of power supply 5TR1PS1PS1 where it is rectified by CR1 and CR2; the dc voltage obtained is smoothed by C1 and fed through current limiting resistor R1 to one side of dual filter FL29 for further filtering. The 7.2 v at the output of FL29 is then fed through filters FL22 and FL23 and P1 pins 20 and 21 respectively as filament voltage to the driver tube of radio frequency amplifier 6AR1. Similarly, the 16 vac peak voltage across pins 10, 11 and 12 of transformer T2 is rectified by CR3 and CR4, smoothed by C2, current limited by R2, filtered by FL29 and fed through FL20 and FL21 and P1, pins 22 and 23, to the output tube of radio frequency amplifier 6AR1 as filament voltage.

(6) 28 vdc and 12 vdc regulator circuits (Fig. 2-33). The 30 v, 5 kHz square wave output across pins 15-17 (fig. 2-31) is rectified by CR16, smoothed by C19, filtered by L4 and C9 and applied simultaneously to the collectors of Q5 and Q6 (fig. 2-33). A reference voltage of 12.4 v is taken across Zeners CR7 and CR8 to the base of Q4. The reference voltage in the base circuit of Q4 is reflected in the Q2 emitter circuit by emitter-follower action to provide base-emitter temperature compensation for Q2. A sample of the 28 v output voltage, taken through voltage divider R9, R10, R11 is fed to the base of Q2 and provides the feedback voltage; Q2 and Q4 being in effect a differential dc amplifier circuit, the Q2 collector current is a function of the difference between the output voltage and the reference voltage. A decrease in the difference between the two voltages will cause a decrease in the Q2 collector current which in turn will cause an increase in the base current into Q6 and decrease the voltages across Q5 to maintain a constant output voltage. A 44 v, 5 kHz square wave output across pins 18, 19 and 20, is fed to rectifiers CR1 and CR2 (fig. 2-33). The 44 vdc obtained is filtered by C1 and R4, and clamped 6.2 v above the 28 v regulated output voltage by Zener diode CR4. This pre-regulator voltage is fed through R6 to the base of Q6, effectively adding a second feedback line in parallel with the amplified feedback to increase regulator efficiency. R1 and CR5 provide shortcircuit protection, a reduction in load resistance causing an increase in the current in the 28 vdc regulator and an increase in the voltage drop across resistor R1. If the load resistance decreases beyond a critical value, Zener

diode CR5 (3.9 v) will fire and drop the voltage at the base of Q6, holding Q6 and Q5 at a constant series current of about 2.2 amperes. Removing the short condition, the circuit reverts again to a constant voltage regulator. The operation of the 12

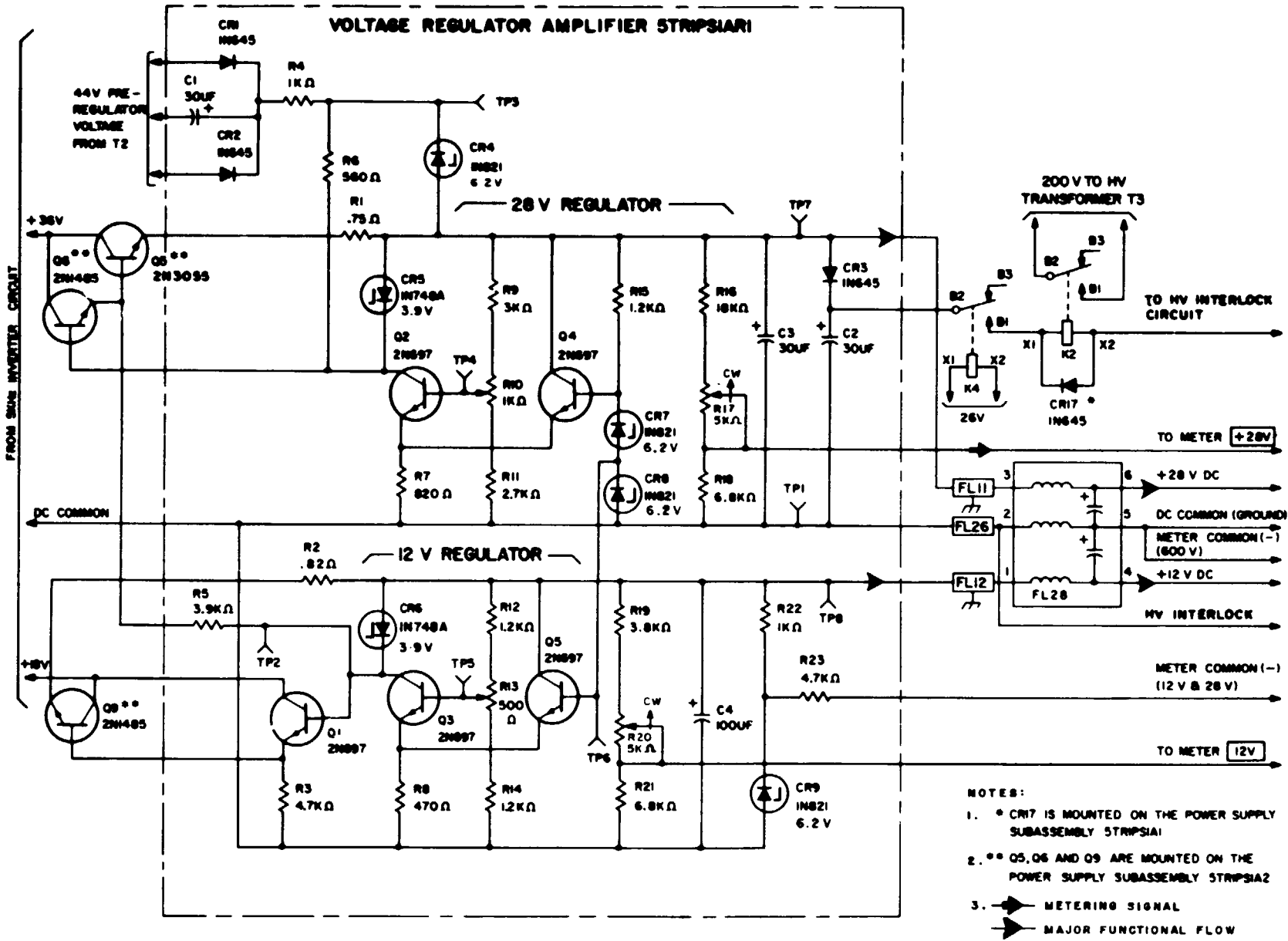


NOTE:

ITEMS MARKED WITH \* ARE MOUNTED ON POWER SUPPLY SUBASSEMBLY STRIPSIA2  
 ITEMS MARKED WITH \*\* ARE MOUNTED ON POWER SUPPLY SUBASSEMBLY STRIPSIA1  
 ALL OTHER ITEMS ARE PART OF THE MAIN CHASSIS ASSEMBLY STRIPS1.

EL5RE032

Figure 2-32. Power Supply, 7.2 Vdc Heater and Constant Current Supplies, Simplified Schematic Diagram.



EL5RE033

Figure 2-33. Power Supply, 12 Volt and 28 Volt Dc Supplies, Simplified Schematic Diagram.





(8) Constant current supplies (Fig. 2-32). Two constant current circuits regulate the cathode current of the driver amplifier tube at 60 ma maximum and that of the output tube at 160 ma maximum. 12 vdc regulated voltage from the 12 vdc regulator (J1 pin J) is fed into power supply subassembly 5TR1PS1A2 through E30 and applied simultaneously to the bases of two high voltage transistors, Q13 and 14, through R21 and R20. The 6.2 v Zener diode CR15 and the emitter resistance keep the base current to Q13 basically constant. The collector of Q13 is connected to the driver amplifier cathode through FL23 and P1-21; the emitter is returned to ground through R23, FL19, P1-24 and a variable resistor (R1) in the transmitter rf head (para 2-27). The value of R23 is chosen to provide the proper nominal value of cathode current; variable resistor R1 in the transmitter rf head is used for fine current adjustment. Similarly, 3.3 v Zener diode CR14 and the emitter resistance keep the base current of Q14 constant. The collector of Q14 is connected to the output amplifier cathode through FL21 and P1-23; the emitter is returned to ground through R19, FL18, P1-25 and variable resistor R2 in the transmitter rf head.

(9) Elapsed time indicator supply. The elapsed time indicator in the power supply is fed a constant current of about 6 microamperes derived from CR15 and R22. The voltage at Zener CR15 is also fed through FL27 and P1-28 to the elapsed time indicator in circuit card assembly 6AR1A2A2 in the transmitter rf head (para 2-27).

2-19. Transmitter Metering Circuits

a. General. The transmitter metering circuits include a 100 microampere meter which is connected into the various metering circuits by a 12 position rotary selector switch. The transmitter metering circuits indicate power and voltage levels throughout the transmitter fixed and rf heads. The meter has a 0 to 100 scale with a green band in the center. For any selector switch position marked with a green dot, a normal reading should fall within the green band. Each metering circuit has its own meter-matching circuit and a calibration resistor so that the one meter can serve to indicate various power and voltage ranges. The following chart lists the metering circuits of the transmitter and their normal indications.

| Switch position | Normal value   | Scale reading<br>(percent fullscale deflection) |
|-----------------|----------------|---|
| Osc             | 25 milliwatts  | 50  |
| DOUBLER         | 3 watts        | 50  |
| MULT            | 600 milliwatts | 30-40   |
| DRIVER          | 3 watts        | 20-60   |
| PWR OUT         | 25 watts       | 70  |
| REFL PWR        | Zero power     | Less than 20                                    |
| 12 CH PCM       | 180 kHz peak*  | 50  |
| 24 CH PCM       | 300 kHz peak*  | 50  |
| FDM             | 75 kHz peak*   | 50  |
| 12 v            | 12 vdc         | 50  |
| 28 V            | 28 vdc         | 50  |
| 600 V           | 630 vdc        | 50  |

\*Transmitter deviation

b. Metering Circuits Analysis (Fig. 2-35). For point-to-point tracing of metering circuits refer to F0-4-43.

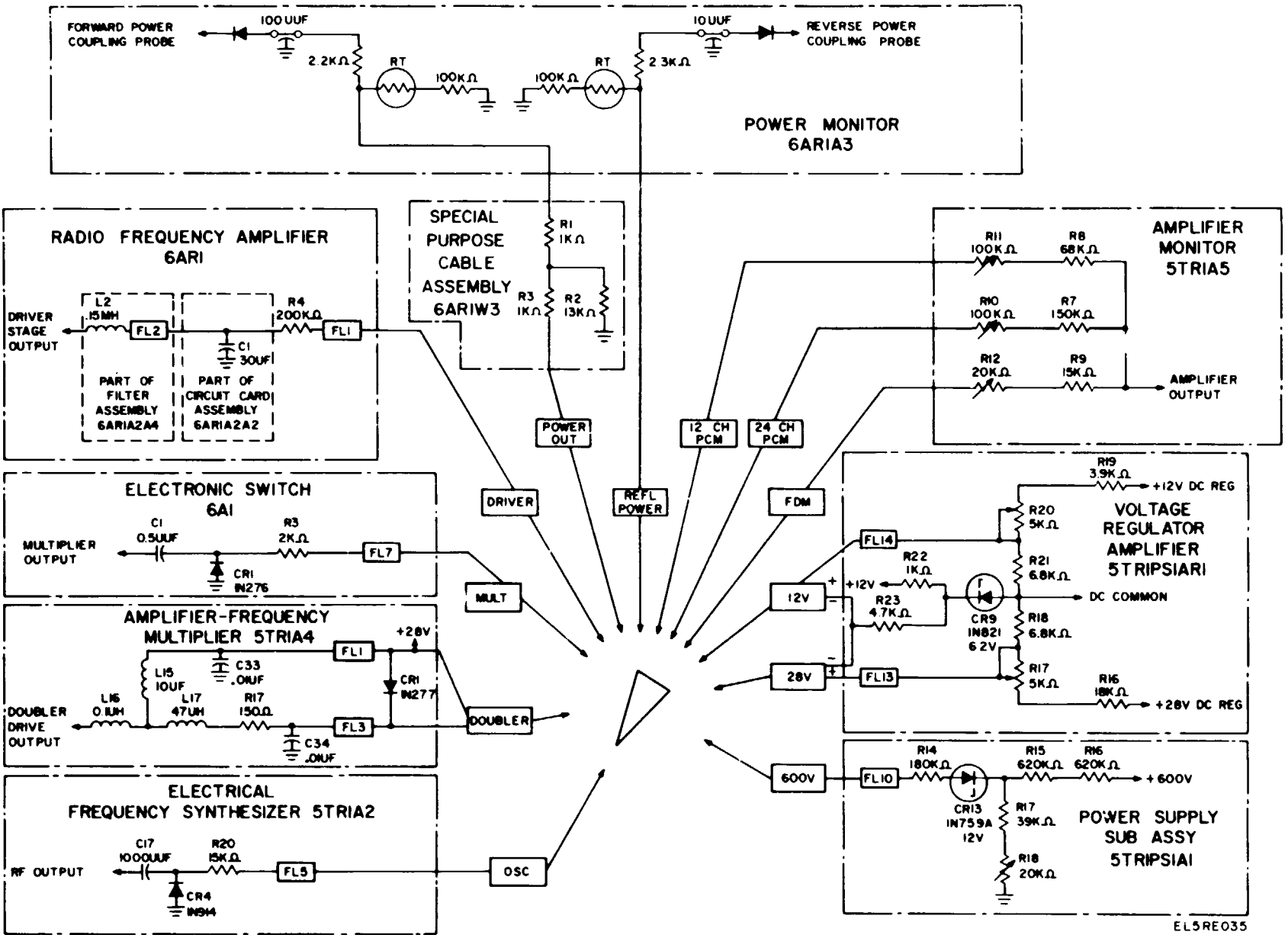
(1) OSC metering (position 1). The OSC meter position gives an indication of the electrical frequency synthesizer 5TR1A2 output signal as it is fed into amplifier-frequency multiplier 5TR1A4. A portion of the rf signal at the output of modulator-oscillator 5TR1A2A2 (para 2-4) is rectified by CR4 to produce a dc metering signal proportional to the rf signal. The dc signal then fed through R20 and FL1, through interconnecting box 5TR1A2A1 in the synthesizer, to monitor panel 5TR1A1 and meter selector switch S1-A (meter positive). The meter return is grounded at interconnecting box 5TR1A2A1. A 50 percent of full scale reading on the meter is equivalent to approximately 25 milliwatts rf output. 40 to 60 percent full scale deflection represents approximate synthesizer outputs from 15 to 40 milliwatts. In synthesizers equipped with modulator-oscillator 5TR1A2A2, Part No. CMC 220-800159-000, a portion of the rf signal at the output of the modulator-oscillator is rectified by CR6 to produce a dc metering signal proportional to the rf signal. The dc signal is then fed through R31 and FL5 to the meter selector switch and meter. Synthesizer outputs of 20 to 40 milliwatts (+12.5 to +15.5 dbm) will produce 20 to 80 percent full-scale deflection on the meter (fig. 2-36).

(2) DOUBLER metering (position 2). The DOUBLER metering signal is derived from the rf output of amplifier-frequency multiplier 5TR1A4 (para 2-16) which is used to drive frequency multiplier assembly 6A2. The signal is derived from the voltage drop across L15 in the Q3 collector circuit, R4, filtered by C35 and FL1, and fed through interconnecting box 5TR1A2A1 to panel monitor 5TR1A1 and meter selector switch S1-A (meter positive). The metering return line is fed through the interconnecting box to amplifier-frequency multiplier 5TR1A4 and is decoupled by C34, R17 and L17. The meter circuit has been calibrated to give a 50 percent of full scale reading for a nominal 3 watt output signal. 40 to 60 percent of full scale deflection represents approximately a 2 to 3.5 watt output signal.

(3) MULT metering (position 3). The MULT metering signal gives an indication of the multiplier drive signal (output of frequency multiplier assembly 6A2) fed into radio frequency amplifier 6AR1. A portion of the rf signal at the output of electronic switch 6A1 (para 2-24) is rectified by CR1 to produce a dc metering signal proportional to the rf signal. The dc voltage is fed through distribution box 5A2A1 to monitor panel 5TR1A1 and meter selector switch SA-1. Diode CR1 across the MULT metering circuit is used to limit the dc voltage fed into the meter. A 600 milliwatt output signal will provide 30 to 40 percent of full scale indication.

(4) DRIVER metering (position 4). The DRIVER meter position gives an indication of the rf output of the driver stage of radio frequency amplifier 6AR1, which is fed into the output stage (para 2-27). Variations in cathode voltage of the output tube, corresponding to changes in rf drive, are metered through resistor R4 of circuit card assembly 6AR1A2A2 and through the distribution box to monitor panel 5TR1A1 and meter selector switch. 3 to 8.5 volts on the output cathode provide a 20 to 60 percent of fullscale reading which corresponds to 2 to 3 watts drive.

(5) PWR OUT metering (position 5). The PWR OUT metering circuit measures forward (output) power at the output of the transmitter rf head (PWR OUT connector). A thermistor-controlled detector circuit in series with the forward power coupling probe produces a dc signal proportional to forward power going through power monitor 6AR1A3 (para 2-27). The dc signal is fed through the distribution box to the panel monitor and meter selector switch (meter positive). The meter common is returned to



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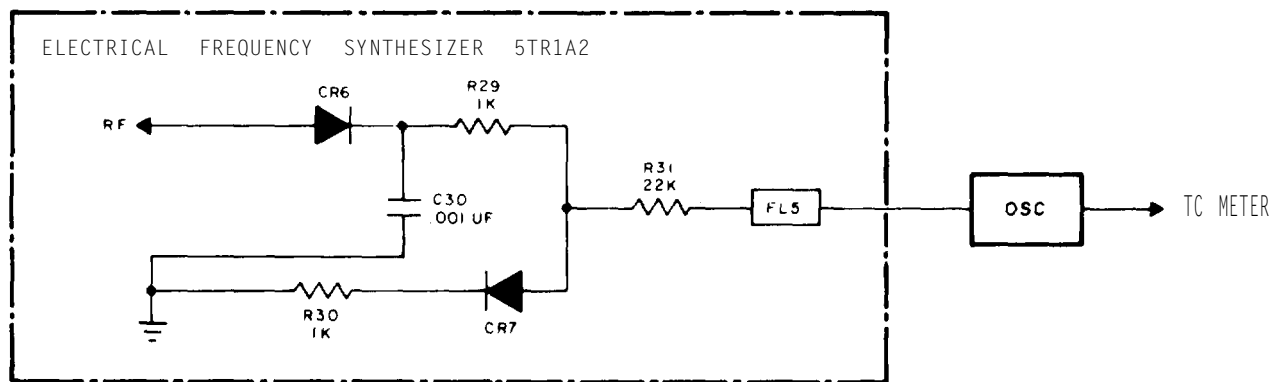
Figure 2-35. Transmitter Metering Circuits (Part No. CMC 456-260), Simplified Schematic Diagram.

ground at the transmitter rf head through the distribution box. A 5,000 ohm resistor, R3, in the monitor panel is connected across the PWR OUT metering signal when the meter selector switch is set to every position except position 5. This is done to make sure that the monitor signal, which is also used to operate alarm control 5TR1A3, is not disturbed when switching the meter selector to other positions. A 100 percent of full scale meter reading indicates a 40 watt output, while a nominal 25 watt output will produce a 70 percent meter indication.

(6) REFL POWER metering (position 6). The REFL POWER metering gives an indication of reverse power at the output of the transmitter rf head. The rf signal from the reverse power coupling probe is detected, producing a dc signal proportional to reflected power through power monitor 6AR1A3. A thermistor connected across the detector circuit provides a constant output independent of temperature. The resulting dc signal is fed through distribution box 5A2A1 into monitor panel 5TR1A1 and meter selector switch S1-A (meter positive). The negative side of the meter returns through S1-B and the distribution box to the meter common point in the transmitter rf head. Normal indication is almost zero power (less than 10 percent of full scale deflection) although as much as 4 watts (approximately 20 percent of full scale) is acceptable.

(7) 12 CH PCM, 24 CH PCM and FDM metering (positions 7, 8 and 9 respectively). These metering circuits are derived from the modulation signal (combined baseband and order wire) before it is fed to electrical frequency synthesizer 5TR1A2. A portion of the composite signal from video monitor 5TR1A5A1 (para 2-2) is amplified, then rectified to produce the dc voltage for metering functions. This dc voltage is fed through separate meter calibration circuits (R8 and R11; R7 and R10; R9 and R12) directly into monitor panel 5TR1A1 selector switch S1-A. The meter return circuit is brought back into amplifier-monitor 5TR1A5 and connected to ground through 220 ohm resistor R5. Meter calibrating potentiometers R11, R10 and R12 are adjusted to indicate 50 percent of full scale deflection for the following transmitter deviations:

R11 12 CH PCM 180 kHz peak-to-peak  
 R10 24 CH PCM 300 kHz peak-to-peak  
 R12 FDM 75 kHz peak-to-peak



EL5RE036

Figure 2-36. Transmitter Metering Circuit for Electrical Synthesizer 5TR1A2 Equipped with Modulator-Oscillator 5TR1A2A2, (Part No. CMC 220-800159-000) , Simplified Schematic Diagram.

(8) 12 v and 28 v metering (positions 10 and 11 respectively). The 12 v and 28 v metering voltages are derived from the corresponding outputs of voltage regulator amplifier AR1 of power supply 5TR1PS1 (para 2-18). Metering voltage for the 12 volt dc regulated supply is derived through the R19, R20 and R21 voltage divider; metering voltage for the 28 volts dc regulated supply is derived through the R16, R17 and R18 voltage divider, R20, METER CAL 12 V and R17, METER CAL 28 V, adjust the 12 volt dc and 28 volt dc voltage dividers respectively for a 50 percent of full scale meter indication. The meter is on an expanded scale; a 10 percent meter variation represents 200 millivolts change in the 12 volt dc supply voltage, and 300 millivolts change in the 28 volt dc supply voltage. Both metering voltages are returned to the same meter common point in voltage regulator amplifier 5TR1PS1AR1, which is clamped by 6.2 volt Zener diode CR9.

(9) 600 v metering (position 12). The 600 v metering circuit provides an indication for the 630 volt dc high-voltage supply to radio frequency amplifier 6AR1. The metering circuit is derived from the 630 volt dc line (para 2-18) through voltage divider R16, R15, R17 and R18. Voltage is adjusted by METER CAL control R20. CR13 and R14 expand the metering scale, so that zero deflection represents 200 volts and fullscale deflection represents 1,000 volts when metering the 630 v supply. The metering circuit is calibrated to indicate 50 percent of full scale deflection for 630 volts dc. The 630 volt metering circuit is fed through distribution box 5A2A1 wiring to monitor panel 5TR1A1 and selector switch S1-A. The metering return point is in power supply 5TR1PS1.

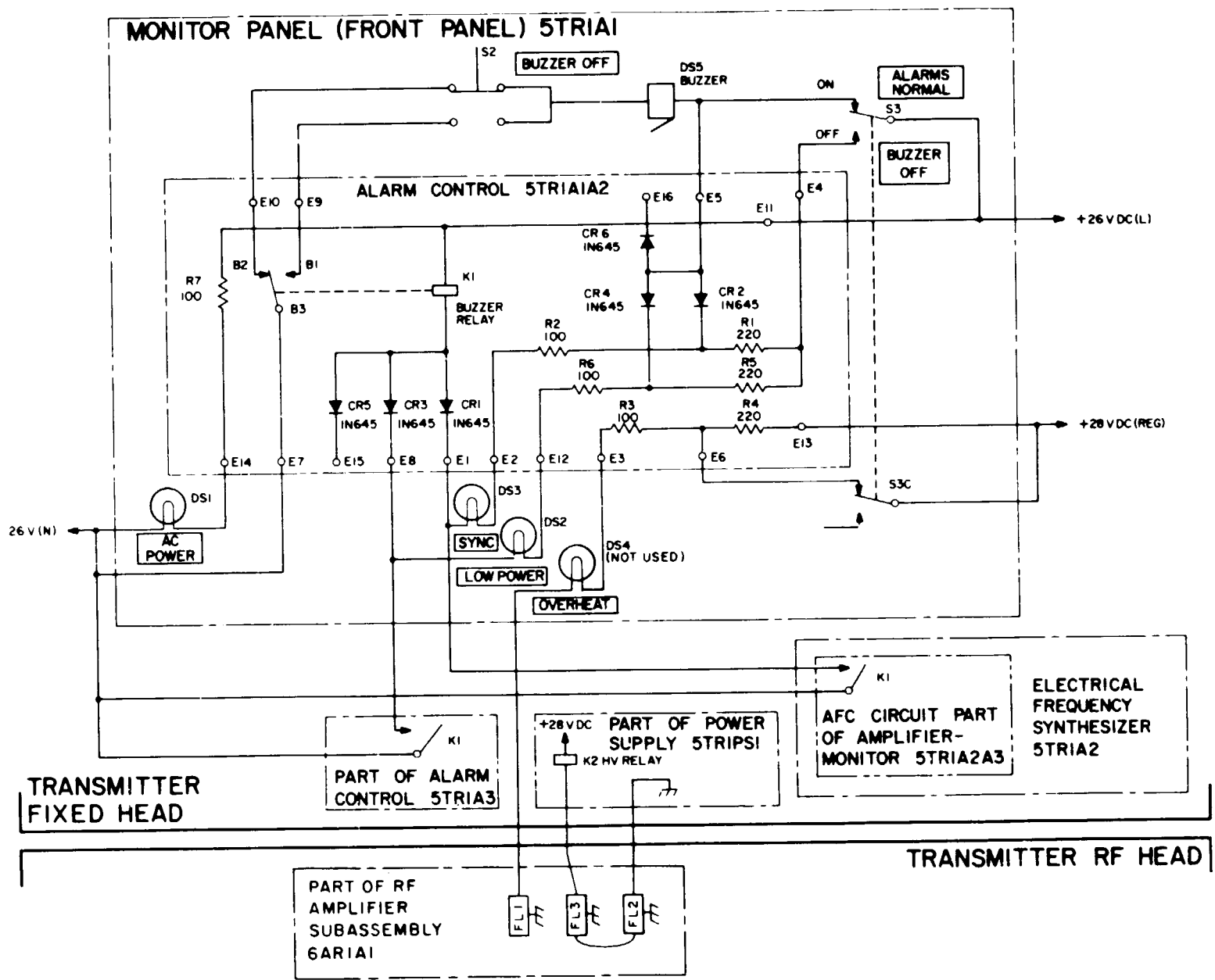
## 2-20. Transmitter Alarm Circuits

a. General. The transmitter alarm circuits are part of the monitor panel (front panel of the transmitter fixed head) and work in conjunction with alarm circuits in the transmitter fixed head (electrical frequency synthesizer 5TR1A2, power supply 5TR1PS1 and alarm control 5TR1A3) and the transmitter rf head (radio frequency amplifier 6AR1). Monitor panel 5TR1A1 includes an alarm control 5TR1A1A2, four indicator lights (AC POWER, SYNC, OVERHEAT, LOW POWER), one buzzer and three manually controlled switches (AC POWER: ON/RESET-OFF, BUZZER OFF and BUZZER OFF-ALARMS NORMAL). The buzzer sounds when a change of state occurs in the associated alarm circuits. A fault will cause the buzzer to sound. Pushing the BUZZER OFF switch silences the buzzer. Once all fault conditions are corrected the buzzer will sound again until the BUZZER OFF switch is operated again. A built-in switch (BUZZER OFF-ALARMS NORMAL) enables the buzzer to be muted and the lamps dimmed during testing, alignment and correction of fault conditions.

b. Indicator and Alarm Circuits Description (Fig. 2-37). For point-to-point tracing of indicator and alarm circuits refer to FO-4-43.

(1) Ac input circuit. When ac power is switched on, +26 volts dc from power supply 5TR1PS1 is fed through J3-4 into monitor panel 5TR1A1 and through E11 of alarm control 5TR1A1A2 to one side of buzzer control relay K1 and to the AC POWER indicator lamp DS1 (through R7 and E14). The 26 vdc is returned through J3-5 to the power supply. 26 volts dc is also applied through the BUZZER OFF-ALARMS NORMAL switch (in the ALARMS NORMAL position) to one side of the buzzer. The dc path through the buzzer is closed through contacts of buzzer control relay K1. At the same time, regulated +28 volts dc from the power supply is fed into the monitor panel through J3-1 and made available through E13 to alarm control 5TR1A1A2.

Figure 2-37. Transmitter Alarm Circuits, Case 5A2 (CY-4637/GRC-103 (V) ), Simplified Schematic Diagram.



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(2) SYNC (aft) alarm. The SYNC alarm circuit operates in conjunction with SYNC alarm relay K1 in amplifier-monitor 5TR1A2A3 (para 2-14) of electrical frequency synthesizer 5TR1A2. Normally the SYNC alarm relay is held operated by the afc SYNC alarm detector circuit and by the clock pulse D integrator. The SYNC alarm relay drops out when afc voltage is outside limits or when clock pulse D is absent. Operating range of the SYNC alarm relay (2.5 to 10 volts on the afc line) is established by Zener diode CR3 and potentiometer R3 and corresponds to the frequency control limits in the vco. When the afc voltage is outside these limits, the afc of the vco has been lost, and the SYNC alarm relay drops out. Normally, clock pulse D, fed into the integrator, holds control transistor Q4 operated and in turn relay control transistor Q5 at cut-off and the SYNC relay operating. In the absence of clock pulse D the relay drops out. When the relay is de-energized, the 26 volt dc path through SYNC indicator lamp DS3, buzzer control relay K1 and control diode CR1 in alarm control 5TR1A1A2 is closed. (The circuit passes through the monitor panel, through interconnecting box 5TR1A2A1 in the synthesizer to the amplifier-monitor board). The SYNC lamp illuminates and the buzzer sounds; the BUZZER OFF switch silences the buzzer while the alarm condition is being corrected. When normal operating conditions are restored, the SYNC alarm relay in the synthesizer is energized, and opens the 25 volt dc path. The SYNC indicator lamp is out, the buzzer relay drops out, but the buzzer sounds. Pushing the BUZZER OFF switch restores the buzzer circuits to normal.

(3) LOW POWER alarm. The LOW POWER alarm circuit operates in conduction with alarm control 5TR1A3 (para 2-17) and is an indication that transmitter power output is below the minimum set level. When the transmitter output is 8 db below the normal output level, the dc amplifier in alarm control 5TR1A3 is cut off, causing the LOW POWER alarm control relay to drop out and close the 26 volt dc path through LOW POWER indicator light DS2, buzzer control relay K1 and control diode CR3. The alarm circuit is connected directly to alarm control 5TR1A3. Operation of the LOW POWER alarm lamp and the buzzer circuit is the same as in the SYNC alarm circuit.

(4) OVERHEAT alarm. OVERHEAT alarm circuit operates in conjunction with pressure differential monitor 5A2A2 and is an indication of a failure in the air cooling system. If the centrifugal fan ceases to operate, or fails to move the required air volume, the difference of pressure between the ends of the sensor switch causes the switch contacts to open; this in turn causes the direct current amplifier to operate and provide a return path for the +28 vdc through DS4, and for the +26 vdc through the coil of buzzer control K1.

#### NOTE

Transmitters using case CY-4637A/GRC-103(V) (fig. 2-38) have the overheat alarm replaced by a temperature sensor located on the transmitter output tube and a control monitor temperature sensor assembly 5A2A2.

The control monitor temperature sensor consists of three printed wiring boards assembled in a metal housing with a top cover. The unit comprises a voltage regulator, fail-safe circuit, alarm, trip and motor speed control circuits.

The voltage regulator provides regulated outputs of 15 vdc and 6.2 vdc from the general purpose 26 vdc supply of the radio set.



The alarm, trip and fail-safe circuit generate the alarm and trips signals from the temperature sensor input and provides control information to the motor speed control. It contains a fail safe circuit to guard against short or open circuit of the temperature sensor.

The motor speed control provides a variable duty ratio 400 Hz bipolar signal to the blower motor for speed control.

(5) BUZZER OFF - ALARMS NORMAL switch. In the BUZZER OFF position, this switch removes the +26 volt dc supply from the buzzer circuit and connects 220 ohm dimming resistors R1, R4 and R5 in series with the SYNC, OVERHEAT and LOW POWER indicator lamps respectively.

2-21. Control Monitor, Temperature Sensor Assembly 5A2A2

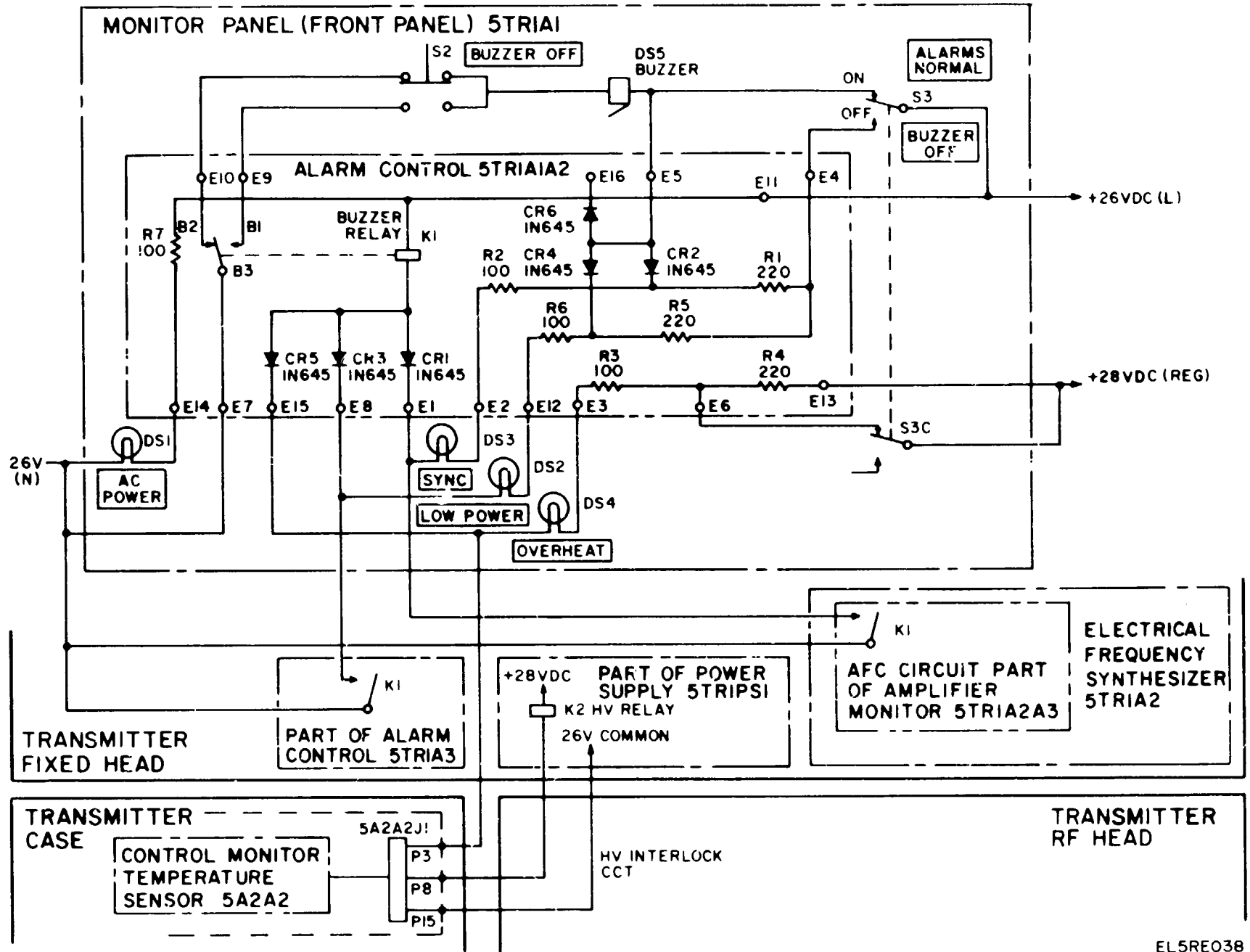
a. General. The control monitor, temperature sensor assembly 5A2A2 is located in the rf head compartment behind the blower. This unit receives its input from the temperature sensor located on the output tube of the power amplifier. From that sensor this unit provides an overheat alarm output, an overheat trip output and a variable power output of 400 Hz to drive the blower at variable speeds according to the transmitter cooling requirement. It also provides a fail safe feature to allow the blower to run full speed with a defective sensor circuit. The control monitor, temperature sensor replaces the differential pressure monitor 5A2A2 in older systems. It gives increased blower life and reduces noise and features a more reliable and positive alarm and an overheat trip function.

b. Circuit Description (F0-4-42 and Fig. 2-38). Regulated 6.2 v and 15 v output from the voltage regulator section of the driver control motor 5A2A2A2 is used to drive the sensor circuits A1 A2 and A3. A2B controls the overheat trip, A2A controls the overheat alarm and A1 controls the speed of blower motor A2B1. The overheat sensor across C2 of 5A2A2A1 provides a variable resistance as follows:

| Temperature | Sensor resistance |
|-------------|-------------------|
| +200°C      | 426 ohms          |
| +180°C      | 656 ohms          |
| +25°C       | 100,000 ohms      |
| -20°C       | 10.1 M ohms       |

The sensor has a negative temperature coefficient and is incorporated into a bridge arrangement which, according to the resistance of the sensor, gives the following conditions:

(1) At very cold temperatures (-20°C) the overheat alarm will operate initially but will extinguish after about two minutes as the system warms up. This is a result of the fail safe" alarm system which detects an apparent open circuit sensor (10 M ohms). As the tubes warm up this high resistance decreases and the alarm disappears. This effect is deliberate since the "fail-safe" alarm causes full power to be applied to the blower to force it to start at very low temperatures. The open



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Figure 2-38. Transmitter Alarm Circuits, Case 5A2 (CY-4637A/GRC-103(V)), Simplified Schematic Diagram.

circuit/high resistance condition across C2 turns off A3A, turns on A3C, A3B, Q3 and Q2 of 5A2A2A1 to operate the overheat alarm. The speed control voltage from A1 of 5A2A2A1 varies from a high state (blower low speed) to a low state (blower high speed) depending on the overheat sensor resistance across C2 of 5A2A2A1. The 400 Hz square wave from T1 of 5A2A2A3 thru Q1, provides a ramp waveform to A1A and A1B, (half cycle passing thru A1A and half cycle passing thru A1B). This ramp waveform is sliced at A1 according to the high or low condition from A1 of 5A2A2A1. This produces timing pulses with a variable delay controlled from the alarm and trip circuits of 5A2A2A1. The delayed pulses are used to trigger the two silicon controlled rectifiers Q1 and Q2 of 5A2A2A3 to give a variable duty square wave drive to the blower motor.

(2) As the system begins to heat up the resistance of the overheat sensor gradually decreases and causes a reduction of the blower speed by increasing the voltage from A1 of 5A2A2A1 to A1A and A1B of 5A2A2A2. At the same time, the lower resistance gives a low condition from A2A of 5A2A2A1 turning off Q2 and cutting off the overheat alarm.

(3) Should a fault condition exist causing the temperature of the tubes to continue to rise, the sensor resistance continues to decrease until at 180°C to 200°C the resistance of the sensor decreases to approximately 656 ohms. At this resistance A2A turns on Q2 and operates the overheat alarm. At the same time the voltage thru A1 to the speed control circuits for the blower drops causing a corresponding increase in the power to the blower motor, increasing blower speed.

(4) Should the temperature continue to climb over 200°C (sensor resistance lower than 426 ohms) the trip circuit A2B of 5A2A2A1 operates. Q1 turns on operating relay K1. Relay K1 cuts off the 26 v supply which in turn cuts off the 600 volt supply to the tubes. With no 600 volts applied to the tubes and the blower operating at full speed the system will cool down.

#### NOTE

With the 600 v cut off and the overheat alarm on and the blower running full speed the system will cool down. When the temperature drops below 190 C, 600 volts is automatically reapplied. The system will function normally but will flip from alarm to no-alarm condition as the system heats up and cools down. Corrective action should be taken immediately (see troubleshooting). Should the 600 v not reset when the set cools down, switch off the system and switch it on again. This will reset the overheat trip.

#### NOTE

The 600 volts applied via the sensor to the tube insures that if the sensor is not securely clipped to the tube, the system will not function.

Section II. AMPLIFIER-FREQUENCY MULTIPLIER AM-4320/GRC-103(V),  
AM-4320A/GRC-103(V) AND AM-4320B/GRC-103(V)

2-22. Functional Block Diagram Analysis of Amplifier-Frequency Multiplier AM-4320/  
GRC-103(V), AM-4320A/GRC-103(V), and AM-4320B/GRC-103(V) (Fig. 2-39 and 2-40)

This section refers to all three units unless otherwise specified. The rf output of amplifier-frequency multiplier 5TR1A4 is fed into Amplifier Frequency Multiplier AM-4320/GRC-103(V) (or Amplifier-Frequency Multiplier AM-4320A/GRC-103(V) or AM-4320B/GRC-103(V)) (transmitter rf head) where it is multiplied and amplified to produce the final transmitter frequency.

a. The transmitter rf head multiplication circuits provide the final multiplication required to produce the selected transmitter channel frequency. The multiplication circuits provide the final multiplication required to produce the selected transmitter channel frequency. The multiplication circuits are made up of electronic switch 6A1 and frequency multiplier assembly 6A2. The electronic switch is a double-pole, double-throw rf switch which routes the rf signal to and from the times-2 or times-3 circuits of the frequency multiplier assembly. Electronic switch 6A1 is programmed by control line 13 from control-indicator 6A3. Frequency multiplier assembly 6A2 contains two separate varactor multiplier circuits, one acting as a frequency doubler, the other as a frequency tripler. The output harmonic frequency of the frequency multiplier assembly is selected in a tuned circuit which is ganged to the front panel XMTR TUNE control. The output frequency in the range of 220 to 405 MHz is then fed back into the electronic switch, which routes the signal through rf power level control 6A5 and filter assembly 6AR1A2A4 to the first stage (driver) of radio frequency amplifier 6AR1 (when radio is equipped with Amplifier-Frequency Multiplier AM-4320A/GRC-103(V) or AM-4320B/GRC-103(V), the output signal from the electronic switch is fed directly to the first stage (driver) of radio frequency amplifier 6AR1).

b. The amplification of the output signal to the final output level is done in two-stage radio frequency amplifier 6AR1 (driver and output power amplifier), using two planar triodes type 7211 mounted within tuned quarter-wave resonant cavities. Tuning of the driver and output cavities is manually accomplished by the XMTR TUNE control on the transmitter rf head front panel; power peaking is accomplished by the PWR OUT PEAK control. Rf power level control 6A5 controls the rf power fed into the driver stage of the radio frequency amplifier to prevent the output stage from operating at an excessively high rf level.

c. Radio frequency amplifier 6AR1 amplifies the final frequency of the transmitter to a level of approximately 30 watts. After rejection of harmonics in low pass filter 6AR1A2FL1, the output signal is delivered through power monitor 6AR1A3 and the PWR OUT connector to Amplifier-Converter AM-4316/GRC-103(V) (Amplifier-Converter AM-4316A/GRC-103(V) when radio is equipped with Amplifier Frequency Multiplier AM-4320A/GRC-103(V) or AM-4320B/GRC-103(V)) (receiver rf head) and through a duplexer,

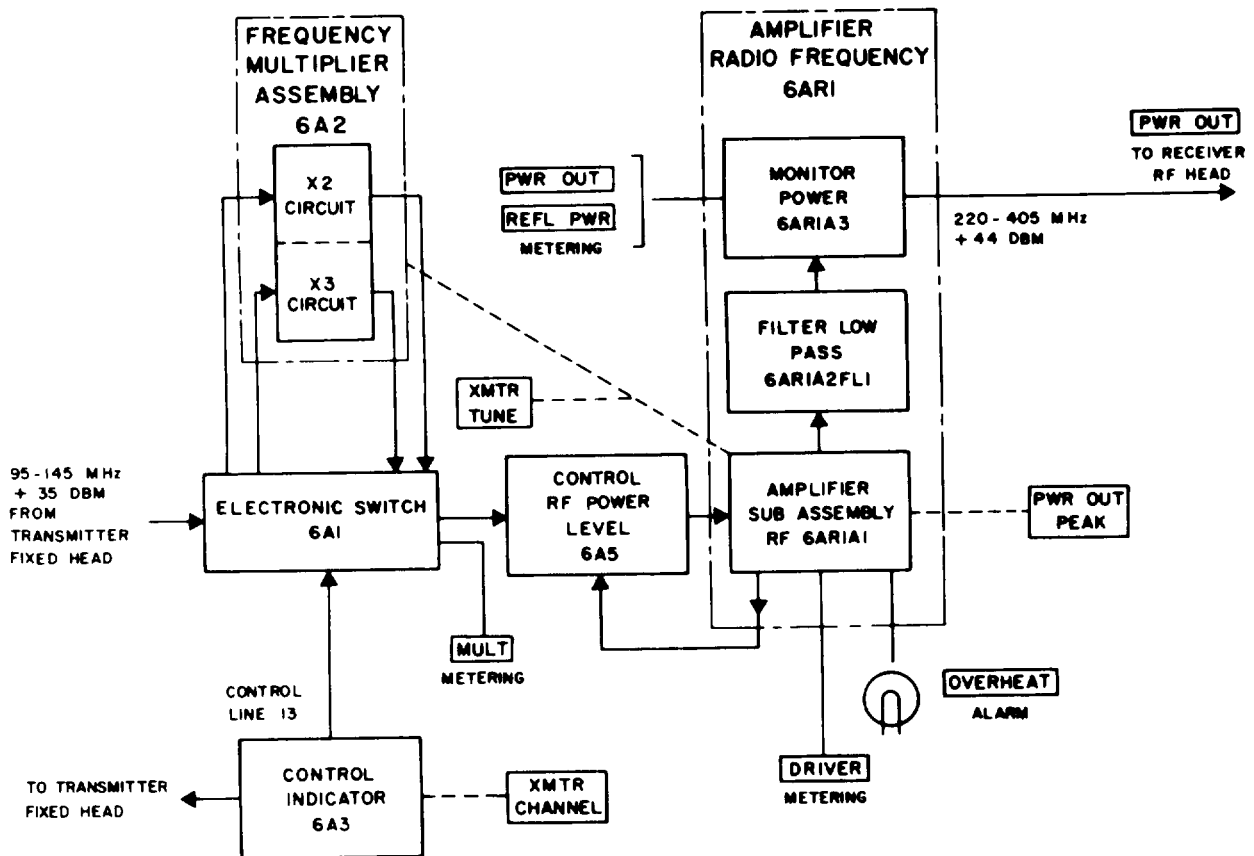
to the antenna system. A sample of the output power taken by power monitor 6A1A3 is rectified and supplied to alarm control 5TR1A3 which provides a warning when the rf signal power falls about 8 db below the nominal output level.

d. Control-indicator 6A3 (channel selector) is an electro-mechanical device operating in conjunction with electrical frequency synthesizer 5TR1A2 and amplifier-monitor 5TR1A5 in the transmitter fixed head, and with the frequency multiplication circuits in the transmitter rf head. The channel selector provides 13 control lines, but only 11 are used in this configuration, lines 1 and 2 being left open. Lines 3 to 13, inclusive, program the frequency synthesizer. Line 13 is also associated with the times-2 or times-3 multiplication factor changeover, thus controlling the variable attenuators in amplifier-monitor 5TR1A5 and the changeover switching in electronic switch 6A1. Channel selection is achieved manually by the XMTR CHANNEL control; a decade counter ganged to the XMTR CHANNEL control provides a visual indication of the selected channel.

e. An overall schematic diagram of the transmitter rf head is shown in F0-4-46.

2-23. Frequency Multiplication Circuits

a. General. The frequency multiplication circuits consist of electronic switch 6A1-and frequency multiplier assembly 6A2. They provide the final frequency multi-

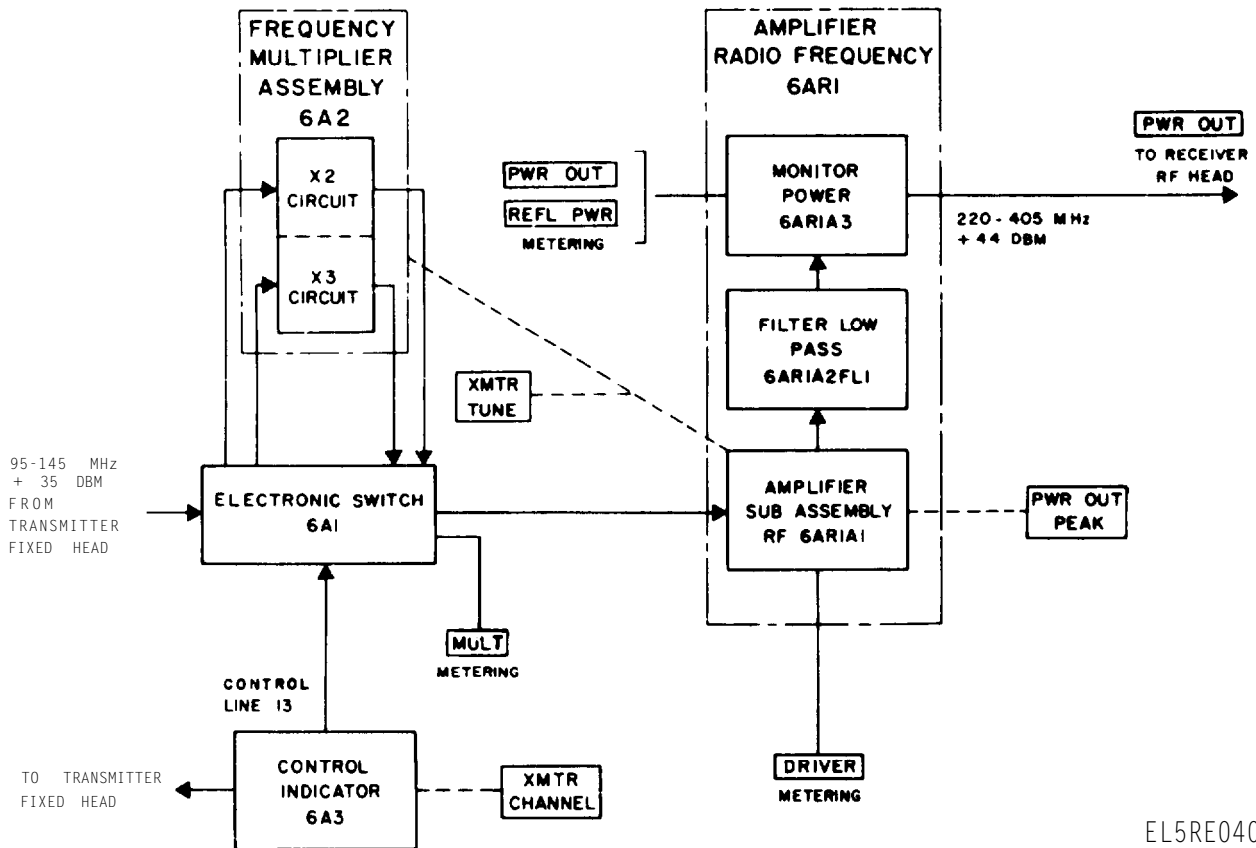


EL5RE039

Figure 2-39. Transmitter Rf Head (AM-4320/GRC-103(V), Block Diagram.

plication required to produce the selected transmitter channel frequency. Frequency multiplier assembly 6A2 contains two separate varactor multiplier circuits; a doubler and a tripler. Switchover from times-2 to times-3 multiplication is accomplished by electronic switch 6A1, which is a double-pole double-throw rf switch operated by changing bias voltages on PIN diodes.

b. Block Diagram Analysis (Fig. 2-39). The output of amplifier frequency multiplier TR1A4 in the range of 95 to 145 MHz at a level of +35 dbm±1 db (3 watts) is fed into the input connector of electronic switch 6A1. For a selected transmitter channel below channel 180 the rf signal is directed to the times-2 multiplier circuits of frequency multiplier assembly 6A2. The output of the times-2 multiplier is then fed through the electronic switch to rf power level control 6A5 (in transmitter equipped with Amplifier-Frequency Multiplier AM-4320/GRC-103(V) the output of the times-2 multiplied is fed through the electronic switch 6A1 to the filter assembly 6AR1A2A4). Similarly, when the selected channel is 180 and above, the rf signal is directed through the electronic switch to the times-3 multiplier circuits, back into the electronic switch to the times-3 multiplier circuits, back into the electronic switch and out to rf power level control 6A5 (out to filter assembly 6AR1A2A4, in transmitter equipped with Amplifier-Frequency Multiplier AM-4320A/GRC-103(V) or AM-4320B/GRC-103(V)). The rf signal after frequency multiplication is at the selected transmitter channel frequency in the range of 220 to 405 MHz at a level of +29 dbm (800 milliwatts) ±2 db.



EL5RE040

Figure 2-40. Transmitter Rf Head (AM-4320A/GRC-103(V) or AM-4320B/GRC-103(V), Block Diagram.

## 2-24. Electronic Switch 6A1

a. General. The electronic switch is a double-pole double-throw rf switch controlled by changing the biases on PIN diodes in the two rf paths. Line 13 of control-indicator 6A3 is grounded below channel 180, and has 26 volts dc on it at channel 180 and above. This ground on line 13 causes relay K1 of the electronic switch to energize and apply a forward bias on two PIN diodes in series with the times-2 multiplier circuits (input and output paths) and a reverse bias on the corresponding diodes in the times-3 multiplier circuits. When line 13 is carrying 26 volts dc the relay drops out, reversing the polarity of the bias on the PIN diodes.

b. Detailed Circuit Analysis (FO-4-45).

(1) Times-2 operation, channels 40 to 179 inclusive. Line 13 from control-indicator 6A3 arriving at 6A1P2 pin 6 is grounded at 6A3. 26 vdc is available at all times at 6A1P2 pin 7 and is applied through CR6 to the coil of relay K1, energizing it. 26 vdc at 6A1P2 pin 1 is applied through K1 contacts B1 and B2 to the cathode of PIN diode CR3 through FL4 and L3, and to the anode of PIN diode CR4 through FL3 and L2. CR3 is forward biased while CR4 is reverse biased. 26 vdc at 6A1P2 pin 3 is applied through K1 contacts A1 and A2 to the cathode of CR5 through FL6 and L4, and to the anode of CR2 through FL1 and L1. CR5 is reverse biased while CR2 is forward biased. Dc common for the two pairs of diodes is provided through R1, FL2, FL5 and R2. The incoming rf signal (110 to 144.75 MHz) at 6A1J5 is therefore routed through C3, CR2, C2 and 6A1J4 to 6A2P1, the input connector of the times-2 multiplier circuits. The output of the times-2 multiplier circuit (220 to 289.5 MHz) at 6A2P2 is then routed through 6A1J3, C5, CR3 and C6 to output connector 6A1J6.

(2) Times-3 operation, channels 180 to 410 inclusive. Control line 13 from the control-indicator carries 26 vdc and K1 relay is deenergized. 26 vdc at 6A1P2 pin 3 is applied through B3 and B2 to the cathode of CR3 (reverse bias) and to the anode of CR4 (forward bias). 26 vdc at 6A1P2 pin 1 is applied through K1 contacts A3 and A2 to the cathode of CR5 (forward biased) and to the anode of CR2 (reverse bias). The incoming rf signal at 6A1J5 is routed through C3, CR4, C4 and 6A1J2 to 6A2P3, the input connector of the times-3 multiplier circuits. The output of the times-3 multiplier circuit (290 to 405 MHz) at 6A2P4 is then routed through 6A1J1, C7, CR5 and C6 to output connector 6A1J6.

(3) Metering circuit. A portion of the rf output signal is rectified by CR1 and the resultant dc is fed through R3, FL7 and 6A1P2 pin 4 to the front panel meter (MULT) position) for metering.

## 2-25. Frequency Multiplier Assembly 6A2

a. General. Frequency multiplier assembly 6A2 contains two separate varactor multiplier, one operating as a frequency doubler and the other operating as a frequency tripler. The output harmonic frequency is selected in a tuned circuit which is ganged to the front panel XMTR TUNE control. The input frequency range of the doubler circuit is 110.0 MHz to 144.75 MHz, producing an output frequency range of 220 to 289.5 MHz (channel 40 to channel 179). The input frequency range of the tripler circuit is 96.666 to 135.0 MHz, producing an output frequency range of 290 to 405 MHz (channel 180 to channel 410). Both multiplier circuits have a series-tuned input circuit feeding the varactor. The varactor produces harmonics of its applied frequency, and feeds a series-tuned output circuit. The tripler circuit

uses a second-harmonic idler circuit to increase tripling efficiency. Both multipliers have broadband input and output impedance matching circuits.

b. Detailed Circuit Analysis (F0-4-45). For transmitter channels below 180 the incoming rf is applied to 6A12P1, the input to the doubler varactor circuit. L1, C1 and C3 form a series-tuned input circuit feeding the signal to varactor CR1. L3 provides broadband input match and R1 provides varactor self-bias. The second harmonic of the input signal is coupled through C3, C5 and L7 to output connector 6A2-P2. L5 provides broadband output match. C3 is tuned to the input and output frequencies by the XMTR TUNE control. For transmitter channels 180 and above the incoming rf signal is applied to 6A2P3, the input to the tripler varactor circuit. L2, C2 and C4 are the series-tuned circuit feeding the signal to varactor CR2. L4 provides broadband input match and R2 provides varactor selfbias. L6, C7 and C8 form an idler circuit tuned to the second harmonic of the input signal. This causes the second harmonic to flow in the varactor circuit where it mixes with the fundamental strengthening the third harmonic. C4, C6 and L9 form the series-tuned output circuit. C4 and C8 are ganged to the XMTR TUNE control. L8 provides broadband output impedance matching.

2-26. Rf Power Level Control 6A5

NOTE

This unit is not part of Amplifier-Frequency Multiplier AM-4320A/GRC-103 (V) or AM-4320B/GRC-103(V).

a. General. Rf power level control 6A5 limits the power level fed into radio frequency amplifier 6AR1. The level of the rf signal from electronic switch 6A1 is approximately +29 dbm±2 db. The tolerance on this level could produce a wide range of transmitter output power variations at the PWR OUT connector and excessive power could cause overdrive within radio frequency amplifier 6AR1, reducing tube life.

b. Detailed Circuit Analysis (Fig. 2-41). The incoming signal at 6A5P1 at a power level of +29 dbm±2 db (600 to 1400 mw approximately) is fed through a 3 db resistive attenuator, R1 and R2, to the controlling element, PIN diode CR1. C1 is a dc block to permit the application of dc bias to CR1. C2 is the dc block in the output path. The cathode voltage to the output tube is applied through 6A5P2 and 6A5FL1 to Zener diode CR2 (8.2 v). This voltage increases with the level of rf signal applied to the driver stage of 6AR1. When the cathode voltage exceeds 8.2 volts, zener diode CR2 will fire and apply a forward bias to PIN diode CR1. CR1 will then conduct part of the rf signal to ground. This action establishes a feedback control, attenuating the rf signal in the correct proportion to insure that the output stage of 6AR1 is not overdriven. The output rf signal level, controlled within the range of 200 to 300 mw, is fed through 6A5J2 to the driver stage of radio frequency amplifier 6AR1.

2-27. Radio Frequency Amplifier 6AR1

a. General. Physically, radio frequency amplifier 6AR1 makes up most of the transmitter rf head, and forms a framework on which the following subassemblies are mounted:

|                          |      |
|--------------------------|------|
| Rf amplifier subassembly | A1   |
| Circuit card assembly    | A2A2 |



|                           |       |
|---------------------------|-------|
| Filter assembly           | A2A4  |
| Radio interference filter | A2FL3 |
| Low pass filter           | A2FL1 |
| Power monitor             | A3    |

(1) Radio frequency amplifier 6AR1 amplifies the final selected transmitter frequency by about 23 db in two power amplifier stages using type 7211 lighthouse tubes mounted in tunable resonant cavities. The cavity design uses a quarter-wave folded resonator in the plate circuit (fig. 2-42). The grid-cathode resonator is of conventional form (nonfolded) with capacity loading at its end. The heater connection to the amplifier tube is made through the hollow lead screw inside the center conductor of the cathode resonator. The lead screw is of double-start nature to enable rapid transit of the tuning plungers. Due to the folded design, the plate tuning assembly is moved toward the gear face to tune to higher frequencies, whereas the cathode assembly moves in the opposite direction. Cathode feed is taken in through a connection which is adjacent to the gear plate. This is then passed through a small coaxial cable, firmly bonded to the inside of the grid-cathode resonator cavity and fed through the cathode contact assembly to the cathode. Dc isolation is achieved within the cathode contact assembly. The plate supply is decoupled by a capacitor integral to the amplifier tube socket; the capacitor is a silvered mica disc in a potted assembly.

(2) Tuning the cathode and plate resonator cavities is accomplished by adjusting mechanically coupled plungers, ganged to the XMTR TUNE control. This control is also ganged to the variable tuned circuits in frequency multiplier assembly 6A2. Cavity output coupling is by capacitive probe; peaking is accomplished by adjusting the PWR OUT PEAK control on the front panel. (This control is pushed in to engage the driver probe drive gears and pulled out to engage the output probe drive gears.

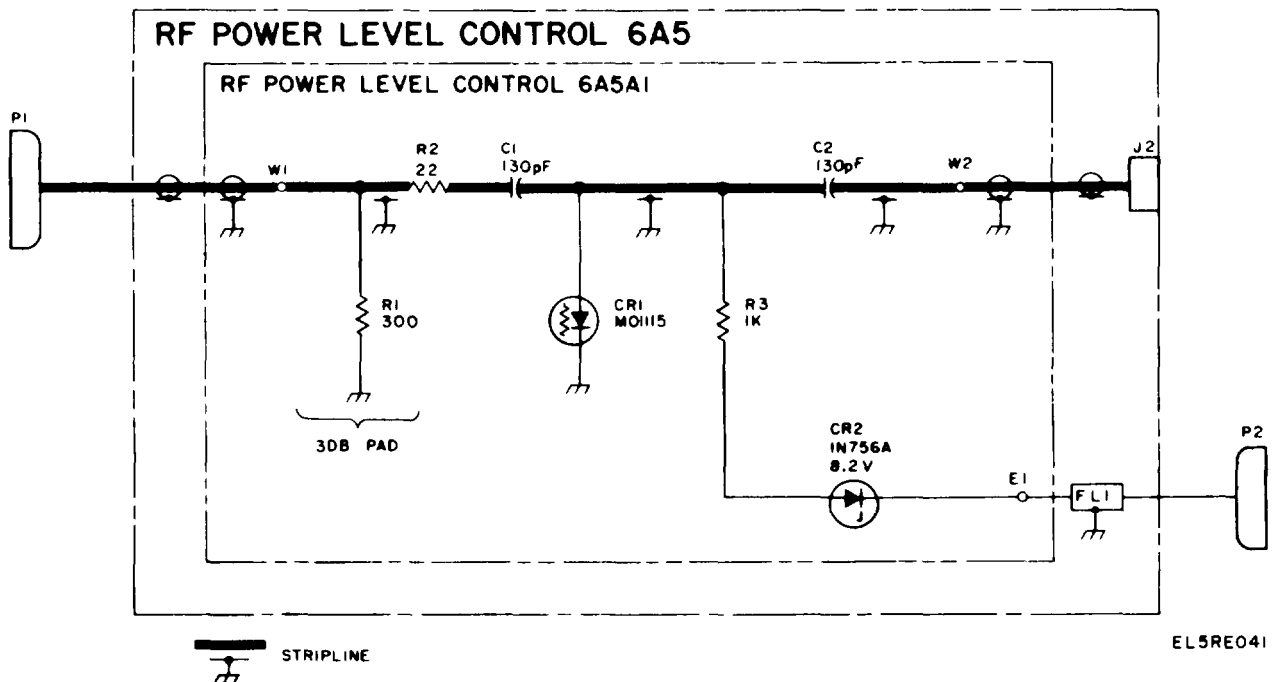
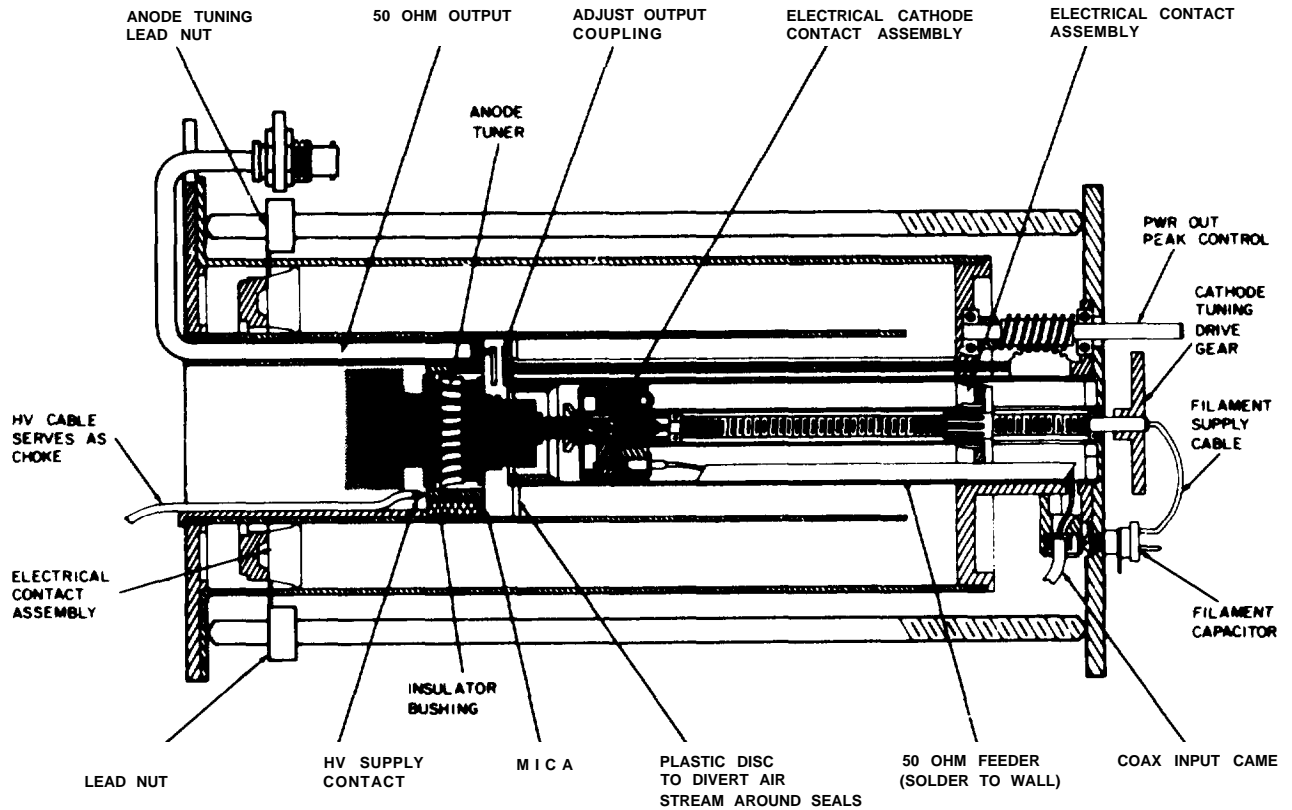


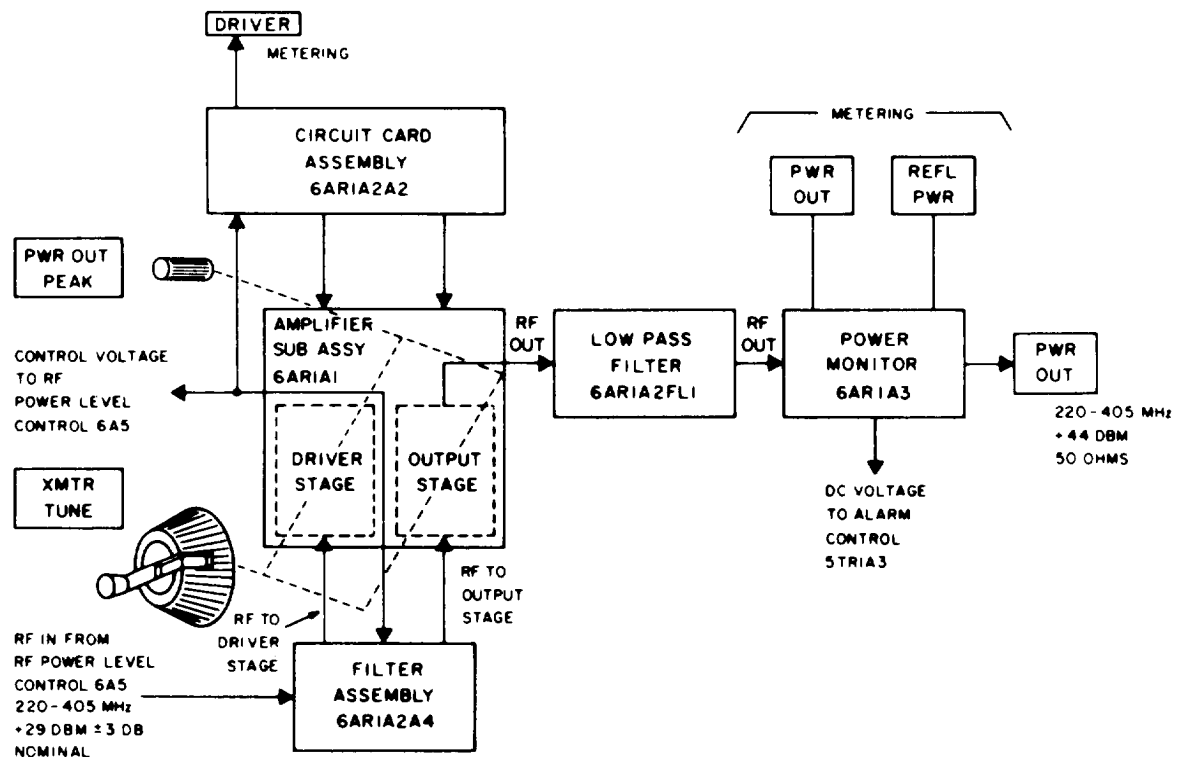
Figure 2-41. Rf Power Level Control 6A5, Schematic Diagram.



EL5RE042

Figure 2-42. Radio Frequency Amplifier 6AR1 Resonator Cavity, Cross-Sectional View.

b. Block Diagram Analysis (Fig. 2-43). The rf signal from rf power level control 6A5 (when unit is equipped with Amplifier-Frequency Multiplier AM-4320/GRC-103(V)) or from electronic switch 6A1 (when unit is equipped with Amplifier-Frequency Multiplier AM-4320A/GRC-103(V) or AM-4320B/GRC-103(V)) is fed through the driver section of filter assembly 6AR1A2A4 into the cathode of driver tube V2. The filter assembly is used to prevent rf feedback to the power supply on the cathode dc line; it also provides impedance matching of the rf input line which would otherwise be mismatched by connecting the line to a dc point. V2 amplifies the rf signal by 13 db (to about 4 watts). The output of the driver tube is fed through the output section of filter assembly 6AR1A2A4 to the cathode of output tube V1, where the signal is amplified by a further 10 db. Filament and cathode supplies to the power amplifier tubes are also fed through filter assembly 6AR1A2A4. Filament voltages and cathode circuits for the two amplifier tubes are applied through adjustment and monitoring circuits in circuit card assembly 6AR1A2A2. Test points and potentiometers permit adjustment of circuits, and this assembly also contains a facility for monitoring the driver tube power. The rf signal from output stage V2 is fed into low pass filter 6AR1A2-FL1 which attenuates all harmonics of the fundamental. The filtered rf signal is then fed through power monitor 6AR1A3 and the PWR OUT connector to the duplexer in the receiver rf head and on to the antenna. Power monitor 6AR1A3, a hi-directional coupler with rf pick-up loops, provides dc metering signal for forward and reflected transmitter power. Part of the forward power metering signal is also fed to alarm control 5TR1A3 (para 2-20) for LOW POWER alarm indication.



EL5RE043

Figure 2-43. Radio Frequency Amplifier 6AR1, Block Diagram.

### C. Detailed Circuit Analysis.

(1) Filter assembly 6AR1A2A4 (Fig. 2-44). The filter assembly has two sections, one section providing impedance matching and rf decoupling on the driver tube cathode connection, and one providing impedance matching and rf decoupling on the output tube cathode connection. Variable capacitors C1 and C2 are adjusted for the best broadband impedance match and coils L1 and L2 provide rf isolation. Heater and cathode supplies are connected to the driver and output tubes through FL1 and L1, and FL2 and L2 as shown.

(2) Rf amplifier subassembly 6AR1A1 (Fig. 2-45). The driver amplifier and the output amplifier are mechanically and electrically identical, the only difference being in the choice of the dc operating point, which is externally adjustable. The plate resonators share a common drive screw. The output matching conditions, however, are different and individual drivers are required for the output probes. The power amplifier is a conventional tuned-cathode, tuned-plate grounded-grid triode amplifier circuit. V2 is the driver stage amplifier, Z3 the cathode resonator and Z4 is the plate resonator. C7 and C8 are dc bypass capacitors. C10 is a cathode rf bypass capacitor, and C16 is a smoothing capacitor. The input signal is fed to the cathode from filter assembly 6AR1A2A4 at a level of 200 milliwatts to excite cathode resonator Z3, connected between cathode and grid. The signal at the plate resonates in Z4, connected between the plate and grid, and is coupled from the cavity to output jack J1 through output coupling probe C12. Driver peaking is accomplished by adjustment of the PWR OUT PEAK control in the pushed-in position. The output from the driver tube is connected through the second section of filter assembly 6AR1A2A4

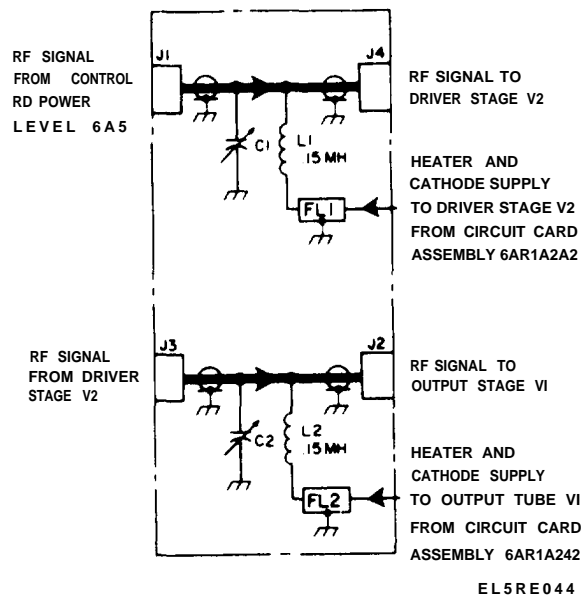


Figure 2-44. Filter Assembly 6AR1A2A4, Schematic Diagram.

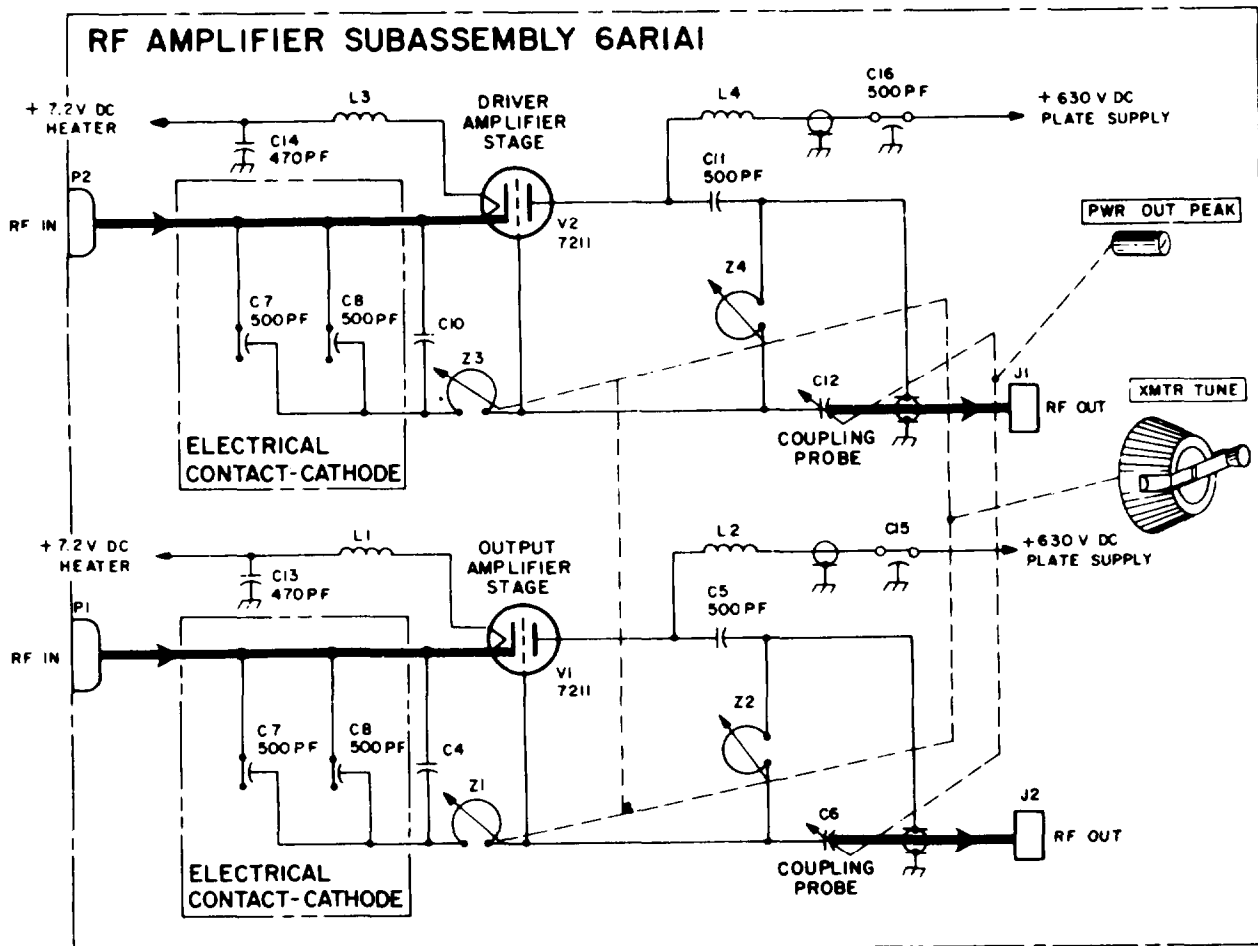
to the cathode of output tube V1, in a circuit similar to the V2 circuit. Here it is amplified, then coupled out of the plate cavity by output coupling probe C6. Output peaking is accomplished by adjustment of the PWR OUT PEAK control in the pulled out position. Tube filament voltages (fig. 2-46 and fig. 2-47) are set to 7.2 volts dc to provide filament current of about 1.3 amperes. Cathode currents are regulated by a constant current source within transmitter power supply 5TR1PS1 (para 2-18) to 60 milliamperes into the driver cathode and 160 milliamperes into the output cathode. The currents are set by adjustments on circuit card assembly 6AR1A2A2. Regulating the cathode currents in this manner extends tube life well in excess of 5,000 hours. Plate supply for the two tubes is 630 volts dc at about 180 milliamperes, supplied through radio interference filter 6AR1A2FL3, and applied to the plates through chokes L2 and L4 formed by wiring inside the cavities. A cross-section of the cavities is shown in figure 2-42.

(3) Circuit card assembly 6AR1A2A2 (Fig. 2-48). This assembly contains several test points and an elapsed time indicator. Four adjustable resistors mounted on a nearby bracket are used in conjunction with the test points in the circuit card assembly and a multimeter to adjust the filament voltages and cathode currents of the power amplifier tubes. A metering circuit (DRIVER position) detects the presence of drive into the output stage. This circuit is connected through E9, R4 and L4 into the cathode circuit of the output amplifier tube. Part of this voltage is also fed to rf power level control 6A5 for limiting the amount of drive (para 2-26). Two test points, TP3 and TP2, are provided in the heater circuit of the driver and output amplifier respectively. External'y mounted resistors, R3 and C4, in the heater line accommodate variations of tube filament circuits and are used to adjust the heater voltages. TP6 and TP7 are test points in the cathode current circuits of the driver and output amplifier respectively; the two constant current networks located in transmitter power supply 5TR1PS1 (para 2-18) are connected to the respective power amplifier tubes through variable resistors R1 and R2 and terminals E3 and E8 respectively. An elapsed time indicator on this board indicates tube running

time. This device contains a thin column of mercury with a small quantity of electrolyte within the column. A constant current will cause the mercury to travel through the electrolyte, causing the electrolyte to move along the column at a constant rate. The device is graduated in 1000 hours increments-and can indicate up to 10,000 hours running time.

(4) Low pass filter 6AR1A2FL1. Since the two cavities in which the tubes are mounted are one-quarter wave resonators they will pass the fundamental and all odd order harmonics. Low pass filter 6AR1A2FL1 is a sealed unit having a very sharp cut off and providing at least 45 db attenuation at 600 MHz (3 x 220 MHz). Passband insertion loss is approximately 5 db.

(5) Power monitor 6AR1A3. This unit has a coaxial line containing two inductive rf pickup loops, one to pick up forward power and one to pick up reflected

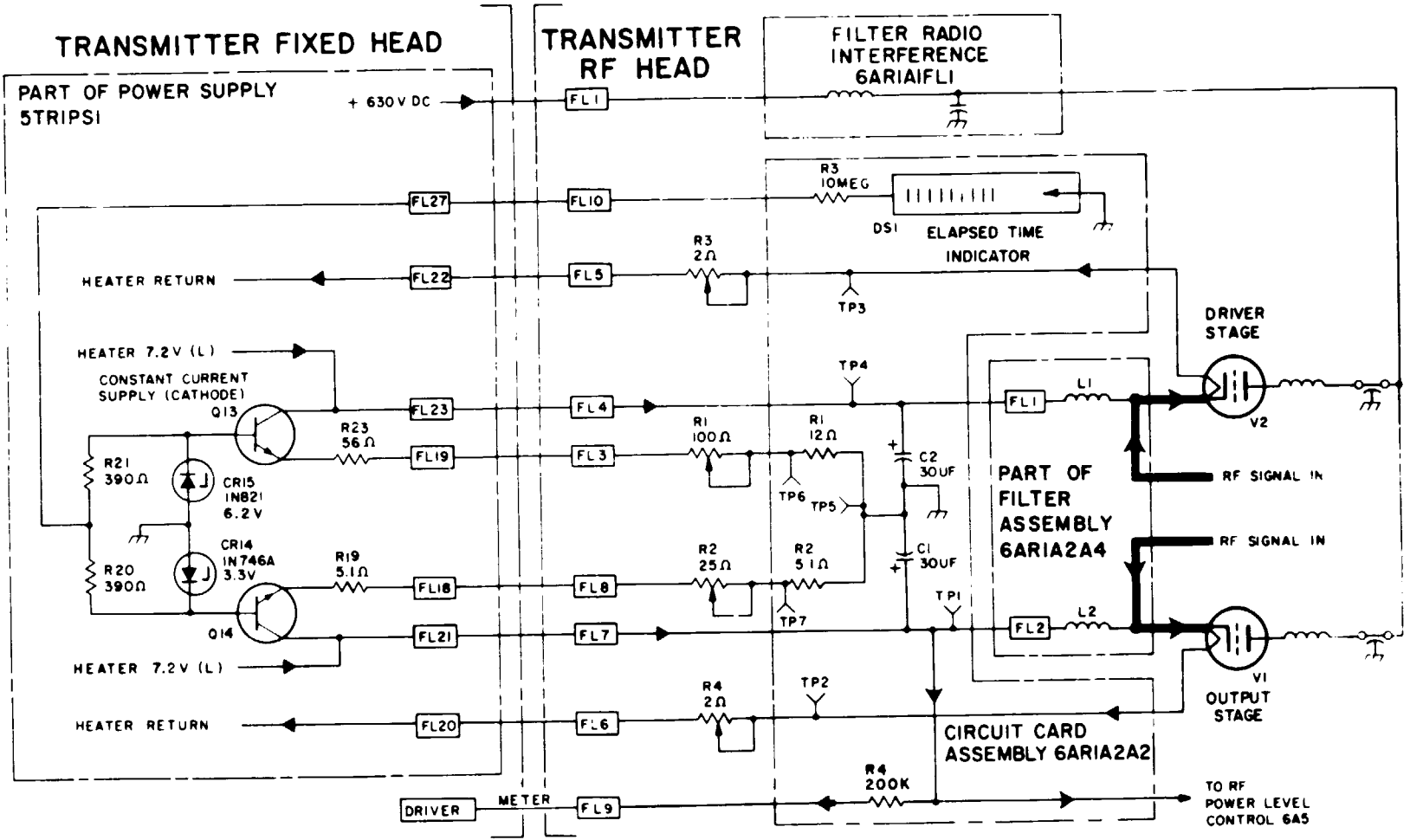


NOTES

- L1, L2, L3, L4 ARE WIRING INDUCTANCE
- C4 a C10 ARE MICA DISCS IN CATHODE CAVITIES
- C5 a C11 ARE MICA DISCS IN PLATE CAVITIES
- Z1 a Z3 ARE INNER CAVITIES
- Z2 a Z4 ARE OUTER CAVITIES

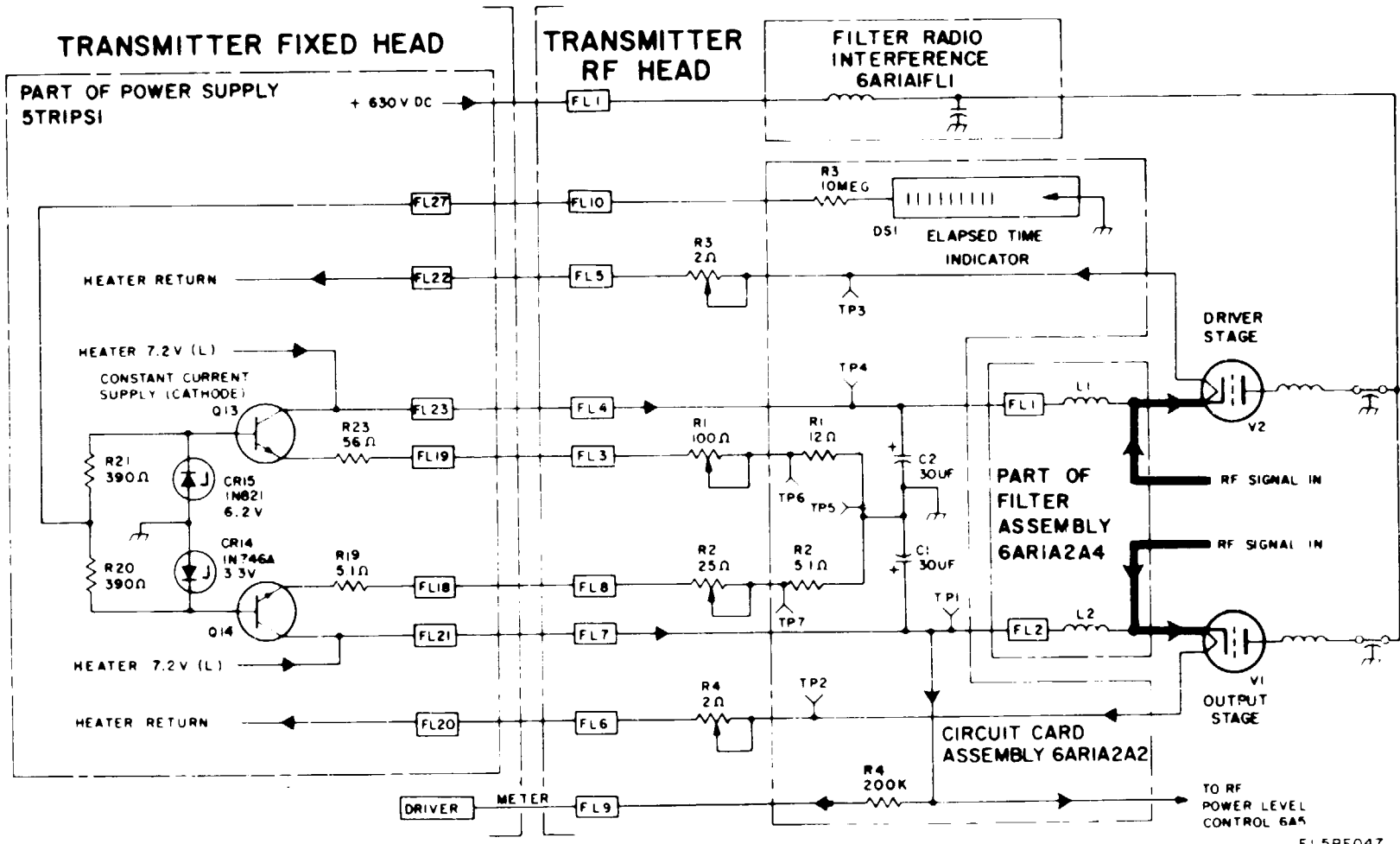
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Figure 2-45. Rf Amplifier Subassembly 6AR1A1, Schematic Diagram.



EL5RE046

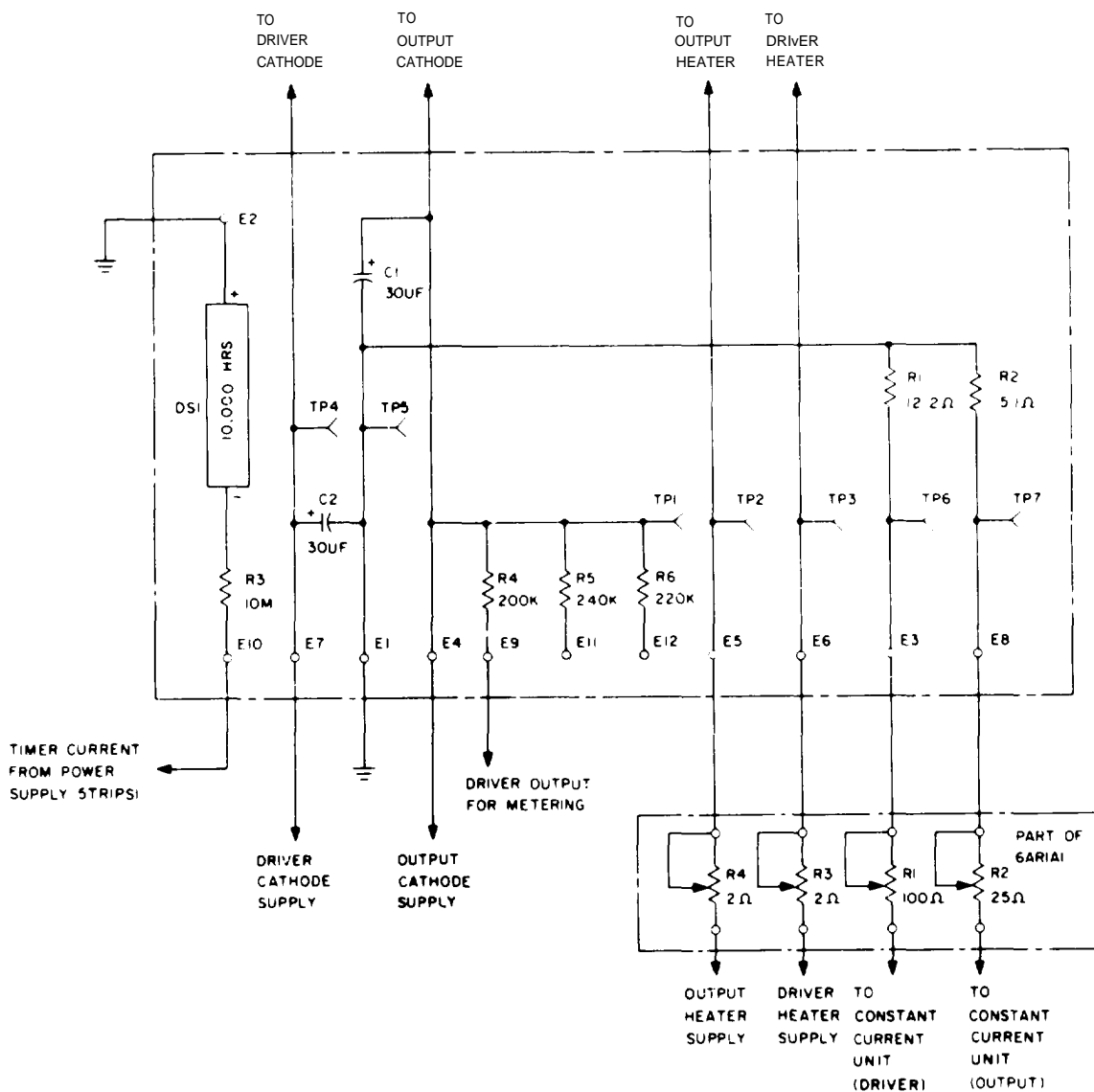
Figure 2-46. Power Amplifier Tubes and Rf Supplies, (AM-4320/GRC-103(V)), Simplified Schematic Diagram.



EL5RE047

Figure 2-47. Power Amplifier Tubes and RF Supplies (AM-4320A/GRC-103(V) or AM-4320B/GRC-103(V)), Simplified Schematic Diagram.

power. Both rf signals are rectified to produce dc metering signals, and thermistors are used to compensate the temperature characteristics of the rectifying diodes. The forward metering signal is fed to the meter through the selector switch in the PWR OUT position. It is also fed in parallel to the input of alarm control 5TR1A3 (para 2-20). The control alarm will initiate a LOW POWER alarm if transmitter output power should drop by 8 db to about 4 watts. A 5,000 ohm resistor is switched into the circuit when the meter selector switch is in any other position, in order that the monitor signal will not be disturbed by switching the meter to the PWR OUT position. The reverse power metering signal is fed to the meter through the selector switch in the REFL PWR position. This metering function is used primarily to assist the operator while tuning the XMTR DUPL control on the receiver rf head. Minimum meter reading indicates correct tuning of the transmitter portion of the duplexer in the receiver rf head.



EL5RE048

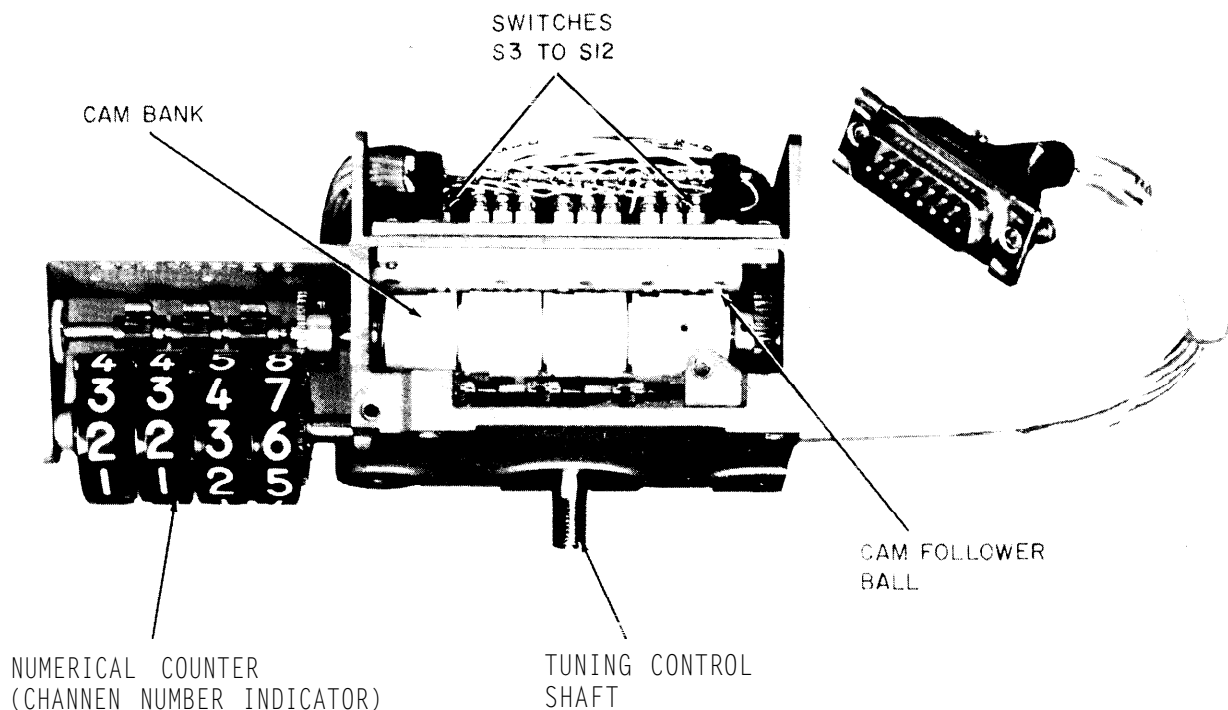
Figure 2-48. Circuit Card Assembly 6AR1A2A2 Schematic Diagram.



## 2-28. Control-Indicator 6A3 or 2A2

a. General. Control-indicators 6A3 (transmitter channel selector) and A2 (receiver channel selector) are identical in function and construction (fig. 2-49). Each channel selector provides 11 control lines (3 through 13) to synthesizer 5TR1A2 or 1RE1A2. To select the required synthesizer frequencies, control lines 3 through 12 are switched on and off in a binary pattern, with line 13 switched between channel 179 and 180 to change the synthesizer output frequency steps. The switching modules are operated by a set of cams and followers which reflect the various coding patterns as shown in the coding tables (FO-4-33). Each selection is presented on the front panel display (XMTR CHANNEL or RCVR CHANNEL by means of a numerical counter). In the transmitter, control line 13, in addition to changing the synthesizer output frequency steps, is also used to switch in the 3.5 db attenuator within amplifier-monitor 5TR1A5 (para 2-2) and to change the frequency multiplication factor from times-2 to times-3 (para 2-23).

b. Description of Operation. The channel selector consists of a bank of 10 cam-operated microswitches, a front panel channel indicator and a multiplier changeover decoder circuit. The 10 microswitches are operated by cams which establish a binary code to preset the required stages of programmed counter in synthesizer 5TR1A2 or 1RE1A2. The front panel channel indicators consist of a series of geneva-operated wheels, each having a series of numbers painted on it. The indicating wheels are geared to the microswitch cams and to a front panel knob. The transmitter channel



EL5RE049

Figure 2-49. Control-Indicator 6A3 or 2A2, Cover Removed.

selector display indicates the channel rather than the frequency selected. The following formulas should be used to translate a selected channel into a frequency and vice versa.

$$(1) \text{ Transmitter frequency} = \frac{\text{Transmitter channel} + 200}{2} \text{ MHz}$$

$$(2) \text{ Transmitter channel} = (\text{Transmitter frequency (MHz)} - 200) \times 2$$

On the receiver channel selector the coding is arranged to produce a local oscillator frequency 30 MHz higher than the channel indicated in the display. This is done to permit the indicator to refer to the received signal frequency, the actual local oscillator frequency being always 30 MHz higher to provide the correct intermediate frequency. The decoder unit is an encapsulated logic circuit designed to sense channel coding on 8 of the 10 microswitch output lines and initiate control line 13 switching to establish multiplication changeover, which takes place between channels 179 and 180 in the transmitter and channels 119 and 120 in the receiver.

### Section III. AMPLIFIER-CONVERTER AM-4316/GRC-103(V) AND AM-4316A/GRC-103 (V)

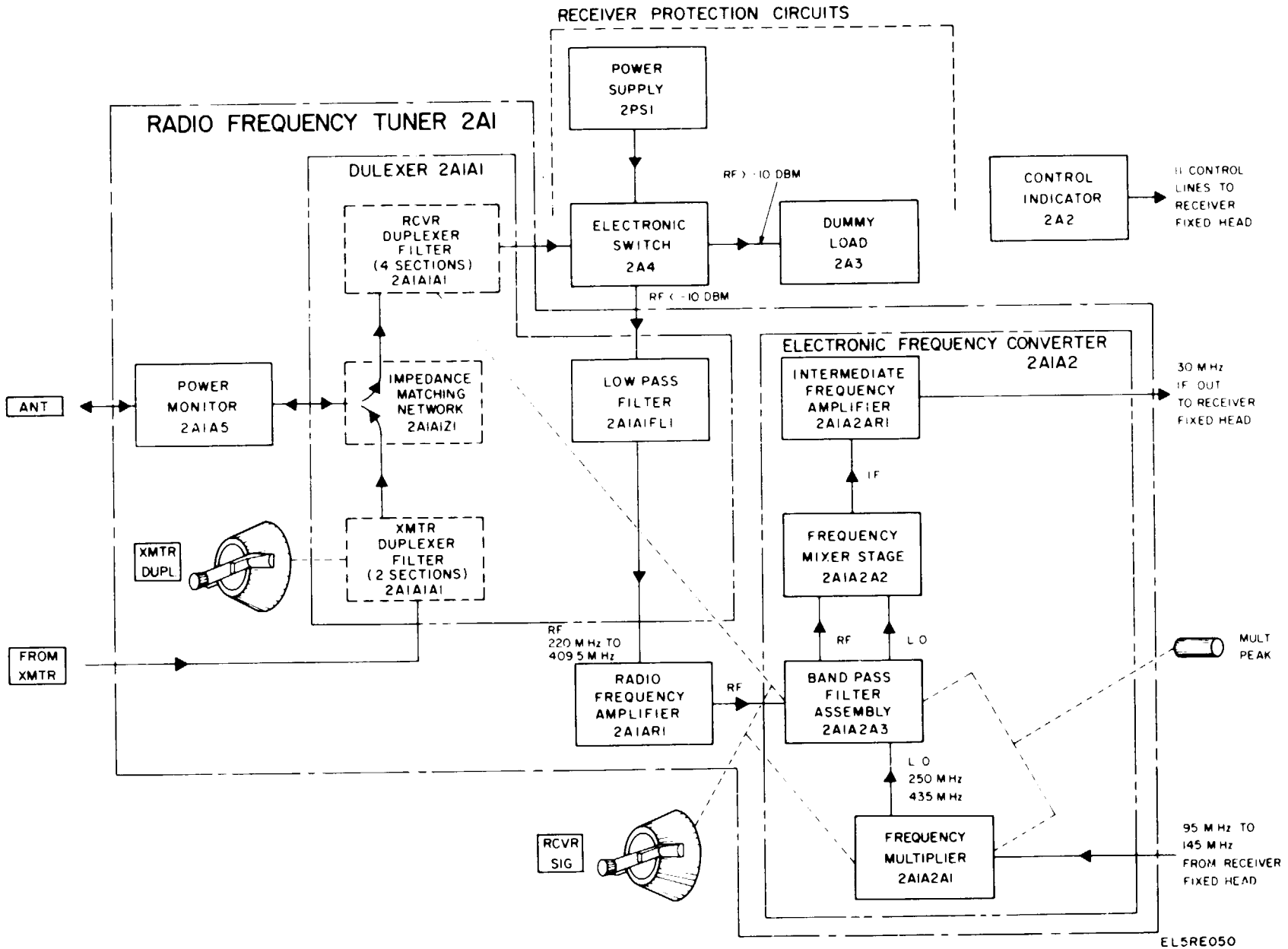
#### 2-29. Functional Block Diagram Analysis of Amplifier-Converters AM-4316/GRC-103(V) and AM-4316A/GRC-103(V) (Figs. 2-50 and 2-51)

a. Amplifier-Converter AM-4316/GRC-103(V) and Amplifier-Converter AM-4316A/GRC-103TV) (receiver rf head), incorporates a duplexing system which enables the radio set to use a single antenna for both transmit and receive functions, and circuits which convert the incoming receive signals into a 30 MHz intermediate frequency.

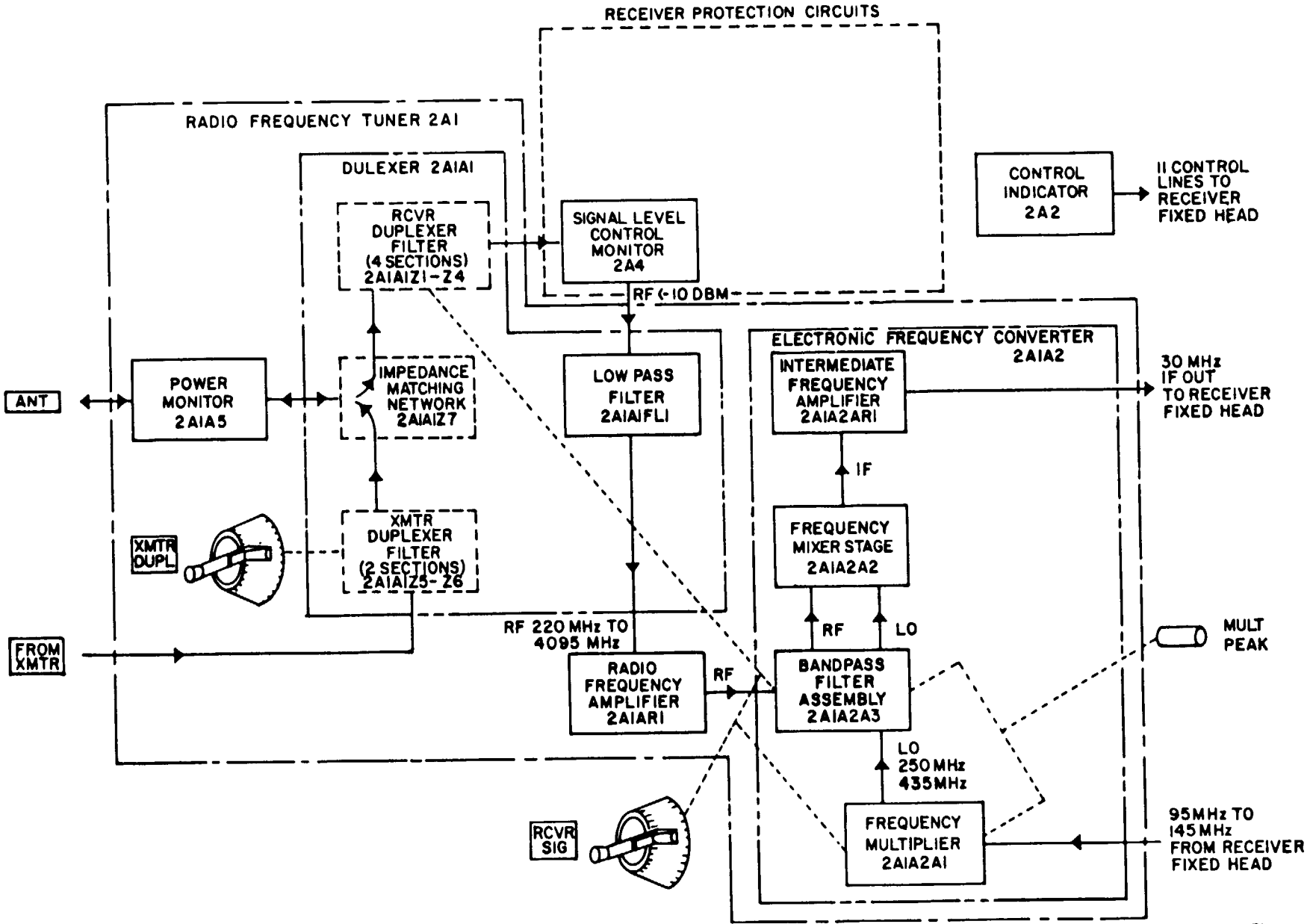
b. Receiver rf head duplexer 2A1A1 provides the necessary isolation and impedance matching between the transmit and receive signals. The rf power at the PUR OUT connector of the transmitter rf head at a level of 25 watts is fed through an external rf coaxial cable through the FROM XMTR connector on the front panel of the receiver rf head to the two-cavity (transmit) portion of bandpass filter assembly 2A1A1A1 (duplexer 2A1A1 in AM-4316A/GRC-103(V)). The tunable transmit filter is manually tuned to the transmit channel by the XMTR DUPL control. The  $\pm 2$  MHz bandwidth of the filter provides additional filtering of the transmit signal while presenting a high attenuation to the received frequency. The rf signal is then directed through impedance matching network 2A1A1Z1 (2A1A1Z7 in AM-4316A/GRC-103(V)) and power monitor 2A1A5 to the ANT. connector, and by cable to the antenna system. Power monitor 2A1A5 samples the forward and reflected rf power to the antenna system. These samples are rectified and the resulting dc voltages are used for XMTR DUPL and REFL PWR metering.

c. The receiving circuits of the receiver rf head accept modulated signals in the frequency range of 220 to 405 MHz, at a level of -54 dbm to -94 dbm and convert them to a 30 MHz intermediate frequency (IF) which is then amplified and demodulated in the receiver fixed head. The signals from the antenna, applied to the ANT. connector by lead-in cable are fed through impedance matching network 2A1A1Z1 (2A1A1Z7 in AM-4316A/GRC-103(V)) to bandpass filter assembly 2A1A1A1, a four-cavity 3 MHz bandwidth tunable bandpass filter. This bandpass filter, part of duplexer 2A1A1, is manually tuned to the receiver frequency by the RCVR SIG control. The received sig-

Figure 2-50. Receiver Rf Head (Amplifier Converter, AM-4316/GRC-103(V))  
Block Diagram.



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Figure 2-51. Receiver RF Head (Amplifier Converter, AM-4316A/GRC-103(V)), Block Diagram.

nal is then fed through a high-signal protection circuit (receiver protection circuit) which prevents rf signals greater than -10 dbm from getting into the receiver. This device, electronic switch 2A4, is essentially a single-pole double-throw rf switch which is operated by changing bias voltages on PIN diodes. A high signal condition opens the normal rf signal path and diverts the high signal to electrical dummy load 2A3, where it is dissipated. The required bias voltages for the operation of electronic switch 2A4 are supplied by power supply 2PS1. The power supply 2PS1 also provides a HIGH SIGNAL alarm indication.

d. The rf signals, below -10 dbm, are fed through low pass filter 2A1A1FL1, part of duplexer 2A1A1, to attenuate all odd harmonics of the incoming frequency. The output of the low pass filter is fed into low-noise, broadband radio frequency amplifier 2A1AR1 which has a fixed gain of  $27 \text{ db} \pm 3 \text{ db}$  over the entire frequency range of 220 to 405 MHz. The output of radio frequency amplifier 2A1AR1 is fed into electronic frequency converter 2A1A2 whose function is to mix the received rf signal with the local oscillator signal to produce the 30 MHz IF signal. The converter contains the post-amplifier and local oscillator filters, bandpass filter assembly 2A1A2A3, frequency multiplier 2A1A2A1, frequency mixer stage 2A1A2A2, and intermediate frequency amplifier 2A1A2AR1. The single section post-amplifier section of bandpass filter assembly 2A1A2A3 rejects the noise (at the image frequency) present in radio frequency amplifier 2A1AR1.

e. The input to frequency multiplier 2A1A2A1 is the output of amplifier-frequency multiplier 1RE2A5, in the range of 95 to 145 MHz. The frequency multiplier doubles the input frequency over one portion of the band and triples it over the remaining portion, to produce a continuously variable output frequency 30 MHz above the frequency of the received signal. Mechanically, the frequency multiplier is ganged to the RCVR SIG control which also drives bandpass filter assembly 2A1A1A1 and bandpass filter assembly 2A1A2A3. The RCVR SIG control adjusts the frequency multiplier and bandpass filter assembly 2A1A2A3 to a point near the required tuning point, approximately 30 MHz above the frequency of the received signal. The MULT PEAK control then tunes the frequency multiplier and both the post-amplifier and local oscillator filters of bandpass filter assembly 2A1A2A3 to their required tuning point. The ganging of the RCVR SIG and MULT PEAK is such that the three-section local oscillator filter is always tuned 30 MHz above the single-section post-amplifier filter. The received rf signal and the local oscillator signal are both fed into frequency mixer stage 2A1A2A1. The frequency mixer stage produces the 30 MHz IF signal, with a 2 db conversion loss. The IF signal is then amplified in intermediate frequency amplifier 2A1A2AR1. A portion of the local oscillator signal, detected at the input to the mixer, is rectified to provide the MULT metering voltage. The intermediate frequency amplifier is part of the IF amplification system which also includes bandpass filter 1RE1FL1 and intermediate frequency amplifier 1RE1AR2 in the receiver fixed head. Intermediate frequency amplifier 2A1A2AR1 contributes the first 30 db of the 80 db gain provided by the IF amplification system. Automatic gain control of two stages in each of the two IF amplifiers provides automatic adjustment of overall gain over a range of 50 db, depending on the input signal. Intermediate frequency amplifier 2A1A2AR1 is a broadband device, all shaping being done bandpass filter 1RE1FL1.

f. Operating voltages, +12 and -12 v regulated and 26 v unregulated, required for the-circuits in the receiver rf head, are supplied by power supply 1RE1PS1 in the

receiver fixed head. A separate power supply, 2PS1, supplies the high dc voltage required to operate electronic switch 2A4 of the receiver protection circuits (Power Supply 2PS1, is not supplied in the AM-4316A/GRC-103(V) model). An overall schematic diagram of the receiver rf head is shown in FO-4-36(FO-4-37 for AM-4316A/GRC-103(V)).

## 2-30. Duplexer 2A1A1 (AM-4316/GRC-103(V) and AM-4316A/GRC-103 (V))

a. General. Since Radio Set AN/GRC-103(V) operates with a single antenna, duplexer 2A1A1, part of radio frequency tuner 2A1, provides the necessary isolation between the transmitted signal and the receiver. The duplexer consists of bandpass filter assembly 2A1A1A1, impedance matching network 2A1A1Z1, and low pass filter 2A1A1FL1. Bandpass filter assembly 2A1A1A1 consists of six tuned cavities and two channel frequency indicators.

### b. Detailed Circuit Analysis (FO-4-36 and 4-37).

(1) Transmitting path. The transmitter portion of bandpass filter assembly 2A1A1A1 (2A1A1 in AM-4316A/GRC-103(V)) consists of two quarter-wave resonant tuned cavities, 2A1A1A1Z5 and 2A1A1A1Z6. The cavities are connected in series with capacitive input and output probes. Both cavities are tuned in parallel with adjustable plungers controlled by the XMTR DUPL front panel control. The channel to which the transmit cavities are tuned is indicated by channel frequency indicator 2A1A1A1DS2 in the X11TR CHANNEL display window. The filter has a passband of  $\pm 2$  MHz and an insertion loss of 1 db nominal. The output of the cavities is connected through a coaxial T-junction to impedance matching network 2A1A1Z1 (2A1A1Z7 in AM-4316A/GRC-103(V)), which matches the impedance of the transmitter to the antenna throughout the operating frequency band. The transmitter output is then fed through power monitor 2A1A5 to the antenna; power monitor 2A1A5 measures the forward and reverse (reflected) power of the transmitted signal.

(2) Receiving path. The received signal from the antenna is connected through power monitor 2A1A5 and impedance matching network 2A1A1Z1 (2A1A1Z7 in AM-4316A/GRC-103(V)) to the coaxial T-junction between the transmit and receive sections of bandpass filter assembly 2A1A1A1 (duplexer 2A1A1 in AM-4316A/GRC-103(V)). The transmit filter presents a high impedance at the receive frequency and the receive signal is directed into the receive section of the duplexer. The receive section consists of four quarter-wave resonant tuned cavities 2A1A1A1Z1, Z2, Z3 and Z4 (2A1A1Z1, Z2, Z3 and Z4 in AM-4316A/GRC-103(V)) similar to those in the transmit section. All four cavities are tuned in parallel by adjustable plungers controlled by the RCVR SIG front panel knob. The frequency to which the receive cavities are tuned is indicated by channel frequency indicator 2A1A1A1DS1 in the RCVR CHANNEL display window. The receive filter has a passband of  $\pm 3$  MHz and an insertion loss of 1.5 db. The signal from the receive cavities is fed through the receiver protection switch circuits (para 2-32 and 2-33) and back into the duplexer's low-pass filter 2A1A1FL1. This filter is a sealed, lumped-constant device mounted in a coaxial shield and provides approximately 35 db rejection at all frequencies above 660 MHz (3 times the lowest fundamental).

(3) Impedance matching network 2A1A1Z1 (2A1A1Z7 in AM-4316 A/GRC-103(V)). This unit consists of two coaxial stub lines and two trimmer capacitors connected across the through coaxial line, to match the transmit and receive filters to the antenna over the entire frequency range of 220 to 405 MHz. Trimmer capacitors C1 and C2 are accessible for adjustment.

(4) Tuning mechanism of bandpass filter assembly 2A1A1A1. The gear box on which bandpass filter assembly 2A1A1A1 (duplexer 2A1A1) is mounted contains two main shafts, one for the transmitter and the other for the receive section. The transmitter drive shaft, XMTR DUPL, (figs. 2-52 and 2-53) is connected to two bevel gears which drive the two individual center conductor drive screws of the resonant cavities. Similarly the receiver drive shaft, RCVR SIG, (figs. 2-54 and 2-55) is connected to four bevel gears which drive the four individual center conductor drive screws of the receiver resonant cavities.

#### 2-31. Power Monitor 2A1A5

Power monitor 2A1A5, located in the receiver rf head, is fitted in the antenna line between impedance matching network 2A1A1Z1 (2A1A1Z7 in AM-4316A/GRC-103 (V)), and the antenna connector (ANT.) on the front panel of the equipment (F0-4-36 and 4-37). The power monitor consists of a hi-directional coupler with integral detectors and temperature compensation circuits. It samples the output power to the ANT. connector and the reflected power from the antenna, rectifies the rf signals and feeds the resulting dc voltages to the meter on the front panel of the receiver fixed head. This provides appropriate meter readings when the meter switch is in either the XMTR DUPL or REFL PWR position. The unit operates in an identical manner to power monitor 6A1A3 (para 2-27).

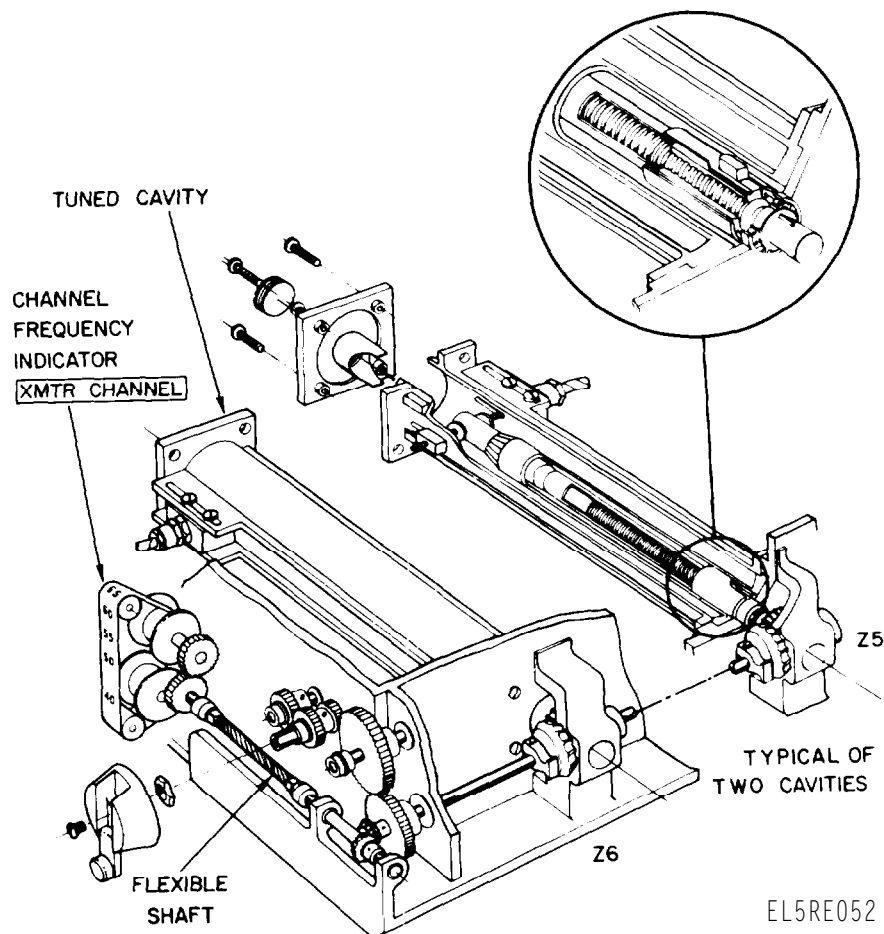


Figure 2-52. Duplexer 2A1A1, Transmitter Section, (AM-4316/GRC-103(V)), Tuning Mechanism.

2-32. Receiver Protection Switch

NOTE

This paragraph applies only to AM-4316/GRC-103(V).

a. General. The receiver protection switch is a single-pole double-throw switching-device inserted between the receive section of bandpass filter assembly 2A1A1A1 and low pass filter 2A1A1FL1. The receiver protection switch prevents any high-level signals from being fed into radio frequency amplifier 2A1AR1 and damaging it. The high-level signals can be either the transmitter output, if the receiver has been tuned to the same channel as the transmitter, or signals received from nearby external sources. The protection switch consists of electronic switch 2A4, power supply 2PS1, and electrical dummy load 2A3.

b. Block Diagram Analysis (Fig. 2-56). The received rf signal at the output of bandpass filter assembly 2A1A1A1 is fed into electronic switch 2A4. Electronic switch 2A4 consists of two separate subassemblies: electronic switch 2A4A1 and electronic switch control 2A4A2. Electronic switch 2A4A1 consists of a stripline connected switch with two PIN diodes in the receive arm and one PIN diode in the load arm. Under normal conditions, the receive arm PIN diodes are forward biased,

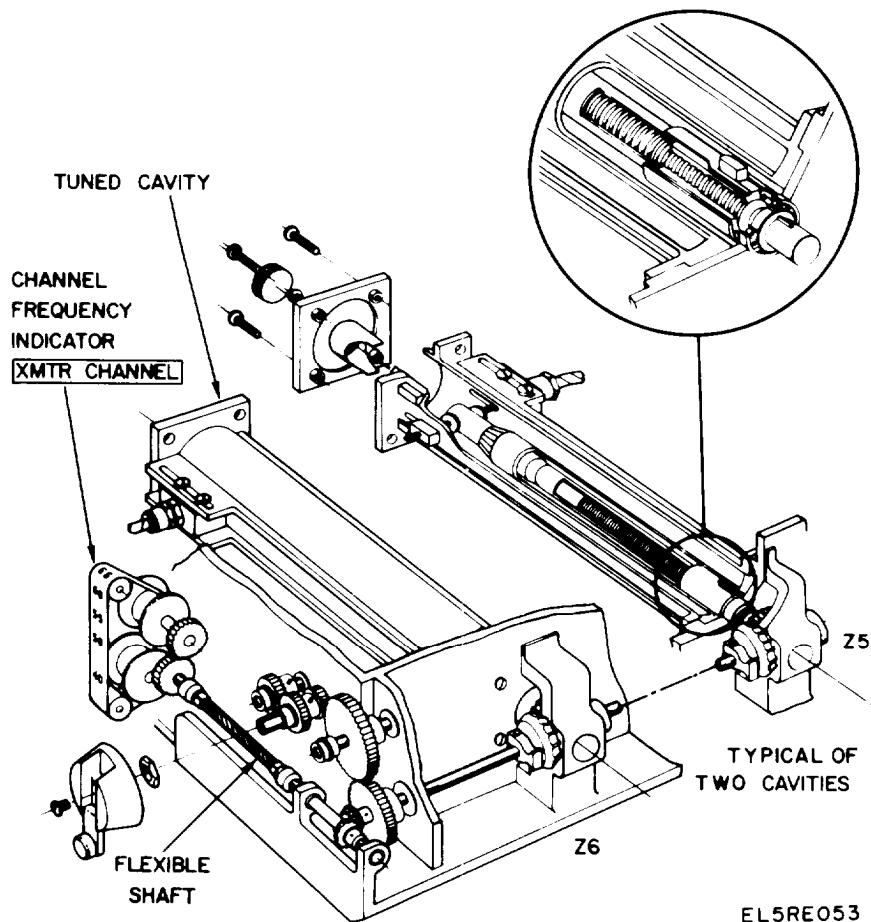


Figure 2-53. Duplexer 2A1A1 Transmitter Section, (AM-4316A/GRC-103 (V)), Tuning Mechanism.



while the load arm PIN diode is zero biased. A PIN diode has a variable rf impedance which varies from less than one ohm when forward biased to several thousand ohms when zero volts or a reverse bias is applied to it. By varying the applied voltage the diode changes very rapidly from the high impedance condition to the low impedance condition. The rf signal is normally routed through forward-biased PIN diodes of the receive arm directly to the output connector. The normal received signal sees a high impedance in the load arm due to the absence of bias on the load arm PIN diode.

(1) A tunnel diode, operating as a back-diode detector, is connected to the receive arm stripline to sense the received rf level. When this level reaches -10 dbm the diode will switch to a positive output voltage to drive the micro-circuit amplifier on electronic switch control 2A4A2. A reference dc input to this amplifier is adjusted by the TRIG LEVEL ADJ control to set the amplifier operating point, and, therefore, the signal switching level. The high gain of the amplifier results in an extremely fast switching operation. The amplifier output to the emitter-follower stage is a negative voltage under high-signal conditions. The emitter-follower stage has two outputs. One output, the alarm drive, is used to operate the switching circuits in power supply 2PS1, when a high signal is detected in the receive arm. The switching action will apply a forward bias of 3 volts to the load arm PIN diode, reducing its rf impedance to less than one ohm, and applies a 97 volt reverse bias to the receive arm PIN diodes. The high rf signal is then directed through the load arm to electrical dummy load 2A3, where it is dissipated.

(2) The second output is fed through a differentiating circuit to switch sampling transistor Q2. The differentiating circuit, which has extremely fast rise time

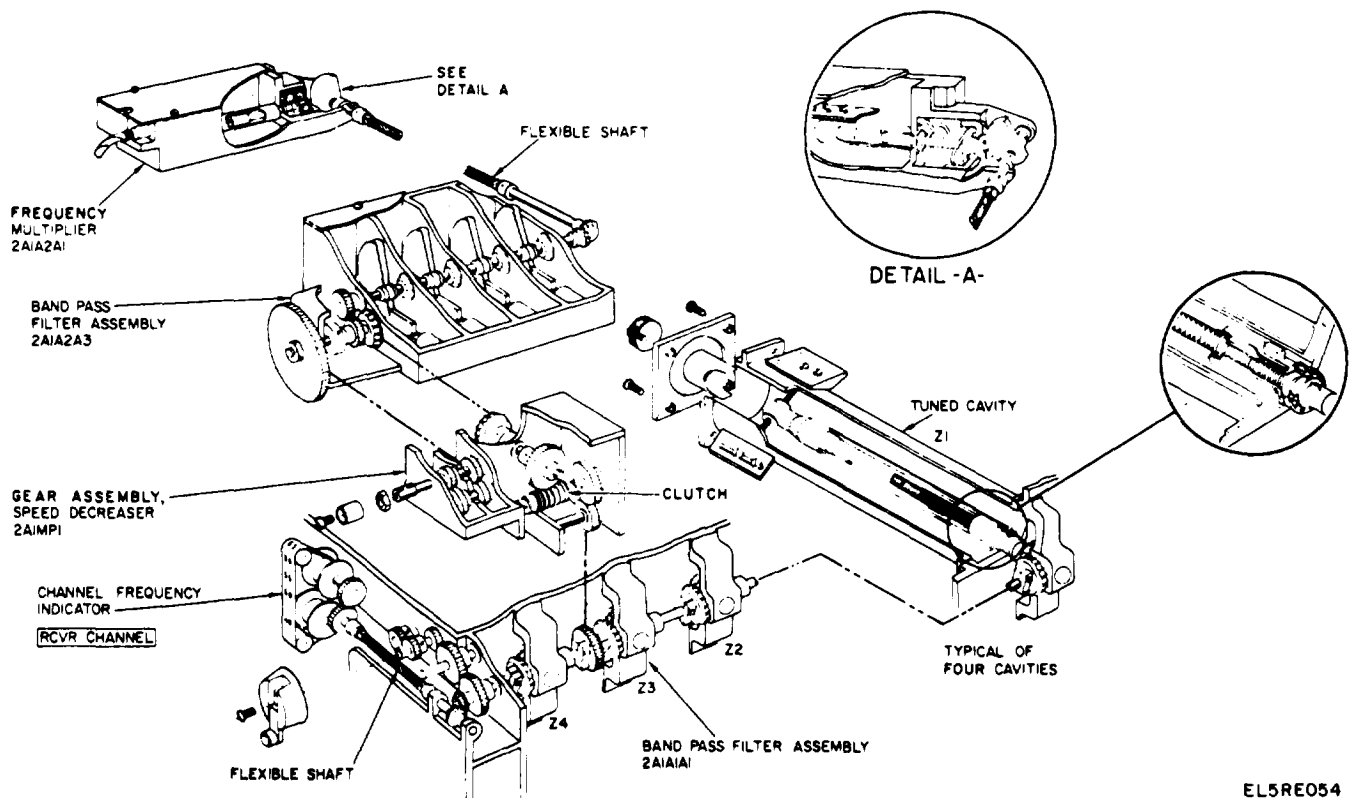
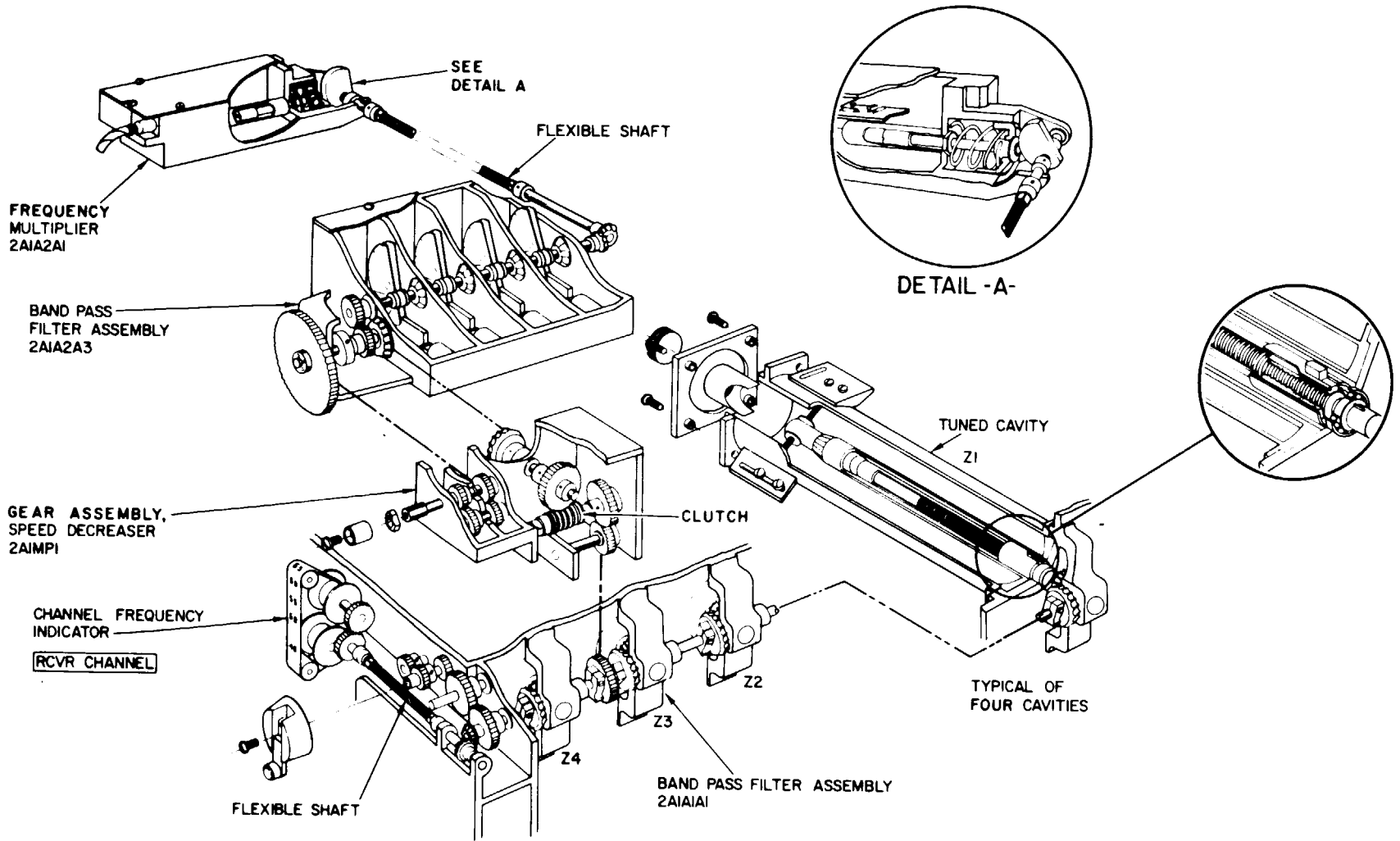
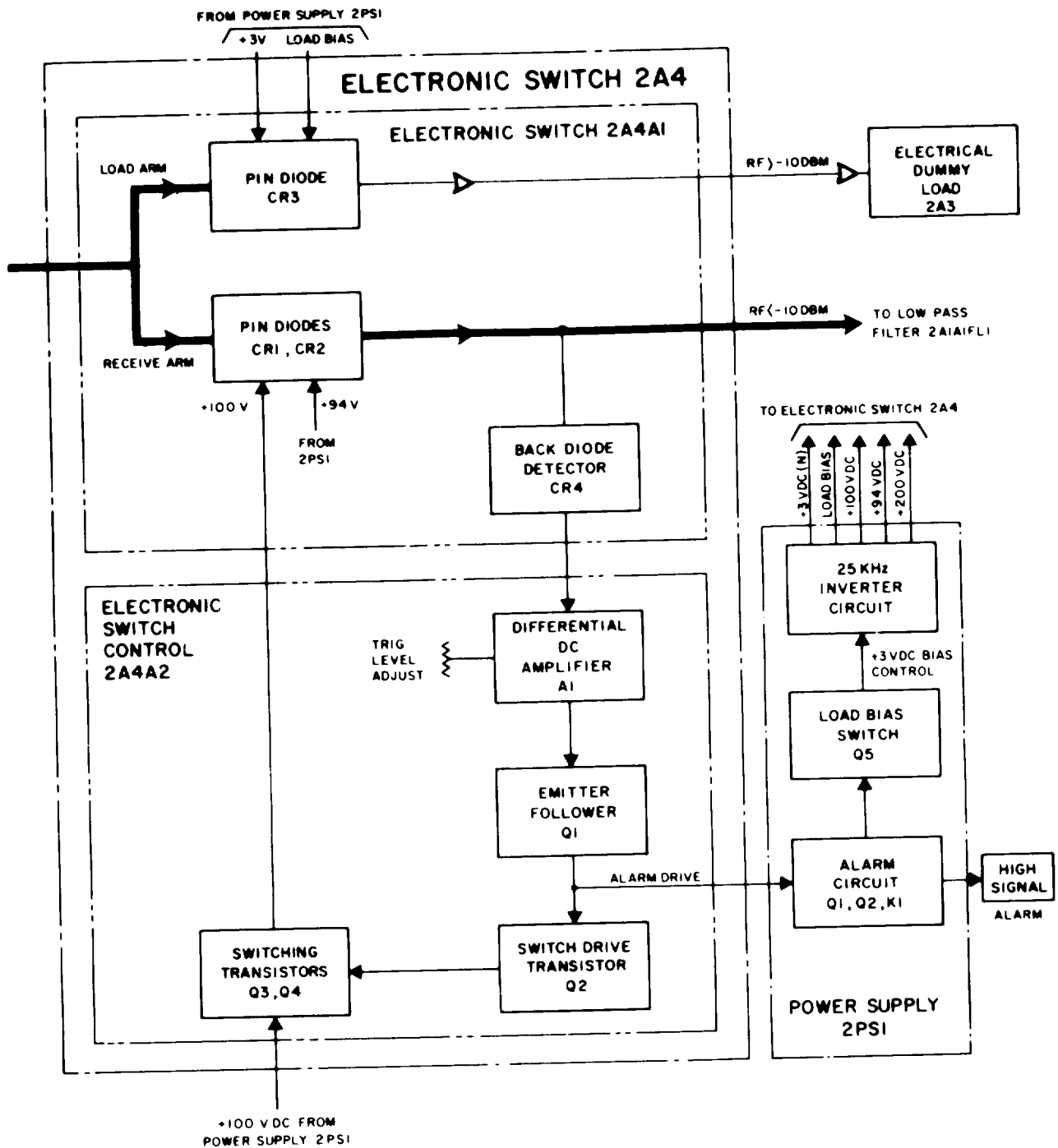


Figure 2-54. Duplexer 2A1A1 Receiver Section, (AM-4316/GRC-103(V)), Tuning Mechanism.





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Figure 2-55. Duplexer 2AIAI Receiver Section, (AM-4316A/GRC-103(V)), Tuning Mechanism.



NOTES

-  NORMAL RF SIGNAL PATH
-  FAULT CONDITION SIGNAL PATH

EL5RE056

Figure 2-56. Receiver Protection Switch, AM-4316/GGRC-103(V), Block Diagram.

and a relatively slow decay time, controls the switch sampling action. This sampling action takes place under high signal condition when no rf power is fed to the detector in the receive arm to keep it operated.

(3) Switching transistor Q3 controls the reversing action of the bias on the receive arm diodes. The normal bias on the receive arm diodes is a 100 volt potential on the positive side applied through a bias reversing stage, and a +94 volts return at the negative side. When the switch operates, the +100 volts supply line is open and the positive sides of the diodes are clamped at ground potential. This results in a reverse bias of 94 volts being applied to the receive arm diodes.

(4) The alarm drive signal at the output of Q1, electronic switch control 2A4-A2, is fed into power supply 2PS1 where it is amplified and used to operate relay drive transistor Q1. A second output from the relay drive transistor is fed to load bias transistor Q5. This transistor turns on the 3 volt forward bias to the PIN diode in the load arm in electronic switch 2A4A1.

(5) Power supply 2PS1 supplies the high level reverse bias to the receive arm PIN diodes for high signal level isolation. It also provides a 200 volt dc supply, and the 3 volt supply which is used to forward bias the load arm PIN diode under high signal conditions.

### c. Detailed Circuit Analysis.

(1) Electronic switch 2A4 (F0-4-34). The rf input signal, arriving from the receive section of bandpass filter assembly 2A1A1A1 to connector P3, is coupled through C2 to the PIN diodes in the receive arm, CR1 and CR2, and then fed through dc blocking capacitors C1 and C4 and connector P2 to low pass filter 2A1A1FL1. Normally, diodes CR1 and CR2 are forward biased; +94 vdc is applied to the cathodes of CR1 and CR2 through L1, while +100 vdc is applied to the anode through R1 and L2, resulting in a 6 vdc forward bias. L1 and L2 prevent the rf from getting into power supply 2PS1 through the dc lines. Load arm diode CR3 is normally zero biased; bias current is applied to CR3 through L3 and C7 (less negative) on one side and L4 and C8 (more negative) on the other side, so that at a low input power (less than -10 dbm) the load arm presents an isolation of at least 20 db. Decoupling capacitor C10 prevents a change in diode bias by providing extra decoupling between the high frequency circuit and the bias network. A portion of the rf signal passing through the receive arm is detected by diode CR4 in series with filter L6 and C9. The output of tunnel diode CR4 is fed to the non-inverting input, pin 3 of microcircuit differential amplifier A1 of electronic switch control 2A4A2. R1, R2 and R3 set a dc reference voltage at pin 2 of the differential amplifier; R2, the TRIG LEVEL ADJUST control, sets the rf switching level. A1 is a high-gain differential dc amplifier which amplifies the dc potential between pins 2 and 3. The output at pin 7 is coupled directly to the base of emitter-follower Q1. The output at the emitter of Q1 is used as an alarm drive and as a switch drive. The alarm drive is applied through connector P1 pin D to power supply 2PS1; the switch drive is applied through CR2 and C4 to the base of transistor Q2. The collector load, R10, of Q2 is connected to the +200 vdc base supply; the collector of Q2 is also connected to the base of Q3 switching transistor. Decoupling capacitor C10 prevents a change in diode bias by providing extra decoupling between the high frequency circuit and the bias network. In the normal operating condition, there is no signal available from the back-diode detector, so that the input at pin 3 is negative relative to the input at pin 2 of the amplifier; the output at pin 7 of the amplifier is negative in this condition. Feedback from output pin 7 is coupled through R4 and CR1 to pin 2. CR1

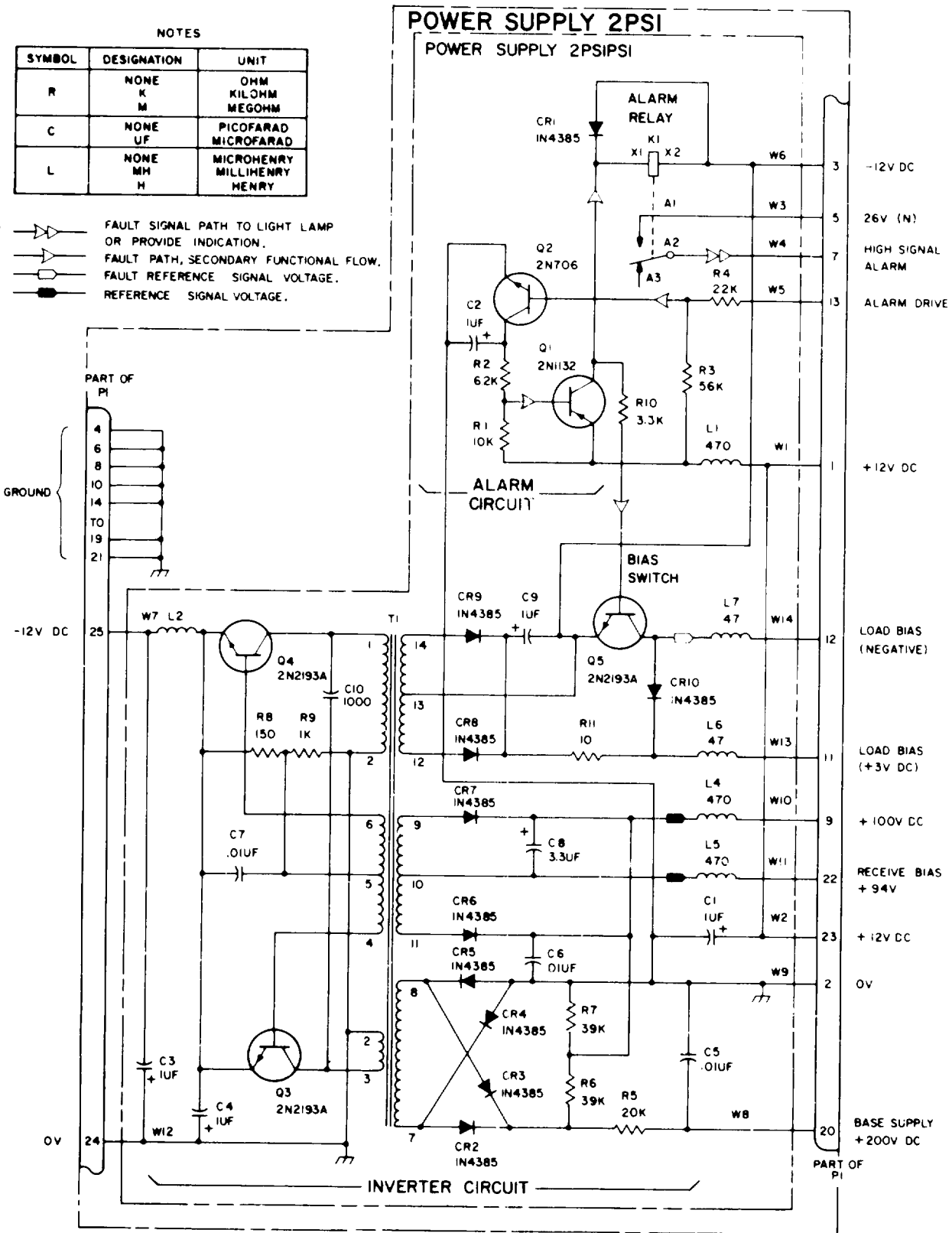
provides limiting of the feedback level to avoid amplifier saturation, which could cause a recovery delay and slow the amplifier switching time. C3 provides frequency compensation feedback. This negative output voltage, fed through emitter-follower Q1 to the base of transistor Q2 through CR2 and C4, is insufficient to make Q2 conduct and therefore Q2 is cut off. Receive arm bias, +100 vdc, is fed through Q3 to PIN diodes CR1 and CR2 in electronic switch 2A4A1; the other sides of the receive arm diodes (cathodes) are connected to +94 vdc. As long as Q2 is cut off, the base of Q4 is fed from +200 v through R10. Q3 and Q4 conduct and do not present any appreciable impedance to the bias supply to the PIN diodes. Consequently, in the normal condition, a steady dc bias is allowed to pass through the PIN diodes. In the event of high input rf power, a voltage from the back-diode detector is fed to pin 3 of the differential amplifier. When this voltage is greater than the voltage set by R2 of the amplifier, the amplifier, because of its extremely high gain, swiftly changes its negative output at pin 7 to a positive output voltage which is transmitted through emitter-follower Q1, through diode CR2 and network CR4 and R9, to the base of Q2, making Q2 conduct. When Q2 is turned on the voltage at its collector drops rapidly from +200 volts to zero while resistor R10 drops the base supply. The drop in voltage at the Q2 collector causes Q4 and Q3 to cut off removing the +100 volt potential from the anodes of the receive arm pin diodes, leaving the +94 volts potential at their cathodes. The +94 volts thus becomes a reverse bias which presents a high impedance to rf in the receive arm path. CR3 at the Q3 emitter will clamp the anodes of the receive arm pin diodes to about 0 volt through Q2, providing a return path for the dc signal, and only a voltage larger than 100 v rf peak applied to the PIN diodes can make them conduct again. However, when the circuit goes into the isolate condition, tunnel diode CR4 ceases to pass any signal back to the amplifier circuit so that the amplifier tends to return to its normal non-overload condition; this re-establishes a non-overload condition and allows a small amount of rf signal to pass to the PIN diodes in the receive arm which trips the circuit once again. This results effectively in a sampling action. The sampling "OFF" time, during which the PIN diodes are cut off and Q2 is conducting, is determined by the time constant of Q2 base circuit CR2, C4, R8 and R9. The time required to drive the PIN diodes from cut-off into conduction and bring Q2 from saturation to cut-off is the sampling "ON" time, and is determined by the time constant of Q2 collector circuit C7 and R10. The sampling "ON" and "OFF" times are 15 microseconds and 33 microseconds respectively, giving a sampling rate of approximately 21 kHz.

(2) Power supply 2PS1 (Fig. 2-57). The alarm drive signal from the Q1 emitter is coupled through inter-unit wiring and R4 to the base of Q2 in power supply 2PS1. Under high-signal conditions this is a positive signal which turns on Q2. The operating point of the alarm circuit is set by +12 vdc, applied to the base of Q2 through R3. The collector of Q2 is connected through R2 to the base of PNP transistor Q1; therefore when Q2 conducts, Q1 conducts also, and alarm relay K1 is turned on, closing the 26 v path to the HIGH SIGNAL alarm circuit. The positive signal at the Q1 collector is also coupled through R10 to the base of Q5, turning it on. Q5 is in series with a 3 volt supply which is connected back to the load arm PIN diode in electronic switch 2A4A1. This voltage then becomes a forward bias to load arm diode CR3, reducing its rf impedance and providing an rf path to electrical dummy load 2A3. The power supply circuits consist of a 25 kHz inverter transformer, T1, and transistor switching circuit Q3 and Q4. When -12 v input voltage is applied through L2 to the circuit, -11 vdc appears between terminal 5 of the inverter transformer T1 and emitters of Q3 and Q4, across C7. Bias voltage is applied to the bases of transistors Q3 and Q4 through terminals 4 and 6 of transformer T1. Q3 is cut off while Q4 is conducting, and the voltage appearing at the collector of Q3

NOTES

| SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM          |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

- 2.
- FAULT SIGNAL PATH TO LIGHT LAMP OR PROVIDE INDICATION.
  - FAULT PATH, SECONDARY FUNCTIONAL FLOW.
  - FAULT REFERENCE SIGNAL VOLTAGE.
  - REFERENCE SIGNAL VOLTAGE.



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Figure 2-57. Power Supply 2PS1, Schematic Diagram.

remains there until the transformer saturates (a period of 1/25,000 second); as saturation is reached, voltages of opposite polarity are induced in all windings, causing a reversal of current and voltage relationship between Q3 and Q4, with Q4 cut off while Q3 is conducting. The resulting output voltage is a dc square wave with a frequency of 25 kHz. The 200 vat, 25 kHz square wave at terminals 7 and 8 is rectified in a conventional bridge rectifier; CR2, CR3, CR4 and CR5. The resultant +200 vdc is fed as a base drive for switching transistors Q3 and Q4 in electronic switch control 2A4A2, through two resistors, R5 in power supply 2PS1 and R10 in electronic switch control 2A4A2. The voltage across secondary windings 9, 10 and 11 is rectified in CR6 and CR7 to give 6 v peak across C8. The upper side is connected to the +100 vdc line, derived from divider R6 and R7, so that the potential of the receiver bias line is 94 volts. The voltage across C8 is fed from the +100 v line through L4 and 2PS1 pin 9 to electronic switch control 2A4A2 through Q3, in series with PIN diodes CR1 and CR2 in the receive arm, and back to the 94 volt line to forward bias the PIN diodes under normal operating conditions. The ac voltage across secondary windings 12, 13 and 14 is rectified by CR8 and CR9 so that 3 vdc is developed across C9. This voltage is fed through transistor Q5 (normally cut off) and chokes L6 and L7 to the load arm to reverse bias PIN diode CR3; Q5 operates in conjunction with the alarm circuits as described above.

(3) Electrical dummy load 2A3. The electrical dummy load is a dissipative element in series with the load arm PIN diode and uses the gear box of the receiver rf head as a heat sink. The rf signal is fed into the center conductor of the electrical dummy load through a coaxial line. A single ground plane is used as the resistive element, and the heat is dissipated through the cast aluminum housing.

### 2-33. Signal Level Control Monitor 2A4 (AM-4316A/GRC-103 (V))

a. General. Signal level control-monitor 2A4, located between the duplexer (receive) filter and low pass filter 2A1A1FL1 (fig. 2-51) protects the low-noise amplifier circuitry (in rf amplifier 2A1AR1) against damage caused by possible high level signals being fed into the receiver. The unit also provides for an audible and visual alarm, available when it goes into protection mode. Protection is achieved by presenting a low impedance to the high-level signals, thus reflecting the unwanted power. The unit consists of two printed circuit boards; the signal level limiter 2A4A1 and alarm control 2A4A2.

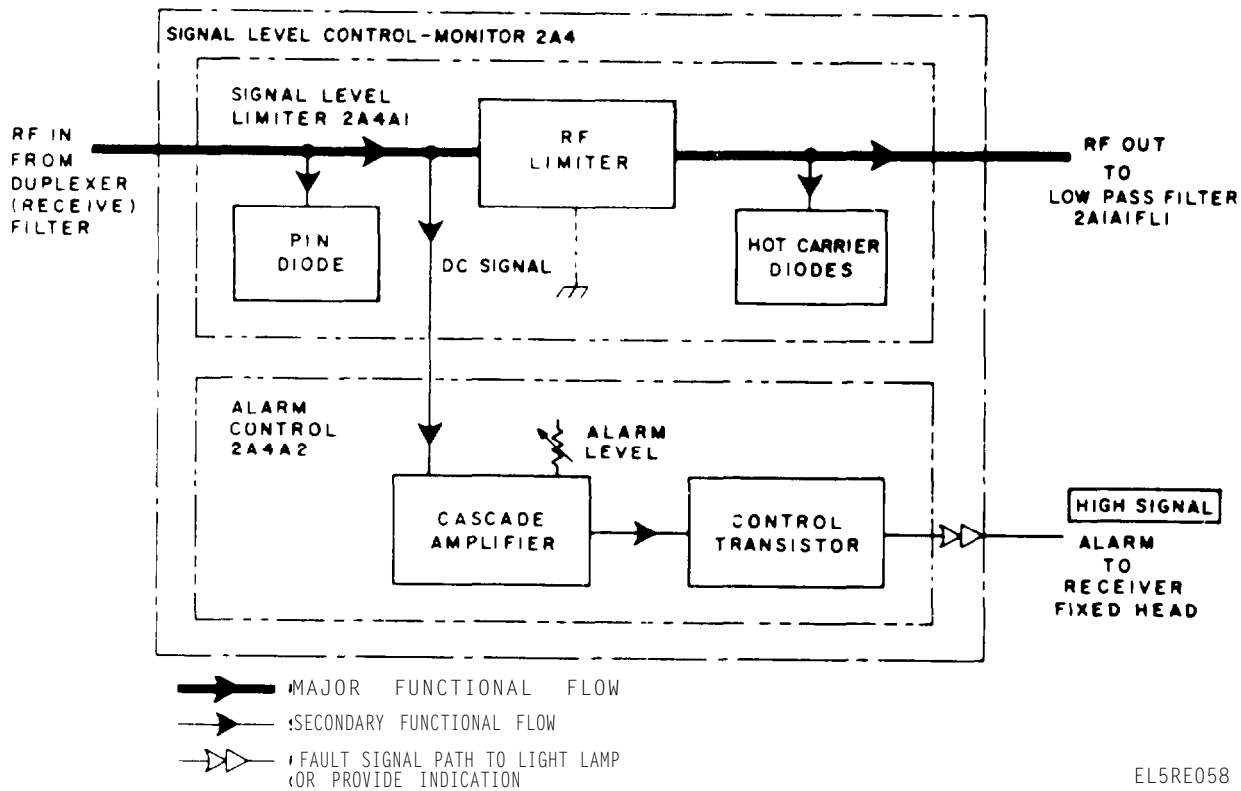
b. Block Diagram Analysis. The incoming rf signal (fig. 2-58) under normal conditions travels along the stripline through a rf limiter to the output connector with negligible loss (0.75 db max.). Two hot carrier diodes clip the peaks of a moderately high level signal (-5 to +10 dbm). Higher level signals cause the rf emitter to generate a dc current which forward biases a pin diode through which the excess rf signal is attenuated. The dc bias through the pin diode is fed to a two-stage cascade amplifier whose operating level is set by an alarm level potentiometer. A high-level signal will cause the cascade amplifier to operate and provides a path for the HIGH SIGNAL alarm circuit, through a control transistor.

### c. Detailed Circuit Analysis (FO-4-35).

(1) Signal level limiter 2A4A1. The rf input signal, from the receiver section duplexer subassembly 2A1A1, is connected to connector J1. The signal is coupled through C1 into signal limiter A1 along the stripline, to which shunt attenuator CR1, rf limiter A1 and clippers CR2 and CR3 are connected. When the input signal level is -5 dbm or less, the signal travels along the stripline from J1 to output J2

with only negligible insertion loss introduced by the stripline. As the level of the input signal increases to 0 dbm, two hot carrier diodes CR2 and CR3 start clipping peaks of the rf signal. When the level of the input signal reaches +10 dbm, rf limited A1 starts generating dc current which flows to ground, the amplitude being proportional to the level of the rf signal incident in A1. Shunt attenuator CR1 and rf limiter A1 being dc blocked within the same section of the stripline, CR1 acts as a dc return for the dc current from A1. CR1 is a PIN diode; the dc current from A1 acts as a forward bias to the diode providing a low shunt impedance to the rf signal, which results in attenuation of the signal. The response time of the circuit is extremely short, limiting high amplitude input signals almost instantly.

(2) A1 arm control 2A4A2. The negative dc voltage from the cathode of CR1 in signal level limiter 2A4A1 is fed through L1 and feed-through capacitor FL3 and applied to the base of Q1 in alarm control A2. The voltage at the emitter of Q1 is adjusted to approximately +0.2 volts by voltage divider R2, R3 and R6, and alarm-level potentiometer R3 sets the operating point for the HIGH SIGNAL alarm circuit by setting the voltage at the emitter of Q1. When the negative voltage at the base of Q1 increases to approximately -0.4 volts, Q1 starts conducting, thereby turning on Q2 and Q3. Q3 emitter-collector current flows through the HIGH SIGNAL alarm lamp and buzzer relay in the receiver fixed head, causing them to operate. R6 in the collector circuit of Q3 is a latching resistor which eliminates chatting of the alarm circuitry. When Q3 is conducting, the collector-current causes a voltage drop across R6, thereby raising the voltage level at the centertrap of R3. This increased voltage at the emitter of Q1 makes it conduct more. CR2 protects Q3 from high inductive spikes at switch off time. Resistor R4 and R5 are collector loads for Q2 and Q3.



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Figure 2-58. Signal Level Control-Monitor 24A, AM-4316A/GRC-103(V), Block Diagram.



## 2-34. Radio Frequency Amplifier 2A1AR1

a. General. Radio frequency amplifier 2A1AR1 is a low-noise, wideband, four-stage fixed-gain amplifier with a stable output, inserted in the receive signal path of the receiver front end, providing  $27 \text{ dB} \pm 3 \text{ dB}$  gain over the entire frequency range of 220 to 405 MHz, independent of input impedance. The circuit is a conventional stagger-tuned, cascaded amplifier, using low-noise transistors. Since radio frequency amplifier 2A1AR1 is the first active device in the receiver amplifier chain, it establishes the overall noise performance of the receiver. The noise figure of the 2A1AR1 is better than 6 db, giving a receiver noise figure of better than 9 db.

b. Functional Description. The incoming received signal from low pass filter 2A1A1FL1 (para 2-30) is amplified in a four-stage amplifier. The four stages are stagger-tuned to provide a bandwidth covering the full frequency range. Low-noise silicon PNP transistors are used for the first two stages, while silicon NPN transistors with good temperature stability are used for the remaining two stages. The first stage is tuned at about 325 MHz, the second at about 220 MHz, the third at about 375 MHz, while the fourth stage provides a relatively flat gain across the entire band. Stage one is connected in a common-emitter configuration which provides good stability; the remaining three stages are connected in a grounded base configuration for broad bandwidth. After amplification, the signal is fed through a 9 db matching attenuator pad to bandpass filter assembly 2A1A2A3. The gain of the amplifier is linear for signals with input levels of up to -30 dbm, while gain compression occurs for input levels above -30 dbm.

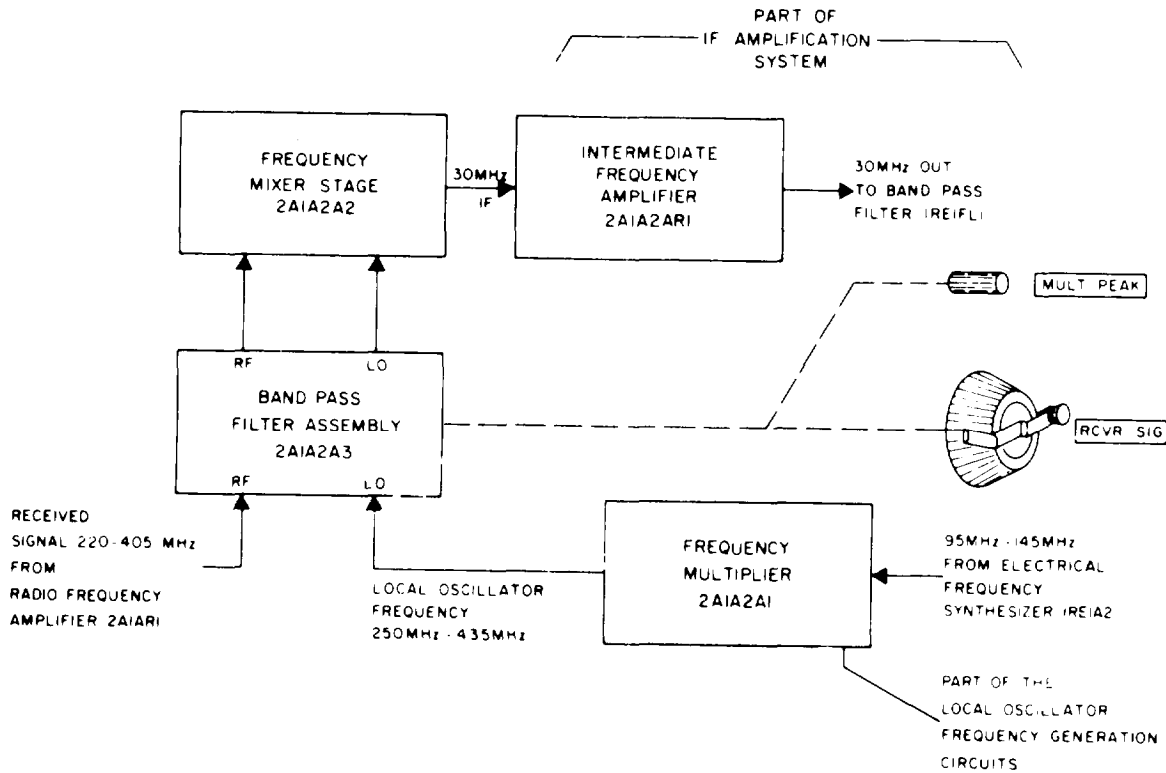
c. Detailed Circuit Analysis (FO-4-32). The incoming receiver rf signal at J1 is coupled through the C1 and L12 input matching circuit to the Q1 base. Q1 is a common-emitter configuration to insure stability under all input load conditions. Trimmer capacitor C1 is the only tuning element in radio frequency amplifier 2A1AR1. The remaining three stages, Q2, Q3 and Q4 are in a grounded base configuration which provides best performance in gain and bandwidth. L2, L4, L6 and L8 are the frequency determining elements. All but two transformer coils are air-core coils which are adjusted during manufacture by shaping or shorting the turns of wire. The 9 db pi-type attenuator, R14, R16 and R17 in the output circuit provides stability of operation in the output stage and a closer match to the 50 ohm nominal impedance.

## 2-35. Electronic Frequency, Converter 2A1A2

a. General. The electronic frequency converter, 2A1A2, consists of frequency multiplier 2A1A2A1, frequency mixer stage 2A1A2A2 and intermediate frequency amplifier 2A1A2AR1, all mounted on bandpass filter assembly 2A1A2A3. Frequency multiplier 2A1A2A1 is part of the local oscillator frequency-generating chain together with control-indicator 2A2, electrical frequency synthesizer 1RE1A2 and amplifier frequency multiplier 1RE1A5. Intermediate frequency amplifier 2A1A2AR1 is part of the intermediate frequency system, together with bandpass filter 1RE1FL1 and intermediate frequency amplifier 1RE1AR2. The bandpass filter assembly contains the post-amplifier and the local oscillator bandpass filters.

b. Block Diagram Analysis (Fig. 2-59). The main function of electronic frequency converter 2A1A2 is to mix the received rf signal with the local oscillator signal to produce the 30 MHz if. signal. The rf signal from radio frequency amplifier 2A1AR1 is fed into the post-amplifier filter section of bandpass filter assembly 2A1A2A3, which removes the image frequency noise components from the received rf signal be-

fore it is fed into frequency mixer stage 2A1A2A2. Image frequency components are not present in the output of radio frequency amplifier 2A1A1; however, without the post-amplifier bandpass filter, the frequency mixer stage will respond to noise in radio frequency amplifier 2A1A1 at the image frequency. The rf output of amplifier-frequency multiplier 1RE1A5 in the range of 95 to 145 MHz, at a level of +15 dbm, is fed into frequency multiplier 2A1A2A1 for multiplication. The output of the frequency multiplier is the local oscillator frequency in the range of 250 to 435 MHz at a level of +7 dbm. Frequency multiplier 2A1A2A1 doubles the input frequency over one portion of the band and triples it over the remaining portion. The output frequency is continuously variable using the front panel controls, RCVR SIG and MULT PEAK. The local oscillator frequency is fed into the local oscillator filter section of the bandpass filter assembly 2A1A2A3 which rejects all but the selected output frequency of frequency multiplier 2A1A2A1. The local oscillator and the post-amplifier filter sections are ganged so that the local oscillator filter is always tuned 30 MHz above the post-amplifier filter. The tuning range of the post-amplifier filter is 220 MHz to 405 MHz, and that of the local oscillator filter is 250 MHz to 435 MHz. The tuning mechanism of bandpass filter assembly 2A1A2A3 is coupled to the main gear drive of the receiver rf head. The tuning to the local oscillator frequency is done in the following two stages. The RCVR SIG control, which drives the four-cavity receiver filter of duplexer 2A1A1 (para 2-30), also adjusts bandpass filter assembly 2A1A2A3 and frequency multiplier 2A1A2A1 to a point near the required tuning point. The MULT PEAK control then tunes frequency multiplier 2A1A2A1 and bandpass filter assembly 2A1A2A3 to the required tuning point. The two outputs of bandpass filter assembly 2A1A2A3 are fed separately into frequency mixer



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Figure 2-59. Electronic Frequency Converter 2A1A2, Block Diagram.

stage 2A1A2A2 where they are mixed to produce the 30 MHz IF frequency, at a level of 2 db below the rf input signal. A metering signal (MULT) derived from the local oscillator signal input to the mixer stage provides an indication of the frequency multiplier output.

2-36. Bandpass Filter Assembly 2A1A2A3

a. Bandpass filter assembly 2A1A2A3 consists of a single section post-amplifier filter and a three-section local oscillator filter. Each section consists of a stripline with ganged variable capacitors providing the adjustment by effectively varying the lengths of stripline. The ganging arrangement is such that it provides a constant 30 MHz offset between the post-amplifier and the local oscillator filters.

b Bandpass filter assembly 2A1A2A3 uses air-spaced stripline techniques; each section consists of a quarter-wavelength coaxial line cavity, capacity-loaded to reduce the length requirement, using air-spaced capacitors for both loading and tuning. The post-amplifier filter is adjusted to resonate at a constant 30 MHz below the local oscillator filter. Tuning the local oscillator filter is achieved by adjusting the vanes of the slotted variable capacitor. The tuning mechanism of bandpass filter assembly 2A1A2A3 is coupled through a variable coupling to the RCVR SIG tuning mechanism. The MULT PEAK control provides fine tuning facilities of bandpass filter assembly 2A1A2A3 and frequency multiplier 2A1A2A1.

c. The insertion loss of the post-amplifier filter is 3.0 db and the bandwidth is 10MHz; insertion loss of the local oscillator filter is 1.0 db and bandwidth is 4.0 MHz .

2-37. Frequency Multiplier 2A1A2A1

a. General. Frequency multiplier 2A1A2A1 provides the final local oscillator frequency by doubling the frequency of the signal from amplifier-frequency multiplier 1RE1A5 over a portion of the band, and tripling it over the remainder of the band.

| Multiplication factor | Frequency range (MHz) |                |
|-----------------------|-----------------------|----------------|
|                       | Input                 | Output         |
| Times-2               | 125.0 to 144.75       | 250.0 to 289.0 |
| Times-3               | 96.66 to 145.0        | 290.0 to 435.0 |

Output frequency selection is continuously variable. The change in multiplication factor is accomplished by changing the input frequency to the point where the output tuned circuit will select the required harmonic. The second harmonic is selected over the required portion of the band and then the input frequency is stepped down to the point where the tuned circuit selects the third harmonic. The tuned circuit is varied by mechanical ganging to the RCVR SIG control and, through an idler trimming arrangement, to the MULT PEAK control.

b. Detailed Circuit Analysis (Fig. 2-60). Input signals in the range of 95 to 145 MHz at  $+14 \text{ dBm} \pm 3 \text{ dB}$  are fed through J1 into the 2 db resistive matching network, R1, R2 and R3. The signal is then coupled through L1 and C2 and capacitive trimmers C3 and C4 to the emitter of harmonic generator Q1. L1, C2, C3 and C4 extend the vswr frequency characteristics of the input matching circuit. C4 is used to adjust the input vswr over the operating frequency range. L2, C5 and R4 form a gain-compensation network (effectively a frequency selection matching network) at the emitter circuit of Q1, which compensates the gain/frequency roll-off characteristics of Q1.

(1) The multiplier circuit is a grounded-base transistor amplifier operating as a class-C amplifier. The output signal at the collector of Q1, rich in harmonics, is applied to L3. Variable capacitor C1 (externally mounted) and L3 form a tuned, selective filter, tuned to the required harmonic of the input frequency.

(2) Tuning is adjusted by front-panel control RCVR SIG, trimmed by front-panel MULT PEAK control. Tracking of the selective filter is adjusted by adjusting the slug in the L2 coil. C1 is a glass capacitor with a freely sliding cam-operated metal plunger. The cam movement closely follows the tuning laws of bandpass filter assembly 2A1A2A3.

(3) The direct transmission method used ensures consistent tracking between frequency multiplier 2A1A2A1 and bandpass filter assembly 2A1A2A3.

(4) The selected harmonic is coupled through C7 to a 3 db matching network, R5, R6 and R7, and then to output connector P2. The output signal is in the range of 250 to 435 MHz at  $+8 \text{ dbm} \pm 3 \text{ db}$ . R4 in the Q1 emitter circuit adjusts the level of the output signal and insures that the output level does not change at the multiplication changeover point.

(5) The output frequency is continuously variable, using the RCVR SIG control and an idler trimming arrangement actuated by the MULT PEAK control. To accomplish the MULT PEAK trimming function, a worm gear is permitted to slip back and forth about 1/2 inch along a square shaft before it starts driving its associated pinion gear. The worm gear is driven by the RCVR SIG control. As it turns it slips along the shaft to the stop, where it starts driving the pinion. The MULT PEAK control turns the pinion gear which then drives the worm gear along the shaft until it reaches the end of its travel. The effect is for the RCVR SIG control to drive four-cavity receiver duplexer filter 2A1A1A1Z1, Z2, Z3, Z4 (2A1A1Z1, Z2, Z3, Z4 when unit is equipped with Amplifier-Converter AM-4316A/GRC-103(V)) and adjust bandpass filter assembly 2A1A2A3 and the frequency multiplier to a point near the required tuning point; the MULT PEAK control then tunes the bandpass filter assembly and frequency multiplier 2A1A2A1 to their required tuning points.

## 2-38. Frequency Mixer Stage 2A1A2A2

a. General. Frequency mixer stage 2A1A2A2 converts the received rf signal to the 30 MHz if signal by mixing the rf signal with a local oscillator signal which is always 30 MHz above the frequency of the received signal. The two separate inputs to the frequency mixer stage are the received rf signal at a level of -33 to -73 dbm, and the local oscillator signal 30 MHz above the received rf frequency at a level of +2 dbm nominal. The output of the frequency mixer stage is a 30 Mhz if signal 2 db below the rf input level. The mixer also produces a signal suitable for metering the output of frequency multiplier 2A1A2A1.

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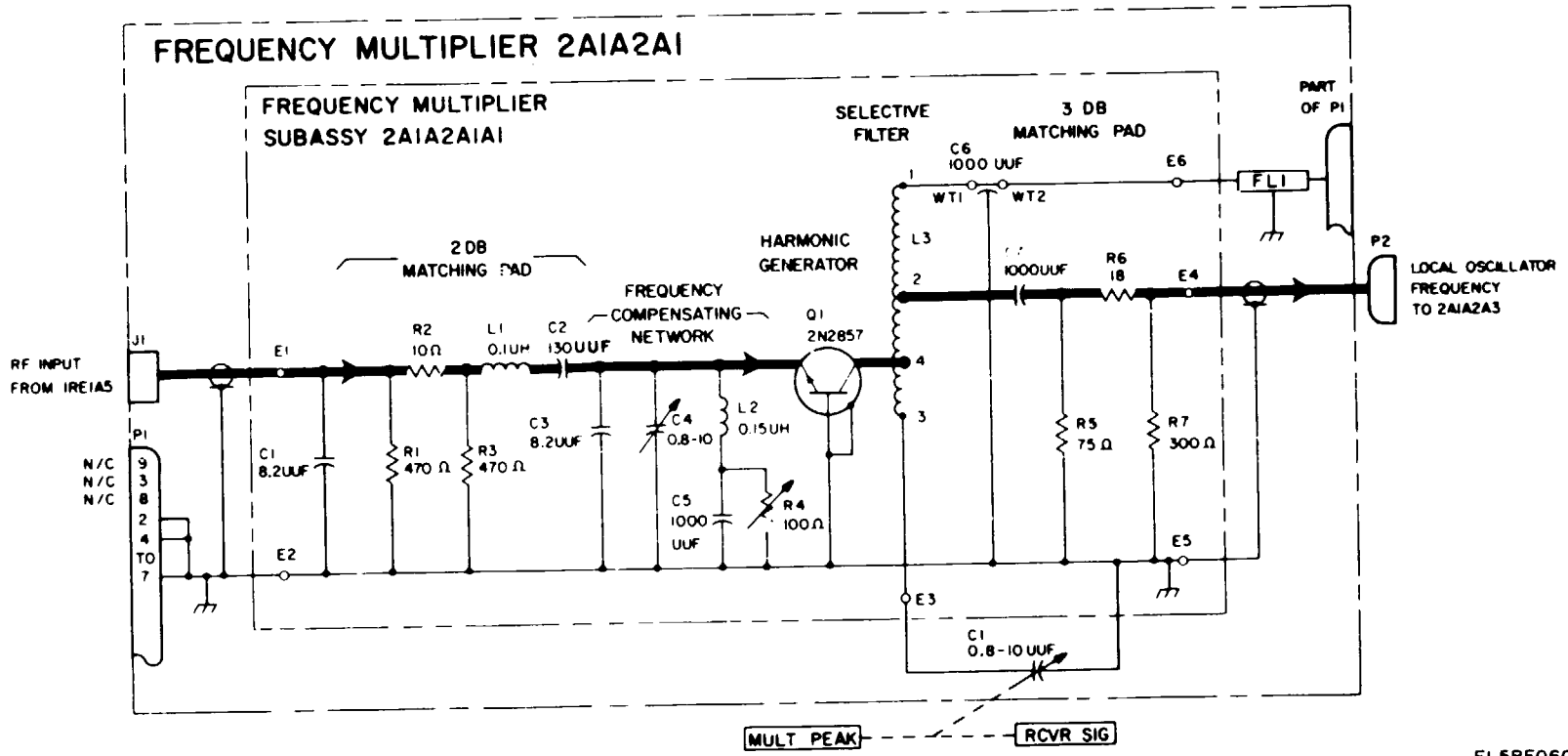


Figure 2-60. Frequency Multiplier 2A1A2A1, Schematic Diagram.

b. Detailed Circuit Analysis (Fig. 2-61). The received rf signal is applied through P2 and a 5 db matching network, R1, R2 and R3, to the base of mixer transistor Q1. Similarly, the local oscillator-signal is applied through P3 and a 17 db matching network, R10, R8 and R7, and coupling capacitor C1 to the emitter of Q1. The two resistive networks help to reduce any mutual interference between the two input signals and also provide a suitable termination for bandpass filter assembly 2A1A2A3.

(1) Mixing takes place in the emitter-base section of the transistor, which then amplifies the 30 MHz difference frequency. The amplified 30 MHz difference frequency (IF) at the collector of Q1 is fed through 30 MHz wideband coupling transformer T1 to highpass filter C7 and L4 to output connector J2.

(2) A portion of the incoming local oscillator signal is rectified in CR1 and connected through rf filter L3 to P1-4 for distribution to the meter (MULT position). L3 and C6 provide rf filtering while CR2 compresses the meter scale.

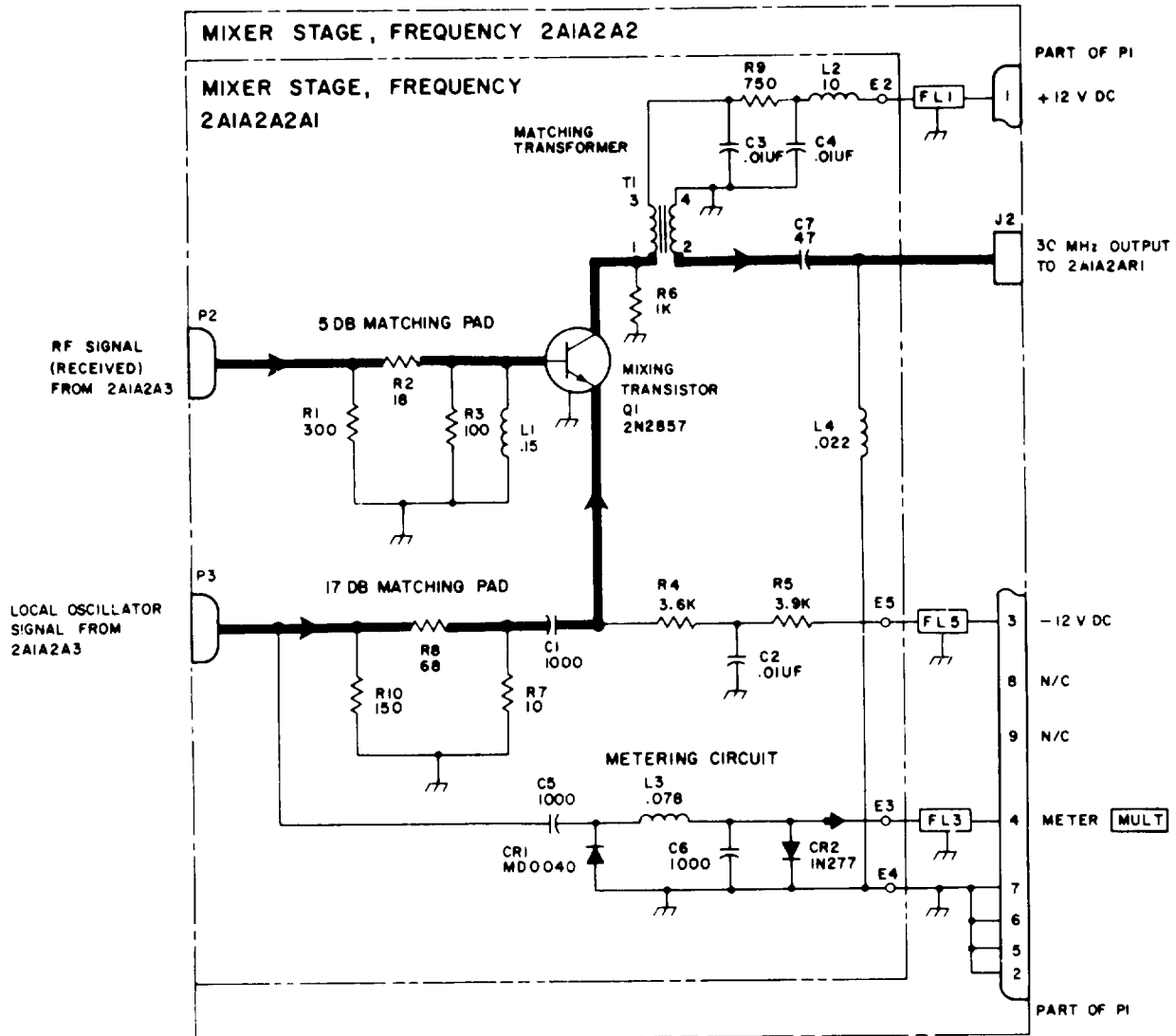
### 2-39. Control-Indicator 2A2

Control-indicator 2A2 is identical to control-indicator 6A3 with the exception of the coding arrangement. Coding in control-indicator 2A2 is arranged to produce a local oscillator frequency 30 MHz higher than the receiver frequency. The receiver channel is indicated on the front panel. The coding arrangement of control-indicator 2A2 is illustrated in FO-4-33. The construction and operation of control-indicator 6A3 and 2A2 are described in paragraph 2-28. Use the same formulas given in paragraph 2-28 to convert the selected channel into the receiver frequency and vice-versa. To obtain the local oscillator frequency add 30 MHz to the receiver frequency.

### 2-40. IF Amplifier System

a. General. The IF system in the receiver includes intermediate frequency amplifier 2A1A2AR1 (located in the receiver rf head), bandpass filter 1RE1FL1 and intermediate frequency amplifier 1RE1AR2 (both located in the receiver fixed head). The IF system can provide up to 72 db overall gain of the 30 MHz IF signal. Intermediate frequency amplifier 2A1A2AR1 provides 34 db gain, and intermediate frequency amplifier 1RE1AR2 provides 50 db gain, while the insertion loss of bandpass filter 1RE1FL1 is 12 db. Automatic adjustment of overall gain over a range of approximately 50 db, depending upon the level of input signal, is provided by automatic gain control of two stages in intermediate frequency amplifier 2A1A2AR1, and another two stages in intermediate frequency amplifier 1RE1AR2. Each of the amplifiers has a broadband response, centered at 30 MHz. All IF response shaping is done in bandpass filter 1RE1FL1, rather than in interstage tuning circuits, to prevent detuning due to the wide operating range of the automatic gain control (agc).

b. Block Diagram Analysis (Fig. 2-62) (Fig. 2-63 in Receiver Equipped With AM-431A/GRC-103(v)). The 30 MHz IF signal from frequency mixer stage 2A1A2A2, at a level ranging from about -35 to -75 dbm (depending upon received signal strength), is fed into the first stage of intermediate frequency amplifier 2A1A2AR1. Intermediate frequency amplifier 2A1A2AR1 is a four-stage (two stages, in receiver equipped with AM-4316A/GRC-103(V)) low-noise transistor amplifier, gain-controlled over a range of 15 to 40 db, and is mounted close to frequency mixer stage 2A1A2A2 to prevent noise pick-up and losses in low-level signal cabling. The first stage has a fixed gain to insure that the noise factor does not change with agc action. The



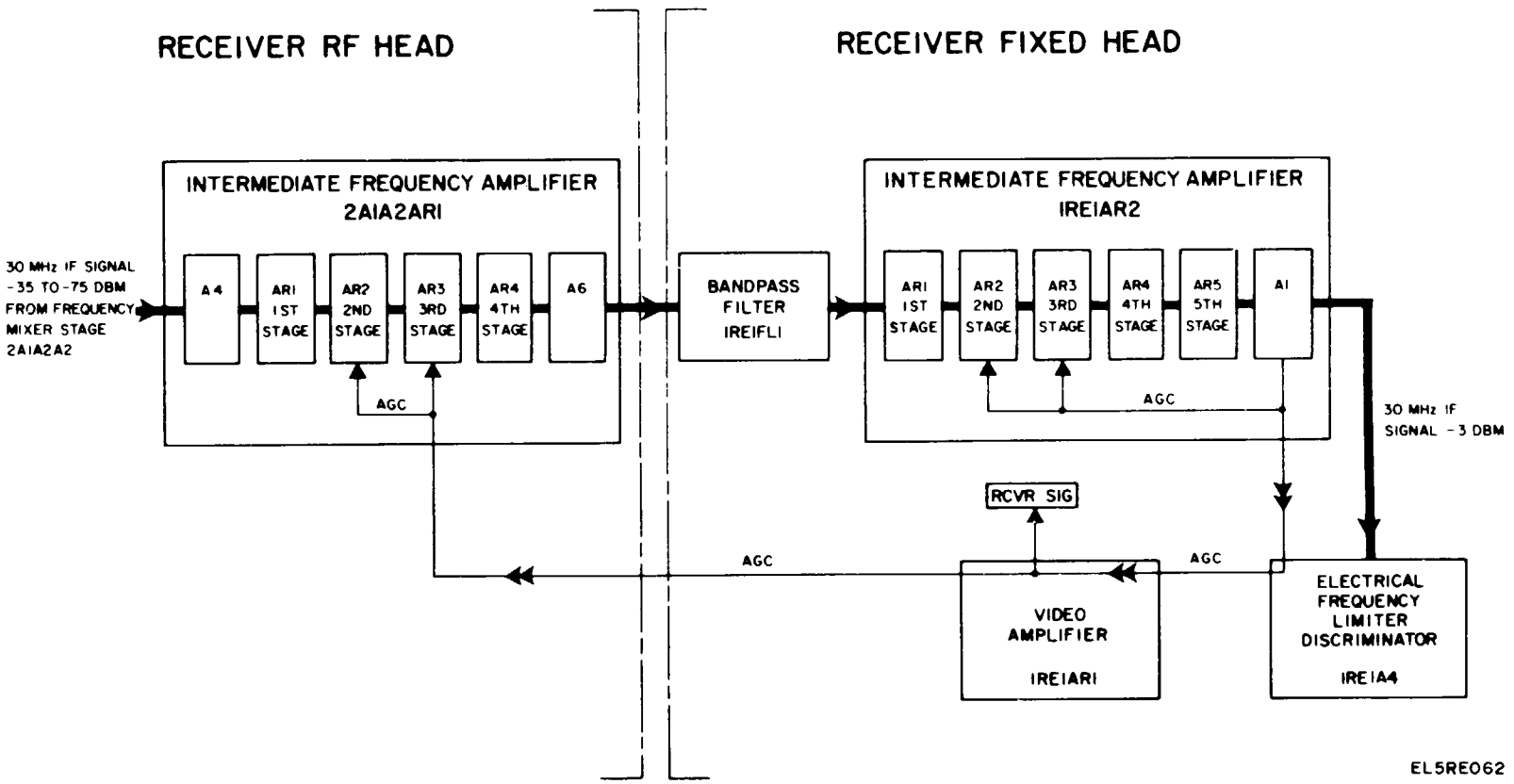
NOTES

| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHM        |
|        | K           | KILOHM     |
|        | M           | MEGOHM     |
| C      | NONE        | PICOFARAD  |
|        | UF          | MICROFARAD |
| L      | NONE        | MICROHENRY |
|        | MH          | MILLIHENRY |
|        | H           | HENRY      |

2. MAJOR FUNCTIONAL FLOW  
 METERING FLOW

EL5RE061

Figure 2-61. Frequency Mixer Stage 2A1A2A2, Schematic Diagram.



EL5RE062

Figure 2-62. IF Amplification System (AM-4316/GRC-103(V)), Block Diagram.



second and third stages (second stage, in receiver equipped with AM-4316A/GRC-103(V)) are agc controlled, their total gain being variable over a range of about 20 db (10 db in receiver equipped with AM-4316A/GRC-103(V)). The agc voltage is generated in the main IF amplifier. The fourth stage (second stage, in receivers equipped with AM-4316A/GRC-103(V)) provides impedance transformation and very little gain; the output impedance is stepped down to 50 ohms to match the input impedance to bandpass filter 1RE1FL1. Bandpass filter 1RE1FL1 is a passive device between the output of 2A1A2AR1 and the input to intermediate frequency amplifier 1RE1AR2. The unit has a closely controlled gaussian-shaped frequency response centered on 30 MHz, with an insertion loss of 12 db. Intermediate frequency amplifier 1RE1AR2 is a five-stage transistor amplifier. The first stage has a fixed gain to insure stable noise performance and input match over the large range of agc operation. The second and third stages are agc controlled, their total gain being variable over a range of about 20 db. The fifth stage has a fixed gain and supplies a signal to the agc detector as well as a -3 dbm signal to electrical frequency limiter-discriminator 1RE1A4. The agc detector is followed by a dc amplifier which raises the agc voltage and increases its sensitivity to variations in the received signal level. A metering circuit (RCVR SIG) located in video amplifier 1RE1AR1 driven by the agc voltage provides monitoring facilities for the received signal.

2-41. Intermediate Frequency Amplifier

a. Model No. 2A1A2AR1 (CMC 455-650).

(1) General. Intermediate frequency amplifier 2A1A2AR1 is constructed by the cordwood technique. This technique groups all components of each stage within a cylindrical shape which is then inserted into a circular hole in a block of cast aluminum. This type of construction has been chosen for its excellent shielding

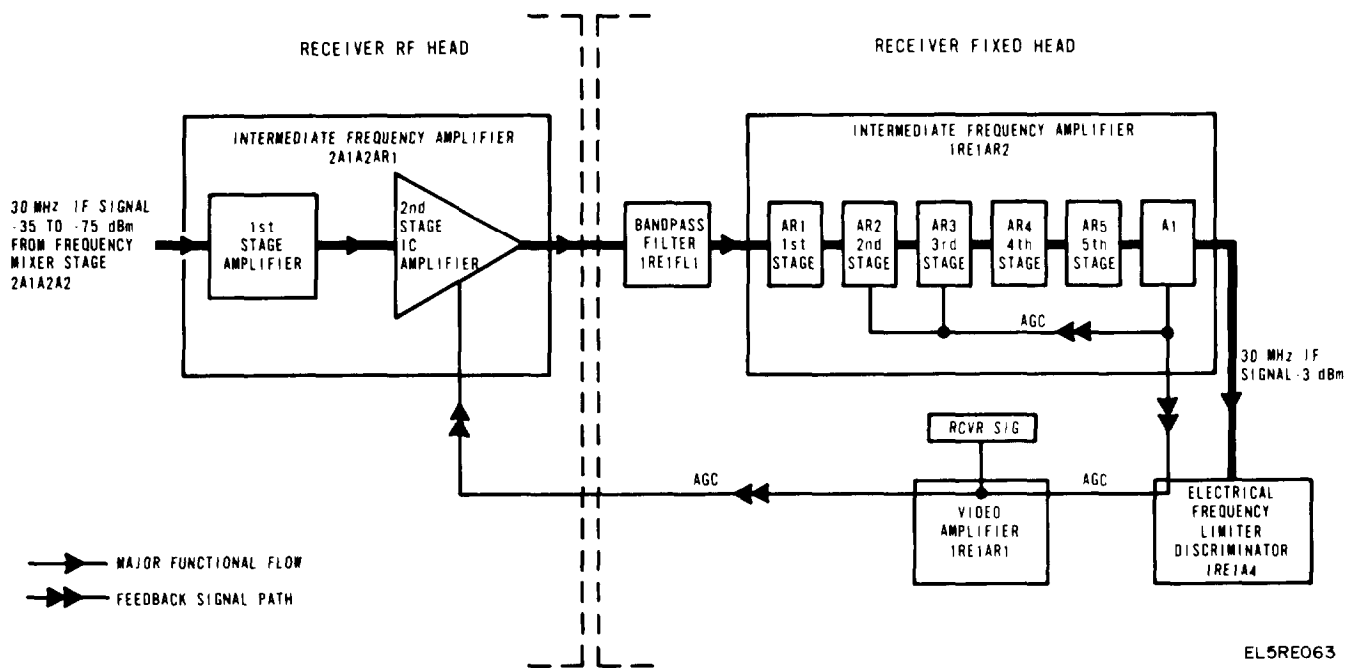


Figure 2-63. IF Amplification System (AM-4316A/GRC-103(V)), Block Diagram.

properties. Intermediate frequency amplifier 2A1A2AR1 contains six cordwood modules, four of which are similar, single-transistor amplifier stages.

(2) Detailed circuit analysis (F0-4-30). The 30 MHz signal from frequency mixer stage 2A1A2A2 is coupled through C3 of amplifier subassembly 2A1A2AR1A4 to the base of Q1, a fixed-gain transistor stage. Bias for transistor Q1 is derived from a resistive divider network, R1, R2 and R3, (amplifier subassembly A4), connected across the -12 vdc supply. The circuit uses a -12 v emitter supply, since emitter signal decoupling is more effective due to its lower signal level potential. The -12 vdc emitter supply is fed through P2 pin 3 into electrical filter assembly 2A1A2AR1A6. L1, C1, L3 and C3 filter the -12 vdc supply before it is connected to the other modules. The -12 vdc is further filtered by similar decoupling circuits (L2-C1 in each module before it is applied through R1 to the emitter of the transistors in each IF amplifier module. In each IF amplifier AR1 through AR4, C2 is the emitter bypass, R2 is the collector load and L1 is the tuning element to provide a flat response. The collector output of Q1 in IF amplifier AR1 is coupled through C3 to the base of Q1 in the next stage, IF amplifier AR2. The second and third amplifier stages have variable bias applied to the bases of their respective transistors. The agc voltage derived from the last stage of IF amplifier 1RE1AR2 is fed through P2 pin 6 into electrical filter assembly A6, filtered by L2 and C2, then filtered again by L3 and C4 in amplifiers AR4, AR2 and AR1 before being applied to the bases of the transistors in AR2 and AR3 through resistors R3. The variable bias applied to the bases of the second and third transistors causes the gain of these amplifier stages to decrease with increasing signal level at the output of intermediate frequency amplifier 1RE1AR2. The output stage, IF amplifier AR4, provides impedance transformation to match the intermediate frequency amplifier 2A1A2AR1 output into bandpass filter 1RE1FL1. Bias for the Q1 transistor of output stage AR4 is derived in IF amplifier AR3 from the -12 vdc supply, filtered by L3, and C4, through resistive divider network, R3, R4 and R5. The output stage has a fixed gain to insure stable impedance matching when the amplifier gain is varied. The amplified 30 MHz output is then fed through P2 pin 5, and through the receiver distribution box wiring, to bandpass filter 1RE1FL1 in the receiver fixed head.

b. Model No. 2A1A2AR1 (SM-D-764158).

(1) General. Intermediate frequency amplifier 2A1A2AR1 is a broadband low-noise age-controlled amplifier centered at 30 MHz, consisting of a two-stage amplifier circuit and a single transistor agc level-shifter. Nominal gain on the amplifier with no agc applied is 36 db.

(2) Detailed circuit analysis (F0-4-31). The 30 MHz from the frequency mixer stage 2A1A2A2 is coupled through C1 of amplifier subassembly 2A1A2AR1AR1 to the base of Q1, a fixed-gain transistor stage. Bias for transistor Q1 is derived from a resistive divider network, R1 and R2, connected across the -12 vdc supply. The gain of transistor Q1 is approximately 10 db and is determined by R3 and R4. L3 tunes the capacity of transistor Q1 to peak the gain at 30 MHz. The Q1 collector output is coupled through C6 to the input of integrated circuit dc amplifier A1. The gain of A1 is controlled by the agc voltage applied to pin 2 of A1. The amplified 30 MHz output of A1 is then fed to an impedance matching transformer T1 to P2 pin 5 and through the receiver distribution box wiring to bandpass filter 1RE1FL1 in the receiver fixed head. The output impedance is set by R9 and four-to-one transformer T1; this makes the output impedance of amplifier A1 look like 100 ohms. The -12 vdc supply A1 is fed through P2 pin 3. L7, C1(1 and C9 filter the -12 vdc supply. The -12 vdc is further filtered by similar decoupling circuits (L4, C4, L5, C7, L1, C2) before it is applied through resistors R4 and R7 to the emitters of Q1 and Q2. The

agc voltage derived from the last stage of IF amplifier 1RE1AR2 at P2 pin 6 is filtered by L2 and C3 and applied to the base of level shifter Q2. The agc voltage varies from -9.7 vdc to -10.7 vdc. At -9.7 vdc, the voltage at pin 2 of A1 is -8 vdc and no agc is effected at -10.7 vdc, the voltage at pin 2 of A1 is -4 vdc and full agc is effected. The range of agc is 10 db nominal and is determined by R8. When the output signal level of intermediate amplifier 1RE1AR1 increases, the dc input to level shifter Q2 will be increasingly negative, and the dc input to amplifier A1 will become increasingly positive, thus instituting agc action. Continued signal increase from intermediate amplifier 1RE1AR1 will result in further agc action.

Section IV. RECEIVER, RADIO R-1329(P)/GRC-103(V)  
R-1329A(P)/GRC-103(V), R-1329B(P)/GRC-103(V)  
AND R-1329C(P)/GRC-103(V)

2-42. Functional Block Diagram Analysis of Receiver, Radio R-1329(P)/GRC-103(V), Receiver, Radio R-1329A(P)/GRC-103(V), Receiver, Radio R-1329B(P)/GRC-103(V) and Receiver, Radio R-1329C(P)/GRC-103(V) (Fig. 2-64).

a. The receiver fixed head circuits shape and amplify the 30 MHz IF signal, detect and amplify the video signals, regenerate the pcm signal and extract the order wire signal, generate the basic crystal-controlled frequency used to obtain the local oscillator frequency, and provide metering and monitoring facilities.

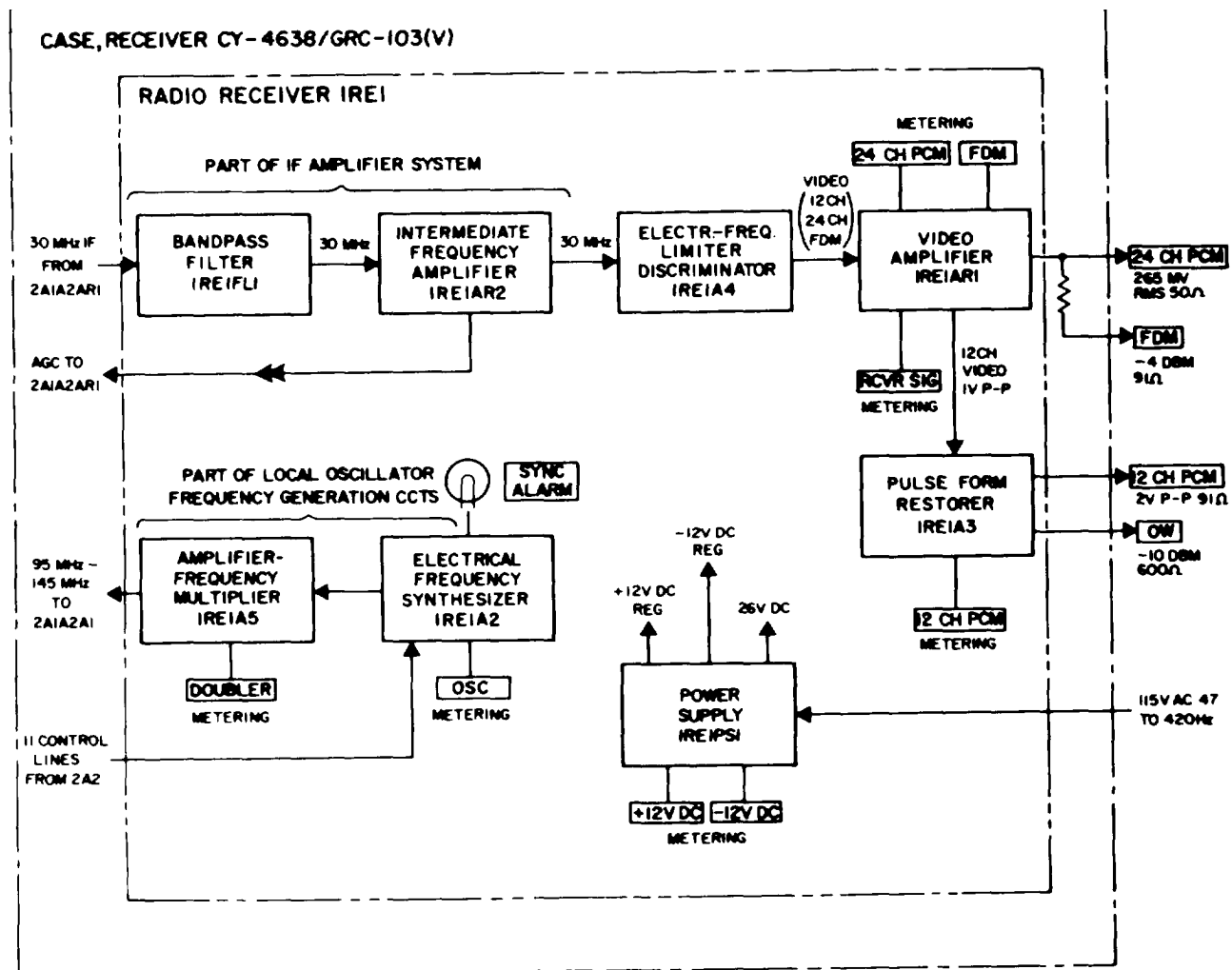
b. Shaping of the 30 MHz IF signal is done in bandpass filter 1RE1FL1, having gaussian type characteristics. The signal is amplified in intermediate frequency amplifier 1RE1AR2, which provides approximately 50 db gain, which is an agc controlled gain over a 25 db range. The agc voltage taken from the last stage controls the gain of intermediate frequency amplifiers 1RE1AR2 and 2A1A2AR1, and is also fed to video amplifier 1RE1AR1 to provide the RCVR SIG metering facility. The 30 MHz output of intermediate frequency limiter-discriminator 1RE1A4, where it is demodulated to produce the combined video (baseband) and order wire signal.

c. Video signals at the output of electrical frequency limiter-discriminator 1RE1A4 are shaped and amplified in video amplifier 1RE1AR1. In Receiver, Radios R-1329, R-1329A, and R-1329B the video amplifier provides three outputs: 12-channel pcm video to pulse form restorer 1RE1A3, pcm regeneration and order wire extraction; 24-channel pcm video at the receiver case VIDEO connector; and fdm video at the receiver case FDM connector. In Receiver, Radio R-1329C the video amplifier provides 12 and 24 channel pcm video to pulse form restorer 1RE1A3 for pcm regeneration and order wire extraction, and fdm video at the receiver case FDM connector. In Receiver, Radio R-1329 and R-1329A the video amplifier also monitors the baseband signals for noise content and provides squelch of regenerated pcm or fdm video when the noise content indicates that the received signal is below the minimum operating level. In Receiver, Radio R-1329B and R-1329C the squelch circuit of the video amplifier (Part No. CMC 455-975-2 in these receivers) has been de-activated. In addition, the amplifier provides metering facilities for 24 CH PCM, FDM, and RCVR SIG levels.

d. In Receiver, Radio R-1329 and R-1329A, pulse form restorer 1RE1A3 reshapes the distorted pulses in the pcm pulse train and passes them into the multiplex equipment through the squelch circuit in video amplifier 1RE1AR1. In Receiver, Radio R-1329B and R-1329C, the pcm pulse train passes through the same circuit in video amplifier 1RE1AR1 but the circuit in this amplifier (CMC 455-975-2) has been de-activated. The pulse form restorer in Receiver, R-1329, R-1329A, and R-1329B

also produces timing pulses at a 570 kHz bit rate, synchronized with the pcm pulse train. Recovery of the order wire signal from the combined video/order wire signal is also done in the pulse form restorer; the recovered order wire signal is then fed through external cabling to Receiver-Transmitter, Order Wire RT-773/GRC-103(V). In addition, the pulse form restorer provides the regenerated 12 CH PCM and OW metering facilities.

In Receiver, Radio R-1329C, the pulse form restorer 1RE1A3 (SM-D-990510, CMC Part No. 245-803110-000) fitted is capable of dealing with three different bit rates. The unit is switched between its two operating modes of 288/576 kb/s and 1152 kb/s by an external control signal. This pulse form restorer receives a filtered baseband video signal from the video amplifier and regenerates the pcm, timing and order wire signals. It also contains provision to select a recovered order wire signal from an external combiner. Under this condition, the external order wire input signal is routed to the order wire output by means of a relay. In addition, the pulse form restorer provides the regenerated 12-channel pcm and order wire metering facilities.



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Figure 2-64. Receivers, Radio R-1329(P)/GRC-103(V), R-1329A(P)/GRC-103(V) and R-1329B(P)/GRC-103(V), Block Diagram.

f. Electrical frequency synthesizer 1RE1A2 generates the basic local oscillator frequency which is doubled in amplifier-frequency multiplier 1RE1A5. The selection of the basic local oscillator frequency is accomplished, as in the transmitter, in conjunction with the manually operated control-indicator in the receiver rf head. Control-Indicator 2A2 (RCVR CHANNEL) coding is chosen so as to automatically obtain a local oscillator frequency 30 MHz above the frequency of the receive channel. The RCVR CHANNEL indicator, however, is calibrated to indicate the frequency of the receive channel rather than the frequency of the local oscillator signal.

g. The receiver fixed head power supply, 1RE1PS1, produces the 26 volt dc non-regulated and the +12 volt dc and -12 volt dc regulated voltages required to operate the receiver fixed and rf head c circuits and the order wire unit. The power supply operates from a 115 volt ac, 47 to 420 Hz source.

h. Metering facilities are provided in the receiver fixed head for the +12 volt and -12 volt dc supplies; for the output levels of electrical frequency synthesizer (OSC), amplifier-frequency multiplier (DOUBLER), frequency multiplier (MULT), antenna transmit signal level (XMTR DUPL), reflected power (REFL PWR), received signal level (RCVR SIG), regenerated pcm level (12 CH PCM), video levels (24 CH PCM and FDM) and recovered order wire output level (OW). Alarm circuits are provided to indicate a high received signal condition (HIGH SIGNAL), out-of-lock condition of the afc loop used to control the output frequency of the synthesizer (SYNC) and a high-noise condition (LOW SIGNAL).

2-43. Bandpass Filter 1RE1FL1

Bandpass filter 1RE1FL1 is a sealed unit, tuned during manufacture to produce a closely controlled gaussian frequency response with the following characteristics: 3 db at  $\pm 375$  kHz and 60 db minimum at  $\pm 1,000$  kHz. The insertion loss is 20 db maximum. The frequency response of bandpass filter 1RE1FL1 is shown in figure 2-65.

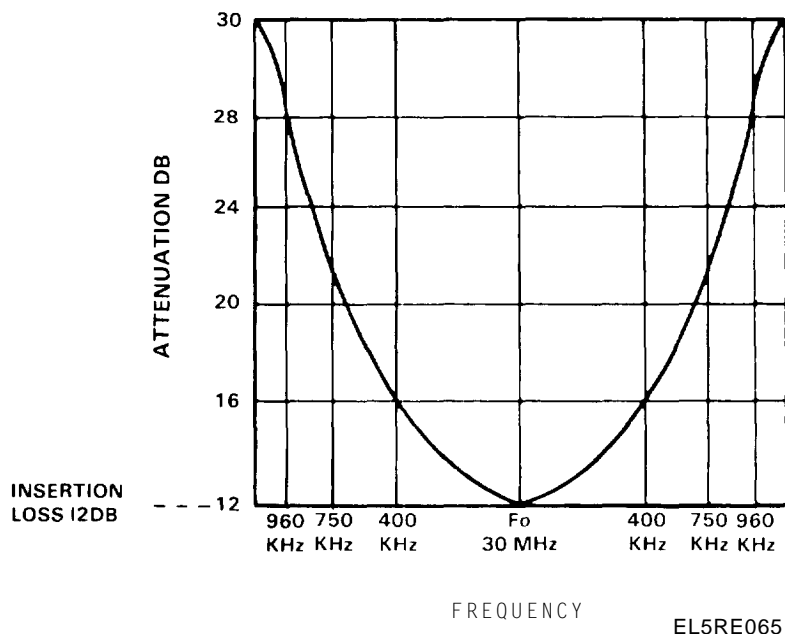


Figure 2-65. Bandpass Filter 1RE1FL1, Frequency Response Curve.

## 2-44. Intermediate Frequency Amplifier 1RE1AR2

a. General. Intermediate frequency amplifier 1RE1AR2 is similar to intermediate frequency amplifier 2A1A2AR1, being constructed by the cordwood technique. Intermediate frequency amplifier 1RE1AR2 contains six cordwood modules, four of which are similar single-transistor amplifier stages.

b. Detailed Circuit Analysis (FO-4-26). The 30 MHz signal from bandpass filter 1RE1FL1 at P2 is coupled through C1 to the base of the first amplifier stage, Q1, which is a fixed-gain amplifier stage to provide a stable impedance match for the output of the bandpass filter 1RE1FL1. R1 and L1 are the input terminating resistance and rf load. Bias for transistor Q1 is derived from resistive divider R2 and R3, connected across the -12 vdc supply line. The circuit uses a -12 v emitter supply for more effective emitter signal decoupling at low signal level potentials. The -12 v emitter supply is connected through J2 pin 3 to terminal E1 of rf detector 1RE1AR2A1 then passed in through coupling filters L2 and C1 of IF amplifiers AR5, AR4, AR3, and AR2 to coupling filter J3 and C2 of IF amplifier AR1. R5 is the collector load, matching the base impedance of the next stage. C3 is the emitter bypass, while L2 is a peaking element to provide a flat response. C5 provides filtering between the -12 v supply and the agc line.

(1) The signal at the collector of Q1 is coupled through C4 to the base of Q1 in the next stage IF amplifier 1RE1AR2AR2. The second and third amplifier stages have variable bias applied to the bases of their respective transistors. The second stage circuit is similar to that of the first stage. Variable bias voltage (age) is applied to the base of Q1 (second stage) through L4 and R6 of IF amplifier 1RE1AR2AR1 (first stage). The signal at the collector of Q1 (second stage) is coupled through C3 to the base of the third stage. Variable bias (age) for the third stage is applied through resistor R3 of 1RE1AR2AR2 to the base of Q1 of 1RE1AR2AR3. The fourth and fifth stages are similar fixed-gain amplifiers. Fixed bias voltage to the bases of the respective transistors is derived from the -12 vdc supply through resistive divider R3 and R4. The -12 vdc supply is filtered by L3 and C4 in 1RE1AR2AR3 before being used as bias voltage. The fifth stage is the output amplifier. A collector load resistor is not required in this stage since the inherent collector output impedance (300 ohms) matches the input impedance of electrical frequency limiter-discriminator 1RE1A4. The collector output is then fed through J2 pin A1 (a coaxial connector) to 1RE1A4.

(2) A portion of this signal is fed into rf detector 1RE1AR2A1 and coupled through C1 to step-up transformer T1. The signal is stepped up by a 2:1 ratio, and rectified in peak detector, CR1, C2, CR2, and C3. The resulting dc voltage is amplified by Q1, a 2N930-type transistor with high base impedance which will not disturb the peak detecting action by drawing too much current from the detector circuit. CR3, a 5.1 v Zener diode, is used to translate the -2 to -3 v potential at Q1 collector to the -7 to -8 v required for agc action. The agc voltage, besides being used to adjust the gain of the two intermediate frequency amplifiers 2A1A2AR1 and 1RE1AR2, is coupled into video amplifier 1RE1AR1 where it is used for receiver signal metering (para 2-46).

## 2-45. Electrical Frequency Limiter-Discriminator 1RE1A4

a. General. Electrical frequency limiter-discriminator 1RE1A4 (demodulator) converts the frequency modulation information contained in the 30 MHz IF signal to

a baseband signal (video), identical to the baseband signal used to modulate the synthesizer output in the remote transmitter. Like the two intermediate frequency amplifiers 2A1A2AR1 and 1RE1AR2, this unit is constructed by the cordwood principle. The 30 MHz IF input signal is frequency-modulated at 75 kHz when carrying fdm traffic, and 180 kHz or 300 kHz when carrying 12- or 24-channel pcm traffic respectively. Order wire signal deviation at 45 kHz may be present with or without any of these types of video traffic. The output of the demodulator will be a video signal at 27 mv rms for fdm traffic, and 53 mv rms or 106 mv rms for 12- and 24-channel pcm traffic. The order wire signal is contained in the video signal.

b. Block Diagram Analysis (Fig.2-66). The 30 MHz IF signal at -3 dbm from the intermediate frequency amplifier 1RE1AR2 is amplitude-limited in two amplifier/limiter stages to insure that amplitude variations will not affect the demodulated output signal. These stages are similar to the fixed-gain amplifier stages in Intermediate frequency amplifier 2A1A2AR1 or 1RE1AR2 (para 2-44), with an additional limiting diode in each collector circuit. The next stage is an amplifier feeding the primary of a tuned high-tuned low discriminator-transformer. The two secondary windings are tuned 2.5 MHz above and 2.5 MHz below 30 MHz. The two transformer outputs are then rectified to reproduce baseband signals. These signals are then fed through an emitter-follower stage which will prevent the video amplifier 1RE1AR1 circuits from loading the discriminator circuits. A LEVEL potentiometer in series with the output signal permits adjustment of the output level.

c. Detailed Circuit Analysis (FO-4-22). The 30 MHz IF signal is fed through connector A1 to the electrical noise limiter 1RE1A4A3 module and coupled through C2 to the base of Q1. Bias for Q1 is derived from the -12 vdc line through resistive divider R2 and R3. Similar to intermediate frequency amplifier 1RE1AR2 and 2A1A2AR1, -12 vdc is used as emitter supply (rather than +12 v collector supply) because emitter signal decoupling is more effective at a lower signal level. C1 and L3 provide rf filtering of the -12 vdc supply. L1 is the rf load in the base circuit and L2 is the rf load in the collector circuit. R1 serves to match the base impedance of Q1 to the output impedance of the main IF amplifier. CR1 limits the level of the signal at Q1 collector. C3 is the emitter bypass. The signal at the collector of Q1 is then coupled through C4 to the base of Q1 of electrical noise limiter 1RE1A4A4. Bias for Q1 of 1RE1A4A4 is obtained from the resistive divider R6, R7 in 1RE1A4A3. The operation of 1RE1A4A4 stage is identical to that of 1RE1A4A3. The output of the second amplifier/limiter stage is then coupled through C3 to the base of Q1, the discriminator divider-amplifier in the discriminator subassembly 1RE1A4A1.

(1) Bias for Q1 is obtained from -12 vdc through resistive divider R3, R4 in 1RE1A4A3. The primary winding of the discriminator transformer T1, together with C4 and C1 in capacitor assembly 1RE1A4A5, form a tuned circuit centered on 30 MHz with a flat response around the midband. The tuned center frequency is adjusted by C1 in 1RE1A4A5. The two secondary windings of T1, together with capacitors in 1RE1A4A5, form two tuned circuits, one centered on 27.5 MHz (C2 and C5) and the other on 32.5 MHz (C3 and C6). These circuits are adjusted by C2 and C3 respectively. R3 and R4 in discriminator subassembly 1RE1A4A1 provide unequal damping of the secondary tuned circuits in the correct ratio to equalize the output voltages, as the frequency is shifted above and below the center frequency.

(2) The output voltages from the secondary tuned circuits are rectified by CR1 and CR2 before they are combined in R1 of video amplifier 1RE1A4AR1. The

demodulated signal is then coupled through C1 to the base of emitter-follower Q1. R1 in the output stage is adjusted to supply zero volts to the base of emitter-follower Q1 at 30 MHz, and positive or negative voltage as the incoming frequency shifts above or below 30 MHz. The output at the emitter of Q1 is then coupled through C2 to level control R2 and then to A1, the output connector. The emitter follower is used to isolate the limiter-discriminator circuits from those of the video amplifier 1RE1AR1.

2-46. Video Amplifier 1RE1AR1

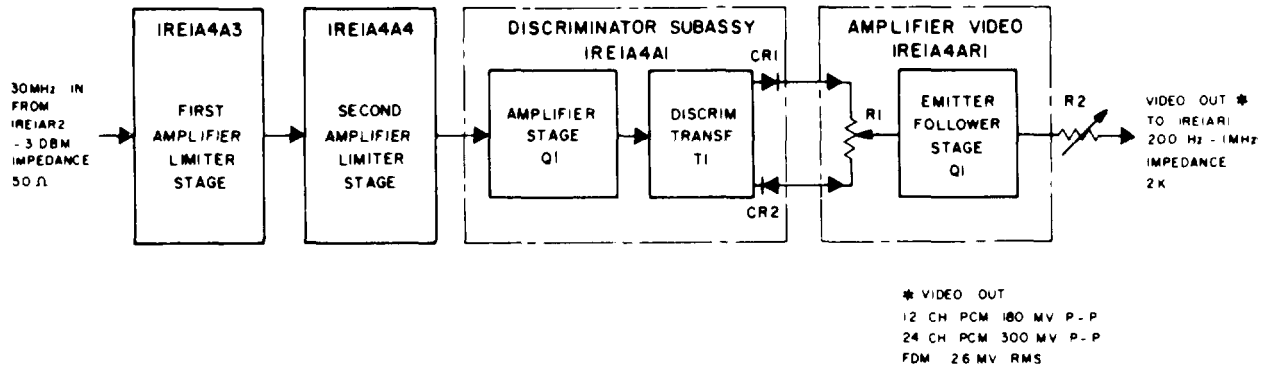


Figure 2-66. Electrical Frequency Limiter-Discriminator 1RE1A4, Block Diagram.

NOTE

The two modes of video amplifier 1RE1AR1 are distinguishable by part numbers CMC 455-975 (SM-C-698003) (fig. 2-67) and CMC 455-975-2 (SM-C-967354 (fig. 2-68). Except where specified otherwise, this paragraph refers to both units.

a. General. Video amplifier 1RE1AR1 provides the last stage of amplification of the received signal and controls the level and the frequency response of the video (baseband) signal. The demodulated signal from electrical frequency limiter-discriminator 1RE1A4 contains both video and order wire signals. The video signal is either 12- or 24-channel pcm traffic or fdm traffic, depending upon the system requirements. In Receiver, Radio R-1329, R-1329A, and R-1329B, order wire separation takes place in pulse form restorer 1RE1A3 for both 12-channel pcm and fdm traffic; order wire separation takes place in the combiner for 24-channel traffic. In Receiver, Radio R-1329C the order wire separation for 12 and 24 channel pcm and fdm traffic all takes place in the pulse form restorer ((SM-D-990510) . In all receivers, in addition, video amplifier 1RE1AR1 produces a dc metering voltage to indicate the level of the fdm or 24-channel pcm video used for system line-up, and a dc metering voltage (derived from the agc voltage) to indicate the received signal level. In Receiver, Radio R-1329, R-1329A, and



R-1329B, the 12-channel pcm video is then fed into pulse form restorer 1RE1A3 for pcm regeneration and order wire separation. Fdm and 24-channel pcm video outputs are connected to the FDM or VIDEO connectors at the rear of the case through a resistive divider mounted in the receiver case. In Receiver, Radio R-1329C, the pcm video is then fed into pulse form restorer 1RE1A3 for pcm regeneration and order wire separation. Fdm video output is connected to the FDM and VIDEO connectors at the rear of the case through a resistive divider and frequency response equalizer mounted in the receiver case.

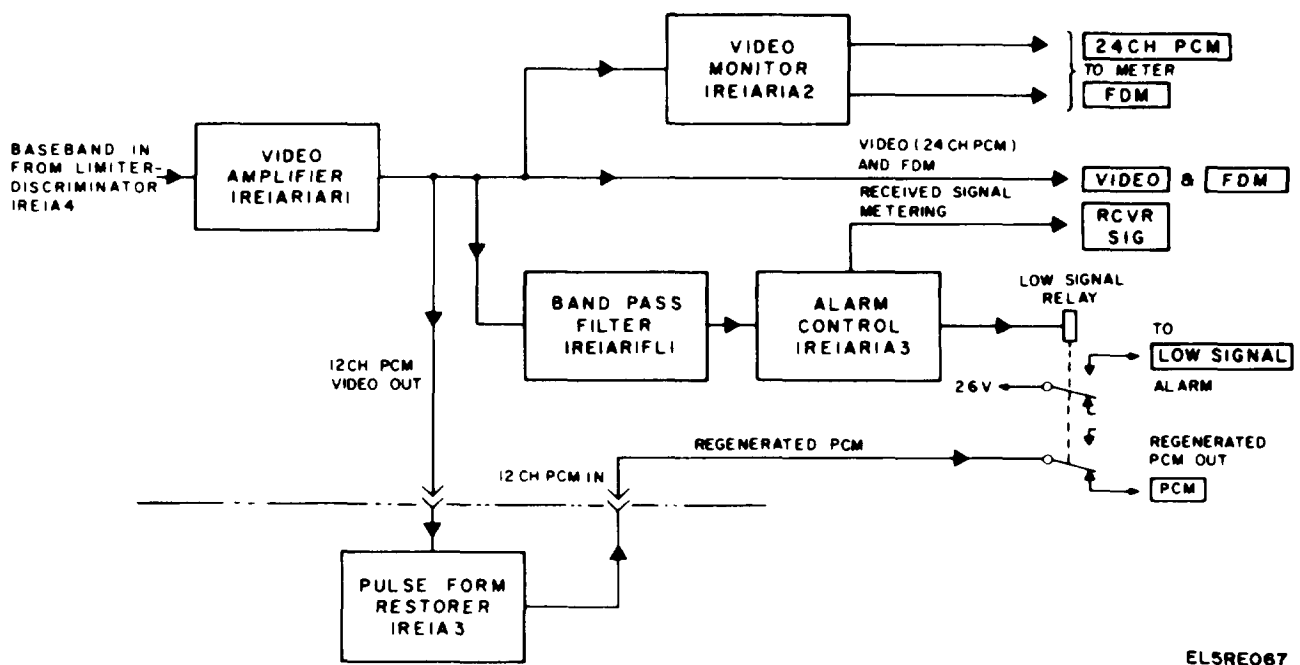


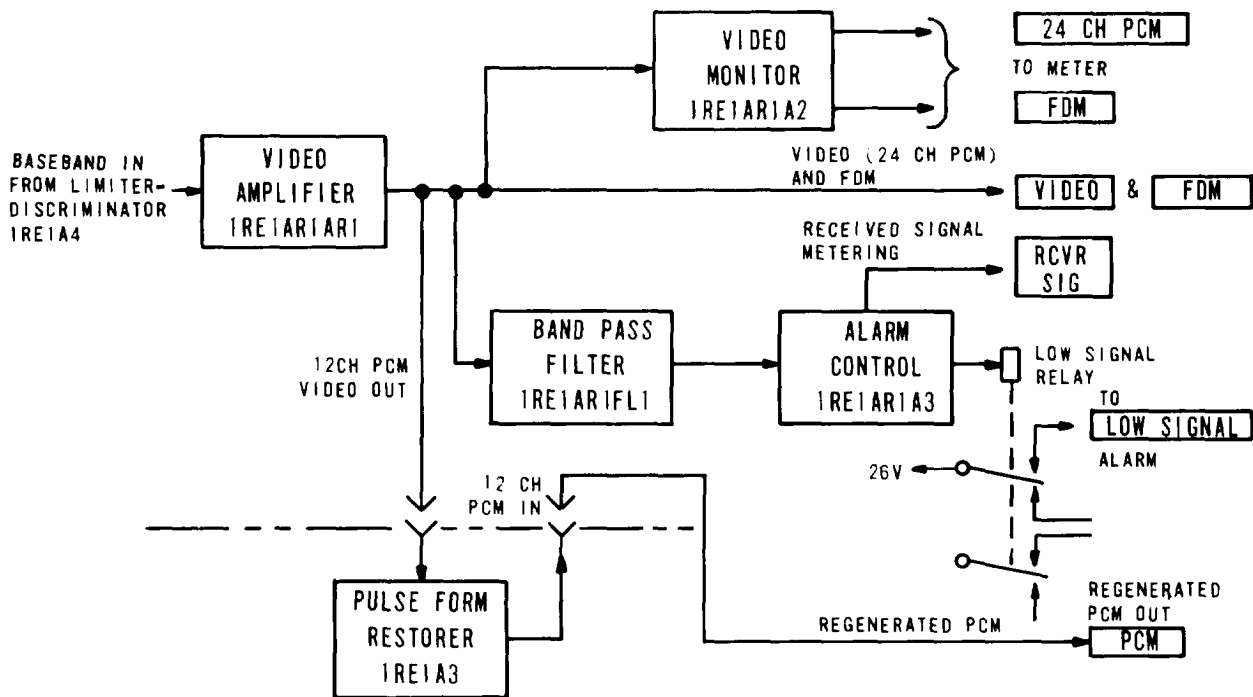
Figure 2-67. Video Amplifier 1RE1AR1 (Part No. CMC 455-975) (SM-C-698003), Block Diagram.

b. Block Diagram Analysis (Fig. 2-67 and 2-68 ) The input to video amplifier 1RE1AR1 can be either 12-channel pcm at 180 mv peak-to-peak, 24-channel pcm at 300 mv peak-to-peak, or fdm at 26 mv rms, depending on the type of traffic in use. The incoming signals from electrical frequency limiter-discriminator 1RE1A4 are coupled through a potentiometer and buffer amplifier Q1 to low pass filter FL1. The potentiometer adjusts the level of the incoming signals applied to the buffer amplifier. The buffer amplifier provides impedance matching between electrical frequency limiter-discriminator 1RE1A4 and the low pass filter. The FL1 low pass filter shapes the video signals in a gaussian response curve which is 3 db down at 400 kHz and 17.5 db down at 960 kHz. The signal at the output of the filter is then amplified in a three-stage cascade amplifier Q2, Q3, Q4, with an emitter-follower output stage. Overall feedback extends the amplifier frequency response to about 5 MHz to insure that all response shaping is accomplished in low pass filter FL1. The gain of the amplifier is 100. The output of the emitter-follower is applied to a cascade emitter-follower stage, Q5 and Q6, which produces a high-level output signal into a low impedance load.

(1) The signal at the output of the cascade emitter-follower stage is distributed as follows:

(a) To the receiver case for connecton to the VIDEO and FDM output connectors for distribution to multiplex equipment.

(b) To pulse form restorer 1RE1A3 for PCM regeneration and order wire recovery.



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Figure 2-68. Video Amplifier 1RE1AR1 (Part No. CMC-455-975-2) (SM-C-967354), Block Diagram.

(c) Through high pass filter 1RE1AR1FL1 to alarm control 1RE1AR1A3 for noise monitoring.

(d) To video monitor 1RE1AR1A2 for video signal metering.

(2) The video signal at the output of Q5-Q6 is coupled through a potentiometer to the buffer amplifier in 1RE1AR1FL1 which provides impedance matching between the wideband amplifier and the high pass filter. The potentiometer is used to adjust the operating point of the low signal alarm circuit. High pass filter FL1 selects a band of high-frequency noise in the range of 520 kHz to 2 MHz and attenuates all frequencies below 500 kHz. The noise signal is then amplified in a three-stage cascade amplifier, Q1, Q2, and Q3 (with a gain of 100) to a level suitable for noise monitoring. The amplified noise signal is then fed to wideband transformer T1 and a bridge rectifier CR1 through CR4. The dc output of the bridge rectifier is used to control Schmitt trigger circuit Q4-Q5 with a snap action, turn-on turn-off operation. The Schmitt trigger circuit is used to control the current through the low signal alarm relay.

(3) During normal operating condition, the relay is de-energized and the regenerated pcm signal from pulse form restorer 1RE1A3 is routed (in video amplifier SM-C-698003) through a pair of normally-closed contacts to the pcm output connector on the receiver case. Under high noise conditions the relay is energized and squelches the regenerated pcm while another pair of contacts provides the LOW SIGNAL alarm. In video amplifier SM-C-967354, the regenerated pcm signal bypasses this relay.

(4) The video signal for metering is amplified in a two-stage amplifier, Q1 and Q2, then rectified by CR1 and CR2 to produce a dc signal suitable for metering the 24-channel pcm and fdm signal levels. Series thermistors provide temperature compensation. The signal is then made available through separate meter calibrating resistors to the 24 CH PCM and FDM metering positions. A separate metering circuit selects a portion of the agc voltage from 1RE1AR2 (through 1RE1A4) and applies it to the meter in the RCVR SIG position.

c Detailed Circuit Analysis (FO-4-24) The incoming video signal is connected through J1 pin A1 to terminal E1 of video amplifier 1RE1AR1AR1, then through R1 to the base of buffer amplifier Q1. R1 adjusts the level of the input signal to the base of Q1. The output at the collector of Q1 is then coupled through C3 to low pass filter FL1 for final shaping. The output of the filter is amplified in Q2 and Q3, then applied to the base of emitter follower Q4. C8 prevents any tendency for spurious oscillation in Q2. The output at the emitter of Q4 is connected to the base of Q5; Q5 and Q6 are connected as a cascade emitter-follower across the +12 v and -12 vdc lines such that their output signal can be nearly 12 v peak-to-peak, if required, into a very low impedance load. This output signal is then coupled through C13 directly to high pass filter 1RE1AR1FL1 and video monitor 1RE1AR1A2. A portion of the output signal is fed through R15 and P1-9 to pulse form restorer 1RE1A3 and through R17 and P1-24 to receiver case 1A2. Negative feedback taken from the output signal is coupled through R9 and C7 to the emitter of Q2.

(1) The signal fed into high pass filter 1RE1AR1FL1 is applied through R1 to the base of Q1, which operates as a buffer amplifier to match the output signal to bandpass filter FL1. FL1 selects the noise components lying between 520 kHz and 2 MHz. This noise is then fed directly to the base of Q1 of alarm control 1RE1AR1A3.

Q1, Q2 and Q3 amplify the noise signal and apply it to the primary winding 3-4 of broadband transformer T1. Negative feedback from the Q3 emitter is coupled through R7 and C3 to the emitter of Q1 to stabilize the amplifier gain and extend the frequency response. The output at the secondary winding 1-2 of T1 is fed to bridge rectifier CR1 through CR4, and the resultant dc voltage, proportional to the noise level, is then connected to the base of Q5. Normally Q5 base is held at about -0.6 v by CR5 and R10 and Q5 is therefore cut off. When the voltage at the rectifier output raises this voltage to +0.7 v, Q5 starts to conduct. This causes the base of Q4, a PNP transistor, to go negative and drive it into conduction. Q4 emitter-collector current flows through low signal alarm relay K1, causing it to operate. When K1 is energized, 26 vdc at P1-5 is connected to the LOW SIGNAL alarm lamp on the front panel; at the same time another pair of relay contacts breaks the regenerated pcm output path, terminating the regenerated pcm output signal into 91 ohm resistor R17.

NOTE

Video Amplifier 1RE1AR1, Part No. CMC 455-975-2 (SM-C-967354) (fig. 2-68 and FO-4-25) has the regenerated pcm output routed directly to P1 pin 11. PCM OUT is not affected with operation of relay K1.

CR7 is a protection diode for Q4. Unstable or intermittent operation of Q1 is prevented, since the noise-generated dc signal at the output of CR1 through CR4 has to overcome a bias voltage.

(2) The input at video monitor 1RE1AR1A2 is coupled through C1 to the base of Q1 amplifier. The amplified signal at the collector of Q1 is applied directly to the base of emitter-follower Q2. The signal at the emitter of Q2 is applied to a voltage doubler rectifier circuit: C3, CR1, CR2, C4 and R5; L1 prevents spurious oscillations in Q2. The resulting dc signal is fed through thermistors R10 and R11 which stabilize the metering circuit against temperature variations. R7 and R9 adjust the level of the 24-channel pcm signal metering voltage; R6 and R8 adjust the level of the fdm signal metering voltage.

(3) Receiver signal metering voltage (RCVR SIG) is derived from voltage divider R14, R15, R16 and CR6, connected across the -12 vdc supply and ground. This voltage is applied to the positive side of the front panel meter in the RCVR SIG position while the agc voltage, filtered by L2 and C14 in video amplifier 1RE1AR1A1, is applied to the negative side. This arrangement is necessary because the agc voltage is negative and directly proportional to the received signal level.

2-47. Pulse Form Restorer 1RE1A3 (CMC Part No. 245-455624-000 (SM-D-698146) Fitted in Receiver, Radio R-1329, R-1329A, and R-1329B)

a. General. Since the original 12-channel pcm pulse train suffers a certain amount of distortion during transmission over the radio system, the pulses must be regenerated to their ideal shape in order to obtain a distortion-free signal at the multiplex equipment. Pulse form restorer 1RE1A3 performs the following major functions:

(1) Generates timing pulses to retime the relative pulse positions, and synchronize the multiplex to pulse form restorer 1RE1A3.

(2) Regenerates the original distorted pulses and forms new pulses, perfectly square and free from noise.

(3) Recovers the order wire signal from the combined order wire and pcm video signal.

(a) Pulse form restorer 1RE1A3 is not used when the AN/GRC-103 is carrying 24-channel pcm traffic, its functions being taken over by an external 24-channel combiner. The recovered order wire signal however is brought back into the pulse form restorer for distribution to the order wire unit.

(b) Order wire recovery also takes place in the pulse form restorer when the AN/GRC-103 is carrying fdm traffic.

b. Block Diagram Analysis (FO-4-20). The input to pulse form restorer 1RE1A3 is the composite order wire/pcm signal from video amplifier 1RE1A1, a 1.0 volt peak-to-peak train of gaussian-filtered video pulses riding upon an order wire signal of 0.25 volt peak-to-peak. The pcm video train is not modulated with the order wire signal; the pulse train baseline and peak voltages vary simultaneously at the audio rate of the order wire signal.

(1) This input signal is applied first to two-stage amplifier Q1 and Q2 of electrical synchronizer 1RE1A3A3 having an emitter-follower output. Here the signal is split, one output being fed to the clamp circuit, CR1 and CR2, and the other to a 150 kHz low pass filter of the order wire recovery circuits, (modulation eliminator 1RE1A3A1). The double-diode clamp circuit sets up a reference dc voltage at the base of input transistor Q3 of the amplifier/slicer circuit. This is done to remove the order wire component from the signal and to permit slicer triggering near the center of each pcm pulse.

(2) Differential amplifier slicer circuit Q3 and Q6 slices the pcm pulse train, amplifying a small portion of each pcm pulse to sharpen the leading and trailing edges. The SLICER LEVEL control at the base of the second half of the slicer is adjusted to a point on the pulse near the triggered operating point of the input side to insure that only a small portion of each pulse is amplified in the differential amplifier Q4 and Q5. The differential amplifier produces two antiphase outputs. The two antiphase outputs are split; one pair is fed to the differentiators/adder circuit and the other pair is fed to the dual gate Q5, Q2 in pulse form restorer 1RE1A3A2.

(3) The two antiphase pcm trains from the differential amplifier are applied through two differentiators to adder circuit CR3 and CR4. one differentiator produces a sharp spike at each transition of the upright pcm signal and the other produces a spike at each transition of the inverted pcm signal. The adder diodes then remove the positive-going spikes, leaving a combined train of negative spikes, each spike representing a transition of the incoming pcm signal. These spikes are then applied to one side of bistable multivibrator Q7 and Q8. The multivibrator is alternately triggered by spikes from the adder circuit and by negative spikes from timing oscillator circuit Q8 and Q9, of pulse form restorer 1RE1A3A2. The output from the multivibrator is a train of square wave pulses at twice the frequency of the incoming pcm pulses. The width of these pulses represents the relative phase of the basic incoming pcm pulse rate and the timing oscillator frequency. These pulses are then fed through amplifier Q9 and an integrator circuit which will generate saw-tooth pulses whose amplitude will depend upon pulse width and, therefore, upon the relative phase of the incoming pcm rate and the timing oscillator frequency.

(4) The sawtooth pulses are peak detected to produce a dc signal which very nearly equals the peak voltage of the sawtooth. The resulting voltage is then amplified in differential dc amplifier Q10 and Q11 in pulse form restorer 1RE1A3A2 before being applied to control varactor CR5 in the timing oscillator circuit.

(5) The timing oscillator consists of a free-running multivibrator, Q8 and Q9, which has a crystal and varactor in series in the feedback loop. The crystal Y1 frequency is 575.9 kHz; the varactor is used to pull its frequency to a nominal 576 kHz. The dc controlling voltage produced from the incoming pulse train is then used to control the timing oscillator over narrow limits (about 40 Hz) and lock it to the pulse rate of the incoming pcm. One output of the timing oscillator is fed through a differentiator to bistable multivibrator Q7 and Q8 of electrical synchronizer 1RE1A3A3 in the frequency control loop. A second output is fed through a differentiator to timing output amplifier Q7.

(6) The spike output of the oscillator is fed through a two-stage amplifier, Q7 and Q6, which removes the negative spikes produced in the oscillator, and adjusts the level of the positive-going spikes to 2.0 volt. Output stage Q6 is an emitter-follower to match the output source impedance to the 91 ohm load. A second output is taken from the first stage of the output amplifier to dual gate Q5 and Q2.

(7) The timing pulses will pass through the dual gate in the presence of anti-phase pcm signals. Thus, one timing pulse will pass through one side of the gate in the presence of each incoming positive pcm pulse, and one will pass through the other side of the gate in the presence of each incoming negative pcm pulse. The two outputs of the dual gate are fed to gated multivibrator Q3 and Q4.

(8) The positive-going timing pulses through the dual gate are used to trigger the multivibrator to produce the regenerated pcm signal. The output of the multivibrator consists of pulses whose leading edges correspond to the leading edge of the first timing pulse in the presence of a pcm pulse and whose trailing edges correspond to the leading edge of the first timing pulse to occur when no pcm is present. The regenerated pcm is delayed by approximately 1/2 bit but has none of the distortion and noise of the received pcm video. The multivibrator produces two antiphase outputs. One output is amplified in Q1 and the resulting 2.0 volts peak-to-peak pulse in a 91 ohm load is fed to the pcm output connector. The other output is fed to the order wire recovery circuits in modulation eliminator 1RE1A3A1. This output also feeds a pcm level metering circuit. When the AN/GRC-103 is used in the fdm mode, the timing oscillator runs free, producing timing pulses which could cause noise on order wire or fdm channels. The timing pulses are inhibited by Zener diode CR7 connected in a voltage divider between the -12 volt dc supply and ground. One resistor in the voltage divider is the external 91 ohm terminating resistance. When the 91 ohm load is not connected, due to the radio set being connected to operate in the fdm mode or the 24-channel pcm mode, the -12 volt dc is fed back through the 6.8 v Zener to timing output amplifier Q7, cutting it off. This action also prevents the pcm regenerator gate and gated multi vibrator from operating.

(9) The order wire recovery circuits are contained in modulation eliminator 1RE1A3A1. The second regenerated pcm output of the gated multivibrator is fed to buffer amplifier Q1. The incoming composite signal (inverted in amplifier Q1 and Q2 in electrical synchronizer 1RE1A3A2) is fed to a 150 kHz low pass filter, R2, C3 and L1, and emitter-follower Q2. This signal is applied to positive and negative peak detectors CR1 and CR2, and then to antiphase limiter Q3 and Q4. Q3 and Q4 limit the level of the regenerated pcm signal to equal the level of the pcm pulses of the in-

coming composite signal. The composite signal is applied to one side of cancellation potentiometer R11, and the level controlled regenerated pcm is fed to the other side. When this PCM CANCEL control is correctly adjusted, the two antiphase signals cancel, leaving only the order wire component to be fed to order wire amplifier Q6.

(10) An equalizer, C10, R12 and R24, introduces a controlled amount of distortion in the regenerated pcm signal, equal to the distortion present in the incoming pcm signal. The amount of delay introduced is adjusted by OW NOISE control R24.

(11) The output of the order wire amplifier is fed through a 3 kHz low pass filter, C12 and L5. The output of the low pass filter is split; one output is fed through order wire relay contacts K1 to the OW output connector, the other is fed to the order wire metering circuit, (J7, CR3 and CR4).

(12) When the AN/GRC-103 is operating in the fdm mode, it is possible for the slicer to trigger on modulation peaks and generate noise which could interfere with the fdm or order wire channels. To prevent this, the voltage at the negative peak detector is used to turn on control transistor Q5, which then clamps one side of slicer circuit Q6 in electrical synchronizer 1RE1A3A3. The control transistor will be turned on, since there will be no incoming signal to generate a negative voltage at the peak detector. Clamping of the slicer circuit in this manner will prevent the amplification of any spurious input signals.

c. Detailed Circuit Analysis (F0-4-21). The composite order wire/pcm signal from P1-7 is fed into electrical synchronizer 1RE1A3A3 and coupled through C1 to the base of Q1. The amplified signal at Q1 collector is connected directly to the base of Q2, an emitter-follower. The output signal from Q2 is split, one output being used for pcm regeneration, the other for order wire recovery. The output used for the recovery of the order wire is fed through E4 to terminal E3 of modulation eliminator 1RE1A3A1. The output used for pcm regeneration is coupled through C2 to double-diode clamp circuit CR1, C3, R6, CR2, C4 and R7.

(1) C2 attenuates the order wire signals while CR1 and CR2 generate positive and negative dc voltages at C3 and C4 respectively. These voltages will be equal if the peak positive and negative excursions of the pcm at Q3 base are equal, relative to the zero volt line. If the positive excursions are greater than the negative excursions, the voltage across R6 will be greater than the voltage across R7. Since R6 and R7 are of equal resistance, this will cause a net positive current to flow out of C2, causing the dc voltage at Q3 base to change until the positive and negative voltage excursions relative to ground are equal.

(2) Transistor pairs Q3 and Q4, and Q6 and Q5 are connected in the alpha configuration, in which each pair can be considered as a single very high-gain transistor. These transistor pairs are connected at their emitters to a single resistor R10, the whole circuit operating as a differential dc amplifier.

(3) The pcm signal applied to Q3 base is centered at zero volts dc by the clamp circuit. The differential amplifier, or slicer response is also centered at zero volts dc by adjustment of SLICER LEVEL control R13; this eliminates the circuit imbalance due to the tolerances of base/emitter voltages of Q3, Q4, Q5 and Q6. The outputs at E5 and E6 are each an amplification of the voltage difference between the Q3 base and the Q6 base. Since the pcm input at the Q3 base is much greater than the input range of the slicer circuit, the signals at the Q4 and Q5 collectors are squared-up versions of the input pulses. The signals at the Q4 and Q5 collectors

are antiphase pcm trains. Each has two outputs, one pair of outputs going through Q5 and E6 to pcm regeneration circuits on pulse form restorer 1RE1A3A2, and the other pair of outputs going to two differentiator circuits. The differentiators, C5 and R15, and C6 and R16, produce spikes at each transition of the pulses. CR3 and CR4 then clip off the positive spikes, leaving a train of negative-going spikes at their common output. Each spike represents one transition of the incoming pcm signal.

(4) These negative spikes are applied to the base of Q7, one half of a bistable multivibrator. Negative timing pulses from the timing oscillator in pulse form restorer 1RE1A3A2 are applied to the base of Q8, the other half of the multivibrator. Triggering of the multivibrator in this manner produces a train of pulses at the Q8 collector whose leading edges correspond to zero crossing of the original pcm pulses and whose trailing edges correspond to zero crossings of the timing oscillator pulses.

(5) The pulse rate is twice the pulse rate of the original pcm train; the pulse width is a function of the difference in time between the zero crossing of the pcm train, and the zero crossing of the next timing pulse. The signal at the collector of Q8 is applied through R24 to the base of amplifier Q9; the collector output of Q9 is fed to an integrator circuit, R26, R27 and C7, which converts the video pulses into sawtooth shape pulses. The peak amplitude of these pulses is proportional to the width of video pulses and therefore is a function of the difference in frequency between pcm pulses and timing oscillator pulses. PCM SYNC control R26 adjusts the nominal sawtooth peak voltage to synchronize the timing oscillator to the pcm signal. The sawtooth voltage is then fed to the base of Q10; R28 and C8, a peak detector circuit at the emitter of Q10, produces a dc voltage whose level is a function of the amplitude of the sawtooth signal applied to the Q10 base. The time constant of R28 and C8 is sufficiently long for very little change in dc voltage to take place even in relatively long periods between incoming pcm pulses. This dc voltage is connected through E10 to E9 of pulse form restorer 1RE1A3A2 and applied to the base of Q11. Q11 and Q10 form an emitter-coupled dc amplifier. Reference voltage applied to the base of Q10 is derived from the +12 v line by voltage divider R27 and R28. The input voltage to the base of Q11 is a function of the difference in phase of the timing oscillator with respect to the zero crossings of the pcm video train. The output dc voltage at the Q10 collector is filtered by C11, L3 and L2, and then used to control the capacity of varactor CR5 in the timing oscillator circuit. CR5 is in series with 575.9 kHz crystal Y1. These two components form the frequency controlling element in the feedback loop of free-running multivibrator Q8 and Q9. Normal bias on the varactor will pull the crystal frequency to a nominal 575 kHz. Any deviation from this frequency of the incoming pcm pulse rate will shift the time relation of the two signals at the bases of bistable multivibrator Q7, and Q8 on electrical synchronizer 1RE1A3A3. This shift will cause a change in output pulse width and sawtooth amplitude. The change in sawtooth amplitude results in a change of dc bias on CR5. This will change CR5 capacity and pull the crystal frequency into exact phase lock with the incoming pcm pulse rate frequency. One output of the timing oscillator is differentiated in C10 and R23 in electrical synchronizer 1RE1A3A3 and passed through CR5 to the bistable multivibrator. CR5 removes the positive spikes. The resulting train of negative-going timing pulses is fed to the base of Q8 of bistable multivibrator circuit Q8 and Q7 for gating.

(6) A second output of the timing oscillator (Q9 collector) is differentiated by R26 and C8, and the train of positive and negative timing pulses is amplified in Q7.



(7) CR3 at Q7 collector removes the negative spikes, leaving the positive spikes to be passed through R19 to the base of emitter-follower Q6. The 2.0 volt peak-to-peak signal at the Q6 emitter is coupled through C6 to P1-15., the timing output connection. The second output at the Q7 collector is applied through R16 to the collectors of a dual gate consisting of Q2 and Q5.

(8) The shaped antiphase pcm pulse trains at the collectors of amplifier-slicer Q4 and Q5 in electrical synchronizer 1RE1A3A3 are applied through R14 and R6 to the bases of dual gate circuit Q2 and Q5 in pulse form restorer 1RE1A3AZ. Q2 and Q5 operate in conjunction with Q3 and Q4 bistable multivibrator in which the actual pcm regeneration takes place. The train of positive-going timing pulses derived from the timing oscillator is applied through R16 simultaneously to the collectors of Q2 and Q5. Q5 and Q2 are so biased that each transistor will conduct a timing pulse when the pcm at Q3 is negative or positive respectively. The sliced pcm pulses applied to the base of Q5 make Q5 conduct for the duration of the pcm pulse. The first positive timing pulse appearing at the emitter of Q5 (Q5 conducting), switches Q2 on and simultaneously, by multivibrator action, switches Q3 off. A positive pulse, for the duration of the pcm pulse and delayed by 1/2 bit, appears at the collector of Q3. Q2 stays switched off until a positive pulse appears at the base of Q2 making Q2 conduct. The first positive timing pulse to appear at the emitter of Q2 switches Q3 on and simultaneously switches Q4 off. A positive pulse appears at the collector of Q4, delayed by 1/2 bit, and remains positive for the duration of the interval between pcm pulses, or until the next positive-going timing pulse at the emitter of Q5 switches Q3 off. The action continues in this manner regenerating a train of pulses which represents the incoming pcm train. This new pulse train will be delayed by one-half pulse but since it is synchronized by the timing output pulses the delay has no effect on multiplexer operation. Inverted regenerated pcm pulses are fed from the Q4 collector through R4 to the base of output amplifier Q1. The signal at the Q1 collector, -2 v peak-to-peak in 91 ohms, is connected through E2 to P1-13. Upright regenerated pcm pulses from the Q3 collector are fed through R5 and C2 to a metering detector, CR1 and CR2. The rectified dc is fed through R1 and E11 to P1-9. A second output from the Q3 collector is connected through E5 to the order wire recovery circuits on modulation eliminator 1RE1A3A1.

(9) A 6.8 v Zener diode CR7 provides protection against spurious operation during the fdm mode of operation, which could cause noise to be induced into order wire circuits. In normal pcm operation, a 91 ohm termination resistor is externally connected between P1-13 and ground. This resistor, along with R2, forms a voltage divider between -12 volts and ground. The voltage at the CR7 cathode is not high enough to fire the Zener. In the fdm or 24-channel pcm modes of operation, however, the external termination is not connected, so the CR7 cathode rises to about -12 volts. The Zener passes about 5.2 volts through L1 to the Q7 collector, effectively removing all timing pulses. The absence of timing pulses at the collectors of the Q2-Q5 gate circuit causes gated multivibrator Q3 and Q4 to be inoperative.

(10) The order wire circuits on modulation eliminator 1RE1A3A1 perform their functions by cancellation of the pcm pulses within the composite signal. The inverted composite signal (amplified) at the Q2 emitter of electrical synchronizer 1RE1A3A3 is fed through E4 to E3 in modulation eliminator 1RE1A3A1 and applied through R2 to low pass filter L1 and C3. This filter removes all high frequency noise components above 150 kHz and single bits of pcm of the composite order wire/pcm input signal before being applied in the base of Q2. Q2 passes the order wire/pcm composite signal at an impedance level suitable for peak detection and pcm cancellation,

and also prevents peak detector voltages from getting into the low pass filter circuit. The output at the Q2 emitter is coupled through L4, C5 and R10 to one side of PCM CANCEL potentiometer R11. The composite signal at the Q2 emitter is also coupled through C6 to positive peak detector CR1, C7 and R4, and to negative peak detector CR2, C9 and R6. CR1 and C7 clamp the base voltage of Q3 to a peak positive pcm signal level; CR2 and C9 clamp the base voltage of Q4 to a peak negative pcm signal level.

(11) Upright regenerated pcm from the collector output of Q3 (pulse form restorer 1RE1A3A2) is brought in through E2 and applied to the base of emitter-follower Q1. The output of Q1 is then coupled through C2 to the emitters of Q3 and Q4 which effectively clamp the level of the regenerated pcm to the level of the composite pcm pulse amplitude. The level controlled regenerated pcm is then coupled through C10 to the other side of PCM CANCEL potentiometer R11. When resistor R11 is correctly adjusted, the two opposite pcm signals will cancel, leaving only order wire signal components. C10, R12 and R24 form a phase-shifting network that introduces a low-frequency phase shift into the regenerated pcm equal to that introduced by the system. This technique eliminates any order wire noise component caused by an unequal low-frequency phase shift. R24, the OW NOISE control, adjusts the amount of shift required to equalize the delay in the incoming signal.

(12) The level of the order wire signal is adjusted by OW GAIN resistor R13, before being amplified by amplifier Q6. C11 attenuates any remaining high frequency components in the order wire signal. The amplified signal at the Q6 collector passes through 3 kHz low pass filter L5, and C12 to E10 and relay contacts A3-A2 to P1-14 for connection to the order wire unit. Some of the signal from L5 is applied through R17 to the base of Q7. The amplified signal at Q7 collector is connected through C14 to metering detector circuit CR3 and CR4. The resulting dc is then connected through R23 and E9 to P1-10.

(13) When the AN/GRC-103(V) operates in the fdm mode, the order wire signals are passed through the path of the composite order wire/pcm signal, passing through low pass filter C3 and L1, amplifier Q2, and one side of the PCM CANCEL potentiometer to amplifier Q6 and so on.

(14) In the fdm mode of operation it is essential that the pcm regenerator be squelched, since there is no incoming pcm to cancel the regenerated pulses which could be caused by noise peaks triggering the slicer. In the 12-channel pcm mode of operation, Q5 in modulation eliminator 1RE1A3A1 is held at cut-off by the negative peak detector voltage on its base and so it has no effect on Q6 in the amplifier slicer circuit in electrical synchronizer 1RE1A3A3. With no incoming pcm this bias is removed, permitting it to conduct and cause a drop in voltage at the Q6 base. This cuts off Q6, in turn cutting off Q5 and Q4, and prevents the amplifier circuit from operating.

(15) When the system is carrying 24-channel pcm, the order wire recovery takes place in the combiner unit.

(16) The recovered order wire signal at a level of -4 dbm is connected through P1-3 and E7 to attenuator R21 and R22. A signal from the multiplex combiner unit is connected through P1-24 to order wire relay K1 energizing it. The order wire signal, now at -10 dbm, is connected through A1 and A2 contacts of K1 to P1-14 for connection to the order wire unit.

2-48. Pulse Form Restorer 1RE1A3 (CMC Part No. 245-803110-000 (SM-D-990510)  
 Fitted in Receiver, Radio R-1329C)

a. General. Since the original 12 or 24 channel pulse train suffers a certain amount of distortion during transmission over the radio system the pulses must be regenerated to their ideal shape in order to obtain a distortion free signal for the multiplex equipment. Pulse form restorer 1RE1A3 (Part No. 245-803110-000) performs the following major functions:

(1) Generates timing pulses to retime the pcm stream and to synchronize external multiplexer with itself.

(2) Regenerates the incoming distorted pulses to form new pulses that are perfectly square and free from noise.

(3) Recovers the order wire signal from the combined order wire and pcm video signal. Order wire recovery also takes place in the pulse form restorer when the AN/GRC-103 is carrying fdm traffic.

b. Block Diagram Analysis, General Circuit Description (FO-4-20.1). The input to the pulse form restorer is the composite order wire/pcm signal from VIDEO AMPLIFIER 1RE1AR1: a 1.4 volt (2.3 volts for the biternary signal of 1152 kb/s) peak-to-peak train of gaussian-filtered video pulses riding upon an order wire signal of 0.345 volts peak-to-peak. The pcm video train is not modulated with the order wire signal. The pulse train baseline and peak voltages vary simultaneously at the audio rate of the order wire signal. The pulse form restorer is composed of four principal circuits each mounted on a separate board inside the case. In addition there is a voltage regulator mounted externally on the case. The four circuits that comprise the pulse form restorer are:

| Board name                        | Board prefix |
|-----------------------------------|--------------|
| Pulse form restorer . . . . .     | A2           |
| Modulation eliminator . . . . .   | A1           |
| Electrical synchronizer . . . . . | A4           |
| Electrical interface . . . . .    | A3           |

(1) Pulse form restorer board.

(a) This portion of the pulse form restorer receives the video input signal first. The signal is applied to buffer-amplifier U13 and then to the lowpass filter which slightly modifies the shape of the pcm pulses. Next the filtered signal passes through the double diode clamp which removes the order wire prior to pcm regeneration. The pcm stream, now without the order wire, is passed on to the peak detector circuitry.

(b) The positive and negative peak voltages from the peak detectors are sensed by a resistive divider, which uses them to set the decision threshold for both the three-level and binary slicers. The output of the three-level slicer is then decoded and both this decoded signal and the output of the binary slicer are fed into pcm selector U10. U10 is a multiplexer used to select one of the two possible signals depending upon the operating mode of the unit. The decision is made according to the state of the COMBINER CONTROL input as reflected in the output signal of gate U1B on the electrical interface board. A "0" indicates the binary mode of 288/576 kb/s while a "1" represents the biternary mode of 1152 kb/s.

(c) The output of the pcm selector is re-timed by U9A and then fed to the output interface which acts as a buffer-amplifier. Associated with the output of the pcm stream is a peak detecting meter. The timing logic circuit consists in part of U6C, with the remainder being on the electrical synchronizer board, and aids in the regeneration of the pcm's timing signal. In addition, U1 and U5D form a level detector which measures the peak-to-peak voltage of the pcm. If this voltage falls below 37% of its expected level, the level detector then sends a signal to the squelch logic causing pcm regeneration to be inhibited.

(d) Also on the pulse form restorer board are two selectable delays used to generate appropriately delayed pcm signals needed by the order wire recovery circuits located on the modulation eliminator board.

(2) Modulation eliminator board.

(a) This section of the pulse form restorer removes the pcm from the video signal and recovers the order wire. The composite video is fed through a delay filter and then to differential amplifier U1. The other input to this amplifier comes from the automatic level control (a/c) amplifier which generates a variable amplitude pcm signal under control of the correlator output in the mixer. The output of the differential amp is the video signal with its pcm component minimized. A portion of this processed video signal is fed back to the mixer. The mixer produces a dc signal with its pcm component minimized. A portion of this processed video signal is fed back to the mixer. The mixer produces a dc signal proportional to the correlation between the local pcm and the remaining pcm component in the video signal at the output of the differential amplifier. This dc signal is corrected and amplified by the loop filter and then fed to the alc amplifier where it controls the level of the pcm that is subtracted from the video. All of the above circuitry forms a feedback loop which subtracts from the video a pcm signal with an amplitude such that the residual pcm component is minimized.

(b) The output of the differential amp is also fed to a lowpass filter and then to the order wire amplifier which brings the order wire signal up to its correct output level. This filtered order wire signal travels via a resistive pad to the output, as well as to the order wire (OW) meter circuitry.

(3) Electrical synchronizer board.

(a) This section of the pulse form restorer receives binary and biternary threshold crossing information from the pulse form restorer board and uses the information to generate the appropriate timing frequencies of 576 and 1152 kb/s. Timing selector U9 is a multiplexer which is used to select between the two sets of signals depending upon the operating mode of the unit. The timing information is then fed to the transition pulse generator which produces sampling pulses of 200 ns width at each crossing of the pcm signal.

(b) A voltage controlled oscillator (vco) forms part of a feedback loop whose purpose is to synchronize the oscillator's output of 4608 kHz with the pcm signal. Divider U8 in conjunction with part of multiplexer U9 divides the vco output by either 4 or 8, for the biternary and binary modes respectively. The output of the divider splits into two paths, the first going to the integrator, sample and hold circuit, and loop filter; whose combined function is to analyze the phase difference between the vco and the pcm and then generate a proportional dc voltage. This dc voltage is in turn used to control the frequency of the vco thus minimizing the phase difference of the two signals. The other output from the divider goes to the phase adjust circuitry that is adjusted to ensure that the decoded pcm on the pulse form restorer board is sampled at the correct instant.

(c) The phase adjust circuitry also sends the corrected timing signal to the pulse generator U4A which produces timing pulses that have a width of 115 ns. Q9 and Q10 form the output interface circuit for this reshaped timing signal.

#### (4) Electrical interface board.

(a) The mode select logic, order wire routing, power supply filtering and squelch circuitry are on this board. The comparators (U2 and U3) in the mode and order wire select circuitry decode the state of the combiner control line. Both outputs go to gate U1B which determines the circuit operating mode (binary or biternary). The order wire select logic controls a relay which selects either the internal order wire, or external order wire attenuated by the 6 db pad.

(b) This board also contains the squelch logic which cuts in if the video input signal falls too low, or if the pcm output is unterminated as indicated by Q1 and Q2 in the termination detector. Either condition causes the output pcm and output timing to be turned off. It also automatically inhibits the pcm going to the modulation eliminator. These operating conditions are intended to inhibit pcm regeneration when there is no input signal or when the radio is being used for fdm traffic. In either case, the regenerated pcm would be meaningless and would hinder order wire recovery, which under these conditions would require only lowpass filtering.

#### c. Detailed Circuit Analysis (F0-4-21.1).

##### (1) Pulse form restorer (Board A2).

(a) Termination resistor R9 presents the proper impedance to the incoming signal from the video amplifier's output circuitry. The operational amplifier U13 and resistors R10 and R11 form a buffer amplifier to raise the input signal level by a gain factor of approximately three. The amplifier signal is then applied to an input filter (R12 and C1) which removes some of the input noise and modifies the shape of the pcm pulses. R13, Q1, R14, and R43 form an emitter-follower buffer which drives the subsequent clamping circuit (C2 - C5, CR1, CR2, R15 and R16) removes the order wire variations from the input video signal present at the emitter of Q1. If the signal rises above its average level, current flows through CR1 and into C4. C2 and C3 are thus charged up, which tends to counteract the upward shift of the video. If the signal drops below its average level, C2 and C3 are charged up in the opposite sense by current flowing through C5 and CR2. This tends to raise the level of the video signal. By this process the signal present at pin three of U12 has had most of the low frequency order wire variations removed. These order wire variations are removed so that they do not degrade the performance of the pcm recovery circuits. U12 is a unity gain buffer-amplifier for the video signal once it has been processed by the clamp circuitry. From here the video signal is fed, via the resistive divider R17 and R18, to both the peak detector and slicer circuits.

(b) There are two peak detectors; a positive and a negative. The positive peak detector comprises U8m Q2, U5A, R19 - R23, and C6. When the video signal at pin 3 of U8 exceeds the peak value at pin 2 of U8, Q2 is turned on and a current pulse raises the voltage on C6. The voltage raises until it reaches the peak of the video signal. This peak voltage is thus present at pin 1 of unity gain amplifier U5A.

(c) The negative peak detector consists of U7, Q3, U5B, R36 - R41, and C7. The negative peak voltage appears at pin 7 of U5B. When the video signal at pin 2 of U7 goes below the negative peak value at pin 3 of U7, Q3 turns on and a current pulse raises the voltage on C7. This voltage is inverted by U5B which also acts as a buffer. The voltage at pin 7 of U5B thus stays at the negative peak of the video signal.

(d) The video signal from the resistive divider (R17 and R18) also goes to the slicers. The slicers are comparators whose outputs are high (approx. 5 v) when the video signal level is higher than a reference voltage and low (approx. 0 v) otherwise. In U4, the output goes low when the video signal is greater than the reference voltage. The reference voltage is set by two resistive divider networks, R24 and R27 for the binary signal; and R25, R26 and R28 for the biternary signals. The binary slicer is composed of U2, while comparators U3 and U4 act as the two biternary slicers. Resistors R1, R3 and R4 equalize the resistances seen by the inverting and non-inverting pins of each comparator. This eliminates slicer offset errors caused by the input bias currents.

(e) The NAND gates U6A, U6B, and U6D form a decoder for the sliced biternary signal. The biternary signal has three levels. When this signal is high, it indicates that a "1" was sent; if it is low, a "0" was sent; and in the middle range it indicates that the signal changed from its value during the previous bit interval. (i.e., from a "1" to a "0" or vice versa). The decoder transforms the sliced three level biternary signal back to a binary form by logically analyzing the three levels. The sliced signal is re-timed by flip-flop U9A directly in the binary case, and after the decoder output of U6D in the biternary case. The signal present at input pin 2 of U9A also goes to test point

TP1 on the modulation eliminator board. In this position it is easily accessible with the cover of the unit still in place. Flip-flop U9B provides a further re-timing of the recovered pcm. This delayed signal is required by the modulation eliminator which will be discussed later. U10 is a quadruple multiplexer circuit which is used to select one of the two sets of signals depending upon the operating mode of the unit (i.e., either binary or biternary).

(f) U11 is an eight bit shift register. It is timed by the vco clock from the electrical synchronizer board and provides several delayed pcm signals for the modulation eliminator. The pulse form restorer also contains the pcm output driver circuitry. The pcm comes from pin eight of U5D on the electrical synchronizer board. The driver consists of Q4, Q5, and R44 - R48. Transistor Q4 is a common-emitter buffer which drives the saturating switch formed by Q5. When the collector of Q5 is loaded with a 91 ohm resistance, the output is either 0 volts or -2 volts, depending on whether Q5 is on or off. The emitter or buffer Q4 also drives the pcm metering circuit consisting of CR3, CR4, R49, R50, C11, and C23. C23 provides ac coupling while CR4 clamps the lower signal peak to ground. R49, CR3 and R50 form a peak detector. When this circuit is loaded with a 5 K ohm resistor, the output voltage is nominally 250 mv when the pcm signal is normal.

(g) This board also contains a squelch circuit comprising U1, U5D, R29 - R35, R42, C9, and C8. This circuit inhibits the pcm regeneration process when the video signal is absent. It accepts the positive and negative peak signals from U5A and U5B which are fed to the differential amplifier U5D, R29 - R31, and R42. The output at pin 14 of U5D is the peak-to-peak voltage of the video signal. This voltage is compared to a threshold by comparator U1. The threshold value is set by resistors R32 and R33. C8 removes any noise pickup. When the peak-to-peak video level drops below the threshold, the comparator turns on. R34, R35, and C9 form a delay filter so that the circuit ignores short interruptions. The circuit output goes to the squelch logic contained on the electrical interface board.

(h) Capacitors C10 and C12 through C22 provide power supply decoupling.

## (2) Modulation eliminator (Board A1).

(a) The inputs to the modulation eliminator board consist of a filtered video signal and several pcm signals with varying delays. The input video signal comes from the emitter of Q1 on the pulse form restorer board. It goes to a Bessel-type delay filter consisting of L1 - L3, C1 - C6, and R1 - R2. C5 and C6 remove the -0.7 vdc offset produced by the base-emitter drop of Q1.

(b) The video signal then goes to a subtraction amplifier consisting of U1, R3, R4, and R22. This circuit is a dual input, unity-gain, inverting feedback amplifier. One input is the delayed video signal via R2, while the other is the adjusted and inverted pcm signal from the feedback loop via R22, which when combined with the incoming video removes most of the latter's pcm content. The output of the subtraction amplifier goes to a correlator circuit, whose main component, U2, is a multiplier integrated circuit. The recovered pcm signal at E3 is correlated with the subtraction amplifier output. C7, C8, and C13 provide AC coupling while C10 - C12 and C14 remove noise and high frequency signal components from the bias points. R5 and C9 form a lowpass filter. R6, R7, R9 - R12 and R42 provide the input dc bias voltages required by U2. R8 sets the operating current of the multiplier while R13 sets the input to output gain. R14 and R15 set the output operating points. C15, C17, C18, and C32 filter the outputs at pins 6 and 9

of U2 to produce dc voltages at these points. The correlation output is the difference between the dc voltages at pins 6 and 9. The magnitude of this difference is dependent upon the amount of residual pcm content of the video signal at the output of U1. These two dc signals are therefore fed to a differential amplifier consisting of operational amplifier U4D and resistors R16 - R18 and R43. The output of the differential amplifier goes to a high gain inverting amplifier consisting of U4A, R19, R20, R21, C19, and C20. U4A is an operational amplifier. R19 and R20 set its gain at about 560. C19 and C20 provide further filtering of the correlator signal.

(c) The signal at pin 1 of U4A is a dc signal which controls the level of the locally regenerated pcm subtracted from the incoming video signal. The level is controlled in the alc amplifier consisting of Q1 - Q3, CR3, and R30 - R33. Q3, R30 and R33 form a current source the magnitude of which is set by the dc control voltage at the base of Q3. This voltage comes from the high gain amplifier U4A. Diode CR3 prevents this voltage from going positive by more than 0.7 volts. The current in the collector of Q3 is swithed between Q1 and Q2, thus creating pcm signals at the collectors of Q1 and Q2 whose magnitudes are controlled by the collector current in Q3 and the resistors R31 and R32. Q1 and Q2 are switched by pcm and inverse pcm signals from the pulse form restorer board which are applied to their bases.

(d) The pcm signals at the collectors of Q1 and Q2 have a dc component which is removed by the differential amplifier consisting of U3, R25 - R28, C23, and C24. U3 is an operational amplifier whose gain is set by R25 - R28; C23 and C24 performing part of the lowpass filtering of the pcm. The other portion of the pcm lowpass filter consists of R24, R29, C21, and C22. R29 is a potentiometer which is adjusted to minimize noise in the recovered order wire. Potentiometer R23 and capacitor C41 form a high pass filter which is intended to match the low frequency phase response which the video signal sees in passing through the radio transmitter and receiver. R23 is adjusted for minimum order wire noise. The output of the subtraction amplifier (pin 6 of U1) goes to a lowpass filter to remove the remaining high frequency noise components from the order wire signal. The filter is a third order Chebychev type with a ripple of 0.1 db and a 3 db bandwidth of 3.6 kHz. It is composed of amplifier U4C, resistors R34 - R36, and capacitors C25 - C29. The output of the filter goes to a buffer amplifier consisting of U4B, R41, and R37. This amplifier has a gain of 11 so that it can drive the order wire metering circuitry. The output of the amplifier (pin 7) drives the resistive pad R39 and R40, which when terminated by 600 ohms give the correct order wire output level. The amplifier output also goes to the pcm metering circuitry which consists of R38, CR1, CR2, and C30, in addition to C11 and R14 on the electrical interface board. CR1 and C30 clamp the negative order wire peaks to about -0.5 volts while CR2 and C11 detect and hold the positive peaks of the clamped order wire signal. C16, C31, and C33 - C40 provide power supply decoupling.

(3) Electrical synchronizer (Board A4).



(a) Transistors Q1 and Q2 with their associated components form the voltage control led oscillator (vco) of the phase-locked loop. Within this circuit, Q1 acts as an amplifier with R1 and R2 providing a bias of 2.7 volts to the base. The emitter voltage is thus about 2.0 volts. R6 is used to set up a bias current of 2 mA through the transistor with R4 and R5 providing a collector load of 500 ohms. L1 and C2 form a tuned circuit which prevents the vco from oscillating at the various harmonics of its base frequency. Transistor Q2 forms an emitter-follower buffer with drives the frequency selective network. C3 and C4 are dc blocking capacitors. R7, R8, and R27 are the dc bias network for the varactor diodes CR1 and CR2. The capacitance of the varactors varies with the dc control voltage (from pin 6 of U3) which in turn pulls the frequency of the oscillator. L2 and L4 compensate for the median capacitance of the varactors and ensure that the center frequency of the oscillator is equal to the crystal frequency. The crystal is an AT cut series resonant with a frequency of 4608 kHz. Inductor L3 turns out the capacitance of the crystal's case.

(b) The vco output at the collector of Q2 is amplified by the circuit comprising C5, C6, R11, CR3, and Q3. C5 is an ac coupling capacitor, C6 is a speed-up capacitor and CR3 keeps the transistor Q3 from being continually saturated. The output present at the collector of Q3 is a 0 to 5 volt signal compatible with the TTL circuits. All integrated circuits used in this unit are of the TTL variety.

(c) The amplified vco output at Q3 goes to quadruple multiplexer U9 which is used to select between the two sets of signals depending on whether the unit is operating in the binary or biternary mode. From U9, the vco output travels to the divider circuit U8, which divides the signal by either 4 or 8. This variable division is accomplished by connecting the input of the second divider stage to either the input or output of the first stage via one of the selectors of multiplexer U9. The signal at pin 8 of U8 is the clock, while the signal at pin 9 is twice the clock frequency.

(d) The variable phase shifter comprises U6A, U6B, U7A, U7B, R33 - R36, C16, and C17. This circuit adjust the delay of the re-timing clock which retimes the sliced video signal at pin 2 of U9A on the pulse form restorer board. This delay must be set to allow for optimum pcm regeneration. U7A is a monostable multivibrator with a variable pulse width set by potentiometer R36, fixed resistor R35, and C17. U7B is a monostable multivibrator with a fixed pulse width set by R33 and C16. Both monostable multivibrators are triggered by the doubled clock signal from pin 9 of U8. Each half cycle of the clock is thus re-timed twice; first by one multivibrator output and then by the other. This circuit arrangement allows for accurate adjustment of small time delays which might be less than the minimum achievable pulse width from one multivibrator acting alone. The clock signal at pin 8 of U6B is connected to TP1 to permit monitoring of the re-timing signal during the units alignment. This clock signal then goes to re-timing fiip-flop U9A on the pulse form restorer board.

(e) A phase shifted clock from pin 6 of U6A goes to the triangular wave generator used in the phase comparator. The triangular wave is generated by lowpass filtering a square wave. The square wave generator consists of Q7, Q8, CR9, R28, R29, C13, and C14. Q7 is a switching transistor which produces a 0 to 12 volt square wave. C13 is a speed-up capacitor. The combination of Q8 and Q7 is an emitter-follower buffer which acts as a low impedance driver for the lowpass filter-amplifier. The amplifier requires a low impedance drive for both low and high inputs to produce a symmetrical triangular wave. The triangular wave must have a very low offset and thus C14 is an ac coupling capacitor used to remove the dc offset from the amplifier input. The lowpass filter-amplifier consists of U1, C15, R30, R31, and R32. U1 is an operational amplifier connected in an inverting mode with input resistor R30 and feedback network R32 and C15. The effect of the filter is to integrate the square wave to produce the triangular shape.

(f) The triangular wave is sampled by narrow pulses occurring at the threshold crossing points of the sliced pcm. The threshold crossing information is generated on the pulse form restorer board. In the binary case the threshold crossing signal is the sliced video signal appearing at pin 7 of comparator U2. In the biternary case the outputs of the two slicers U3 and U4 are combined in gate U6C, the result appearing at pin 8. These two threshold crossing signals are sent to the selector circuit on the electrical synchronizer board. The appropriate signal is selected depending upon the operating mode (i.e., either binary or biternary). The selected signal appears at pin 4 of U9 and goes to pin 1 of U5A. The circuit comprising U5A, U5B, U5C, C7, C8, R13, R14, and R15 produces a narrow pulse on each input transition by an exclusive or function performed by gate U5C. U5A, U5B, R14, C7, and C8 produce a two stage delay which is necessary to achieve equal pulse widths on both positive and negative going transitions. The output pulse appears at pin 11 of U5C.

(g) The sampling switch is a MOSFET transistor (Q6), which is open when gate G is at +12 volts. Thus, the pulses coming out of U5C must be transformed to have a peak value of +12 volts and a baseline of -12 volts. This transformation is accomplished by the high speed drive circuit consisting of Q4, Q5, CR4, CR5, CR12, R16 - R20, C9, C10, and C27. Q4 produces 0 to 12 volt pulses while Q5 shifts the level into the -12 to +12 volts range. C9 and C10 are speed-up capacitors and CR4 and CR5 prevent saturation of Q4 and Q5 respectively, thus allowing for faster switching. CR12 prevents a reverse base-emitter voltage greater than 0.7 volts from appearing on Q5. C27 gives additional +12 volt power supply line decoupling. The sampling pulse drive appears at the collector of Q5 and drives the gate of Q6.

(h) Q6 samples the triangular wave while resistors R21, R22, and capacitor C1 provide averaging over many samples of the wave, the average value being held in C11. U2 is a very high input impedance voltage follower buffer. Its low input bias currents are required to avoid fast discharge of C11. The phase-locked loop can thus tolerate short interruptions of the video input signal.

(i) The output of U2 pin 6 goes to the loop filter of the phase-locked loop. This circuit consists of U3, CR6, CR7, CR8, CR10, C12, and R23 - R26. U3 is an operational amplifier connected in an Inverting mode. The filter time constants are set by R24, R26, and C12. CR6, CR7, and R23 produce a faster synchronization when the loop is out of lock. When the loop is locked, the signal at pin 6 of U2 is close to 0 volts, however, when it is unlocked it swings between the peaks of the triangular wave and overcomes the diode drops of CR6 and CR7. R23 then appears in parallel with R24 and the gain of the amplifier and hence the bandwidth of the phase-locked loop is increased. CR8 prevents saturation of the output stage of U3. CR10 prevents the output of U3 from going too far negative as this would turn the vco off. It should be noted that CR8 does this as well, but the forward drop of a zener diode is normally higher than that of a regular diode. The output at pin 6 of U3 is the vco control voltage.

(j) The timing output of the pulse form restorer consists of narrow pulses. These are produced by the monostable multivibrator U4A. It is triggered by the clock from pin 8 of U6B. The pulse width (nominally 115 ns) is determined by C18 and R37. The output at pin 4 of U4A goes to the output driver circuit consisting of Q9, Q10, C19 - C22, and R28 - R42. Q9 drives the emitter-follower output buffer of Q10 which when terminated in 91 ohms produces a 2 volt peak-to-peak ac coupled clock signal. C19 and C20 are speed-up capacitors. C21 controls the rise and fall times of the output timing signal. C22 provides ac coupling.

(k) This board also contains a pcm delay circuit which is needed to maintain proper timing relationships between the output pcm and the timing. This circuit consists of U5D, CR11, R43, R44, and C29. Gate U5D is a buffer for the pcm output driver, (Q4, Q5, etc. on the pulse form restorer board). The remaining circuitry assures correct delay times for positive and negative going transitions.

(l) Capacitors C23 - C26 provide power supply decoupling.

(4) Electrical interface (Board A3).

(a) The mode control circuitry consists of U2, U3, U1B, R1 - R5, and C7. The input at E16 can be either an open connection, ground, or a 1K ohm resistance to ground. These correspond to the operating modes as follows:

| Input             | Mode                                |
|-------------------|-------------------------------------|
| Open . . . . .    | Binary with internal order wire.    |
| Ground . . . . .  | Binary with external order wire.    |
| 1 K ohm . . . . . | Biternary with internal order wire. |

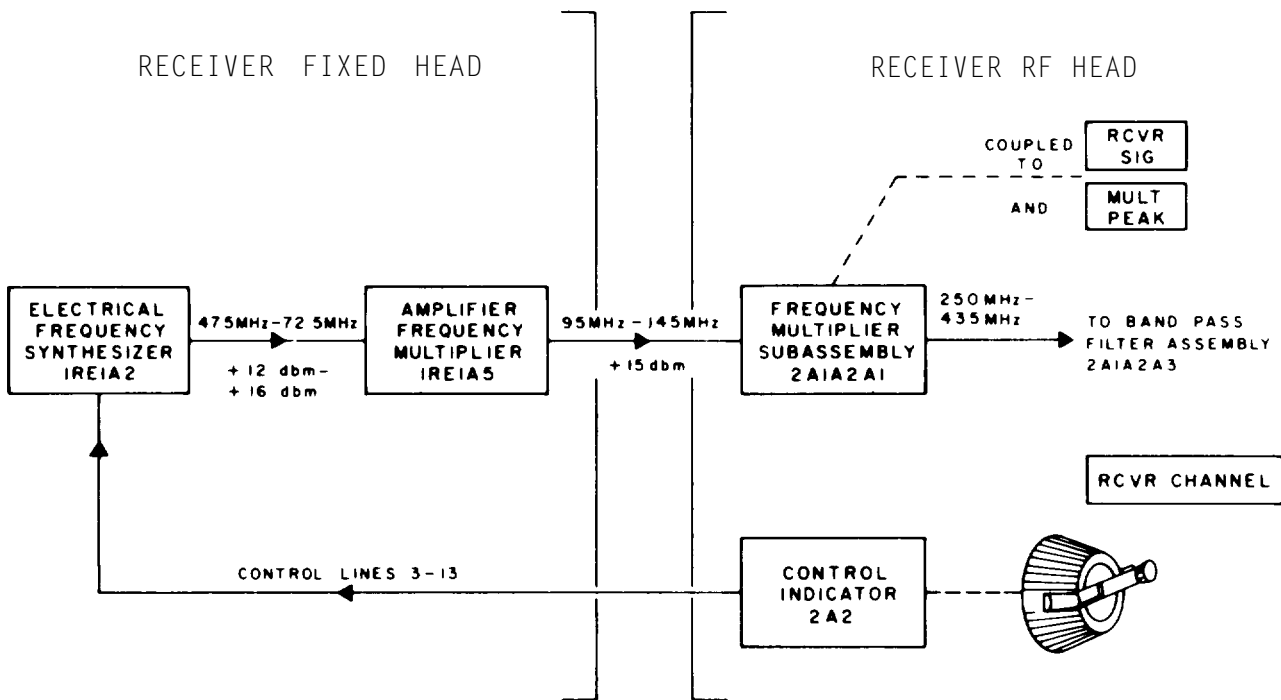
(b) The bias network R1 and R2 converts these conditions into three dc levels at pins 2 and 3 of comparators U3 and U2 respectively. C7 filters out any picked up noise. The bias network of R3, R4, and R5 sets the dc reference voltages at pins 3 and 2 of U3 and U2 respectively. Comparison of these reference voltages to the input conditions determines the circuit operating mode. This is done by comparators U2 and U3 in conjunction with logic gate U1B. The pulse form restorer operates in the binary mode when the output (pin 4) of U1B is low and in the biternary mode when the output is high. This mode control signal goes to the selector circuits of U10 and U9 on the pulse form restorer and electrical synchronizer boards respectively. Pin 7 of U2 controls the external order wire selection circuit consisting of relay K1, transistor Q3 and resistors R6 and R7. R8 and R9 form a pad which adjusts the external order wire signal to the correct input level. The squelch logic must turn off the pcm retiming and the clock input when the pcm output is unterminated or when the video level is low. The pcm termination is detected by the circuit consisting of Q1, Q2, CR1, R10 - R13, R15, and C9. When the pcm output is terminated with 91 ohms the pcm signal is 0 to -2 volts. Unterminated, it rises to 0 to -12 volts. The pcm output signal via R10 will turn off transistor Q1 part of the time if the pcm output is left unterminated. This in turn will switch on Q2, discharging C9 and keeping pin 12 of U1D constantly low. This occurs because the charging time constant of C9 is much longer than the discharging time constant. The charging time constant is equal to C9 times (R13) while the discharging time constant equals C9 times (R13 + R12). When the pcm output is terminated, Q1 is always on, Q2 always off and pin 12 of U1D is high. U1D is used here as an inverter.

(c) U1C combines the termination detector squelch signal with the low video level squelch signal from E1 of the pulse form restorer board. Either condition causes a "0" level to be produced at pin 10 of U1C. This signal inhibits pcm re-timing at UJ9A of the pulse form restorer board and also inhibits timing pulse generation at U4A of the electrical synchronizer board. C5 and C6 provide decoupling of the supply line from the +5 volt external regulator U1. Filtering of the  $\pm 12$  volt supply lines is done by inductors L1, L2, L3; capacitors C1, C2, C3, C4, C8, and C10; and ferrite beads Z1 and Z2. The ferrite beads prevent the escape of internally generated high frequency noise onto power lines.

## 2-49. Local Oscillator Frequency Generating Chain

a. General. The local oscillator frequency is generated and doubled in the receiver fixed head then fed to the receiver rf head where it is multiplied to its final frequency. Local oscillator frequency selection is determined by control-indicator 2A2, located in the receiver rf head. The basic frequency is generated in electrical frequency synthesizer 1RE1A2, depending on the coding information received from control-indicator 2A2. The output of the electrical frequency synthesizer is doubled in amplifier-frequency multiplier 1RE1A5 and then applied to frequency multiplier 2A1A2A1 in the receiver rf head, where it is doubled or tripled as required. Final control of the local oscillator frequency is exercised by tunable bandpass filter assembly 2A1A2A3, before it is applied to frequency mixer stage 2A1A2A2.

b. Block Diagram Analysis (Fig. 2-69) Electrical frequency synthesizer 1RE1A2, in conjunction with control-indicator 2A2, generates selected frequencies in the range of 47.5 to 72.5 MHz. Each of the selected frequency steps is referenced to a crystal-controlled oscillator to provide the required frequency stability. The local oscillator multiplication factor is times-4 for channel 119 and below and times-6 at channel 120 and above. The channel selector provides a 10 digit binary code to the synthesizer to select the correct basic frequency. An eleventh digit (control line 13) is generated between channels 119 and 120 to change the frequency steps of the synthesizer output from 125 kHz (times-4 multiplication) to 83.33 kHz (times-6 multiplication). The decade counter of control-indicator 2A2 within the front panel is offset by 60 channels in the cam coding arrangement. Thus the frequency of the local oscillator is 30 MHz higher than the frequency of the received channel as indicated on the front panel. The 47.5 to 72.5 MHz output of the synthesizer is fed into amplifier-frequency multiplier 1RE1A5 which doubles the synthesizer output frequency and amplifies the resulting signal to the level required by the subsequent multipliers in the receiver local oscillator frequency generating chain. The output rf signal, 95 to 145 MHz at +15 dbm±2 db, is then fed into frequency multiplier 2A1A2A1, located in the receiver rf head, which provides the final frequency multiplication. Frequency multiplier 2A1A2A1 doubles the incoming rf frequency over a portion of the band and triples it over the remainder of the band (para 2-37).



EL5RE069

Figure 2-69. Local Oscillator Frequency Generation, Block Diagram.

2-50. Amplifier-Frequency Multiplier 1RE1A5

a. General. Amplifier-frequency multiplier 1RE1A5 is functionally similar to amplifier frequency multiplier 5TR1A4 (para 2-16), but they are not interchangeable.

b. Block Diagram Analysis (Fig. 2-70). Electrical frequency synthesizer 1RE1A2 output, in the range of 47.5 to 72.5 MHz at a nominal level of +16 dbm (at 47.5 MHz) to 12 dbm (at 72.5 MHz), is first fed to low pass filter 1RE1A5FL1. The low pass filter attenuates all unwanted harmonics generated by electrical frequency synthesizer 1RE1A2 which would otherwise lower the efficiency of the doubler circuit. The rf signal at the output of the filter is applied to 4 to 1 transformer T1 in amplifier-frequency multiplier 1RE1A5A1. T1 converts the unbalanced input line to a balanced output which is then fed into full-wave rectifier CR1. CR1 consists of a matched pair of hot carrier diodes. Hot carrier diodes provide efficient frequency doubling with low spurious output. The rectifier output circuits are balanced to remove the fundamental input frequency and all odd harmonics. Total conversion loss is about 8 db; the resulting signal is applied to three-stage, stagger-tuned, broadband amplifier Q1 through 1)3. The first stage is tuned at the low end of the frequency range, while the second stage is tuned at the high end of the frequency range; the third stage is tuned at mid-frequency. Amplifier gain is fixed at about 10 db. The output of the amplifier is then coupled to a tuned bandpass filter which attenuates all unwanted harmonics. The output signal in the range of 95 to 145 MHz in 50 ohms is fed to frequency multiplier 2A1A2A1 in the receiver rf head. A dc me-

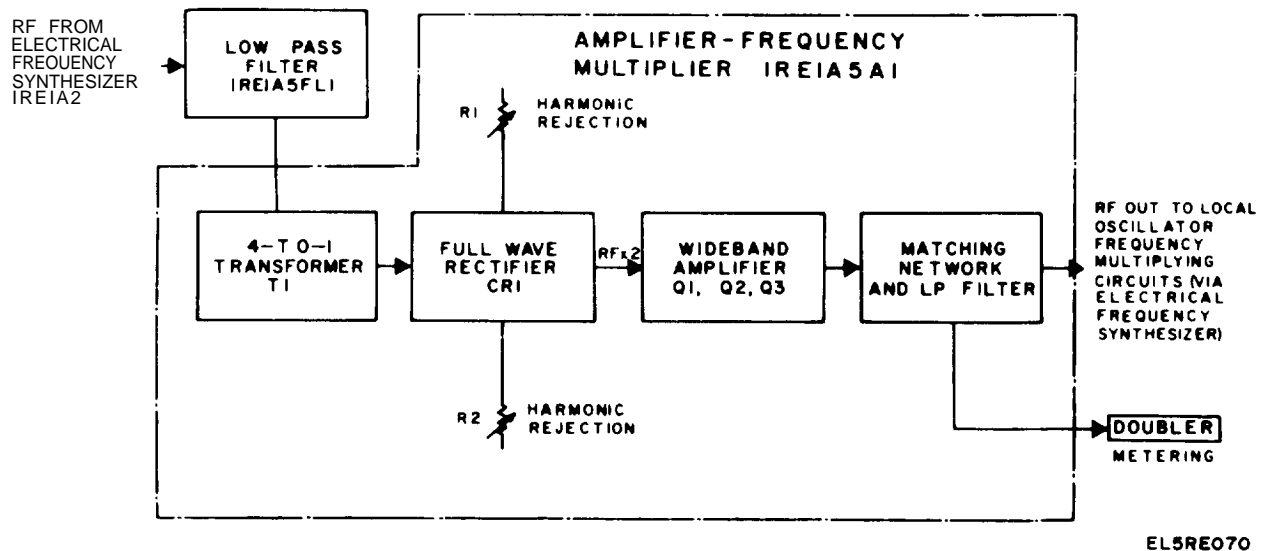


Figure 2-70. Amplifier Frequency Multiplier 1RE1A5, Block Diagram.

tering signal, derived from the output signal, provides an indication of the actual power delivered to frequency multiplier 2A1A2A1 (DOUBLER metering).

c. Detailed Circuit Analysis (F0-4-23). The incoming signal is fed through P1-A1 to low pass filter 1RE1A5FL1 conventional LC-type filter mounted on a separate board. The unbalanced output of the filter is connected across terminals E2 and E1 of amplifier-frequency multiplier 1RE1A5A1 then to terminals 1 and 2 of transformer T1. The output at pins 3 and 5 is balanced to ground and stepped up in voltage four times to increase the efficiency of full-wave rectifier CR1, L1, R1, and C3, and L2, R2, and C4, balanced tuning circuits, eliminate the fundamental frequency and all odd harmonics of the fundamental. Balance of the two sides of the rectifier output is achieved by adjusting R1 and R2, the HARMONIC REJECT potentiometers. The output of the rectifier, at twice the input frequency, is then coupled through C1 C2, C5 and L3 to the base of Q1. C5 is adjusted for optimum input matching to first stage amplifier (Q1. The output at the collector of Q1 is coupled through C8 and L5 to the base of (Q2. C11 adjusts the low-frequency portion (95 to 120 MHz) of the amplifier response. The signal at the Q2 collector is then coupled through C14 and L7 to the base of Q3. The response of the second amplifier stage is tuned to the high-frequency portion (120 to 145 MHz) of the amplifier response by C14 and C17. The wideband response (95 to 145 MHz) of the third amplifier stage Q3 is adjusted by L8. R9 adjusts the bias of all transistors while R11 compensates for any temperature variation. The output of the third amplifier stage is fed into a bandpass filter circuit C22, L10, C23, C24, L11, L12, C26 which attenuates all unwanted harmonics. C23 and C24 adjust the response of the bandpass filter. L13 across the rf output prevents any output impedance variations from affecting the filter response. The filtered output at twice the input frequency is then coupled through C28 and E4 to P1-A2, the rf output connection, for distribution to the frequency multiplying circuits in the receiver rf head. The DOUBLER metering signal, derived directly from the rf output, is rectified by CR2 and the resulting dc signal is fed through R12 and FL3 to P1-10.

## 2-51. Power Supply 1RE1PS1 (Fig. 2-71)

a. General. Power supply 1RE1PS1 converts the 115 vac input voltage to the dc voltages required for the operation of the receiver and the order wire unit. It provides regulated outputs of +12 v and -12 vdc for use by all transistor circuits and 26 vdc unregulated for the operation of relays, indicator lamps and alarm circuits.

(1) The 115 vac from the AC connector at the rear of the receiver is applied through the AC POWER circuit breaker to the primary of input transformer T1. The two outputs of the transformer are individually rectified and filtered; one is used as the 26 vdc unregulated supply, the other becomes the 24 vdc regulated supply from which two 12 vdc supplies are derived. Part of the second output voltage, taken from transformer T1, is fed into a pre-regulator circuit, which provides a constant current to the 24 vdc regulator circuit.

(2) In the regulator circuit, a sample of the 24 vdc regulated output is compared with a reference Zener diode voltage in a dc amplifier circuit. Any variation in the 24 vdc output will produce an error voltage at the output of the amplifier Q1-Q2. This error voltage is then amplified and fed back to control the impedance of transistors Q1 and Q2 in series with the 24 v output line. The change in impedance changes the output voltage in the proper direction to restore it to the preset nominal value. This nominal value is adjusted by the 24 V VOLTAGE ADJUST control.

The amplifier voltage regulator circuits are provided with a short circuit protection device. Zener diode CR4 in series with the 24v output voltage limits the current through Q2 of the series regulator in the event of short circuit, the 24 v supply circuit being restored to normal when the short circuit condition is removed.

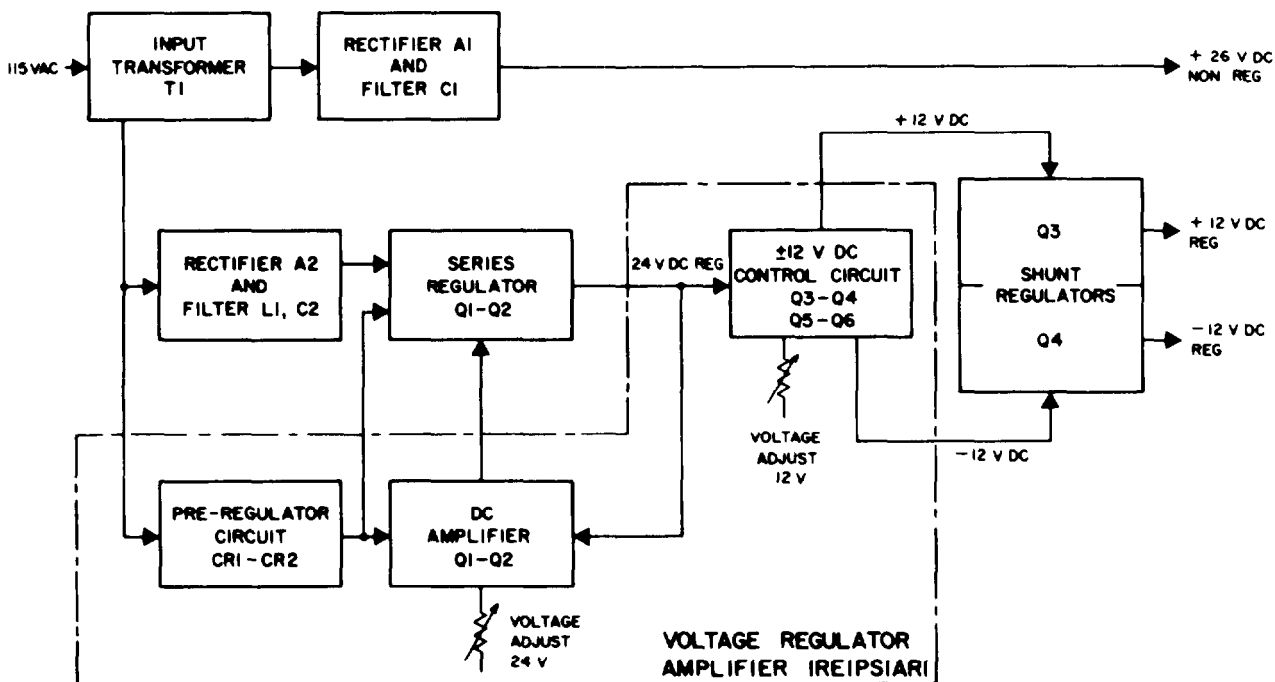
(3) The pre-regulator voltage increases the overall efficiency of series regulator Q1-Q2. This voltage is held constant above the regulated output voltage by Zener diode CR3 and is applied in parallel with the feedback control voltage to the base of Q2. The ripple on the output line is cancelled by a ripple feedback circuit adjusted by a HUM NEUTRALIZE control.

(4) The +12 vdc and -12 vdc supplies are derived from a pair of complementary shunt regulators, Q3 and Q4, which establish a zero reference (ground) potential exactly midway between the positive and negative sides of the 24 vdc supply. (Q3 and Q4 also provide return paths for unbalanced current between the two 12 vdc supplies. The reference point is set by the 12 V VOLTAGE ADJUST control.

(5) The metering voltages are taken from the +12 vdc and -12 vdc outputs, referenced to Zener diode voltages, and adjusted by individual meter calibration potentiometers in their respective voltage divider circuits.

b. Detailed Circuit Analysis (F0-4-27).

(1) 26 vdc unregulated supply. The 115 vac source voltage is applied through P2-6 and P2-7 to the primary winding 1-2 of input transformer T1. The output at terminals 3 and 4 is rectified in A1 and the resulting 26 vdc is connected to P2-4 and P2-5 for distribution. C1 and CR1, connected across the 26 vdc line, provide filtering and overvoltage protection.



EL5RE071

Figure 2-71. Power Supply 1RE1PS1, Block Diagram.



(2) 24 vdc regulation. The output at terminals 5 and 6 of T1 is fed to rectifier A2 and to the pre-regulator circuits in voltage regulator amplifier 1RE1PS1AR1. The 24 vdc output of A2 is filtered by L1 and C2, is then fed to the collectors of Q1 and Q2, the series regulator circuit. Zener diode CR2 provides overvoltage protection of the 24 vdc line. Series regulator transistors Q1 and Q2 (mounted on the heat sink) are connected in a high-gain dc amplifier arrangement, the emitter of Q1 being the regulated output line. The reference voltage for the 24 vdc series regulator is developed from the 24 v line through Zener diodes CR5 and CR6 in voltage regulator amplifier 1RE1PS1AR1. The reference potential of 12 v across CR5 and CR6 at the base of transistor Q2, is reflected in the Q1 emitter circuit by emitter-follower action to provide base-emitter temperature compensation for Q1. The voltage at the base of Q1 is derived from voltage divider R6, R7 and R8, connected across the 24 v output line. 24 V VOLTAGE ADJUST potentiometer R7 sets the series regulator output voltage to nominal. The peak potential taken across terminals 5 and 6 of transformer T1 is fed through J2 pins P and S to full-wave rectifier CR1 and CR2 in voltage regulator amplifier 1RE1PS1AR1, to be used as a pre-regulator voltage. C4 filters the pre-regulator voltage. The output of CR1 and CR2, clamped 6 v above the regulated 24 v by CR3, is fed through R1 and R2 to the collector of Q1, and through P1-U to the base of Q2 of the series regulator circuit. The constant current source to the base of Q2 effectively provides a second feedback control voltage in parallel with the control voltage derived from potentiometer R7 and applied to the base of Q1. Any change in the 24 vdc output voltage will cause a change in the Q1 emitter-collector; this change in current will be added or subtracted from the current to the base of Q2 of the series regulator. This will change the  $(1/2)$  emitter-collector impedance and simultaneously change the voltage drop across Q1 in the correct direction to compensate for the change in the output voltage, thus restoring the 24 vdc output voltage to nominal. R28 and CR4 form an over-current protection device for series regulator circuit Q1 and Q2. The voltage drop across R28, Q1 and Q2 will approach 4.3 v as the current approaches 2.2 amperes. As it reaches 4.3 v, CR4 fires and causes the voltage at Q2 base to drop, by-passing the nominal feedback control voltage and limiting the current through Q1 to 2.2 amperes. This current-limiting function effectively protects the power supply against any direct short circuit, restoring the voltage to normal as soon as the short circuit has been removed. Ripple voltage of the pre-regulator supply is fed through R3 and R5 (HUM NEUTRALIZE potentiometer) to the base of control transistor Q1 in the correct polarity to neutralize the ripple in the regulated output.

(3) +12 v and -12 vdc regulated supply. The center zero voltage reference point is maintained exactly midway between +12 vdc and -12 vdc by the action of shunt regulator transistors Q3 and Q4, mounted on the heat sink. Q3 and Q4 act as load resistances across the +12 vdc and -12 vdc supplies and as such equalize the current around the zero reference value. The circuits that control the +12 v and -12 vdc shunt regulation consist of transistors Q3 through Q6 of voltage regulator amplifier 1RE1PS1AR1. Zener diode CR7 provides the reference voltage used in the shunt regulator control circuit. CR7 clamps the Q4 base voltage 6 volts below the dc common (ground) line. The Q3 emitter is connected to the emitter of Q4, effectively clamping it to the reference voltage. The voltage at the base of Q3 (voltage regulator amplifier) is taken through divider R10, R11 and R12 across the 24 vdc regulated supply, and adjusted by R11 to set up the zero reference point at Q3 collector. If the output currents on the +12 v and -12 vdc lines become unbalanced, this zero reference level will tend to drift toward one of the output voltages; this will cause a change in the Q4 emitter current (voltage regulator amplifier 1RE1PS1AR1 - AR1). Since the Q4 base is clamped to the same voltage as the (J3 collector by the

action of Zener diode CR7, its collector voltage will change and will permit either Q5 or Q6 to draw base current. Since Q5 is a PNP transistor and Q6 is an NPN transistor, their reactions to a change in base voltage are complementary. As a result, either shunt regulator transistor Q3 or Q4 on the heat sink will draw emitter-collector current to balance the two current load. Capacitors C2 and C5 prevent the regulator circuits from oscillating. Thus if the +12 v current exceeds the -12 v current, Q4 will pass the imbalance current, and if the -12 v current exceeds the +12 v current, Q3 will pass the imbalance current.

(4) Metering circuits. The metering voltages of the +12 vdc supply are taken from voltage divider R21, R22 and R23, across the +12 vdc supply, and fed through R29 to the +12 V meter connection on the front panel. The negative side of the meter (meter common) is returned to a 6 volt reference voltage across CR8, thus establishing an expanded scale for meter reading. A 10 percent of full scale deflection on the meter scale represents a 0.5 v change in the output voltage. R22 is the 12 vdc meter calibration potentiometer. A similar meter circuit is provided for the -12 vdc supply, which is derived from voltage divider R18, R19 and R20. The -12 vdc metering voltage is referenced to Zener diode CR9. R19 is the -12 vdc meter calibration Potentiometer.

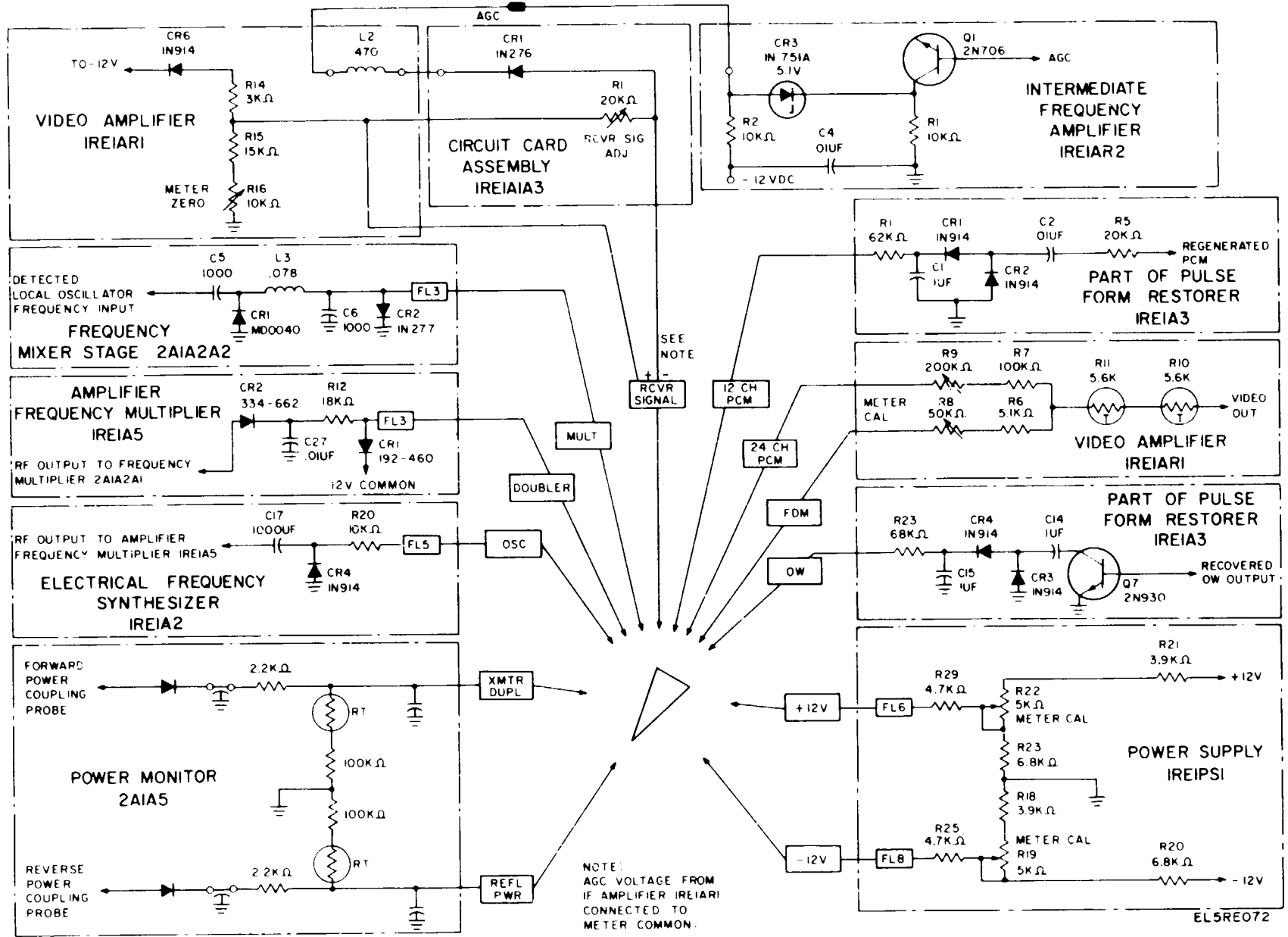
2-52. Receiver Metering Circuits

a. General. The receiver metering circuits include a 100 microampere meter which is connected into the various metering circuits by a 12-position rotary selector switch. The receiver metering circuits give an indication of power and voltage levels throughout the receiver fixed and rf heads. The meter has a 0 to 100 scale with a green band in the center. For any selector switch position marked with a green dot, a normal meter reading should fall within the green band. Each metering circuit has its own meter-matching circuit and a calibration resistor so that this single meter can serve to indicate various power and voltage ranges. The following chart lists the metering circuits of the receiver and their nominal indications:

| Switch position | Nominal value              | Scale reading<br>(percentage of full-scale) |
|-----------------|----------------------------|---|
| REFL PWR        | Zero Power                 | 10  |
| XMTR DUPL       | 20 watts (antenna)         | 65  |
| OSC             | 25 milliwatts              | 50  |
| DOUBLER         | 30 milliwatts              | 50  |
| MULT            | +6 dbm                     | 40 to 50                                    |
| RCVR SIG        | -74 dbm (antenna)          | 50  |
| 12 CH PCM       | 2.0 v pp/91 ohms           | 50  |
| 24 CH PCM       | 265 milliwatts rms 51 ohms | 50  |
| FDM             | -4 dbm/91 ohms             | 50  |
| OW              | -10 dbm/600 ohms           | 50  |
| +12 v           | +12 vdc                    | 50  |
| -12 v           | -12 vdc                    | 50  |

b. Metering Circuits Analysis (Fig. 2-72, 2-73, 2-74). For point-to-point tracing of metering circuits, refer to FO-4-28.

Figure 2-72. Receiver Metering Circuits (Part No. CMC 456-260), Simplified Schematic Diagram.



(1) REFL PWR metering (position 1). The REFL PWR metering gives an indication of reverse power at the antenna connector. The rf signal from the reverse-power coupling probe is detected, to produce a dc signal proportional to the amount of reflected power sensed through power monitor 2A1A5. A thermistor connected across the detector circuit provides a constant output independent of temperature. The resulting dc signal is fed through distribution box 1A2A1 into monitor panel 1RE1A1 and meter selector switch S1-A (meter positive). The negative side of the meter is returned through S1-B and the distribution box to the meter common point in the receiver rf head. Normal indication is almost zero power (less than 10 percent of full scale).

(2) XMTR DUPL metering (position 2). The XMTR DUPL metering circuit gives an indication of the forward (output) power at the ANT. connector. A thermistor-controlled detector circuit in series with the forward power coupling probe produces a dc signal proportional to forward power going through power monitor 2A1A5 (para 2-31). The thermistor, connected across the detector circuit, provides the same output independent of temperature. The dc signal is fed through distribution box 1A2A1 to monitor panel 1RE1A1 and meter selector switch S1-A (meter positive). The meter common is returned to ground at the receiver rf head through the distribution box. A nominal 20 watts at the antenna will produce a 65 percent meter indication.

(3) OSC metering (position 3). The OSC meter position gives an indication of the electrical frequency synthesizer 1RE1A2 output signal as it is fed into amplifier-frequency multiplier 1RE1A5. A portion of the rf signal at the output of modulator-oscillator 1RE1A2A2 (para 2-4) is rectified by CR4 to produce a dc metering signal proportional to the rf signal. The dc signal is then fed through R20 and FL5, through interconnecting box 1RE1A2A1 in electrical frequency synthesizer 1RE1A2, and monitor panel 1RE1A1 to meter selector switch S1-A (meter positive). The meter return is grounded at interconnecting box 1RE1A2A1 (F0-4-3). A 50 percent of full scale indication on the meter is equivalent to approximately 25 milliwatts rf output. 40 to 60 percent of full scale represents a synthesizer output ranging approximately from 15 to 40 milliwatts. In synthesizers equipped with modulator-oscillator 1RE1A2A2 CMC No. 220-800159-000, a portion of the rf signal at the output of the modulator-oscillator is rectified by CR6 to produce a dc metering signal proportional to the rf signal. The dc signal is then fed through R31 and FL5 to the meter selector switch and the meter. Synthesizer outputs of 20 to 40 milliwatts (+12.5 to +15.5 dbm) will produce 20 to 80 percent full-scale deflection on the meter (fig 2-73).

(4) DOUBLER metering (position 4). The DOUBLER metering signal is derived from the rf output of amplifier-frequency multiplier 1RE1A5 (para 2-49) which is used to drive frequency multiplier 2A1A2A1 (para 2-37). A portion of the output signal is rectified in CR2, then filtered by R12 and C27 to produce a dc voltage suitable for metering. The dc signal is then fed through interconnecting box 1RE1A2A1 to monitor panel 1RE1A1 and meter selector switch S1-A (meter positive). The metering return line is fed through interconnecting box 1RE1A2A1 to frequency multiplier 1RE1A5. The meter circuit has been calibrated to give a 50 percent of full scale indication for a nominal 30 milliwatt (+13 dbm) output signal. 40 to 60 percent of full scale meter indications represent approximately 20 to 35 milliwatts output signal.

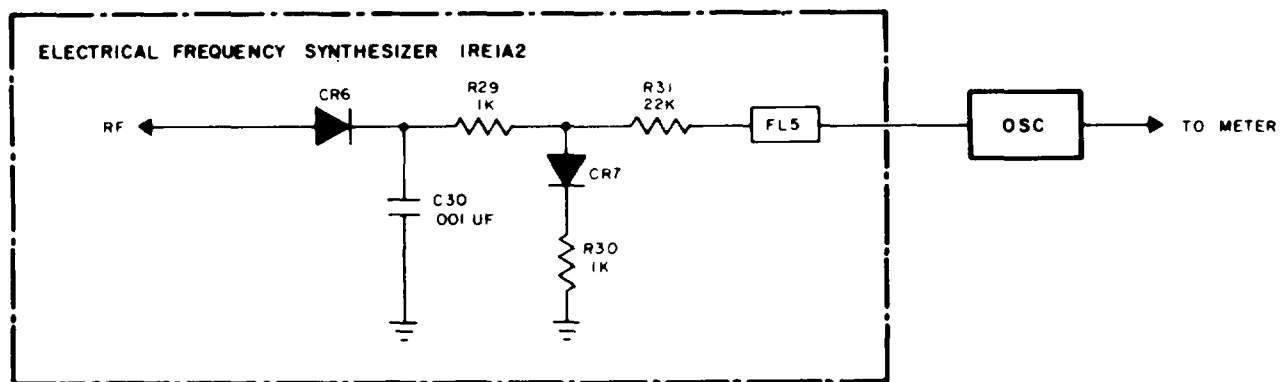
(5) MULT metering (position 5). The MULT metering signal gives an indication of the local oscillator signal level and is taken at the input to frequency mixer stage 2A1A2A2. A portion of the local oscillator input to the frequency mixer stage is rectified by CR1 and filtered to produce a dc signal suitable for metering. The

dc voltage is fed through distribution box 1A2A1 to monitor panel 1RE1A1 and meter selector switch S1-A (meter positive). The meter common is returned to the receiver rf head through distribution box 1A2A1. A local oscillator signal of +6 dbm will provide a 40 to 50 percent of full scale indication.

(6) RCVR SIG metering (position 6). The RCVR SIG metering gives an indication of the level of the incoming received signal at the antenna connector. The metering signal is derived from the agc voltage generated in intermediate frequency amplifier 1RE1AR2, which adjusts the gain of the receiver IF amplification system. The agc voltage from intermediate frequency amplifier 1RE1AR2 is routed through electrical frequency limiter-discriminator 1RE1A4 into video amplifier 1RE1AR1. The agc voltage is then fed through inductor L2 to monitor panel 1RE1A1 and through diode CR1 of circuit card assembly 1RE1A1A3 to switch S1-B (position 6) and the negative side of the meter. RCVR SIG ADJ control potentiometer R1 of circuit card assembly 1RE1A1A3 is connected across the meter at this position and calibrates the scale to indicate 50 percent of full scale deflection for a -74 dbm received signal at the antenna port. The positive side of the meter is returned through S1-A to video amplifier 1RE1AR1 to a point on voltage divider CR6, R14, R15 and R16 connected between -12 v dc and ground. R1b is the meter zero adjustment when no signal is present at the antenna connector.

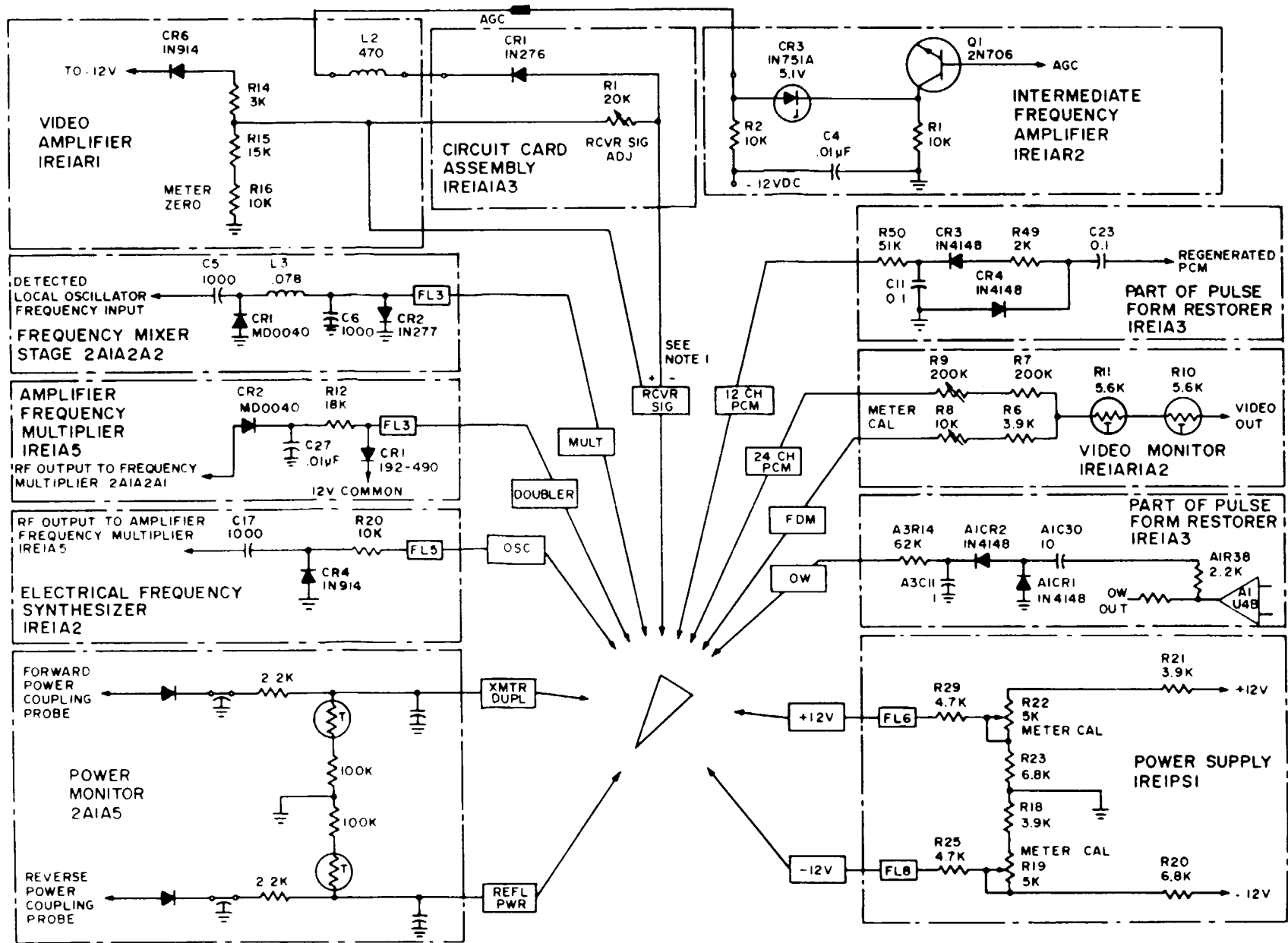
(7) 12 CH PCM metering (position 7). The 12 CH PCM metering provides an indication of the regenerated pcm level at the output of pulse form restorer 1RE1A3. In Receiver, Radio R-1329, R-1329A, and R-1329B the non-inverted regenerated pcm pulses from the gated multivibrator (para 2-47) are fed through R5 and C2 to metering detector CR1 and CR2. The rectified dc signal, suitable for level metering, is fed through RI and PI-9 to monitor panel 1RE1A1 and switch S1-A (meter position). The meter common is returned to ground in pulse form restorer 1RE1A3. The meter is calibrated to indicate 50 percent of full scale for a 2.0 volt peak-to-peak (in 91 ohms) regenerated pcm output signal. In Receiver, Radio R-1329C the emitter of buffer Q4 drives the pcm metering circuit (fig. 2-73.1). When this circuit is loaded with a 5 k ohm resistor, the output voltage is nominally 250 mV (50%) when the pcm signal is normal. The rectified dc signal, suitable for level metering, is fed through P1-9 to monitor panel 1RE1A1 and switch S1-A (meter position). The meter common is returned to ground in pulse form restorer 1RE1A3.

(8) 24 CH PCM and FDM metering (positions 8 and 9 respectively). 24 CH PCM and FDM metering give an indication of the video levels at the receiver output; these levels are used mainly for system line-up. The metering voltages are derived from the video output of video amplifier 1RE1AR1 (para 2-46). A portion of the video output is amplified in a two-stage amplifier, then rectified to produce dc signals suitable for metering. The metering circuit is stabilized for varying temperatures by two thermistors in series. The metering signal is then split into two paths; the 24 CH PCM metering signal is taken through R7 and R9 to monitor panel 1RE1A1 switch S1-A (meter positive). R9 adjusts the level of the 24 CH PCM metering voltage to indicate 50 percent of full scale when the video output level at the VIDEO OUT connector is 265 millivolts rms in 51 ohms (equivalent to a  $\pm 300$  kHz peak deviation). The fdm metering signal is taken through R6 and R8 to monitor panel 1RE1A1 and switch S1-A (meter positive, position 9). R8 adjusts the level of the fdm metering voltage to indicate 50 percent of full scale when the video output level at the fdm connector is -4 dbm in 91 ohms (equivalent to  $\pm 75$  kHz peak deviation). The meter common of both 24 CH PCM and FDM is returned to the -12 volt dc line in video amplifier 1RE1AR1.



EL5RE073

Figure 2-73. Receiver Metering Circuit for Electrical Synthesizer 1RE1A2 Equipped with Modulator-Oscillator 1RE1A2A2 (Part No. CMC 220-800159-000), Simplified Schematic Diagram.



NOTE  
 1 AGC VOLTAGE FROM IF AMPLIFIER IREIAR1  
 CONNECTED TO METER COMMON.

EL5RE308

Figure 2-74. Receiver Metering Circuits (R-1329C) Simplified Schematic Diagram.

Fig 2-74

2-145

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(9) OW metering (position 10) (Receivers R-1329, R-1329A, and R-1329B). The OW metering circuit provides an Indication of the recovered order wire signal level at the output of pulse form restorer 1RE1A3. A portion of the recovered order wire signal is first amplified, then rectified in metering detector circuit CR3 and CR4. The resulting dc signal is then connected through R23 to monitor panel 1RE1A1 and switch S1-A (meter positive). The meter common is returned to ground in pulse form restorer 1RE1A3. A 50 percent of full scale indication is equivalent to an order wire signal level of -10 dbm in 600 ohms.

(9.1) OW metering (Receivers R-1329C). The OW metering circuit provides an indication of the recovered order wire signal level at the output of the pulse form restorer 1RE1A3. The recovered order wire signal from the buffer amplifier U4B is rectified in metering detector circuit R38, CR1, CR2, and C30 on the modulation eliminator board in addition to C11 and R14 on the electrical interface board (fig. 2-74). The resulting dc signal is then connected through P1-10 to monitor panel 1RE1A1 and switch S1-A (meter positive). The meter common is returned to ground in pulse form restorer 1RE1A3. A 50% of full scale indication is equivalent to an order wire signal level of -10 dbm in 600 ohms.

(10) +12 V and -12 V metering (positions 11 and 12 respectively). The +12 V and -12 V metering voltages are derived from the corresponding outputs of voltage regulator amplifier 1RE1PS1AR1 of power supply 1RE1PS1 (para 2-50). Metering voltage for the +12 vdc regulated supply is derived from voltage divider R21, R22 and R23, across the +12 vdc supply, and fed through R29 to monitor panel 1RE1A1 and switch S1-A (meter positive, position 11). The meter common is returned to voltage regulator amplifier 1RE1PS1AR1 and connected to the cathode of diode CR8 which raises its potential to 6 volts, thus establishing an expanded scale for letter reading. Control R22 adjusts the meter reading to indicate 50 percent of full scale for 12 vdc. A 10 percent variation on the meter scale represents a 200 millivolt change in output voltage. Metering voltage for the -12 vdc regulated supply is derived from R20, R19 and R18 across the -12 vdc circuit and fed through R25 to monitor panel 1RE1A1 and switch S1-A (meter positive, position 12). The negative side of the meter is returned to voltage regulator amplifier 1RE1PS1AR1 and connected to the cathode of diode CR9 to obtain an expanded meter scale. Potentiometer R19 adjusts the meter to indicate 50 percent of full scale for -12 vdc. A 10 percent variation on the meter scale represents 200 millivolts change in output voltage.

## 2-53. Receiver Alarm Circuits

a. General. The receiver alarm circuits are part of monitor panel 1RE1A1 (front panel of receiver fixed head) and work in conjunction with the alarm circuits in the receiver fixed head, electrical frequency synthesizer 1RE1A2, and video amplifier 1RE1AR1, and electronic switch 2A4 in the receiver rf head. Monitor panel 1RE1A1 includes alarm control 1RE1A1A2, four indicator lights (AC POWER, SYNC, LOW SIGNAL and HIGH SIGNAL), one buzzer and three manually-controlled switches (AC POWER ON-OFF, BUZZER OFF, and BUZZER OFF-ALARMS NORMAL). The buzzer sounds when a change of state occurs in the associated alarm circuits. A fault will cause the buzzer to sound. Pushing the BUZZER OFF switch silences the buzzer. Once all fault indications are corrected, the buzzer will sound again until the BUZZER OFF switch is operated again. A built-in switch (BUZZER OFF-ALARMS NORMAL) enables the buzzer to be muted and the lamps dimmed during testing, alignment, and correction of fault conditions.

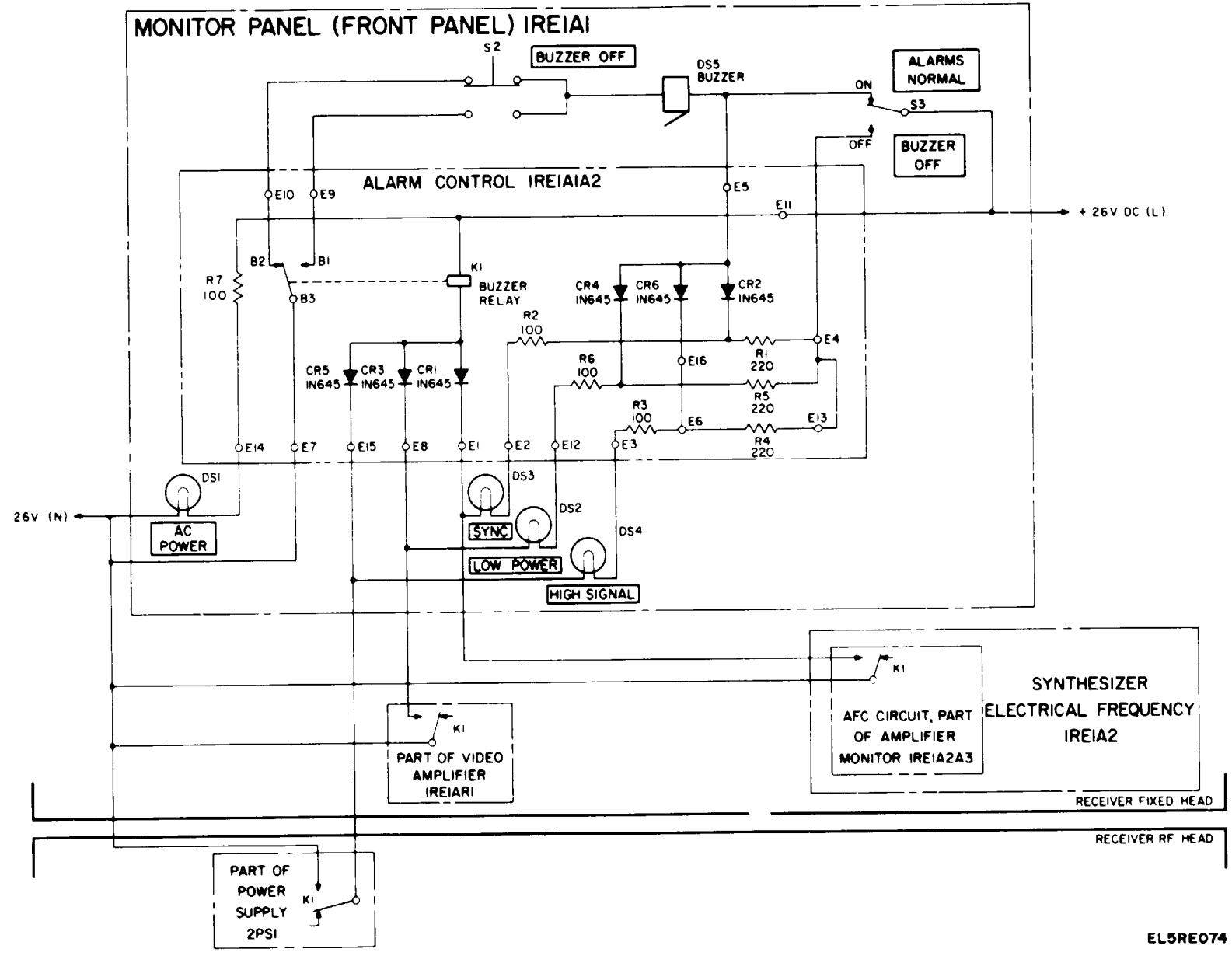


b. Indicator and Alarm Circuits Description (Fig. 2-75). For point-to-point tracing of indicator and alarm circuits, refer to F0-4-28.

(1) Ac input circuit. When ac power is switched on, +26 volts dc from power supply 1RE1PS1 is fed through P2-4 and J1-4 into monitor panel 1RE1A1, and through E11 of alarm control 1RE1A1A2 to one side of buzzer control relay K1 and to AC POWER indicator lamp DS1, through R7 and E14. The 26 vdc is returned through J1-5 and P2-5 to power supply 1RE1PS1. +26 volts dc is also applied through the BUZZER OFF-ALARMS NORMAL switch (in the ALARMS NORMAL position) to one side of the buzzer. The dc path through the buzzer is closed through contacts of buzzer control relay K1.

(2) SYNC (aft) alarm. The SYNC alarm circuit operates in conjunction with SYNC alarm relay K1 in amplifier-monitor 1RE1A2A3 (para 2-14) of electrical frequency synthesizer 1RE1A2. Normally the SYNC alarm relay is held operated by the afc SYNC alarm detector circuit and by the clock pulse D integrator. The SYNC alarm relay drops out either when afc voltage is outside limits or when clock pulse D is absent. The operating range of the SYNC alarm relay (2.5 volts to 10 volts on the afc line) is established by Zener diode CR3 and potentiometer R3 and corresponds to frequency control limits in the vco. When the afc voltage is outside these limits, the afc of the vco has been lost, and the SYNC alarm relay drops out. Normally clock pulse D), fed into the integrator, holds control transistor Q4 operated and in turn relay control transistor Q5 is cut-off and the SYNC alarm operates. In the absence of clock pulse D the relay drops out. When the relay is de-energized the +26 volt dc path through SYNC indicator lamp DS3, the buzzer control relay, and control diode CR1 in alarm control 1RE1A1A2 is closed. The circuit passes through monitor panel 1RE1A1, and interconnecting box 1RE1A2A1 of electrical frequency synthesizer 1RE1A2, to amplifier-monitor 1RE1A2A3. The SYNC lamp illuminates and the buzzer sounds; the BUZZER OFF switch silences the buzzer while the alarm condition is being corrected. When normal operating conditions are restored, the SYNC alarm relay in the synthesizer is energized, and opens the +26 volt dc path. The SYNC indicator lamp is out, the buzzer relay drops out, and the buzzer sounds. Pushing the BUZZER OFF switch restores buzzer circuits to normal.

(3) LOW SIGNAL alarm. The LOW SIGNAL alarm circuit operates in conjunction with the low signal alarm circuits in video amplifier 1RE1AR1 (para 2-46) and provides an alarm indication and squelch of the pcm signal when the noise content determines that the received signal is below the minimum operating level. A portion of the amplified video signal (VIDEO OUT) is fed through a filter which extracts the high-frequency noise components (520 kHz to 2 MHz). The extracted noise signal is first amplified, then rectified in alarm control 1RE1AR1A3. The resulting dc signal is used to control Schmitt trigger circuit Q4 and Q5, with a turn on/turn off operation. Normally the Q5 base is held at about -0.6 v by CR5 and R10. When the voltage at the rectifier output raises the voltage at the Q5 base to about +0.7 v, corresponding to a received signal level of -99 dbm at the antenna connector, Q5 starts to conduct. This causes the base of Q4, a PNP transistor, to go negative and drive it into conduction. Q4 controls the current through low signal alarm relay K1, causing it to operate. K1, energized, closes the -26 vdc path through LOW SIGNAL alarm indicator lamp DS2 and buzzer control relay K1 through control diode CR3. At the same time, low-signal alarm relay K1 in the video amplifier breaks the regenerated pcm output path terminating the pcm output in R17 (51 ohms). The operation of the buzzer in the event of a LOW SIGNAL alarm condition is as described in (2) above for the SYNC alarm. When the received signal level increases to approximately -96 dbm, Q5 and Q4 are cut-off and the low signal alarm relay is de-energized. The 3 db backlash prevents jittering when operating with near-limit signals. The 26 vdc to



EL5RE074

Figure 2-75. Receiver Alarm Circuits, Simplified Schematic Diagram.

the LOW SIGNAL lamp is off but the buzzer sounds. Pushing the BUZZER OFF button restores the buzzer circuits to normal.

(4) HIGH SIGNAL alarm. The HIGH SIGNAL alarm circuit operates in conjunction with HIGH SIGNAL indicator lamp DS4 on the front panel of the receiver fixed head and with the receiver protection circuits (para 2-32) in the receiver rf head. A detector diode connected in the receive arm stripline of electronic switch 2A4 senses the received rf level. When the received rf level reaches -10 dbm the dc output of the diode is sufficient to drive the high gain microcircuit differential dc amplifier whose output becomes positive under high signal condition (-10 dbm). The differential dc amplifier output is fed to an emitter-follower stage with two outputs. One of the outputs, the alarm drive, is fed into power supply 2PS1 to the base of Q2. Under high signal conditions, the alarm drive signal voltage will turn on Q2. The drop in voltage at the Q2 collector turns on Q1, a PNP relay drive transistor, which in turn will cause high-signal alarm relay K1 in power supply 2PS1 to energize. K1, when energized, closes the 26 vdc path through HIGH SIGNAL indicator lamp DS4 (alarm control 1RE1A1A2) and buzzer control relay K1. The HIGH SIGNAL lamp illuminates and the buzzer sounds. At the same time, the rf receive path is opened and the high received signal is dissipated in the dummy load. When the received signal drops below -10 dbm the rf receive path is reestablished and alarm indications are received.

(5) BUZZER OFF-ALARMS NORMAL switch. In the BUZZER OFF position, this switch removes the +26 volt dc supply from the buzzer circuit and connects additional 220 ohm dimming resistors, R1, R5 and R4, in series with the SYNC, LOW SIGNAL and HIGH SIGNAL indicator lamps respectively.

## Section V. RECEIVER-TRANSMITTER ORDER WIRE RT-773/GRC-103(V)

### 2-54. Order Wire Unit

a. General. The order wire unit provides a handset facility, with ringing on a party-line basis to all communication points in the radio system. At a repeater station, the unit provides for talking and signaling simultaneously in both directions of transmission, and provides a through circuit for the party-line communication. The order wire unit operates as an active 4-wire, 3-way hybrid which permits one order wire unit to operate with two radio sets in a repeater configuration. For transmission, the order wire send signals are connected to amplifier-monitor 5TR1A5 of each radio set, where they are added to the baseband signal. The order wire receive signals are connected from pulse form restorer 1RE1A3 of each radio set to the order wire unit. The speech and ring-out signals are fed to both transmitters; both receive path signals are fed into the handset receiver, as well as to the ringing receiver, to activate the buzzer and the CALL lamp. When the system is carrying pcm video, the order wire unit provides a through-path for order wire signals as well as the local send and receive functions. The order wire through-path, however, is opened during fdm operation, to prevent parallel-path signal cancellation. The order wire circuits are contained on two printed circuit boards interconnected through the front and rear panel wiring. Amplifier assembly 9A4 interconnects the order wire circuits of two radio sets and a handset, by means of an active 4-wire 3-way hybrid; in addition, the order wire amplifier introduces a sidetone into the handset receiver. Telephone signal converter 9A3 generates a 1,600 Hz signalling tone for

calling over the system and also detects the 1,600 Hz incoming call signal. The telephone signal converter circuits operate in conduction with the RING switch, the CALL indicator light, and the buzzer. The 12 vdc required for the operation of the order wire circuits, and the 26 vdc required for the buzzer and front panel lights, are obtained from either receiver (A or B). Two power control relays choose the receiver which will supply the required voltages. In repeater operation these voltages are normally obtained from receiver A.

## NOTE

In a repeater configuration, radio set A is connected to the TO RADIO connector, while radio set B is connected to the PATCH THRU connector.

b. Block Diagram Analysis (Fig. 2-76).

(1) Through path. The order wire signal from receiver A (speech and/or signaling) in the range of 200 Hz to 3 kHz at a level of -10 dbm/600 ohms is fed into amplifier-splitter Q1. One of the two outputs of Q1 is fed through PCM/FDM switch S1 to amplifier Q2. The output of Q2 is then filtered and fed to transmitter B. Similarly, the incoming signals from receiver B are fed into amplifier-splitter Q5. One of the two outputs of Q5 is fed through PCM/FDM switch S1 to amplifier Q6 and then to transmitter A through a 3 kHz low pass filter. Cross-talk from receiver A to transmitter A is at least 40 db below signal level.

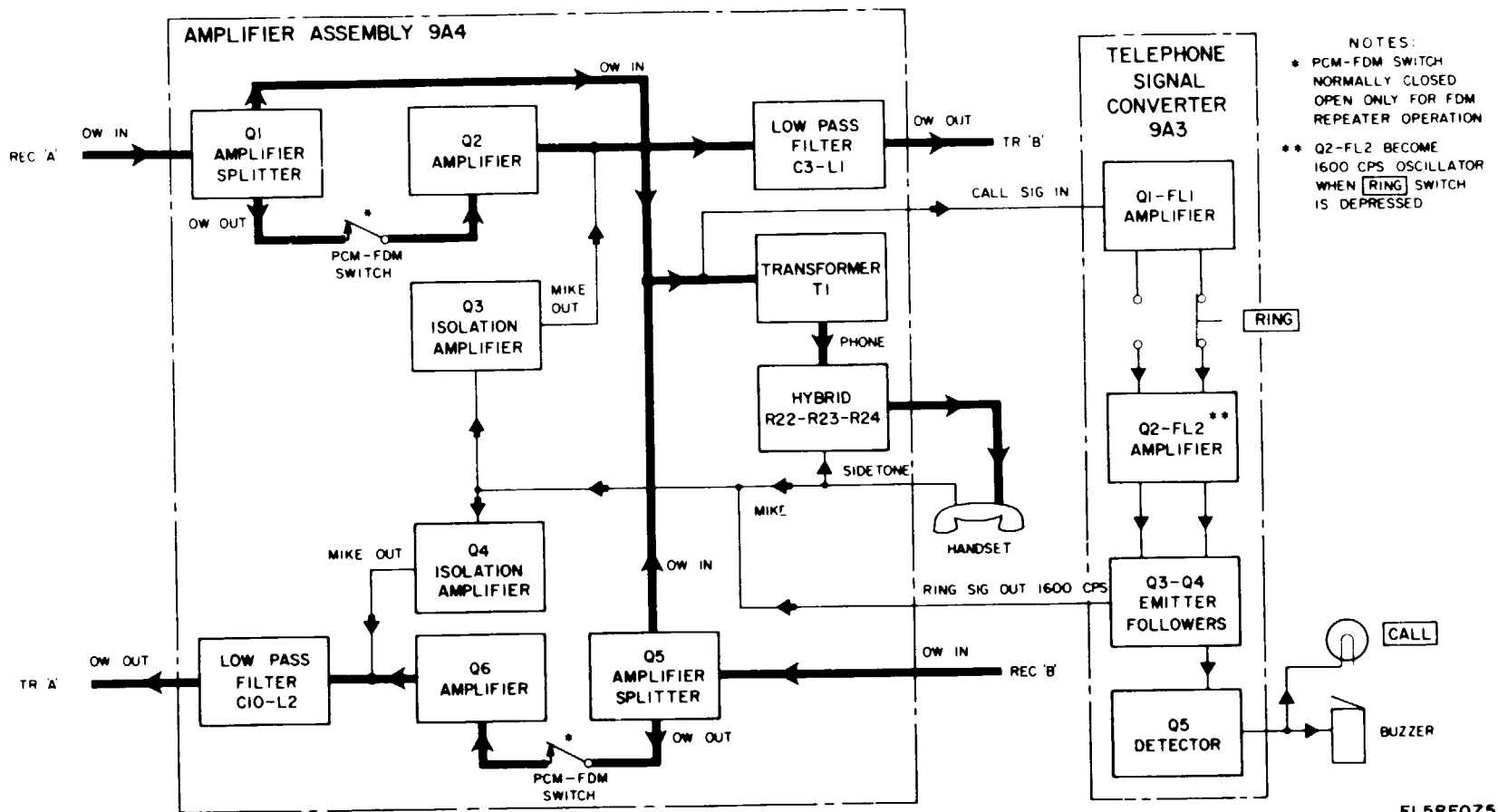
(2) Handset receive-transmit paths. The second output of amplifier-splitter Q1 (receiver A) is fed to the input circuit of transformer T1 whose secondary winding feeds the handset receiver. Similarly the second output of amplifier-splitter Q5 (receiver B) is fed to the input circuit of T1. Speech signals from the handset (PRESS-TO-TALK switch operated) at a level of -18 dbm are connected simultaneously to isolation amplifiers Q3 and Q4. The output of Q3 is then fed through the low pass filter to transmitter B, while the output of Q4 is fed through the outputs of splitter-amplifiers Q1 and Q5 and Q4 also provide limiting of speech signals if required.

(3) Sidetone. Speech signals from the microphone are coupled into a 6 db resistive hybrid with the earphone connected as one arm of the bridge. This results in the speech signal from the microphone appearing at the earphone at a level of -24 dbm.

(4) Signaling receive path. The incoming signals from receiver A or receiver B containing the 1,600 Hz signaling frequency are taken off the outputs of splitter-amplifier Q1 and Q5 and fed to telephone signal converter 9A3. The signal is first amplified, in a highly selective filter, Q1 and FL1 then fed through normally closed contacts in the RING switch to a second amplifier stage with an identical selective filter, Q2 and FL2. The output of the filter is coupled through a pair of cascaded emitter-followers Q3 and Q4, a gain control, and, through a second pair of normally-closed contacts on the RING switch, to detector amplifier Q5 to operate the ring relay. The relay operates the buzzer and CALL lamp.

(5) Signaling send path. When signaling to other sites in the system is required the RING switch must be depressed. This action opens the connection between the output of Q1 and the input of Q2, and turns Q2 into an oscillator. The oscillator output is then connected through Q3 and Q4, emitter-followers through the RING

Figure 2 - 7.6. Order Wire Unit, Block Diagram.



switch, now closed, to the same amplifier input point (Q3, Q4) as speech signals from the handset microphone. Level at this point will be 330 millivolts. Signaling is then transmitted through Q3 and Q4 in both directions.

## 2-55. Amplifier Assembly 9A4

a. General. Amplifier assembly 9A4 consists of three two-stage amplifiers Q1-Q2, Q3-Q4 and Q5-Q6, each giving two mutually isolated outputs and a bridge for the sidetone circuit. The order wire outputs from the two radio receivers are fed one each to an amplifier pair, Q1-Q2 and Q5-Q6. The handset output is fed to amplifier Q3-Q4, which also provides amplitude limiting.

(1) The two mutually isolated outputs of Q3 and Q4 transistors are combined with the secondary outputs of the other two amplifiers (Q2 and Q6 collectors) and fed to radio transmitters A and B inputs respectively. R7 and R18 are common gain controls for the Q2-Q3 and Q4-Q6 combined outputs respectively.

(2) The collector outputs of transistors Q1 and Q5 are combined in a common collector load and then fed through transformer T1 and a 6 db hybrid bridge to the handset receiver (PHONE). The sidetone is injected into the handset receiver through the same hybrid bridge. Decoupling capacitors C15, C17, and C16, C18 suppress parasitic oscillations and reduce cross-talk distortion.

### b. Detailed Circuit Analysis (FO-4-48).

(1) Through path PCM mode. Incoming signals (speech and/or signaling) from receiver A (J1-E) are applied at P4-K, and are coupled through C1 to the base of transistor Q1. The Q1 emitter output is fed through R5, C2 and S1-A PCM/FDM switch (in the PCM position) to the emitter of transistor Q2. The Q2 collector output is then fed through low pass filter C3-L1 and P4-L to transmitter B (J2-G). Similarly, incoming signals from receiver B (J2-E) are applied to P4-F and are coupled through C13 to the base of transistor Q5. The Q5 emitter output is fed through R28, C14 and switch S1-B to the emitter of transistor Q6. The Q6 collector output is then fed through low pass filter C10-L2, and P4-H to transmitter A (J1-G).

(2) Handset receive-transmit path. The handset receiver gets its signals from the collector output of Q1 (receiver A) and Q5 (receiver B). Q1 and Q5 collectors have a common collector load R4. The combined outputs are then fed through transformer T1 through the active 4-wire 3-way hybrid, R22, R23 and R24, to the handset receiver (PHONE) through P4-J. The local microphone circuit (MIKE) applied to P4-C (PRESS-T0-TALK switch depressed) is coupled through C8 simultaneously to the bases of amplifiers Q3 and Q4. Q3 and Q4 each amplify the local microphone or ringing signal and also function as peak limiters to prevent overmodulation on high level speech peaks. R10 and R20 are the peak limiting resistors. The Q3 collector output is then combined with the Q2 collector output and fed through C3 and L1 to transmitter B. Similarly, the Q4 collector output is combined with the Q6 collector output and fed through C10 and L2 to transmitter A. Part of the incoming microphone signal (sidetone) is coupled through C6 to one side of the hybrid bridge and fed through R23 to the handset receiver.

(3) Signalling path. Part of the combined outputs of Q2 and Q6 are fed through C9, R17, and P4-B to telephone signal converter 9A3 (para 2-54) where the 1,600 Hz CALL signal is extracted. The 1,600 Hz RING signal from telephone signal converter 9A3 is fed through P4-E into amplifier assembly 9A4. The 'RING' signal is then fed through R13 and C7 to the Q3-Q4 amplifier pair for transmission in both directions.

(4) Through path-FDM mode. The patch-thru facilities of amplifier assembly 9A4 are disabled when switch S1 is in its FDM position. This is done in order not to interfere with the patch-thru facilities of the fdm repeater equipment. However, the handset receive and transmit facilities, as well as signaling facilities (CALL and RING) in both directions of transmission are not affected.

#### 2-56. Telephone Signal Converter 9A3

a. General. This unit, in conjunction with amplifier assembly 9A4 and monitor panel 9A2, provides signalling facilities on the order wire channel. Telephone signal converter 9A3 consists of a three-stage amplifier and a detector circuit driving a relay. The second stage functions as a 1,600 Hz generator when the RING switch is depressed.

#### b. Detailed Circuit Analysis (FO-4-48).

(1) CALL signal in. Part of the incoming signal (speech and signaling) from amplifier assembly 9A4 is applied through distribution panel 9A1 wiring to Pi-L of telephone signal converter 9A3. The signal is then applied through SENSITIVITY control R1 and capacitor C1 to the base of transistor Q1. FL1 in the Q1 collector circuit is tuned to 1,600 Hz  $\pm$ 4 Hz, and capacitor C2 provides fine frequency tuning of the selective circuit. The output from FL1 is then connected through normally-closed contacts 4 and 5 of RING switch S1 in monitor panel 9A2, back into telephone signal converter 9A3 and coupled by capacitor C3 to the base of transistor Q2. Q2, and FL2 in its collector circuit, form another highly selective amplifier tuned to 1,600 Hz  $\pm$ 4 Hz. Capacitor C4 provides fine frequency tuning of FL2. The output of Q3 is coupled through C5 to the base of Q3. Q3 and Q4 are emitter followers connected in cascade. In the presence of 1,600 Hz signaling frequency extracted by Q1-FL1 and Q2-FL2, the output at the emitter of Q4 is fed through C6 and R13 GAIN potentiometer, through normally-closed contacts 8 and 1 of RING switch S1 in monitor panel 9A2, back into telephone signal converter 9A3, to the base of detector Q5. Q5 operates CALL relay K1 which in turn closes the 26 v path through the BUZZER ON-OFF switch (in the ON position) in monitor panel 9A2, to the buzzer, and, through R1, to CALL lamp DS1. When the BUZZER ON-OFF switch is in its OFF position, the buzzer is bypassed, and the CALL lamp will glow at about half normal brightness due to series resistor R2.

(2) RING signal out. When the RING switch on monitor panel 9A2 is depressed, the output of FL2 in telephone signal converter 9A3 is connected through contacts 3 and 6 of the RING switch, and capacitor C3, to the base of transistor Q2, thus forming a Hartley-type oscillator which oscillates at 1,600 Hz  $\pm$ 4 Hz. The 1,600 Hz output is connected through C5 to emitter-followers Q3 and Q4. The output at the Q4 emitter is then connected through C6, GAIN control R13, and contacts 7 and 2 of the RING switch to Pi-E of amplifier assembly 9A4. The RING signal out is then fed through R13, C7 and C8 to the bases of transistors Q3 and Q4. The two separate ringing signals are then transmitted along the transmit speech paths to the TO RADIO and PATCH THRU connectors.

#### 2-57. Distribution Panel 9A1 (FO-4-78)

a. Distribution panel 9A1 (rear panel) contains all interconnecting circuits of the order wire unit including the TO RADIO and PATCH THRU connectors, resistor assembly board 9A1A1, two power distribution relays K1 and K2, and the buzzer. Power is fed to the order wire unit from the receiver to provide listening watch faci-

lities with the transmitter switched off. Two power distribution relays, K1 and K2, enable power to be supplied from either the TO RADIO or the PATCH THRU connector. When only one radio set is connected, as in a terminal, the 26 vdc at the TO RADIO connector operates K1 and K2 to route the 12 vdc to amplifier assembly 9A4 and to telephone signal converter 9A3, and the 26 vdc to monitor panel 9A2. When both radio sets are connected, as in a repeater, the same power distribution takes place; the second power source at the PATCH THRU connector stops at the opened contacts of K1 and K2. If a failure should occur in the radio set supplying power to the TO RADIO connector, the two relays will de-energize and supply power from the second radio set at the PATCH THRU connector to operate the order wire unit.

b. Resistor assembly 9A1A1 contains two 620 ohm resistors that change the order wire transmit level from -4 dbm to -10 dbm when the order wire facility is extended to Multiplexer TD-754/G or TD-204/U in a pcm terminal, 24-channel radio-to-cable configuration. When used in this configuration, J1-K or J2-K is grounded in the multiplexer; otherwise J1-K and J2-K remain open.

#### 2-58. Monitor Panel 9A2 (F0-4-78)

Monitor panel 9A2 (front panel) contains CALL and POWER lamps DS1 and DS2, BUZZER ON-OFF switch S2, RING switch S1, and resistor assembly 9A2A1, which contains indicator lamp resistors R1 and R3 and CALL lamp dimming resistor R2.

### Sect ion VI. AMPLIFIER-FREQUENCY MULTIPLIER AM-4321/GRC-103(V) AND AM-4321A/GRC-103(V)

#### 2-59. Functional Block Diagram Analysis of Amplifier-Frequency Multiplier AM-4321/GRC-103(V) and AM-4321A/GRC-103(V) (Fig. 2-77)

##### NOTE

There are two models of Frequency Multiplier 37A1, distinguishable by part numbers SM-D-696417 and SM-D-865053. This paragraph refers to both units unless otherwise specified.

The rf output of the transmitter fixed head in the frequency range of 95 to 145 MHz, at a level of 35 dbm, is fed into amplifier-frequency multiplier AM-4321/GRC-103(V) or AM-4321A/GRC-103(V) (Band II transmitter rf head) where it is multiplied and amplified to produce the final transmitter frequency.

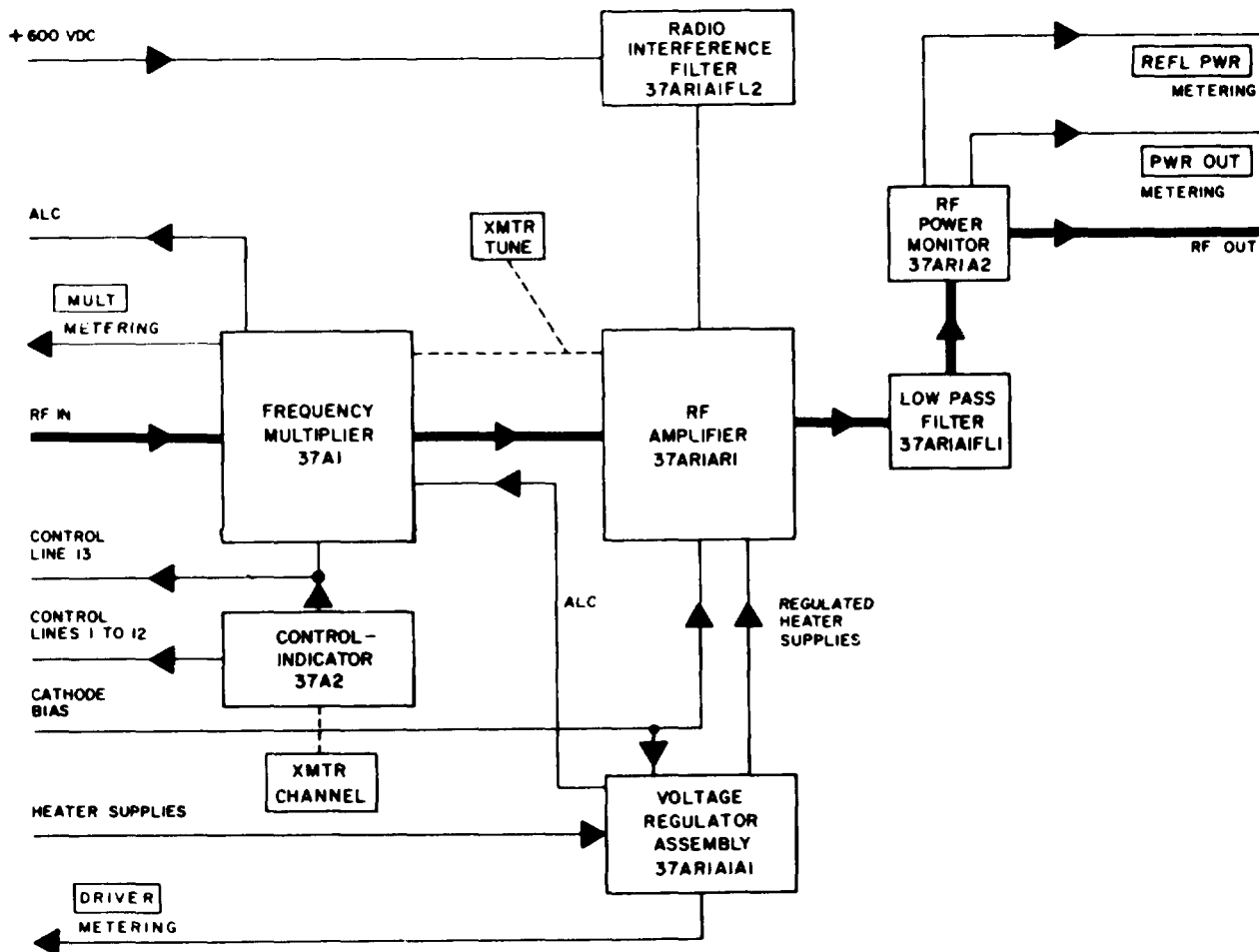
a. The transmitter rf head multiplication circuits provide the final multiplication required to produce the selected transmitter channel frequency. The multiplication is accomplished in frequency multiplier 37A1 which contains a frequency doubler and a variable multiplier which extracts the second or third harmonics of the doubled frequency. The multiplication factor of the variable frequency multiplier is selected by a switching circuit controlled by control line 13 from control-indicator 37A2. The frequency multiplier also produces an automatic load control (ale) voltage which limits the power level of the transmitter fixed head output. The output of the variable multiplier is selected in a tunable resonator which is ganged to XMTR TUNE front panel control. An impedance equalizer and a voltage con-



trolled attenuator are also contained, in frequency multiplier 37A1, to control the output level of the multiplier. The alc voltage to operate the voltage controlled attenuator is derived from voltage regulator assembly 37AR1A1A1. The output of 37A1 in the range of 395 to 705 MHz, at the minimum level of 23 dbm, is fed into rf amplifier 37AR1AR1.

b. The amplification of the output signal to the final output level is done in two-stage radio frequency amplifier 37AR1AR1 (driver and output amplifier), using two planar triodes type 7211 mounted in tuned-cathode, tuned-plate coaxial quarter-wave resonant cavities. The XMTR TUNE control, on the front panel, tunes the cathode and plate plungers of both stages. Output coupling of the resonators is done by capacitive probes which are geared to the XMTR TUNE control. The probes are fine-tuned by the PWR OUT PEAK control. The tubes are cooled by forced air. Due to the concentric cavity design, maximum exposure of the plate radiators to the air stream is accomplished.

c. Radio frequency amplifier 37AR1AR1 amplifies the final frequency of the transmitter at a level of 30 to 40 watts. The amplified rf signal is then fed through low pass filter 37AR1A1FL1 for spurious harmonic suppression. After rejection of



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Figure 2-77. Band II Transmitter RF Head, Block Diagram.

unwanted harmonics, the output signal is delivered through rf power monitor 37AR1A2 and the PWR OUT connector to amplifier-converter AM-4317/GRC-103(V) (Band II receiver rf head), and through a duplexer, to the antenna system. A sample of output power and reflected power is rectified in the power monitor and taken out as REFL PWR and PWR OUT metering signals.

d. Control-indicator 37A2 (channel selector) is an electromechanical device operating in conjunction with electrical frequency synthesizer and amplifier monitor in the transmitter fixed head. The channel selector provides 13 control lines. Control lines 1 to 12 inclusive program the frequency generating circuits in the electrical frequency synthesizer. Control line 13 is fed through amplifier frequency multiplier to the transmitter fixed head to control variable attenuators in amplifier-monitor 5TR1A5. Voltage regulator assembly 37AR1A1A1 supplies the regulated heater supply for the driver and output tubes.

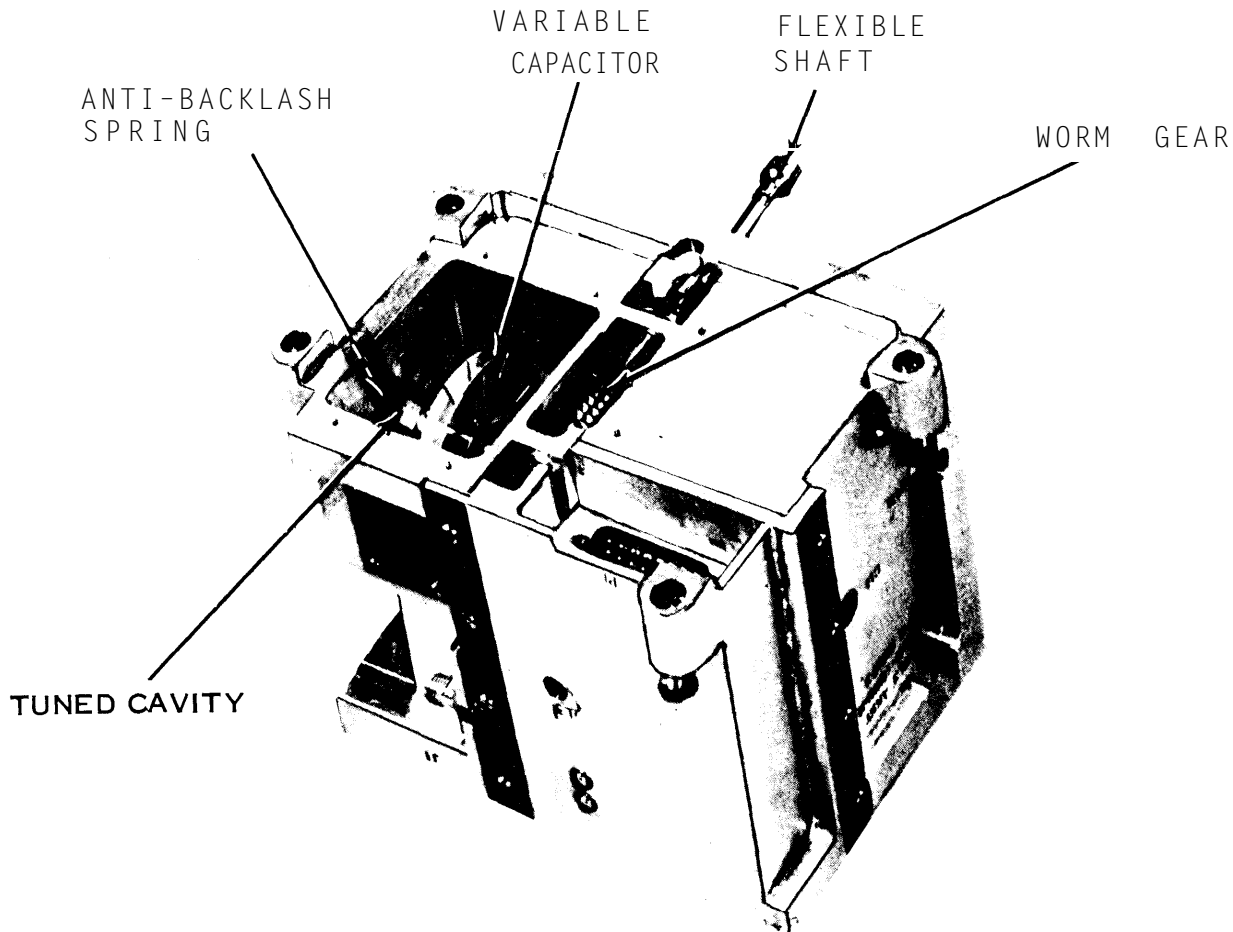
e. An overall schematic diagram of the Band II transmitter rf head, amplifier-frequency multiplier AM-4321/GRC-103(V), and AM-4321A/GRC-103(V) is shown in FO-4-67 and interconnection diagram is shown in FO-4-68.

#### NOTE

1. In many of the schematic diagrams, triangular symbols, identified by "Z" numbers, are used. These are in accordance with USA Standard Y32, 2-1967. Section 19, paragraph 15.1. They represent impedances introduced by ferrite beads, which are used extensively in certain sections of the receiver and transmitter rf heads for Bands II and III.
2. The words "END SEAL," inclosed in a rectangle, appear in several schematic diagrams. This symbol represents printed wiring board receptacles used with RG-188/U 50 ohm miniature coaxial cable. End seals are permanently soldered connections used to terminate the cable shield to ground. They may be of either straight or right-angle configuration.

2-60. Frequency Multiplier 37A1 (Part No. SM-D-696417 or SM-D-865053)

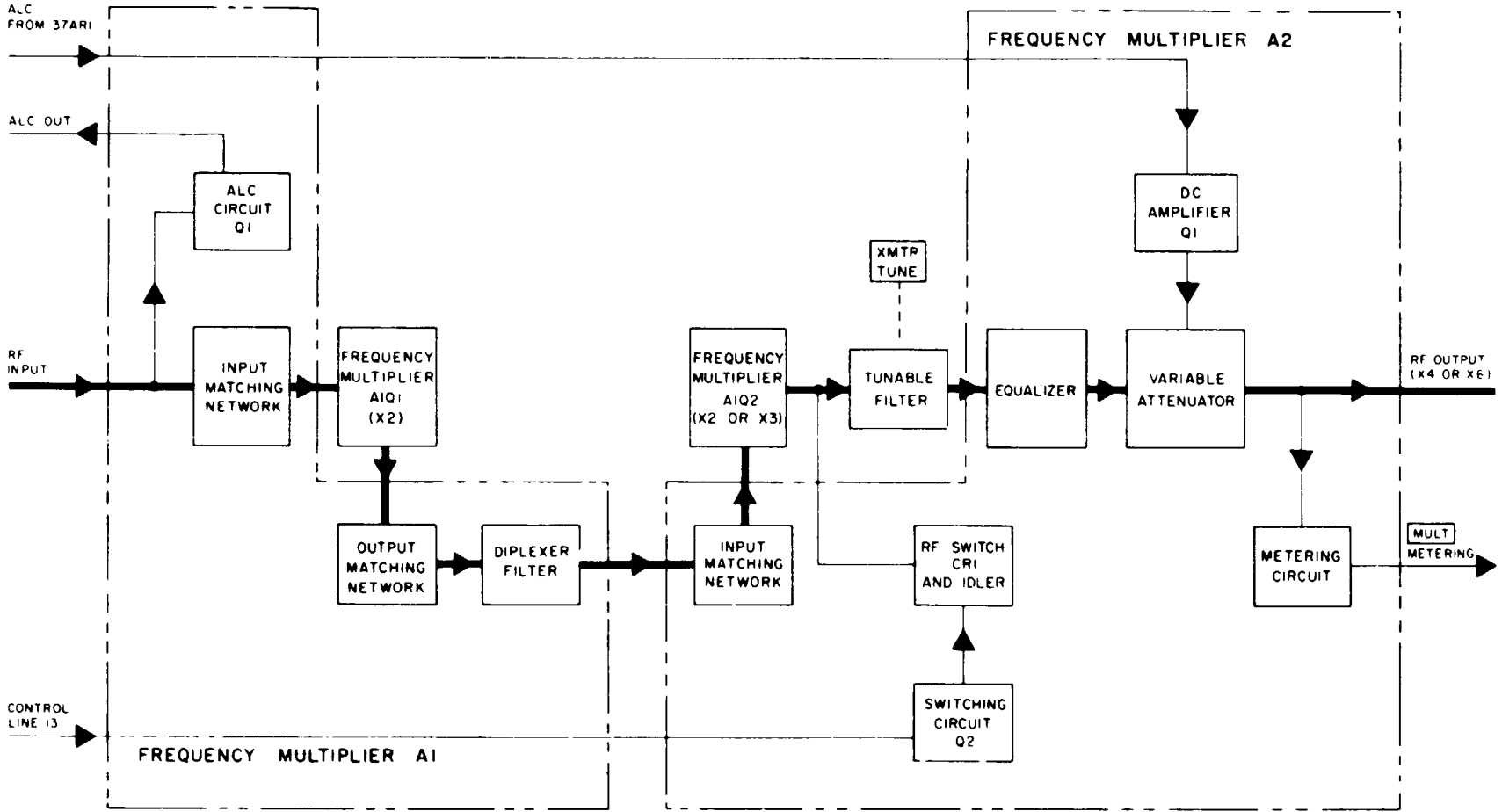
a. General. Frequency multiplier 37A1 multiplies the transmitter fixed head signal by four or by six to provide the input drive for radio frequency amplifier 37AR1. Frequency multiplier 37A1 consists of two transistor stages on separate printed wiring boards with the transistors mounted on the cast aluminum housing. The first transistor stage 37A1A1 is a wide-band frequency doubler and the second stage 37A1A2 is a variable frequency multiplier. The variable multiplier multiplies the doubled frequency by two or three as selected by a control signal from the control-indicator. The output frequency is selected in a tuned cavity filter which is ganged to the front panel XMTR TUNE control. The output level of the unit is automatically controlled by a signal from radio frequency amplifier 37AR1. The unit is contained in two precision cast aluminum housings. The major casting incorporates the tuning cavity as an integral part of the casting. The smaller casting supports the electrical connector and f i filters. The cavity is tuned by a variable capacitor mounted within the cavity (fig. 2-78). An antibacklash spring is fitted on the end of the capacitor rotor hub to reduce backlash. The XMTR TUNE control is coupled through a flexible shaft, worm and worm gear to the capacitor rotor.



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Figure 2-78. Frequency Multiplier 37A1, Bottom View.

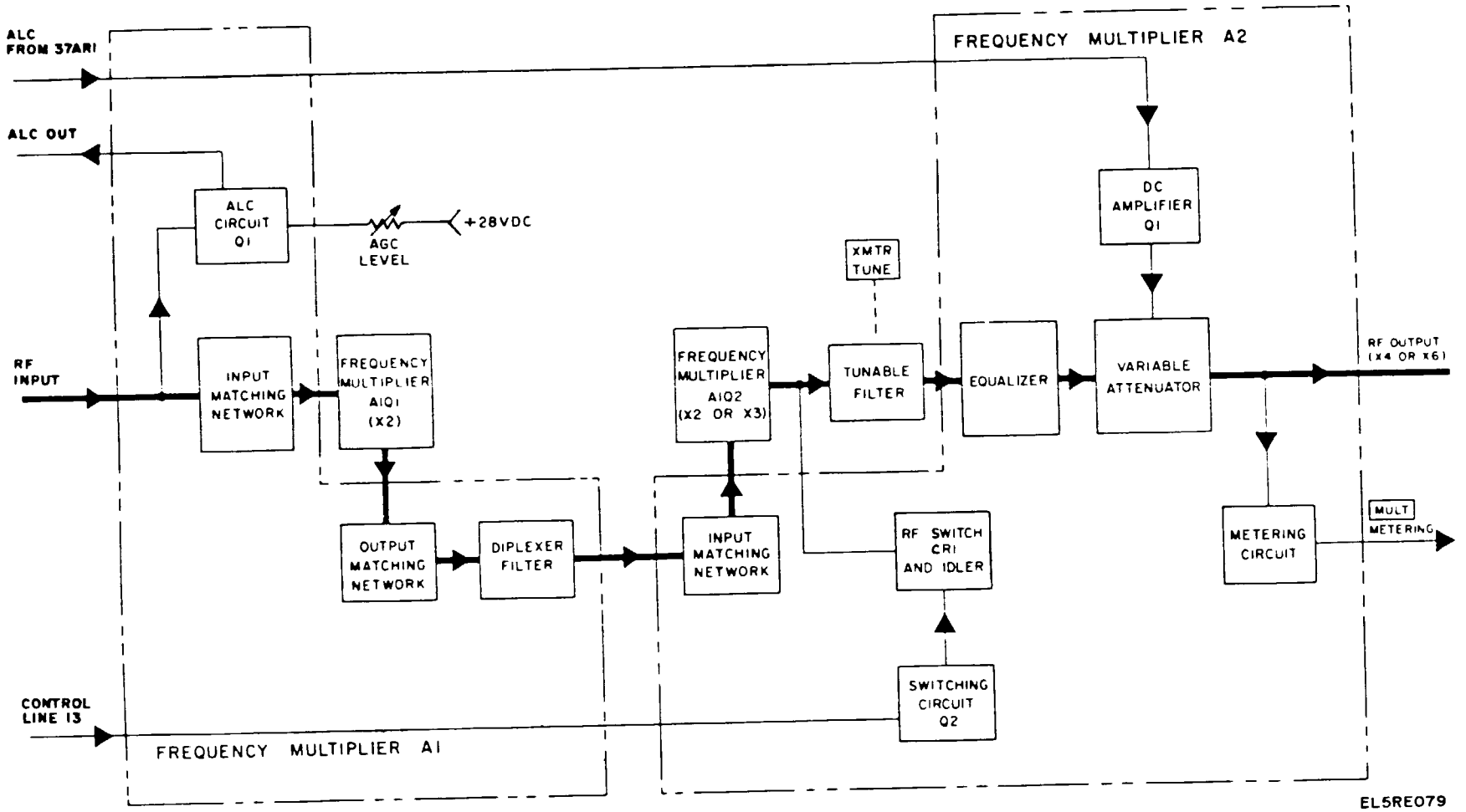
b. Block Diagram Analysis (Fig. 2-79) (Fig. 2-80 when Transmitter Equipped with SM-D-865053). the output of amplifier frequency Multiplier 5~TR1A4, in the range Of 95 to 145 MHz at a level of +35 dBm  $\pm$  1 db, is fed through the input matching network to the 0A1Q1 broadband doubler circuit. The rf power transistor A1Q1, amplifies the input fundamental frequency while the Collector to base capacitance acts as a varactor for harmonic generation. A portion of the rf input is fed to an alc circuit where the signal is rectified. The dc signal, proportional to the rf input is fed back to the transmitter fixed head to maintain the rf input at the required level. The output of the wideband doubler is fed through an output matching network to the diplexer filter which terminates the fundamental frequencies and provides a path for the second harmonics. The output of the diplexer filter is applied to variable frequency multiplier transistor 1AQ2 through the input matching network. The output of the variable frequency multiplier is a signal rich in second harmonics. When the third harmonic frequencies are required, control line 13 turns on transistor Q2 in the switching circuit, which then forward biases switching diode CR1. CR1 switches in an idler circuit which allows the second harmonics to mix with the fundamental frequency to produce third harmonic frequencies. The frequency multiplier output is fed to the tunable filter which is ganged to the front panel XMTR TUNE control. The filtered signal is fed to the constant impedance equalizer which reduces the amplitude at the low frequency end of the signal. The equalized signal



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Figure 2-79. Frequency Multiplier 37A1 (SM-D-696417), Block Diagram.

Figure 2-80. Frequency Multiplier 37A1 (SM-D-865053), Block Diagram.



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is fed to the variable attenuator which controls the output level. The alc voltage, from the voltage regulator in rf amplifier 37AR1, is amplified by dc amplifier Q1 and used to control the variable attenuator. The output of the attenuator is coupled to the output connector and fed to the rf amplifier 37AR1. A portion of the output signal is fed into the metering circuit where it is rectified and used as the MULT metering signal.

c. Detailed Circuit Analysis (F0-4-65).

(1) Input alc circuit.

(a) Transmitter equipped with SM-D-696417 (F0-4-65). A portion of the input rf signal applied to connector J1, is coupled through capacitor C1 to voltage divider R1, R2 and diode CR1 of the alc circuit. Normally CR1 is zero biased and is not conducting. The input signal fed through voltage divider R1, R2 provides approximately 5.1 volts peak-to-peak riding on 28 vdc. On the negative peaks of this signal, CR1 is forward biased thereby charging C3 to approximately 23 volts (28.0 - 5.1 volts). This in turn causes Q1 to conduct. The base current required to turn on Q1 is determined by R3 which is adjusted to give approximately 8.5 volts at E4. This voltage is used to operate the alc system in the transmitter fixed head. R4 is used to prevent the 28 volts dc from being applied to the emitter of Q1 if R3 is set to zero ohm. C2, C4 are rf decoupling capacitors. C5 is a feedthrough capacitor and prevents rf interference with the power supply line. R5 is the Q1 collector load.

(b) Transmitter equipped with SM-D-865053 (F0-4-66). The voltage applied to the input alc transistor 37A1A1Q1 is developed across resistor 37A1R2 through which passes the current consumed by the two multiplier stages 37A1Q1 and 37A1Q2. R3, the ALC LEVEL potentiometer, is set for maximum current through 37A1R2. When the incoming rf signal is too high, the voltage at the base of alc transistor Q1 causes its collector voltage (input alc) to increase; this increase in the input alc voltage applied to the alc circuit in the amplifier-frequency multiplier 5TR1A4 will cause a decrease of the rf output. The reverse is true for a weaker incoming rf signal. Since the input rf signal is a function of the dc current consumption, the supply current once set, controlling the input rf level becomes independent of multiplier transistor efficiency or transistor parameters. C6 provides rf decoupling and R4 is the collector load.

(2) Wide band doubler. The rf input to A1Q1 transistor multiplier is fed through an input matching network. The input matching network contains a bandpass network and an impedance transforming network. The bandpass network consists of C6, L1, C7 and L2, and is used to isolate the input driver stage from the multiplier output frequencies. The parallel resistive network R6 and R7, in series with 4:1 transformer T1, matches the input impedance of A1Q1. The fundamental frequency, from the input matching network, is coupled through dc blocking capacitor C8 to the base of A1Q1. R8 provides a small reverse bias on the base of A1Q1 for optimum efficiency. The 20 volt dc collector supply, for A1Q1 and A1Lj2, is derived from the +28 vdc line by Zener diode CR1. (In transmitter equipped with SM-D-865053 the collector supply for 37A1Q1 and 37A1Q2 is derived from the +28 vdc through 37A1R2.) L3 resonates the transistor output capacitance at the fundamental midband frequency while C9 provides a ground return through L3 to decouple the fundamental current. The capacitance between the base and collector of A1Q1 varies nonlinearly with transistor collector voltage. The transistor amplifies the fundamental which drives the variable base-collector junction capacitance producing a highly distorted output waveform. This waveform contains components of the fundamental and harmonic fre-

quencies. The A1Q1 output is fed through output matching network C11 and L4 to the diplexer filter.

(3) Diplexer filter. The diplexer filter is a power splitter providing a path to terminate the fundamental frequencies at one port and a path for the second harmonics at the third port. The diplexer is a combination low pass - high pass filter with seven sections. The fundamental frequencies are fed through the filter and terminated in R1. The second harmonics, fed through the filter to the outer port, are coupled through C18 to the variable frequency multiplier 37A1A2 circuit.

(4) Variable frequency multiplier. The output of the frequency doubler is fed to the base of frequency multiplier A1Q2 through an input impedance matching network. The input matching network provides an input vswr of 2:1 maximum. R1 and R2 are used to increase the resistive component of the input impedance to facilitate wideband matching. The output at the collector of A1Q2 is the signal rich in second or third harmonics. L3 and C8 form an idler circuit which resonates with the collector to base varactor capacitance at midband of the fundamental input frequencies to produce second harmonic frequencies. L4 and C16 are switched into the collector circuit to allow the second harmonic current to flow through the varactor capacitance to produce third harmonic frequencies. R4 at the collector provides a resistive load to the fundamental frequency power. The 20 vdc supply from zener diode CR1 is decoupled by feed through capacitor C9.

(5) Switching circuit. When third harmonics are required, transistor Q2 is turned on by +26 volts from control line 13. CR1 is forward biased by Q2 conducting, and idler circuit L4 and C16 is switched into the collector circuit of multiplier A1Q2. When second harmonics are required, transistor Q2 is turned off by a ground on control line 13. CR6 increases the minimum turn-on voltage of Q2 to over 1 volt to insure that Q2 turns off. When Q2 is turned off, CR1 is reverse biased and cuts off the third harmonic idler circuit.

(6) Output matching network. The output of the variable frequency multiplier is coupled through C14 to cavity filter Z1. The cavity filter is a coaxial line cavity capacitively tuned by air-dielectric variable capacitor C1. The tuning of the variable capacitor is done by the front panel XMTR TUNE control. Inductors L1 and L2 provide input and output coupling respectively, for constant bandwidth over the multiplier frequency range. From Z1, the output signal is fed through a constant impedance equalizer and then coupled to PIN diode attenuator CR2, CR3 and CR4.

(7) Constant impedance equalizer. The output power of the frequency multiplier is greater at the low frequency end than at the high frequency end. It is possible for the maximum power at the low frequency end to be +31 dbm, while the power at some higher frequency is +25 dbm. The alc controlled PIN diode attenuator CR2, CR3, CR4 cannot handle such high power due to partial rectification effect at high level operation. The constant impedance equalizer, R10, R11, R12, L5, C17, levels the output power so that the maximum power at the lower frequency end is reduced to +27 dbm while at the higher frequency end the maximum is maintained at +23 dbm. The equalized signal is coupled through C18 to the output attenuator.

(8) Output automatic level control. An alc positive voltage from power amplifier 37AR1, proportional to the input signal to 37AR1, is applied to the base of dc amplifier Q1 through C26 and R16. C25 and C26 decouple any rf that enters the Q1 base region. R16 presents a high dc resistance to the alc voltage source. C24 is used for rf decoupling at the collector and R14 is the collector load. R15 stabi-

lizes the dc voltage gain of Q1. The output loading of the transistor is essentially 1.8 kilohm and the maximum output voltage is approximately +14 vdc without ale. As the alc voltage rises, the output voltage of Q1 collector will drop. The output of the dc amplifier Q1 is fed to the PIN diode voltage controlled attenuator CR2, CR3, CR4 connected in a T-network. Voltage divider R5, R6, across the 28 volt supply, provides a reference voltage for the attenuator. When Q1 output voltage is high (minimum alc voltage), CR3 and CR4 are forward biased and produce a voltage drop across R7. The voltage across R7 is higher than the reference voltage, hence CR2 is reverse biased and turned off. The attenuation on the signal through CR3 and CR4 is minimal. As the alc voltage increases, the Q1 output voltage decreases, reducing the forward bias on (and current through) CR3 and CR4 until the voltage drop across R7 is less than the reference voltage. The reduced voltage drop across R7 forward biases CR2 which begins to conduct. The CR2 current flows through R7, CR3 and CR4 toward the dc amplifier, thereby increasing the attenuation of CR3 and CR4. In the extreme case, CR3 and CR4 are turned off when Q1 collector voltage drops to zero. C18, C27, C12 and C11 are dc blocking capacitors and L6 and L7 are rf chokes for dc paths.

(9) Metering circuit. A portion of rf is coupled to a directional coupler composed of two striplines on the printed circuit board. Since the coupling energy increases with increasing frequency, coil L8 is placed in series with detector diode CR5 to provide a constant rf drive to the diode. Rf decoupling is provided by C13. The detected rf is fed to the metering circuit in the transmitter fixed head for MULT meter indication.

## 2-61. Radio Frequency Amplifier 37AR1AR1

a. General. Radio frequency amplifier 37AR1AR1 amplifies the final transmitter frequency in the frequency range of 395 to 705 MHz to a level of 30 to 40 watts. The amplifier consists of two grounded-grid triode stages in cascade. The two stages of the amplifier are of identical construction. Each stage uses a planar triode type 7211 electron tube mounted in tuned-cathode, tuned-plate coaxial quarterwave resonant cavities. The cathode and plate resonators are tuned simultaneously, over the frequency range, by moving mechanically coupled plungers, ganged to the XMTR TUNE control on the front panel. Output coupling of the resonators is by capacitive probes which are also ganged to the XMTR TUNE control. Peaking of the amplifier output (output probe) is accomplished by adjusting the PWR OUT PEAK control on the front panel. A trimmer capacitor within the plate resonator is used to compensate for tube plate-to-grid capacitance differences.

b. Cavity Construction and Tuning Mechanism (Fig. 2-81). The heater connection to the amplifier tube is made through the hollow cathode lead screw inside the center conductor of the cathode-grid resonator. The lead screw is of a double-start nature to enable rapid transit of cathode tuning plungers. Cathode feed is taken through the input connector which is adjacent to the gear plate. This input signal is then passed through a 50 ohm coaxial feeder cable, firmly bonded to the outside of the grid-cathode resonator cavity, and fed through the cathode contact assembly to the cathode. Dc isolation is achieved within the cathode contact assembly. The plate supply is decoupled by a capacitor (bypass capacitor assembly) integral to the amplifier tube socket. The capacitor is a silvered mica disc in a potted assembly. Dc power to the tube plate is fed to the high voltage connection mounted on the plate side of the bypass capacitor assembly. Plate and cathode tuning is accomplished by varying the position of the respective short circuit tuning plungers. The short circuit to the resonator walls is made through sets of flexible silver-



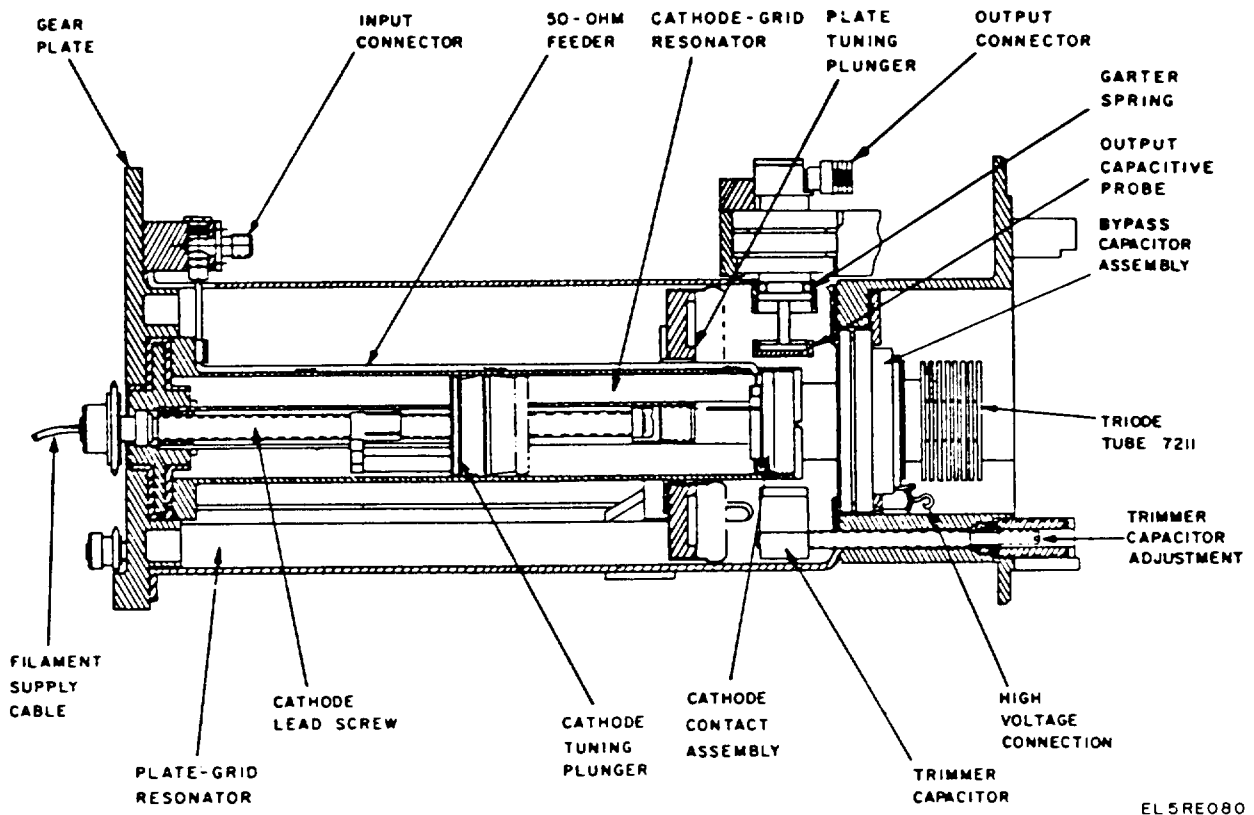


Figure 2-81. RF Amplifier 37AR1AR1 , Resonator Cavity Cross-Section View.

plated fingers. The resonator frequency will increase as the short circuiting plunger is moved toward the tube. The output capacitive probe is located at the tube end of the plate-grid resonator and tracks with the resonator tuning mechanism. The PWR OUT PEAK control overrides this mechanical tracking to permit final probe positioning for optimum output power.

c. Detailed Circuit Analysis (Fig. 2-82).

(1) The output of frequency multiplier 37A1, in the frequency range of 395 - 705 MHz, is fed through input connector J1 to the cathode of driver tube V1. Driver tube V1 and output tube V2 are identical and are connected in a grounded-grid configuration. Common grid configuration is used to minimize amplifier feedback effects due to triode interelectrode capacitance. Z1 and Z5 are cathode-grid resonant cavities; Z4 and Z8 are plate-grid resonant cavities for the driver and output stages respectively. C5 and C12 are feed-through capacitors for the regulated heater supply to the driver and output stages. C7 and C14 are the feed through capacitors for high voltage plate supply to both the stages. C1, C3, and C8, C10 are bypass capacitors and provide dc isolation. C4 is a trimmer capacitor in parallel with the plate-grid circuit and is used to compensate the electron tube plate-grid capacitance spread of the driver stage. C11 is the trimmer capacitor in the output stage. C15, R1 is a suppressor loop in the driver stage and C16, R2 is a suppressor loop in the output stage. These suppressor loops prevent any self-oscillation during mismatch conditions.

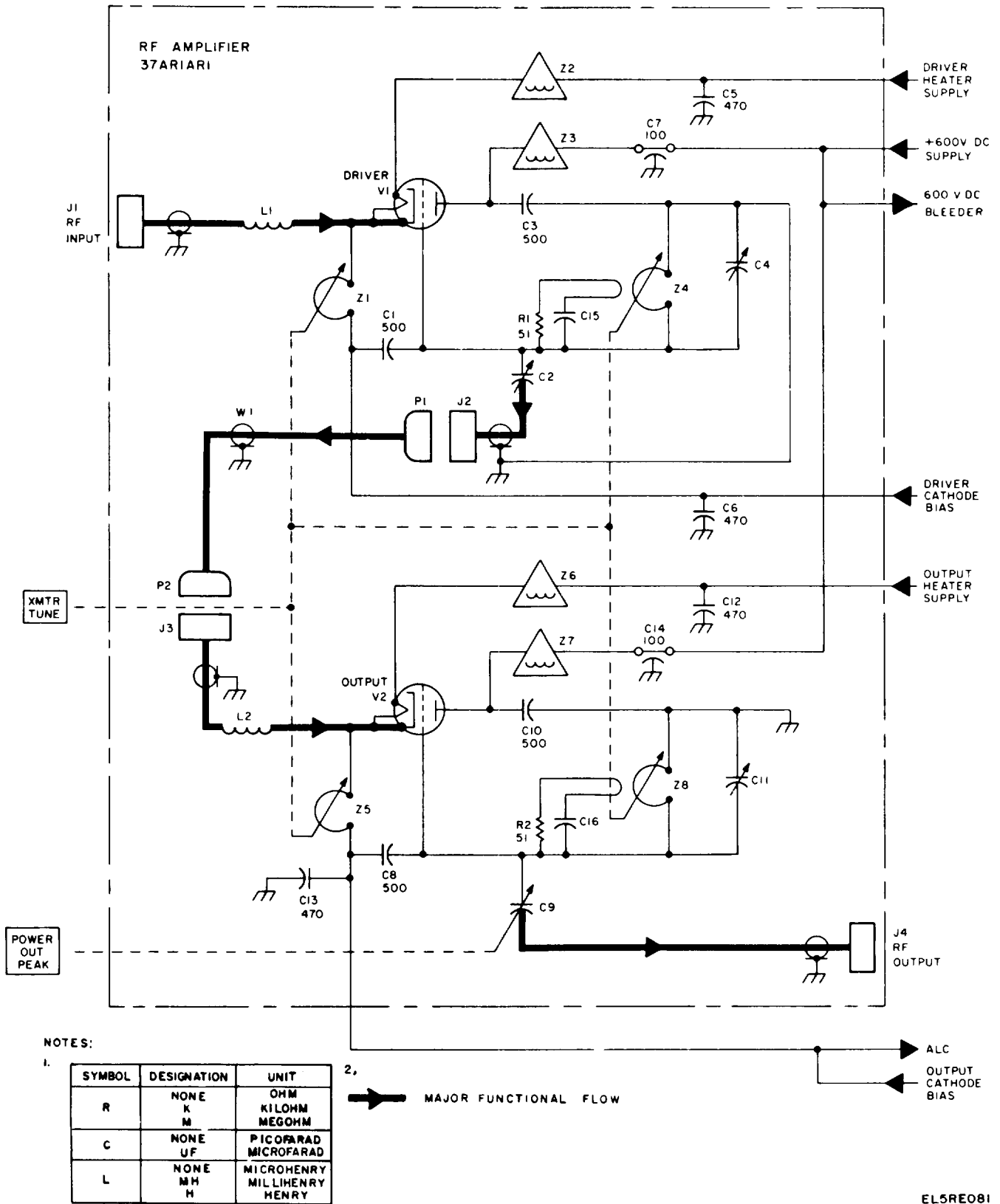


Figure 2-82. RF Amplifier 37ARIAR1, Schematic Diagram.

(2) The input signal when fed to the cathode of driver tube V1, excites cathode resonator Z1 connected between cathode and grid of V1. The signal, amplified by approximately 13 db at the plate of V1, resonates in Z4 (connected between plate and grid) and is coupled from the cavity to output connector J2 through the coupling probe C2. The output from the driver tube is connected through connector P1, coaxial cable W1, coaxial connectors P2 and J3 to the cathode of the output stage V2. Output stage V2 is electrically and mechanically similar to the driver stage. The output cathode bias changes are fed to the heater voltage regulator assembly to produce an alc voltage for frequency multiplier 37A1. This alc voltage controls the output of the frequency multiplier (input to the power amplifier). The output stage provides a further amplification of about 10 db. The final amplified signal is fed through coupling probe C9 to output coaxial connector J4. Output coupling probe C9 is ganged to front panel controls XMTR TUNE and PWR OUT PEAK. Cathode currents are regulated by a constant current source within transmitter power supply 5TR1PS1. Plate supply for the tubes is 630 volts dc at about 180 milliamperes, and is supplied through radio frequency interference filter 37AR1A1FL2 which suppresses any 5 kHz components on the 630 volt supply. Resistor assembly 37AR1A1A2 bleeds off any residual high voltage when the unit is disconnected. Channel-frequency indicator DS1 is ganged to the XNTR TUNE control and provides a visual indication of the selected channel.

## 2-62. Voltage Regulator Assembly 37AR1A1A1, 38AR1A1A1 or 40A3

a. General. The voltage regulator assembly regulates the heater supply voltages to the transmitter rf power amplifier tubes. It also provides an alc reference circuit, metering voltages, and two resistive paths which control the constant cathode current regulators in the transmitter fixed head power supply. The unit consists of the following functional circuits:

(1) Two identical heater voltage regulator circuits, one for the driver and the other for the output stage of the rf power amplifier.

(2) An alc reference circuit using the bias potential from the cathode of the output stage of the rf power amplifier as the input.

(3) A metering circuit for monitoring dc bias at the cathode of the output stage (DRIVER metering).

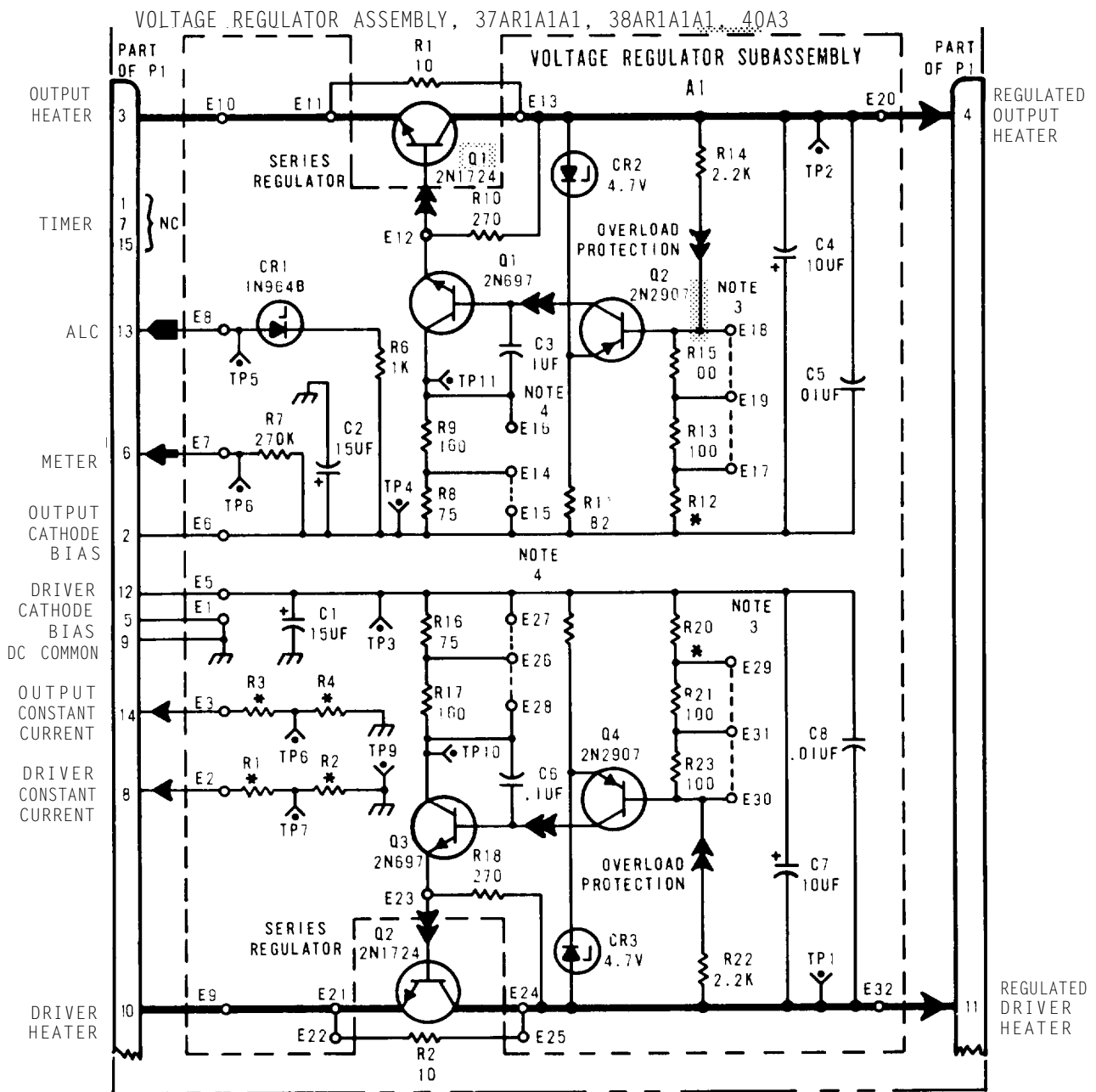
(4) Two resistive paths which form part of the driver and output constant cathode current circuits located in the transmitter fixed head power supply.

### NOTE

Since the two heater voltage regulator circuits are identical, only the output stage regulator is explained in the following paragraph, together with the other circuits explained in a (2), (3) and (4) above.

### b. Detailed Circuit Analysis (Fig. 2-83).

(1) Regulator circuit. The 7.2 vdc heater supply voltage from the transmitter fixed head power supply F0-4-40 is fed to the emitter of transistor A1Q2 which acts as a series regulator controlling the output voltage at a constant value of 6.2 vac (+0.4 v) on 37AR1A1A1 and 38AR1A1A1 or 5.8 vdc (+0.4 v) on 40A3. Two different vol -



NOTES: 1

| SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM          |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

3-E17, E18, AND E19 ARE STRAPPED TO SET OUTPUT HEATER REGULATED VOLTAGE. E29, E30 AND E31 ARE STRAPPED TO SET DRIVER HEATER REGULATED VOLTAGE.

4-E14, E15 AND E16 ARE STRAPPED TO SET Q1 COLLECTOR VOLTAGE. E26, E27 AND E28 ARE STRAPPED TO SET Q3 COLLECTOR VOLTAGE.

★ TABLE

|     | 37AR1A1A1 | 38AR1A1A1 | 40A3 |
|-----|-----------|-----------|------|
| R1  | 22        | 13        |      |
| R2  | 12        | 9.1       |      |
| R3  | 6.8       | 7.5       |      |
| R4  | 5.1       | 5.6       |      |
| R12 | 1.1K      | 910       |      |
| R20 | 1.1K      | 910       |      |

- 2 -
- ➔ MAJOR FUNCTIONAL FLOW
  - ➔ SECONDARY FUNCTIONAL FLOW
  - ➔ DC METERING FLOW
  - ➔ FEEDBACK SIGNAL PATH
  - ➔ REFERENCE SIGNAL VOLTAGE

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Figure 2-83. Voltage Regulator Assembly 37AR1A1A1, 38AR1A1A1 and 40A3, Schematic Diagram.

tages are obtained by selection of resistors R12 and R2U. Zener diode CR2 and R11 maintain the emitter potential of Q2 at a constant value with respect to the negative line of the regulator output. Q2 base voltage divider, R12, R13, R14 and R15, samples the output voltage. Any variation in the output voltage will cause the Q2 emitter-base voltage to vary, resulting in a corresponding variation in the collector current. These collector current variations are amplified in Q1 and used to control the base current of A1Q1, which causes the output of A1Q1 to change in such a way as to compensate for the change in output voltage and bring it back to the original value. The base voltage divider of Q2 is adjustable to compensate for component tolerances. The correct voltage division is required to obtain the output voltage limits specified above. Capacitor C3, between the base and the collector of Q1, neutralizes any oscillation of the regulator circuit. Capacitor C4, shunted by capacitor C5, further stabilizes the circuit and suppresses any ripples or spikes at the output. Q1 collector resistors R8 and R9 provide short circuit current limiting. This resistance is made adjustable to achieve short circuit current limits in the range from 1.6 to 2.8 A. Resistors R10 and A1R1 are the starting resistors. In the initial state of operation, the tube is cold and the filament resistance (load resistance) is so low that the output heater voltage drops between 2.5 vdc, cutting off CR2. The Q1 collector current then reduces to its cutoff value. A1Q1 base current will then be effectively determined by R10 and the input voltage. R10 and A1R1 draw sufficient current, in this initial state, to heat up the filament. The regulator circuit operates normally after approximately 15 seconds. During normal operation, the current through R10 and A1R1 is minimal and regulation is not impaired.

(2) A1c circuit. The output cathode bias supply is connected to E6 and fed through current limiting resistor R6 to 13 volt dc Zener diode CR1. R6 and CR1 stabilize the voltage between TP4 and TP5 at approximately 14 vdc which is the normal cathode voltage level to the output tube. When this voltage increases, due to a higher input drive to the output tube, CR1 conducts. The resultant a1c voltage is fed through P1 pin 13 to the respective amplifier-frequency multiplier (37A1, 38A1 or 40A2).

(3) Metering circuit. The metering circuit consists of resistor R7 and capacitor C2. The cathode bias is connected through series resistor R7 to the front panel meter to indicate the cathode bias level of the power amplified output stage. Smoothing capacitor C2 removes any ripple from the dc supply and smoothes out the bias variations due to frequency changes of the modulated signal.

(4) Resistive paths for constant current supply. R1 and R2 are connected in the emitter line of the constant cathode current source transistor (transmitter fixed head power supply) (F0-4-40) for the driver stage. R1 and R2 effectively limit the maximum current in the emitter circuit. Test point TP7 is provided to measure the voltage level between the two resistors. This voltage level is used to determine the constant cathode current level. R3 and R4 form a similar arrangement for the constant cathode current of the power amplifier output stage.

## 2-63. Low Pass Filter 37AR1A1FL1

Low pass filter 37AR1A1FL1 is connected between the output of rf amplifier 37AR1AR1 and power monitor 37AR1A2. Low pass filter 37AR1A1FL1 is a sealed, high-power filter with a sharp cutoff above 1,000 MHz. It filters out any spurious harmonics of the transmitter output rf signal.

## 2-64. Rf Power Monitor 37AR1A2 or 38AR1A2

Rf power monitor 37AR1A2 or 38AR1A2 is connected between the low pass filter and the PWR OUT connector. The rf power monitor consists of two bidirectional couplers placed back-to-back in a sealed unit. One coupler monitors the output power of the transmitter and the other monitors the power reflected back to the transmitter. Both forward and reverse signals are rectified to produce dc metering signals. The forward power metering is fed to the meter through the selector switch in the PWR OUT position. It is also fed in parallel to alarm control 5TR1A3 (para 2-20). Alarm control 5TR1A3 will initiate a LOW POWER alarm if the transmitter output power should drop by 8 db to about 4 watts. A 5,000 ohm resistor is switched into the circuit when the meter selector switch is in any other position, so that the monitor signal will not be disturbed by switching the meter to the PWR OUT position. The reverse power metering signal is fed to the meter through the selector switch in the REFL PWR position. This metering function is used primarily to assist the operator while tuning the XMTR DUPL tuning control on the receiver rf head. Minimum meter reading indicates correct tuning of the transmitter position of the duplexer in the receiver rf head.

## 2-65. Control-Indicator 37A2 or 33A4

a. General. Control-indicators 37A2 (F0-4-67) (transmitter channel selector) and 33A4 (receiver channel selector) are identical in function and construction and also similar to control-indicator 6A3 (fig. 2-49). Each channel selector provides 12 control lines (2 through 13) to the frequency synthesizer in the transmitter or receiver. To select the required synthesizer frequency, control lines 2 to 12 are switched on and off in a binary pattern with line 13 switched between channels 759 and 760 to change the synthesizer output frequency steps. The switching modules are operated by a set of cams and followers which reflect the various coding patterns as shown in the coding tables (F0-4-51).

b. Description of Operation. The control-indicator consists of a set of 11 microswitches and a logic module (command signal decoder). The microswitches are operated by a set of cams to generate the binary code which presets the required stages of the programmed counter in synthesizer 5TR1A2 or 1RE1A2. The front panel channel-indicators consist of a series of numbered wheels. The indicating wheels are geared to the microswitch cams and to a front panel control knob. The transmitter channel selector display indicates the channel rather than the frequency selected. The following formulas should be used to translate a selected channel into a frequency and vice versa.

$$\text{Transmitter frequency} = \frac{\text{Transmitter Channel}}{2} + 200 \text{ MHz}$$

$$\text{Transmitter Channel} = (\text{Transmitter frequency} - 200) \times 2$$

c. Receiver Coding. On the receiver channel selector the coding is arranged to produce a local oscillator frequency 30 MHz higher than the channel indicated in the display. This is done to permit the indicator to refer to the received signal frequency, the actual local oscillator frequency being always 30 MHz higher to provide the correct intermediate frequency. The decoder unit is an encapsulated logic circuit designed to sense channel coding on the 11 microswitch output lines and initiate control line 13 switching to establish multiplication changeover, which takes

place between channels 759 and 760 in the transmitter and channels 699 and 700 in the receiver.

## Section VII. AMPLIFIER-CONVERTER AM-4317/GRC-103(V)

### 2-66. Functional Block Diagram Analysis of Amplifier-Converter AM-4317 GRC-103(V) (FO-4-56)

a. Amplifier-Converter AM-4317/GRC-103(V) (Band II receiver rf head) incorporates a duplexing system which enables the radio set to use a single antenna for both transmit and receive sections, and circuits which convert the incoming signal into a 30 MHz intermediate frequency.

b. Receiver rf head duplexer 33A1 provides the necessary isolation and impedance matching between the transmitted and received signals. The transmit signal at the PWR OUT connector of the transmitter rf head at a level of 25 watts is fed through an external rf coaxial cable, through the FROM XMTR connector on the front panel of the receiver rf head to duplexer subassembly 33A1A1. In the duplexer subassembly, the transmit signal is fed to a tuned two-cavity filter (resonator). The tunable transmit filter is manually tuned to the transmit channel by the XMTR DUPL control. The  $\pm 2$  MHz bandwidth of the filter provides additional filtering of the transmitted signal while presenting a high attenuation to the received frequency. The transmitted signal is then directed through impedance matching network 33A1A1Z1 and rf power monitor 33A3 to the ANT. connector, and through an rf coaxial cable to the antenna system. Rf power monitor 33A3 samples the forward and reflected rf power to and from the antenna system. These samples are rectified and the resulting dc voltages are used for XMTR DUPL and REFL PWR metering.

c. The receiving circuits of the receiver rf head accept modulated signals in the frequency range of 395 to 705 MHz, at a level of -54 dbm to -94 dbm and convert them to a 30 MHz intermediate frequency (IF) which is then amplified and demodulated in the receiver fixed head. The signals from the antenna, applied to the ANT. connector by the lead-in cable, are fed through impedance matching network 33A1A1Z1 to a 3 MHz bandwidth, tunable four-cavity filter (receiver section of duplexer subassembly). The tunable receive filter is manually tuned to the receive channel by the RCVR SIG control. The received signal is then fed through a high signal protection circuit (Signal Level Control-Monitor) which prevents rf signals greater than +15 dbm nominal from getting into the receiver. The signal level control-monitor also monitors the protection level and triggers the HIGH SIGNAL ALARM circuit when the input level at the antenna port exceeds +15 dbm.

d. The rf signals are fed through low pass filter 33FL1 which attenuates all harmonics of the incoming frequency. The output of the low pass filter is fed into the frequency mixer stage 33A7. The frequency mixer stage consists of two subassemblies, radio frequency amplifier 33A7AR1 and frequency mixer stage 33A7A1. The radio frequency amplifier contains a voltage-tuned bandpass filter which tracks with the receiver section of the duplexer and rejects image frequencies. The radio frequency amplifier 33A7AR1 has a nominal gain of 13.5-db, including the filter loss, over the frequency range of 395 to 705 MHz. The amplified signal is fed into the frequency mixer stage 33A7A1 where the received rf signals mixed with the local oscillator signal to produce the 3U MHz IF. The frequency mixer stage 33A7A1 con-

sists of a wideband balanced mixer with a nominal conversion loss of 7 db and a local oscillator metering circuit.

e. The input to frequency multiplier group 33A2 is the output of amplifier-frequency multiplier 1RE1A5, in the range of 95 to 145 MHz. The frequency multiplier group 33A2 consists of three modules, frequency multiplier 33A2A2, frequency multiplier 33A2A1 and bandpass filter 33A2FL1. Frequency multiplier 33A2A2 doubles the input frequency from 1RE1A5. The resultant frequency from 33A2A2 is applied to the second module, frequency multiplier 33A2A1, which doubles the frequency over one portion of the band and triples it over the remaining portion, to produce a continuously variable output frequency 30 MHz above the frequency of the received signal. Mechanically, frequency multiplier 33A2A1 is ganged to the RCVR SIG control which also drives bandpass filter 33A2FL1, the third module of the frequency multiplier group. Bandpass filter 33A2FL1 attenuates the unwanted submultiple of the output frequency from the frequency multipliers. The RCVR SIG control adjusts variable frequency multiplier 33A2A1 and bandpass filter 33A2FL1 to a point near the required tuning point, approximately 30 MHz above the frequency of the received signal. The MULT PEAK control then tunes the variable frequency multiplier and the bandpass filter to the required tuning point. The ganging of the RCVR SIG and MULT PEAK is such that the output frequency from frequency multiplier group 33A2 (local oscillator) is always 30 MHz above the duplexer receiver section. The local oscillator signal is then fed into frequency mixer stage 33A7A1 where it is amplified and then mixed with received rf signal to produce a 30 MHz IF signal. A portion of the local oscillator signal is detected and rectified in frequency mixer stage 33A7 to provide the MULT metering voltage. The IF signal from the mixer stage is amplified in intermediate frequency amplifier 33AR1. Intermediate frequency amplifier 33AR1 is part of the IF amplification system which also includes bandpass filter 1RE1FL1 and intermediate frequency amplifier 1RE1AR2 in the receiver fixed head. Intermediate frequency amplifier 33AR1 has a nominal gain of 50 db without agc and a maximum gain of 10 db with maximum age. Automatic gain control of two stages in each of the two IF amplifiers provides automatic adjustment of overall gain over a range of 50 db, depending on the input signal. Intermediate frequency amplifier 33AR1 is a broadband device, all shaping being done in bandpass filter 1RE1FL1 (para 2-43).

f. Operating voltages, +12 v and -12 v regulated and 26 v unregulated, required for-the circuits in the receiver rf head, are supplied by power supply 1RE1PS1 in the receiver fixed head. An overall schematic diagram of the Band 11 receiver rf head is shown in F0-4-57 and the interconnecting diagram is shown in F0-4-58.

## 2-67. Duplexer Subassembly 33A1A1

a. General. Since Radio Set AN/GRC-103(V) operates with a single antenna, duplexer subassembly 33A1A1, part of duplexer 33A1, provides the necessary isolation between the transmitted and the received signal. The duplexer subassembly, basically consists of two coaxial cavity filters with a common port (ANT. connector); one filter provides filtering of the transmitter signal and the other filters the received signal. The duplexer subassembly also contains an impedance matching network 33A1A1Z1 which matches the transmit and receive filters to the antenna over the entire frequency range; S1 is a shorting device used during the alignment of transmit cavity Z7 and receive cavities Z2, Z3. In addition to the cavity filters and impedance matching network, the duplexer subassembly also contains the gearing and mechanical drive for the voltage control assembly 33A1A2 and frequency multiplier group 33A2. The chassis of the duplexer subassembly is the main structural member of the amplifier-converter AM-4317/GRC-103(V).



b. Detailed Circuit Analysis (F0-4-57).

consists Transmitting path. The transmitter portion of the duplexer subassembly of two quarter-wave resonant tuned cavities, 33A1A1Z6 and 33A1A1Z7. The cavities are connected in series through an intercavity coupling network. The coupling network provides the correct impedance transformation between adjacent resonators for realization of proper filter response. Both cavities are tuned in parallel with adjustable plungers controlled by the XMTR DUPL front panel control. The channel to which the transmitter cavities are tuned is indicated by channel-frequency indicator 33A1A1DS2 in the XMTR CHANNEL display window. The input and output of the resonators are connected through the end resonator coupling networks which transform the 50 ohm impedance of the system up to the correct level required by the resonators, for realization of the proper filter response. The filter has a passband of  $\pm 2$  MHz and an insertion loss of 1.5 db for 90 percent of the band and 2.0 db for the remainder. The output of the filter, from the end resonator coupling network, is fed to the impedance matching network 33A1A1Z1 which matches the impedance of the transmitter to the antenna. The transmitter output is then fed through power monitor 33A3 to the antenna. Power monitor 33A3 measures the forward and reverse (reflected) power of the transmitted signal. Spark protection during tuning is afforded the cavities by spark gaps E2 and E4.

(2) Receiving path. The received signal from the antenna is connected through power monitor 33A3 and impedance matching network 33A1A1Z1 to the end resonator coupling network of the receiver cavity filter. The receiver portion of the duplexer subassembly consists of four quarter-wave resonant tuned cavities, 33A1A1Z2 to 33A1A1Z5. The cavities are connected in series through intercavity coupling networks. Spark protection during tuning is afforded the cavities by spark gaps E1, E3, E5 and E6. The coupling networks provide the correct impedance transformation between adjacent resonators. All four cavities are tuned in parallel by adjustable plungers controlled by RCVR SIG front panel knob. The channel to which the receiver cavities are tuned is indicated by channel-frequency indicator 33A1A1DS1 in RCVR CHANNEL display window. The receiver filter has a pass band of  $\pm 3$  MHz and an insertion loss of 2.0 db for 90% of the band and 2.5 db for the remainder of the band. The input and output of the resonators are coupled through end coupling networks which provide the correct source and termination impedance for the filters.

(3) Coupling networks. A coupling network between two adjacent resonators is provided to give the correct impedance transformation. The required characteristics are achieved by using a T-network of L-C circuits. These coupling networks between resonators Z1, Z3, Z4 and Z5, in the receive section, are identical except for the value of their components. A typical coupling network, such as that between resonator Z2 and Z3 consists of a series inductor L4 in parallel with variable capacitor C5, a series inductor L8 in parallel with variable capacitor C6 and a variable shunt inductor L6. Z11 in parallel with L6 is the stray capacitance existing between the coils when located in their housing. The coupling network between resonator Z6 and Z7 in the transmit section consists of series inductors L3, L7 and a variable shunt inductor L5. Z10 in parallel with L3 is the stray capacitance of L3 and similarly Z12 and Z13 are stray capacitances of L5 and L7 respectively.

(4) End resonator coupling network. The input and output end resonators of the receive and transmit filters are terminated in special coupling networks. These networks transform the 50 ohm impedance of the system up to the correct level required by the resonators. The input network in the receive filter consists of a variable inductor L2 in parallel with Z9. Z9 is the capacitance of the coil. A si-

milar network at the output consists of variable inductor L16 and parallel capacitor Z17. The input and output networks in the transmit section are similar except that the inductors are fixed, but the capacitance due to these fixed inductors can be varied.

(5) Impedance matching network 33 A1A1Z1. This unit provides a common junction for the transmit and receive filters. The network consists of a T-junction. One arm is a 50 ohm transmission line which terminates at the duplexer connector J1 and the other two arms of the T are identical, 100 ohm transmission lines. The two 100 ohm arms are connected in series with their respective filter at the resonator coupling network coil. The electrical length of these two arms changes with the on-tune and off-tune frequencies and thereby maintains the proper match between transmit and receiver filters to the antenna over the entire frequency range of 390 to 705 MHz.

(6) Tuning mechanism. The tuning of duplexer subassembly 33A1A1 and variable frequency multiplier 33A2A1, is accomplished through two main shafts mounted on the duplexer chassis. One shaft tunes the transmitter section of the duplexer subassembly and the other shaft tunes the receiver section of the duplexer subassembly and the frequency multiplier. The transmitter section drive shaft, connected to the XMTR DUPL control through reduction gears (fig. 2-84), carries three bevel gears. Two bevel gears drive the two individual center conductor drive screws of the resonant cavities and the third gear drives the XMTR CHANNEL indicator. Similarly, the receiver drive shaft, connected to the RCVR SIG control through

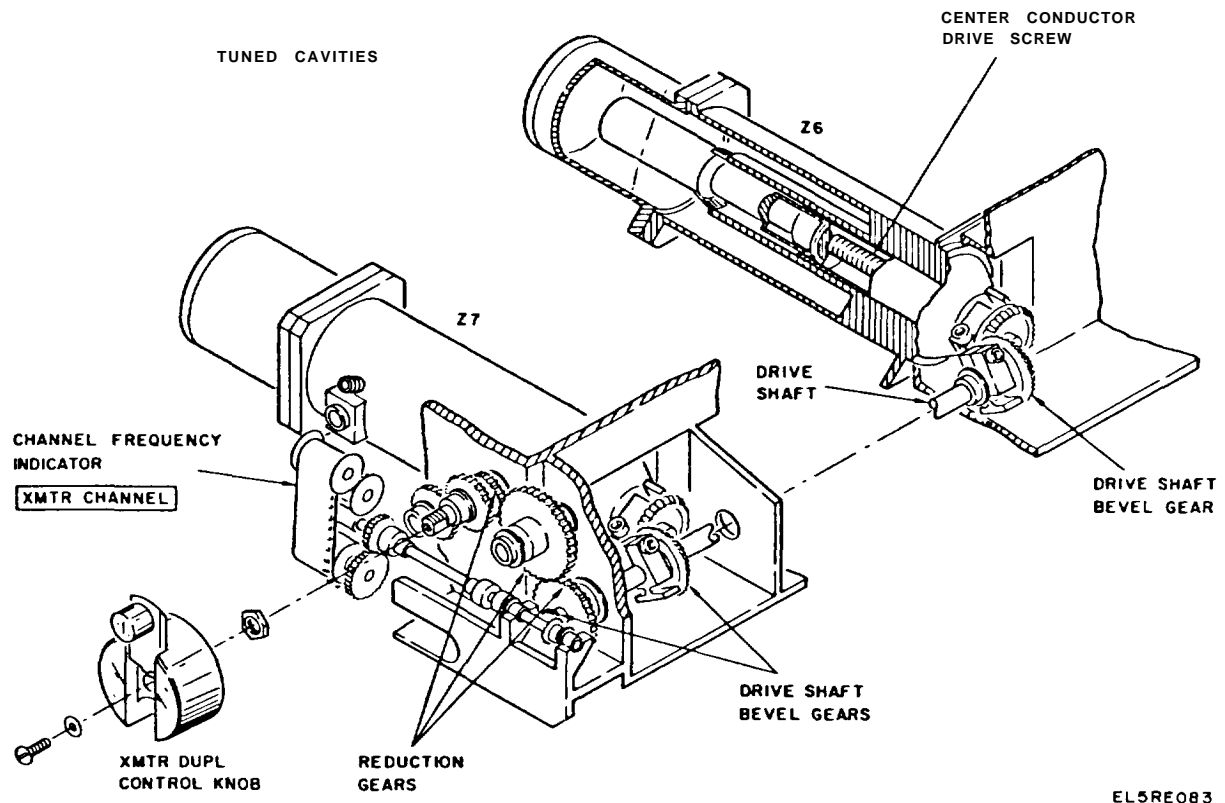


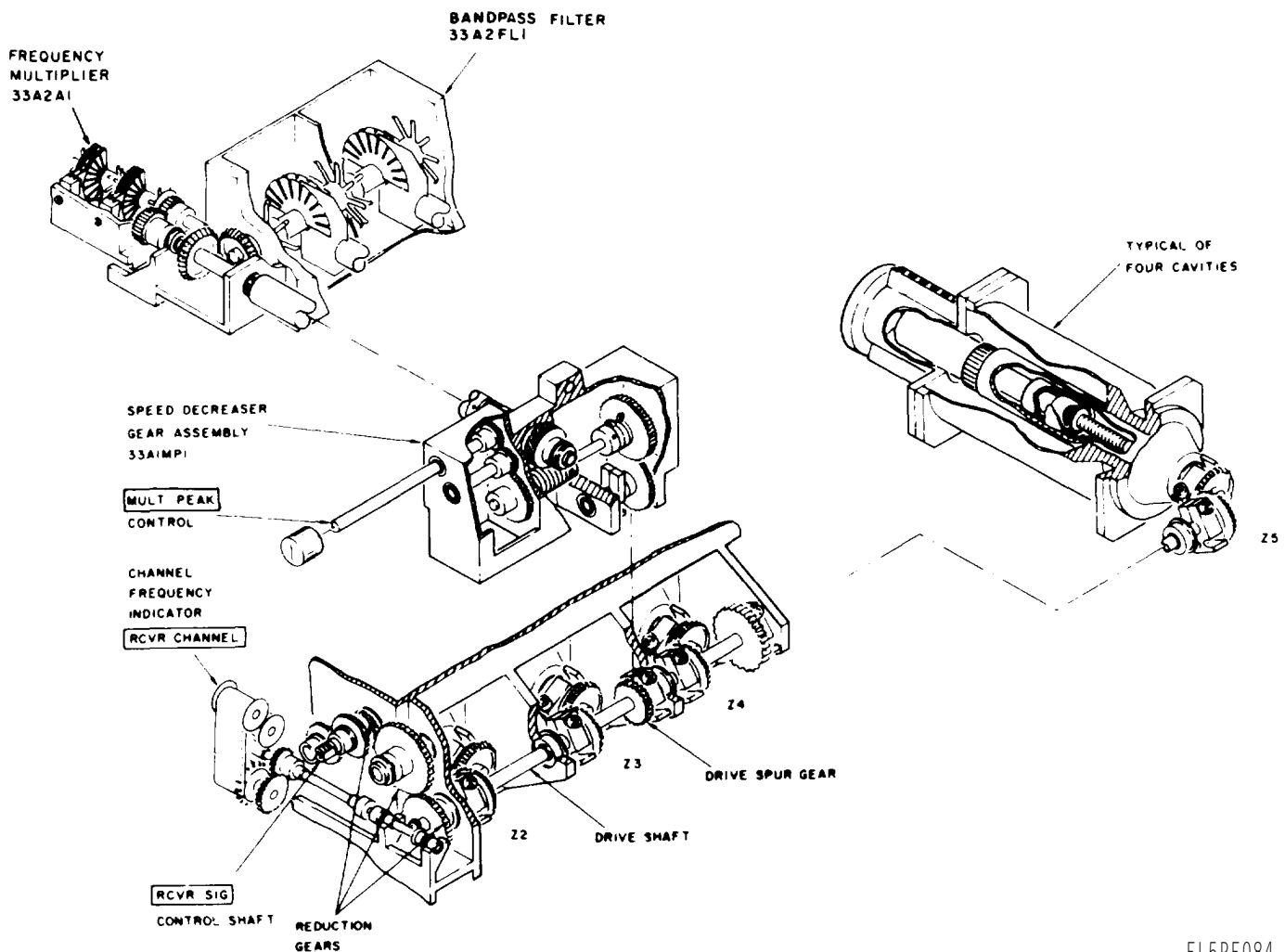
Figure 2-84. Duplexer Subassembly 33A1A1 or 34A1A1, Transmitter Section, Tuning Mechanism.

reduction gears (fig. 2-85), carries five bevel gears. Four bevel gears drive the four individual center conductor drive screws of the receiver resonant cavities. The fifth gear drives the channel frequency indicator RCVR CHANNEL. Also carried on the receiver section drive shaft are two reduction spur gears, one of which drives the speed deceiver gear assembly. The speed deceiver gear assembly provides tracking between the receiver duplexer cavities and the frequency multiplier and at the same time permits a small adjustment of the frequency multiplier, relative to the receiver duplexer, using the MULT PEAK control. The second spur gear on the receiver drive shaft provides a coupling to voltage control assembly 33A1A2. The voltage control assembly provides the tuning voltage for a varactor filter in frequency mixer stage 33A7.

c. An interconnection diagram of the Band II receiver rf head is shown in F0-4-58.

2-68. Rf Power Monitor 33A3 or 34A3

Rf power monitor 33A3 or 34A3, located in the receiver rf head, is fitted in the antenna line, between impedance matching network 33A1A1Z1 or 34A1A1Z1 and the antenna



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2-85. Duplexer Subassembly 33A1A1, Receiver Section, Tuning Mechanism.

connector (ANT.) on the front panel of the receiver rf head. The power monitor consists of two directional couplers, placed back-to-back with integral detectors and temperature compensation circuits. It samples the output power from the antenna, rectifies the rf signals and feeds the resulting dc voltages to the meter on the front panel of receiver fixed head. This provides appropriate meter readings when the meter switch is in either the XMTR DUPL or REFL PWR position.

## 2-69. Signal Level Control-Monitor 33A5 or 34A5

a. General. Signal level control-monitor 33A5 or 34A5 protects the receiver low noise circuitry, contained in frequency mixer stage 33A7 or 34A7, against possible high-level signals coming into the receiver from the antenna or transmitter terminal. Protection is obtained by presenting a low impedance to high-level signals, hence reflecting the unwanted rf power. The output of duplexer subassembly 33A1A1 or 34A1A1 is connected to input connector J1 and the output is taken from connector J2 and fed to low pass filter 33FL1 or 34FL1. Operating voltages are connected to the unit through 9-pin connector P1. The unit also monitors the protection level and triggers an alarm circuit. The alarm circuit is located in the radio receiver and is connected to audio and visual indicators.

### b. Detailed Circuit Analysis (F0-4-52).

(1) Signal level limiter 33A5A1 or 34 A5A1. The rf input signal, from the receiver section of duplexer subassembly 33A1A1 or 34A1A1, is connected to connector J1. The signal is coupled through C1 into rf level limiter A1, along the stripline, to which the shunt attenuator CR1, rf limiter A1, and clippers CR2 and CR3 are connected. When the input signal level is -5 dbm or less, the signal travels through the stripline from J1 to the output J2, with only negligible insertion loss introduced by the stripline. If the level of the input signal increases to 0 dbm the two hot-carrier diodes, CR2 and CR3, start clipping the peaks of the rf signal. When the level of the input signal reaches +10 dbm, rf limiter A1 starts generating dc current which flows to ground. The dc current increases proportionally with the level of the rf signal incident on A1. Shunt attenuator CR1 and rf limiter A1 are dc blocked within the same section of the stripline and therefore CR1 acts as a dc return for the dc current from A1. CR1 is a PIN diode and the dc current acts as a forward bias to the diode providing a low shunt impedance to the rf signal; this results in attenuation of the signal. The response time of the circuit is very low and therefore high amplitude input signals are limited almost instantly.

(2) Alarm control 33A5A2 or 34A5A2. The negative dc voltage from the cathode of CR1 in signal level limiter A1 is fed through L1 and feedthrough capacitor FL3 and applied to the base of Q1 in alarm control A2. The voltage at the emitter of Q1 is adjusted to approximately +0.2 volt by voltage divider R2, R3 and R6. ALARM LEVEL potentiometer R3 sets the operate point for the HIGH SIGNAL ALARM circuit by setting the voltage at the emitter of Q1. When the negative voltage at the base of Q1 increases to approximately -().4 volt, Q1 starts conducting, thereby turning on Q2 and Q3. Q3 emitter-collector current flows through the HIGH SIGNAL ALARM relay, in the receiver fixed head, causing it to operate. R6 in the collector circuit of Q3, is a latching resistor which eliminates chattering of the alarm circuitry. CR1 is connected across the alarm relay circuit and suppresses switching spikes. When Q3 is conducting, the collector current causes a voltage drop across R6 thereby raising the voltage level at the tap of R3. This increased voltage at the emitter of Q1 makes it conduct more. Resistor R4 and R5 provide a path for the leakage currents in Q2 and Q3.

2-70. Low-Pass Filter 33FL1

Low-pass filter 33FL1 is a sealed unit connected between signal level control 33A5 and frequency mixer stage 33A7. It is used to suppress the harmonics of the incoming frequencies and provides a minimum of 35 db rejection at all frequencies above 1185 MHz (3 times the lowest fundamental). The VSWR at either port does not exceed 1.31:1 and the power handling capacity is 25 dbm continuous.

2-71. Frequency Mixer Stage 33A7

a. General. The frequency mixer stage consists of the following four separate integrated circuit subassemblies, soldered to a printed circuit board 33A7A1: rf amplifier 33A7A1AR1, integrated circuit (I/C) monitor-power 33A7A1A1, two balanced mixers 33A7A1A2 and 33A7A1A3, and a hybrid quadrature 3 db coupler 33A7A1HYB1 (IF). The monitor-power, the two balanced mixers, and the quadrature hybrid IF are part of the image rejection mixer circuit. The received rf signal in the range of 395 to 705 MHz from the low-pass filter 33FL1, and the local oscillator signal between 425 and 735 MHz from the bandpass filter 33A2FL1 are mixed in the two balanced mixers; the resultant 30 MHz IF outputs are then fed to the IF amplifier 33AR1. Conversion gain of the frequency mixer stage 33A7 is between 10 and 18 db, while the noise figure is below 3.6 db.

b. Circuit Description (F0-5-53). The rf input at 33A7J1 is applied to pin 1 of the rf amplifier. The two-stage, low-noise, broadband amplifier is a microwave integrated circuit using high-gain, low-noise microwave transistors in their co-planar stripline package; fabrication of the rf amplifier on an alumina substrate using thin-film technology provides a good control of assembly parasitic. The gain of the rf amplifier is  $19 \pm 2$  db with a noise figure of 2.8 db. +12 vdc and -12 vdc operating voltages are applied to pins 3 and 2 of the rf amplifier; FL1 and FL2 provide rf filtering of the dc lines.

(1) Integrated circuit (I/C) monitor-power 33A7A1A1 combines the function of a 3 db coupler, an in-phase power divider, and a power monitor. The rf signal at pin 4 of the rf amplifier is applied to the 3 db coupler assembly (rf quadrature hybrid) (fig. 2-86). The two rf outputs in quadrature phase are applied through pins 7 and 2 (F0-4-53) to balance mixers 33A7A1A2 and 33A7A1A3 respectively.

(2) The local oscillator signal is applied through pin 4 of I/C monitor-power to an in-phase hybrid power divider; the two resultant local oscillator outputs are

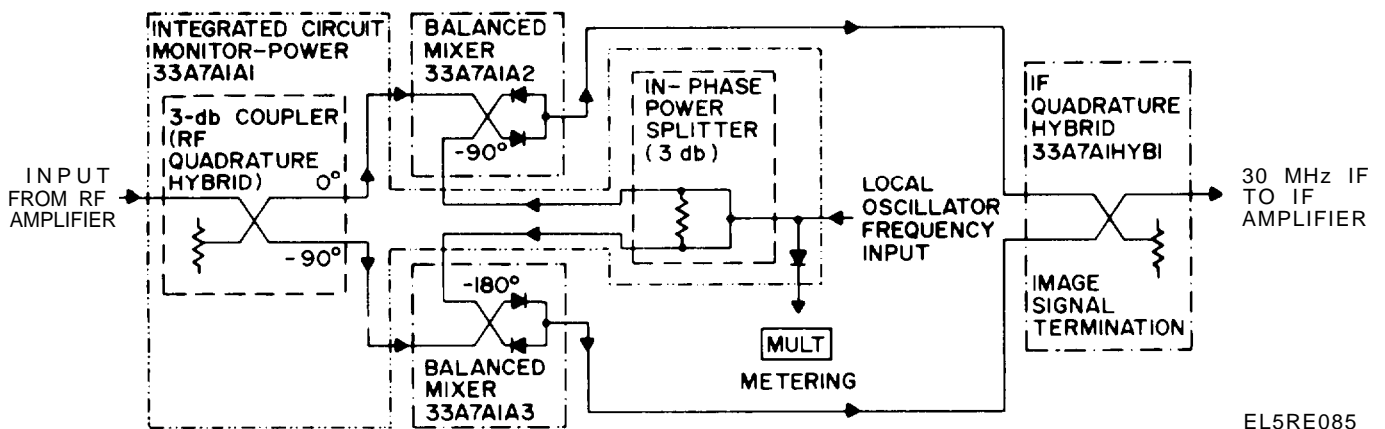


Figure 2-86. Frequency Mixer Stage 33A7, Block Diagram.

then applied in-phase through pins 3 and 6 to the two balanced mixers. The rf voltage of the incoming local oscillator signal is detected and the dc voltage is made available through pin 5 to output connector P1 pin 4 for MULT metering. Like the rf amplifier 33A7A1AR1, the monitor power is a microwave integrated circuit realized by using thin film technology on alumina substrate.

(3) The two balanced mixer stages provide products  $\pm 30$  MHz around the local oscillator frequency. The two mixers are identical, only the pin numbers are different; the balanced configuration of the mixers provides optimum spurious rejection.

(4) The two IF signals are then quadrature coupled within the 3 db coupler quadrature hybrid 33A7A1HYB1 where the image noise product is terminated within a resistive load. The output port of the hybrid is matched for interface with the IF amplifier 33AR1. L1-A, C1 and L1-B, C2 (low-pass filters) filter the two mixer outputs. Image rejection is achieved within R1.

## 2-72. Frequency Multiplier Group 33A2

a. General. The frequency multiplier group provides the final local oscillator frequency, 30 MHz higher than the received rf signal. The frequency multiplier group consists of three subassemblies, frequency multiplier 33A2A2, frequency multiplier 33A2A1 and bandpass filter 33A2FL1. The 33A2A2 doubles the incoming frequency from the receiver fixed head. The 33A2A1 is a variable frequency multiplier, and produces the continuously variable, final local oscillator frequency in the range of 425 to 735 MHz by doubling the input frequencies from 212.5 to 289.75 MHz and tripling the input frequencies from 193.333 to 245.0 MHz. The change in multiplication factor is accomplished by changing the input frequency to the point where the output tuned circuit selects the required harmonics. The second harmonic is selected over the required portion of the band and then the input frequency is stepped down to the point where the tuned circuit selects the third harmonic. Bandpass filter 33A2FL1 is a tunable filter which attenuates all unwanted sub-multiples of the local oscillator frequency applied to the frequency mixer stage.

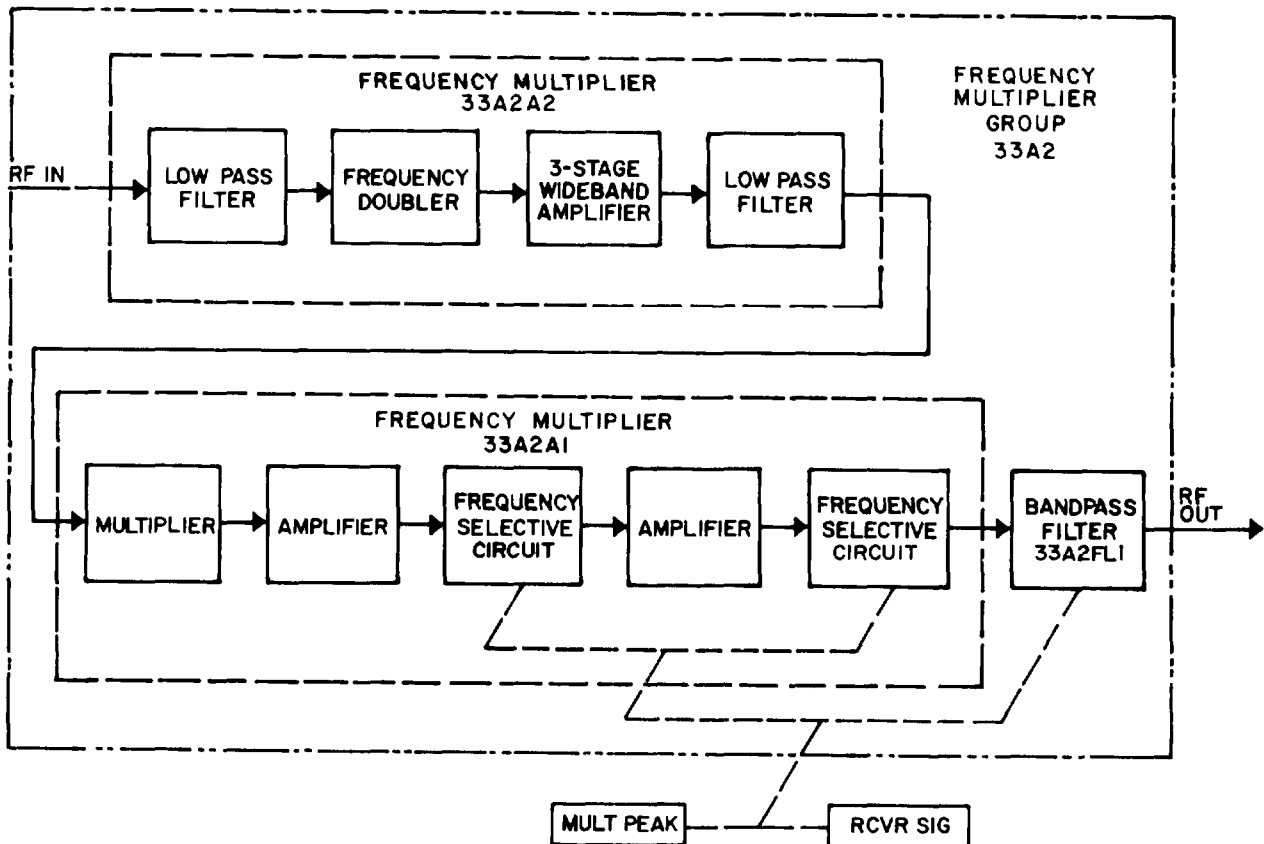
b. Block Diagram Analysis (Fig. 2-87). The rf input in the range of 95 to 145 MHz, at a level of +15 dbm, is fed into the low pass filter section of frequency multiplier 33A2A2, where the unwanted signals are removed. The filtered signal is then fed to the full-wave diode frequency doubler and then amplified in the 3-stage wideband rf amplifier. The output signal in the frequency range of 190 to 290 MHz is filtered again in the low pass filter at the output of 33A2A2. The output of frequency multiplier 33A2A2, at a level of +16 dbm  $\pm 1.5$  dbm, is fed to the multiplier section of the variable multiplier 33A2A1. The multiplier section generates a signal rich in harmonics, which is then amplified and filtered in two separate stages. The frequency selective circuits are ganged to the front panel RCVR SIG and MULT PEAK controls. The tuned circuits select the second or third harmonics, thereby producing a variable frequency 30 MHz higher than the received frequency. The output of 33A2A1 is fed to tunable bandpass filter 33A2FL1 which attenuates the unwanted submultiple of the local oscillator frequency. The bandpass filter, is also ganged to the front panel RCVR SIG and MULT PEAK controls (fig. 2-85) and is tuned, with the frequency selective circuits, 30 MHz above the frequency of the received signal.

## 2-73. Frequency Multiplier 33A2A2 or 34A2A2

a. General. Frequency multiplier 33A2A2 or 34A2A2 is fixed multiplier which doubles the rf output of amplifier-frequency multiplier 1RE1A5, part of the receiver

fixed head. The unit consists of three subassemblies, low pass filter FL1, frequency multiplier assembly A1 and low pass filter assembly FL2. The input to the unit is in the frequency range of 95 to 145 MHz, at a level of +15 dbm ±3 db. The output of the unit is in the frequency range of 190 to 290 MHz, at a level of +17 dbm ±2.0 db.

b. Detailed Circuit Analysis (FO-4-50). The output of 1RE1A5 is fed through pin A1 of P1 to low pass filter FL1. Low pass filter FL1 is a seven-element, M-derived filter which provides a 30 db attenuation at 190 MHz (2nd harmonic of the lowest input frequency) and 3 db at 150 MHz. The N-derived filter provides a sharp cutoff, necessary because the operating range is 95 to 145 MHz and the second harmonic of 95 MHz is 190 MHz. The insertion loss of the filter is 0.75 db over the operating frequency range. The filter consists of L1, L2, L3, L4, C2, C3 and C4; variable capacitors C1 and C5 are provided for alinement. The filtered rf signal is fed through J1 of frequency multiplier assembly A1 to the frequency doubler, T1 and CR1. Transformer T1 is a three-wire ferrite transformer with a balanced output. The output of T1 is balanced by variable capacitor C1. Balancing the output of T1 reduces the fundamental and third harmonics of the doubler output. The output of transformer T1 drives the full-wave doubler, consisting of the pair of matched hot carrier diodes CR1A and CR1B in CR1. Shunt tuned circuit L1 and C2 along with R1 provides a return path to circulate harmonics. The nominal loss of the doubler is 10 db. The doubled signal is coupled through C3 and series tuned equalizer circuit, C4, L2 and R2, to the base of amplifier Q1. The output of Q1 is fed to amplifier Q2 and then to Q3,



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Figure 2-87. Frequency Multiplier Group 33A2, Block Diagram.

through respective series-tuned equalizer circuits L4, C6, R8 and L5, C7, R11. The interstage equalizer networks ensure optimum gain of the three-stage amplifier over the frequency range. The nominal gain of the amplifier is 16 db. The first two amplifier stages, Q1 and Q2, are class A operated to obtain maximum gain. To obtain constant output power over the frequency range, the third stage Q3 is driven into class C operation. Voltage dividers R3-R4, R5-R7 and R9-R12 provide the appropriate dc bias for Q1, Q2 and Q3 respectively. The output of frequency multiplier assembly A1, is coupled through C18 to J2 and fed to P1 of low pass filter assembly FL2. The rf signal, in the frequency range of 195 to 290 MHz, at a level of 17.75 db  $\pm$ 2.0 db, is fed through low pass filter assembly FL2 which consists of L1, L2, L3, C1, C3, C5 and C7. Four variable capacitors C2, C4, C6 and C8 are provided for filter alignment. The insertion loss of the filter is 0.75 db at the operating frequency and 13 db minimum above the operating frequency.

#### 2-74. Frequency Multiplier 33A2A1

a. General. Frequency multiplier 33A2A1 provides the final local oscillator frequency by doubling the frequency of the signal from frequency multiplier 33A2A2 over a portion of the band and tripling it over the remainder of the band. The unit consists of a transistor harmonic generator and a two-stage amplifier. The two stages of the amplifier are coupled to tuned circuits which select the required harmonics. The change in multiplication factor is accomplished by changing the input frequency to the point where the output tuned circuit selects the required harmonic.

##### b. Circuit Description (F0-4-49).

(1) Multiplier section. The output of the frequency multiplier 33A2A2, in the frequency range of 195 to 290 MHz, at a level of +17 dbm  $\pm$ 2.0 db, is applied to input connector J1. The signal from J1 is applied to the base of harmonic generator Q1 through the input matching network which consists of tuned circuit L1, R1, Z1, C1, R2 and 33A2A1C1 (C1 is mounted outside circuit board 33 A2A1A1). L1 and 33A2A1C1 are adjusted for a low Q. Q1 is the harmonic generator, operated in class C. Zener diode CR1, connected across the dc supply line for Q1, limits the power dissipation of the transistor by limiting the collector voltage to 5.6 volts. The output of the multiplier, a signal rich in harmonics, is coupled to the amplifier section through broadband matching network L2, R3 and C2. L2 attenuates the fundamental frequency to enhance the harmonic production. R3 provides a load at any frequency to keep Q1 stable and it also reduces feedback of high frequency harmonics through the collector-base capacitance. C2 couples the desired harmonics to amplifier Q2.

(2) Amplifier section. The output of multiplier Q1 is coupled to the base of Q2. R4, R5 controls the dc bias of Q2. C3 and R6 in the dc feedback circuit provide bias stability for a more linear response. The output of Q2 is coupled through output matching network L3, R7, C5 to resonant circuit Z2, C2. Both amplifier stages are operated in class "A", and contain similar input and output coupling networks, except that the first stage works on a smaller collector current due to lower rf level. The tunable resonant circuits, in the output of the amplifiers, reject the unwanted frequencies and select the required frequencies. Multileaf air capacitors C2 and C3, in the resonant circuit cavities Z2 and Z3 respectively, are ganged to the tuning mechanism of the local oscillator filter and receive tunable filter of the duplexer.

(3) Tuning mechanism. The direct transmission method used insures consistent tracking between frequency multiplier 33A2A1 and filter bandpass 33A2FL1. The out-



put frequency is continuously variable, using the RCVR SIG control and idler trimming arrangement actuated by the MULT PEAK control. The tuning mechanisms of variable amplifier 33A2A1 and filter bandpass 33A2FL1 are ganged to each other through two bevel gears, mounted on different shafts, driving their respective capacitors. The multiplier shaft is then coupled to the duplexer receive filter mechanism through a reduction gear box. The RCVR SIG control actuates the four-cavity duplexer filter and adjusts bandpass filter assembly 33A2FL1 and multiplier assembly 33A2A1 to a point near the required tuning point; the MULT PEAK control then tunes the bandpass filter and multiplier assembly to their required tuning point.

#### 2-75. Bandpass Filter 33A2FL1

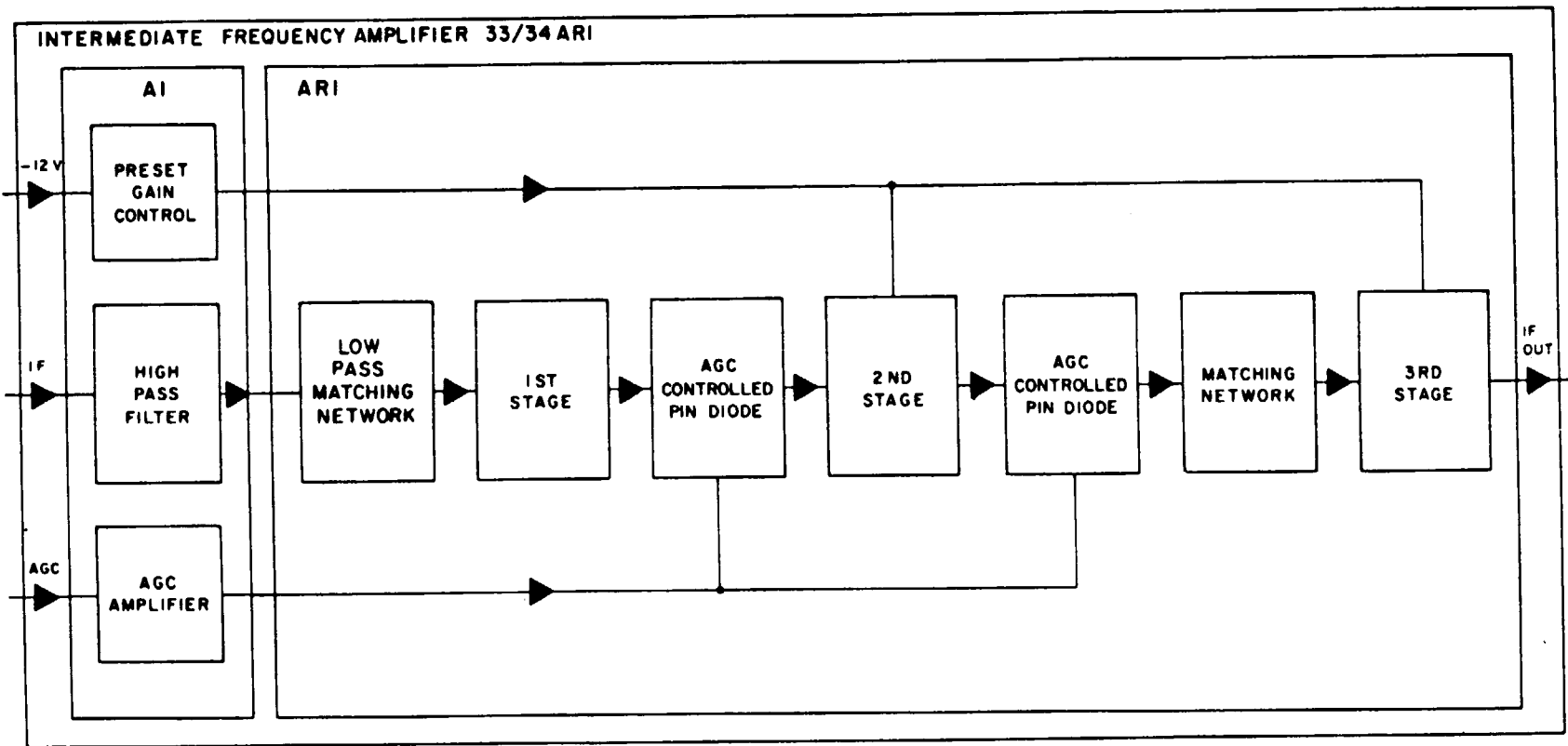
The output of variable frequency multiplier is applied to the input connector J1 of bandpass filter 33A2FL1 (F0-4-57). From J1 the signal is fed to resonator Z2 through input matching network L1, Z1. The filter consists of two fixed length capacitively loaded coaxial resonators Z2 and Z6. The loading capacitors C1 and C5 are variable and ganged to the tuning mechanism of variable multiplier 33A2A1. The input and output loading networks are similar and consist of an inductor and a parallel capacitor. The signal is coupled from Z2 to Z6 through a T-network consisting of inductors L2, L3 and L4. Z3, Z4 and Z5 are parallel self capacitances of the coils.

#### 2-76. Intermediate Frequency Amplifier 33AR1 or 34AR1

a. General. The intermediate frequency amplifier 33AR1 or 34AR1 is part of an IF system consisting of intermediate frequency amplifier 33AR1 or 34AR1, bandpass filter 1RE1FL1 and intermediate frequency amplifier 1RE1AR2. (The latter two are located in the receiver fixed head.) IF amplifier 33AR1 or 34AR1 is a three-stage amplifier with automatic gain control of the last two stages. The agc voltage is derived from video amplifier 1RE1AR1, located in the receiver fixed head. The overall gain of the IF amplifier is 50 db nominal and the automatic gain control provides gain adjustment down to 10 db.

b. Block Diagram Analysis (Fig. 2-88). The 30 MHz IF signal from frequency mixer stage 33A7 or 34A7, at a level ranging from -35 to -75 dbm (depending upon the receiving signal strength), is fed into the high-pass filter, part of amplifier-filter 33AR1A1 or 34AR1A1. The high-pass filter attenuates all signals below 30 MHz. The output of the high-pass filter is fed to the first stage of the IF amplifier through a low pass matching network (part of 33/34AR1AR1). The low-pass matching network matches the output impedance of the high-pass filter to the input impedance of the first amplifier stage. The outputs of the first and second amplifier stages are controlled by age-controlled PIN diodes. The input to these PIN diodes is current from the agc amplifier. The input to the agc amplifier is voltage from the receiver fixed head. A preset gain control provides a  $\pm 5$  db adjustment of the overall gain.

c. Detailed Circuit Analysis (F0-4-54). The 30 MHz IF signal from frequency mixer stage 33A7 or 34A7, at pin A1 of connector P1, is fed to the high-pass filter consisting of C1, C2, C3, C4, C5, L1, L2, L3 and L4 in amplifier-filter 33/34AR1A1. This filter provides 56 db attenuation at 15 MHz. The adjustable inductors L1, L2, L3 and L4 are aligned using the pole-zero method. The filtered IF signal, at connector J1 of IF amplifier 33/34AR1AR1, is fed through low pass through C4 to the base of Q1. The low pass matching network L1, L2, C1, C2 and coupled through C4 to the base of Q1. The low pass matching network matches the impedance of the high pass filter to the input impedance of Q1. L1, L2 are adjustable and are aligned by



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Figure 2-88. Intermediate Frequency Amplifier 33ARI or 34ARI, Block Diagram.

the swept vswr method. R1, RT1, R2 is the bias network for Q1 and L4, C6 and R3 forms the collector load. R3 provides isolation against the impedance variations of CR1. The amplified signal is coupled through C9 to the base of second amplifier stage Q2. R5, R7 and R4 forms the bias network for Q2. R6 is the collector load for Q2. 1-7 prevents CR2 from being back-biased by the potential developed across R6. The gain of this transistor stage is adjusted by potentiometer R4 mounted on 33AR1A1. The output of the second stage is coupled to the base of the third stage Q3, through input matching network R8, C14, L11. The gain of the third stage is also adjusted by gain control potentiometer R4 in 33AR1A1. The amplified output is fed to the receiver fixed head through the output matching network consisting of R9, L12 and C18. Two PIN diodes CR1 and CR2 are connected at the input of the second and the third stages. The resistance of these two PIN diodes is controlled by the agc current through Q1 in amplifier-filter 33AR1A1. The agc voltage from the video amplifier in the fixed head is fed through pin 1 of P1 through filter-network L5, C7 to the base of agc amplifier Q2. Q1 and Q2 of the amplifier are connected in a differential configuration and the input voltage variations are converted into current variations which in turn control the resistance of the PIN diodes.

## 2-77. Power Supply 33PS1 or 34PS1

a. General. Power supply 33PS1 or 34PS1, situated in the receiver rf head, converts -12 volts dc to a regulated +70 volt dc supply. The -12 volt input is derived from the main power supply situated in the receiver fixed head. The regulated output supply is used on a tuning potentiometer which tunes a voltage controlled filter in frequency mixer stage 33A7 or 34A7.

b. Detailed Circuit Analysis (F0-4-55). -12 volts dc at pin 3 of P1 is applied to the input filter L1, L2, C1, C2, C3, C4 and C5. The input filter prevents any spikes generated in the oscillator to be fed back to the -12 v line. C6, a 0.1 uf capacitor shunting the filter capacitors, provides extra protection against high frequency spikes. The output of the filter is fed to a self-starting oscillator Q1, Q2. The starting voltage, 1 volt minimum on turn-on, is provided by voltage divider R2, R12. Resistor R1 acts as a load for the oscillator during the transition in switching from one state to the other. The oscillator converts the -12 volts dc into an ac signal which is then applied to the primary windings of inverter transformer T1. Transformer T1 steps up the ac converter signal to a 90 volt peak-to-peak supply. The output of the inverter, taken across terminals 5 and 6, is rectified in the full-wave bridge rectifier CR1, CR2, CR3, CR4. The rectified voltage is fed through the output filter (C8, C9, C10, L3 and L4) which suppresses the ripple in the rectified dc supply. The voltage at the output of the filter, approximately 90 volts, is then fed to the preregulator circuit consisting of a constant current preregulator and a series regulator circuit. Series regulator transistor Q4 and Q5 are connected in a high-gain dc amplifier arrangement; Q4 provides additional closed-loop gain for higher regulation. The emitter of Q5 is the regulated output line.

(1) The constant current circuit consists of CR5, R3, R4 and Q3. CR5 provides a reference voltage for Q3 resulting in a constant current through R4 and Q3 emitter to collector which is used to control the current through Q4 and Q5. A reference voltage is taken from CR7 to the base of Q6. A sample of the 70 volt output is applied through R9 and R10 to the base of Q7. Q6 and Q7, being a differential dc amplifier, the Q6 collector current is a function of the difference between the output voltage and the reference voltage. +70 V LEVEL potentiometer R1(1) adjusts the output voltage. An increase in the output voltage will increase the voltage at the base of Q7. This causes an increase in Q6 collector-emitter current and reduces the

base current into Q4 and consequently the base current into Q5. A decrease in Q5 base current causes an increase in its collector-to-emitter voltage which reduces the output voltage. The reverse occurs when the output voltage decreases below the set value.

(2) R5 and R6 form a current limiting network which provides output short circuit protection. A reduction in load resistance causes an increase in the current through regulator circuit Q4 and Q5 and an increase in the voltage drop across R5. When the voltage drop exceeds the reverse bias of CR6, it turns on and shunts the current away from constant current transistor Q3. The Q3 emitter current reduces and, as a result, the base current into Q4 and Q5 is reduced, limiting the current through regulator Q5.

#### 2-78. Voltage Control Assembly 33A1A2 or 34A1A2

The voltage control assembly provides the tuning voltage for the varactor filter in the frequency mixer stage 33A7 or 34A7. The variable voltage controls the tuning law so that the frequency mixer stage tracks with the duplexer. The input to the voltage control assembly is the +70 volts dc regulated supply from power supply 33PS1 or 34PS1. The unit consists of an aluminum casting, a potentiometer, a worm and worm gear and a spur gear coupled to duplexer subassembly 33A1A1 (fig. 2-85) or 34A1A1 main tuning shaft.

### Section VIII. AMPLIFIER-FREQUENCY MULTIPLIER AM-4322/GRC-103(V) AND AM-4322A/GRC-103(V)

#### 2-79. Functional Block Diagram Analysis of Amplifier-Frequency Multiplier AM-4322/GRC-103(V) and AM-4322A/GRC-103(V) (Fig. 2-89)

The rf output of the Band III transmitter fixed head, in the range of 95 to 145 MHz at a level of 35 dbm, is fed into amplifier-frequency multiplier AM-4322/GRC-103(V) or AM-4322A/GRC-103(V) (transmitter Rf head), where it is multiplied and amplified to produce the final transmitter frequency.

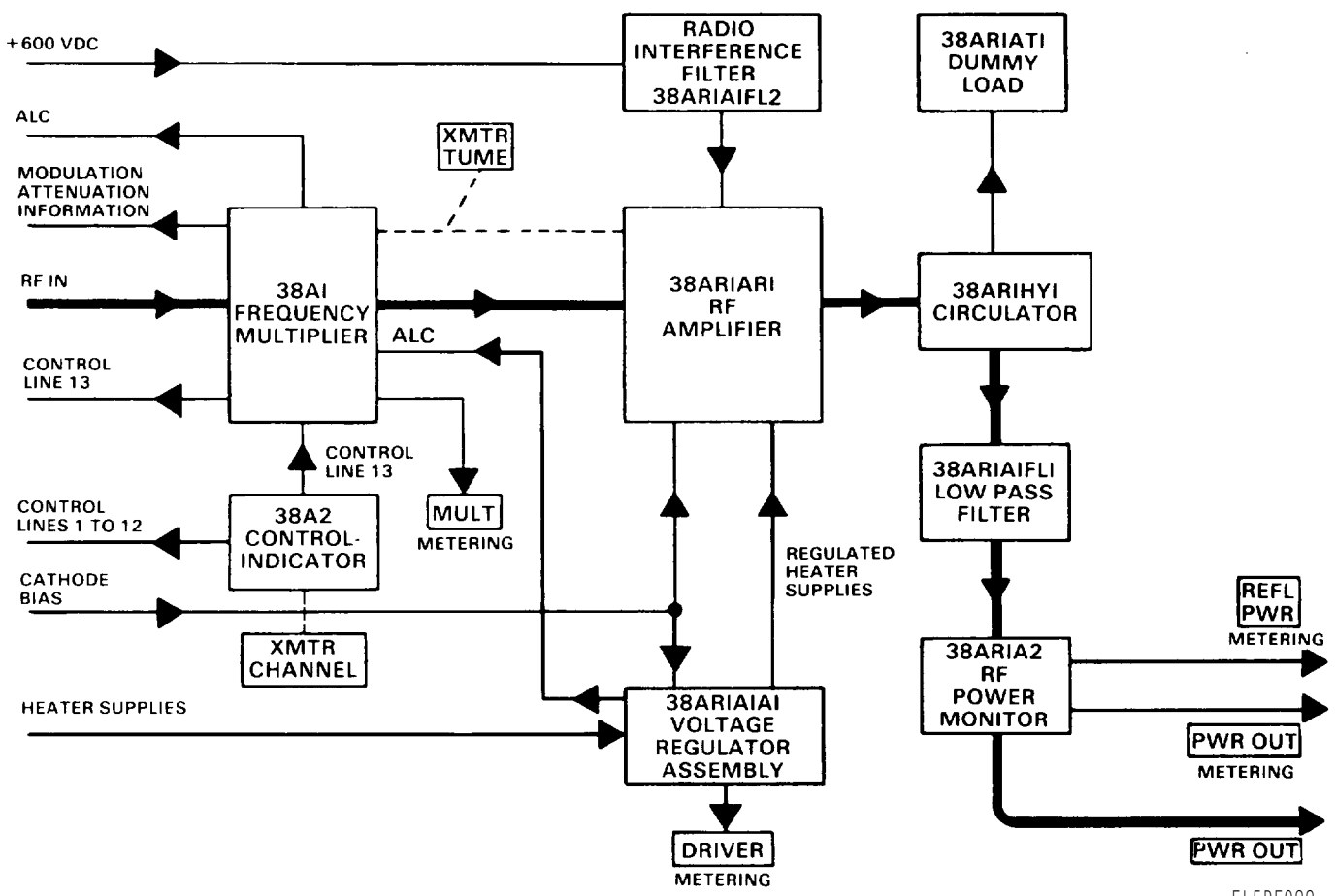
a. The transmitter rf head multiplication circuits provide the final multiplication required to produce the selected transmitter channel frequency. The multiplication is accomplished in frequency multiplier 38A1 which contains a frequency doubler and a variable multiplier which multiplies the second harmonic frequency by three or by four. The output harmonic frequency of the frequency multiplier is selected by two tuned cavities which are ganged to the front panel XMTR TUNE control. The frequency multiplier also produces an alc voltage which keeps the transmitter fixed head output at a preset value. The multiplied frequency is also amplified in the frequency multiplier circuit by an alc controlled amplifier. The output of frequency multiplier 38A1, in the range of 695 to 1000 MHz at a level of 23 dbm, is fed into rf amplifier 38AR1AR1.

b. The amplification of the output signal to the final output level is done in two-stage radio frequency amplifier 38AR1AR1 (driver and output amplifier), using two planar triodes type 7211 mounted in tuned-cathode, tuned-plate coaxial quarter-wave resonant cavities. The XMTR TUNE control, in the front panel, tunes the cath-

ode and plate plungers of both stages. Coupling is achieved by coupling probes. Forced air is used for cooling the tubes. Concentric cavity design gives adequate exposure of the plate radiators to the airstream.

c. Radio frequency amplifier 38ARIAR1 amplifies the final frequency of the transmitter to a level of approximately 30 watts. The amplifier rf signal is then fed to a 3-port circulator 38ARIHY1. The circulator permits the outgoing signal to pass from port 1 to port 2, but prevents any reflected signal from reaching port 1. The reflected signal is bypassed through the third port to a dummy load. After rejection of unwanted harmonics in low pass filter 38ARIAIFL1, the output signal is fed through rf power monitor 38ARIA2 and PWR OUT connector to amplifier-converter AM-4318/GRC-103(V) (Band III receiver rf head) and through a duplexer, to the antenna system. A sample of output power and reflected power is rectified in the power monitor and taken out as PWR OUT and REFL PWR metering signals.

d. Control-indicator 38A2 (channel selector) is an electromechanical device operating in conjunction with electrical frequency synthesizer and amplifier monitor in the transmitter fixed head. The channel selector provides 13 control lines. Control lines 1 to 12 inclusive program the frequency generating circuits in the electrical frequency synthesizer. Control line 13 is fed through the amplifier frequency multiplier to the amplifier monitor in the transmitter fixed head to control variable attenuators in amplifier-monitor 5TR1A5. Voltage regulator assembly 38ARIA1A1 supplies the regulated heater supply for the driver and output tubes.



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Figure 2-89. Band III Transmitter RF Head, AM-4322/GRC-103(V) and AM-4322A/GRC-103(V), Block Diagram.

e. An overall schematic diagram of the Band III transmitter rf head is shown in F0-4-70 and the interconnecting diagram is shown in F0-4-71.

## 2-80. Frequency Multiplier 38A1

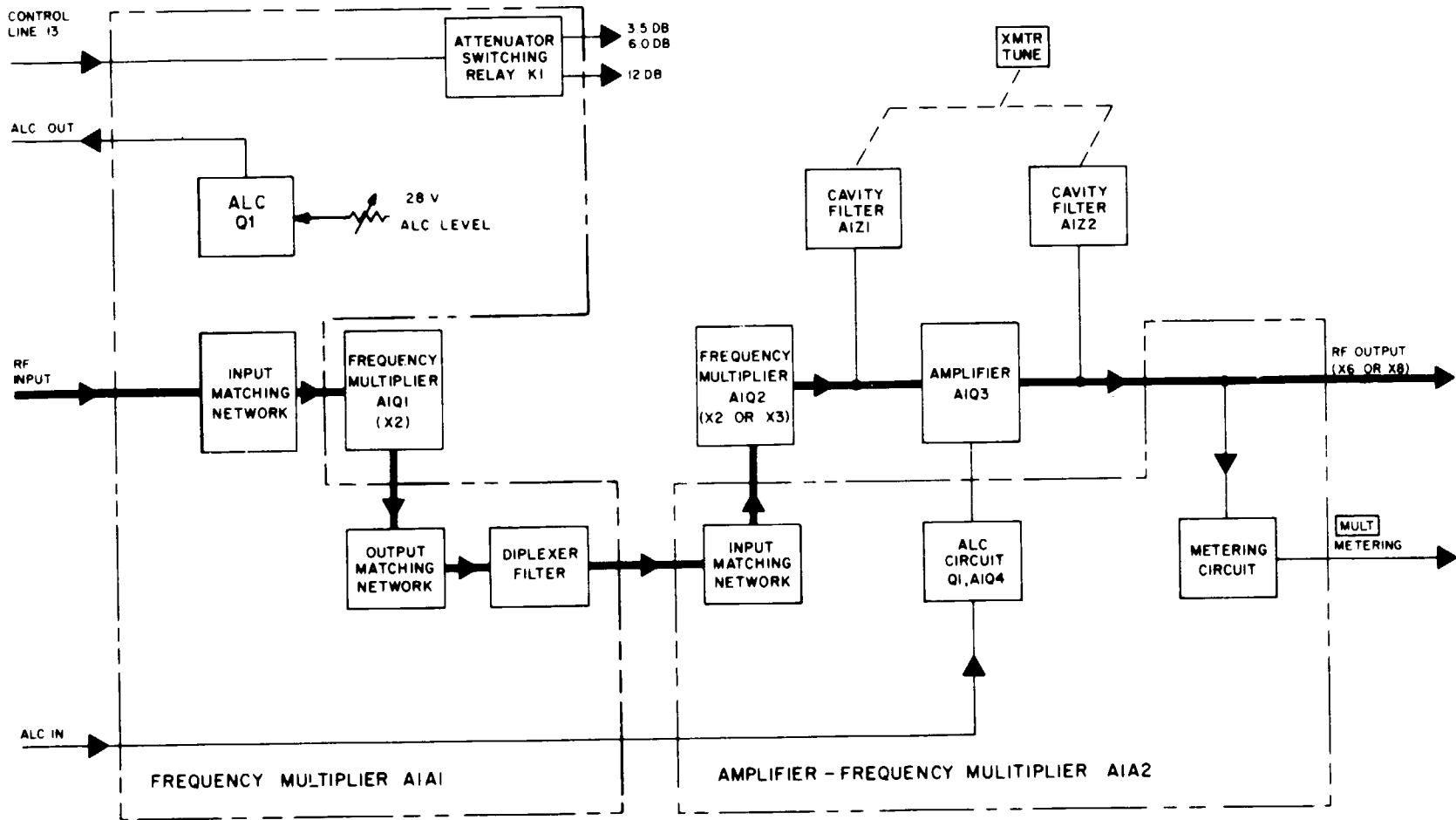
a. General. Frequency multiplier 38A1 multiplies the transmitter fixed head output-signal by six to produce 695 to 839.5 MHz, or by eight to produce 840 to 1,000 MHz. The output signal, at a level of +23 dbm, is the input drive for radio frequency amplifier 38AR1. Frequency multiplier 38A1 consists of two printed wiring boards mounted in a six-compartment aluminum casting. Two casting compartments incorporate two tuned cavities, while a doubler, a multiplier, the cavities gear drive, and an electrical connector are contained in the remaining compartments. The center conductors of the cavities are variable plungers driven by precision lead screws which are ganged to the XMTR TUNE control.

b. Block Diagram Analysis (Fig. 2-90). The output of amplifier frequency multiplier 5TR1A4, in the frequency range of 104 to 140 MHz at a level of +35 dBm, is fed through the input matching network to the A1Q1 wideband doubler circuit. Parametric multiplier A1Q1 amplifies the input fundamental frequency while the collector-to-base capacitance acts as a varactor for harmonic generation. The output of the wideband doubler is fed through the output matching network to the diplexer filter which terminates the fundamental frequencies and provides a path for the second harmonics. The output of the diplexer filter is applied through the input matching network to variable frequency multiplier transistor A1Q2. The A1Q2 circuit multiplies the rf signal by three or by four. Tunable cavity A1Z1 selects the required harmonic from the output of the multiplier. The filtered output is fed to amplifier stage A1Q3, which provides up to 7 db gain for the multiplier signal. The output of the amplifier is tuned by cavity A1Z2 which is ganged to A1Z1 and the front panel XMTR TUNE control. The amplifier-frequency multiplier 38A1 contains two automatic level control (alc) circuits: the input alc which maintains a constant drive to the X2 multiplier circuit (A1Q1) and the output alc which regulates the X6 or X8 rf output, which in turn drives the radio frequency amplifier 38AR1. The transistor in the alc circuit controls the incoming rf level by controlling the dc current consumption of the two multiplier stages (X2 and X3-X4). Automatic level control of the output signal is provided by A1Q1 and A1Q4. This circuit controls the collector voltage supply to A1Q3 amplifier stage. The alc circuit is driven by a signal from the rf power amplifier 38AR1 in proportion to the rf drive signal. A portion of the output signal is fed into the metering circuit where it is rectified and used as the MULT metering signal. Control line 13 from control-indicator 38A2 is used to operate attenuator switching relay K1. The relay supplies information to the modulator in the fixed head to change its sensitivity when the multiplication factor changes from six to eight.

### c. Detailed Circuit Analysis (F0-4-69).

(1) Frequency doubler. The rf input from J1 is fed through an input matching network to transistor multiplier A1Q1. The input matching network contains a bandpass network and an impedance transforming network. The bandpass network consists of C4, L1, C5 and L2 and is used to isolate the input circuit from the multiplier output frequencies. The parallel resistive network R5 and R6 in series with 4:1 transformer T1, matches the input impedance of A1Q1. The fundamental frequency, from the input matching network, is coupled through dc blocking capacitor C8 to the base of A1Q1. R7 provides a small reverse bias on the base of A1Q1 for optimum efficiency. C7 cancels any inductance introduced by the transformer at midband.

Figure 2-90. Frequency Multiplier 38A1, Block Diagram.



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Collector supply for 38A1Q1 and 38A1Q2 is derived from the +28 vdc through 38A1R2. L7 and C12 resonate with the transistor output capacitance at the fundamental mid-band frequency. The capacitance between the base and collector of A1Q1 varies non-linearly with the transistor collector voltage. The transistor amplifies the fundamental which drives the variable base-collector junction capacitance, producing a highly distorted output waveform. This waveform contains components of the fundamental and harmonic frequencies. The A1Q1 output is fed through output matching network C14, L8 to the diplexer filter.

(2) Input a/c circuit. The voltage applied to the input a/c transistor 38A1A1-Q1 is developed across resistor 38A1R2 through which passes the current consumed by the two multiplier stages 38A1Q1 and 38A1Q2. R3, the ALC LEVEL potentiometer, is set for maximum current through 38A1R2. When the incoming rf signal is too high, the voltage at the base of a/c transistor Q1 causes its collector voltage (input a/c) to increase; this increase in the input a/c voltage applied to the a/c circuit in the amplifier-frequency multiplier 5TR1A4 will cause a decrease of the rf output. The reverse is true for a weaker incoming rf signal. Since the input rf signal is a function of the dc current consumption, the supply current once set, controlling the input rf level becomes independent of multiplier transistor efficiency or transistor parameters. C6 provides rf decoupling and R4 is the collector load.

(3) Diplexer filter. The diplexer filter is a power splitter providing a path to terminate the fundamental frequencies at one port and a path for the second harmonics to the third port. The diplexer is a combination low-pass - high-pass filter with seven sections. The fundamental frequencies are fed through the filter and terminated in A1R1. The second harmonics, fed through the filter to the output port, are coupled through C18 to the variable frequency multiplier 38A1A2 circuit.

(4) Variable frequency multiplier. The output of the frequency doubler is coupled through input matching network R1, C1, C2, C3 to the base of frequency multiplier A1Q2. The output at the collector of A1Q2 is the signal rich in second or third harmonics. L1 in parallel with R10 forms an idler circuit which resonates with the collector-to-base varactor capacitance at, 250 MHz (midband of the fundamental input frequencies) to produce second harmonic frequencies. Capacitors C5 and C6 provide rf decoupling at the operating frequencies and at low frequencies. The second harmonic idler, L2, C7 and A1Q2 collector-base capacitance, provide a low impedance path to circulate the second harmonic current, thereby producing third harmonic frequencies. C4 completes the idler loop, along with the second harmonic idler components. The multiplier output is coupled through C7 to filter cavity A1Z1 through A1L1 and A1L2 to the base of amplifier A1Q3.

(5) Cavity filter A1Z1 and A1Z2. The output of the variable frequency multiplier is coupled through A1L1 to cavity filter A1Z1. The cavity is a quarter-wavelength tunable filter which tunes the output from the multiplier. The selected harmonics are coupled through A1L2 to the amplifier A1Q3. The value of coupling coils A1L1 and A1L2, in parallel with the coaxial line, is selected to provide a constant bandwidth over the frequency range. A1L1 and A1L2 provide an effective inductance of .0081 uh. The required capacitance to resonate this inductance is obtained from the capacitance of the plunger. Trimmer capacitors A1C1 and A1C2 resonate the fixed portion of the coaxial line. A1Z2 filter circuit, in the output of amplifier A1Q3, is identical to the A1Z1 filter circuit. A1L3 and A1L4 are the input and output coupling coils, for A1Z2, and A1C4 and A1C5 the trimmer capacitors. The bandwidth of the circuit is determined primarily by the multiplier cavity. The amplifier cavity bandwidth is wider to compensate for small tracking errors between the two cavities. Both cavities are ganged to the front panel XMTR TUNE control.



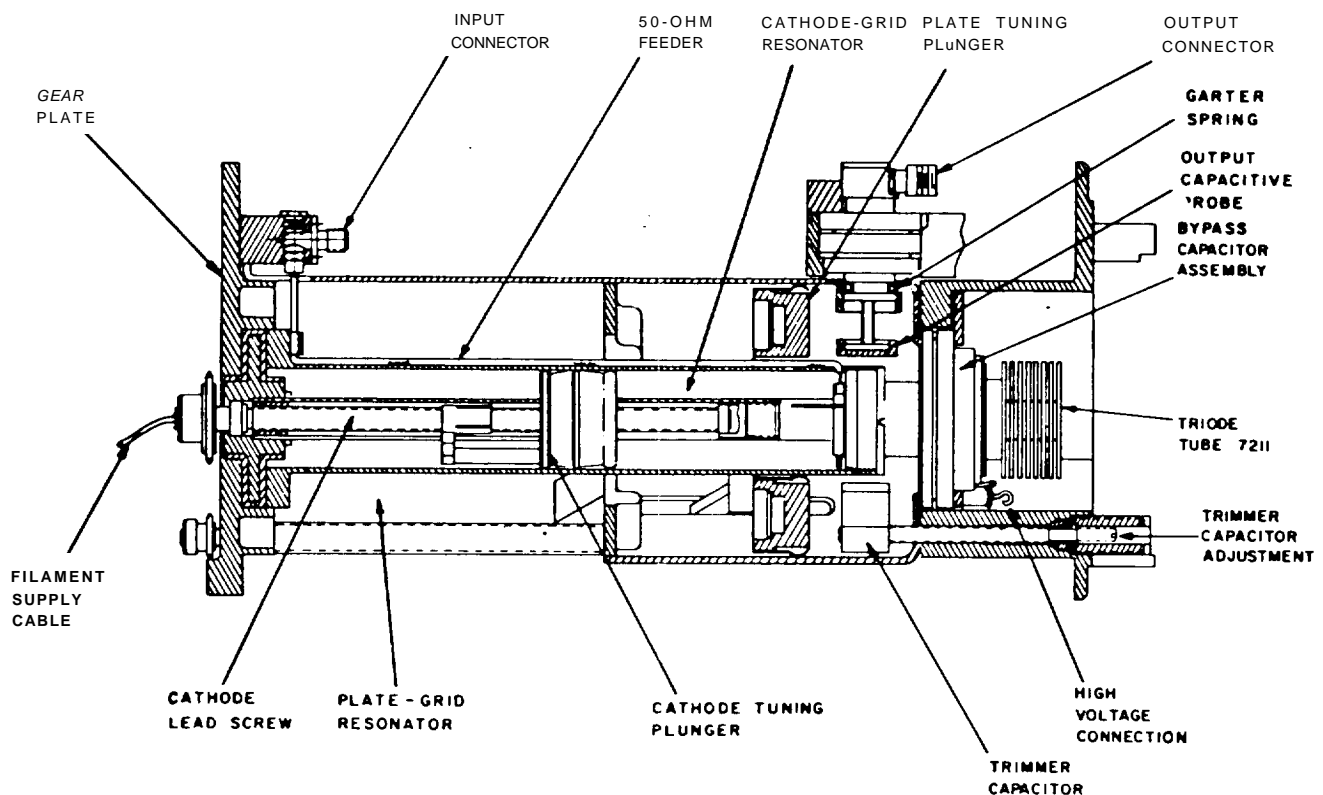
(6) Alc controlled amplifier A1Q3. The filtered output from cavity A1Z1 is coupled into the amplifier A1Q3 which provides approximately 7 db gain. R11 slightly forward biases the base of A1Q3 to increase the gain of the amplifier stage at lower drive levels. L3, C9 and R7 form an equalizer to reduce the drive to the amplifier over the low frequency end of the times three range. L3 and C9 resonate at 950 MHz and present a high impedance to the base signal at the high frequency end of the band and a low impedance at the low frequency end. L4 and C10 filter the collector dc supply. The collector supply voltage is fed through a series regulator A1Q4 to provide automatic level control. A1Q4 is controlled by Q1 which receives its drive from the power amplifier. The input alc signal is proportional to the rf drive to the cathode of the power amplifier driver tube. This signal is applied through P1 pin 8 to zener diode CR1 and the base of transistor Q1. CR1 limits the drive into Q1 to 3.3 volts, to insure that Q1 output never goes below 3 volts. Potentiometer R6 is adjusted for a minimum output level of +23 dbm from rf out connector J2, or 15 volts at the emitter of A1Q4, whichever is the least. Q1 drives the base of series regulator A1Q4 thereby varying the collector supply voltage to A1Q3 and consequently the gain of A1Q3. The amplified signal is coupled through C11 to cavity filter A1Z2 where the signal is further tuned to the required transmitter frequency. The output signal to rf amplifier 38AR1AR1, is coupled through low pass filter Z2, C14, Z3 to the output connector J2. The low-pass filter has a cutoff frequency above 1000 MHz.

(7) Metering Circuit. A portion of the output is coupled to a directional coupler comprising two striplines on the printed circuit board. Since the coupling energy increases with the increasing frequency, coil L5 is placed in series with the detector diode CR2 to provide a constant rf drive to the diode. Rf decoupling is provided by C12. The detected rf is fed to the metering circuit in the transmitter fixed head for MULT meter indication.

(8) Modulator sensitivity relay K1. Relay K1 receives its actuating signal through control line 13 from the channel selector. For output frequencies of 695 to 839.5 MHz, control line 13 is open and 26 v neutral is applied to the 12 db line through K1 contacts A2, A3. From 480 to 1000 MHz, line 13 is grounded and 26 v neutral is supplied to the 3.5 and 6 db line through contacts A2, A1

## 2-81. Radio Frequency Amplifier 38AR1AR1

a. General. Radio frequency amplifier 38AR1AR1 amplifies the final selected transmitter frequency by 23 db in two power amplifier stages. Each stage uses a type 7211 lighthouse tube mounted in a tunable resonant cavity. The cavity design uses a coaxial quarter-wave resonant cavity (fig. 2-91) for both the plate and cathode circuits. The heater connection to the amplifier tube is made through the hollow cathode lead screw inside the center conductor of the cathode grid resonator. The lead screw is of a double-start nature to enable rapid transit of the tuning plungers. Cathode feed (input signal) is taken in through the input connector which is adjacent to the gear plate. This input signal is then passed through a 50 ohm feeder coaxial cable, firmly bonded to the outside of the grid cathode resonator cavity, and fed through the cathode contact assembly to the cathode. Dc isolation is achieved within the cathode contact assembly. The plate supply is decoupled by a capacitor (bypass capacitor assembly) integral to the amplifier tube socket. The capacitor is a silvered mica disc in a potted assembly. Dc power to the tube plate is fed to the high voltage connection mounted on the plate side of the bypass capacitor assembly. Tuning the cathode and plate resonators is accomplished by adjusting mechanically coupled plungers, ganged to the XMTR TUNE control. Output coupling

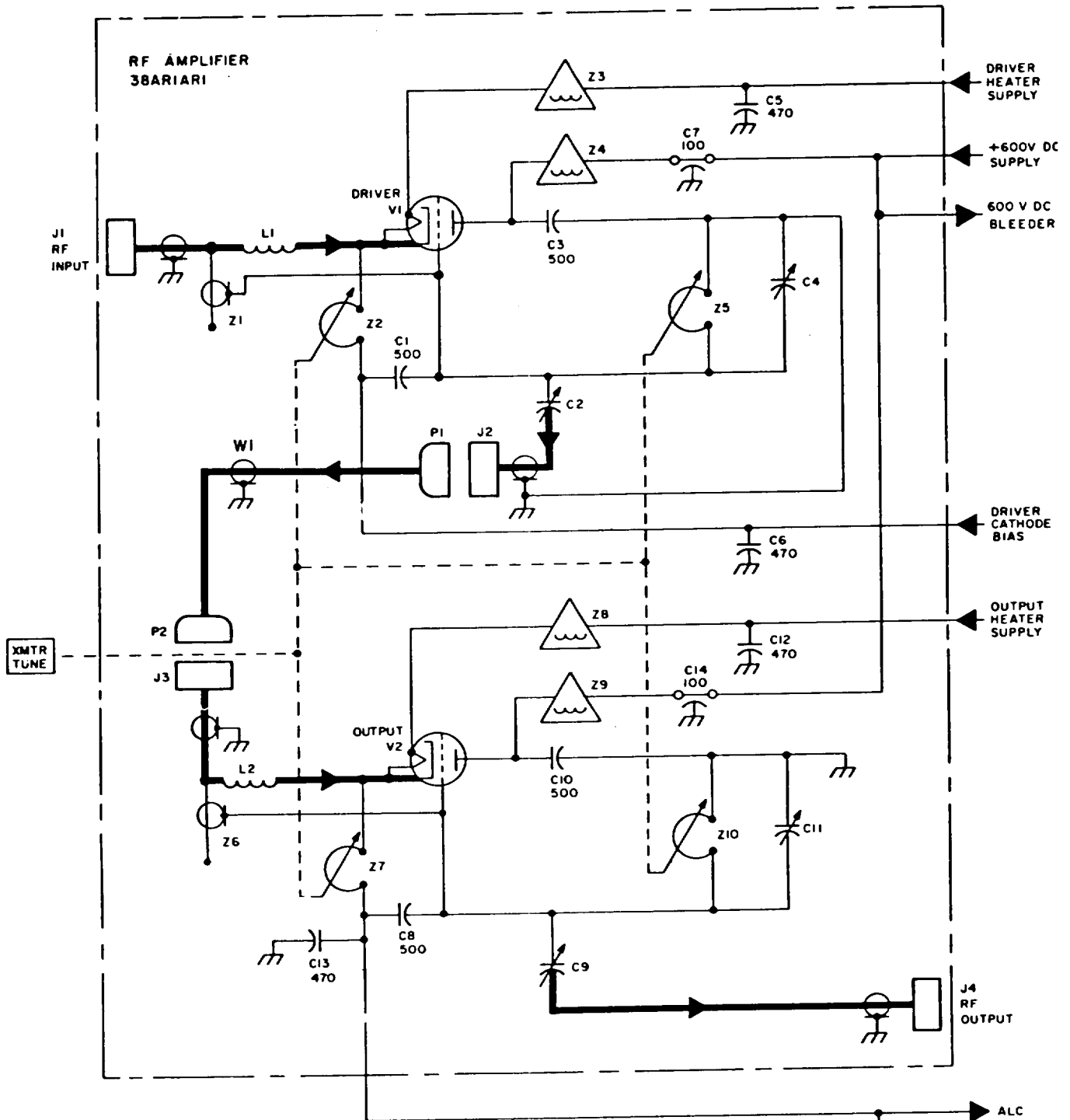


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Figure 2-91. RF Amplifier 38AR1AR1, Resonator Cavity, cross-sectional View.

of the resonators is by capacitive probes located at the tube of the plate-grid resonator.

b. Detailed Circuit Analysis (Fig. 2-92). The signal from amplifier frequency multiplier 38A1 is fed through connector J1 and input matching network L1, Z1 to the cathode of driver tube V1. Z1 is a section of open-circuit transmission line which forms a shunt capacitance to the grid of V1 which is at Dc ground. Z6 in the V2 circuit is similar and both provide impedance matching at the high frequency end of the frequency range. The driver V1 and output V2 circuits are identical. Z2 and Z7 are the cathode-grid resonant cavities and Z5 and Z10 are the plate-grid resonant cavities for the driver and output stages respectively. C5 and C12 are button-type standoff capacitors for the regulated heater supply to the driver and output stages. C7 and C14 are the feedthru capacitors for high voltage plate supply to the two stages. C4 is a trimmer capacitor in parallel with the plate-grid circuit and is used to compensate electron tube plate-grid capacitance spread of the driver stage. Similarly C11 is the trimmer capacitor in the output stage. C3 and C10 and C1 C8 are bypass capacitors and provide dc isolation. The input signal, at a level of 200 milliwatts, is fed to the cathode of the driver tube V1. The signal excites cathode resonator Z2 connected between cathode and grid of V1. The output signal from the plate of V1 resonates in plate-grid resonator Z5 and is coupled through coupling probe C2 to the output connector J2. Coupling probe C2 is preset during alignment. The driver tube output is fed through coaxial cable W1 to connector J3 of the output stage and then to the input matching network, Z6, L2. Z6 and L2 perform the same



NOTES 1.

| SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEGOHM           |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

2.

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Figure 2-92. RF Amplifier 38AR1AR1, Schematic Diagram.

function as Z1 and L1 in the driver circuit and Z6 is similar to Z1. The output and driver stages are electrically and mechanically similar. The cathode dc voltage of the output stage is fed back through the heater voltage regulator assembly to the amplifier frequency multiplier. The output cathode bias changes are used to produce the alc voltage which controls the output of the amplifier frequency multiplier (input to power amplifier). The final amplified signal is fed through coupling probe C9 to the output connector J4. The cathode currents are regulated by a constant current source within the transmitter power supply 5TR1PS1. Plate supply for the two tubes is 630 volts dc at about 180 milliamperes and is supplied through radio frequency interference filter 38AR1A1FL2 which suppresses any 5 kHz components on the 630 volt supply. Resistor assembly 38AR1A1A2 bleeds off any residual high voltage when the unit is disconnected. Channel-frequency indicator DS1 is also ganged to the XMTR TUNE control and provides a visual indication of the selected channel.

2-82. Voltage Regulator Assembly 38AR1A1A1

Voltage regulator assembly 38AR1A1A1 is identical to voltage regulator assembly 37AR1A1A1. Refer to paragraph 2-61 for general and detailed circuit descriptions.

2-83. Circulator 38AR1HY1

Circulator 38AR1HY1 is a 3-port ferrite device using permanent magnets. The rf output from power amplifier 38AR1AR1 is fed to J1 (port 1) of the circulator (FO-4-70). The circulator permits the transmission of the outgoing signal from port 1 to port 2 (J2) but prevents any reflected signal from reaching port 1. The reflected signal at port 2 is directed to port 3 (J3) where it is terminated in electrical dummy load 38AR1AT1. The dummy load is a resistive network with a low vswr and dissipates up to 35 watts at 1 GHz.

2-84. Low-Pass Filter 38AR1A1FL1

Low-pass filter 38AR1A1FL1 is connected between circulator 38AR1HY1 and power monitor 38AR1A2. Low-pass filter 38AR1A1FL1 is a sealed high power filter with a cutoff above 1,000 MHz. It filters out any harmonics of the transmitter output rf signal.

2-85. Rf Power Monitor 38AR1 A2

Rf power monitors 38AR1A2 and 37AR1A2 are identical. Refer to paragraph 2-63 for a functional description.

2-86. Control-Indicator 38A2 or 34A4

a. General. Control-indicators 38A2 (FO-4-70) (transmitter channel selector) and 34A4 (receiver channel selector) are identical in function and construction and also similar to control-indicator 6A3 (fig. 2-49). Each channel selector provides 13 control lines (1 through 13) to the frequency synthesizer in transmitter and receiver respectively. To select the required synthesizer in frequency, control lines 1 to 12 are switched on and off in a binary pattern with line 13 switched between channels 1279 and 1280 to change the synthesizer output frequency steps. The switching modules are operated by a set of cams and followers which reflect the various coding patterns as shown in the coding tables (FO-4-60).

b. Description of Operation. The control-indicator consists of a set of eleven microswitches and a logic module (decoder command signals). The microswitches are

operated by a set of cams to generate the binary code which presets the required stages of the programmed counter in synthesizer 5TR1A2 or 1RE1A2. The front panel channel-indicators consist of a series of numbered wheels. The indicating wheels are geared to the microswitch cams and to a front panel control knob. The transmitter channel selector display indicates the channel rather than the frequency selected. The following formulas should be used to translate a selected channel into a frequency and vice versa.

$$(1) \text{ Transmitter frequency} = \frac{\text{Transmitter channel} + 200}{2} \text{ MHz}$$

$$(2) \text{ Transmitter channel} = (\text{Transmitter frequency} - 200) \times 2$$

On the receiver channel selector the coding is arranged to produce a local oscillator frequency 30 MHz higher than the channel indicated in the display. This is done to permit the indicator to refer to the received signal frequency, the actual load oscillator frequency being always 30 MHz higher to provide the correct intermediate frequency. The decoder unit is an encapsulated logic circuit designed to sense channel coding on eleven microswitch output lines. Up to number 1280 (transmitter) the logic module produces the same output as the input, input two to output two and so on. At channel 1280 the logic module switches the inputs so that input 12 appears at output 11 and so on. The logic module then produces output 12 (line 12) and control line 13.

## Section IX. AMPLIFIER-CONVERTER AM-4318/GRC-103(V)

### 2-87. Functional Block Diagram Analysis of Amplifier-Converter AM-4318/GRC-103(V) (FO-4-62)

a. Amplifier-Converter AM-4318/GRC-103(V) (Band III receiver rf head), incorporates a duplexing system which enables the radio set to use a single antenna for both transmit and receive sections, and circuits which convert the incoming receive signal into a 30 MHz intermediate frequency.

b. The receiver rf head duplexer 34A1 provides the necessary isolation and impedance matching between the transmit and receive signals. The transmit signal at the PWR OUT connector of the transmitter rf head at a level of approximately 25 watts is fed through an external coaxial cable, through the FROM XMTR connector on the front panel of the receiver rf head, to duplexer subassembly 34A1A1. In the duplexer subassembly, the transmit signal is fed to a tuned two-cavity filter (resonators). The tunable transmit filter is manually tuned to the transmit channel by the XMTR DUPL control. The  $\pm 2$  MHz bandwidth of the filter provides additional filtering of the transmit signal while presenting a high attenuation to the received frequency. The transmit signal is then directed through impedance matching network 34A1A1Z1 and rf power monitor 34A3 to the ANT. connector, and through an rf coaxial cable to the antenna system. Rf power monitor 34A3 samples the forward and reflected power to and from the antenna system. These samples are rectified and the resulting dc voltages are used for XMTR DUPL and REFL PWR metering.

c. The receiving circuits of the receiver rf head accept modulated signals in the frequency range of 695 to 1000 MHz, at a level of -54 dbm to -94 dbm and convert

them to a 30 MHz intermediate frequency (IF) which is then amplified and demodulated in the receiver fixed head. The signals from the antenna, applied to the ANT. connector by the lead-in cable, are fed through impedance matching network 34A1A1Z1 to a 3 MHz bandwidth tunable four-cavity filter (receiver section of duplexer subassembly). The tunable receive filter is manually tuned to the receive channel by the RCVR SIG control. The received signal is then fed through a high signal protection circuit (signal level control-monitor) which prevents rf signals greater than +15 dbm from getting into the receiver. Signal level control-monitor also monitors the protection level and triggers the HIGH SIGNAL ALARM circuit when the input level exceeds +15 dbm.

d. The rf signals are fed through low pass filter 34FL1 which attenuates all harmonics of the incoming frequency. The output of the low pass filter is fed into the frequency mixer stage 34A7. The frequency mixer stage consists of two main circuits, a low-noise broadband rf amplifier and an image rejection mixer circuit. The 695 to 1000 MHz received rf signal is first amplified in a microwave integrated circuit amplifier. The second input to the frequency mixer stage is the local oscillator signal in the range of 725 to 1035 MHz from the frequency multiplier group 34A2 (e. below). The two signals are mixed in the two balanced mixers and the two resultant IF signals combined in a hybrid where the image rejection takes place. The 30 MHz IF output signal, 10 to 18 db above the level of the received rf signal is then fed to the IF amplifier 34AR1; the frequency mixer stage also contains a local oscillator signal metering circuit.

e. The input to the frequency multiplier group 34A2 is the output of amplifier-frequency multiplier 1RE1A5, in the range of 95 to 145 MHz. The frequency multiplier group 34A2 consists of three modules, frequency multiplier 34A2A2, frequency multiplier 34A2A1, and bandpass filter 34A2FL1. Frequency multiplier 34A2A2 doubles the input frequency from 1RE1A5. The resultant frequency from 34A2A2 is applied to the second module, frequency multiplier 34A2A1, which triples the frequency over one portion of the band and quadruples it over the remaining portion, to produce a continuously variable output frequency 30 MHz above the frequency of the received signal. Mechanically, the frequency multiplier 34A2A1 is ganged to the RCVR SIG control which also drives bandpass filter 34A2FL1, the third module of the frequency multiplier group. The bandpass filter 34A2FL1 attenuates the unwanted submultiple of the output frequency from the frequency multipliers. The RCVR SIG control adjusts the variable frequency multiplier 34A2A1 and the bandpass filter 34A2FL1 to a point near the required tuning point, approximately 30 MHz above the frequency of the received signal. The MULT PEAK control then tunes the variable frequency multiplier and the bandpass filter to the required tuning point. The ganging of the RCVR SIG and MULT PEAK is such that the output frequency from the frequency multiplier group 34A2 (local oscillator) is always 30 MHz above the duplexer receiver section. The local oscillator signal is then fed into the frequency mixer stage 34A7A1 where it is mixed with received rf signal to produce a 30 MHz IF signal. A portion of the local oscillator signal is detected and rectified in the frequency mixer stage 34A7A1 to provide the MULT metering voltage. The IF signal from the mixer stage is amplified in intermediate frequency amplifier 34AR1. The intermediate frequency amplifier 34AR1 is part of the IF amplification system which also includes bandpass filter 1RE1FL1 and intermediate frequency amplifier 1RE1AR2 in the receiver fixed head. Intermediate frequency amplifier 34AR1 has a nominal gain of 50 db without agc and d maximum gain of 10 db with maximum age. Automatic gain control of two stages in each of the two IF amplifiers provides automatic adjustment of overall gain over a range of 50 db, depending on the input signal. Intermediate frequency amplifier 34AR1 is a broadband device, all shaping being done in bandpass filter 1RE1FL1.

f. Operating voltages, +12 v and -12 v regulated and 26 v unregulated, required for the circuits in the receiver rf head, are supplied by the power supply 1RE1PS1 in the receiver fixed heads. An overall schematic diagram of the receiver rf head unit 34 is shown in F0-4-63 and an interconnecting diagram is shown in F0-4-64.

## 2-88. Duplexer Subassembly 34A1A1

a. General. Since Radio Set AN/GRC-103(V) operates with a single antenna, duplexer subassembly 34A1A1, part of duplexer 34A1, is necessary to provide isolation between the transmitted signal and the received signal. The duplexer subassembly, basically, consists of two coaxial cavity filters with a common port (ANT. connector); one filter provides filtering of the transmitter signal and the other filters the received signal. The duplexer subassembly also contains an impedance matching network 34A1A1Z1 which matches the transmit and receive filters to the antenna over the entire frequency range; S1 is a shorting device used during the alignment of transmit cavity 27 and receive cavities Z2, Z3. In addition to the cavity filters and impedance matching network, the duplexer subassembly also contains the gearing and mechanical drive for the voltage control assembly 34A1A2 and frequency multiplier group 34A2. The chassis of the duplexer subassembly is the main structural member of the amplifier-converter Am-4318/GRC-103(V).

### b. Detailed Circuit Analysis (F0-4-63).

(1) Transmitting path. The transmitter portion of the duplexer subassembly consists of two quarter-wave resonant tuned cavities, 34A1A1Z6 and 34A1A1Z7. The cavities are connected in series through an intercavity coupling network. The coupling network provides the correct impedance transformation between adjacent resonators for realization of proper filter response. Both cavities are tuned in parallel with adjustable plungers controlled by the XMTR DUPL front panel control. The channel to which the transmitter cavities are tuned is indicated by channel-frequency indicator 34A1A1DS2 in the XMTR CHANNEL display window. The input and output of the resonators are connected through the end resonator coupling networks which transform the 50 ohm impedance of the system up to the correct level required by the resonators. The filter has a pass band of  $\pm 2$  MHz and an insertion loss of 1.5 db for 90 percent of the band and 2.0 db for the remainder. The output of the filter, from the end resonator coupling network, is fed to the impedance matching network 34A1A1Z1 which matches the impedance of the transmitter to the antenna. The transmitter output is then fed through power monitor 34A3 to the antenna. Power monitor 34A3 measures the forward and reverse (reflected) power of the transmitted signal. Spark protection during tuning is afforded the cavities by spark gaps E2 and E4.

(2) Receiving path. The received signal from the antenna is connected through power monitor 34A3 and impedance matching network 34A1A1Z1 to the end resonator coupling network of the receiver cavity filter. The receiver portion of the duplexer subassembly consists of four quarter-wave resonant tuned cavities, 34A1A1Z2 to 34A1A1Z5. The cavities are connected in series through intercavity coupling networks. The coupling networks provide the correct impedance transformation between adjacent resonators for realization of proper filter response. All four cavities are tuned in parallel by adjustable plungers controlled by RCVR SIG front panel knob. The channel to which the receiver cavities are tuned is indicated by channel-frequency indicator 34A1A1DS1 in RCVR CHANNEL display window. The receiver filter has a pass band of  $\pm 3$  MHz and an insertion loss of 2.0 db for 90% of the band and 2.5 db for the remainder of the band. The input and output of the resonators are

coupled through end coupling networks which provide the correct source and terminating impedances for the filter. Spark protection during tuning is afforded the cavities by spark gaps E1 E3, E5 and E6.

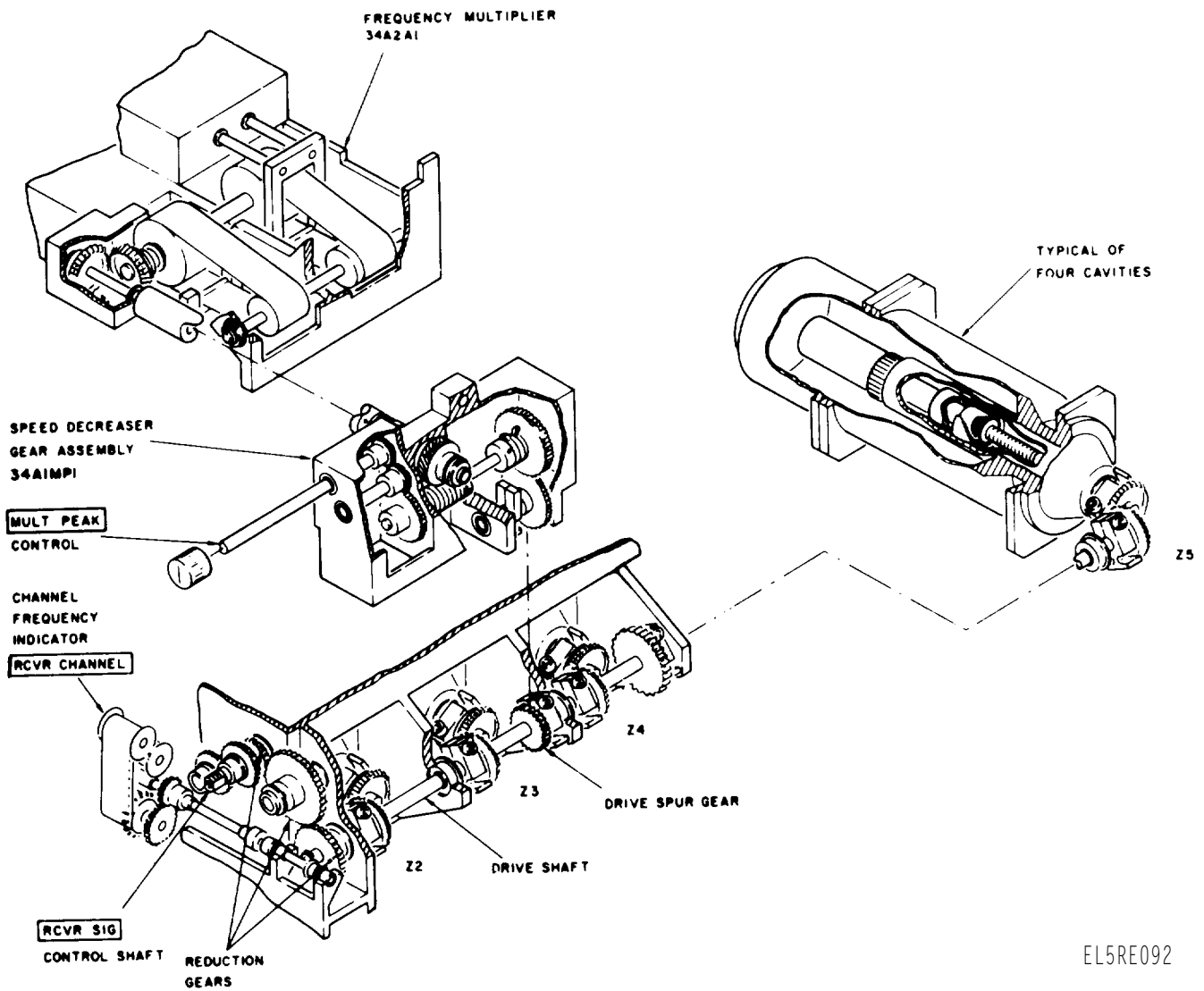
(3) Coupling networks. A coupling network between two adjacent resonators is provided to give the correct impedance transformation. The required characteristics are achieved by using a T-network of L-C circuits. These coupling networks between resonators Z2, Z3, Z4 and Z5, in the receive section, are identical except for the value of their components. A typical coupling network between resonator Z2 and Z3 consists of a series inductor L4 in parallel with variable capacitor C4, a series inductor L8 in parallel with variable capacitor C5 and a variable shunt inductor L6. Z11 in parallel with L6 is the stray capacitance existing between the coils when located in their housing. The coupling network between resonator Z6 and Z7 in the transmit section consists of series inductors L3, L7 and a variable shunt inductor L5. Z10 in parallel with L3 is the stray capacitance of L3 and similarly Z12 and Z13 are stray capacitance of L5 and L7 respectively.

(4) End resonator coupling network. The input and output end resonators of the receive and transmit filters are terminated in special coupling networks. These networks transform the 50 ohm impedance of the system up to the correct level required by the resonators, for realization of proper filter response. The input network in the receive filter consists of an inductor L2 in parallel with variable capacitor C1. A similar network at the output consists of inductor L16 and parallel variable capacitor C14. The input and output networks in the transmit section are similar, the inductors are fixed but the capacitance of these fixed inductors can be varied by a movable shield.

(5) Impedance matching network 34 A1A1Z1. This unit provides a common junction for the transmit and receive filters. The network consists of a T-junction. One arm is a 50 ohm transmission line which terminates at the duplexer connector J1, and the other two arms of the T are identical 100 ohm transmission lines. The two 100 ohm arms are connected in series with their respective filter at the resonator coupling network coil. The electrical length of these two arms changes with the on-tune and off-tune frequencies and thereby maintains the proper match between transmit and receive filters to the antenna over the entire frequency range of 695 to 1000 MHz.

(6) Tuning mechanism. The tuning of duplexer subassembly 34A1A1, variable frequency multiplier 34A2A1; and voltage control assembly 34A1A2 is accomplished through two main shafts mounted on the duplexer chassis. One shaft tunes the transmitter section of the duplexer subassembly and the other shaft tunes the receiver section of the duplexer subassembly, the frequency multiplier and the voltage control assembly. The transmitter section drive shaft, connected to the XMTR DUPL control through reduction gears (fig. 2-84), carries three bevel gears. Two bevel gears drive the two individual center conductor drive screws of the resonant cavities, and the third gear drives the XMTR CHANNEL indicator. Similarly, the receiver drive shaft, connected to the RCVR SIG control through reduction gears (fig. 2-93), carries five bevel gears. Four bevel gears drive the four individual center conductor drive screws of the receiver resonant cavities. The fifth gear drives the RCVR CHANNEL indicator. Also carried on the receiver section drive shaft are two reduction spur gears. One gear drives speed decriaser gear assembly 34A1MP1. The speed decriaser gear assembly provides tracking between the receiver duplexer cavities and the frequency multiplier and at the same time permits a small adjustment of the frequency mulitplier, relative to the receiver duplexer, using the MULT PEAK control.





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Figure 2-93. Duplexer Subassembly 34A1A1, Receiver Section, Tuning Mechanism.

This unit consists of a precision aluminum casting which incorporates a speed reduction of 40 to 1 through a worm and plastic worm gear. The clutch and stop device, mounted on the unit's main shaft, provides continuous coupling between the duplexer subassembly and the frequency multiplier during tuning by the RCVR SIG control; it also permits a slippage during two and one-quarter turns of the MULT PEAK control. The stop device is made of three stop washers and prevents failure of the clutch. The second spur gear on the receiver drive shaft provides a coupling to voltage control assembly 34A1A2. The voltage control assembly provides the tuning voltage for a varactor filter in frequency mixer stage 34A7.

2-89. Rf Power Monitor 34A3

Rf power monitor 34A3 is identical to rf power monitor 33A3. Refer to paragraph 2-67 for a functional description.

2-90. Signal Level Control-Monitor 34A5

Signs level control-monitor 34A5 is identical to signs level control-monitor 33A5. Refer to paragraph 2-68 for a functional description.

2-91. Low-Pass Filter 34FL1

Low-pass filter 34FL1 is a sealed unit connected between signal level control 34A5 and frequency mixer stage 34A7. It is used to suppress the-harmonics of the incoming frequencies and provides a minimum of 35 db rejection at all frequencies above 2085 MHz (3 times the lowest fundamental). The vswr at either port does not exceed 1.31:1 and the power handling capacity is 25 dbm continuous.

2-92. Frequency Mixer Stage 34A7

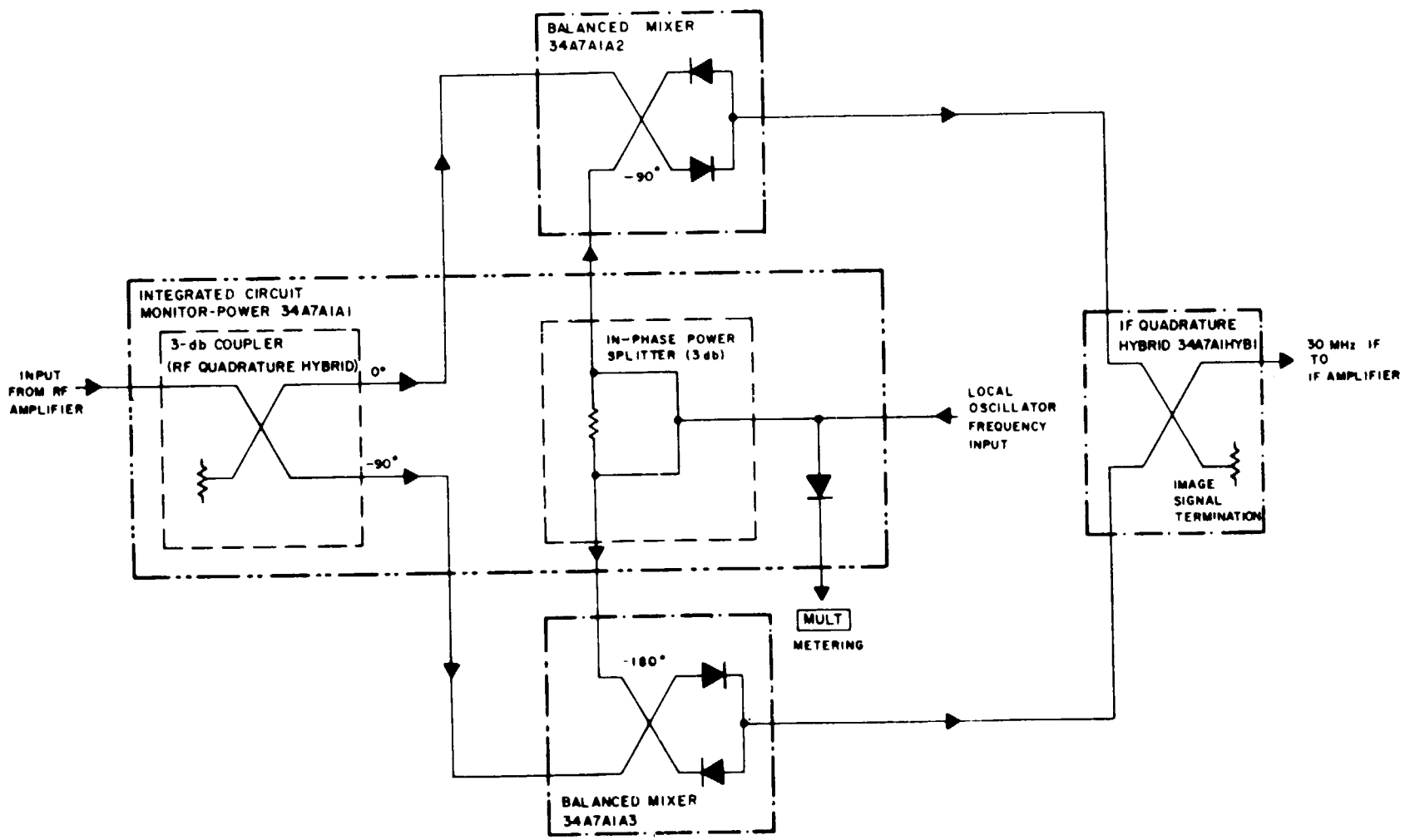
a. General. The frequency mixer stage consists of the following four separate integrated circuit subassemblies, soldered to a printed circuit board 34A7A1: rf Amplifier 34A7A1AR1, I/C monitor-power 34A7A1A1, two balanced mixers 34A7A1A2 and 34A7A1A3, and a 3 db coupler quadrature hybrid 34A7A1HYB1 (IF). The construction of frequency mixer stage 34A7 is identical to that of frequency mixer stage 33A7 (para 2-70). The received rf signal in the range of 695 to 1000 MHz from the low pass filter 34FL1, and the local oscillator signal between 725 and 1035 MHz from the bandpass filter 34A2FL1 are mixed in the two balanced mixers; the resultant 30 MHz IF outputs are then quadrature coupled and fed to the IF amplifier 34AR1. Conversion gain of the frequency mixer stage 34A7 is between 10 and 18 db, while the noise figure is below 4.5 db.

b. Circuit Description (F0-4-61). The rf input at 34A7J1 is applied directly to pin-1 of the rf amplifier 34A7A1AR1. The two-stage, low-noise, broadband amplifier is a microwave integrated circuit, using high gain; low-noise microwave transistors in their coplanar stripline package; fabrication of the rf amplifier circuits on an alumina substrate using thin film technology, provides a good control of assembly parasitic. The gain of the rf amplifier is 19 dbm  $\pm$ 2 db with a noise figure 2.8 db. +12 v and -12 vdc operating voltages are applied to pins 3 and 2 of the rf amplifier, FL1 and FL2 provide rf filtering of the dc lines.

(1) The integrated circuit monitor-power 34A7A1A1 combines the functions of a 3 db coupler, an in-phase power divider and a power monitor. The rf signal at pin 4 of the rf amplifier is applied through pin 1 of monitor-power to the 3 db coupler assembly (rf quadrature hybrid) (fig. 2-93). The two rf outputs in quadrature phase are applied through pins 7 and 2 (F0-4-61) to balance mixers 34A7A1A2 and 34A7A1A3 respectively.

(2) The local oscillator signal is applied through pin 4 of monitor-power to an in-phase hybrid power divider; the two resultant local oscillator outputs are then applied in-phase through pins 3 and 6 to the two balanced mixers. The rf voltage of the incoming local oscillator signal is detected and the dc voltage is made available through pin 5 to output connector P1 pin 4 for MULT metering. Like the rf amplifier 34A7A1AR1, the monitor-power is a microwave integrated circuit realized by using thin film technology on alumina substrate.

(3) The two balanced mixer stages provide products  $\pm$  30 MHz around the local oscillator frequency. The two mixers are identical, only the input pin numbers are



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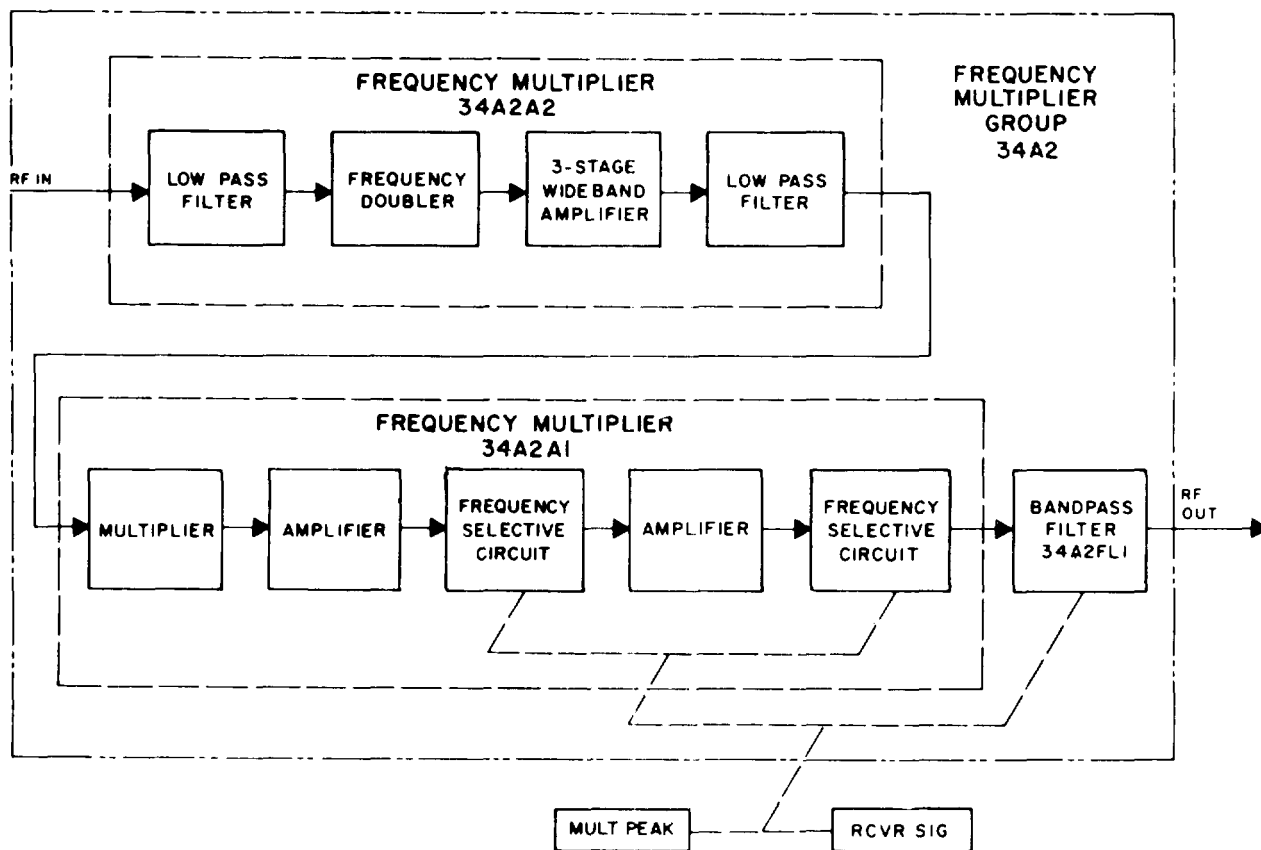
Figure 2-94. Image Rejection Mixer Circuit, Simplified Functional Diagram.

different. The balanced configuration of the mixers provides optimum spurious performance.

(4) The two IF signals are then quadrature coupled within the 3 db coupler quadrature hybrid 34A7A1HYB1 where the image noise product is terminated within a resistive load. The output port of the hybrid is matched for interface with the IF Amplifier 34AR1. L1-A, C1 and L1-B, C2 (low pass filters) filter the two mixer outputs. Image rejection is achieved within R1.

2-93. Frequency Multiplier Group 34A2 (Fig. 2-95)

a. General. Frequency multiplier group 34A2 provides the final local oscillator frequency to the mixer, 30 MHz higher than the received rf signal. The frequency multiplier group consists of three subassemblies; frequency multiplier 34A2A2, frequency multiplier 34A2A1, and bandpass filter 34A2FL1. The 34A2A2 doubles the incoming frequency from the receiver fixed head. The 34A2A1 is a variable frequency multiplier, and produces the final local oscillator frequency in the range of 725 to 1,030 MHz, by multiplying a portion of the input frequencies by three to produce 725.0 to 839.5 MHz, and multiplying the other portion of the input frequencies by four to produce 840.0 to 1,030 MHz. The change in multiplication factor is accomplished by changing the input frequency to the point where the output tuned circuit selects the required harmonics. The third harmonic is selected over the required portion of the band and then the input frequency is stepped down to the point where



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Figure 2-95. Frequency Multiplier Group 34A2, Block Diagram.

the tuned circuit selects the fourth harmonic. Bandpass filter 34A2FL1 is a tunable filter which attenuates all unwanted submultiple of the local oscillator frequency applied to the frequency mixer stage.

b. Block Diagram Analysis (Fig. 2-95). The rf input in the range of 95 to 145 MHz, at a level of +15 dBm, is fed into the low pass filter section of frequency multiplier 34A2A2 where the unwanted signals are removed. The filtered signal is then fed to the full-wave diode frequency doubler and then amplified in the 3-stage wide band rf amplifier. The output signal in the frequency range of 190 to 290 MHz is filtered again in the low pass filter at the output of 34A2A2. The output of the frequency multiplier 34A2A2 in the frequency range of 190 to 290 MHz, at a level of +16 dBm $\pm$ 1.5 dBm, is fed to the multiplier section of the variable multiplier 34A2A1. The multiplier section generates a signal rich in harmonics, which is then amplified and filtered in two separate stages. The frequency selective circuits are ganged to the front panel RCVR SIG and MULT PEAK controls. The tuned circuits select the third or fourth harmonics, thereby producing a variable frequency 39 MHz higher than the received frequency. The output of 34A2A1 is fed to tunable bandpass filter 34A2FL1 which attenuates the unwanted submultiple of the local oscillator frequency. The bandpass filter is also ganged to the front panel RCVR SIG and MULT PEAK controls (fig. 2-93) and is tuned, with the frequency selective circuits, 30 MHz above the frequency of the received signal.

#### 2-94. Frequency Multiplier 34A2A2

Frequency multipliers 33A2A2 and 34A2A1 are identical. Refer to paragraph 2-72 for general and detailed circuit analysis descriptions.

#### 2-95. Frequency Multiplier 34A2A1

a. General. The frequency multiplier 34A2A1 is part of the local oscillator chain and provides the final local oscillator frequency to the frequency mixer stage. It provides times-three (725.00 to 839.5 MHz) or times-four (840.00 to 1030.00 MHz) multiplication of the input frequency at an output level of +12 dBm. The input to the unit is the output of frequency multiplier 34A2A2. The output of the unit is fed to bandpass filter 34A2FL1 before being applied to frequency mixer stage 34A7. The 34A2A1 unit consists of one printed wiring board and a casting which contains two tunable cavities. The tuning plungers of the cavities are coupled mechanically through a stainless steel band to speed decreaser gear assembly 34A1MP1 (fig. 2-93). The unit is tuned by the RCVR SIG and MULT PEAK controls through 34A1MP1.

#### b. Detailed Circuit Analysis (FO-4-59).

(1) Multiplier section. The output of the frequency multiplier 34A2A2, in the frequency range of 195 to 290 MHz at a level of +17 dbm  $\pm$ 2.0 db, is applied to 34A2-A1 input connector J1. The signal from J1 is applied to a low pass filter consisting of R8, R9, L2, L3 and C9. The low-pass filter reduces the input power to approximately +14 dbm, the optimum input level for fourth harmonic frequency generation by transistor multiplier Q1. The low-pass filter also provides input matching to the transistor. The output of the low pass filter is coupled through C10 to the base of multiplier transistor Q1. C11 is a bias feed-through capacitor. R10 sets the bias level so that multiplier transistor Q1 operates in class C. Q1 produces a signal rich in third and fourth harmonics which is fed through resonator Z5 to a two stage amplifier Q2, Q3. Z5 and Z8, at the output of the harmonic generator Q1 and

amplifier Q3 respectively, are tuned to select the required harmonics. Both resonators are ganged to the front panel RCVR SIG control. CR1 defines the voltage across Q1 so that the class C output current peaks applied to Z5 are of constant amplitude. Z2 is an inductive distributed impedance tuned by shorting strap E4. Z2 is a strip-line which tunes the input reactance of Z5. Z4 and Z6 are the inductive impedance of Z5. At Z5 and Z8, cavity adjustment capacitors C1 and C3 respectively are the middle frequency adjustment screws and C2 and C4 are the high frequency adjustment screws. R19 is the collector load resistance for Q1 and provides stability of in-band frequencies. C13 is the Q1 emitter decoupling capacitor.

(2) Amplifier section. The output of the frequency multiplier transistor tuned to the received frequency in resonator Z5, is coupled through C14 and input matching network C15, Z4, Z5, R11, R12 to the base of amplifier Q2. R11 and shunt resistor R12 provide stability at the input and similarly, R14 and shunt resistor R13 provide stability at the output. The amplified signal is coupled from the collector of Q2 through equalizer C18, Z6, R14 to a bandpass filter network. The bandpass filter attenuates the fundamental frequencies. The input and output matching networks for the second amplifier stage Q3 are similar to the first stage. Both stages are operated in class A with an overall nominal gain of 12 db. R2, R3 and R4, the voltage divider, provide proper bias for the operation of Q2 in class A. Similarly, R5, R6 and R7 provide proper bias for Q3. CR2 and CR3 provide reverse bias breakdown protection. The output of the amplifier is coupled through C27 and the tuned resonator Z8 to the output connector J2.

#### 2-96. Bandpass Filter 34A2FL1 (F0-4-63)

The output of variable frequency multiplier 34A2A1 is fed to the input connector PI of bandpass filter 34A2FL1. The filter consists of two quarterwave coaxial line cavities Z1 and Z2. The cavities are tuned by varying the length of their center conductor plunger. The rf signal is coupled to and from the cavities by inductive loops. The loops are adjusted by a setscrew. The coupling between the two cavities is by fixed slot coupling. The two cavities are ganged to the front panel RCVR SIG and MULT PEAK controls. The bandpass filter attenuates the unwanted submultiple of the local oscillator frequency to be applied to the frequency mixer stage. The cavities are located in an aluminum casting with the cavities tuning drive mechanism forming an integral part of the unit. A drive band of stainless steel fixed to a roller is coupled to the cavity plungers. The tuning drive rollers of frequency multiplier 34A2A1 and bandpass filter 34A2FL1 (fig. 2-931, use a common shaft which is actuated by the front panel controls.

#### 2-97. Intermediate Frequency Amplifier 34AR1

Intermediate frequency amplifier 34AR1 is identical to intermediate frequency amplifier 33AR1. Refer to paragraph 2-76 for circuit descriptions.

#### 2-98. Power Supply 34PS1

Power supply 34PS1 and power supply 33PS1 are identical. Refer to paragraph 2-77 for circuit descriptions.

#### 2-99. Voltage Control Assembly 34A1A2

Voltage control assembly 34A1A2 and voltage control assembly 33A1A2 are identical. Refer to paragraph 2-77 and figure (F0-4-63).

Section X. AMPLIFIER-FREQUENCY MULTIPLIER AM-4323/GRC-103 (V)  
BAND IV TRANSMITTER RF HEAD (UNIT 40)

2-100. Functional Block Diagram Analysis of Amplifier-Frequency Multiplier  
AM-4323/GRC-103(V) (Fig. 2-96)

a. The rf output of the transmitter fixed head (95 to 145 MHz at approximately +35 dbm) is fed into Amplifier-Frequency Multiplier AM-4323/GRC-103(V), the Band IV transmitter rf head, where it is multiplied and amplified to produce the final transmitter channel frequency. Multiplication is accomplished in amplifier-frequency multiplier 40A2, which multiplies the signal received from the transmitter fixed head by 12 to provide frequencies of 1350 to 1679.5 MHz and by 16 for frequencies of 1680 to 1849.5 MHz. The desired frequency is selected in a tunable cavity resonator, which is incorporated in the amplifier-frequency multiplier and ganged to the XMTR TUNE control on the front panel. An alc controlled rf amplifier (40A2AR2) amplifies the multiplied signal to a nominal +27 dbm level.

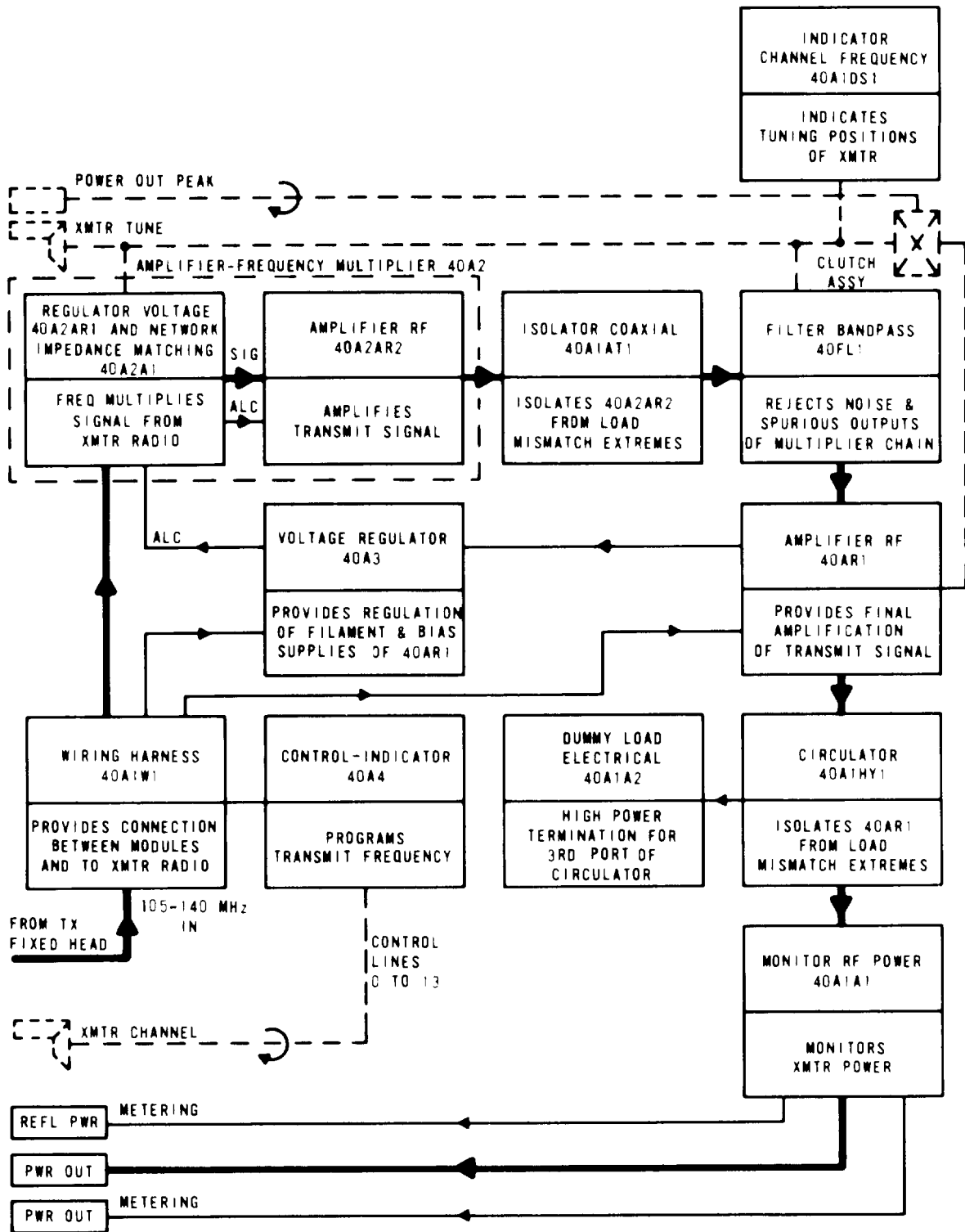
b. The amplified signal is fed through two-port isolator 40A1AT1 to bandpass filter 40FL1. Rf amplifier 40A2AR2 is isolated from load mismatch extremes by the isolator. Spurious outputs and noise from the multiplier chain is rejected by the bandpass filter, which also delivers a nominal +24 dbm output to amplifier 40AR1.

c. Amplification of the signal to the final output level is accomplished in tunable two-stage rf amplifier 40AR1 with two selected planar triodes (type 7211, SM-A-794144). The triodes are mounted in tuned-cathode 3/4 wavelength and tuned-plate 1/4 wavelength coaxial cavities. Input/output power coupling is achieved by fixed capacitive probes, and triodes are cooled by air forced through a honeycomb structure incorporated to minimize radio frequency interference. Voltage regulator assembly 40A3 provides the regulated heater supply for the driver and output tubes.

d. Rf amplifier 40AR1, bandpass filter 40FL1, and amplifier-frequency multiplier 40A2 are ganged to the XMTR TUNE control on the front panel, which tunes all three stages to the desired frequency. Channel frequency indicator 40A1DS1 indicates the frequency to which the transmitter is being tuned, and the front panel PWR OUT PEAK control permits rf amplifier 40AR1 to be fine tuned separately for maximum output power.

e. The amplified signal is fed through three-port circulator 40A1HY1 and power monitor 40A1A1 to the PWR OUT connector on the front panel. Isolation of rf amplifier 40AR1 from load mismatch extremes is effected by the circulator. The third port of the circulator is terminated in dummy load 40A1A2. Samples of output power and reflected power are rectified by power monitor 40A1A1. Resultant dc voltages are taken out as REFL PWR and PWR OUT metering signals.

f. Control-indicator 40A4 (channel selector) is an electromechanical device operating in conjunction with electrical frequency synthesizer 5TR1A2 and amplifier-monitor 5TR1A5 to the transmitter fixed head to provide 14 control lines (0 through 13). Control lines 0 through 12 program the frequency generating circuits in the electrical frequency synthesizer. In order to keep the transmitted deviation constant for different multiplication factors, control line is fed through amplifier-frequency multiplier 40A2 to the transmitter fixed head to control variable attenuators in the amplifier-monitor at the multiplication factor changeover point.



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Figure 2-96. Band IV Transmitter RF Head, AM-4323/GRC-103(V), Block Diagram

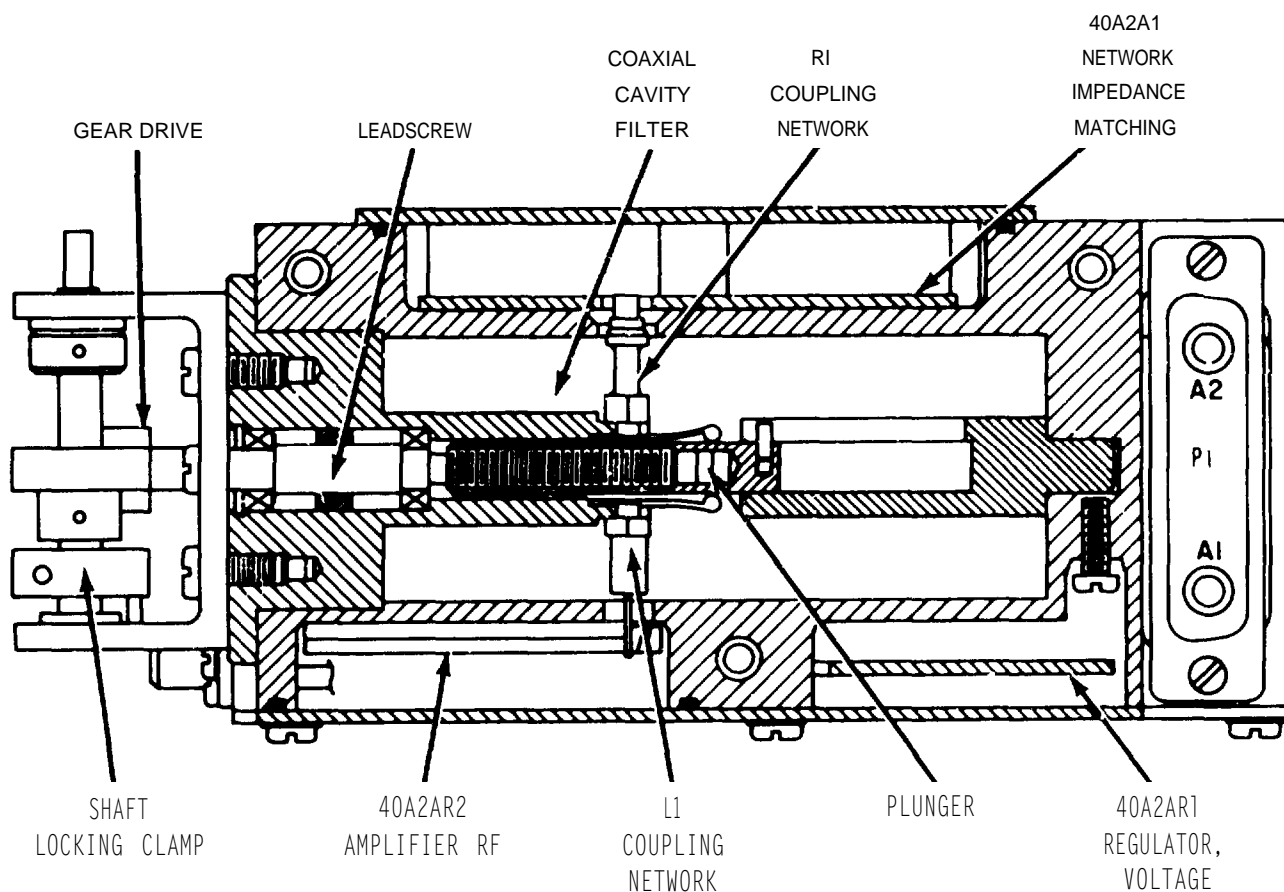


An overall schematic diagram of the Band IV transmitter rf head is shown in FO-4-76. An interconnecting diagram is shown in figure FO-4-77.

2-101. Amplifier-Frequency Multiplier 40A2

a. General. Amplifier-frequency multiplier 40A2 multiplies the transmitter fixed head signal by 12 or 16 to produce the final transmitter frequency of 1350 to 1849.5 MHz. This frequency is fed through coaxial isolator 40A1AT1 to bandpass filter 40FL1 to provide the input drive for rf amplifier 40AR1.

b. Mechanical Assembly (Fig. 2-97). Amplifier-frequency multiplier 40A2 consists of three printed circuit board assemblies mounted in a cast-aluminum housing which incorporates a tunable, coaxial, cavity filter as an integral part of the casting. Impedance matching network 40A2A1 is found on one printed circuit board assembly, voltage regulator 40A2AR1 on another, and rf amplifier 40A2AR2 on the third. The coaxial cavity is tuned by a plunger connected to a leadscrew which is externally ganged through a gear assembly to the front panel XMTR TUNE control. A signal from rf amplifier 40AR1 automatically controls the output level of amplifier-frequency multiplier 40A2.



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Figure 2-97. Amplifier-Frequency Multiplier 40A2, Cross-Sectional View.

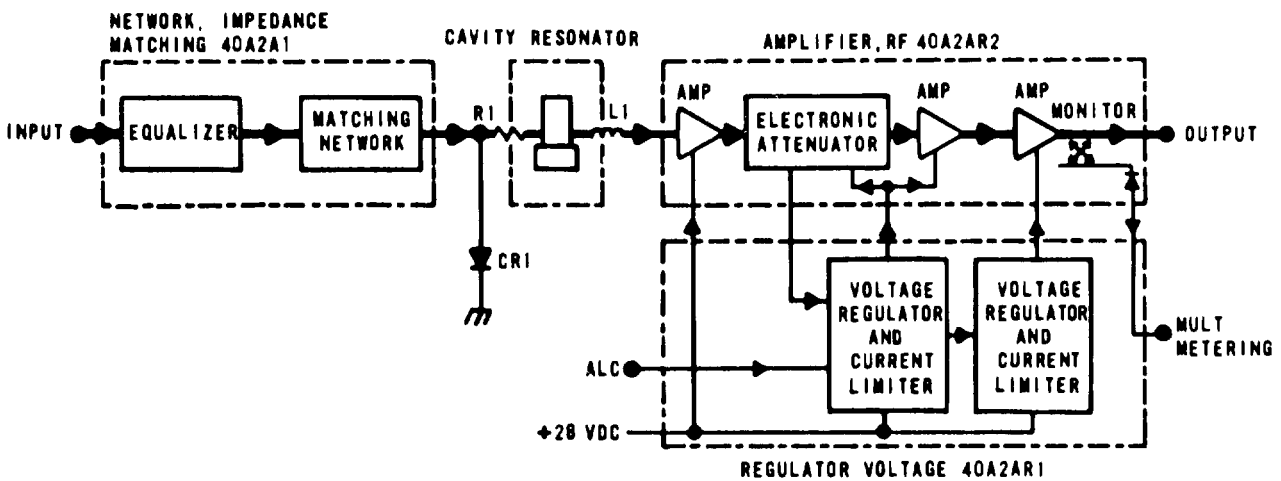
c. Block Diagram Analysis (Fig. 2-98). The output of amplifier-frequency multiplier 5TR1A4, in the range of 105 to 140 MHz at a level of approximately +35 dBm, is fed through impedance matching network 40A2A1. Frequencies in the lower part of the range are attenuated, while frequencies in the upper part are transmitted with no loss, by the equalizer stage of 40A2A1, to help maintain a more constant level of generated harmonics from multiplier diode CR1. The matching network stage transforms the 50 ohm input impedance to match the impedance of multiplier diode CR1.

(1) Diode CR1 generates a series of harmonics of the received signal (below and above 2,000 MHz) which are applied to the tunable cavity resonator of 40A2. The resonator selects the 12th harmonic for all frequencies from 1350 to 1679.5 MHz or the 16th harmonic for all frequencies from 1680 to 1849.5 MHz. It feeds the selected harmonic to rf amplifier 40A2AR2, a three-stage wideband amplifier that amplifies the signal by a nominal 12 db.

(2) Couplings R1 and L1 ensure sufficient match of resonator input and output impedance to achieve the correct loaded Q. A portion of the output signal is fed into a metering circuit where it is rectified and used as the MULT metering signal.

(3) Automatic level control of the output signal from 40A2AR2 is provided through voltage regulator 40A2AR1. The alc circuit is driven by a signal from rf amplifier 40AR1 which is fed through voltage regulator 40A3 to voltage regulator 40A2AR1. Two current limiters in 40A2AR1 provide current limitation for the second and third stages of 40A2AR2. A switching relay in 40A2AR1, operated by a signal on control line 13 from control-indicator 40A4, provides modulation control to the modulator in the fixed head at the multiplication factor changeover point.

d. Detailed Circuit Analysis (FO-4-75). An input of 105 to 140 MHz is fed to pin E1n the printed circuit board of impedance matching network 40A2A1 via connector P1 (pin A1). Resistors A1R1, A1R2 and A1R3 provide an attenuation network for lower frequencies, while components A1C1-A1L2 and A1C2-A1L1 provide an rf bypass circuit for the higher frequencies. A lowpass matching network (A1C3 through A1C7, A1L3 and A1L4) matches the impedance of step recovery diode CR1. Temperature variable bias resistance is provided by A1RT1, and A1L5 tunes with the capacitance of CR1 to maxi-



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Figure 2-98. Amplifier-Frequency Multiplier 40A2, Block Diagram.

mize rf current circulation through the diode. Capacitor C1 acts as a dc block, preventing a shortcircuit of bias through tuned cavity resonator Z1. Network R1-L1 matches input and output impedances to the cavity resonator. The selected frequency (1350 to 1849.5 MHz) is fed to terminal E1 on the printed circuit board of rf amplifier 40A2AR2, where it is amplified by approximately 12 db. Amplifier 40A2AR2 consists of three amplifier stages, with a variable electronic attenuator between the first and the second amplifier stages and a monitor stage after the third amplifier stage to supply the MULT metering signal. The first stage is a grounded emitter circuit which operates in class AB and normally draws about 35 ma of idling current at 6 volts VCE, while the second and third stages are grounded base circuits operating in class C.

(1) Resistors AR2R1, AR2R2 and AR2R3 form a 4.0 db Pi-type attenuator which provides a good source impedance for AR2Q1 and isolates it from cavity resonator Z1. A highpass filter network, consisting of AR2C2, AR2L1 and AR2C3, rejects the fundamental frequency from cavity resonator Z1 (105 to 140 MHz) to prevent saturation of AR2Q1.

(2) Variable microwave capacitors AR2C4, AR2C8, AR2C11, AR2C13, AR2C18, AR2C19 and AR2C23 provide interstate impedance matching of the three amplifier stages. Capacitors AR2C14 and AR2C20 function as blocking capacitors, whereas AR2L4 and AR2L6 provide a dc return for the two class C stages. Resistors AR2R7, AR2R9, AR2R10 and AR2R11 stabilize the amplifier in the required frequency range of 1350 to 1849.5 MHz.

(3) All dc supplies from voltage regulator 40A2AR1 are applied to the amplifier through Pi-type filters to reduce the effect of spurious signals or noise from the power supply on amplifier stability. A portion of the rf output power is capacity coupled through AR2C25 and detected by diode AR2CR2. Rf decoupling is provided by AR2C26, and a dc return is provided by AR2R14. The detected dc signal is fed to the metering circuit in the transmitter fixed head for MULT meter indication.

(4) Zener diodes AR1CR2 and AR1CR3 regulate the dc voltage at AR1E11 (second stage supply) and AR1E7 (third stage supply) to within 11.5 v ( $\pm 0.5$  v) and 19.5 v ( $\pm 0.5$  v) respectively. Current (11.5 v ( $\pm 0.5$  v) and 19.5 v ( $\pm 0.5$  v)) limitation in the second and third stages is set to 80 ma max and 220 ma max respectively by resistors AR1R15 and AR1R16, to keep transistor stress below 65 percent.

(5) When the input drive at the second or third stage of 40 A2AR2 is excessive, transistor AR1Q5 or AR1Q6 turns on and the voltage at the collector of AR1Q4 drops. Less current therefore flows through PIN diode AR1CR1. PIN diode resistance increases, resulting in attenuation to the second or third stage, until equilibrium is reached.

(6) ALC signal from voltage regulator 40A3 is fed through connector P1 (pins 7 and 8) to amplifier circuit AR1Q2. In case of excessive rf input drive to rf amplifier 40AR1, an alc signal turns on transistor AR1Q2, which pulls down the base voltage of AR1Q5 and hence the emitter voltage. This reduces the gain of the third stage and consequently the rf output power of 40A2AR2.

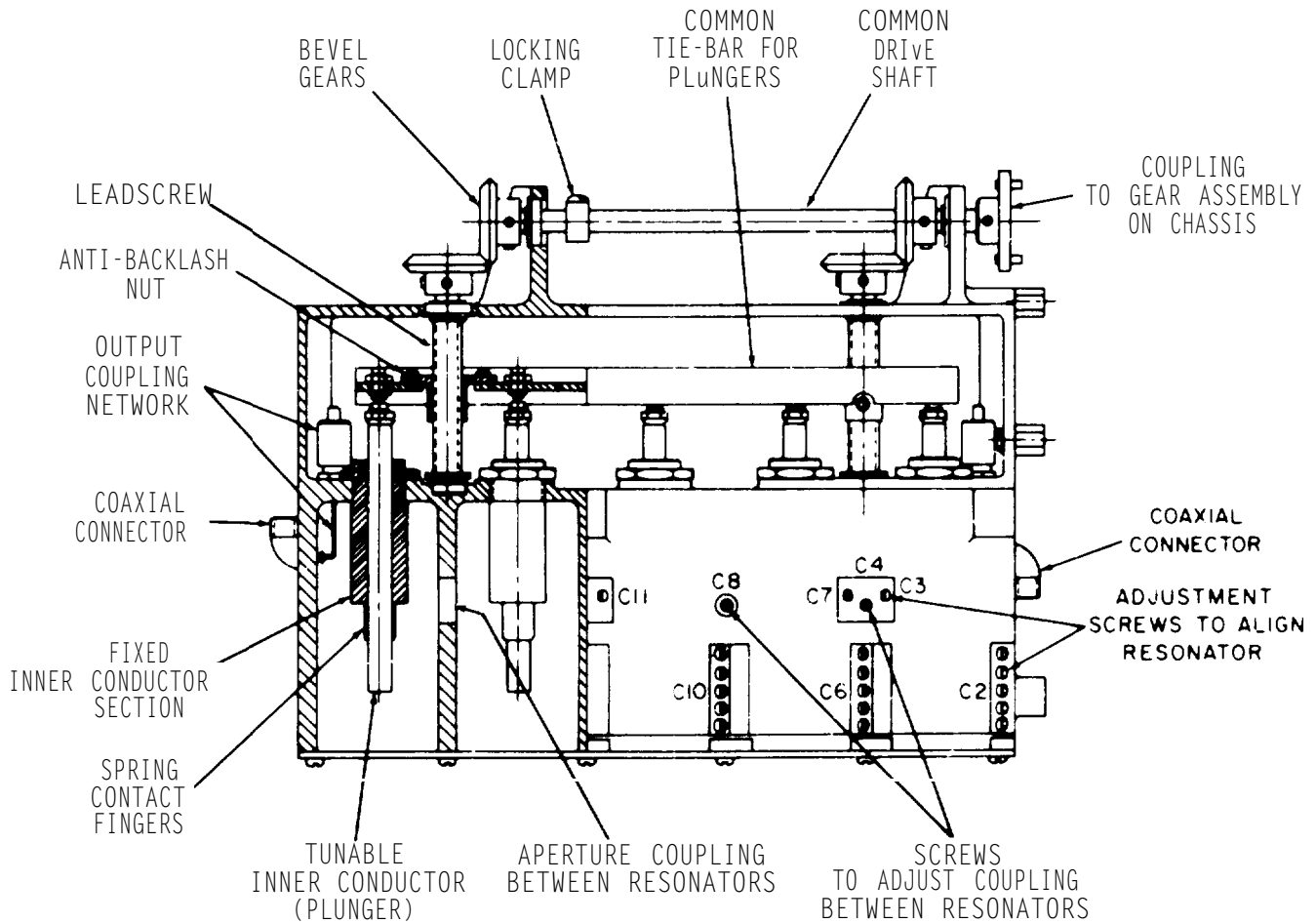
(7) Diode AR1CR1 ensures that the voltage at AR1E7 does not fall below that at AR1E11, preventing premature saturation of rf amplifier 40A2AR2. If the voltage at AR1E7 should fall below 12.5 v, the voltage at AR1E11 begins to reduce accordingly.

(8) Relay AR1K1 is energized by a signal on line 13 from control indicator 40A4 and switches +26 vdc neutral from the 6 db or the 3.5 db line as required. Diodes AR1CR5, AR1CR6 and AR1CR7 provide protection from the transients generated in the solenoid of AR1K1 and the relays of the amplifier monitor in the fixed head.

2-102. Bandpass Filter 40FL1 (Fig. 2-99)

a. General. Bandpass filter 40FL1 is identical to bandpass filters 39FL1 and 39FL2 in the Band IV receiver rf head, and is located in the transmit signal path following coaxial isolator 40A1AT1. It filters the multiplied transmit signal, rejecting spurious outputs (sub-multiples, signals and noise) of the frequency generator and multiplication circuits, before passing the signal to rf amplifier 40AR1.

(1) Bandpass filter 40FL1 consists of five tunable coaxial resonators ganged to a common shaft and tunable over the frequency range of 1350 to 1849.5 MHz by a single control. All five resonators are positioned side by side in a common structure consisting of five-cavity cast-aluminum housing and five plungers connected to a common tie bar. The tie bar is actuated by two parallel spring-loaded leadscrews with antibacklash nuts. Two sets of bevel gears couple the leadscrews to a common



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Figure 2-99. Bandpass Filter 40FL1, 39FL1 or 39FL2, Cross-Sectional View.

drive shaft that connects to the XMTR TUNE control on the front panel via a gear assembly.

(2) Internally, each resonator consists of a cavity and a centrally located hollow conductor section with spring contact fingers. A smaller conductor (plunger) slides through the conductor section and the contact fingers, ensuring good electrical contact and thus tuning the resonator. Coupling between each resonator is achieved by an aperture in which peripheral screws adjust the cross-sectional area.

(3) The electrical input and output connections to bandpass filter 40FL1 are made through rf connectors and an inductive-capacitive network coupling in the end resonators (i.e. first and fifth cavity). Alinement of the resonators is achieved by a series of adjustable screws which protrude through housing walls and into each cavity. The screws act as adjustable capacitors and electrically match the plunger position to the required frequency.

b. Detailed Circuit Analysis (Fig. 2-100). Input signal is received at connector J1 and tea through an inductive loop and capacitor C1 to Z1, a transverse electric and magnetic (TEM) coaxial, quarter-wavelength resonator. The resonator is tuned by varying the length of its inner conductor and is loaded by capacitive adjustment screws C2 and C3. The filtered signal is then fed through an aperture coupling, pretuned by adjustable capacitive screws C4 and C5, to resonant circuit Z2-C6-C7. This signal path is continued through all resonant circuits to Z5, accomplishing the necessary rejection. The signal is then coupled out to connector J2 through an inductive loop and capacitor C20.

2-103. Rf Amplifier 40AR1 (Fig. 2-101)

a. General. Rf amplifier 40AR1 amplifies the final selected transmitter frequency of 1350 to 1849.5 MHz by approximately 20 db before the signal is fed to circulator 40A1HY1. Two grounded-grid triode stages in cascade, and identical in construction, make up the amplifier. Each stage uses a planar triode tube (type 7211, SM-A-794144) which is mounted in a tuned-cathode, coaxial, 3/4 wave resonant cavity and a tuned-plate, coaxial, 1/4 wave resonant cavity. Tuning of cathode and plate resonators is effected simultaneously over the frequency range by mechanically coupled plungers that vary the effective length of the resonant cavities. Cathode tuning plungers are moved by individual leadscrews, while plate tuning plungers are mounted on a common carriage and moved by two leadscrews running parallel to each other. All four leadscrews are interconnected by a chain and sprockets which couple with the front panel XMTR TUNE control through a main chassis gear mechanism. This mech-

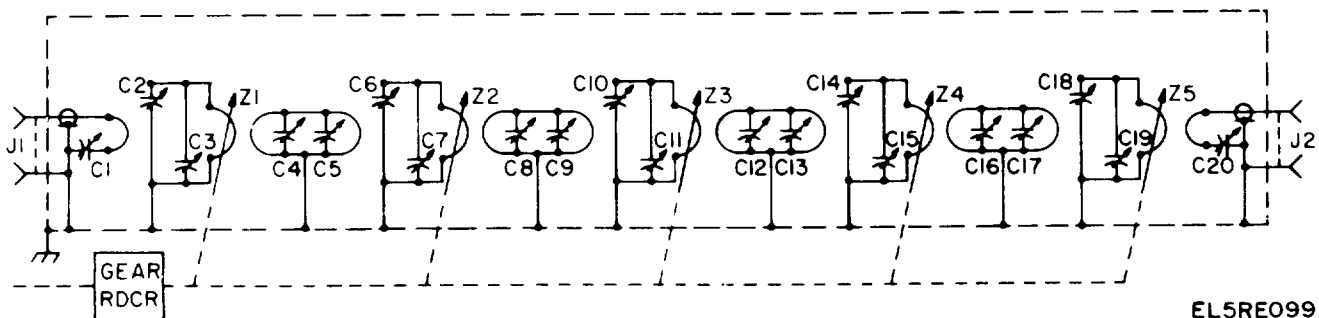
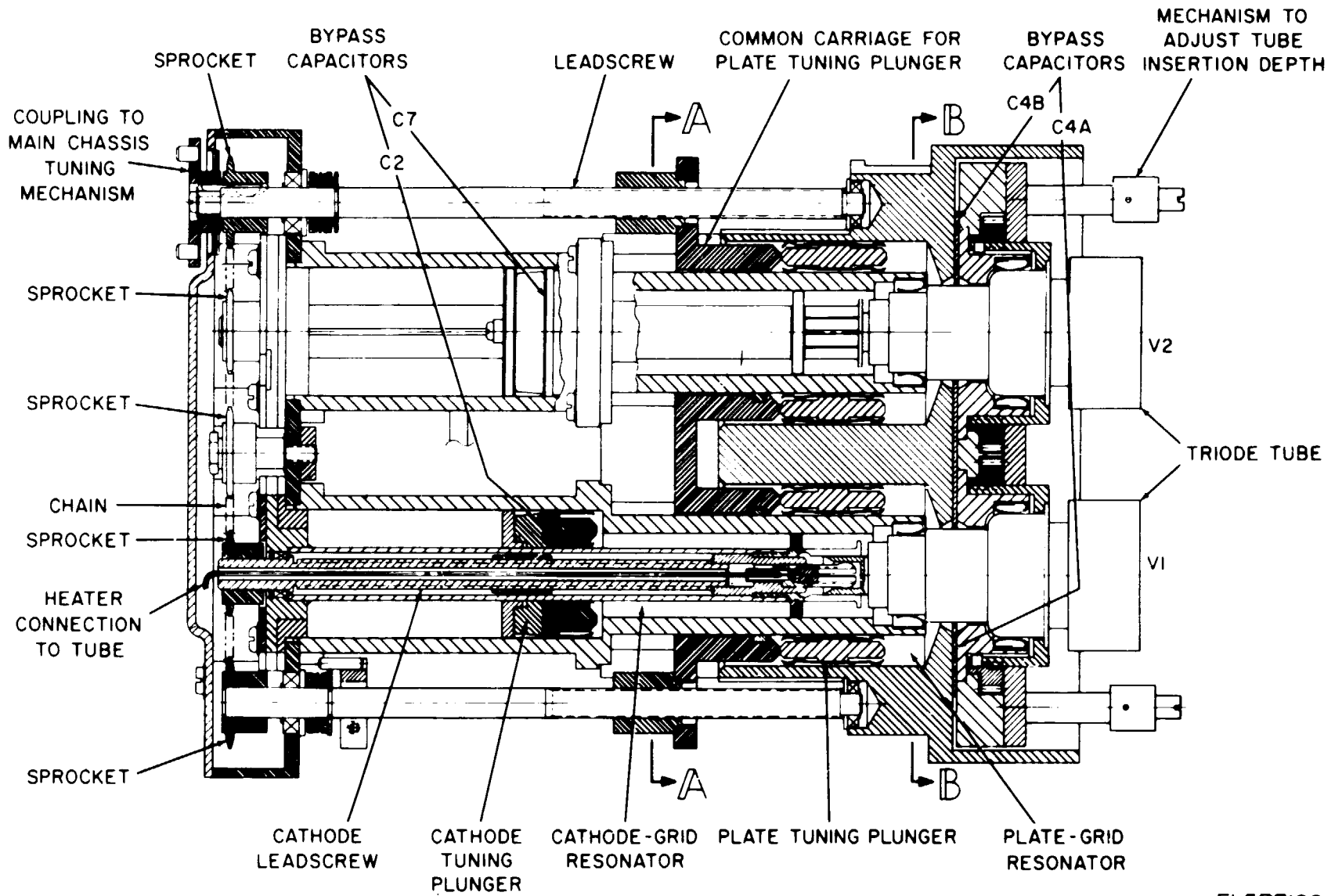


Figure 2-100. Bandpass Filter 40FL1 , 39FL1 or 39FL2, Schematic Diagram.

Figure 2-101. RF Amplifier 40AR1, Cross-Sectional View (Sheet 1).



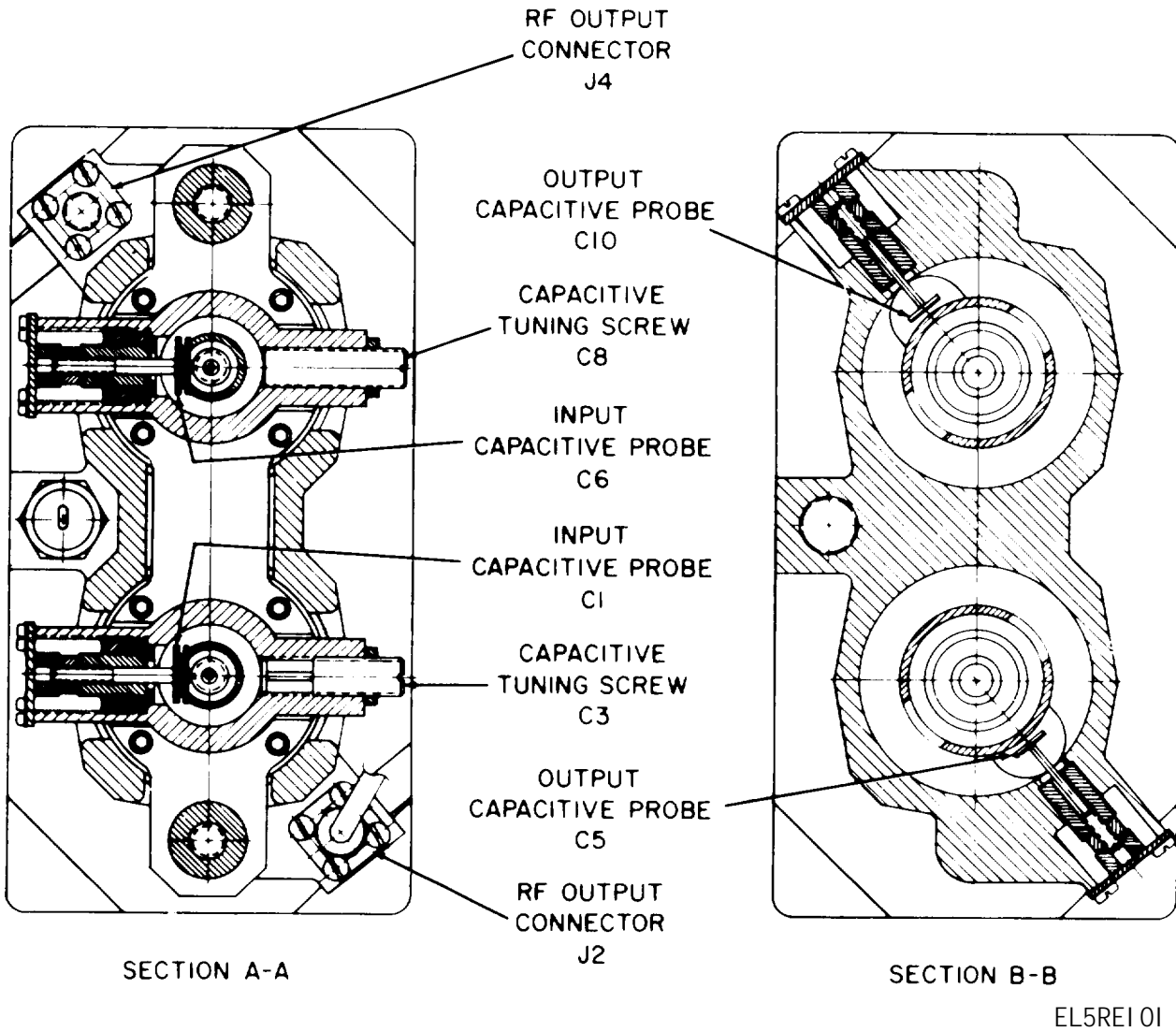


Figure 2-101. RF Amplifier 40AR1, Cross-Sectional View (Sheet 2).

anism incorporates the PWR OUT PEAK control of the fine tuning of 40AR1 . To accommodate geometric tolerances and compensate for tube plate-to-grid capacitance differences, tube insertion depths can be varied by an adjusting mechanism at the side of the tubes (fig. 2-101 (sheet 1)). Input and output coupling to the resonators is effected by capacitive probes which are preadjusted and locked (fig. 2-101 (sheet 2)).

b. Cavity Construction and Tuning Mechanism. Heater connections to the amplifier tubes are made through the hollow cathode leadscrews inside the center conductors of the cathode-grid resonators. Cathode feed (input signal) is supplied through a coaxial connector on the capacitive probe in the first cathode-grid resonator. DC isolation is achieved within the cathode tuning contact assembly. A capacitor integral to the amplifier tube socket decouples the plate supply, while dc power is fed through a high-voltage filter connection to the tube plate. Plate and cathode tuning is accomplished by varying the position of the respective short-circuit tuning plungers, and the short-circuit to the resonator walls is made through sets of flexible silver-plated fingers. The amplified output from the first plate-grid resonator is taken by a capacitive probe to a coaxial connector and fed by a semi-rigid coaxial cable to the input connector and capacitive probe of the second cathode-grid resonator, where amplification is repeated identically.

c. Detailed Circuit Analysis (Fig. 2-102). Driver V1 and the output V2 circuits are identical, Z1 and Z8 are the cathode-grid resonant cavities, and Z7 and Z14 are for the driver and output stages respectively. Capacitance tuning screws C3 and C8 form the shunt capacitance to the grids of V1 and V2, which are at dc ground, and provide impedance matching at the low frequency end of the band. The regulated heater supply to the driver and output stages is fed through filters FL4 and FL2, while the high voltage plate supply to both stages is fed through filter FL1. Bypass capacitors C2, C7, C4A and C4B provide dc isolation. Output signal from bandpass filter 40FL1 flows through input connector J1 and preset capacitive probe C1 to the cathode of driver tube V1. The signal excites cathode resonator Z1, which is connected between the cathode and the grid of V1.

(1) The amplified output signal from the plate of V1 resonates in plate-grid resonator Z7 and is coupled through preset capacitive probe C5 to output connector J2. Driver tube V1 output is fed through coaxial cable W1 to input connector J3 of the output stage and then to capacitive probe C6, where amplification in the V2 circuit is repeated as in the V1 circuit. The final amplified signal is fed through capacitive probe C10 to output connector J4.

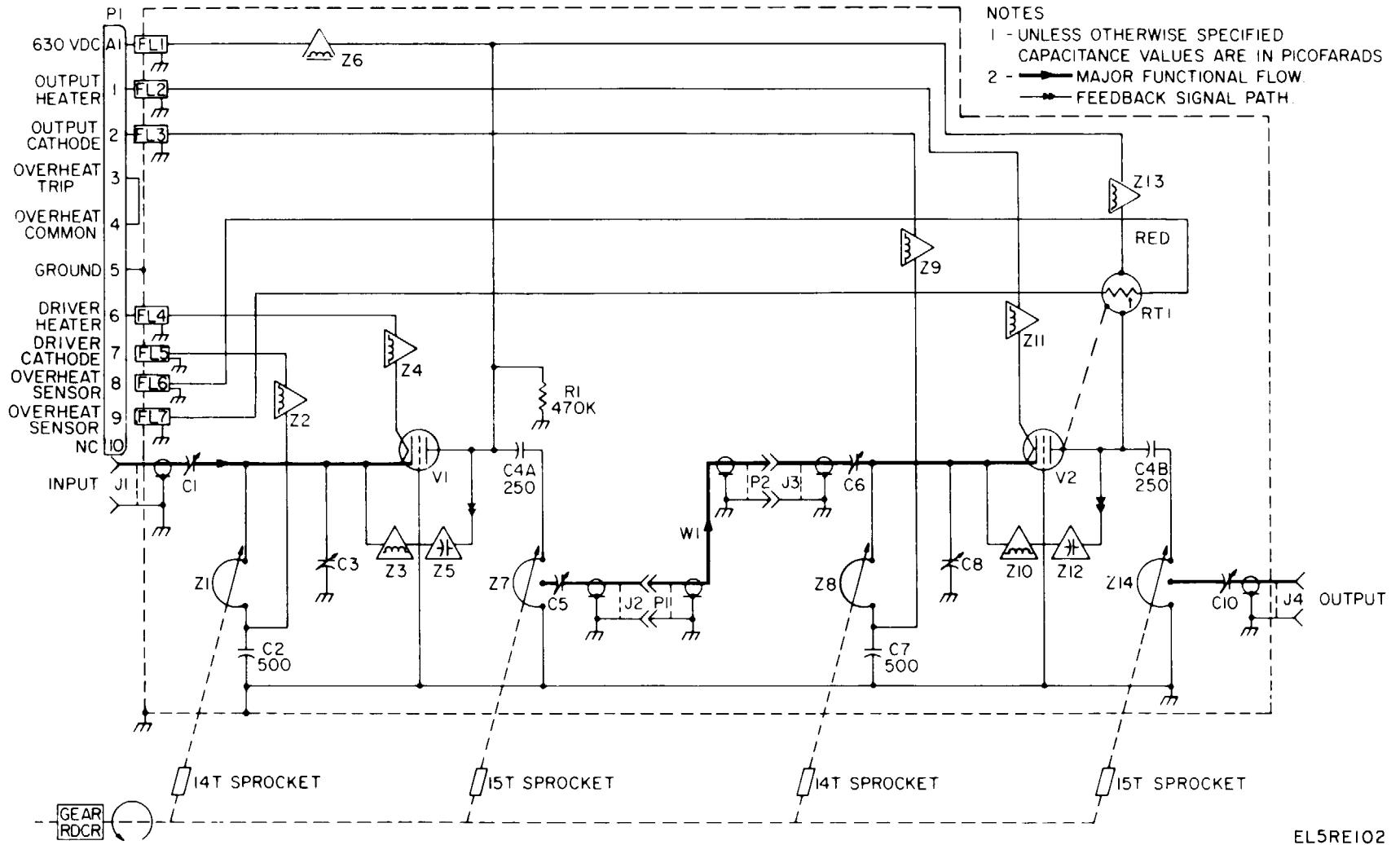
(2) The cathode dc voltage of the output stage is fed back through pin 2 of connector P1, through heater voltage regulator 40A3, to amplifier-frequency multiplier 40A2. Output cathode bias changes are used to produce the alv voltage which controls the output of the amplifier-frequency multiplier and hence the input to the power amplifier. Cathode current is regulated by a constant current source within transmitter power supply 5TR1PS1, which also supplies 630 vdc (at approximately 180 milliamperes) for the plate supply.

#### 2-104. Voltage Regulator Assembly 40A3

Voltage regulator assembly 40A3 is identical to voltage regulator assembly 37/38AR1A1A1 except for resistor values R1 through R4, R12 and R20 (fig. 2-83). General and detailed circuit descriptions applicable to voltage regulator 40A3 are given in paragraph 2-61.



Figure 2-102. RF Amplifier 40AR1, Schematic Diagram.



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2-105. Circulator 40A1HY1 and Electrical Dummy Load 40A1A2

Circulator 40A1HY1 is a 3-port ferrite device with permanent magnets which permit the transmission of outgoing signals from port J3 to port J1 but prevent reflected signals from reaching port J3. The rf output from power amplifier 40AR1 is fed to port J3 of the circulator (F0-4-6) while the reflected signal at port J1 is directed to port J2 and terminated in electrical dummy load 40A1A2. The dummy load is low vswr resistive network capable of continuously dissipating up to 35 watts at 1850 MHz .

2-106. Rf Power Monitor 40A1A1

The power monitor is connected between port J1 of circulator 40A1HY1 and the PWR OUT connector. It is similar to power monitor 37AR1A2. Refer to paragraph 2-63 for a functional description.

2-107. Control-Indicators 40A4 and 39A4

a. General. Control-indicator 40A4 (the transmitter channel selector, F0-4-76) and control indicator 30A4 (the receiver channel selector, F0-4-73) are similar in function and construction to control-indicator 6A4 (fig. 2-49). Each channel selector provides 14 control lines (0 through 13) to the frequency synthesizer in the transmitter and receiver respectively. To select the required synthesizer frequency, control lines 0 to 12 are switched on or off in a binary pattern as shown in F0-4-72. At the changeover point between high band and low band (transmitter channels 2959-2960, receiver channels 2899-2900), line 13 is also switched on or off as required to change the synthesizer output frequency. The switching modules are operated by a set of reflective cams and followers which reflect the coding patterns shown in F0-4-72.

b. Description of Operation (Fig. 2-1031. The control-indicator consists of an optical module and a logic module (command signal decoder). Reflective and nonreflective surfaces on the rotating cams allow the optical module to generate an n-bit binary code which presets the required stages of the programmed counter in synthesizer 5TR1A2 or 1RE1A2. The front panel channel indicators consist of a series of numbered wheels geared to the rotating cams and to a front panel control knob. Transmitter channel frequency indicator 40A1DS1 displays the channel rather than the frequency selected. Use the following formulas to translate a selected channel into a frequency and vice versa:

$$\text{Transmitter frequency} = (\text{Tx chan} \div 2) + 200 \text{ MHz}$$

$$\text{Transmitter channel} = (\text{Tx freq} - 200 \text{ MHz}) \times 2$$

(1) Coding on the receiver channel selector is arranged to produce a local oscillator frequency 30 MHz higher than the frequency of the channel indicated in the display to ensure that the intermediate frequency is correct.

(2) The command signal decoder unit is an encapsulated logic circuit designed to sense channel coding on the input lines (1 through 12) and to provide control logic to control lines 0 through 13. Inputs 1 through 11 are programmed by optical module outputs E1 through E11 respectively, while input 12 is hard-wired to ground.

(3) Up to and including channel 2959 (TX)/2899 (RX), the logic level on output control lines 1 through 12 follows the logic level on the corresponding inputs (1



through 12) of the decoder. For example, the logic level on input 1 appears on control line 1, the level on input 2 appears on control line 2, and so on through input 12 (which appears on control line 12). However, control lines 0 and 13 are commanded to a high level.

(4) At and above channel 2960 (Tx)/2900 (Rx), the decoder module switches the inputs so that input 12 appears at control line 11, input 11 appears at control line 10, and so on through input 1 (which appears at control line 0). Control line 12 is commanded to a high level and control 13 to a low level.

Section XI. AMPLIFIER-CONVERTER AM-4319/GRC-103(V) - BAND  
IV RECEIVER RF HEAD (UNIT 39)

2-108. Functional Block Diagram Analysis of Amplifier-Converter  
AM-4319/GRC-103(V) (Fig. 2-104)

a. Amplifier-Converter AM-4319/GRC-103(V). the Band IV receiver rf head, incorporates a duplexing system which enables the radio set to use a single antenna for both transmission and reception, as well as circuits which convert the incoming signal into a 30 MHz intermediate frequency.

b. The receiver rf head duplexer circuit (consisting of 39FL3, 39A1HY1, 39A1A1 and 39FL1) provides the necessary isolation between the transmit and receive signals. Transmit signal (15 watts) at the PWR OUT connector of the transmitter rf head is fed through an external rf coaxial cable, through the FROM XMTR connector on the front panel of the receiver rf head, to bandpass filter 39FL3. This tunable transmit filter is manually tuned to the transmit channel by the XMTR DUPL control, and provides additional filtering of the transmit signal while presenting a high attenuation to the received frequency. From filter 39FL3, the transmit signal is directed to the ANT connector (through circulator 39A1HY1 and rf power monitor 39A1A1) and to the antenna system (through an rf coaxial cable). Forward and reflected power to and from the antenna system is sampled by power monitor 39A1A1, and rectified. Resultant dc voltages are used for XMTR DUPL and REFL PWR metering.

c. The receive circuits of the receiver rf head accept fm signals of 1350 to 1849.5 MHz and convert them to a 30 MHz intermediate frequency which is then amplified and demodulated in the receiver fixed head.

(1) Signals from the antenna are applied to the ANT. connector by the lead-in cable and are fed through power monitor 39A1A1 and circulator 39A1HY1 to bandpass filter 39FL1. The filter selects the required signal and reduces all others to a level which will not cause degradation of the selected signal. (Filter 39FL1 is manually tuned to the receive channel by the RCVR SIG control. )

(2) The receive signal is then fed to frequency converter assembly 39A2. Here it is amplified to a suitable level to mask mixer noise contributions and is mixed with the local oscillator signal to produce an intermediate frequency of 30 MHz. Frequency converter 39A2 also protects the receiver front end from possible damage by inadvertent tuning of the transmit frequency to the receive frequency. In the event of high signal entry, it also triggers the HIGH SIGNAL alarm in the receiver fixed head.

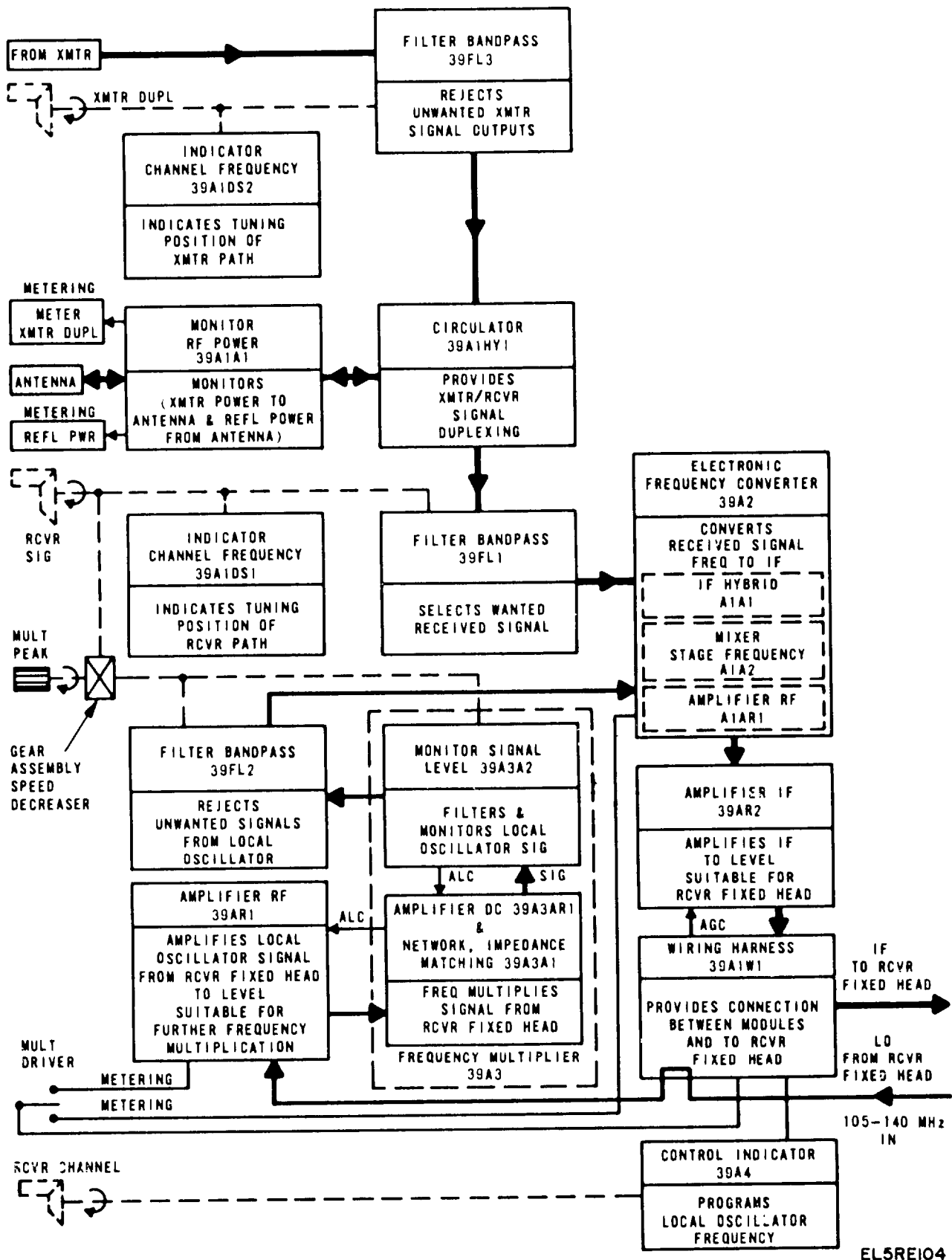


Figure 2-104. Band IV Receiver RF Head, AM-4319/GRC-103(V), Block Diagram.

(3) After leaving the frequency converter, the 30 MHz if signal is fed to intermediate frequency amplifier 39AR2, which is automatically gain controlled to amplify the if signal as required by the fixed head. This if signal is then passed to the receiver fixed head through wiring harness 39A1W1 interconnections.

(4) Channel frequency indicators 39A1DS2 and 39A1DS1 indicate the transmitter and receiver frequencies being tuned.

d. The fundamental local oscillator frequency is generated in the receiver fixed head, in the range of 105 to 140 MHz, and is fed to the receiver rf head wiring harness 39A1W1.

(1) Control-indicator 39A4, which is operated by a front panel RCVR CHANNEL tuning control, programs this basic signal and sends codes to the electrical frequency synthesizer in the receiver fixed head. The codes permit variation of the frequency multiplied local oscillator signal in 0.5 MHz increments. The selected local oscillator signal is then passed to rf amplifier 39AR1, which amplifies the signal to a level suitable for further frequency multiplication.

(2) Frequency multiplier 39A3 receives the amplified signal and multiplies it by 12 to provide final local oscillator frequencies of 1380 to 1679.5 MHz and by 16 for frequencies of 1680 to 1879.5 MHz.

(3) A tunable cavity resonator in the frequency multiplier selects the local oscillator frequency. The multiplied signal is then fed to five-cavity bandpass filter 39FL2, which reflects the unwanted signals from the local oscillator chain.

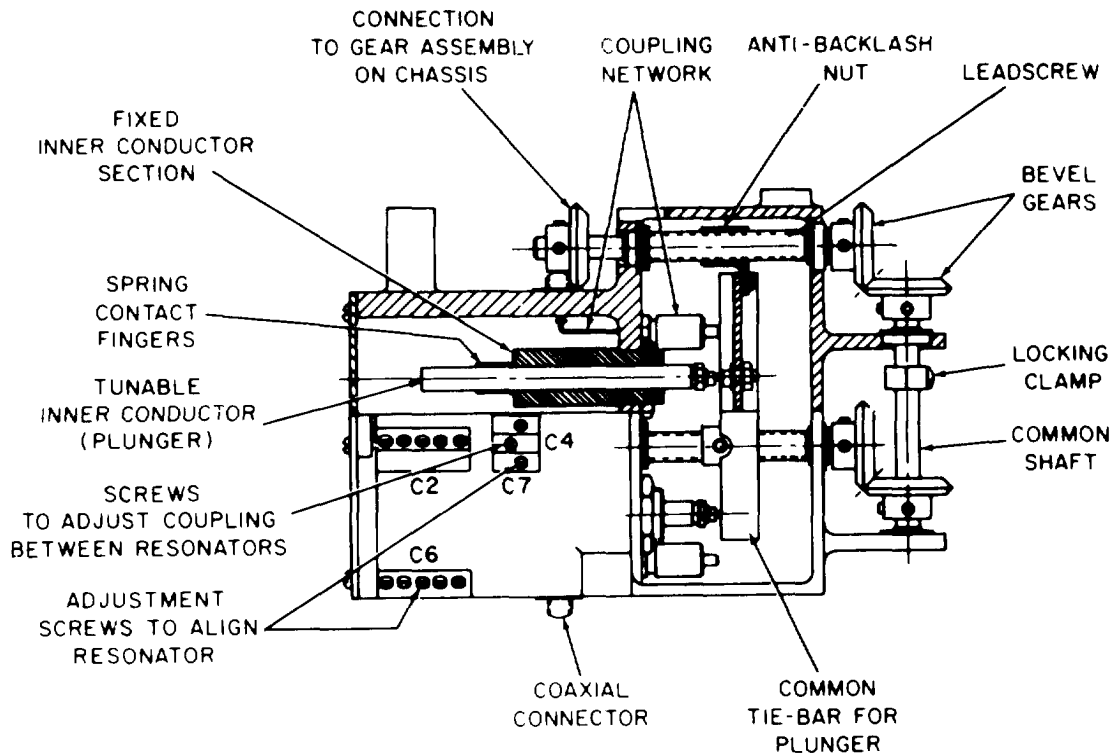
e. Mechanically, frequency multiplier 39A3 is ganged to bandpass filter 39FL2 and then, through a gear assembly speed decriaser, to the RCVR SIG control, which also drives bandpass filter 39FL1. The RCVR SIG control adjusts frequency multiplier 39A3 and bandpass filter 39FL2 to a frequency near the required tuning point, approximately 30 MHz above the frequency of the receive signal selected by bandpass filter 39FL1. Then, the MULT PEAK control fine-tunes frequency multiplier 39A3 and bandpass filter 39FL2 to the optimum tuning point. Ganging of the RCVR SIG and MULT PEAK controls is such that the output frequency of 39A3 is always 30 MHz above the signal received at 39FL1. The local oscillator signal is then fed from bandpass filter 39FL2 to the mixer stage of electronic frequency converter 39A2.

f. Operating voltages at +12 vdc and -12 vdc regulated and 26 vdc unregulated for the receiver rf head circuits are supplied by power supply 1RE1PS1 in the receiver fixed head. An overall schematic diagram of the Band IV receiver rf head is shown in FO-4-73 and an interconnecting diagram is shown in FO-4-74.

## 2-109. Bandpass Filter 39FL3 (Fig. 2-105)

a. General. Bandpass filter 39FL3 is located in the transmit signal path and provides final filtering of the signal before it is fed to the antenna through circulator 39A1HY1 and rf power monitor 39A1A1. The major function of the filter is to reject unwanted transmit signal outputs and noise produced in rf amplifier 40AR1 to a level that will cause minimal degradation of receiver performance under conditions of narrow receive and transmit channel spacing.

(1) Bandpass filter 39FL3 consists of two tunable coaxial resonators ganged to a common shaft and tunable from 1350 to 1849.5 MHz by the XMTR DUPL control. Both cavities are located in common housing. A common tie bar that is actuated by two



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Figure 2-105. Bandpass Filter 39FL3, Resonator Cavity Construction.

parallel spring-loaded leadscrews with anti-backlash nuts connects the plunger of each. The leadscrews are coupled by a common shaft and two sets of bevel gears, with one leadscrew connected to the XMTR DUPL control on the front panel through a gear assembly. Coupling between resonators is achieved by an aperture in which screws around the periphery adjust the cross-sectional area.

(2) Input and output connections to the bandpass filter are made through coaxial connectors and an inductive/capacitive network in each of the resonators. Alinement of the resonators is achieved by adjustable screws which protrude through housing walls and into each cavity. The screws act as adjustable capacitors, and electrically match the plunger position to the required frequency.

b. Detailed Circuit Analysis (Fig. 2-106). The input signal from transmitter rf head is received at connector J1 and fed through an inductive loop and capacitor C1 to Z1, a TEM-coaxial, quarter-wavelength resonator. Resonator Z1 is tuned by varying the length of its inner conductor and is loaded by capacitive adjustment screws C2 and C3. Filtered signal is then fed to the following resonant circuit (Z2, C6, C7) through an aperture coupling pretuned by adjustable capacitive screws C4 and C5, thereby accomplishing the necessary rejection. The signal is then coupled out through an inductive loop and capacitor C8 to connector J2.

#### 2-109. Circulator 39A1HYI

A 3-port ferrite device with permanent magnets, circulator 39A1HY1 is identical to circulator 40A1HY1 (para 2-104). However, in the receiver rf head, it performs the

duplexing function of routing the transmit signal to the antenna and of routing the receive signal from the same antenna to the receive circuits. The transmit signal arrives at the FROM XMTR connector and passes to port J3 through bandpass filter 39FL3. It is directed through the circulator to port J1, through power monitor 39A-1A1, and on to the ANT. connector. The receive signal from the ANT. connector arrives at port J1 of the circulator power monitor through 39A1A1, is directed through the circulator to port J2, and then through bandpass filter 39FL1 and into frequency converter 39A2.

2-111. Rf Power Monitor 39A1A1

Rf power monitor 39A1A1 is located in the antenna line, between circulator 39A1HY1 and the ANT. connector on the front panel of the receiver rf head. The unit is similar to rf power monitor 33A3 or 34A3. Refer to paragraph 2-67 for a functional description.

2-112. Control-Indicator 39A4

This unit is similar to control-indicator 40A4. Refer to paragraph 2-106 for a functional description.

2-113. Bandpass Filters 39FL1 and 39FL2

a. General. Bandpass filters 39FL1 and 39FL2 are identical and interchangeable within the receiver rf head (fig. 2-99). Filter 39FL1, located in the receive signal path between circulator 39A1HY1 and frequency converter 39A2, provides preselective filtering of the receive signal by sufficiently rejecting transmitter power leakage and transmitter (or external) spurious signals. Filter 39FL2, in the local oscillator input path of frequency converter 39A2, provides filtering of the local oscillator frequency that would otherwise generate spurious responses within the receiver.

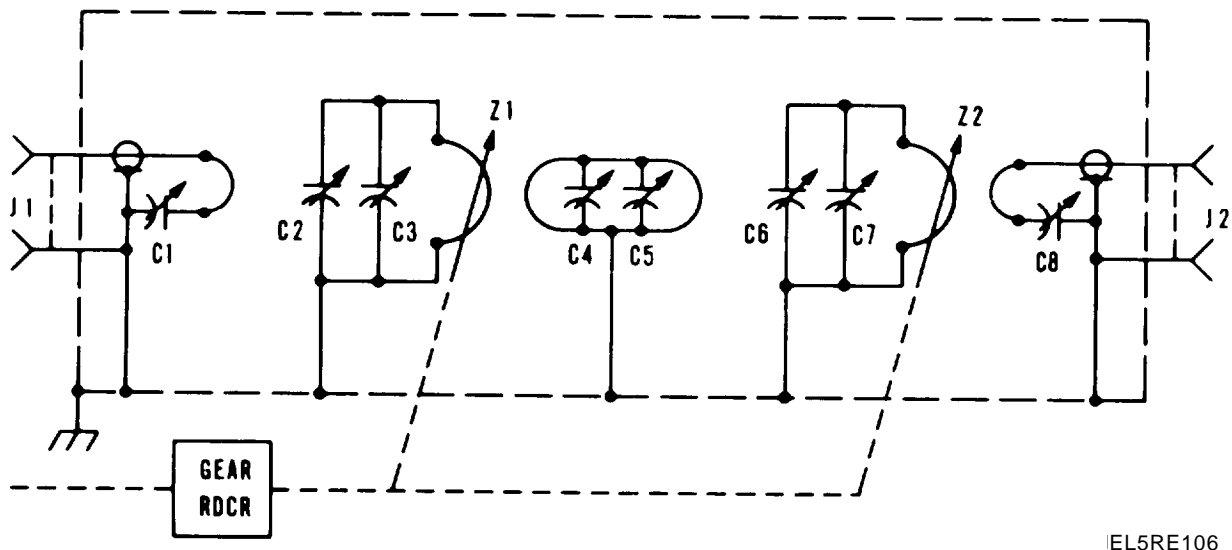


Figure 2-106. Bandpass Filter 39FL3, Schematic Diagram.



(1) Each bandpass filter consists of five tunable coaxial resonators ganged to a common shaft and tunable over the frequency range by a single control. All five resonators are positioned side by side within a common structure consisting of a five-cavity, cast-aluminum housing and five plungers connected to a common tie bar. The tie bar is motivated by two parallel spring-loaded leadscrews with anti-backlash nuts. Two sets of bevel gears couple the leadscrews to a common drive shaft that connects to controls on the front panel through a gear assembly. Filter 39FL1 is connected to the RCVR SIG control, while filter 39FL2 is connected to the RCVR SIG and the MULT PEAK controls.

(2) Internally, each resonator consists of a cavity and a centrally located hollow conductor section with spring contact fingers. A small conductor (plunger) slides through the conductor section and contact fingers, making good electrical contact, and tunes the resonator. Coupling between each resonator is achieved by an aperture with screws around the periphery to adjust the cross-sectional area.

(3) Electrical input and output connections to the bandpass filters are made through coaxial connectors and an inductive/capacitive network coupling in each of the end resonators (i.e. first and fifth cavities). Alinement of the resonators is achieved by a series of adjustable screws which protrude through housing walls and into each cavity. These screws act as adjustable capacitors and electrically match the plunger position to the required frequency.

b. Detailed Circuit Analysis (Fig. 2-100). An input signal is received at connector J1 and fed through an inductive loop and capacitor C1 to Z1, a TEM-coaxial, quarter-wavelength resonator. Resonator Z1 is tuned by varying the length of its inner conductor and is loaded by capacitive adjustment screws C2 and C3. The filtered signal is then fed to the following resonant circuit (Z2, C6, C7), through an aperture coupling pretuned by adjustable capacitive screws C4 and C5. This signal path is continued through all resonant circuits to Z5, accomplishing the necessary rejection. The signal is then coupled out to connector J2 through an inductive loop and capacitor C8.

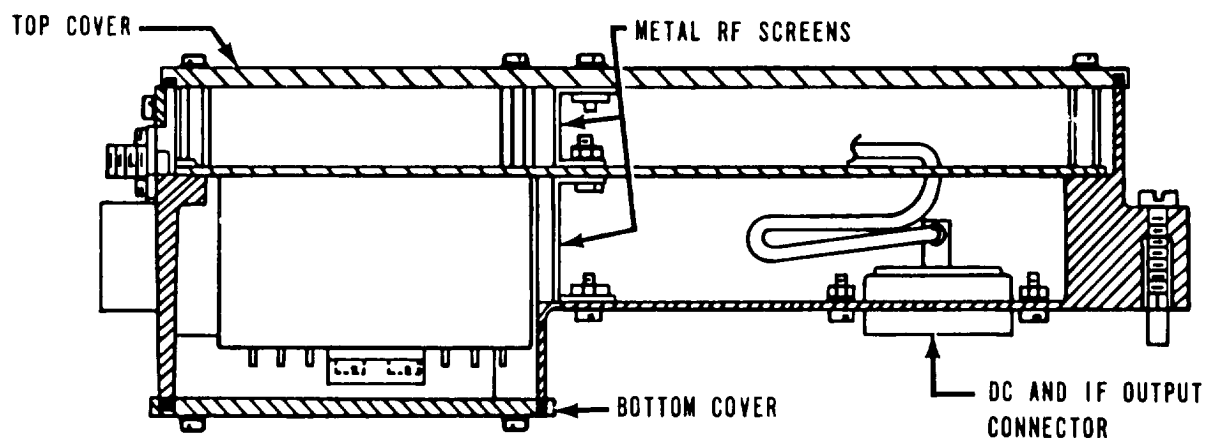
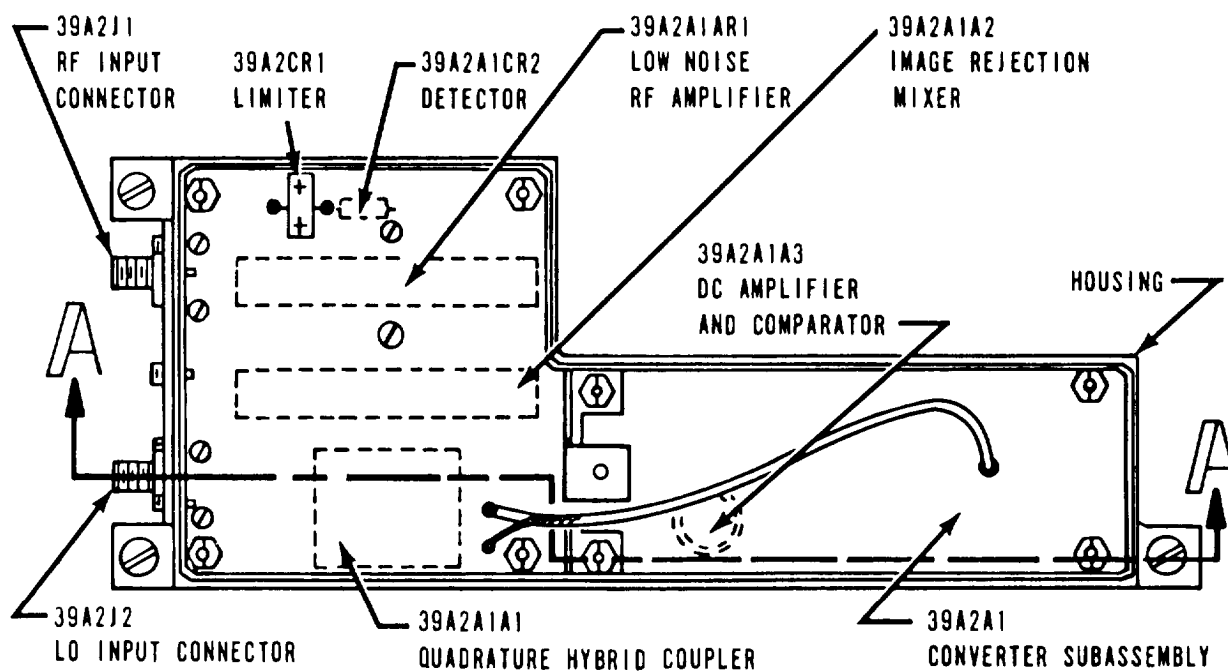
2-114. Electronic Frequency Converter 39A2 (Fig. 2-1071)

a. General. Located in the receive signal path following bandpass filter 39FL1, frequency converter 39A2 amplifies the rf signal of 1350 to 1849.5 MHz, mixes it with the local oscillator signal of 1380 to 1879.5 MHz, and converts it to the intermediate frequency of 30 MHz, which is then fed to IF amplifier 39AR2. The local oscillator signal is supplied by frequency multiplier 39A3 and received through bandpass filter 39FL2.

(1) Frequency converter 39A2 consists of a detector and limiter circuit, a dc amplifier and comparator, a low-noise rf amplifier, and an image-frequency rejection mixer and associated hybrid coupler. The mixer is a microwave integrated circuit packaged in a hermetically sealed enclosure, while the rf amplifier is assembled on a printed circuit board and packaged in an enclosure similar to that of the mixer. Limiter and detector circuitry, as well as the dc amplifier and comparator, are packaged on a printed circuit board.

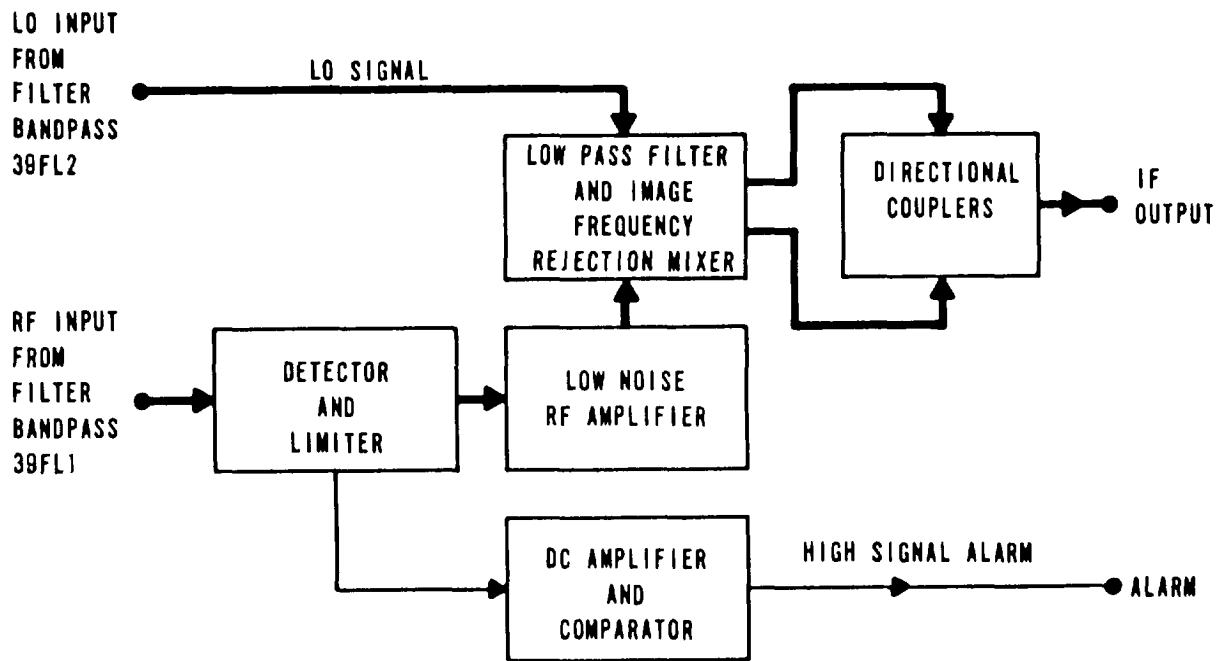
(2) All of the electronic components and circuitry are mounted on the printed circuit board, including the two rf hybrid microcircuits, a dc connector, two rf connectors, and two sheet-metal rf shields. The whole electronic assembly is fitted in an L-shaped, cast-aluminum housing with top and bottom sheet-metal covers.

b. Block Diagram Analysis (Fig. 2-108). The signal entering the rf input connector passes through a detector and protection circuit (limiter), which self-energizes at signals exceeding +15 dBm and forms a low impedance path to ground, thus protecting the hybrid amplifier from these high signals. Simultaneously, the limiter provides a dc voltage that is fed to a dc amplifier and comparator circuit which in turn operates a high signal alarm in the receiver fixed head. The signal is also passed to a high-gain, low-noise amplifier where the rf gain masks noise from the mixer stage. The amplified signal is then fed through a low-pass filter, to ensure rejection of unwanted signals that may not have been rejected by bandpass filter 39FL1. Signal from the low-pass filter, together with the incoming local oscillator



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Figure 2-107. Electronic Frequency Converter 39A2, Cross-Sectional View.  
2-220



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Figure 2-108. Electronic Frequency Converter 39A2, Block Diagram.

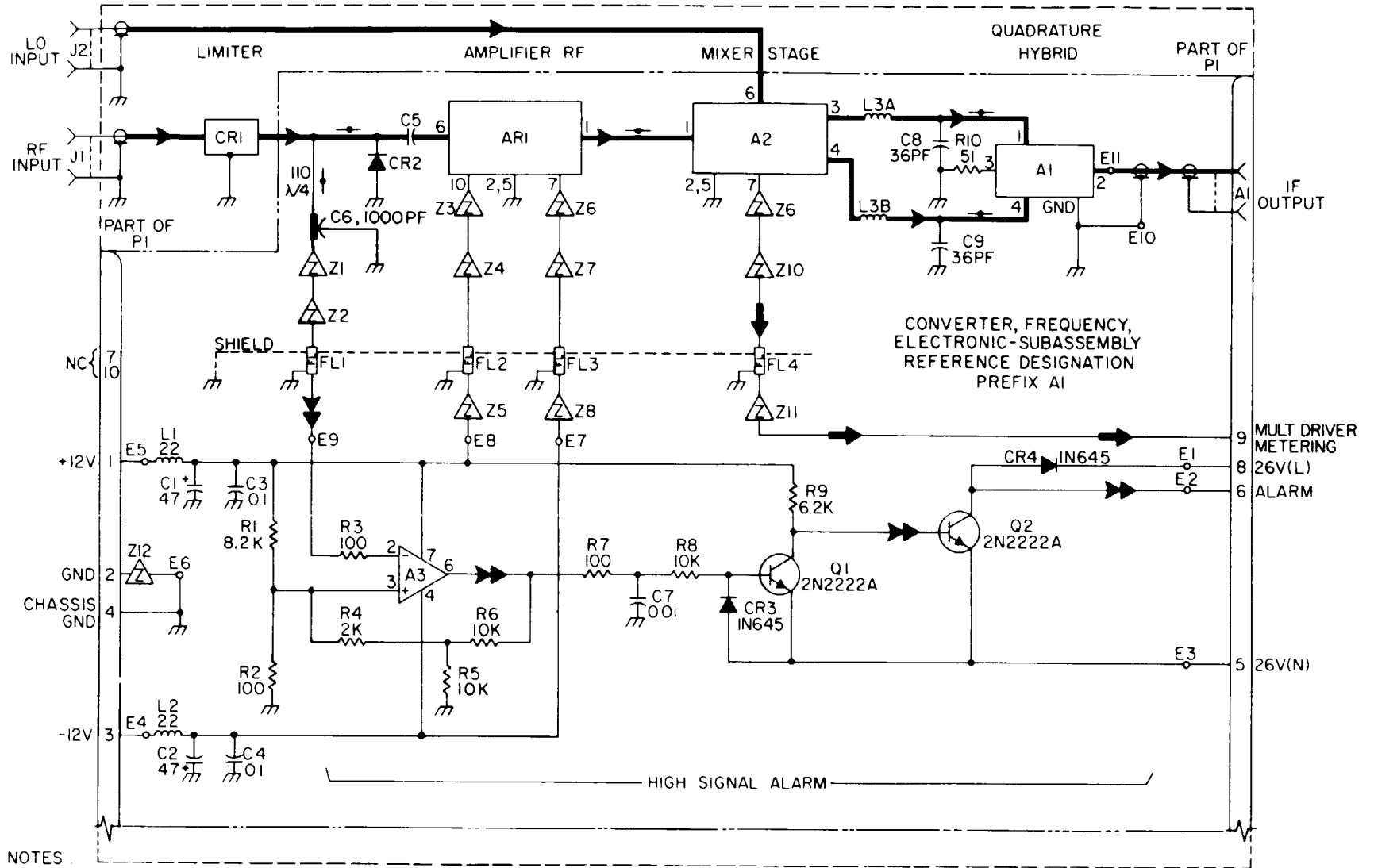
signal, is fed to an image-frequency rejection mixer consisting of two balanced mixers with signals applied and combined in quadrature by directional couplers. The mixer stage suppresses image-frequency noise from the rf amplifier and converts the received signal to an intermediate frequency of 30 MHz which is then fed through the output connector to the receiver fixed head.

c. Detailed Circuit Analysis (Fig. 2-109). The incoming rf signal passes through PIN diode CR1 and is applied to pin 6 of two-stage rf amplifier AR1 (through dc blocking capacitor C5), where it is amplified by approximately 30 db. The amplified signal at pin 1 of mixer AZ is mixed with the incoming local oscillator signal from connector J2, to produce the 30 MHz intermediate frequency that appears in quadrature phase at mixer output pins 3 and 4. The applied local oscillator signal level is monitored and rectified within mixer AZ, and the resultant dc signal is fed through pin 7 for application as MULT DRIVER metering.

(1) The signals at pins 3 and 4 of mixer A2 are passed through matching networks L3A-C8 and L3B-C9 and applied to input pins 1 and 4 of 3 db quadrature coupler A1. Here, the converted receive signals are combined to appear on pin 2, and the converted image signals are combined to appear on pin 3 for dissipation in R10. The 30 MHz if signal from pin 2 is fed to output pin A1 of connector P1.

(2) When incoming signals exceed +10 dbm, they are rectified by CR2. Rectification produces a dc voltage which biases PIN diode CR1 into conduction and presents a short circuit to the high signals, thereby protecting the input stages of AR1 from overload and burnout. Simultaneously, the dc voltage is fed through rf decoupling elements C6, Z1, Z2, FL1, and limiting resistor R3, for application to dc amplifier

Figure 2-109. Electronic Frequency Converter 39A2, Schematic Diagram.



NOTES

| SYMBOL | DESIGNATION, UNIT                                |
|--------|--|
| R      | NONE (OHM)<br>K (KILOHM)<br>M (MEGOHM)           |
| C      | PF (PICOFARAD)<br>NONE (MICROFARAD)              |
| L      | NONE (MICROHENRY)<br>m (MILLIHENRY)<br>H (HENRY) |

- 2- ➔ MAJOR FUNCTIONAL FLOW.
- ➔ DC METERING FLOW
- ➔➔ INDICATOR OR ALARM CIRCUIT.

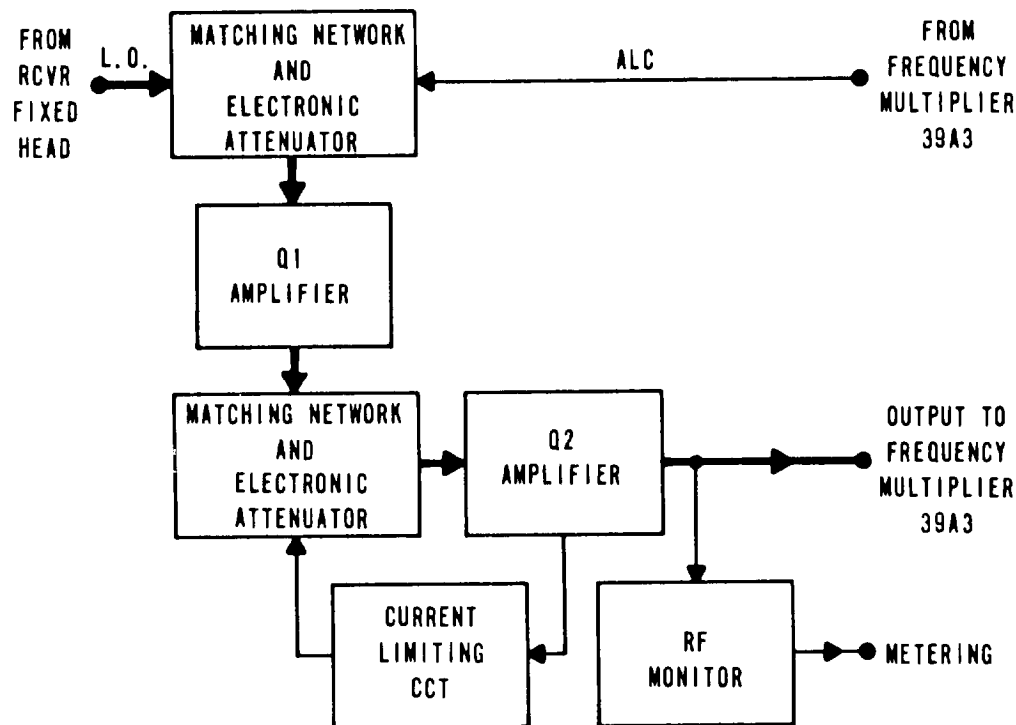
and comparator A3. Resistors R1 and R2 provide the reference bias for A3, while R4, R5 and R6 provide feedback that sets the amplifier loop gain. Decoupling of the +12 vdc and -12 vdc supply lines is provided by L1-C1-C3 and L2-C2-C4, respectively.

(3) The output signal from A3 is fed to the base of Q1 through current limiting resistor R8 and decoupling components R7 and C7. Reverse biasing of the base-emitter junction is prevented by CR3. When the voltage at pin 2 of A3 is more positive than at pin 3, the output from A3 turns off transistor Q1 and allows current from the +12 vdc line through R9 to force transistor Q2 into heavy conduction. This provides the necessary dc ground to operate the relay coil of the alarm unit in the receiver fixed head. Diode CR4 suppresses transients when the alarm relay solenoid operates.

2-115. Rf Amplifier 39AR1

a. General. Rf amplifier 39AR1 is situated in the local oscillator path of the receiver and amplifies local oscillator signal from the receiver fixed head to a level suitable for further frequency multiplication by frequency multiplier 39A3. Amplifier 39AR1 consists of a single printed circuit board assembly mounted on a simple cast-aluminum housing with a removable sheet-metal cover. Access holes are provided on the sides of the housing for adjustment of components during alinement of the unit.

b. Block Diagram Analysis (Fig. 2-110). Amplifier 39AR1 consists basically of a two-stage amplifier with a combination of reflective and dissipative matching net-



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Figure 2-110. RF Amplifier 39AR1, Block Diagram.

works to ensure gain flatness and stability. The input stage is operated in class A while the output stage is operated in class B.

(1) Incoming local oscillator signal of 105 to 140 MHz is fed through an input matching network, which includes a PIN diode attenuator. The diode is used for level control purposes and is operated by an alc signal from frequency multiplier 39A3. The signal is then applied to the base of Q1, where it is amplified and passed through an interstage matching network to Q2 for further amplification to the required output.

(2) A feedback circuit from the emitter bias circuit of Q2 to a PIN diode attenuator in the interstage network limits current consumption of the output under high drive or load mismatch. Sampling of the rf output voltage and metering are provided by a peak-detecting rf monitor circuit.

c. Detailed Circuit Analysis (Fig. 2-110). Input signal of 105 to 140 MHz is fed through pin A2 of connector P1 to input matching network circuits C1-L1, C5-L3 and C9-L5. Fine adjustment of the matching network is provided by variable capacitors C2, C4 and C7, while R4 is used to stabilize the input matching network. PIN diode CR1 shunts the input signal through C8 to ground when biased into conduction by an alc signal through pin 5 of connector P1. Resistors R2 and R3 provide the reference bias for diode CR1, while R1, C3, C6 and L4 form decoupling elements.

(1) The first amplifier stage, Q1, is a medium power rf transistor operating in class A. Base biasing is provided by R5 and R6, decoupling by L6, C11 and C12, and emitter biasing by R7 and C14. Inductor L7 tunes with the output capacitance of Q1 to form the first element of the interstage coupling network. Coupling components C16, C20 and L8 match the output of Q1 to the base of Q2, with C17 providing fine adjustment. The second stage amplifier, Q2, a high power transistor operating in class B for high efficiency, further amplifies the signal to approximately 30 dbm (1 watt). Resistors R10, R11 and R12 reduce the bias offset on the base of Q2 to ensure class B operation, while L9, C21, C24 and C25 provide decoupling.

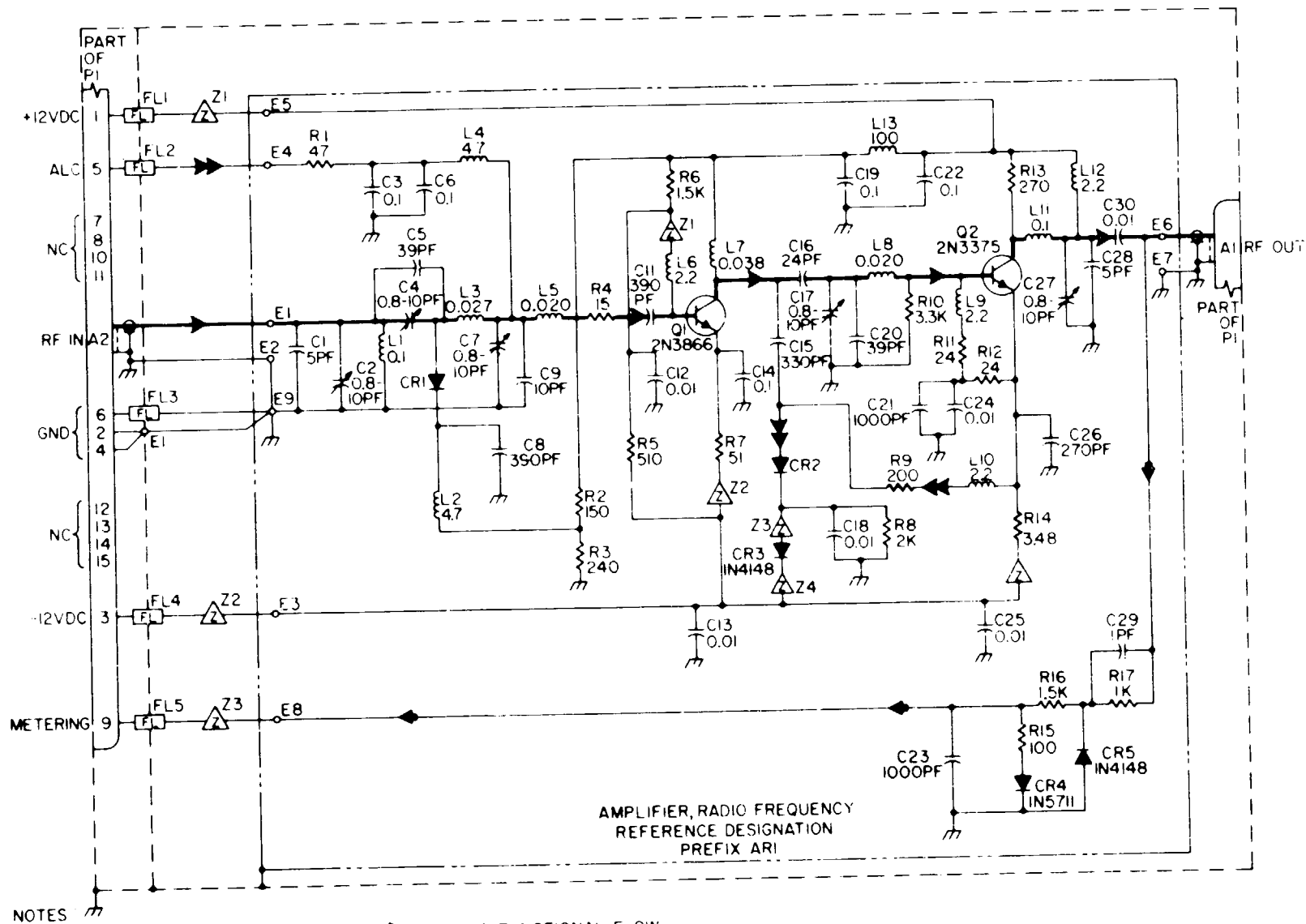
(2) The output of Q2 is matched at the 50 ohm load through L11 and C28, with C27 providing fine adjustment. Indicator L12 supplies the +12 vdc bias to the collector of Q2, while C30 provides a dc block to the output connector and R13 ensures rf stability under mismatch load conditions. Excessive current consumption by the output stage under high drive conditions is prevented by network L10-R9-C18-CR2. PIN diode CR2 acts as an electronic attenuator to shunt the interstage signal to ground when biased into conduction by the potential developed across R14. DC blocking is provided by C15, reverse biasing to PIN diode CR2 by R8 and CR3, and supply line decoupling by L13, C19, C22, C13 and C25.

(3) The rf output voltage is sampled through R17 and C29, and then rectified by CR5, to provide a dc metering signal. Excessive buildup of metering voltage, which may occur during tuning, is limited by R15, R16 and CR4 (thus preventing full scale deflection on the front panel meter), while C23 decouples the metering line. All dc input and outputs pass through rf interference filters FL1 through FL5.

## 2-116. Frequency Multiplier 39A3 (Fig. 2-112)

a. General. Frequency multiplier 39A3 is located in the local oscillator signal path of the receiver and multiplies the signal frequency from rf amplifier 39AR1 by 12 or 16 to provide the final local oscillator frequency to bandpass filter 39FL2.

Figure 2-111. RF Amplifier 39AR1, Schematic Diagram.



NOTES

| SYMBOL | DESIGNATION, UNIT                                |
|--------|--|
| R      | NONE (OHM)<br>K (KILOHM)<br>M (MEGOHM)           |
| C      | PF (PICOFARAD)<br>NONE (MICROFARAD)              |
| L      | NONE (MICROHENRY)<br>m (MILLIHENRY)<br>H (HENRY) |

- 2- → MAJOR FUNCTIONAL FLOW  
 → ALC  
 → METERING

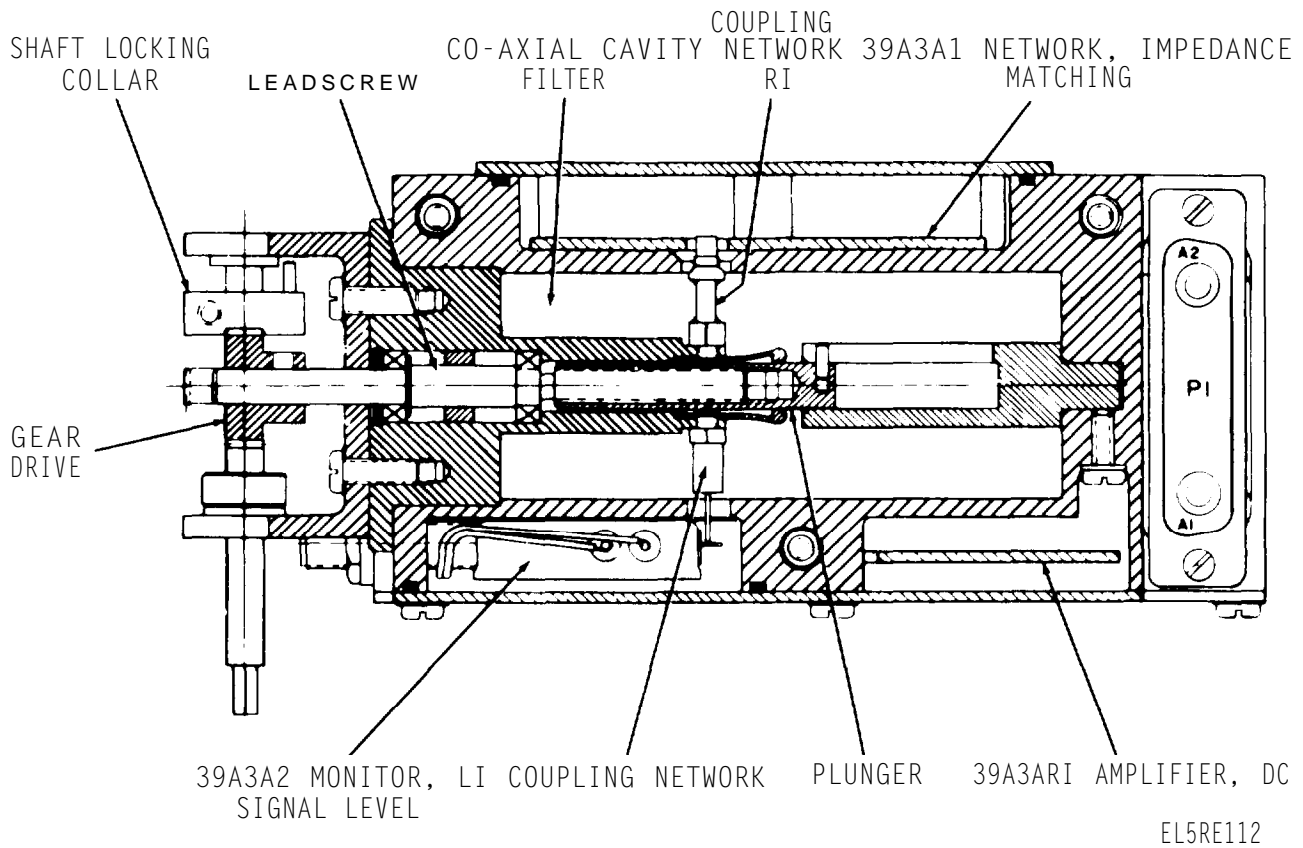


Figure 2-112. Frequency Multiplier 39A3, Cross-Sectional View.

The multiplier consists of three subassemblies: Impedance matching network 39A3A1, signal level monitor 39A3A2, and dc amplifier 39A3AR1. All three are mounted in a cast-aluminum housing which incorporates a tunable coaxial cavity filter as an integral part of the casting. Cavity tuning is accomplished with a plunger connected to a leadscrew. The leadscrew is connected externally, through speed decriaser gear assembly 39A1MP1, to the MULT PEAK and RCVR SIG tuning mechanism of the receiver rf head and is ganged to bandpass filter 39FL2.

b. Block Diagram Analysis (Fig. 2-113). The output of rf amplifier 39AR1 (105 to 140 MHz) is fed through impedance matching network 39A3A1, which consists of an equalizer stage and a matching stage. Frequencies in the lower part of the range are attenuated by the equalizer, while those in the upper part of the range are transmitted with no loss, to help maintain a more constant level of generated harmonics from multiplier diode CR1. The 50 ohm input impedance is transformed by the matching stage to match the impedance of CR1.

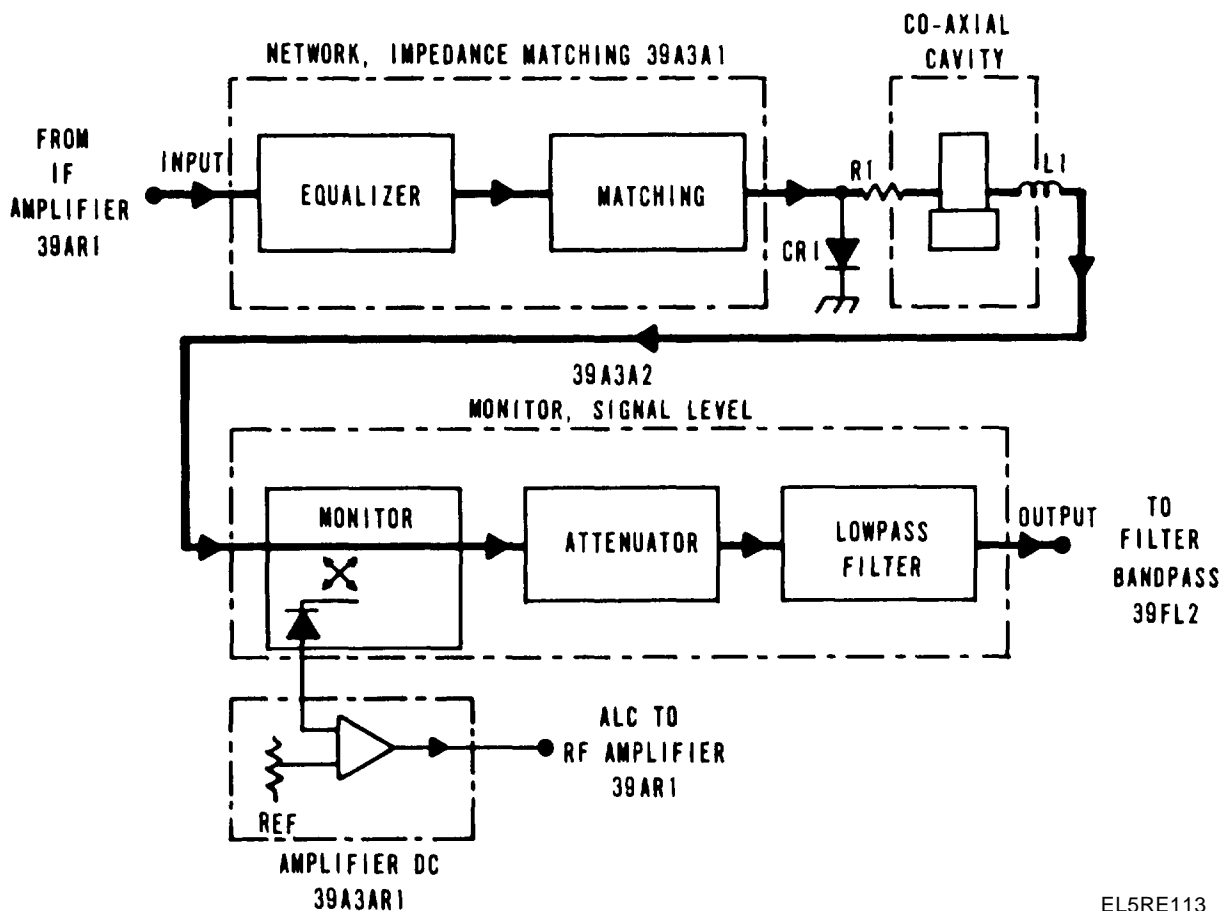
(1) Multiplier diode CR1 generates a series of harmonics of the applied signal above and below 2000 MHz. The harmonics are applied to the tunable cavity resonator, which selects either the 12th harmonic for all frequencies up to 1679.5 MHz, or the 16th harmonic for all frequencies of 1680 MHz and higher. Coupling networks R1 and L1 match the source and load impedances to the cavity resonator and achieve the correct loaded Q.



(2) The selected signal is fed to signal monitor 39A3A2, where an attenuator stage reduces signal level power to a level suitable for later application as a local oscillator at the mixer stage. A low-pass filter suppresses high-order harmonics that may have passed through the resonator filter.

(3) The amplitude of the multiplied signal is sampled and rectified by the monitor stage and passed to dc amplifier 39A3AR1, where a comparison is made with a reference signal preset to the correct output level. If the output is high and exceeds the reference signal, a control voltage is generated and applied to rf amplifier 39AR1 to reduce the drive to the multiplier and restore the required output.

c. Detailed Circuit Analysis (Fig. 2-114). An input of 105 to 140 MHz is fed from pin A1 of connector P1 to pin E1 on the printed circuit board of impedance matching network 39A3A1. Resistors A1R1, A1R2 and A1R3 provide an attenuating network for lower frequencies in the band, while A1C1-A1L2 and A1L1-A1C2 provide an rf bypass for the higher frequencies. A low-pass matching network to match the impedance of step recovery diode CR1 is provided by A1C3 through A1C7, A1L3 and A1L4. Component A1RT1 acts as a temperature-variable bias resistor, and A1L5 tunes with the capacitance of CR1 to maximize circulation of rf current through the diode. Capacitor C1 acts as a dc block to prevent the bias from short-circuiting through the tuned cavity resonator and networks. Input and output impedance is matched to cavi-



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Figure 2-113. Frequency Multiplier 39A3, Block Diagram.

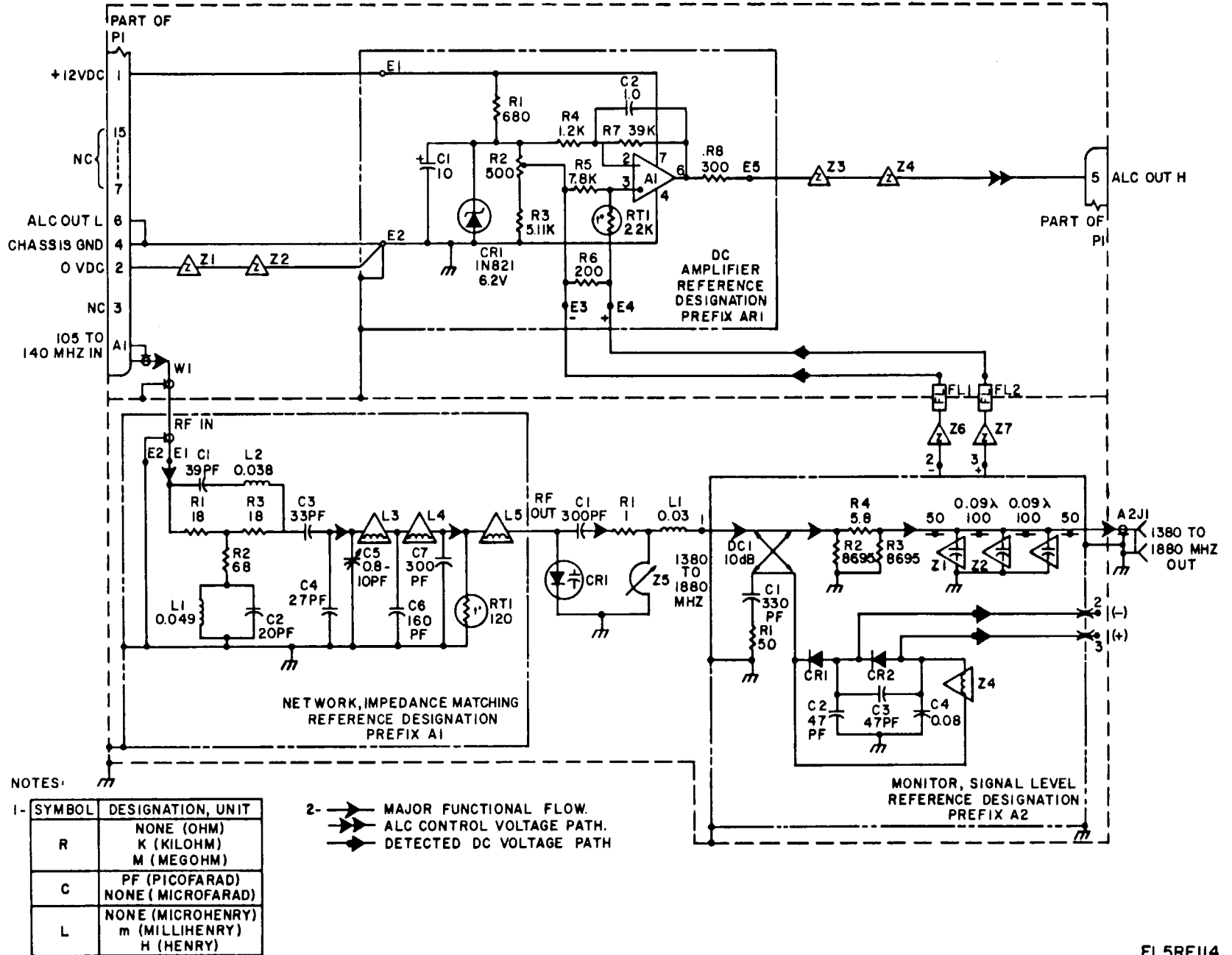


Figure 2-114. Frequency Multiplier 39A3, Schematic Diagram.

ty resonator Z5 by R1 and L1. The selected frequency from the cavity resonator (1380 to 1879.5 MHz) is fed to pin 1 on the microwave integrated circuit (MIC) case of signal level monitor 39A3A2.

(1) The 1380 to 1879.5 MHz signal is fed through a 1 db attenuator in the MIC of 39A3A2, and through a low-pass filter to output connector J1. Before the attenuator is reached, input signal amplitude is sampled through a 10 db coupling, and the result is fed to an rf detector diode. After passing through a protection and decoupling circuit, the detected dc voltage is fed from pins 2 and 3 on the MIC case, through filters FL1 and FL2, to terminals E3 and E4 on dc amplifier circuit board 39A3AR1. The +12 vdc required to operate the dc amplifier is applied through pins 1 and 2 of connector P1 and fed to terminals E1 and E2 on the dc amplifier circuit board.

(2) Microcircuit AR1A1 is an operational dc amplifier which provides a potential swing at output pin 6 when differing voltages are applied to input pins 2 and 3. Amplifier feedback is accomplished through AR1R4, AR1R7 and AR1C2, which also set the gain of the amplifier. Bias is provided to pin 2 of the amplifier by AR1R1 and voltage reference diode AR1CR1, while decoupling is provided by AR1C1. A voltage reference level to pin 3 of the amplifier is provided by AR1R2 and AR1R3, with AR1R2 set to ensure that alc maintains an output of approximately 10 Mv at connector A2J1.

(3) Signal level monitor 39A3A2 samples the detected dc voltage. When the voltage creates a potential difference across AR1R5, it is applied to pin 3 of the amplifier, causing a potential swing at pin 6. The voltage difference is then fed to rf amplifier 39AR1 through pin 5 of connector P1, thereby providing ale. If the output is short-circuited, AR1R8 provides current limiting. Thermistor AR1RT1, in the detected voltage line, provides temperature compensation for characteristic changes in the MIC hot carrier diode. A load to the detected dc voltage circuits in signal level monitor 39A3A2 is provided by AR1R6.

#### 2-117. IF Amplifier 39AR2 (F0-4-54)

Intermediate frequency amplifier 39AR2 is identical with intermediate frequency amplifier 33AR1/34AR1. Refer to paragraph 2-76 for the description of operation.



CHAPTER 3

DIRECT SUPPORT MAINTENANCE

Section I. INTRODUCTION

3-1. General

. This chapter covers direct support maintenance for Radio Set AN/GRC-103(V)1, Radio Set AN/GRC-103(V)2, Radio Set AN/GRC-103(V)3, and Radio Set AN/GRC-103(V)4. It lists the tools and test equipment needed to completely troubleshoot the radio set, trace faults to defective modules, and replace defective modules. Removal and replacement procedures for modules not replaced at the organizational level (TM 11-5820-540-12) are also included in this chapter. The troubleshooting and fault location techniques in this chapter supplement the operational check loop test procedure and troubleshooting charts of TM 11-5820-540-12. A loop test procedure that permits the radio set to be checked when associated multiplex equipment is not available is provided in paragraph 3-4.

b. For Repair Parts and Special Tools List (RPSTL), refer to TM 11-5820-540-34P, Direct Support and General Support Maintenance Repair Parts and Special Tools Lists (Including Depot Maintenance Repair Parts and Special Tools) for Radio Set AN/GRC-103(V)1.

3-2. Test Equipment Required

The following test equipment, cables, connectors, and tools are required for troubleshooting Radio Sets AN/GRC-103(V)1, AN/GRC-103(V)2, AN/GRC-103(V)3, and AN/GRC-103(V)4.

a. Test Equipment

| Equipment   | Common Name                    | Qty |
|---|--------------------------------|-----|
| Attenuator Fixed, 10dB, CN-1286/U . . . . .             | 10dB Attenuator. . . . .       | 1   |
| Attenuator Fixed, 20dB, CN-1287/U . . . . .             | 20dB Attenuator . . . . .      | 1   |
| Converter, Signal Frequency, CV-2500/GRC . . . . .      | Loop Test Set . . . . .        | 1   |
| Counter, Electronic Frequency, AN/USM-459 . . . . .     | Frequency Counter . . . . .    | 1   |
| Dummy Load, Electrical, DA-437/U/GRC-103 . . . . .      | Dummy Load . . . . .           | 1   |
| Generator, Signal AN/USM-213 . . . . .                  | Signal Generator . . . . .     | 1   |
| Generator, Signal SG-340A/U . . . . .                   | Signal Generator . . . . .     | 1   |
| Generator, Signal SG-1170/U . . . . .                   | Signal Generator . . . . .     | 1   |
| Generator, Signal, SG-1171/U . . . . .                  | Wide Range Oscillator. . . . . | 1   |
| Load, 91 ohms, ±2%, RF-239/U, P/O MK-1184 Kit . . . . . | Load, 91 ohms . . . . .        | 1   |

| Equipment  | Common Name                  | Qty |
|--|------------------------------|-----|
| Load, 51 ohms, $\pm 2\%$ , RF-240/U, P/O MK-1184 Kit . . . . . | Load. 51 ohms . . . . .      | 1   |
| Meter, Modulation, ME-57A/U . . . . .                          | Deviation Meter . . . . .    | 1   |
| Meter, Power, ME-441/U with Thermistor Mount . . . . .         | Power Meter . . . . .        | 1   |
| HP-478A  | Thermistor Mount . . . . .   | 1   |
| Multimeter, Digital, AN/USM-486 . . . . .                      | Digital Multimeter . . . . . | 1   |
| Oscilloscope, Dual Trace, OS-261C(V)/1/U . . . . .             | Oscilloscope . . . . .       | 1   |
| Voltmeter, Electronic, ME-30A/U . . . . .                      | VTVM . . . . .               | 1   |
| Wattmeter, RF, AN/URM-120 . . . . .                            | Wattmeter . . . . .          | 1   |
| Wattmeter, RF, AN/USM-298 (Band IV only) . . . . .             | Wattmeter . . . . .          | 1   |
| Element, Wattmeter: Bird No. 10K, 1100-1800MHZ . . . . .       | Element . . . . .            | 1   |
| Element, Wattmeter: Bird No. 25K, 1100-1800MHZ . . . . .       | Element . . . . .            | 1   |
| Element, Wattmeter: Bird No. 433-103, 50 Watt, . . . . .       | Element . . . . .            | 1   |
| modified, 1350-1850MHZ   |                              |     |
| Voltmeter, RF, ME-426/U . . . . .                              | RF Voltmeter . . . . .       | 1   |

(1) Connectors, p/o Maintenance Kit MK-1184/GRC.

Description

|   |   |
|---|---|
| Adapter-Connector UG-29B/U (N (Female) to N (Female) ) . . . . .  | 3 |
| Adapter-Connector UG-201A/U (BNC (Female) to N (Male) ) . . . . . | 2 |
| Adapter-Connector UG-274/U (BNC "T", 2 Female, 1 Male) . . . . .  | 2 |
| Adapter-Connector UG-491A/U (BNC (Male) to BNC (Male) ) . . . . . | 1 |
| Adapter-Connector UG-564A/U (C (Female) to N (Male)) . . . . .    | 1 |
| Adapter-Connector UG-565A/U (C (Male) to N (Female)) . . . . .    | 2 |
| Adapter-Connector UG-636A/U (BNC (Female) to C (Male) ) . . . . . | 1 |

(2) Additional connectors required.

Description

|  |   |
|--|---|
| Adapter-Connector, UG-914/U (BNC (Female) top BNC (Female)) . . . . .  | 1 |
| Adapter-Connector, OS-20200-2 (OSM "T", 2 Female and 1 Male) . . . . . | 1 |

| Description   | Qty |
|---|-----|
| Adapter-Connector, OS-21010 (OSM (Female) to N (Female) ) . . . . . | 2   |
| Adapter-Connector, OS-21030 (OSM (Male) to N (Female) ) . . . . .   | 2   |
| Adapter-Connector, OS-21020 (OSM (Female) to N (Male) ) . . . . .   | 2   |

c. General Purpose Cable Assemblies.

(1) Cable Assemblies, P/O Maintenance Kit MK-1184/GRC.

| Type No.            | Connector Types                               | Qty |
|---------------------|---|-----|
| CG-3578/U . . . . . | Male microminiature to female BNC . . . . .   | 1   |
| CG-3579/U . . . . . | Male microminiature to male BNC. . . . .      | 1   |
| CG-3580/U . . . . . | Female microminiature to female BNC . . . . . | 1   |
| CG-3581/U. . . . .  | Female microminiature to female BNC . . . . . | 1   |
| CG-409H/U . . . . . | Male BNC to male BNC . . . . .                | 3   |
| CG-1883/U . . . . . | Male to male. N . . . . .                     | 1   |

(2) Additional General Purpose Cable Assemblies.

| Type No.            | Connector Types   | Qty |
|---------------------|---|-----|
| CG-3568/U . . . . . | Male N to Male N, 2 feet . . . . .                                  | 1   |
| CG-3573/U . . . . . | Male OSM to Male OSM, 4.8 inches . . . . .                          | 2   |
| CG-3570/U.....      | Male BNC to Female electrical contact, Cannon No ..<br>DM53740-5001 | 1   |
| CG-3444/U . . . . . | Male C to Male C, 1.5 feet . . . . .                                | 1   |
| CG-3444/U . . . . . | Male C to Male C, 3.5 feet. . . . .                                 | 2   |
| CG-3569/U . . . . . | Male C to Male N, 2 feet . . . . .                                  | 1   |

d. Special Purpose Cable Assemblies

(1) Cable Assemblies, P/O Maintenance Kit MK-1184/GRC.

| Type No.             | Connects   | Qty |
|----------------------|--|-----|
| CX-12092/U . . . . . | Radio transmitter 5TR1 to transmitter case 5A2 . . . . . | 1   |
| CX-12093/U . . . . . | Radio transmitter 5TR1 to transmitter case 5A2 . . . . . | 1   |
| CX-12094/U . . . . . | Transmitter RF head to transmitter case 5A2 . . . . .    | 1   |

| Type No.             | Connects   | Qty |
|----------------------|--|-----|
| CX-12095/U . . . . . | Radio receiver 1RE1 to receiver case 1A2 . . . . .   | 1   |
| CX-12096/U . . . . . | Radio receiver 1RE1 to receiver case 1A2 . . . . .<br>and/or<br>Video amplifier 1RE1AR1 to radio receiver 1RE1<br>and/or<br>Pulse form restorer 1RE1A3 to radio receiver 1RE1<br>and/or<br>Amplifier-monitor 5TR1A5 to radio receiver 1RE1 | 4   |
| CX-12097/U . . . . . | Receiver RF head to receiver case 1A2 . . . . .  | 1   |
| CX-12098/U . . . . . | Power supply 1RE1PS1 to radio receiver 1RE1 . . . . .<br>and/or<br>Control-indicator 6A2, 37A2, 38A2, or 40A4 to transmitter<br>RF head<br>and/or<br>Control-indicator 2A2, 33A4, 34A4, or 39A4 to receiver RF<br>head                     | 3   |
| CX-12099/U . . . . . | Electrical frequency limiter-discriminator 1RE1A4 to . . . . .<br>video amplifier 1RE1AR1  | 1   |
| CX-12100/U . . . . . | Electrical frequency synthesizer 1RE1A2 to radio . . . . .<br>receiver 1RE1<br>and/or<br>Electrical frequency synthesizer 5TR1A2 to radio . . . . .<br>transmitter 5TR1  | 2   |
| CX-12101/U . . . . . | Power Supply 5TR1PS1 to transmitter case 5A2 . . . . .   | 1   |
| CX-12102/U . . . . . | Amplifier assembly 9A4 to distribution panel 9A1 . . . . .<br>and/or<br>Telephone signal converter 9A3 to distribution panel<br>9A1  | 2   |
| CX-12103/U . . . . . | Alarm control 5TR1A3 to radio transmitter 5TR1 . . . . .   | 1   |

(2) Additional Special Purpose Cable Assemblies.

| Type No.            | Connects  | Qty |
|---------------------|---|-----|
| CMC 217-800000-000. | If amplifier 1RE1AR2 to electrical frequency limiter-<br>discriminator 1RE1A4 (Fabricated Figure 3-7) | 1   |

e. Special Tools.

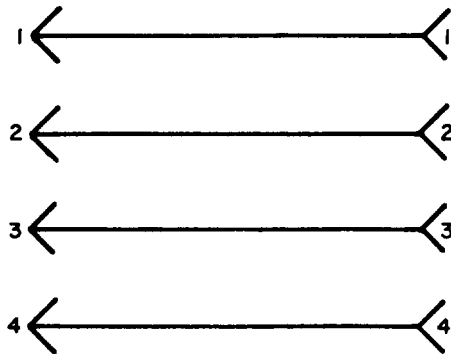
| Item  | National Stock Number | Qty |
|---|-----------------------|-----|
| Wrench socket 1/2-inch drive, 7/8-inch head | 5120-00-243-7342      | 1   |
| Handle, 9-inch                              | 5120-00-230-6385      | 1   |



FABRICATE SPECIAL PURPOSE CABLE 217-800000-00

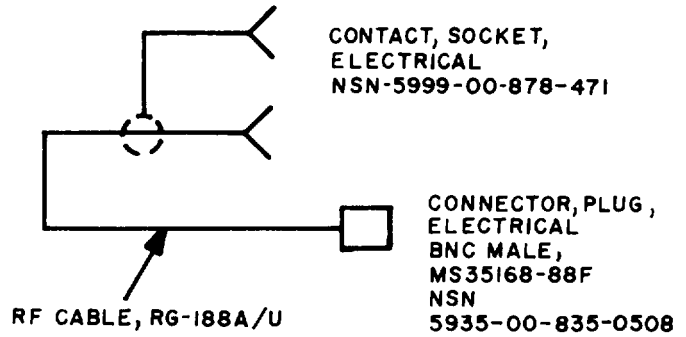
CONNECTOR, PLUG,  
ELECTRICAL DEM5WIPC 33  
NSN 5935-00-102-3868

4 PIN MALE



CONNECTOR, PLUG,  
ELECTRICAL DEM5WISC 33  
NSN-5935-00-990-7521

4 PIN FEMALE



EL5RE350

Section II. TROUBLESHOOTING

3-3. General

a. This section contains the systematic troubleshooting procedure required to sectionalize a fault in the radio set and to trace the fault to the defective module or part. Front panel indications may help in locating faults without the use of test equipment. Operational tests frequently indicate the general location of trouble and in many instances help in determining the nature of the fault. The operational check, loop testing procedure, and the troubleshooting charts contained in TM 11-5820-540-12 are suitable starting points. The modified loop test procedure (para 3-4), troubleshooting charts (paras 3-5 through 3-43), and signal substitution procedures enable direct support personnel quickly to localize the faulty module. Replacement of one or more suspected defective modules may be a quick and effective method of repairing a radio set in emergency conditions.

b. For Repair Parts and Special Tools List (RPSTL), refer to TM 11-5820-540-34P, Direct Support and General Support Maintenance Repair Parts and Special Tools Lists (Including Depot Maintenance Repair Parts and Special Tools) for Radio Set AN/GRC-103(V)1.

3-4. Loop Test Procedure

The purpose of this procedure is to sectionalize faults in the radio set, using the loop test procedure and troubleshooting charts in chapter 6 of TM 11-5820-540-12, but using a test signal of known amplitude instead of a test signal from the associated multiplex equipment.

a. Equipment Required.

| Equipment  | Common Name           |
|--|-----------------------|
| Generator, Signal SG-1171/U  | Wide range oscillator |
| Oscilloscope, Dual Trace OS-261C(V)1/U                             | Oscilloscope          |
| Converter, Signal Frequency, Electronic CV-2500/GRC                | Loop test set         |
| Dummy Load, Electrical DA-437/U/GRC-103                            | Dummy load            |
| Cable Assembly, Radio Frequency CG-409H/U (4.5 ft)<br>(2 required) |                       |
| Connector, Adapter UG-274/U  |                       |

b. Connections and Test Procedures

- (1) Set up the loop test as shown in figure 6-3, TM 11-5820-540-12.
- (2) Connect the output of the wide range oscillator to the VIDEO connector at the rear of the transmitter case and to the oscilloscope using two CG-409H/U (4.5 ft) cables and the UG-274A/U.
- (3) Set the frequency of the wide range oscillator to 10 kHz and adjust the amplitude of the output signal to 2 volts peak-to-peak as measured on the oscilloscope.

- (4) Proceed with the loop test procedure and troubleshooting charts as described in chapter 6 of TM 11-5820-540-12, supplemented by the troubleshooting charts in paragraphs 3-5 through 3-7 in this manual.
- (5) If the fault cannot be sectionalized using the loop test procedure and troubleshooting charts, proceed to isolate the fault by signal substitution or fault locating procedures described in paragraphs 3-8 through 3-43.

### 3-5. Transmitter Troubleshooting

#### CAUTION

The transmitter rf head when extended must be air-cooled during tests; a cooling fan must be pointed toward the power amplifier tubes at all times. If a cooling fan is not available the transmitter rf head must not be operated for longer than 5 minute periods. Another alternative is to place the transmitter rf head back into the transmitter case while troubleshooting radio transmitter 5TR1.

a. General. For effective troubleshooting of the transmitter, remove the transmitter rf head and radio transmitter 5TR1 from the transmitter case. Remove the transmitter rf head dust cover. Connect the transmitter rf head to the transmitter case using CX-12094/U extender cable and connect radio transmitter 5TR1 to the transmitter case using CX-12092/U and CX-12093/U extender cables. Connect the transmitter to a 115 volt, 47 to 420 Hz source and proceed to troubleshoot the transmitter.

#### CAUTION

The transmitter rf head PWR OUT connector must be connected to the dummy load, during troubleshooting. Damage to the equipment will result if this is not done.

#### NOTE

There are three models of Amplifier-Frequency Multiplier distinguishable by nomenclatures AM-4320/GRC-103(V), AM-4320A/GRC-103(V) and AM-4320B/GRC-103(V). Unless otherwise indicated this paragraph refers to all units.

#### NOTE

On Transmitter Radio T-983B(P)/GRC-103(V) the centrifugal fan does not start instantaneously if the unit is at room temperature (25°C). Allow a few minutes warm up time. At very cold temperatures, or if unit is already warmed up, the fan should start when AC POWER switch is set to ON/RESET.

b. Transmitter Troubleshooting Chart.

| Symptom  | Probable cause  | Checks and corrective measures   |
|--|---|--|
| <p>1. When AC POWER switch is set to ON/RESET, centrifugal fan does not start, AC POWER AND LOW POWER lamps do not light, buzzer does not sound.</p> | <p>a. Defective power supply 5TR1PS1.</p> <p>b. Defective switch 5TR1-A1CB1 (fig. 3-3).</p> | <p>a. Check for 115 v ac at connector J3 (5TR1PS-1P1) pins 6 and 7 (para 3-8) . If voltage is present, replace 5TR1-PS1 (para 3-50).</p> <p>b. If voltage not present (a above”), check for 115 v ac at switch LINE and LOAD terminals. If indications are normal make wiring continuity checks.</p> |
| <p>2. 28V and 12V metering reads negative, all other metering zero. LOW POWER and SYNC lamps light.</p>  | <p>Short circuit.</p>   | <p>Check for short on 28 v supply line.</p>  |
| <p>3. 12V metering reads negative, 28V full scale, 600 V high, DRIVER normal, all other metering zero. LOW POWER and SYNC lamps light.</p>           | <p>Short circuit.</p>   | <p>Check for short on 12 v supply line.</p>  |
| <p>4. All metering reads zero, all lamps are inoperative, centrifugal fan operates.</p>  | <p>Short circuit.</p>   | <p>Check for short on 26 v supply line.</p>  |
| <p>5. 28V normal or zero, 12V normal, DOUBLER, MULT, DRIVER and PWR OUT low, OSC high. LOW POWER and SYNC lamps light.</p>                           | <p>Open circuit.</p>  | <p>Check for open 28 v supply line.</p>  |
| <p>6. When AC POWER switch is set to ON/RESET centrifugal fan does not start; AC POWER, LOW POWER, and OVER-HEAT lamps light; buzzer sounds.</p>     | <p>a. Defective centrifugal fan 5A2B1.</p>  | <p>a. Check for 140 vac at connector J5 (5A2B1P1). pins 1 and 2, in transmitter case. If voltage is present replace 5A2B1 (section X).</p>   |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom   | Probable cause   | Checks and corrective measures  |
|---|--|---|
| 6. Continued.   | b. Defective power supply 5TR1PS1.   | b. (1) Check for 140 vac at power supply filter terminals FL5 and FL6 of 5TR1PS1 (fig. 3-2). If no voltage is present replace 5TR1PS1 (para 3-50).<br><br>(2) If voltage is present at FL5 and FL6 of 5TR1PS1 but not at pins 1 and 2 of connector J5 (5A2B-1P1) in the transmitter case disconnect 115 vac power source and check for continuity between these two points. |
| 7. When AC POWER switch is set to ON/RESET, centrifugal fan does not start. OVERHEAT lamp is not on. Buzzer may or may not sound. All other indications normal. | a. Defective OVERHEAT lamp 5TR1A2A2DS4.<br><br>b. Defective pressure differential monitor 5A2A2. | a. Replace indicator lamp 5TR1A2A2A2DS4.<br><br>b. Replace 5A2A2 (section x).   |
| 8. Buzzer does not sound when an alarm lamp lights or goes out.   | a. Defective buzzer 5TR1-A1DS5 (fig. 3-3).<br><br>b. Defective switch 5TR1-A1S2 (fig. 3-3).      | a. Check for +26 vdc at buzzer terminals. If voltage is present replace the buzzer (para 3-52).<br><br>b. If voltage is not present at buzzer terminals disconnect 115 vac power source and check for continuity from the buzzer negative terminal to pin 5 of connector J3 (5TR1PS1P1) and from the buzzer positive terminal to pin 4                                      |

b. Transmitter Troubleshooting Chart - Continued

| Symptom   | Probable cause  | Checks and corrective measures  |
|---|---|---|
| 8. Continued.   | <p>c. Defective alarm control 5TR1A1A2 (fig. 3-3)</p>                                 | <p>of 5TR1A1J3. If continuity is broken because of 5TR1A1S2, higher category maintenance is required.</p> <p>c. If continuity is broken because of 5TR1A1A2, replace 5TR1A1A2 board (para 3-51).</p>  |
| 9. OVERHEAT lamp does not go off within 10 seconds after AC POWER switch is set to ON/RESET.                      | <p>a. Defective pressure differential monitor 5A2A2 .</p> <p>b. Defective wiring.</p> | <p>a. Replace 5A2A2 (section x).</p> <p>b. If other than zero, resistance may exist between 6AR1A1FL1 and ground (FO-4-43).</p>   |
| 10. AC POWER switch set to ON/RESET at room temperature centrifugal fan operates full speed (Case CY-4637A only). | <p>Defective control monitor temperature sensor 5A2A2.</p>                            | <p>Check sensor connections. If connections are not defective, replace 5A2A2 (section X).</p>   |
| 11. SYNC light does not go out within 10 seconds after AC POWER switch is set to ON/RESET.                        | <p>a. Defective synthesizer 5TR1A2.</p> <p>b. Defective power supply 5TR1PS1.</p>     | <p>a. Extend the synthesizer (para 3-10) and check for 12 v, 26 v and 28 v at J1 (X5TR1A2P2) (fig. 3-3). If normal indications are obtained replace synthesizer 5TR1A2 (para 3-48).</p> <p>b. If indications in a above are abnormal, check 5TR1PS1 (para 3-8). If abnormal indications are obtained replace 5TR1PS1 (para 3-50).</p> |

b. Transmitter Troubleshooting Chart - Continued

| Symptom  | Probable cause   | Checks and corrective measures   |
|--|--|--|
| <p>12. DRIVER metering greater than 100% (Transmitter equipped with Amplifier-Frequency Multiplier AM-4320/GRC-103(V)).</p>                                    | <p>c. Defective wiring.</p> <p>Loss of control voltage to rf power level control 6A5.</p>  | <p>c. If abnormal indications are obtained in b above check the wiring between 5TR1PS1 and J2 (X5TR1A22P2) FO-4-43).</p> <p>Voltage at 6A4FL1 (fig. 3-6) should be between 7.2 and 9.5 volts (para 3-16). If normal or high replace 6A5 (para 3-57). If zero, check wiring (FO-4-43).</p>  |
| <p>13. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR OUT position reads low.</p>                             | <p>a. Defective power monitor 6AR1A3.</p> <p>b. Defective low pass filter 6AR1A2FL1 (para 3-20).</p> <p>c. Defective amplifier subassembly 6AR1A1 (para 3-18).</p> | <p>a. Measure power at P2 (6AR1A3J1) (fig. 3-14). If normal (para 3-20), check 6AR1A3 (para 3-21).</p> <p>b. If power indication at P2 (6AR1A3J1) is abnormal, (a above), measure the power at 6AR1A1J2 (fig. 3-6). If normal, (para 3-18) higher category of maintenance is required.</p> <p>c. If abnormal indication is obtained in b above measure the power at 6AR1A2A4J2 (fig. 3-6) (not less than 3.5 watts). If normal, higher category maintenance is required.</p> |
| <p>14. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR OUT position reads low, DRIVER position reads high.</p> | <p>No OUTPUT CATHODE regulation.</p>   | <p>Remove radio transmitter 5TR1 and measure the resistance from pin 30 of connector J8 (X5TR1A1A1P3) (transmitter case) to ground (approximately 14 ohms). If normal, replace 5TR1PS1 (para 3-50). If abnormal check 6AR1A2A2 (para 3-19).</p>  |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom   | Probable cause  | Checks and corrective measures  |
|---|---|---|
| <p>15. LOW POWER light does go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR OUT position reads low, DRIVER position reads low.</p> | <p>a. Defective OUTPUT CATHODE/OUTPUT HEATER circuit.</p> <p>b. Defective filter assembly 6AR1A2A4.</p> <p>c. No DRIVER CATHODE regulation.</p> <p>d. Defective DRIVER CATHODE/DRIVER HEATER circuit.</p> <p>e. Defective amplifier subassembly 6AR1A1.</p> | <p>a. Measure the power at 6AR-1A2A4J2 (fig. 3-6). If normal (not less than 3.5 watts) check the voltage at TP1 and TP2 of 6AR1A2A2 (fig. 3-13). If normal (para 3-19) disconnect the transmitter rf head and measure resistance between TP1 and TP2 of 6AR1A2A2 (should be 1.5 ohm approximately).</p> <p>b. If voltage at TP1 and TP2 is abnormal check the OUTPUT HEATER/OUTPUT CATHODE circuit of 5TR-1PS1 (para 3-8).</p> <p>c. If 5TR1PS1 check is normal, check continuity of OUTPUT HEATER/OUTPUT CATHODE wiring between 5TR1PS1 and 5TR1A1P3 (FO-4-43).</p> <p>d. If the power at 6AR1A-2A4J2 is abnormal measure the power at P1 (6AR1A2A4J3). If normal, (not less than 3.5 watts), higher category of maintenance is required.</p> <p>e. Remove the radio transmitter from the case and measure the resistance from pin 29 of connector J8 (X5TR1-A1A1P3) to ground (36 ohms approximately). If normal replace 5TR1PS1 (para 3-50). If abnor-</p> |



h. Transmitter Troubleshooting Chart - Continued

| Symptom        | Probable cause   | Checks and corrective measures  |
|----------------|--|---|
| 15. Continued. | <p>f. Defective filter assembly 6AR1A2A4.</p> <p>g. Defective rf power level control 6A5. Transmitter equipped with Amplifier-Frequency Multiplied AM-4320/GRC-103(V).</p> | <p>mal check 6AR1A2A2 (para 3-19). Check 6AR1A1C5/C11 (para 4-20 TM 11-5820-540-40).</p> <p>f. Measure the power at 6AR1A2A4J4 (para 3-17). If normal, check the voltage across TP3(-) and TP4(+) of 6AR1A2A2. It should be +5.8 v <math>\pm 0.5</math> vdc (fig. 3-13). If normal, remove the transmitter rf head and measure the resistance at TP3 and TP4 of 6AR1A2A2 (1.5 ohms approximately). If voltage at TP3 and TP4 is abnormal, check the DRIVER HEATER/DRIVER CATHODE circuit of 5TR1PS1 (para 3-8). if 5TR1PS1 check is normal, check the continuity of the OUTPUT HEATER/OUTPUT CATHODE wiring between 5TR1PS1 and transmitter rf head (FO-4-43).</p> <p>g. If the DRIVER CATHODE/DRIVER HEATER circuit is normal higher category maintenance is required.</p> <p>h. If the power at 6AR1A2AJ4 is abnormal measure the power at P2 (6AR1A2A4J1). If it is normal (+23 dbm minimum), higher category maintenance is required.</p> |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom   | Probable cause   | Checks and corrective measures  |
|---|--|---|
| 15. Continued.  |  | i. If power at P2 (6AR2A2-A4J1) is abnormal measure the power at 6A1J6 (+26.4 dbm minimum). If normal, replace 6A5 (para 3-571).  |
| 16. At channel 180 and above or channel 179 and below LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR CUT position reads low, DRIVER position reads low, and MULT position reads low. | a. Defective frequency multiplier assembly 6A2 .<br>b. Defective wiring.     | a. Check the output of 6A2 (para 3-15).<br>b. Check voltages at 6W1J1 (para 3-14).  |
| 17. Same as 14 above but at all channels.   | a. Defective wiring.<br>b. Defective amplifier-frequency multiplier 5TR1A4 . | a. Measure power at P2 (XA1J5) (fig. 3-6) 2.5 watts minimum (para 3-11). If abnormal, check for continuity from P2 (XA1J5) to pin AZ of J11 (X5TR1A4P1) (FO-4-43).<br>b. If power indication at P2 in a above is normal, replace 5TR1A4 (para 3-49) . |
| 18. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. DRIVER position reads low, MULT position reads low, DOUBLER position reads low.   | a. Defective amplifier-frequency multiplier 5TR1A4 .<br>b. Defective wiring. | a. Measure the power at pin A1 of J11 (X5TR1A4P1) (para 3-10). If it is normal, check 5TR1A4 (para 3-11).<br>b. Check for +28 v at pin 1 of J11 (X5TR1A4P1). Check for ground at pin 17 of J11 (X5TR1A4P1) with the transmitter rf head connected.    |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom   | Probable cause  | Checks and corrective measures  |
|---|---|---|
| <p>19. LOW POWER light does not go out within 60 seconds after AC POWER switch is set ON/RESET. DRIVER position reads low, MULT position reads low, DOUBLER position reads low, OSC position reads low.</p> | <p>a. Defective electrical frequency synthesizer 5TR1A2.<br/>b. Defective wiring.</p>                       | <p>a. Check synthesizer 5TR1A2 (para 3-10).<br/>b. Check inputs to 5TR1A2 at J1 (X5TR1A2P2) (FO-4-43) pin 1 +28 vdc pin 3 0 v pin 2 +12 vdc pin 37 +28 vdc.</p> |
| <p>20. SYNC alarm does not go out within 10 seconds after AC POWER switch is set to ON/RESET.</p>   | <p>a. Defective synthesizer 5TR1A2.<br/>b. Defective power supply 5TR1PS1.</p>                              | <p>a. Check synthesizer 5TR1A2 (para 3-10).<br/>b. Check power supply 5TR1PS1 (para 3-8).</p>   |
| <p>21. When AC POWER switch is set to ON/RESET, buzzer and centrifugal fan operate, LOW POWER and SYNC alarm lights come on, DRIVER metering is low, all other metering reads zero.</p>                     | <p>Defective power supply 5TR1PS1.</p>  | <p>Check voltage regulator amplifier 5TR1PS1AR1 of power supply 5TR1PS1 (para 3-8).</p>   |
| <p>22. No communication. Metering and LOW POWER and SYNC alarms may or may not indicate norms .</p>   | <p>Synthesizer is off frequency due to -<br/>a. Defective synthesizer 5TR1A2 .<br/>b. Defective wiring.</p> | <p>a. Check synthesizer (para 3-10).<br/>b. Check wiring from control indicator 6A3 to the synthesizer (FO-4-43).</p>   |

3-6. Receiver Troubleshooting

a. General. For effective troubleshooting of the receiver, remove the receiver rf head and radio receiver 1RE1 from the receiver case. Remove the receiver rf head dust cover. Connect the receiver rf head to the receiver case using CX-12097/U extender cable. Connect the radio receiver to the receiver case using CX-12095/U and CX-12096/U extender cables. Connect the receiver to a 115 volt, 47 to 420 Hz source and proceed to troubleshoot the receiver.

NOTE

There are two models of Amplifier-Converter distinguishable by nomenclatures AM-4316/GRC-103(V) and AM-4316A/GRC-103(V). Unless otherwise indicated, reference is to both units.

b. Receiver Troubleshooting Chart.

| Symptom  | Probable cause   | Checks and corrective measures  |
|--|--|---|
| 1. With AC POWER switch set to ON, there are no meter indications and no alarms. | Defective switch 1RE1A1CB1.  | Check for 115 vac at switch LINE and LOAD terminals (fig. 3-40). If switch is normal, make wiring continuity checks (F0-4-28).  |
| 2. Buzzer does not sound when any alarm lamp lights or goes out.                 | a. Defective buzzer 1RE1A1DS5.<br><br>b. Defective alarm control 1RE1A1A2 (fig. 3-37). | a. Check for 26 vdc at buzzer terminals (fig. 3-37). If voltage is present replace buzzer (para 3-60). If voltage is not present, make wiring continuity checks (F0-4-28) .<br><br>b. If continuity is broken because of 1RE1A1A2 replace 1RE1A1A2 (para 3-61). |
| 3. AC POWER switch will not stay on.   | Short circuit.   | Make resistance checks on -12 vdc, +12 vdc and +26 vdc lines to isolate short.  |
| 4. LOW SIGNAL alarm is on; RCVR SIG metering reads low.                          | a. Defective power monitor 2A1A5.  | a. Inject a signal at -65 dbm at the receiver frequency into 2A1A-1Z14J1 (fig. 3-18). If the alarm clears replace 2A1A5 (para 3-64).  |

b. Receiver Troubleshooting Chart - Continued

| Symptom       | Probable cause   | Checks and corrective measures  |
|---------------|--|---|
| 4. Continued. | <p>b. Defective duplexer 2A1A1 .</p> <p>c. Defective wiring.</p> <p>d. Defective low pass filter 2A1A1FL1.</p> <p>e. Defective radio frequency amplifier 2A1AR1.</p> | <p>b. If the alarm condition remains, inject the signal into P3 (2A1A-1A1J2) (fig. 3-20). If alarm clears, higher category of maintenance is required.</p> <p>c. If the alarm condition remains, inject the signal into 2A1A1FL1J1 (fig. 3-20). If the alarm clears, check voltages at pins 1, 2, and 3 on J5 (XPS1P1) (under power supply 2PS1). Pin 1(+) to pin 2(-) +12 vdc. Pin 2(+) to pin 3(-) -12 vdc.</p> <p>d. If the alarm condition remains, inject the signal into P1 (2A1A1F-L1J2) (fig. 3-20). If the alarm clears replace low pass filter 2A1A1FL1, (para 3-67).</p> <p>e. If the alarm condition remains, inject signal into P1 (2A1AR1J2) (fig. 3-18). If the alarm clears, check the voltages at pins 1, 2, and 3 on connector J1 (X2A1AR1P2). Voltages should be as in c above. If voltages at J1 (X2A1AR1P2) are normal, replace radio frequency amplifier 2A1-AR1 (para 3-63).</p> |

b. Receiver Troubleshooting Chart - Continued.

| Symptom  | Probable cause                                 | Checks and corrective measures  |
|--|--|---|
| 4. Continued.  | f. Defective bandpass filter assembly 2A1A2A3. | f. If the alarm condition remains, remove frequency mixer stage 2A1A2A2 and inject the signal into connector P2 to 2A1A2A2; connect connector P3 of 2A1A2A2 to J2 (X2A1A2A2P3). If the alarm clears, higher category maintenance is required.   |
|  | g. Defective frequency mixer stage 2A1A2A2.    | g. If the alarm condition remains, inject a 30 MHz signal at -35 dbm into P1 (XA1A2A2J2). If alarm clears replace 2A1A2A2 (para 3-66).  |
|  | h. Defective wiring.                           | h. If the alarm condition remains, inject the signal into PI (XA1-W3J4) (fig. 3-20). If the alarm clears, check voltage between pin 1(+) and pin 3(-) of connector J1 of 2A1A-2AR1. It should be -12 vdc. If the alarm condition remains the fault will be in the remaining module interconnections (FO-4-28). Check the continuity of signal path to 1RE1AR1. If normal, check voltages at pins 1, 2 and 3 on 1RE1A1J2. Voltages should be as under c above. |
| 5. LOW SIGNAL alarm, RCVR SIG reading low; MULT reading low. | a. Defective wiring                            | a. Measure power at plug P2 (fig. 3-20) (minimum of +12.5 dBm). If abnormal check wiring between plug P2 or connector 2A1A3 and pin A1 of 1RE1A1A1J3.   |

b. Receiver Troubleshooting Chart - Continued

| Symptom   | Probable cause  | Checks and corrective measures   |
|---|---|--|
|   | b. Defective bandpass filter 2A1A2A3/frequency multiplexer 2A1A2A1 combination.                     | b. If power at P2 is normal (a above) measure the power at J1 (P/O 2A1A2-A3) (para 3-33). If abnormal, higher category of maintenance is required. |
| 6. SYNC alarm and/or LOW SIGNAL alarm, RCVR SIG reading low, MULT reading low, OSC reading low. | Defective synthesizer 1RE1A2.   | Check supply voltages at J3 (1RE1A2P2). If normal, change synthesizer 1RE1A2 (para 3-59). If abnormal, check wiring (FO-4-28).                     |
| 7. LOW SIGNAL alarm, RCVR SIG reading low.  | Local oscillator frequency off due to -<br>a. Defective synthesizer 1RE1A2.<br>b. Defective wiring. | a. Check synthesizer (para 3-33)<br>b. Check wiring from control-indicator 2A2 to J3 (1RE1A2P2) (FO-4-28).   |

3-7. Order Wire Troubleshooting

a. General. To troubleshoot this unit, first remove monitor panel 9A2 (front panel); loosen the four green circled screws that secure the front panel to the order wire case and pull the front panel away from the case (fig. 3-49). Repeat the above procedure to remove distribution panel 9A1 (rear panel) from the case (fig. 3-49). The printed circuit boards remain connected to the rear panel.

NOTE

The complete radio set is required for troubleshooting the order wire equipment. The multiplex equipment may or may not be connected.

b. Order Wire Troubleshooting Chart

| Symptom   | Probable cause  | Checks and corrective measures  |
|---|---|---|
| 1. Power lamp does not light when receiver AC POWER switch is set to ON.  | Defective relay 9A1K1 (fig. 3-49).                              | Check for 26 vdc across the relay coil. if not present, check wiring between relay and 1RE1PS1 (FO-4-28 and FO-4-78). If voltage present, check that relay is operated. If not operated, higher category of maintenance is required. If relay is operated, check the wiring between the relay and POWER lamp (FO-4-78). |
| 2. CALL lamp does not light, buzzer sounds; receiver meter indication is normal with switch at OW.                  | a. Defective wiring.<br>b. Defective switch 9A2S2 (fig. 3-49) . | a. Check wiring between pins 5 and 6 of 9A2J2 (FO-4-78) .<br>b. If normal indication is obtained in a above, higher category of maintenance is required.  |
| 3. CALL lamp lights; buzzer does not sound; receiver meter indication is normal with switch at OW.                  | a. Defective wiring<br>b. Defective switch 9A2S2 (fig. 3-49).   | a. Check wiring between pins 5 and 3 9A2J2 (FO-4-78).<br>b. If normal indication is obtained in a above, higher category of maintenance is required.  |
| 4. 1600 Hz signaling tone is not heard in handset receiver when the RING button is pressed. No voice communication. | a. Defective handset.<br>b. Defective relay 9A1K2 (fig. 3-49).  | a. Measure the resistance between pin of 9A1J4 (FO-4-78) and ground. If other than 25 ohms, replace the handset.<br>b. Check for 26 v across the relay coil. If not present, check the wiring between the relay and 1RE1PS1 (FO-4-28 and FO-4-78). If voltage is present, check   |



bl. Order Wire Troubleshooting Chart - Continued .

| Symptom  | Probable cause   | Checks and corrective measures  |
|--|--|---|
|  |  | that the relay is operated. If not operated, higher category of maintenance is required. If relay is operated check interunit wiring (FO-4-78). |
|  | c. Defective amplifier assembly 9A4 or telephone signal converter 9A3. | c. Check per para 3-43 for test procedures. If abnormal indications are obtained, higher category of maintenance is required.                   |
| 5. 1600 Hz signaling tone is not heard in the handset receiver when the RING button is pressed. Voice communication is normal .  | Defective switch 9A2S1 (fig. 3-49) .                                   | Check switch 9A2S1. If defective, higher category of maintenance is required. If normal, check interunit wiring (FO-4-78).                      |
| 6. CALL lamp does not light and buzzer does not sound when the distant station RING button is pressed. Receiver meter indication is normal with switch at OW. Voice communication is normal. | Defective wiring.  | Check for continuity from terminal E2 of 9A2A1 (FO-4-78) to pin D of 9A1J3.   |

3-8. Power Supply 5TR1P1

a. Test Equipment Required

| Equipment  | Common Name                              |
|--|--|
| Multimeter, Digital, AN/USM-486<br>Voltmeter, Electronic, ME-30A/U<br>Cable Assembly Special Purpose, Electrical | Digital Multimeter<br>VTVM<br>CX-12101/U |

b. Operational Checks.

- (1) Remove power supply 5TR1PS1 as described in paragraph 3-50.
- (2) Connect power supply 5TR1PS1 to radio transmitter 5TR1 using the CMC 456-926 cable between connectors 5TR1PS1P1 and J3 (X5TR1PS1P1) (fig. 3-1).
- (3) Set the transmitter AC POWER switch to ON/RESET.
- (4) Using the multimeter, measure the dc voltages at the test points on voltage regulator amplifier 5TR1PS1AR1, as shown in the chart below:

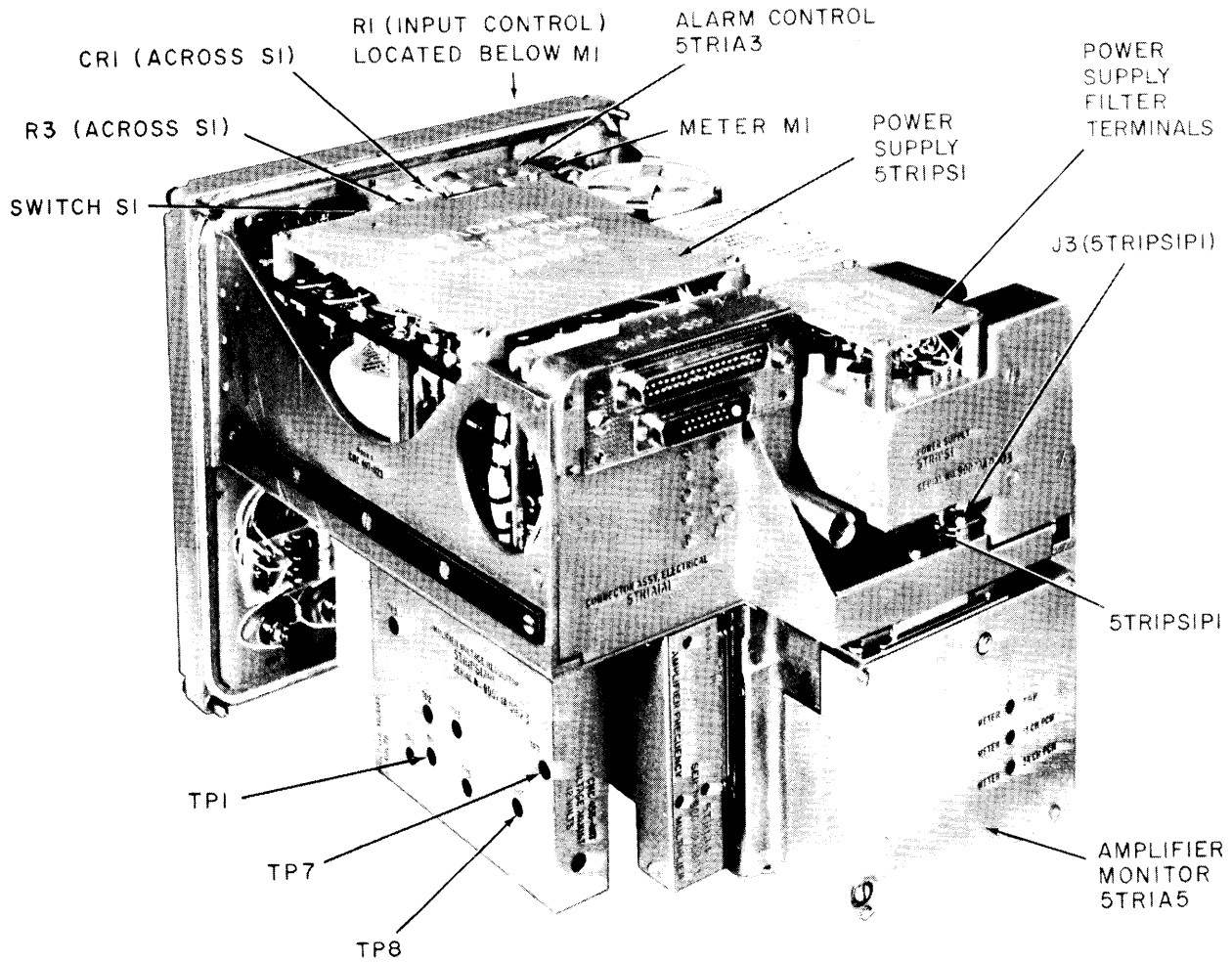
| Test point        | Volts  |
|-------------------|--------|
| TP1(-) and TP7(+) | 28±0.2 |
| TP1(-) and TP8(+) | 12±0.1 |

WARNING

Be extremely careful when working with the safety cover removed, 600 volts dc is exposed.

- (5) Carefully remove the smaller of the two red safety covers labeled DANGER 600 V WHEN COVER REMOVED.
- (6) Using the multimeter, measure the dc voltages at the filters, as shown in the following chart. Filter terminals are shown in figure 3-2.

| Filter terminals | volts    |
|------------------|----------|
| 16(-) and 17(+)  | 26±5     |
| 22(-) and 23(+)  | 6.8±0.4  |
| 20(-) and 21(+)  | 6.8±0.4  |
| GRD and 24(+)    | 630±31.5 |



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Figure 3-1. Radio Transmitter 5TR1, Top Rear View.

(7) Using the VTVM, measure the 400 Hz ac voltages at the filters, as shown in the chart below.

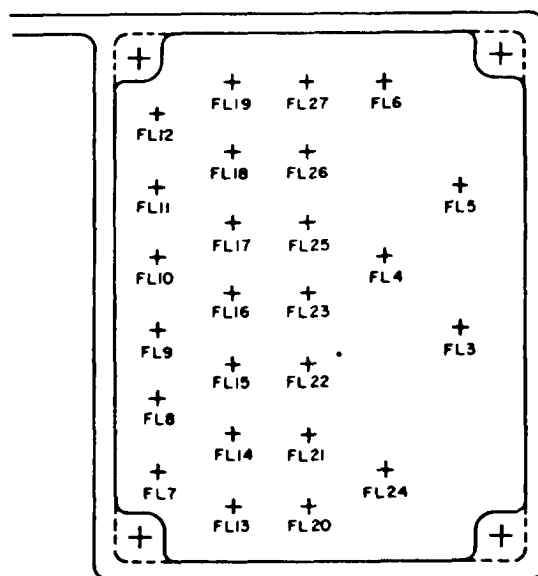
| Filters | volts   |
|---------|---------|
| 5 and 6 | 140 ± 5 |
| 7 and 8 | 29±5    |
| 8 and 9 | 29±5    |

(8) Set the transmitter AC POWER switch to OFF. Reinstall the red safety cover. Replace 5TR1PS1 if indications in (4), (6) or (7) above are incorrect. Refer to paragraph 3-50 for replacement procedures.

3-9. Amplifier-Monitor 5TR1A5

a. Test Equipment Required.

| Equipment                                       | Common name           |
|---|-----------------------|
| Generator, Signal, SG-1171/U                    | Wide range oscillator |
| Oscilloscope, Dual Trace, OS-261C(V)/U          | Oscilloscope          |
| Adapter-Connector UG-274/U                      |                       |
| Cable Assembly, Radio Frequency<br>(2 required) | CG-409H/U (4.5 ft)    |
| Cable Assembly, Special Purpose,<br>Electrical  | CX-12092/U            |



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Figure 3-2. Power Supply 5TR1PS1, Filter Terminals.

a. Test Equipment Required - Continued.

| Equipment                                   | Common name |
|---|-------------|
| Cable Assembly, Special Purpose, Electrical | CX-12093/U  |
| Cable Assembly, Special Purpose Electrical  | CX-12096/U  |

b. Operational Checks.

- (1) Remove amplifier-monitor 5TR1A5 as described in chapter 6 of TM 11-5820-540-12.
- (2) Connect amplifier-monitor 5TR1A5 to radio transmitter 5TR1, using the CX-12096/U cable between connectors 5TR1A5P1 and J2 (X5TR1A5P1) (fig. 3-3).

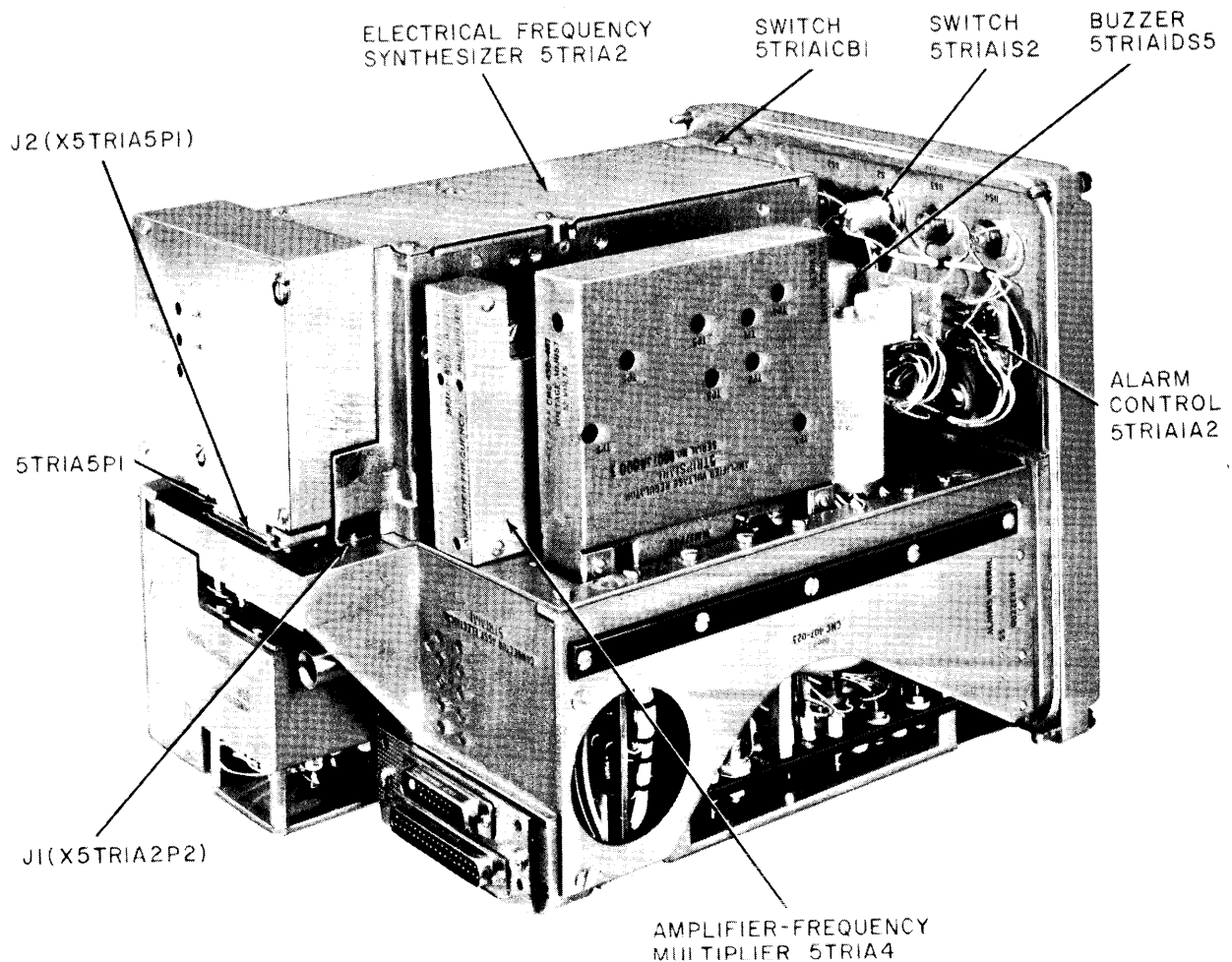
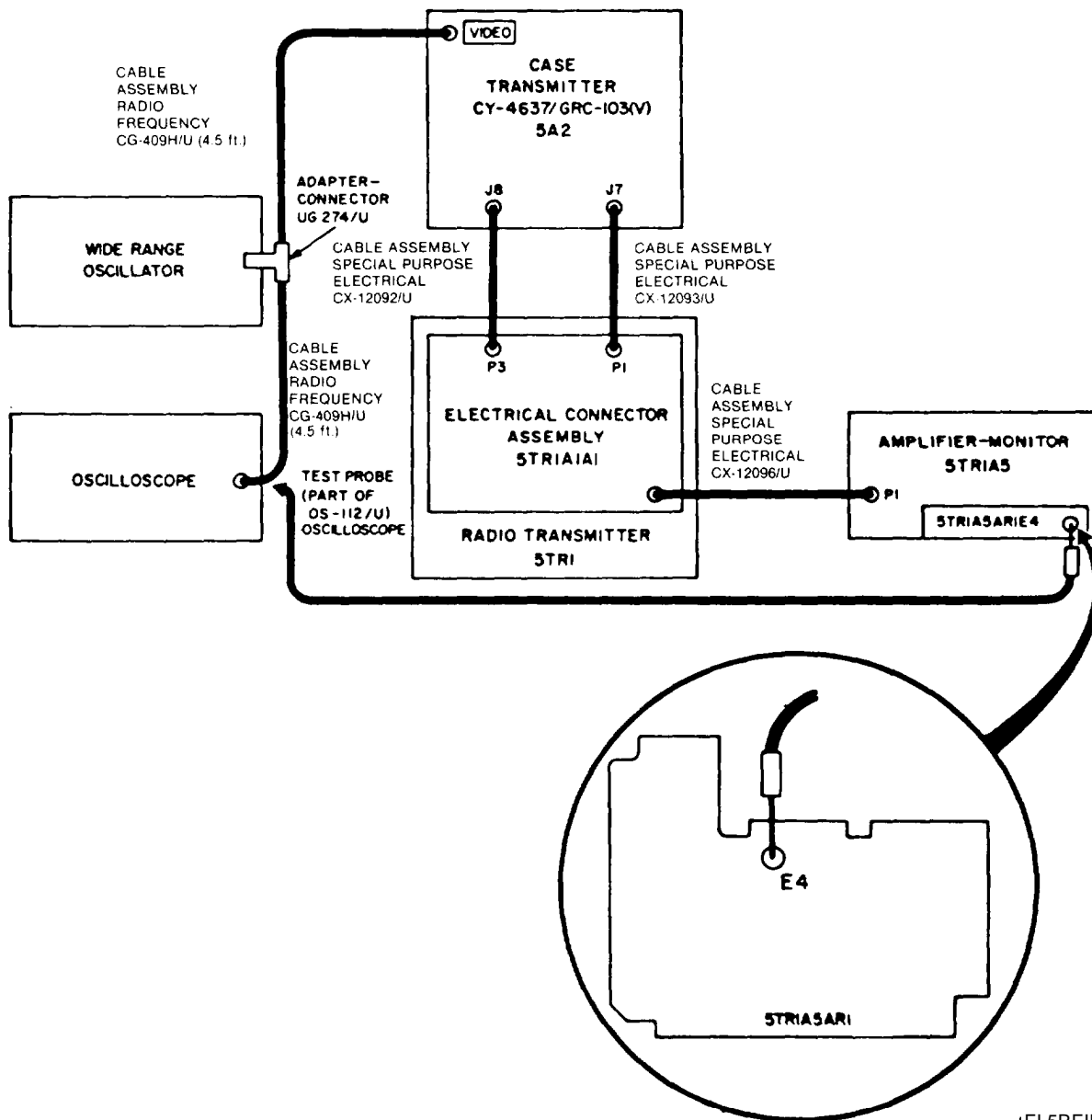


Figure 3-3. Radio Transmitter 5TR1, Bottom Rear View.

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- (3) Loosen the four screws securing 5TR1A5 cover plate. Remove the cover plate.
- (4) Connect the test equipment as shown in figure 3-4.
- (5) Set the frequency of the wide range oscillator to 10 kHz and adjust the amplitude to 2 volts peak-to-peak as measured on the oscilloscope. Disconnect the oscilloscope.
- (6) Set the transmitter rf head XMTR CHANNEL control to channel 179.
- (7) Set the transmitter AC POWER switch to ON/RESET.



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Figure 3-4. Amplifier Monitor 5TR1A5 Operational Check, Test Setup.

- (8) Set the transmitter meter switch to 12 CH PCM, 24 CH PCM, and FDM in turn. In each meter switch position, adjust the transmitter INPUT control for a 50 percent of full scale deflection on the transmitter meter.
- (9) In each meter switch position of (8) above, measure the voltage at terminal E4 of video amplifier 5TR1A5AR1 board, using the oscilloscope probe. The voltages should be as shown in the chart below.

| Meter switch position | Voltage at E4 (volts) |
|-----------------------|-----------------------|
| 12 CH PCM             | 0.18 (peak)           |
| 24 CH PCM             | 0.3 (peak)            |
| FDM                   | 0.075 (peak)          |

- (10) Set the transmitter rf head XMTR CHANNEL control to channel 180.
- (11) Repeat (8) above.
- (12) Repeat (9) above. The voltages should be as shown in the chart below.

| Meter switch position | Voltage at E4 (volts) |
|-----------------------|-----------------------|
| 12 CH PCM             | 0.12 (peak)           |
| 24 CH PCM             | 0.2 (peak)            |
| FDM                   | 0.05 (peak)           |

- (13) Set the AC POWER switch to OFF. Reinstall the 5TR1A5 cover plate. Replace 5TR1A5 if the indications in (9) or (12) above are abnormal. Refer to chapter 6 of TM 11-5820-540-12 for replacement procedures.

3-10. Electrical Frequency Synthesizer 5TR1A2

NOTE

The troubleshooting of electrical frequency synthesizer 5TR1A2 also involves checking control-indicator 6A3. If abnormal indications are obtained in any of the following tests, troubleshoot control-indicator 6A3 as described in paragraph 3-13 before replacing electrical frequency synthesizer 5TR1A2.

a. Test Equipment Required.

| Equipment                              | Common name           |
|--|-----------------------|
| Generator, Signal, SG-1171/U           | Wide range oscillator |
| Oscilloscope, Dual Trace, OS-261C(V)/U | Oscilloscope          |

a. Test Equipment Required - Continued

| Equipment  | Common Name        |
|--|--------------------|
| Meter, Modulation, ME-57A/U                            | Deviation Meter    |
| Counter, Electronic Digital Readout AN/USM-459         | Counter            |
| Wattmeter AN/URM-98                                    | Power Meter        |
| Attenuator, fixed, 10 db, Microlab AD-10 MN            |                    |
| Load, 51 ohms $\pm 2\%$ , BNC male termination 335-053 |                    |
| Cable Assembly, Radio Frequency (3 required)           | CG-409H/U (4.5 ft) |
| Cable Assembly, Special Purpose, Electrical            | CX-12092/U         |
| Cable Assembly, Special Purpose, Electrical            | CX-12093/U         |
| Cable Assembly, Special Purpose, Electrical            | cX-12100/U         |
| Cable Assembly, Radio Frequency                        | CG-3580/U (6 in.)  |
| Cable Assembly, Radio Frequency                        | CG-3570/U (6 in.)  |
| Adapter-Connector UG-29B/U                             |                    |
| Adapter-Connector UG-201A/U (2 required)               |                    |
| Adapter-Connector UG-274/U (2 required)                |                    |

b. Test Setup.

- (1) Remove electrical frequency synthesizer 5TR1A2 as described in paragraph 3-48.
- (2) Remove amplifier-frequency multiplier 5TR1A4 from 5TR1A2 as described in paragraph 3-49.
- (3) Connect electrical frequency synthesizer 5TR1A2 to radio transmitter 5TR1 using the CX-12100/U cable between connectors 5TR1A2P2 and J1 (X5TR1A2P2) (fig. 3-3).

c. Frequency Measurements.

- (1) Connect the test equipment as shown in A, figure 3-5.
- (2) Set the AC POWER switch to ON/RESET.
- (3) Using the XMTR CHANNEL control on the transmitter rf head, sequentially select the channels indicated in the chart below and read the corresponding frequencies on the counter.

| Channel | Frequency (MHz) | Tolerance (Hz) |
|---------|-----------------|----------------|
| 40      | 55.000          | $\pm 550.0$    |
| 111     | 63.875          | $\pm 630.0$    |
| 112     | 64.000          | $\pm 640.0$    |
| 179     | 72.375          | $\pm 720.0$    |
| 180     | 48.333          | $\pm 480.0$    |
| 410     | 67.500          | $\pm 675.0$    |



d. Output Power Measurement.

- (1) Disconnect the counter from the test setup of c above.
- (2) Connect the power meter probe to the 10 db attenuator as shown in B figure 3-5.
- (3) Measure the power output at channels 170 and 180. Set the channels using the XMTR CHANNEL control. The power output indication on the power meter as shown in the chart below is for modulator-oscillator 5TR1A2A2, Part No. CMC 456-260.

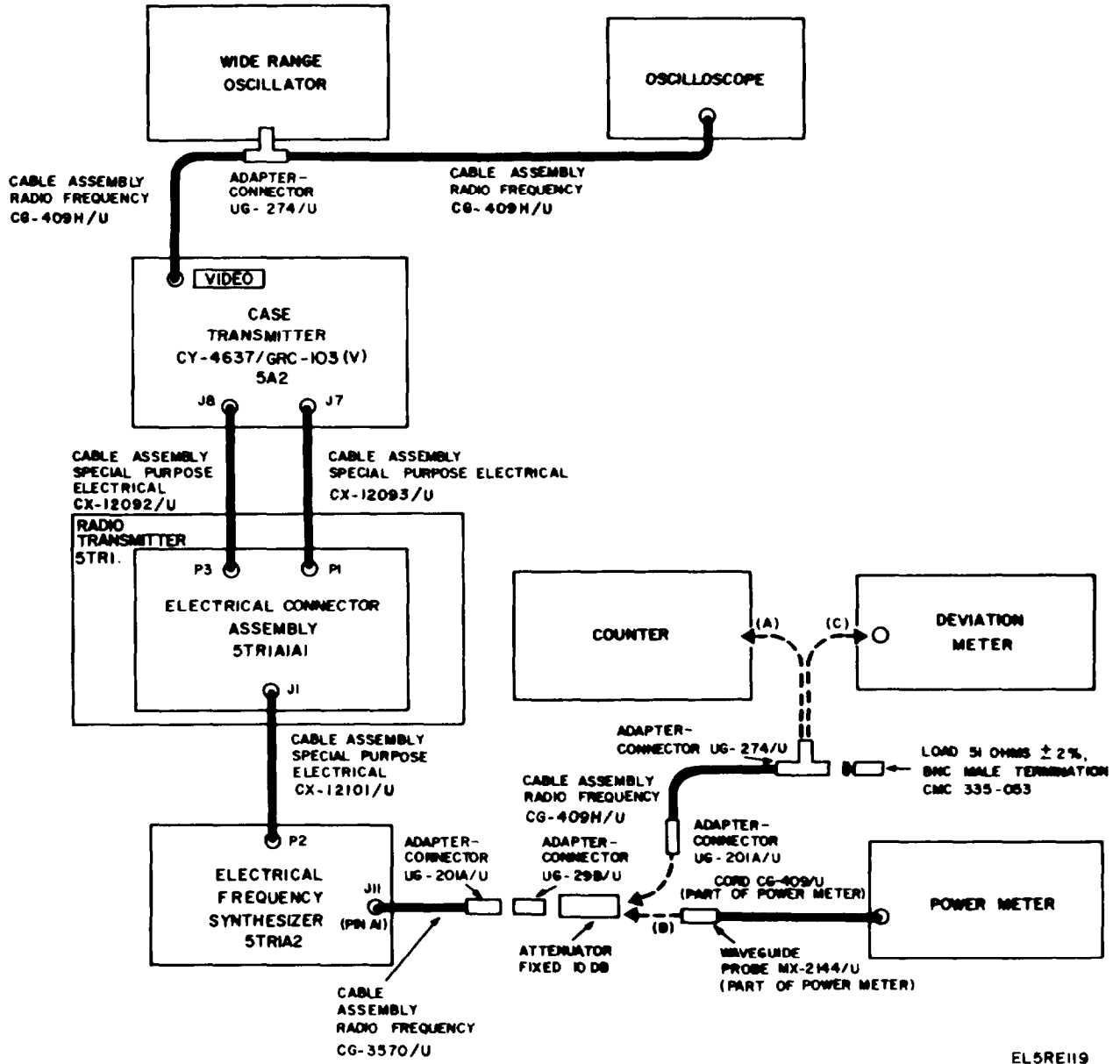


Figure 3-5. Electrical Frequency Synthesizer 5TR1A2 Operational Check, Test Setup.

| Channel | Power output |
|---------|--------------|
| 179     | 12 dbm±1 db  |
| 180     | 16 dbm±1 db  |

NOTE

When electrical frequency synthesizer is equipped with modulator-oscillator Part No. CMC 220-800159-000, power output should be +14 dbm±1.5 db at channels 179 and 180.

e. Frequency Deviation Measurement.

- (1) Disconnect the power meter from the test setup of d above.
- (2) Connect the deviation mixer to the 10 db attenuator as shown in C figure 3-
- (3) Set the frequency of the wide range oscillator to 10 kHz and adjust the amplitude to 2 volts peak-to-peak as measured on the oscilloscope.
- (4) Set the transmitter meter switch to 24 CH PCM and adjust the INPUT control for a 50 percent of full scale deflection of the meter.
- (5) Measure the frequency deviation at channels 179 and 180. Set the channels using the XMTR CHANNEL control. The frequency deviation indication on the deviation meter should be as shown in the chart below.

| Channel | Frequency (kHz) |
|---------|-----------------|
| 179     | 75, +25 -13.5   |
| 180     | 50, +16.6 -9    |

f. Conclusion of Operational Checks. Set the transmitter AC POWER switch to OFF. Troubleshoot control-indicator as described in paragraph 3-13 if abnormal indications are obtained in either c, d, or e above to insure that electrical frequency synthesizer 5TR1A2 and not control-indicator 6A3 is defective. Reinstall amplifier-frequency multiplier 5TR1A4 on 5TR1A2, or on the 5TR1A2 replacement, as described in paragraph 3-49. Reinstall 5TR1A2 as described in paragraph 3-48.

## 3-11. Amplifier-Frequency Multiplier 5TR1A4

a. Test Equipment Required.

| Equipment                                     | Common Name       |
|---|-------------------|
| Test Set, Radio Frequency Power<br>AN/URM-120 | Wattmeter         |
| Adapter-Connector UG-29B/U                    |                   |
| Adapter-Connector UG-201A/U<br>(2 required)   |                   |
| Cable Assembly, Radio Frequency               | CG-3580/U (6 in.) |
| Cable Assembly, Radio Frequency               | CG-3579/U (6 in.) |
| Cable Assembly, Special Purpose<br>Electrical | CX-12094          |

b. Operational Check.

- (1) Remove the transmitter rf head from the transmitter case and remove the dust cover, as described in chapter 6 of TM 11-5820-540-12.
- (2) Connect the transmitter rf head to the transmitter case using the CX-12094/U cable.
- (3) Disconnect rf lead P2 (XA1J5) from connector J5 on electronic switch 6A1 (fig. 3-6 and fig. 3-7).
- (4) Connect P2 (XA1J5) to the wattmeter input and the wattmeter output to connector J5 of 6A1 as shown in figure 3-8.
- (5) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (6) Set the transmitter AC POWER switch to ON/RESET.
- (7) Set the XMTR CHANNEL control to channel 179. The wattmeter should indicate no less than 2.5 watts.
- (8) Set XMTR CHANNEL control to channel 180. The wattmeter should indicate no less than 2.5 watts.
- (9) Set the AC POWER switch to OFF. Replace 5TR1A4 if abnormal indications are obtained in (7) and (8) above, refer to paragraph 3-49 for replacement procedures.

## 3-12. Alarm Control 5TR1A3

**NOTE**

The operation of alarm control 5TR1A3 depends on the dc output from power monitor 6AR1A3.

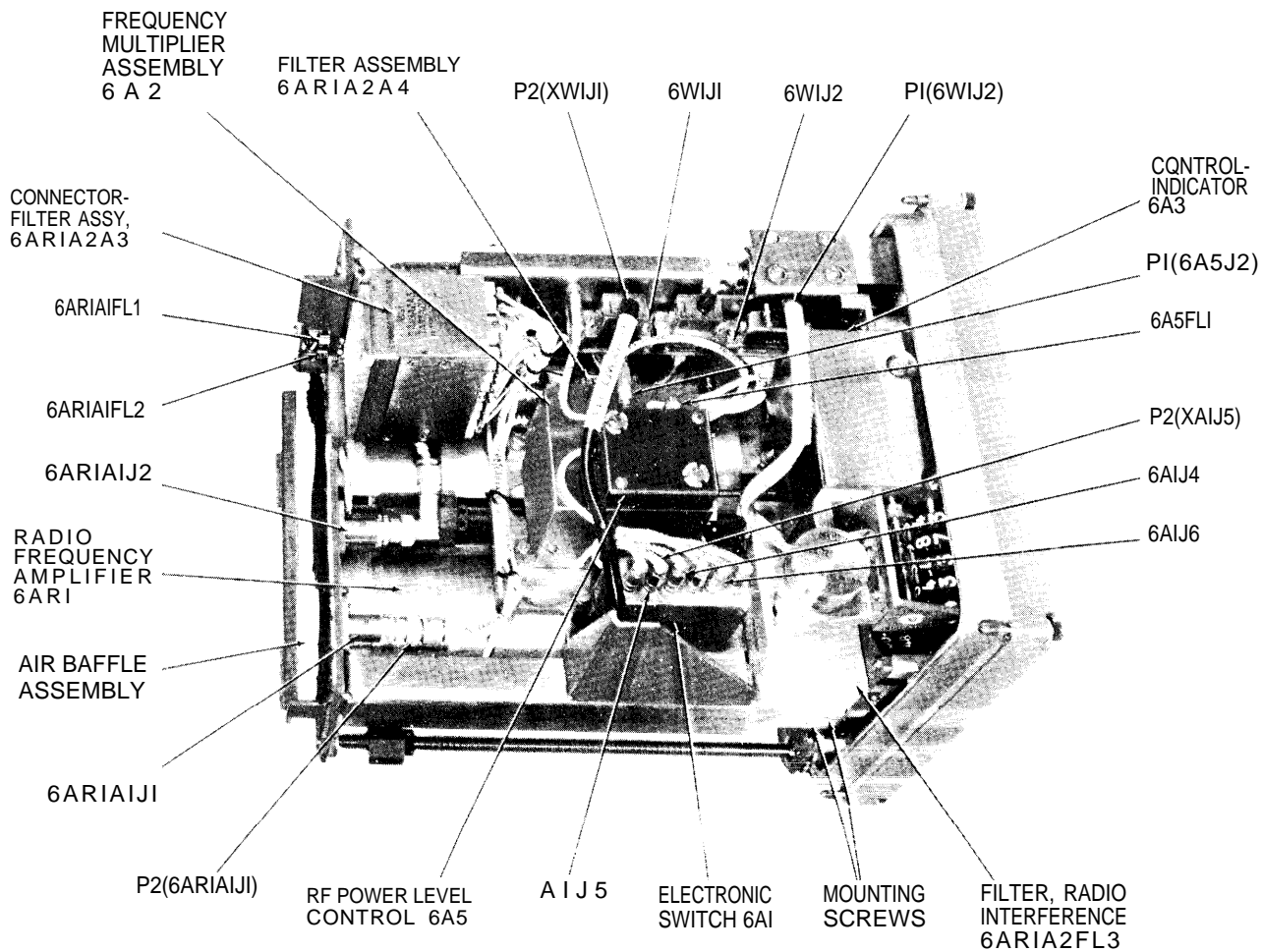
a. Test Equipment Required

| Equipment  | Common Name                    |
|--|--------------------------------|
| Multimeter, Digital AN/USM-486<br>Cable Assembly, Special Purpose,<br>Electrical | Digital Multimeter<br>CX-12103 |

1

b. Operational Check

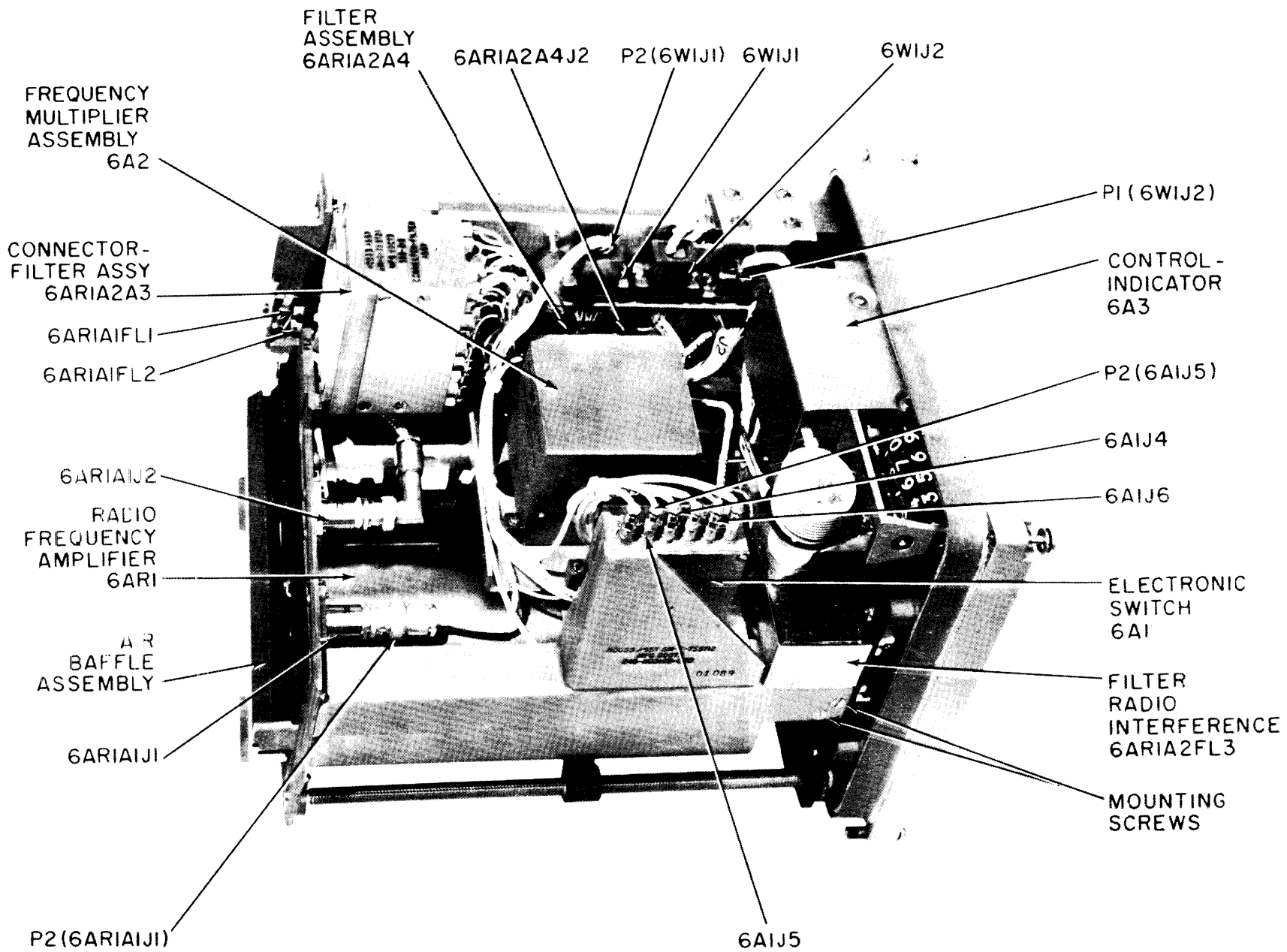
- (1) Remove alarm control 5TR1A3 as described in chapter 6 of TM 11-5820-540-12.
- (2) Connect the alarm control to radio transmitter 5TR1, using the CX-12103 cable between connectors 5TR1A3J1 and P2 (5TR1A3J1).



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Figure 3-6. Transmitter Rf Head (AM-4320/GRC-103(V)), Top View.

Figure 3-7. Transmitter Rf Head (AM-4320A/GRC-103(V) or AM-4320B/GRC-103(V)), Top View.



- (3) Remove the cover of 5TR1A3.
- (4) Set the XMTR CHANNEL and XMTR TUNE controls to channel 180.
- (5) Set the AC POWER switch to ON/RESET.
- (6) Set the meter switch to DRIVER and adjust the PWR OUT PEAK control for a maximum indication on the transmitter meter.
- (7) Set the meter switch to PWR OUT and adjust the PWR OUT PEAK control for a maximum indication on the transmitter meter.
- (8) Using the multimeter, measure the voltage at the terminals of 5TR1A3A1 (printed circuit board) as shown in the chart below.

| Terminal                       | Voltage                               |
|--------------------------------|---------------------------------------|
| E6 and ground<br>E1 and ground | Greater than 170 millivolts<br>26 vdc |

- (9) Rotate the XMTR TUNE control until the transmitter meter indicates zero. The LOW POWER lamp should light. The buzzer may sound; mute the buzzer.

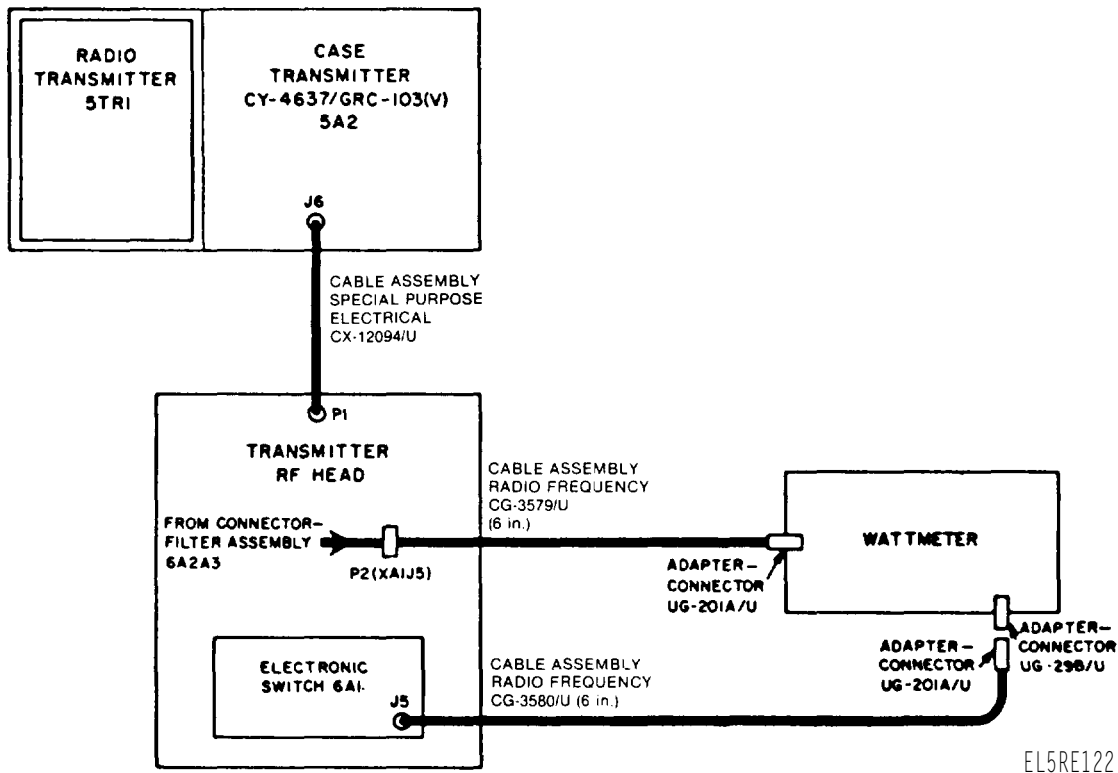


Figure 3-8. Amplifier-Frequency Multiplier 5TR1A4 Operational Check, Test Setup.

(10) Using the multimeter, measure the voltage at the terminals of 5TR1A3A1 as shown in the chart below.

| Terminal      | Voltage                  |
|---------------|--------------------------|
| E6 and ground | Less than 120 millivolts |
| E1 and ground | 0                        |

(11) Set the AC POWER switch to OFF. If abnormal indications are obtained, replace 5TR1A3 as described in chapter 6 of TM 11-5820-540-12.

3-13. Control-Indicator 6A3

**a. Test Equipment Required.**

| Equipment   | Common Name                      |
|---|----------------------------------|
| Multimeter, Digital, AN/USM-486<br>Cable Assembly, Special Purpose,<br>Electrical | Digital Multimeter<br>CX-12098/U |

**b. Operational Checks.**

- (1) Loosen the two screws securing plug P1(6W1J2) to chassis connector 6W1J2  
Disconnect P1 (6W1J2) from 6W1J2.
- (2) Set the XMTR CHANNEL control to channel 112.
- (3) Using the multimeter, check for correct resistance between the following pins of P1(6W1J2) as shown in the chart below.

| Pins      | Resistance |
|-----------|------------|
| 3 and 14  | Infinity   |
| 4 and 14  | Infinity   |
| 5 and 14  | Infinity   |
| 6 and 14  | Infinity   |
| 7 and 14  | Infinity   |
| 8 and 14  | Infinity   |
| 9 and 14  | Infinity   |
| 10 and 14 | Infinity   |
| 11 and 14 | Infinity   |
| 12 and 14 | Zero       |

(4) Set the XMTR CHANNEL control to channel 111.

(5) Using the Multimeter, check for correct resistance between the following pins of P1(6W1J2) as shown in the chart below.

| Pins      | Resistance |
|-----------|------------|
| 3 and 14  | Zero       |
| 4 and 14  | Zero       |
| 5 and 14  | Zero       |
| 6 and 14  | Zero       |
| J and 14  | Zero       |
| 8 and 14  | Zero       |
| 9 and 14  | Zero       |
| 10 and 14 | Zero       |
| 11 and 14 | Zero       |
| 12 and 14 | Infinity   |

(6) Remove control-Indicator 6A3 from the transmitter rf head as described in chapter 6 of TM 11-5820-540-12.

(7) Connect plug PI (6W1J2) to chassis connector 6W1J2, using the CX-12098/U cable.

(8) Remove the four screws securing the control-indicator cover and remove the cover.

(9) Set the AC POWER switch to ON/RESET.

(10) Set control-indicator 6A3 to channel 179.

(11) Using the multimeter, check the voltage at terminal E12 on command signal decoder 6A3A2. The multimeter should indicate 0 volt.

(12) Set control-indicator 6A3 to channel 180.

(13) Using the multimeter, check the voltage at terminal E12 on 6A3A2. The indication should be +26 volts dc.

(14) Set the AC POWER switch to OFF. Reinstall the control-indicator cover. If abnormal indications are obtained in either (3), (5) or (13) above, replace control-indicator 6A3. Refer to chapter 6 of TM 11-5820-540-12 for replacement procedures.

### 3-14. Electronic Switch 6A1

#### a. Test Equipment Required.

| Equipment                       | Common name        |
|---------------------------------|--------------------|
| Multimeter, Digital, AN/USM-486 | Digital Multimeter |



a. Test Equipment Required - Continued.

| Equipment   | Common Name                   |
|---|-------------------------------|
| Test Set, Radio Frequency Power AN/URM-120            | Wattmeter                     |
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter, Thermistor Mount |
| Attenuator, Fixed 20 dB CN-1287/U                     | 20 dB attenuator              |
| Adapter-Connector UG-201A/U (2 required)              |                               |
| Adapter-Connector UG-29B/U (2 required)               |                               |
| Cable Assembly, Special Purpose, Electrical           | CX-12094                      |
| Cable Assembly, Radio Frequency                       | CG-3579/U (6 in.)             |
| Cable Assembly, Radio Frequency                       | CG-3580/U (6 In.)             |

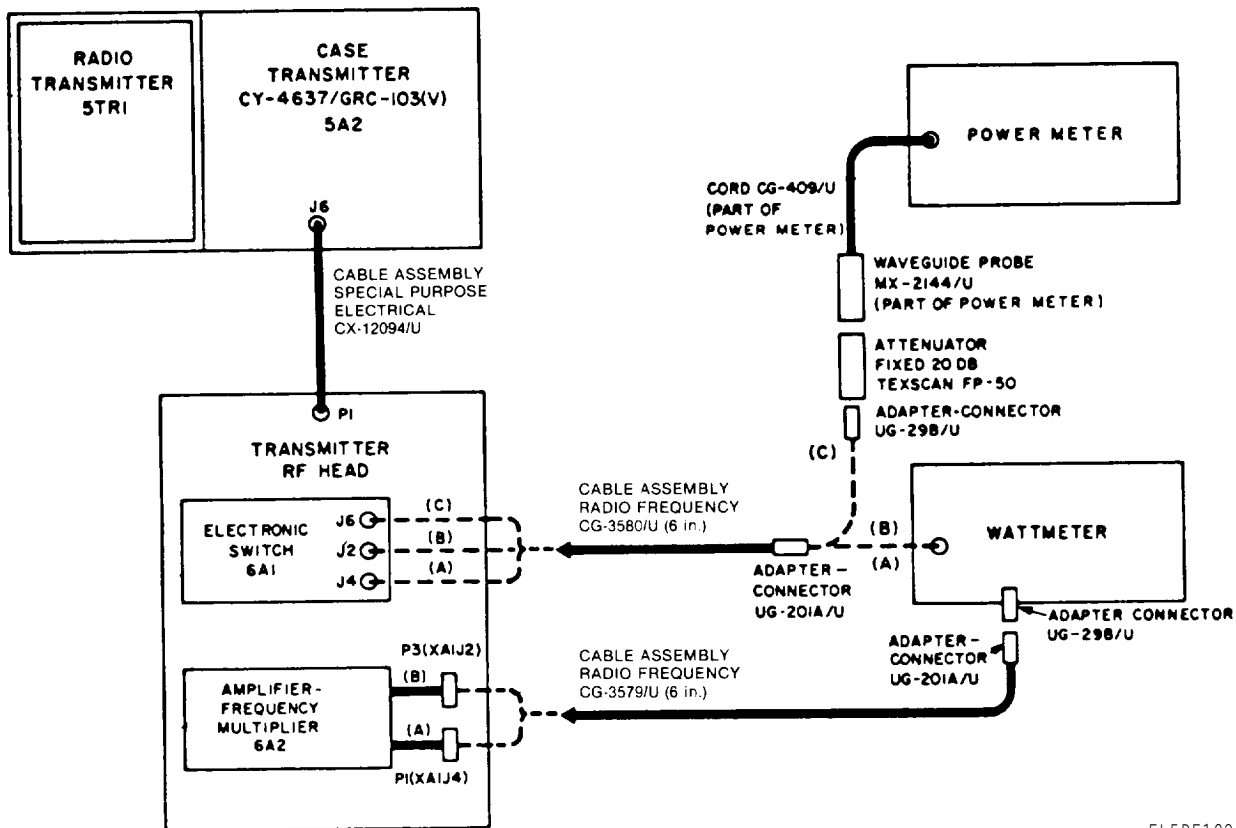
b. Operational Checks.

- (1) Loosen the two screws that secure plug P2 (XW1J1) to chassis connector 6W1J1 (fig. 3-6). Disconnect plug P2 (XW1J1) from connector 6W1J1.
- (2) Set the AC POWER switch to ON/RESET.
- (3) Set the XMTR CHANNEL control to channel 179.
- (4) Using the multimeter, check the voltage between pin 6 (-) and pin 7 (+) of 6W1J1. The multimeter should indicate 26 volts.
- (5) Set the XMTR CHANNEL control to channel 180.
- (6) Again check the voltage between pin 6 (-) and pin 7 (+) of 6W1J1. The multimeter should indicate 0 volt.
- (7) Check between the remaining pins of 6W1J1 as shown in the chart below.

| Pins (dc        | Voltage |
|-----------------|---------|
| 3 (+) and 1 (-) | +26     |
| 3 (+) and 5 (-) | +26     |
| 7 (+) and 5 (-) | +26     |

- (8) Set the AC POWER switch to OFF.
- (9) Reconnect plug P2 (XW1J1) to connector 6W1J1.
- (10) Disconnect plug P1 (XA1J4) from connector J4 on 6A1 (fig. 3-6).
- (11) Connect the test equipment as shown in A, figure 3-9.

- (12) Insert the 10 to 500 watt probe into the wattmeter.
- (13) Set the XMTR CHANNEL control to channel 179.
- (14) Set the transmitter AC POWER switch to ON/RESET. The wattmeter should indicate no less than 2.5 watts.
- (15) Set the AC POWER switch to OFF.
- (16) Reconnect plug P1 (XA1J4) to connector 6A1J4.
- (17) Disconnect plug P3 (XA1J12) from connector 6A1J2.
- (18) Connect the test equipment as shown in B, figure 3-9.
- (19) Set the XMTR CHANNEL control to channel 180.
- (20) Set the AC POWER switch to ON/RESET. The wattmeter should indicate no less than 2.5 watts.
- (21) Set the AC POWER switch to OFF.
- (22) Reconnect plug P3 (XA1J2) to connector 6A1J2.



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Figure 3-9. Electronic Switch 6A1 Operational Check, Test Setup.

- (23) Disconnect plug P1 (XA1J6) from connector 6A1J6.
- (24) Connect the test equipment as shown in C, figure 3-9.
- (25) Set the XMTR CHANNEL and XMTR TUNE controls to channel 179.
- (26) Set the AC POWER switch to ON/RESET. The level at 6A1J6 should not be less than +26.4 dBm (power meter reading of +6.4 dBm).
- (27) Set the XMTR CHANNEL and XMTR TUNE controls to channel 180. The level at 6A1J6 should not be less than +26.4 dBm (power meter reading of +6.4 dBm).
- (28) Set the AC POWER switch to OFF. If abnormal indications are obtained in either (4), (6), or (7) above, check control-indicator 6A3 (para 3-13). If abnormal indications are obtained in (14) and (20) above, check frequency multiplier assembly 6A2 (paragraph 3-15) before changing electronic switch 6A1. Replace electronic switch 6A1 if remaining requirements are not met. Refer to chapter 6 of TM 11-5820-540-12 for replacement procedures.

3-15. Frequency Multiplier Assembly 6A2

a. Test Equipment Required.

| Equipment   | Common Name                  |
|---|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Attenuator, Fixed, 20 dB, CN-1287/U                   | 20 dB attenuator             |
| Cable Assembly, Special Purpose, Electrical           | CX-12094/U                   |
| Cable Assembly, Radio Frequency                       | CG-3579/U (6 In.)            |
| Adapter-Connector UG-201A/U                           |                              |
| Adapter-Connector UG-29B/U                            |                              |

b. Operational Check Text

- (1) Disconnect plug P2 (XA1J3) from connector J3 of electronic switch 6A1
- (2) Connect the test equipment as shown in A, figure 3-10.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 179.
- (4) Set the transmitter AC POWER switch to ON/RESET. The level at 6A1P2 should not be less than +26.4 dBm (power meter indication of +6.4 dBm)
- (5) Set the AC POWER switch to OFF.
- (6) Reconnect plug P2 (XA1J3) to connector 6A1J3.
- (7) Disconnect plug P4 (XA1J1) from connector 6A1J1.
- (8) Connect the test equipment as shown in B, figure 3-10.

- (9) Set the XMTR CHANNEL and XMTR TUNE controls to channel 180.
- (10) Set the AC POWER switch to ON/RESET. The level at 6A1P should not be less than +26.4 dBm (power meter indication of +6.4 dBm).
- (11) Set the AC POWER switch to OFF. Replace frequency multiplier assembly 6A2, if abnormal indications are obtained in either (4) or (10) above. Refer to paragraph 3-56 for replacement procedures.

3-16. Rf Power Level Control 6A5

NOTE

This unit is used only on Amplifier-Frequency Multiplier AM-4320/GRC-103(V).

a. Test Equipment Required.

| Equipment   | Common Name                  |
|---|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Attenuator, Fixed, 20 dB, CN-1287/U                   | 20 dB attenuator             |
| Cable Assembly, Special Purpose, Electrical           | CX-12094/U                   |
| Cable Assembly, Radio Frequency                       | CG-3580/U (6 in.)            |
| Adapter-Connector UG-201A/U                           |                              |
| Adapter-Connector UG-29B/U                            |                              |

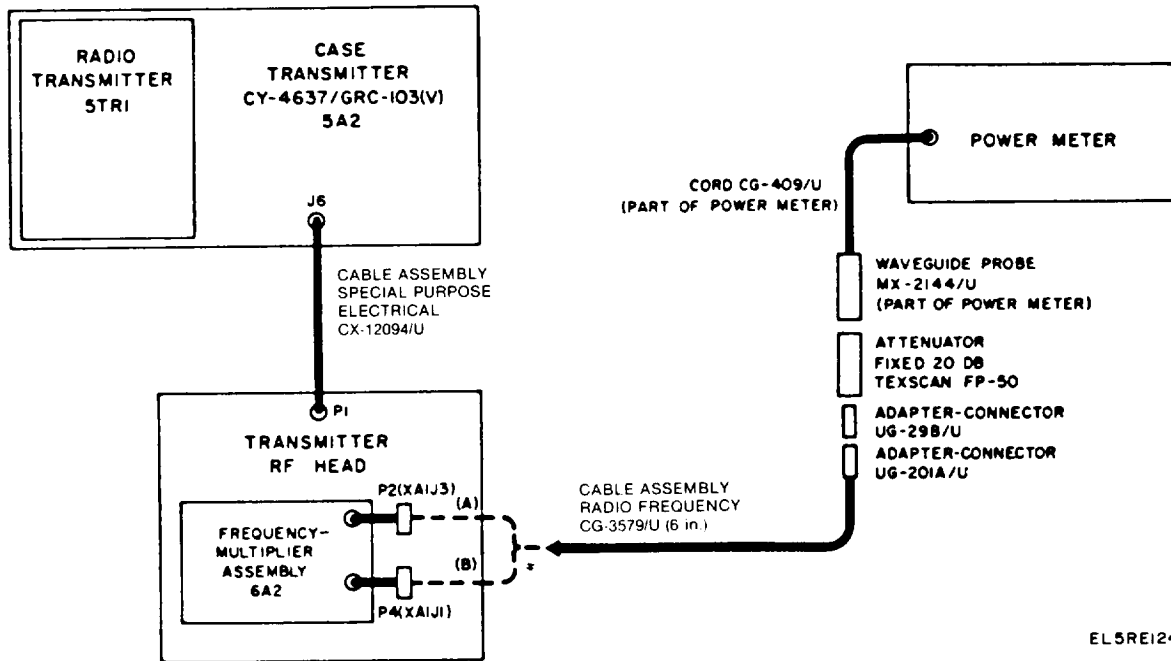


Figure 3-10. Frequency Multiplier Assembly 6A2 Operational Check, Test Setup.

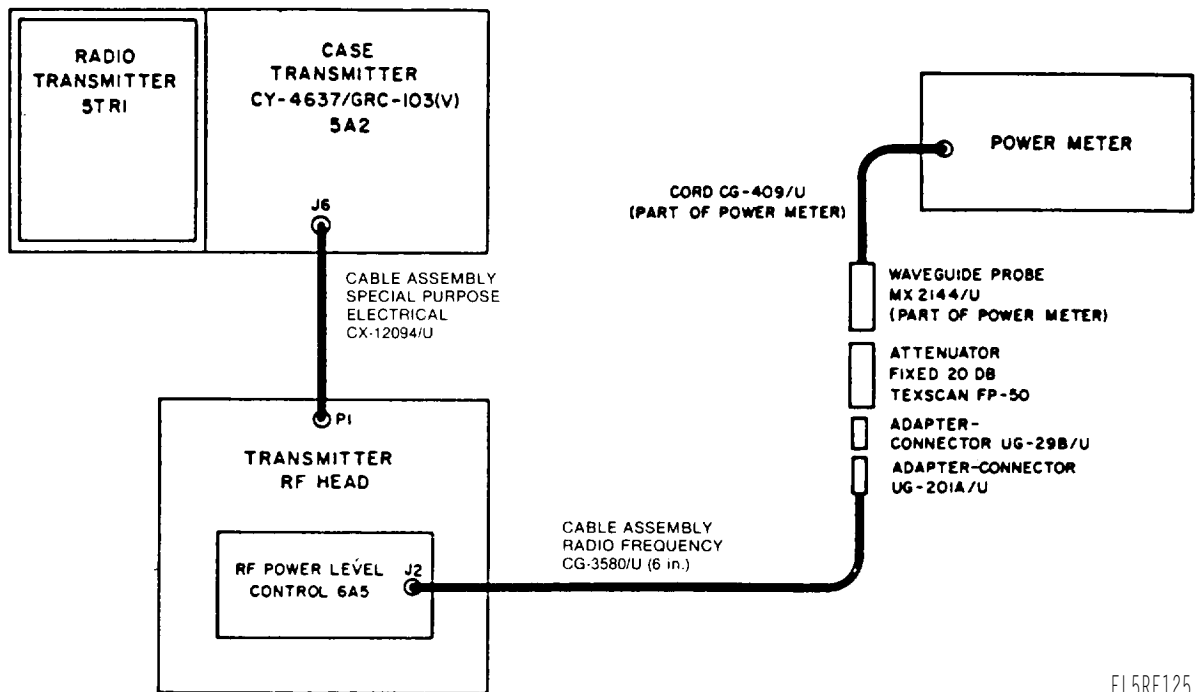
b. Operational Check.

- (1) Disconnect plug P1 (6A5J2) from connector J2 of the rf power level control 6A5 (fig. 3-6).
- (2) Connect the test equipment as shown in figure 3-11.
- (3) Set the AC POWER switch to ON/RESET. The level at 6A5J2 should be +23 dbm minimum, (power meter indication of +3 dbm).
- (4) Disconnect the power meter and reconnect P1 (6A5J2) to 6A5J2.
- (5) Using the multimeter, check the control voltage at 6A5FL1 (fig. 3-6). The multimeter should indicate 7.2 volts dc minimum (voltage increases as input power increases).
- (6) If an abnormal indication is obtained in (3) or (5) above, replace 6A5 as described in paragraph 3-57.

3-17. Filter Assembly 6AR1A2A4

a. Test Equipment Required

| Equipment   | Common Name                  |
|---|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Test Set, Radio Frequency Power AN/URM-120            | Wattmeter                    |



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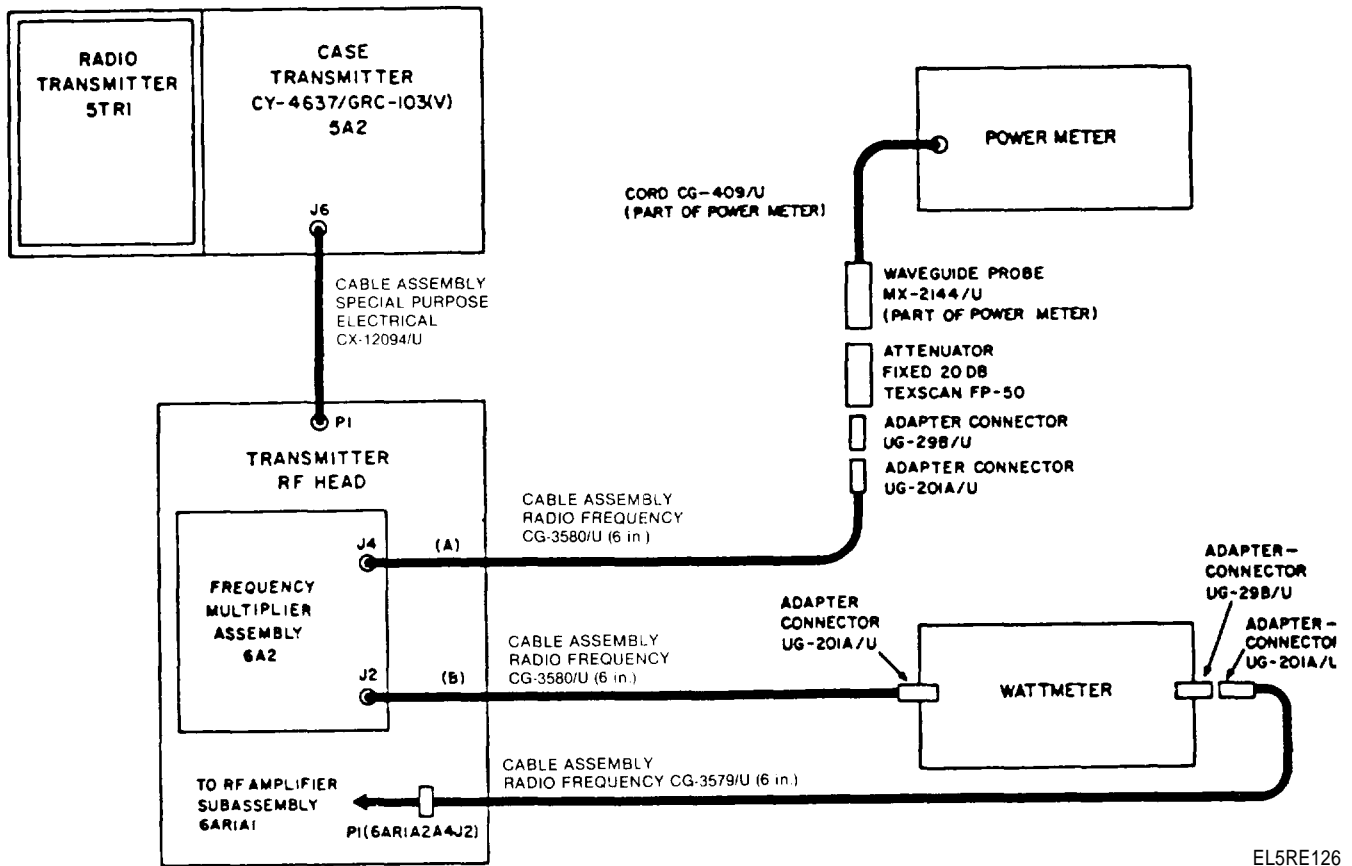
Figure 3-11. Rf Power Level Control 6A5 Operational Check, Test Setup.

a. Test Equipment Required-Continued

| Equipment                                    | Common Name       |
|--|-------------------|
| Attenuator, Fixed, 20 dB, CN-1287/U          | 20 dB attenuator  |
| Cable Assembly, Special Purpose, Electrical  | CX-12094/U        |
| Cable Assembly, Radio Frequency              | CG-3579/U (6 in.) |
| Cable Assembly, Radio Frequency (2 required) | CG-3580/U (6 in.) |
| Adapter-Connector UG-201A/U (2 required)     |                   |
| Adapter-Connector UG-29B/U (2 required)      |                   |

b. Operational Check.

- (1) Disconnect plug P2 (6AR1A2A4J4) from connector J4 on filter assembly 6AR1A-2A4 (fig. 3-6).
- (2) Connect the test equipment as shown A, figure 3-12.



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Figure 3-12. Filter Assembly 6AR1A2A4 Operational Check, Test Setup.

- (3) Set the AC POWER switch to ON/RESET. The level at 6AR1A2A4J4 should be +23 dbm minimum, (power meter indication of +3 dbm).
- (4) Set the AC POWER switch to OFF.
- (5) Reconnect plug P2 (6 AR1A2A4J4) to connector J4 on filter assembly 6AR1A2A4.
- (6) Disconnect plug P1 (6 AR1A2A4J2) from connector J2 on filter assembly 6AR1A-2A4.
- (7) Connect the test equipment as shown in B, figure 3-12.
- (8) Set the AC POWER switch to ON/RESET.
- (9) Set the transmitter meter switch to the DRIVER position and adjust the PWR OUT PEAK control for maximum indication on the transmitter meter. The wattmeter should indicate no less than 3.5 watts.
- (10) Set the AC POWER switch to off.
- (11) If abnormal indications are obtained in either (3) or (9) above, higher category of maintenance is required.

### 3-18. Radio Frequency Amplifier 6AR1

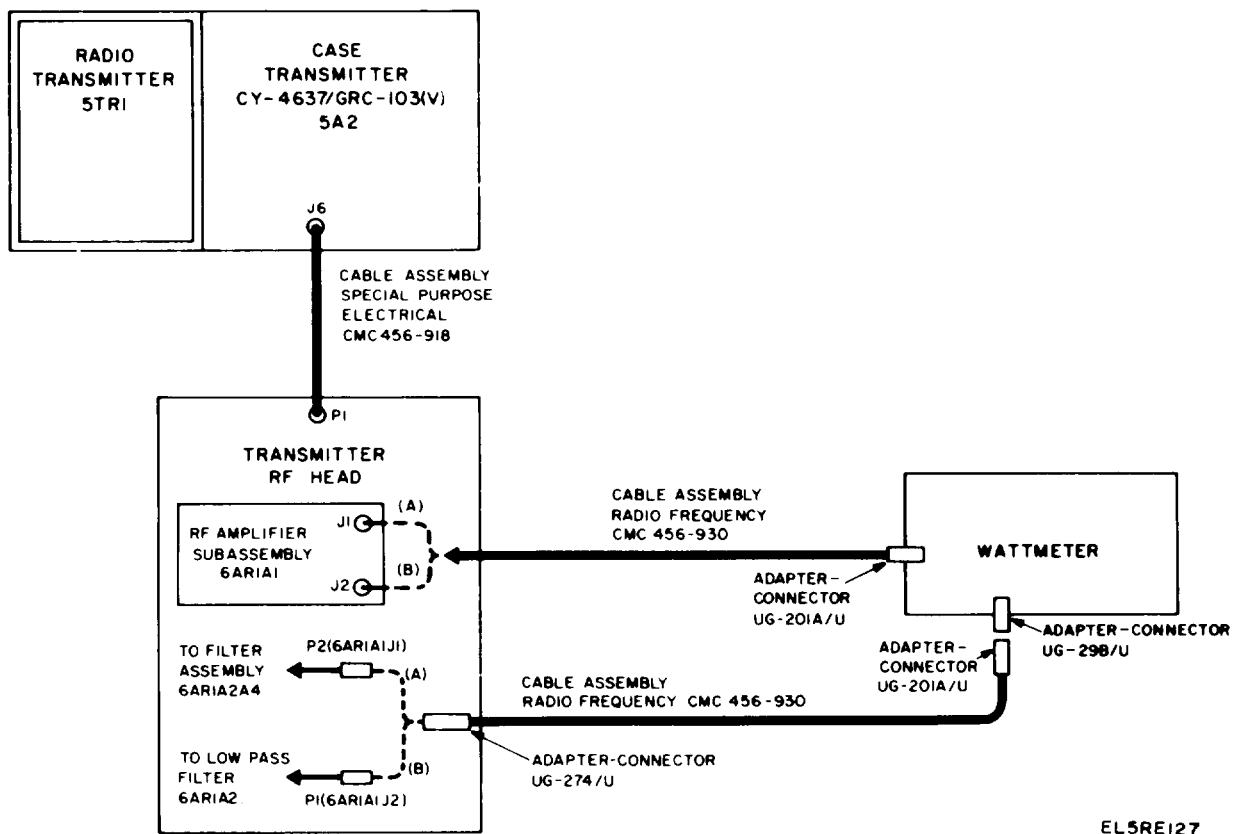
#### a. Test Equipment Required.

| Equipment                                    | Common Name         |
|--|---------------------|
| Test Set, Radio Frequency Power, AN/URM-120  | Wattmeter           |
| Cable Assembly, Special Purpose, Electrical  | CX-12094/U          |
| Cable Assembly, Radio Frequency (2 required) | CG-409H/U (4.5 ft.) |
| Adapter-Connector UG-201A/U (2 required)     |                     |
| Adapter-Connector UG-29B/U                   |                     |
| Adapter-Connector UG-274/U                   |                     |

#### b. Operational Check.

- (1) Disconnect plug P2 (6AR1A1J1) from connector J1 on radio frequency amplifier 6AR1 (fig. 3-6).
- (2) Connect the test equipment as shown in A, figure 3-13.
- (3) Insert the coupler-detector CU-755/URM-120 into the wattmeter.

- (4) Set the XMTR CHANNEL and XMTR TUNE controls to channel 180.
- (5) Set the transmitter AC POWER switch to ON/RESET and the meter switch to DRIVER.
- (6) Adjust the PWR OUT PEAK control for maximum indication on the transmitter meter. The wattmeter should indicate no less than 3.5 watts.
- (7) Set the AC POWER switch to OFF.
- (8) Reconnect plug P2 (6AR1A1J1) to connector J1 of radio frequency amplifier 6AR1.
- (9) Disconnect plug P1 (6AR1A11J2) from connector J2 on 6AR1.
- (10) Connect the test equipment as shown in B, figure 3-13.
- (11) Set the AC POWER switch to ON/RESET.
- (12) Set the meter switch to DRIVER and adjust the PWR OUT PEAK control for maximum indication on the transmitter meter.
- (13) Set the meter switch to PWR OUT and adjust the PWR CUT PEAK control for maximum indication on the meter. The wattmeter should indicate a minimum of 32 watts.



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Figure 3-13. Radio Frequency Amplifier 6AR1 Operational Check, Test Setup.



(14) Set the AC POWER switch to OFF.

(15) Replace the transmitter rf head if abnormal indications are obtained in (6) and (13) above.

3-19. Circuit Card Assembly 6AR1A2A2

a. Test Equipment Required.

| Equipment                       | Common name        |
|---------------------------------|--------------------|
| Multimeter, Digital, AN/USM-486 | Digital Multimeter |

b. Operational Check.

(1) Remove the transmitter rf head from its case.

(2) Using the multimeter, check for correct resistance between the following test points as shown in the chart below.

| Test points | Resistance (ohms $\pm 10\%$ ) |
|-------------|-------------------------------|
| E1 and E3   | 12                            |
| E1 and TP5  | 0                             |
| E1 and TP6  | 12                            |
| E1 and TP7  | 5.1                           |
| E1 and E8   | 5.1                           |
| E2 and E10  | Infinity                      |
| E4 and TP1  | 0                             |
| E4 and E9   | 200 k                         |
| E4 and E11  | 240 k                         |
| E4 and E12  | 220 k                         |
| E5 and TP2  | 0                             |
| E6 and TP3  | 0                             |
| E7 and TP4  | 0                             |

(3) If abnormal indications are obtained in (2) above, higher category of maintenance is required.

3-20. Low Pass Filter 6AR1A2FL1

a. Test Equipment Required.

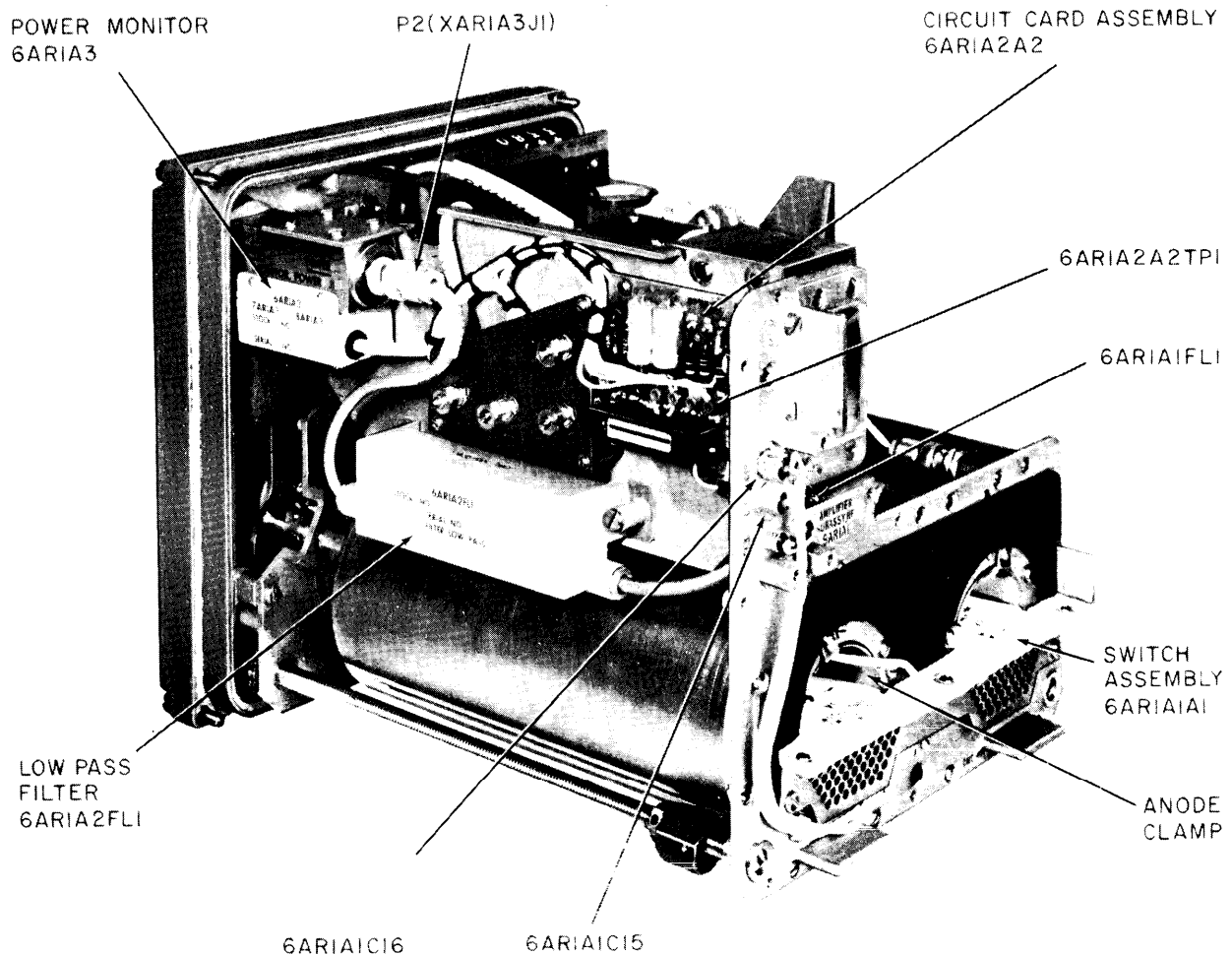
| Equipment                                   | Common name |
|---|-------------|
| Test Set, Radio Frequency Power, AN/URM-120 | Wattmeter   |

a. Test Equipment Required-Continued.

| Equipment  | Common Name         |
|--|---------------------|
| Cable Assembly, Special Purpose, Electrical                              | CX-10294/U          |
| Cable Assembly, Radio Frequency Adapter-Connector UG-201A/U (2 required) | CG-409H/U (4.5 ft.) |
| Adapter-Connector UG-29B/U   |                     |

b. Operational Check.

- (1) Disconnect plug P2 (XAR1A3J1) from connector J1 of power monitor 6AR1A3, (fig. 3-14 and fig. 3-15).



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Figure 3-14. Transmitter Rf Head (AM-4320/GRC-103(V)), Side View.

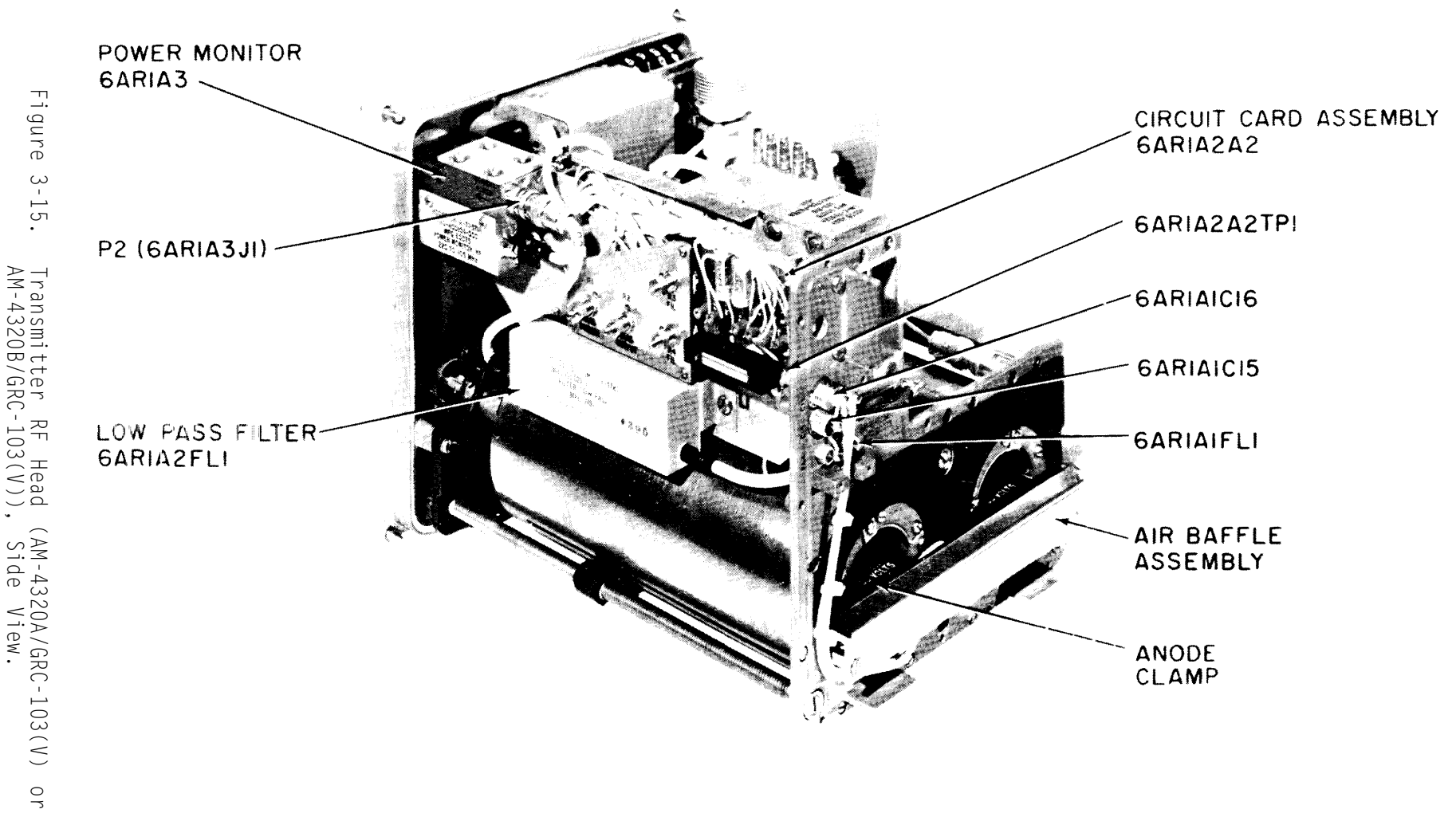


Figure 3-15. Transmitter RF Head (AM-4320A/GRC-103(V) or AM-4320B/GRC-103(V)), Side View.

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- (2) Connect the test equipment as shown in figure 3-16.
- (3) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (4) Set the XMTR CHANNEL and XMTR TUNE controls to channel 180.
- (5) Set the transmitter AC POWER switch to ON/RESET.
- (6) Set the transmitter meter switch to DRIVER and adjust the PWR OUT PEAK control for maximum indication on the transmitter meter.
- (7) Set the meter switch to PWR OUT and adjust the PWR OUT PEAK control for maximum reading on the meter. The wattmeter should indicate a minimum of 27 watts.
- (8) Set the AC POWER switch to OFF. Replace low pass filter 6AR1A2FL1, if an abnormal indication is obtained in (7) above, refer to paragraph 3-54 for replacement procedures.

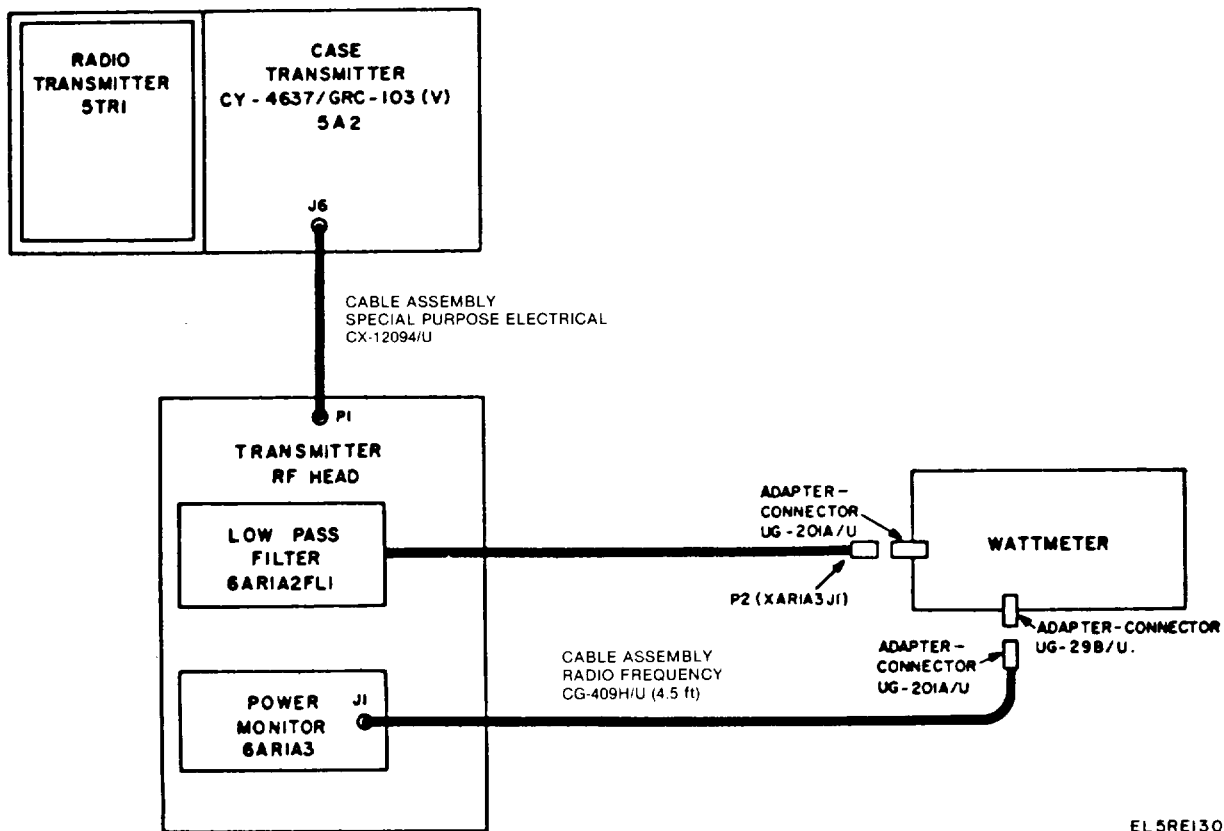


Figure 3-16. Low Pass Filter 6AR1A2FL1 Operational Check, Test Setup.

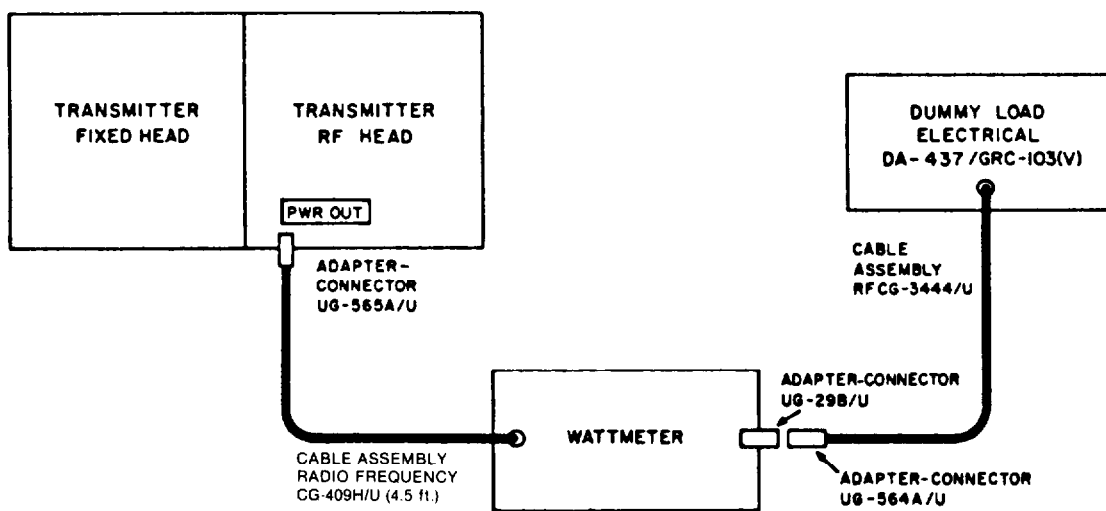
3-21. Power Monitor 6AR1A3

a. Test Equipment Required.

| Equipment   | Common Name          |
|---|----------------------|
| Test Set, Radio Frequency Power<br>AN/URM-120   | Wattmeter            |
| Cable Assembly, Radio Frequency<br>Adapter-Connector UG-565A/U<br>Adapter-Connector UG-29B/U<br>Adapter-Connector UG-564A/U | CX3-1883/U (4.5 ft.) |

b. Operational Check.

- (1) Connect the test equipment as shown in figure 3-17.
- (2) insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 180.
- (4) Set the transmitter AC POWER switch to ON/RESET.
- (5) Set the transmitter meter switch to DRIVER and adjust the PWR OUT PEAK control for maximum indication on the transmitter meter.
- (6) Set the meter switch to PWR OUT and adjust the PWR OUT PEAK control for maximum reading on the meter. The wattmeter should indicate a minimum of 25 watts.
- (7) Set the AC POWER switch to OFF. If abnormal indication is obtained, replace power monitor 6AR1A3 as described in paragraph 3-55.



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Figure 3-17. Power Monitor 6AR1A3 Operational Check, Test Setup.

3-22. Bandpass Filter Assembly 2A1A1A1 and Impedance Matching Network 2A1A1Z1

a. Test Equipment Required

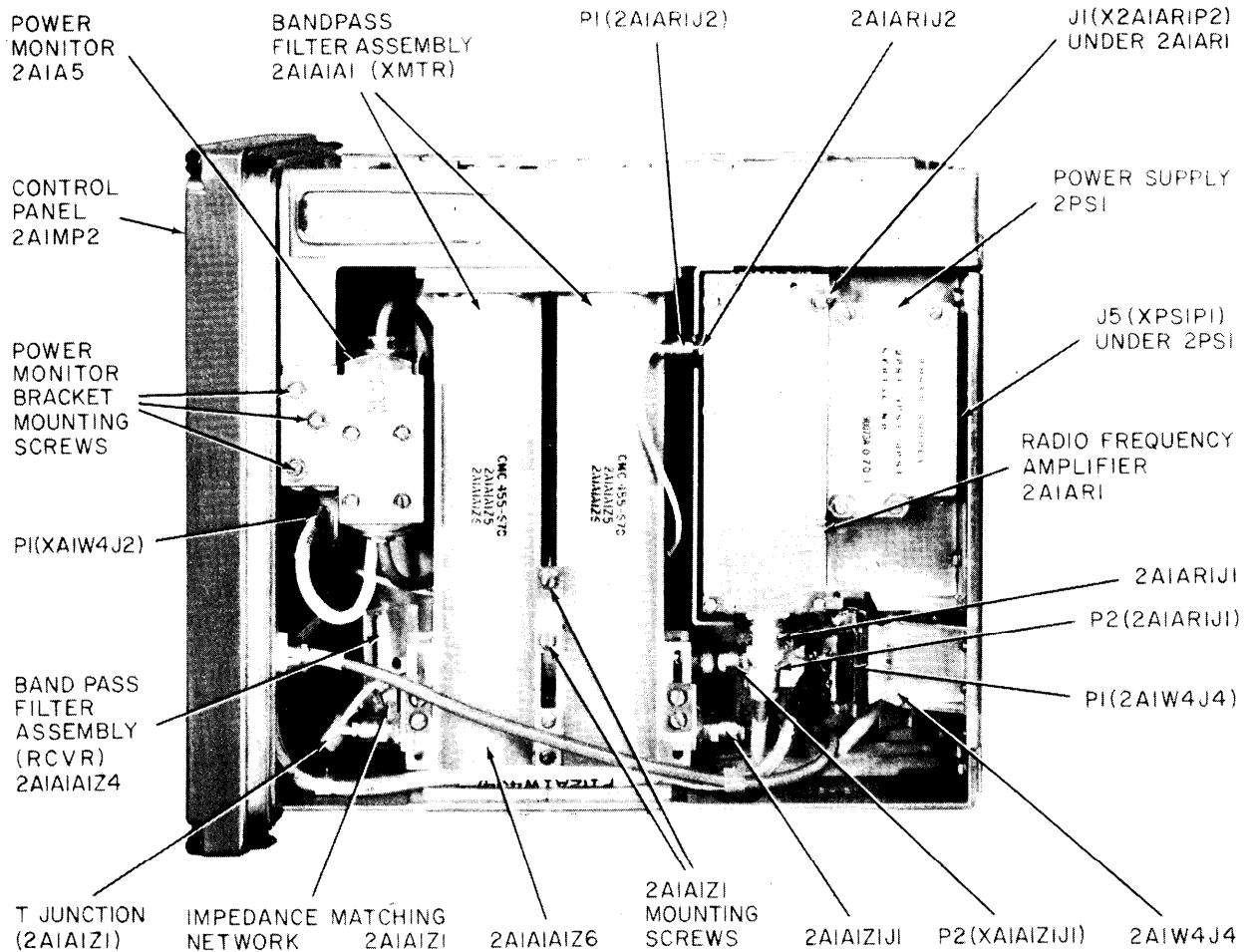
| Equipment                                       | Common Name        |
|---|--------------------|
| Test Set, Radio Frequency Power<br>AN/URM-120   | Wattmeter          |
| Generator, Signal SG-1170/U                     | Signal Generator   |
| Voltmeter, Electronic ME-30A/U                  | VTVM               |
| Load, 51 ohms                                   | CMC 335-053        |
| Adapter-Connector UG-201A/U<br>(2 required)     |                    |
| Adapter-Connector UG-29B/U                      |                    |
| Adapter-Connector UG-274/U                      |                    |
| Cable Assembly, Special Purpose,<br>Electrical  | CX-12097/U         |
| Cable Assembly, Radio Frequency<br>(2 required) | CG-409H/ (4.5 ft.) |

b. Operational Check-Transmitter Path.

- (1) Disconnect plug P2 (XA1A1Z1J1) (fig. 3-18) from connector J1 on impedance matching network 2A1A1Z1.
- (2) Connect the test equipment as shown in figure 3-19.
- (3) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (4) Connect the PWR OUT connector of the transmitter rf head to the FROM XMTR connector of the receiver fixed head.
- (5) Set the transmitter AC POWER switch to ON/RESET. The wattmeter should indicate a minimum of 19 watts.
- (6) Set the AC POWER switch to OFF. If an abnormal reading is obtained in (5) above, higher category of maintenance is required.

c. Operational Check-Receiver Path.

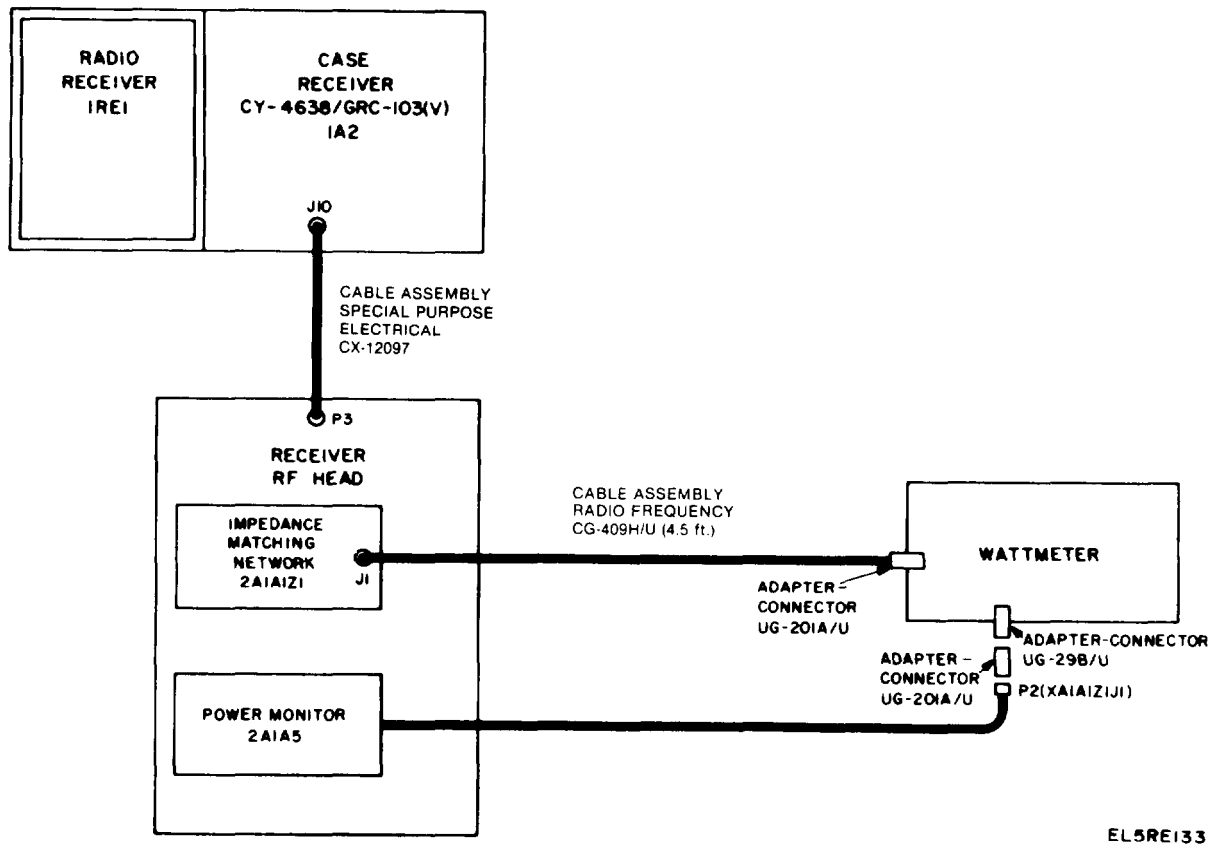
- (1) Disconnect plug P3 (2A1A1A1J2) (fig. 3-20) from connector J2 on bandpass filter assembly 2A1A1A1.
- (2) Connect the test equipment as shown in A, figure 3-21.
- (3) Set the receiver to channel 200.
- (4) Set the frequency of the signal generator to 300 MHz and adjust the output level until a reading of -50 dbm is obtained on the VTVM. Note the attenuator setting on the signal generator.



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Figure 3-18. Receiver Rf Head (AM-4316/GRC-103(V)), Bottom View.

- (5) Reconnect plug P3 (2A1A1A1J2) to connector J2 on bandpass filter assembly 2A1A1A1.
- (6) Disconnect plug P2 (2A1A1Z1J1) (fig. 3-18) connector J1 on impedance matching network 2A1A1Z1.
- (7) Connect the test equipment as shown in 13, figure 3-21.
- (8) Increase the output of the signal generator until a reading of -50 dbm is obtained on the VTVM. The output attenuator setting on the signal generator should not be more than 2 db higher than the setting noted in (4) above.
- (9) If the indication in (8) above is not obtained, replace the receiver rf head.



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Figure 3-19. Duplexer Bandpass Filter (AM-4316/GRC-103(V)), (Transmit) Operational Check, Test Setup.

3-23. Duplexer 2A1A1 and Impedance Matching Network 2A1A1Z7

NOTE

This unit is part of Amplifier Converter AM-4316A/GRC-103(V).

a. Test Equipment Required.

| Equipment                                   | Common Name      |
|---|------------------|
| Test Set, Radio Frequency Power, AN/URM-120 | Wattmeter        |
| Generator, Signal, SG-1170/U                | Signal Generator |
| Voltmeter, Electronic ME-30A/U              | VTVM             |
| Load, 51 ohms                               | CMC 335-053      |
| Adapter-Connector UG-201A/U (2 required)    |                  |
| Adapter-Connector UG29B/U                   |                  |



a. Test Equipment Required-Continued

| Equipment                                    | Common Name         |
|--|---------------------|
| Adapter-Connector UG-274/U                   |                     |
| Adapter-Connector UG-914/U                   |                     |
| Cable Assembly, Special Purpose, Electrical  | CX-12097/U          |
| Cable Assembly, Radio Frequency (2 required) | CG-409H/U (405 ft.) |

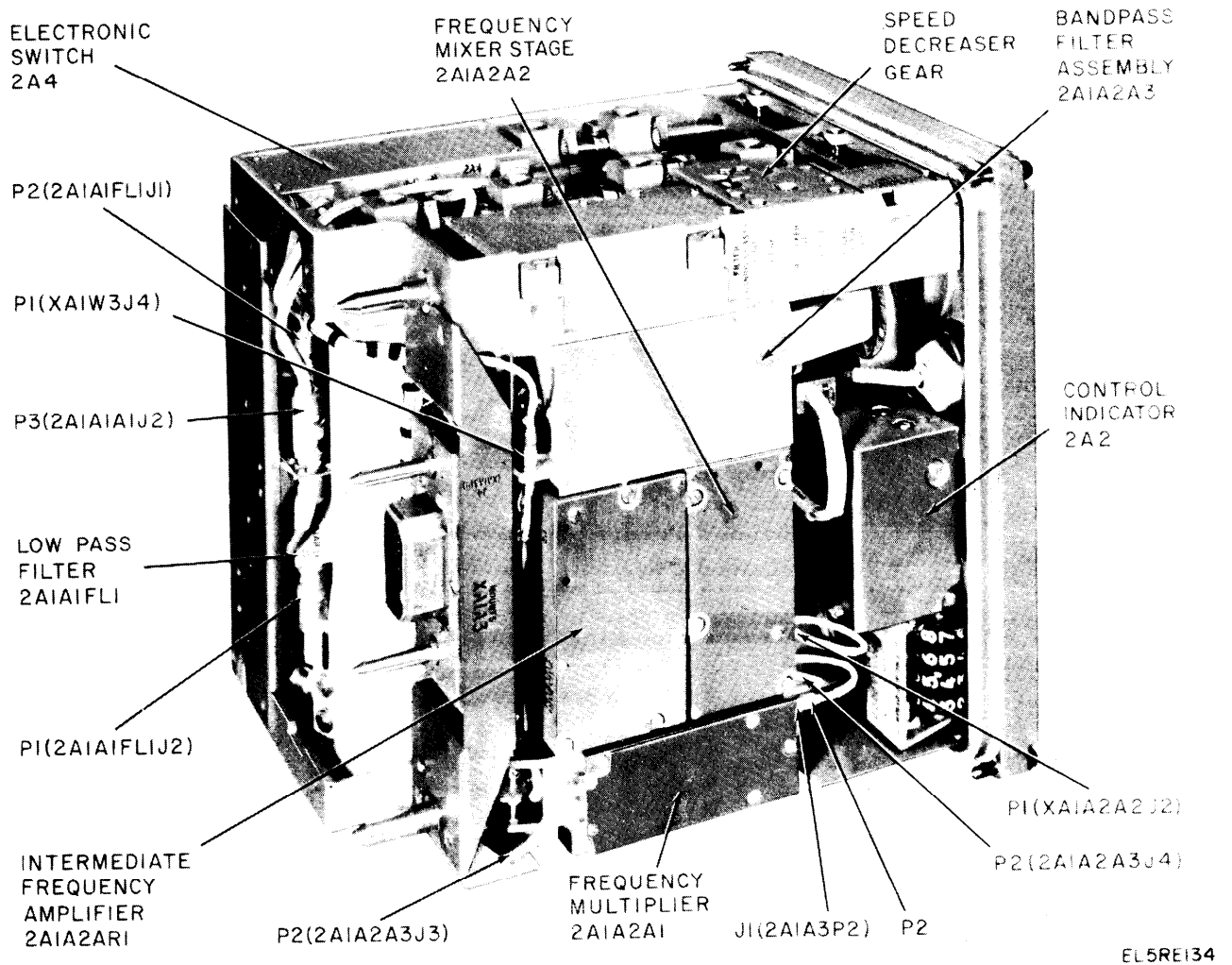


Figure 3-20. Receiver Rf Head (AM-4316/GRC-103(V)), Top and Rear View.

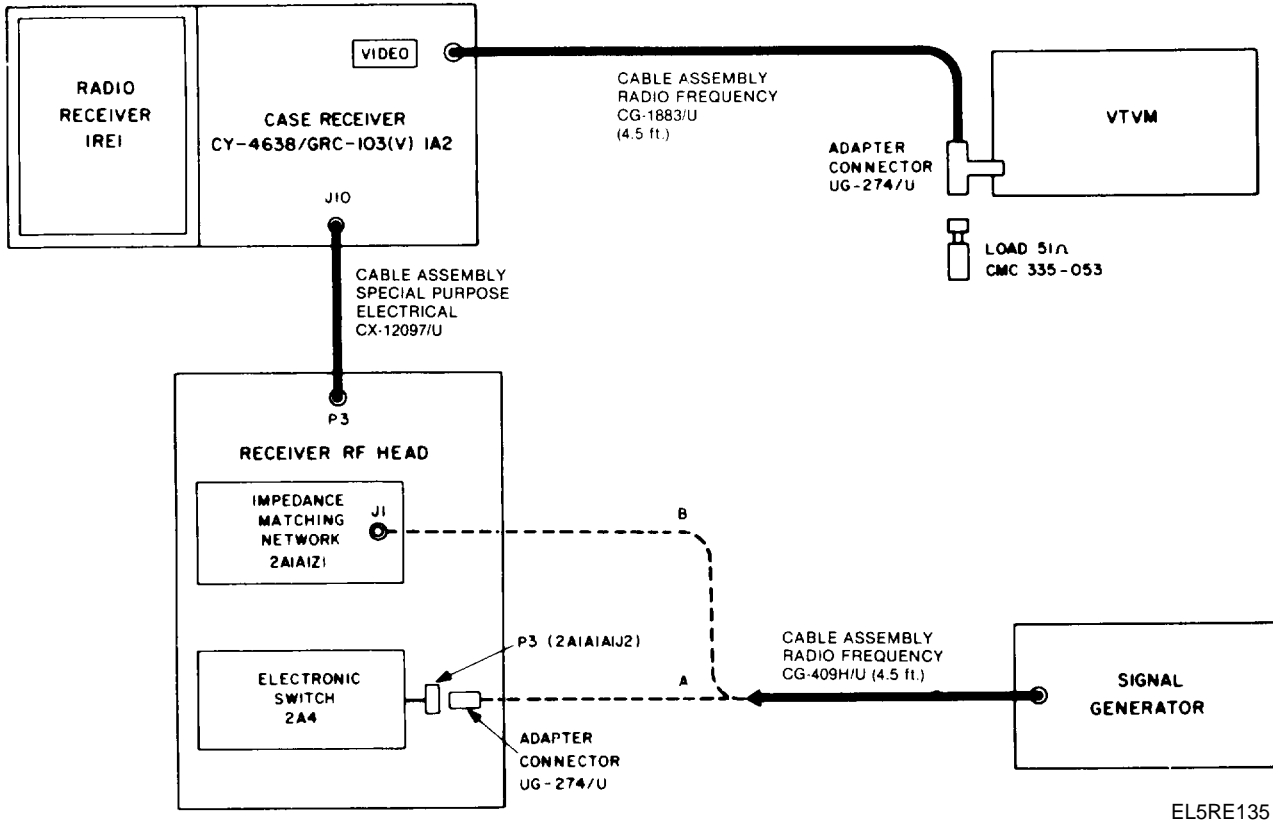
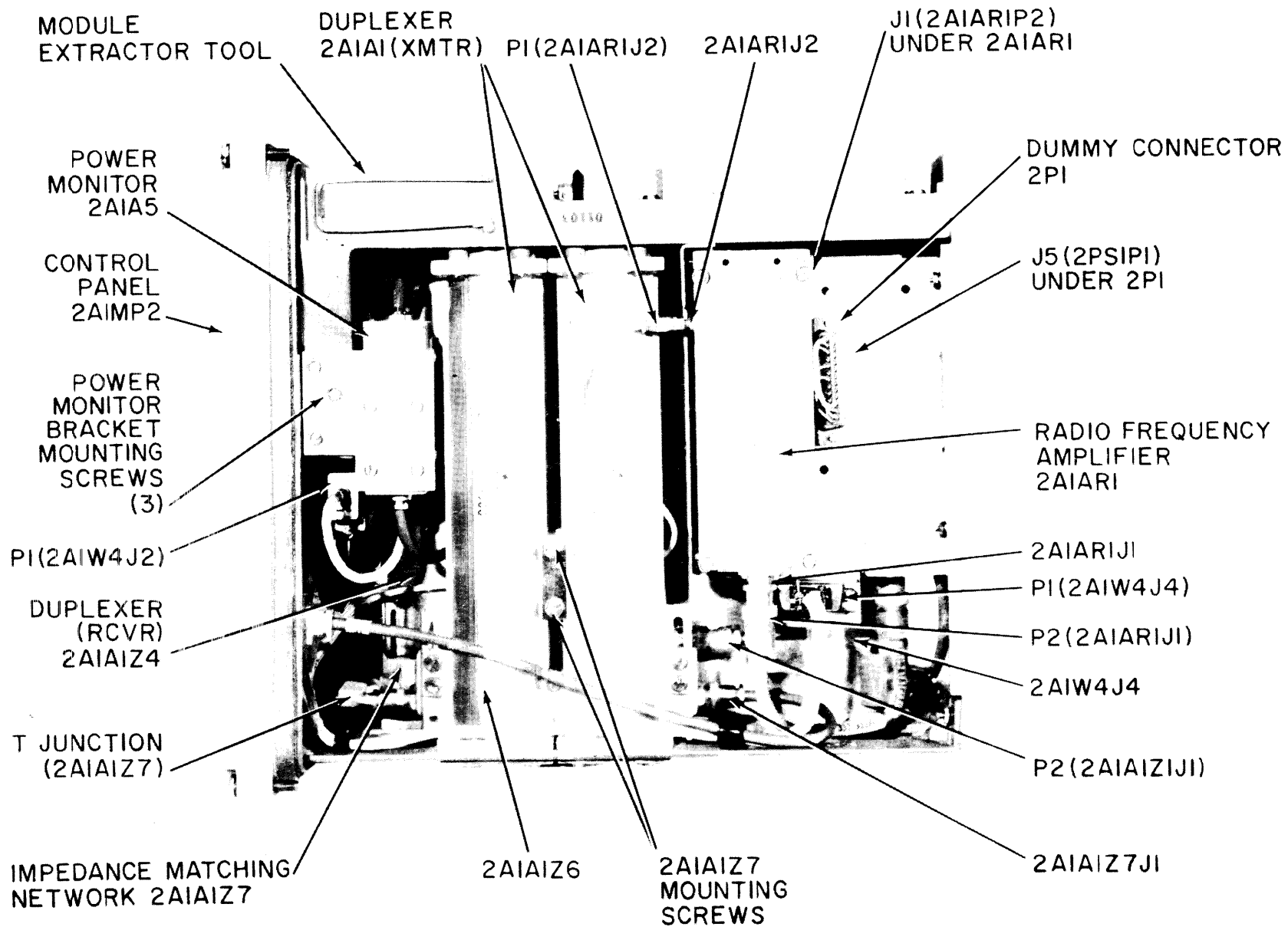


Figure 3-21. Duplexer Bandpass Filter (AM-4316/GRC-103(V)), (Receive) Operational Check, Test Setup.

b. Operational Check-Transmitter Path.

- (1) Disconnect plug P2 (2A1A1Z7J1) (fig. 3-22) from connector J1 on impedance matching network 2A1A1Z7.
- (2) Connect the test equipment as shown in figure 3-23.
- (3) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (4) Connect the PWR OUT connector of the transmitter rf head to the FROM XMTR connector of the receiver fixed head.
- (5) Set the transmitter AC POWER switch to ON/RESET. The wattmeter should indicate a minimum of 19 watts.
- (6) Set the AC POWER switch to OFF. if an abnormal reading is obtained in (5) above, higher category of maintenance is required.
- (7) Disconnect test equipment and reconnect for normal operation.

Figure 3-22. Receiver Rf Head (AM-4316A/GRC-103(V)), Bottom View.



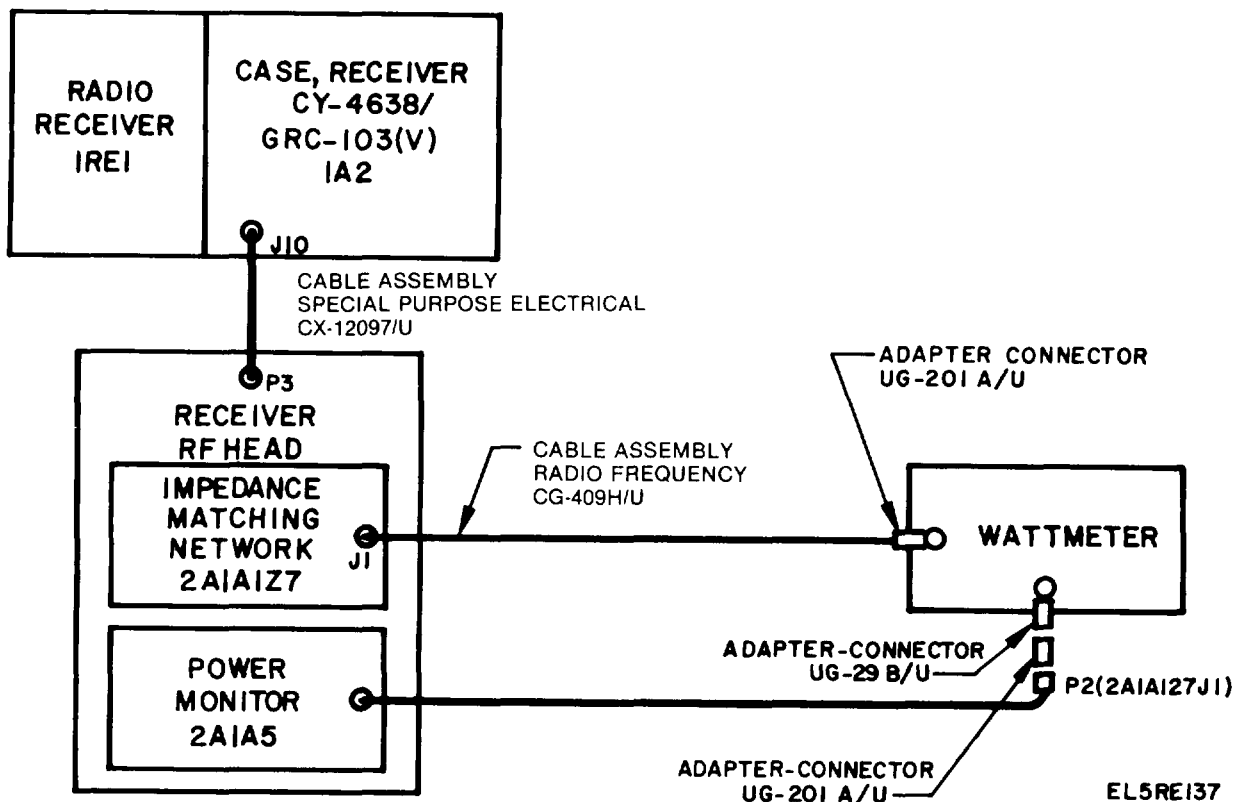
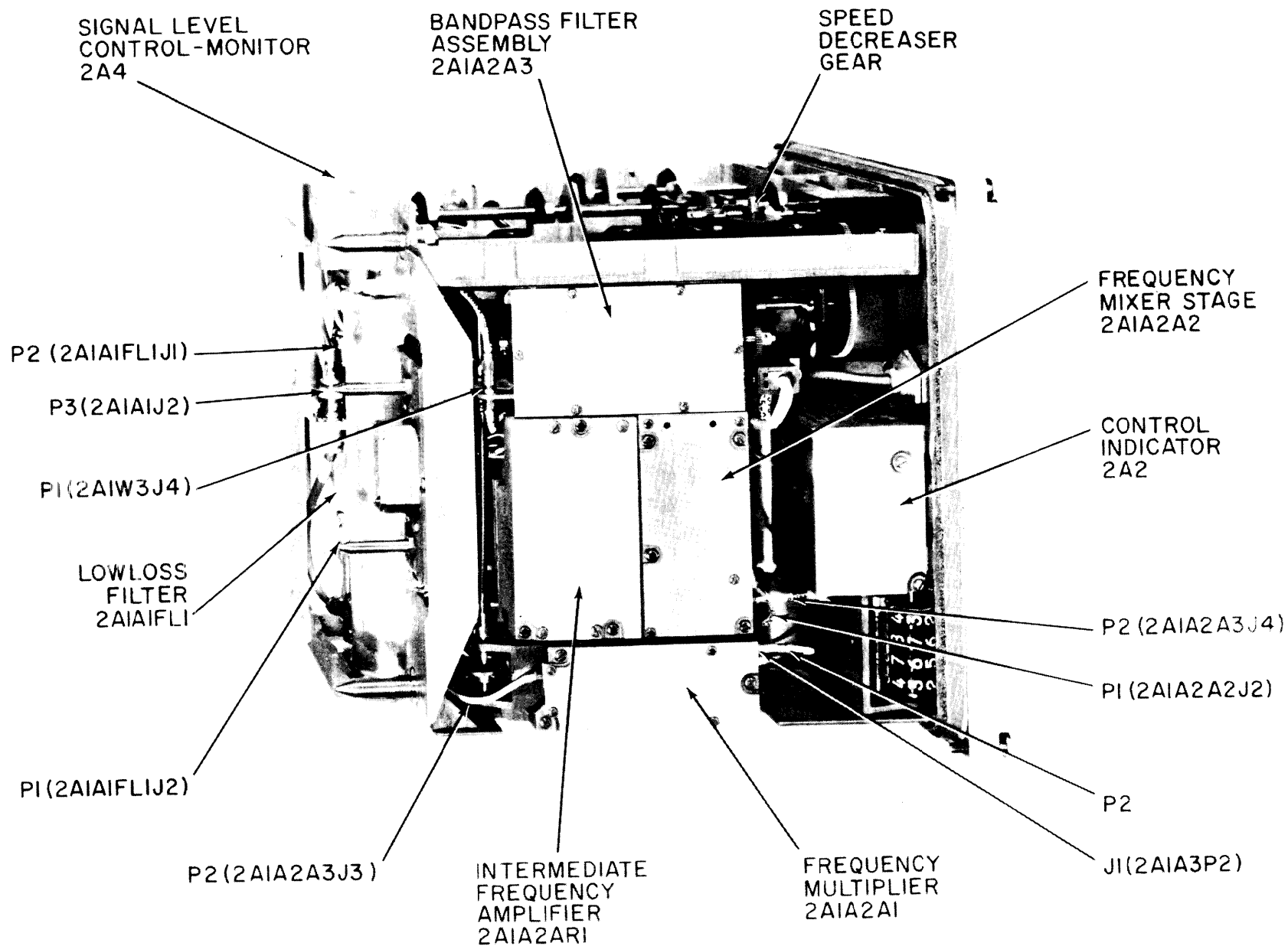


Figure 3-23. Duplexer Bandpass Filter (AM-4316A/GRC-103(V)), (Transmit)Text  
Operational Check, Test Setup.Text

c. Operational Check, Receiver Path.

- (1) Disconnect plug P3 (2A1A1J2) (fig. 3-24) from connector J2 on duplexer 2A1A1.
- (2) Connect the test equipment as shown in A, figure 3-25.
- (3) Set the receiver to channel 200, and receiver AC switch to ON.
- (4) Set the frequency of the signal generator to 300 MHz and adjust the output level until a reading of -50 dbm is obtained on the VTVM. Note the attenuator setting on the signal generator.
- (5) Reconnect plug P3 (2A1A1J2) to connector J2 on duplexer 2A1A1.
- (6) Disconnect plug P2 (2A1A1Z7J1) (fig. 3-22) connector J1 on impedance matching network 2A1A1Z7.
- (7) Connect the test equipment as shown in B figure 3-25.
- (8) Increase the output of the signal generator until a reading of -50 dbm is obtained on the VTVM. The output attenuator setting on the signal generator should not be more than 2 db higher than the setting noted in (4) above.
- (9) If abnormal reading is obtained in (8) above replace receiver rf head.

Figure 3-24. Receiver Rf Head (AM-4316A/GRC-103(V)), Top and Side View.



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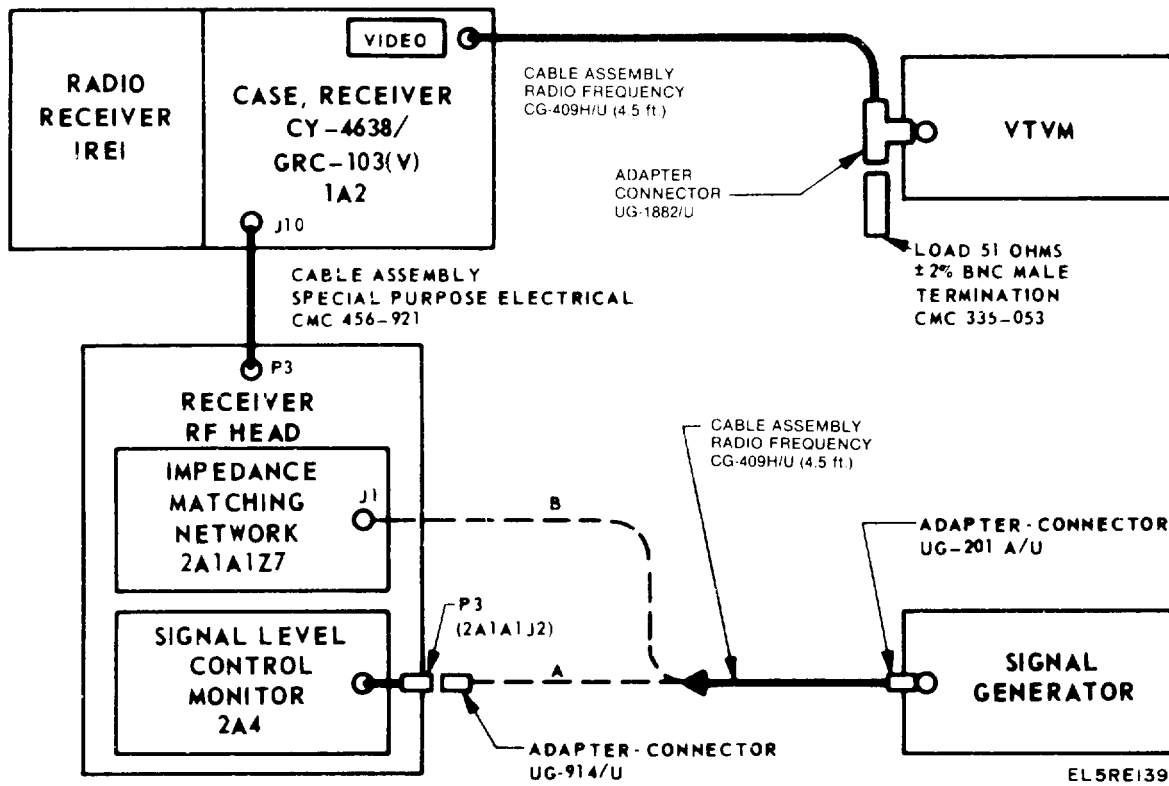


Figure 3-25. Duplexer Bandpass Filter (AM-4316A/GRC-103(V)), (Receive) Operational Check, Test Setup.

3-24. Power Monitor 2A1A5 (AM-4316/GRC-103(V))

a. Test Equipment Required.

| Equipment                                    | Common Name         |
|--|---------------------|
| Test Set, Radio Frequency Power AN/URM-120   | Wattmeter           |
| Generator, Signal, SG-1170/U                 | Signal Generator    |
| Voltmeter, Electronic ME-30A/U               | VTVM                |
| Load, 51 ohms                                | CMC 335-053         |
| Adapter-Connector UG-565A/U                  |                     |
| Adapter-Connector UG-29B/U                   |                     |
| Adapter-Connector UG-564A/U                  |                     |
| Adapter-Connector UG-274/U                   |                     |
| Adapter-Connector UG-636A/U                  |                     |
| Cable Assembly, Radio Frequency (2 required) | CG-409H/U (4.5 ft.) |
| Cable Assembly, Radio Frequency              | CG-1883/U (4.5 ft.) |
| Cable Assembly, Special Purpose, Electrical  | CX-12097/U          |

b. Operational Check-Transmit Path.

- (1) Connect the test equipment as shown in figure 3-26.
- (2) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (3) Set the transmitter AC POWER switch to ON/RESET. The wattmeter should indicate a minimum of 18 watts.
- (4) If an abnormal indication is obtained in (3) above, replace 2A1A5 as described in paragraph 3-64.

c. Operational Check-Receiver Path.

- (1) Disconnect plug P2 (2A1A1Z1J1) (fig. 3-18) from connector J1 of impedance matching network 2A1A1Z1.
- (2) Connect the test equipment as shown in A, figure 3-27.
- (3) Tune the receiver to channel 200.
- (4) Set the frequency of the signal generator to 300 MHz, and adjust the output until the VTVM indicates -50 dbm.
- (5) Reconnect plug P2 (2A1A1Z1J1) to connector J1 of impedance matching network 2A1A1Z1.
- (6) Connect the equipment as shown in B, figure 3-27. The indication on the VTVM should not be greater than -49.5 dbm.
- (7) If an abnormal indication is obtained in (6) above, replace power monitor 2A1A5 as described in paragraph 3-64.

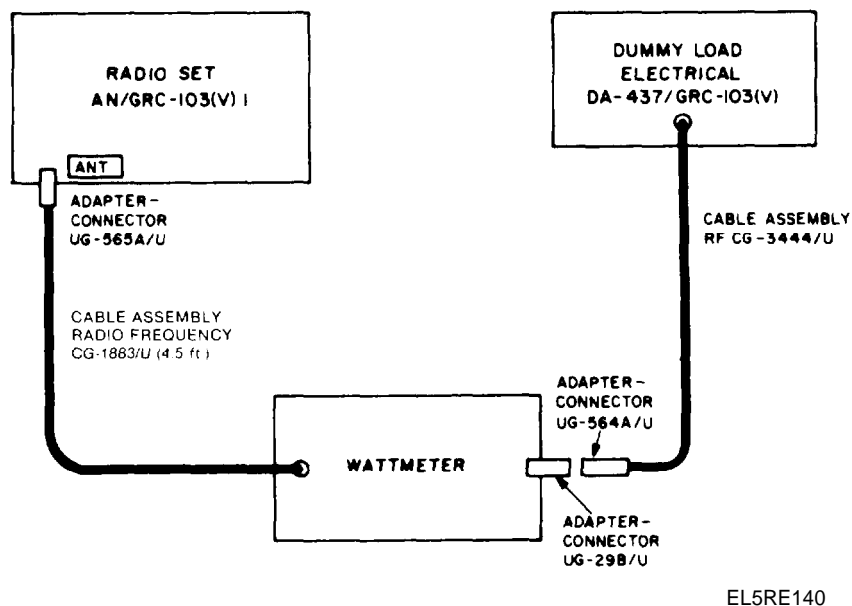
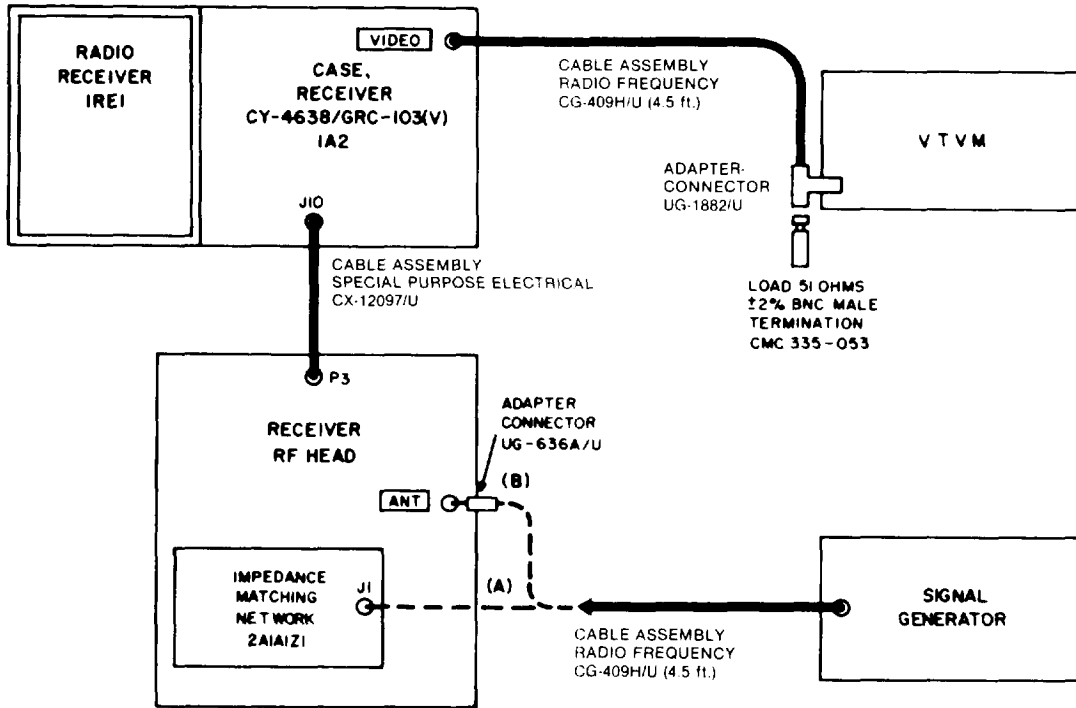


Figure 3-26. Power Monitor 2A1A5, (Transmit Path) Operational Check, Test Setup.



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Figure 3-27. Power Monitor 2A1A5 (AM-4316/GRC-103(V)), (Receive Path) Operational Check, Test Setup.

3-25. Power Monitor 2A1A5 (AM-4316A/GRC-103(V))

a. Test Equipment Required.

| Equipment                                       | Common Name         |
|---|---------------------|
| Test Set, Radio Frequency Power.<br>AN/URM-120  | Wattmeter           |
| Generator, Signal, SG-1170/U                    | Signal Generator    |
| Voltmeter, Electronic ME-30A/U                  | VTVM                |
| Load, 51 ohms                                   | CMC 335-053         |
| Adapter-Connector UG565A/U                      |                     |
| Adapter-Connector UG-29B/U                      |                     |
| Adapter-Connector UG-564A/U                     |                     |
| Adapter-Connector UG-274A/U                     |                     |
| Adapter-Connector UG636A/U                      |                     |
| Cable Assembly, Radio Frequency<br>(2 required) | CG-409H/U (4.5 ft.) |
| Cable Assembly, Radio Frequency                 | CG-1883/U (4.5 ft.) |
| Cable Assembly, Special Purpose,<br>Electrical  | CX-12097/U          |



b. Operational Check-Transmit Path.

- (1) Connect the test equipment as shown in figure 3-26.
- (2) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (3) Set the transmitter AC POWER switch to ON/RESET. The wattmeter should indicate a minimum of 19 watts.
- (4) If an abnormal indication is obtained in (3) above, replace 2A1A5 as described in paragraph 3-64.

c. Operational Check-Receiver Path.

- (1) Disconnect plug P2 (2A1A1Z7J1) from connector J1 of impedance matching network 2A1A1Z7.
- (2) Connect the test equipment as shown in A, figure 3-28.
- (3) Tune the receiver to channel 200, and set receiver AC switch to ON.
- (4) Set the frequency of the signal generator to 300 MHz, and adjust the output until the VTVM indicates -50 dBm. Note the signal generator attenuator setting.

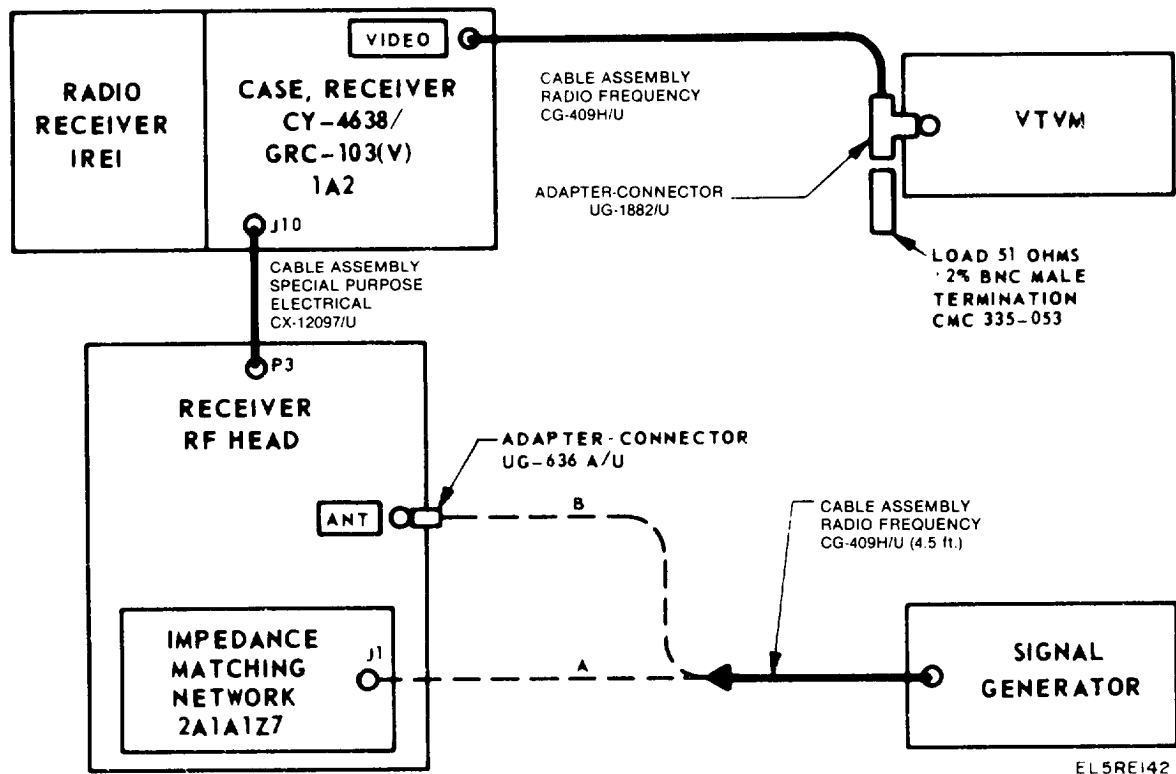


Figure 3-28. Power Monitor 2A1A5 (AM-4316A/GRC-103(V)), (Receive Path) Operational Check, Test Setup.

- (5) Reconnect plug P2 (2A1A1Z7J1) to connector J1 of impedance matching network 2A1A1Z7.
- (6) Connect the equipment as shown in B, figure 3-28. The indication on the VTVM should not be greater than -49.5 dBm.
- (7) If an abnormal indication is obtained, replace power monitor 2A1A5 (para 3-64).

3-26. Electronic Frequency Converter 2A1A2

a. Test Equipment Required.

| Equipment   | Common Name           |
|---|-----------------------|
| Voltmeter, RF, ME-426/U                                   | RF Voltmeter          |
| General, Signal, SG-1170/U                                | Signal Generator No.1 |
| Adapter-Connector UG-274/U                                |                       |
| Cable Assembly, Radio Frequency CG-409H/U                 |                       |
| Cable Assembly, Radio Frequency CG-3578/U                 |                       |
| Cable Assembly, Radio Frequency CG-3579/U                 |                       |
| Cable Assembly, Radio Frequency CG-3580/U                 |                       |
| Cable Assembly, Special Purpose, CX-12097/U<br>Electrical |                       |

b. Operational Check

- (1) Disconnect plug P2 (2A1A2A3J4) (fig.3-20) from connector J4 bandpass filter assembly 2A1A2A3.
- (2) Connect the test equipment as shown in figure 3-29.
- (3) Set the RCVR SIG control and RCVR CHANNEL to channel 410 and set meter selector switch on the receiver, fixed head to MULT.
- (4) Adjust the MULT PEAK control for a maximum indication on the receiver meter.
- (5) Tune the signal generator to 405 MHz and adjust the output level to -57 dBm.
- (6) The RF voltmeter should indicate between -30 dBm and -18 dBm.
- (7) Repeat (3) through (6) above for the remaining channels and frequencies listed below.

| RCVR CHANNEL | RCVR SIG | Signal Generator frequency (MHZ) |
|--------------|----------|----------------------------------|
| 410          | 410      | 405                              |
| 344          | 344      | 372                              |
| 288          | 288      | 344                              |
| 200          | 200      | 300                              |
| 152          | 152      | 276                              |
| 120          | 120      | 260                              |
| 119          | 119      | 259.5                            |
| 73           | 73       | 236.5                            |
| 54           | 54       | 227                              |
| 40           | 40       | 220                              |

(8) If an abnormal indication was obtained above, test Intermediate Frequency Amplifier 2A1A2AR1 (para 3-31), Frequency Mixer Stage 2A1A2A2 (para 3-32), and Bandpass Filter 2A1A2A3/Frequency Multiplier 2A1A2A1 combination (para 3-33).

3-27. Radio Frequency Amplifier 2A1AR1

| Equipment                                    | Common Name         |
|--|---------------------|
| Voltmeter, Electronic. ME-30A/U              | VTVM                |
| Generator, Signal. SG-1170/U                 | Signal Generator    |
| Load, 51 ohms                                | CMC 335-053         |
| Adapter-Connector, UG-274/U                  |                     |
| Cable Assembly, Special Purpose, Electrical  | CX-10297/U          |
| Cable Assmebly, Radio Frequency (2 required) | CG-409H/U (4.5 ft.) |
| Cable Assembly, Radio Frequency              | CG-3578/U (6 In.)   |

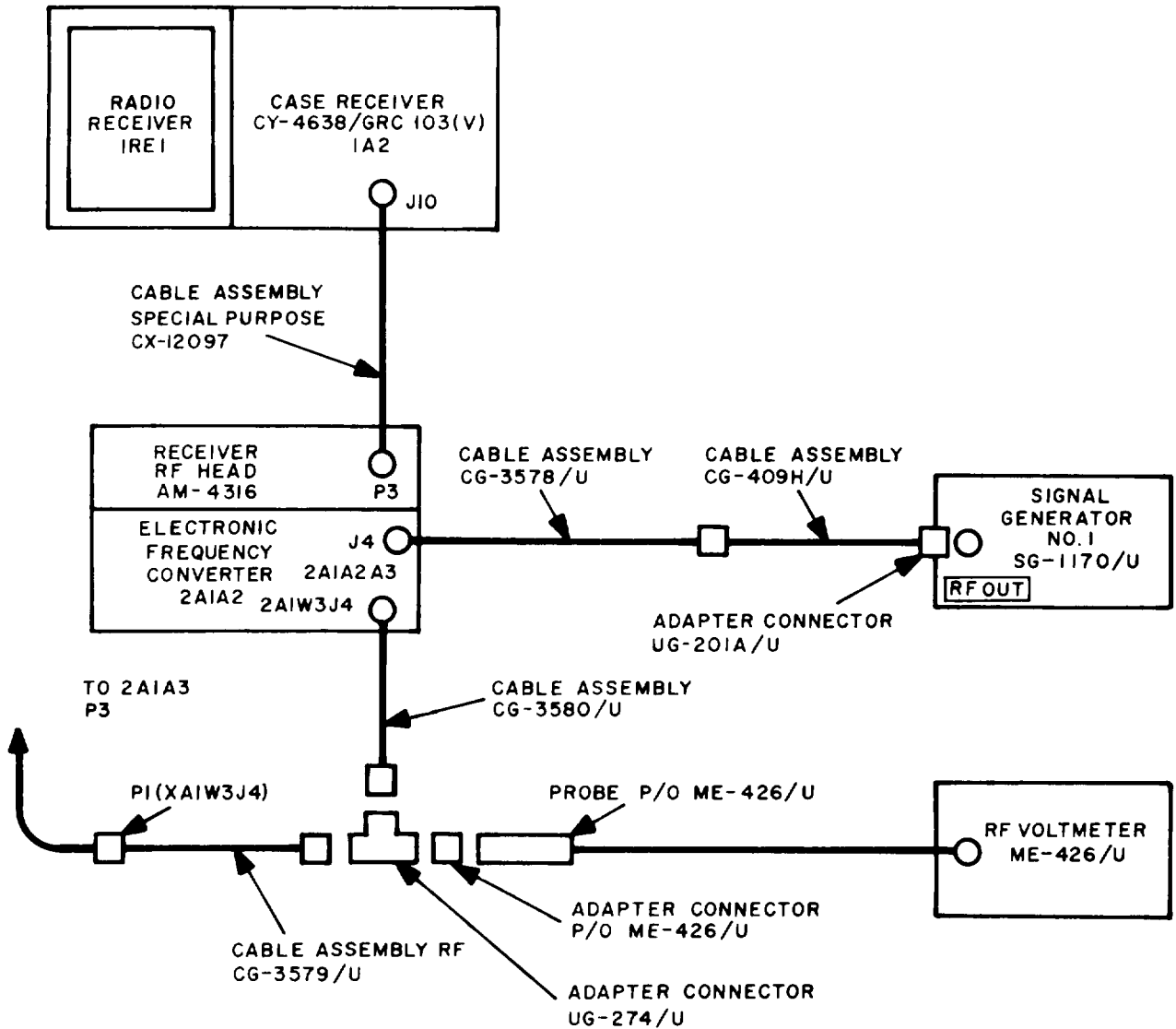
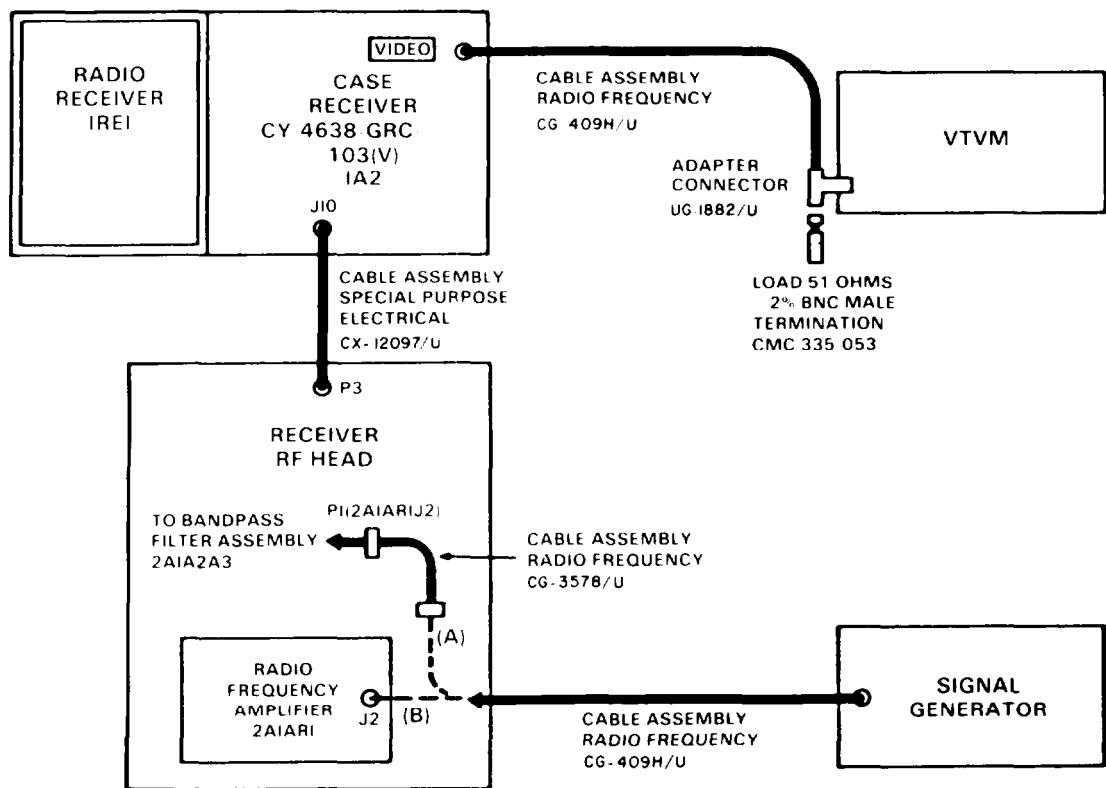


Figure 3-29. Electronic Frequency Converter 2A1A2 Operational Check, Test Setup.

b. Operational Check.

- (1) Disconnect plug P1 (2A1AR1J2) (fig. 3-18) from connector J2 of radio frequency amplifier 2A1AR1.
- (2) Connect the test equipment as shown in A, figure 3-30.
- (3) Tune the receiver rf head to channel 200.
- (4) Set the AC POWER switch to ON.
- (5) Set the frequency of the signal generator to 300 MHz and adjust the output level until a reading of -50 dbm is obtained on the VTVM.
- (6) Connect the test equipment as shown in B, figure 3-30.
- (7) Decrease the output of the signal generator by 27 db.
- (8) The indication on the VTVM should be the same as that obtained in (5) above,  $\pm 3$  db.
- (9) Set the AC POWER switch to OFF.
- (10) If the reading specified in (8) above is not obtained, replace radio frequency amplifier 2A1AR1. Refer to chapter 6 of TM 11-5820-540-12 for replacement procedures.



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Figure 3-30. Radio Frequency Amplifier 2A1AR1 Operational Check, Test Setup.

3-28. Low Pass Filter 2A1AFL1

a. Test Equipment Required.

| Equipment                                     | Common Name        |
|---|--------------------|
| Voltmeter, Electronic, ME-30A/U               | VTVM               |
| Generator, Signal, SG-1170/U                  | Signal Generator   |
| Load, 51 ohms                                 | CMC 335-053        |
| Cable Assembly, Special Purpose, Electrical   | CX-10297/U         |
| Cable Assmbeley, Radio Frequency (2 required) | CG-409H/ (4.5 ft.) |

b. Operational Check

- (1) Disconnect plug P2 (2A1AR1J1) (fig. 3-18) from connector J1 of radio frequency amplifier 2A1AR1.
- (2) Connect the test equipment as shown in B, figure 3-31.

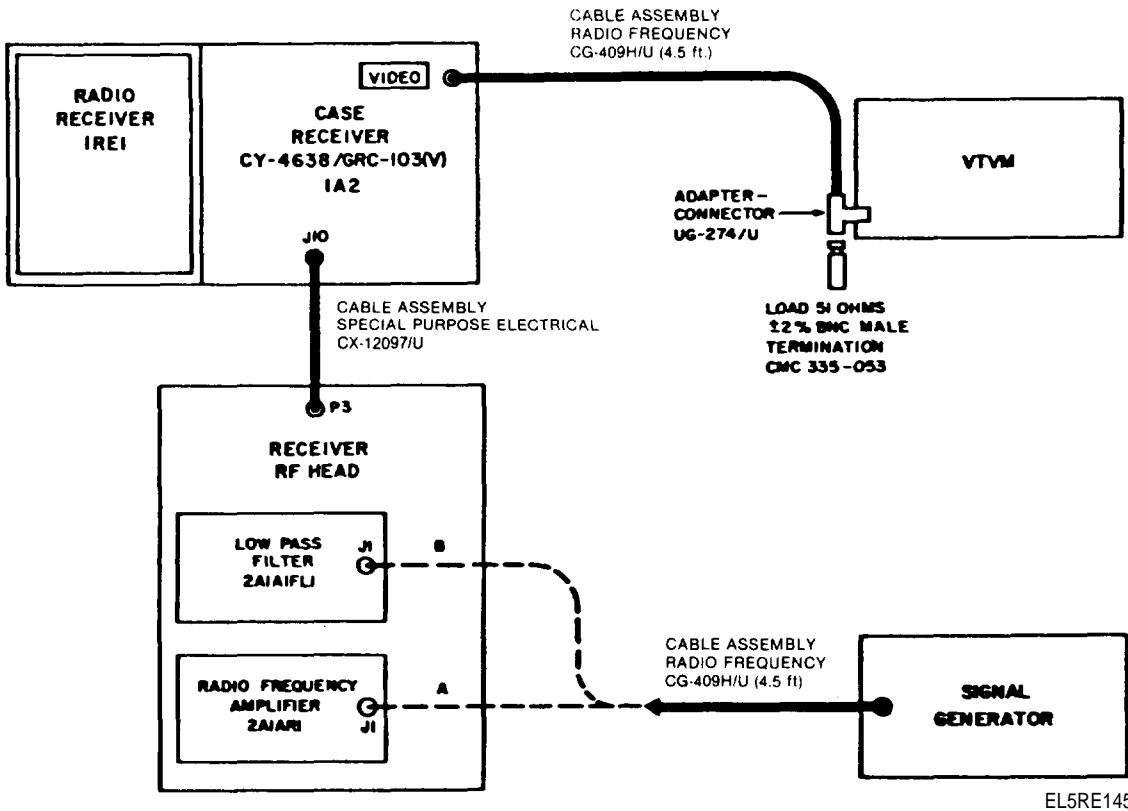


Figure 3-31. Low Pass Filter 2A1AFL1 Operational Check, Test Setup.

- (3) Tune the receiver rf head to channel 200.
- (4) Set the frequency of the signal generator to 300 MHz and adjust the output level for a -50 dbm reading on the VTVM.
- (5) Reconnect plug P2 (2A1AR1J1) to connector J1 of radio frequency amplifier 2A1AR1.
- (6) Disconnect plug P2 (2A1A1FL1J1) (fig. 3-20) from the connector J1 of low pass filter 2A1A1FL1.
- (7) Connect the test equipment as shown in A, figure 3-31.
- (8) The indication on the VTVM should not be greater than -49.5 dBm.
- (9) If an abnormal indication is obtained in (8) above, replace 2A1A1FL1. Refer to chapter 6 of TM 11-5820-540-12 for replacement procedures.

3-29. Signal Level Control Monitor 2A4 (AM-4316A/GRC-103(V))

a. Test Equipment Required.

| Equipment  | Common Name                                  |
|--|--|
| Voltmeter, Electronic, ME-30A/U<br>Generator, Signal, SG-1170/U<br>Load, 51 ohms<br>Adapter-Connector UG-274/U<br>(2 required) | Voltmeter<br>Signal Generator<br>CMC 335-053 |

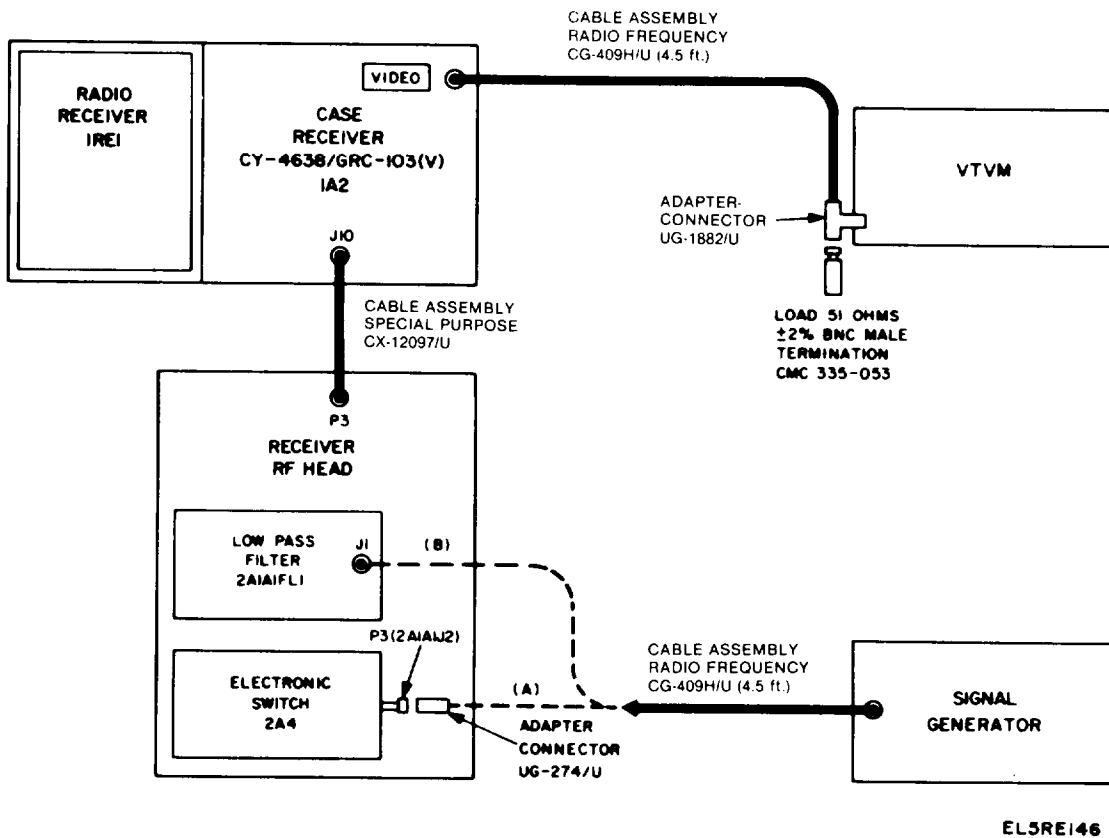


Figure 3-32. Electronic Switch 2A4 and Power Supply 2PS1 Operational Check, Test Setup.



a. Test Equipment Required-Continued.

| Equipment                                       | Common Name         |
|---|---------------------|
| Cable Assembly, Special Purpose Electrical      | CX-12097/U          |
| Cable Assembly, Radio Frequency<br>(2 required) | CG-409H/U (4.5 ft.) |

b. Operational Check.

- (1) Disconnect plug P3 (2A1A1J2) (fig. 3-24) from connector J2 of bandpass filter assembly 2A1A1.
- (2) Connect the test equipment as shown in A, figure 3-33.
- (3) Tune the receiver to channel 200 and the signal generator to 300 MHz.
- (4) Set the AC POWER switch to ON.
- (5) Increase the output level of the signal generator to a maximum +10 dbm. The HIGH SIGNAL alarm should operate and the buzzer may sound if it is not muted.

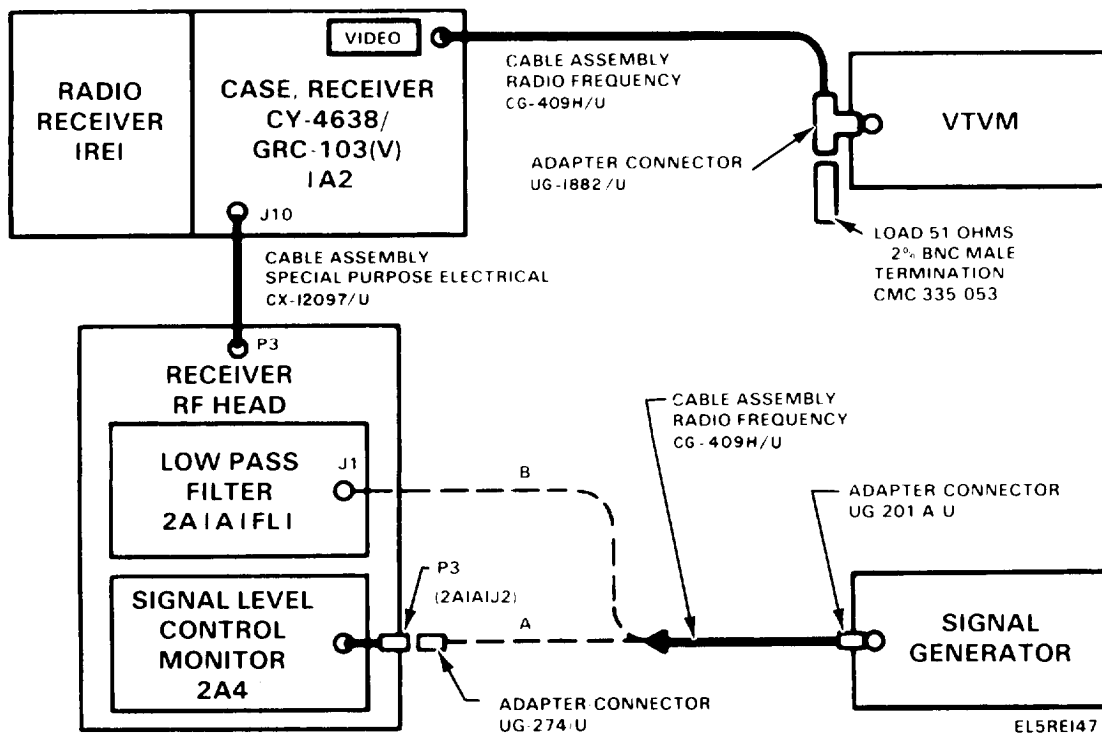


Figure 3-33. Signal Level Control Monitor 2A4 Operational Check, Test Setup (AM-4316A/GRC-103(V)).

- (6) Decrease the level of the signal generator until the VTVM indicates -50 dbm.
- (7) Connect the test equipment as shown in B, figure 3-33.
- (8) The indication obtained on the VTVM should not be higher than -49.5 dbm.
- (9) Set the AC POWER switch to OFF.
- (10) If the HIGH SIGNAL alarm does not come on in (5) above, or the indication obtained in (8) above is beyond the specified limit, signal level control-monitor 2A4 and/or dummy connector 2P1 should be replaced. Refer to TM 11-5820-540-12 for replacement procedures.

3-30. Intermediate Frequency Amplifier 2A1A2AR1

a. Test Equipment Required.

| Equipment                                  | Common Name         |
|--|---------------------|
| Generator, Signal, SG-1170/U               | Signal Generator    |
| Adapter-Connector UG-201A/U                |                     |
| Adapter-Connector UG-274/U                 |                     |
| Cable Assembly, Special Purpose Electrical | CX-12097/U          |
| Cable Assembly, Radio Frequency            | CG-3580/U (6 in.)   |
| Cable Assembly, Radio Frequency            | CG-3578/U (6 in.)   |
| Cable Assembly, Radio Frequency            | CG-409H/u (4.5 ft.) |
| Voltmeter, RF, ME-426/U                    | RF Voltmeter        |
| Cable Assembly, RF                         | CG-3579/U           |

b. Operational Check

- (1) Disconnect plug P1 (XA1A2A2J2) (fig. 3-20 or 3-24) from connector J2 of frequency mixer stage 2A1A2A2. Disconnect PI (XA1W3J4).
- (2) Connect the test equipment as shown in figure 3-34.
- (3) Set the frequency of the signal generator to 30 MHz at an output level of -60 dBm.
- (4) Set the receiver AC POWER switch to ON. The RF Voltmeter should indicate between -30 dBm and -18 dBm.
- (5) Set the receiver AC POWER switch to OFF.
- (6) If the indication obtained in (4) above is outside specified limits, replace intermediate frequency amplifier 2A1A2AR1. Refer to TM 11-5820-540-12, chapter 6, for replacement procedures.

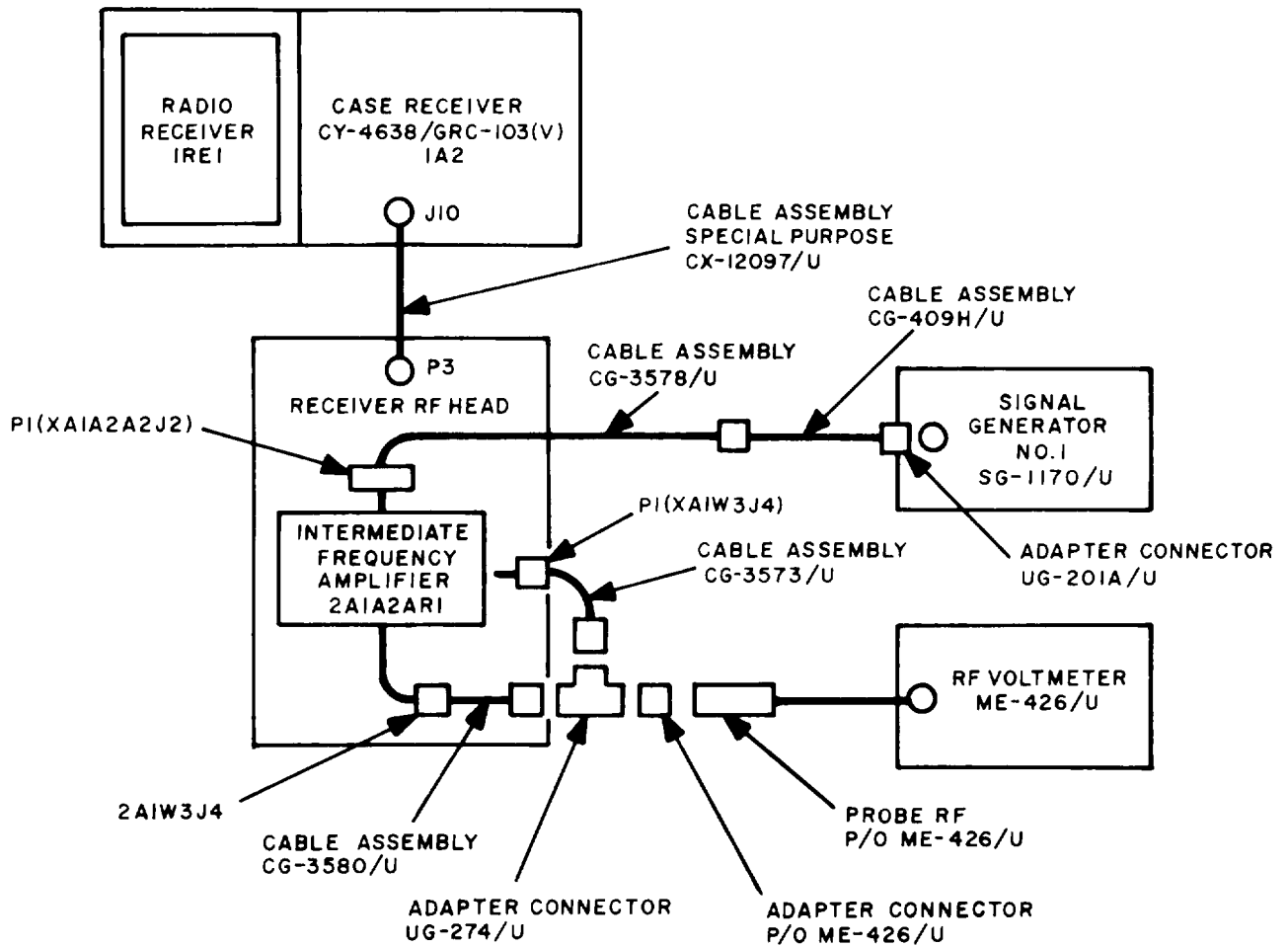


Figure 3-34. Intermediate Amplifier 2A1A2AR1 Operational Check, Test Setup.

| Equipment                                  | Common Name        |
|--|--------------------|
| Generator, Signal, SG-1170/U               | Signal Generator   |
| Adapter-Connector UG-201A/U                |                    |
| Cable Assembly, Special Purpose Electrical | CX-12097/U         |
| Cable Assembly, Radio Frequency            | CG-3580/U 6 in.)   |
| Cable Assembly, Radio Frequency            | CG-3578/U 6 in.)   |
| Cable Assembly, Radio Frequency            | CG-409H/U 4.5 ft.) |
| Voltmeter, RF, ME-426/U                    | RF Voltmeter       |
| Cable Assembly, RF                         | CG-3579/U          |

b. Operational Check

NOTE

Intermediate frequency amplifier 2A1A2AR1 and bandpass filter 2A1A2A3/frequency multiplier 2A1A1A1 combination must be serviceable for this test. Test as described in paragraphs 3-30 and 3-32 respectively.

- (1) Disconnect plug P2 (2A1A2A3J4) (fig. 3-20 or 3-24) from connector J4 of frequency mixer stage 2A1A2A3.

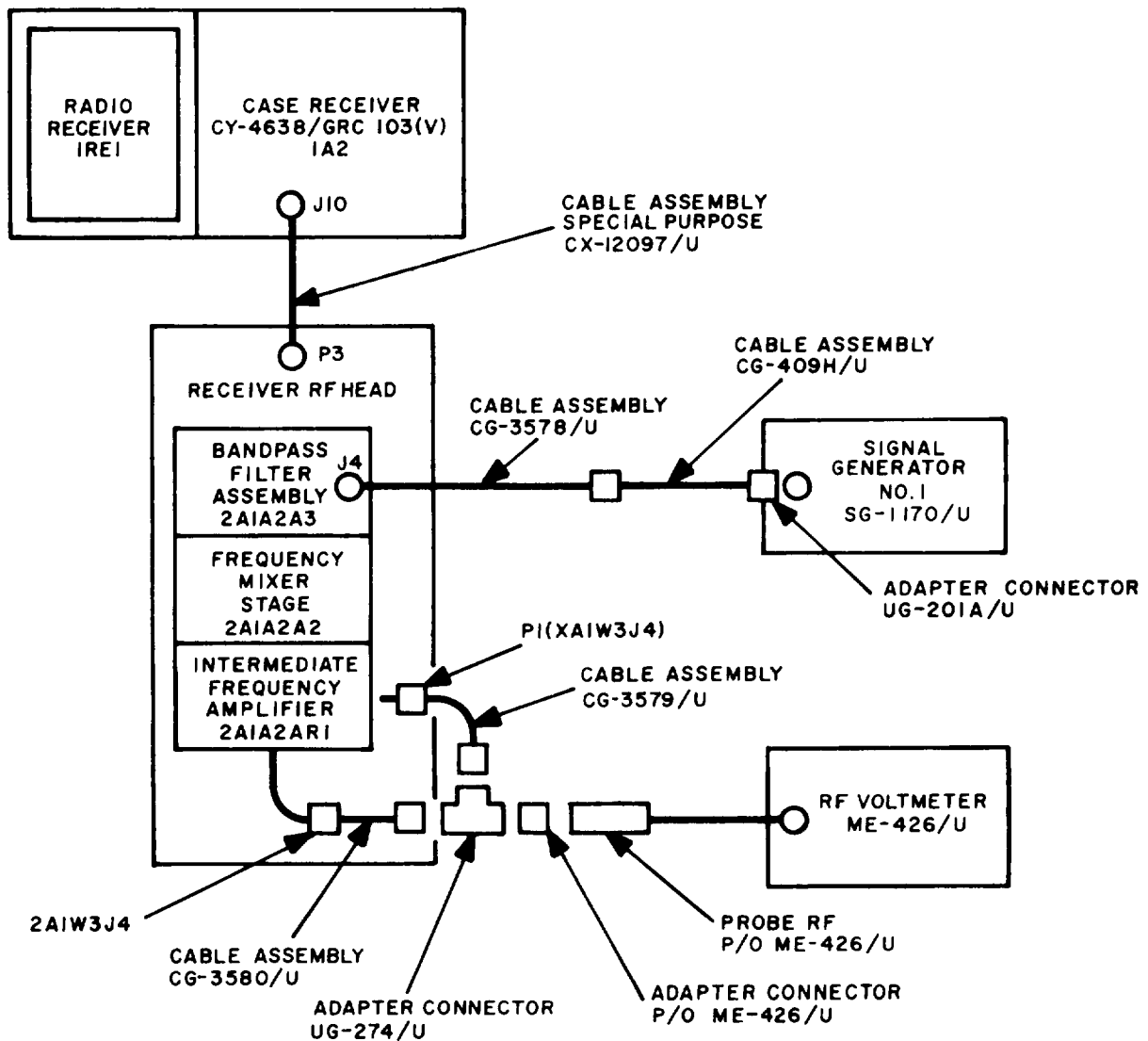


Figure 3-35. Frequency Mixer Stage 2A1A2A2 Operational Check, Test Setup.

- (2) Connect the test equipment as shown in figure 3-35.
- (3) Tune the receiver to channel 200.
- (4) Set the frequency of the signal generator to 300 MHz at an output level of -57 dBm.
- (5) Set the receiver AC POWER switch to ON. The RF Voltmeter should indicate between -30 dBm and -18 dBm.
- (6) If the indication obtained in (5) above is outside specified limits, replace frequency mixer stage 2A1A2A2 as described in paragraph 3-66.

3-32. Bandpass Filter 2A1A2A3/Frequency Multiplier 2A1A2A1 Combination

a. Test Equipment Required.

| Equipment                                     | Common Name       |
|---|-------------------|
| Adapter-Connector UG-29B/U                    |                   |
| Adapter-Connector UG-201A/U<br>(2 required)   |                   |
| Cable Assembly, Special Purpose<br>Electrical | CX-12097/U        |
| Cable Assembly, Radio Frequency               | CG-3580/U (6 in.) |
| Cable Assembly, Radio Frequency               | CG-3578/U (6 in.) |
| Meter, Power, ME-441/U                        | Power Meter       |
| Thermistor Mount, Power Meter, HP-478A        | Thermistor Mount  |
| Cable Assembly, RF                            | CG-409H/U         |

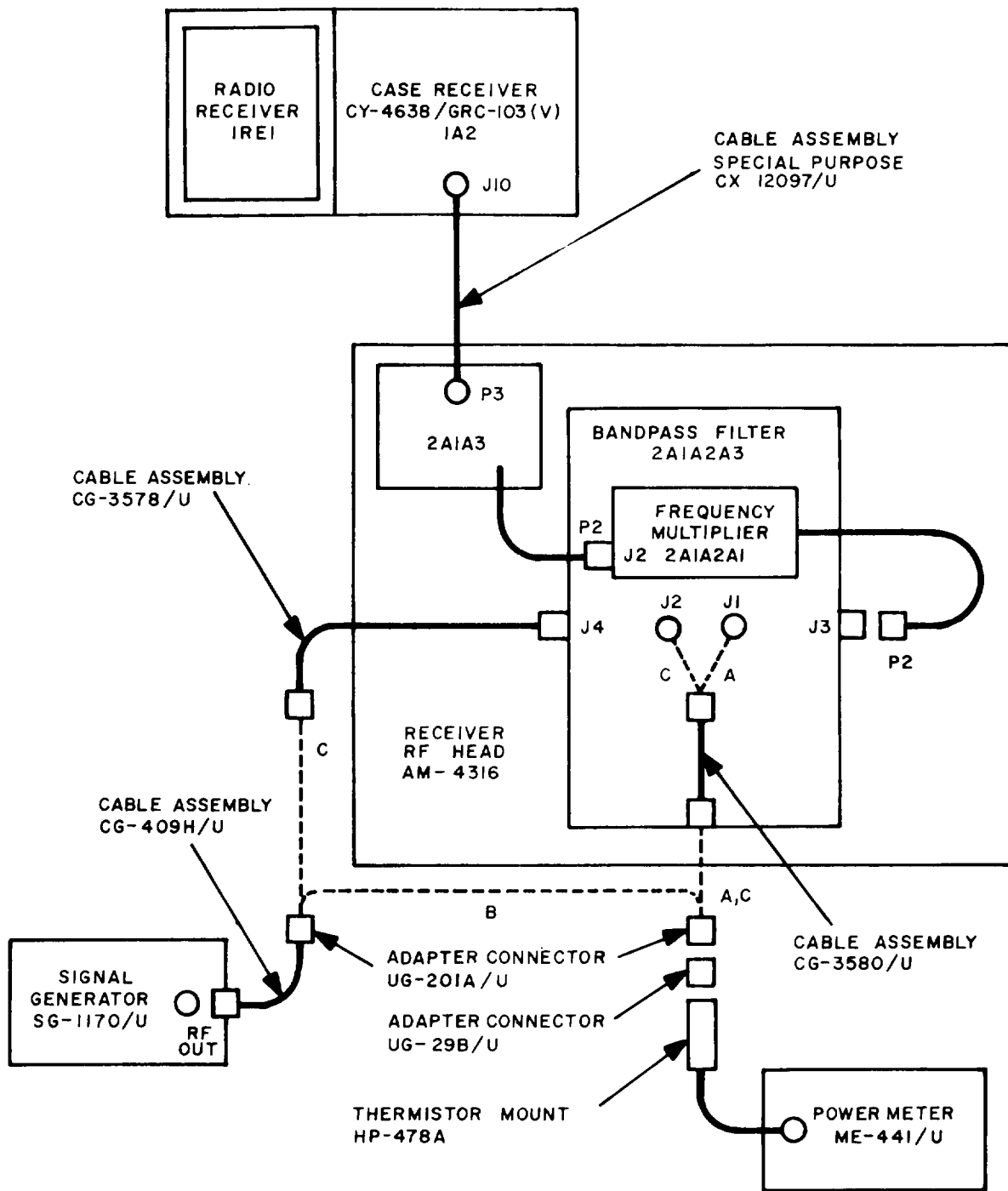


Figure 3-36. Bandpass Filter 2A1A2A3/Frequency Multiplier 2A1A2A1 Combination, Operational Test Setup.

b. Test Procedure

- (1) Remove frequency mixer 2A1A2A2 and Intermediate frequency amplifier 2A1A2AR1 from the electronic frequency converter 2A1A2.
- (2) Connect the test equipment as shown in A, figure 3-36.
- (3) Set the RF head RCVR SIG and RCVR CHANNEL controls to channel 410.
- (4) Adjust the MULT PEAK control for a peak indication on the power meter. The level must be a minimum of +1.0 dBm.
- (5) Connect test equipment as shown In B, figure 3-36.
- (6) Tune the signal generator to 405 MHz and adjust the output level for +8 dBm, as indicated on the power meter.
- (7) Connect test equipment as shown in C, figure 3-36. The power meter indication should not be less than +7.0 dBm.
- (8) Repeat (3) through (7) above for the remaining channels and frequencies listed below.

| RCVR CHANNEL | RCVR SIG | Signal Generator frequency<br>(MHZ) |
|--------------|----------|-------------------------------------|
| 410          | 410      | 405                                 |
| 344          | 344      | 372                                 |
| 288          | 288      | 344                                 |
| 200          | 200      | 300                                 |
| 120          | 120      | 260                                 |
| 119          | 119      | 259.5                               |
| 73           | 73       | 236.5                               |
| 54           | 54       | 227                                 |
| 40           | 40       | 220                                 |

- (9) If an abnormal indication was obtained above, refer RF head to higher category of maintenance.

3-33. Control-Indicator 2A2

a. Test Equipment Required.

| Equipment  | Common Name                      |
|--|----------------------------------|
| Multimeter, Digital, AN/USM-486<br>Cable Assembly, Special Purpose<br>Electrical | Digital Multimeter<br>CX-12098/U |

b. Operational Check.

- (1) Loosen the two screws that secure plug P1 (2A1W4J4) to chassis connector 2A1W4J4 (fig. 3-18). Disconnect P1 (2A1W4J4) from 2A1W4J4.
- (2) Set the RCVR CHANNEL control to channel 52.
- (3) Using the multimeter, check for correct resistance between the following pins of P1 (2A1W4J4) as shown in the chart below.

| Pins      | Resistance |
|-----------|------------|
| 3 and 14  | Infinity   |
| 4 and 14  | Infinity   |
| 5 and 14  | Infinity   |
| 6 and 14  | Infinity   |
| 7 and 14  | Infinity   |
| 8 and 14  | Infinity   |
| 9 and 14  | Infinity   |
| 10 and 14 | Infinity   |
| 11 and 14 | Infinity   |
| 12 and 14 | Zero       |

- (4) Set the RCVR CHANNEL control to channel 51.
- (5) Using the multimeter, check for correct resistance between the following pins of P1 (2A1W4J4) as shown in the chart below.



| Pins      | Resistance |
|-----------|------------|
| 3 and 14  | Zero       |
| 4 and 14  | Zero       |
| 5 and 14  | Zero       |
| 6 and 14  | Zero       |
| 7 and 14  | Zero       |
| 8 and 14  | Zero       |
| 9 and 14  | Zero       |
| 10 and 14 | Zero       |
| 11 and 14 | Zero       |
| 12 and 14 | Infinity   |

- (6) Remove control-indicator 2A2 from the receiver rf head, as described in chapter 6 of TM 11-5820-540-12.
- (7) Connect plug P1 (2A1W4J4) to chassis connector 2A1W4J4 using the CX-12098/U extender cable.
- (8) Remove the four screws that secure the cover on control-indicator 2A2. Remove the cover.
- (9) Set the receiver AC POWER switch to ON.
- (10) Set control-indicator 2A2 to channel 119.
- (11) Using the multimeter, check the voltage at terminal E12 on command signal decoder 2A2A2. The multimeter should indicate 0 volt.
- (12) Set control-indicator 2A2 to channel 120.
- (13) Using the multimeter, check the voltage at terminal E12 on command signal decoder 2A2A2. The multimeter should indicate 10 volts.
- (14) Set AC POWER switch to OFF. Reinstall control-indicator 2A2 cover. If abnormal Indications are obtained in either (3), (5), (11), or (13) above, replace control-indicator 2A2. Refer to chapter 6 of TM 11-5820-540-12 for replacement procedures.

### 3-34. Power Supply 1RE1PS1

#### a. Test Equipment Required.

| Equipment   | Common Name                      |
|---|----------------------------------|
| Multimeter, Digital, AN/USM-486<br>Cable Assembly, Special Purpose,<br>Electrical | Digital Multimeter<br>CX-12098/U |

b. Operational Check.

- (1) Remove power supply 1RE1PS1 as described in chapter 6 of TM 11-5820-540-12.
- (2) Connect connector P2 of 1RE1PS1 to receptacle 1RE1A1J1 of radio receiver 1RE1, using the CX-12098/U extender cable.
- (3) Set the receiver AC POWER switch to ON.
- (4) Using the multimeter, measure the dc voltages at test points on voltage regulator amplifier 1RE1PS1AR1, as shown in the chart below.

| Test point          | Volts dc |
|---------------------|----------|
| TP5 (-) and TP6 (+) | +12±0.1  |
| TP4 (-) and TP5 (+) | +12±0.1  |
| TP4 (-) and TP6 (+) | +24±0.2  |

WARNING

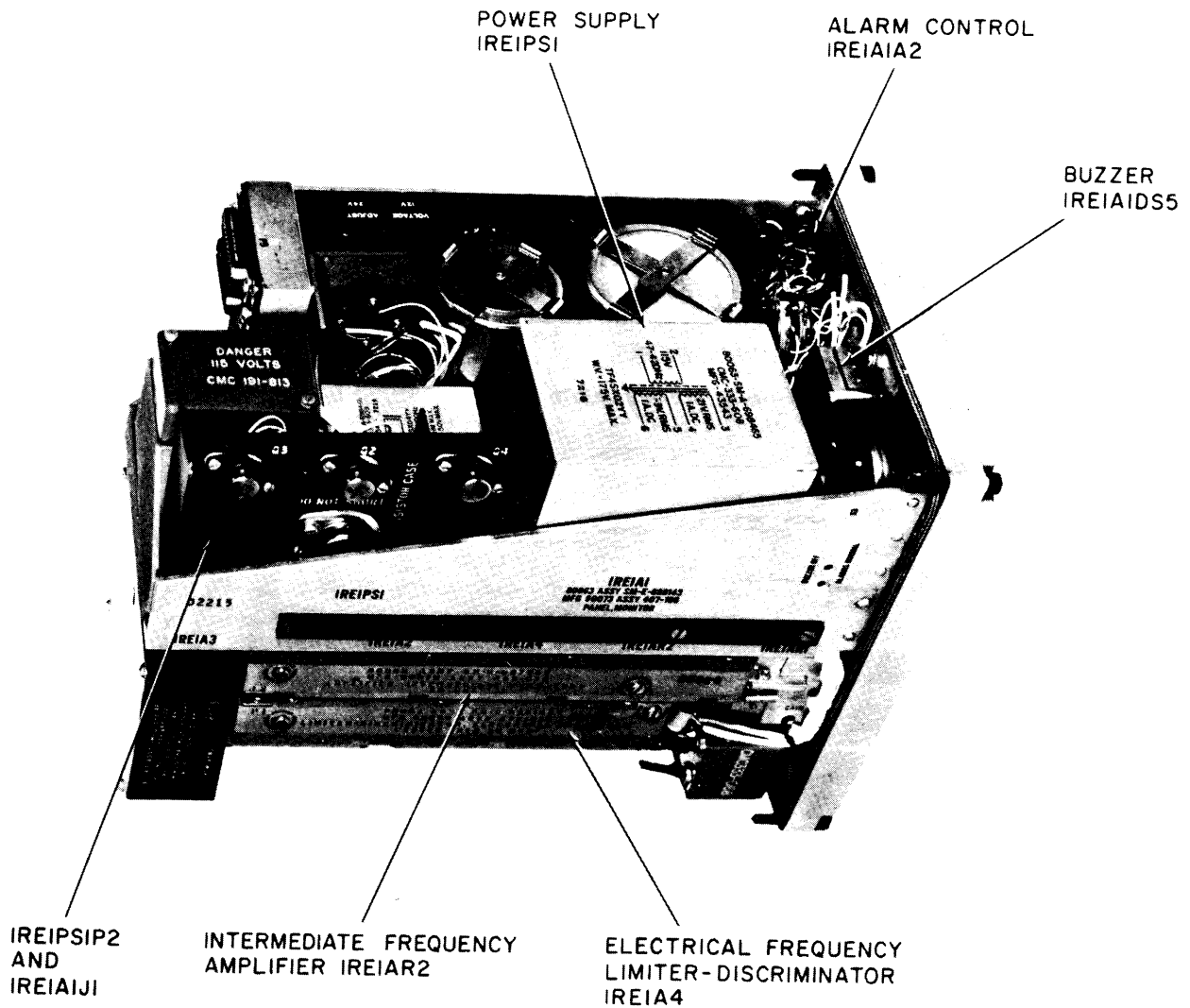
Be extremely careful when working with the safety cover removed, 115 volts ac is exposed.

- (5) Carefully remove the small red safety cover marked DANGER 115V (fig. 3-37).
- (6) Using the multimeter measure the dc voltage across filter connectors FL4 (-) and FL3 (+). A 26 volt dc indication should be obtained.
- (7) Set the AC POWER switch to OFF. Reinstall the red safety cover. Replace power supply 1RE1PS1 if abnormal indications are obtained in either (4) or (6) above. Refer to chapter 6 of TM 11-5820-540-12 for replacement procedures.

3-35. Electrical Frequency Synthesizer 1RE1A2

NOTE

Troubleshooting electrical frequency synthesizer 1RE1A2 also involves checking the appropriate control-indicator for the band in use. If abnormal indications are obtained in any of the following tests, troubleshoot control-indicators 2A2 for Band I, 33A4 for Band III, 34A4 for Band III, and 39A4 for Band IV as described in paragraphs 3-33, 3-90, 3-114, and 3-153 respectively, before replacing electrical frequency synthesizer 1RE1A2.



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Figure 3-37. Radio Receiver 1RE1, Top View.

a. Test Equipment Required.

| Equipment  | Common name                  |
|--|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A        | Power Meter Thermistor Mount |
| Counter, Electronic Digital Readout AN/USM-207               | Counter                      |
| Attenuator, Fixed, 10 dB, AD-10MN                            | 10 dB attenuator             |
| Load, 51 ohms<br>Adpater-Connector UG-201A/U<br>(2 required) | CMC 335-053                  |

a. Test Equipment Required - Continued.

| Equipment                                   | Common Name         |
|---|---------------------|
| Adapter-Connector UG-29B/U                  |                     |
| Adapter-Connector UG-274/U                  |                     |
| Cable Assembly, Special Purpose, Electrical | CX-2095/U           |
| Cable Assembly, Special Purpose, Electrical | CX-2096/U           |
| Cable Assembly, Special Purpose, Electrical | CX-2100/U           |
| Cable Assembly, Radio Frequency             | CG-409H/U (4.5 ft.) |
| Cable Assembly, Radio Frequency             | CG-3570/U (6 in.)   |

b. Test Setup.

- (1) Remove electrical frequency synthesizer 1RE1A2 as described in paragraph 3-59.
- (2) Remove amplifier-frequency multiplier 1RE1A5 from electrical frequency synthesizer 1RE1A2 as described in chapter 6 of TM 11-5820-540-12.
- (3) Connect connector P2 of 1RE1A2 to receptacle 1RE1A1AJ3 of radio receiver 1RE1, using the CX-12100/U extender cable as shown in figure 3-38.

c. Frequency Measurement.

- (1) Connect the test equipment as shown in A, figure 3-38.
- (2) Set the receiver AC POWER switch to ON.
- (3) Using the RCVR CHANNEL control on the receiver rf head, sequentially select the channels indicated in the chart below, and read the corresponding frequencies on the counter.

| Channel | Frequency (MHz) | Tolerance (Hz) |
|---------|-----------------|----------------|
| 40      | 62.500          | ± 630.0        |
| 51      | 63.875          | ± 630.0        |
| 52      | 64.000          | ± 640.0        |
| 119     | 72.375          | ± 720.0        |
| 120     | 48.333          | ± 480.0        |
| 410     | 72.500          | ± 720.0        |

d. Output Power Measurement.

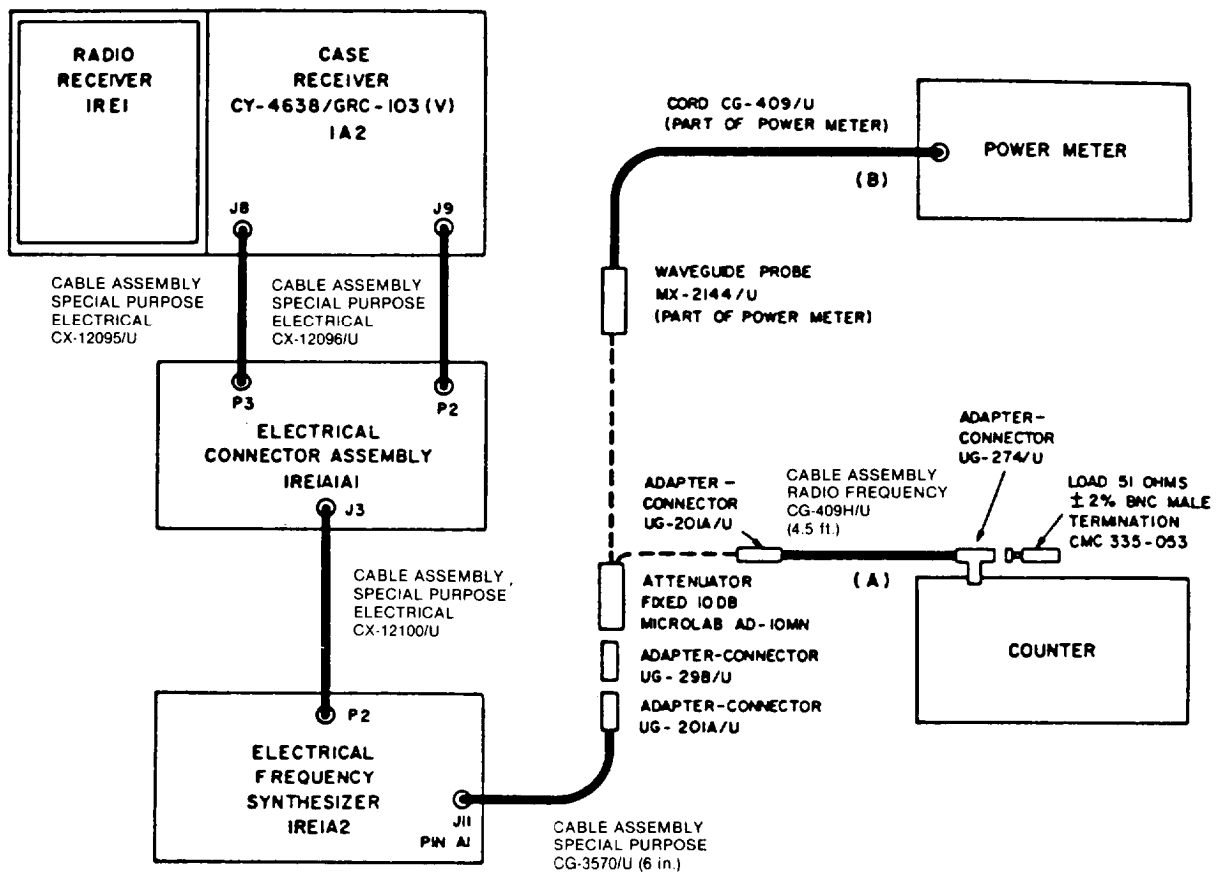
- (1) Disconnect the counter from the test setup used in c above.

- (2) Connect the power meter probe to the 10 db attenuator as shown in B, figure 3-38.
- (3) Measure the power output at channels 119 and 120. Set the channels using the RCVR CHANNEL control. The power output indication on the power meter as shown in the chart below is for modulator-oscillator 1RE1A2A2, Part No. CMC 456-260.

| Channel | Power output   |
|---------|----------------|
| 119     | +12.0 dbm±1 db |
| 120     | +16.0 dbm±1 db |

NOTE

When electrical frequency synthesizer is equipped with modulator-oscillator 1RE1A2A2, Part No. CMC 22(1-800159-000, power output should be +14 dbm±1.5 db at channels 119 and 120.



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Figure 3-38. Electrical Frequency Synthesizer 1RE1A2 Operational Check, Test Setup.

e. Conclusion of Operational Check.

- (1) Set the receiver AC POWER switch to OFF. Troubleshoot control indicator 2A2 as described in paragraph 3-33. If abnormal indications are obtained in either c or d above, to insure that electrical frequency synthesizer and not control-indicator 2A2 is defective.
- (2) Reinstall amplifier-frequency multiplier 1RE1A5 on 1RE1A2, or on the 1RE1A2 replacement, as described in chapter 6 of TM 11-5820-540-12. Reinstall 1RE1A2 as described in paragraph 3-59.

3-36. Amplifier-Frequency Multiplier 1RE1A5

a. Test Equipment Required.

| Equipment   | Common Name                  |
|---|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Counter, Electronic Digital Readout AN/USM-207        | Counter                      |
| Attenuator, Fixed, 10 dB, Microlab AD-10MN            | 10 dB attenuator             |
| Load, 51 ohms   | CMC 335-053                  |
| Adpater-Connector UG-201A/U (2 required)              |                              |
| Adapter-Connector UG-29B/U                            |                              |
| Adpater-Connector UG-274/U                            |                              |
| Cable Assembly, Special Purpose, Electrical           | CX-12097/U                   |
| Cable Assembly, Radio Frequency                       | CG-409H/U (4.5 ft.)          |
| Cable Assembly, Radio Frequency                       | CG-3579/U (6 in.)            |

b. Test Setup

- (1) Remove the receiver rf head from the receiver case and remove the dust cover as described in chapter 6 of TM 11-5820-540-12.
- (2) Connect the receiver rf head to the receiver case, using the CX-12097/U as shown in figure 3-39.
- (3) Disconnect rf head plug P2 (fig. 3-20) from connector J1 (2A1A3P2) on frequency multiplier 2A1A2A1.

c. Frequency Measurement.

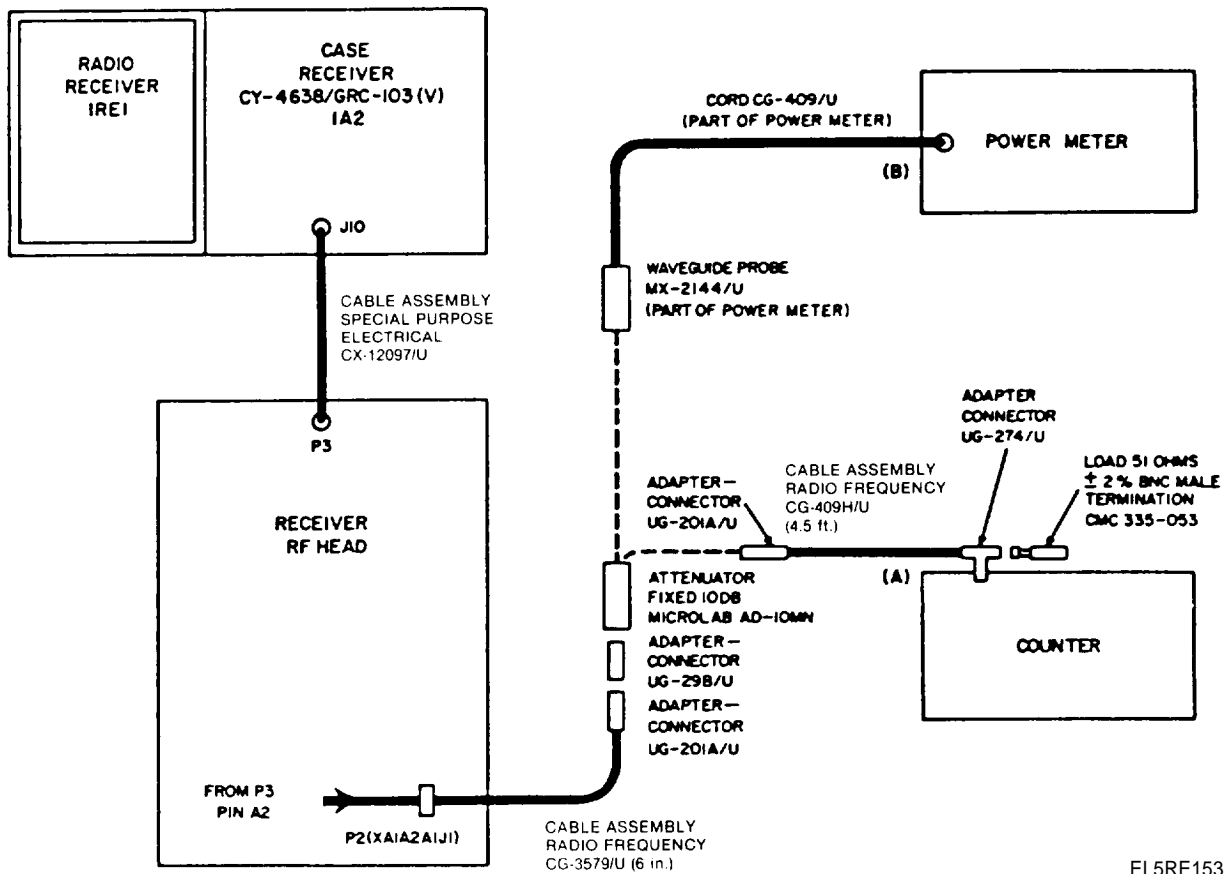
- (1) Connect the test equipment as shown in A, figure 3-39.
- (2) Set the receiver AC POWER switch to ON.
- (3) Using the RCVR CHANNEL control on the receiver rf head, sequentially select the channels indicated in the chart below and read the corresponding frequencies on the counter.

| Channel | Frequency (MHz ) | Tolerance (Hz) |
|---------|------------------|----------------|
| 119     | 144.750          | ± 2400.0       |
| 120     | 96.666           | ± 2400.0       |

d. Output Power.

- (1) Connect the test equipment as shown in B, figure 3-39.
- (2) Measure the power output at channels 119 and 120. Set the channels using the RCVR CHANNEL control. The power output indication on the power meter should be as shown in chart below.

| Channel | Power output  |
|---------|---------------|
| 119     | +14 dbm± 1 db |
| 120     | +14 dbm± 1 db |



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Figure 3-39 Amplifier Frequency Multiplier 1RE1A5 Operational Check, Test Setup.

e. Conclusion of Operational Checks. Set the receiver AC POWER switch to OFF. If abnormal indications are obtained in c and d above, replace amplifier-frequency multiplier 1RE1A5. Refer to chapter 6 of TM 11-5820-540-12 for replacement procedures.

3-37. Bandpass Filter 1RE1FL1

a. Test Equipment Required.

| Equipment                                     | Common Name         |
|---|---------------------|
| Generator, Signal, SG1170/U                   | Signal Generator    |
| Voltmeter, Electronic ME-30A/U                | VTVM                |
| Load, 51 ohms                                 | CMC 456-053         |
| Adpater-Connector UG-274/U                    |                     |
| Cable Assembly, Special Purpose, Electrical   | CX-12095/U          |
| Cable Assembly, Special Purposes, Electrical  | CX-12096/U          |
| Cable Assembly, Radio Frequency (2 required)) | CG-409H/U (4.5 ft.) |
| Cable Assembly, Radio Frequency               | CG-3578/U (6 in.)   |
| Cable Assembly, Radio Frequency               | CG-3581/U (6 in.)   |

b. Operational Check.

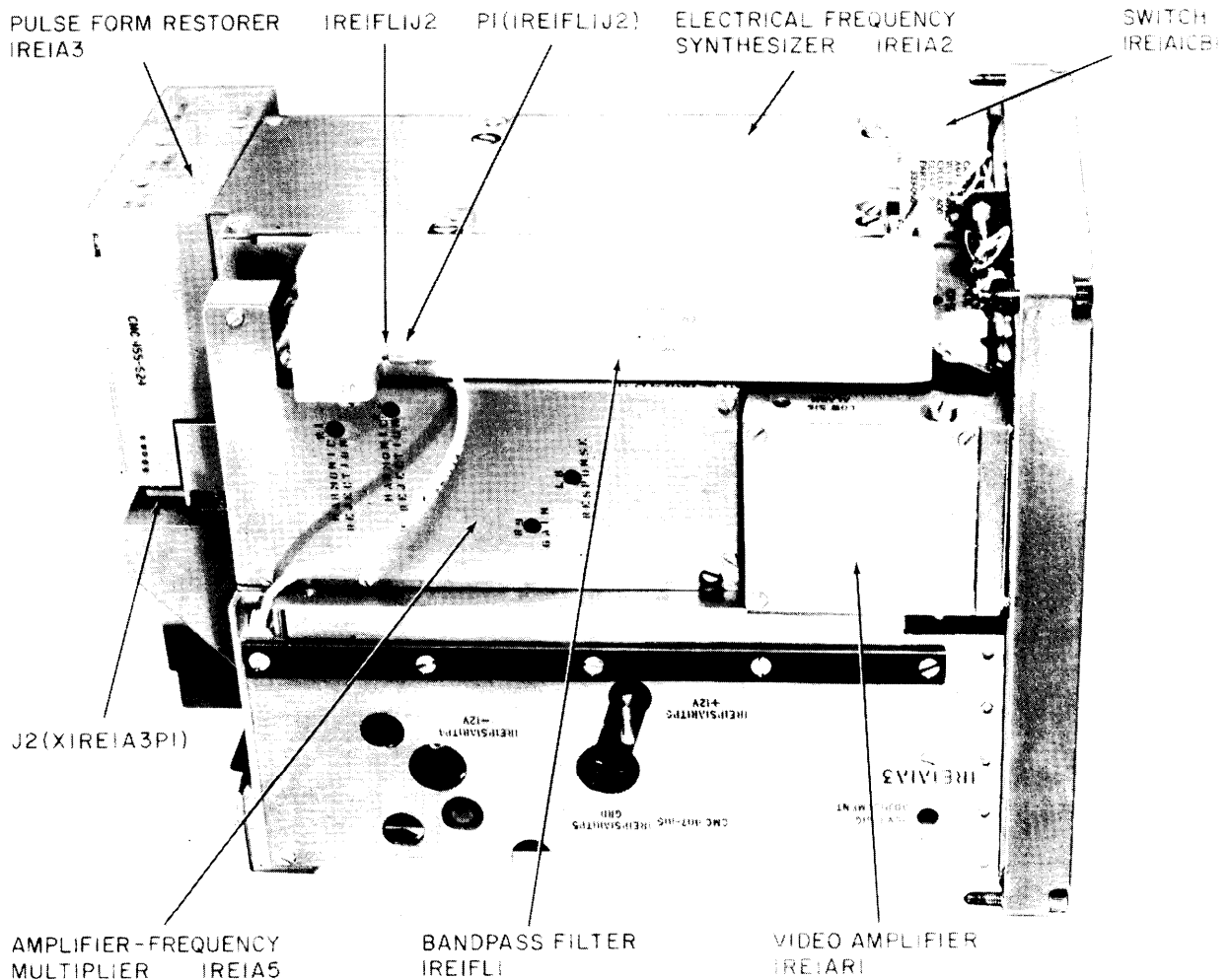
- (1) Disconnect plug P1 (1RE1FL1J2) (fig. 3-40) from connector J2 of bandpass filter 1RE1FL1.
- (2) Connect the test equipment as shown in A, figure 3-41.
- (3) Set the signal generator to 30 MHz.
- (4) Set the receiver AC POWER switch to ON.
- (5) Adjust the output of the signal generator until the VTVM indicates approxi-  
-50 dbm.
- (6) Adjust the frequency of the signal generator slightly for minimum indica-  
tion on the VTVM, and readjust the output level of the signal generator  
again for a reading of -50 dbm on the VTVM.
- (7) Note the attenuator setting on the signal generator.
- (8) Disconnect plug P2 (1RE1FL1J1) from connector J1 of 1RE1FL1.
- (9) Connect the test equipment as shown in B, figure 3-41.
- (10) Repeat (6) above.
- (11) The attenuator setting on the signal generator should not be more than 12  
db below the level noted in (7) above.



(12) Set the AC POWER switch to OFF. If the indication obtained in (11) above is not within the specified limit, replace bandpass filter 1RE1FL1. Refer to chapter 6 of TM 11-5820-540-12, for replacement procedures.

3-38. Intermediate Frequency Amplifier 1RE1AR2

| Equipment  | Common Name                  |
|--|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount HP-478A | Power Meter Thermistor Mount |
| Generator, Signal, SG-1170/U                         | Signal Generator             |
| Adapter-Connector UG-636A/U                          |                              |
| Adapter-Connector UG-29B/U                           |                              |
| Adapter-Connector UG-201A/U                          |                              |
| Cable Assembly, Special Purpose, Electrical          | CX-12095/U                   |



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Figure 3-40. Radio Receiver 1RE1, Bottom and Side View.

a. Test Equipment Required-Continued.

| Equipment                                   | Common Name         |
|---|---------------------|
| Cable Assembly, Special Purpose, Electrical | CX-12096/U          |
| Cable Assembly, Radio Frequency             | CG-409H/U (4.5 ft.) |
| Cable Assembly, Radio Frequency             | CMC 217-800000-000  |

b. Operational Check.

- (1) Remove electrical frequency limiter-discriminator 1RE1A4 as described in TM 11-5820-540-12 and connect it to intermediate frequency amplifier 1RE1AR2 using the CMC 217-800000-000 extender cable.
- (2) Connect the test equipment as shown in figure 3-42.

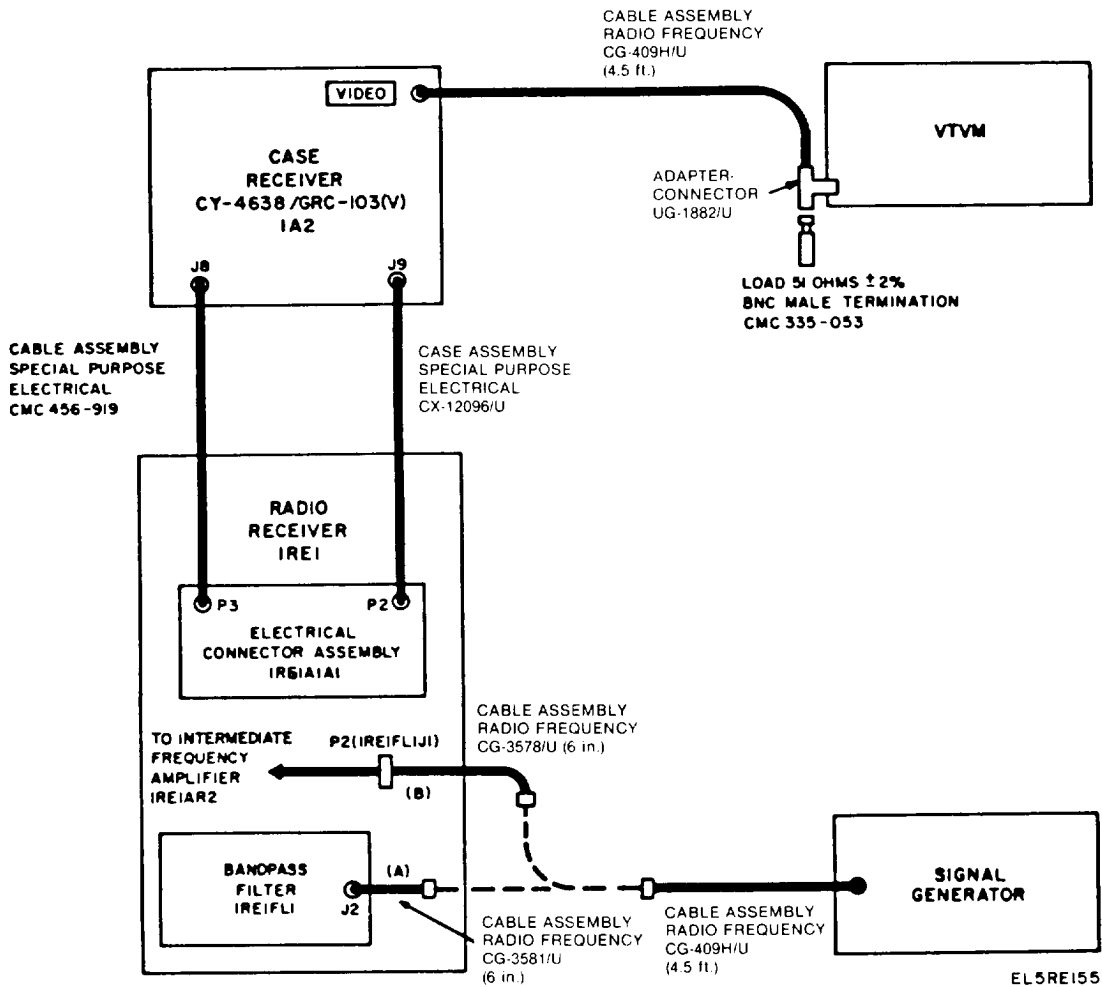


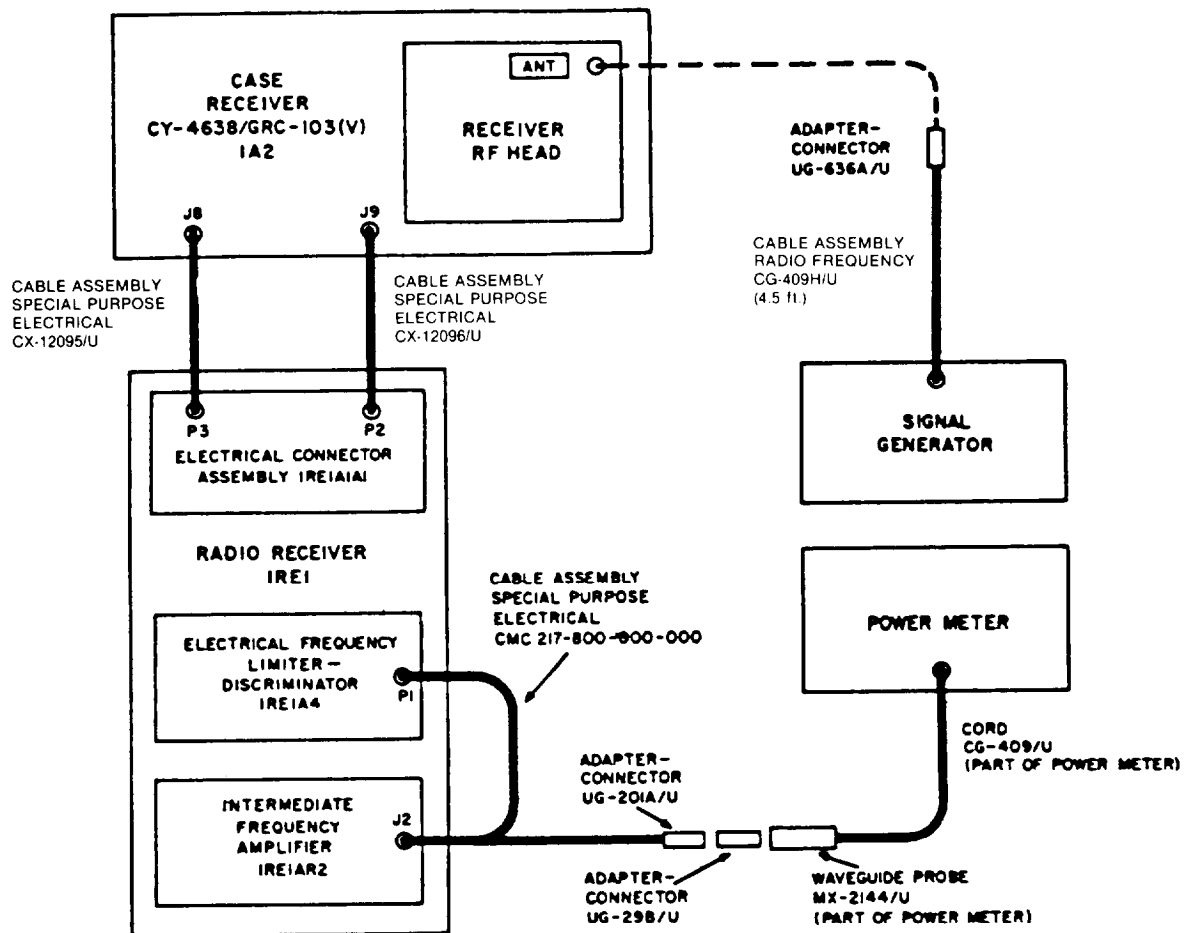
Figure 3-41. Bandpass Filter 1RE1FL1 Operational Check, Test Setup.

- (3) Set the signal generator to 300 MHz at a level of -74 dbm.
- (4) Set the receiver AC POWER switch to ON.
- (5) Tune the receiver to channel 200. The power meter should indicate between -1.5 dbm and -4.5 dbm.
- (6) If the indication in (5) above is outside the specified limits, replace intermediate frequency amplifier 1RE1AR2 as described in chapter 6 of TM 11-5820-540-12.

3-39. Electrical Frequency Limiter-Discriminator 1RE1A4

a. Test Equipment Required.

| Equipment                               | Common Name           |
|---|-----------------------|
| Generator, Signal, SG1171/U             | Wide Range Oscillator |
| Oscilloscope, Dual Trace, OS-261C(V)1/U | Oscilloscope          |



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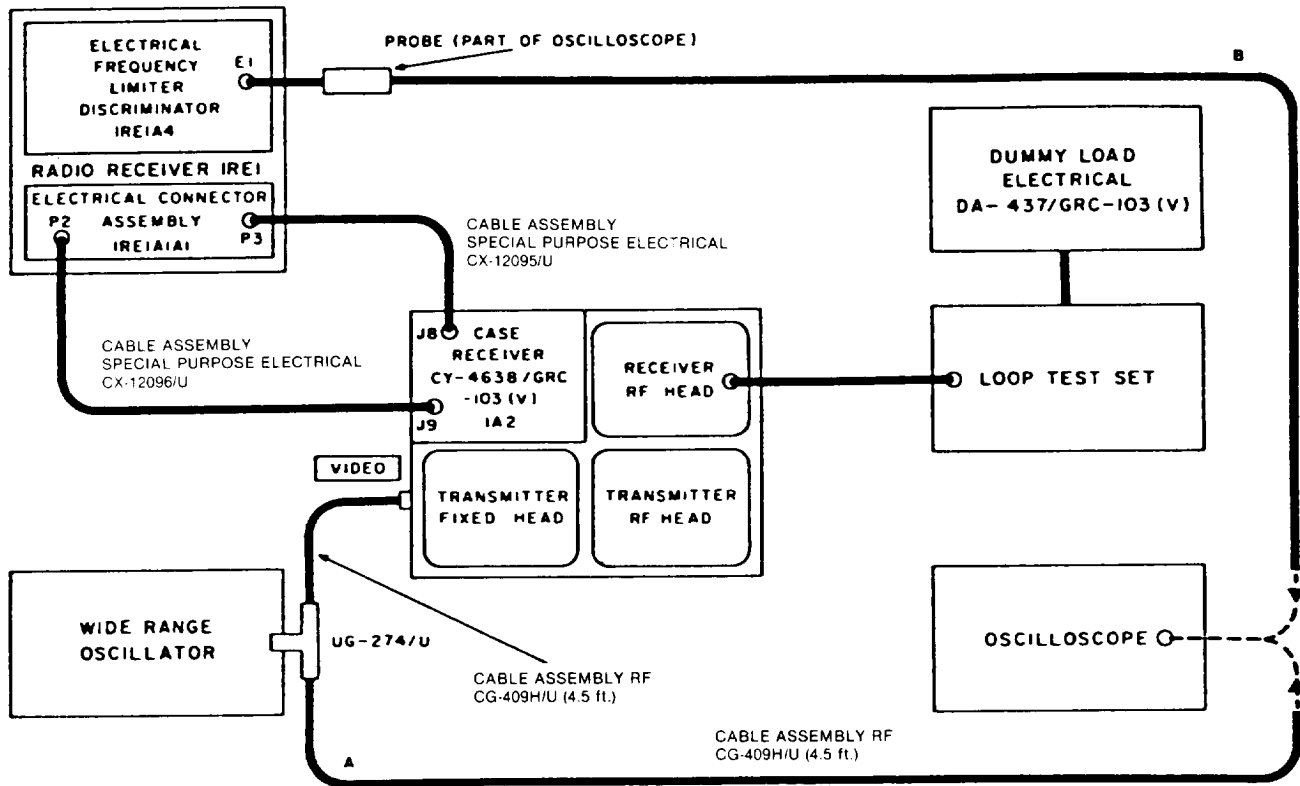
Figure 3-42. Intermediate Frequency Amplifier 1RE1AR2 Operational Check, Test Set.

a. Test Equipment Required-Continued.

| Equipment  | Common Name         |
|--|---------------------|
| Converter, Signal, Electronic<br>CV-2500/GRC     | Loop Test Set       |
| Dummy Load, Electrical<br>DA-437/GRC-103(v)      | Dummy load          |
| Adapter-Connector UG-274/U                       |                     |
| Cable Assembly, Special Purpose,<br>Electrical   | CX-12095/U          |
| Cable Assembly, Radio Frequency<br>(2 required)) | CG-409H/U (4.5 ft.) |

b. Operating Procedure.

- (1) Remove the six screws that secure the bottom cover plate to the case of electrical frequency limiter-discriminator 1RE1A4. Remove the cover plate.
- (2) Set up the loop test as described in paragraph 3-4, connecting the test equipment as shown in A, figure 3-43.



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Figure 3-43. Electrical Frequency Limiter-Discriminator, 1RE1A4 Operational Check, Test Setup.

- (3) Set the frequency of the wide range oscillator to 10 kHz and adjust the amplitude of the output signal to 2 volts peak-to-peak as measured on the oscilloscope. Disconnect the oscilloscope from the wide range oscillator, and connect the oscilloscope probe to 1RE1A4E1 as shown in B, figure 3-43.
- (4) Proceed with the loop test procedure as described in paragraph 3-4.

NOTE

Set the transmitter INPUT control for 50 percent of full scale meter deflection, with the transmitter meter switch in the 24 CH PCM position.

- (5) Using the oscilloscope, measure the voltage between ground and terminal E1 at the electrical frequency limiter-discriminator 1RE1A4 output. The oscilloscope should indicate between 250 and 400 millivolts peak-to-peak.
- (6) If the indication in (5) above is outside the specified limits, replace electrical frequency limiter-discriminator 1RE1A4. Refer to TM 11-5820-540-12 for replacement procedures.

3-40. Video Equipment 1RE1AR1

a. Test Equipment Required.

| Equipment   | Common Name           |
|---|-----------------------|
| Generator, Signal, SG-1171/U                                | Wide range oscillator |
| Oscilloscope, Dual Trace, OS-261C(V)/U                      | Oscilloscope          |
| Adapter-Connector UG-274/U<br>(2 required)                  |                       |
| Cable Assembly, Radio Frequency<br>(2 required)             | CG-409H/U (4.5 ft.)   |
| Cable Assembly, Radio Frequency                             | CG-3570/U             |
| Cable Assembly, Special Purpose,<br>Electrical              | CX-12095/U (6 in.)    |
| Cable Assembly, Special Purpose,<br>Electrical (2 required) | CX-12096/U            |

b. Operational Check.

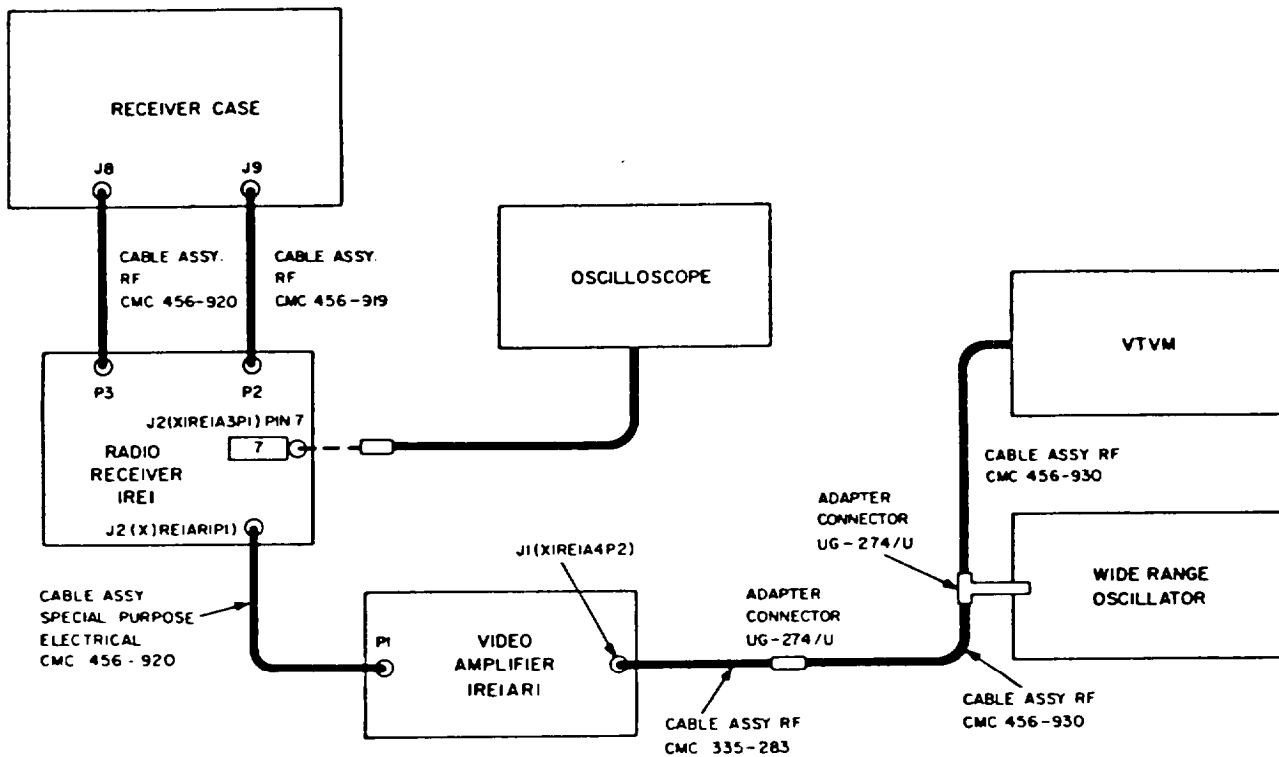
- (1) Remove pulse form restorer 1RE1A3 from radio receiver 1RE1 as described in chapter 6 of TM 11-5820-540-12.
- (2) Connect the test equipment as shown in figure 3-44.
- (3) Set the frequency of the wide range oscillator to 10 kHz and adjust the amplitude of the output signal to 106 millivolt rms as measured on the VTVM.
- (4) Using the oscilloscope probe, measure the open circuit voltage between pin 7 of J2 (X1RE1A3P1) and ground (fig. 3-40). The oscilloscope should display a 5.6 volt peak-to-peak undistorted 10 kHz sinewave.

- (5) If an abnormal display is obtained in (4) above, check continuity between pin 7 of J2 (X1RE1A3PI) and J2 X1RE1AR1P1) (FO-4-28 or 4-29).
- (6) If the wiring is normal, replace video amplifier 1RE1AR1. Refer to chapter 6 of TM 11-5820-540-12 for replacement procedures.

3-41. Pulse Form Restorer 1RE1A3 (SM-D-698146, CMC Part No. 2445-455624-000)

a. Test Equipment Required.

| Equipment  | Common Name           |
|--|-----------------------|
| Generator, Signal, SG-1171/U                           | Wide Range Oscillator |
| Oscilloscope, Dual Trace, OS-261C(V)/U                 | Oscilloscope          |
| Converter, Signal Frequency, Electronic CV-1500( )/GRC | Loop test set         |
| Dummy Load, Electrical DA-437/GRC-103 (v)              | Dummy load            |
| Load, 91 ohms  | CMC 335-052           |
| Adapter-Connector UG274/U (2 required)                 |                       |
| Cable Assembly, Radio Frequency (2 required)           | CG-409H/U (4.5 ft.)   |



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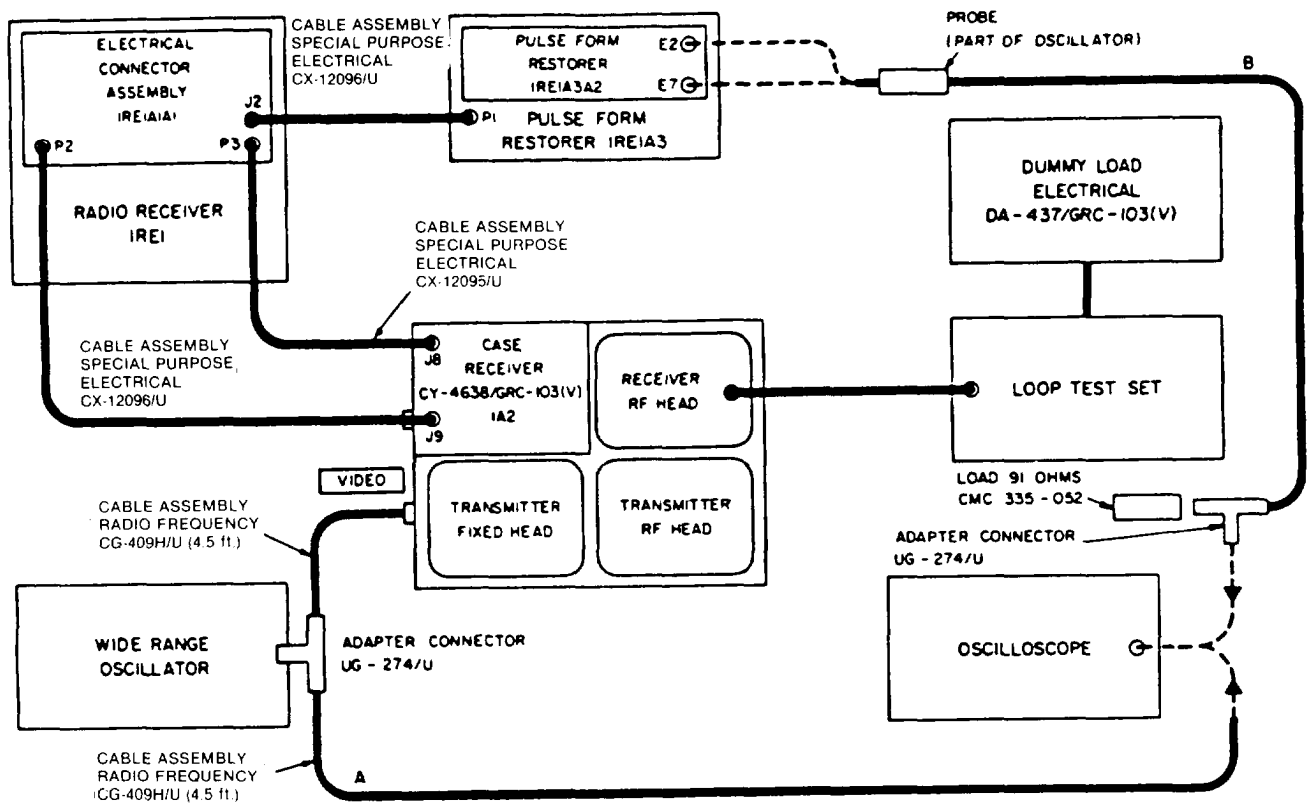
Figure 3-44. Video Amplifier 1RE1AR1 Operational Check, Test Setup.

a. Test Equipment Required-Continued.

| Equipment  | Common Name |
|--|-------------|
| Cable Assembly, Special Purpose, Electrical              | CX-12095/U  |
| Cable Assembly, Special Purpose, Electrical (2 required) | CX-12096/U  |

b. Operational Check.

- (1) Remove pulse form restorer 1RE1A3 from radio receiver 1RE1, as described in chapter 6 of TM 11-5820-540-12.
- (2) Connect the test equipment as shown in figure 3-45.
- (3) Remove the cover plate of pulse form restorer 1RE1A3, secured to the unit case with four countersunk screws.
- (4) Remove the four screws that secure pulse form restorer 1RE1A3A2 board to the unit case. Carefully Dull the board away from the case until terminals E2 and E7 are accessible;



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Figure 3-45. Pulse Form Restorer 1RE1A3 Operational Check, Test Setup.

- (5) Proceed with the loop test procedure as described in chapter 6 of TM 11-5820-540-12.

NOTE

Set the transmitter INPUT control for 50 percent of full scale meter deflection with the transmitter meter switch in the 12 CH PCM position.

- (6) Connect the oscilloscope test lead between terminal E2 on pulse form restorer 1RE1A3A2 board and ground. A 2 volt peak-to-peak square wave should be displayed on the oscilloscope.
- (7) Connect the oscilloscope test lead between terminal E7 on the pulse form restorer 1RE1A3A2 board and ground. A 2 volt peak-to-peak positive-going timing spike should be displayed on the oscilloscope (fig. 3-46).
- (8) If abnormal indications are obtained in (6) or (7) above, replace pulse form restorer 1RE1A3. Refer to chapter 6 of TM 11-5820-540-12 for replacement procedures.

3-42. Pulse Form Restorer 1RE1A3 (SM-D-990510, CMC Part No. 245-803110-000)

a. Test Equipment Required.

| Equipment   | Common Name                                  |
|---|--|
| Synthesizer, Function generator HP3325A<br>Oscilloscope, Dual Trace, OS-261C(V)/U<br>Converter, Signal Frequency Electronic<br>CV-2500( )/GRC | Synthesizer<br>Oscilloscope<br>Loop test set |
| Dummy Load, Electrical DA-437/GRC-103(V)<br>Load, 91 ohms Adapter-Connector UG-274/U<br>(2 required)  | Dummy load<br>CMC 335-052                    |
| Cable Assembly, Radio Frequency<br>(2 required)   | CG-409H/U (4.5 ft.)                          |
| Cable Assembly, Special Purpose, Electrical   | CX-12095/U                                   |
| Cable Assembly, Special Purpose, Electrical<br>(2 required)   | CX-12096/U                                   |



b. Operational Check.

- (1) Remove Pulseform Restorer 1RE1A3 from Radio Receiver 1RE1, as described in Chapter 6 of TM 11-5820-540-12.
- (2) Connect the equipment as shown in figure 3-47.
- (3) Remove the cover plate (DCDR CLK and PHASE ADJ side) of pulseform restorer 1RE1A3, secured to the unit case with three countersunk screws.
- (4) Proceed with the loop test procedure as described in Chapter 6, paragraph 6-10 of the TM 11-5820-540-12.

## NOTE

Disregard also paragraphs 6-10 (29) (30) in the TM 11-5820-540-12 and replace them with steps (5) and (6) below

- (5)(a) Set the synthesizer for a square wave output of 576 kHz at 1.12 v peak-to-peak.
  - (b) Adjust the transmitter INPUT control for 50 percent full scale deflection (FSD) with the transmitter meter switch to the 12 CH PCM position.
  - (c) The receiver meter should indicate in the green band with the meter switch set to 12 CH PCM.
  - (d) Connect the oscilloscope probe to terminal E13 on electrical synchronizer board 1RE1A3A4. A 4 volt peak-to-peak square wave with a period of 3.4 usec should be displayed on the oscilloscope.
  - (e) Connect the oscilloscope probe to terminal E7 on electrical synchronizer board 1RE1A3A4. A 2 volt peak-to-peak timing spike should be observed on the oscilloscope (fig. 3-48) (period of 1.74 usec).
- (6)(a) Place termination connector (Part No. 243-800012) on the COMB. 0W. connector on the back of the receiver radio. Set the synthesizer for a square wave output of 1152 kHz at a level of 1.86 volts peak-to-peak.
  - (b) Adjust the transmitter INPUT control for 50 percent FSD with the transmitter meter switch to the 24 CH PCM position.
  - (c) The receiver meter should indicate in the green band with the meter switch set to either 12 CH PCM or 24 CH PCM.
  - (d) Connect the oscilloscope probe to terminal E13 on electrical synchronizer board 1RE1A3A4. A 4 volt peak-to-peak square wave with a period of 1.74 usec should be displayed on the oscilloscope.

(e) Connect the oscilloscope probe to terminal E7 on electrical synchronizer board 1RE1A3A4. A 2 volt peak-to-peak timing spike should be observed on the oscilloscope (period of 0.87 usec).

(7) If abnormal indications are obtained in (5)(c), (d), (e), or (6)(c), (d), (e) above, replace pulse form restorer 1RE1A3. Refer to Chapter 6 of TM 11-5820-540-12 for replacement procedures.

3-43. Order Wire Unit

NOTE

The complete radio set is required to troubleshoot the order wire unit boards. Extend amplifier assembly 9A4 and telephone signal converter 9A3 boards using two CX-12102/U cables (fig. 3-49).

a. Test Equipment Required

| Equipment  | Common Name   |
|--|---|
| Voltmeter, Electronic, ME-30A/U<br>Converter, Signal Frequency, Electronic<br>CV-2500( )/GRC<br>Dummy Load, Electrical DA-437/GRC-103(V)<br>Cable Assembly, Special Purpose,<br>Electrical | VTVM<br>Loop test set<br><br>Dummy load<br>CX-12102/U |

b. Operational Check.

(1) Set up the loop test as described in chapter 6 of TM 11-5820-540-12.

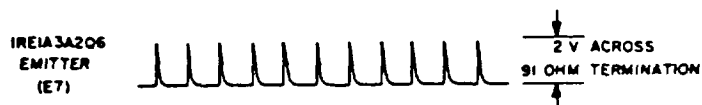
NOTE

It is not necessary to connect multiplex equipment to the radio set.

(2) Proceed with the loop test procedures described in chapter 6 of TM 11-5820-540-12.

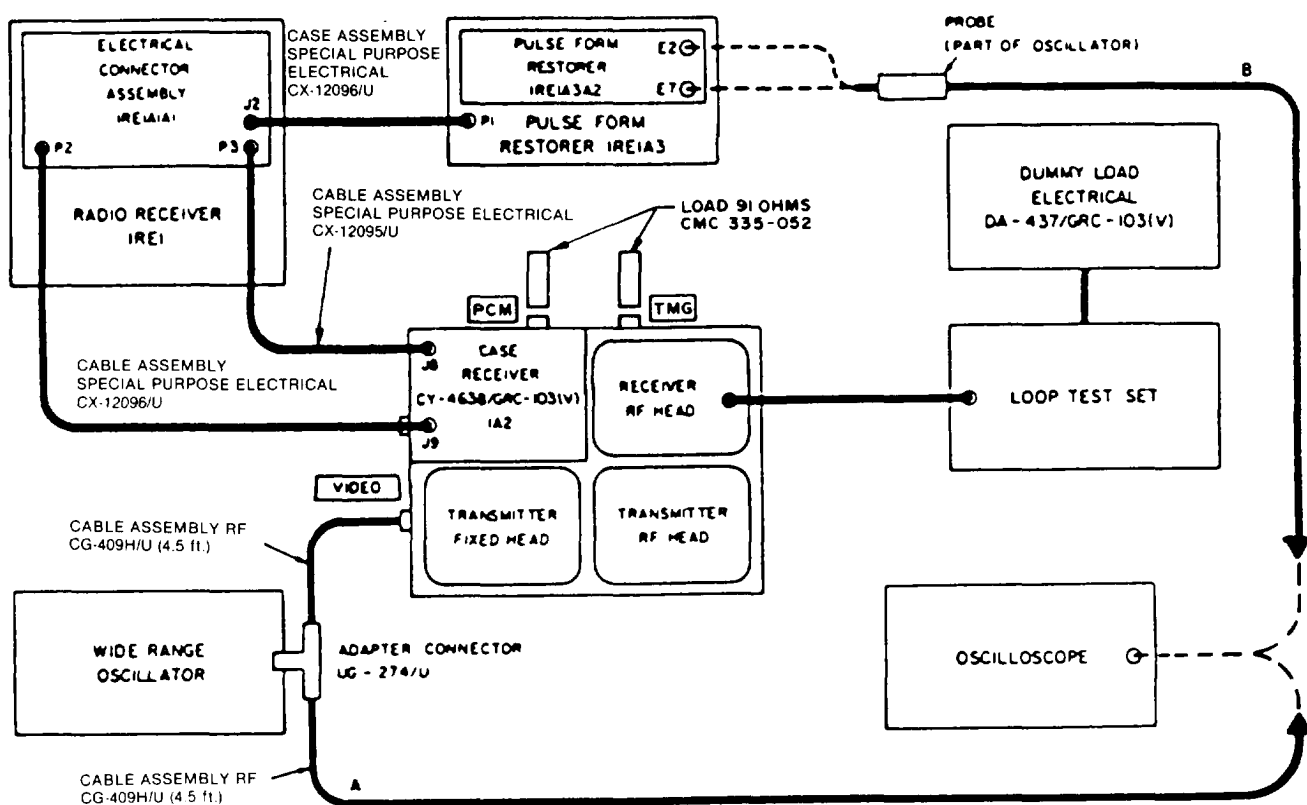
(3) Press order wire unit RING button located on monitor panel 9A2 (fig. 3-49) .

(4) Using the VTVM, measure the power level between TP4 and TP2 (Grid) on amplifier assembly 9A4. The VTVM should indicate -7.2 dBm ±0.5 db.



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Figure 3-46. Pulse Form Restorer 1RE1A3, Timing Pulses.



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Figure 3-47. Pulse Form Restorer 1RE1A3, Operational Setup.

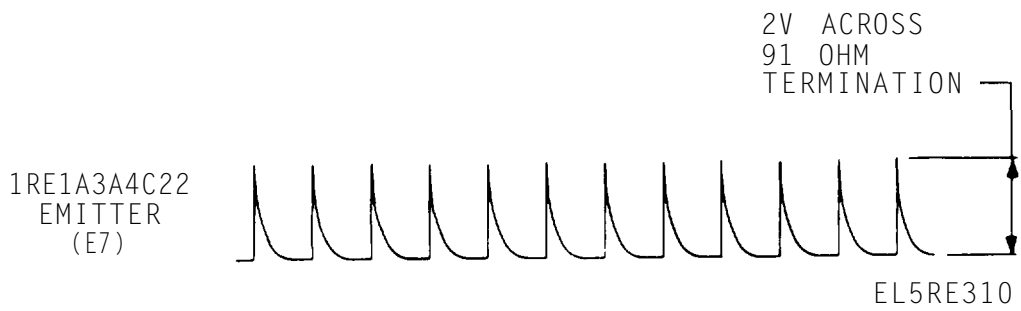


Figure 3-48. Pulse Form Restorer 1RE1A3, Timing Pulses.

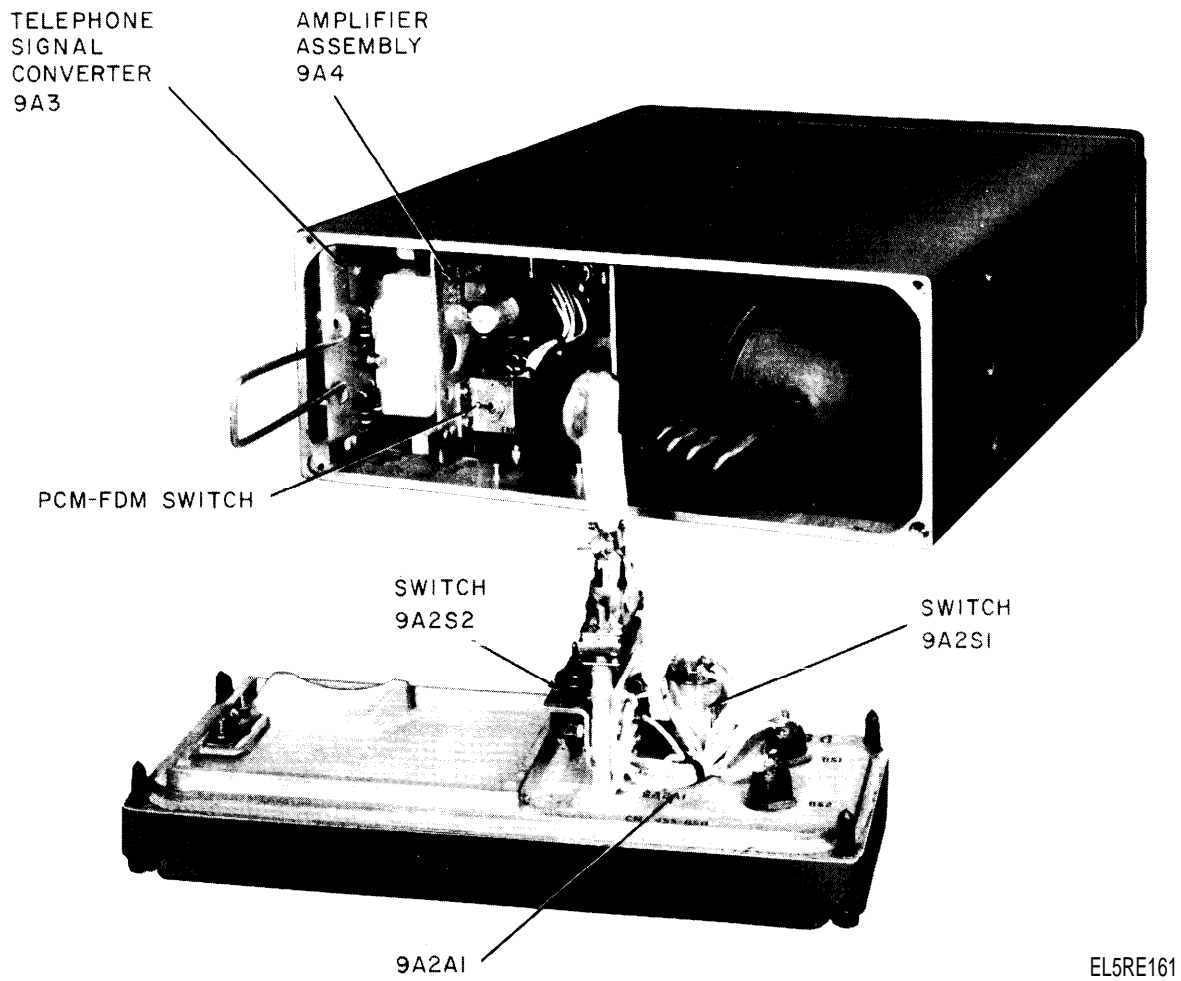


Figure 3-49. Order Wire Unit, Monitor Panel 9A2.

- (5) If the indication obtained in (4) above is outside the specified limits, replace telephone signal converter 9A3.
- (6) Press the RING button.
- (7) Using the VTVM measure the level at the amplifier assembly 9A4 test points as shown in the chart below.

| Test point           | Signal Level         |
|----------------------|----------------------|
| TP1 to TP2 . . . . . | -10 dbm $\pm$ 3.0 dB |
| TP9 to TP2 . . . . . | -10 dbm $\pm$ 1.0 dB |
| TP7 to TP2 . . . . . | 24 dbm $\pm$ 1.0 dB  |

- (8) Disconnect Cable Assembly, Special Purpose, Electrical, Branched CX-10763/GRC-103(V) from the TO RADIO connector of the order wire unit and connect it to the PATCH THRU connector.
- (9) Press RING button.
- (10) Using the VTVM, measure the level at the amplifier assembly 9A4 test points as shown in the chart below.

| Test point            | Signal Level         |
|-----------------------|----------------------|
| TP3 to TP2 . . . . .  | -10 dbm $\pm$ 1.0 dB |
| TP10 to TP2 . . . . . | -10 dbm $\pm$ 3.0 dB |
| TP7 to TP2 . . . . .  | -24 dbm $\pm$ 1.0 dB |

- (11) If abnormal indications are obtained in (10) above, replace amplifier assembly 9A4.
- (12) If abnormal indications persist, refer to higher category maintenance.

Section III. MODULE REMOVAL AND REPLACEMENT PROCEDURES

3-44. General

When trouble has been localized to a module of the radio set, replace the defective part as described in paragraphs 3-46 to 3-69. Before installing a replacement module, always check connector for bent or damaged pins. Do not tighten the module mounting" screws to press home connectors. Whenever difficulty is encountered in mating connectors, remove the module and inspect the connectors for damage.

3-45. Equipment Required

The following equipment is required for the replacement of power monitor 6AR1A3, frequency multiplier assembly 6A2, and power monitor 2A1A5.

| Description   | Manufacturers number | Qty |
|---|----------------------|-----|
| Socket wrench 7/8 inch . . . . .                      |                      | 1   |
| Cable Assembly, Special Purpose, Electrical . . . . . | CX-12094/U . . . . . | 1   |

3-46. General Module Replacement Procedures

a. Transmitter, Radio T-983(P)/GRC-103(V), T-983A(P)/GRC-103(V) or T-98313(P)/GRC-103TV) Modules. To replace a module first remove radio transmitter TR1 from the transmitter case as described in chapter 6 of TM 11-5820-540-12. To replace centrifugal fan 5A2B1, the transmitter rf head must also be removed from the transmitter case, as described in chapter 6 of TM 11-5820-540-12.

b. Amplifier-Frequency Multiplier AM-4320/GRC-103(V), AM-4320A/GRC-103(V) and AM-4320B/GRC-103(V) Modules. To replace a module first remove the transmitter rf head from the transmitter case. as described in chapter 6 of TM 11-5820-540-12. then remove the transmitter rf head dust cover, which is secured to the unit with nine screws. Reinstall the dust cover after replacing the faulty module.

c. Receiver, Radio R-1329(P)/GRC-103(V), R-1329A(P)/GRC-103(V) or R-1329B(P)/GRC-103(V) Modules. To replace module remove radio receiver from the receiver case as described in chapter 6 of TM 11-5820-540-12.

d. Amplifier-Converter AM-4316/GRC-103(V) or AM-4316A/GRC-103(V) Modules. To replace a module of this unit, first remove the receiver rf head from the receiver case, as described in chapter 6 of TM 11-5820-540-12, then remove the receiver rf head dust cover, which is secured to the unit with twelve screws and two hexagonal nuts on the locating pins. Reinstall the dust cover after replacing the faulty module.

e. Receiver-Transmitter, Order Wire RT-773/GRC-103(V) Modules. Replacement of telephone signal converter 9A3 and amplifier assembly 9A4 is covered in chapter 6 of TM 11-5820-540-12.

3-47. Replacement of Amplifier-Monitor 5TR1A5, Alarm Control 5TR1A3 and Centrifugal Fan 5A2B1

Replacement of the amplifier-monitor and the alarm control is covered in chapter 6, TM 11-5820-540-12. Refer to section X of this chapter for the centrifugal fan.

3-48. Replacement of Electrical Frequency Synthesizer 5TR1A2

- a. Place radio transmitter 5TR1 bottom side up and locate 5TR1A2 (fig. 3-3).
- b. Loosen the four green-circled screws and lift 5TR1A2, together with amplifier-monitor 5TR1A5 and amplifier-frequency multiplier 5TR1A4, straight up from the chassis to disengage the connectors. If the connectors do not separate easily, pry the chassis and modules apart with a screwdriver but do not touch the mating connectors.
- c. Locate and loosen the two green-circled mounting screws that secure amplifier-monitor 5TR1A5 to 5TR1A2 and remove the module.
- d. Loosen the two green-circled mounting screws that secure amplifier-frequency multiplier 5TR1A4 to 5TR1A2 and pull straight away to disengage the connectors.
- e. To install the 5TR1A2 replacement module, first mount and secure 5TR1A4 on 5TR1A2. Then place 5TR1A2 in position over its chassis connector and press down to engage the connector. Tighten the four mounting screws.
- f. Reinstall amplifier-monitor 5TR1A5, as described in chapter 6 of TM 11-5820-540-12.

3-49. Replacement of Amplifier-Frequency Multiplier 5TR1A4

- a. Replacement of 5TR1A4 is a second-order removal. Electrical frequency synthesizer 5TR1A2 must be removed first, as described in paragraph 3-48.
- b. Loosen the two green-circled mounting screws that secure 5TR1A4 to 5TR1A2; pull 5TR1A4 straight away from 5TR1A2 to disengage the connectors.
- c. To install the 5TR1A4 replacement module, place the module in position against 5TR1A2. then press in until the connectors are fully engaged. The holes for the mounting screws are not properly aligned unless the connectors are fully engaged.
- d. Tighten the two mounting screws.
- e. Reinstall 5TR1A2 with its attached modules as described in paragraph 3-48.



## 3-50. Replacement of Power Supply 5TR1PS1

- a. Replacement of 5TR1PS1 is a second-order removal. Electrical frequency synthesizer 5TR1A2 must be removed first as described in paragraph 3-48.
- b. Locate and loosen the eight green-circled screws that secure 5TR1PS1 to the chassis. Place radio transmitter 5TR1 upright and lift 5TR1PS1 straight up from the chassis until the large multipin connector is disengaged.
- c. To install the 5TR1PS1 replacement module, place it in position above the chassis then press straight down until the connector is fully engaged. Turn radio transmitter 5TR1 on its left or right side and tighten the eight mounting screws securing 5TR1PS1 to the chassis.
- d. Place radio transmitter 5TR1 bottom side up and reinstall 5TR1A2 with its attached modules, as described in paragraph 3-48.

## 3-51. Replacement of Alarm Control 5TR1A1A2

- a. Place radio transmitter 5TR1 bottom side up and locate alarm control 5TR1A1A2 (fig. 3-3).
- b. Locate electrical frequency synthesizer 5TR1A2 and remove it, with associated modules, as described in paragraph 3-48.
- c. Unsolder, and identify with tags, the wires at terminals E1 and E14 and E17.
- d. Loosen the two mounting screws and remove the 5TR1A1A2 board.
- e. Install the new 5TR1A1A2 board and tighten the two mounting screws.
- f. Reconnect and resolder the wires removed in c above.
- g. Reinstall 5TR1A2, with its attached modules, as described in paragraph 3-48.

## 3-52. Replacement of Buzzer 5TR1A1DS5

- a. Place radio transmitter 5TR1 bottom side up and locate buzzer 5TR1A1DS5 (fig. 3-3).
- b. Locate electrical frequency synthesizer 5TR1A2 and remove it, with associated modules, as described in paragraph 3-48.
- c. Unsolder the two wires from the 5TR1A1DS5 terminals; note the polarity and tag the leads. Loosen the green-circled screws and remove 5TR1A1DS5.
- d. To install the 5TR1A1DS5 replacement module, position the module over the two mounting holes and tighten the mounting screws. Resolder the two wire leads to their appropriate terminals.
- e. Reinstall 5TR1A2 with its attached modules as described in paragraphs 3-48.

3-53. Replacements of Electronic Switch 6A1 and Control-Indicator 6A3

Replacement of electronic switch 6A1 and control-indicator 6A3 is covered in chapter 6 of TM 11-5820-540-12.

3-54. Replacement of Low Pass Filter 6AR1A2FL1

- a. Place the transmitter rf head top side up and locate low-pass filter 6AR1A2FL1 on the right-hand side.
- b. Disconnect the two rf leads, P1 (6AR1A1J2) and P2 (XAR1A3J1), from their respective mating connectors.
- c. Loosen the two green-circled mounting screws that secure 6AR1A2FL1 to the chassis. Remove 6AR1A2FL1.
- d. To install the 6AR1A2FL1 replacement module, position the module over the two mounting holes and tighten the mounting screws. Connect plugs P1 (6AR1A1J2) and P2 (XAR1A3J1), at the ends of rf leads, to mating connectors J2 of amplifier subassembly 6AR1A1 and J1 of power monitor 6AR1A3 respectively.

3-55. Replacement of Power Monitor 6AR1A3

- a. Place the transmitter rf head top side up and locate power monitor 6AR1A3 at the top right side.
- b. On the front panel of the transmitter rf head, loosen and remove the hexagonal nut that secures the PWR OUT connector to the front panel.
- c. Loosen the two screws that secure plug P1 (XW1J3) to its connector. Disconnect the P2 (XAR1A3J1) lead from connector J1 of 6AR1A3 (fig. 3-14).
- d. Remove the four screws that secure power monitor 6AR1A3 to its bracket and remove the module.
- e. To install the 6AR1A3 replacement, slide connector J2 of the power monitor into the PWR OUT opening in the front panel and secure with the hexagonal nut. Secure 6AR1A3 to its mounting bracket with four screws.

NOTE

The PWR OUT connector must be well secured before tightening the 6AR1A3 mounting screws.

- f. Connect the P2 (XAR1A3J1) rf lead to connector J1 of 6AR1A3. Connect plug P1 (XW1J3) to connector 6W1J3 on the chassis and secure with two screws.

3-56. Replacement of Frequency Multiplier Assembly 6A2

NOTE

Replacement of frequency multiplier assembly 6A2 requires electromechanical alignment and should not be attempted unless absolutely necessary.

## NOTE

Rf Power Level Control 6A5 is not part of AM-4320A/GRC-103(V) or AM-4320B/GRC-103(V).

a. Equipment Required.

| Equipment                                      | Common Name |
|--|-------------|
| Dummy Load, Electrical DA-437/GRC-103(V)       | Dummy load  |
| Cable Assembly, RF CG-3444/U<br>(1 ft. 6 in.)  |             |
| Cable Assembly, Special Purpose,<br>Electrical | CX-12094/U  |

- b. Set the transmitter rf head XMTR TUNE and XMTR CHANNEL controls to channel 340.
- c. Set the transmitter rf head top side up and locate frequency multiplier assembly 6A2 (fig. 3-6). Locate electronic switch 6A1 and disconnect the rf leads from the J1, J2, J3, J4 and J6 connectors. Disconnect the rf lead from the 6W2J1 chassis connector (from rf power level control 6A5). Disconnect the rf lead from the J2 connector of rf power level control 6A5.
- d. Loosen the four red-circled screws that secure frequency multiplier assembly 6A2 to the chassis. Slide 6A2 away from the front panel to disengage the flexible drive shaft. Remove the module from the transmitter rf head.
- e. Loosen the two green-circled screws that secure rf power level control 6A5 to frequency multiplier assembly 6A2. Remove the 6A5 module.
- f. To install the 6A2 replacement module, first secure rf power level control 6A5 to frequency multiplier assembly 6A2 replacement with the two screws provided.
- g. Set the transmitter rf head XMTR TUNE and XMTR CHANNEL controls to channel 340.

## NOTE

The 6A2 replacement module is shipped with its shaft clamped to channel 340. Remove the throwaway clamp carefully to avoid disturbing the shaft position.

- h. Lower the 6A2 replacement module into position on the chassis but do not connect it to the flexible drive shaft. Connect the rf leads to electronic switch 6A1 as shown in the chart below:

| Rf lead   | Connects to 6A1 connector |
|-----------|---------------------------|
| P4(XA1J1) | J1                        |
| P3(XA1J2) | J2                        |
| P2(XA1J3) | J3                        |
| P1(XA1J4) | J4                        |

NOTE

In Amplifier-Frequency Multiplier AM1-4320A/GRC-103(V) and AM-4320B/GRC-103(V), the connections are as shown below:

| Rf lead   | Connects to 6A1 connector |
|-----------|---------------------------|
| P4(6A1J1) | J1                        |
| P3(6A1J2) | J2                        |
| P2(6A1J3) | J3                        |
| P1(6A1J4) | J4                        |

- i. Connect the P1 (XA1J6) and P2 (6W2J1) rf leads of 6A5 to connector J6 of 6A1 and to chassis connector 6W2J1 respectively. Connect P1 (6A5J2) rf lead to connector J2 of 6A5.
- j. Connect the dummy load to the PWR OUT connector of the transmitter rf head using Cable Assembly, RF CG-3444/U (1 ft. 6 in.). Connect cable CX-12094/U between the transmitter case and the transmitter rf head.

**WARNING**

Do not touch the exposed filter-connectors on connector filter assembly 6AR1A2A3. Dangerous voltages exist at these filter-connectors.

- k. Set the transmitter meter switch to the MULT position and the AC POWER switch to ON/RESET.
- l. Carefully rotate the shaft of frequency multiplier assembly 6A2 until a maximum indication is obtained on the transmitter meter. It should not be necessary to rotate the shaft more than 90 degrees from its original position.
- m. Set the transmitter meter switch to the DRIVER and PWR OUT positions in turn, and check to see that the meter indicates between 25 percent and 90 percent of full scale when using the transmitter rf head PWR OUT PEAK control.
- n. If the meter indication in m above cannot be obtained, repeat l above.

- o. Set the AC POWER switch to OFF.
- p. Carefully slide the shaft of frequency multiplier assembly 6A2 into the coupling of the flexible drive shaft. Secure 6A2 to the chassis with the four screws provided.
- q. Set the AC POWER switch to ON/RESET.
- r. Set the XMTR TUNE and XMTR CHANNEL controls to channel 40.
- s. Set the transmitter meter switch to MULT position. Check to see that the meter indicates between 25 percent and 90 percent of full scale.
- t. Set the meter switch to the DRIVER and PWR OUT positions in turn, and check to see that the meter indicates between 25 percent and 90 percent of full scale when tuning the PWR OUT PEAK control.
- u. If the meter indications are below normal in MULT, DRIVER and PWR OUT positions, reset the XMTR TUNE and XMTR CHANNEL controls to channel 340 and repeat steps 1 through t above.
- v. Repeat steps through t above for channels 179, 180 and 400.
- w. Set the AC POWER switch to OFF. Disconnect the CX-12094/U cable from the transmitter case and the transmitter rf head. Disconnect the dummy load, from Cable Assembly, RF CG-3444/U (1 ft. 6 in.).

### 3-57. Replacement of Rf Power Level Control 6A5

#### NOTE

Used only in Amplifier-Frequency Multiplier AM-4320/  
GRC-103(V).

- a. Place the transmitter rf head upright and locate 6A5 (fig. 3-6).
- b. Disconnect the rf lead from chassis connector 6W1J1, and the rf lead from connector J6 of electronic switch 6A1.
- c. Loosen and remove the two green-circled screws and remove the 6A5 module.
- d. Install the new 6A5 module and tighten the two green-circled mounting screws. Connect the P2 (6W1J1) lead to chassis connector 6W1J1 and the P1 (QA1J6) lead to the connector of electronic switch 6A1.

### 3-58. Replacement of Power Supply 1RE1PS1, Pulse Form Restorer 1RE1A3, Electrical Frequency Limiter-Discriminator 1RE1A4, Intermediate Frequency Amplifier 1RE1AR2, Amplifier-Frequency Multiplier 1RE1A5, Bandpass Filter 1RE1FL1 and Video Amplifier 1RE1AR1

Replacement of these modules is described in chapter 6 of TM 11-5820-540-12.

3-59. Replacement of Electrical Frequency Synthesizer 1RE1A2

- a. Place radio receiver 1RE1 bottom side up and locate 1RE1A2 (fig. 3-40). Disconnect the leads from connector J2 of bandpass filter 1RE1FL1 and connector J1 of video amplifier 1RE1AR1.
- b. Loosen the four green-circled screws and lift 1RE1A2 with the attached modules straight up from chassis to disengage the connectors. If the connectors do not separate easily, pry chassis and module apart with a screwdriver but do not touch the mating connectors.
- c. On 1RE1A2, locate pulse form restorer 1RE1A3, electrical frequency limiter-discriminator 1RE1A4, intermediate frequency amplifier 1RE1AR2, amplifier-frequency multiplier 1RE1A5 and bandpass filter 1RE1FL1. Remove each of these modules as described in chapter 6 of TM 11-5820-540-12.
- d. To reinstall the 1RE1A2 replacement module, first attach the modules listed in c above to 1RE1A2, as described in chapter 6 of TM 11-5820-540-12. Place 1RE1A2 in position on the chassis and press straight down to engage the connectors. Tighten the four mounting screws.
- e. Connect the P1 (1RE1FL1J2) rf lead to connector J2 of 1RE1FL1, and plug P2 from 1RE1A4 to connector J1 of 1RE1AR1.

3-60. Replacement of Buzzer 1RE1A1DS5

- a. Place radio receiver 1RE1 upright and locate module 1RE1A1DS5 (fig. 3-37) behind the front panel.
- b. Remove power supply 1RE1PS1 as described in chapter 6 of TM 11-5820-540-12.
- c. Unsolder the two leads from the 1RE1A1DS5 terminals; note the polarity and tag the leads.
- d. Loosen the two screws holding the buzzer to the chassis.
- e. To install the 1RE1A1DS5 replacement module place buzzer over the two mounting holes and tighten the mounting screws.
- f. Resolder the two leads to their proper terminals.
- g. Reinstall power supply 1RE1PS1 as described in chapter 6 of TM 11-5820-540-12.

3-61. Replacement of Control Alarm 1RE1A1A2

- a. Place radio receiver 1RE1 top side up and locate 1RE1A1A2 (fig. 3-37) behind the front panel.
- b. Remove power supply 1RE1PS1 as described in chapter 6 of TM 11-5820-540-12.
- c. Remove circuit card assembly 1RE1A1A3 mounting screws and pull 1RE1A1A3 away from 1RE1A1A2.

- d. Remove the two mounting screws and pull 1RE1A1A2 free of the monitor panel 1R-E1A1.
- e. Unsolder and tag the leads from 1RE1A1A2 terminals. Remove 1RE1A1A2.
- f. Position the new 1RE1A1A2 above its mounting posts. Reconnect and solder the wires removed in e above.
- g. Reposition 1RE1A1A2 and secure with the two mounting screws.
- h. Reinstall power supply 1RE1PS1 as described in chapter 6 of TM 11-5820-540-12.

3-62. Replacement of Control-Indicator 2A2, Signal Level Control Monitor 2A4, Electronic Switch 2A4, Power Supply 2PS1 and Intermediate Frequency Amplifier 2A1-A2 AR 1

Replacement of these modules is described in chapter 6 of TM 11-5820-540-12.

3-63. Replacement of the Radio Frequency Amplifier 2A1AR1

- a. Place the receiver rf head bottom side up and locate radio frequency amplifier 2A1AR1.
- b. Locate the module extractor tool stored on the chassis (fig. 3-22).
- c. Disconnect the two rf leads from connectors J1 and J2 on 2A1AR1.
- d. Loosen the four green-circled mounting screws of 2A1AR1 and use the extractor tool to remove the module.
- e. To install the 2A1AR1 replacement module, position the module over the four mounting holes and press down to engage the connector. Tighten the mounting screws. Connect the P1 (2A1AR1J2) lead to connector J2 and the P2 (2A1AR1J1) lead to the connector J1 on radio frequency amplifier 2A1AR1.

3-64. Replacement of Power Monitor 2A1A5 (AM-4316/GRC-103(V))

- a. Removal of 2A1A5 is a second-order removal. Control-indicator 2A2 must be removed first, as described in chapter 6 of TM 11-5820-540-12.
- b. Place the receiver rf head bottom side up and locate 2A1A5 (fig. 3-18).
- c. Disconnect connector J1 (ANT.) from the front panel. Disconnect the power monitor rf lead from connector J1 of impedance matching network 2A1A1Z1.
- d. Loosen the two screws that secure plug P1 (XA1W4J2) to its mating connector and disconnect the plug.
- e. Loosen the three green-circled mounting screws that secure the power monitor 2A1A5 mounting bracket to the chassis and lift up 2A1A5 with the bracket attached. Remove the four screws that secure 2A1A5 to the bracket.

- f. To install the 2A1A5 replacement module, first attach the replacement to the mounting bracket.
- g. Connect plug P1 (XA1W4J2) to chassis connector 2A1W4J2 and tighten the two plug screws.
- h. Slide connector J1 (ANT.) at the end of the rf lead through the ANT. opening in the front panel and secure with the hexagonal nut.
- i. Connect plug P2 (XA1A1Z1J1) at the end of the rf lead to connector J1 of impedance matching network 2A1A1Z1.
- j. Position the replacement module, with the mounting bracket attached, over the three mounting holes and tighten the mounting screws.
- k. Reinstall control-indicator 2A2, as described in chapter 6 of TM 11-5820-540-12.

3-65. Replacement of Power Monitor 2A1A5 (AM-4316A/GRC-103(V))

- a. Removal of 2A1A5 is a second-order removal. Control-indicator 2A2 must be removed first, as described in TM 11-5820-540-12.
- b. Place the receiver rf head bottom side up and locate 2A1A5 (fig. 3-22).
- c. Disconnect connector J1 (ANT.) from the front panel. Disconnect the power monitor rf lead from connector J1 of impedance matching network 2A1A1Z7.
- d. Loosen the two screws that secure plug P1 (2A1W4J2) to its mating connector and disconnect the plug.
- e. Remove the three green-circled mounting screws that secure the power monitor 2A1A5 mounting bracket to the chassis and lift up 2A1A5 with the bracket attached. Remove the four screws that secure 2A1A5 to the bracket.
- f. To install the 2A1A5 replacement module, first attach the replacement to the mounting bracket. With the four screws removed in e above, secure the mounting bracket to the 2A1A5.
- g. Connect plug P1 (2A1W4J2) to chassis connector 2A1W4J2 and tighten the two plug screws.
- h. Slide connector J1 (ANT.) at the end of the rf lead through the ANT. opening in the front panel and secure with the hexagonal nut.
- i. Connect plug P2 (2A1A1Z7J1) at the end of the rf lead to connector J1 of impedance matching network 2A1A1Z7.
- j. Position the replacement module, with the mounting bracket attached, over the three mounting holes and tighten the mounting screws.
- k. Reinstall control-indicator 2A2, as described in TM 11-5820-540-12.



- 3-66. Replacement of Frequency Mixer Stage 2A1A2A2
- a. Place the receiver rf head upright and locate 2A1A2A2 (fig. 3-20).
  - b. Disconnect the rf lead from connector J2 on 2A1A2A2.
  - c. Loosen the four green-circled screws and lift up frequency mixer stage 2A1A2A2 from the chassis using the module extractor tool.
  - d. To install the 2A1A2A2 replacement module, position the module over the four mounting holes and press straight down to engage the connectors. Tighten the mounting screws. Reconnect plug P1 (XA1A2A2J2) at the end of the rf lead to connector J2 on 2A1A2A2.
- 3-67. Replacement of Low Pass Filter 2A1A1FL1 (AM-4316/GRC-103(V))
- a. Place the receiver rf head upright and locate low pass filter 2A1A1FL1 at rear (fig. 3-20). Disconnect the two rf cables connected to connectors J2 and J1 of low pass filter 2A1A1FL1.
  - b. Disconnect P3 (2A1A1A1J2) from 2A1A1A1J2.
  - c. Remove the four green-circled mounting screws on power supply 2PS1 and remove 2PS1 by pulling it away from chassis to allow access to one mounting screw of 2A1A1FL1.
  - d. Remove the two countersunk mounting screws of 2A1A1FL1 and remove 2A1A1FL1 through the access hole located at the bottom of the left side of the chassis.
  - e. Insert the replacement 2A1A1FL1 through the access hole at the bottom of the left side of the chassis and secure it to the chassis using the two countersunk screws.
  - f. Replace power supply 2PS1 by plugging P1 of 2PS1 into J5 (XPS1P1) and replace the four green-circled mounting screws removed in c above.
  - g. Connect the P2 (2A1A1FL1J1) cable to connector J1 of low pass filter 2A1A1FL1.
  - h. Connect the P2 (2A1A1A1J2) cable to the 2A1A1A1J2 bulkhead connector (fig. 3-20).
  - i. Connect the P1 (2A1A1FL1J2) cable to connector J2 of low pass filter 2A1A1FL1.
- 3-68. Replacement of Low Pass Filter 2A1A1FL1 (AM-4316A/GRC-103(V))
- a. Place the receiver rf head upright and locate low pass filter 2A1A1FL1 at rear (fig. 3-24). Disconnect the rf cable connected to connector J2.
  - b. Disconnect rf cable connected to J1 of low pass filter 2A1A1FL1.

- c. Disconnect P3 (2W2) from 2A1A1J2.
- d. Place receiver rf head with bottom side facing out and left side up.
- e. Remove the two countersunk mounting screws of 2A1A1FL1 and remove 2A1A1FL1 through the access hole located at the top of the left side of the chassis.
- f. With receiver rf head placed with bottom side facing outward and left side up, insert the replacement 2A1A1FL1 through the access hole at the top of the left side of the chassis and secure it to the chassis using the two countersunk screws.
- g. Place receiver rf head upright and connect plug P4 of cable 2W1 to connector J1 of low pass filter 2A1A1FL1.
- h. Connect the cable P1 (2A1A1FL1J2) to J2 of low pass filter 2A1A1FL1.
- i. Connect the plug P3 of cable 2W2 to bulkhead connector 2A1A1J2 (fig. 3-24).

### 3-69. Replacement of Buzzer 9A1DS1

- a. Loosen the four green-circled captive screws that secure the rear panel of the order wire unit case.
- b. Pull the rear panel away from case (fig. 3-48). Locate buzzer 9A1DS1 on rear panel.
- c. Unsolder the two leads connected to 9A1DS1; tag the leads.
- d. Loosen the two screws that hold 9A1DS1 to the rear panel.
- e. To install the 9A1DS1 replacement module, place the buzzer over the two mounting holes and tighten the mounting screws.
- f. Resolder the two leads to 9A1DS1; observe correct polarity of leads.
- g. Reinstall the rear panel and tighten the four green-circled mounting screws.

## Section IV. TROUBLESHOOTING (BAND II)

### 3-70. General

This section contains the systematic troubleshooting procedures required to sectionalize a fault in the radio set and to trace the fault to the defective module or part. Meter readings may help in locating faults without the help of test equipment or measuring circuits. Operational tests frequently indicate the general location of trouble and in many instances help in determining the nature of the fault. The operational check, loop testing procedure and the troubleshooting charts contained in TM 11-5820-540-12 are suitable starting points. The modified loop test proce-

ture, troubleshooting charts and signal substitution procedures enable direct support personnel to quickly localize the faulty module. Replacement of one or more suspected defective modules may be a quick and effective method of repairing a radio set in emergency conditions.

### 3-71. Loop Test Procedure

### 3-72. Transmitter Troubleshooting

#### CAUTION

The transmitter rf head when extended must be air cooled during tests; a cooling fan must be pointed toward the power amplifier tubes at all times. If a cooling fan is not available the transmitter rf head must not be operated for longer than 5 minute periods. Another alternative is to place the transmitter rf head back into the transmitter case while troubleshooting radio transmitter 5TR1.

a. General. The troubleshooting chart contains troubleshooting procedures for radio transmitter 5TR1 and the transmitter rf head. Paragraphs 3-74 through 3-79 contain test procedures for the transmitter rf head only. Refer to paragraphs 3-8 through 3-12 for test procedures for radio transmitter 5TR1. For more effective troubleshooting of the transmitter remove the transmitter rf head and radio transmitter 5TR1 from the transmitter case. Remove the transmitter rf head dust cover. Connect the transmitter rf head to the transmitter case using CX-12094/U extender cable and connect radio transmitter 5TR1 to the transmitter case using CX-12092/U and CX-12093/U extender cables. Connect the transmitter to a 115 volts, 47 to 420 Hz source and proceed to troubleshoot the transmitter.

CAUTION

The transmitter rf head PWR OUT connector must be connected to the dummy load during troubleshooting. Damage to the equipment will result if this is not done.

NOTE

There are two models of Amplifier-Frequency Multiplier distinguished by nomenclatures AM-4321/GRC-103(V) and AM-4321A/GRC-103(V). Unless otherwise indicated this paragraph refers to both units.

b. Transmitter Troubleshooting Chart.

| Symptom   | Probable cause   | Checks and corrective measures  |
|---|--|---|
| <p>1. When AC POWER switch is set to ON/RESET centrifugal fan does not start, AC POWER and LOW POWER lamps do not light, buzzer does not sound.</p> | <p>a. Defective power supply 5TR1PS1 (fig. 3-1).<br/><br/>b. Defective switch 5TR1-A1CB1 (fig. 3-3).</p> | <p>a. Check for 115 vac at connector J3 (5TR1PS1P1) pins 6 and 7 (para 3-8). If voltage is present, replace 5TR1PS1 (para 3-50).<br/><br/>b. If voltage not present in a above, check for 115 vac at switch LINE and LOAD terminals. If indications are normal make wiring continuity checks (FO-4-43).</p> |
| <p>2. 28 VDC and 12 VDC metering reads negative, all other metering zero, LOW POWER and SYNC lamps light.</p>                                       | <p>Short circuit.</p>  | <p>Check for short on 28 v supply line (FO-4-43, 4-68) .</p>  |
| <p>3. 12 VDC reads negative, 28 VDC full scale, 600 VDC high, DRIVER normal, all other metering zero. LOW POWER and SYNC lamps light.</p>           | <p>Short circuit.</p>  | <p>Check for short on 12 v supply line (FO-4-43, 4-68) .</p>  |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom   | Probable cause  | Checks and corrective measures   |
|---|---|--|
| 4. All metering reads zero, all lamps are inoperative, centrifugal fan operates.  | Short circuit.  | <p>a. Check for short on 26 v supply line (F0-4-43, 4-68) .</p> <p>b. Check for short on 600 v supply line (F0-4-43, 4-68) .</p>   |
| 5. 28 VDC normal or zero, 12 VDC normal, DOUBLER, MULT, DRIVER and PWR OUT low, OSC high. LOW POWER and SYNC lamps light.                 | Open circuit.   | Check for open 28 v supply (F0-4-43, 4-68).  |
| 6. When AC POWER switch is set to ON/RESET, centrifugal fan does not start; AC POWER, LOW POWER, and OVERHEAT lamps light; buzzer sounds. | <p>a. Defective centrifugal fan 5A2B1 (section X).</p> <p>b. Defective power supply 5TR1PS1 (fig. 3-1).</p> | <p>a. Check for 140 vac at connector J5 (5A2B1P1) pins 1 and 2 (transmitter case). If voltage is present replace 5A2B1 (section X).</p> <p>b. (1) Check for 140 vac at power supply filter terminals FL5 and FL6 of 5TR1PS1 (figs. 3-1, 3-2). If no voltage is present replace 5TR1PS1 (para 3-50).</p> <p>(2) If voltage is present at FL5 and FL6 of 5TR1PS1 but not at pins 1 and 2 of connector J5 (5A2B1P1) in the transmitter case, remove 115 vac power source and check for continuity between these two points (F0-4-43).</p> |

b. Transmitter Troubleshooting Chart-Continued.

| Symptom   | Probable cause   | Checks and corrective measures   |
|---|--|--|
| 7. When AC POWER switch is set to ON/RESET, centrifugal fan does not start. OVERHEAT lamp is not on. Buzzer may or may not sound. All other indications normal. | <ul style="list-style-type: none"> <li>a. Defective OVERHEAT lamp 5TR1A2A2DS4.</li> <li>b. Defective pressure differential monitor 5A2A2 .</li> </ul>  | <ul style="list-style-type: none"> <li>a. Change indicator lamp 5TR1A2A2DS4.</li> <li>b. Replace 5A2A2 (section X).</li> </ul>   |
| 8. Buzzer does not sound when an alarm lamp lights or goes out  | <ul style="list-style-type: none"> <li>a. Defective buzzer 5TR-1A1DS5 (fig. 3-3).</li> <li>b. Defective switch 5TR-1A1S2 (fig. 3-3).</li> <li>c. Defective alarm control 5TR1A1A2 (fig. 3-3).</li> </ul> | <ul style="list-style-type: none"> <li>a. Check for +26 vdc at buzzer terminals. If voltage is present replace the buzzer (para 3-52).</li> <li>b. Higher category of maintenance is required.</li> <li>c. If continuity is broken because of 5TR1A1A2, replace 5TR1A1A2 (para 3-51).</li> </ul>   |
| 9. SYNC lamp does not go out within 10 seconds after AC POWER switch is set to ON/RESET.  | <ul style="list-style-type: none"> <li>a. Defective synthesizer 5TR1A2 (fig. 3-3).</li> <li>b. Defective power supply 5TR1PS1 (fig. 3-1).</li> </ul>   | <ul style="list-style-type: none"> <li>a. Extend the synthesizer (para 3-10) and check for +12 v, 26 v (N) and +28 v at J1 (X5TR1A2P2) (fig. 3-3). If normal indications are obtained, replace synthesizer 5TR1A2 (para 3-48).</li> <li>b. If indications in a above are abnormal, check 5TR-1PS1 (para 3-8). If abnormal indications are obtained replace 5TR1PS1 (para 3-50).</li> </ul> |
| 10. When AC POWER switch is set to ON/RESET at room temperature, centrifugal fan operates full speed. (Case CY-4637A only.)                                     | <ul style="list-style-type: none"> <li>a. Defective control monitor temperature sensor 5A2A2.</li> </ul>   | <ul style="list-style-type: none"> <li>a. Check sensor connections. If connections are not defective, replace 5A2A2 (Section X).</li> </ul>  |
| OVERHEAT lamp does not go off within 10 seconds.  | <ul style="list-style-type: none"> <li>b. Defective pressure differential monitor 5A2A2 .</li> </ul>   | <ul style="list-style-type: none"> <li>b. Replace 5A2A2 (Section X).</li> </ul>  |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom   | Probable Cause  | Checks and Corrective Measures   |
|---|---|--|
| 11. DRIVER metering greater than 100%.  | Short circuit in voltage regulator assembly 37AR1A1A1 or rf amplifier 37AR1A1AR (fig. 3-51).  | Replace voltage regulator assembly and two electron tubes. If indication becomes normal, replace one original tube. If the indication still remains normal, replace the other original tube. If indications still remain normal, then only the voltage regulator assembly 37AR1A1 was shorted. If the indication after replacement of the tubes and voltage regulator assembly does not become normal, higher category of maintenance is required. |
| 12. LOW POWER lamp does not go out within 60 second: after AC POWER switch is set to ON/RESET. PWR OUT position reads low.                              | <p>a. Defective rf power monitor 37AR1A2 (fig. 3-51).</p> <p>b. Defective low pass filter 37AR1A1FL1 (fig. 3-51).</p> <p>c. Defective radio frequency amplifier 37AR1AR1 (fig. 3-51).</p> | <p>a. Measure power (26 watts) at P2 (37AR1A-2J1) (fig. 3-51). if normal, check 37AR1A2 (para 3-79).</p> <p>b. If power indication at 37AR1A1FL1J2 is abnormal, measure the power at P2 (37AR1A1-FL1J1) (para 3-76). If normal, check 37AR1A1FL1 (para 3-78) .</p> <p>c. if abnormal indication is obtained in b above, measure the power at 37A1J2 (para 3-75). if normal, higher category maintenance is required.</p>                           |
| 13. LOW POWER light does not go out within 60 second! after AC POWER switch is set to ON/RESET. PWR OUT position reads low, DRIVER position reads high. | No output cathode regulation.   | Remove transmitter 5TR1 and measure the resistance from pin 30 of connector J8 X5TR1A1A1P3 (transmitter case) (section X) to ground approximately 12 ohms). If normal, replace 5TR1-PS1 (para 3-50). If ab-  |

b. Transmitter Troubleshooting Chart- Continued.

| Symptom  | Probable Cause   | Checks and Corrective Measures  |
|--|--|---|
| 13. Continued.   |  | normal, check voltage regulator assembly 37AR1A1A1 (para 3-77).   |
| 14. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR OUT position reads low, DRIVER position reads low. | <p>a. Defective voltage regulator 37AR1A1A1 fig. 3-51).</p> <p>b. Defective amplifier subassembly 37AR1AR1 (fig. 3-51).</p> <p>c. No driver cathode voltage.</p> | <p>a. (1) Measure the power (3.5 watts minimum) at 37AR1AR1J3 (fig. 3-51). If normal check the voltage at TP2 and TP4 of 37AR1A1A1 (para 3-77). If normal, disconnect the transmitter rf head and measure the resistance between TP2 and TP4 of voltage regulator assembly 37AR1A1A1 (fig. 3-51) (should be 1.5 ohms approximate y).</p> <p>(2) If voltage at TP2 and TP4 is abnormal check the output heater/output cathode circuit of 5TR1PS1 (para 3-8)</p> <p>(3) If 5TR1PS1 check is normal, check continuity of output heater/output cathode wiring between 5TR1PS1 and transmitter rf head (F0-4-43 and 4-68).</p> <p>b. If the power at 37AR1AR1J3 (para 3-76) is abnormal, higher category of maintenance is required.</p> <p>c. Remove the radio transmitter 5TR1 from the case and measure the resistance from pin 29 of connector J8 (X5TR1A1A1P3) (section X) to</p> |



b. Transmitter Troubleshooting-Continued

| Symptom   | Probable Cause   | Checks and Corrective Measures  |
|---|--|---|
| <p>14. Continued.</p>   | <p>d. Defective driver cathode/driver heater.</p> <p>e. Defective rf amplifier 37AR1AR1 (fig. 3-51).</p> | <p>ground (34 ohms approximately). If normal, replace 5TR1PS1 (para 3-50). If abnormal, check voltage regulator assembly 37AR1A1A1 (para 3-77).</p> <p>d. Measure the power at 37A1J2 (fig. 3-49) (para 3-75). If normal, check the voltage across TP1 and TP3 of voltage regulator assembly 37AR1A1A1 (para 3-77). If normal, disconnect the transmitter rf head and measure resistance between TP1 and TP3 of voltage regulator assembly 37AR1A1A1 (fig. 3-51) (should be 1.5 ohms approximately) If voltage at TP1 and TP3 is abnormal, check the driver heater/driver cathode circuit of 5TR1PS1 (para 3-8). If 5TR1PS1 check is normal, check the continuity of the driver heater/driver cathode wiring between 5TR1PS1 and transmitter rf head (FO-4-43, 4-68).</p> <p>e. If driver cathode/driver heater circuit is normal, higher category maintenance is required.</p> |
| <p>15. At channel 760 and above or channel 759 and below, LOW POWER light does not go out within 60 seconds after AC POWER switch is set to</p> | <p>Defective frequency multiplier 37A1 (fig. 3-51).</p>  | <p>Check the output of 37A1 (para 3-75). Check the continuity of 26 V UNREG and 28 V REG wiring between 5TR1PS1 and transmitter rf head (FO-4-43, 4-68).</p>  |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom  | Probable cause  | Checks and corrective measures   |
|--|---|--|
| <p>15. Continued.</p> <p>ON/RESET. PWR OUT position reads low, DRIVER position reads low and MULT position reads low.</p>  |   |  |
| <p>16. Same as 13 above but at all channels.</p>   | <p>a. Defective wiring.</p> <p>b. Defective amplifier-frequency multiplier 5TR1A4 (fig. 3-3).</p>   | <p>a. Measure power into frequency multiplier at 37A1J1 (2.5 watts minimum) (para 3-11). If abnormal, check for continuity from 37A1J1 to pin A2 of J11 (X5TR1-A4P1) (FO-4-43, 4-68).</p> <p>b. If the wiring continuity check in a above is normal, replace 5TR1A4 (para 3-49).</p> |
| <p>17. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. DRIVER position reads low, MULT position reads low, DOUBLER position reads low.</p>     | <p>a. Defective amplifier-frequency multiplier 5TR1A4 (fig. 3-3).</p> <p>b. Defective wiring.</p>   | <p>a. Measure the power at pin A1 of J11 (X5TR1A4P1) (para 3-10). If it is normal, check 5TR1A4 (para 3-11).</p> <p>b. Check for +28 v at pin 1 and check for ground at pin 17 of J11 (X5TR1-A4P1) (para 3-11) with the transmitter rf head connected.</p>                           |
| <p>18. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. DRIVER position reads low, MULT position reads low, DOUBLER position reads low, OSC</p> | <p>a. Defective electrical-frequency synthesizer 5TR1A2 (fig. 3-3).</p> <p>b. Defective wiring.</p> | <p>. Check synthesizer 5TR1A2 (para 3-10).</p> <p>b. Check inputs to 5TR1A2 at J1 (X5TR1A2P1) (FO-4-43) pin 1 +28 vdc pin 3 0 v pin 2 +12 vdc pin 37 +28 vdc.</p>  |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom  | Probable cause  | Checks and corrective measures   |
|--|---|--|
| 18. Continued.<br><br>position reads low.  |   |  |
| 19. SYNC alarm does not go out within 10 seconds after AC POWER switch is set to ON/RESET.   | a. Defective synthesizer 5TR1A2 (fig. 3-3).<br>b. Defective power supply 5TR1PS1 (fig. 3-1).              | a. Check synthesizer 5TR1A2 (para 3-10).<br>b. Check power supply 5TR1PS1 (para 3-8).                                |
| 20. When AC POWER switch is set to ON/RESET, buzzer and centrifugal fan operate, LOW POWER and SYNC alarm lights come on, DRIVER metering is low, all other metering reads zero. | Defective power supply 5TR1PS1 (fig. 3-1).  | Check voltage regulator amplifier 5TR1PS1AR1 of power supply 5TR1PS1 (para 3-8).                                     |
| 21. No communication. Metering and LOW POWER and SYNC alarms may or may not indicate normal.   | Synthesizer off frequency due to -<br>a. Defective synthesizer 5TR1A2 (fig. 3-3).<br>b. Defective wiring. | a. Check synthesizer (para 3-10).<br>b. Check wiring from control-indicator 37A2 to the synthesizer (FO-4-43, 4-68). |

3-73. Receiver Troubleshooting

a. General. The troubleshooting chart contains troubleshooting procedures for radio receiver 1RE1 and the receiver RF head. Paragraphs 3-80 through 3-90 contain test procedures for the receiver rf head only. Refer to paragraphs 3-35 through 3-42 for test procedures for radio receiver 1RE1. For more effective troubleshooting of the receiver, remove the receiver rf head (fig. 3-50) and radio receiver 1RE1 from the receiver case. Remove the receiver rf head dust cover. Connect the receiver rf head to the receiver case using CX-12097/U extender cable. Connect the radio receiver 1RE1 to the receiver case using CX-12095/U and CX-12096/U extender cables. Connect the receiver to a 115 volt, 47 to 420 Hz source and proceed to troubleshoot the receiver.

b. Receiver Troubleshooting Chart.

| Symptom  | Probable Cause   | Checks and Corrective Measures   |
|--|--|--|
| 1. With AC POWER switch set to ON, there are no meter indications and no alarms. | Defective switch 1RE1A-1CB1 (fig. 3-40).   | Check for 115 vac at switch LINE and LOAD terminals (fig. 3-40). If switch is normal, make wiring continuity checks (FO-4-28).   |
| 2. Buzzer does not sound when any alarm lamp lights or goes out.                 | Defective buzzer 1RE1A-1DS5 (fig. 3-37).   | Check for 26 vdc at buzzer terminals (fig. 3-37). if voltage is present, replace buzzer (para 3-60). if voltage is not present, make wiring continuity checks (FO-4-28).   |
| 3. LOW SIGNAL alarm is on; RCVR SIG metering reads low.                          | <p>a. Defective rf power monitor 33A3 (fig. 4-80 TM 11-5820-540-40) or duplexer sub-assembly 33A1A1 (fig. 3-56) .</p> <p>b. Defective signal level control-monitor 33A5 (3-56) .</p> <p>c. Defective low-pass filter 33FL1 (fig. 3-56).</p> <p>d. Defective frequency mixer stage 33A7, (fig. 3-63).</p> | <p>a. Inject a signal at -65 dBm at receive frequency into P1 (33A1A-1J2) (fig. 3-56). If the alarm clears, higher category of maintenance is required.</p> <p>b. if the alarm condition remains, inject signal into P1 (33A5J2) (fig. 3-60) . If the alarm clears, replace signal level control-monitor 33A5 (para 3-98).</p> <p>c. If the alarm condition remains, inject the signal into P1 (33FL1-J2) (fig. 3-56). If the alarm clears, replace low pass filter 33FL1 (para 3-102).</p> <p>d. If the alarm condition remains, remove frequency mixer stage 33A7 (para 3-102) and feed a signal of 30 MHz at -35 dBm into pin A1 of 33A1W1J8 (fig. 3-63). if alarm clears, frequency mixer stage 33A7 is defective.</p> |

b. Transmitter Troubleshooting Chart-Continued.

| Symptom   | Probable Cause   | Checks and Corrective Measures  |
|---|--|---|
| 3. Continued.   | <p>e. Defective Intermediate frequency amplifier 33AR1 (fig. 3-63).</p> <p>f. Local oscillator off frequency due to-</p> <p>(1) Defective synthesizer 1RE1A2 (fig. 3-46).</p> <p>(2) Defective wiring.</p> | <p>check frequency mixer stage 33A7 (para 3-88).</p> <p>e. If alarm remains inject a 30 MHz signal at a level of -35 dBm into 33A1W1A1P2 (fig. 3-63) If alarm clears, replace intermediate frequency amplifier 33AR1 (para 3-101).</p> <p>(1) Check synthesizer (para 3-35).</p> <p>(2) Check wiring from control Indicator 33A4 to J3 (X1RE-1A2P2) (FO-4-28, 4-68) .</p> |
| 4. LOW SIGNAL alarm, RCVR SIG reading low; MULT reading low.                                    | Defective frequency multiplier 33A2A1 or 33A2A2 (fig. 3-56).   | Check the output power level at P1 (33A7J21, (para 3-89). If abnormal replace receiver rf head.   |
| 5. SYNC alarm and/or LOW SIGNAL alarm, RCVR SIG reading low, MULT reading low, OSC reading low. | Defective synthesizer 1RE-1A2 (fig. 3-40).   | Check supply voltages at J3 (X1RE1A2P2). If normal, change synthesizer 1RE1A2 (para 3-59). If abnormal check wiring (FO-4-28).  |

3-74. Control-Indicator 37A2

a. Test Equipment Required.

| Equipment                       | Common Name        |
|---------------------------------|--------------------|
| Multimeter, Digital, AN/USM-486 | Digital Multimeter |

a. Test Equipment Required-Continued

| Equipment                                   | Common Name |
|---|-------------|
| Cable Assembly, Special Purpose, Electrical | CX-12098/U  |
| Cable Assembly, Special Purpose, Electrical | CX-12094/U  |

b. Operational Checks.

(1) Loosen the two screws securing plug P1 (37AR1A1W1J3) to chassis connector 37AR1A1WIJ3 (fig. 3-50). Disconnect P1 from 37AR1A1WIJ3.

(2) Set the XMTR CHANNEL control to channel 624.

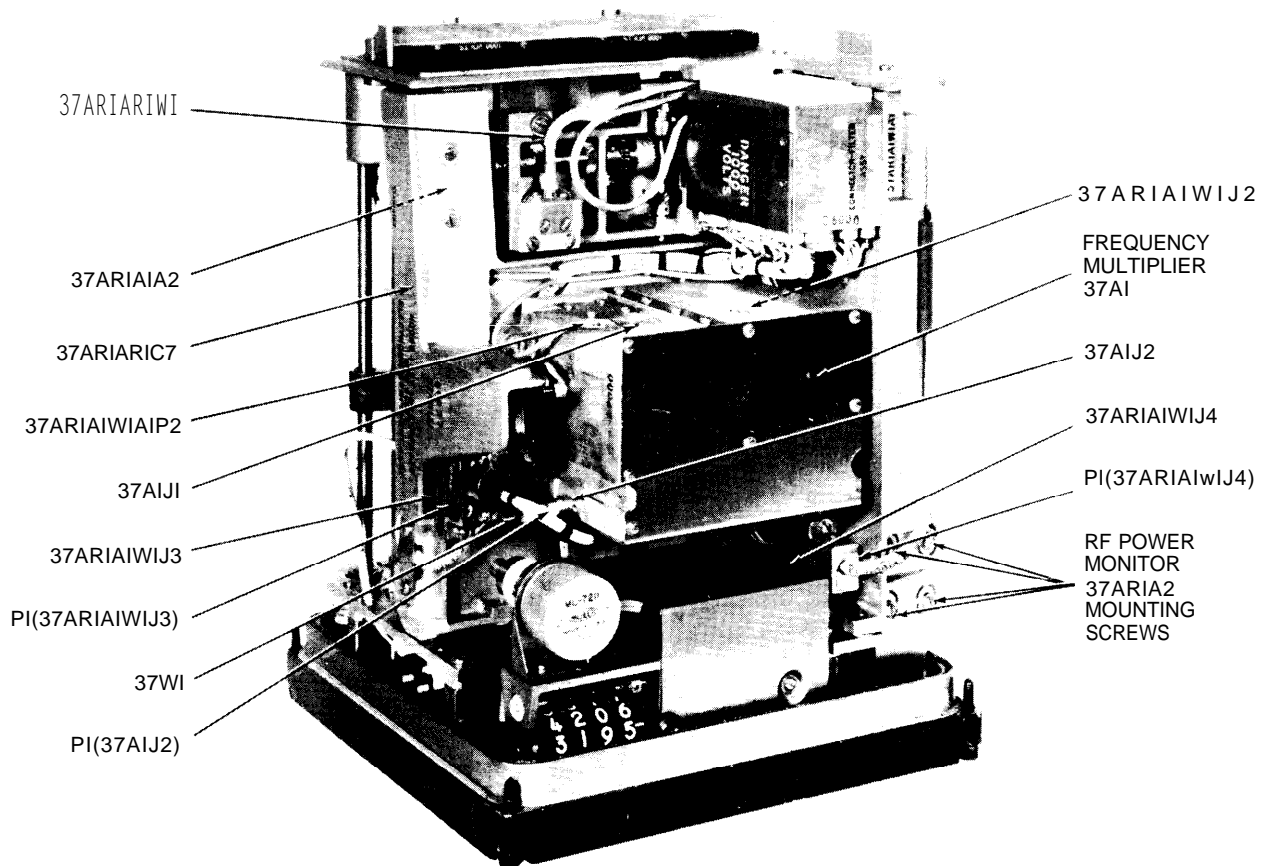


Figure 3-50. Band II Transmitter RF Head, Top View.

(3) Using the multimeter, check for correct resistance between the following pins of P1 (37AR1A1W1J3) as shown in the chart below.

| Pins      | Resistance |
|-----------|------------|
| 1 and 14  | Infinity   |
| 2 and 14  | Infinity   |
| 3 and 14  | Infinity   |
| 4 and 14  | Infinity   |
| 5 and 14  | Infinity   |
| 6 and 14  | Infinity   |
| 7 and 14  | Infinity   |
| 8 and 14  | Infinity   |
| 9 and 14  | Infinity   |
| 10 and 14 | Infinity   |
| 11 and 14 | Infinity   |
| 12 and 14 | Zero       |

(4) Set the XMTR CHANNEL control to channel 623.

(5) Using the multi meter, check for correct resistance between the following pins of P1 (37AR1A1W1J3) as shown in the chart below.

| Pins      | Resistance |
|-----------|------------|
| 1 and 14  | Infinity   |
| 2 and 14  | Zero       |
| 3 and 14  | Zero       |
| 4 and 14  | Zero       |
| 5 and 14  | Zero       |
| 6 and 14  | Zero       |
| 7 and 14  | Zero       |
| 8 and 14  | Zero       |
| 9 and 14  | Zero       |
| 10 and 14 | Zero       |
| 11 and 14 | Zero       |
| 12 and 14 | Infinity   |

(6) Remove control-indicator 37A2 from the transmitter rf head as described in chapter 6, TM 11-5820-540-12.

(7) Connect plug PI (37AR1A1W1J3) to chassis connector 37AR1A1W1J3 using cable CX-12098/U.

(8) Remove the four screws securing the control-indicator cover and remove the cover.

(9) Connect the transmitter rf head to the transmitter case using cable CX-12094/U and set the AC POWER switch to ON/RESET.

- (10) Set the control-indicator to channel 759.
- (11) Using the multimeter check the voltage at terminal 24 (pin 13 of Pi). The multimeter should indicate zero volt.
- (12) Set the control-indicator to channel 760.
- (13) Using the multimeter, check the voltage at terminal 24. The indication should be +26 volts dc.
- (14) Set the AC POWER switch to OFF. Reinstall the control-indicator cover. If abnormal indications are obtained in either (3), (5), (11) or (13) above, replace control-indicator 37A2. Refer to chapter 6, TM 11-5820-540-12 for replacement procedures.

3-75. Frequency Multiplier 37A1

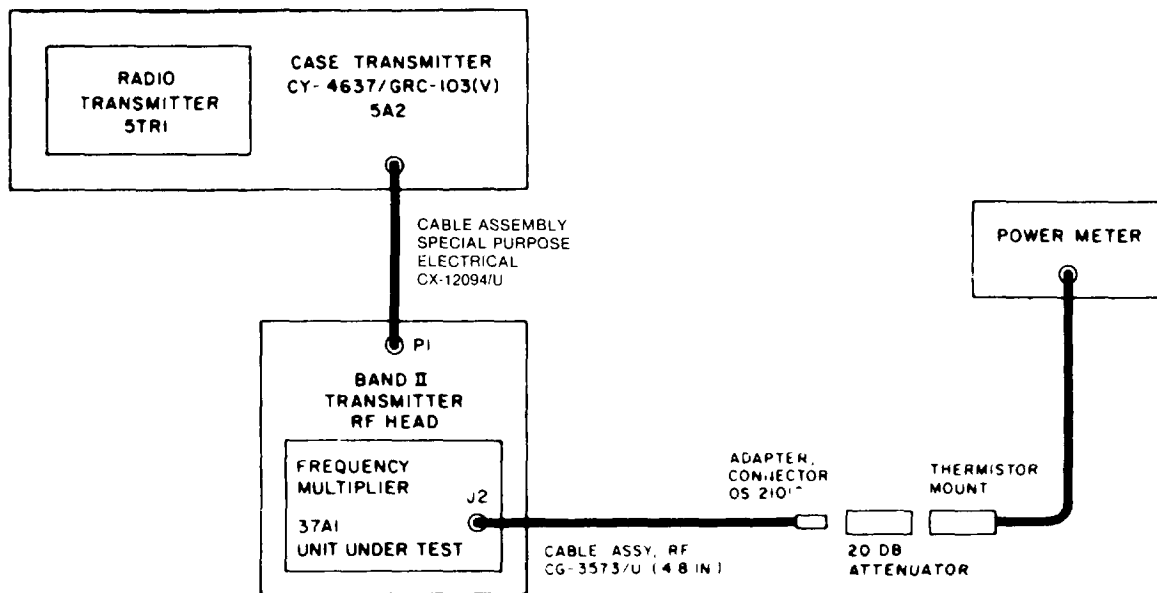
a. Equipment Required.

| Equipment   | Common Name                  |
|---|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Attenuator, Fixed 20 dB Empire Devices AT-75-20       | 20 dB attenuator             |
| Cable Assembly, Special Purpose, Electrical           | CX-12094/U                   |
| Cable Assembly, Radio Frequency CG-3573/U (4.8 in.)   |                              |
| Adapter-Connector Omni Spectra 21010                  | Adapter-connector 0S21010    |

b. Operational Check.

- (1) Disconnect plug P1 (37A1J2) from connector J2 on frequency multiplier 37A1 (fig. 3-49).
- (2) Connect test equipment as shown in figure 3-50.
- (3) Set the XMTR CHANNEL and XMTR TUNE control to channel 759.
- (4) Set the transmitter AC POWER switch to ON/RESET. The level at 37A1J2 should be +22 dbm minimum (+20 dbm for unit SM-D-865053).
- (5) Set the XMTR CHANNEL and XMTR TUNE control to channel 760. The level at 37A1J2 should be +22 dbm minimum (+20 dbm for unit SM-D-865053).
- (6) Set the AC POWER switch to OFF. If abnormal indications are obtained in either (4) or (5) above, replace the transmitter rf head.





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Figure 3-51. Frequency Multiplier 37A1 Operational Check, Test Setup.

3-76. Radio Frequency Amplifier 37AR1AR1

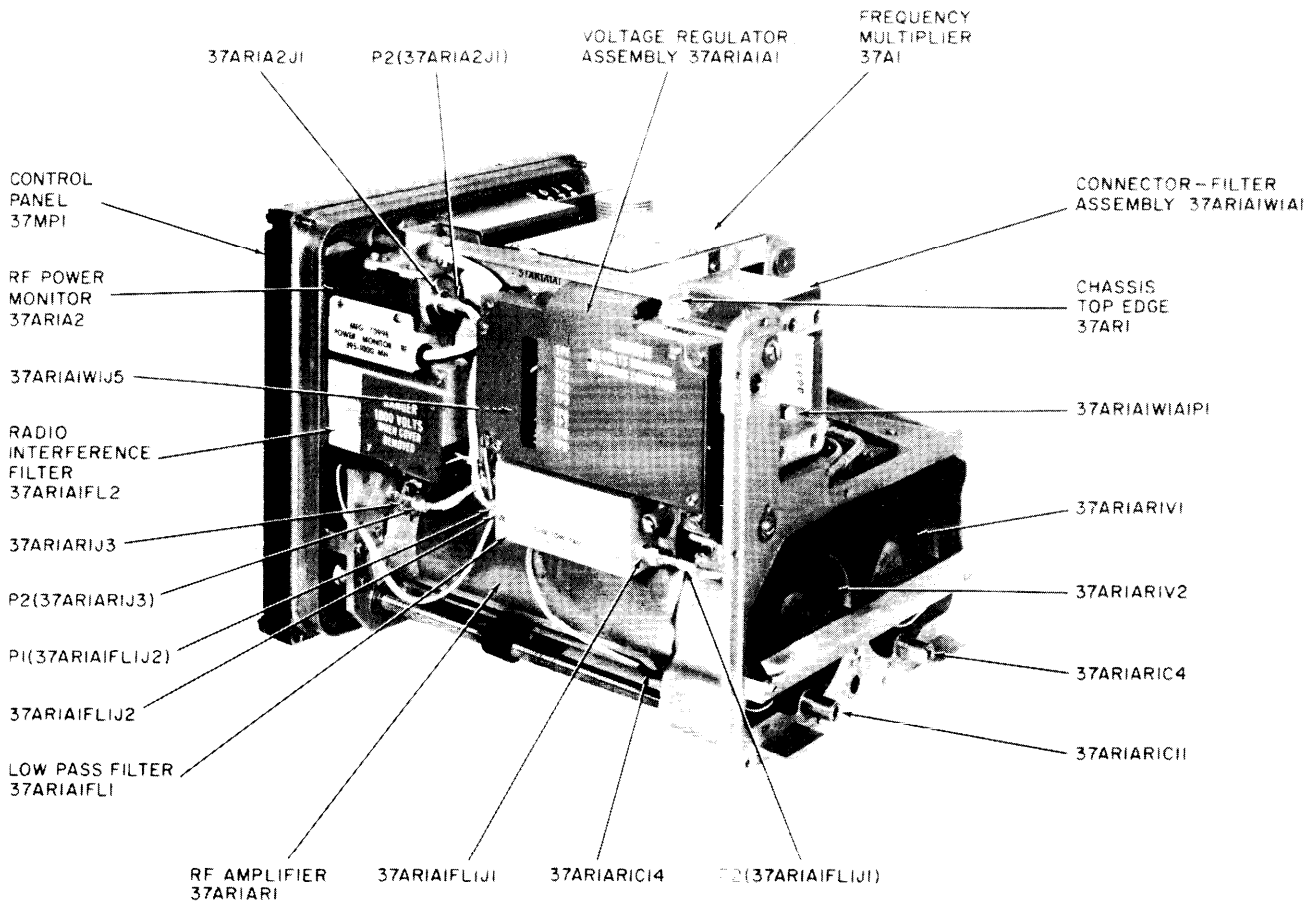
a. Test Equipment Required.

| Equipment  | Common Name               |
|--|---------------------------|
| Wattmeter AN/URM-120   | Wattmeter                 |
| Cable Assembly, Special Purpose, Electrical                      | CX-12094/U                |
| Cable Assembly, RF (2 required)                                  | CG-1883/U (4.5 ft.)       |
| Cable Assembly, Radio Frequency CG-3573/U (4.8 in.) (2 required) |                           |
| Adapter-Connector, Omni Spectra 21010 (2 required)               | Adapter-connector OS21010 |
| Adapter-Connector UG-29B/U                                       |                           |
| Cable Assembly, RF   | CG-3568/U                 |

b. Operational Check.

- (1) Disconnect P2 (37AR1AR1J3) from connector 37AR1AR1J3 (fig. 3-52).
- (2) Connect the test equipment as shown in A, figure 3-53.
- (3) Insert the coupler-detector CU-755/URN-120 into the wattmeter.
- (4) Set the XMTR CHANNEL and XMTR TUNE control to channel 760.

- (5) Set the transmitter AC POWER switch to ON/RESET. The wattmeter should indicate no less than 3.5 watts.
- (6) Set the AC POWER switch to OFF.
- (7) Reconnect plug P2 (37AR1AR1J3) to connector J3 on 37AR1AR1J3.
- (8) Disconnect plug P2 (37AR1A1FL1J1) from connector 37AR1A1FL1J1 (fig. 3-52) .
- (9) Connect the test equipment as shown in B, figure 3-53.
- (10) Set the AC POWER switch to ON/RESET.
- (11) Set the meter switch to PWR OUT and adjust the PWR OUT PEAK control for maximum indication on the meter. The wattmeter should indicate 32 watts minimum.
- (12) Set the AC POWER switch to OFF.
- (13) Reconnect plug P2 (37AR1A1FL1J1) to connector 37AR1A1FL1J1.



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Figure 3-52. Band II Transmitter RF Head, Side View.

(14) Replace the transmitter rf head if abnormal indications are obtained in (5) and (11) above.

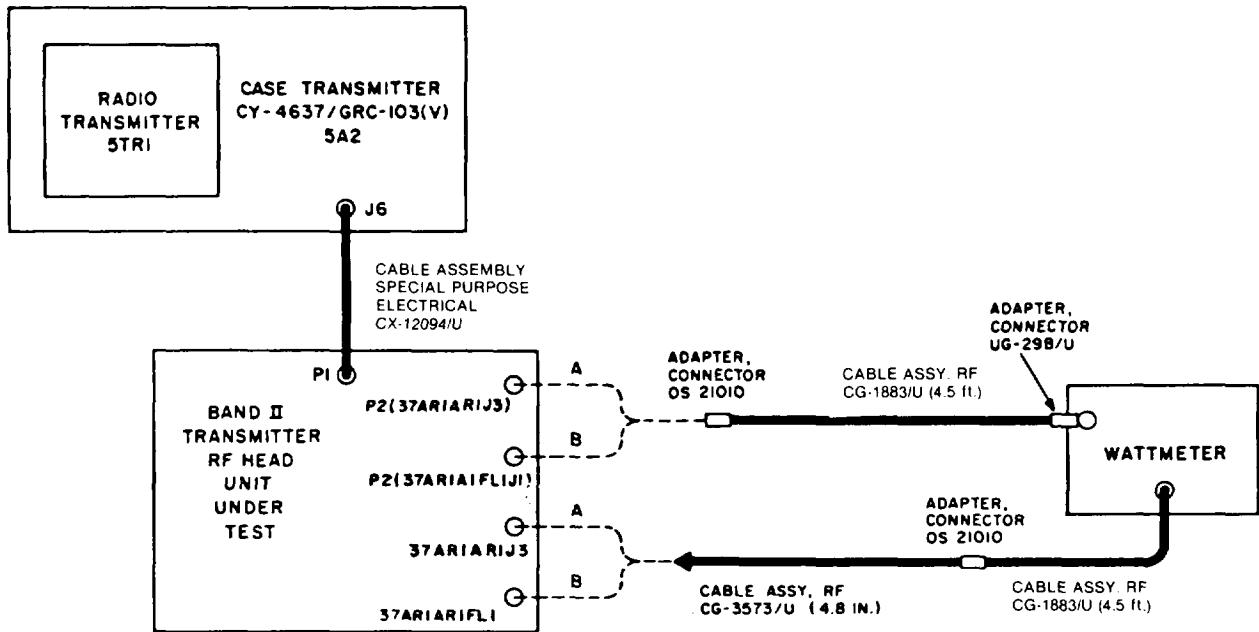


Figure 3-53. Radio Frequency Amplifier 37AR1AR1 Operational Check, Test Setup.

3-77, Voltage Regulator Assembly 37AR1A1A1

i. Test Equipment Required.

| Equipment                                   | Common Name        |
|---|--------------------|
| Multi meter, Digital, AN/USM-486            | Digital Multimeter |
| Cable Assembly, Special Purpose, Electrical | CX-12094/U         |
| Cable Assembly, RF                          | CG-3568/U          |
| Cable Assembly, RF                          | CG-1883/U          |

b. Operational Check.

- (1) Remove the transmitter rf head from the case. Remove the dust cover from the rf head and locate voltage regulator assembly 37AR1A1A1 (fig. 3-52).
- (2) Connect J6 on the transmitter case to 37AR1A1W1A1P1 (fig. 3-52) on the transmitter rf head using cable CX-12094/U.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 760.
- (4) Set the AC POWER switch to ON/RESET.
- (5) Set the meter switch to PWR OUT and adjust the PWR OUT PEAK control for maximum indication on the meter.

(6) Using multimeter, check for correct voltage between the following test points on the voltage regulator assembly as shown in the chart below.

| Multimeter |      |                |
|------------|------|----------------|
| (+)        | (-)  | Voltage        |
| TP4        | TP2  | 6.3 vdc±0.13 V |
| TP3        | TP1  | 6.3 vdc±0.13 V |
| TP4        | TP5  | 13.8 vdc±0.7 V |
| TP4        | TP11 | 3.2 vdc±1.5 V  |
| TP3        | TP10 | 3.2 vdc±1.5 V  |

(7) Remove voltage regulator assembly 37 AR1A1A1 (chapter 6, TM 11-5820-540-12) and check the resistance between the following pins of P1.

| Pins     | Resistance<br>(ohms ± 10%) |
|----------|----------------------------|
| 14 and 5 | 12                         |
| 8 and 5  | 34                         |
| 7 and 5  | 10 M                       |
| 2 and 6  | 270 k                      |

(8) Set the AC POWER switch to OFF. If abnormal indication is obtained in (6) or (7) above, replace voltage regulator assembly 37AR1A1A1. Refer to paragraph 3-97 for replacement procedures.

3-78. Low-Pass Filter 37AR1A1FL1

a. Test Equipment Required.

| Equipment   | Common Name               |
|---|---------------------------|
| Wattmeter, RF, An/URM-120                           | Wattmeter                 |
| Cable Assembly, Special Purpose, Electrical         | CX-12094/U                |
| Cable Assembly, Radio Frequency CG-3573/U (4.8 in.) |                           |
| Cable Assembly, Radio Frequency (2 required)        | CG-1883/U (4.5 ft.)       |
| Adapter-Connector Omni Spectra 21020                | Adapter-connector 0S21020 |
| Adapter-Connector UG-29B/U (3 required)             |                           |

b. Operational Check.

- (1) Disconnect plug P1 (37AR1A1FL1J2) from connector J2 on low-pass filter 37AR1A1FL1 (fig. 3-52).
- (2) Connect the test equipment as shown in figure 3-54.
- (3) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (4) Set the XMTR CHANNEL and XMTR TUNE controls to channel 760.
- (5) Set the transmitter AC POWER switch to ON/RESET.
- (6) Set the meter switch to PWR OUT and adjust the PWR OUT PEAK control for maximum indication on the meter. The wattmeter should indicate a minimum of 26 watts.
- (7) Set the AC POWER switch to OFF. Replace low pass filter 37AR1A1FL1 if an abnormal indication is obtained in (6) above. Refer to paragraph 3-93 for replacement procedures.

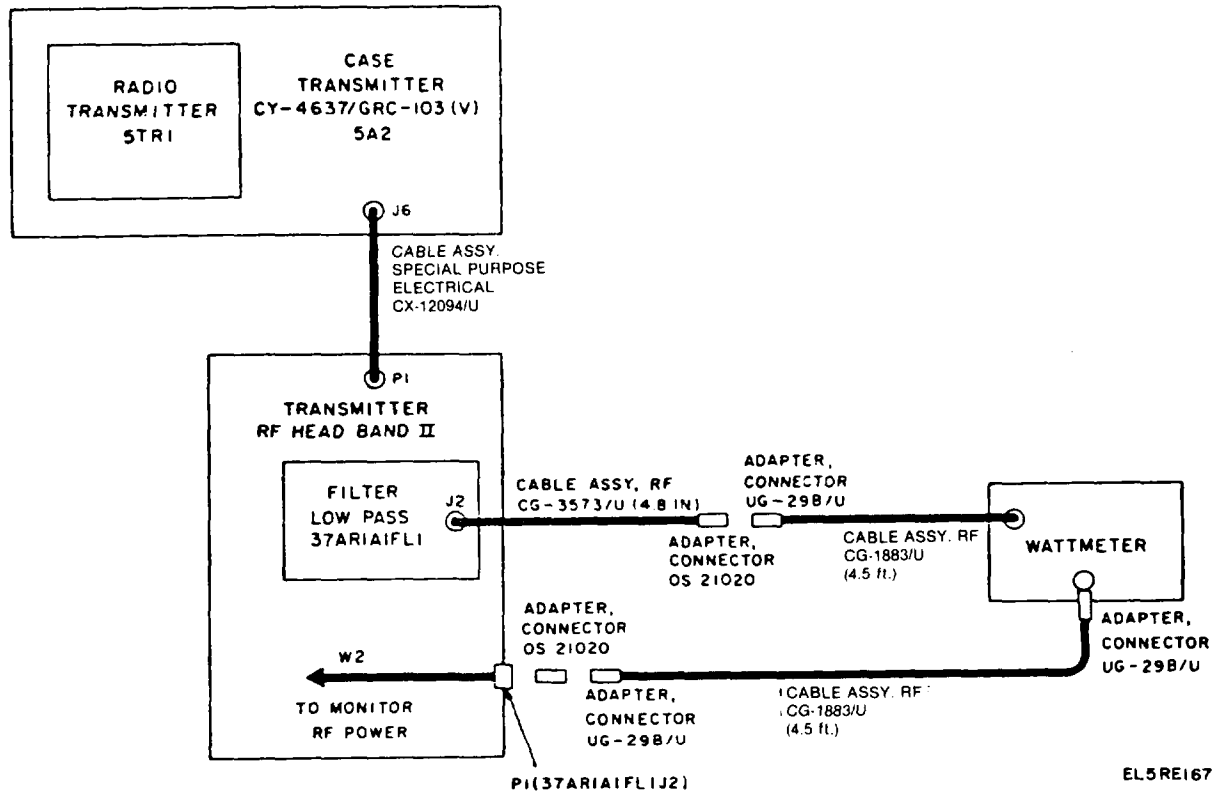


Figure 3-54. Low Pass Filter 37AR1A1FL1 Operational Check, Test Setup.

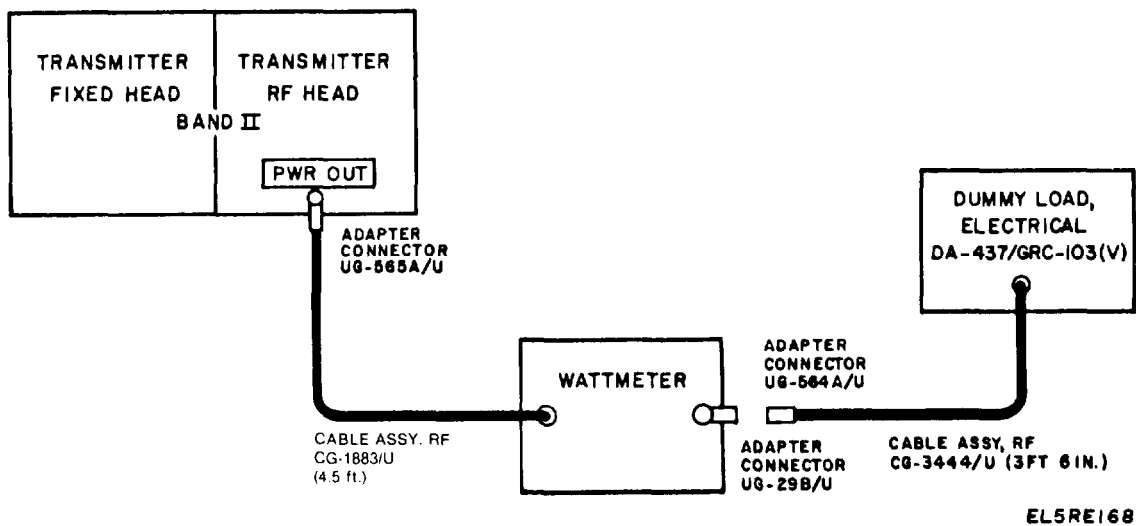
3-79. RF Power Monitor 37AR1A2

a. Test Equipment Required.

| Equipment                                | Common Name         |
|--|---------------------|
| Wattmeter, RF, An/URM-120                | Wattmeter           |
| Cable Assembly, Radio Frequency          | CG-1883/U (4.5 ft.) |
| Cable Assmly, Radio Frequency            |                     |
| CG-3444/U (3 ft. 6 in.)                  |                     |
| Adapter-Connector UG-565A/U              |                     |
| Adapter-Connector UG-29B/U               |                     |
| Adapter-Connector UG-564A/U              |                     |
| Dummy Load, Electrical DA-437/GRC-103(V) |                     |

b. Operational Check.

- (1) Connect the test equipment as shown in figure 3-55.
- (2) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 760.
- (4) Set the transmitter AC POWER switch to ON/RESET.
- (5) Set the transmitter switch to PWR CUT and adjust the PWR OUT PEAK control for maximum indication on the meter. The wattmeter should indicate a minimum of 25 watts.
- (6) Set the AC POWER switch to OFF. If an abnormal indication is obtained, replace power monitor 37AR1A2 as described in paragraph 3-93.



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Figure 3-55. RF Power Monitor 37AR1A2 Operational Check, Test Setup.

3-80. Duplexer Subassembly 33A1A1 and Monitor RF Power 33A3

a. Test Equipment Required.

| Equipment                                   | Common Name               |
|---|---------------------------|
| Wattmeter, RF, An/URM-120                   | Wattmeter                 |
| Generator, Signal SG-340A/G                 | Signal Generator No. 2    |
| Voltmeter, Electronic, 11E-30A/U            | VTVM                      |
| Load, 51 ohms                               | CMC 335-053               |
| Dummy Load, Electrical DA-437/GRC-103(V)    |                           |
| Adapter-Connector UG-565A/U                 |                           |
| Adapter-Connector UG-29B/U                  |                           |
| Adapter-Connector UG-564A/U                 |                           |
| Adapter-Connector UG-274/U                  |                           |
| Adapter-Connector, Omni Spectra 21010       | Adapter-connector OS21010 |
| Cable Assembly, RF, CG-3444/U (1 ft. 6 in.) |                           |
| Cable Assembly, RF, CG-3444/U (3 ft. 6 in.) |                           |
| Cable Assembly, Radio Frequency             | CG-1883/U (4.5 ft.)       |
| Cable Assembly, Radio Frequency             | CG-409H/U (4.5 ft.)       |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U                |

b. Operational Check.

- (1) Connect the test equipment as shown in figure 3-56.
- (2) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 760.

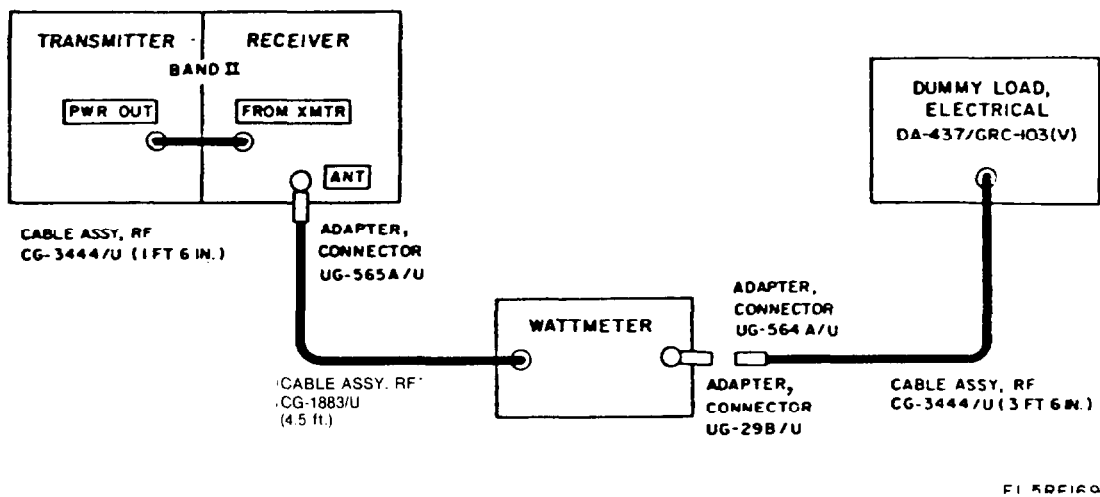


Figure 3-56. Duplexer Subassembly 33A1A1, (Transmit) Operational Check, Test Setup.

- (4) Set the transmitter AC POWER switch to ON/RESET. The wattmeter should indicate 15 watts minimum.
- (5) Set the AC POWER switch to OFF. If an abnormal reading is obtained in (4) above, replace the receiver rf head.

C. Operational Check-Receiver Path

- (1) Disconnect plug P1 (33A1A1J2) from connector 33A1A1J2 on duplexer 33A1A1 (fig. 3-57).
- (2) Connect the test equipment as shown in A, figure 3-58.
- (3) Tune the receiver to channel 640.
- (4) Set the frequency of signal generator No. 2 to 520 MHz and adjust the output level until a reading of -50 dBm is obtained on the VTVM. Note the attenuator setting on signal generator No. 2.
- (5) Reconnect plug P1 (33A1A1J2) to 33A1A1J2.

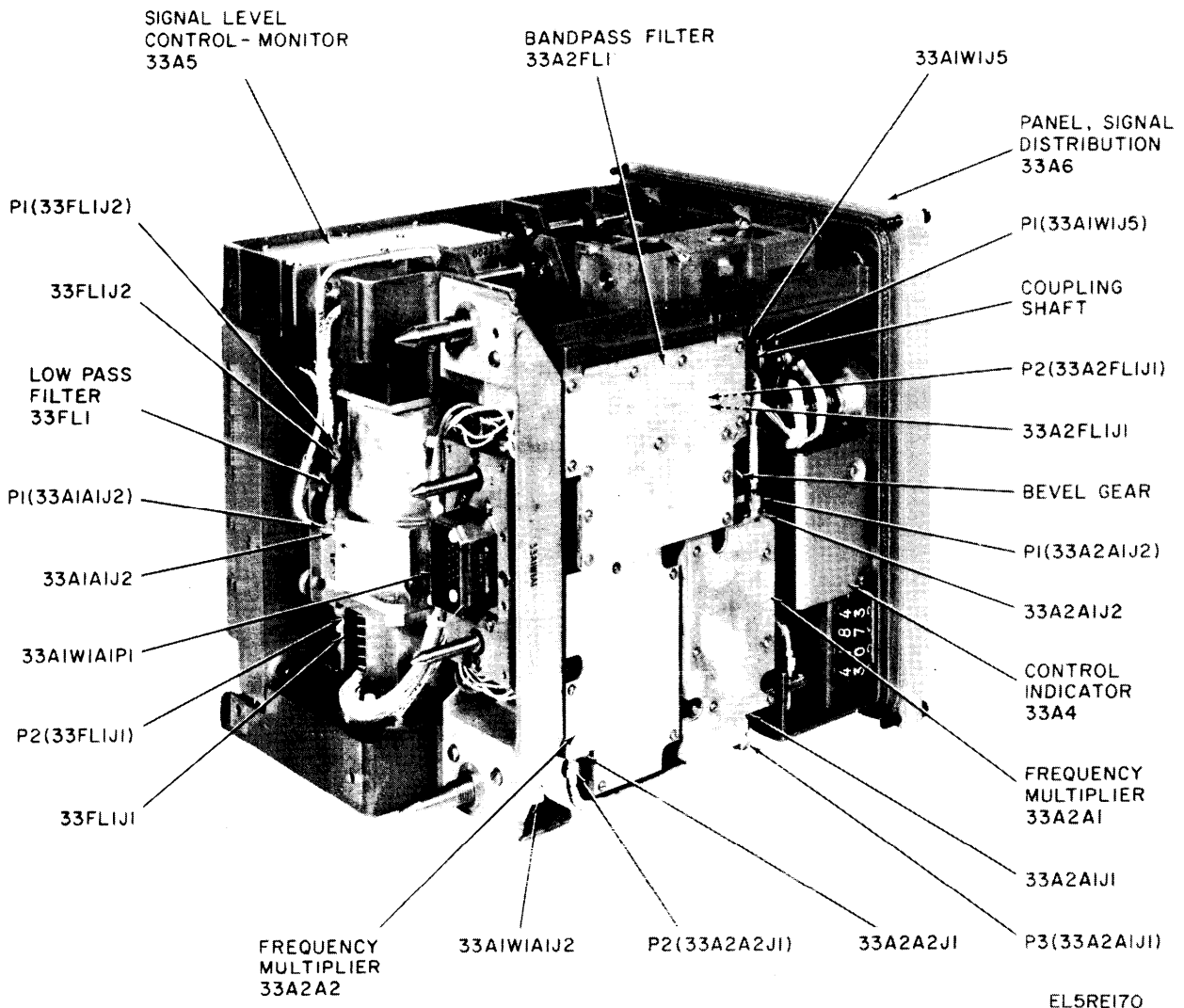
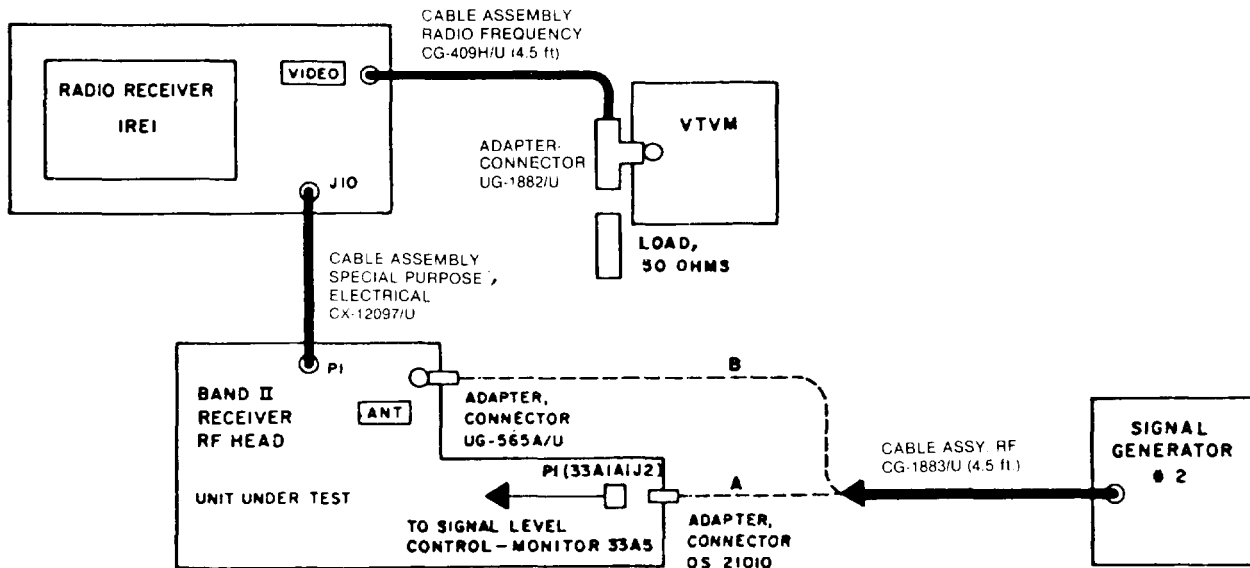


Figure 3-57. Band II Receiver RF Head, Top and Rear View.





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Figure 3-58. Duplexer Subassembly 33A1A1, (Receive) Operational Check, Test Setup.

- (6) Connect the test equipment as shown in B, figure 3-58.
- (7) Increase the output of signal generator No.2 until a reading of -50 dbm is obtained on the VTVM. The output attenuator setting on signal generator No. 2 should not be more than 2.5 db lower than the setting noted in (4) above.
- (8) If the indication in (7) above is not obtained, replace the receiver rf head.

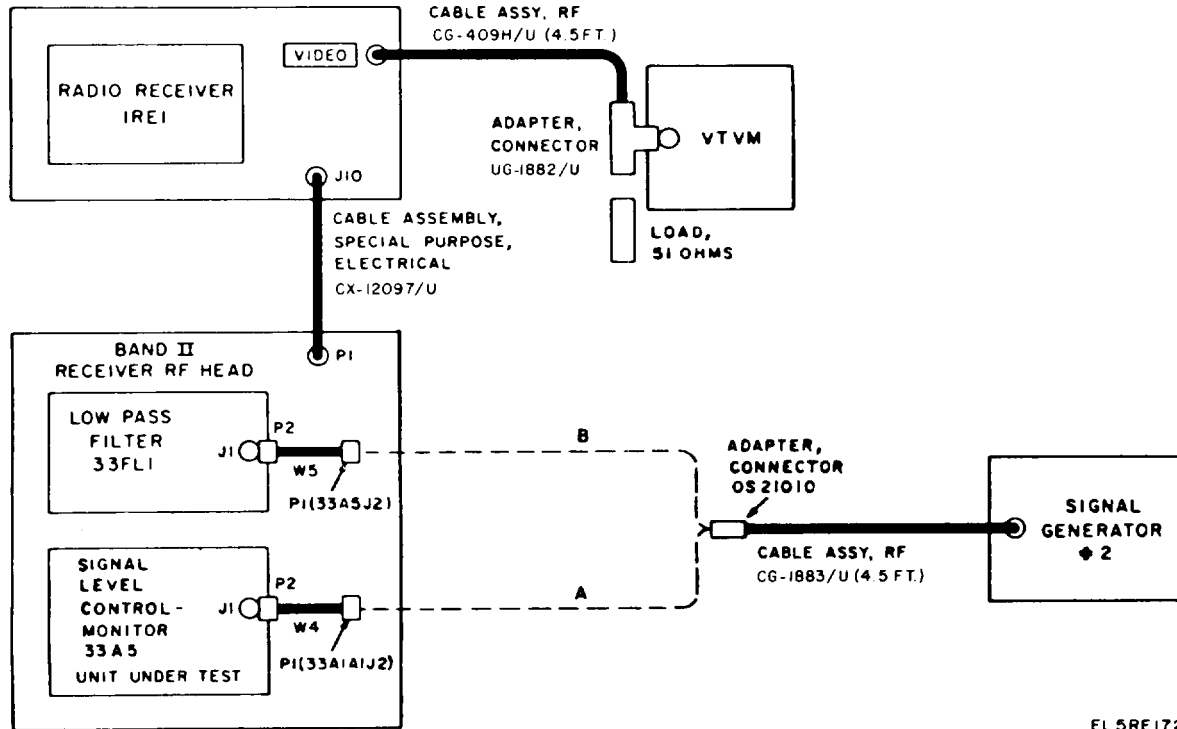
3-81. Signal Level Control-Monitor 33A5

a. Test Equipment Required

| Equipment                                   | Common Name               |
|---|---------------------------|
| Voltmeter, Electronic, ME-30A/U             | VTVM                      |
| Generator, Signal SG-340A/G                 | Signal Generator No. 2    |
| Load, 51 ohms                               | CMC 335-053               |
| Adapter-Connector, Omni Spectra 21010       | Adapter-connector OS21010 |
| Adapter-Connector, UG-274/U                 |                           |
| Cable Assembly, Radio Frequency             | CG-409H/(4.5 ft.)         |
| Cable Assembly, Radio Frequency             | CG-1883/U (4.5 ft.)       |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U                |

b. Operational Check.

- (1) Disconnect plug P1 (33A1A1J2) (fig. 3-57) from 33 A1A1J2 on duplexer 33 A1A1.
- (2) Connect the test equipment as shown in A, figure 3-59.
- (3) Tune the receiver to channel 640 and signal generator No. 2 to 520 MHz.
- (4) Set the AC POWER switch to ON.
- (5) Increase the output level of signal generator No. 2 until the high signal alarm operates (buzzer may sound if not muted). the signal generator No. 2 level will be 0 dBm±10 dBm.
- (6) Decrease the level of signal generator No. 2 until the VTVM indicates -50 dBm.
- (7) Connect the test equipment as shown in B, figure 3-59.
- (8) The indication on the VTVM should not be higher than -49.25 dBm.
- (9) Set the AC POWER switch to OFF.
- (10) If the high signal alarm does not come on in (5) above, and/or the indication obtained in (8) above is beyond the specified limit, the unit under test should be replaced. Refer to paragraph 3-97 for replacement procedures.



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Figure 3-59. Signal Level Control Monitor 33A5 Operational Check, Test Setup.

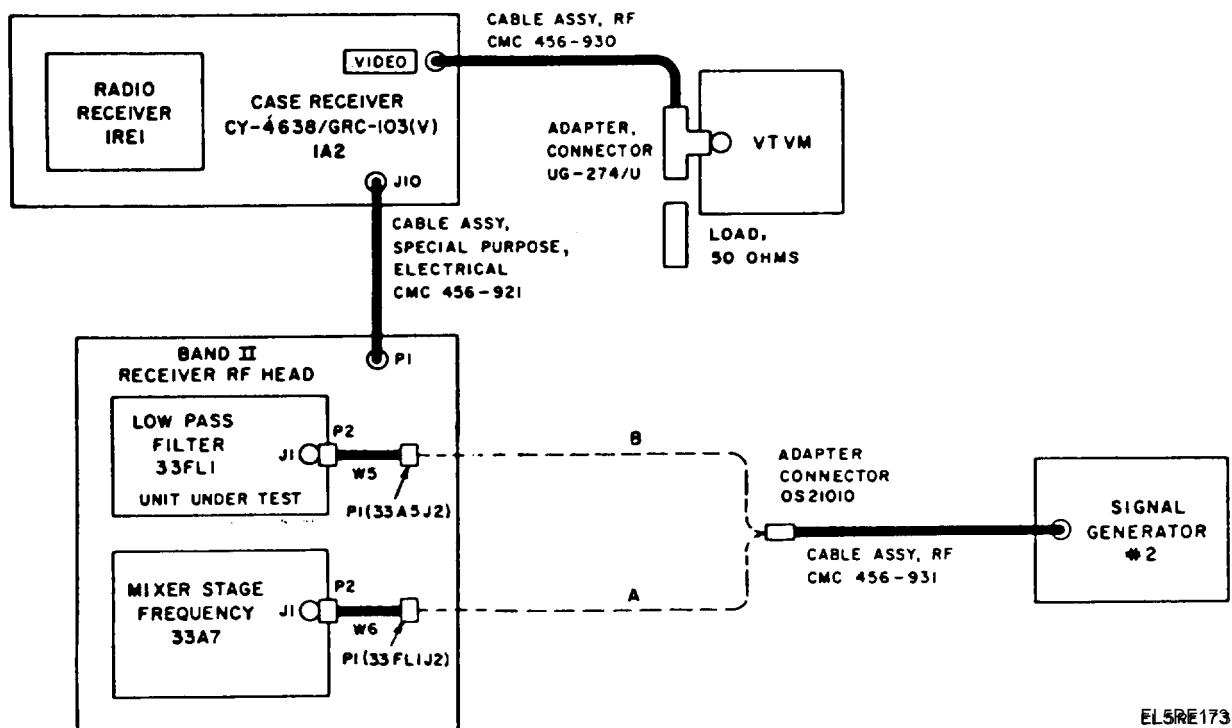
3-82. Low-Pass Filter 33FL1

a. Test Equipment Required.

| Equipment                                   | Common Name               |
|---|---------------------------|
| Voltmeter, Electronic, ME-30A/U             | VTVM                      |
| Generator, Signal, SG-340A/U                | Signal generator No. 2    |
| Load, 51 ohms                               | CMC 335-053               |
| Adapter-Connector Omni Spectra 21010        | Adapter-connector OS21010 |
| Adapter-Connector UG-274/U                  |                           |
| Cable Assembly, Radio Frequency             | CG-409H/U (4.5 ft.)       |
| Cable Assembly, Radio Frequency             | CG-1883/U (4.5 ft.)       |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U                |

b. Operational Check.

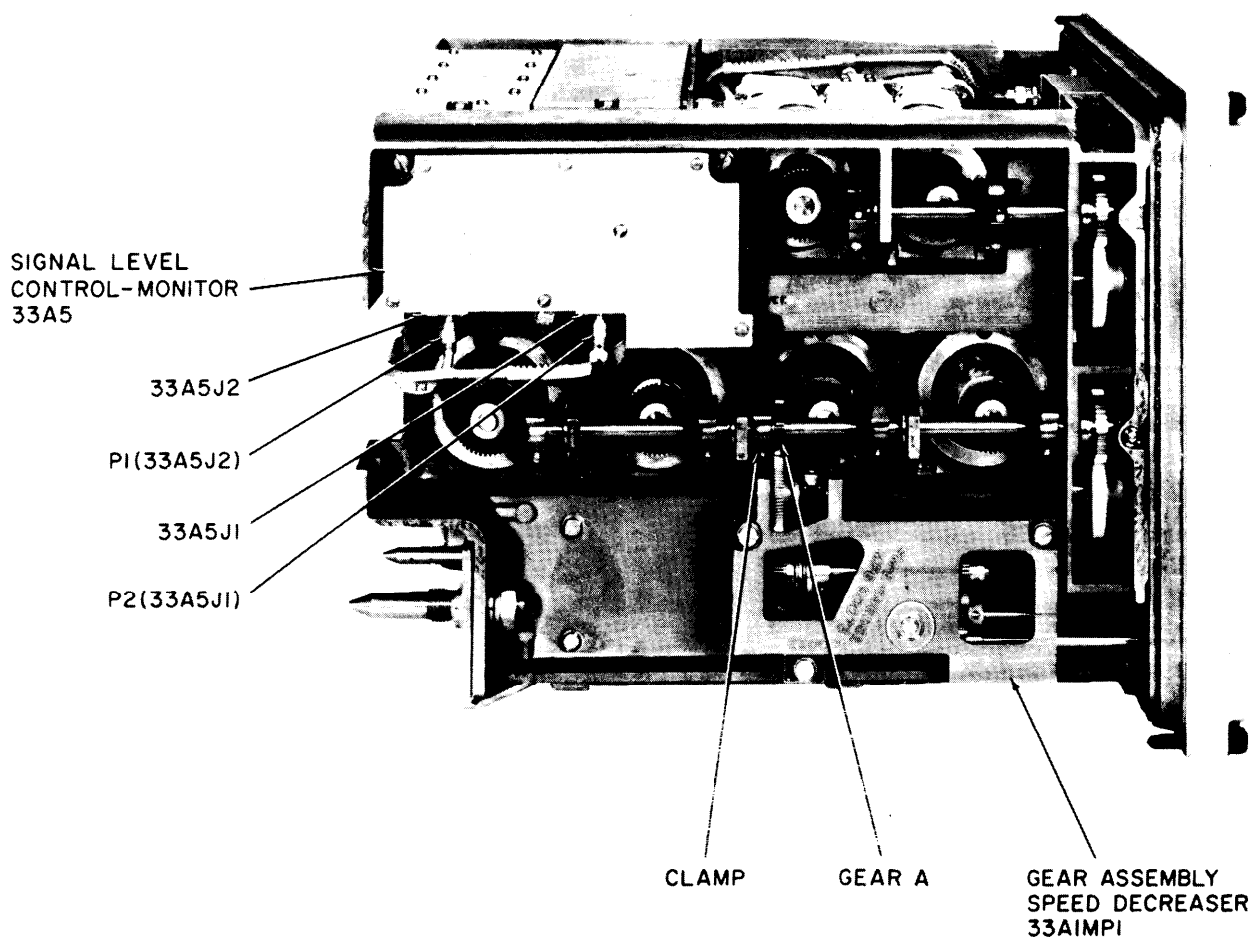
- (1) Disconnect plug P1 (33FL1J2) from 33FL1J2 on filter low-pass 33FL1 (fig. 3-57).
- (2) Connect the test equipment as shown in A, figure 3-60.



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Figure 3-60. Low Pass Filter 33FL1 Operational Check, Test Setup.

- (3) Tune the receiver to channel 640 and signal generator No. 2 to 520 MHz.
- (4) Set the AC POWER switch to ON.
- (5) Adjust the output level of signal generator No. 2 until a reading of -50 dBm is obtained on the VTVM.
- (6) Reconnect plug PI (33FL1J2) to 33FL1J2.
- (7) Disconnect plug P1 (33A5J2) (fig. 3-61) from 33A5J2 on signal level control monitor 33A5.
- (8) Connect the test equipment as shown in B, figure 3-60.
- (9) The indication on the VTVM should not be greater than -49.5 dBm.
- (10) If an abnormal indication is obtained in (9) above, replace 33FL1. Refer to paragraph 3-104 for replacement procedures.



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Figure 3-61. Band II Receiver RF Head, Right Side View.

3-83. Frequency Multiplier 33A2A2

a. Test Equipment Required.

| Equipment  | Common Name                  |
|--|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A  | Power Meter Thermistor Mount |
| Attenuator Fixed Empire Devices AT-75-10               | 10 db attenuator             |
| Adapter-Connector Omni Spectra 21010                   | Adapter-connector OS21010    |
| Adapter-Connector UG-29B/U                             |                              |
| Cable Assembly, Radio Frequency CG-11383/U (4.5 ft.)   |                              |
| Cable Assembly, Special Purpose, Electrical CX-12097/U |                              |

b. Operational Check.

- (1) Disconnect plug P3 (33A2A1J1) from 33A2A1J1 on frequency Multiplier 33A2A1 (fig. 3-56).
- (2) Connect the test equipment as shown in figure 3-62.
- (3) Set the AC POWER switch to ON and tune the receiver to channel 699. The output power level at P3 (33A2A1J1) should be +17 dBm  $\pm$ 2.5 db (power meter indication of +7 dBm  $\pm$ 2.5 db).
- (4) Set the RCVR CHANNEL control to channel 700. The power meter indication should be +17 dBm  $\pm$ 2.5 db (power meter indication of +7 dBm  $\pm$ 2.5 db).

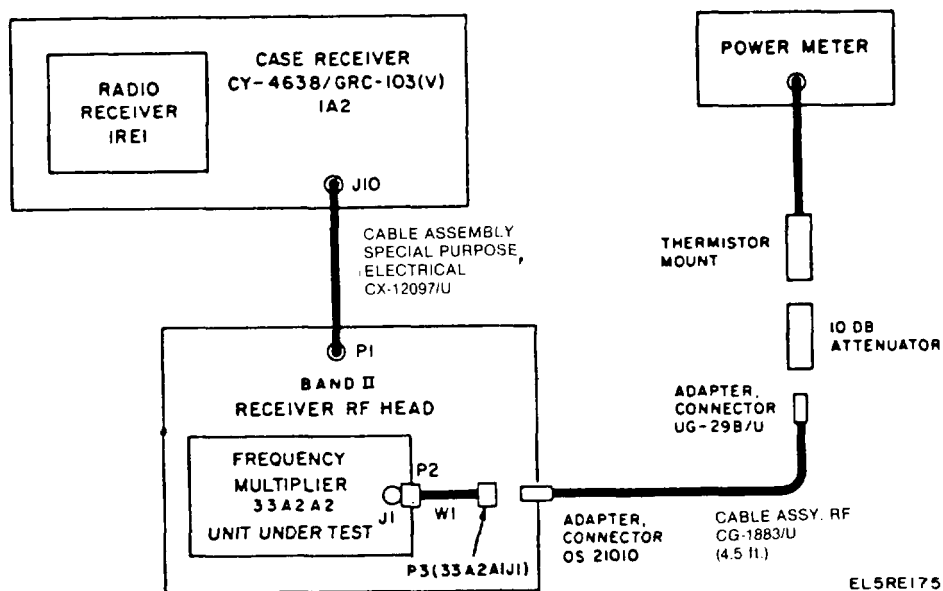


Figure 3-62. Frequency Multiplier 33A2A2 Operational Check, Test Setup.

- (5) Set the AC POWER switch to OFF. If the indications in (3) and (4) above are not within the specified limits, replace receiver rf head.

3-84. Frequency Multiplier 33A2A1

a. Test Equipment Required.

| Equipment   | Common Name                  |
|---|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Attenuator Fixed Empire Devices AT-7510               | 10 db attenuator             |
| Adapter-Connector Omni Spectra 21010                  | Adapter-connector OS21010    |
| Adapter-Connector UG-29B/U                            |                              |
| Cable Assembly, Radio Frequency                       | CG-1883/U (4.5 ft.)          |
| Cable Assembly, Special Purpose, Electrical           | CX-12097/U                   |

b. Operational Check.

- (1) Disconnect plug P2 (33A2FL1J1) from 33A2FL1J1 on bandpass filter 33A2FL1JI (fig. 3-57).
- (2) Connect the test equipment as shown in figure 3-63.
- (3) Set the AC POWER switch to ON and tune the receiver to channel 699. The output power level at P2 (33A2FL1J1) should be a minimum of 8.0 dBm (power meter indication of -2 dBm).

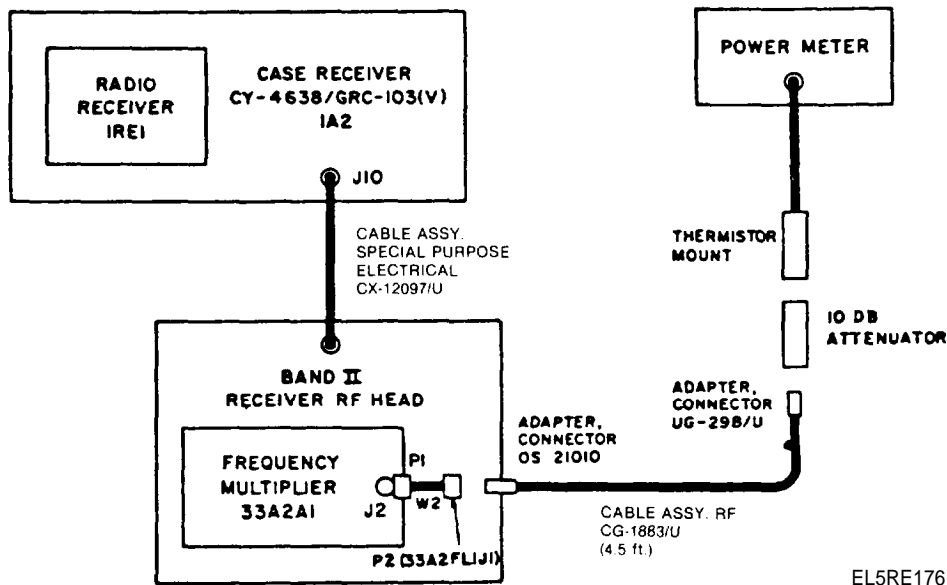


Figure 3-63. Frequency Multiplier 33A2A1 Operational Check, Test Setup.

- (4) Set the RCVR CHANNEL control to channel 700. The power meter indication should still be a minimum of +8.0 dBm.
- (5) Set the AC POWER switch to OFF. If the indications in (3) and (4) above are not within the specified limits, replace the receiver rf head.

3-85. Bandpass Filter 33A2FL1

a. Test Equipment Required

| Equipment   | Common Name                  |
|---|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Attenuator Fixed Empire Devices AT-75-10              | 10 db attenuator             |
| Adapter-Connector Omni Spectra 21010                  | Adapter-connector 0S21010    |
| Adapter-Connector UG-29B/U                            |                              |
| Cable Assembly, Radio Frequency                       | CG-1883/U (4.5 ft.)          |
| Cable Assembly, Special Purpose, Electrical           | CX-12097/U                   |

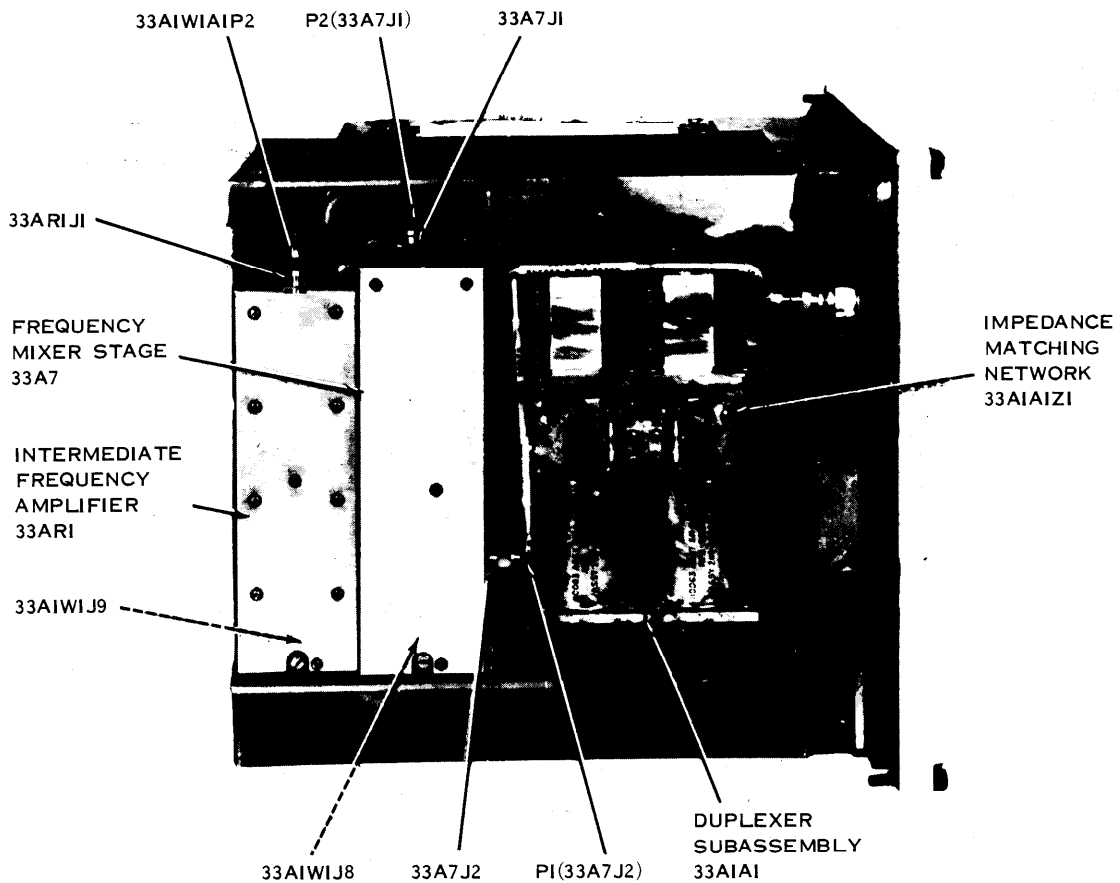
b. Operational Check

- (1) Disconnect plug P1 (33A7J2) from 33A7J2 of frequency mixer stage 33A7 (fig. 3-64).
- (2) Connect the test equipment as shown in figure 3-65.
- (3) Set the AC POWER switch to ON and tune the receiver to channel 699. The output power level at P1 (33A7J2) should be a minimum of +6.0 dBm (power meter indication of -4.0 dBm).
- (4) Set the RCVR CHANNEL control to channel 700. The power meter indication should still be a minimum of +6.0 dBm (power meter indication of -4.0 dBm).
- (5) Set the AC POWER switch to OFF. If the indications in (3) and (4) above are not within the specified limits, replace the receiver rf head.

3-86. Intermediate Frequency Amplifier 33AR1

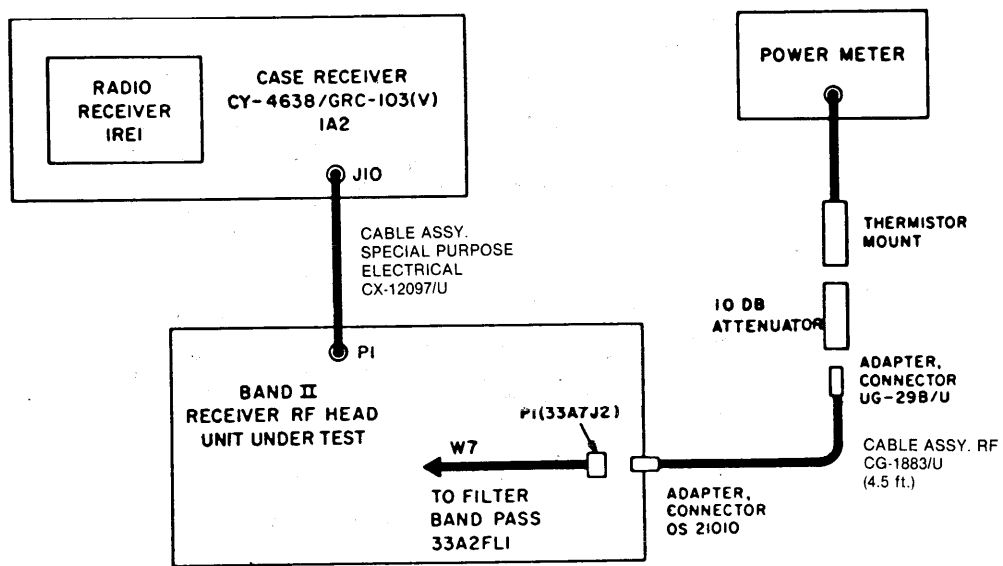
a. Test Equipment Required

| Equipment   | Common Name                  |
|---|------------------------------|
| Generator, Signal, SG-1170/U                          | Signal Generator             |
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Adapter-Connector UG-201A/U                           |                              |



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Figure 3-64. Band II Receiver RF Head, Bottom View.



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Figure 3-65. Bandpass Filter 33A2FL1 Operational Check, Test setup.



a. Test Equipment Required-Continued.

| Equipment                                   | Common Name       |
|---|-------------------|
| Adapter-Connector, OS-20200-2               |                   |
| Adapter-Connector, OS-21010                 |                   |
| Voltmeter, RF, ME-426/U                     | RF, Voltmeter     |
| Cable Assembly, RF                          | CG-3581/U (6 in.) |
| Cable Assembly, RF CG-409H/U (3 ft.)        |                   |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U        |

b. Operational Check.

- (1) Remove frequency mixer stage 33A7 as explained in paragraph 3-102. (Connector 33A1W1J8 (fig. 3-64) is now exposed.)
- (2) Disconnect plug 33A1W1A1P2 from 33AR1J1 on intermediate frequency amplifier 33AR1 (fig. 3-64).
- (3) Connect the test equipment as shown in figure 3-66.
- (4) Set the frequency of signal generator No. 1 to 30 MHz at an output level of -75 dBm.
- (5) Set the receiver AC POWER switch to ON. The RF voltmeter should indicate between -28 dBm and -22 dBm.

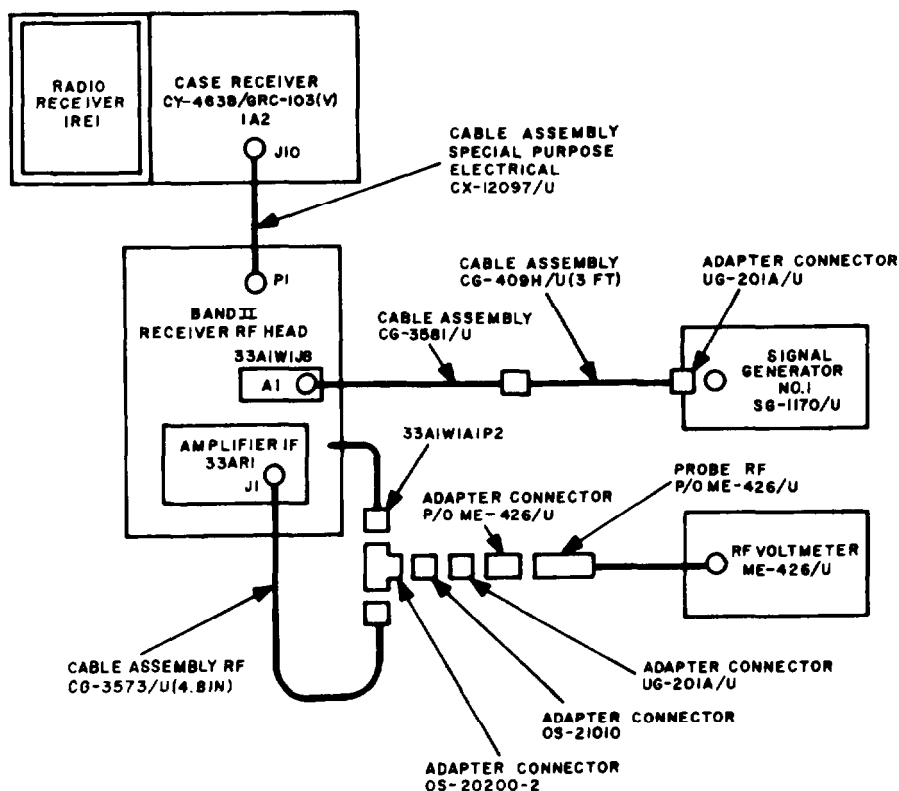


Figure 3-66. Intermediate Frequency Amplifier 33AR1 Operational Check, Test Setup.

- (6) Set the receiver AC POWER switch to OFF. If the indication obtained in (5) above is outside the specified limits, replace the intermediate amplifier 33AR1. Refer to paragraph 3-101 for replacement procedures.

3-87. Frequency Mixer Stage 33A7

a. Test Equipment Required

| Equipment   | Common Name                  |
|---|------------------------------|
| Generator, Signal SG-340A/U                           | Signal generator No. 2       |
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Adapter-Connector, OS-20200-2                         |                              |
| Adapter-Connector, UG-201A/U                          |                              |
| Cable Assembly, RF CG-3573/U (4.8 in.) (2 required)   |                              |
| Cable Assembly, RF                                    | CG-1883/U (4.5 ft.)          |
| Cable Assembly, Special Purpose, Electrical           | CX-12097/U                   |
| Voltmeter, RF, ME-426/U                               | RF, Voltmeter                |

b. Operational Check.

- (1) Disconnect plug P2 (33A7J1) from 33A7J1 of frequency mixer stage 33A7 (fig. 3-64).
- (2) Disconnect plug 33A1W1A1P2 from 33AR1J1 on intermediate frequency amplifier 33AR1.
- (3) Connect the test equipment as shown in figure 3-67.
- (4) Tune the receiver to channel 624.
- (5) Set the frequency of signal generator No. 2 to 512 MHz at an output level of -89 dBm.
- (6) Set the receiver AC POWER switch to ON. The RF voltmeter should indicate between -28 dBm and -22 dBm.
- (7) If the indication obtained in (6) above is outside the specified limits replace frequency mixer stage 33A7 as described in paragraph 3-102.

3-88. Power Supply 33PS1

a. Test Equipment Required

| Equipment                                   | Common Name        |
|---|--------------------|
| Multimeter, Digital, AN/USM-486             | Digital Multimeter |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U         |

b. Operational Checks.

- (1) Remove the receiver rf head from receiver case and connect it to the receiver case using cable CX-12097/U.
- (2) Remove frequency mixer stage 33A7 as described in paragraph 3-100
- (3) Connect a jumper wire between pin 7 and pin 8 and between pins 5 and 9 of chassis 33A1W1J8 (fig. 3-63).
- (4) Set receiver AC POWER switch to ON.
- (5) Multimeter connected between pin 7 (+) and pin 5 (-) of chassis connector 33A1W1J8 should measure 70 volts dc  $\pm 0.5$  volt dc.
- (6) if the indication in (5) above is not obtained, replace power supply 33PS1. Refer to paragraph 3-101 for replacement procedures.

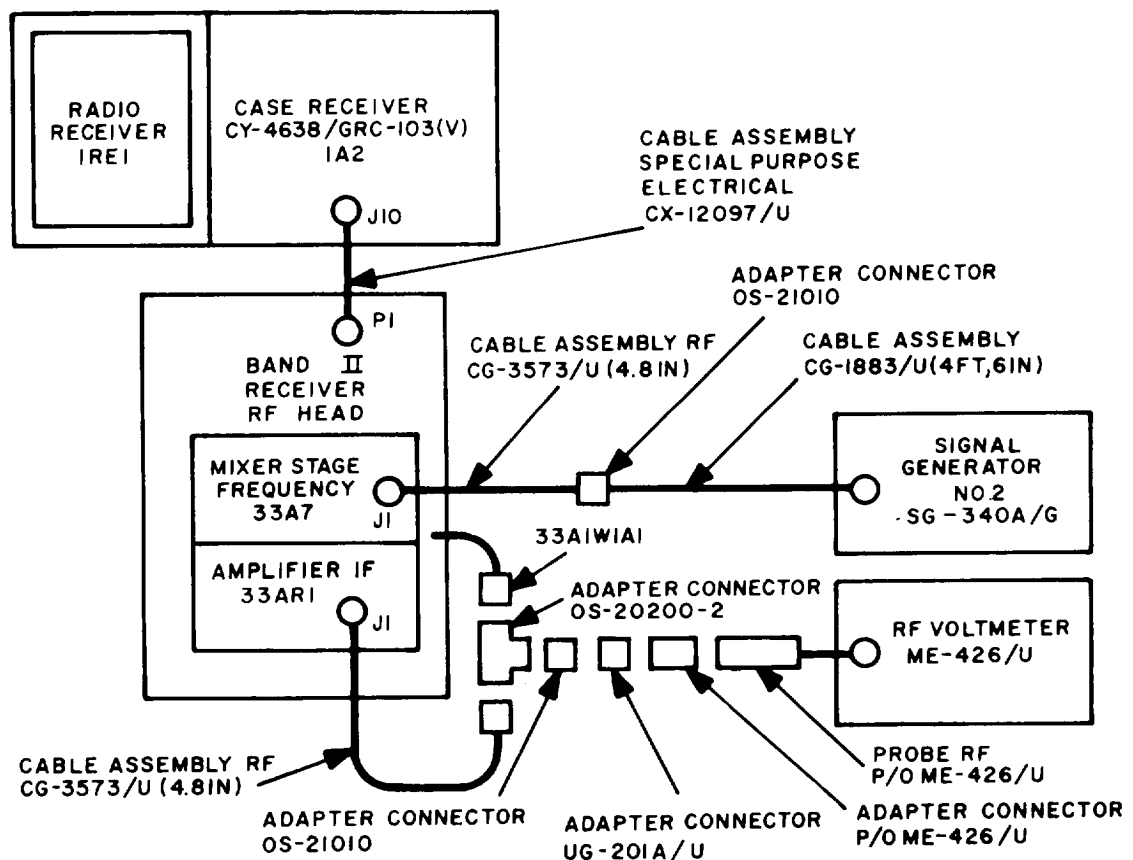


Figure 3-67. Frequency Mixer Stage 33A7 Operational Check, Test Setup.

3-89. Voltage Control Assembly 33A1A2

a. Test Equipment Required.

| Equipment                         | Common Name        |
|-----------------------------------|--------------------|
| Multimeter, Digital, AN/USM-486/U | Digital Multimeter |

b. Operational Check.

- (1) Remove the receiver rf head from the receiver case.
- (2) Locate voltage control assembly 33A1A2 (fig. 3-61).
- (3) Measure the resistance between E1 and E3 using the multimeter. The indication obtained should be 20K ohms  $\pm$ 200 ohms.
- (4) Check the resistance between E1 and E2 while slowly adjusting the variable resistor from full clockwise to full counter-clockwise. The multimeter indication should change smoothly across the resistance range of zero to 20K ohms.
- (5) If the indications in (3) and/or (4) above are abnormal, replace the receiver RF head.

3-90. Control-Indicator 33A4

a. Test Equipment Required.

| Equipment                                   | Common Name        |
|---|--------------------|
| Multimeter, Digital, AN/USM-486             | Digital Multimeter |
| Cable Assembly, Special Purpose, Electrical | CX-12098/U         |
| Cable Assembly, Special Purpose Electrical  | CX-12097/U         |

b. Operational Check.

- (1) Loosen the screws securing plug P1 (33A1W1J5) to chassis connector 33A1W1J5 and disconnect the plug (fig. 3-57).
- (2) Set the RCVR CHANNEL control to channel 564.
- (3) Using the multimeter, check for the correct resistance between the following pins of P1 (33A1W1J5) as shown in the chart below.

| Pins     | Resistance |
|----------|------------|
| 1 and 14 | Infinity   |
| 2 and 14 | Infinity   |
| 3 and 14 | Infinity   |

| Pins      | Resistance |
|-----------|------------|
| 4 and 14  | Infinity   |
| 5 and 14  | Infinity   |
| 6 and 14  | Infinity   |
| 7 and 14  | Infinity   |
| 8 and 14  | Infinity   |
| 9 and 14  | Infinity   |
| 10 and 14 | Infinity   |
| 11 and 14 | Infinity   |
| 12 and 14 | Zero       |

(4) Set the RCVR CHANNEL control to channel 563.

(5) Using the multimeter, check for correct resistance between the following pins of P1 (33A1W1J5) as shown in the chart below.

| Pins      | Resistance |
|-----------|------------|
| 1 and 14  | Infinity   |
| 2 and 14  | Zero       |
| 3 and 14  | Zero       |
| 4 and 14  | Zero       |
| 5 and 14  | Zero       |
| 6 and 14  | Zero       |
| 7 and 14  | Zero       |
| 8 and 14  | Zero       |
| 9 and 14  | Zero       |
| 10 and 14 | Zero       |
| 11 and 14 | Zero       |
| 12 and 14 | Infinity   |

(6) Remove control-indicator 33A4 from the transmitter rf head as described in chapter 6, TM 1-5820-540-12.

(7) Connect plug P1 (33A1W1J5) to chassis connector 33A1W1J5 using cable CX-12098/U.

(8) Remove the four screws securing the control-indicator cover and remove the cover.

(9) Connect the receiver rf head to the receiver case using cable CMC 756-921 and set the AC POWER switch to ON.

(10) Set the control indicator to channel 699.

(11) Check the voltage at pin 13 of P1 (33A1W1J5) using the multimeter. The multimeter should indicate zero.

- (12) Set the control-indicator to channel 700.
- (13) Check the voltage at pin 13 of P1 (33A1W1J5) using the multimeter. The indication should be +26 volts dc.
- (14) Set the AC POWER switch to OFF. Reinstall the control indicator cover. If abnormal indications are obtained in either (3), (5), (11) or (13) above, replace control-indicator 33A4. Refer to chapter 6, TM 11-5820-540-12 for replacement procedures.

Section V. MODULE REMOVAL AND REPLACEMENT PROCEDURES  
FOR BAND II RF HEADS

3-91. General

When trouble has been localized to a module of the radio set, replace the defective part as described in paragraphs 3-94 to 3-104. Before installing a replacement module, always check connectors for bent or damaged pins. Make sure the multipin connectors are properly mated and pressed home before tightening the mounting screws: Whenever difficulty is encountered in mating connectors, remove the module and inspect the connectors for damage.

3-92. Replacement of Control-Indicator 37A2

Replacement of control-indicator 37A2 is covered in chapter 6, TM 11-5820-540-12.

3-93. Replacement of Low-Pass Filter 37AR1A2FL1

- a. Place the transmitter rf head right-hand side up and locate low-pass filter 37AR1A1FL1 (fig. 3-51).
- b. Disconnect the two electrical plugs, P2 (37AR1A1FL1J1) and P1 (37AR1A1FL1J2) from their mating connectors (fig. 3-51).
- c. Loosen the green-circled mounting screws that secure 37AR1A1FL1 to the chassis. Remove 37AR1A1FL1.
- d. To install the 37AR1A1FL1 replacement module, position the module over the two mounting holes and tighten the mounting screws. Connect plugs P1 (37AR1A1FL1J2) and P2 (37AR1A1FL1J1) to their respective mating connectors.

3-94. Replacement of RF Power Monitor 37AR1A2

- a. Place the transmitter rf head top side up and locate rf power monitor 37AR1A2 (fig. 3-51).
- b. On the front panel of the transmitter rf head, loosen and remove the hexagonal nut that secures the PWR OUT connector to the front panel.
- c. Disconnect plug P2 (37AR1A2J1) from 37AR1A2J1 (fig. 3-51).

- d. Disconnect plug P1 (37AR1A1W1J4) from connector 37AR1A1W1J4 (fig. 3-50).
- e. Remove the four red-circled mounting screws that secure rf power monitor 37AR1A2 to its bracket and remove the module.
- f. To install the 37AR1A2 replacement module, slide connector J2 of the rf power monitor into the PWR CUT opening in the front panel and secure the hexagonal nut. Secure 37AR1A2 to its mounting bracket with four screws.

## NOTE

The PWR OUT connector must be well-secured before tightening the 37AR1A2 mounting screws.

- g. Connect plug P2 (37AR1A2J1) to 37AR1A2J1. Connect plug P1 (37AR1A1W1J4) to 37AR1A1W1J4 on the chassis and secure with two screws.

## 3-95. Replacement of Voltage Regulator Assembly 37AR1A1A1

- a. Place the transmitter rf head right-hand side up.
- b. Locate the voltage regulator assembly 37AR1A1A1 (fig. 3-52). Loosen and remove the four green-circled mounting screws. Pull the module up, carefully disengaging the connector.
- c. To install the replacement module, carefully engage the connector of the module with the chassis connector by pushing the module straight down.
- d. Tighten the four green-circled screws.

## 3-96. Replacement of Control-Indicator 33A4

Replacement of control-indicator 33A4 is covered in chapter 6, TM 11-5820-540-12.

## 3-97. Replacement of Frequency Multiplier 33A2A2

- a. Place the receiver rf head top side up and locate frequency multiplier 33A2A2 (fig. 3-57).
- b. Disconnect plug P2 (33A2A2J1) from 33A2A2J1 of frequency multiplier 33A2A2.
- c. Loosen three green-circled mounting screws and carefully lift the module, disengaging it from the chassis connector.
- d. To install the 33A2A2 replacement module, position the module over three mounting holes and carefully press home the connector.
- e. Tighten the three mounting screws and connect the plug P2 (33A2A2J1) to 33A2A2J1.

3-98. Replacement of Signal Level Control-Monitor 33A5

- a. Place the receiver right-hand side up and locate signal level control-monitor 33A5 (fig. 3-61).
- b. Disconnect P1 (33A5J2) and P2 (33A5J1) from their mating connectors.
- c. Loosen three green-circled mounting screws and carefully lift the module, disengaging it from the chassis connector.
- d. To install the 33A5 replacement module, position the module over the mounting holes and carefully press home the connector.
- e. Tighten the mounting screws and connect plugs P1 (33A5J2) and P2 (33A5J1) to 33A5J2 and J1 respectively.

3-99. Replacement of Intermediate Frequency Amplifier 33AR1

- a. Place the receiver rf head bottom side up and locate intermediate frequency amplifier 33AR1 (fig. 3-64).
- b. Disconnect plug 33A1W1A1P2 from 33AR1J1.
- c. Loosen the three green-circled mounting screws and carefully lift the module, disengaging it from the chassis connector.
- d. To install the replacement module, position the module over the mounting holes and carefully press home the connector.
- e. Tighten the three mounting screws and reconnect plug 33A1W1A1P2 to 33AR1J1.

3-100. Replacement of Frequency Mixer Stage 33A7

- a. Place the receiver rf head bottom side up and locate frequency mixer stage 33A7 (fig. 3-64).
- b. Disconnect plugs P1 (33A7J2) and P2 (33A7J1) from 33A7J2 and 33A7J1 respectively.
- c. Loosen the three green-circled mounting screws and carefully lift the module, disengaging it from the chassis connector.
- d. To install the replacement module, position the module over the mounting holes and carefully press home the connector.
- e. Tighten the three mounting screws and reconnect P1 (33A7J2) and P2 (33A7J1) to 33A7J2 and 33A7J1 respectively.

3-101. Replacement of Power Supply 33PS1

- a. Place the receiver rf head left-hand side up and locate power supply 33PS1.



- b. Loosen the three green-circled mounting screws and carefully lift the module, disengaging it from the chassis connector.
- c. To install the replacement module, position the module over the mounting holes and carefully press home the connector.
- d. Tighten the three mounting screws.

### 3-102. Replacement of Low-Pass Filter 33FL1

- a. Place the receiver rf head rear side up. Locate low-pass filter 33FL1 (fig. 3-57) .
- b. Disconnect plug P1 (33FL1J2) and P2 (33FL1J1) from their respective connectors.
- c. Place the receiver rf head bottom side up and remove intermediate frequency amplifier 33AR1 as explained in paragraph 3-101.
- d. Remove the two mounting screws for 33FL1 which are located on the chassis under the if amplifier.
- e. To install the 33FL1 replacement module, position the module on the mounting holes and tighten the two screws from the other side of the chassis.
- f. Replace intermediate frequency amplifier 33AR1 as explained in paragraph 3-101.
- g. Connect plugs P1 (33FL1J2) and P2 (33FL1J1) to their respective connectors.

## Section VI. TROUBLESHOOTING (BAND III)

### 3-103. General

This section contains the systematic troubleshooting procedure required to sectionalize a fault in the radio set and to trace the fault to the defective module or part. Meter readings may help in locating faults without the help of test equipment or measuring circuits. Operational tests frequently indicate the general location of trouble and in many instances help in determining the nature of the fault. The operational check, loop testing procedure and the troubleshooting charts contained in TM 11-5820-540-12 are suitable starting points. The modified loop test procedure, troubleshooting charts and signal substitution procedures enable direct support personnel to quickly localize the faulty module. Replacement of one or more suspected defective modules may be a quick and effective method of repairing a radio set in emergency conditions.

### 3-104. Loop Test Procedure

Refer to paragraph 3-4.

3-105. Transmitter Troubleshooting

CAUTION

The transmitter rf head when extended must be air-cooled during tests; a cooling fan must be pointed toward the power amplifier tubes at all times. If a cooling fan is not available the transmitter rf head must not be operated for longer than 5 minute periods. Another alternative is to place the transmitter in the transmitter case while troubleshooting radio transmitter 5TR1.

a. General. Troubleshooting charts contain troubleshooting procedures for radio transmitter 5TR1 and the transmitter rf head. Paragraphs 3-110 through 3-116 contain test procedures for the transmitter rf head only. Refer to paragraphs 3-5 through 3-12 for test procedures for radio transmitter 5TR1. For more effective troubleshooting of the transmitter, remove the transmitter rf head and radio transmitter 5TR1 from the transmitter case. Remove the transmitter rf head dust cover. Connect the transmitter rf head to the transmitter case using CX-12094/U extender cable and connect radio transmitter 5TR1 to the transmitter case using CX-12092/U and CX-12093/U extender cables. Connect the transmitter to a 115 volt, 47 to 420 Hz source and proceed to troubleshoot the transmitter.

CAUTION

The transmitter rf head PWR OUT connector must be connected to the dummy load during troubleshooting. Damage to the equipment will result if this is not done.

NOTE

On Transmitter, Radio T-983B(P)/GRC-103(V) the centrifugal fan does not start instantaneously when the AC POWER switch is set to ON/RESET if the transmitter is at room temperature (+25 C), allow a few minutes warm up time. At very cold temperatures, or if the transmitter is warm, the fan should start when the AC POWER switch is set to ON/RESET.

b. Transmitter Troubleshooting Chart.

| Symptom  | Probable cause                                | Checks and corrective measures  |
|--|---|---|
| 1. When AC POWER switch is set to ON/RESET centrifugal fan does not start, AC POWER and LOW POWER lamps do not light, buzzer does not sound. | a. Defective power supply 5TR1PS1 (fig. 3-1). | a. Check for 115 vac at connector J3 (5TR1PS1P1) pins 6 and 7 (para 3-8). If voltage is present, replace 5TR1PS1 (para 3-50). |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom   | Probable cause   | Checks and corrective measures   |
|---|--|--|
| 1. Continued.   | b. Defective switch 5TR1A1CB1 (fig. 3-3).  | b. If voltage not present in a above, check for 115 vac at switch LINE and LOAD terminals. If indications are normal make wiring continuity checks.  |
| 2. 28V and 12V metering reads negative, all other metering zero, LOW POWER and SYNC lamps light.  | Short circuit.   | Check for short on 28 v supply line (F0-4-43, 4-71).   |
| 3. 12V reads negative, 28V full scale, 600V high, DRIVER normal, all other metering zero. LOW POWER and SYNC lamps light.                 | Short circuit.   | Check for short on 12 v supply line (F0-4-43, 4-71).   |
| 4. All metering reads zero, all lamps are inoperative, centrifugal fan operates.  | Short circuit.   | Check for short on 26 v supply line (F0-4-43, 4-71). Check for short on 600v supply line (F0-4-43, 4-71).  |
| 5. 28V normal or zero, 12V normal, DOUBLER, MULT, DRIVER and PWR OUT low, OSC high. LOW POWER and SYNC lamps light.                       | Open circuit.  | Check for open 28 v supply (F0-4-43, 4-71).  |
| 6. When AC POWER switch is set to ON/RESET, centrifugal fan does not start; AC POWER, LOW POWER, and OVERHEAT lamps light; buzzer sounds. | <p>a. Defective centrifugal fan 5A2B1 (Section X).</p> <p>b. Defective power supply 5TR1PS1 (fig. 6-8, TM 11-5820-540-12).</p> | <p>a. Check for 140 vac at connector J5(5A2B1P1) pins 1 and 2 (transmitter case). If voltage is present replace 5A2B1 (Section X).</p> <p>b. (1) Check for 140 vac at power supply filter terminals FL5 and FL6 of 5TR1PS1 (fig. 3-2). If no voltage is present replace 5TR1PS1 (para 3-50).</p> |

b. Transmitter Troubleshooting Chart-Continued.

| Symptom   | Probable cause   | Checks and corrective measures   |
|---|--|--|
| 6. Continued.   |  | (2) If voltage is present at FL5 and FL6 of 5TR1PS1 (fig. 3-2) but not at pins 1 and 2 of connector J5 (5 A2B1P1) (section X) in the transmitter case, remove 115 vac power source and check for continuity between these two points.  |
| 7. When AC POWER switch is set to ON/RESET, centrifugal fan does not start. OVERHEAT lamp is not on. Buzzer may or may not sound. All other indications normal. | <ul style="list-style-type: none"> <li>a. Defective OVERHEAT lamp 5TR1A2A2DS4.</li> <li>b. Defective pressure differential monitor 5A2A2.</li> </ul> | <ul style="list-style-type: none"> <li>a. Change indicator lamp 5TR1A2A2DS4.</li> <li>b. Replace 5A2A2 (section X)</li> </ul>  |
| 8. Buzzer does not sound when am alarm lamp lights or goes out.   | <ul style="list-style-type: none"> <li>a. Defective buzzer 5TR1A1DS5 (fig. 3-3).</li> <li>b. Defective switch 5TR1A1S2 (fig. 3-3).</li> </ul>        | <ul style="list-style-type: none"> <li>a. Check for 26 vdc at buzzer terminals. If voltage is present replace the buzzer (para 3-52).</li> <li>b. If voltage is not present at buzzer terminals remove 115 vac power source and check for continuity from the buzzer negative terminal to pin 5 of connector J3 (5 TR1PS1P1) (fig. 3-1) and from the buzzer positive terminal to pin 4 of 5TR1A1J3. If continuity is broken because of 5TR1A1S2, higher category maintenance is required.</li> </ul> |

b. Troubleshooting Chart - Continued

| Symptom   | Probable Cause   | Checks and Corrective Measures  |
|---|--|---|
| 8. Continued.   | c. Defective alarm control (fig. 3-3).   | c. If continuity is broken because of 5TR1A1A2, replace 5TR1A1A2 board (para 3-51).   |
| 9. SYNC light does not go out within 10 seconds after AC POWER switch is set to ON/RESET.                         | a. Defective synthesizer 5TR1A2 (fig. 3-3).<br><br>b. Defective power Supply 5TR1PS1 (fig. 3-1). | a. Extend the synthesizer (para 3-10) and check for 12 v, 26 v, and 28 v at J1 (X5TR1A2P2) (fig. 3-3). If normal indications are obtained, replace synthesizer 5TR1A2 (para 3-48).<br><br>b. If indications in a above are abnormal, check 5TR1PS1 (para 3-8). If abnormal indications are obtained, replace 5TR1PS1 (para 3-50). |
| 10. OVERHEAT amp does not go off with n 10 seconds after AC POWER switch is set to ON/RESET.                      | Defective pressure differential monitor.   | Replace 5A2A2 (Section X).  |
| 11. AC POWER switch set to ON/RESET at room temperature centrifugal fan operates full speed (Case CY-4637A only). | Defective control monitor temperature sensor 5A2A2.  | Check sensor connections. If connections are not defective, replace 5A2A2 (Section X).  |
| 12. DRIVER metering greater than 100%.  | Short circuit in voltage regulator assembly 38AR1A1A1 or rf amplifier 38AR1AR1 (fig. 3-70),      | Replace voltage regulator assembly and two electron tubes. If indication becomes normal, replace one original tube. If the indication still remains normal. replace the other original tube. If indications still remain normal then only the voltage regulator 38AR1A1 was shorted. If the indica-                               |

b. Transmitter Troubleshooting Chart Continued

| Symptom   | Probable Cause  | Checks and Corrective Measures  |
|---|---|---|
| 12. Continued.  |   | tion after replacement of the tubes and voltage regulator assembly does not become normal, higher category of maintenance is required.  |
| 13. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR OUT position reads low.                             | <p>a. Defective rf power monitor 38AR1A2 (fig. 3-70).</p> <p>b. Defective low pass filter 38AR1A1FL1 (fig. 3-70) .</p> <p>c. Defective circulator 38AR1HY1 (fig. 3-74).</p> <p>d. Defective radio frequency amplifier 38AR1AR1 (fig. 3-70).</p> | <p>a. Measure power (21 watts minimum) at P2 (38AR1A2J1). If normal, check 58AR1A2 (para 3-111).</p> <p>b. If power indication at P2 (38AR1A2J1) is abnormal, measure the power (23 watts minimum) at 38AR1A1FL1J1. If normal, check 38AR1A1FL1 (para 3-110).</p> <p>c. If abnormal indication is obtained in b above, measure the power (27 watts nominal) at 38AR1AR1J4 (FO-4-71). If normal, check 38AR1HY1 (para 3-112).</p> <p>d. If abnormal indication is obtained in c above measure the power at 38A1J2 (para 3-107). If normal, higher category of maintenance is required.</p> |
| 14. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR OUT position reads low, DRIVER position reads high. | No output cathode regulation. Defective power supply 5TR1PS1 (fig. 3-1) or voltage regulator assembly 38AR1A1A1 (fig. 3-70).  | Remove transmitter 5TR1 and measure the resistance from pin 30 of connector J8 X5TR1A1A1P3 (FO-4-9) (transmitter case) to ground (approximately 12 ohms). If normal, replace 5TR1-  |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom  | Probable Cause  | Checks and Corrective Measures  |
|--|---|---|
| 14. Continued.   |   | PS1 (para 3-50). If abnormal, check voltage regulator assembly 38AR1A1A1 (para 3-109).  |
| 15. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR CUT position reads low, DRIVER position reads low. | <p>a. Defective power supply 5TR1PS1 (fig. 3-1) or voltage assembly 38AR1A1A1 (fig. 3-70) .</p> <p>b. Defective amplifier subassembly 38AR1AR1 (fig. 3-70).</p> | <p>a. (1) Measure the power (2.5 watts minimum) at 38AR1AR1J3 (fig. 3-71). If normal check the voltage at TP2 and TP4 of 38AR1A1A1 (para 109). If normal , disconnect the transmitter rf head and measure the resistance between TP2 and TP4 of 38AR1A1A1 (should be 1.5 ohms approximately).</p> <p>(2) If voltage at TP2 and TP4 is abnormal check the output heater/output cathode circuit of 5TR1PS1 (para 3-8)</p> <p>(3) If 5TR1PS1 check is normal, check continuity of output heater/output cathode wiring between 5TR1PS1 and transmitter rf head (FO-4-43), 4-71).</p> <p>b. If the power at 38AR1AR1J3 (para 3-108) is abnormal, higher category of maintenance is required.</p> |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom        | Probable Cause   | Checks and Corrective Measures  |
|----------------|--|---|
| 15. Continued. | <p>c. No driver cathode regulation. Defective power supply 5TR1PS1 (fig. 3-1) or voltage regulator assembly 38AR1A1A1 (fig. 3-70).</p> | <p>c. Remove the radio transmitter 5TR1 from the case and measure the resistance from pin 29 to connector J8 (X5TR1A1AIP3) to ground (34 ohms approximately). If normal, replace 5TR1PS1 (para 3-50). If abnormal, check voltage regulator assembly 38AR1A1A1 (para 3-109).</p>   |
|                | <p>d. Defective driver cathode/driver heater circuit.</p>  | <p>d. Measure the power at 36A1J2 (para 3-107). If normal, check the voltage across TP1 and TP3 of voltage regulator assembly 38AR1A1A1 (para 3-109). If normal, disconnect the transmitter rf head and measure resistance between TP1 and TP3 of voltage regulator assembly 38AR1A1A1 (should be 1.5 ohm approximately). if voltage at TP1 and TP3 is abnormal, check the DRIVER HEATER/DRIVER CATHODE circuit of 5TR1PS1 (para 3-8). If 5TR1PS1 check is normal, check the continuity of the DRIVER HEATER/DRIVER CATHODE wiring between 5TR1PS1 and transmitter rf head (FO-4-43, 4-71).</p> |



b. Transmitter Troubleshooting Chart - Continued.

| Symptom  | Probable Cause   | Checks and Corrective Measures  |
|--|--|---|
| 15. Continued.   | e. Defective rf amplifier 38AR1AR1 (fig. 3-70).  | e. If driver cathode/-driver heater circuit is normal, higher category maintenance is required.   |
| 16. At channel 1280 and above or channel 1279 and below LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR OUT position reads low, DRIVER position reads low and MULT position reads low. | a. Defective amplifier frequency multiplier 38A1 (fig. 3-70).<br>b. Defective wiring.      | a. Check the output of 38A1 (para 3-107).<br>b. Check the continuity of 26V UNREG and 28V REG wiring between 5TR1-PS1 and transmitter rf head (F0-4-43, 4-71).  |
| 17. Same as 14 above but at all channels.  | a. Defective wiring.<br><br>b. Defective amplifier frequency multiplier 5TR1A4 (fig. 3-3). | a. Measure power at amplifier frequency multiplier 38A1J1 (2.5 watts minimum). If abnormal, check for continuity from 38A1J1 to pin A2 of J11 (X5TR1A4P1) (F0-4-43, 4-71).<br>b. If the wiring continuity check in a above is normal, replace 5TR1A4 (para 3-49). |
| 18. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. DRIVER position reads low, MULT position reads low, DOUBLER position reads low.  | a. Defective amplifier frequency multiplier 5TR1A4 (fig. 3-3).<br>b. Defective wiring.     | a. Measure the power at pin A1 of J11 (X5TR1A4P1) (para 3-10). If it is normal, check 5TR1A4 (para 3-11).<br>b. Check for -28 v at pin of J11 (5TR1A4P1). Check for ground at pin 17 of J11 (X5TR1A4P1) with the transmitter rf head connected.                   |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom  | Probable cause   | Checks and corrective measures  |
|--|--|---|
| <p>19. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. DRIVER position reads low, MULT position reads low, DOUBLER position reads low, (OSC position reads low).</p> | <p>a. Defective electrical-frequency synthesizer 5TR1A2 (fig. 3-3).<br/>b. Defective wiring.</p>           | <p>a. Check synthesizer 5TR1A2 (para 3-10).<br/>b. Check inputs to 5TR1A2 at J1 (X5TR1A2P2) (FO-4-43).<br/>pin 1 +28 vdc<br/>pin 3 0 v<br/>pin 2 +12 vdc<br/>pin 37 +28 vdc</p> |
| <p>20. SYNC alarm does not go out within 10 seconds after AC POWER switch is set to ON/RESET.</p>  | <p>a. Defective synthesizer 5TR1A2 (fig. 3-3).<br/>b. Defective power Supply 5TR1PS1 (fig. 3-1).</p>       | <p>a. Check synthesizer 5TR1A2 (para 3-10).<br/>b. Check power supply 5TR1PS1 (para 3-8).</p>   |
| <p>21. When AC POWER switch is set to ON/RESET, buzzer and centrifugal fan operate, LOW POWER and SYNC alarm lights come on, DRIVER metering is low, all other metering reads zero.</p>                          | <p>Defective power supply 5TR1PS1 (fig. 3-1).</p>  | <p>Check voltage regulator amplifier 5TR1PS1AR1 of power supply 5TR1PS1 (para 3-8).</p>   |
| <p>22. No communication. Metering and LOW POWER and SYNC alarms may or may not indicate normal.</p>  | <p>Synthesizer is off frequency due to -<br/>a. Defective synthesizer 5TR1A2.<br/>b. Defective wiring.</p> | <p>a. Check synthesizer (para 3-10).<br/>b. Check wiring from control-indicator 38A2 to the synthesizer (FO-4-43, 4-71).</p>  |

3-106. Receiver Troubleshooting (Band III)

a. General. The troubleshooting charts contain troubleshooting procedures for radio receiver 1RE 1 and the receiver rf head. Paragraphs 3-117 through 3-127 contain test procedures for the receiver rf head only. Refer to paragraphs 3-35 through 3-42 for test procedures for radio receiver 1RE1. For more effective troubleshooting of the receiver, remove the receiver rf head and radio receiver 1RE1 from the receiver case. Remove the receiver rf head dust cover. Connect the radio receiver 1RE1 to the receiver case using CX-12095/U and CX-12096/U extender cables. Connect the receiver to a 115 volt, 47 to 420 Hz source and proceed to troubleshoot the receiver.

b. Receiver Troubleshooting Chart.

| Symptom  | Probable Cause   | Checks and Corrective Measures  |
|--|--|---|
| 1. With AC POWER switch set to ON, there are no meter indications and no alarms. | Defective switch 1RE1A-1 CBL (fig. 3-40).  | Check for 115 vac at switch LINE and LOAD terminals (fig. 3-40). If switch is normal, make wiring continuity checks (FO-4-28).  |
| 2. Buzzer does not sound when any alarm lamp lights or goes out.                 | Defective buzzer 1RE1A-1DS5 (fig. 3-37).   | Check for 26 vdc at buzzer terminals (fig. 3-37). if voltage is present, replace buzzer (para 3-60). If voltage is not present, make wiring continuity checks (FO-4-28).  |
| 3. AC POWER switch Will not stay on.   | Short circuit.   | Make resistance checks on -12 vdc, +12 vdc and +26 vdc lines to isolate short (FO-4-28, 4-64).  |
| 4. LOW SIGNAL alarm is on RCVR SIG metering reads low.                           | <p>a. Defective power monitor 33A3 or duplexer sub-assembly 34A1A1 (fig. 3-84).</p> <p>b. Defective signal level control-monitor 34A5 (fig. 3-77).</p> | <p>a. Inject a signal at -65 dBm receive frequency into P1 (34A1A1J2) (fig. 3-77). If the alarm clears, higher category of maintenance is required.</p> <p>b. if the alarm condition remains, inject signal into P1 (34A5J2) (fig. 3-81). If the alarm clears, replace signal level control-monitor</p> |

b. Receiver Troubleshooting Chart - Continued.

| Symptom       | Probable Cause   | Checks and Corrective Measures   |
|---------------|--|--|
| 4. Continued. | <p>c. Defective low-pass filter 34FL1 (fig. 3-77) .</p> <p>d. Defective frequency mixer stage 34A7 (fig. 3-84) .</p> <p>e. Defective intermediate frequency amplifier 34AR1 (fig. 3-84).</p> <p>f. Local oscillator off frequency due to:</p> <p>(1) Defective synthesizer 1RE1A2 (fig, 3-40) .</p> <p>(2) Defective wiring.</p> | <p>34A5 (para 3-131).</p> <p>c. If the alarm condition remains, inject the signal into P1 (34FL-1J2) (fig. 3-77). If the alarm clears, replace low-pass filter 34FL1 (para 3-135).</p> <p>d. If the alarm condition remains, remove frequency mixer stage 34A7 (para 3-133) and feed a signal of 30 MHz at -35 dBm into pin A1 of 34A1W1J8 (fig. 3-83) . If alarm clears frequency mixer stage 34A7 is defective. Check frequency mixer stage 34A7 (para 3-120).</p> <p>e. If alarm remains inject a 30 MHz signal at a level of -35 dBm into 34A1W1A1P2 (fig. 3-84). If alarm clears, replace intermediate frequency amplifier 34AR1 (para 3-132).</p> <p>(1) Check synthesizer (para 3-36).</p> <p>(2) Check wiring from control indicator 33A4 to J3 (X1RE-1A2P2) (FO-4-28, 4-58)</p> |

b. Receiver Troubleshooting Chart - Continued.

| Symptom   | Probable Cause   | Checks and Corrective Measures   |
|---|--|--|
| 5. LOW SIGNAL alarm, RCVR SIG reading low; MULT reading low.                                    | Defective frequency multiplier group 34A2 (fig. 3-84). | Check the output power level at P1 (34A7J2) (para 3-116). If abnormal, replace receiver rf head.                               |
| 6. SYNC alarm and/or LOW SIGNAL alarm, RCVR SIG reading low, MULT reading low, OSC reading low. | Defective synthesizer 1RE1A2 (fig. 3-40).              | Check supply voltages at J3 (X1RE1A2P2). If normal change synthesizer 1RE1A2 (para 3-59). If abnormal, check wiring (FO-4-28). |

3-107. Control-Indicator 38A2

a. Test Equipment Required.

| Equipment                                   | Common Name        |
|---|--------------------|
| Multimeter, Digital, AN/USM-486             | Digital Multimeter |
| Cable Assembly, Special Purpose, Electrical | CX-12098/U         |
| Cable Assembly, Special Purpose Electrical  | CX-12094/U         |

b. Operational check.

- (1) Loosen the two screws securing plug P1 (38AR1A1W1J3) to chassis connector 38AR1A1W1J3 (fig. 3-68). Disconnect P1 from 38AR1A1W1J3.
- (2) Set the XMTR CHANNEL control to channel 1648.
- (4) Using the multimeter, check for correct resistance between the following pins of P1 (38AR1A1W1J3) as shown in the chart below.

| Pins     | Resistance |
|----------|------------|
| 1 and 14 | Infinity   |
| 2 and 14 | Infinity   |
| 3 and 14 | Infinity   |
| 4 and 14 | Infinity   |

| Pins      | Resistance |
|-----------|------------|
| 5 and 14  | Infinity   |
| 6 and 14  | Infinity   |
| 7 and 14  | Infinity   |
| 8 and 14  | Infinity   |
| 9 and 14  | Infinity   |
| 10 and 14 | Infinity   |
| 11 and 14 | Infinity   |
| 12 and 14 | Zero       |

(4) Set the XMTR CHANNEL control to channel 1647.

(5) Using the multi meter, check for correct resistance between the following pins of P1 (38AR1A1W1J3) as shown in the chart below.

| Pins      | Resistance |
|-----------|------------|
| 1 and 14  | Infinity   |
| 2 and 14  | Zero       |
| 3 and 14  | Zero       |
| 4 and 14  | Zero       |
| 5 and 14  | Zero       |
| 6 and 14  | Zero       |
| 7 and 14  | Zero       |
| 8 and 14  | Zero       |
| 9 and 14  | Zero       |
| 10 and 14 | Zero       |
| 11 and 14 | Zero       |
| 12 and 14 | Infinity   |

(6) Remove control indicator 38A2 from the transmitter rf head as described in chapter 6, TM 11-5820-540-12.

(7) Connect plug P1 (38AR1A1W1J3) to chassis connector 38AR1A1W1J3 using cable CMC 456-922.

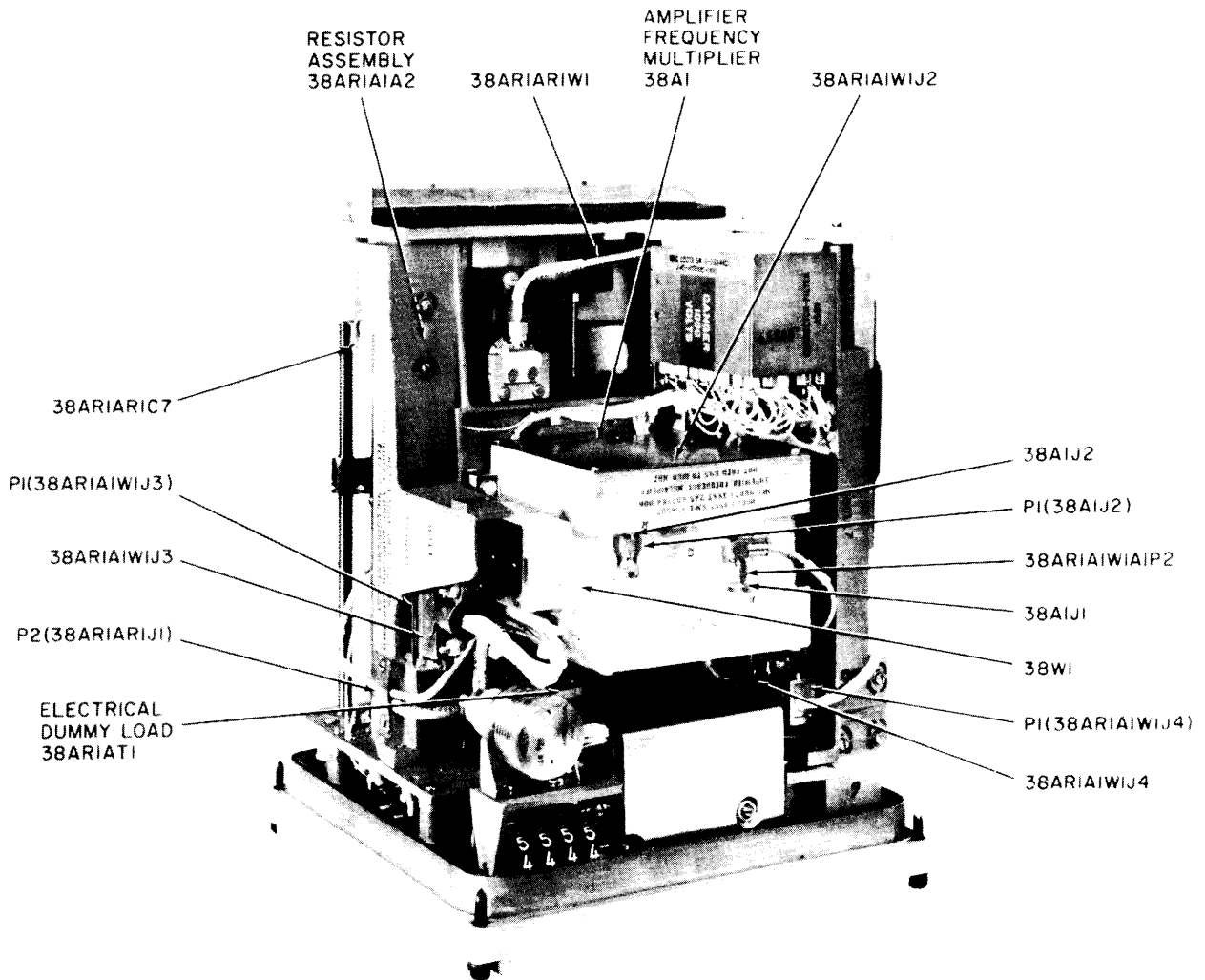
(8) Remove the four screws securing the control-indicator cover and remove the cover.

(9) Connect the transmitter rf head to the transmitter case using cable CX-12094/U and set the AC POWER switch to ON/RESET.

(10) Set the control-indicator to channel 1279.

(11) Using the multimeter check the voltage at terminal 24 (pin 13 of P1). The multimeter should indicate zero volt.

- (12) Set the control-indicator to channel 1280.
- (13) Using the multimeter, check the voltage at terminal 24. The indication should be +26 volts dc.
- (14) Set the AC POWER switch to OFF. Reinstall the control-indicator cover. If abnormal indications are obtained in either (3)9 (5), (11) or (13) above, replace control-indicator 38A2. Refer to chapter 6, TM 11-5820-540-12 for replacement procedures.



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Figure 3-68. Band III Transmitter RF Head, Top View.

3-108. Amplifier-Frequency Multiplier 38A1

a. Test Equipment Required.

| Equipment   | Common Name                  |
|---|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Attenuator, Fixed, 20 db, Empire Devices AT-75-20     | 20 db attenuator             |
| Cable Assembly, Special Purpose, Electrical           | CX-12094/U                   |
| Cable Assembly, Radio Frequency CG-3573/U (4.8 in.)   |                              |
| Adapter-Connector, Omni Spectra 21010                 | Adapter-connector OS21010    |

b. Operational Check.

- (1) Disconnect plug P1 (38A1J2) from 38A1J2 on amplifier-frequency multiplier 38A1 (fig. 3-68).
- (2) Connect test equipment as shown figure 3-69.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 1279.
- (4) Set the transmitter AC POWER switch to ON/RESET. The level at 38A1J2 should be +21 dBm minimum.
- (5) Set the XMTR CHANNEL and XMTR TUNE controls to channel 1280. The level at 38A1J2 should be +21 dBm minimum.

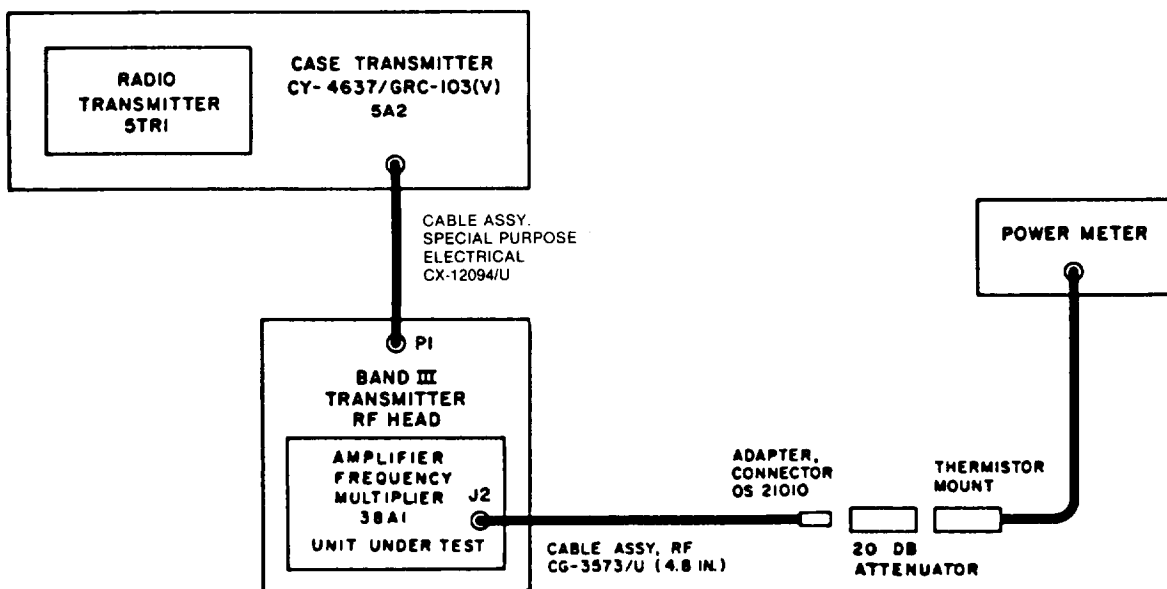


Figure 3-69. Amplifier Frequency Multiplier 38A1 Operational Check, Test Setup.



- (6) Set the AC POWER switch to OFF. Replace transmitter rf head if abnormal indications are obtained in either (4) or (5) above.

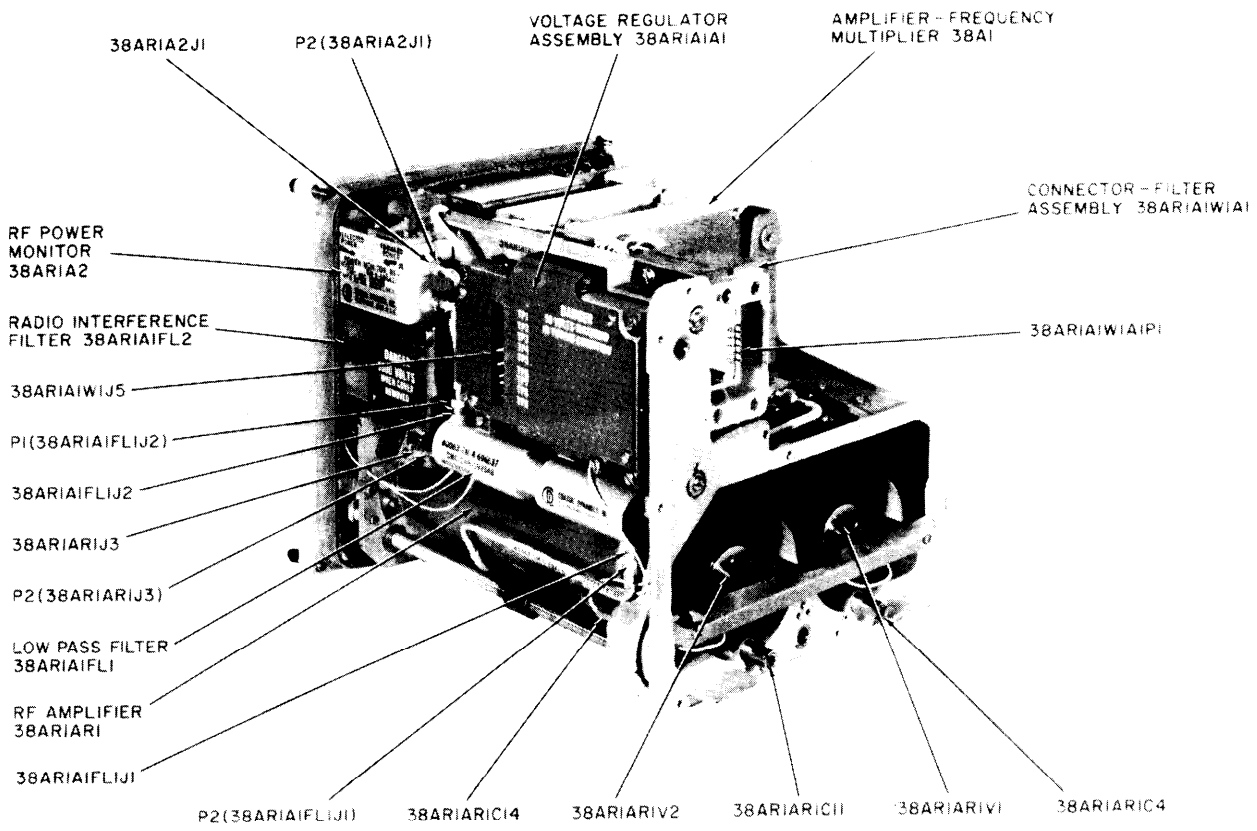
3-109. Radio Frequency Amplifier 38AR1AR1

a. Test Equipment Required.

| Equipment  | Common Name               |
|--|---------------------------|
| Wattmeter, RF, AN/URM-120                              | Wattmeter<br>CX-12094/U   |
| Cable Assembly, Special Purpose,<br>Electrical         |                           |
| Cable Assembly, RF                                     | CG-1883/U (4.5 ft.)       |
| Cable Assembly, Radio Frequency<br>CG-3573/U (4.8 in.) |                           |
| Adapter-Connector, Omni Spectra 21010<br>(2 required)  | Adapter-connector OS21010 |
| Adapter-Connector, UG-29B/U                            |                           |
| Cable Assembly, RF                                     | CG-3568/U                 |

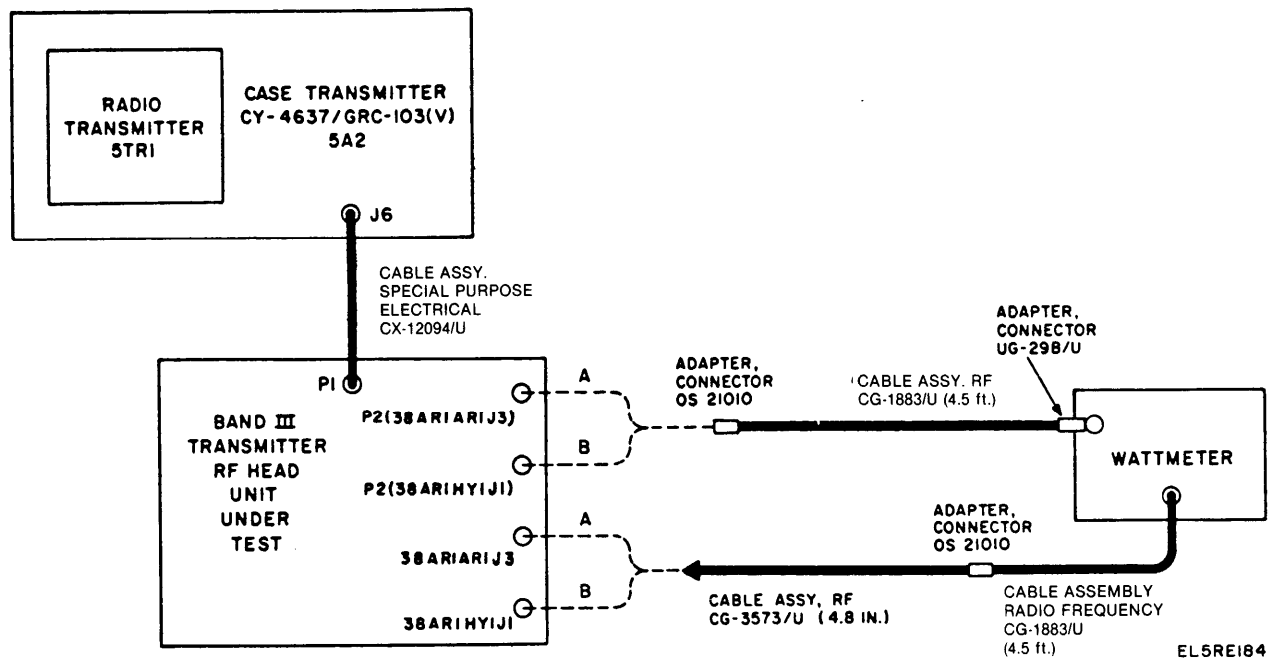
b. Operational Check.

- (1) Disconnect Plug P2 (38AR1AR1J3) from 38AR1AR1J3 on radio frequency amplifier 38AR1AR1 (fig. 3-70).
- (2) Connect test equipment as shown in A, figure 3-71.
- (3) Insert the coupler-detector CU-755/URM- 20 into the wattmeter.
- (4) Set the XMTR CHANNEL and XMTR TUNE controls to channel 1280.
- (5) Set the transmitter AC POWER switch to ON/RESET and the meter switch to DRIVER. The wattmeter should indicate 2.5 watts minimum.
- (6) Set the AC POWER switch to OFF.
- (7) Reconnect plug P2 (38AR1AR1J3) to 38AR1AR1J3.
- (8) Disconnect plug P2 (38AR1HY1J1) from 38AR1HY1J1 on circulator 38AR1HY1 (fig. 3-74).
- (9) Connect the test equipment as shown in B, figure 3-71.
- (10) Set the AC POWER switch to ON/RESET.
- (11) Set the meter switch to PWR OUT. The wattmeter should indicate 27 watts minimum.
- (12) Set the AC POWER switch to OFF.
- (13) Replace the transmitter rf head if abnormal indications are obtained in (5) and (11) above.



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Figure 3-70. Band III Transmitter RF Head, Side View.



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Figure 3-71. Radio Frequency Amplifier 38ARIAIR1 Operational Check, Test Setup.

3-110. Voltage Regulator Assembly 38AR1A1A1

a. Test Equipment Required

| Equipment   | Common Name                      |
|---|----------------------------------|
| Multimeter, Digital, AN/USM-486<br>Cable Assembly, Special Purpose,<br>Electrical | Digital Multimeter<br>CX-12094/U |

b. Operational Check.

- (1) Remove the transmitter rf head from the case. Remove the dust cover from the rf head and locate voltage regulator assembly 38AR1A1A1 (fig. 3-70).
- (2) Connect J6 on the transmitter case to 38AR1A1W1A1P1 on the transmitter rf head using cable CX-12094/U.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 1280.
- (4) Set the AC POWER switch to ON/RESET.
- (5) Set the meter switch to PWR OUT.
- (6) Using multimeter, check for correct voltage between the following test points on the voltage regulator assembly as shown in the chart below.

| Multimeter |      | Voltage          |
|------------|------|------------------|
| +          | (-)  |                  |
| TP4        | TP2  | 6.3 vdc ± 0.13 V |
| TP3        | TP1  | 6.3 vdc ± 0.13 V |
| TP4        | TP5  | 13.8 vdc ± 0.7 V |
| TP4        | TP11 | 3.2 vdc ± 1.5 V  |
| TP3        | TP10 | 3.2 vdc ± 1.5 V  |

- (7) Remove voltage regulator assembly 38AR1A1A1 (para 3-133) and check the resistance between the following pins of P1

| Pins     | Resistance (ohms ± 10%) |
|----------|-------------------------|
| 14 and 5 | 12                      |
| 8 and 5  | 34                      |
| 7 and 5  | 10 M                    |
| 2 and 6  | .270 k                  |

- (8) Set the AC POWER switch to OFF. If abnormal Indication Is obtained In (6) above, replace voltage regulator assembly 38AR1A1A1. Refer to paragraph 3-133 for replacement procedures.

3-111. Low-Pass Filter 38AR1A1FL1

a. Test Equipment Required.

| Equipment   | Common Name               |
|---|---------------------------|
| Wattmeter, RF, AN/URM-120                           | Wattmeter                 |
| Cable Assembly, Special Purpose, Electrical         | CX-12094/U                |
| Cable Assembly, Radio Frequency CG-3573/U (4.8 in.) |                           |
| Cable Assembly, RF (2 required)                     | CG-1883/U (4.5 ft.)       |
| Cable Assembly, RF                                  | CG-3568/U                 |
| Adapter-Connector, Omni Spectra 21020 (2 required)  | Adapter-connector OS21020 |
| Adapter-Connector, UG-29B/U (3 required)            |                           |

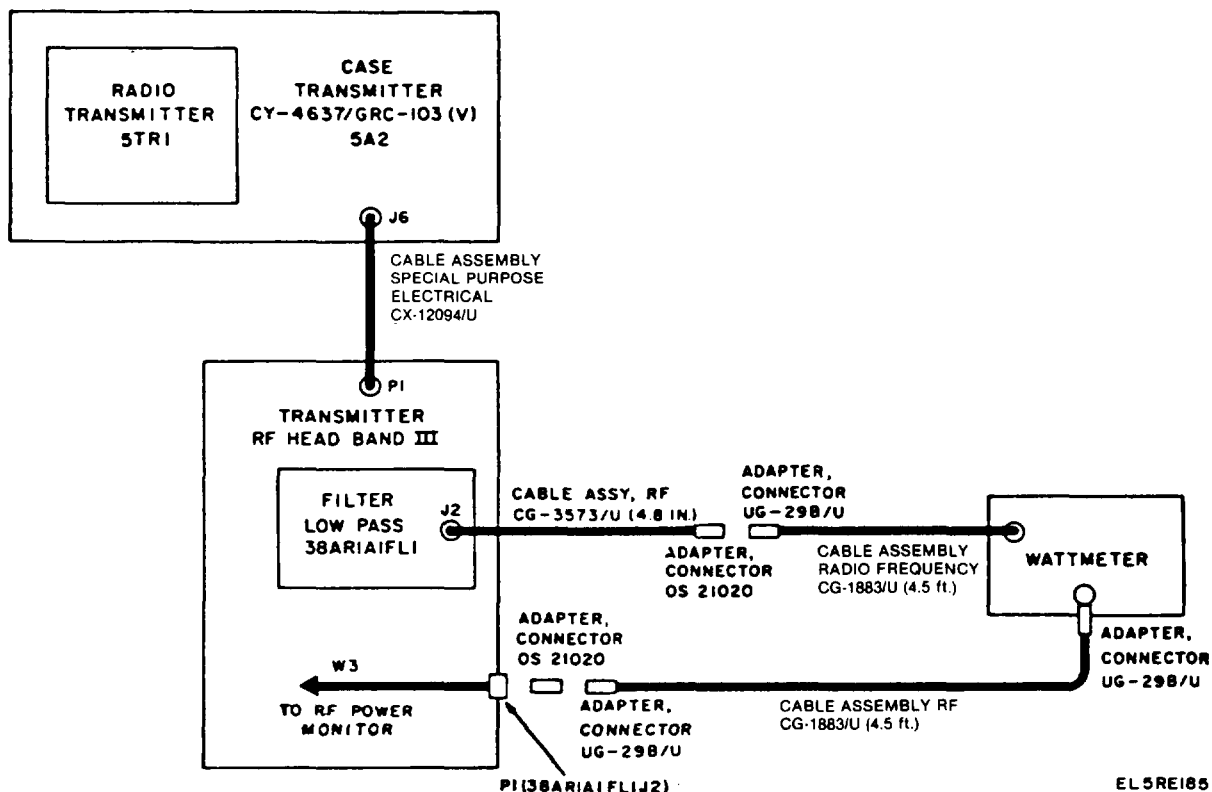


Figure 3-72. Low Pass Filter 38AR1A1FL1 Operational Check, Test Setup.

b. Operational Checks.

- (1) Disconnect plug P1 (38AR1A1FL1J2) from 38AR1A1FL1J2 on low-pass filter 38AR1A1FL1 (fig. 3-70).
- (2) Connect test equipment as shown in figure 3-72.
- (3) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (4) Set the XMTR CHANNEL and XMTR TUNE controls to channel 1280.
- (5) Set the transmitter AC POWER switch to ON/RESET.
- (6) Set the meter switch to PWR OUT. The wattmeter should indicate 21 watts minimum.
- (7) Set the AC POWER switch to OFF. Replace low pass filter 38AR1A1FL1 if an abnormal indication is obtained in (6) above. Refer to paragraph 3-131 for replacement procedure.

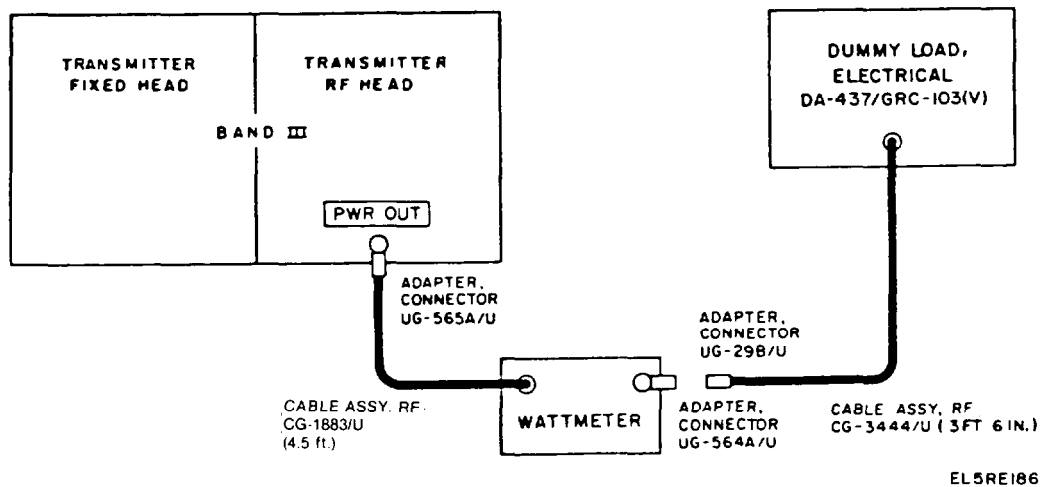
3-112. RF Power Monitor 38AR1A2

a. Test Equipment Required.

| Equipment   | Common Name                      |
|---|----------------------------------|
| Wattmeter, RF, AN/URM-120<br>Cable Assembly, Radio Frequency<br>Adapter-Connector UG-565A/U<br>Adapter-Connector UG-29B/U<br>Adapter-Connector, UG-564A/U<br>Dummy Load, Electrical DA-437/GRC-103(V)<br>Cable Assembly, Radio Frequency<br>CG-3444/U (3 ft. 6 in.) | Wattmeter<br>CG-1883/U (4.5 ft.) |

a. Operational Check.

- (1) Connect the test equipment as shown in figure 3-73.
- (2) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 1280.
- (4) Set the transmitter AC POWER switch to ON/RESET.
- (5) Set the transmitter meter switch to PWR OUT. The wattmeter should indicate 20 watts minimum.
- (6) Set the AC POWER switch to OFF. If an abnormal indication is obtained, replace power monitor 38AR1A2 as described in paragraph 3-128.



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Figure 3-73. RF Power Monitor 38AR1A2 Operational Check, Test Setup.

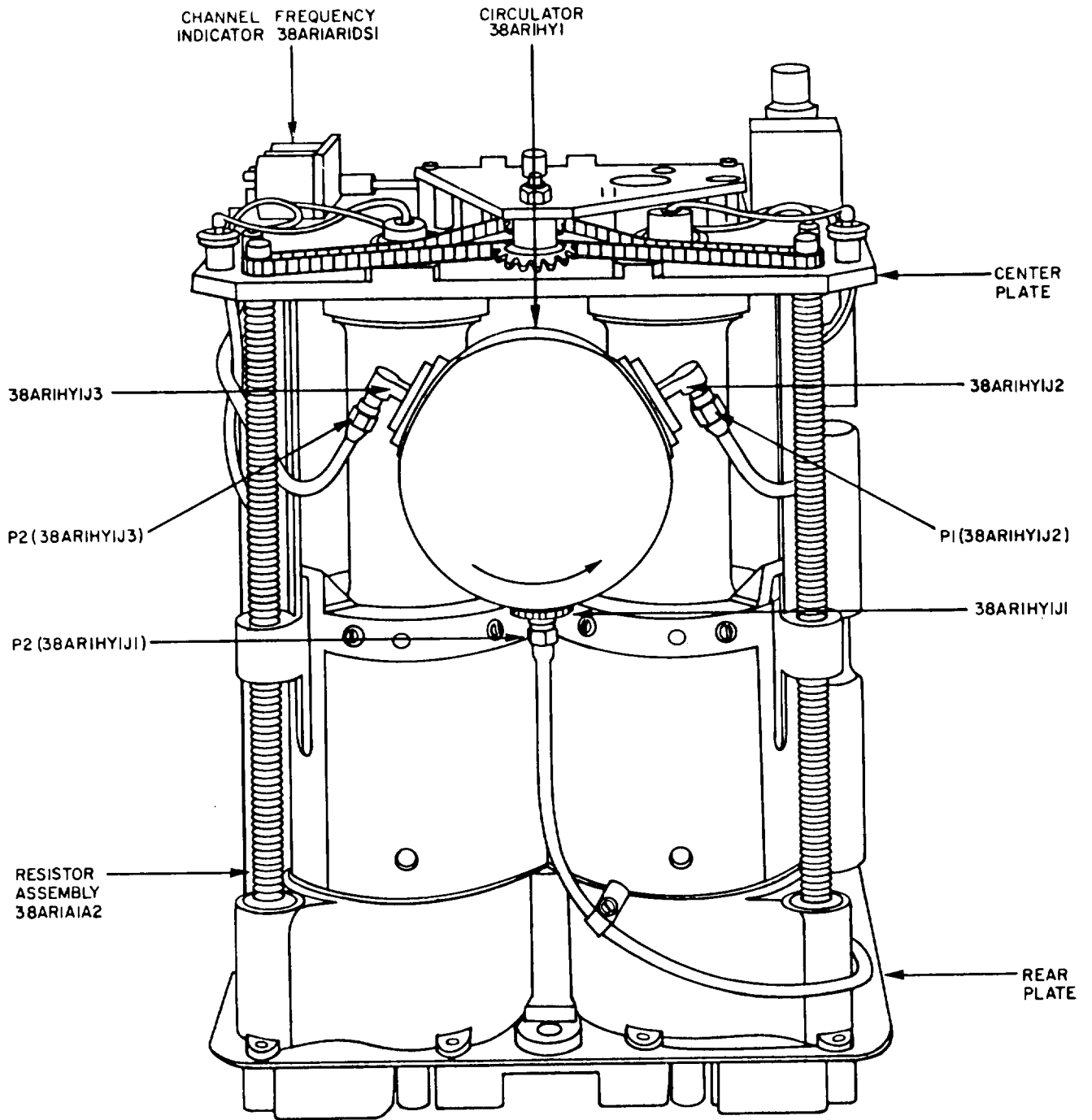
3-113. Circulator 38AR1HY1 and Electrical Dummy Load 38AR1AT1

a. Test Equipment Required.

| Equipment   | Common Name               |
|---|---------------------------|
| Wattmeter, RF, AN/URM-120                           | Wattmeter                 |
| Cable Assembly, Special Purpose, Electrical         | CX-12094/U                |
| Cable Assembly, Radio Frequency CG-3573/U (4.8 in.) |                           |
| Cable Assembly, RF (2 required)                     | CG-1883/U (4.5 ft.)       |
| Adapter-Connector, Omni Spectra 21010 (2 required)  | Adapter-connector OS21010 |
| Adapter-Connector, UG-29B/U (3 required)            |                           |
| Cable Assembly, RF                                  | CG-3568/U                 |

b. Operational Check.

- (1) Disconnect plug P1 (38AR1HYIJ2) from 38AR1HY1J2 on circulator 38AR1HY1 (fig. 3-74).
- (2) Connect test equipment as shown in figure 3-75.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 1280.
- (4) Set the transmitter AC POWER switch to ON/RESET.
- (5) Set the meter switch to PWR OUT. The wattmeter should indicate 23 watts minimum.
- (6) Set the AC POWER switch to OFF. If an abnormal indication is obtained in (5) above, replace the transmitter rf head.



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Figure 3-74. Band III Transmitter RF Head, Bottom View.

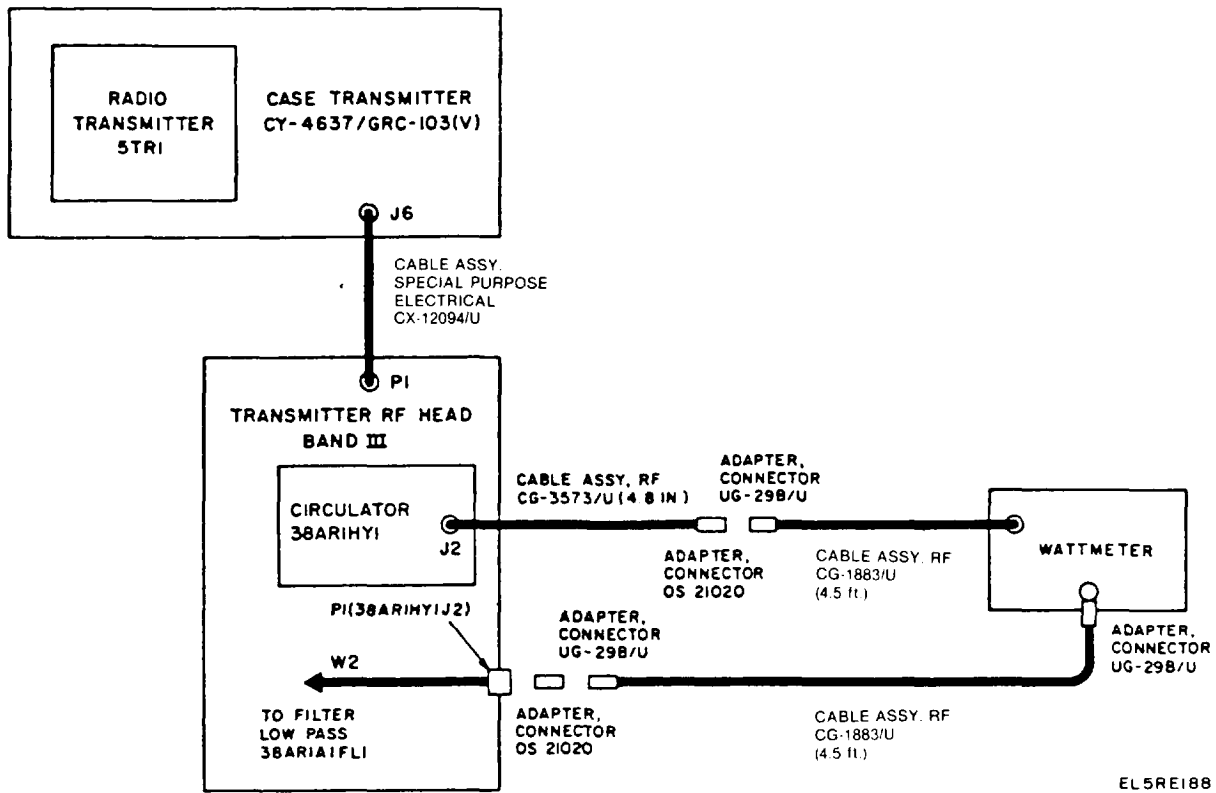


Figure 3-75. Circulator 36AR1HY1 and Electrical Dummy Load 38AR1AT1 Operational Check, Test Setup.

3-114. Duplexer Subassembly 34A1A1 and RF Power Monitor 34A3

a. Duplexer Equipment Required.

| Equipment                                   | Common Name               |
|---|---------------------------|
| Wattmeter, RF, AN/URM-120                   | Wattmeter                 |
| Generator, Signal SG-340A/U                 | Signal generator No. 2    |
| Voltmeter, Electronic, ME-30A/U             | VTVM                      |
| Load, 51 ohms                               | CMC 355-053               |
| Adapter-Connector, UG-565A/U                |                           |
| Adapter-Connector, UG-29B/U                 |                           |
| Adapter-Connector, UG-564A/U                |                           |
| Adapter-Connector, UG-274/U                 |                           |
| Dummy Load, Electrical DA-437/GRC-103(V)    |                           |
| Adapter-Connector, Omni Spectra 21010       | Adapter-connector OS21010 |
| Cable Assembly, Radio Frequency             | CG-1883/U (4.5 ft.)       |
| Cable Assembly, Radio Frequency             | CMC-930                   |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U                |



a. Test Equipment Required - Continued.

| Equipment  | Common name |
|--|-------------|
| Cable Assembly, Radio Frequency<br>CG-3444/U (1 ft. 6 in.) |             |
| Cable Assembly, Radio Frequency<br>CG-3444/U (3 ft. 6 in.) |             |

b. Operational Check - Receive Path.

- (1) Connect the test equipment as shown in figure 3-76.
- (2) Insert the coupler-detector CU-755/URM-120 into the wattmeter.
- (3) Set the XTMR CHANNEL and XMTR TUNE controls to channel 1280.
- (4) Set the transmitter AC POWER switch to ON/RESET. The wattmeter should indicate 13 watts minimum.
- (5) Set the AC POWER switch to OFF. If an abnormal reading is obtained in (4) above, higher category of maintenance is required.

c. operational Check - Receive Path.

- (1) Disconnect plug P1 (34A1A1J2) (fig. 3-77) from 34A1A1J2 on duplexer 34A1A1 .
- (2) Connect the test equipment as shown in A, figure 3-78.
- (3) Tune the receiver to channel 1390.

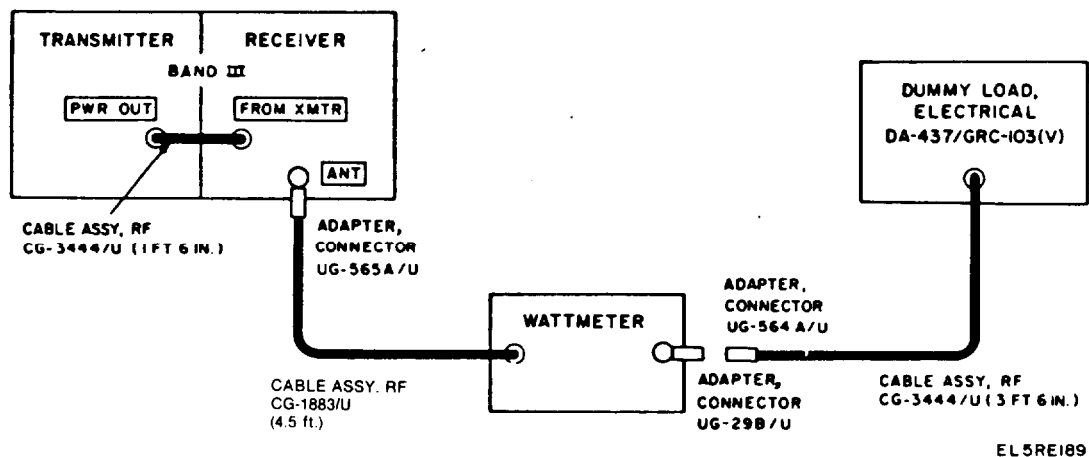


Figure 3-76. Duplexer Subassembly 34A1A1, (Transmit) Operational Check, Test Setup

- (4) Set the frequency of signal generator No. 2 to 895 MHz and adjust the output level until a reading of -50 dbm is obtained on the VTVM. Note the attenuator setting on signal generator No. 2.
- (5) Reconnect plug P1 (34A1A1J2) to 34A1A1J2.
- (6) Connect the test equipment as shown in 5, figure 3-78.
- (7) Increase the output of signal generator No. 2 until a reading of -50 dbm is obtained on the VTVM. The output attenuator setting on signal generator No. 2 should not be more than 3 db lower than the setting noted in (4) above.
- (8) If the attenuator in (7) above is not obtained, replace the receiver rf head.

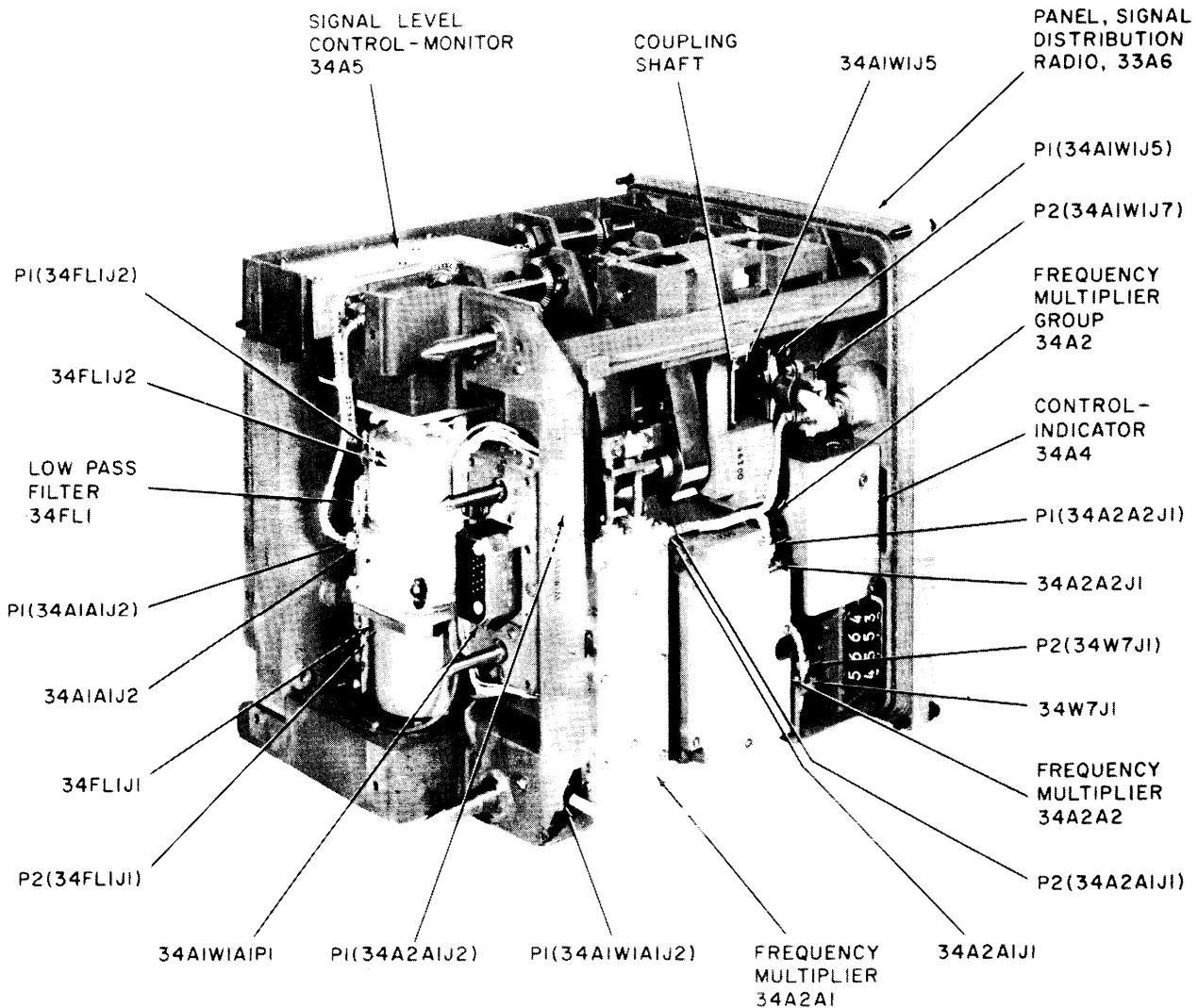


Figure 3-77. Band III Receiver RF Head, Top and Rear View.

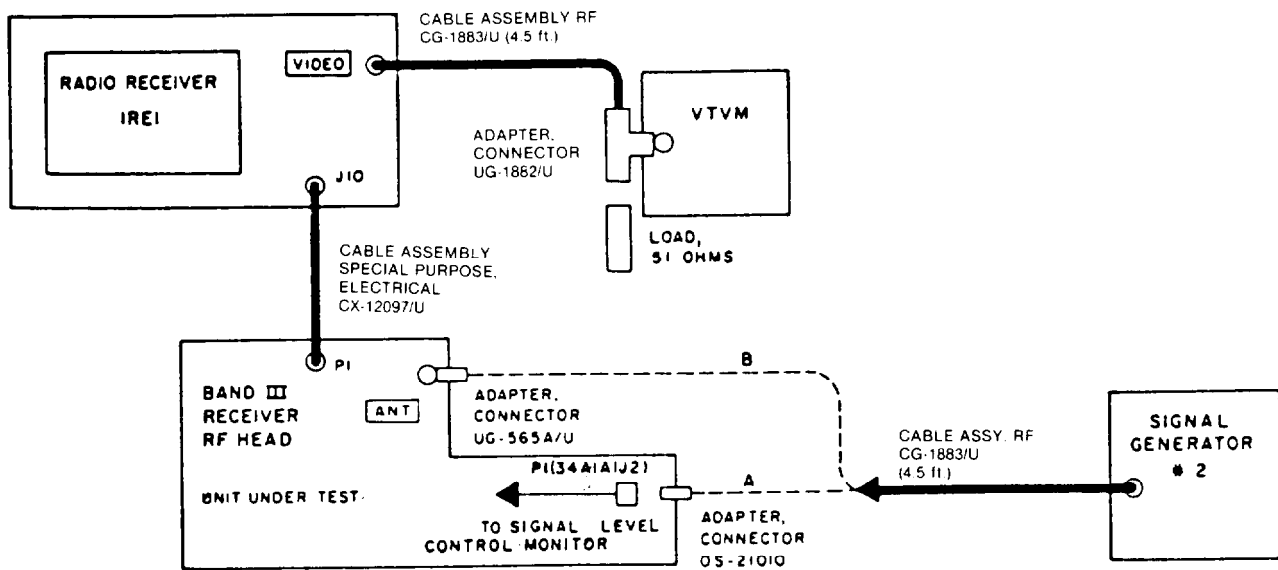


Figure 3-78. Duplexer Subassembly 34A1A1, (Receive) Operational Check, Test Setup.

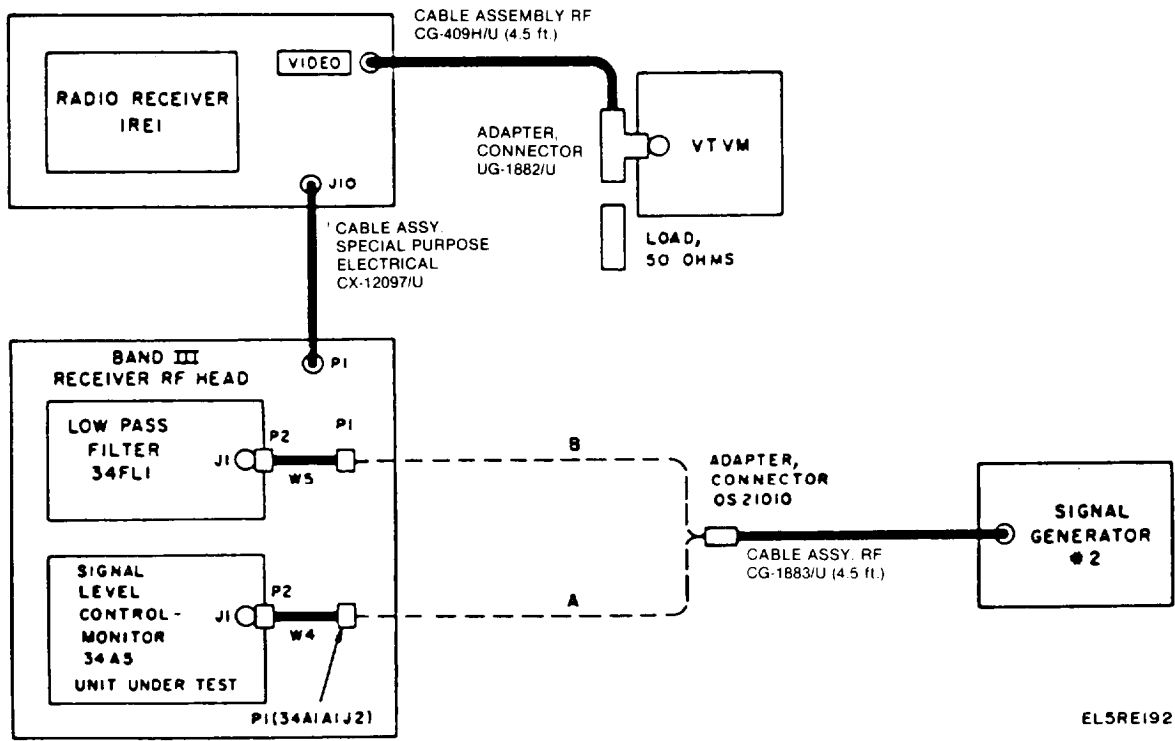
3-115. Signal Level Control-Monitor 34A5

a. Test Equipment Required.

| Equipment                                   | Common Name               |
|---|---------------------------|
| Voltmeter, Electronic, ME-30A/U             | VTVM                      |
| Generator, Signal SG-340A/G                 | Signal generator No. 2    |
| Load, 51 ohms                               | CMC 335-053               |
| Adapter-Connector, Omni Spectra 21010       | Adapter-connector OS21010 |
| Adapter-Connector, UG-274/U                 |                           |
| Cable Assembly, RF                          | CG-409H/u (4.5 ft.)       |
| Cable Assembly, RF                          | CG-1883/U (4.5 ft.)       |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U                |

b. Operational Checks.

- (1) Disconnect plug P1 (34A1A1J2) (fig. 3-77) from 34A1A1J2 on duplexer 34A1A1 .
- (2) Connect the test equipment as shown in A, figure 3-79.
- (3) Tune the receiver to channel 1390 and the signal generator to 895 MHz.
- (4) Set the AC POWER switch to ON.



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Figure 3-79. Signal Level Control Monitor 34A5 Operational Check, Test Setup.

- (5) increase the output level of signal generator No. 2 until the high signal alarm operates (buzzer may sound if not muted). The signal Generator No. 2 level will be 0 dBm  $\pm$ 10 dBm.
- (6) Decrease the level of signal generator No. 2 until the VTVM indicates -50 dBm.
- (7) Connect the test equipment as shown in B, figure 3-79.
- (8) The indication on VTVM should not be higher than -49.25 dBm.
- (9) Set the AC POWER switch to OFF.
- (10) If the high, signal alarm does not come on in (5) above, and/or the indication obtained in (8) above is beyond the specified limit, the unit under test should be replaced. Refer to paragraph 3-136 for replacement procedures.

3-116. Low Pass Filter 34FL1

a. Test Equipment Required

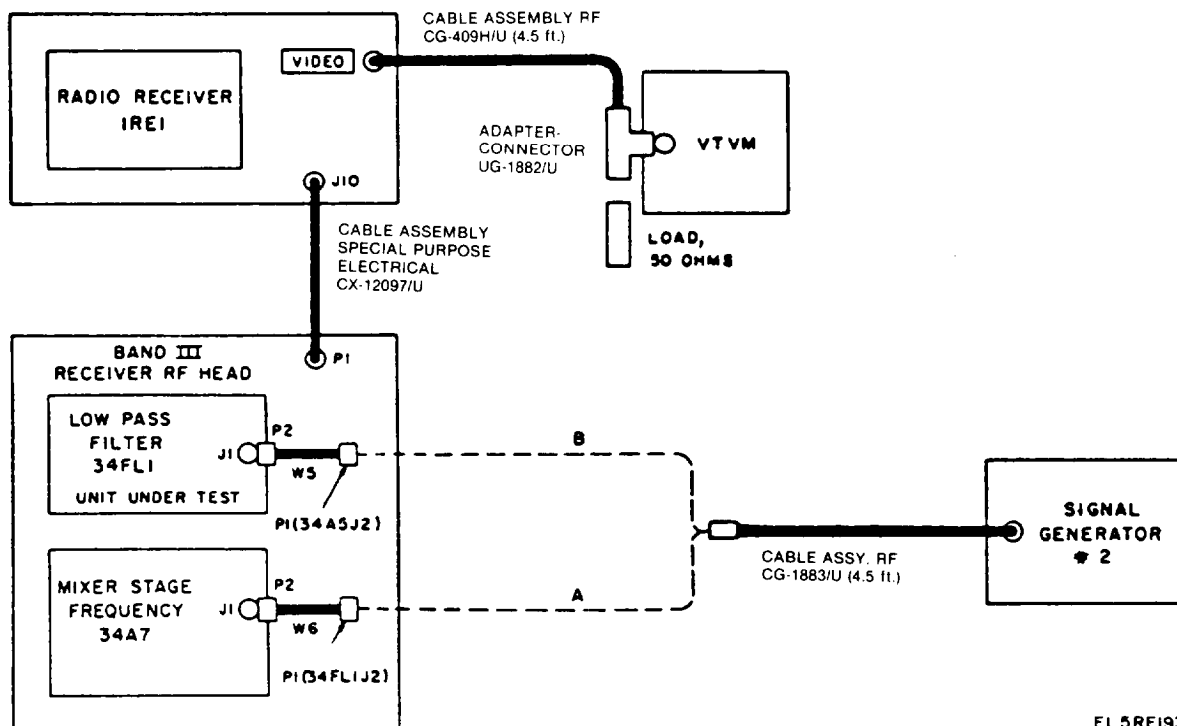
| Equipment                       | Common Name            |
|---------------------------------|------------------------|
| Voltmeter, Electronic, ME-30A/U | VTVM                   |
| Generator, Signal SG-340A/G     | Signal generator No. 2 |

a. Test Equipment Required - Continued

| Equipment                                   | Common Name               |
|---|---------------------------|
| Load, 51 ohms                               | CMC 335-053               |
| Adapter-Connector, Omni Spectra 21010       | Adapter-connector OS21010 |
| Adapter-Connector, UG-274/U                 |                           |
| Cable Assembly, RF                          | CG-1883/U (4.5 ft.)       |
| Cable Assembly, RF                          | CG-409H/u (4.5 ft.)       |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U                |

b. Operational Checks.

- (1) Disconnect plug P1 (34FL1J2) from 34FL1J2 on filter low pass 34FL1 (fig. 3-77).
- (2) Connect the test equipment as shown in A, figure 3-80.
- (3) Tune the receiver to channel 1390 and the signal generator No. 2 to 895 MHz.
- (4) Set the AC POWER switch to ON.
- (5) Adjust the output level of signal generator No. 2 until a reading of -50 dBm is obtained on the VTVM.



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Figure 3-80. Low Pass Filter 34FL1 Operational Check, Test Setup.

- (6) Reconnect plug P1 (34FL1J2) to 34FL1J2.
- (7) Disconnect plug P1 (34A5J2) (fig. 3-81) from 34A5J2 on signal level control monitor 34A5.
- (8) Connect the test equipment as shown in B, figure 3-80.
- (9) The indication on the VTVM should not be greater than -49.5 dBm.
- (10) If an abnormal indication is obtained in (9) above, replace 34FL1. Refer to paragraph 3-140 for replacement procedures.

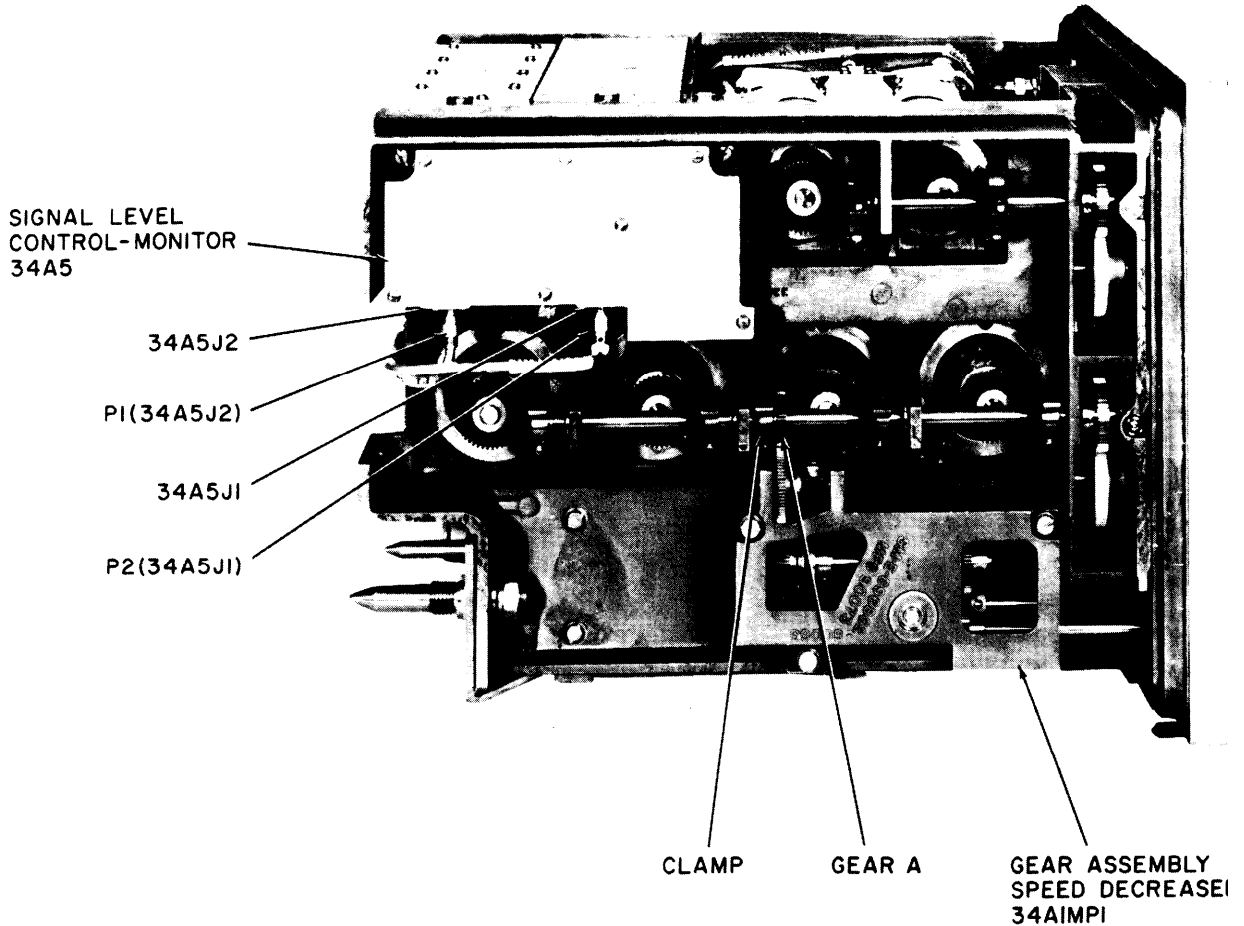
3-117. Frequency Multiplier 34A2A2

a. Test Equipment Required

| Equipment  | Common Name                  |
|--|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount HP-478A | Power Meter Thermistor Mount |
| Attenuator Fixed, Empire Devices AT-75-10            | 10 db attenuator             |
| Adapter-Connector, Omni Spectra OS21010              | Adapter-connector OS21010    |
| Adapter-Connector, UG-29B/U                          |                              |
| Cable Assembly, RF                                   | CG-1883/U (4.5 ft.)          |
| Cable Assembly, Special Purpose, Electrical          | CX-12097/U                   |

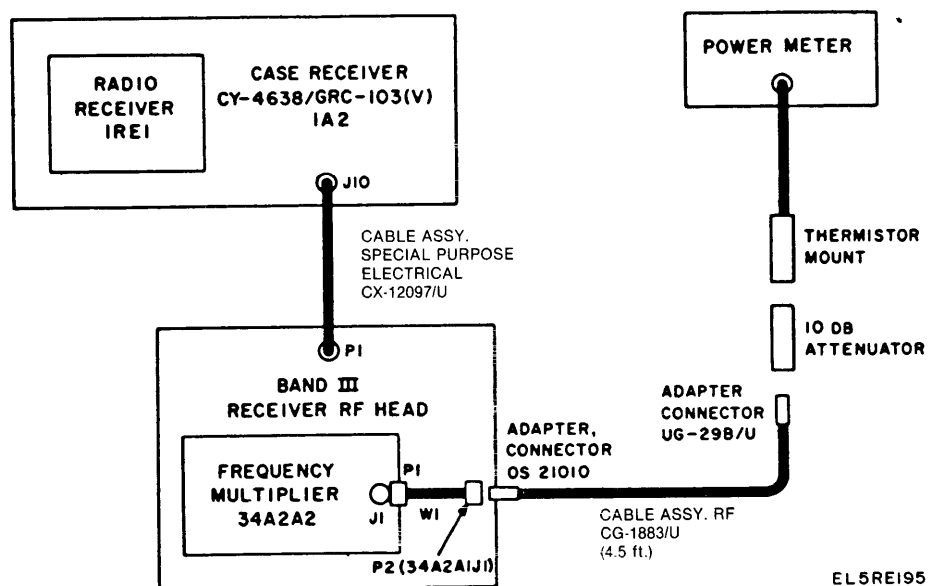
b. Operational Checks.

- (1) Disconnect plug P2 (34A2A1J1) from 34A2A1J1 on frequency multiplier 34A2A1 (fig. 3-77).
- (2) Connect the test equipment as shown in figure 3-82.
- (3) Set the AC POWER switch to ON and tune the receiver to channel 1219. The output power level at P2 (34A2A1J1) should be a minimum of +14.5 dBm (power meter indication of +4.5 dBm).
- (4) Set the RCVR CHANNEL control to channel 1220. The power meter indication should be within limits specified in (3) above.
- (5) Set the AC POWER switch to OFF. If the indication in (3) and (4) above are not within the specified limits, replace receiver rf head.



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Figure 3-81. Band III RF Head, Right Side View.



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Figure 3-82. Frequency Multiplier 34A2A2 Operational Check, Test Setup.

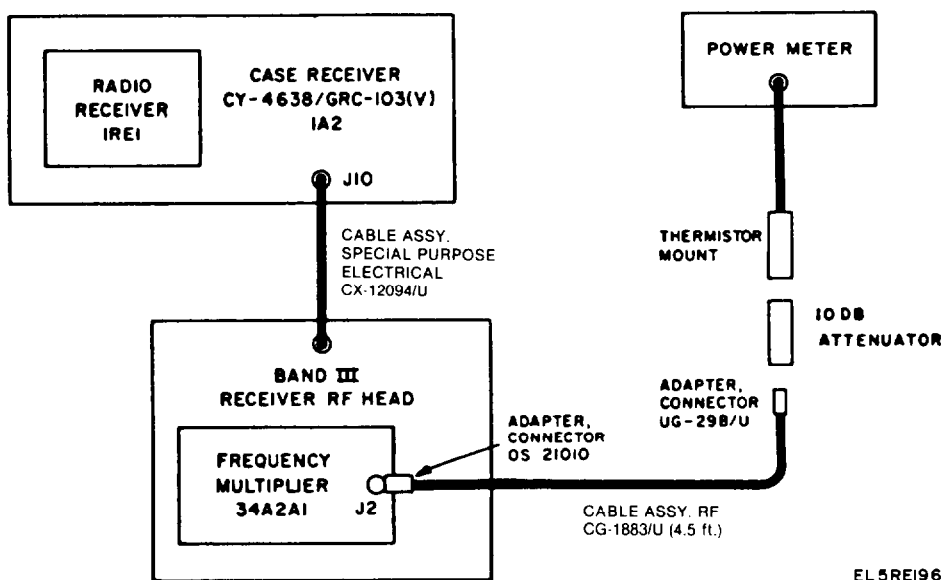
3-118. Frequency Multiplier 34A2A1

a. Equipment Required.

| Equipment  | Common Name                  |
|--|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount HP-478A | Power Meter Thermistor Mount |
| Attenuator Fixed, Empire Devices AT-75-10            | 10 db attenuator             |
| Adapter-Connector, Omni Spectra OS21010              | Adapter-connector OS21010    |
| Adapter-Connector, UG-29B/U                          |                              |
| Cable Assembly, RF                                   | CG-1883/U (4.5 ft.)          |
| Cable Assembly, Special Purpose, Electrical          | CX-12097/U                   |

b. Operational Checks.

- (1) Disconnect plug P1 (34A2A1J2) (fig. 3-77) from 34A2A1J2 of frequency multiplier 34A2A1.
- (2) Connect the test equipment as shown in figure 3-83.
- (3) Set the AC POWER switch to ON and tune the receiver to channel 1219. The output power level at P2 (34A2A1J1) should be a minimum of +7 dBm (power meter Indication of -3 dBm).
- (4) Set the RCVR CHANNEL control to channel 1220. The power level should be a minimum of +8 dBm (power meter indication of -2 dBm).
- (5) Set the AC POWER switch to OFF. If the indications in (3) and (4) above are not within the specified limits, replace the receiver rf head.



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Figure 3-83. Frequency Multiplier 34A2A1 Operational Check, Test Setup.



## 3-119. Bandpass Filter 34A2FL1

a. Test Equipment Required.

| Equipment  | Common Name                  |
|--|------------------------------|
| Meter, Power, ME-441/U with Thermistor Mount HP-478A | Power Meter Thermistor Mount |
| Attenuator Fixed, Empire Devices AT-75-10            | 10 db attenuator             |
| Adapter-Connector, Omni Spectra 21010                | Adapter-connector OS21010    |
| Adapter-Connector, UG-29B/U                          |                              |
| Cable Assembly, RF                                   | CG-1883/U (4.5 ft.)          |
| Cable Assembly, Special Purpose, Electrical          | CX-12097/U                   |

b. Operational Checks.

- (1) Disconnect plug P1 (34A7J2) from 34A7J2 of frequency mixer stage 34A7 (fig. 3-84).
- (2) Connect the test equipment as shown in figure 3-85.
- (3) Set the AC POWER switch to ON and tune the receiver to channel 1219. The output power level at P1 (34A7J2) should be a minimum of +5 dBm (power meter indication of -5 dBm).
- (4) Set the RCVR CHANNEL control to channel 1220. The power level should be a minimum of +6 dBm (power meter indication of -4 dBm).
- (5) Set the AC POWER switch to OFF. If the indications in (3) and (4) above are not within the specified limits, replace the receiver rf head.

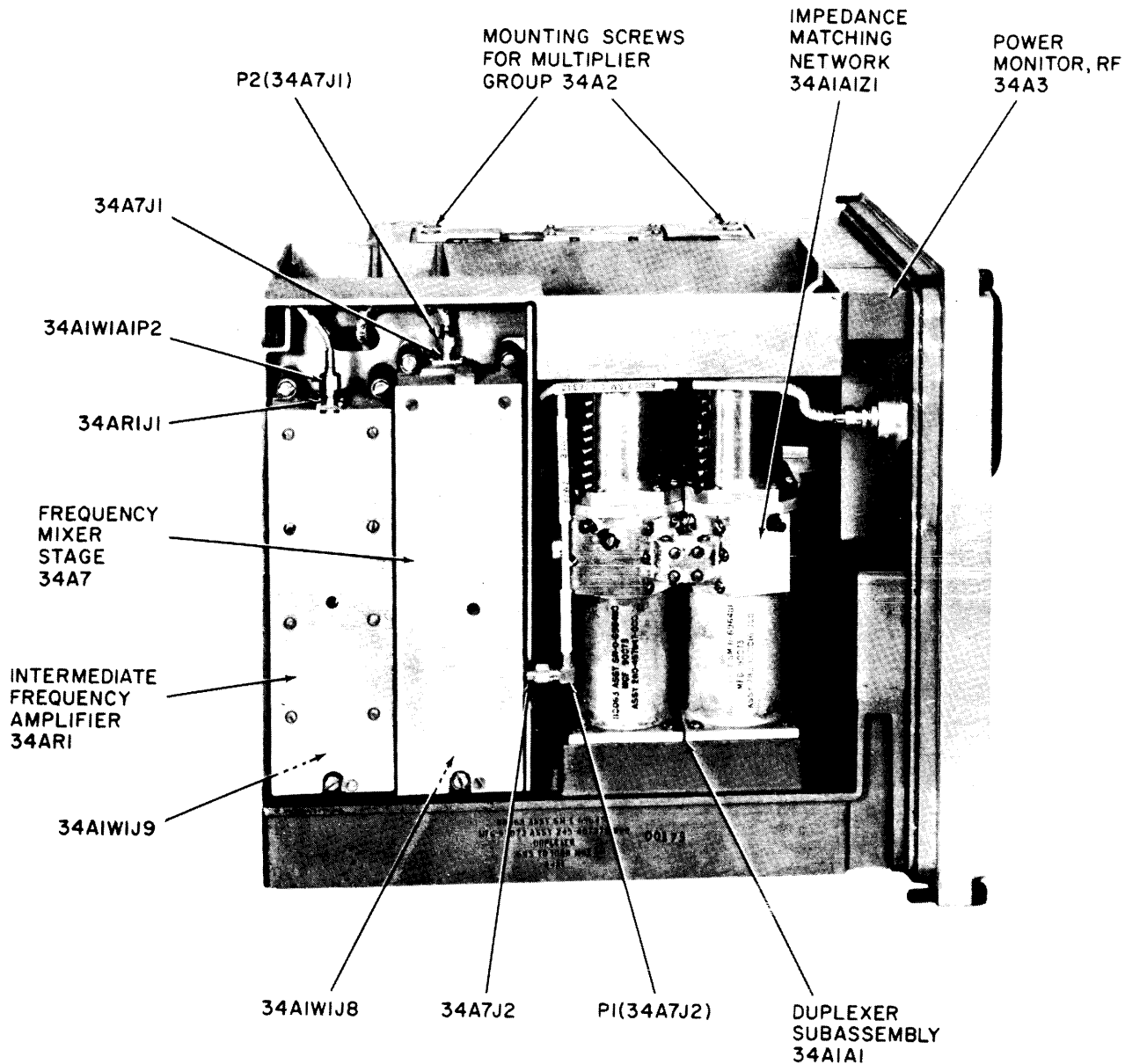
## 3-120. Intermediate Frequency Amplifier 34AR1

a. Test Equipment Required.

| Equipment   | Common Name                  |
|---|------------------------------|
| Generator, Signal, SG-1170/U                          | Signal Generator             |
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Cable Assembly, RF CG-3573/U (4.8 in.)                |                              |
| Cable Assembly, RF                                    | CG-3581/U (6 in.)            |
| Cable Assembly, RF                                    | CG-409H/u (4.5 ft.)          |
| Cable Assembly, Special Purpose, Electrical           | CX-12097/U                   |
| Adapter-Connector                                     | OS-21010                     |
| Adapter-Connector                                     | OS-20200-2                   |
| Voltmeter, RF, ME-426                                 | RF, Voltmeter                |

b. Operational Check .

- (1) Remove frequency mixer stage 34A7 as explained in paragraph 3-138 (Connector 34A1W1J8 (fig. 3-84) is now exposed.) e
- (2) Disconnect plug 34A1W1A1P2 from 34AR1J1 on intermediate frequency amplifier 34AR1 (fig. 3-84).
- (3) Connect the test equipment as shown in figure 3-86.
- (4) Set the frequency of signal generator No. 1 to 30 MHz at an output level of -75 dBm.



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Figure 3-84. Band III Receiver RF Head, Bottom View.

- (5) Set the receiver AC POWER switch to ON. The RF voltmeter should indicate between -28 dBm and -22 dBm.
- (6) Set the receiver AC POWER switch to OFF. If the indications obtained in (5) above is outside the specified limits, replace the intermediate frequency amplifier 34AR1. Refer to paragraph 3-133 for replacement procedures.

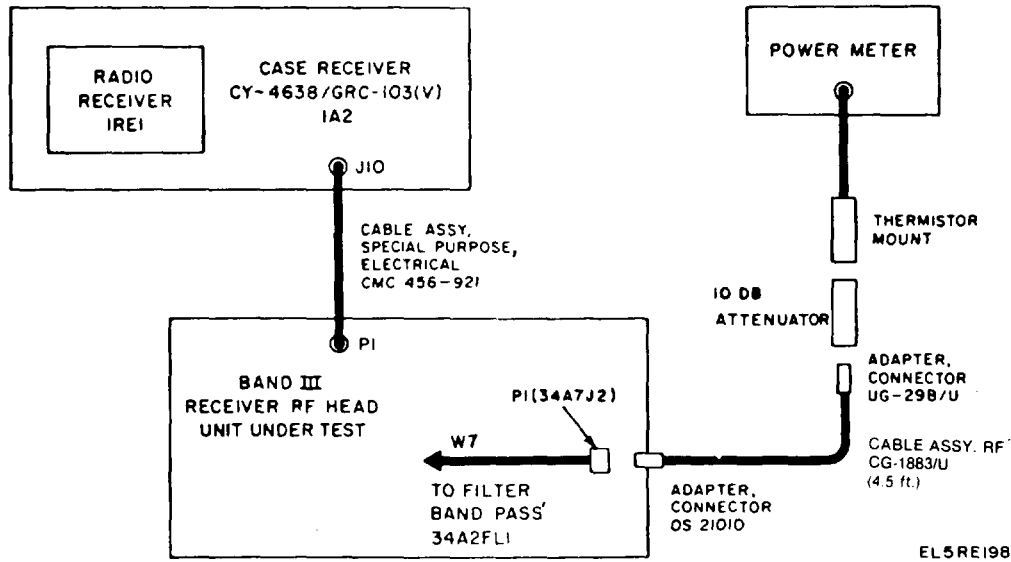


Figure 3-85. Bandpass Filter 34A2FL1 Operational Check, Test Setup.

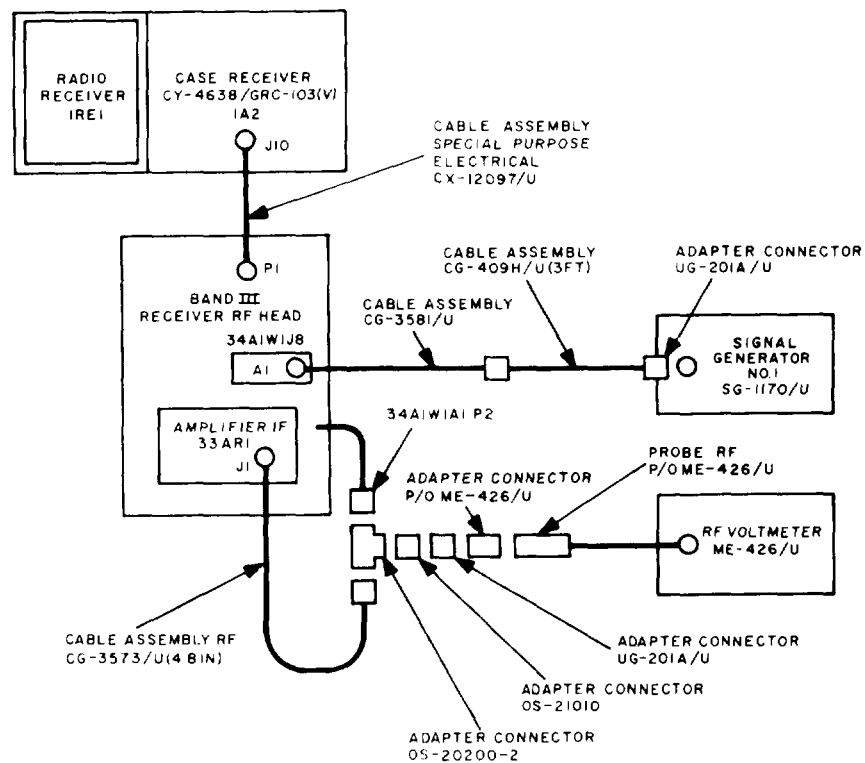


Figure 3-86. Intermediate Frequency Amplifier 34AR1 Operational Check, Test Setup.

3-121. Frequency Mixer Stage 34A7

a. Test Equipment Required.

| Equipment   | Common Name                  |
|---|------------------------------|
| Generator, Signal, SG-340A/U                          | Signal Generator             |
| Meter, Power, ME-441/U with Thermistor Mount, HP-478A | Power Meter Thermistor Mount |
| Cable Assembly, RF CG-3573/U (4.8 in.) (2 required)   |                              |
| Cable Assembly, RF                                    | CG-1883/U                    |
| Cable Assembly, Special Purpose, Electrical           | CX-12097/U                   |
| Adapter-Connector, Omni Spectra 21010                 | Adapter-connector OS21010    |
| Adapter-Connector                                     | OS-20200-2                   |
| Adapter-Connector                                     | UG-201A/U                    |
| Voltmeter, RF   | ME-426/U                     |

b. Operational Check.

- (1) Disconnect plug P2 (34A7J1) from 34A7J1 on frequency mixer stage 34A7 (fig. 3-84).
- (2) Disconnect plug 34A1W1A1P2 from 34AR1J1 on intermediate frequency amplifier 34AR1.
- (3) Connect the test equipment as shown in figure 3-87.
- (4) Tune the receiver to channel 1390.
- (5) Set the frequency of signal generator No. 2 to 895 MHz at an output level of -89 dBm.
- (6) Set the receiver AC POWER switch to ON. The RF voltmeter should indicate between -28 dBm and -22 dBm.
- (7) If the indication obtained in (6) above is outside specified limits, replace frequency mixer stage 34A7 as described in paragraph 3-134.

3-122. Power Supply 34PS1

a. Test Equipment Required

| Equipment                                   | Common Name        |
|---|--------------------|
| Multimeter, Digital, AN/USM-486             | Digital Multimeter |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U         |

b. Operational Check.

- (1) Remove the receiver rf head from receiver case and connect it to the receiver case using cable CX-12097/U.
- (2) Remove frequency mixer stage 34A7 as described in paragraph 3-134.
- (3) Connect a Jumper wire between pin 7 and pin 8 and another Jumper wire between pin 5 and pin 9 of chassis 34A1W1J8 (fig. 3-84).
- (4) Set receiver AC POWER switch to ON.
- (5) Multimeter connected between pin 7 (+) and pin 5 (-) should measure 70 volts dc  $\pm 0.5$  volts dc.
- (6) If the indication in (5) above is not obtained, replace power supply 34PS1. Refer to paragraph 3-135 for replacement procedures.

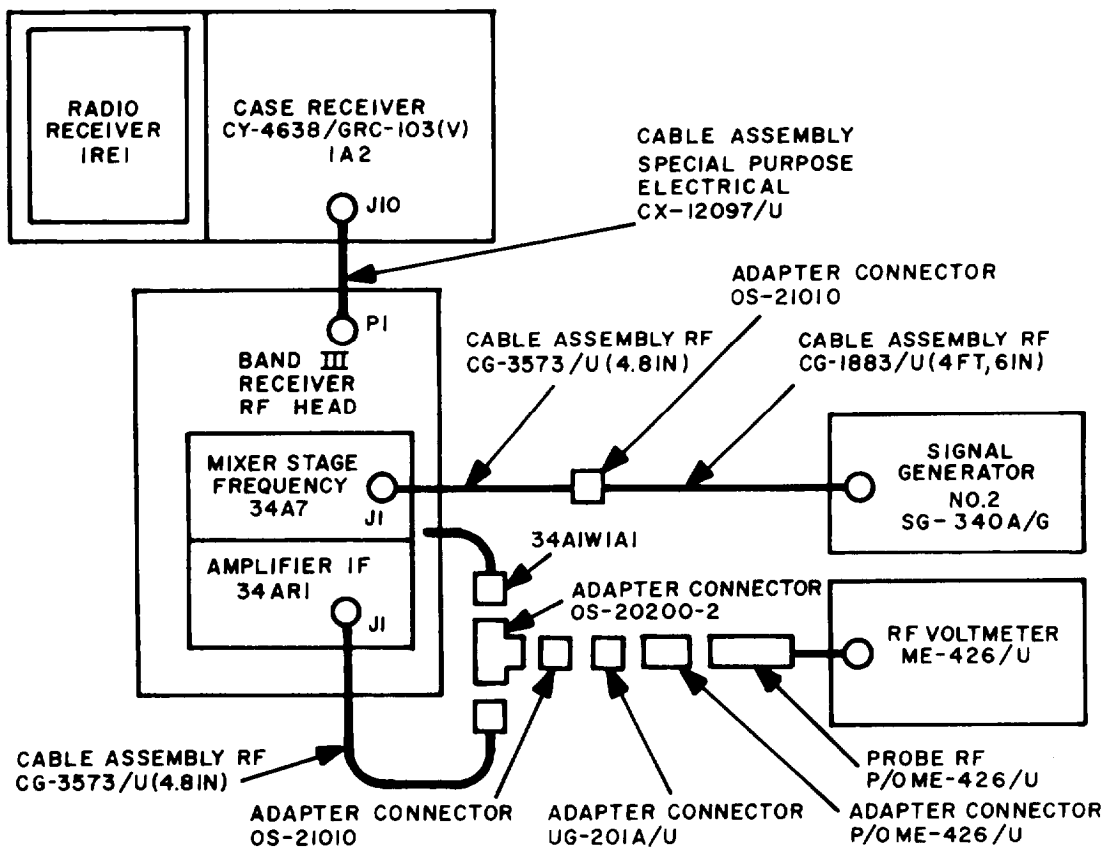


Figure 3-87. Frequency Mixer Stage 34A7 Operational Check, Test Setup.

3-123. Voltage Control Assembly 34A1A2

a. Test Equipment Required.

| Equipment                       | Common Name        |
|---------------------------------|--------------------|
| Multimeter, Digital, AN/USM-486 | Digital Multimeter |

b. Operational Check

- (1) Remove the receiver rf head from the receiver case.
- (2) Locate voltage control assembly 34A1A2 (fig. 3-81).
- (3) Measure resistance between E1 and E3 using multimeter. It should measure 20 K ohm  $\pm$ 200 ohm.
- (4) Check the resistance between E1 and E2 while slowly adjusting the variable resistor from full clockwise to full counter-clockwise. The multimeter indication should change smoothly across the resistance range of zero to 20K ohms.
- (5) If the indications in (3) and/or (4) above are abnormal, replace the receiver rf head.

3-124. Control-indicator 34A4

a. Test Equipment Required

| Equipment                                   | Common Name        |
|---|--------------------|
| Multimeter, Digital, AN/USM-486             | Digital Multimeter |
| Cable Assembly, Special Purpose, Electrical | CX-12098/U         |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U         |

b. Operational Check.

- (1) Loosen the screws securing plug P1 (34A1W1J5) to chassis connector 34A1W1J5 and disconnect the plug (fig. 3-77).
- (2) Set the RCVR CHANNEL control to channel 1588.
- (3) Using the multimeter, check for the correct resistance between the following pins of P1 (34A1W1J5) as shown in the chart below:

| Pins     | Resistance |
|----------|------------|
| 1 and 14 | Infinity   |
| 2 and 14 | Infinity   |

| Pins      | Resistance |
|-----------|------------|
| 3 and 14  | Infinity   |
| 4 and 14  | Infinity   |
| 5 and 14  | Infinity   |
| 6 and 14  | Infinity   |
| 7 and 14  | Infinity   |
| 8 and 14  | Infinity   |
| 9 and 14  | Infinity   |
| 10 and 14 | Infinity   |
| 11 and 14 | Infinity   |
| 12 and 14 | Zero       |

(4) Set the RCVR CHANNEL control to channel 1587.

(5) Using the multimeter, check for correct resistance between the following pins of P1 (34A1W1J5) as shown in the chart below:

| Pins      | Resistance |
|-----------|------------|
| 1 and 14  | Infinity   |
| 2 and 14  | Zero       |
| 3 and 14  | Zero       |
| 4 and 14  | Zero       |
| 5 and 14  | Zero       |
| 6 and 14  | Zero       |
| 7 and 14  | Zero       |
| 8 and 14  | Zero       |
| 9 and 14  | Zero       |
| 10 and 14 | Zero       |
| 11 and 14 | Zero       |
| 12 and 14 | Infinity   |

(6) Remove control indicator 34A4 from the transmitter rf head as described in chapter 6, TM 11-5820-540-12.

(7) Connect plug PI (34A1W1J5) to chassis connector 34A1W1J5 using cable CX-12098/U.

(8) Remove the four screws securing the control-indicator cover and remove the cover.

(9) Connect the receiver rf head to the receiver fixed head using cable CX-12097/U and set the AC POWER switch to ON.

(10) Set the control-indicator to channel 1219.

(11) Check the voltage at terminal 24 (pin 13 of P1) using the multimeter. The multimeter should indicate zero volt.

- (12) Set the control-indicator to channel 1220.
- (13) Check the voltage at terminal 24 using the multimeter. The indication should be +26 volts dc.
- (14) Set the AC POWER SWITCH to OFF. Reinstall the control-indicator cover. If abnormal indications are obtained in either (3), (5), (11) or (13) above, replace control-indicator 34A4. Refer to chapter 6, TM 11-5820-540-12 for replacement procedures.

Section VII. MODULE REMOVAL AND REPLACEMENT PROCEDURES  
FOR BAND III RF HEADS

3-126. Replacement of Control-Indicator 38A2

Replacement of control-indicator 38A2 is covered in chapter 6, TM 11-5820-540-12.

3-127. Replacement of Low-Pass Filter 38AR1A1FL1

- a. Place the transmitter rf head right-hand side up and locate low-pass filter 38AR1A1FL1 (fig. 3-70).
- b. Disconnect the two rf leads, P2 (38AR1A1FL1J1) and P1 (38AR1A1FL1J2) from their mating connectors.
- c. Loosen the green-circled mounting screws that secure 38AR1A1FL1 to the chassis. Remove 38AR1A1FL1.
- d. To install the 38AR1A1FL1 replacement module, position the module over the two mounting holes and tighten the mounting screws. Connect plugs P1 (38AR1A1FL1J2) and P2 (38AR1A1FL1J1) to their respective mating connectors.

3-128. Replacement of RF Power Monitor 38AR1A2

- a. Place the transmitter rf head top side up and locate rf power monitor 38AR1A2 (fig. 3-70).
- b. On the front panel of the transmitter rf head, loosen and remove the hexagonal nut that secures the PWR OUT connector to the front panel.



- c. Disconnect plug P2 (38AR1A2J1) from 38AR1A2J1.
- d. Disconnect plug P1 (38AR1A1W1J4) from 38Ar1A1W1J4 (fig. 3-68).
- e. Remove the four red-circled mounting screws that secure rf power monitor 38AR1A2 to its bracket and remove the module.
- f. To install the 38AR1A2 replacement module, slide connector J2 of the power into the PWR OUT opening in the front panel and secure the hexagonal nut. Secure 38AR1A2 to its mounting bracket with four screws.

## NOTE

The PWR OUT connector hexagonal nut must be well secured before tightening the 38AR1A2 mounting screws.

- g. Connect plug P2 (38AR1A2J1) to 38AR1A2J1. Connect plug P1 (38AR1A1W1J4) to 38AR1A1W1J4 on the chassis and secure with two screws.
- 3-129. Replacement of Voltage Regulator Assembly 38AAR1A1A1
- a. Place the transmitter rf head right-hand side up.
  - b. Locate the voltage regulator assembly 38AR1A1A1 (fig. 3-70). Loosen and remove the four green-circled mounting screws. Pull the module up, carefully disengaging the connector.
  - c. To install the replacement module, carefully engage the connector of the module with the chassis connector by pushing the module straight down.
  - d. Tighten the four green-circled screws.

## 3-130. Replacement of Control-indicator 34A4

Replacement of control-indicator 34A4 is covered In chapter 6, TM 11-5820-540-12.

## 3-131. Replacement of Frequency Multiplier 34A2A2

- a. Place the receiver rf head top side up and locate frequency multiplier 34A2A2 (fig. 3-77).
- b. Disconnect plug P1 (34A2A2J1) from 34A2A2J1 of frequency multiplier 34A2A2.
- c. Loosen three green-circled mounting screws and carefully lift the module, disengaging it from the chassis connector.
- d. To install the 34A2A2 replacement module, position the module over three mounting holes and carefully press home the connector.
- e. Tighten the three mounting screws and connect the plug P1 (34A2A2JI) to 34A2A2J1 on the replacement module.

3-132. Replacement of Signal Level Control-Monitor 34A5

- a. Place the receiver right-hand side up and locate signal level control-monitor 34A5 (fig. 3-81).
- b. Disconnect P1 (34A5J2) and P2 (34A5J1) from their mating connectors.
- c. Loosen three green-circled mounting screws and carefully lift the module, disengaging it from the chassis connector.
- d. To install the 34A5 replacement module, position the module over the mounting holes and carefully press home the connector.
- e. Tighten the mounting screws and connect plugs P1 (34A5J2) and P2 (34A5J1) to connectors J1 and J2 respectively of the replacement module.

3-133. Replacement of Intermediate Frequency Amplifier 34AR1

- a. Place the receiver rf head bottom side up and locate intermediate frequency amplifier 34AR1 (fig. 3-84).
- b. Disconnect plug 34A1W1A1P2 from 34AR1J1.
- c. Loosen the three green-circled mounting screws and carefully lift the module, disengaging it from the chassis connector.
- d. To install the replacement module, position the module over the mounting holes and carefully press home the connector.
- e. Tighten the three mounting screws and reconnect plug 34A1W1A1P2 to 34AR1J1.

3-134. Replacement of Frequency Mixer Stage 34A7

- a. Place the receiver rf head bottom side up and locate frequency mixer stage 34A7 (fig. 3-84).
- b. Disconnect plug PI (34A7J2) from P2 (34A7J1) from J2 and J1 respectively of 33A7.
- c. Loosen the three green-circled mounting screws and carefully lift the module, disengaging it from the chassis connector.
- d. To install the replacement module, position the module over the mounting holes and carefully press home the connector.
- e. Tighten the three mounting screws and reconnect P1 (34A7J2) and P2 (34A7J1) to J2 and J1 respectively of 34A7.

3-135. Replacement of Power Supply 34PS1

- a. Place the receiver rf head left-hand side up and locate power supply 34PS1.
- b. Loosen three green-circled screws and carefully lift the module disengaging it from the chassis connector.

- c. To install the replacement module, position the module over the mounting holes and carefully press home the connector.
- d. Tighten the three mounting screws.

### 3-136. Replacement of Low-Pass Filter 34FL1

- a. Place the receiver rf head rear side up. Locate low pass filter 34FL1 (fig. 3-77).
- b. Disconnect plugs P1 (34FL1J2) and P2 (34FL1J1) from their respective connectors.
- c. Place the receiver rf head bottom side up and remove intermediate frequency amplifier 34AR1 as explained in paragraph 3-137.
- d. Remove the two mounting screws for 34FL1 which are located on the chassis under intermediate frequency amplifier 34AR1.
- e. To install the 34FL1 replacement module, place the module on the mounting holes and tighten the two screws from the other side of the chassis.
- f. Replace intermediate frequency amplifier 34AR1 as explained in paragraph 3-137.
- g. Connect plugs P1 (34FL1J2) and P2 (34FL1J1) to their respective connectors.

### 3-137. Removal and Replacement Procedures for Antenna Connector on Band II and III (Fig. 3-88)

- a. Remove antenna element (2) AS-2194/GRC-103(V) (Band II) or AS-2195/GRC-103(V) (Band III) from antenna system AS-1853/GRC-103(V) (Band II) or AS-1854/GRC-103(V) (Band III).
- b. Remove three screws (4) and lift washer (3) off connector (1).
- c. Unscrew connector (1) and remove.
- d. Screw new connector (1) into antenna element assembly (2).
- e. Replace washer (3).
- f. Replace three screws (4), and tighten with torque driver. Tighten to 8.5 in. - lb.
- g. Replace antenna element (2) AS-2194/GRC-103(V) (Band II) or AS-2195/GRC-103(V) (Band III) into antenna system AS-1853/GRC-103(V) (Band II) or AS-1854/GRC-103(V) (Band III).
- h. Reconnect antenna coax to receiver rf head.
- i. With switch on receiver in REFL PWR position, check for reflected power indication. Meter should read less than 20 percent of full scale.

- g. Replace antenna element (2) AS-2194/GRC-103(V) (Band II) or AS-2195/GRC-103(V) (Band III) into antenna system AS-1853/GRC-103(V) (Band II) or AS-1854/GRC-103(V) (Band III).
- h. Reconnect antenna coax to receiver rf head.
- i. With switch on receiver in REFL PWR position, check for reflected power indication. Meter should read less than 20 percent of full scale.
- j. If reading is greater than 20 percent of full scale, proceed to troubleshoot the system.

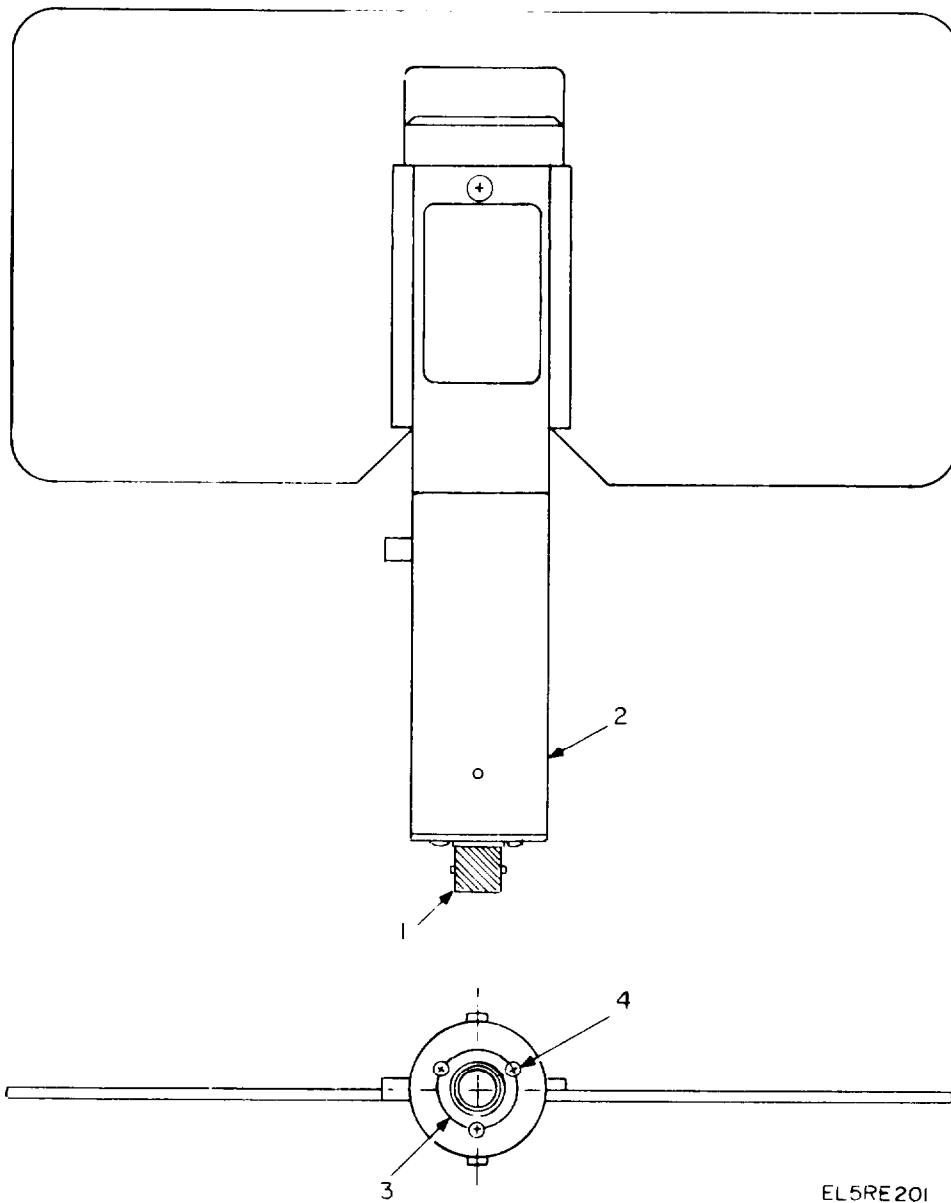


Figure 3-88. Removal of Antenna Element AS-2194/GRC-103(V) on Antenna Assembly AS-1853/GRC-103(V) (Band II) or Antenna Element AS-2195/GRC-103(V) on Antenna Assembly AS-1854/GRC-103(V) (Band III).

## Section VIII. TROUBLESHOOTING (BAND IV)

## 3-138. General

This manual contains the systematic troubleshooting procedures required to sectionalize a fault in the radio set and trace it to the defective module or part. Meter readings may facilitate the location of a fault without the help of test equipment or measuring circuits. Operational tests frequently indicate the general location of trouble, and in many instances help in determining the nature of the fault. Suitable starting points are provided by the operational check, loop testing procedure, and troubleshooting charts in TM 11-5820-540-12. The modified loop test procedure, troubleshooting charts and signal substitution procedures in the following paragraphs are provided to facilitate localization of faulty modules by direct support personnel.

## NOTE

Replacement of one or more suspected defective modules may be a quick and effective method of repairing a radio set in emergency conditions.

## 3-139. Modified Loop Test Procedure

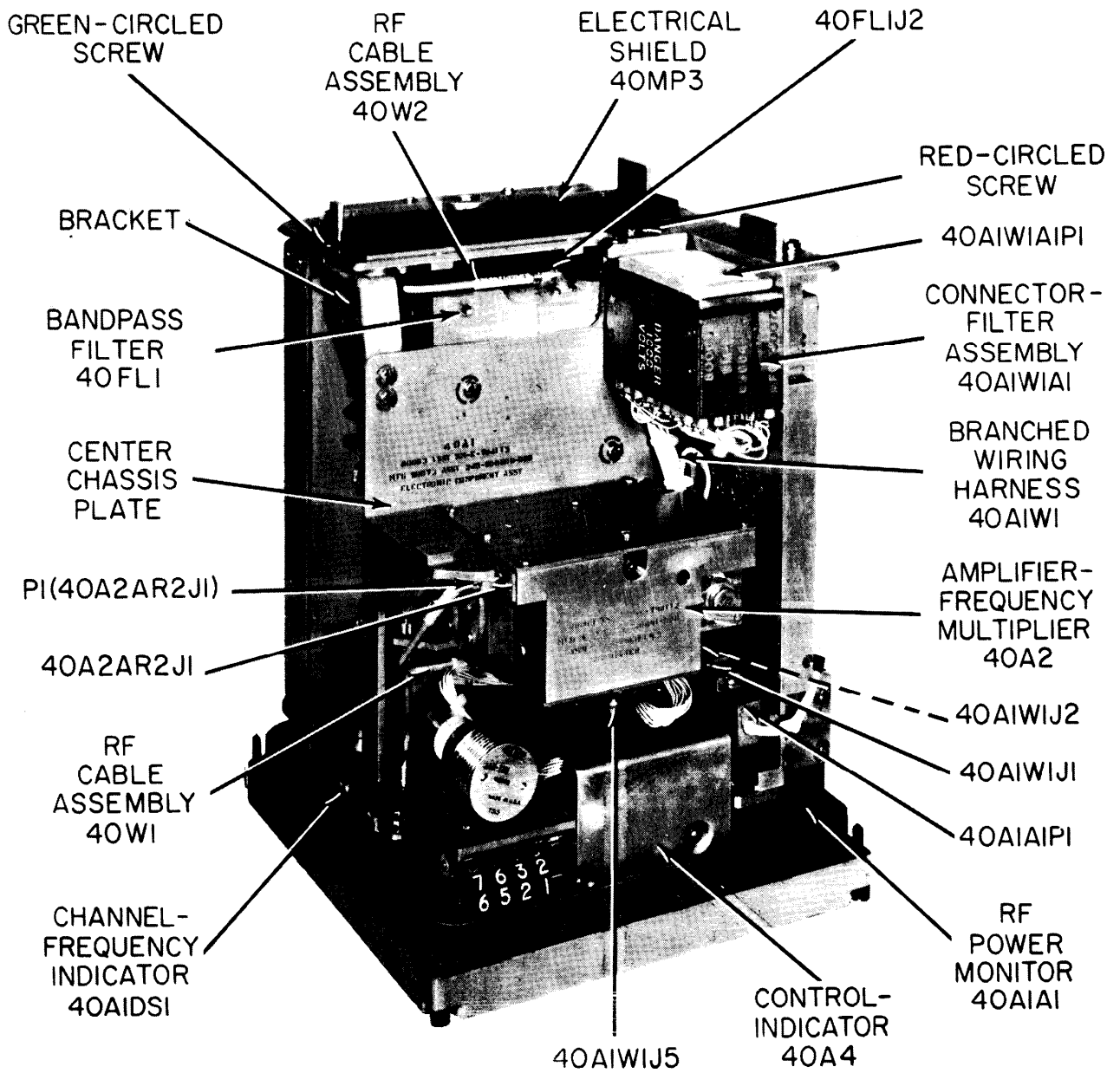
Refer to paragraph 3-4.

## 3-140. Amplifier-Frequency Multiplier AM-4323/GRC-103(V), Band IV Transmitter RF Head (Unit 40) (Fig. 3-88, 3-89, and 3-90)

## CAUTION

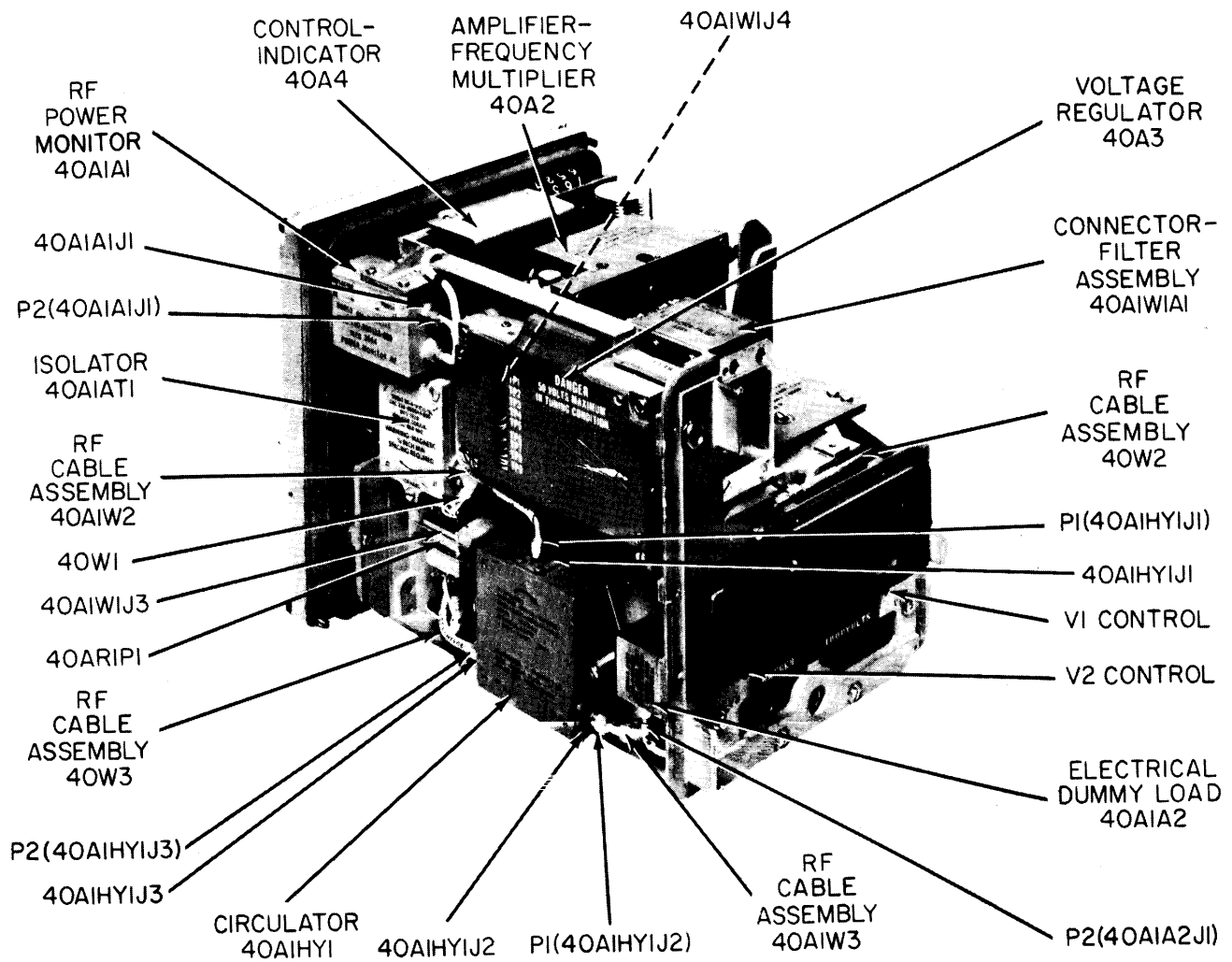
The transmitter rf head, when extended, must be air-cooled during tests. A cooling fan must be pointed toward the power amplifier tubes at all times. If a cooling fan is not available, do not operate the transmitter rf head for periods longer than 3 minutes. Another alternative is to place the transmitter rf head back into the transmitter case while troubleshooting radio transmitter 5TR1,

a. General. The troubleshooting chart in b below contains troubleshooting procedures for the transmitter fixed and rf heads (units 5TR1 and 40). Paragraphs 3-143 through 3-156 contain test procedures for the transmitter rf head only. Refer to paragraphs 3-8 through 3-12 for test procedures for the transmitter fixed head. For more effective troubleshooting and testing of the transmitter modules, proceed as follows:



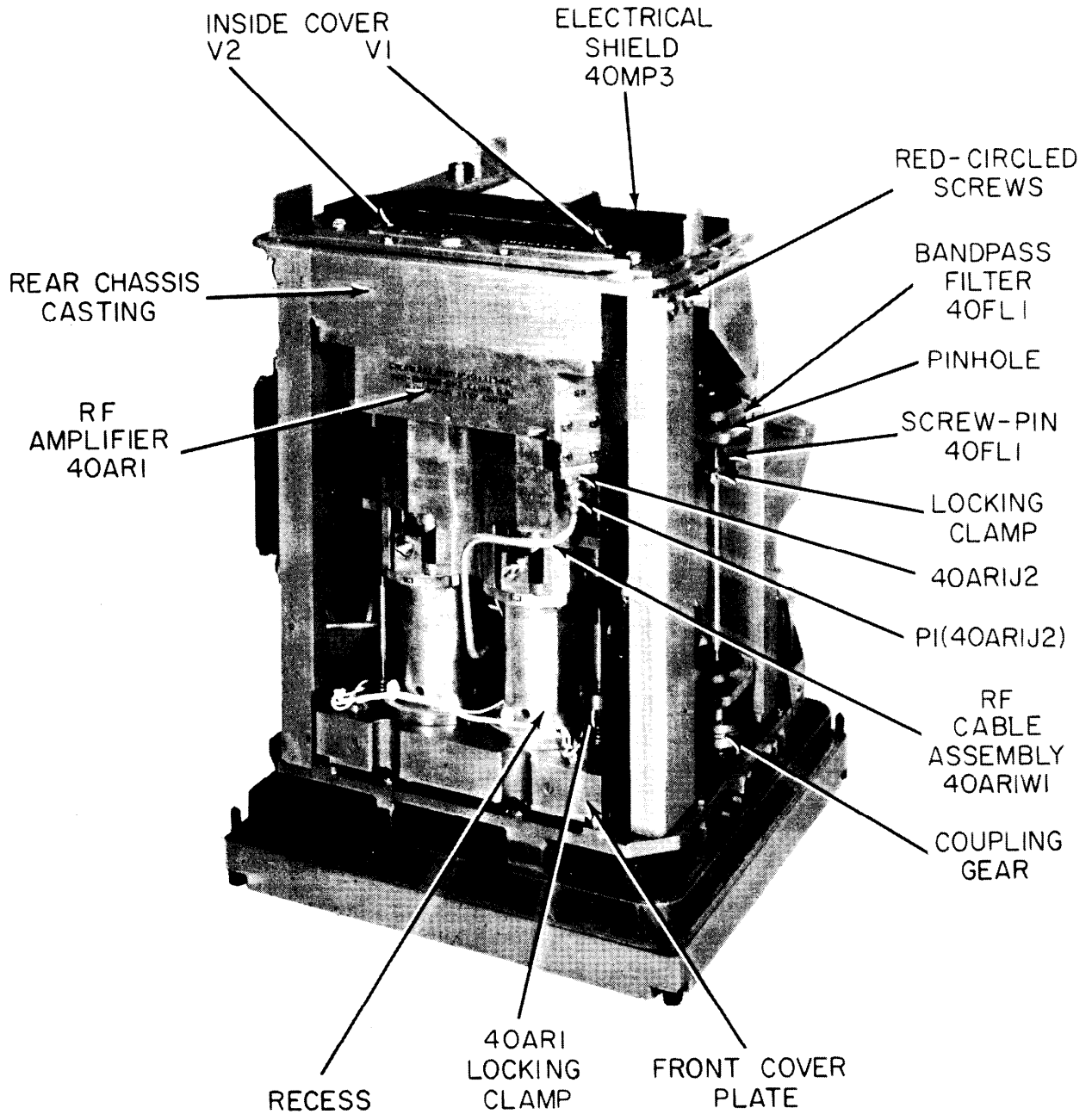
EL5RE202

Figure 3-89. Band IV Transmitter RF Head, Top View.



EL5RE203

Figure 3-90. Band IV Transmitter RF Head, Side View.



EL5RE204

Figure 3-91. Band IV Transmitter RF Head, Bottom View.



- (1) Remove the transmitter rf and fixed heads from the transmitter case.
- (2) Remove the transmitter rf head dust cover.
- (3) Connect the transmitter rf head to the transmitter case with cable CX-12094/U. Connect the transmitter fixed head to the transmitter case with CX-12092/U and CX-12093.

CAUTION

The transmitter rf head PWR OUT connector must be connected to the dummy load during troubleshooting. Damage to the equipment will result if this is not done.

b. Transmitter Troubleshooting Chart.

| symptom  | Probable cause   | Checks and corrective measures  |
|--|--|---|
| <p>1. When AC POWER switch is set to ON/RESET centrifugal fan does not start, AC POWER and LOW POWER lamps do not light, buzzer does not sound.*</p> | <p>a. Defective power supply 5TR1PS1 (fig. 3-1).</p> <p>b. Defective switch 5TR1-A1Cb1 (fig. 3-3).</p> | <p>a. Check for 115 vac at connector J3 (5TR1PS1-P1) pins 6 and 7 (para 3-8). If voltage is present, replace 5TR1PS1 (para 3-50).</p> <p>b. If voltage is not present in a above, check for 115 vac at switch LINE and LOAD terminals. If indications are normal make wiring continuity checks (FO-4-43).</p> |
| <p>2. 28 v and 12 v metering negative, all other metering zero, LOW POWER and SYNC lamps light.</p>  | <p>Short circuit.</p>  | <p>Check for short on 28 vdc supply line (FO-4-43, 4-77).</p>   |
| <p>3. 12 v negative, 28 v full scale, 600 v high, DRIVER normal, all other metering zero, LOW POWER and SYNC lamps light.</p>                        | <p>Short circuit.</p>  | <p>Check for short on 26 vdc supply line (FO-4-43, 4-77). check for short on 630 vdc supply line (FO-4-43, 4-77).</p>   |

The fan should start after 2 minutes.

b. Transmitter Troubleshooting Chart - Continued.

| Symptom   | Probable cause                                    | Checks and corrective measures  |
|---|---|---|
| 4. All metering zero, all lamps inoperative, centrifugal fan operates.  | Short circuit.                                    | Check for short on 26 vdc supply line (F0-4-43, 4-77); check for short on 630 vdc supply line (F0-4-43, 4-77).  |
| 5. 28 v normal or zero, 12 v normal; DOUBLER, MULT, DRIVER and PWR OUT low; OSC high; LOW POWER and SYNC lamps lights.                                      | Open circuit.                                     | Check for open on 28 vdc Supply (F0-4-43, 4-77) between 5TR1A1J3 (pin 1) and 40A1W1A1P1 (pin 11).   |
| 6. When AC POWER switch is set to ON/RESET, centrifugal fan does not start; AC POWER, LOW POWER, and OVERHEAT lamps light, buzzer sounds.                   | a. Defective centrifugal fan 5A2B1 (section x).   | a. Check for 140 vac at connector J5 (5A2-B1P1), pins 1 and 2 (transmitter case). If voltage is present, replace 5A2131 (section x).  |
|   | b. Defective power supply 5TR1PS1 (fig. 3-1).     | b. Check for 140 vac at power supply filter terminals FL5 and FL6 of 5TR1PS1 (fig. 3-2). If no voltage is present, replace 5TR1PS1 (para 3-50). If voltage is present at FL5 and FL6 of 5TR1PS1 (fig. 3-2) but not at pins 1 and 2 of connector J5 (5A2B1P1) (fig. 3-113) in the transmitter case, remove 115 vac power source and check for continuity between these two points. |
| 7. When AC POWER switch is set to ON/RESET, centrifugal fan does not start, OVERHEAT lamp is not on. Buzzer may or not sound. All other indications normal. | a. Defective OVERHEAT lamp 5TR1A2ADS4.            | a. Replace indicator lamp 5TR1A2ADS4.   |
|   | b. Defective pressure differential monitor 5A2A2. | b. Replace 5A2A2 (section x).   |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom   | Probable Cause  | Checks and Corrective Measures   |
|---|---|--|
| <p>8. Buzzer does not sound when any alarm lamp lights or goes out.</p>   | <p>a. Defective buzzer 5TR1A1DS5 (fig. 3-3) .</p> <p>b. Defective switch 5TR1A1S2 (fig. 3-3) .</p> <p>c. Defective alarm control 5TR1A1A2 (fig. 3-3).</p> | <p>a. Check for vdc at buzzer terminals. If voltage is present, replace buzzer (para 3-52).</p> <p>b. if voltage is not present at buzzer terminals, remove 115 vac power source and check for continuity from buzzer negative terminal to pin 5 of connector J3 (5TR1PS1P1) (fig. 3-1) and from buzzer positive terminal to pin 4 of 5TR1A1J3. If continuity is broken because of 5TR1A1S2, higher category maintenance is required.</p> <p>c. If continuity is broken because of 5TR1A1A2, replace 5TR1A1A2 board (para 3-45).</p> |
| <p>9. OVERHEAT amp does not go off with n 10 seconds after AC POWER switch is set to ON/RESET.</p> <p>AC POWER switch set to ON/RESET at room temperature centrifugal fan operates full speed (Case CY-4637A only).</p> | <p>Defective pressure differential monitor 5A2A2.</p> <p>Defective control monitor temperature sensor 5A2A2.</p>  | <p>Rep ace 5A2A2 (Section X).</p> <p>Check sensor connections. If connections are not defective, replace 5A2A2 (Section X).</p>  |
| <p>10. SYNC LAMP does not go out within 10 seconds after AC POWER switch is set to ON/RESET.</p>  | <p>a. Defective synthesizer 5TR1A2 (fig. 3-3).</p> <p>b. Defective power Supply 5TR1PS1 (fig3 - 1) .</p>  | <p>a. Remove synthesizer (para 3-10, 3-48) and check for 12 vdc, 26 vdc, and 28 vdc at J1 (5TR1A2P2) (fig. 3-3). If normal indications are obtained, replace synthesizer 5TR1A2 (para 3-48) .</p> <p>b. f indications in a above are abnormal,</p>   |

b. Transmitter Troubleshooting Chart - continued

| Symptom   | Probable Cause   | Checks and Corrective Measures  |
|---|--|---|
| 10. Continued.  |  | check 5TR1PS1, (para 3-8) . If abnormal indications are obtained replace 5TR1PS1 (para 3-50) .  |
| 11. DRIVER metering 0%, or greater than 100% (Band IV only).  | Short circuit in voltage regulator assembly 40A3 (fig. 3-90) or rf amplifier 40AR1 (fig. 3-91) . | Replace driver amplifier tube VI (para 6-13b, TM 11-5820-540-12) . If indication remains abnormal reinstall and replace final amplifier tube V2. If indication remains abnormal, reinstall original tube and replace voltage regulator assembly 40A3 (chapter 6, para 6-16b, TM 11-5820-540-12). If indication remains abnormal, higher category maintenance is required. |
| 12. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR OUT position reads low. | a. Defective rf power monitor 40A1A1 (fig. 3-90).  | a. Measure power (16.5 w minimum) at P2 (40A1A1J1). If normal, check 40A1A1 (para 3-149).   |
|   | b. Defective circulator 40A1HY1 (fig. 3-90).   | b. If abnormal indication is obtained in a above, measure power (18.5 w minimum at 40W3P2) (FO 4-77). If normal, check 40A1HY1 (para 3-150).  |
|   | c. Defective rf amplifier 40AR1 (fig. 3-91).   | c* If indication is abnormal in b above, measure power at 40FL1J2 (para 3-146). If normal, higher category maintenance is required.   |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom  | Probable Cause  | Checks and Corrective Measures   |
|--|---|--|
| <p>13. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR CUT position reads low, DRIVER position reads high.</p> | <p>No OUTPUT CATHODE regulation.<br/>Defective power supply 5TR1PS1 (fig. 3-1) or voltage regulator assembly 40A3 (fig. 3-90).</p>  | <p>Remove transmitter 5TR1 and measure resistance from pin 30 of connector J8 (5TR1A1P3) (FO-4-43) (transmitter case) to ground (approximately 12 ohms). If normal, replace 5TR1PS1 (para 3-50). If abnormal, check assembly 40A3 (para 3-143).</p>  |
| <p>14. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR CUT position reads low. DRIVER position reads low.</p>  | <p>a. Defective power supply 5TR1PS1 (fig. 3-1) or voltage assembly 40A3 (fig. 3-90).</p> <p>b. Defective rf amplifier 40AR1 (fig. 3-91).</p> <p>c. No DRIVER CATHODE regulation.<br/>Defective</p> | <p>a. Measure the power (2 watts minimum) at 40-AR1P1 (para 3-146). If normal, check voltage at TP2 and TP4 of 40A3 (para 3-143). If normal, disconnect transmitter rf head and measure resistance between TP2 and TP4 of 40A3 (should be 1.5 ohms approximately). If voltage at TP2 and TP4 is abnormal, check OUTPUT HEATER/OUTPUT CATHODE circuit of 5TR1PS1 (para 3-8). If 5TR1PS1 check is normal check continuity of OUTPUT HEATER/OUTPUT CATHODE wiring between 5TR1PS1 and transmitter rf head (FO-4-43, 4-77).</p> <p>b. If power at 40W3P2 (FO-4-76), is abnormal (less than 18.5 watts) higher category of maintenance is required.</p> <p>c. Remove radio transmitter 5TR1 from case and</p> |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom        | Probable Cause   | Checks and Corrective Measures   |
|----------------|--|--|
| 14. Continued. | <p>power supply 5TR1PS1 (fig. 3-1) or voltage regulator assembly 40A3 (fig. 3-90).</p> <p>d. Defective DRIVER CATHODE/DRIVER HEATER circuit.</p> <p>e. Defective rf amplifier 40AR1 (fig. 3-91).</p> | <p>measure resistance from pin 29 of connector J8 (5TR1A1P3) (FO-4-43) to ground (34 ohms approximately). If normal, replace 5TR1PS1 (para 3-50). If abnormal, check voltage regulator assembly 40A3 (para 3-143).</p> <p>d. Measure power at 40FL1J2 (para 3-146). If normal, check voltage across TP1 and TP3 of voltage regulator assembly 40A3 (para 3-143). If normal, disconnect transmitter rf head and measure resistance between TP1 and TP3 of voltage regulator assembly 40A3 (should be 1.5 ohms approximately). If voltage at TP1 and TP3 is abnormal, check the DRIVER HEATER/DRIVER CATHODE circuit of 5TR1PS1 (para 3-8). If 5TR1PS1 check is normal, check continuity of DRIVER HEATER/DRIVER CATHODE wiring between 5TR1PS1 and transmitter rf head (FO-4-43, 4-77).</p> <p>e. If DRIVER CATHODE/DRIVER HEATER circuit is normal, higher category maintenance is required.</p> |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom   | Probable Cause  | Checks and Corrective Measures  |
|---|---|---|
| 15. At channel 2960 or 2959, and slightly above and below, LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. PWR OUT position reads low, DRIVER position reads low, and MULT position reads normal or high. | Defective bandpass filter 40FL1 (fig. 3-89) .                 | Measure power at 40FL1J2 (para 3-146). If below +24.8 dBm, higher category maintenance is required.   |
| 16. Same as 14 above, but at all channels.  | a. Defective rf amplifier 40AR1 (fig. 3-91) .                 | a. If power at 40W3P2 (FO-4-76) is abnormal (less than 18.5 watts), higher category of maintenance is required.                               |
|   | b. Defective bandpass filter 40FL1 (fig. 3-89) .              | b. Measure power at 40FL-1J2 (para 3-146). If below +24.8 dBm, higher category of maintenance is required.                                    |
|   | c. Defective isolator 40A1AT1 (fig. 3-90) .                   | c. Measure power at 40A-2AR2J1 (para 3-142). If +27.5 dBm minimum, power is normal; check 40A1AT1 (para 3-148).                               |
|   | d. Defective cables.  | d. If a, b, and c above check normal, test continuity of cables 40W1, 40W2, and 40W4 (fig. 3-90). Higher category of maintenance is required. |
| 17. At channel 2960 or 2959, and slightly above and below, LOW POWER light does not go out within 60 seconds after AC POWER switch is set.  | a. Defective amplifier frequency multiplier 40A2 (fig. 3-90). | a. Check output of 40A2 (para 3-142) at 40A2-AR2J1. If below +27.5 dBm, higher category maintenance is required                               |

b. Transmitter Troubleshooting Chart - Continued.

| Symptom  | Probable Cause  | Checks and Corrective Measures   |
|--|---|--|
| <p>17. Continued.</p> <p>to ON/RESET. PWR OUT position reads low, DRIVER position reads low and MULT position reads low.</p>   | <p>b. Defective wiring.</p>   | <p>b. Check continuity of 26 vdc and 28 vdc REG wiring between 5TR1PS1 and transmitter rf head (FO-4-43, and 4-77).</p>  |
| <p>18. Same as 16 above but at all channels.</p>   | <p>a. Defective wiring.</p> <p>b. Defective amplifier frequency multiplier 5TR1A4 (fig. 3-3).</p> | <p>a. Measure power at amplifier frequency multiplier 40A2AR2J1 (+27.5 dBm minimum). If abnormal, check for continuity from pin A1 of 40A1W1J2 to pin A2 of J11 (5TR1A4P1) (FO-4-43, and 4-77).</p> <p>b. If the wiring continuity check in a above is normal, replace 5TR1A4 (para 3-50).</p> |
| <p>19. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. DRIVER position reads low, MULT position reads low, and DOUBLER position reads low*</p>                     | <p>a. Defective amplifier frequency multiplier 5TR1A4 (fig 3-3).</p> <p>b. Defective wiring.</p>  | <p>a. Measure power at pin A1 of J11 (5TR1A4P1) (para 3-10). If normal, check 5TR1A4 (para 3-11).</p> <p>b. Check for +28 vdc at pin 1 of J11 (5TR1A4P1)</p>   |
| <p>20. LOW POWER light does not go out within 60 seconds after AC POWER switch is set to ON/RESET. DRIVER position reads low, MULT position reads low, DOUBLER position reads low, OSC position reads low.</p> | <p>a. Defective synthesizer 5TR1A2 (fig. 3-3) .</p> <p>b. Defective wiring.</p>                   | <p>a. Check synthesizer 5TR1A2 (para 3-10).</p> <p>b. Check inputs to 5TR1A2 at J1 (5TR1A2P2) (FO-4-43 )</p> <p>pin 1 +28 vdc<br/> pin 2 +12 vdc<br/> pin 3 0v<br/> pin 37 +28 vdc.</p>  |



b. Transmitter Troubleshooting Chart - Continued.

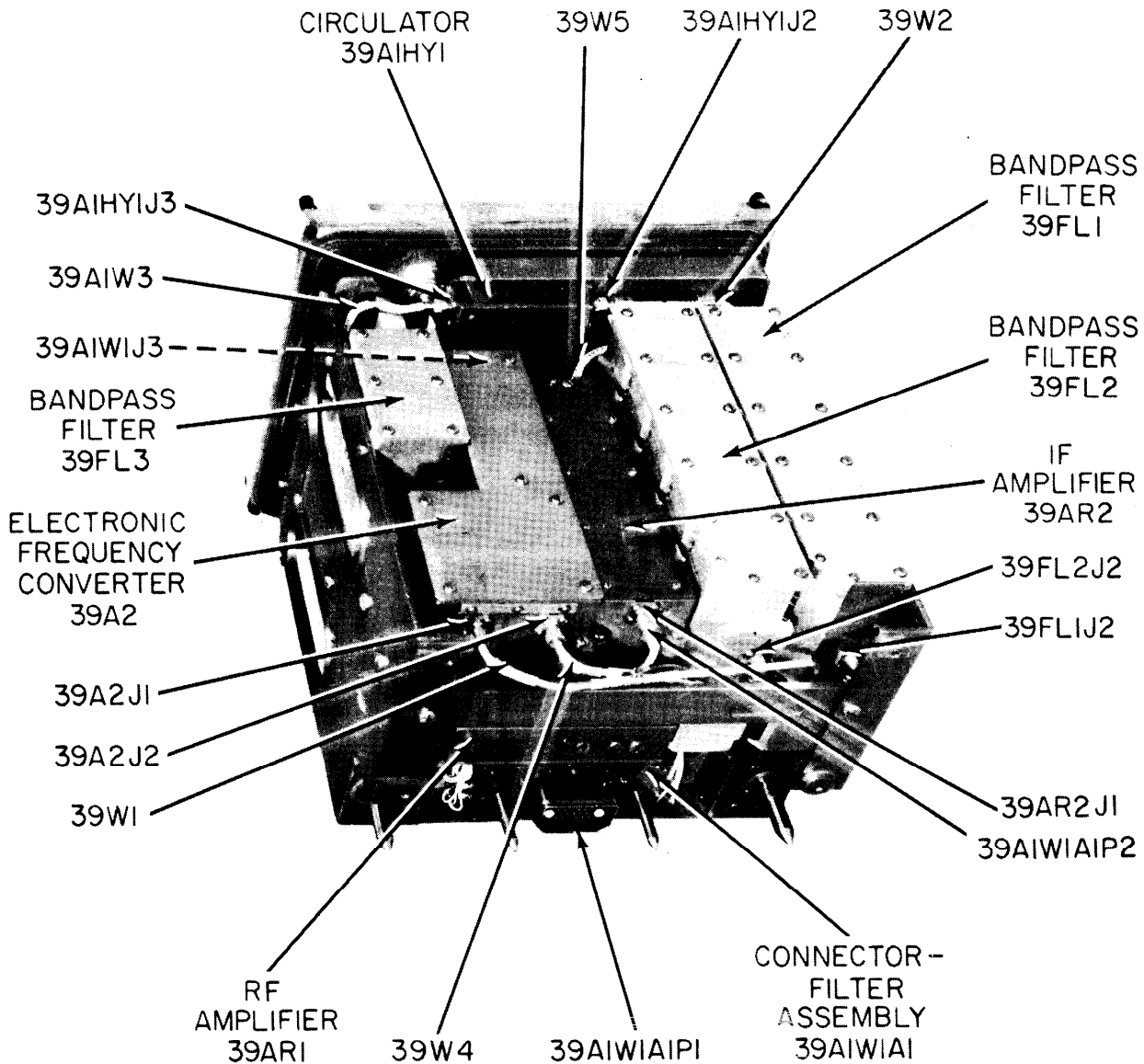
| Symptom  | Probable cause  | Checks and corrective measures   |
|--|---|--|
| 21. SYNC alarm does not go out within 10 seconds after AC POWER switch is set to ON/RESET.   | a. Defective synthesizer 5TR1A2 (fig. 3-3).<br>b. Defective power supply 5TR1PS1 (fig. 3-1).                    | a. Check synthesizer 5TR1A2 (para 3-10).<br>b. Check power supply 5TR1PS1 (para 3-8).  |
| 22. When AC POWER switch is set to ON/RESET, buzzer and centrifugal fan operate, LOW POWER and SYNC alarm lights come on, DRIVER metering is low, all other metering reads zero. | Defective power supply 5TR1PS1 (fig. 3-1).  | Check voltage regulator amplifier 5TR1PS1AR1 of power supply 5TR1PS1 (para 3-8).   |
| 23. No communication. Metering and LOW POWER and SYNC alarms may or may not indicate normal.   | Synthesizer 5TR1A2 off frequency due to:<br>a. Defective synthesizer 5TR1A2 (fig. 3-3).<br>b. Defective wiring. | a. Check synthesizer 5TR1A2 (para 3-10).<br>Check wiring from control-indicator 40A4 to synthesizer 5TR1A2 (FO-4-47 and 4-77). |

3-141. Amplifier-Converter AM-4319/GRC-103(V), Band IV Receiver RF Head (Unit 39) (Figs 3-92, 3-93, and 3-94)

a. General. The troubleshooting chart in b below contains troubleshooting procedures receiver fixed and rf heads (units 1RE1 and 39). Since paragraphs 3-157 through 3-168 contain test procedures for the receiver rf head only, refer to paragraphs 3-35 through 3-42 for test procedures for the receiver fixed head. For more effective troubleshooting and testing of the receiver modules, proceed as follows:

- (1) Remove the receiver rf and fixed heads from the receiver case.
- (2) Remove the receiver rf head dust cover.

- (3) Connect the receiver rf head to the receiver case with cable CX-12097/U. Connect the receiver fixed head to the receiver case with cables CX-12095/U and CX-12096/U.
- (4) Connect the receiver to a 115 vat, 47 to 420 Hz source, and 1 troubleshoot the receiver.



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Figure 3-92. Band IV Receiver RF Head, Bottom View.

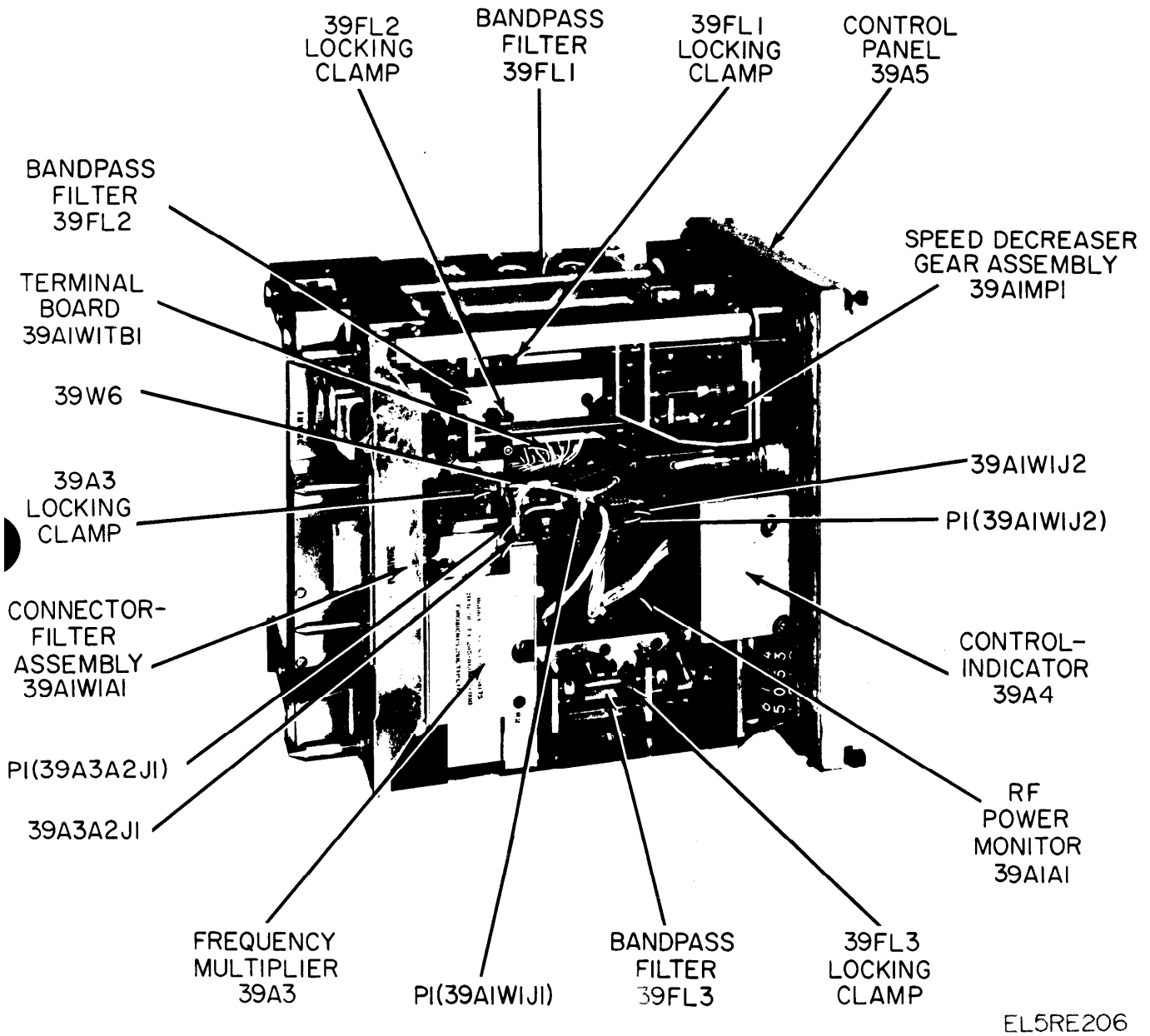
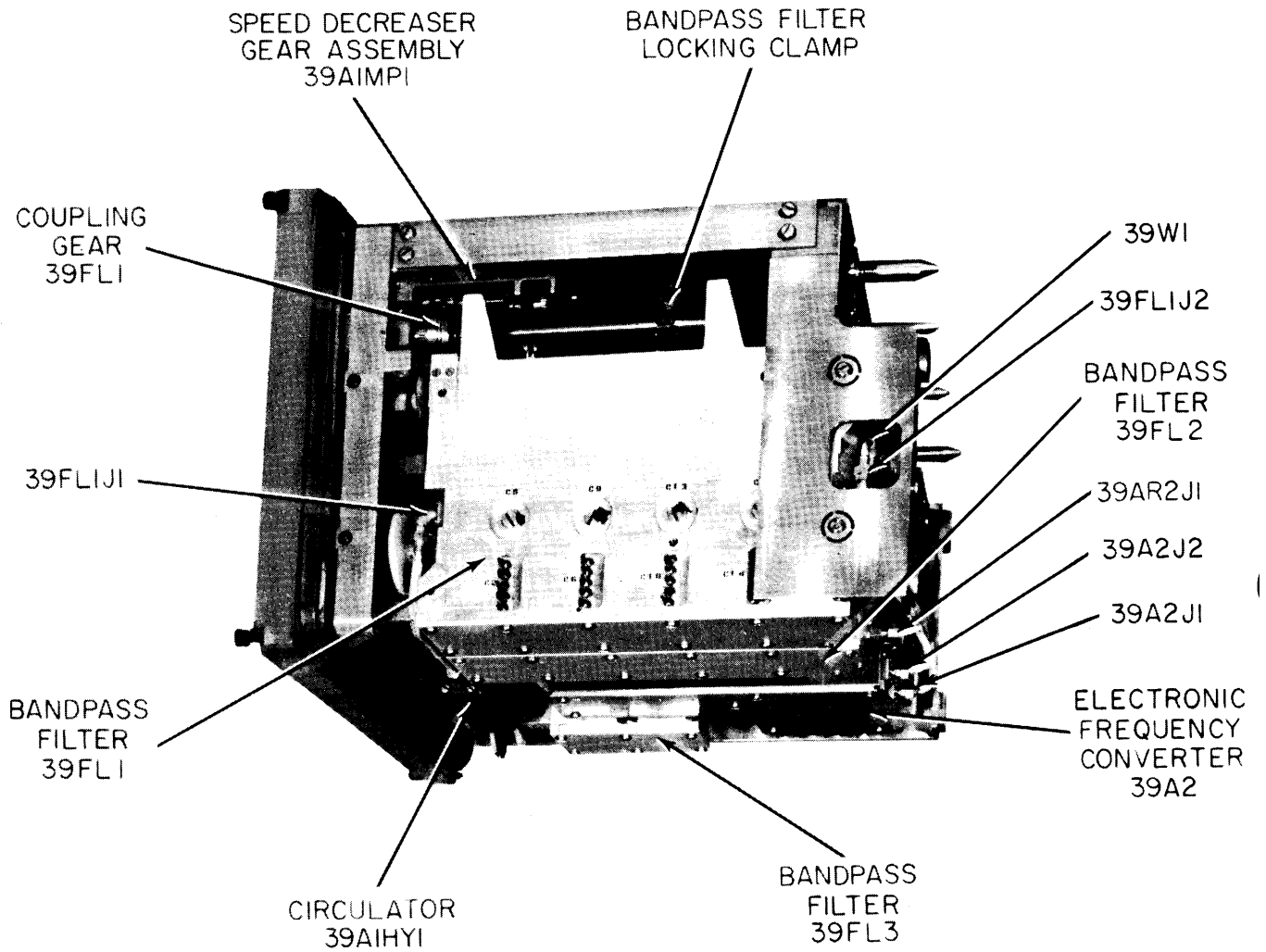


Figure 3-93. Band IV Receiver RF Head, Top and Rear View.



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Figure 3-94. Band IV Receiver RF Head, Right Side View.

b. Receiver Troubleshooting chart.

| Symptom   | Probable Cause  | Checks and Corrective Pleasures  |
|---|---|--|
| <p>1. With AC POWER switch set to ON, there are no meter indications and no alarms.</p> | <p>Defective switch 1RE1A-1CB1 (fig. 3-40).</p>   | <p>Check for 115 vac at switch LINE and LOAD terminals of switch 1RE1A1CB1 (fig. 3-40). If switch is normal, make wiring continuity checks (F0-4-28).</p>  |
| <p>2. Buzzer does not sound when any alarm lamp lights or goes out.</p>                 | <p>Defective buzzer 1RE1A-1DS5 (fig. 3-37).</p>   | <p>Check for 26 vdc at terminals of buzzer (fig. 3-37). If voltage is present, replace buzzer (para 3-60). If voltage is not present, make wiring continuity checks (F0-4-28).</p>   |
| <p>3. AC POWER switch will not stay on.</p>   | <p>Short circuit.</p>   | <p>Make resistance check on -12 Vdc, +12 vdc and +26 vdc lines to isolate short circuit (F0-4-28 and 4-74).</p> <p style="text-align: center;">NOTE</p> <p>To gain access to J1, remove control-indicator 39A4 (para 6-18.1a., TM 11-5820-540-12) .</p>  |
| <p>4. LOW SIGNAL alarm is on; RCVR SIG metering reads low.</p>                          | <p>a. Defective rf power monitor 39A1A1 (fig. 3-93) .</p> <p>b. Defective circulator 39A1HY1 (fig. 3-92).</p> <p>c. Defective bandpass filter 39FL1 (fig. 3-92) .</p> | <p>a. Inject a signal at -60 dBm receive frequency into J1 of circulator 39A1A1 (para 3-174).</p> <p>b. Inject a signal at -62 dBm receive frequency into P1 (39A1HY1J2) (fig. 3-92) . If the alarm clears, higher category maintenance is required.</p> <p>c. Inject a signal at -65 dBm receive frequency into 39A2J1 (fig. 3-92). If the aarm clears, higer cate-</p> |

b. Receiver Troubleshooting Chart - Continued.

| Symptom   | Probable Cause   | Checks and Corrective Measures   |
|---|--|--|
| <p>4. Continued.</p>  | <p>d. Defective electronic frequency converter</p> <p>e. Defective IF amplifier 39AR2 (fig. 3-92).</p> <p>f. Local oscillator off frequency due to:</p> <p>(1) Defective synthesizer 1RE1A2 (fig. 3-40) .</p> <p>(2) Defective wiring.</p> | <p>gory maintenance is required.</p> <p>d. Perform operational check (para 3-151).</p> <p>e. Inject a 30 MHz signal at -35 dBm into 39A1W-1A1P2 (fig. 3-92). If the alarm clears, replace IF amplifier 39AR2 (para 3-175).</p> <p>f.(1) Check synthesizer (para 3-36).</p> <p>(2) Check wiring from 39A4 to J3 (1REIA-2P2) (FO-4-28 and 4-74).</p> |
| <p>5. LOW SIGNAL alarm, RCVR SIG reading low, MULT reading low, MULT DRIVER reading normal.</p> | <p>a. Defective frequency multiplier 39A3 (fig. 3-93).</p> <p>b. Defective bandpass filter 39FL2 (fig. 3-94) .</p>   | <p>a. Check that output power level at 39A3J1 (fig. 3-93) is +10 dBm minimum. If abnormal, higher category maintenance is required.</p> <p>b. Check that output power level at 39W4P2 (fig. 3-92, FO-4-74), with MULT PEAK control adjusted to maximum output level, is +8 dBm minimum. If abnormal, higher category maintenance is required.</p>  |
| <p>6. LOW SIGNAL alarm, RCVR SIG reading low, MULT reading low, MULT DRIVER reading low.</p>    | <p>Defective rf amplifier 39AR1 (fig. 3-92).</p>   | <p>Check output power of the rf amplifier 39AR1 (para 3-160).</p>  |

b. Receiver Troubleshooting Chart - Continued.

| Symptom  | Probable cause                             | Checks and corrective measures   |
|--|--|--|
| 7. SYNC alarm and/or LOW SIGNAL alarm, RCVR SIG reading low, MULT reading low, MULT DRIVER reading low, OSC reading low. | Defective synthesizer 1R-E1A2 (fig. 3-40). | Check supply voltage at J3 (1REIA2P2). If normal, replace synthesizer 1RE1-A2 (para 3-64). If abnormal, check wiring (F0-4-28 and 4-74). |

3-142. Amplifier-Frequency Multiplier 40A2

a. Test Equipment Required.

| Equipment  | Common Name   |
|--|---|
| Power Meter ME-441/U<br>Thermistor Mount HP-478A<br>Attenuator, Fixed, 20 dB, CN-1287/U<br>Cable Assembly, Special Purpose, Electrical<br>Cable Assembly, RF, CG-3573/U<br>Adapter-Connector OS-21010 (504-800054-000) | Power meter<br>Thermistor mount<br>20 dB attenuator<br>CX-12094/U |

b. Operational Check.

- (1) Disconnect P1 (40A2AR2J1) from 40A2AR2J1 on amplifier-frequency multiplier 40A2 (figs. 3-89 and F0-4-76).
- (2) Connect the test equipment as shown in figure 3-95.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 2959.
- (4) Set the AC POWER switch to ON/RESET. The power level should be +27.5 dBm minimum (power meter indicates +7.5 dBm).
- (5) Set the XMTR CHANNEL and XMTR TUNE controls to channel 2960. The power level should be +27.5 dBm minimum (power meter indicates +7.5 dBm).
- (6) Set the AC POWER switch to OFF.
- (7) Reconnect P1 (40A2AR2J1) to 40A2AR2J1 on amplifier-frequency multiplier 40A2.

- (8) Replace the transmitter rf head if an abnormal indication was obtained in (4) and (5) above (chapter 6, para 6-12c, TM 11-5820-540-12) .

3-143. Voltage Regulator 40A3

a. Test Equipment Required.

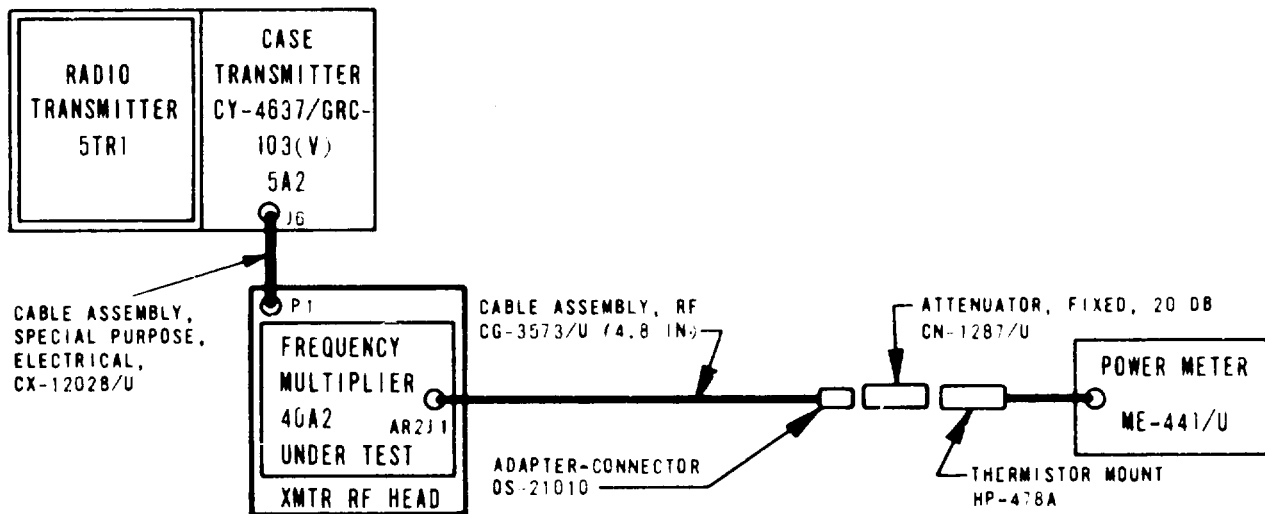
| Equipment  | Common Name                      |
|--|----------------------------------|
| Multimeter, Digital, AN/USM-486<br>Cable Assembly, Special Purpose, Electrical | Digital Multimeter<br>CX-12094/U |

CAUTION

These voltage checks must be completed within the 3 minute time limit, or the driver and output stages of the power amplifier will be damaged.

b. Operational Check.

- (1) Remove the plastic protective cover from voltage regulator 40A3 (fig. 3-90).
- (2) Connect the transmitter rf head to J6 on the transmitter case, using cable CX-12028/U.



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Figure 3-95. Amplifier Frequency Multiplier 40A2 Operational Check, Test Setup.



- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 2500.
- (4) Set the AC POWER switch to ON/ RESET.
- (5) Set the multimeter to measure dc voltage. Connect it between TP4 and TP5 with the test leads provided.
- (6) Adjust the PWR OUT PEAK control for the maximum multimeter indication.
- (7) Check for the correct voltages between the following voltage regulator assembly test points with the multimeter.

| Multimeter |      | DC voltages |
|------------|------|-------------|
| (+)        | (-)  |             |
| TP4        | TP2  | 5.4 to 6.2  |
| TP3        | TP 1 | 5.4 to 6.2  |
| TP4        | TP5  | 13.8 0.7    |
| TP4        | TP11 | 3.2 1.5     |
| TP3        | TP10 | 3.2 1.5     |

NOTE

To attain the proper voltage at TP4 and TP5, the POWER OUT PEAK control must be readjusted for the maximum indication.

- (8) Set the AC POWER switch to OFF.
- (9) Remove voltage regulator assembly 40A3 (chapter 6, para 6-16b, TM 11-5820-540-12) . Check for the correct resistance between the following pins of 40A3P1 with the multimeter.

| Pins     | Resistance (ohms 10%) |
|----------|-----------------------|
| 14 and 5 | 13                    |
| 8 and 5  | 22                    |
| 2 and 6  | 270 k                 |

- (10) Reinstall the plastic protective cover which was removed in (1) above.
- (11) If an abnormal indication was obtained in (7) or (9) above, replace voltage regulator assembly 40A3 (chapter 6, para 6-16b, TM 11-5840-12).

3-144. Control-Indicator 40A4

a. Test Equipment Required.

| Equipment   | Common Name                      |
|---|----------------------------------|
| Multimeter, Digital, AN/USM-486<br>Cable Assembly, Special Purpose,<br>Electrical | Digital Multimeter<br>CX-12094/U |

b. Operational Check.

- (1) Set the control-indicator to channel 2672.
- (2) Remove control-indicator 40A4 from the transmitter rf head (para 6-16a, TM 11-5820-540-12).
- (3) Remove the four screws securing the control-indicator cover, and remove the cover.
- (4) Reconnect plug P1 (40A1W1J5) to chassis connector 40A1W1J5 (figs. 3-89 and F0-4-76).
- (5) Connect the transmitter rf head to the transmitter case using cable CX-12028/U (1 ft. 3 in.). Set the AC POWER switch to ON/RESET.
- (6) Recheck the control-indicator for the channel setting of 2672.
- (7) Check for correct voltages between the following terminals on the command signals decoder with the multi meter.

| Terminals |     |          |
|-----------|-----|----------|
| (+)       | (-) | Dc volts |
| 29        | 21  | +5       |
| 28        | 21  | +5       |
| 25        | 21  | +5       |
| 24        | 21  | +5       |
| 23        | 21  | +5       |
| 22        | 21  | +5       |
| 20        | 21  | +5       |
| 19        | 21  | +5       |

| Terminals |     | DC<br>volts  |
|-----------|-----|--------------|
| +         | (-) |              |
| 18        | 21  | +5           |
| 16        | 21  | +5           |
| 15        | 21  | +5           |
| 13        | 21  | +5           |
| 14        | 21  | +0.5 or less |
| 17        | 21  | +0.5 or less |

(8) Set the control-indicator to channel 2671.

(9) Check for correct voltages between the following terminals on the command signals decoder with the multimeter.

| Terminals |     | DC<br>volts  |
|-----------|-----|--------------|
| +         | (-) |              |
| 29        | 21  | +0.5 or less |
| 28        | 21  | +0.5 or less |
| 25        | 21  | +0.5 or less |
| 24        | 21  | +5           |
| 23        | 21  | +0.5 or less |
| 22        | 21  | +0.5 or less |
| 20        | 21  | +0.5 or less |
| 19        | 21  | +0.5 or less |
| 18        | 21  | +5           |
| 16        | 21  | +0.5 or less |
| 15        | 21  | +0.5 or less |
| 14        | 21  | +0.5 or less |
| 13        | 21  | +0.5 or less |
| 17        | 21  | +5           |

(10) Set the control-indicator to channel 2961.

(11) Check for the correct voltages between the following terminals on the command signals decoder with the multimeter.

| Terminals |     | DC<br>volts  |
|-----------|-----|--------------|
| (+)       | (-) |              |
| 24        | 21  | +0.5 or less |
| 18        | 21  | +0.5 or less |

- (12) Set the AC POWER switch to OFF, and reinstall the control-indicator cover. If abnormal indications were obtained in (7), (9), or (11) above, replace control-indicator 39A4 (para 6-18.1a, TM 11-5820-540-12) .

3-145. RF Amplifier 40AR1

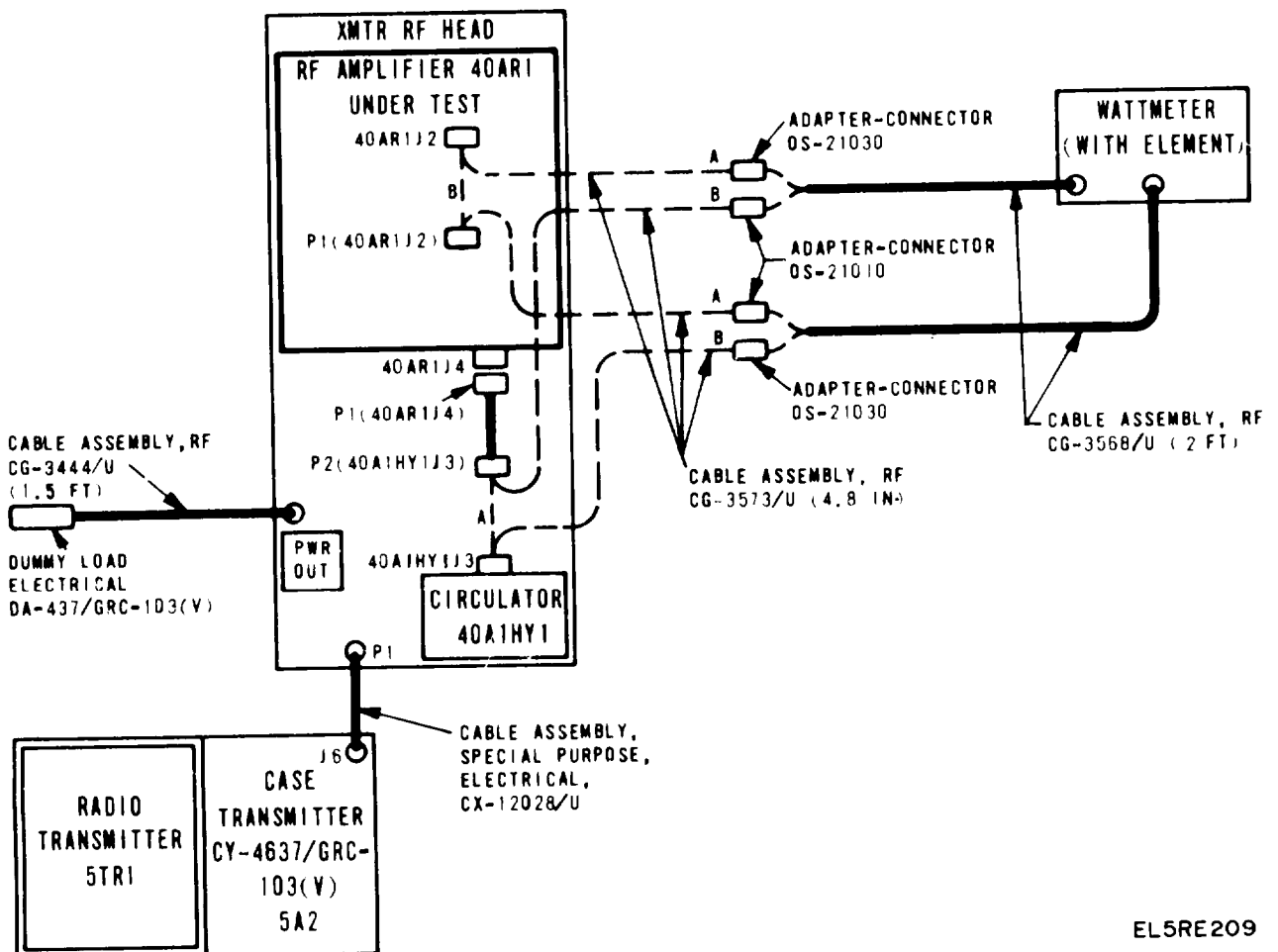
a. Test Equipment Required.

| Equipment  | Common Name |
|--|-------------|
| Wattmeter, RF, AN/USM-298  | Wattmeter   |
| Cable Assembly, RF, CG-3568/U, 2 ft.<br>(2 required)                   |             |
| Element, Wattmeter, Bird No. 433-103, 50 W,<br>Modified, 1350-1850 MHz | Element     |
| Bird No. 10K, 1100-1800 MHz  |             |
| Cable Assembly, Special Purpose,<br>Electrical                         | CX-12094/U  |
| Cable Assembly, RF, CG-3444/U, 1.5 ft.                                 |             |
| Cable Assembly, RF, CG-3573/U, 2 required                              |             |
| Adapter-Connector, OS-21010<br>(504-800054-000) 2 required             |             |
| Adapter-Connector, OS-21030<br>(504-800069-000), 2 required            |             |
| Dummy Load, Electrical, DA-437/GRC-103(V)                              | Dummy Load  |

b. Operational Check.

- (1) Remove plug P1 (40AR1J2) from 40AR1J2 on unit 40AR1 (fig. 3-91).
- (2) Connect test equipment as shown in A, figure 3-96.
- (3) Insert the 10 w element into the wattmeter.
- (4) Set the XMTR CHANNEL and XMTR TUNE controls to channel 2960.
- (5) Set the transmitter AC POWER switch to ON/RESET.
- (6) Adjust the PWR OUT PEAK control for the maximum power meter indication. The meter should indicate a minimum of 2.0 watts.
- (7) Set the AC POWER switch to OFF.
- (8) Reconnect plug P1 (40AR1J2) to 40AR1J2.
- (9) Disconnect P2 (40A1HY1J3) from 40A1HY1J3 on circulator 40A1HY1 (fig. 3-74) .

- (10) Connect the test equipment as shown in B, figure 3-96. Insert the 50 w element into the wattmeter.
- (11) Set the transmitter AC POWER switch to ON/RESET.
- (12) Adjust the PWR OUT PEAK control for the maximum wattmeter indication. The meter should read 18.5 watts minimum.
- (13) Set the AC POWER switch to OFF.
- (14) Replace the transmitter rf head if abnormal indications were obtained in (6) or (12) above (para 6-12c, TM 11-5820-540-12).



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Figure 3-96. RF Amplifier 40AR1 Operational Check, Test Setup.

3-146. Bandpass Filter 40FL1

a. Test Equipment Required.

| Equipment                                   | Common Name      |
|---|------------------|
| Power Meter NE-441/U                        | Power meter      |
| Thermistor Mount HP-478A                    | Termistor mount  |
| Attenuator, Fixed 20 dB, CN-1287/U          | 20 dB attenuator |
| Cable Assembly, Special Purpose, Electrical | CX-12094/U       |
| Cable Assembly, RF, CG-3573/U               |                  |
| Adapter-Connector OS-21010 (504-800054-000) |                  |

b. Operational Check.

- (1) Disconnect P1 (40FL1J2) from 40FL1J2 on bandpass filter 40FL1 (fig. 3-89) .
- (2) Connect the equipment as shown in figure 3-97.
- (3) Set the XMTR CHANNEL and XMTR TUNE controls to channel 2400.
- (4) Set the transmitter AC POWER switch to ON/RESET.
- (5) The power level should be +24.8 dBm minimum (power meter indication of +4.8 dBm).
- (6) Set the transmitter AC POWER switch to OFF.
- (7) Reconnect P1 (40FL1J2) to 40FL1J2 on bandpass filter 40FL1.

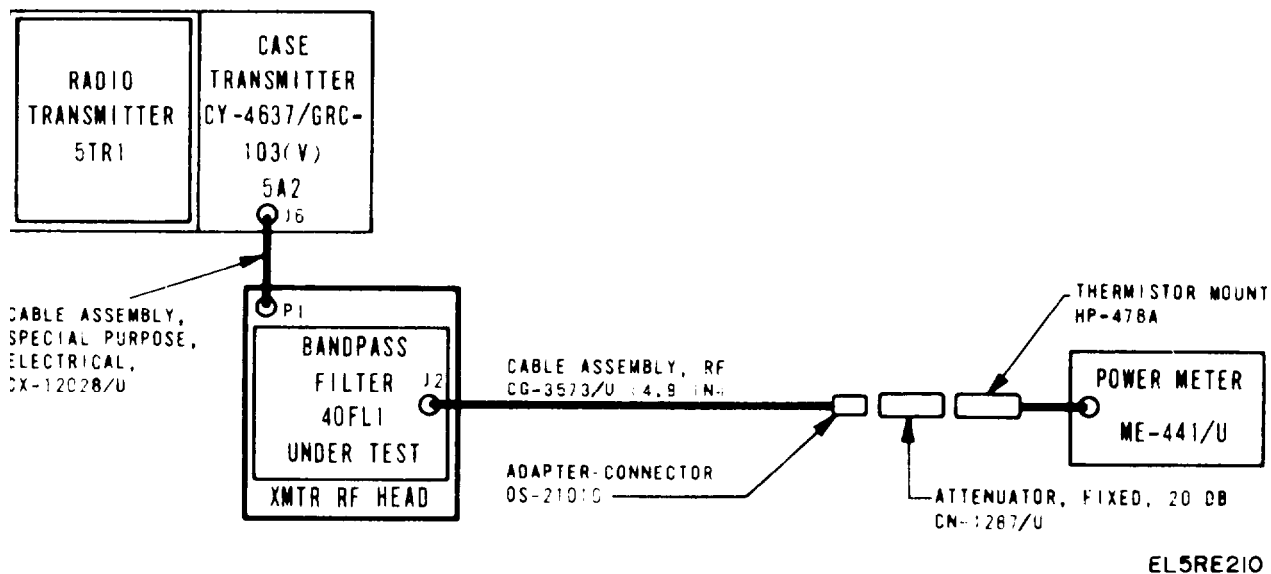


Figure 3-97. Bandpass Filter 40FL1 Operational Check, Test Setup.

- (8) Replace the transmitter rf head if abnormal indication was obtained in (5) above (chapter 6, para 6-12c, TM 11-5820-540-12).

3-147. Electronic Component Assembly 40A1

a. Test Equipment Required.

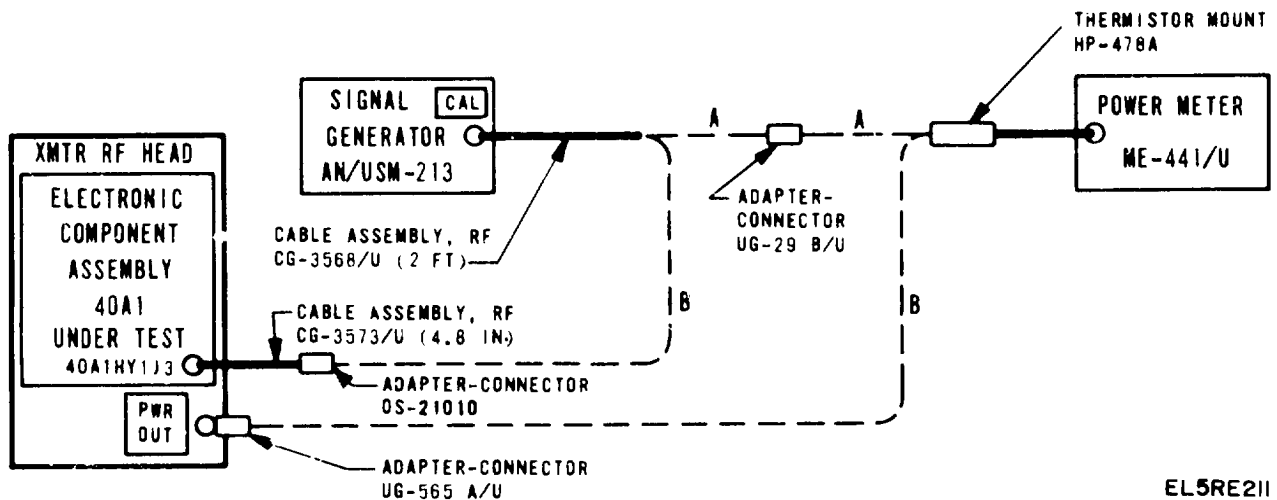
| Equipment                                      | Common Name      |
|--|------------------|
| Generator, Signal, AN/USM-213                  | Signal Generator |
| Power Meter ME-441/U                           | Power Meter      |
| Thermistor Mount HP-478A                       | Termistor Mount  |
| Cable Assembly, RF, CG-3573/U                  |                  |
| Cable Assembly, RF, CG-3568/U, 2 ft.           |                  |
| Adapter-Connector OS-21010<br>(504-800054-000) |                  |
| Adapter-Connector UG-29B/U                     |                  |
| Adapter-Connector UG-565A/U                    |                  |

b. Operational Check.

NOTE

The following test does not include isolator 40A1AT1, which must be checked separately (para 3-148).

- (1) Disconnect P2 (40A1HY1J3) from 40A1HY1J3 on circulator 40A1HY1 (fig. 3-90).
- (2) Connect the equipment as shown in A, figure 3-98.



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Figure 3-98. Electronic Component Assembly 40A1 Operational Check, Test Setup.

- (3) Set the signal generator for +8 dBm outside power at 1850 MHz (power meter indicates +8 dBm).
- (4) Connect the equipment as shown in B, figure 3-98. The power meter reading should not be more than 0.5 dB lower than the reading obtained in (3) above.
- (5) If an abnormal indication was obtained in (4) above, check the following modules:
  - (a) RF power monitor 40A1A1 (para 3-149).
  - (b) Circulator 40A1HY1 and electrical dummy load 40A1A2 (para 3-150).

3-148. Coaxial isolator 40A1AT1

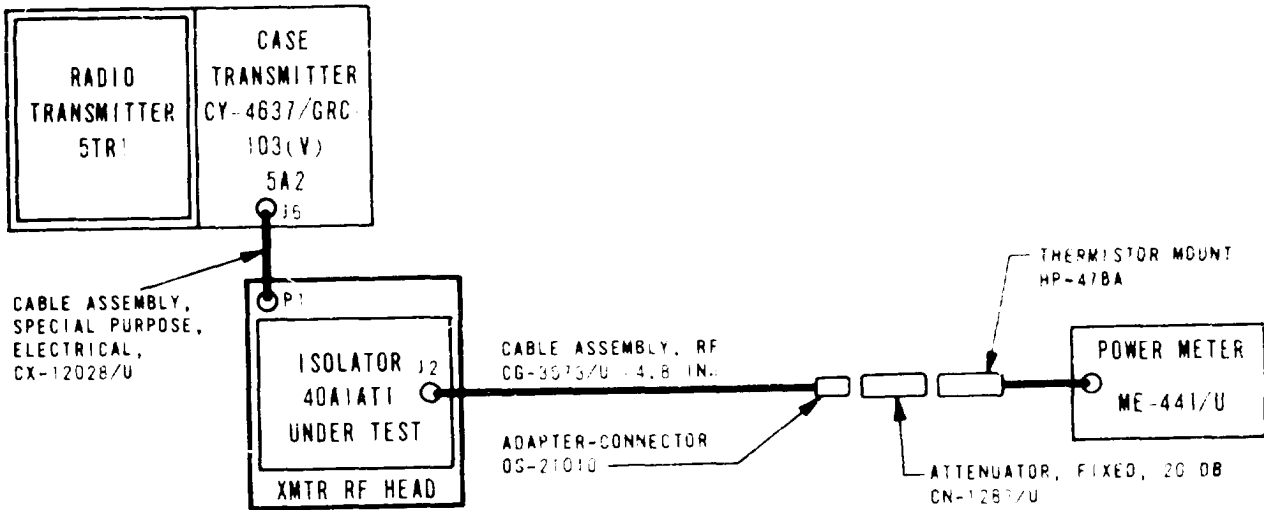
a. Test Equipment Required.

| Equipment  | Common Name   |
|--|---|
| Power Meter ME-441/U<br>Thermistor Mount HP-478A<br>Attenuator, Fixed 20 dB, CN-1287/U<br>Cable Assembly, RF, CG-3573/U<br>Cable Assembly, Special Purpose<br>Electrical<br>Adapter-Connector OS-21010<br>(504-800054-000) | Power Meter<br>Thermistor Mount<br>20 dB attenuator<br><br>CX-12094/U |

b. Operational Check

- (1) Disconnect P1 (40A1AT1J2) from 40A1AT1J2 on isolator 40A1AT1 (fig. 3-90).
- (2) Connect the equipment as shown in figure 3-99.
- (3) Set the transmitter AC POWER switch to ON/RESET.
- (4) Set the XMTR CHANNEL and XMTR TUNE controls to channel 2960. The power level should be +26.8 dBm minimum (power meter indicates 6.8 dBm ).
- (5) Set the AC POWER switch to OFF.
- (6) Reconnect P1 (40A1AT1J2) to 40A1AT1J2 on the isolator.
- (7) if an abnormal indication was obtained in (4) above, replace the coaxial isolator (para 3-167).





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Figure 3-99. Isolator 40A1A1 Operational Check, Test Setup.  
3-149. RF Power Monitor 40A1A1

a. Test Equipment Required.

| Equipment  | Common Name |
|--|-------------|
| Wattmeter, RF, AN/USM-298  | Wattmeter   |
| Element, Wattmeter, Bird No. 433-103,<br>50 W, Modified, 1350-1850 MHz | Element     |
| Dummy Load, Electrical DA-437/GRC-103(V)                               | Dummy load  |
| Cable Assembly, RF, CG-3444/U  |             |
| Cable Assembly, RF, CG-3568/U  |             |
| Adapter-Connector UC-564/U   |             |
| Adapter-Connector UG-565/U   |             |

b. Operational Check

- (1) Connect the equipment as shown in figure 3-100.
- (2) Set the XMTR CHANNEL and XMTR TUNE controls to channel 2960.
- (3) Set the transmitter AC POWER switch to ON/RESET.
- (4) Adjust the PWR OUT PEAK control for the maximum wattmeter indication.  
It should read 15 watts minimum.

(5) Set the AC POWER switch to OFF. If an abnormal Indication was obtained In (4) above, replace power monitor 40A1A1 (para 3-168).

3-150. Circulator 40A1HY1 and Electrical Dummy Load 40A1A2

a. Test Equipment Required.

| Equipment   | Common Name        |
|---|--------------------|
| Multimeter, Digital, AN/USM-486                                     | Digital Multimeter |
| Wattmeter, RF, AN/USM-298 (Band IV only)                            | Wattmeter          |
| Dummy Load, Electrical DA-437/GRC-103(V)                            | Dummy load         |
| Cable Assembly, Special Purpose Electrical                          | CX-12094/U         |
| Cable Assembly, RF, CG-3573/U                                       |                    |
| Cable Assembly, RF, CG-3568/U                                       |                    |
| Cable Assembly, RF, CG-3444/U                                       |                    |
| Adapter-Connector OS-21010 (504-800054-000)                         |                    |
| Adapter-Connector UG-564A/U   |                    |
| Element, Wattmeter, Bird No. 433-103, 50 W, Modified, 1350-1850 MHz | Element            |

b. Operational Check.

(1) Set the transmitter AC POWER switch to OFF.

(2) Set the multimeter to the RX1 scale.

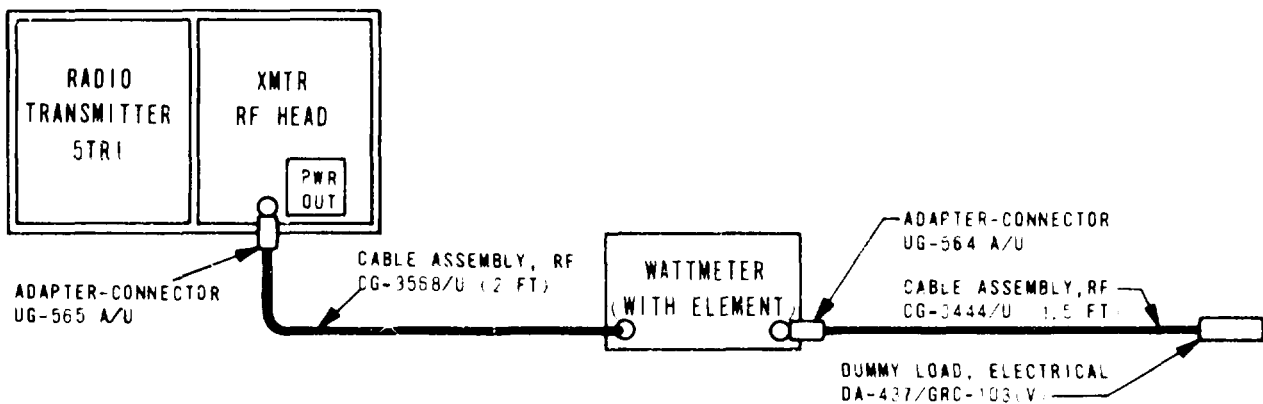
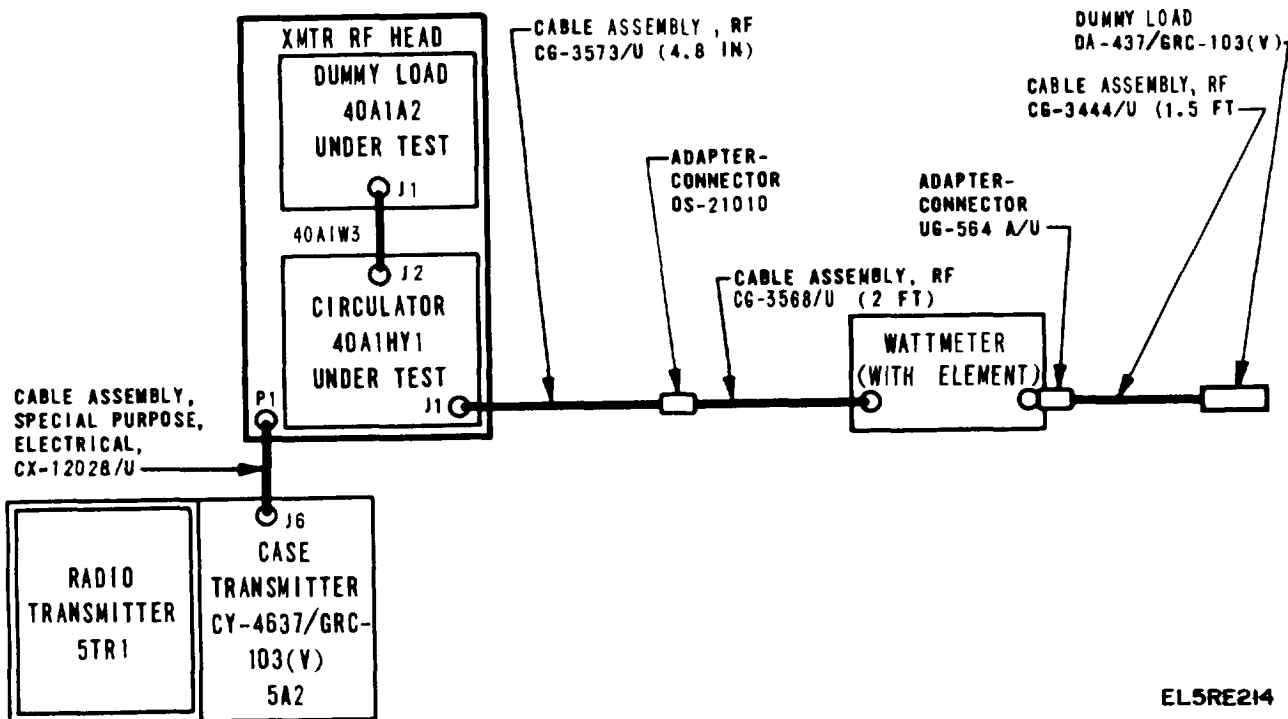


Figure 3-100. RF Power Monitor 40A1A1 Operational Check, Test Setup.

- (3) Connect the multimeter between the center and outer conductors of PWR CUT connector 40A1A1J2 on the front panel of the transmitter rf head. If a reading of 45 to 55 ohms is not obtained, replace dummy load 40A1A2 (para 3-161) and check circulator 40A1HY1 as indicated in (4) through (12) below.
- (4) Disconnect P1 (40A1HY1J1) from 40A1HY1J1 on circulator 40A1HY1 (fig. 3-90).
- (5) Connect the equipment as shown in figure 3-101.
- (6) Set the XMTR CHANNEL and XMTR TUNE controls to channel 2960.
- (7) Insert the element into the wattmeter.
- (6) Set the transmitter AC POWER switch to ON/RESET.
- (9) Adjust the PWR OUT PEAK control for the maximum wattmeter indication. The meter should indicate a minimum of 16 watts.
- (10) Set the AC POWER switch to OFF.
- (11) Reconnect plug P1 (40A1HY1J1) to 40A1HY1J1 on circulator 40A1HY1.
- (12) If an abnormal indication was obtained in (9) above, replace the circulator 40A1HY1 (para 3-171).



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Figure 3-101. Circulator 40A1HY1 and Electrical Load 40A1A2 Operational Check, Test Setup.

3-151. Electronic Frequency Converter 39A2

a. Test Equipment Required.

| Equipment   | Common Name  |
|---|--|
| Generator, Signal, AN/USM-213<br>Power Meter ME-441/U<br>Thermistor Mount HP-478A<br>Cable Assembly, Special Purpose Electrical<br>Cable Assembly, RF, CG-3568/U, 2 ft.<br>Cable Assembly, RF, CG-3573/U<br>Adapter-Connector, UG-201A/U<br>Adapter-Connector, UG-565A/U<br>Adapter-Connector, OS-21010 (504-800054-000)<br>Adapter-Connector, OS-20200-2<br>Attenuator, Fixed, 10 dB, CN-1286/U<br>Voltmeter, RF, ME-426/U | Signal Generator<br>Power Meter<br>Thermistor Mount<br>CX-12097/U<br><br><br><br><br>10 dB attenuator<br>RF, Voltmeter |

- (1) Connect the equipment as shown in A1, figure 3-102).
- (2) Tune the receiver to channel 3000. Set the signal generator to 1700 MHz.
- (3) Set the receiver AC POWER switch to ON.
- (4) Increase the signal generator output level until the high signal arm operates (buzzer may sound if not muted). The signal generator output level should not exceed +15 dBm. (The power meter should indicate +5 dBm maximum when connected as in A2.)
- (5) Set the AC POWER switch to OFF.
- (6) Disconnect P2 (390A1W1A1) from 39A2J2 on IF amplifier 39AR2 (fig. 3-92).
- (7) Connect the equipment as shown in B, figure 3-102.
- (8) Set the signal generator output level to -80 dBm.
- (9) Set the AC POWER switch to ON. The RF voltmeter should indicate between -28 dBm and -22 dBm.
- (10) Set the AC POWER switch to OFF.
- (11) Reconnect P2 (39A1N1A1) to 39AR2J1 on IF amplifier 39AR2.
- (12) If an abnormal indication was obtained in (4) or (9) above, replace electronic frequency converter 39A2 (para 3-172).

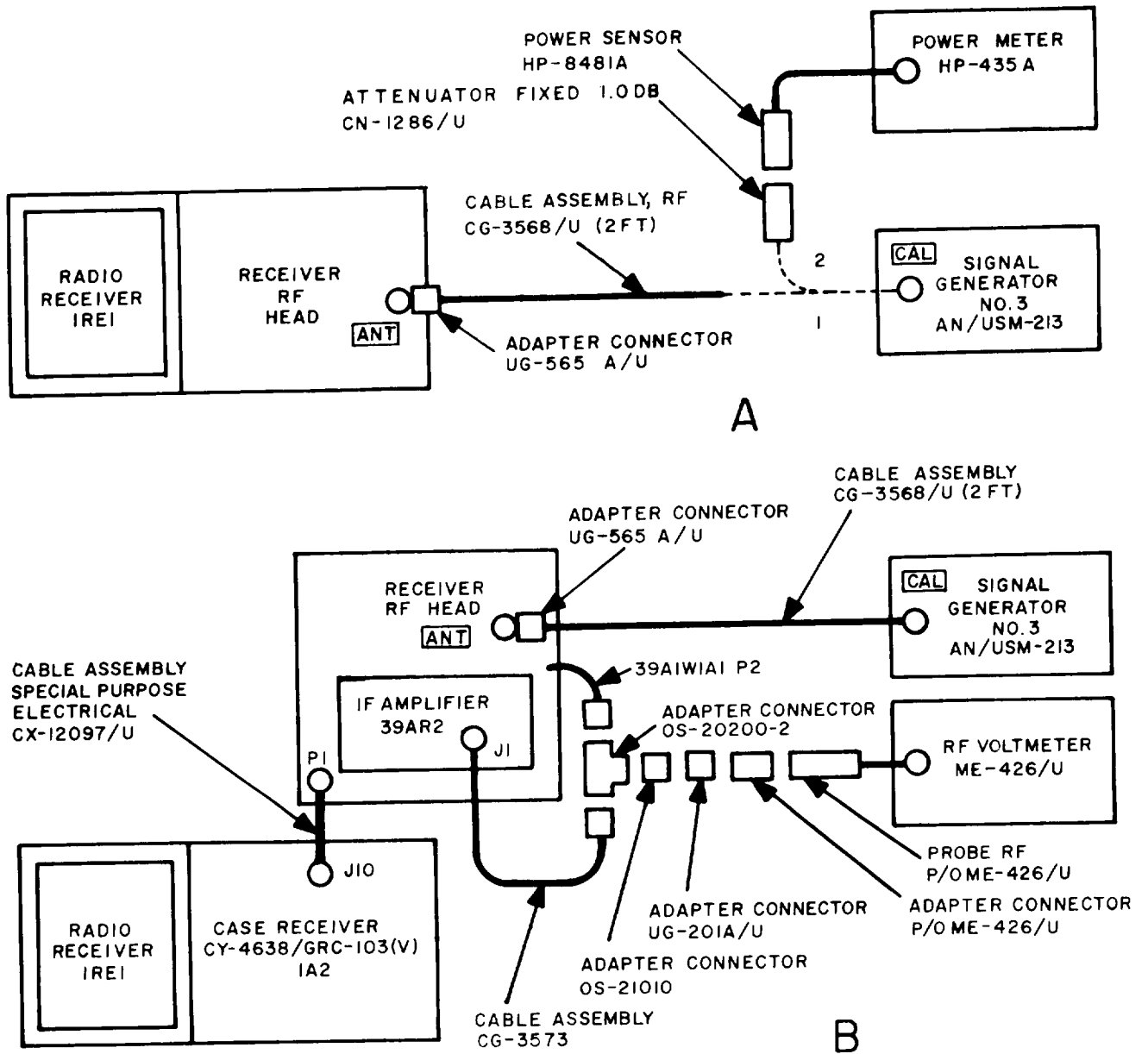


Figure 3-102. Electronic Frequency Converter 39A2 Operational Check, Test Setup.

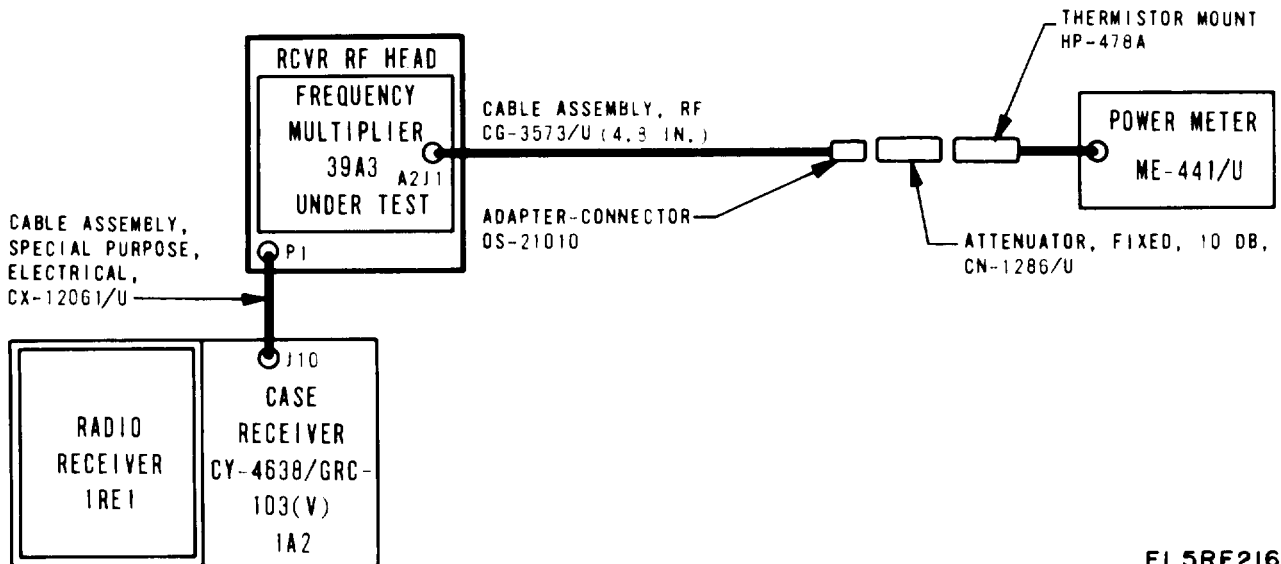
3-152. Frequency Multiplier 39A3

a. Test Equipment Required.

| Equipment   | Common Name   |
|---|---|
| Power Meter ME-441/U<br>Thermistor Mount HP-478A<br>Attenuator, Fixed 10 dB, CN-1286/U<br>Cable Assembly, Special Purpose, Electrical<br>Cable Assembly, RF, CG-3573/U<br>Adapter-Connector OS-21010 (504-800054-000) | Power Meter<br>Thermistor Mount<br>10 dB attenuator<br>CX-12097/U |

12. Operational Check.

- (1) Disconnect P1 (39A3A2J1) from 39A3A2J1 on frequency multiplier 39A3 (fig. 3-93).
- (2) Connect the equipment as shown in figure 3-103.
- (3) Set the RCVR CHANNEL and RCVR SIG controls to channel 2899.
- (4) Set the receiver AC POWER switch to ON, and adjust the MULT PEAK control for the maximum power meter indication. The power level should be +10 dBm minimum (power meter indicates 0 dBm).
- (5) Set the RCVR CHANNEL and RCVR SIG controls to channel 2900.



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Figure 3-103. Frequency Multiplier 39A3 Operational Check, Test Setup.

- (6) Adjust the MULT PEAK control for the maximum power meter indication. The meter should indicate +12 dbm ( $\pm 4$  db).
- (7) Set the AC POWER switch to OFF. If an abnormal indication was obtained in (4) or (6) above, replace the receiver rf head (para 6-12c, TM 11-5820-540-12).

3-153. Control-Indicator 39A4

a. Test Equipment Required.

| Equipment  | Common name                      |
|--|----------------------------------|
| Multimeter, Digital, AN/USM-486<br>Cable Assembly, Special Purpose<br>Electrical | Digital Multimeter<br>CX-12097/U |

a. Operational Check.

- (1) Set the control-indicator to channel 2612.
- (2) Remove control-indicator 39A4 from the receiver rf head (para 6-18.1a, TM 11-5820-540-12).
- (3) Remove the four screws securing the control-indicator cover. Remove the cover.
- (4) Reconnect plug P1 (39A1W1J2) to chassis connector 39A1W1J2 (fig. 3-93).
- (5) Connect the receiver rf head to the receiver case, using cable CX-12061/U (1 ft. 3 in.). Set the AC POWER switch to ON.
- (6) Make sure the control-indicator is set to channel 2612.
- (7) Check for the correct voltage between the following terminals on the command signals decoder with the multimeter.

| Terminals |     | DC<br>volts |
|-----------|-----|-------------|
| (+)       | (-) |             |
| 29        | 21  | +5          |
| 28        | 21  | +5          |
| 25        | 21  | +5          |
| 24        | 21  | +10         |
| 23        | 21  | +5          |
| 22        | 21  | +5          |

| Terminals |    | DC volts     |
|-----------|----|--------------|
| 20        | 21 | +5           |
| 19        | 21 | +5           |
| 18        | 21 | +5           |
| 16        | 21 | +5           |
| 15        | 21 | +5           |
| 13        | 21 | +5           |
| 14        | 21 | +0.5 or less |
| 17        | 21 | +0.5 or less |

(8) Set the control-indicator to channel 2611.

(9) Check for correct voltages between the following terminals on the command signals decoder with the multimeter.

| Terminals |     | DC volts     |
|-----------|-----|--------------|
| +         | (-) |              |
| 29        | 21  | +0.5 or less |
| 28        | 21  | +0.5 or less |
| 25        | 21  | +0.5 or less |
| 24        | 21  | +5           |
| 23        | 21  | +0.5 or less |
| 22        | 21  | +0.5 or less |
| 20        | 21  | +0.5 or less |
| 19        | 21  | +0.5 or less |
| 18        | 21  | +5           |
| 16        | 21  | +0.5 or less |
| 15        | 21  | +0.5 or less |
| 14        | 21  | +0.5 or less |
| 13        | 21  | +0.5 or less |
| 17        | 21  | +5           |

(10) Set the control-indicator to channel 2901.

(11) Check for correct voltages between the following terminals on the command signals decoder with the multimeter.

| Terminals |     | DC volts     |
|-----------|-----|--------------|
| +         | (-) |              |
| 24        | 21  | +0.5 or less |
| 18        | 21  | +0.5 or less |



- (12) Set the AC POWER switch to OFF, and reinstall the control-indicator cover. If abnormal indications were obtained in (7), (9) or (11) above, replace control-indicator 39A4 (para 6-18.1a, TM 11-5820-540-12).

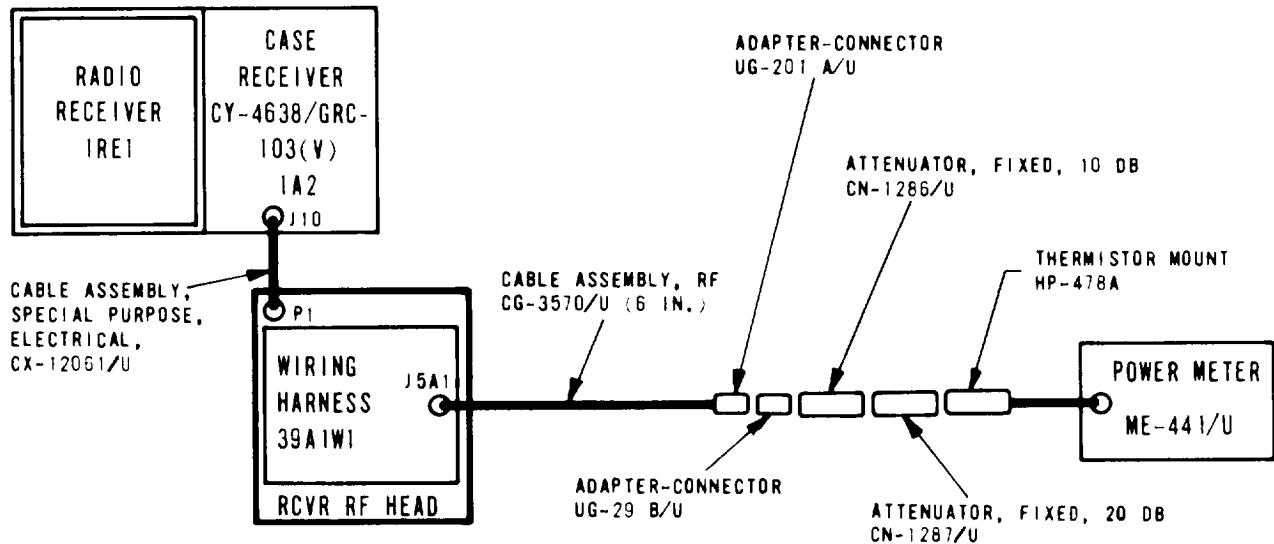
3-154. RF Amplifier 39AR1

a. Test Equipment Required.

| Equipment                                   | Common Name      |
|---|------------------|
| Power Meter ME-441/U                        | Power Meter      |
| Thermistor Mount HP-478A                    | Thermistor Mount |
| Attenuator, Fixed 20 dB, CN-1287/U          | 20 dB attenuator |
| Attenuator, Fixed 10 dB, CN-1286/U          | 10 dB attenuator |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U       |
| Cable Assembly, RF, CG-3570/U               |                  |
| Adapter-Connector UG-201A/U                 |                  |
| Adapter-Connector UG-29B/U                  |                  |

b. Operational check.

- (1) Remove frequency multiplier 39A3 (fig. 3-93) as follows:
  - (a) Rotate the RCVR SIG and MULT PEAK controls fully clockwise.
  - (b) Lock the drive shaft of frequency multiplier 39A3 with the locking clamp provided.
  - (c) Disconnect plug P1 (39A3A2J1) from 39A3A2J1 on frequency multiplier 39A3.
  - (d) Remove the three red-circled mounting screws that secure frequency multiplier 39A3. Lift the module carefully, disengaging the drive shaft from the flexible coupling as well as the mating connector.
- (2) Connect the equipment as shown in figure 3-104.
- (3) Set the RCVR CHANNEL control to channel 2900.
- (4) Set the receiver AC POWER switch to ON. The power meter should indicate -0.5 dBm minimum (+29.5 dBm output from the unit under test).
- (5) Set the AC POWER switch to OFF.
- (6) Replace frequency multiplier 39A3, reversing the removal procedure outlined in (1) above.
- (7) If an abnormal indication was obtained in (4) above, replace rf amplifier 39AR1 (para 6-18.1c, TM 11-5820-540-12).



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Figure 3-104. RF Amplifier 39AR1 Operational Check, Test Setup.

3-155. IF Amplifier 39AR2

a. Test Equipment Required.

| Equipment                                   | Common Name       |
|---|-------------------|
| Generator, Signal, SG-1170/U                | Signal Generator  |
| Power Meter ME-441/U                        | Power Meter       |
| Thermistor Mount HP-478A                    | Thermistor Mount  |
| Cable Assembly, Special Purpose Electrical  | CX-12097/U        |
| Cable Assembly, RF, CG-3568/U, 2 ft.        |                   |
| Cable Assembly, RF, CG-3570/U               | CG-3570/U (6 in.) |
| Cable Assembly, RF, CG-3573/U               |                   |
| Adapter-Connector UG-29B/U                  |                   |
| Adapter-Connector UG-201A/U                 |                   |
| Adapter-Connector OS-20200-2                |                   |
| Adapter-Connector OS-21010 (504-800054-000) |                   |
| Voltmeter, RF, ME-426/U                     | RF Voltmeter      |

b. Operational Check.

- (1) Remove frequency converter 39A2 (para 3-172).
- (2) Disconnect plug P2 (39A1W1A1) from 39AR2J1 on if amplifier 39AR2 (fig. 3-92).
- (3) Connect the equipment as shown in figure 3-105.

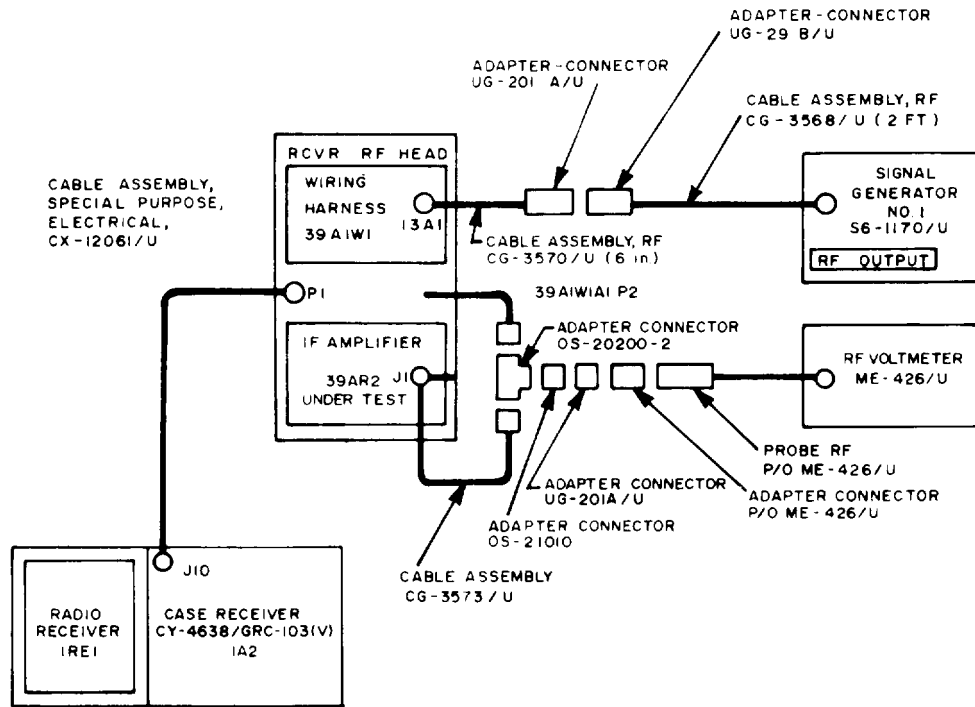


Figure 3-105. IF Amplifier 39AR2 Operational Check, Test Setup.

- (4) Set the signal generator frequency to 30 MHz, at an output level of -75 dBm.
- (5) Set the receiver AC POWER switch to ON. The RF Voltmeter should Indicate between -28 dBm and -22 dBm.
- (6) Set the AC POWER switch to OFF.
- (7) Reconnect plug P2 (39A1W1A1) to 39AR2J1 on IF amplifier 39AR2.
- (8) Reinstall frequency converter 39A2 (para 3-173).
- (9) If an abnormal Indication was obtained in (5) above, replace IF amplifier 39AR2 (para 3-176).

3-156. Bandpass Filter 39FL1

a. Test Equipment Required.

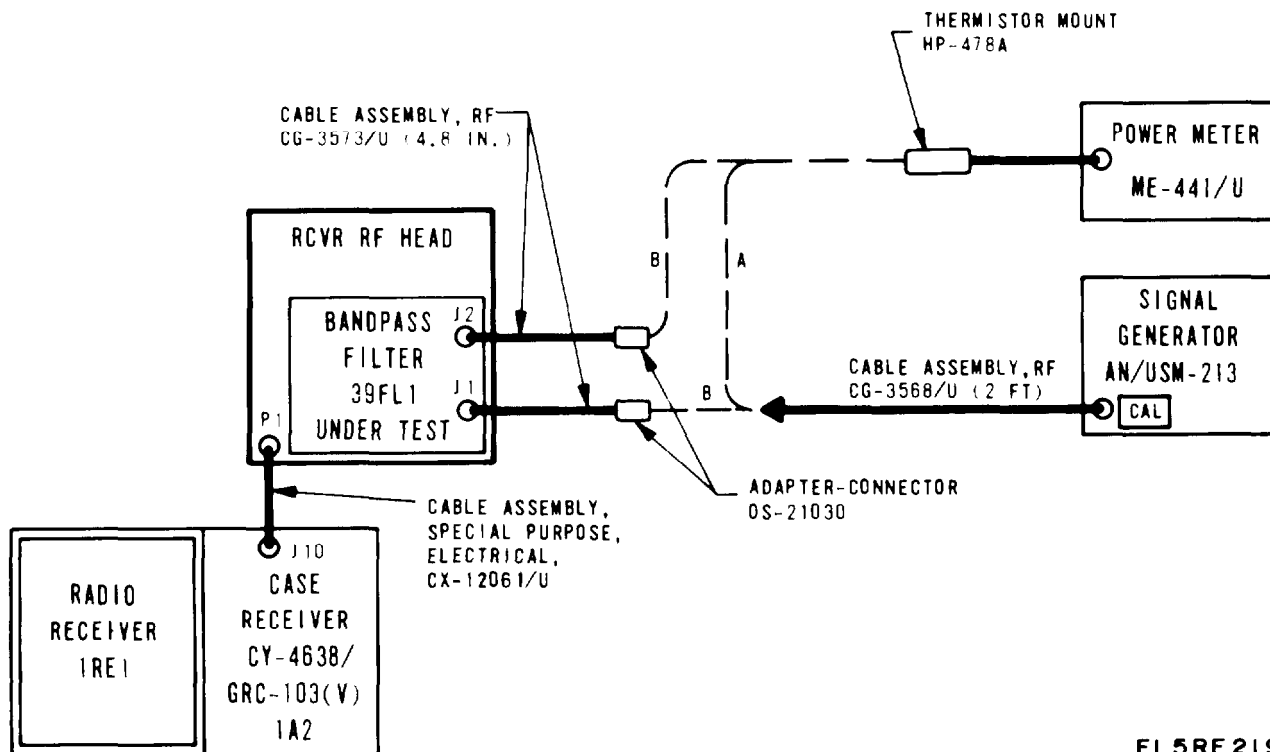
| Equipment  | Common Name      |
|--|------------------|
| Generator, Signal, AN/USM-213                      | Signal Generator |
| Power Meter ME-441/U                               | Power Meter      |
| Cable Assembly, Special Purpose, Electrical        | CX-12097/U       |
| Cable Assembly, RF, CG-3573/U 4.8 in. (2 required) |                  |
| Cable Assembly, RF, CG-3568/U                      |                  |

a. Test Equipment Required - Continued.

| Equipment   | Common Name      |
|---|------------------|
| Adapter-Connector CS-21030<br>(504-800069-0C0) (2 required)<br>Thermistor Mount HP-478A | Thermistor Mount |

b. Operational Check

- (1) Disconnect P2 (39FL1J1) from 39FL1J1 and P1 (39FL1J2) from 39FL1J2 on bandpass filter 39FL1 (fig. 3-94).
- (2) Connect the equipment as shown in A, figure 3-106.
- (3) Set the signal generator to 1850 MHz and adjust the output level for an indication of +5 dBm on the power meter.
- (4) Connect the equipment as shown in B, figure 3-106. Set REC SIG control to channel 3300.
- (5) Tune the REC SIG control for maximum power meter indication. The power meter should indicate not less than +3.0 dBm.
- (6) Reconnect P2 (39FL1J1) to 39FL1J1 and P1 (39FL1J2) to 39FL1J2.



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Figure 3-106. Bandpass Filter 39FL1 Operational Check, Test Setup.

(7) If an abnormal indication was obtained in (5) above, replace the receiver rf head (para 6-12c, TM 11-5820-540-12).

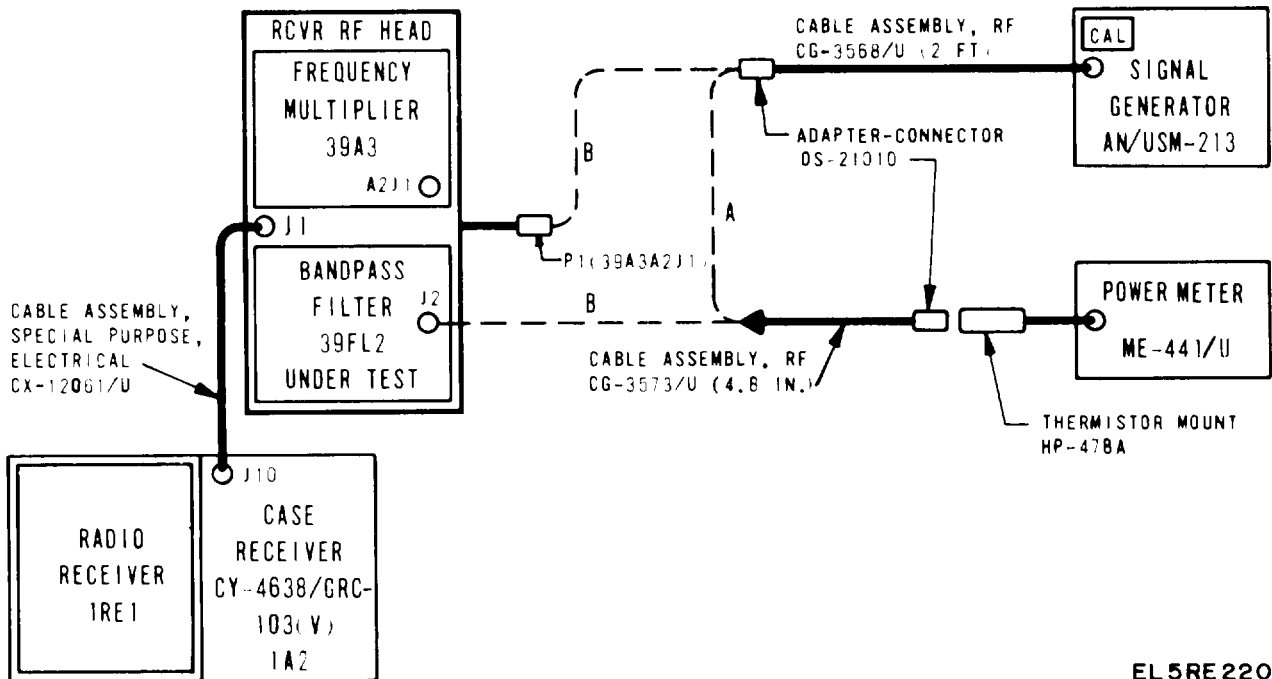
3-157. Bandpass Filter 39FL2

a. Test Equipment Required.

| Equipment                                   | Common Name      |
|---|------------------|
| Generator, Signal, AN/USM-213               | Signal Generator |
| Power Meter ME-441/U                        | Power Meter      |
| Thermistor Mount HP-478A                    | Thermistor Mount |
| Cable Assembly, Special Purpose, Electrical | CX-12097/U       |
| Cable Assembly, RF, CG-3573/U               |                  |
| Adapter-Connector OS-21010 (504-800054-000) |                  |

b. Operational Check.

- (1) Disconnect P1 (39A3A2J1) from 39A3A2J1 on frequency multiplier 39A3 (fig. 3-93).
- (2) Connect the equipment as shown in A, figure 3-107.
- (3) Set the RCVR CHANNEL and RCVR SIG controls to channel 2900.



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Figure 3-107. Bandpass Filter 39FL2 Operational Check, Test Setup.

- (4) Set the signal generator to 1680 MHz.
- (5) Set the signal generator for a power meter indication of 0 dBm.
- (6) Remove cable 39W4 from 39FL2J2 on bandpass filter 39FL2 (fig. 3-92).
- (7) Connect the equipment as shown in B, figure 3-107.
- (8) Tune MULT PEAK control for maximum indication on power meter. Power meter should indicate not less than -2.0 dBm.
- (9) Reconnect cable 39W4 to 39FL2J2 of bandpass filter 39FL2 and P1 (39A3A2J1) to 39A3A3J1.
- (10) If an abnormal indication was obtained in (7) above, replace the receiver rf head (para 6-12c, TM 11-5820-540-12).

3-158. Bandpass Filter 39FL3

a. Test Equipment Required.

| Equipment   | Common Name          |
|---|----------------------|
| Wattmeter, RF, AN/USN-298 (Band IV only)<br>Element, Wattmeter, Bird No. 25K<br>1100-1800 MHz | Wattmeter<br>Element |
| Dummy Load, Electrical DA-437/GRC-103(V)  | Dummy Load           |
| Cable Assembly, Special Purpose,<br>Electrical  | CX-12097/U           |
| Cable Assembly, RF, CG-3573/U<br>(2 required)   |                      |
| Cable Assembly, RF, CG-3568/U, 2 ft.<br>(2 required)  |                      |
| Cable Assembly, RF, CG-3444/U, 1.5 ft.  |                      |
| Adapter-Connector OS-21010<br>(504-800054-000) (2 required)                                   |                      |
| Adapter-Connector UG-564A/U   |                      |
| Adapter-Connector UG-565A/U   |                      |

b. Operational Check.

- (1) Disconnect P2 (39FL3J2) from plug P1 (39FL3J1) from 39FL3J2 and 39FL3J1 respectively (figs. 3-92 and 3-101).
- (2) Connect the equipment as shown in figure 3-108.
- (3) Set the XMTR CHANNEL, XMTR TUNE, and XMTR DUPL controls to channel 2960.
- (4) Set the transmitter AC POWER switch to ON/RESET.

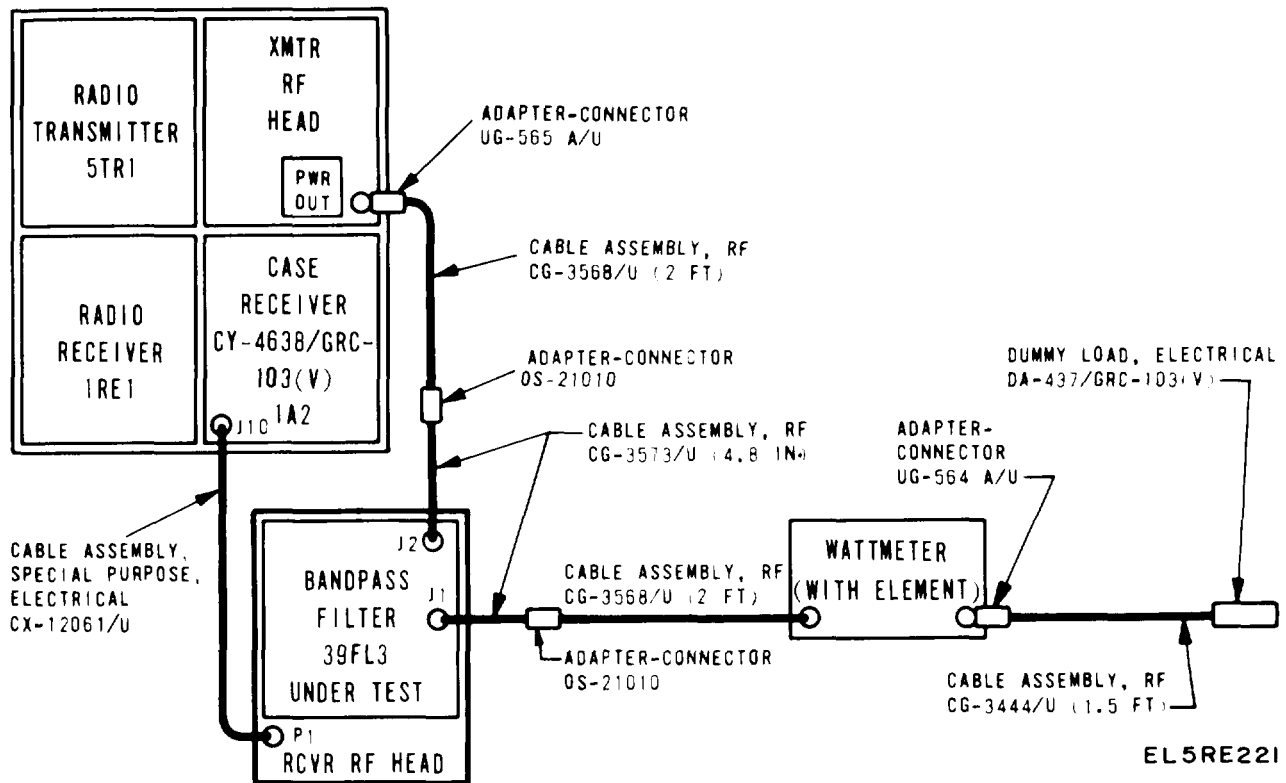


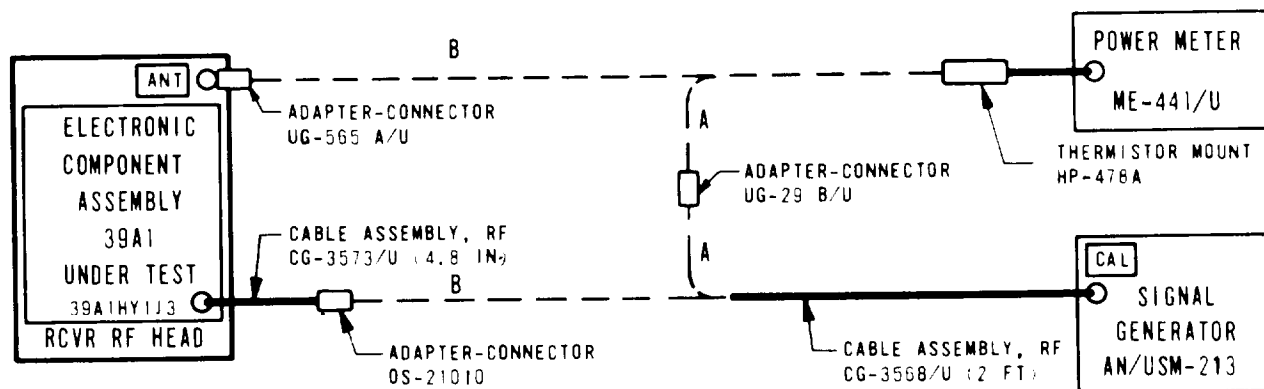
Figure 3-108. Bandpass Filter 39FL3 Operational Check, Test Setup.

- (5) Adjust the XMTR DUPL and PWR OUT PEAK controls for the maximum wattmeter indication. The meter should read 12 watts minimum.
- (6) Set the AC POWER switch to OFF. If an abnormal indication was obtained in (5) above, replace the receiver rf head (para 6-12c, TM 11-5820-540-12) .

3-159. Electronic Component Assembly 39A1

a. Test Equipment Required.

| Equipment                                      | Common Name      |
|--|------------------|
| Generator, Signal, ANN/USM-213                 | Signal Generator |
| Power Meter ME-441/U                           | Power Meter      |
| Thermistor Mount HP-478A                       | Thermistor Mount |
| Cable Assembly, RF, CG-3568/U, 2 ft.           |                  |
| Cable Assembly, RF, CG-3573/U                  |                  |
| Adapter-Connector OS-21010<br>(504-800054-000) |                  |
| Adapter-Connector UG-29B/U                     |                  |
| Adapter-Connector UG-565A/U                    |                  |



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Figure 3-109. Electronic Component Assembly 39A1 Operational Check, Test Setup.

b. Operational Check.

- (1) Disconnect P2 (39A1HY1J3) from 39A1HY1J3 on circulator 39A1HY1 (fig. 3-92).
- (2) Connect the equipment as shown in A, figure 3-109.
- (3) Set the signal generator for +8 dBm output power at 1850 MHz (power meter indicates +8 dBm).
- (4) Connect the equipment as shown in B, figure 3-109. The power meter reading should not be more than 0.5 dB lower than the reading recorded in (3) above.
- (5) If an abnormal indication was obtained in (4) above, check the following modules.
  - (a) RF power monitor 39A1A1 (para 3-160).
  - (b) Circulator 39A1HY1 (para 3-161).

3-160. RF Power Monitor 39A1A1

a. Test Equipment Required.

| Equipment   | Common Name |
|---|-------------|
| Wattmeter, RF, AN/USM-298 (Band IV only)          | Wattmeter   |
| Element, Wattmeter, Bird No. 25K<br>1100-1800 MHz | Element     |
| Dummy Load, Electrical DA-437/GRC-103(V)          | Dummy Load  |



a. Test Equipment Required - Continued.

| Equipment   | Common name |
|---|-------------|
| Cable Assembly, Rf CG-3568/U, 2 ft.<br>Cable Assembly, Rf CG-3444/U, 1.5 ft.<br>Cable Assembly, Rf CG-3569/U, 2 ft.<br>Adapter-Connector UG-565 A/U |             |

b. Operational Check.

- (1) Connect the equipment as shown in figure 3-110.
- (2) Set the XMTR CHANNEL, XMTR TUNE and XMTR DUPL controls to channel 2960.
- (3) Set the RCVR SIG control to channel 2900.
- (4) Set the transmitter AC POWER switch to ON/RESET.
- (5) Set the XMTR DUPL and PWR OUT PEAK controls for the maximum wattmeter indication. The meter should read 9 watts minimum.
- (6) Set the transmitter AC POWER switch to OFF.
- (7) If an abnormal indication was obtained in (5) above, replace the rf power monitor 39A1A1 (para 3-184).

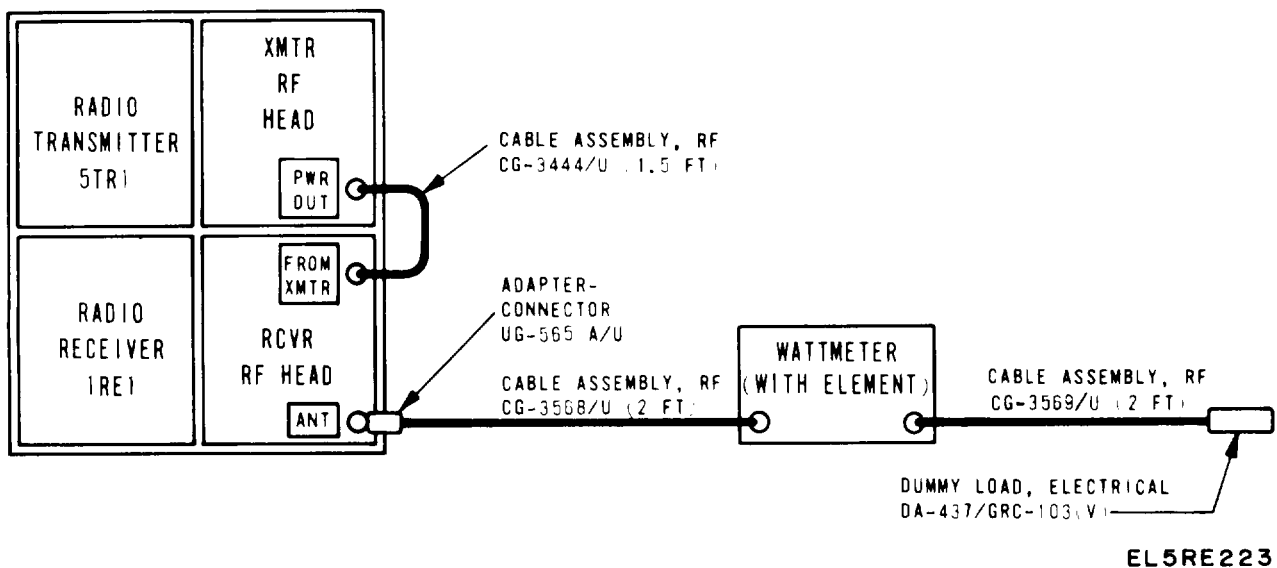


Figure 3-110. RF Power Monitor 39A1A1 Operational Check, Test Setup.

3-161. Circulator 39A1HY1

a. Test Equipment Required.

| Equipment  | Common Name                  |
|--|------------------------------|
| Wattmeter, RF, AN/USM-298 (Band IV only)<br>Element, Wattmeter, Bird No. 25K<br>1100-1800 MHz    | Wattmeter<br>Element         |
| Dummy Load, Electrical DA-437/GRC-103(V)<br>Cable Assembly, RF, CG-3568/U, 2 ft.<br>(2 required) | Dummy Load                   |
| Cable Assembly, Special Purpose,<br>Electrical   | CX-12097/U                   |
| Cable Assembly, RF, CG-3444/U (3.5 ft.)  |                              |
| Cable Assembly, RF, CG-3573/U<br>(2 required)  |                              |
| Adapter-Connector UG-29B/U   |                              |
| Adapter-Connector UG-565A/U  |                              |
| Adapter-Connector OS-21010<br>(504-800054-000)   |                              |
| Adapter-Connector OS-21030   |                              |
| Attenuator, Fixed, 10 dB, CN-1286/U  | 10 dB attenuator             |
| Attenuator, Fixed, 20 dB, CN-1287/U  | 20 dB attenuator             |
| Thermistor Mount HP-478A   | Thermistor Mount             |
| Power Meter ME-441/U with Thermistor<br>Mount HP-478A  | Power Meter Thermistor Mount |

b. Operational Check.

- (1) See figure 3-93 and remove control-indicator 39A4 from the receiver rf head (para 6-18.1a TM 11-5820-540-12).
- (2) Disconnect P2 (39A1HY1J1) from 39A1HY1J1 on circulator 39A1HY1 (FO-4-73) .
- (3) Connect the equipment as shown in A, figure 3-111.
- (4) Set the XMTR CHANNEL, XMTR TUNE and XMTR DUPL controls to channel 2960.
- (5) Set the RCVR SIG control to channel 2900.
- (6) Insert the element into the wattmeter.
- (7) Set the transmitter AC POWER switch to ON/RESET.
- (8) Adjust the XMTR DUPL and PWR OUT PEAK controls for the maximum wattmeter indication. The meter should read 11 watts minimum.

- (9) Set the AC POWER switch to OFF.
- (10) Disconnect test cable CG-3573/U from J1 on the circulator. Reconnect plug P2 (39A1HY1J1) from 39A1HY1J1.
- (11) Disconnect plug P1 (39A1HY1J2) from 39A1HY1J2 and plug P2 (39A1HY1J3) from 39A1HY1J3 on circulator 39A1HY1.
- (12) Disconnect plug P1 (39FL3J1) from 39FL3J1 on bandpass filter 39FL3. Connect the test equipment as shown in figure 3-111.

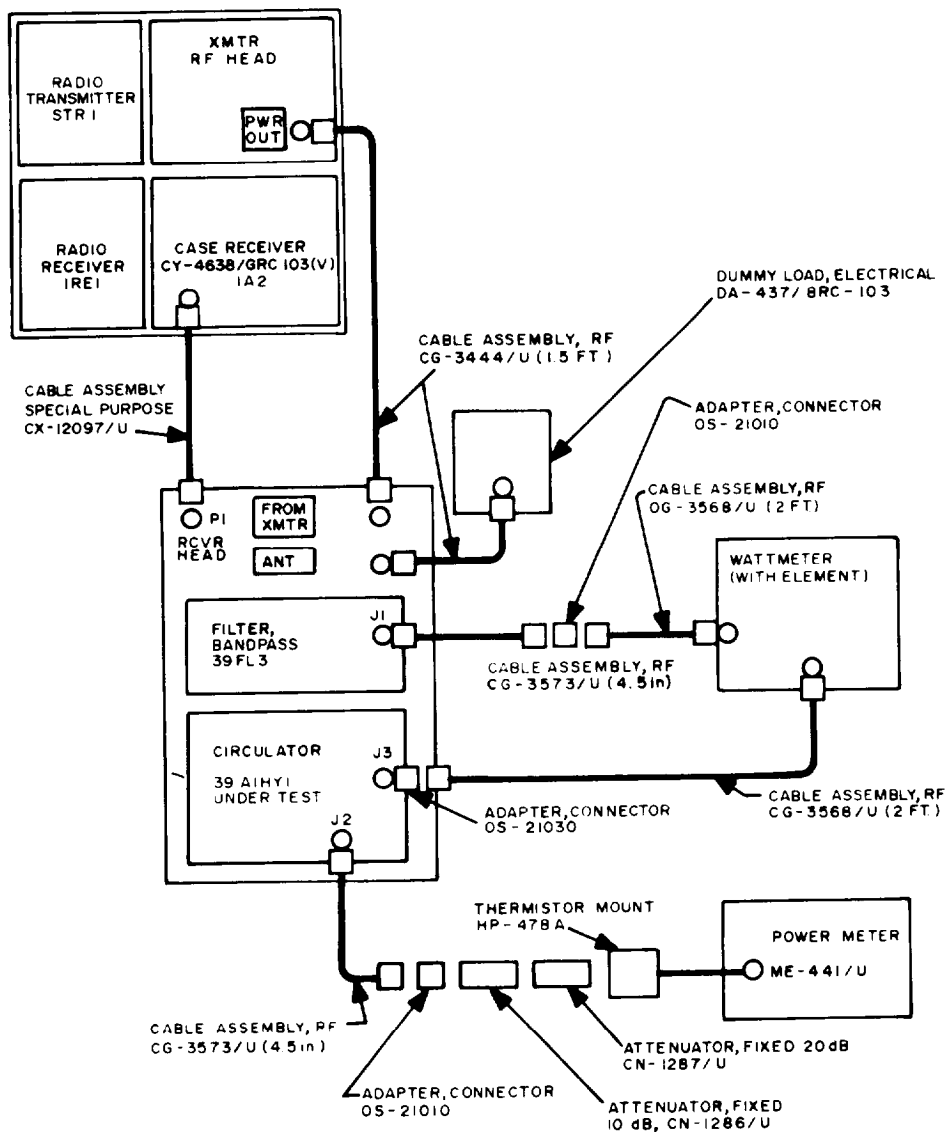


Figure 3-111. Circulator 39A1HY1 Operational Check, Test Setup.

- (13) Set the transmitter AC POWER switch to ON/RESET.
- (14) Adjust XMTR DUPL and PWR CUT PEAK controls for a 12 watt indication on the wattmeter.
- (15) Note the power meter indication. It should not be more than +25 dBm (power meter indication of -5 dBm).
- (16) Set the AC POWER switch to OFF.
- (17) Reconnect plug PI (39A1HY1J2) to 39A1HY1J2 and plug P2 (39A1HY1J3) to 39A1HY1J3 on the circulator, and reconnect plug PI (39FL3J1) to 39FL3J1.
- (18) Reinstall control-indicator 39A4 in the receiver RF head (chapter 6, para 6-18.1a, TM 11-5820-540-12).
- (19) If an abnormal indication was obtained in (8) or (15) above, replace the receiver RF head (chapter 6, para 6-12c, TM 11-5820-540-12).

3-162. Antenna AS-3047/GRC-103(V), Unit 41

a. Test Equipment Required.

| Equipment                        | Common Name        |
|----------------------------------|--------------------|
| Multi meter, Digital, AN/USM-486 | Digital Multimeter |

h. Operational Check.

- (1) Check that there is no mechanical damage at the following points:
  - (a) Antenna Feed 41A1.
  - (b) Reflector 41A2.
  - (c) Adapter-Connector MS 90579-1375.
  - (d) RF Cable Assemblies CG-3443/U and CG-3444/U.
- (2) Check Adapter-Connector MS 90579-1375, CG-3443/U, and CG-3444/U for continuity or short circuit between inner and outer conductors.
- (3) Check the Antenna Feed as described in paragraph 3-163.
- (4) If an abnormal indication was obtained in 1 (2), or (3) above, replace the defective component. If the antenna is still inoperative, higher category maintenance is required.

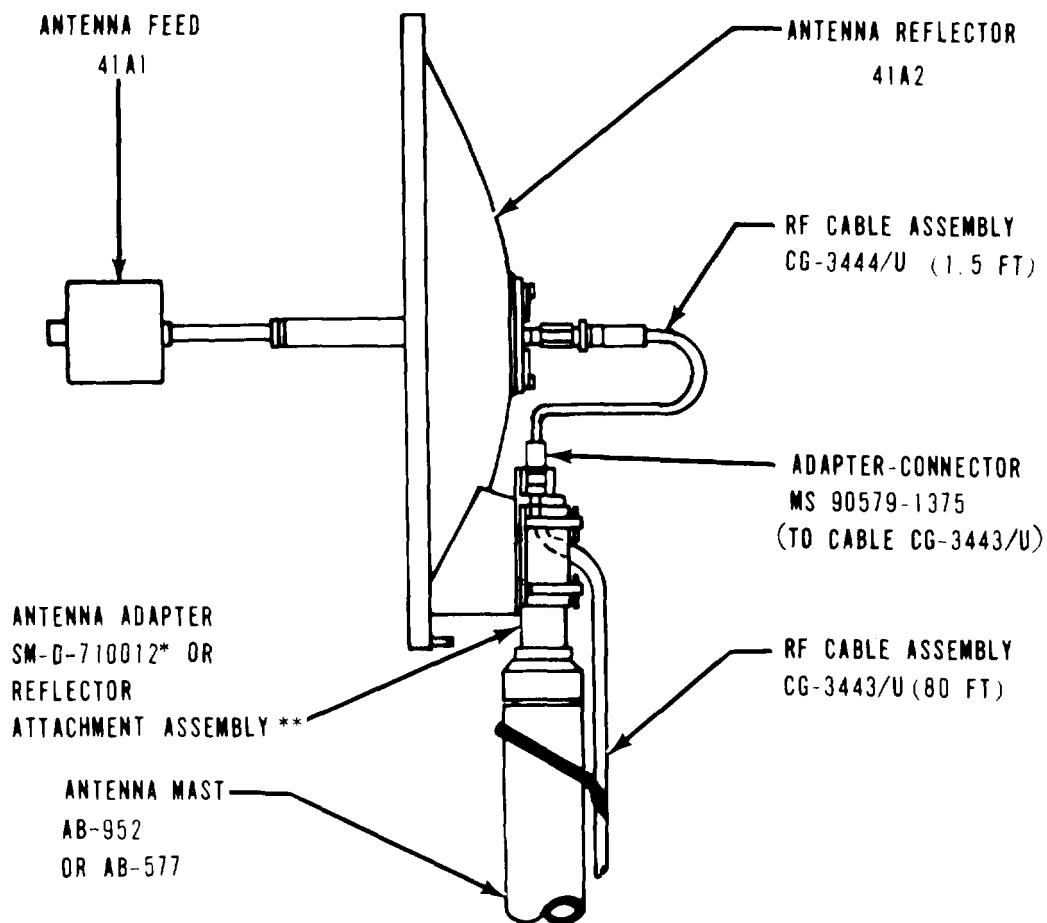
3-163. Antenna Feed 41A1

a. Test Equipment Required.

| Equipment                       | Common Name        |
|---------------------------------|--------------------|
| Multimeter, Digital, AN/USM-486 | Digital Multimeter |

b. Operational Check.

- (1) Remove cable assembly CG-3444/U from the antenna feed end connector (fig. 5-112).
- (2) Using the multi meter, check that there is a short circuit between the center and outer conductors of the end connector in the antenna feed assembly.
- (3) If an abnormal indication was obtained in (2) above, higher category of maintenance is required.



\* FOR MAST AB-577

\*\* FOR MAST AB-952

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Figure 3-112. Band IV antenna AS-3047/GRC-103(V), Side View.

Section IX. MODULE REMOVAL AND REPLACEMENT PROCEDURES  
FOR BAND IV RF HEADS

3-164. General

When trouble has been localized to a module of the radio set, replace the defective part as indicated in the paragraphs below. Before installing a replacement module, check connectors for bent or damaged pins. Make sure multipin connectors are properly mated and pressed home before mounting screws are tightened. Whenever difficulty is encountered in mating connectors, remove the applicable module and inspect the connectors for damage.

3-165. Additional Equipment Required

In addition to the equipment listed in paragraph 3-45, the following is required.

| Description   | Purpose               |
|---|-----------------------|
| Torque Wrench, Omni-Spectra model T-8438, 2 in. = 1b. | Tighten rf connectors |

3-166. Voltage Regulator 40A3

Replacement of the voltage regulator is covered in chapter 6, paragraph 6-16b of TM 11-5820-540-12.

3-167. Control-indicator 40A4

Replacement of the control-indicator is covered in chapter 6, paragraph 6-16a of TM 11-5820-540-12.

3-168. Coaxial Isolator 40A1AT1

Replace the isolator in accordance with the following:

- a. Replace the transmitter rf head top side up. Locate coaxial isolator 40A1AT1 (fig. 3-90).
- b. Disconnect plug P2 (40A1AT1J1) from 40A1AT1J1 and plug P1 (40A1AT1J2) from 40A1AT1J2.
- c. Remove the three green-circled mounting screws. Lift the module free.
- d. Aline the replacement module with the mounting holes. Replace the three mounting screws.

3-169. RF Power Monitor 40A1A1

Replace the monitor as follows:

- a. Place the transmitter rf head top side up. Locate rf power monitor 40A1A1 (fig. 3-90).

- b. Loosen and remove the hexagonal nut that secures the PWR CUT connector to the front panel of the transmitter rf head.
- c. Disconnect plug P1 (40A1W1J1) from 40A1W1J1 (fig. 3-89). Remove the cable clamp to free the cable.
- d. Disconnect plug P2 (40A1A1J1) from 40A1A1J1 (fig. 3-90).
- e. Remove the four green-circled screws that secure the power monitor to the mounting bracket. Remove the monitor.
- f. Slide monitor connector J2 of the replacement module into the PWR OUT opening on the front panel. Replace the hexagonal nut.

## NOTE

The hexagonal nut must be well-secured before the four screws are tightened.

- g. Secure the replacement module to the mounting bracket with the four screws removed in e above.
- h. Connect plug P2 (40A1A1J1) and plug P1 (40A1W1J1) to 40A1W1J1. Replace the cable clamp.

## 3-170. Electrical Dummy Load 40A1A2

Replace the electrical dummy load as follows:

- a. Place the transmitter rf head top side up. Locate electrical dummy load 40A1A2 (fig. 3-90).
- b. Disconnect plug P2 (40A1A2J1) from 40A1A2J1.
- c. Remove the two green-circled screws that secure the electrical dummy load to the housing. Remove the electrical dummy load carefully.
- d. Aline the replacement module with the mounting holes. Replace the two green-circled screws.
- e. Reconnect plug P2 (40A1A2J1) to 40A1A2J1.

## 3-171. Circulator 40A1HY1

Replace the circulator as follows:

- a. Place the transmitter rf head top side up. Locate circulator 40A1HY1 (fig. 3-90).
- b. Disconnect plug P1 (40A1HY1J1) from 40A1HY1J1, plug P2 (40A1HY1J3) from 40A1HY1J3 and plug P1 (40A1HY1J2) from 40A1HY1J2.
- c. Remove the two green-circled screws that secure the circulator to the mounting bracket. Remove the circulator along with the mounting plate.

- d. Remove the mounting plate from the existing circulator. Attach the plate to the replacement module.
- e. Position the replacement module over the mounting bracket. Replace the two green-circled screws.
- f. Reconnect the plugs which were disconnected in b above.

3-172. Electrical Shield 40MP3

Replace the electrical shield as follows:

- a. Place the transmitter rf head top side up. Locate electrical shield 40MP3 (fig. 3-89).
- b. Remove the six green-circled mounting screws. Carefully lift the module free.
- c. Aline the replacement module with the mounting holes. Replace the six green-circled screws.

3-173. Electronic Frequency Converter 39A2

Replace the electronic frequency converter as follows:

- a. Place the receiver rf head bottom side up. Locate electronic frequency converter 39A2 (fig. 3-92).
- b. Disconnect plug P2 (39A2J1) from 39A2J1 and plug P2 (39A2J2) from 39A2J2.
- c. Remove the three green-circled screws. Raise the converter carefully, disengaging it from the chassis connector.
- d. Position the replacement module over the mounting holes. Press down carefully, engaging the chassis connector.
- e. Replace the three green-circled screws.
- f. Reconnect plug P2 (39A2J1) to 39A2J1 and plug P2 (39A2J2) to 39A2J2.

3-174. Control-Indicator 39A4

Replacement of the control-indicator is covered in paragraph 6-18.1a, TM 11-5820-540-12.

3-175. RF Amplifier 39AR1

Replacement of the control-indicator is covered in paragraph 6-18.1a, TM 11-5820-540-12.

3-176. IF Amplifier 39AR2

Replace the if amplifier as follows:



- a. Place the receiver rf head top side up and locate if amplifier 39AR2 (fig. 3-92).
- b. Remove control-indicator 39A4 (para 6-18.1a, TM 11-5820-540-12).
- c. Disconnect plug 39A1W1A1PZ from 39AR2J1.
- d. Remove the three green-circled mounting screws. Raise the amplifier carefully, disengaging it from the chassis connector.
- e. Position the replacement module over the mounting holes. Press down carefully, engaging the chassis connector.
- f. Replace the three green-circled screws, and reconnect plug 39A1WIA1P2 to 39AR2J1.

## 3-177. RF Power Monitor 39A1A1

Replace the power monitor as follows:

- a. Place the receiver rf head to side up. Locate rf power monitor 39A1A1 and control-indicator 39A4 (fig. 3-93).
- b. Remove control-indicator 59A4 (para 6-18.1a, TM 11-5820-540-12).
- c. Loosen both retaining screws, and disconnect plug P1 (39A1W1J1) from 39A1W1J1.
- d. Disconnect plug P1 (39A1A1J2) from 39A1A1J2, as well as plug P1 (39A1A1J1) from 39A1A1J1.
- e. Remove the three green-circled mounting screws; remove the monitor.
- f. Remove the mounting plate from the existing monitor. Secure the plate to the replacement module.
- g. Position the replacement module over the mounting holes. Replace the three screws.
- h. Reconnect plug P1 (39A1A1J1) to 39A A1 and plug P1 (59A1A1J2) to 39A1A1J2.
- i. Reconnect plug P1 (39A1W1J1) to 39A1W1J1. Replace both retaining screws.
- j. Replace control-indicator 39A4(para 6-18.1a, TM 11-5820-540-12).

Section X. REMOVAL AND REPLACEMENT OF CENTRIFUGAL FAN 5A2B1 AND PRESSURE DIFFERENTIAL MONITOR 5A2A2 FROM TRANSMITTER CASE.CY-4637/GRC-103(V) OR CENTRIFUGAL FAN 5A2B1 AND CONTROL MONITOR TEMPERATURE SENSOR 5A2A2 FROM TRANSMITTER CASE 4637A/GRC-103(V)

## 3-178. General

There are two versions of the transmitter case, (CY-4637/GRC-103(V) and CY-4637A/GRC-103(V)). In both versions, the centrifugal fan 5A2B1 and sub-assembly 5A2A2 must be removed together. Removal and replacement of the two versions are covered separately.

NOTE

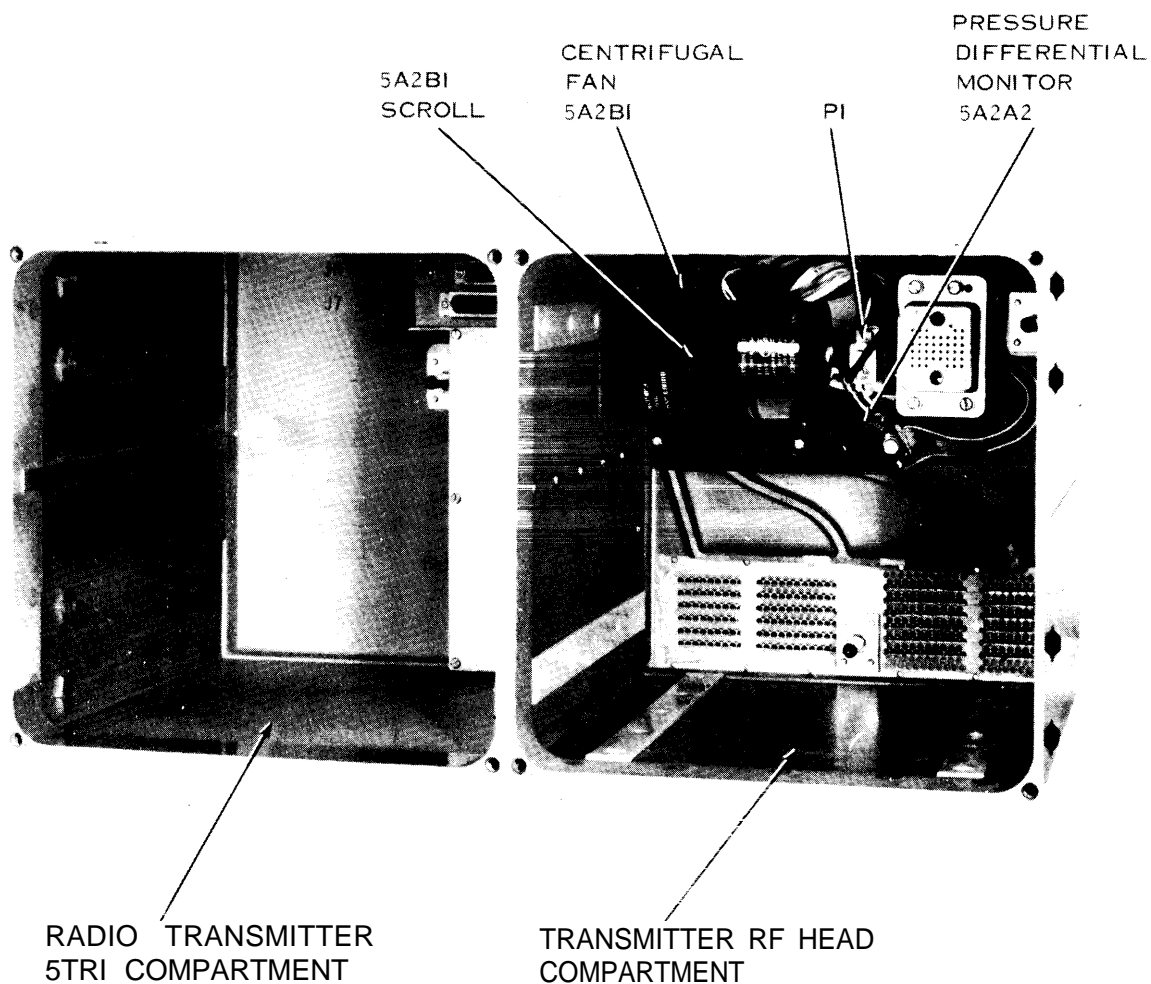
Whenever a 5A2B1 or 5A2A2 is to be replaced, both units must be removed from the transmitter case. The faulty unit is set aside, and the new unit is carefully mated with the operational unit through the square rubber tube that is glued to the pressure differential monitor. Then they are to be held together carefully and replaced in the transmitter case as a unit to maintain a tight air seal at the scroll (air outlet) of centrifugal fan 5A2B1.

3-179. Remove Transmitter Case (CY-4637/GRC-103(V)) (Fig. 3-113)

- a. Remove the transmitter fixed and rf heads from transmitter case 5A2.
- b. Unsolder and remove the wires that are connected to E3 and E4 on the pressure differential monitor. Tag or mark the wires for identification.
- c. Loosen the two screws that secure plug PI to its mating connector.
- d. Loosen and remove the four mounting screws that secure the pressure differential monitor to the rear wall of the transmitter case. (Two of the screw heads are accessible from the back of the rear wall.)
- e. In radio transmitter 5TR1 compartment, remove the three nuts and lockwashers that secure 5A2B1 to the partition wall. Remove 5A2B1 and 5A2A2 .
- f. Slip off the square rubber tube from the scroll of 5A2B1 to detach it from 5A2A2 .

3-180. Remove Transmitter Case (CY-4637A/GRC-103(V)) (Fig. 3-114)

- a. Remove the transmitter fixed and rf heads from transmitter case 5A2.
- b. Loosen the two screws that secure connector P1 to J1 (5A2A2).
- c. Loosen the two screws that secure the fan connector P1 to J5 (5A2A1).
- d. Loosen and remove the two mounting screws that secure the control monitor (5A2A2).
- e. Disconnect the two connectors and remove control monitor temperature sensor 5A2A2.
- f. In the radio transmitter compartment 5TR1, remove the three nuts and lockwashers that secure fan 5A2B1 to the partition wall.
- g. Remove fan 5A2B1.

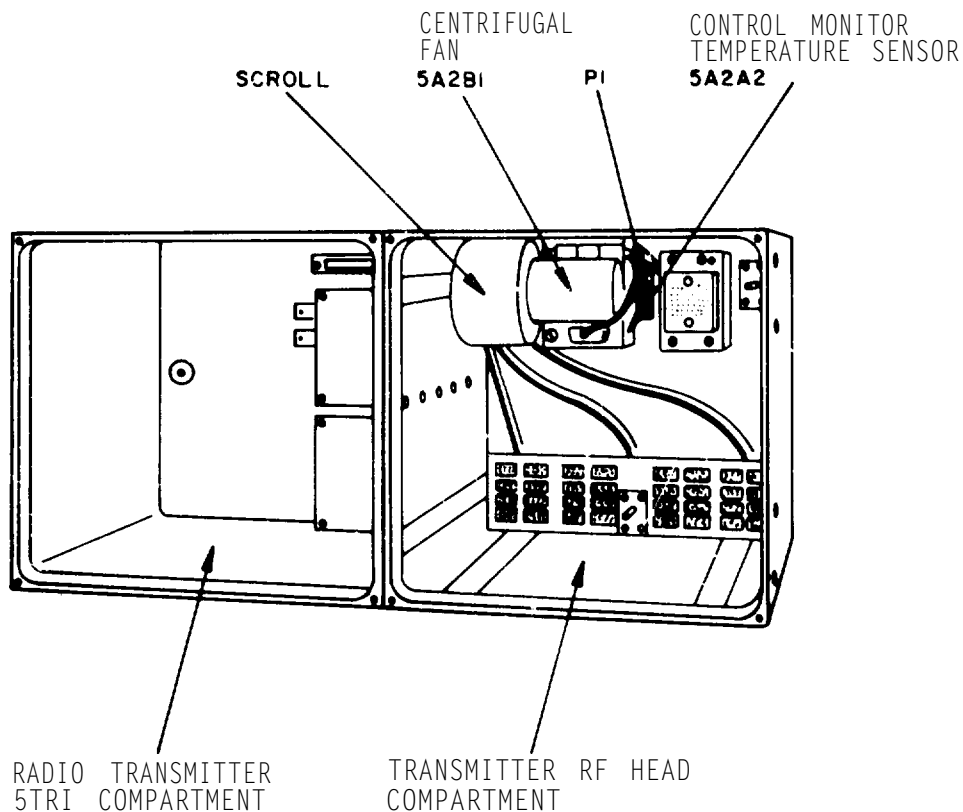


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Figure 3-113. Case Transmitter CY-4637/GRC-103(V), Front View.

3-181. Replacement Transmitter Case (CY-4637/GRC-103(V)) (Fig. 3-113)

- a. Mate the replacement unit (5A2B1 or 5A2A2) with the other by Sliding the square rubber tube that is glued to 5A2A2 over the scroll of 5A2B1. This must be done with care, since the tube is sized to make a tight fit around the scroll. Be sure the fit is tight and the tube is slipped on the scroll as far as it will go. Check 1-o see that the small connecting tube on the pressure differential monitor is properly connected.
- b. Holding the two units together, place the 5A2B1 into its position of the partition wall. Fit the lockwashers and nuts over the three bolts and tighten the nuts. Install and tighten the mounting screws that were removed in 3-180 d above. Replace the transmitter fixed and rf heads.



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Figure 3-114. Case Transmitter CY-4637A?GRC-103(V), Front View.

- 3-182. Replacement Transmitter Case (CY-4637A/GRC-103(V1) (Fig. 3-114)
- a. Secure fan 5A2B1 to the partition wall by replacing the three nuts and lockwashers in the radio transmitter compartment 5TR1.
  - b. Replace control monitor temperature sensor 5A2A2 and secure to rear of transmitter case with the two mounting screws.
  - c. Connect P1 of fan to connector J1 (5A2A1) and secure with two screws.
  - d. Connect PI of wiring harness to connector J5 (5A2A2) and secure with two screws.

#### CAUTION

Ensure that the screws at the four corners of the heads are tightened firmly. Leakage of air around the heads will defeat the purpose of the air filter and endanger the internal, heat generating parts of the transmitter.

#### 3-183. Testing After Replacement

- a. Connect Dummy Load, Electrical DA 437/GRC-103(V), or equivalent, to the transmitter front-panel PWR CUT connector.
- b. Set the transmitter AC POWER switch to ON/RESET. The OVERHEAT lamp should light and go out within 10 seconds.
- c. Completely cover the air filter with a suitable flat object, such as a sheet of heavy paper cut to the proper size. The OVERHEAT lamp should light and the buzzer should sound. Remove the obstruction immediately.

#### NOTE

When testing units equipped with case CY-4637A/GRC-103(V) and control monitor temperature sensor 5A2A2, the fan will increase speed to maximum. If blockage is not cleared OVERHEAT lamp will operate as above and the 600 v supply will be disconnected from tubes.



## CHAPTER 4

## SCHEMATIC AND BLOCK DIAGRAMS

## 4-1. General

This chapter contains the foldout schematic and block diagrams for Radio Set AN/GRC-103(v)1, 2, 3, 4. All text pertaining to the functioning of the radio set is in chapter 2.

## 4-2. Troubleshooting Data

The following information will aid the technician in locating the correct schematic or block diagram in this chapter.

| Foldout Caption   | Foldout No. |
|---|-------------|
| Electrical-Frequency Synthesizer 5TR1A2 or 1RE1A2 (SM-D-618945),<br>Overall Block Diagram . . . . .     | 4-1         |
| Electrical-Frequency Synthesizer 5TR1A2 or 1RE1A2 (SM-D-865030),<br>Overall Block Diagram . . . . .     | 4-2         |
| Interconnecting Box 5TR1A2A1 or 1RE1A2A1, Schematic Diagram . . . . .                                   | 4-3         |
| Interconnecting Box 5TR1A2A11 or 1RE1A2A11, Schematic Diagram . . . . .                                 | 4-4         |
| Modulator-Oscillator 5TR1A2A2 or 1RE1A2A2 (Part No. CMC 456-260),<br>Schematic Diagram . . . . .        | 4-5         |
| Modulator-Oscillator 5TR1A2A2 or 1RE1A2A2 (Part No. CMC<br>220-800159-000), Schematic Diagram . . . . . | 4-6         |
| Frequency-Divider 5TR1A2A4 or 1RE1A2A4, Schematic Diagram . . . . .                                     | 4-7         |
| Frequency-Divider 5TR1A2A14 or 1RE1A2A14, Schematic Diagram . . . . .                                   | 4-8         |
| Digital Electronic Divider-Counter 5TR1A2A5 or 1RE1A2A5,<br>Schematic Diagram . . . . .                 | 4-9         |
| Digital Electronic Divider-Counter 5TR1A2A15 or 1RE1A2A15,<br>Schematic Diagram . . . . .               | 4-10        |
| Digital Electronic Counter 5TR1A2A6 or 1RE1A2A6, Schematic Diagram . . . . .                            | 4-11        |
| Digital Electronic Counter 5TR1A2A16 or 1RE1A2A16, Schematic Diagram..                                  | 4-12        |
| Electrical Synchronizer 5TR1A2A7 or 1RE1A2A7, Schematic Diagram . . . . .                               | 4-13        |
| Electrical Synchronizer 5TR1A2A17 or 1RE1A2A17, Schematic Diagram . . . . .                             | 4-14        |
| Signal Data Converter-Storer 5TR1A2A8 or 1RE1A2A8, Schematic Diagram..                                  | 4-15        |
| Signal Data Converter-Storer 5TR1A2A18 or 1RE1A2A18, Schematic<br>Diagram . . . . .                     | 4-16        |
| Frequency Divider 5TR1A2A9 or 1RE1A2A9, Schematic Diagram . . . . .                                     | 4-17        |
| RF Oscillator 5TR1A2Y1 or 1RE1A2Y1, Schematic Diagram . . . . .   | 4-18        |
| RF Oscillator 5TR1A2Y11 or 1RE1A2Y11, Schematic Diagram . . . . .                                       | 4-19        |
| Pulse Form Restorer 1RE1A3, (SM-D-698146, CMC PN 245-455624-000),<br>Block Diagram . . . . .            | 4-20        |
| Pulse Form Restorer 1RE1A3, (SM-D-990510, CMC PN 245-803110-000),<br>Block Diagram . . . . .            | 4-20.1      |
| Pulse Form Restorer 1RE1A3 (SM-D-698146, CMC PN 245-455624-000),<br>Schematic Diagram . . . . .         | 4-21        |
| Pulse Form Restorer 1RE1A3 (SM-D-990510, CMC PN 245-803110-000),<br>Schematic Diagram . . . . .         | 4-21.1      |
| Electrical Frequency Limiter-Discriminator 1RE1A4, Schematic<br>Diagram . . . . .                       | 4-22        |
| Amplifier-Frequency Multiplier 1RE1A5, Schematic Diagram . . . . .                                      | 4-23        |

| Foldout Caption  | Foldout No |
|--|------------|
| Video Amplifier 1RE1AR1 (R-1329(P)/GRC-103(V) and R-1329A(P)/GRC-103(V)), Schematic Diagram . . . . .  | 4-24       |
| Video Amplifier 1RE1AR1 (R-1329B(P)/GRC-103(V) ), Schematic Diagram . . . . .  | 4-25       |
| Intermediate Frequency Amplifier 1RE1AR2, Schematic Diagram . . . . .  | 4-26       |
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| Radio Frequency Amplifier 2A1AR1, Schematic Diagram . . . . .  | 4-32       |
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| Electronic Switch 2A4, Schematic Diagram . . . . .   | 4-34       |
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| Receiver, RF Head AM-4316A/GRC-103(V), Schematic Diagram . . . . .   | 4-37       |
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| Amplifier-Frequency Multiplier AM-4320/GRC-103(V), Schematic Diagram . . . . .   | 4-46       |
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| Control-Indicator 37A2 or 33A4 Coding Tables . . . . .   | 4-51       |
| Signal Level Control Monitor 33A5 or 34A5, Schematic Diagram . . . . .   | 4-52       |
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| Foldout Caption   | Foldout No. |
|---|-------------|
| Frequency-Multiplier 34A2A1, Schematic Diagram . . . . .  | 4-59        |
| Control- indicator 38A2 or 34A4, Coding Tables . . . . .  | 4-60        |
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| Receiver-Transmitter Order Wire RT-773/GRC-103(V) interconnecting<br>Diagram . . . . .  | 4-78        |



APPENDIX A

REFERENCES

A-1 . SCOPE

The following is a list of all Army regulations, pamphlets, forms, service bulletins, technical bulletins, and technical manuals.

A-2 . ARMY REGULATIONS

- Report of Transportation Discrepancies in Shipment . . . . . AR 55-38
- Reporting of Item and Packaging Discrepancies . . . . . AR 735-11-2

A-3 . PAMPHLETS

- Consolidated Index of Army Publications and Bland Forms . . . . DA Pam 25-30
- The Army Maintenance I'management Systems) (TAMMS). . . . . DA Pam 738-750

A - 4 . SERVICE BULLETINS

- Preservation, Packaging, Packing, and Marking Materials, Supplies, and Equipment Used by the Army . . . . . SB 38-100

A-5. TECHNICAL BULLETINS

- Field instructions for Painting and preserving . . . . . TB 43-0118  
     Communications-Electronics Equipment
- Safety Measures to be Observed When Installing and Using Whip Antennas, Field-Type Masts, Towers, Antennas, and Metal Poles That Are Used with Communication, Radar, and Direction Finder Equipment . . . . . TB 43-0129

A-6 . TECHNICAL MANUALS

- Operators and Organizational Maintenance Manual (Including Repair Parts and Special Tool Lists: Radio Set AN/GRC-103(V)1,2, 3, and Extension Kit, Mast, MK-1009/GRC-103(V) (NSN 5820-00-935-4931 ) . . . . . TM 11-5820-540-12
- DS, GS, and Depot Maintenance Repair Parts and Special Tools List: Radio Set AN/GRC-103(V)1; Mast Extension and Direct support Cable kit. . . . . TM 11-5820-540-34P
- Operator Is, Organizational, Direct Support and General Support I'maintenance Repair Parts and Special Tools Lists (Including Depot Maintenance Repair Parts and Special Tools): Handsets H-60/PT and H-165/U . . . . . TM 11-5965-224-14P

A-6. TECHNICAL MANUALS (CONT)

Operator's and Organizational Maintenance Manual:  
 Voltmeter, *Meter* ME-30A/U and Voltmeters, Electronic  
 ME-30B/U, ME-30C/U, and ME-30E/U . . . . . TM 11-6625-320-12

Operator and Organizational Maintenance Manual:  
 Indicators, Standing Wave Ratio AN/UPM-108 and  
 AN/UPM-108A . . . . . TM 11-6625-335-12

Operator's Organizational, DS, GS, and Depot Maintenance  
 Manual: Multimeter TS-352B/U . . . . . TM 11-6625-366-15

Operator and Organizational Maintenance Manual: Meter,  
 Modulation ME-57/U . . . . . TM 11-6625-400-12

Operator's Manual: Thermal Noise Generator SG-419/U . . . . . TM 11-6625-413-10

Organizational, DS, GS, and Depot Maintenance Manual:  
 Wattmeters AN/URM-98 and AN/URM-98A . . . . . TM 11-6625-433-15

Operator's, Organizational, Direct Support, General  
 Support and Depot Maintenance Manual: Voltmeter, Digital  
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Operator's, Organizational, DS, GS, and Depot Maintenance  
 Manual: Wattmeter AN/URM-120 . . . . . TM 11-6625-446-15

Operator's Manual: Signal Generators AN/USM-44 and  
 AN/USM-44A . . . . . TM 11-6625-508-10

Operator, Organizational, DS, GS, and Depot Maintenance  
 Manual: Oscilloscope AN/USM-140A . . . . . TM 11-6625-535-15

Organizational, DS, GS, and Depot Maintenance Manual  
 (Including Repair Parts and Special Tool Lists):  
 Oscilloscopes AN/USM-140B, AN/USM-140C, AN/USM-141A,  
 and AN/USM-141b . . . . . TM 1-6625-535-15-1

Operator's Organizational, DS, GS, and Depot Maintenance  
 Manual: Generator, Signal AN/USM-205 . . . . . TM 11-6625-665-15

Operator's Manual: Digital Readout, Electronic Counter  
 AN/USM-207 (NSN 6625-00-911-6368) . . . . . TM 11-6625-700-10

Operator and Organizational Maintenance Manual: Test  
 Facilities Set AN/GRM-95(V)2 . . . . . TM 11-6625-1696-12

Administrative Storage of Equipment . . . . . TM 740-90-1

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TM 11-5840-340-12

PUBLICATION DATE

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FO3

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°.

REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.

Item 5, Function column. Change "2 db" to "3db."

REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.

Add new step f.1 to read, "Replace cover plate removed in step e.1, above."

REASON: To replace the cover plate.

Zone C 3. On J1-2, change "+24 VDC to "+5 VDC."

REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER

SSG I. M. DeSpiritof 999-1776

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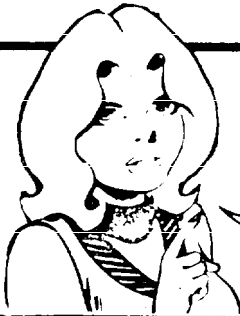
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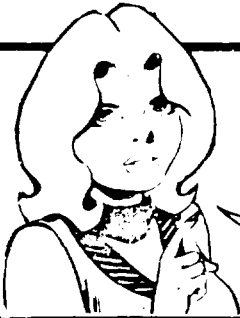
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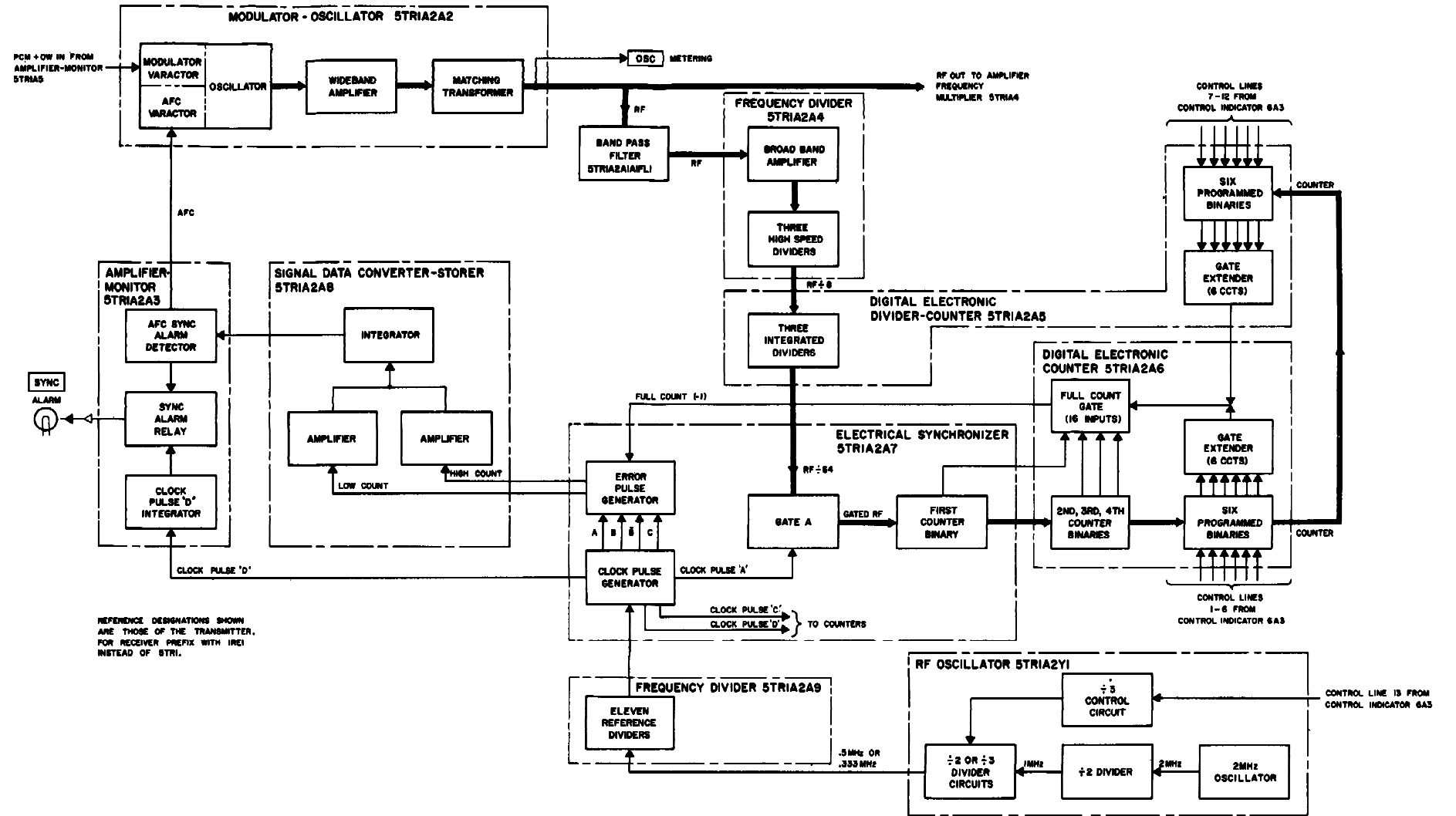
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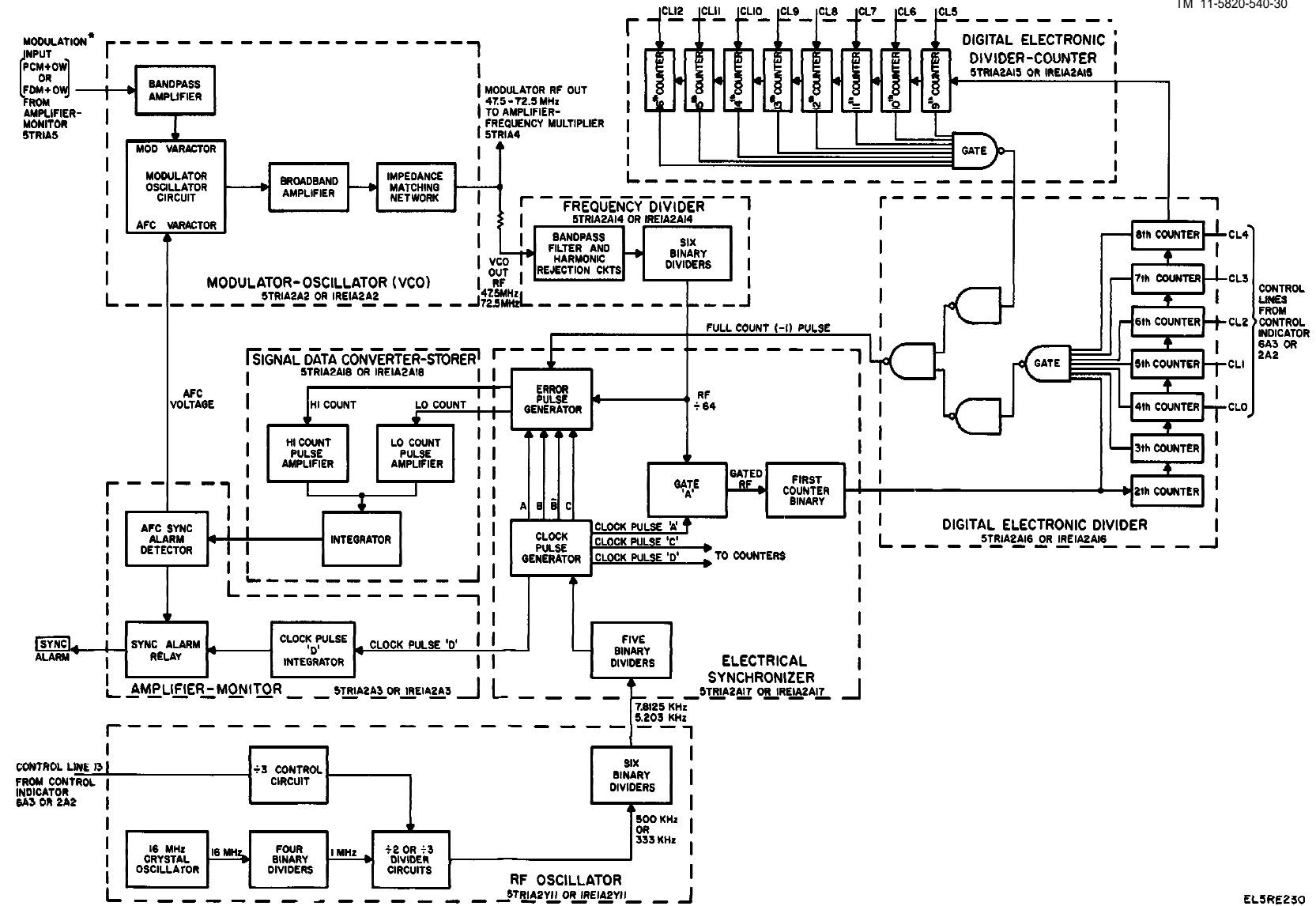






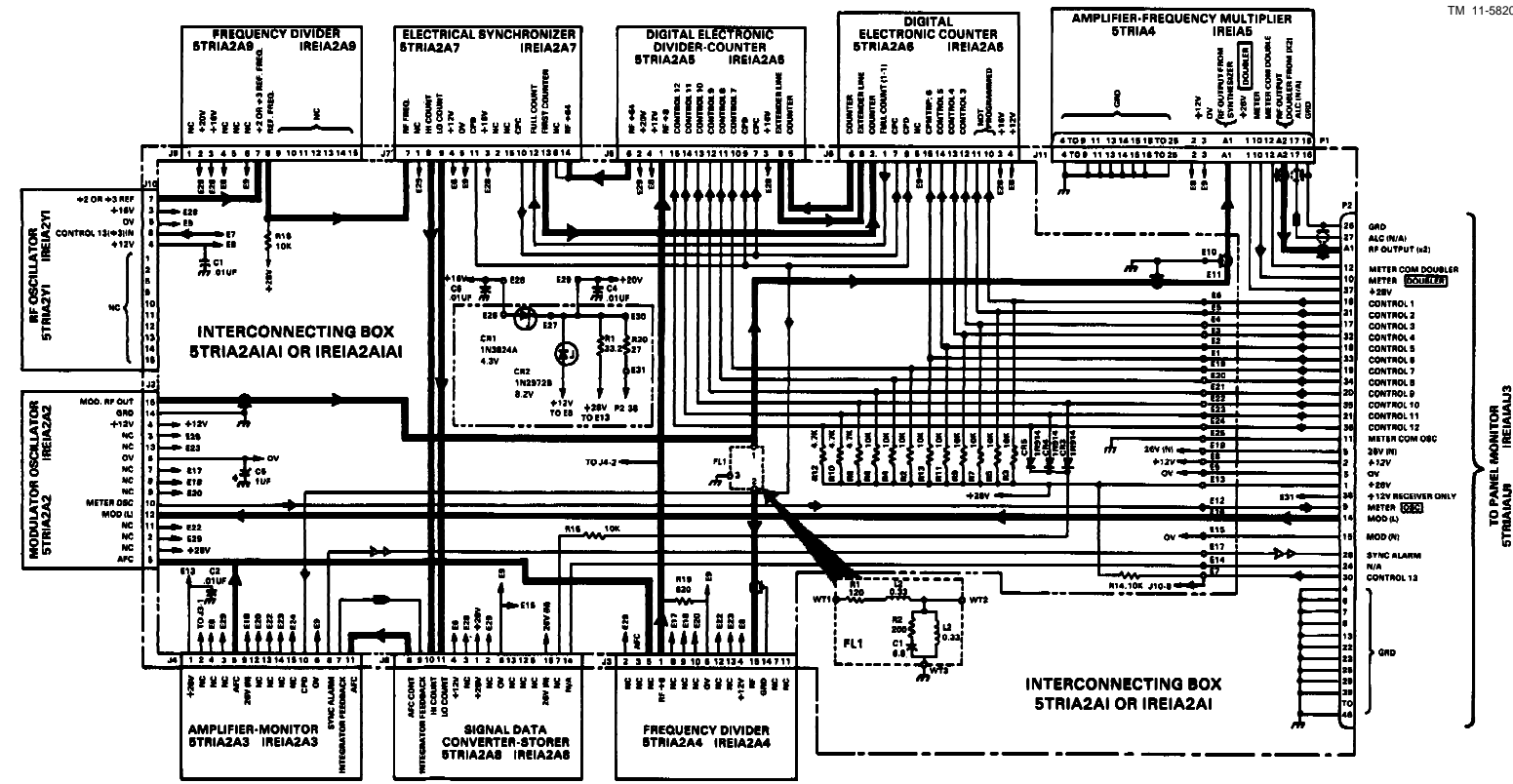
EL5RE229

FO-4-1. Electrical-Frequency Synthesizer 5TR1A2 or 1RE1A2 (SM-D-618945), Overall Block Diagram.



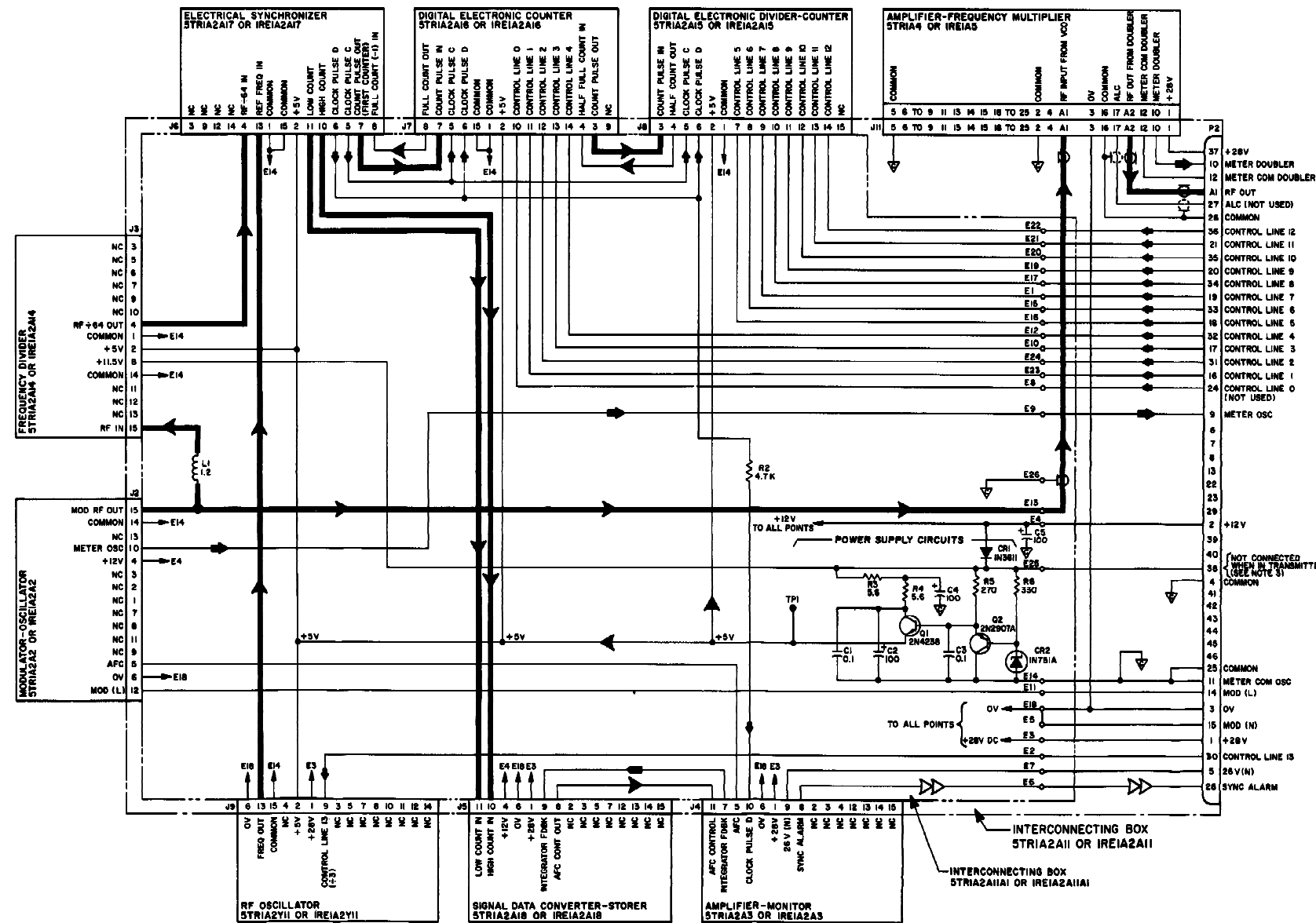
EL5RE230

FO-4-2. Electrical-Frequency Synthesizer 5TR1A2 or 1RE1A2 (SM-D-865030), Overall Block Diagram.



- NOTES**
- | SYMBOL | DEGNATION | UNIT        |
|--------|-----------|-------------|
| R      | NONE      | OHM         |
|        | K         | KILOHM      |
|        | M         | MEG OHM     |
| C      | NONE      | PICTOFARAD  |
|        | UF        | MICROFARAD  |
| L      | NONE      | MICROHENRY  |
|        | MH        | MILLI HENRY |
|        | H         | HENRY       |
2. THE VOLTAGES SHOWN ARE THOSE USED IN THE TRANSMITTER. FOR RECEIVER CONVERT AS FOLLOWS:  
 TRANSMITTER: +12V DC → +18V DC, 0 → 0V, +28V DC → +12V DC, +30V DC → +9V DC, +15V DC → +4V DC  
 RECEIVER: +12V DC → +18V DC, 0 → 0V, +28V DC → +12V DC, +30V DC → +9V DC, +15V DC → +4V DC
3. MAJOR FUNCTIONAL FLOW: DC METERING FLOW: SECONDARY SIGNAL FLOW: FAULT SIGNAL PATH TO LIGHT LAMP OR PROVIDE INDICATION: REFERENCE SIGNAL VOLTAGE: GATING OR SYNCHRONIZING SIGNAL:
4. CONNECTORS J2 TO J10 INCL. MAY HAVE PINS IDENTIFIED BY LETTER LETTERS OR NUMERALS. THE FOLLOWING TABLE SHOWS THE EQUIVALENT IDENTIFICATIONS:
- |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |     |
|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | 100 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |     |
| A | B | C | D | E | F | G | H | I | J  | K  | L  | M  | N  | O  | P  | Q  | R  | S  | T  | U  | V  | W  | X  | Y  | Z  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74  | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | 100 |

FO-4-3. Interconnecting Box 5TR1A2A1 or 1RE1A2A1, Schematic Diagram.



- NOTES:**
- | SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHM        |
| K      | NONE        | MILIOHM    |
| M      | NONE        | MEGOHM     |
| C      | PF          | PICOFARAD  |
|        | NONE        | MICROFARAD |
| L      | NONE        | MICROHENRY |
|        | m           | MILLIHENRY |
|        | H           | HENRY      |
  - THE VOLTAGES SHOWN ARE THOSE USED IN THE TRANSMITTER, FOR RECEIVER CONVERT AS FOLLOWS:

| TRANSMITTER | RECEIVER   |
|-------------|------------|
| OV          | -12V       |
| +12V        | OV         |
| +28V        | +12V       |
| +5V         | +5V        |
| +11.5V      | +12V       |
| P2-38 NC    | P2-38 +12V |
  - CONNECTORS J2 TO J10 INCL. MAY HAVE PINS IDENTIFIED BY EITHER LETTERS OR NUMERALS. THE FOLLOWING TABLE SHOWS THE EQUIVALENT IDENTIFICATIONS.

|   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| A | B | C | D | E | F | G | H | I | J  | K  | L  | M  | N  | P  |
  - MAJOR FUNCTIONAL FLOW.
    - DC METERING FLOW.
    - GATING, SYNCHRONIZING OR CONTROL SIGNAL.
    - FAULT SIGNAL PATH PROVIDES INDICATION, ALARM.
    - REFERENCE SIGNAL VOLTAGE.
    - SECONDARY FUNCTIONAL FLOW.

FO-4-4. Interconnecting Box 5TR1A2A11 or 1RE1A2A11, Schematic Diagram.

NOTES

1-

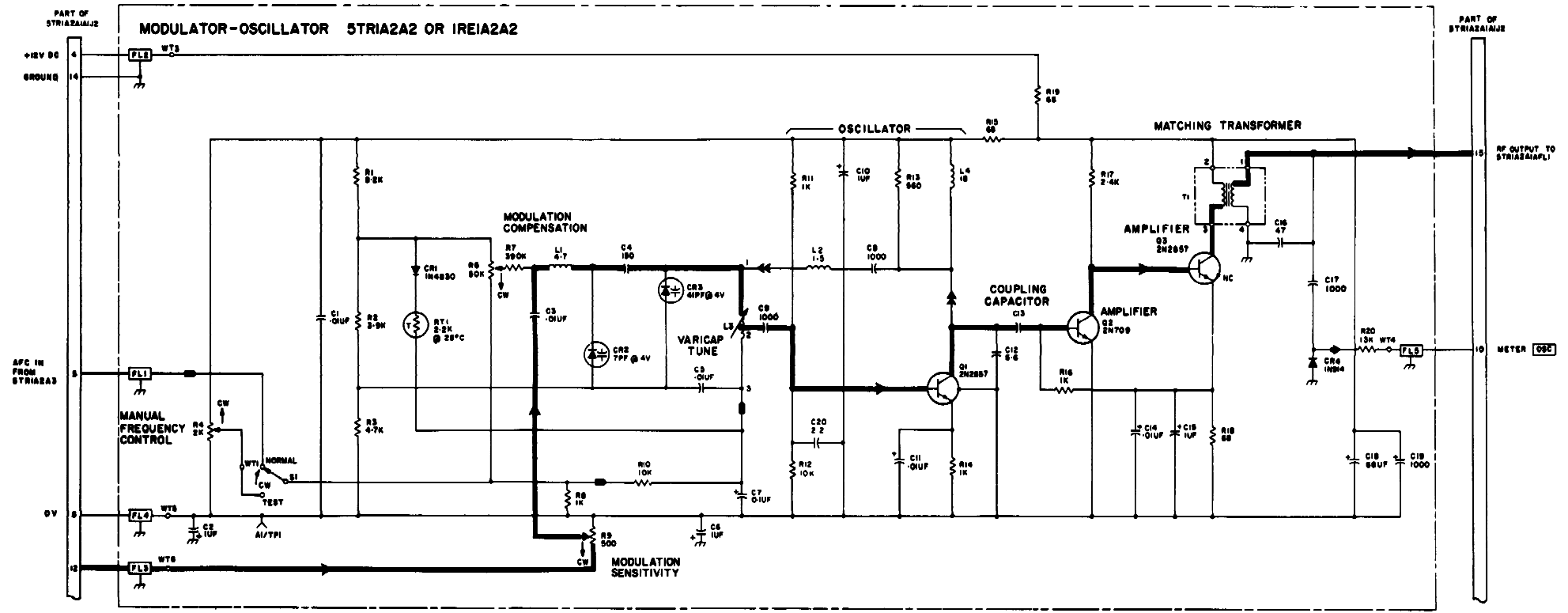
| SYMBOL | DESIGNATION     | UNIT                               |
|--------|-----------------|------------------------------------|
| R      | NONE<br>M<br>K  | OHMS<br>KILOHMS<br>MEG OHMS        |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD            |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLI HENRY<br>HENRY |

2-

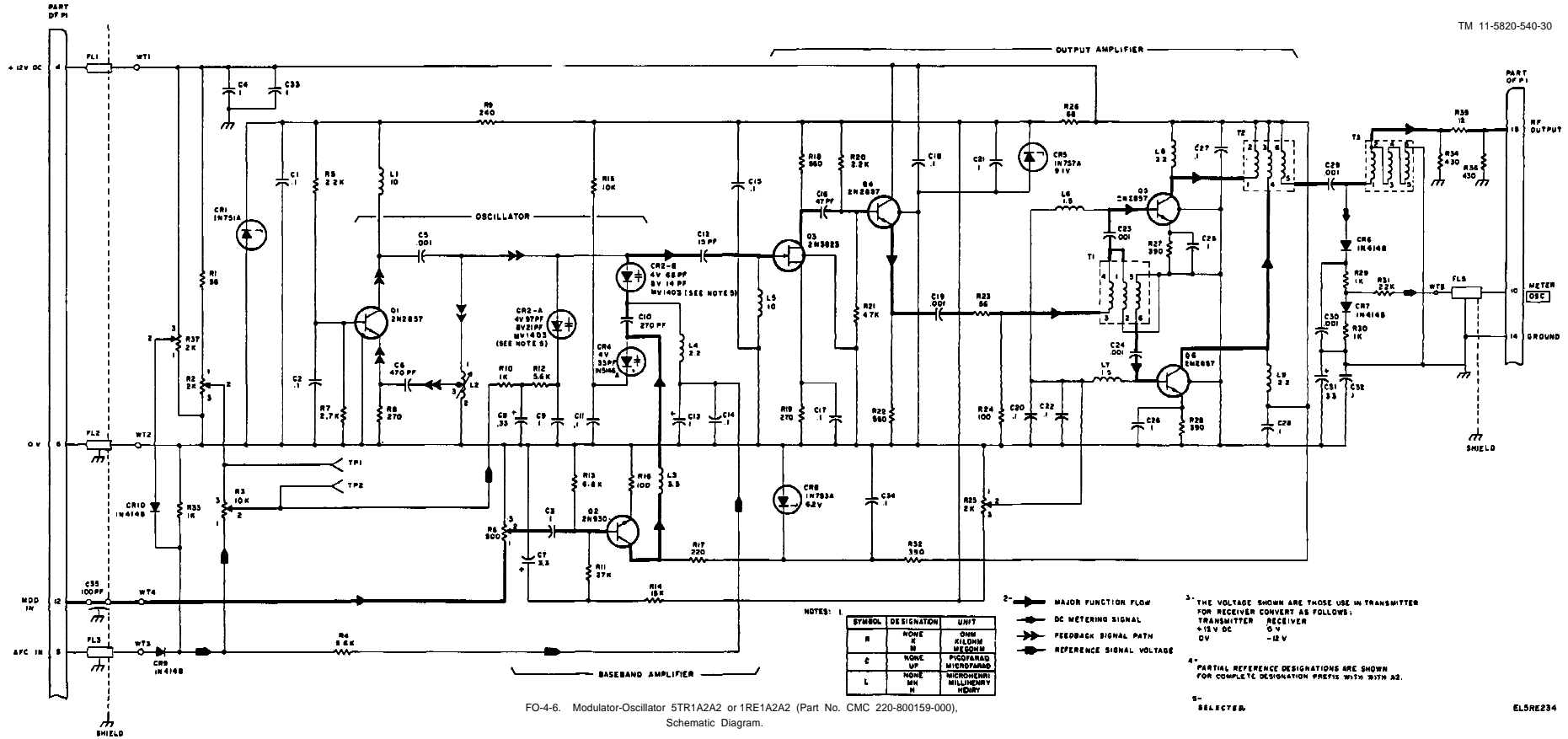
- ➔ MAJOR FUNCTIONAL FLOW
- ➔ FEEDBACK SIGNAL PATH
- ➔ DC METERING SIGNAL
- ➔ REFERENCE SIGNAL VOLTAGE

3-

THE VOLTAGES SHOWN ARE THOSE USED IN THE TRANSMITTER. FOR RECEIVER CONVERT AS FOLLOWS:  
 TRANSMITTER: +12 V DC  
 0V  
 RECEIVER: 0V  
 +12 V DC



4609233



NOTES: 1

| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHM        |
| K      | NONE        | KILOHM     |
| M      | NONE        | MEGOHM     |
| C      | NONE        | PICOFARAD  |
| P      | UP          | MICROFARAD |
| M      | NONE        | MINI       |
| L      | NONE        | MILLIHENRY |
| H      | NONE        | HENRY      |

- 2- MAJOR FUNCTION FLOW  
 DC METERING SIGNAL  
 FEEDBACK SIGNAL PATH  
 REFERENCE SIGNAL VOLTAGE
- 3- THE VOLTAGE SHOWN ARE THOSE USE IN TRANSMITTER FOR RECEIVER CONVERT AS FOLLOWS:  
 TRANSMITTER +12 V DC  
 RECEIVER 0 V  
 DV -12 V
- 4- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH WITH A2.
- 5- SELECTED.

FO-4-6. Modulator-Oscillator 5TR1A2A2 or 1RE1A2A2 (Part No. CMC 220-800159-000), Schematic Diagram.



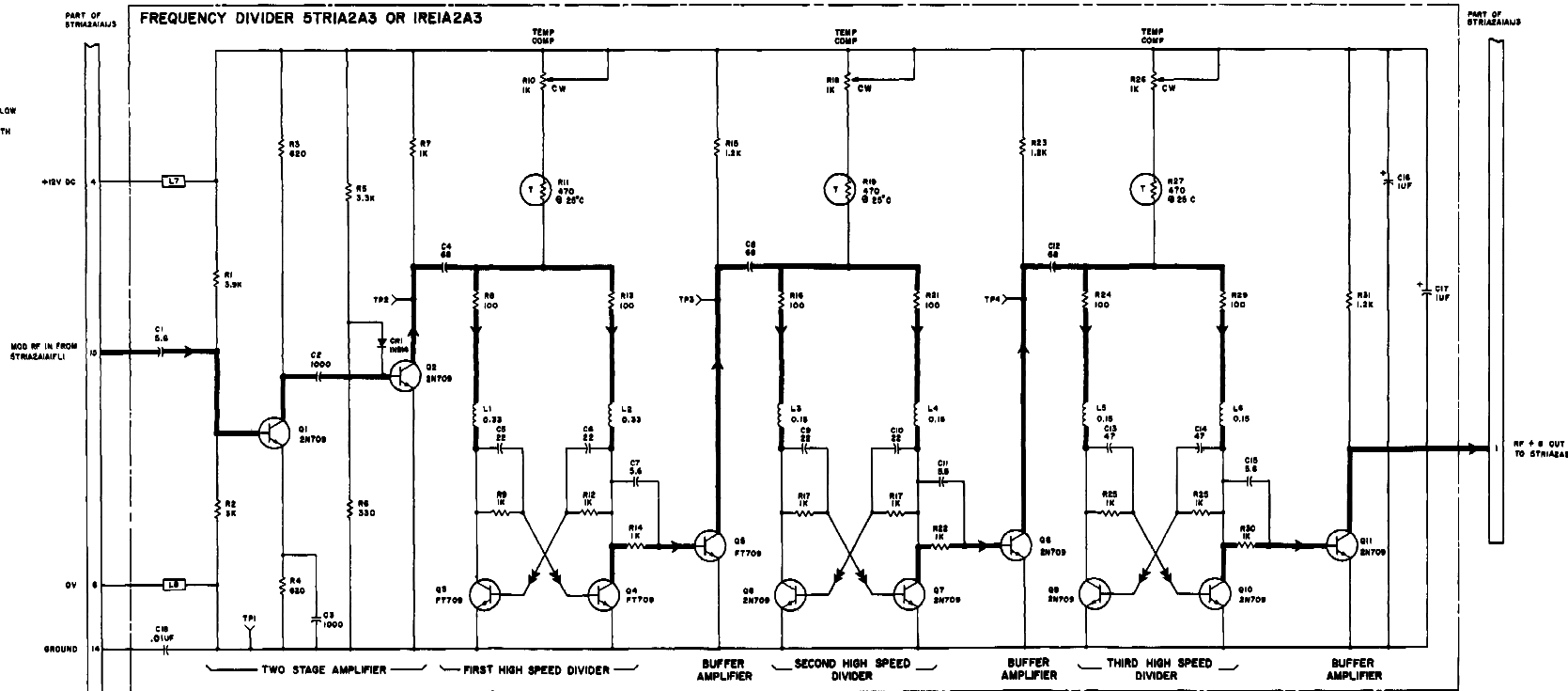
- NOTES
- MAJOR FUNCTIONAL FLOW

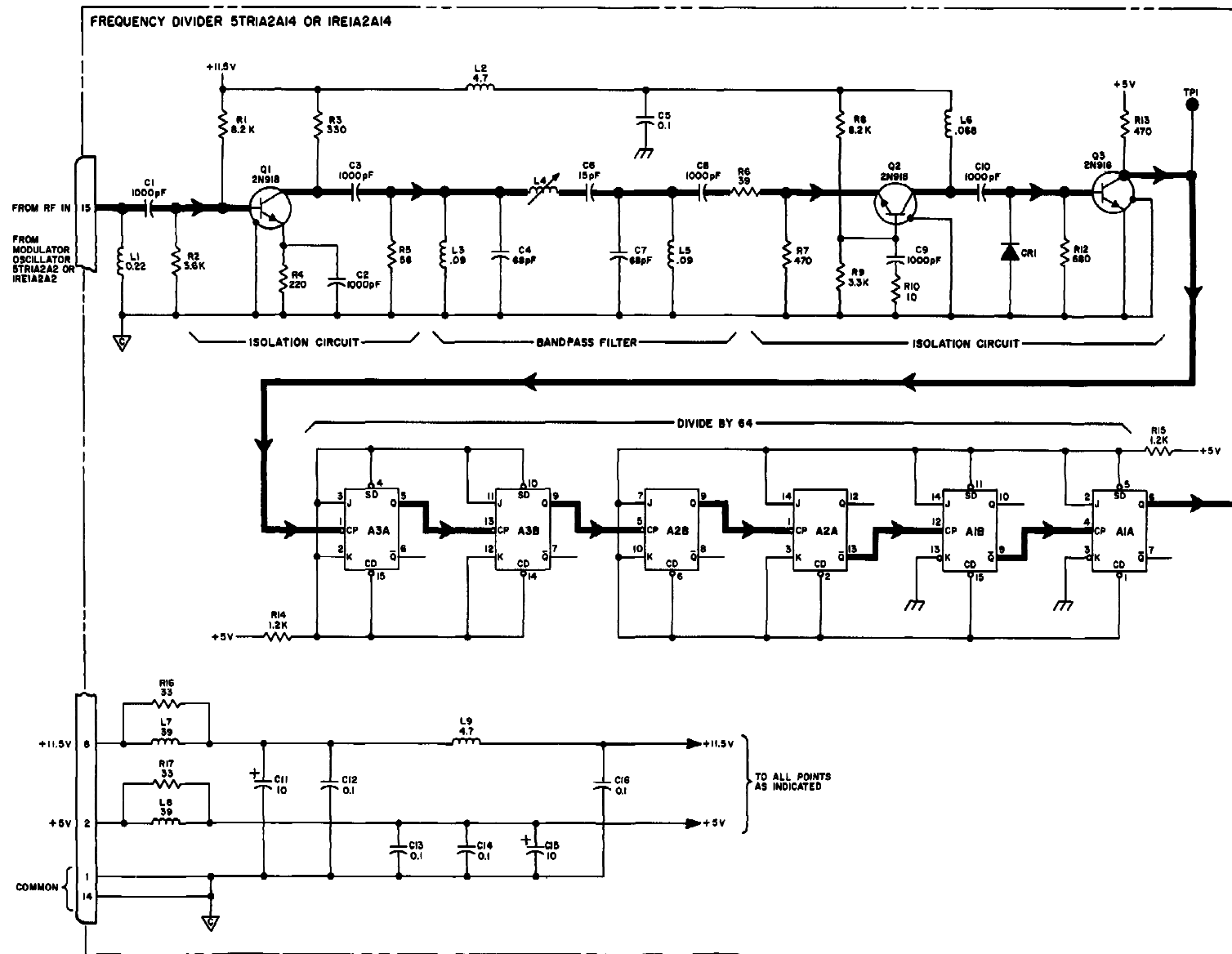
FEEDBACK SIGNAL PATH

| SYMBOL | DESIGNATION | UNIT                               |
|--------|-------------|------------------------------------|
| R      | RESISTOR    | OHM<br>KILOHM<br>MEG OHM           |
| C      | CAPACITOR   | PICOFARAD<br>MICROFARAD            |
| L      | INDUCTOR    | MICROHENRY<br>MILLI HENRY<br>HENRY |

- THE VOLTAGES SHOWN ARE USED IN THE TRANSMITTER. FOR RECEIVER CONVERT AS FOLLOWS:

|             |          |
|-------------|----------|
| TRANSMITTER | RECEIVER |
| +12 V DC    | 0 V      |
| 0 V         | -12 V DC |





NOTES : TM 11-5820-540-30

1.

| SYMBOL | DESIGNATION    | UNIT                              |
|--------|----------------|-----------------------------------|
| R      | NONE<br>K<br>M | OHM<br>KILOHM<br>MEG OHM          |
| C      | pF<br>NONE     | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>m<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

2.

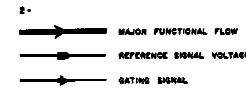
| REFERENCE DESIGNATION | SUPPLY VOLTAGE |        |
|-----------------------|----------------|--------|
|                       | +5V            | COMMON |
| A1, A3                | PIN 16         | PIN 8  |
| A2                    | PIN 4          | PIN 11 |
|                       |                |        |

3. MAJOR FUNCTIONAL FLOW.

NOTES

1-

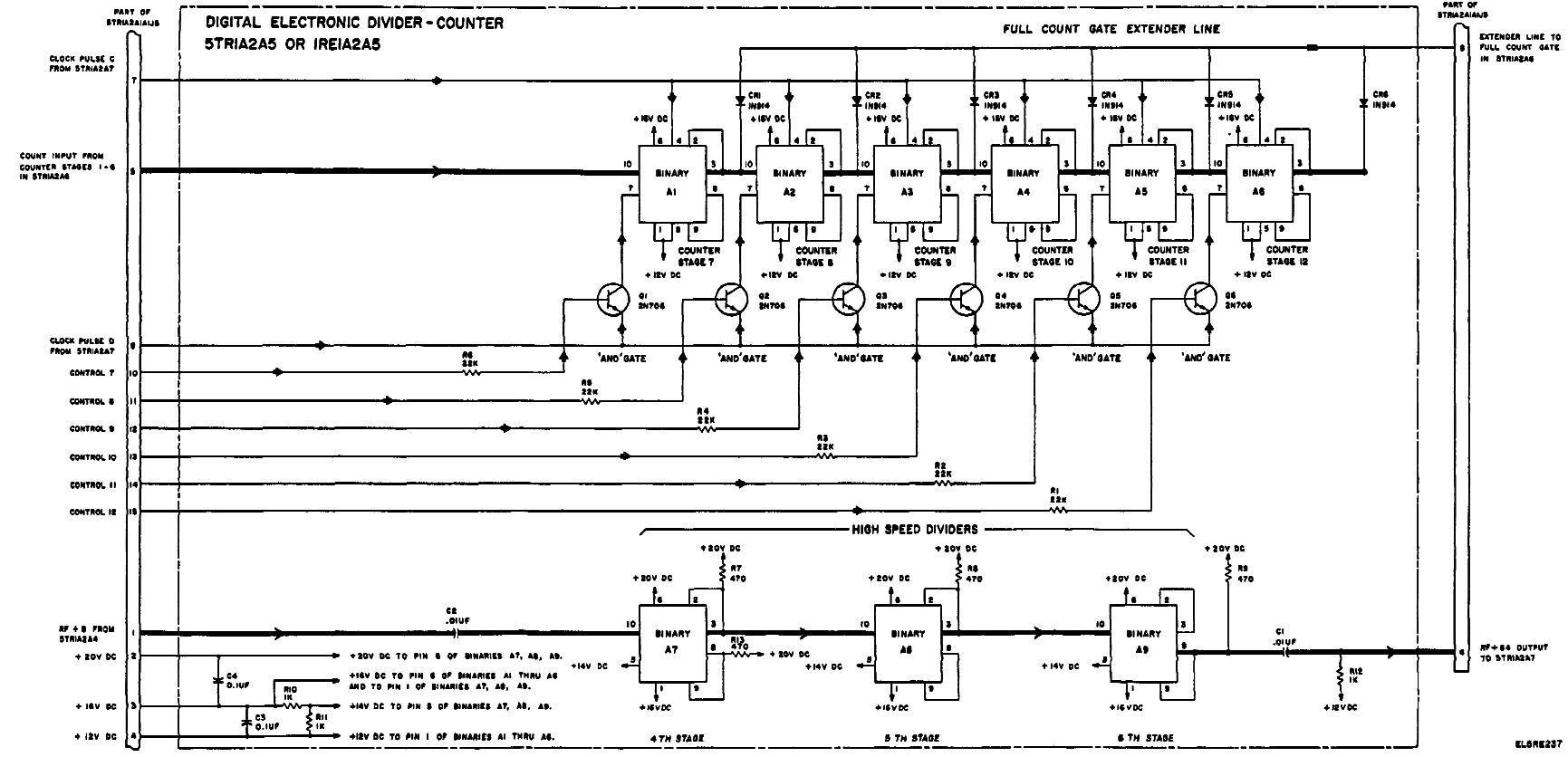
| SYMBOL | DESIGNATION | UNIT                              |
|--------|-------------|-----------------------------------|
| R      | RESISTOR    | OHM<br>KILOHM<br>MEGOM            |
| C      | CAPACITOR   | PICOFARAD<br>MICROFARAD           |
| L      | INDUCTOR    | MICROHENRY<br>MILLIHENRY<br>HENRY |

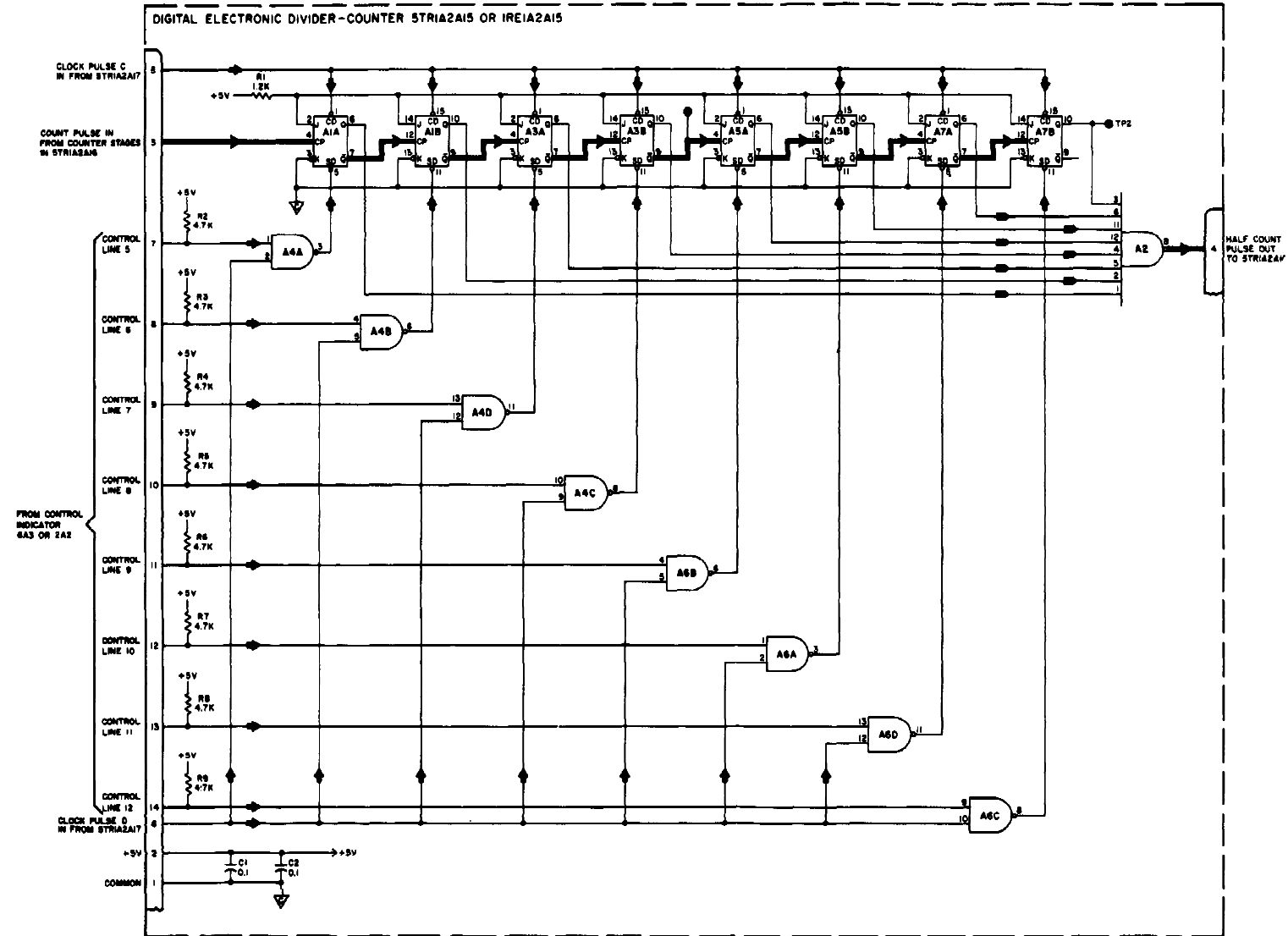


3-

THE VOLTAGES SHOWN ARE THOSE USED IN THE TRANSMITTER. FOR RECEIVER CONVERT AS FOLLOWS:

|         |        |
|---------|--------|
| +20V DC | +8V DC |
| +16V DC | +4V DC |
| +14V DC | +2V DC |
| +12V DC | 0V     |





**NOTES:**

1.

| SYMBOL | DESIGNATION | UNIT                  |
|--------|-------------|-----------------------|
| R      | NONE        | OHM                   |
| K      | K           | 10 <sup>3</sup> OHM   |
| M      | M           | 10 <sup>6</sup> OHM   |
| C      | PF          | PICOFARAD             |
| L      | NONE        | MICROHENRY            |
| H      | H           | 10 <sup>3</sup> HENRY |

2.

| HIGHEST REFERENCE DESIGNATION |
|-------------------------------|
| A7                            |
| C2                            |
| R9                            |

- 3.
- A1, A3, A5, A7  
PIN 16 +5V  
PIN 8 COMMON
  - A2, A4, A6  
PIN 14 +5V  
PIN 7 COMMON

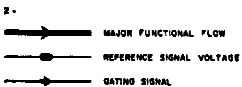
- 4.
- ➔ MAJOR FUNCTIONAL FLOW.
  - ⤴ GATING OR SYNCHRONIZING SIGNAL
  - ⤵ REFERENCE SIGNAL VOLTAGE.

FO-4-10. Digital Electronic Divider-Counter 5TR1A2A15 or 1RE1A2A15, Schematic Diagram.

NOTES

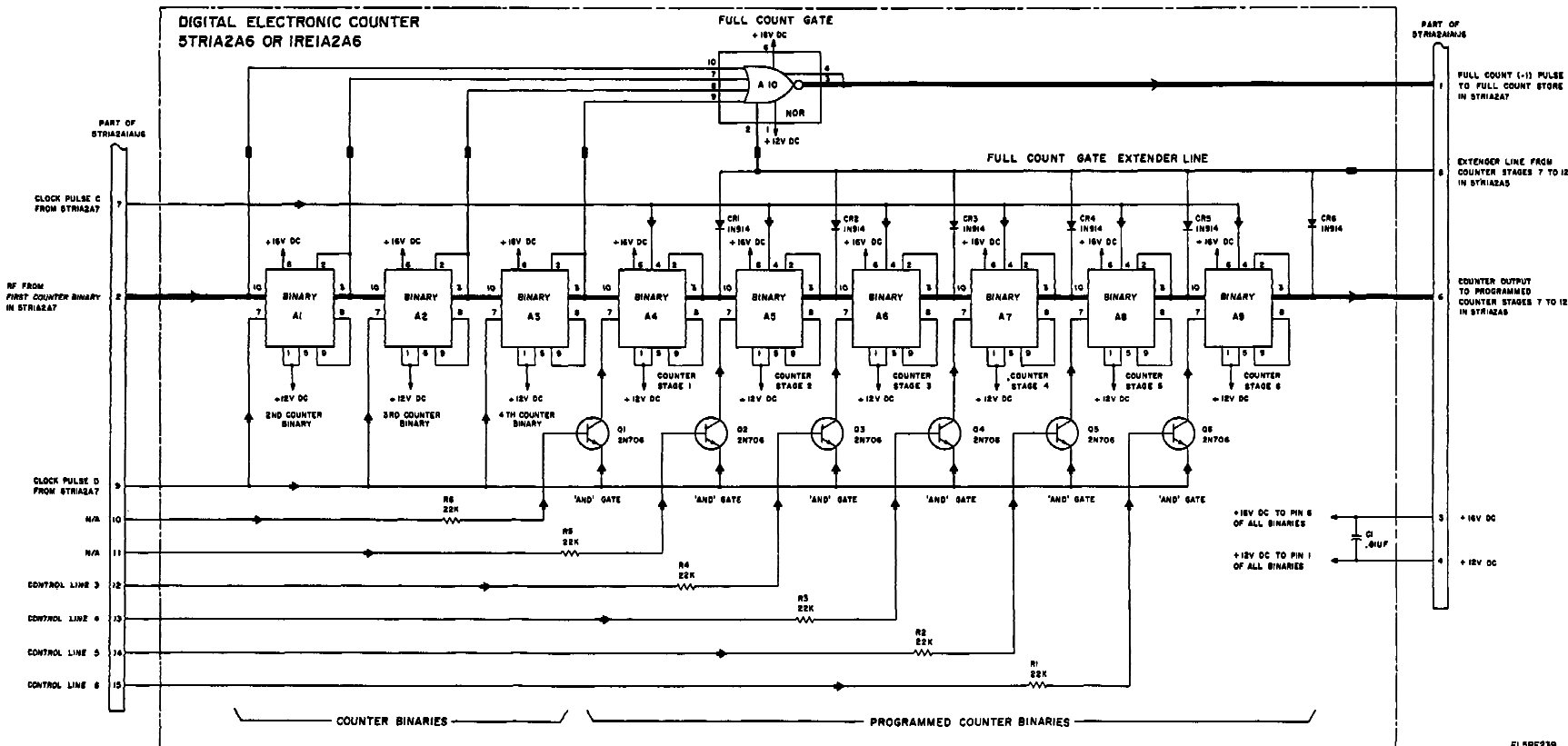
1-

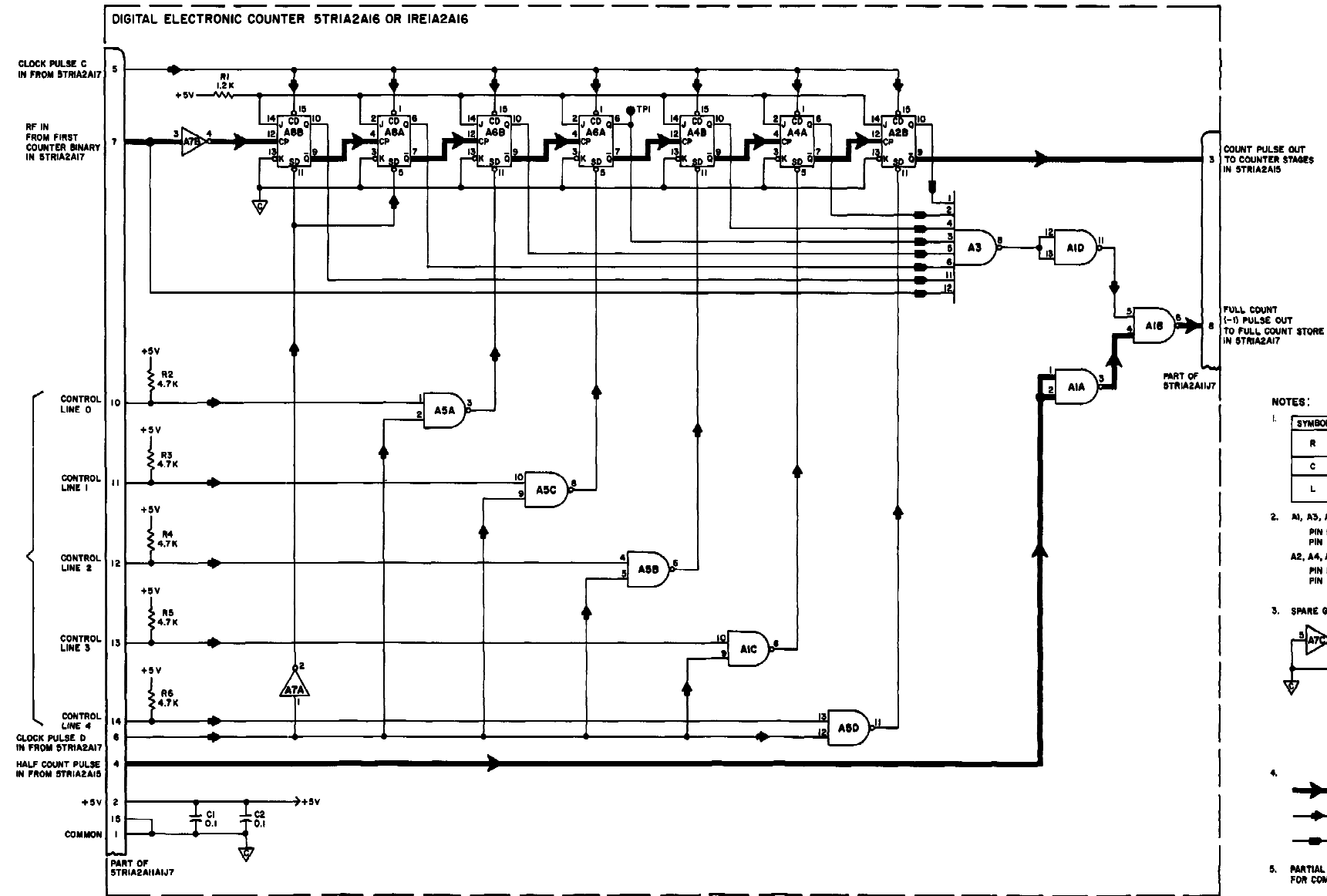
| SYMBOL | DEFINITION | UNIT                              |
|--------|------------|-----------------------------------|
| R      | RESISTOR   | OHM<br>KILOHM<br>MEGOM            |
| C      | CAPACITOR  | PICOFARAD<br>MICROFARAD           |
| L      | INDUCTOR   | MICROHENRY<br>MILLIHENRY<br>HENRY |



3-

THE VOLTAGES SHOWN ARE THOSE USED IN THE TRANSMITTER. FOR RECEIVER CONVERT AS FOLLOWS:  
TRANSMITTER: +16V DC  
RECEIVER: +4V DC  
OV



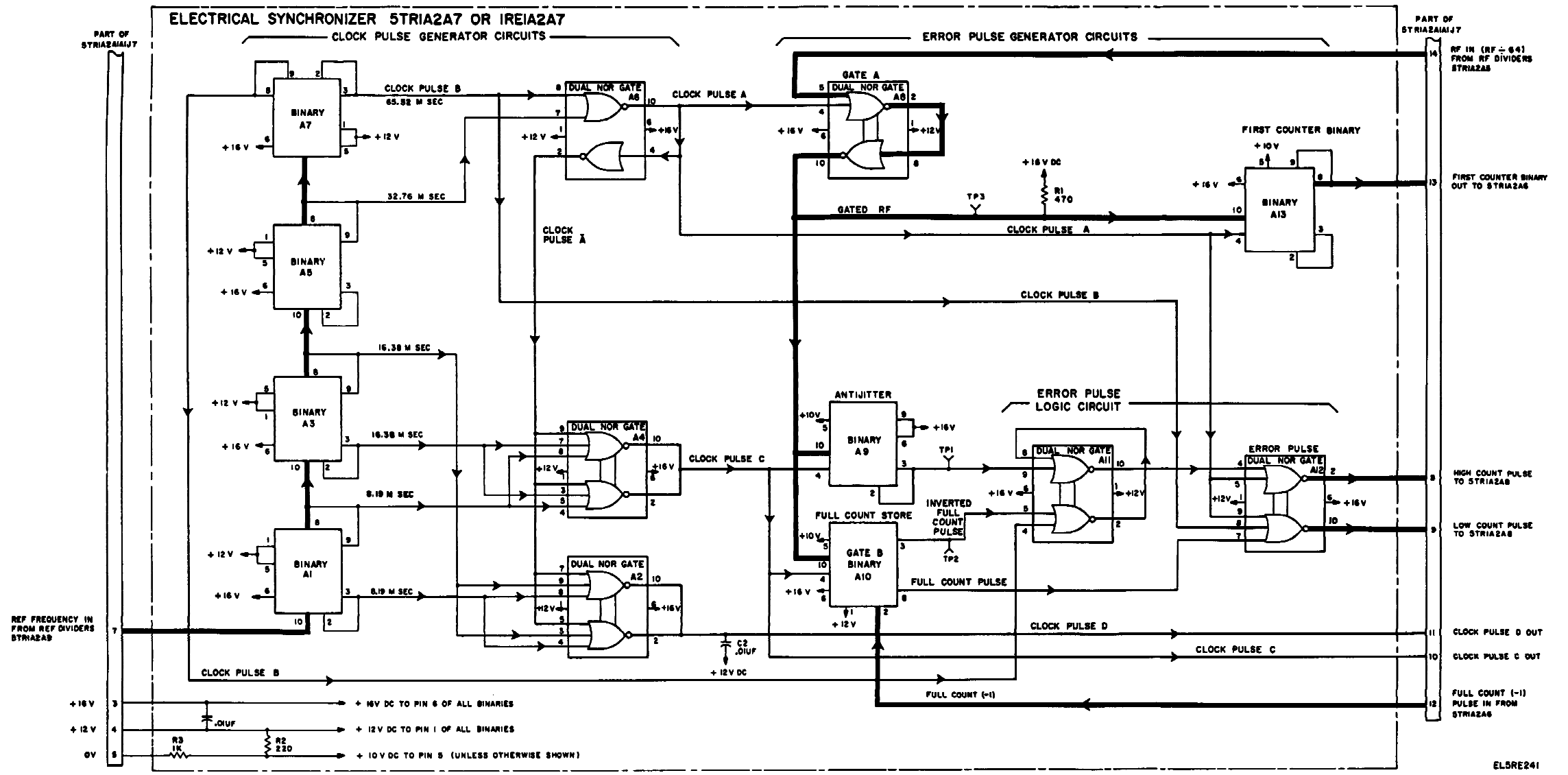


- NOTES
- | SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEGOMH           |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |
  - MAJOR FUNCTIONAL FLOW

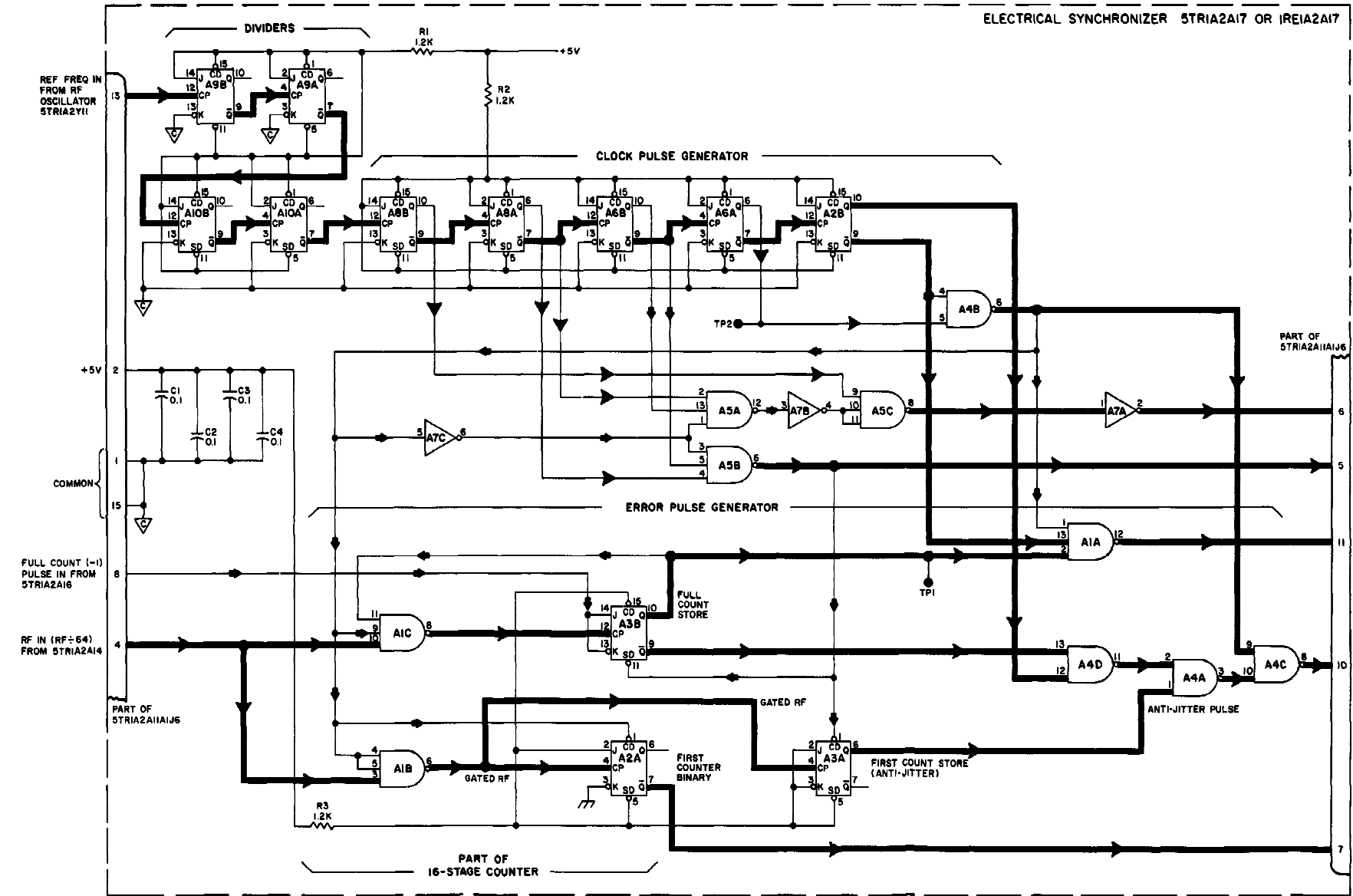
CLOCK PULSE FLOW

SECONDARY FUNCTIONAL FLOW
  - THE VOLTAGES SHOWN ARE THOSE USED IN THE TRANSMITTER. FOR RECEIVER CONVERT AS FOLLOWS:

| TRANSMITTER | RECEIVER |
|-------------|----------|
| +16 V DC    | +4 V DC  |
| +12 V DC    | 0V       |
| +10 V DC    | -2 V DC  |
| 0V          | -12 V DC |



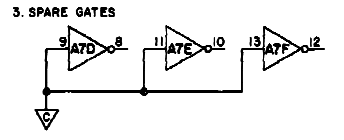
FO-4-13. Electrical Synchronizer 5TR1A2A7 or 1RE1A2A7 Schematic Diagram.



NOTES:

| SYMBOL | DESIGNATION    | UNIT                               |
|--------|----------------|------------------------------------|
| R      | NONE<br>K<br>M | OHM<br>KILOHM<br>MEG OHM           |
| C      | pF<br>NONE     | PICOPFARAD<br>MICROFARAD           |
| L      | NONE<br>mH     | MICROHENRY<br>MILLI HENRY<br>HENRY |

- 2. A1, A4, A5, A7  
PIN 14 +5V  
PIN 7 COMMON  
A2, A3, A6, A8, A9, A10  
PIN 16 +5V  
PIN 8 COMMON



- 4. MAJOR FUNCTIONAL FLOW. (thick arrow)
- SECONDARY FUNCTIONAL FLOW. (medium arrow)
- GATING OR SYNCHRONIZING SIGNAL. (thin arrow)

FO-4-14. Electrical Synchronizer 5TR1A2A17 or 1RE1A2A17, Schematic Diagram.

EL5RE242



NOTES

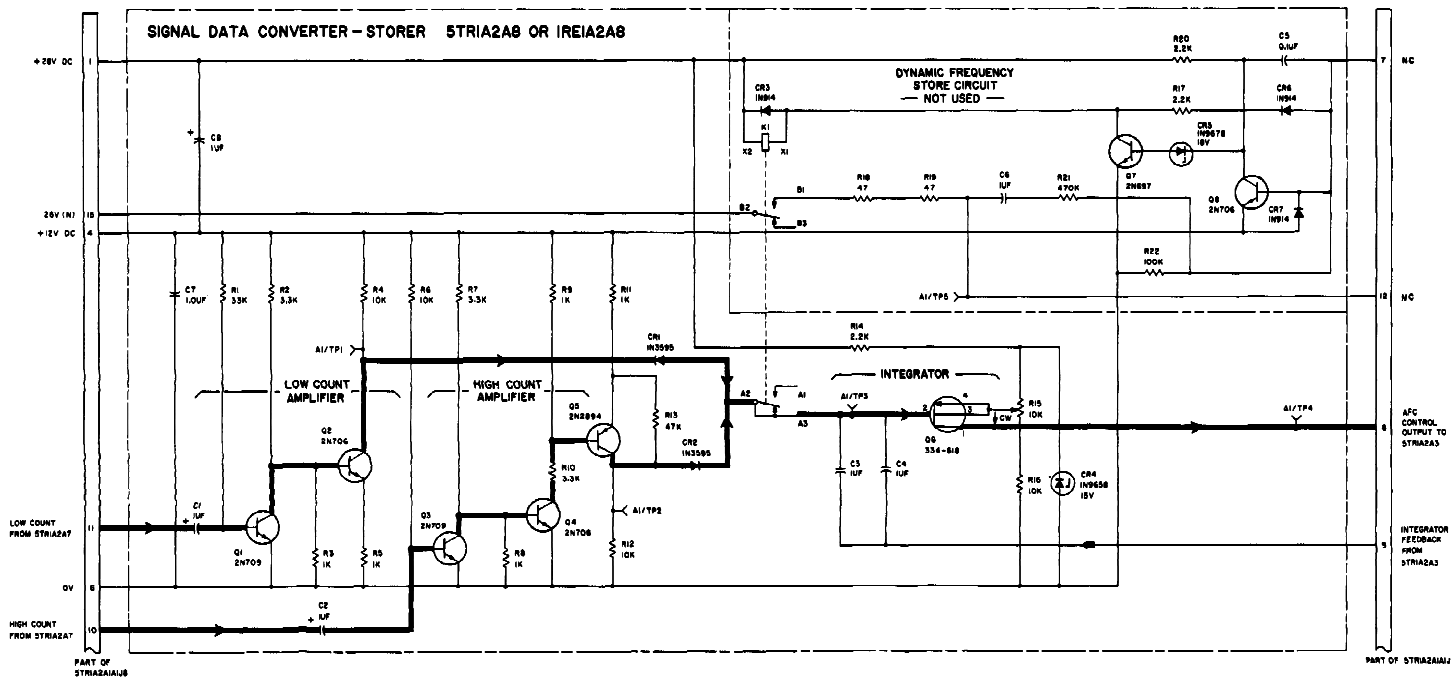
| SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM          |
| C      | NONE<br>P       | PICOFARAD<br>PICOFARAD            |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHEMPY<br>HENRY |

2 RELAY BASE PINS AS VIEWED FROM PIN END.



3 MAJOR FUNCTIONAL FLOW REFERENCE SIGNAL VOLTAGE

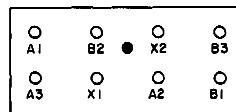
4 THE VOLTAGES ARE THOSE USED IN THE TRANSMITTER.  
FOR RECEIVER CONVERT AS FOLLOWS:  
TRANSMITTER RECEIVER  
+28V DC +12V DC  
+12V DC 0V  
0V -12V DC



NOTES:

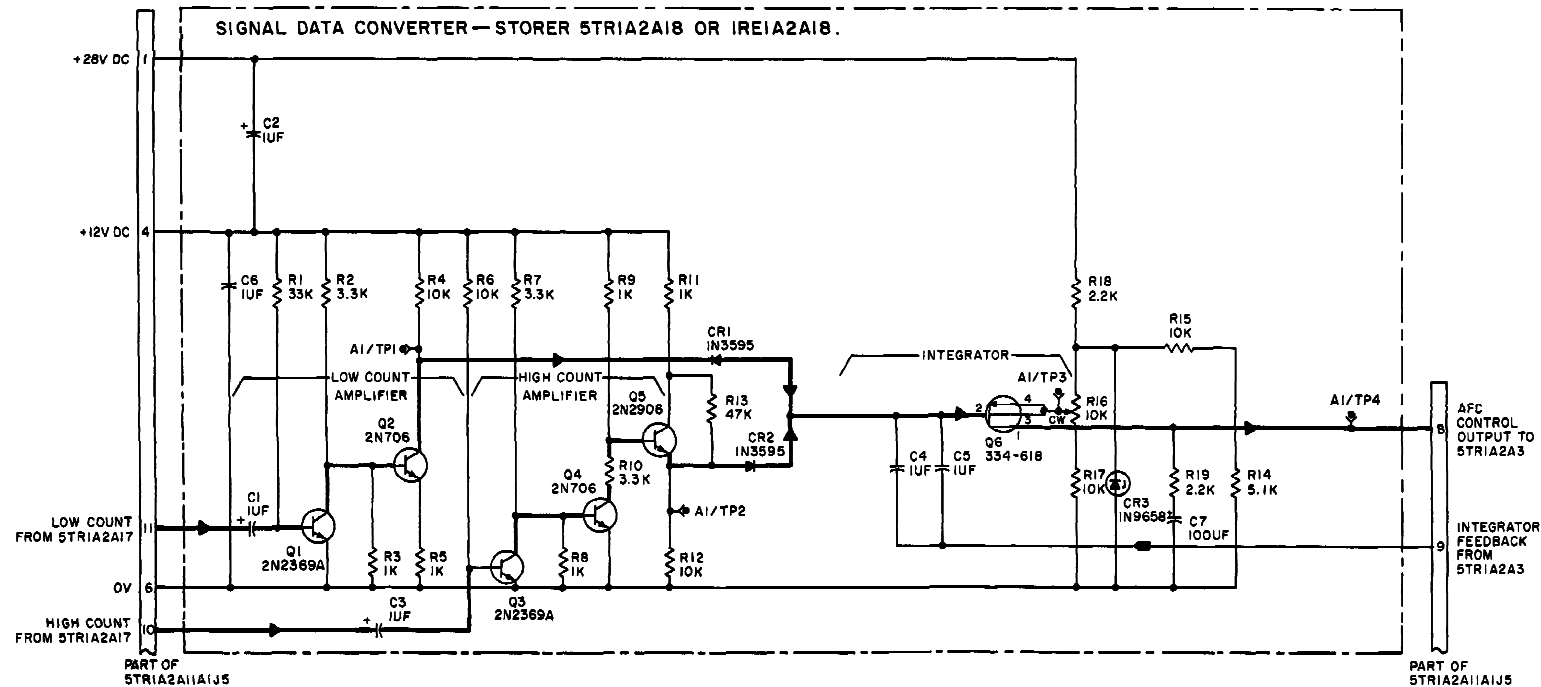
| 1- | SYMBOL | DESIGNATION     | UNIT                              |
|----|--------|-----------------|-----------------------------------|
|    | R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEGOHM           |
|    | C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
|    | L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

2- RELAY BASE PINS AS VIEWED FROM PIN END



3- MAJOR FUNCTIONAL FLOW.  
 REFERENCE SIGNAL VOLTAGE.

4- THE VOLTAGES ARE THOSE USED IN THE TRANSMITTER.  
 FOR RECEIVER CONVERT AS FOLLOWS:  
 TRANSMITTER RECEIVER  
 +28V DC +12V DC  
 +12V DC 0V  
 0V -12V DC



EL5 RE244

**FREQUENCY DIVIDER 5TR1A2A9 OR 1RE1A2A9**

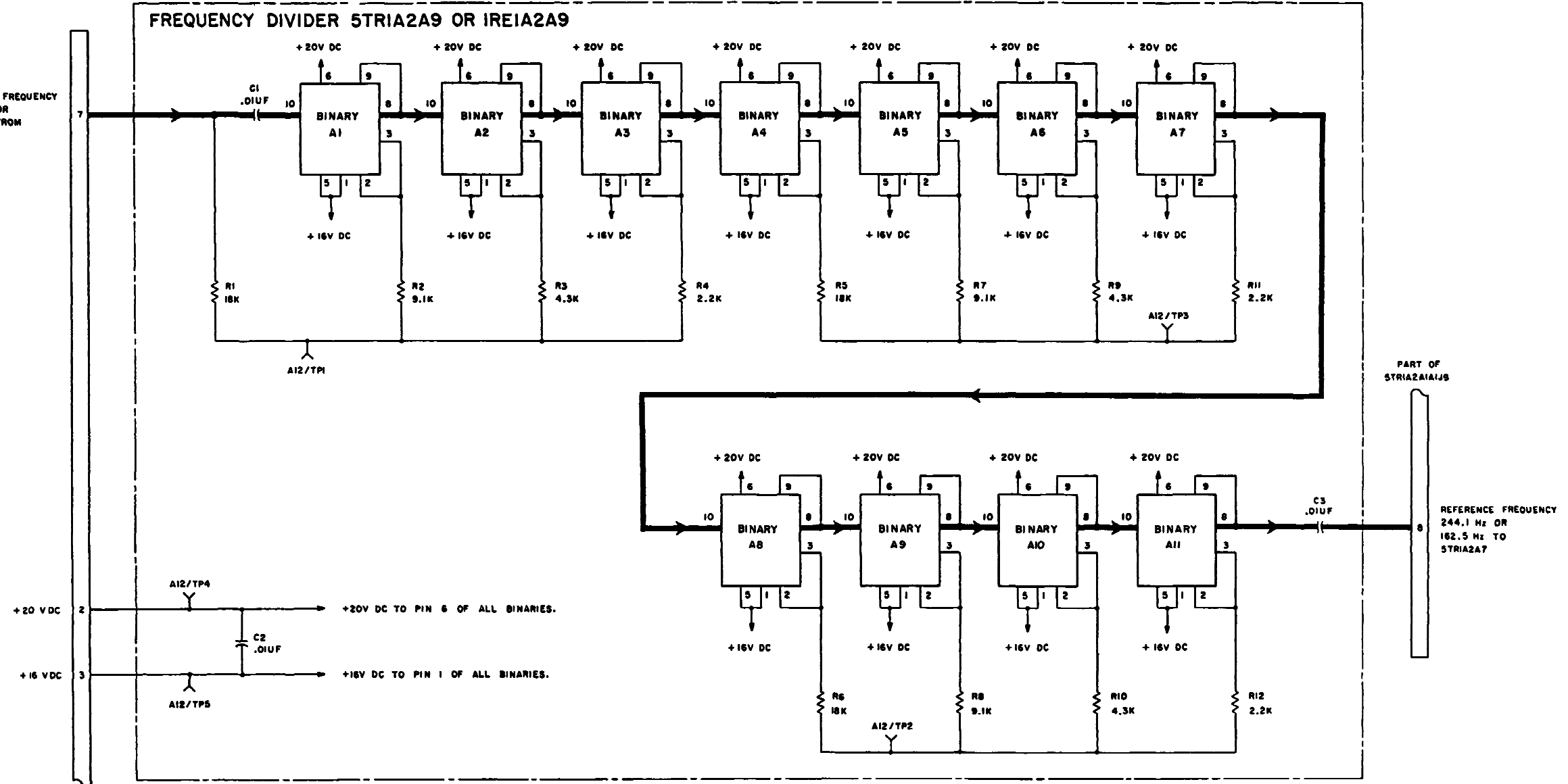
NOTES

- | SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM          |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

2. MAJOR FUNCTIONAL FLOW

3. THE VOLTAGES SHOWN ARE THOSE FOR TRANSMITTER. FOR RECEIVER CONVERT AS FOLLOWS:  
 TRANSMITTER      RECEIVER  
 +20V DC              +8V DC  
 +16V DC              +4V DC

REFERENCE FREQUENCY  
 500 KHz OR  
 333 KHz FROM  
 5TR1A2V1



PART OF  
 5TR1A2A1A9S

PART OF  
 5TR1A2A1A9S

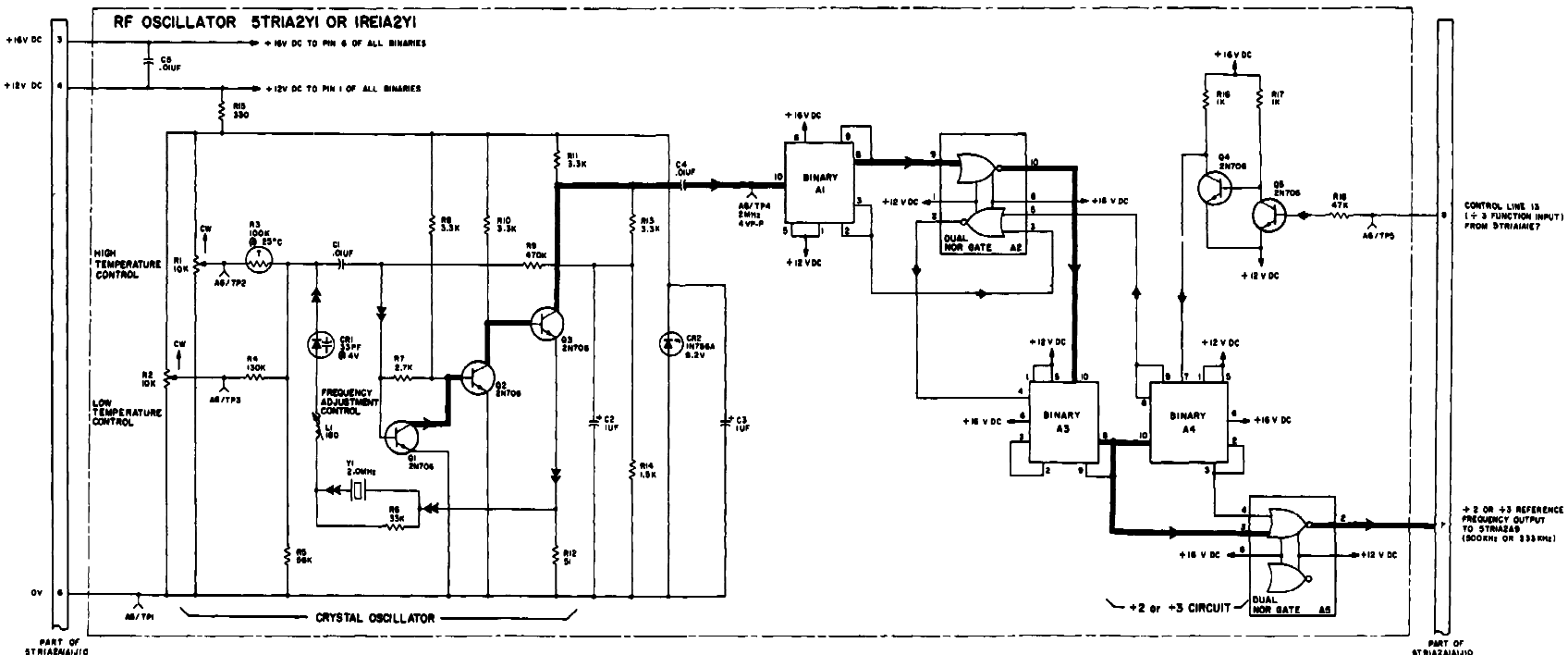
REFERENCE FREQUENCY  
 244.1 Hz OR  
 162.5 Hz TO  
 5TR1A2A7

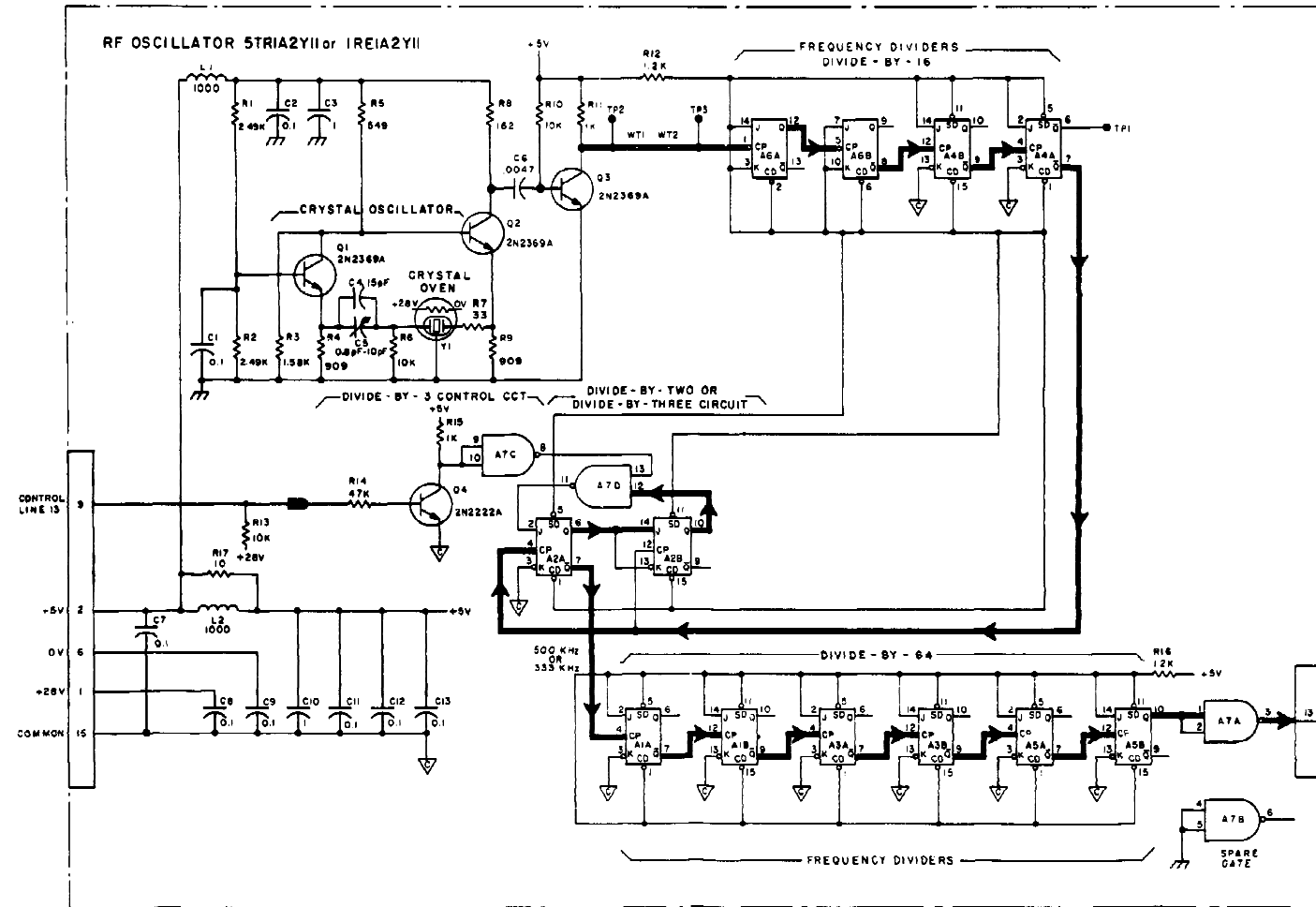
NOTES

| SYMBOL | DESIGNATION     | UNIT                               |
|--------|-----------------|------------------------------------|
| R      | NONE<br>K<br>M  | OHMS<br>KILOHMS<br>MEG OHMS        |
| C      | NONE<br>UF      | POICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLI HENRY<br>HENRY |

- 2. MAJOR FUNCTIONAL FLOW
- FEEDBACK SIGNAL PATH
- GATING OR SYNCHRONIZING SIGNAL

3. THE VOLTAGES SHOWN ARE THOSE USED IN THE TRANSMITTER. FOR RECEIVER CONVERT AS FOLLOWS  
 +16V DC → +4V DC  
 +12V DC → 0V  
 0V → +12V DC





NOTES :

1-

| SYMBOL | DESIGNATION | UNIT        |
|--------|-------------|-------------|
| R      | NONE        | OHM         |
|        | K           | KILOHM      |
|        | M           | MEG OHM     |
| C      | pF          | PICOFARAD   |
|        | NONE        | MICROFARAD  |
| L      | NONE        | MICROHENRY  |
|        | m           | MILLI HENRY |
|        | H           | HENRY       |

2-

| REFERENCE DESIGNATION | SUPPLY VOLTAGE |        |
|-----------------------|----------------|--------|
|                       | +5V            | COMMON |
| A1, A2, A3, A4, A5    | PIN 16         | PIN 8  |
| A6                    | PIN 4          | PIN 11 |
| A7                    | PIN 14         | PIN 7  |

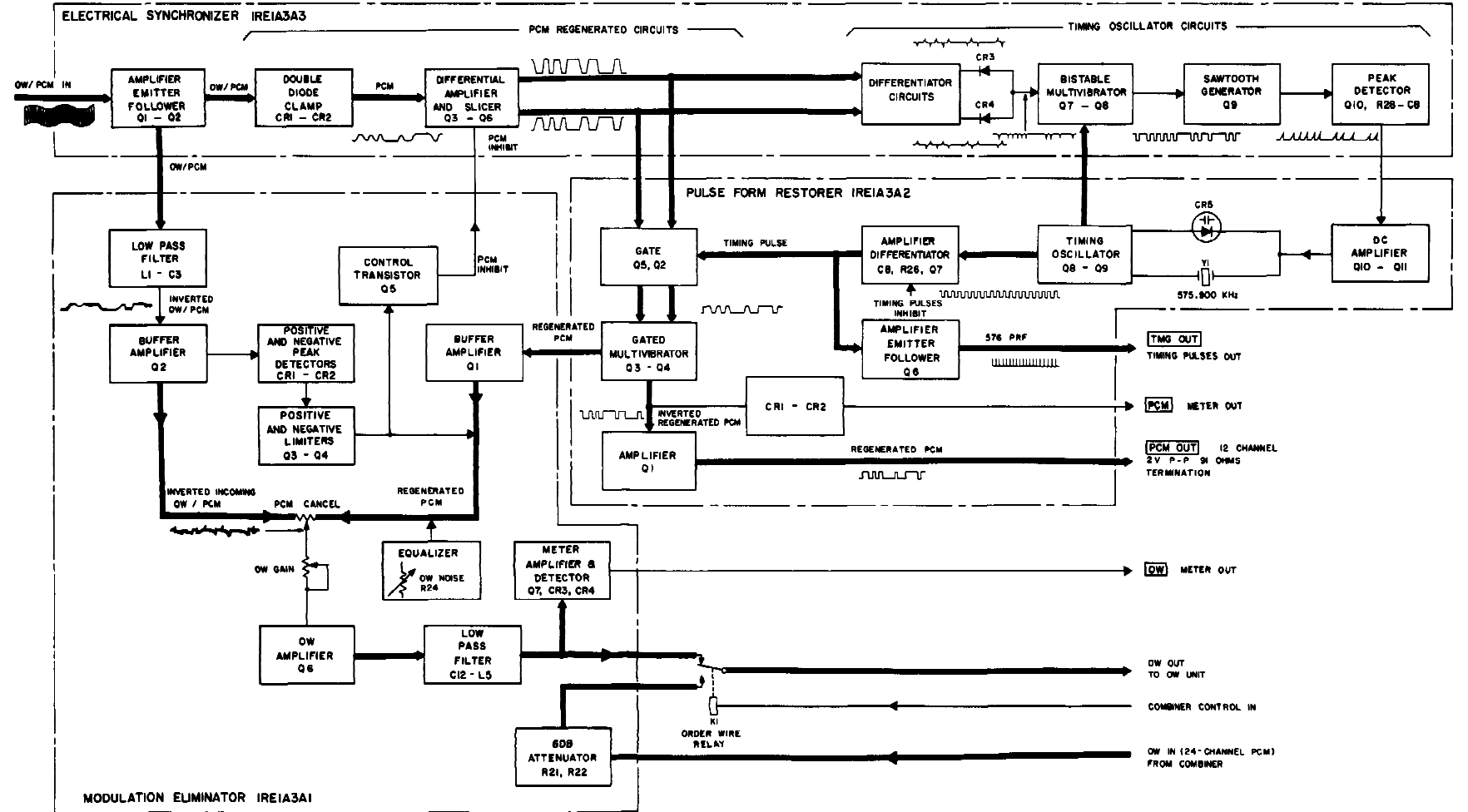
3- THE VOLTAGES SHOWN ARE THOSE USED IN THE TRANSMITTER, FOR RECEIVER CONVERT AS FOLLOWS:

| TRANSMITTER | RECEIVER |
|-------------|----------|
| 0V          | -12V     |
| +12V        | 0V       |
| +28V        | +12V     |
| +5V         | +5V      |
| +11.5V      | +12V     |

➔ MAJOR FUNCTIONAL FLOW  
 ➔ REFERENCE SIGNAL VOLTAGE

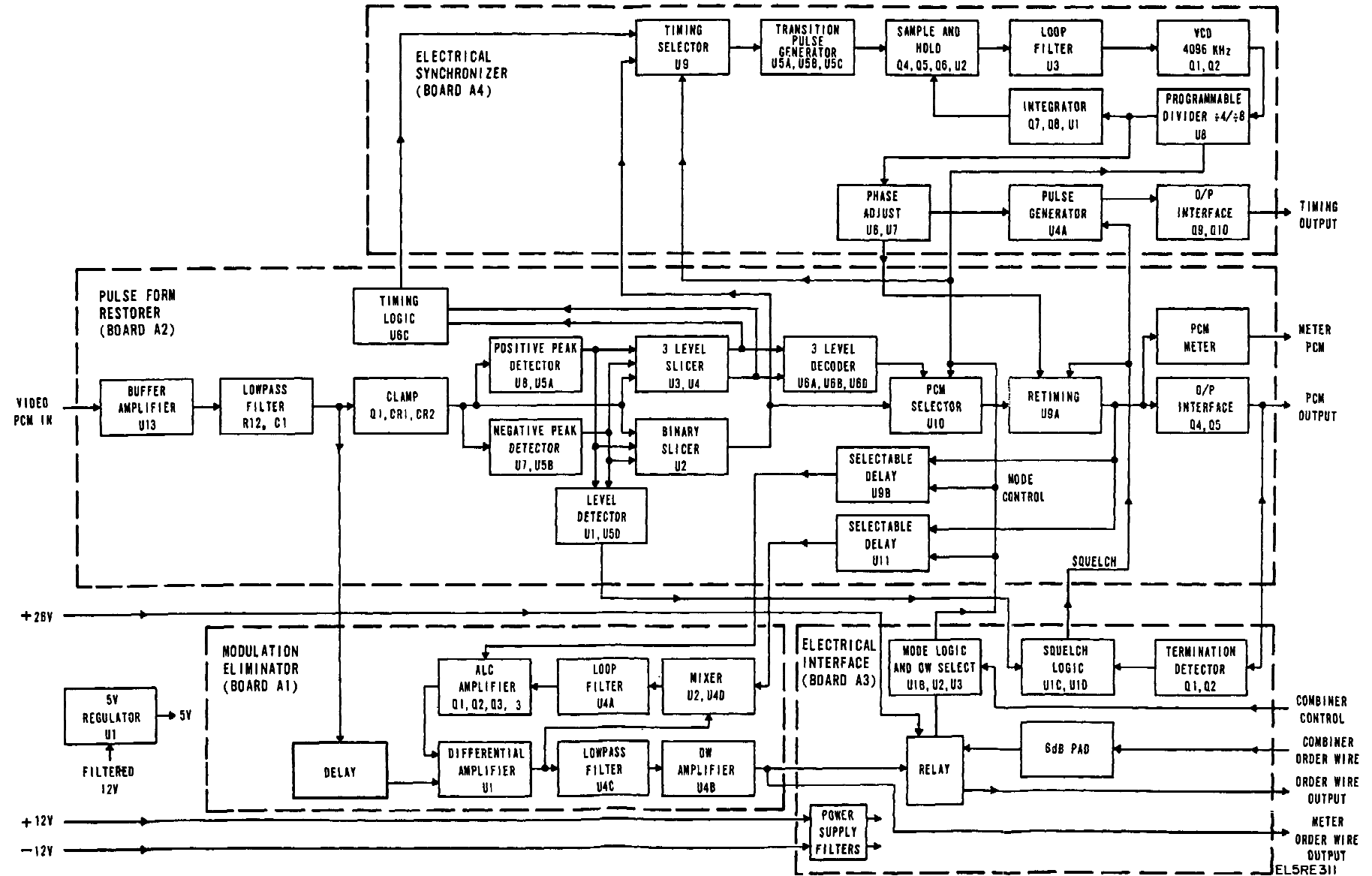
EL59E247

FO-4-19. Rf Oscillator 5TR1A2Y11 or 1RE1A2Y11, Schematic Diagram.



EL5RE248

FO-4-20. Pulse Form Restorer 1RE1A3, Block Diagram.

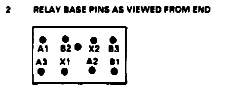


FO-4-20.1. Pulse Form Restorer 1RE1A3 (SM-D-990510, CMC PN 245-803110-000, Block Diagram.

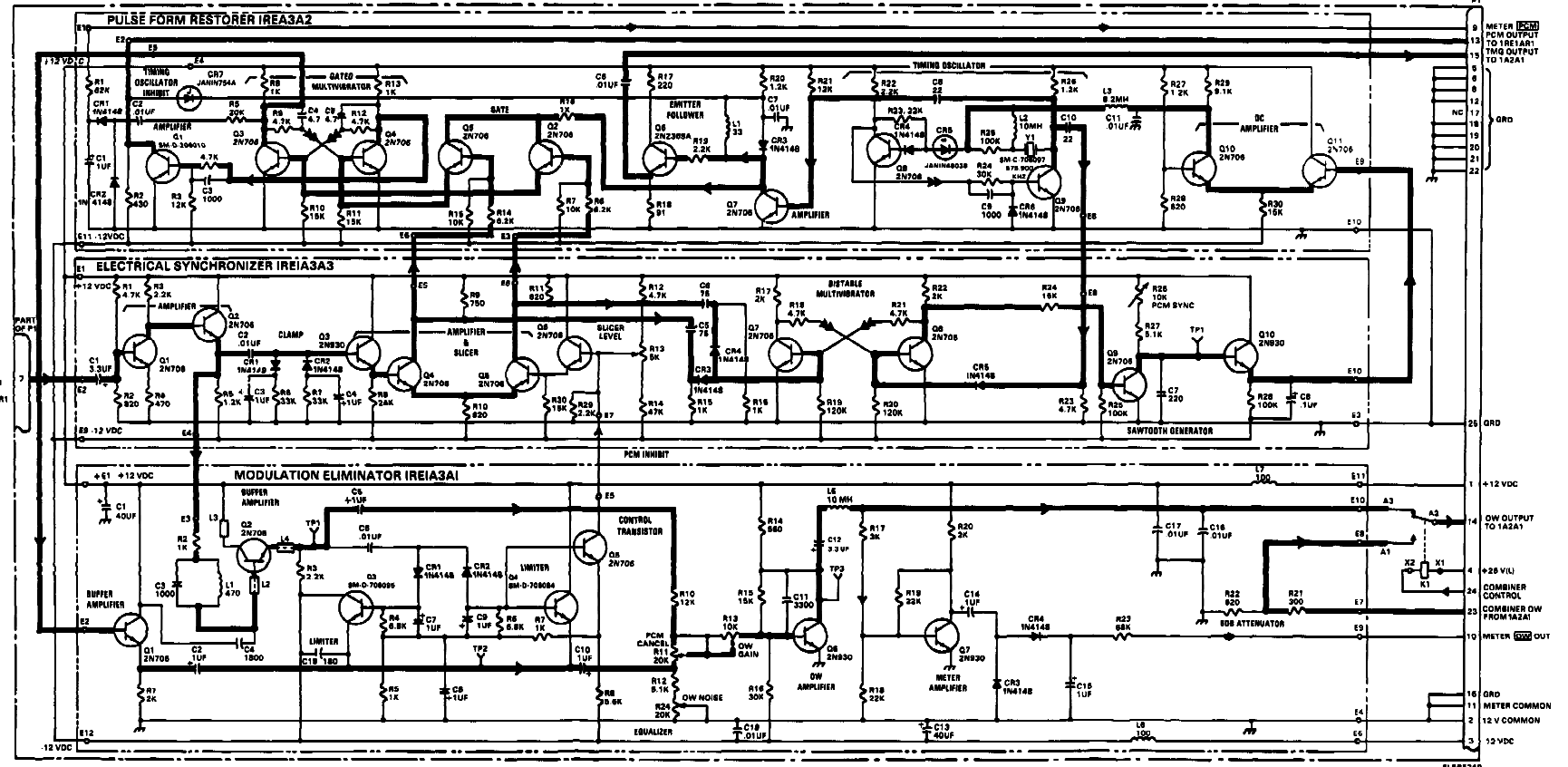
ELSRE311

NOTES

| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHM        |
| K      | NONE        | KILOHM     |
| M      | NONE        | MEG OHM    |
| C      | NONE        | PICOFARAD  |
| UF     | NONE        | MICROFARAD |
| L      | NONE        | MICROHENRY |
| H      | NONE        | HENRY      |

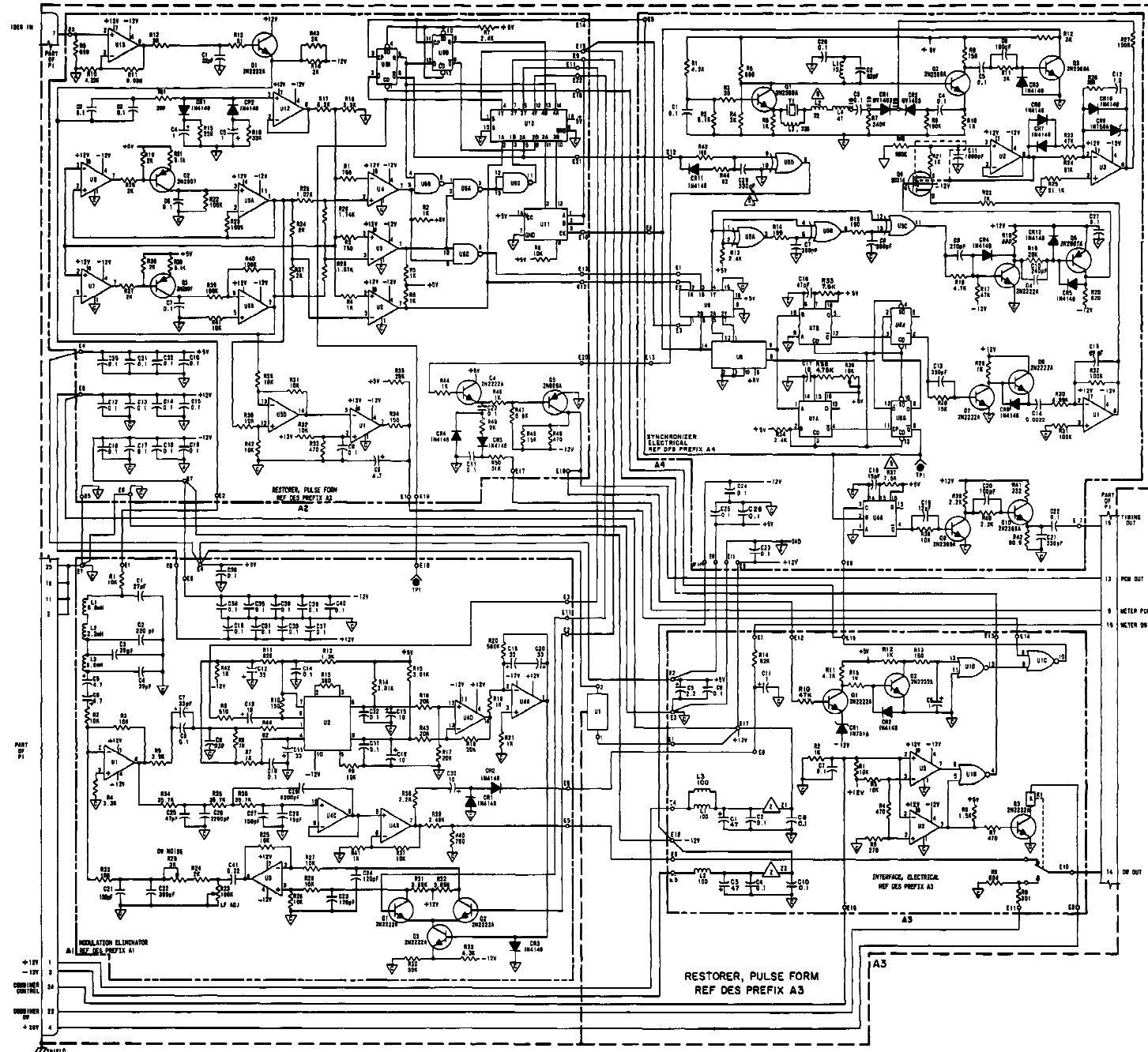


Pulse form restorer 1RE1A3, schematic diagram. (part No. prefixed by "0744A").



FO-4-21. Pulse Form Restorer 1RE1A3, Schematic Diagram.





**NOTES:**

| SYMBOL | DESCRIPTION | UNIT         |
|--------|-------------|--------------|
| R      | RESISTOR    | OHMS         |
| C      | CAPACITOR   | PIECES       |
| L      | INDUCTOR    | MICROHENRIES |

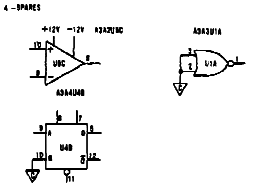
**WAVEFORM REFERENCE DESIGNATION**

| WAVEFORM | REF. DES. PREFIX | UNIT |
|----------|------------------|------|
| U4       | U13              | U3   |
| C4       | C20              | C11  |
| C5       | C24              | C12  |
| L3       | L3               | L4   |
| D3       | D3               | D10  |
| R44      | R18              | R45  |
| T1       | T1               | T1   |
| E11      | E7               | E20  |

REFERENCE DESIGNATION NOT USED  
ASAP4 TO C17

**REFERENCE DESIGNATION NOT USED**

| REFERENCE DESIGNATION | SUPPLY VOLTAGE |      |        |
|-----------------------|----------------|------|--------|
|                       | +12V           | -12V | COMMON |
| A104                  |                |      |        |
| A105                  |                |      |        |
| A106                  |                |      |        |
| A107                  |                |      |        |
| A108                  |                |      |        |
| A109                  |                |      |        |
| A110                  |                |      |        |
| A111                  |                |      |        |
| A112                  |                |      |        |
| A113                  |                |      |        |
| A114                  |                |      |        |
| A115                  |                |      |        |
| A116                  |                |      |        |
| A117                  |                |      |        |
| A118                  |                |      |        |
| A119                  |                |      |        |
| A120                  |                |      |        |
| A121                  |                |      |        |
| A122                  |                |      |        |
| A123                  |                |      |        |
| A124                  |                |      |        |
| A125                  |                |      |        |
| A126                  |                |      |        |
| A127                  |                |      |        |
| A128                  |                |      |        |
| A129                  |                |      |        |
| A130                  |                |      |        |
| A131                  |                |      |        |
| A132                  |                |      |        |
| A133                  |                |      |        |
| A134                  |                |      |        |
| A135                  |                |      |        |
| A136                  |                |      |        |
| A137                  |                |      |        |
| A138                  |                |      |        |
| A139                  |                |      |        |
| A140                  |                |      |        |



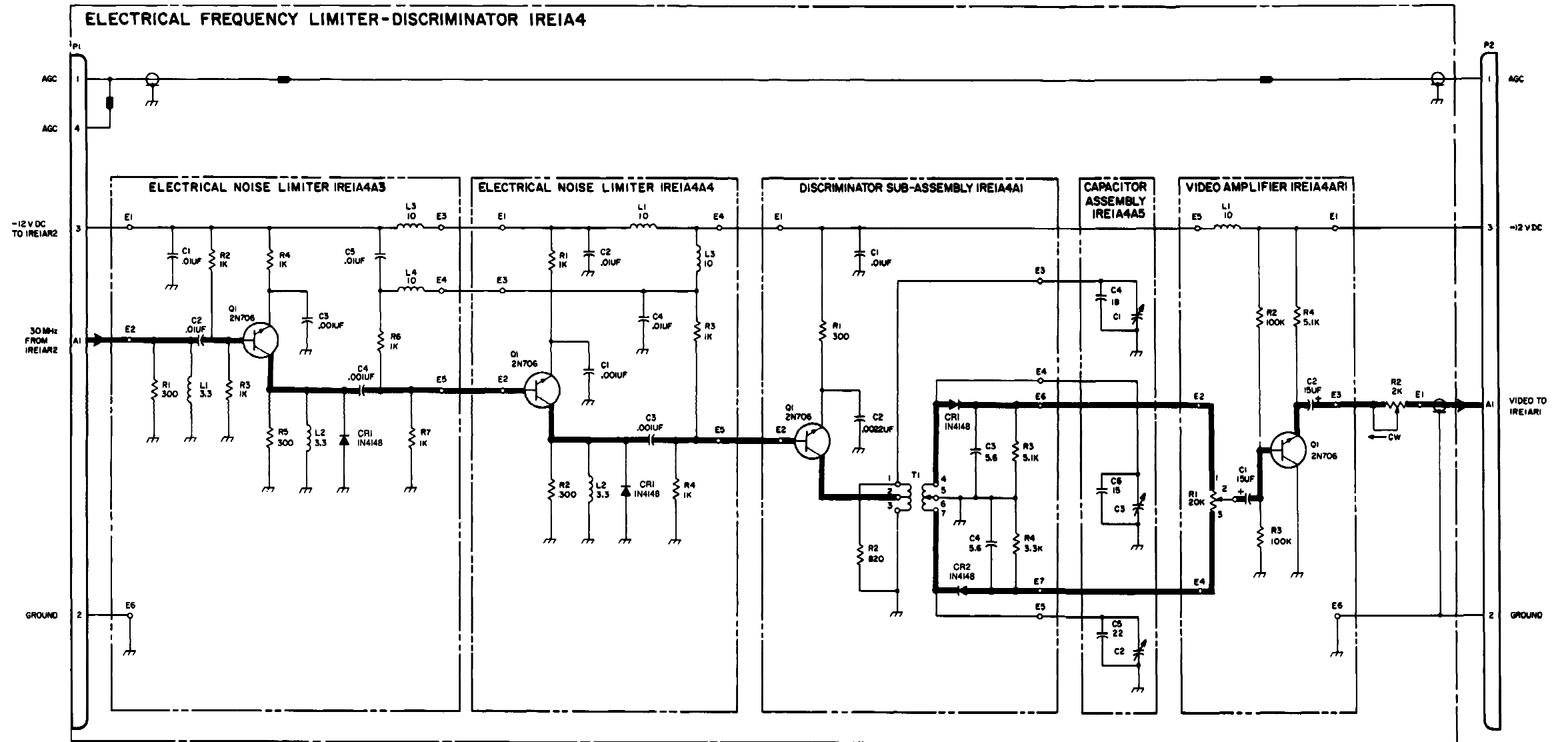
MINIMUM VALUE OF ASAP4, ASAP5 AND ASAP6  
SHALL BE REPLACED ON TEST BY VALUES GIVEN BELOW

| ASAP4   | ASAP5 | ASAP6  |
|---------|-------|--------|
| 0.04 IN | 19 IN | 200 IN |
| 10 IN   | 27 IN | 200 IN |

NOTES

| 1. SYMBOL | DESIGNATION     | UNIT                              |
|-----------|-----------------|-----------------------------------|
| R         | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM          |
| C         | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L         | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

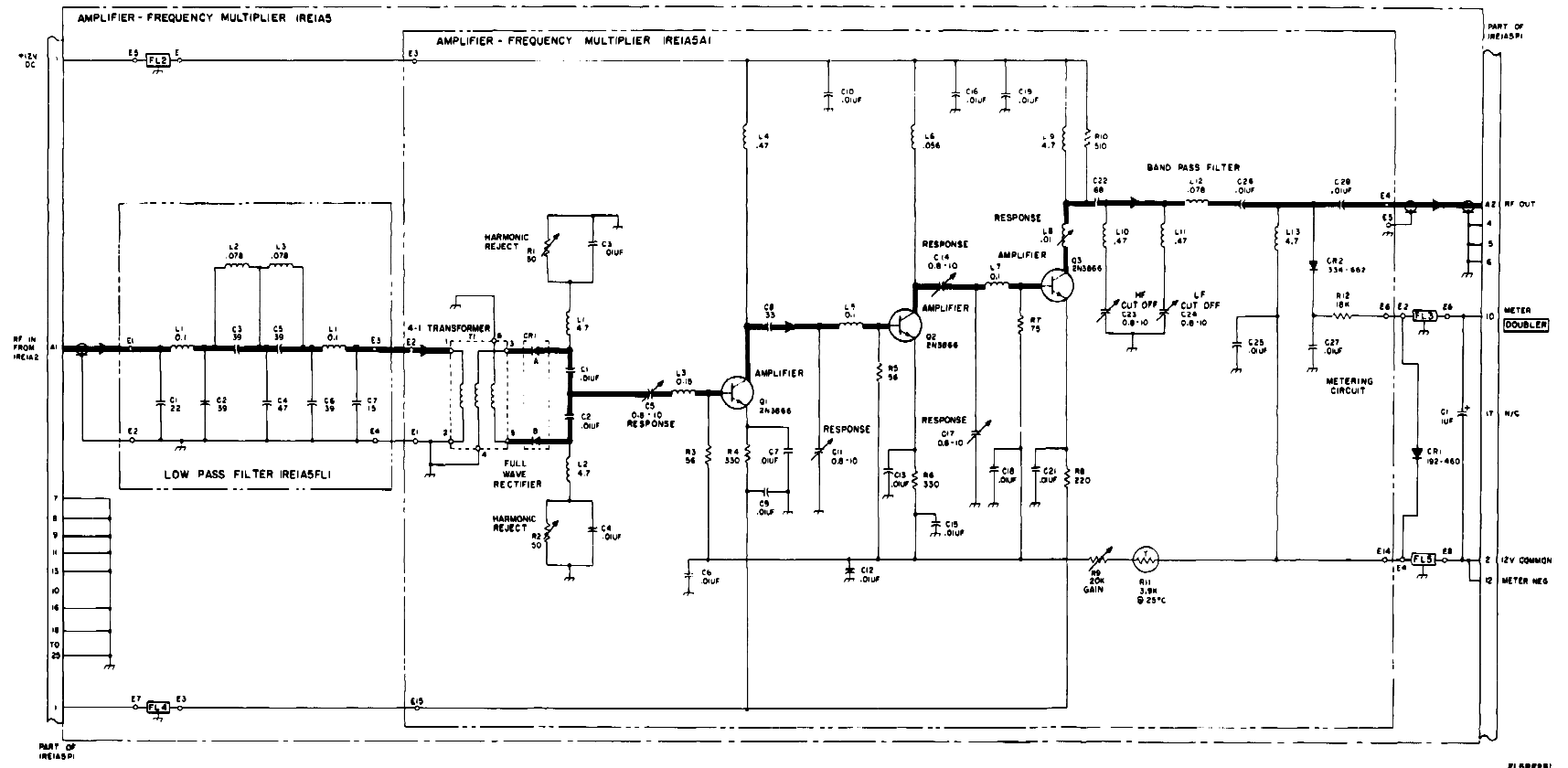
2. MAJOR FUNCTIONAL FLOW  
 REFERENCE SIGNAL VOLTAGE



NOTES

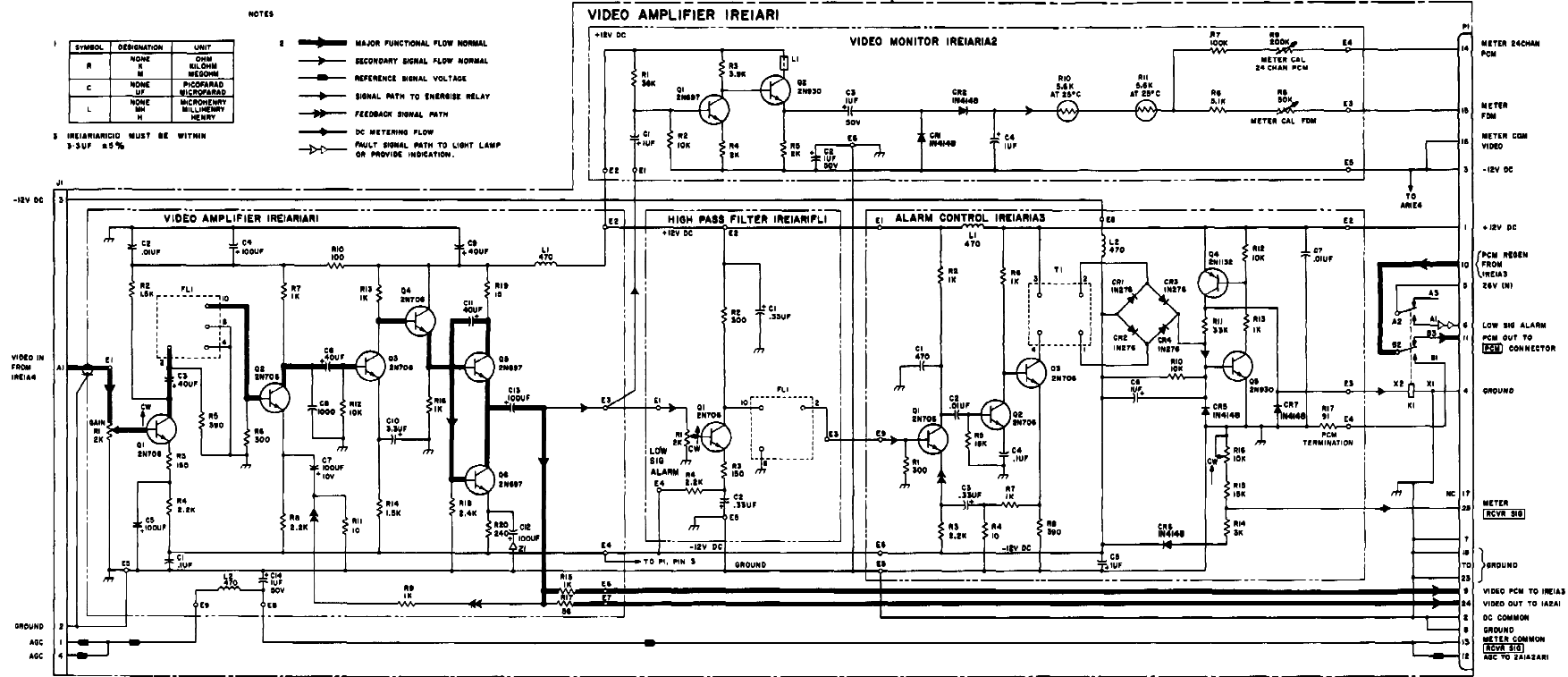
| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHM        |
|        | S           | KILOHM     |
|        | M           | MEGOM      |
| C      | NONE        | PICOFARAD  |
|        | UF          | MICROFARAD |
|        | MF          | MILLIFARAD |
| L      | NONE        | MICROHENRY |
|        | MH          | MILLIHENRY |
|        | H           | HENRY      |

2. DC METERING FLOW  
 MAJOR FUNCTIONAL FLOW  
 REFERENCE SIGNAL VOLTAGE

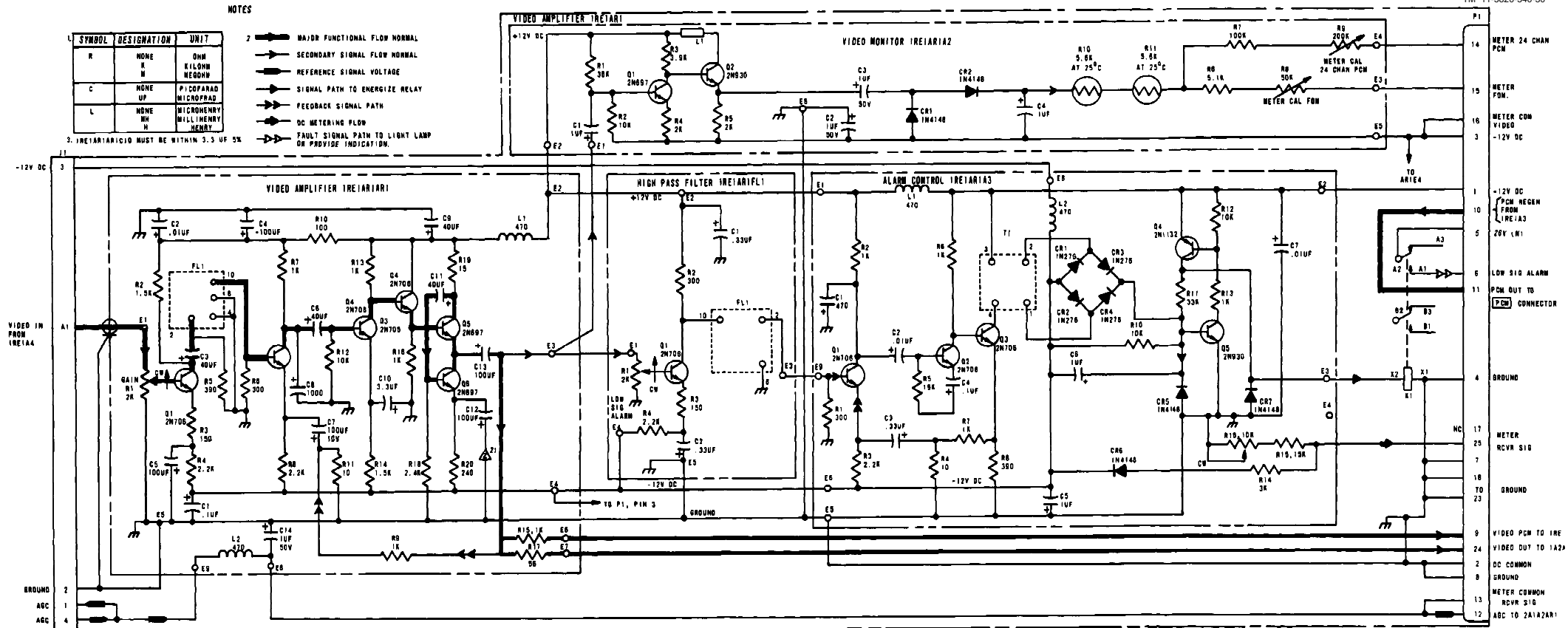


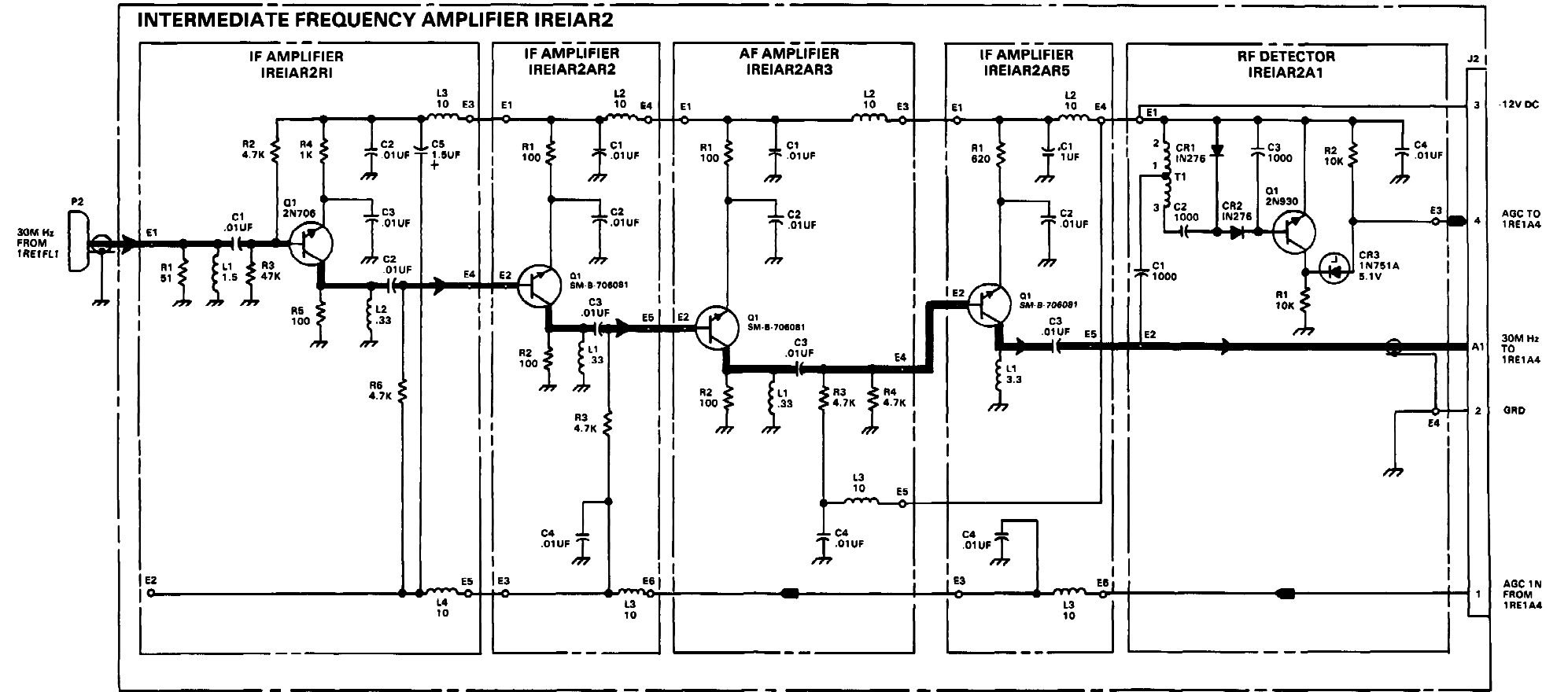
FO-4-23. Amplifier-Frequency Multiplier 1RE1A5, Schematic Diagram.

ELDRB:1



EL5RE252





NOTES

| SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEGOHM           |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

- 2- MAJOR FUNCTIONAL FLOW NORMAL  
 REFERENCE SIGNAL VOLTAGE

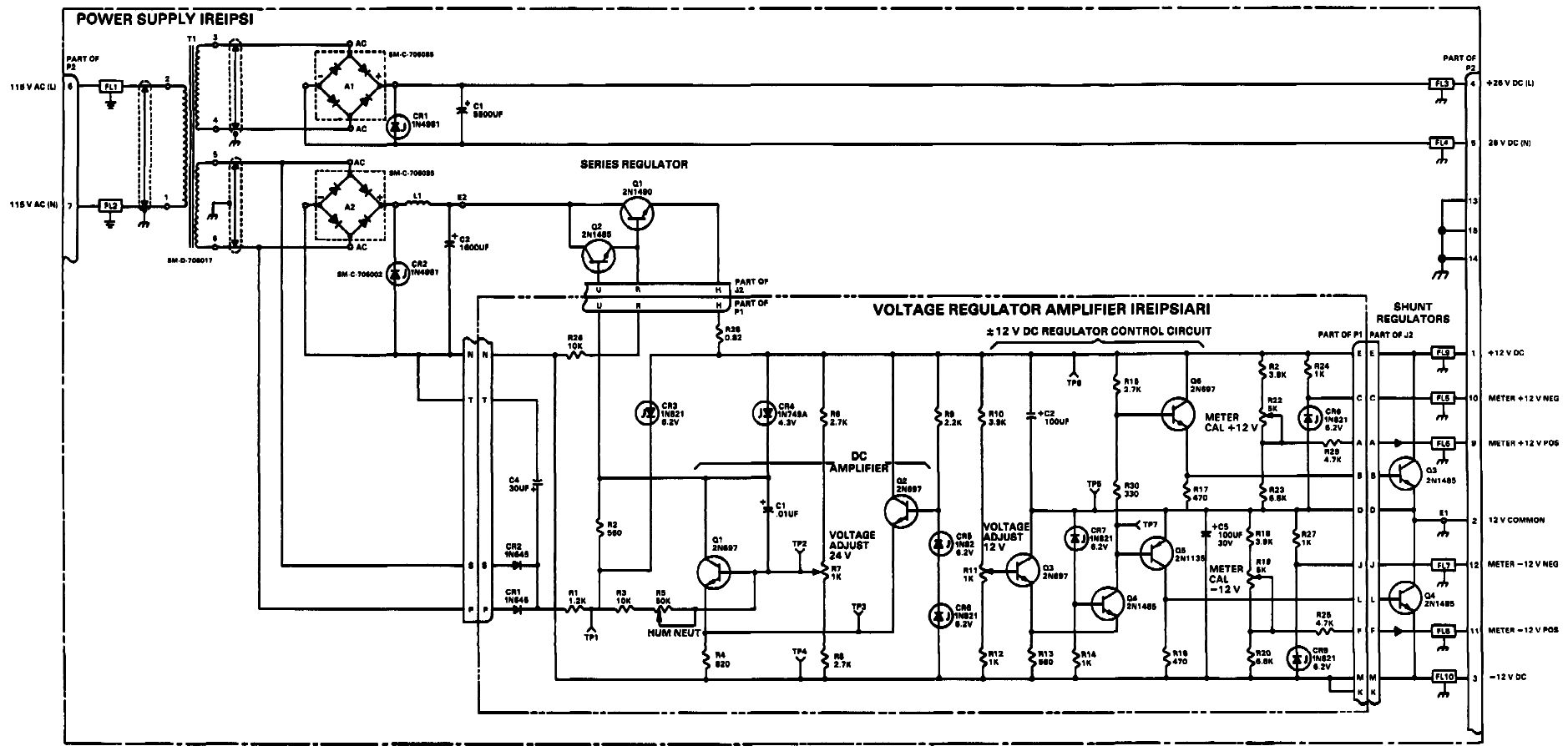
EL5RE254

NOTES

| SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM          |
| C      | NONE<br>UF      | PICOPFARAD<br>MICROFARAD          |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

2 → DC METERING FLOW

Figure 6-28. Power supply 1RE1PS1, schematic diagram. (part No. prefixed by "0744A").



FO-4-27. Power Supply 1RE1PS1, Schematic Diagram.

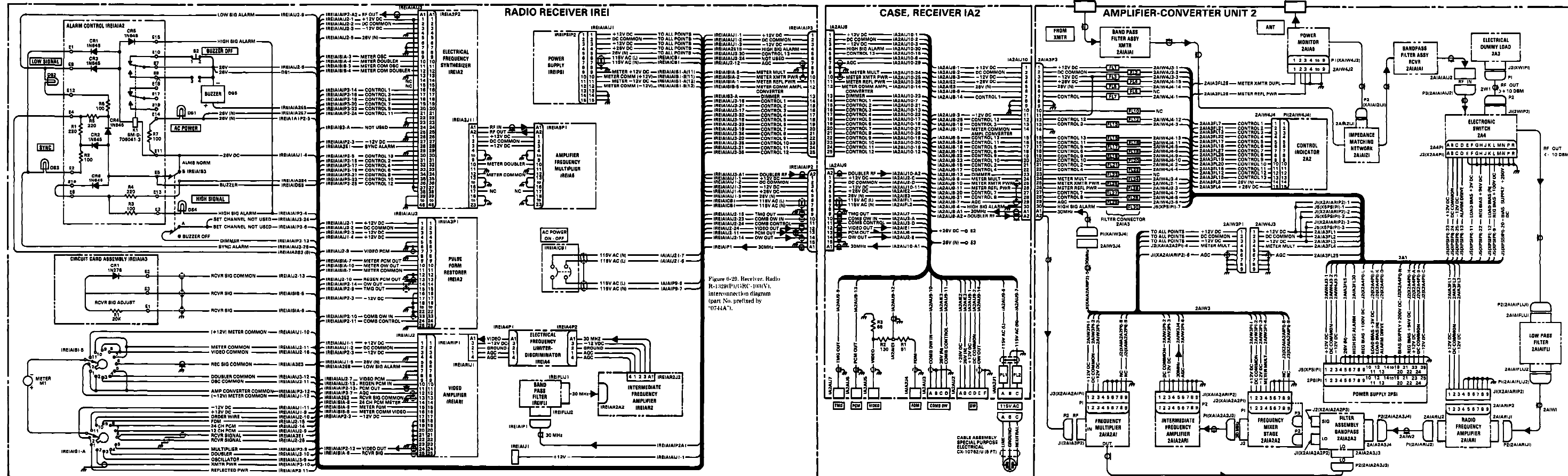
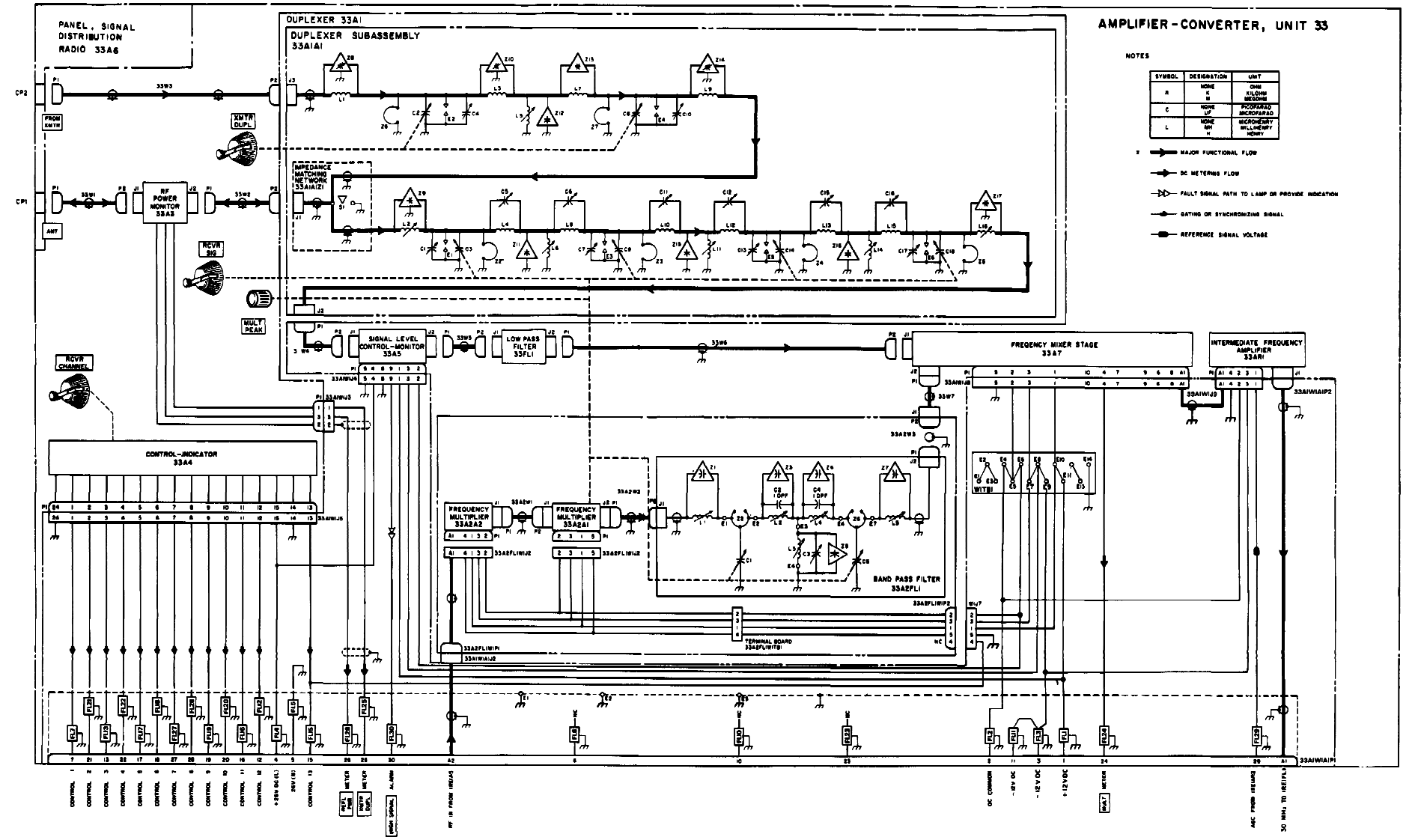
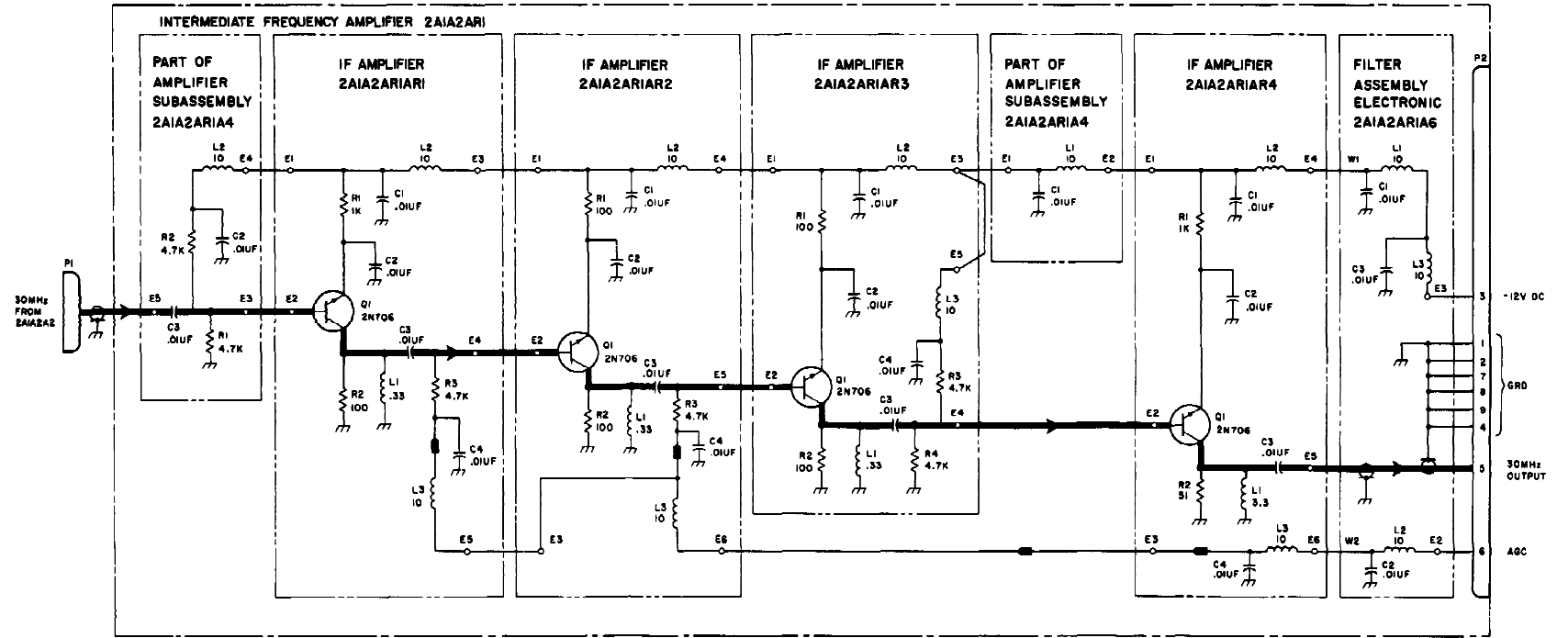


Figure 6-29. Receiver, Radio R-1329(P)(GRC-103V), Interconnecting diagram (part No. prefixed by 0744A).





FO-4-29. Receiver, Radio R-1329(P)/GRC-103(V), R-1329A(P)/GRC-103(V) or R-1329B(P)/GRC-103(V) and Intermediate Frequency Amplifier AM-4316A/GRC-103(V), Interconnecting Diagram.



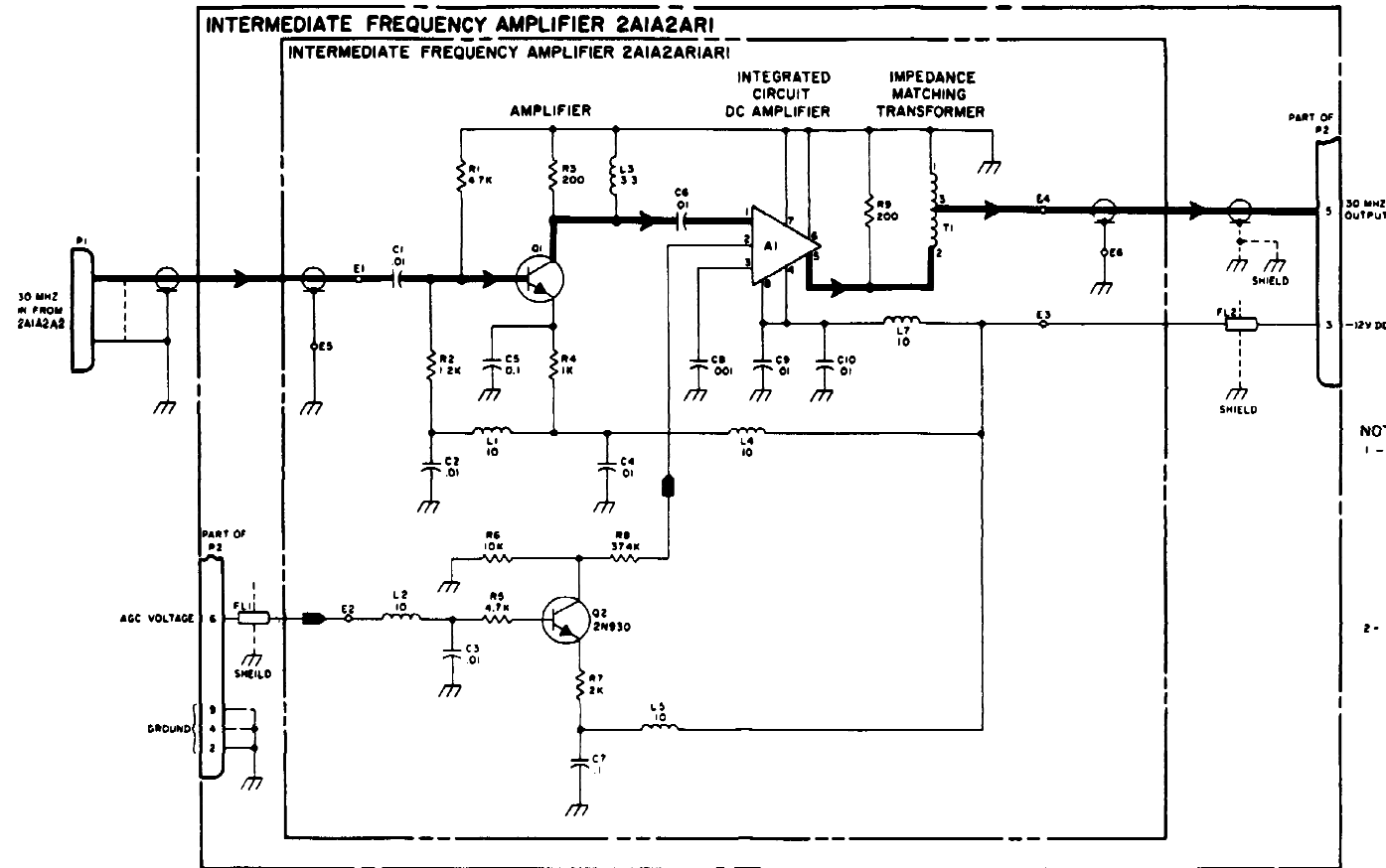
NOTES:

| SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM          |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

- 2. MAJOR FUNCTIONAL FLOW
- 3. REFERENCE SIGNAL VOLTAGE (AGC)

EL5RE258

FO#33



NOTES:

| 1 - SYMBOL | DESIGNATION     | UNIT                              |
|------------|-----------------|-----------------------------------|
| R          | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM          |
| C          | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L          | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

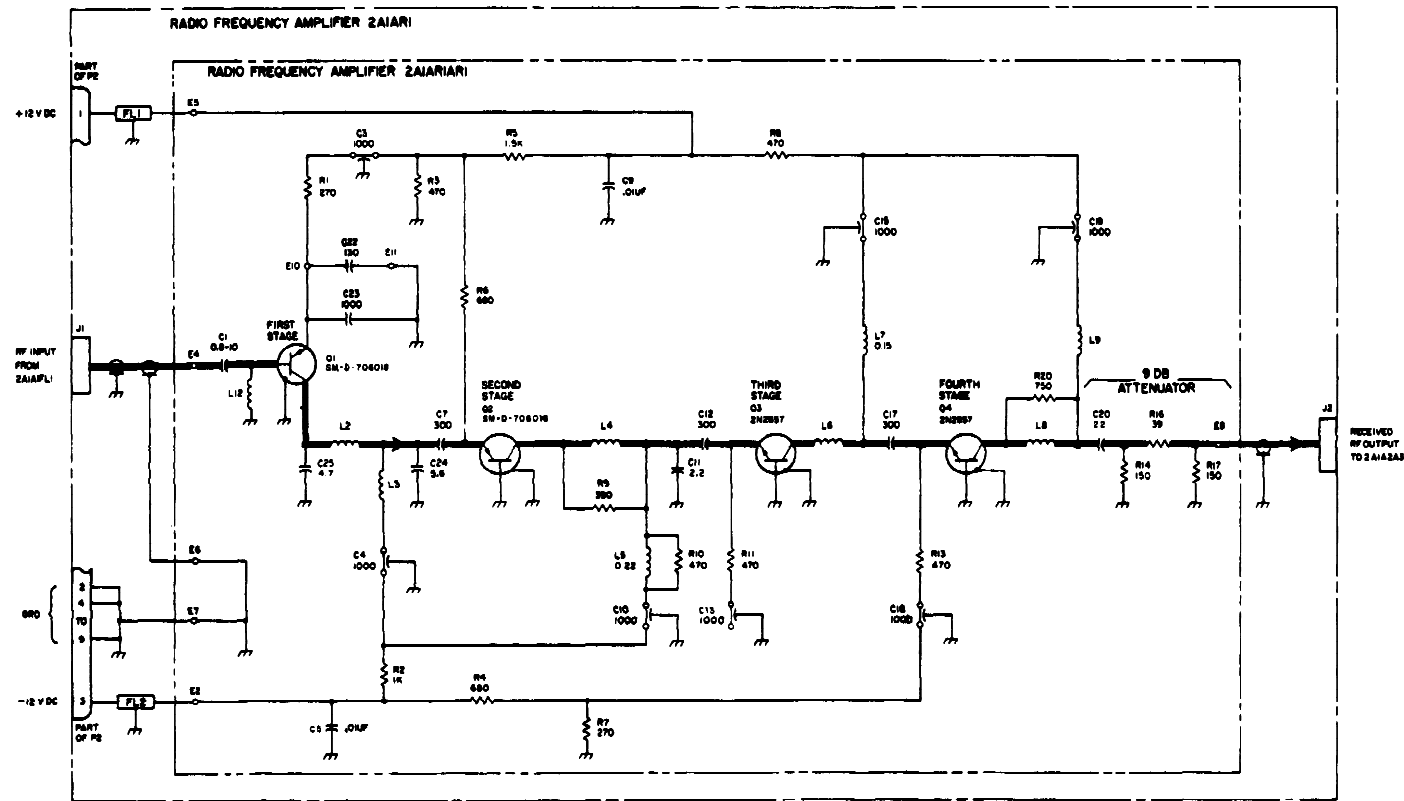
2 - MAJOR FUNCTIONAL FLOW  
 REFERENCE SIGNAL VOLTAGE (AGC)

ELSRE259

NOTES:







| SYMBOL | DESIGNATION | UNIT                               |
|--------|-------------|------------------------------------|
| R      | RESISTOR    | OHM<br>KILOHM<br>MEG OHM           |
| C      | CAPACITOR   | PICOFARAD<br>NEG OHM<br>MICROFARAD |
| L      | INDUCTOR    | MICROHENRY<br>MILLI HENRY<br>HENRY |

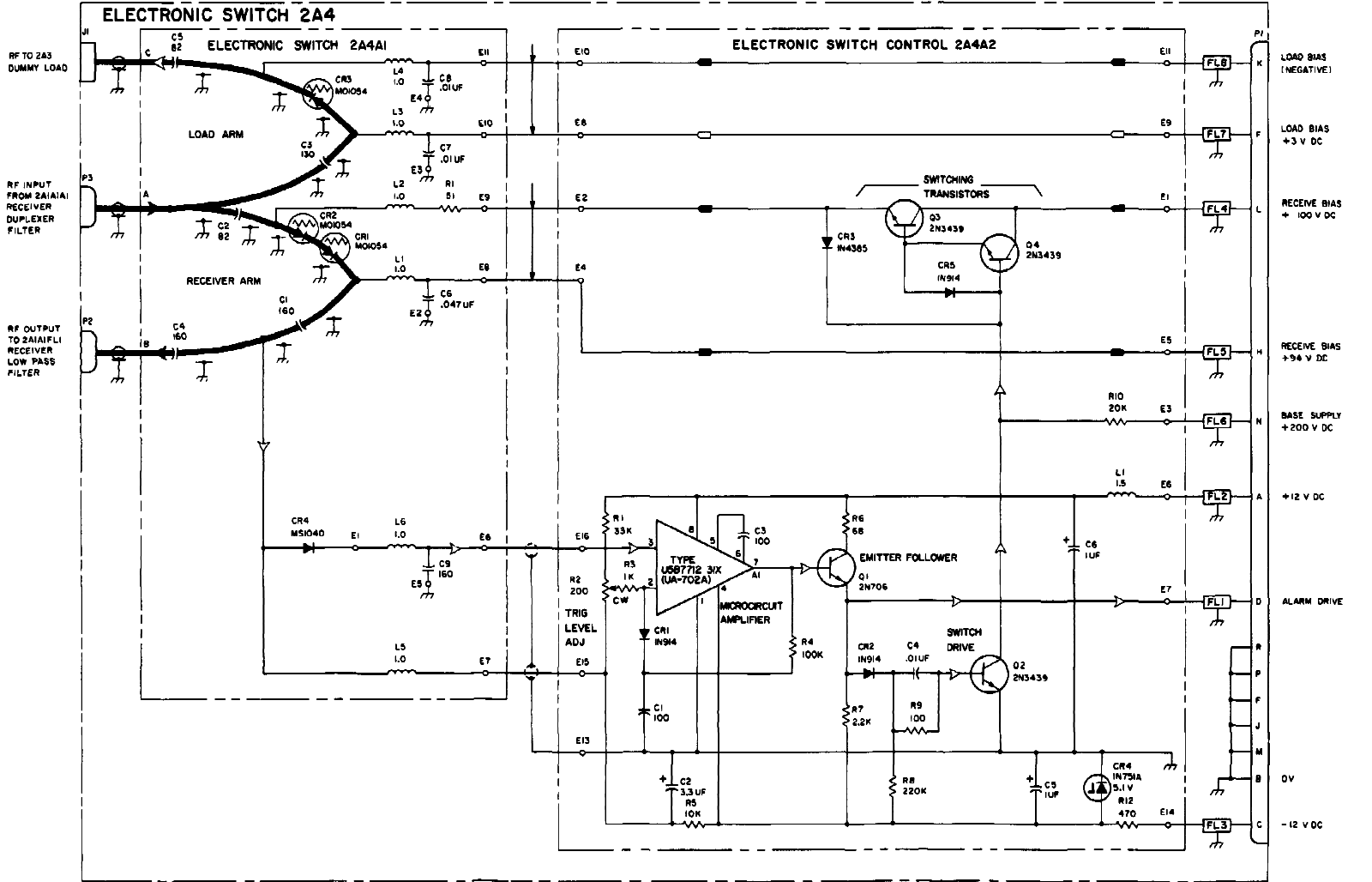
➔ MAJOR FUNCTIONAL FLOW



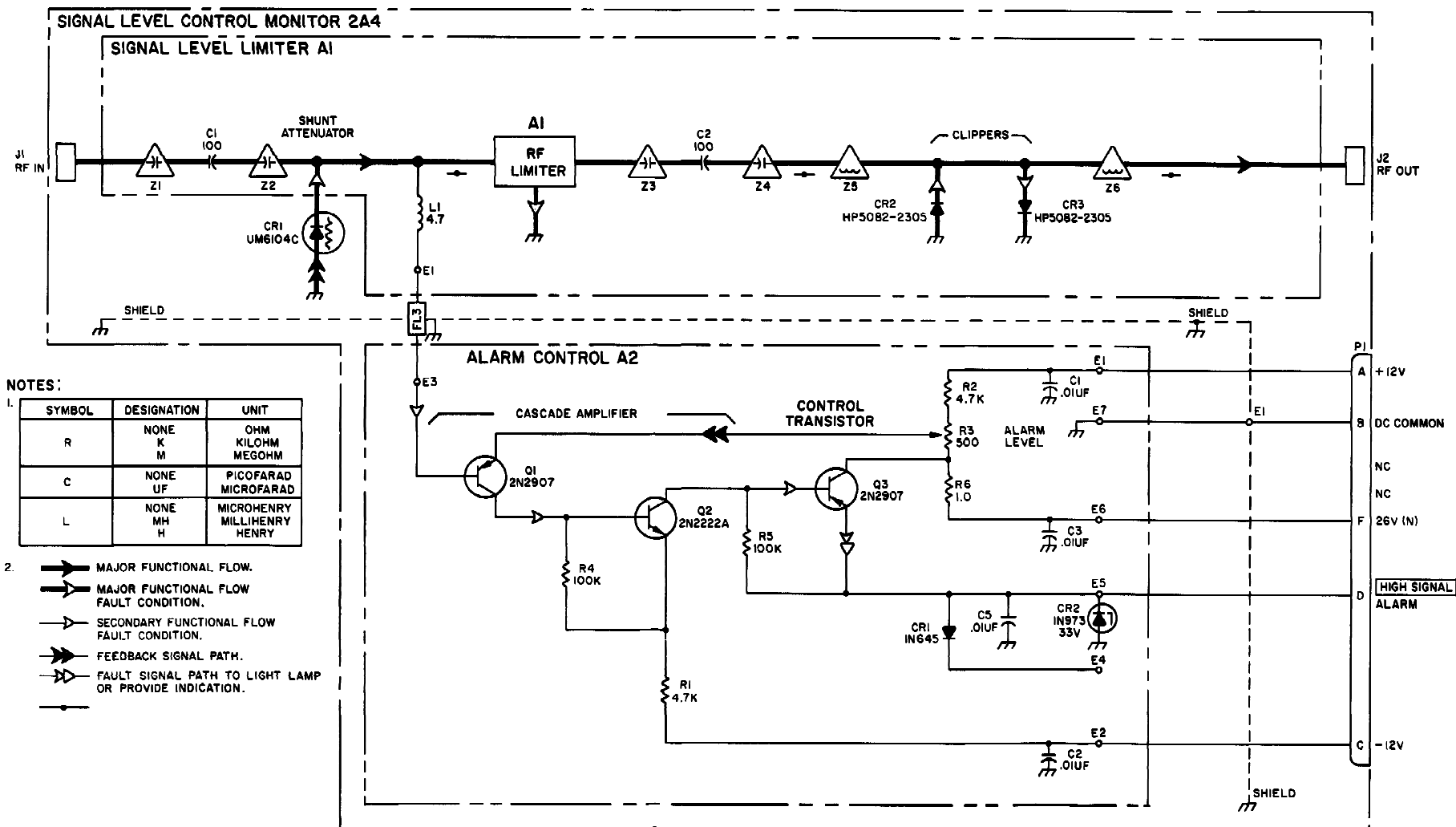
EL582660

| CHANNEL NO. | HOLE NUMBERS |   |   |   |   |   |   |   |   |    |
|-------------|--------------|---|---|---|---|---|---|---|---|----|
| DEPTH FEET  | 1            | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| 38          |              |   |   |   |   |   |   |   |   |    |
| 40          |              |   |   |   |   |   |   |   |   |    |
| 41          |              |   |   |   |   |   |   |   |   |    |
| 42          |              |   |   |   |   |   |   |   |   |    |
| 43          |              |   |   |   |   |   |   |   |   |    |
| 44          |              |   |   |   |   |   |   |   |   |    |
| 46          |              |   |   |   |   |   |   |   |   |    |
| 48          |              |   |   |   |   |   |   |   |   |    |
| 49          |              |   |   |   |   |   |   |   |   |    |
| 50          |              |   |   |   |   |   |   |   |   |    |
| 51          |              |   |   |   |   |   |   |   |   |    |
| 52          |              |   |   |   |   |   |   |   |   |    |
| 53          |              |   |   |   |   |   |   |   |   |    |
| 54          |              |   |   |   |   |   |   |   |   |    |
| 55          |              |   |   |   |   |   |   |   |   |    |
| 56          |              |   |   |   |   |   |   |   |   |    |
| 57          |              |   |   |   |   |   |   |   |   |    |
| 58          |              |   |   |   |   |   |   |   |   |    |
| 59          |              |   |   |   |   |   |   |   |   |    |
| 60          |              |   |   |   |   |   |   |   |   |    |
| 61          |              |   |   |   |   |   |   |   |   |    |
| 62          |              |   |   |   |   |   |   |   |   |    |
| 63          |              |   |   |   |   |   |   |   |   |    |
| 64          |              |   |   |   |   |   |   |   |   |    |
| 65          |              |   |   |   |   |   |   |   |   |    |
| 66          |              |   |   |   |   |   |   |   |   |    |
| 67          |              |   |   |   |   |   |   |   |   |    |
| 68          |              |   |   |   |   |   |   |   |   |    |
| 69          |              |   |   |   |   |   |   |   |   |    |
| 70          |              |   |   |   |   |   |   |   |   |    |
| 71          |              |   |   |   |   |   |   |   |   |    |
| 72          |              |   |   |   |   |   |   |   |   |    |
| 73          |              |   |   |   |   |   |   |   |   |    |
| 74          |              |   |   |   |   |   |   |   |   |    |
| 75          |              |   |   |   |   |   |   |   |   |    |
| 76          |              |   |   |   |   |   |   |   |   |    |
| 77          |              |   |   |   |   |   |   |   |   |    |
| 78          |              |   |   |   |   |   |   |   |   |    |
| 79          |              |   |   |   |   |   |   |   |   |    |
| 80          |              |   |   |   |   |   |   |   |   |    |
| 81          |              |   |   |   |   |   |   |   |   |    |
| 82          |              |   |   |   |   |   |   |   |   |    |
| 83          |              |   |   |   |   |   |   |   |   |    |
| 84          |              |   |   |   |   |   |   |   |   |    |
| 85          |              |   |   |   |   |   |   |   |   |    |
| 86          |              |   |   |   |   |   |   |   |   |    |

- NOTES
- | SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHM        |
| K      | K           | KILOHM     |
| M      | M           | MEGOHM     |
| C      | NONE        | PICOFARAD  |
| UF     | UF          | MICROFARAD |
| L      | NONE        | MICROHENRY |
| MH     | MH          | MILLIHENRY |
| H      | H           | HENRY      |
-  STRIPLINE.
  -  MAJOR FUNCTIONAL FLOW.
  -  MAJOR FUNCTIONAL FLOW FAULT CONDITION.
  -  SECONDARY FUNCTIONAL FLOW FAULT CONDITION.
  -  REFERENCE SIGNAL VOLTAGE.
  -  REFERENCE SIGNAL VOLTAGE FAULT CONDITION.

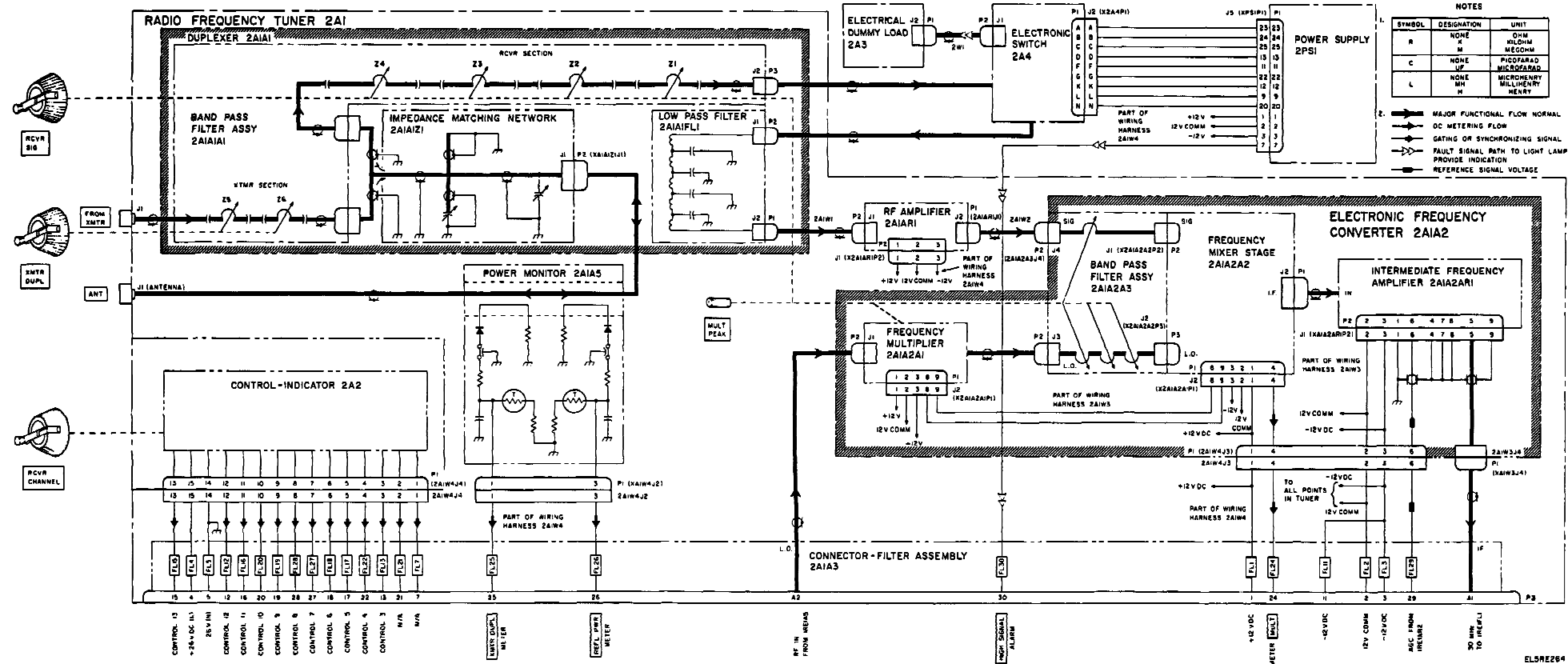


EL 5RE262



NOTES:

- | SYMBOL | DESIGNATION     | UNIT                              |
|--------|-----------------|-----------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM          |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |
2. **MAJOR FUNCTIONAL FLOW.** (indicated by a solid arrow)
- MAJOR FUNCTIONAL FLOW FAULT CONDITION.** (indicated by a solid arrow with a diagonal slash)
- SECONDARY FUNCTIONAL FLOW FAULT CONDITION.** (indicated by a dashed arrow)
- FEEDBACK SIGNAL PATH.** (indicated by a solid arrow with a diagonal slash)
- FAULT SIGNAL PATH TO LIGHT LAMP OR PROVIDE INDICATION.** (indicated by a solid arrow with a diagonal slash)

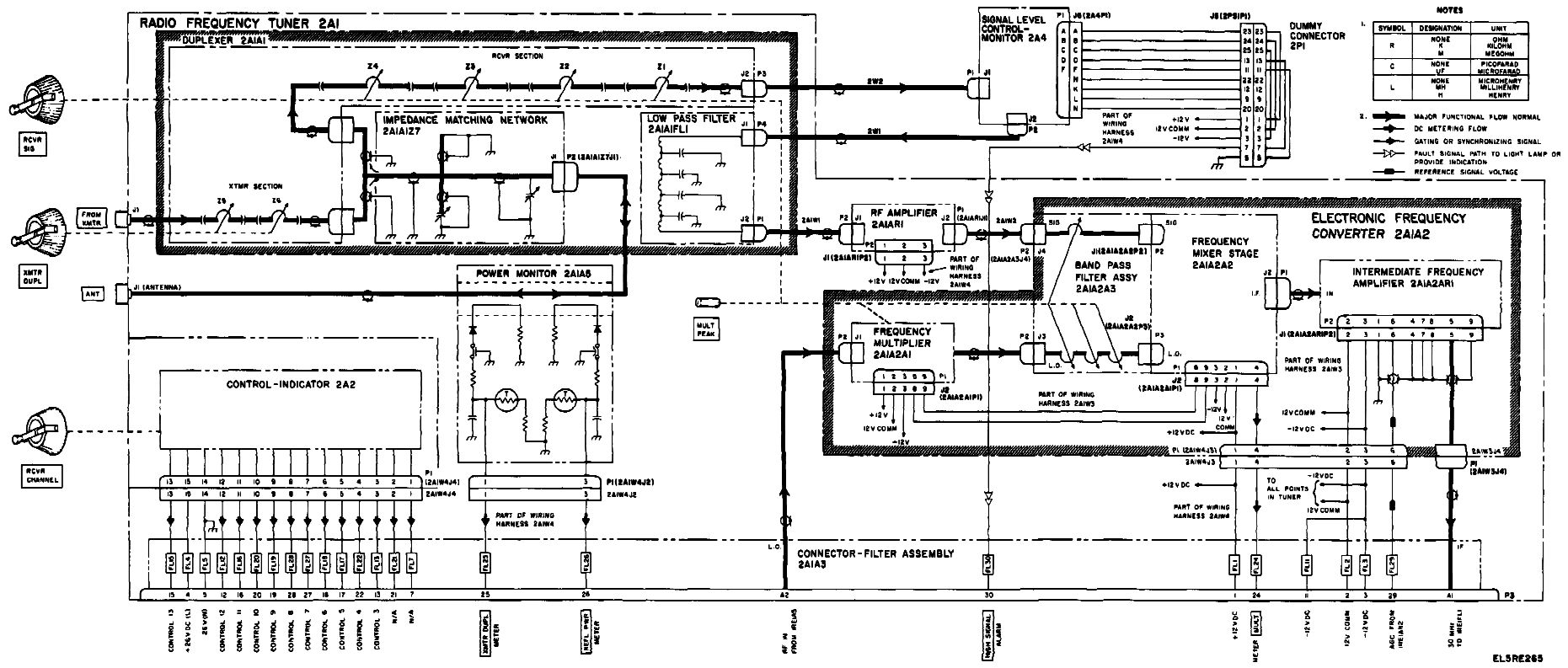


NOTES

| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHM        |
| M      | NONE        | MILIOHM    |
| C      | NONE        | PICOFARAD  |
| UF     | NONE        | MICROFARAD |
| MH     | NONE        | MICROHENRY |
| H      | NONE        | MILLIHENRY |

- MAJOR FUNCTIONAL FLOW NORMAL
- DC METERING FLOW
- GATING OR SYNCHRONIZING SIGNAL
- FAULTY SIGNAL PATH TO LIGHT LAMP OR PROVIDE INDICATION
- REFERENCE SIGNAL VOLTAGE

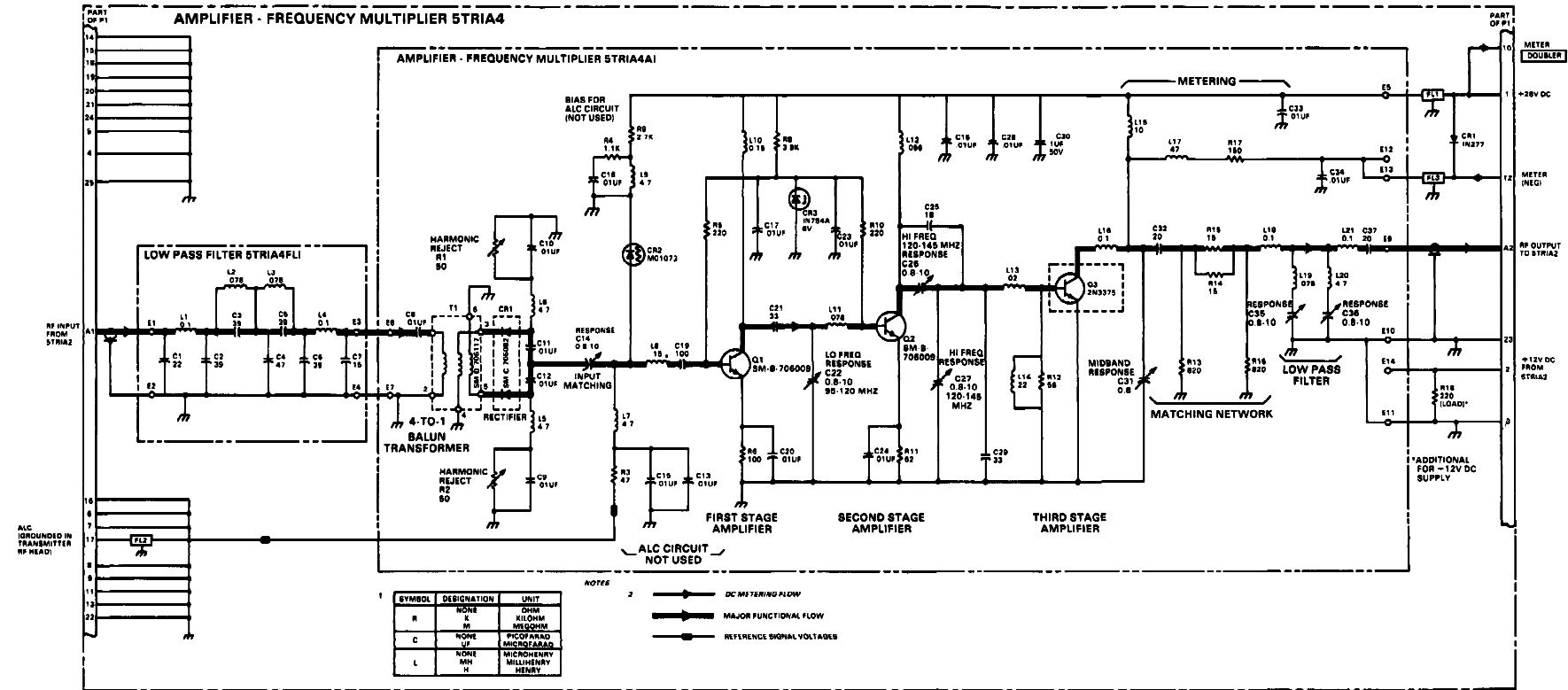




**NOTES**

| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHM        |
| M      | NONE        | MILIOHM    |
| C      | NONE        | PICOFARAD  |
| UF     | NONE        | MICROFARAD |
| L      | NONE        | MICROHENRY |
| H      | NONE        | MILLIHENRY |

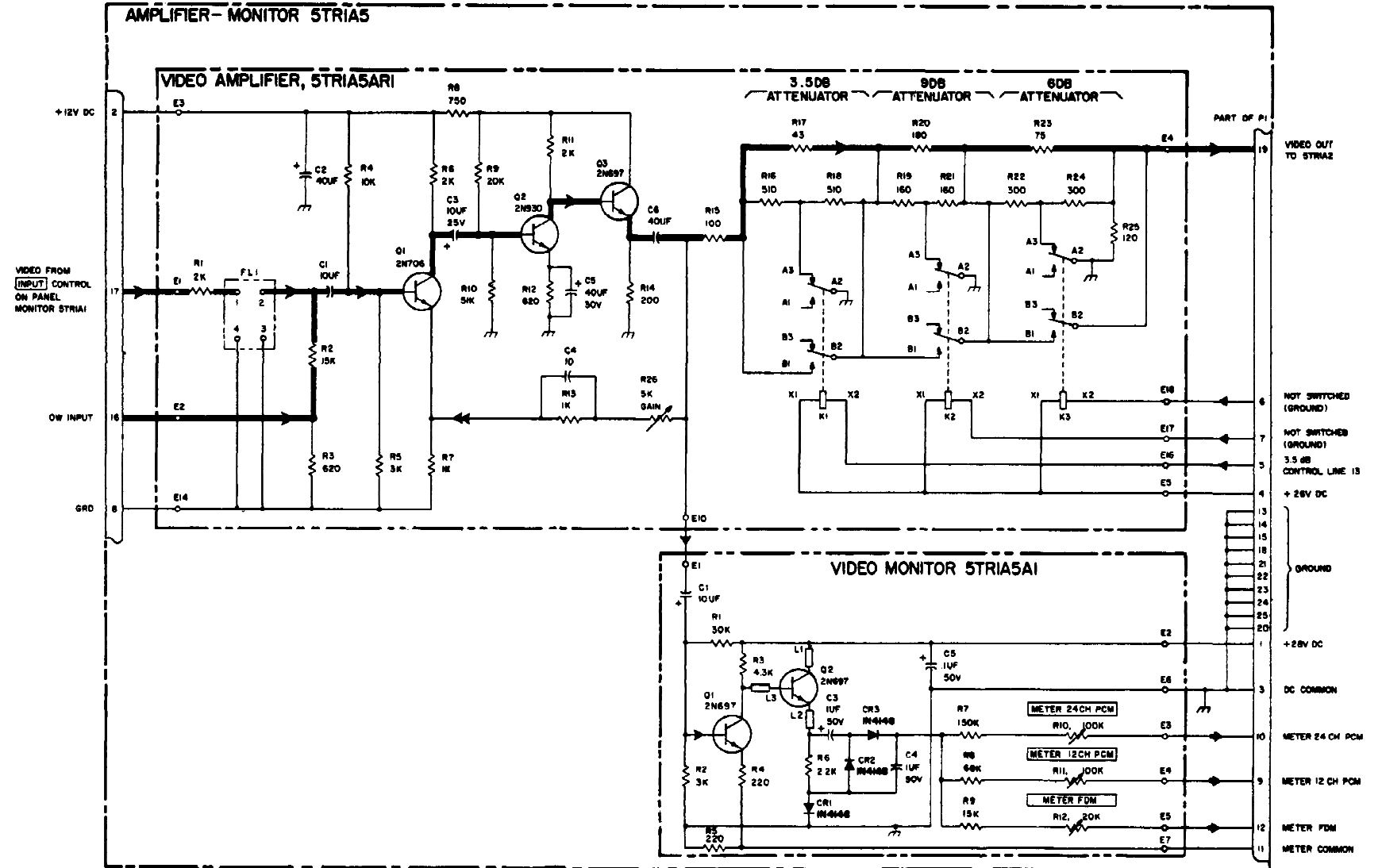
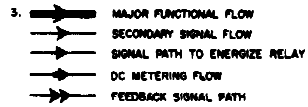
- MAJOR FUNCTIONAL FLOW NORMAL
- DC METERING FLOW
- GATING OR SYNCHRONIZING SIGNAL
- FAULT SIGNAL PATH TO LIGHT LAMP OR PROVIDE INDICATION
- REFERENCE SIGNAL VOLTAGE

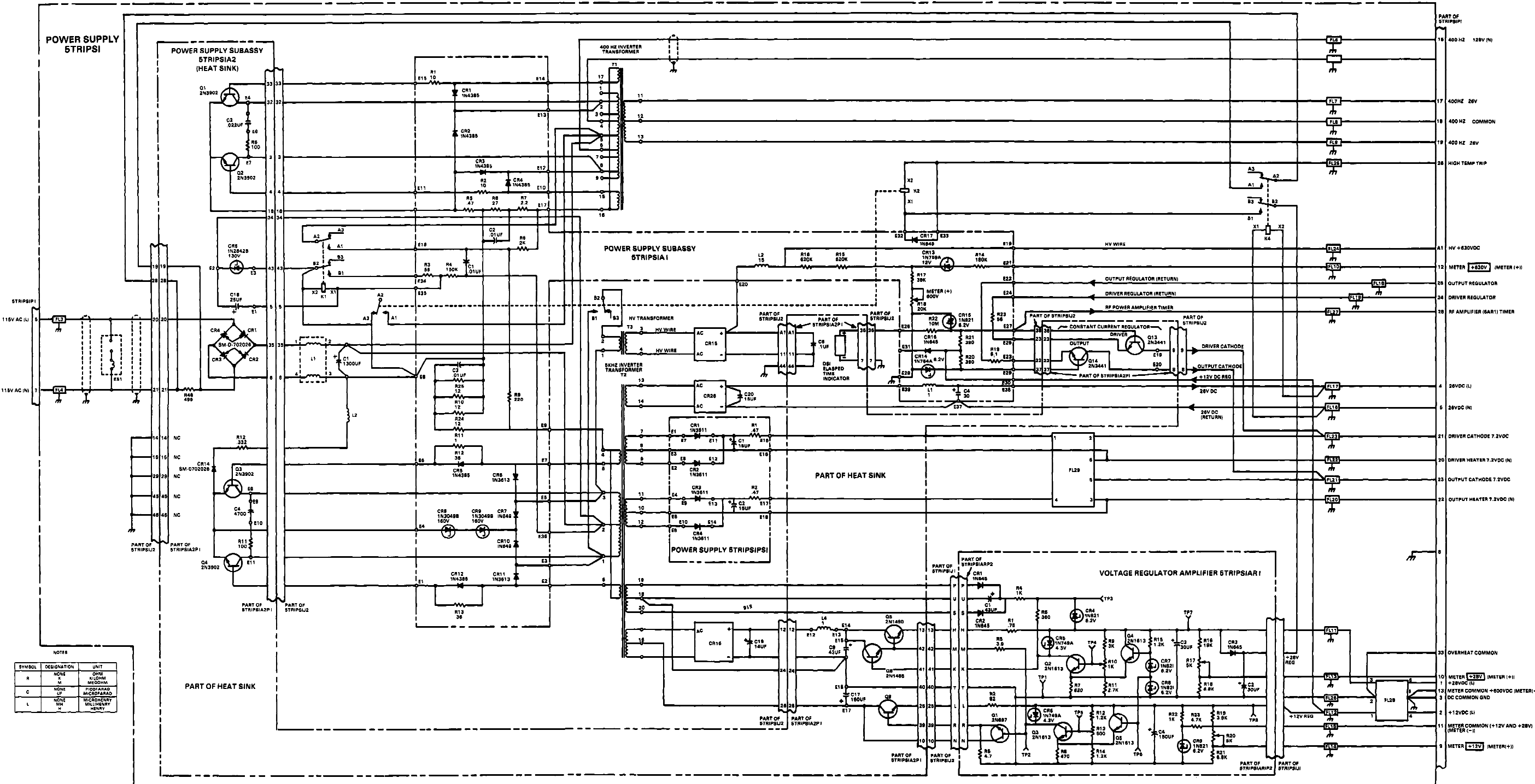


FO-4-38. Amplifier-Frequency Multiplier 5TR1A4, Schematic Diagram.

NOTES:

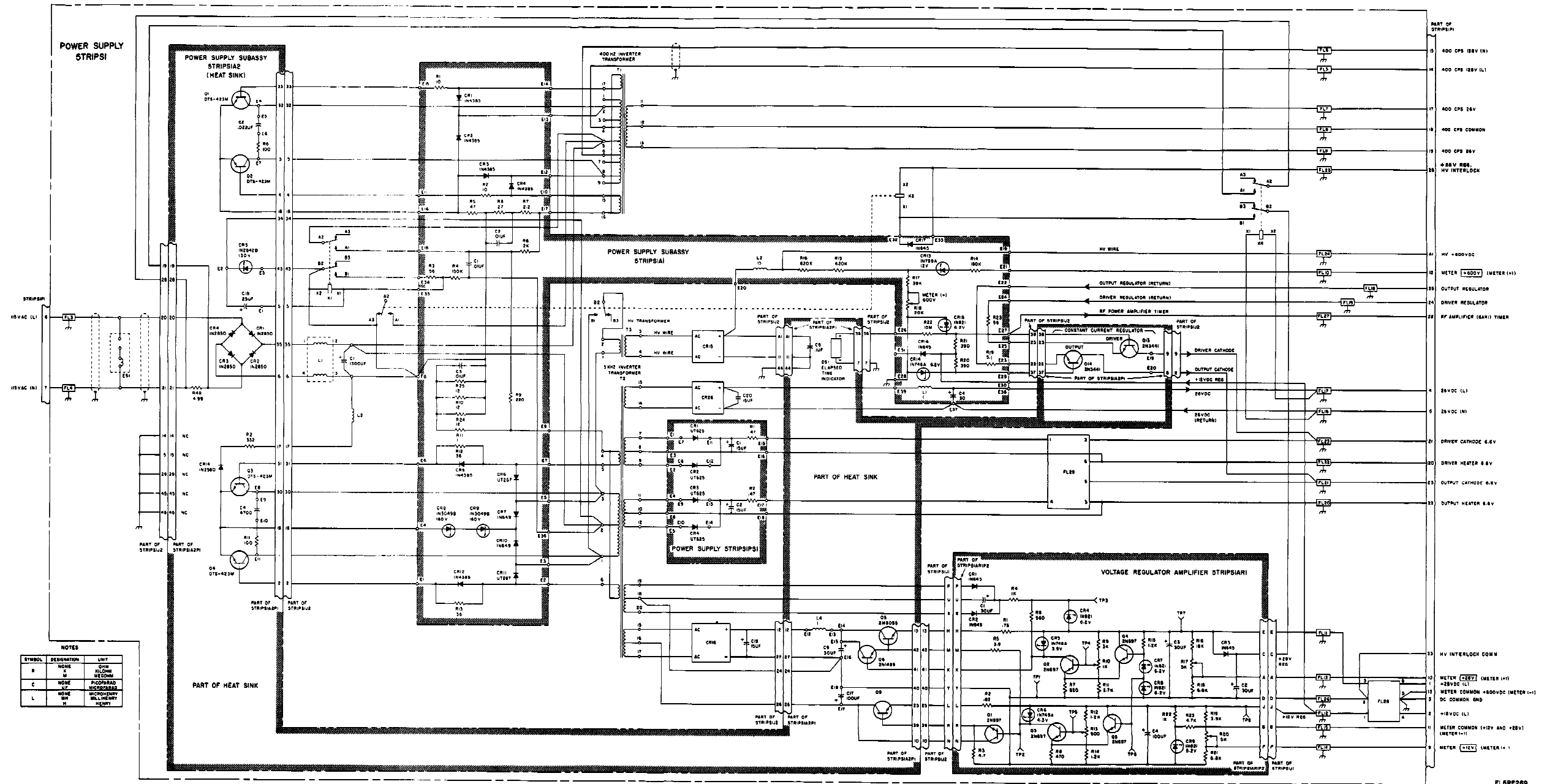
| SYMBOL | DESIGNATION | UNIT  |
|--------|-------------|---|
| R      | RESISTOR    | OHM, 100 OHM, 1000 OHM, 10000 OHM, 100000 OHM |
| C      | CAPACITOR   | PICOFARAD, MICROFARAD                         |
| L      | INDUCTOR    | MICROHENRY, MILLIHENRY, HENRY                 |





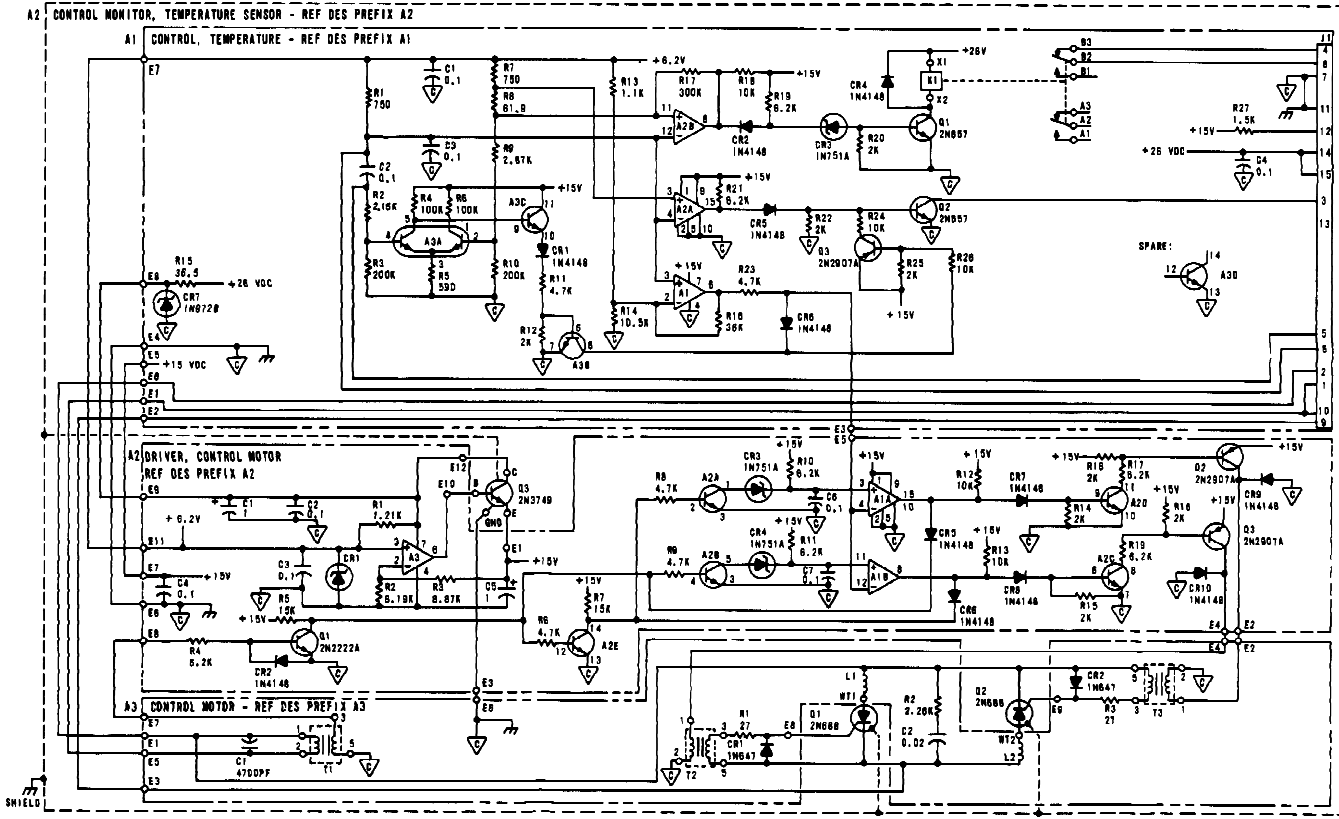
NOTES

| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | RESISTOR    | OHM        |
| K      | KILOHM      | KILOHM     |
| M      | MEGOHM      | MEGOHM     |
| C      | CAPACITOR   | PICOFARAD  |
| UF     | MICROFARAD  | MICROFARAD |
| L      | INDUCTOR    | MICROHENRY |
| H      | HENRY       | HENRY      |



NOTES

| SYMBOL | DESIGNATION | UNIT                  |
|--------|-------------|-----------------------|
| R      | RESISTOR    | OHM, KILOHM, MEGOHM   |
| C      | CAPACITOR   | PICOFARAD, MICROFARAD |
| L      | INDUCTOR    | MILLIHENRY, HENRY     |



NOTES:

1-

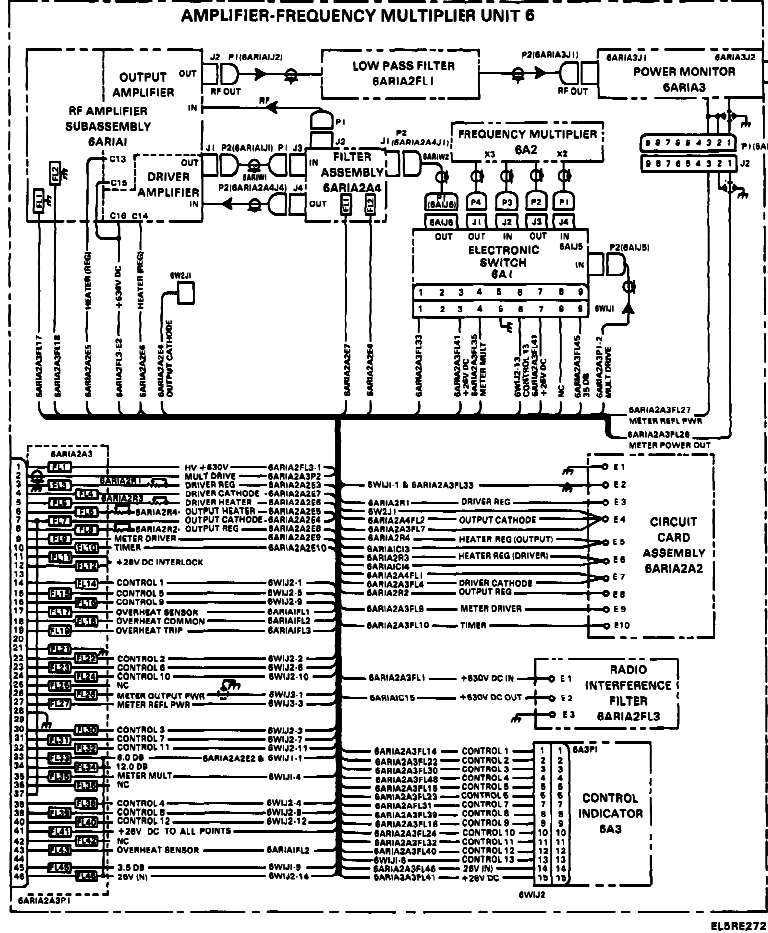
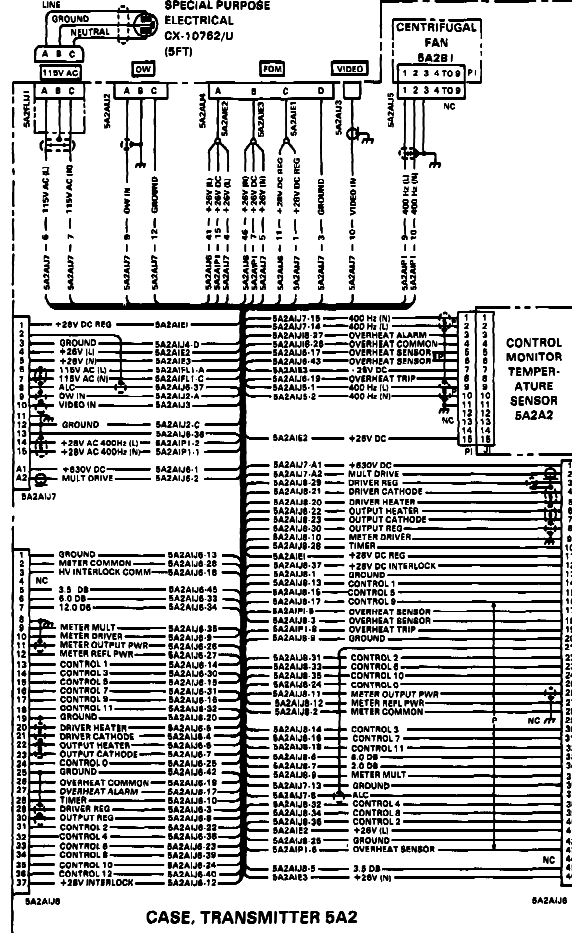
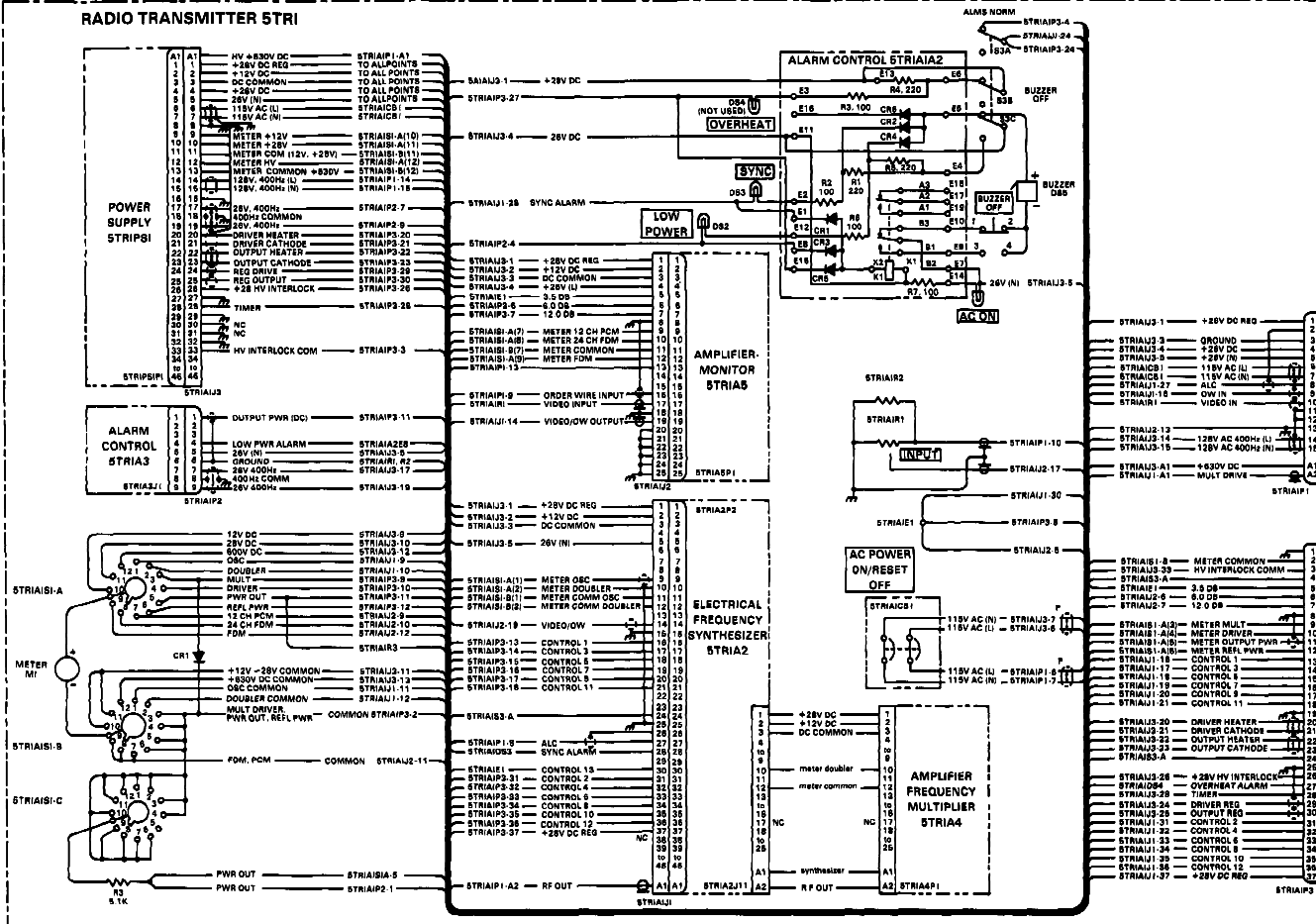
| SYMBOL | DESIGNATION     | UNIT                                  |
|--------|-----------------|---------------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM              |
| C      | pF<br>NONE<br>n | PICOFARAD<br>MICROFARAD<br>MICROHENRY |
| L      | NONE<br>m<br>H  | MILLI HENRY<br>HENRY                  |

2-

| HIGHEST REFERENCE DESIGNATION |        |       |     |
|-------------------------------|--------|-------|-----|
| AZ1A3                         | AZ2A3  | AZ3C2 | AZ3 |
| AZ1C4                         | AZ2C7  | AZ3C2 |     |
| AZ1C7                         | AZ2C10 | AZ3E0 |     |
| AZ1E8                         | AZ2E12 |       |     |
| AZ1J1                         |        | AZ2A3 |     |
| AZ1Q3                         | AZ2R19 | AZ3T3 |     |
| AZ1R27                        |        | AZ3W2 |     |
|                               |        | AZ3L2 |     |

OVERHEAT COMMON  
OVERHEAT TRIP  
26 VDC NEUTRAL  
GROUND  
+15 VDC MONITOR  
+26 VDC INTERLOCK  
+26 VDC UNREGULATED  
OVERHEAT ALARM  
NC  
OVERHEAT SENSOR  
400 Hz HI INPUT  
400 Hz LO INPUT  
400 Hz LO OUTPUT  
400 Hz HI OUTPUT





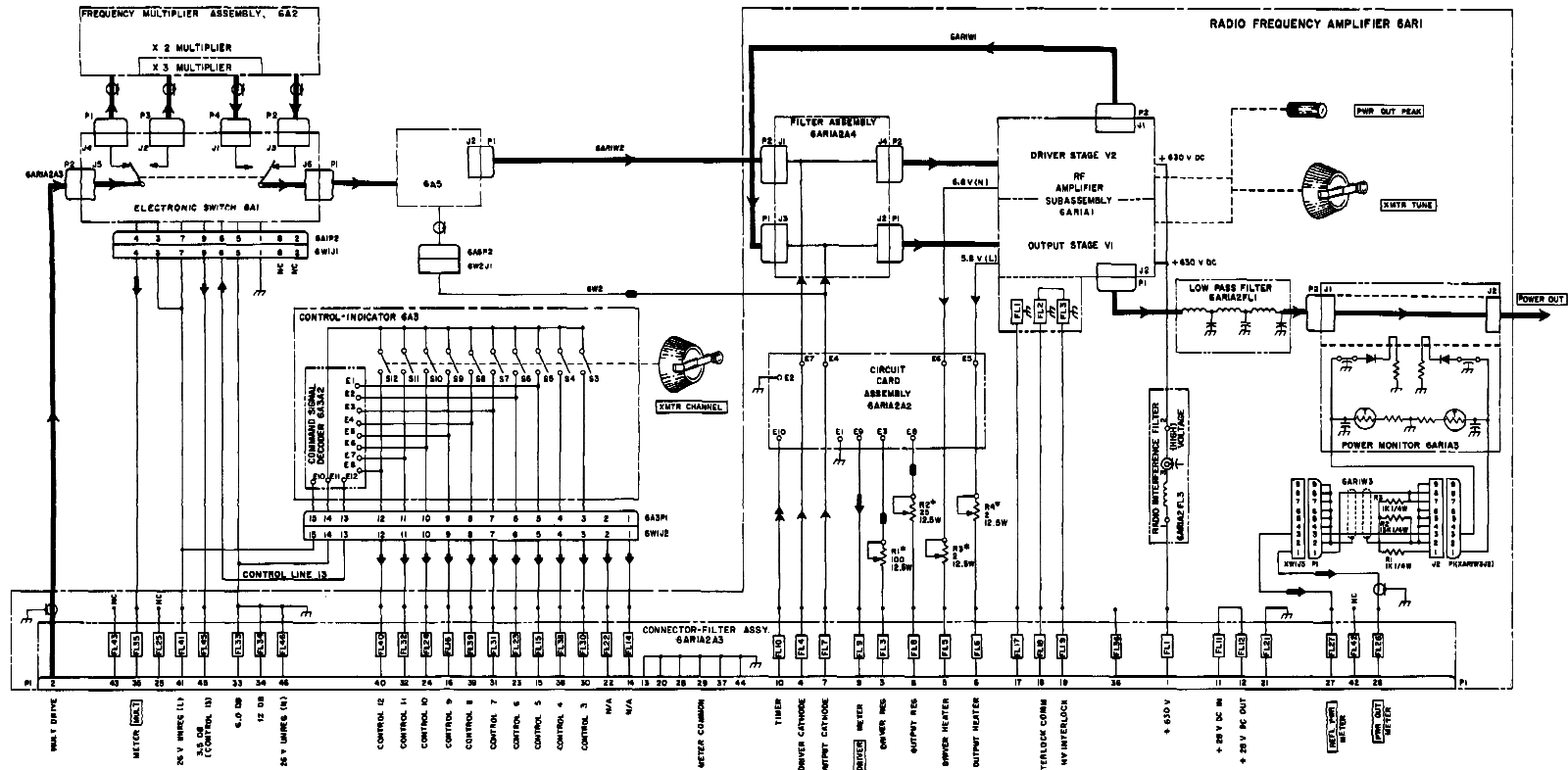




NOTES

| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHM        |
| M      | NONE        | KILOHM     |
| C      | NONE        | MEG OHM    |
| L      | NONE        | PICOFARAD  |
|        | NONE        | NEOPFARAD  |
|        | NONE        | MICROHENRY |
|        | NONE        | MILLIHENRY |
|        | NONE        | HENRY      |

- 1. MAJOR FUNCTIONAL FLOW
- 2. SECONDARY FUNCTIONAL FLOW
- 3. DC METERING FLOW
- 4. BATING OR SYNCHRONIZING SIGNAL
- 5. INDICATOR OR ALARM CIRCUIT
- 6. REFERENCE SIGNAL VOLTAGE
- 7. FOR FULL DESIGNATION PREFIX WITH GARXX

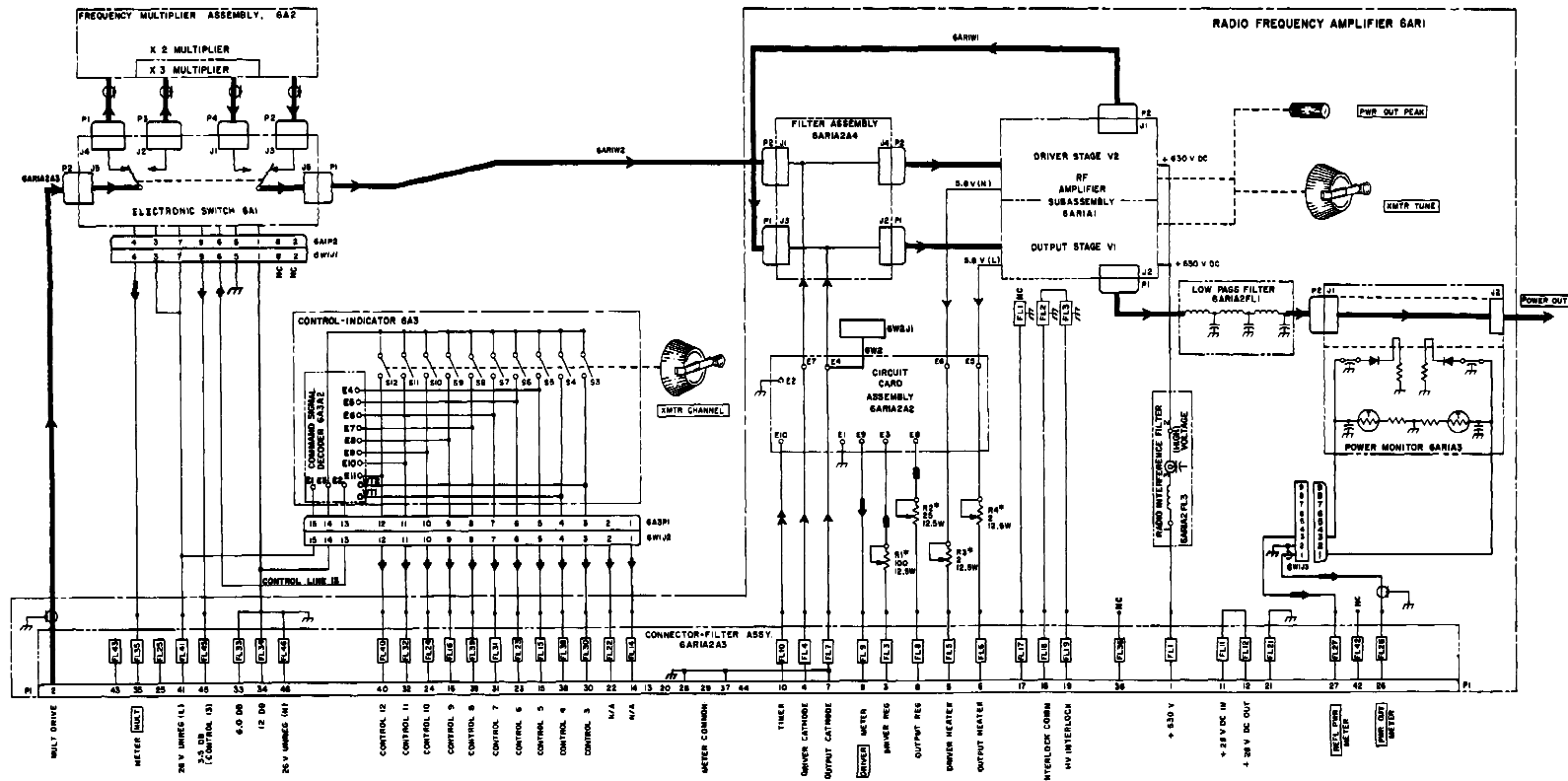


FO-4-46. Amplifier-Frequency Multiplier AM-4320/GRC-103(V). Schematic Diagram.

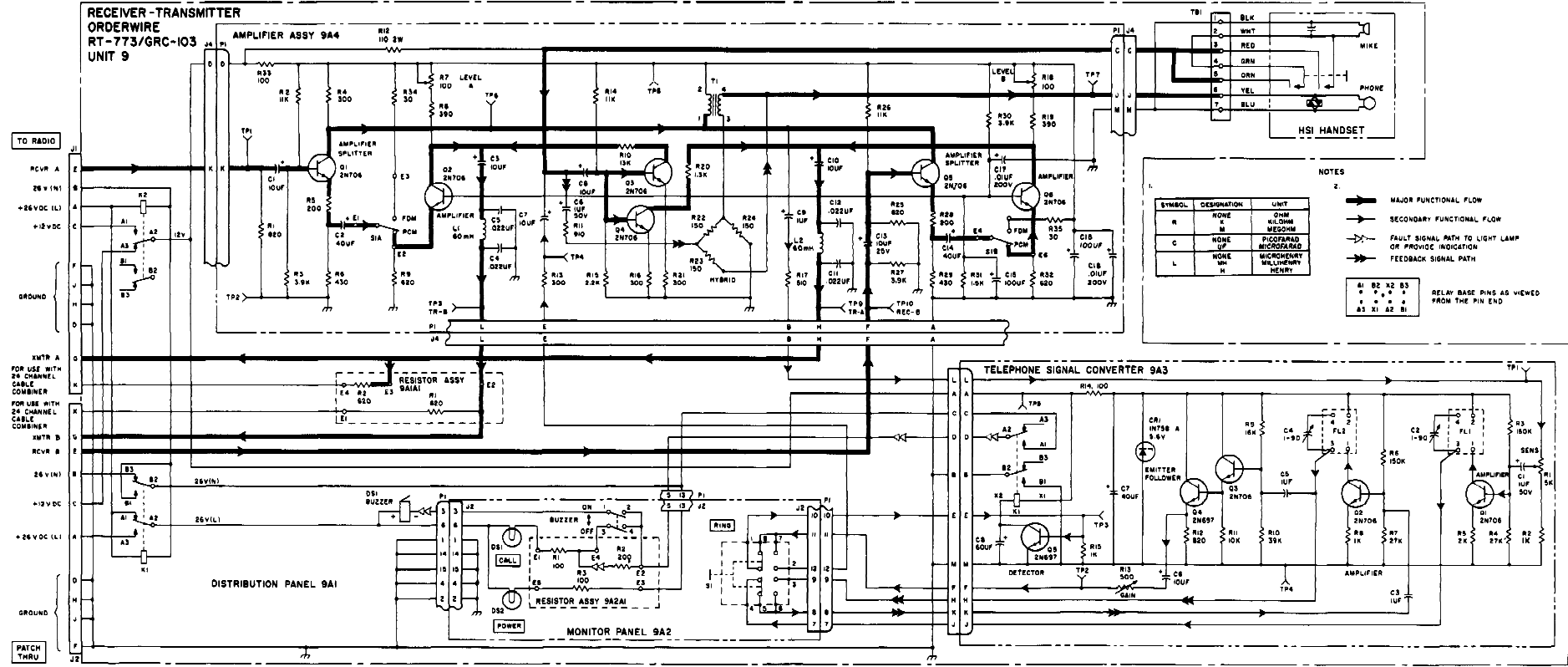
NOTES

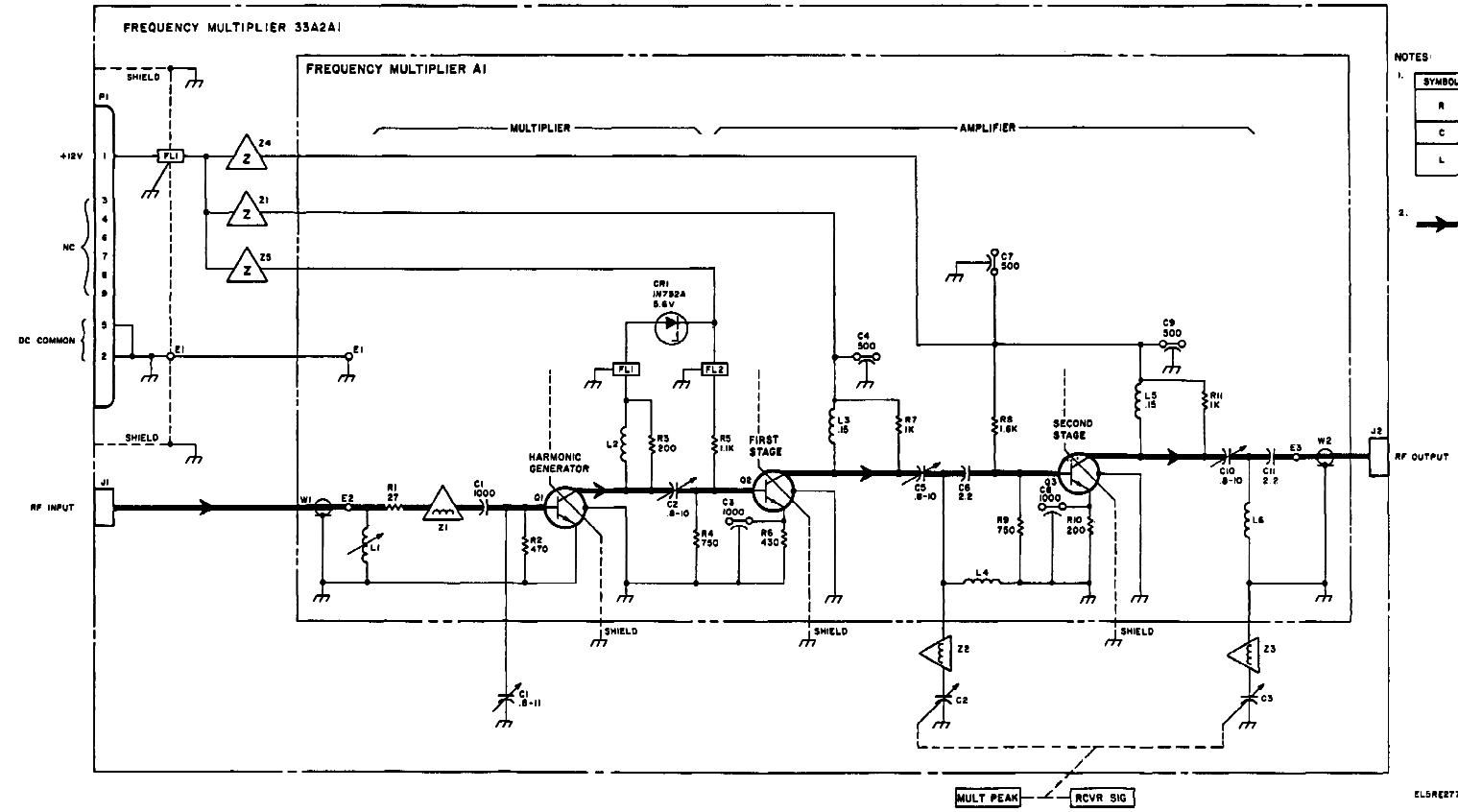
| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | OHM         | OHM        |
| K      | KILOHM      | KILOHM     |
| M      | MEGOHM      | MEGOHM     |
| C      | PICOFARAD   | PICOFARAD  |
| UF     | MICROFARAD  | MICROFARAD |
| L      | MILLIHENRY  | MILLIHENRY |
| H      | HENRY       | HENRY      |

- 1. MAJOR FUNCTIONAL FLOW
- 2. SECONDARY FUNCTIONAL FLOW
- 3. DC METERING FLOW
- 4. GATING OR SYNCHRONIZING SIGNAL
- 5. INDICATOR OR ALARM CIRCUIT
- 6. REFERENCE SIGNAL VOLTAGE
- 7. \* FOR FULL DESIGNATION PREFIX WITH SARIAS



F0-4-47. Amplifier-Frequency Multiplier AM-4320A/GRC-103(V) and AM-4320B/GRC-103(V), Schematic Diagram.



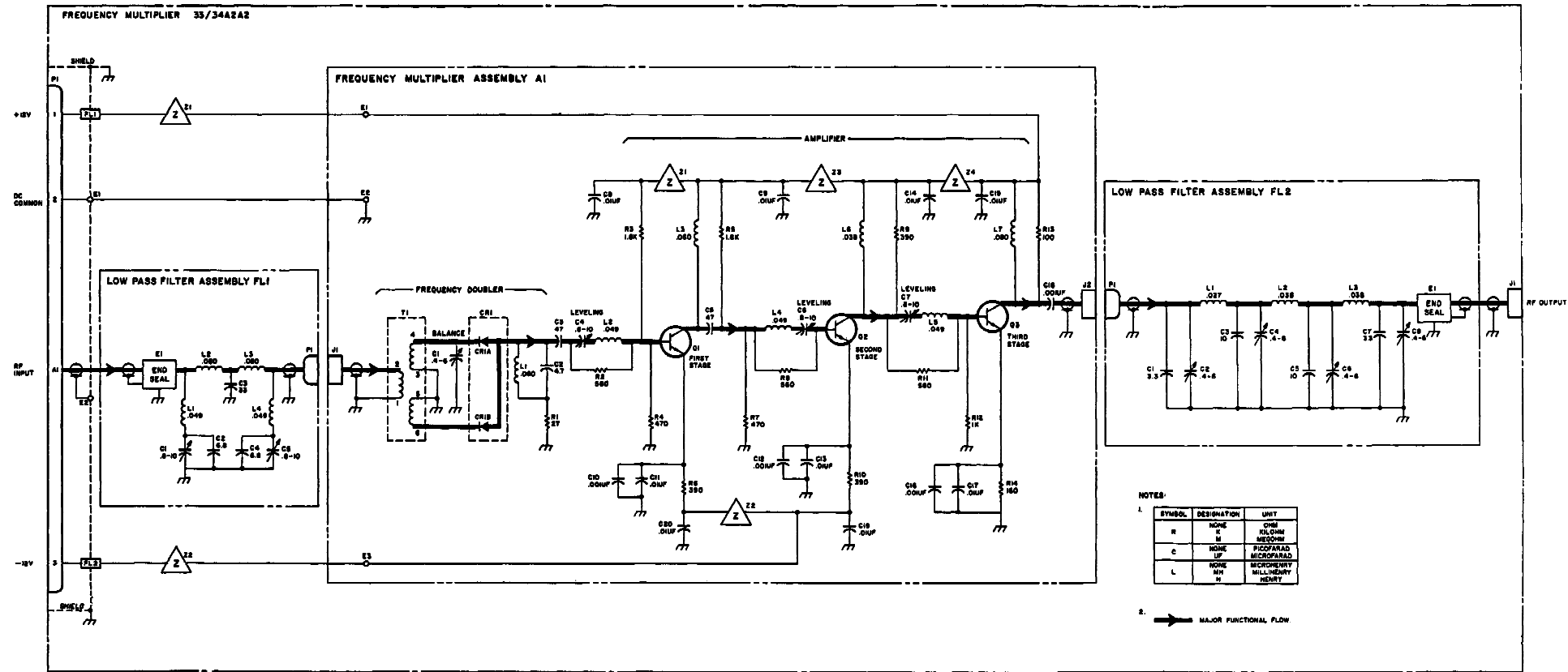


NOTES:

| SYMBOL | DESIGNATION     | UNIT                               |
|--------|-----------------|------------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM           |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD            |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLI HENRY<br>HENRY |

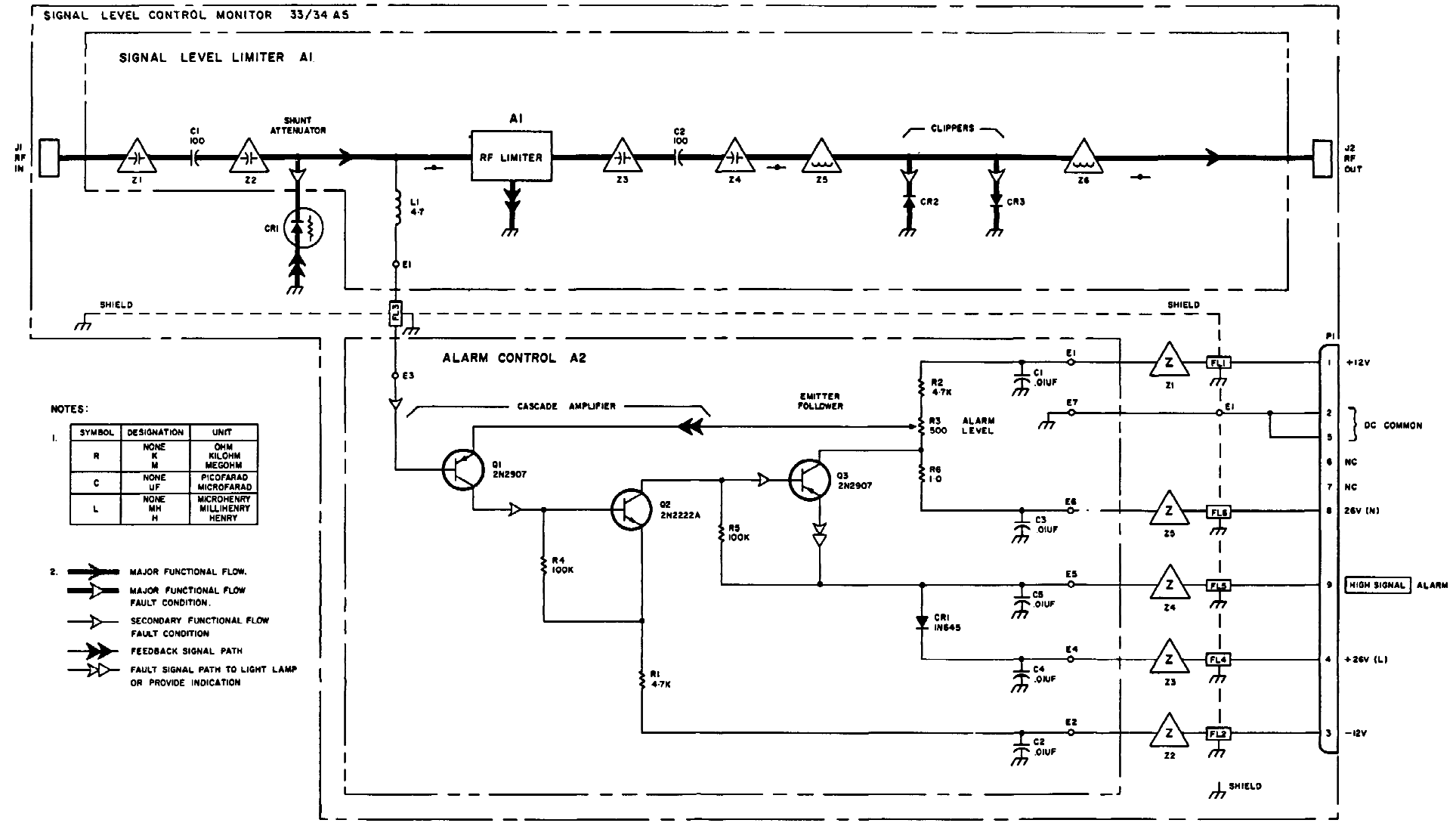
2. ———> MAJOR FUNCTIONAL FLOW

EL5RER77



EL68276

| CHANNEL NO. COORDS |      |   |   |   |   |   |   |   |   |   |    |    | CHANNEL NO. COORDS |      |   |   |   |   |   |   |   |   |   |    |    | CHANNEL NO. COORDS |      |   |   |   |   |   |   |   |   |   |    |    | CHANNEL NO. COORDS |      |   |   |   |   |   |   |   |   |   |    |    | CHANNEL NO. COORDS |      |   |   |   |   |   |   |   |   |   |    |    | CHANNEL NO. COORDS |      |   |   |   |   |   |   |   |   |   |    |    | CHANNEL NO. COORDS |      |   |   |   |   |   |   |   |   |   |    |    | CHANNEL NO. COORDS |      |   |   |   |   |   |   |   |   |   |    |    | CHANNEL NO. COORDS |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |      |   |   |   |   |   |   |   |   |   |    |    |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |
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-|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|--|--|--|--|--|
| SWR                | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR                | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR                | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR                | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR                | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR                | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR                | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR                | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR                | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | SWR | RCVR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |  |  |  |  |  |
| 382                |      |   |   |   |   |   |   |   |   |   |    |    | 383                |      |   |   |   |   |   |   |   |   |   |    |    | 384                |      |   |   |   |   |   |   |   |   |   |    |    | 385                |      |   |   |   |   |   |   |   |   |   |    |    | 386                |      |   |   |   |   |   |   |   |   |   |    |    | 387                |      |   |   |   |   |   |   |   |   |   |    |    | 388                |      |   |   |   |   |   |   |   |   |   |    |    | 389                |      |   |   |   |   |   |   |   |   |   |    |    | 390                |      |   |   |   |   |   |   |   |   |   |    |    | 391 |      |   |   |   |   |   |   |   |   |   |    |    | 392 |      |   |   |   |   |   |   |   |   |   |    |    | 393 |      |   |   |   |   |   |   |   |   |   |    |    | 394 |      |   |   |   |   |   |   |   |   |   |    |    | 395 |      |   |   |   |   |   |   |   |   |   |    |    | 396 |      |   |   |   |   |   |   |   |   |   |    |    | 397 |      |   |   |   |   |   |   |   |   |   |    |    | 398 |      |   |   |   |   |   |   |   |   |   |    |    | 399 |      |   |   |   |   |   |   |   |   |   |    |    | 400 |      |   |   |   |   |   |   |   |   |   |    |    | 401 |      |   |   |   |   |   |   |   |   |   |    |    | 402 |      |   |   |   |   |   |   |   |   |   |    |    | 403 |  |  |  |  |  |  |  |  |  |  |  |  | 404 |  |  |  |  |  |  |  |  |  |  |  |  | 405 |  |  |  |  |  |  |  |  |  |  |  |  | 406 |  |  |  |  |  |  |  |  |  |  |  |  | 407 |  |  |  |  |  |  |  |  |  |  |  |  | 408 |  |  |  |  |  |  |  |  |  |  |  |  | 409 |  |  |  |  |  |  |  |  |  |  |  |  | 410 |  |  |  |  |  |  |  |  |  |  |  |  | 411 |  |  |  |  |  |  |  |  |  |  |  |  | 412 |  |  |  |  |  |  |  |  |  |  |  |  | 413 |  |  |  |  |  |  |  |  |  |  |  |  | 414 |  |  |  |  |  |  |  |  |  |  |  |  | 415 |  |  |  |  |  |  |  |  |  |  |  |  | 416 |  |  |  |  |  |  |  |  |  |  |  |  | 417 |  |  |  |  |  |  |  |  |  |  |  |  | 418 |  |  |  |  |  |  |  |  |  |  |  |  | 419 |  |  |  |  |  |  |  |  |  |  |  |  | 420 |  |  |  |  |  |  |  |  |  |  |  |  | 421 |  |  |  |  |  |  |  |  |  |  |  |  | 422 |  |  |  |  |  |  |  |  |  |  |  |  | 423 |  |  |  |  |  |  |  |  |  |  |  |  | 424 |  |  |  |  |  |  |  |  |  |  |  |  | 425 |  |  |  |  |  |  |  |  |  |  |  |  | 426 |  |  |  |  |  |  |  |  |  |  |  |  | 427 |  |  |  |  |  |  |  |  |  |  |  |  | 428 |  |  |  |  |  |  |  |  |  |  |  |  | 429 |  |  |  |  |  |  |  |  |  |  |  |  | 430 |  |  |  |  |  |  |  |  |  |  |  |  | 431 |  |  |  |  |  |  |  |  |  |  |  |  | 432 |  |  |  |  |  |  |  |  |  |  |  |  | 433 |  |  |  |  |  |  |  |  |  |  |  |  | 434 |  |  |  |  |  |  |  |  |  |  |  |  | 435 |  |  |  |  |  |  |  |  |  |  |  |  | 436 |  |  |  |  |  |  |  |  |  |  |  |  | 437 |  |  |  |  |  |  |  |  |  |  |  |  | 438 |  |  |  |  |  |  |  |  |  |  |  |  | 439 |  |  |  |  |  |  |  |  |  |  |  |  | 440 |  |  |  |  |  |  |  |  |  |  |  |  | 441 |  |  |  |  |  |  |  |  |  |  |  |  | 442 |  |  |  |  |  |  |  |  |  |  |  |  | 443 |  |  |  |  |  |  |  |  |  |  |  |  | 444 |  |  |  |  |  |  |  |  |  |  |  |  | 445 |  |  |  |  |  |  |  |  |  |  |  |  | 446 |  |  |  |  |  |  |  |  |  |  |  |  | 447 |  |  |  |  |  |  |  |  |  |  |  |  | 448 |  |  |  |  |  |  |  |  |  |  |  |  | 449 |  |  |  |  |  |  |  |  |  |  |  |  | 450 |  |  |  |  |  |  |  |  |  |  |  |  | 451 |  |  |  |  |  |  |  |  |  |  |  |  | 452 |  |  |  |  |  |  |  |  |  |  |  |  | 453 |  |  |  |  |  |  |  |  |  |  |  |  | 454 |  |  |  |  |  |  |  |  |  |  |  |  | 455 |  |  |  |  |  |  |  |  |  |  |  |  | 456 |  |  |  |  |  |  |  |  |  |  |  |  | 457 |  |  |  |  |  |  |  |  |  |  |  |  | 458 |  |  |  |  |  |  |  |  |  |  |  |  | 459 |  |  |  |  |  |  |  |  |  |  |  |  | 460 |  |  |  |  |  |  |  |  |  |  |  |  | 461 |  |  |  |  |  |  |  |  |  |  |  |  | 462 |  |  |  |  |  |  |  |  |  |  |  |  | 463 |  |  |  |  |  |  |  |  |  |  |  |  | 464 |  |  |  |  |  |  |  |  |  |  |  |  | 465 |  |  |  |  |  |  |  |  |  |  |  |  | 466 |  |  |  |  |  |  |  |  |  |  |  |  | 467 |  |  |  |  |  |  |  |  |  |  |  |  | 468 |  |  |  |  |  |  |  |  |  |  |  |  | 469 |  |  |  |  |  |  |  |  |  |  |  |  | 470 |  |  |  |  |  |  |  |  |  |  |  |  | 471 |  |  |  |  |  |  |  |  |  |  |  |  | 472 |  |  |  |  |  |  |  |  |  |  |  |  | 473 |  |  |  |  |  |  |  |  |  |  |  |  | 474 |  |  |  |  |  |  |  |  |  |  |  |  | 475 |  |  |  |  |  |  |  |  |  |  |  |  | 476 |  |  |  |  |  |  |  |  |  |  |  |  | 477 |  |  |  |  |  |  |  |  |  |  |  |  | 478 |  |  |  |  |  |  |  |  |  |  |  |  | 479 |  |  |  |  |  |  |  |  |  |  |  |  | 480 |  |  |  |  |  |  |  |  |  |  |  |  | 481 |  |  |  |  |  |  |  |  |  |  |  |  | 482 |  |  |  |  |  |  |  |  |  |  |  |  | 483 |  |  |  |  |  |  |  |  |  |  |  |  | 484 |  |  |  |  |  |  |  |  |  |  |  |  | 485 |  |  |  |  |  |  |  |  |  |  |  |  | 486 |  |  |  |  |  |  |  |  |  |  |  |  | 487 |  |  |  |  |  |  |  |  |  |  |  |  | 488 |  |  |  |  |  |  |  |  |  |  |  |  | 489 |  |  |  |  |  |  |  |  |  |  |  |  | 490 |  |  |  |  |  |  |  |  |  |  |  |  | 491 |  |  |  |  |  |  |  |  |  |  |  |  | 492 |  |  |  |  |  |  |  |  |  |  |  |  | 493 |  |  |  |  |  |  |  |  |  |  |  |  | 494 |  |  |  |  |  |  |  |  |  |  |  |  | 495 |  |  |  |  |  |  |  |  |  |  |  |  | 496 |  |  |  |  |  |  |  |  |  |  |  |  | 497 |  |  |  |  |  |  |  |  |  |  |  |  | 498 |  |  |  |  |  |  |  |  |  |  |  |  | 499 |  |  |  |  |  |  |  |  |  |  |  |  | 500 |  |  |  |  |  |  |  |  |  |  |  |  |

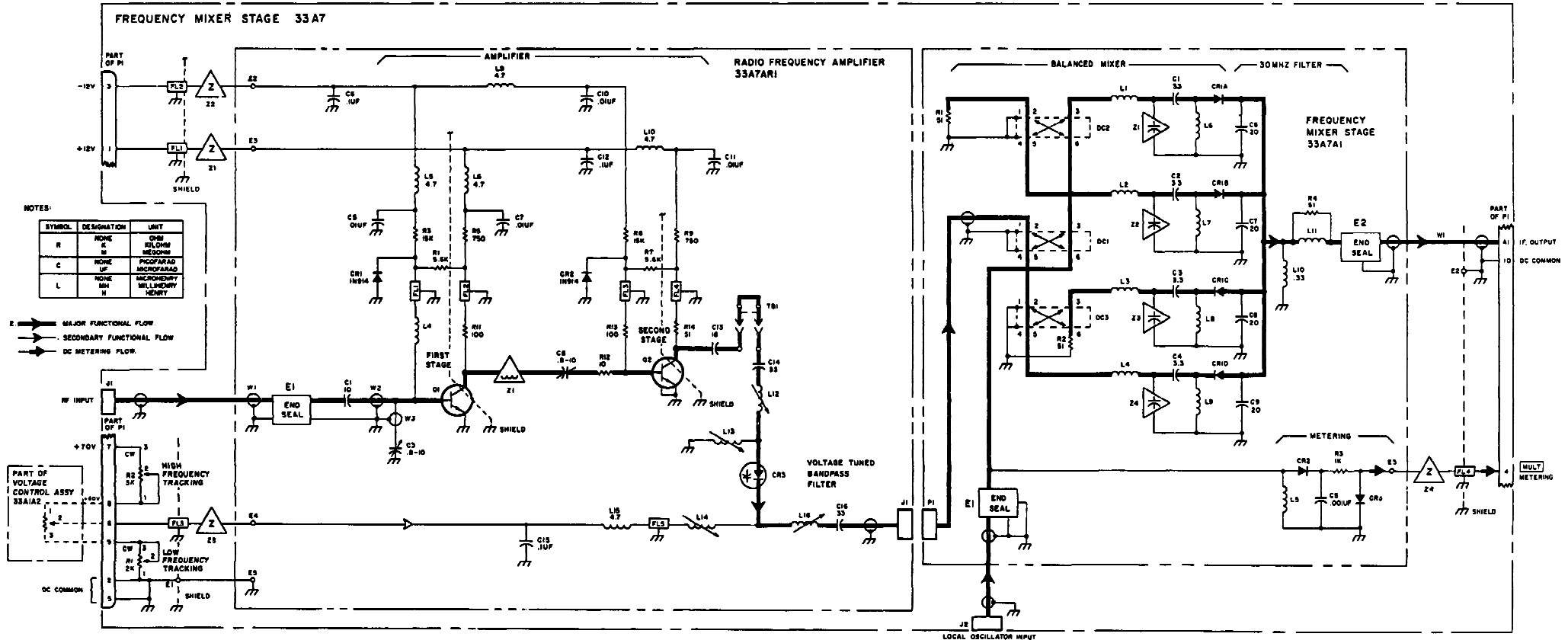


NOTES:

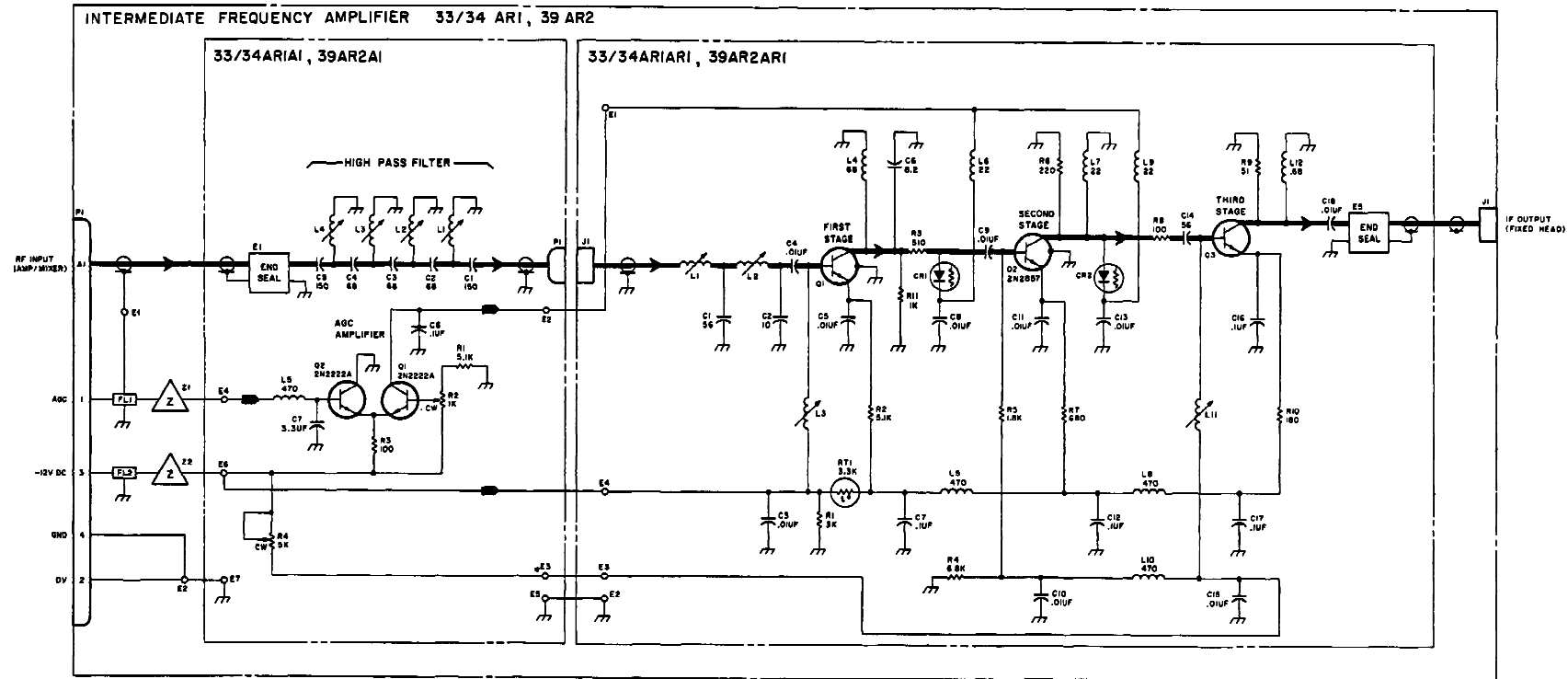
| 1. SYMBOL | DESIGNATION     | UNIT                              |
|-----------|-----------------|-----------------------------------|
| R         | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM          |
| C         | NONE<br>UF      | PICOFARAD<br>MICROFARAD           |
| L         | NONE<br>MH<br>H | MICROHENRY<br>MILLIHENRY<br>HENRY |

- 2.
- MAJOR FUNCTIONAL FLOW.
  - MAJOR FUNCTIONAL FLOW FAULT CONDITION.
  - SECONDARY FUNCTIONAL FLOW FAULT CONDITION.
  - FEEDBACK SIGNAL PATH.
  - FAULT SIGNAL PATH TO LIGHT LAMP OR PROVIDE INDICATION.





F0-4-53. Frequency Mixer Stage 33A7, Schematic Diagram.

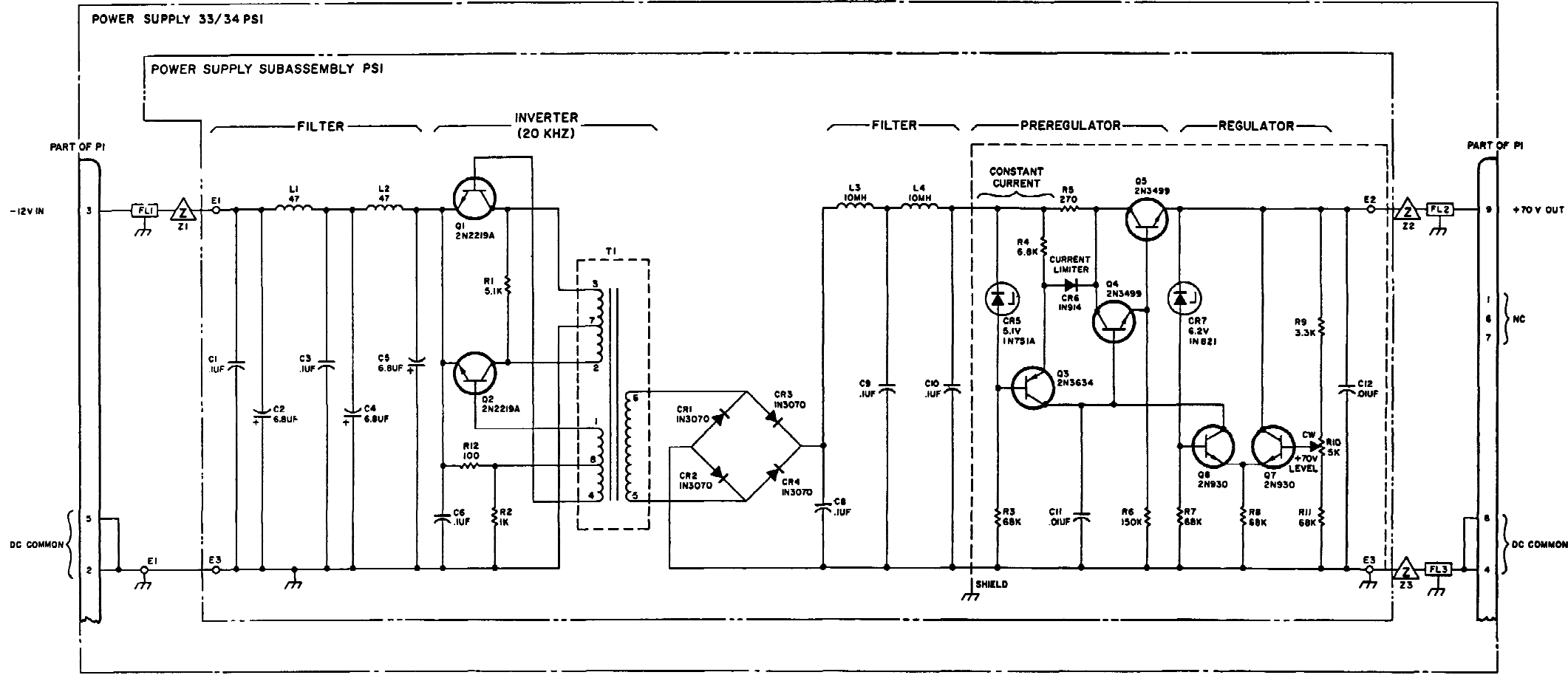


**NOTES:**

| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHM        |
| E      | NONE        | KILOHM     |
| M      | NONE        | MEG OHM    |
| C      | NONE        | PICOFARAD  |
| UF     | NONE        | MICROFARAD |
| MH     | NONE        | MICROHENRY |
| H      | NONE        | MILLIHENRY |
| H      | NONE        | HENRY      |

- 1. ——— MAJOR FUNCTIONAL FLOW.
- 2. — REFERENCE SIGNAL VOLTAGE.

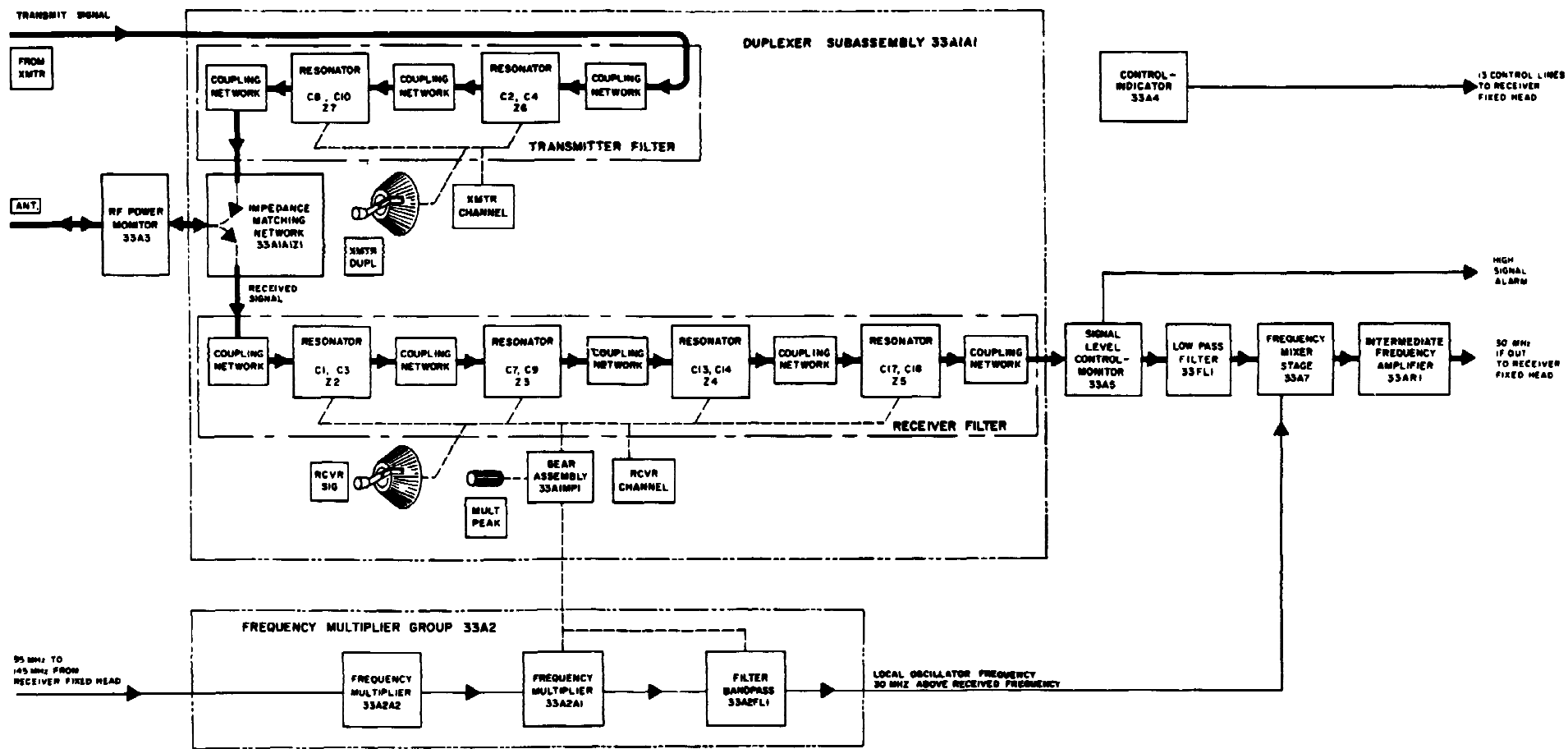
ELSRE288



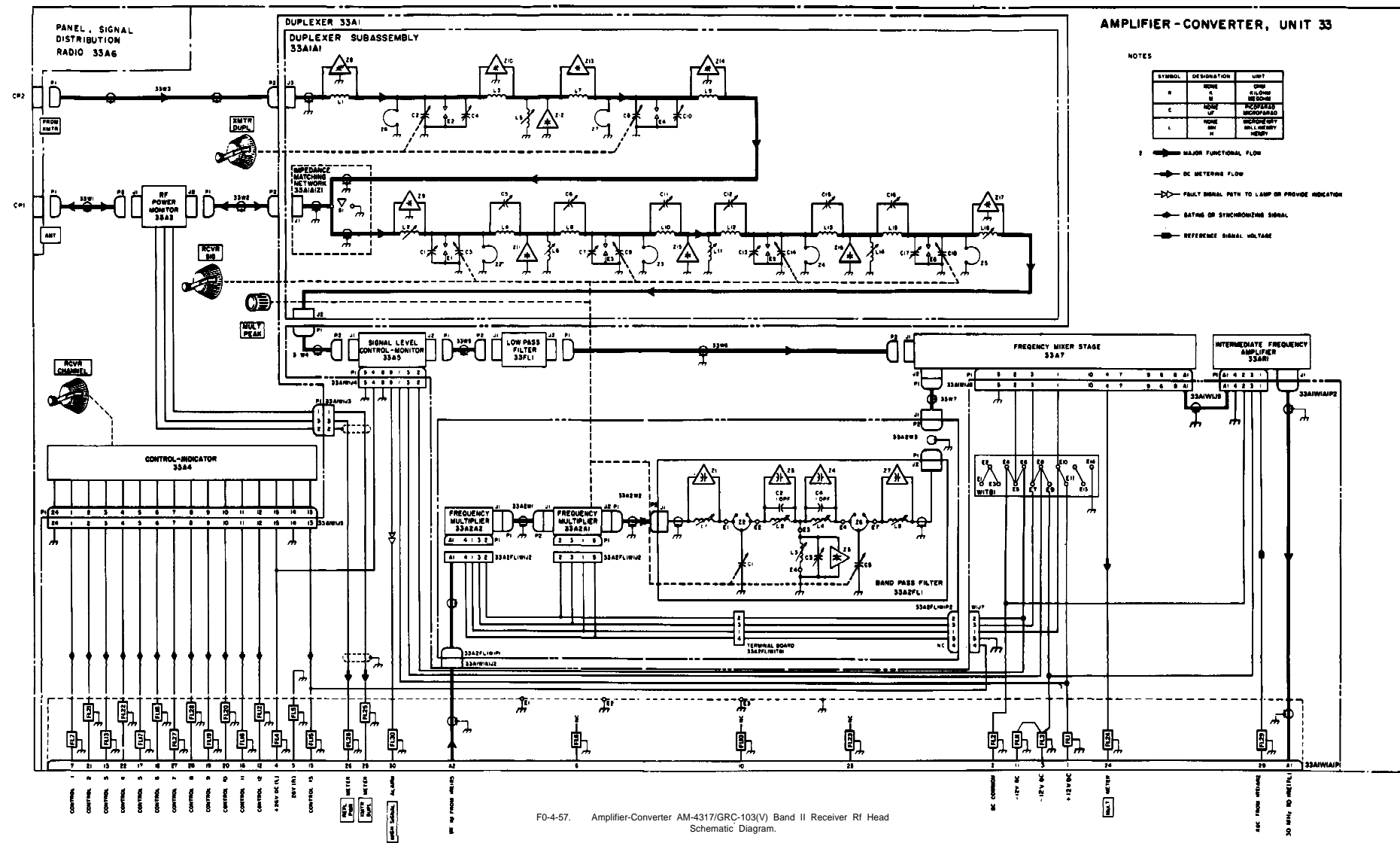
NOTE:

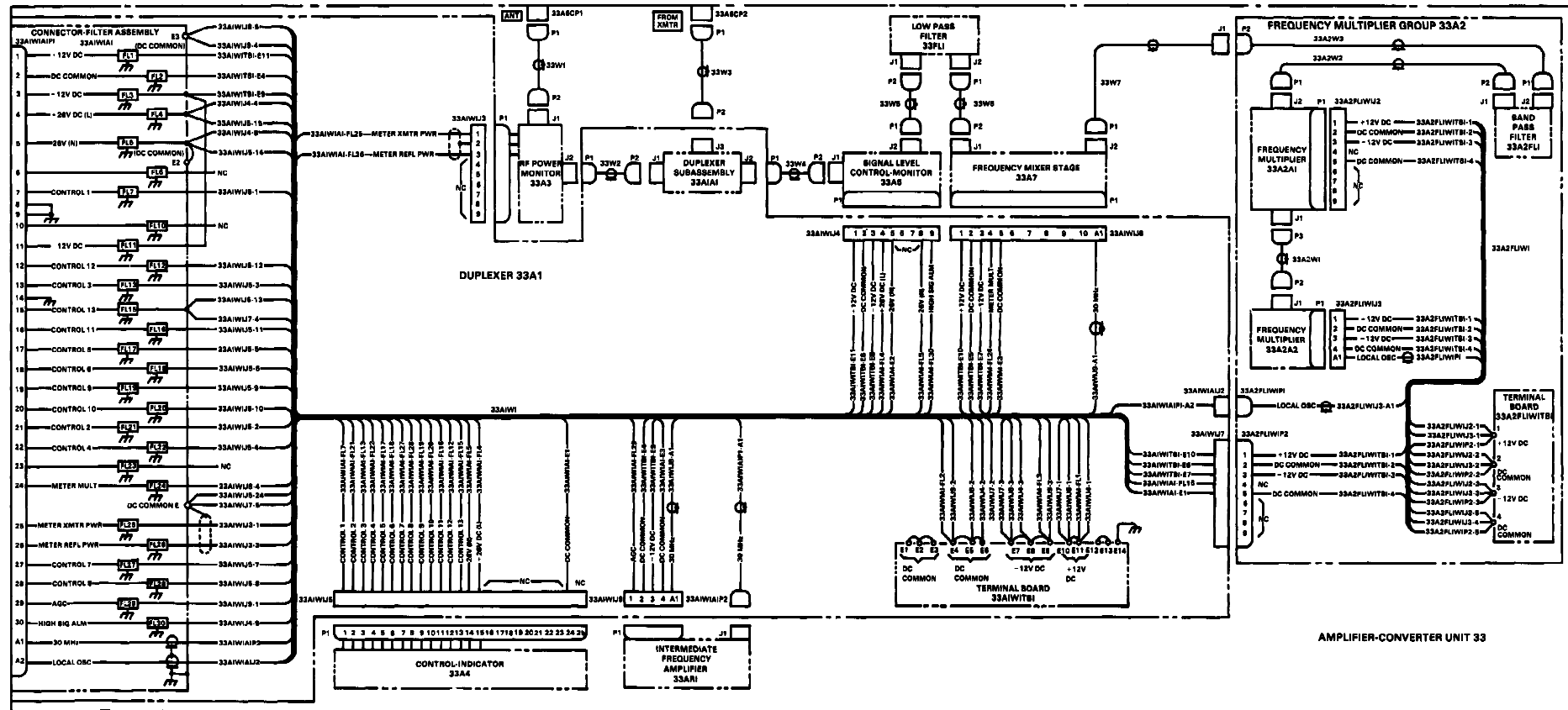
| SYMBOL | DESIGNATION     | UNIT                               |
|--------|-----------------|------------------------------------|
| R      | NONE<br>K<br>M  | OHM<br>KILOHM<br>MEG OHM           |
| C      | NONE<br>UF      | PICOFARAD<br>MICROFARAD            |
| L      | NONE<br>MH<br>H | MICROHENRY<br>MILLI HENRY<br>HENRY |

EL5RE265

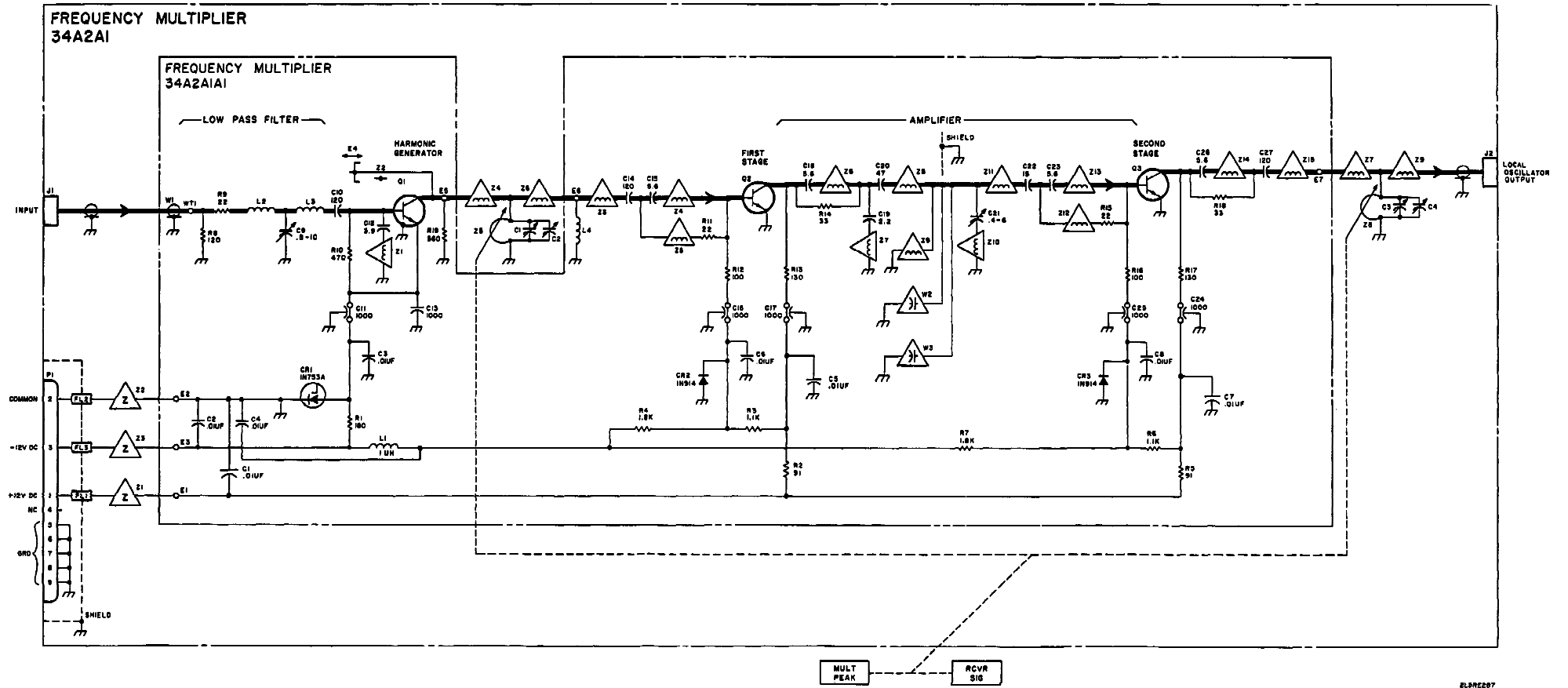


EL5RE284





F0-4-58. Amplifier-Converter AM-4317/GRC-103(V) Band II Receiver Rf Head, Interconnecting Diagram.



F0-4-59. Frequency-Multiplier 34A2A1, Schematic Diagram.

EL39287

CHANNEL NO CODING table with columns XMTA, RCVR, and 12 coding positions (1-12).

CHANNEL NO CODING table with columns XMTA, RCVR, and 12 coding positions (1-12).

CHANNEL NO CODING table with columns XMTA, RCVR, and 12 coding positions (1-12).

CHANNEL NO CODING table with columns XMTA, RCVR, and 12 coding positions (1-12).

CHANNEL NO CODING table with columns XMTA, RCVR, and 12 coding positions (1-12).

CHANNEL NO CODING table with columns XMTA, RCVR, and 12 coding positions (1-12).

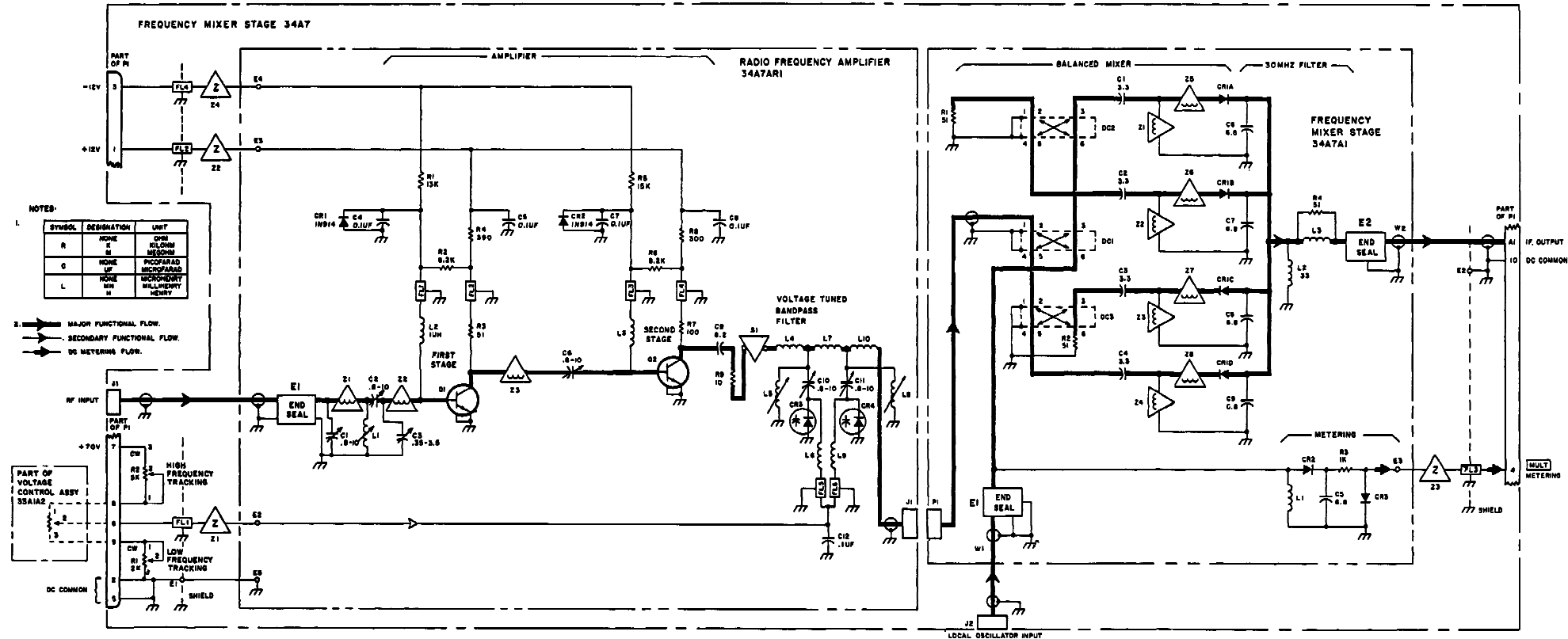
CHANNEL NO CODING table with columns XMTA, RCVR, and 12 coding positions (1-12).

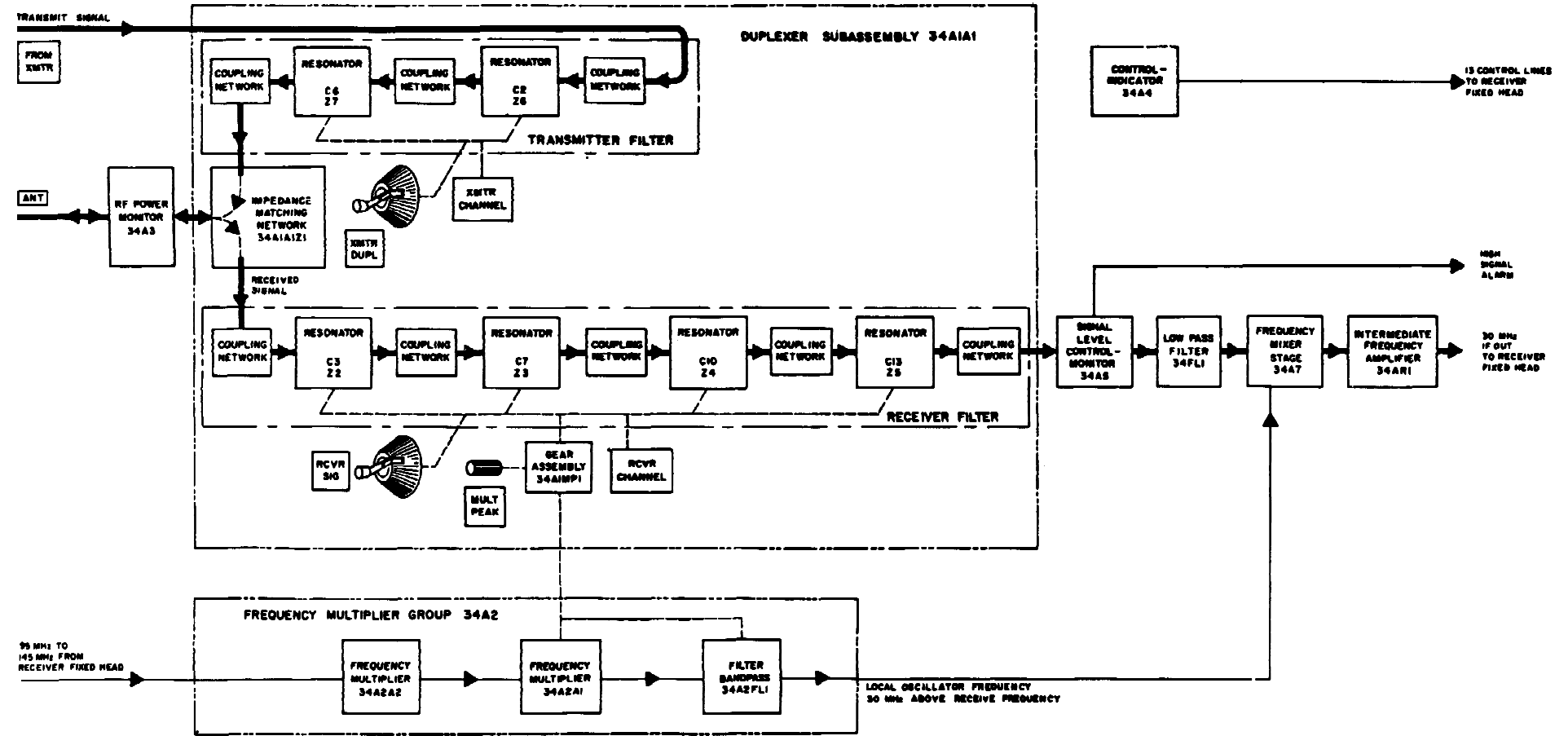
CHANNEL NO CODING table with columns XMTA, RCVR, and 12 coding positions (1-12).

CHANNEL NO CODING table with columns XMTA, RCVR, and 12 coding positions (1-12).

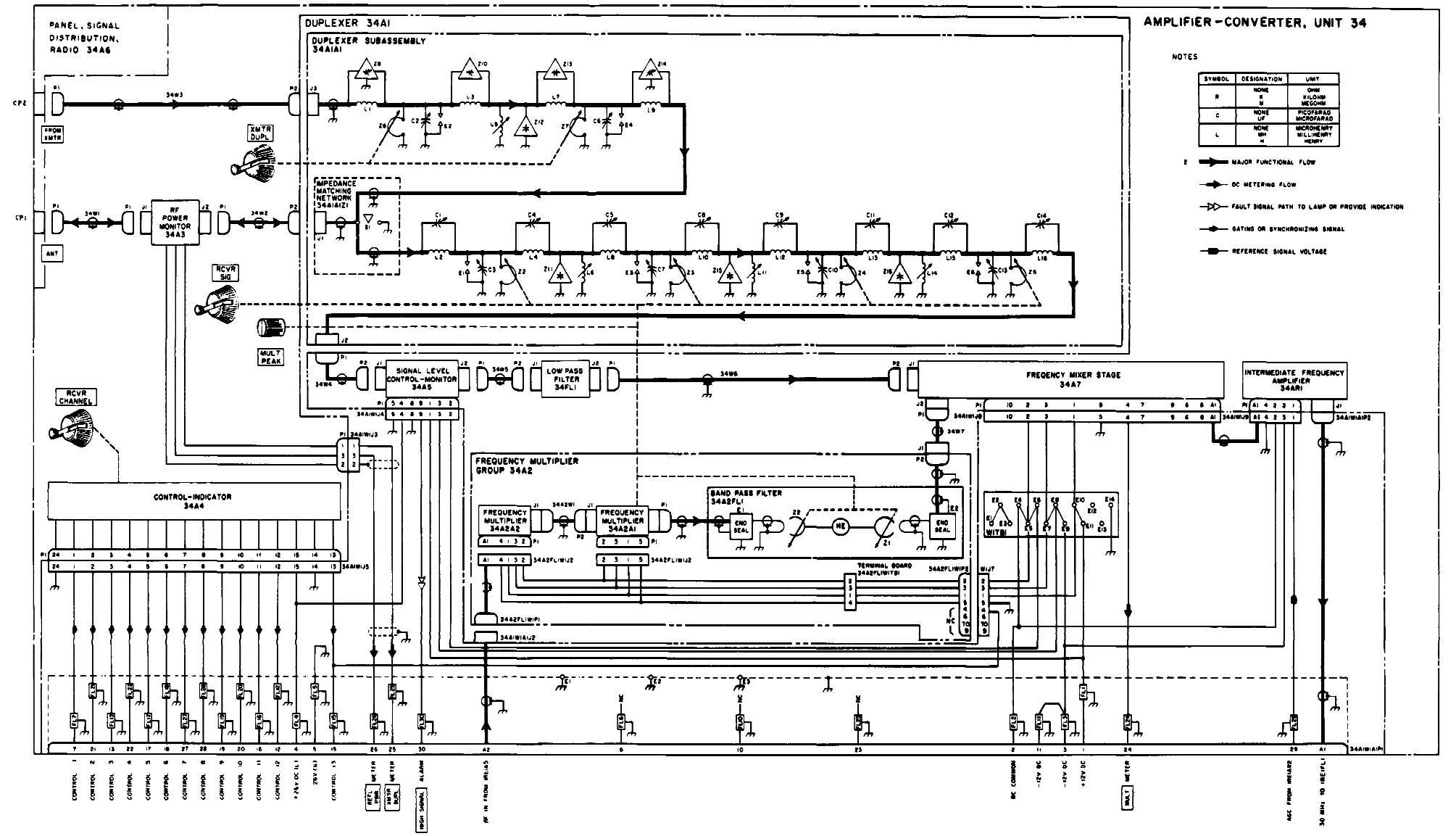
CHANNEL NO CODING table with columns XMTA, RCVR, and 12 coding positions (1-12).



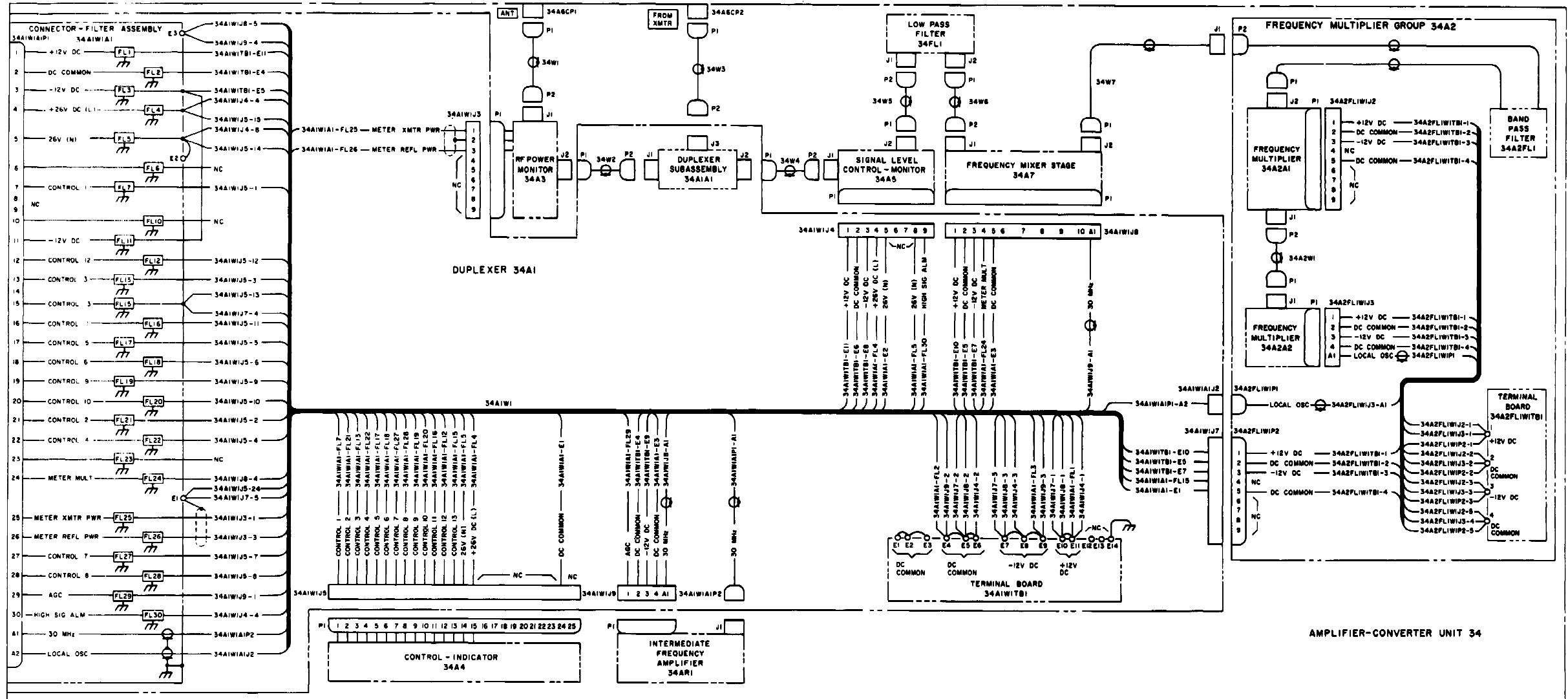




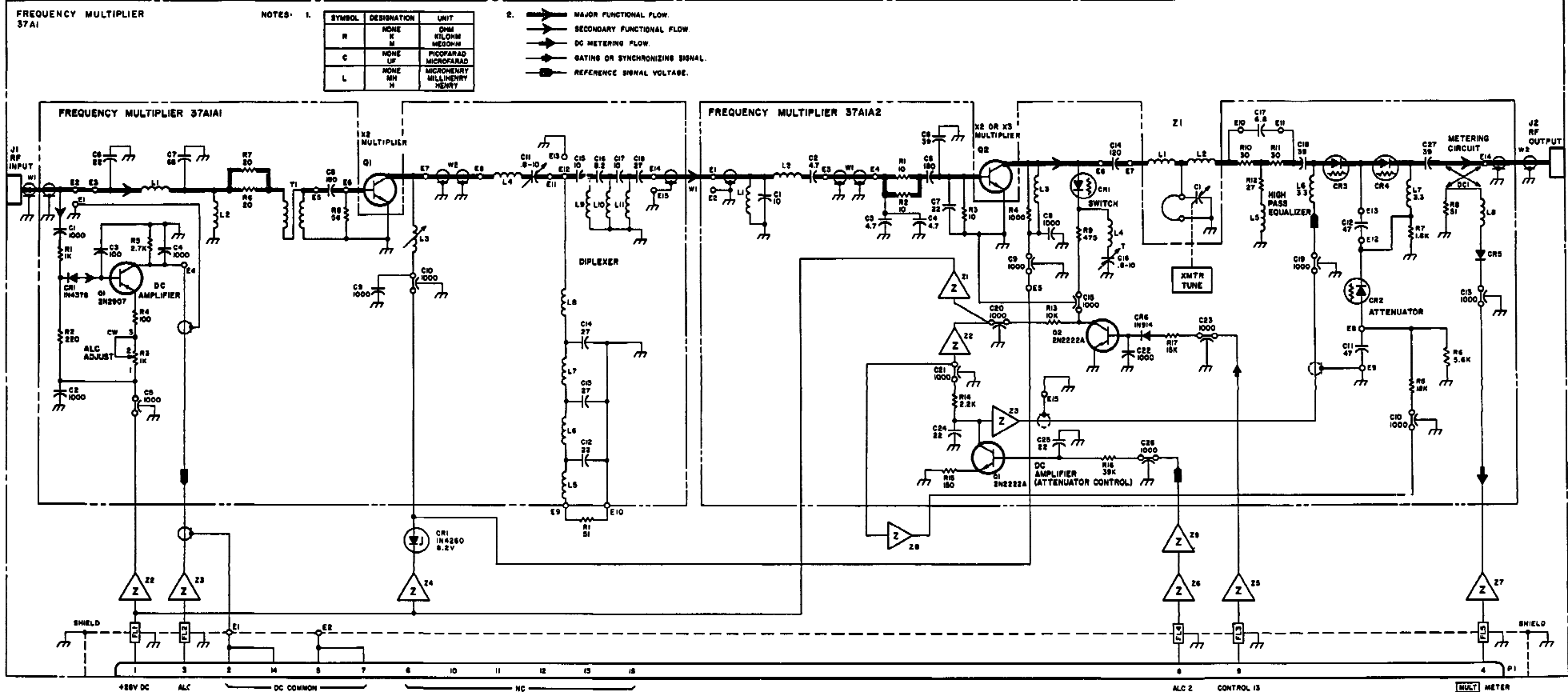
EL5RE290



FO-4-63. Amplifier - Converter AM-4318/GRC-103(V) Band III Receiver Rf Head, Schematic Diagram.



FO-4-64. Amplifier-Converter AM-4318/GRC-103(V) Band III Receiver R1 Head, Interconnecting Diagram.

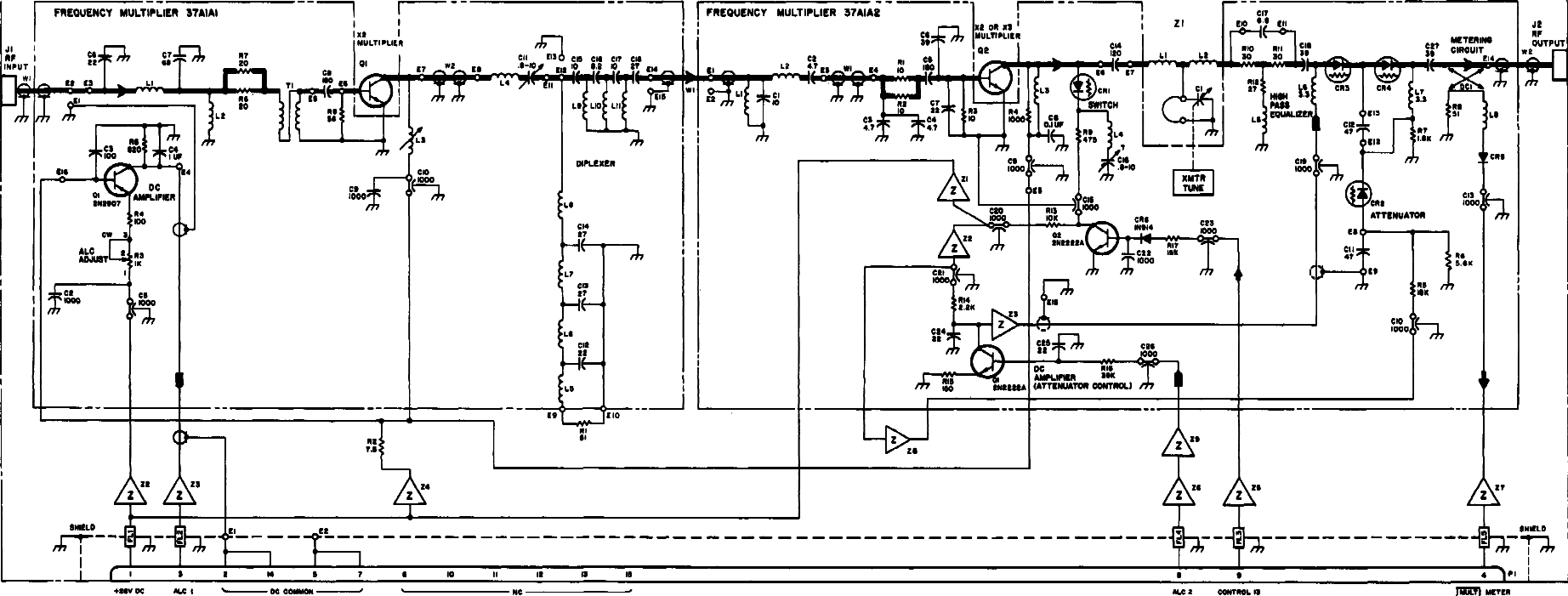


FREQUENCY MULTIPLIER  
37A1

NOTES: 1.

| SYMBOL | DESIGNATION | UNIT                                  |
|--------|-------------|---------------------------------------|
| R      | RESISTOR    | OHM<br>K<br>M                         |
| C      | CAPACITOR   | PICOFARAD<br>MICROFARAD<br>MILLIFARAD |
| L      | INDUCTOR    | OHM<br>MILLIHENRY<br>HENRY            |

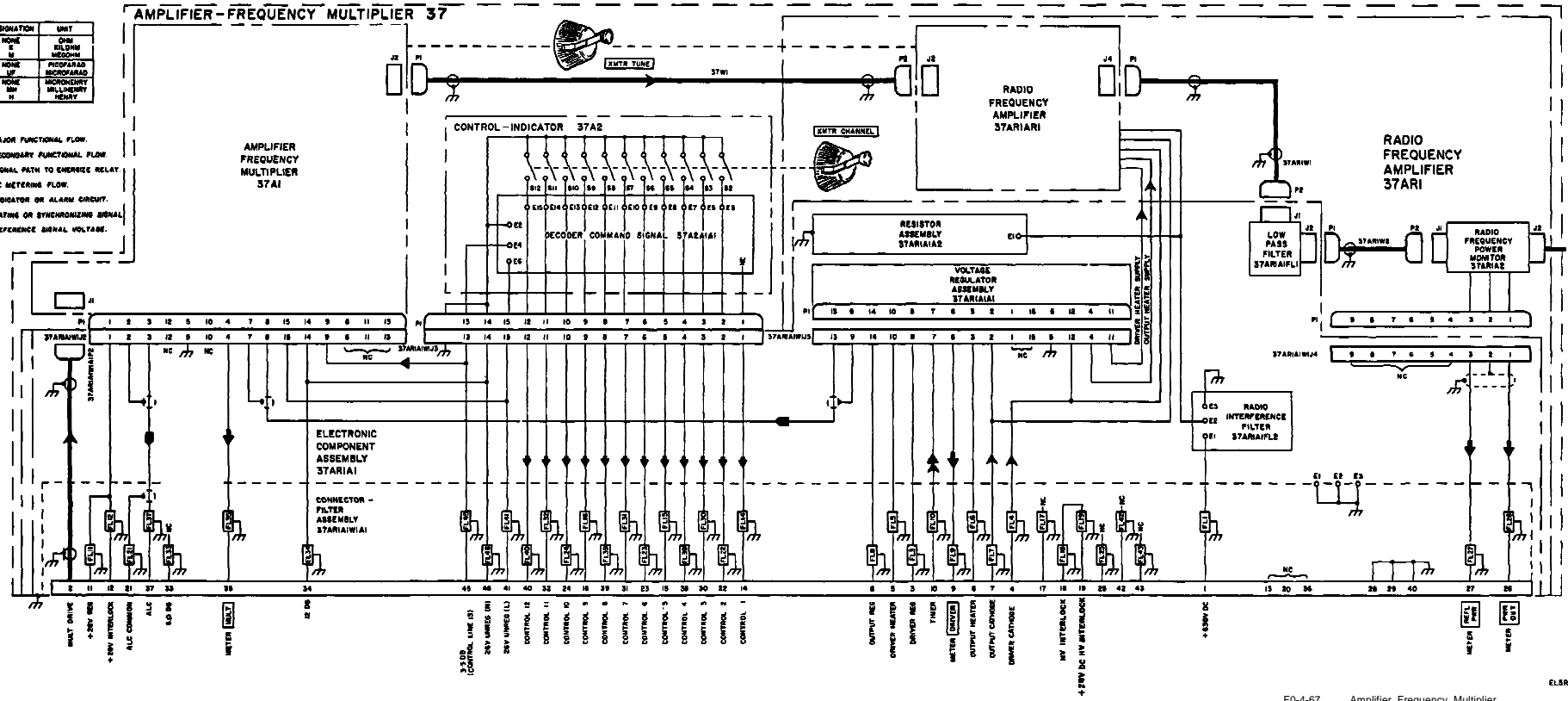
- 2.
- ➔ MAJOR FUNCTIONAL FLOW.
  - ➞ SECONDARY FUNCTIONAL FLOW.
  - ➞ DC METERS FLOW.
  - ➞ GATING OR SYNCHRONIZING SIGNAL.
  - ➞ REFERENCE SIGNAL VOLTAGE.



NOTES:

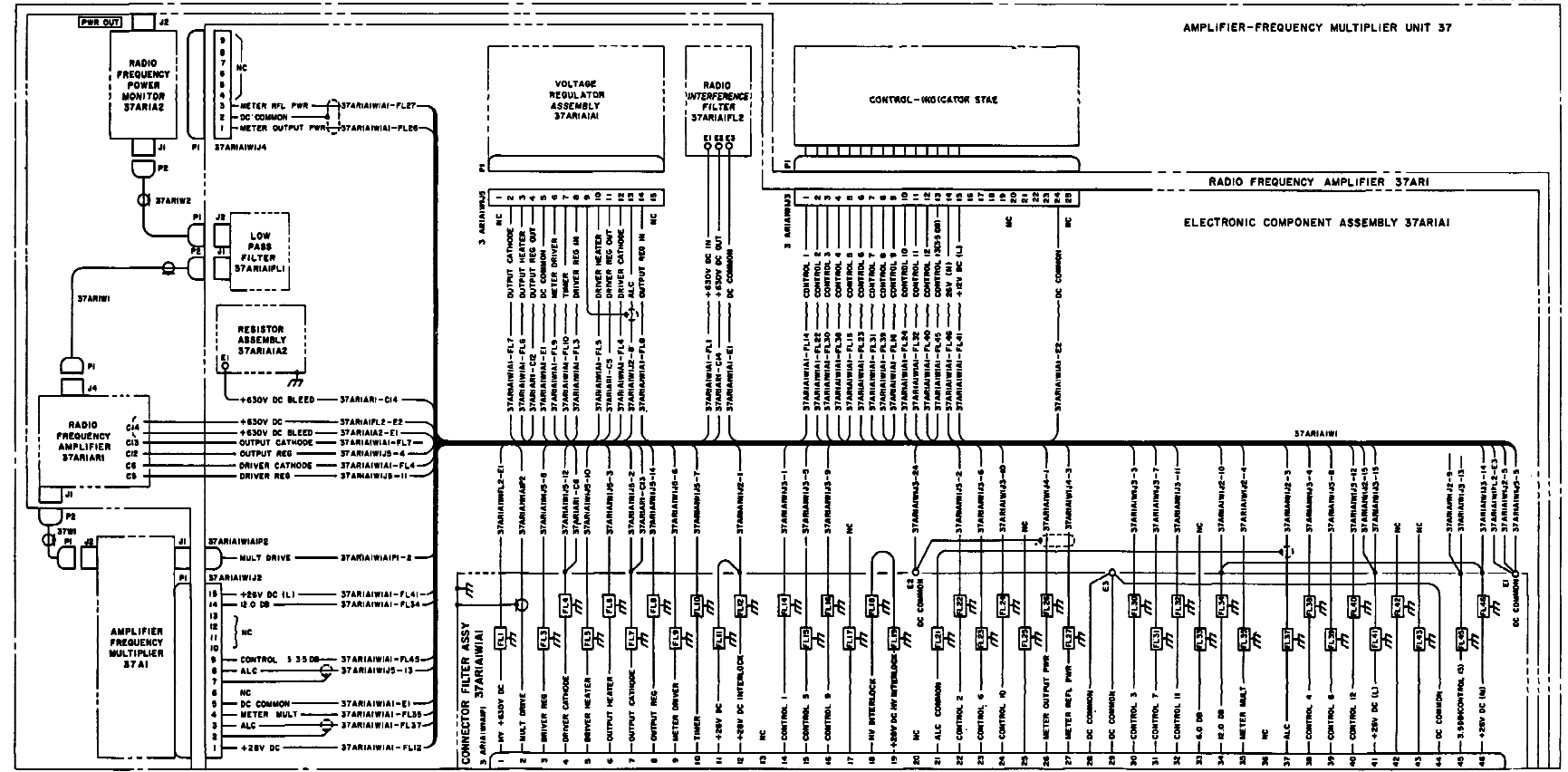
| SYMBOL | DESCRIPTION | UNIT          |
|--------|-------------|---------------|
| R      | NONE        | OHM           |
| K      | NONE        | KILOHM        |
| M      | NONE        | MEGOHM        |
| C      | NONE        | PICOPICOFARAD |
| P      | NONE        | PICOPICOFARAD |
| L      | NONE        | MICROHENRY    |
| H      | NONE        | MILLIHENRY    |

- ➔ MAJOR FUNCTIONAL FLOW.
- ➔ SECONDARY FUNCTIONAL FLOW.
- ➔ SIGNAL PATH TO ENERGIZE RELAY.
- ➔ DC METERING FLOW.
- ➔ INDICATOR OR ALARM CIRCUIT.
- ➔ GATING OR SYNCHRONIZING SIGNAL.
- ➔ REFERENCE SIGNAL VOLTAGE.



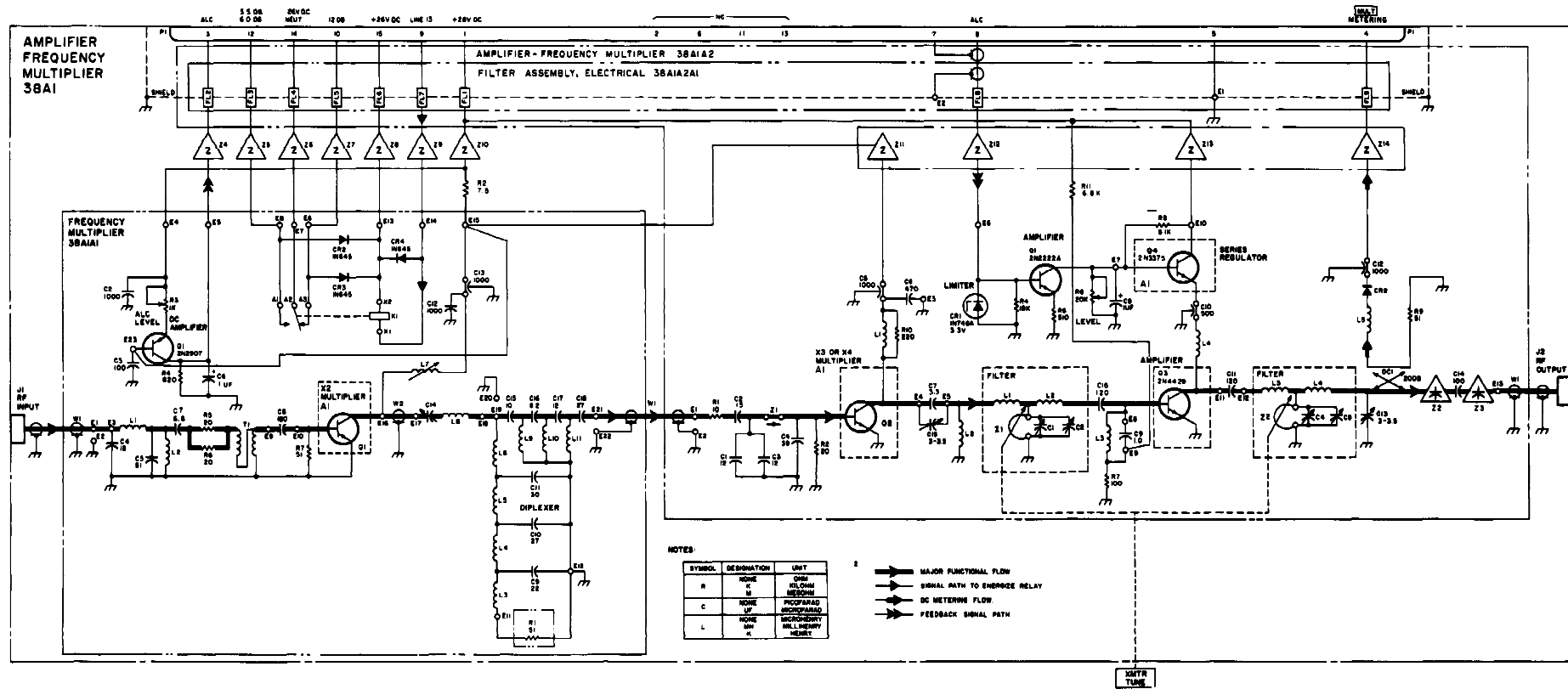
F0-4-67. Amplifier Frequency Multiplier AM-4321/GRC-103(V) and AM-4321A/GRC-103(V) Band II Transmitter Rf Head, Schematic Diagram.

ELSR209



F0-4-68. Amplifier-Frequency Multiplier AM-4321/GRC-103(V) and AM-4321A/GRC-103(V) Band II Transmitter RF Head, Interconnecting Diagram.

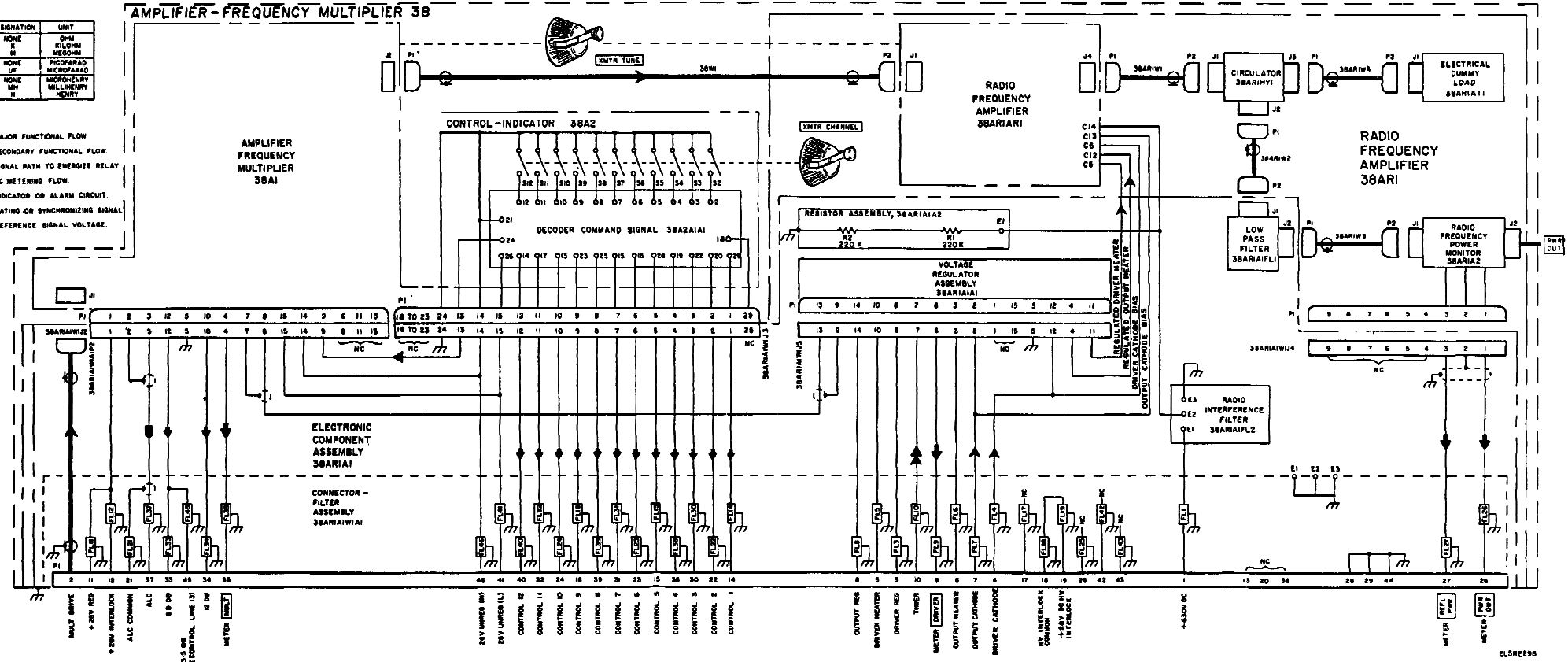




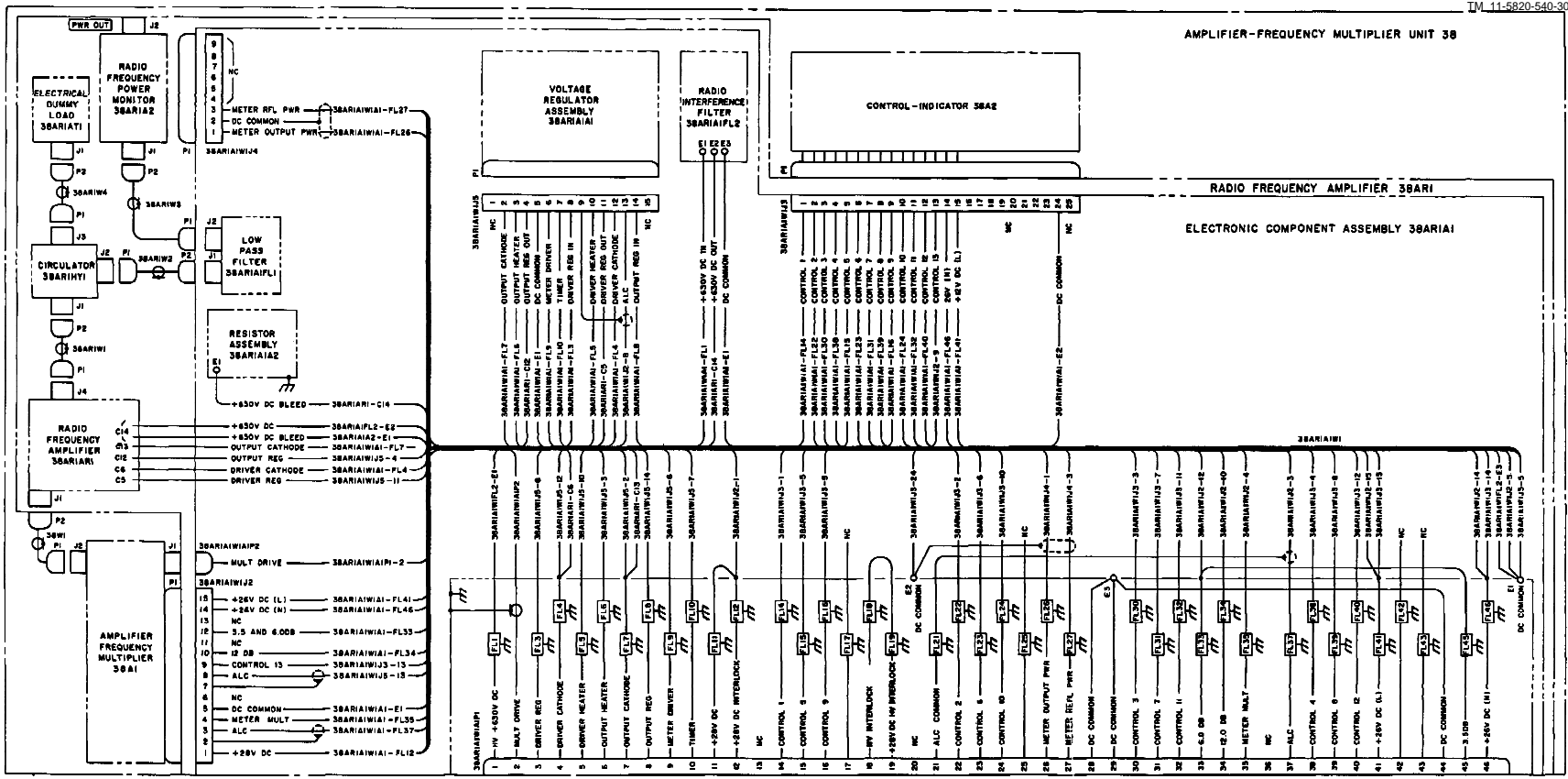
NOTES

| SYMBOL | DESIGNATION | UNIT       |
|--------|-------------|------------|
| R      | NONE        | OHMS       |
| K      | NONE        | KILOHMS    |
| M      | NONE        | MEG OHMS   |
| C      | NONE        | PICOFARAD  |
| P      | NONE        | PICOFARAD  |
| L      | NONE        | MICROHENRY |
| MH     | NONE        | MILLIHENRY |
| H      | NONE        | HENRY      |

- ➔ MAJOR FUNCTIONAL FLOW
- ➔ SECONDARY FUNCTIONAL FLOW
- ➔ SIGNAL PATH TO ENERGIZE RELAY
- ➔ DC METERING FLOW
- ➔ INDICATOR OR ALARM CIRCUIT
- ➔ BATING OR SYNCHRONIZING SIGNAL
- ➔ REFERENCE SIGNAL VOLTAGE



F0-4-70. Amplifier-Frequency Multiplier AM-4322/GRC-103(V) and AM-4322A/GRC-103(V) Band III Transmitter Rf Head, Schematic Diagram.



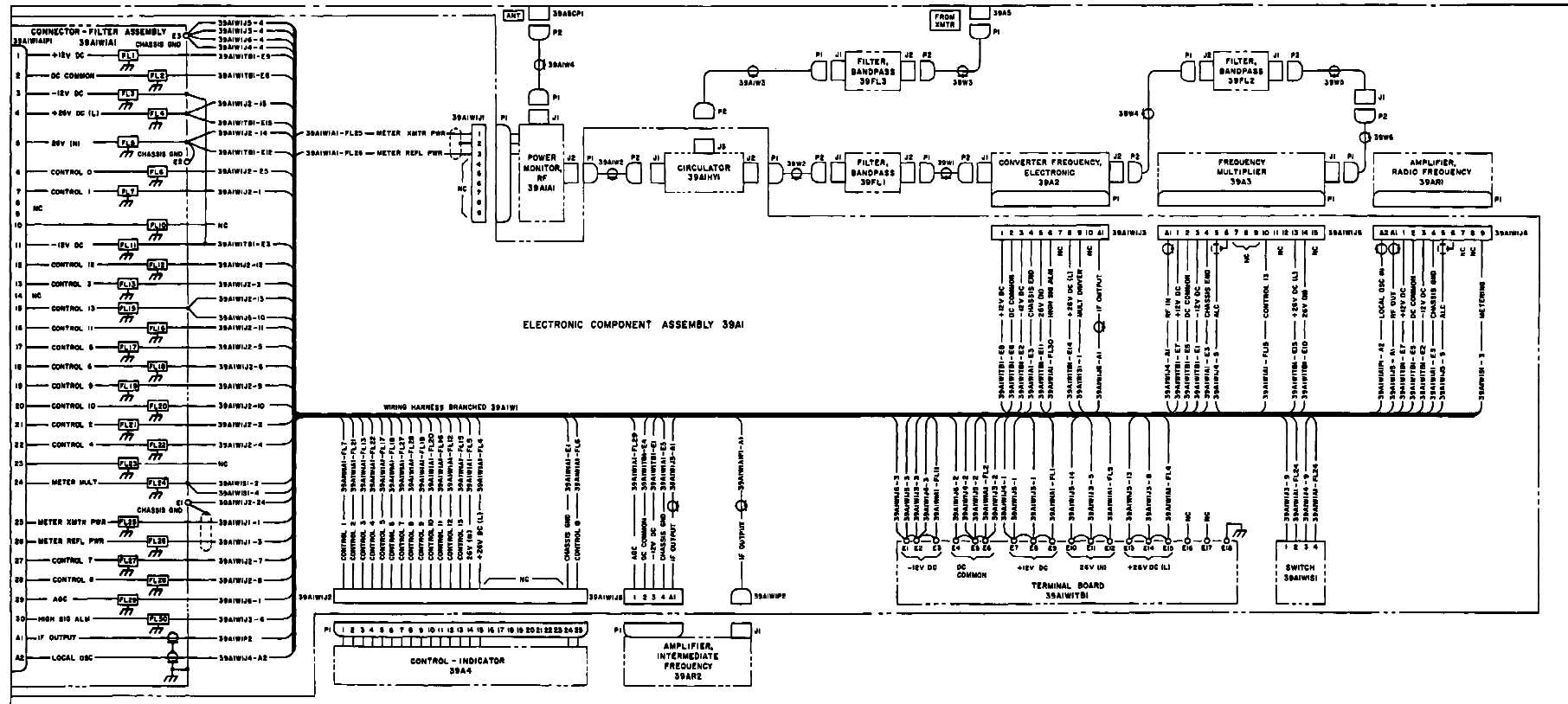
FO-4-71. Amplifier-Frequency Multiplier AM-4322(GRC-103(V)) and AM-4322A(GRC-103(V)) Band III Transmitter RF Head, Interconnecting Diagram.









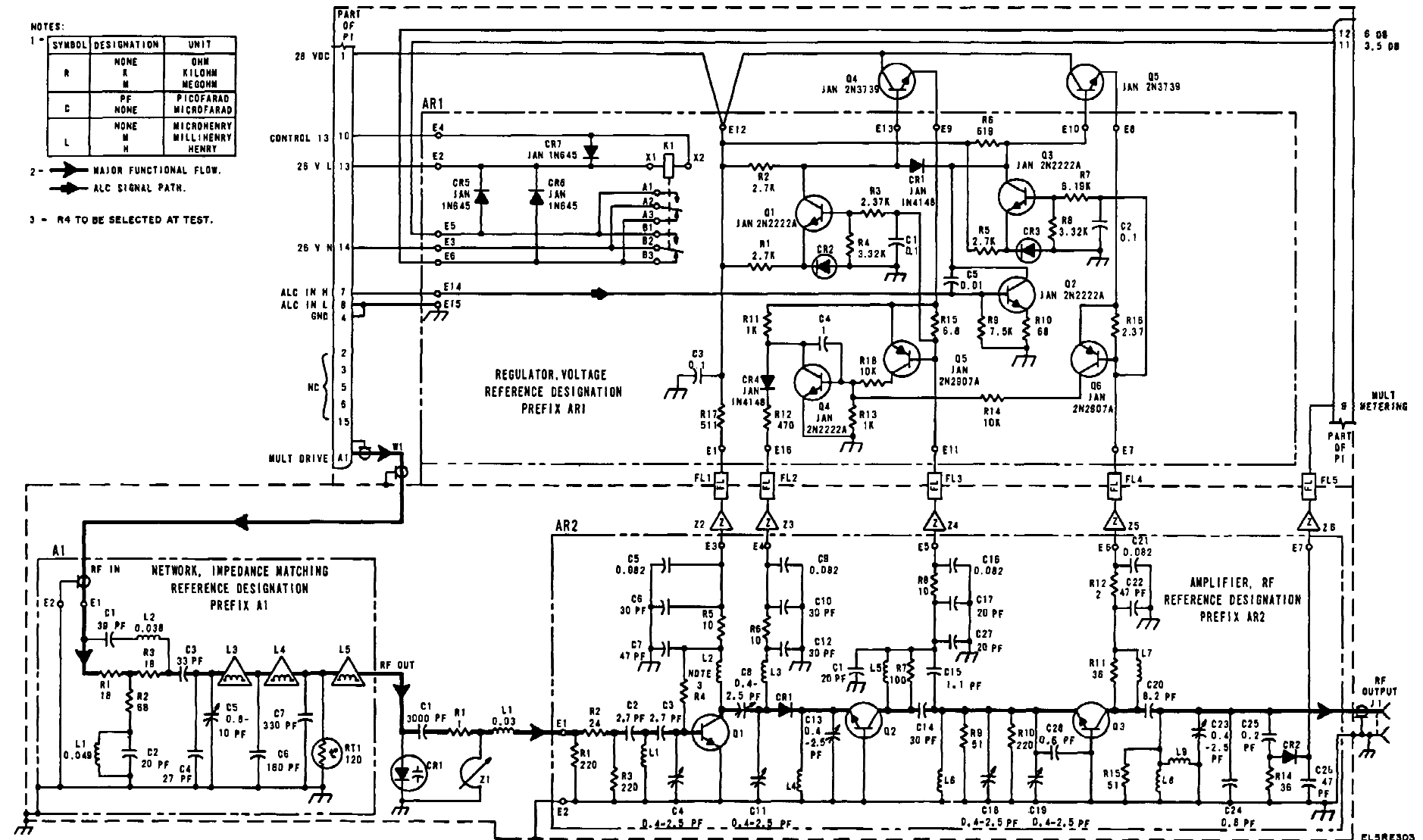




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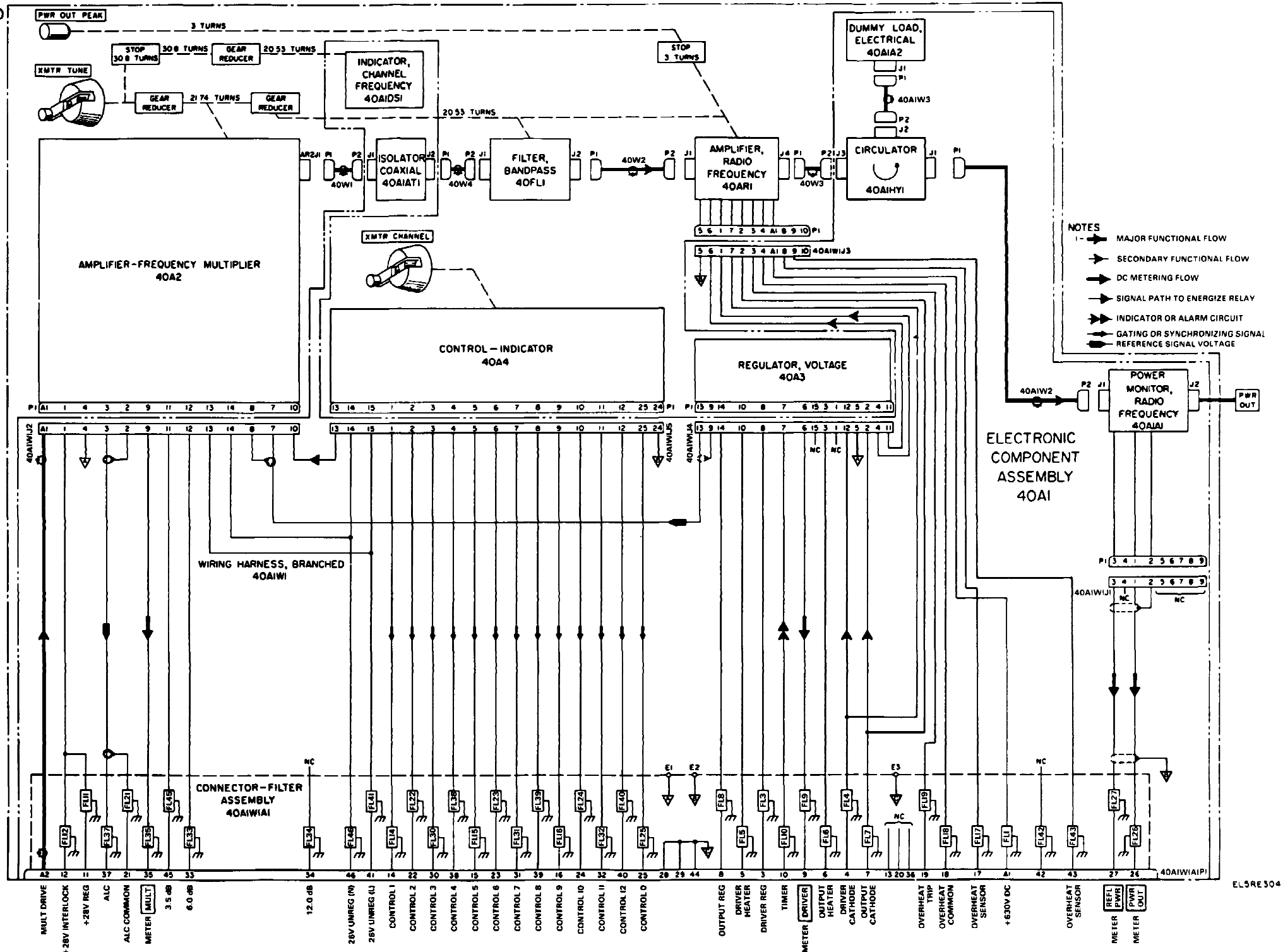
| 1 - SYMBOL | DESIGNATION    | UNIT                               |
|------------|----------------|------------------------------------|
| R          | NONE<br>K<br>M | OHM<br>KILOHM<br>MEG OHM           |
| C          | PF<br>NONE     | PICOFARAD<br>MICROFARAD            |
| L          | NONE<br>M<br>H | MICROHENRY<br>MILLI-HENRY<br>HENRY |

2 - MAJOR FUNCTIONAL FLOW.  
 3 - ALC SIGNAL PATH.  
 3 - R4 TO BE SELECTED AT TEST.



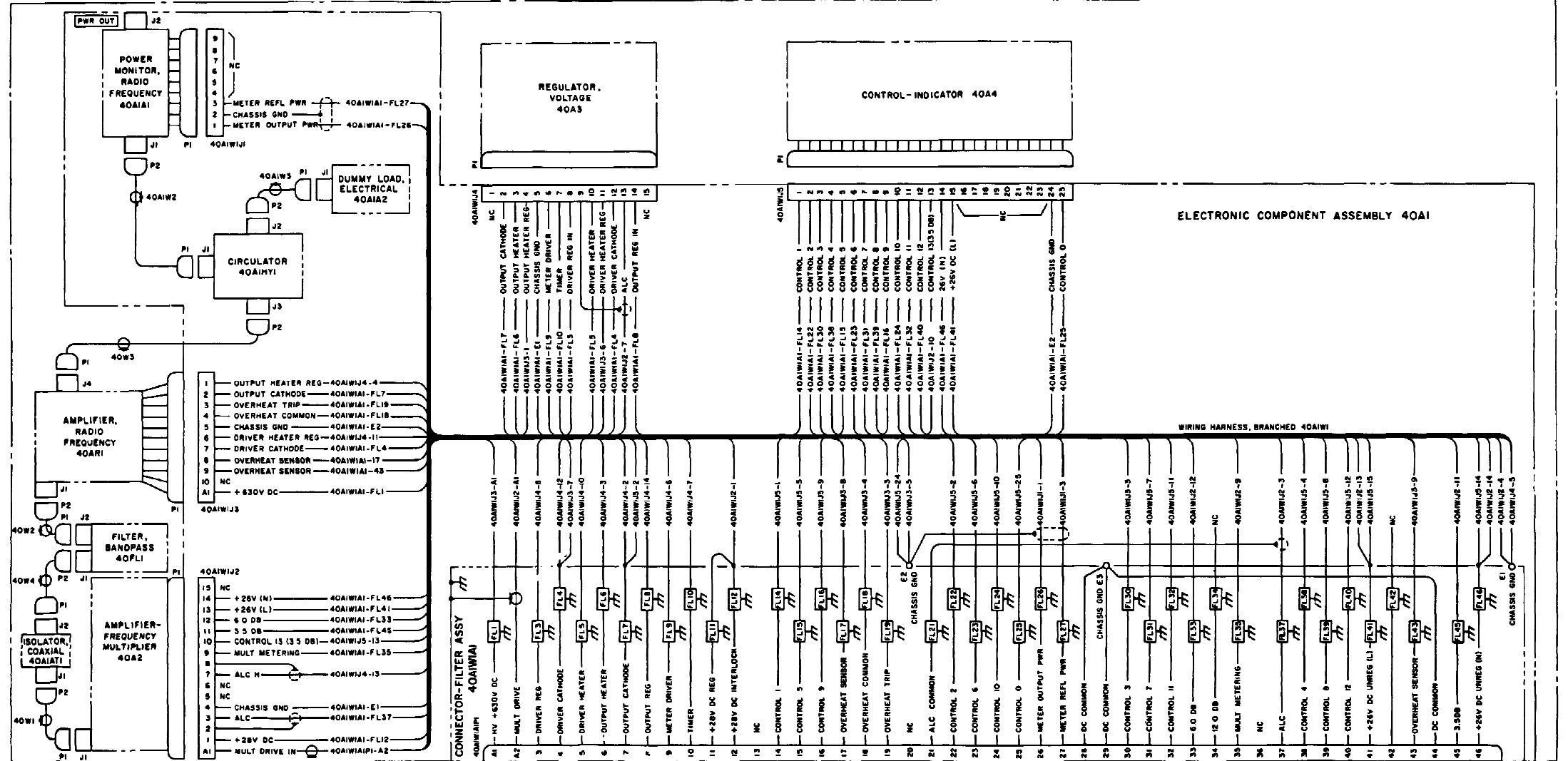
F0-4-75. Amplifier-Frequency Multiplier 40A2, Schematic Diagram.

UNIT 40



F0-4-76. Amplifier-Frequency Multiplier AM-4323/GRC-103(V) Band IV Transmitter Rf Head, Schematic Diagram.

EL5RE304



F0-4-77. Amplifier-Frequency Multiplier AM-4323/GRC-103(V) Band IV Transmitter Rf Head, Interconnecting Diagram.

