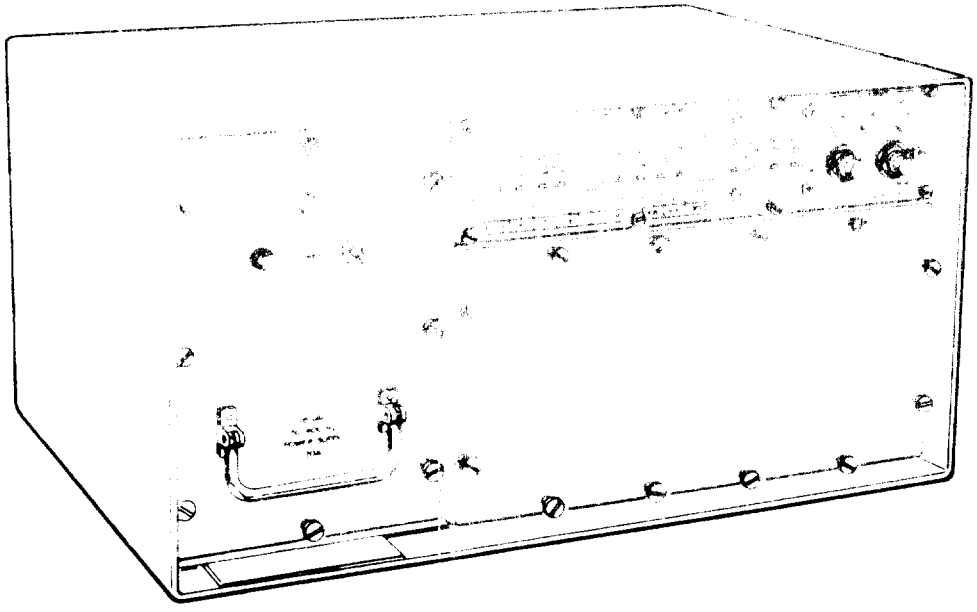
TM 11-5805-638-34

DIRECT SUPPORT AND GENERAL SUPPORT

MAINTENANCE MANUAL



MULTIPLEXER, TIME DIVISION, DIGITAL TD-1069/G (NSN 5805-01-028-8425)

This copy is a reprint which includes current pages from Changes 1.

HEADQUARTERS, DEPARTMENT OF THE ARMY

23 MARCH 1983

CHANGE

No. 1

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 17 September 1984

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL MULTIPLEXER, TIME DIVISION, DIGITAL TD-1069/G (NSN 5805-01-028-8425)

TM 11-5805-638-34, 23 March 1983, is changed as follows.

1. New or changed materiel is indicated by a vertical bar in the margin of the page.

2. Remove old pages and insert new pages as indicated below:

Remove pages	*Insert pages*
l-l and l-2	l-l and l-2
2-l and 2-2	2-l and 2-2
3-13 through 3-16	3-13 through 3-16
A-l and A-2	A-l and A-2

3. File this change sheet in front of the publication.

By Order of the Secretary of the Army:

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General, United States Army
Chief of Staff

Official:

ROBERT M. JOYCE
Major General, United States Army
The Adjutant General

Distribution:

To be redistributed in accordance with specialist.

WARNING

When TDDM is connected to 115 Vac power source, high voltage is present at exposed power supply connector inside the chassis. Also, high voltage is present at exposed components when power supply covers are removed. DEATH or SERIOUS injury may result from contact.

WARNING

Compressed air shall not be used for cleaning purposes except where reduced to less than 29 pounds per square inch (psi) and then only with effective chip guarding and personnel protective equipment. Do not use compressed air to dry parts when TRICHLOROTRIFLUOROETHANE has been used. Compressed air is dangerous and can cause serious bodily harm if protective means or methods are not observed to prevent chip or particle (of whatever size) from being blown into the eyes or unbroken skin of the operator or other personnel.

WARNING

Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL

4. SEND FOR HELP AS SOON AS POSSIBLE

5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

Technical Manual
No. 11-5805-638-34

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 23 March 1983

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL TIME DIVISION DIGITAL MULTIPLEXER TD-1069/G (NSN 5805-01-028-8425)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703. In either case, a reply will be furnished direct to you.

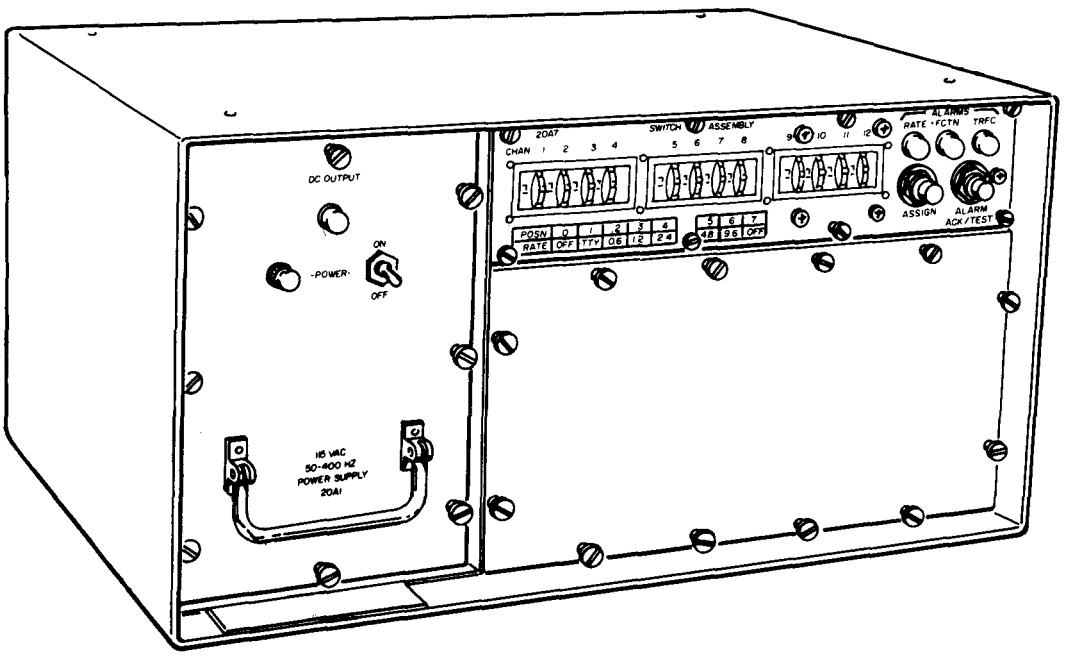
Table of Contents

Table of Contents (Continued)

HOW TO USE THIS MANUAL

- This manual tells you about direct support and general support maintenance for the Time Division Digital Multiplexer TD-1069/G.
- Remember when you read this manual that your mission will be to determine the type of equipment you have at your site and use only those instructions applicable to your category of maintenance and equipment configuration.
- Additional manuals that you should use when operating and maintaining the TD-1069/G are listed in Appendix A. Components of end item and basic issue items to help you inventory items are listed in Appendix C, TM 11-5805-638-12 and additional items you are authorized for support of the TD-1069/G are listed in Appendix D, TM 11-5805-638-12.
- Use Appendix B, Maintenance Allocation Chart (MAC) TM 11-5805-638-12 to determine items applicable to your maintenance level. Use Appendix B of this manual for Items you will need during repair of the TD-1069/G.
- In this manual, paragraphs are numbered sequentially. If you are looking for specific information, use the subject index at the back of the manual to locate the page where the topic is discussed. For your convenience a table of contents is included at the beginning of each chapter.

MULTIPLEXER, TIME DIVISION
DIGITAL TD-1069/G



CHAPTER 1
INTRODUCTION

Section I. GENERAL INFORMATION

1-1. SCOPE

This manual describes direct and general support maintenance for Time Division Digital Multiplexer TD-1069/G hereafter referred to as the TDDM. It includes instructions and information for troubleshooting, repairing and testing the TDDM. Also contained in the manual is a description of all tools, test equipment and materials needed for maintenance. The TDDM and its components are described in section III of this chapter. Operating instructions are covered in TM 11-5805-638-12.

1-2. MAINTENANCE FORMS, RECORDS, AND REPORTS

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750 as contained in Mainteannce Management Update.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73A/AFR 400-54/MCO 4430.3F.

c. Discrepancy in Shipment Report (DISREP) (SF361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1-2.1 CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

1-3. DESTRUCTION OF ARMY ELECTRONIC MATERIEL

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 11-750-244-2.

1-4. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR)

If your TDDM needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703. We'll send you a reply.

1-5. ADMINISTRATIVE STORAGE

Administrative Storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS charts before storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness. Disassembly and repacking of equipment for shipment or limited storage are covered in TM 11-5805-638-12.

Section II. EQUIPMENT DESCRIPTION AND DATA

1-6. PURPOSE AND USE

PURPOSE:

- Multiplexes and Demultiplexes up to twelve channels of digital data through land lines.
- Accommodates one to twelve channels of mixed data/TTY with combined input rates of up to 30 kbps maximum.
- Provides interface capability for frequency shift keying (FSK) TTY signals compatible with TH-22/TG telegraph terminal.
- Provides interface capability with devices using balanced conditioned diphase (CDP) and/or balanced NRZ teletypewriter signals.

USE:

- Ground transportable communications device.
- For use in field Army at Command and Area Signal Centers.

1-7. LOCATION AND DESCRIPTION OF COMPONENTS

See TM 11-5805-638-12.

1-8. SUMMARY OF DESIGN CHARACTERISTICS

a. Size and Weight. The TDDM measures: 8.5 inches high, 17.25 inches wide, 12.0 inches deep and weighs approximately 34 pounds.

b. Digital Channel Characteristics. Accommodates the following:

(1) CDP data at 600, 1200, 2400, 4800 and 9600 bits per second (b/s).

(2) NRZ teletype signals up to 150 baud synchronous or start stop.

(3) FSK teletype signal up to 150 baud at 1317.5 Hz (mark) and 1232.5 Hz (space).

c. Channel Configuration. Each of the twelve channel positions in the PWB card nest accept either digital or FSK channel cards (modules). Any configuration of the two types of modules may be used, in any order, in the twelve channel positions. The desired mode and data rate selection is made, for each channel, by using the thumbwheel switches provided on the Switch Assembly (20A7).

d. Multiplexed Characteristics. The twelve data channels are multiplexed and demultiplexed in conditioned diphase (CDP) full duplex group MUX traffic at a rate of 32 kbps.

e. Power Requirements. The power requirement is 115 Vac plus or minus 10 percent at 50, 60 or 400 Hz. Provides +5 Vdc, +12 Vdc and -12 Vdc to the functional modules.

1-9. SAFETY, CARE AND HANDLING

Safety instructions are on the WARNING page found inside the manual's front cover. All WARNINGS, CAUTIONS and NOTES should be read carefully. Cleaning instructions are provided in TM 11-5805-368-12.

Although the TDDM is lightweight (34 pounds), use a firm grip with both hands when carrying. Do not attempt to hand carry for long distances.

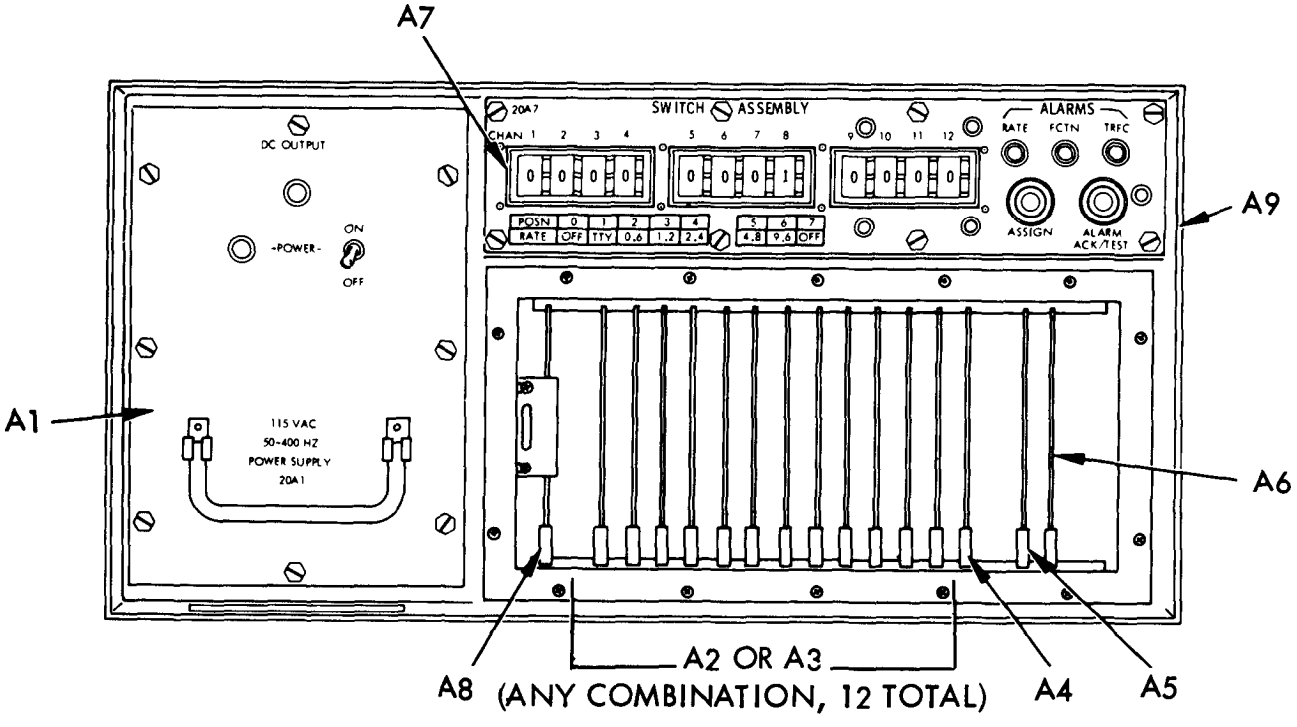
The card nest cover, backplane cover, Switch Assembly, and the Power Supply, employ the use of captive screws for ease of removal.

Use care when cabling the TDDM. Connector and cable assemblies are keyed for easy installation. If not properly aligned, the equipment may be damaged.

1-10. REFERENCE DESIGNATIONS AND ABBREVIATIONS

Assembly numbers identify the TDDM assemblies, modules and chassis.

Assembly Number	Assembly/Item Name	Quantity
20A1	Power Supply Assembly (A1)	1
20A2	Digital Data Channel (A2)	6
20A3	FSK Data Channel (A3)	6
20A4	Digital Clock Pulse Generator (A4)	1
20A5	Digital Controller (A5)	1
20A6	Alarm Memory (A6)	1
20A7	Switch Assembly (A7)	1
20A8	Overvoltage Absorber Assembly (A8)	1
20A9	TDDM Chassis (A9)	1



Section III. TECHNICAL PRINCIPLES OF OPERATION

1-11. GENERAL

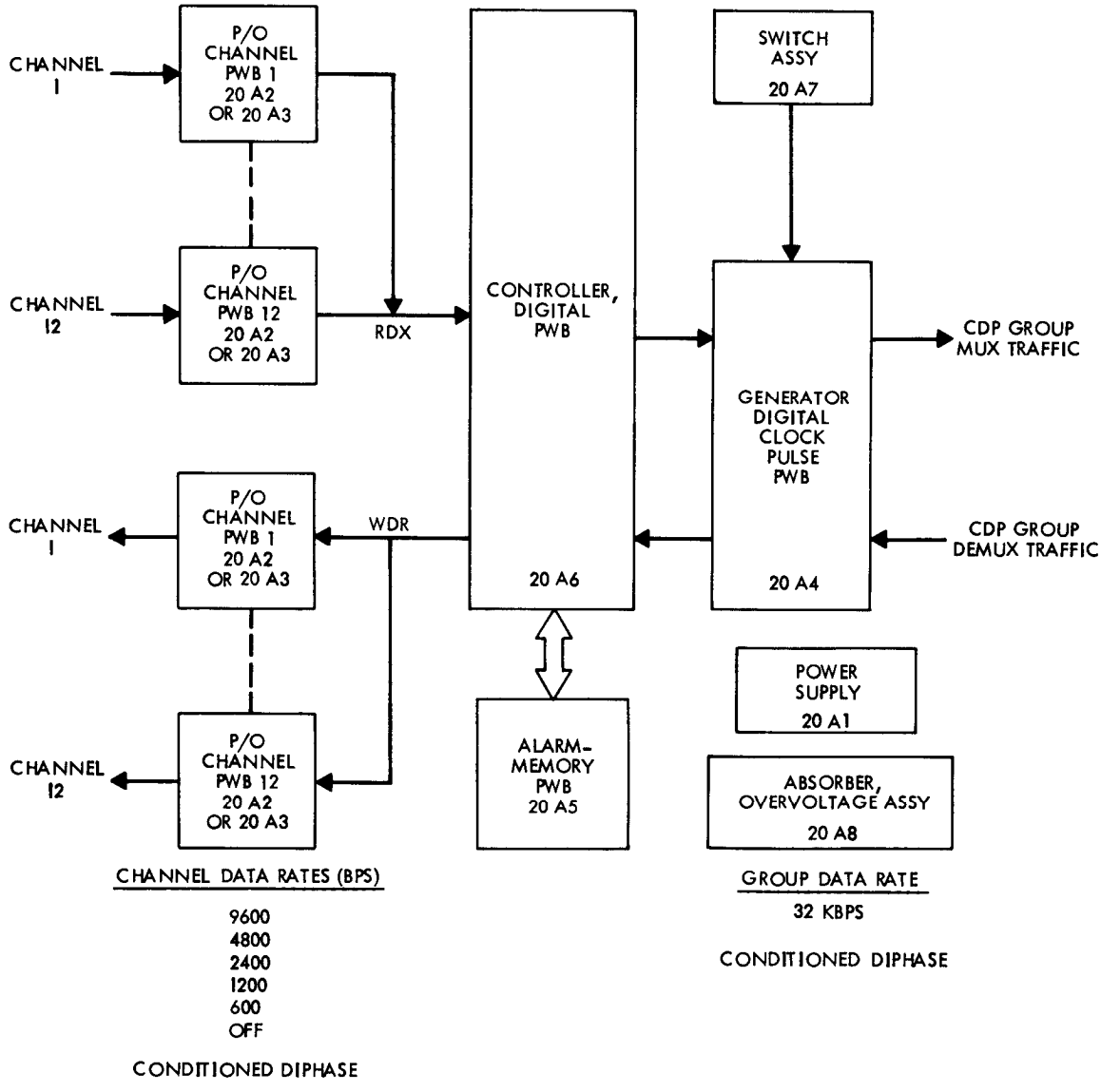
The TDDM provides 12 channels of full duplex digital communications. Functions required for each channel interface are duplicated on individual channel cards (modules). Each channel is functionally independent of the mode of operation of all other channels. As such, the system may contain any intermix of Digital Data (20A2) or FSK Data (20A3) channel modules up to a total of 12.

Each channel module contains one full duplex channel which is capable of operating at a data rate of 600, 1200, 2400, 4800 or 9600 bits per second (b/s). The data rate is selected by manipulation of the thumbwheel switches located on the Switch Assembly (20A7). The data channels are multiplexed and demultiplexed on Conditioned Diphase (CDP) full duplex group mux traffic at 32 kb/s. Protection from input surge is provided by the Overvoltage Absorber module (20A8).

The common logic for the TDDM is contained in the Digital Controller (20A5) and Alarm Memory (20A6) modules. The Common Control derives timing from the Digital Clock Pulse Generator (DCPG) module (20A4) and provides signals to the twelve channel modules which multiplex and demultiplex the 32 kHz group transmit and receive digital traffic.

The Power Supply (20A1) for the TDDM is a linear series regulator type and operates from 115 Vat, 50, 60 Hz or 400 Hz. It provides +5 Vdc, +12 Vdc and -12 Vdc to the functional modules. There are no timing or sequential circuits in the Power Supply.

Each module (including the Power Supply) has its own Built-In Test Equipment (BITE) to monitor and detect faults. The BITE circuits advise the operator of fault conditions through fault indicators and/or audible alarm. Detailed descriptions of each module are given later in this chapter.



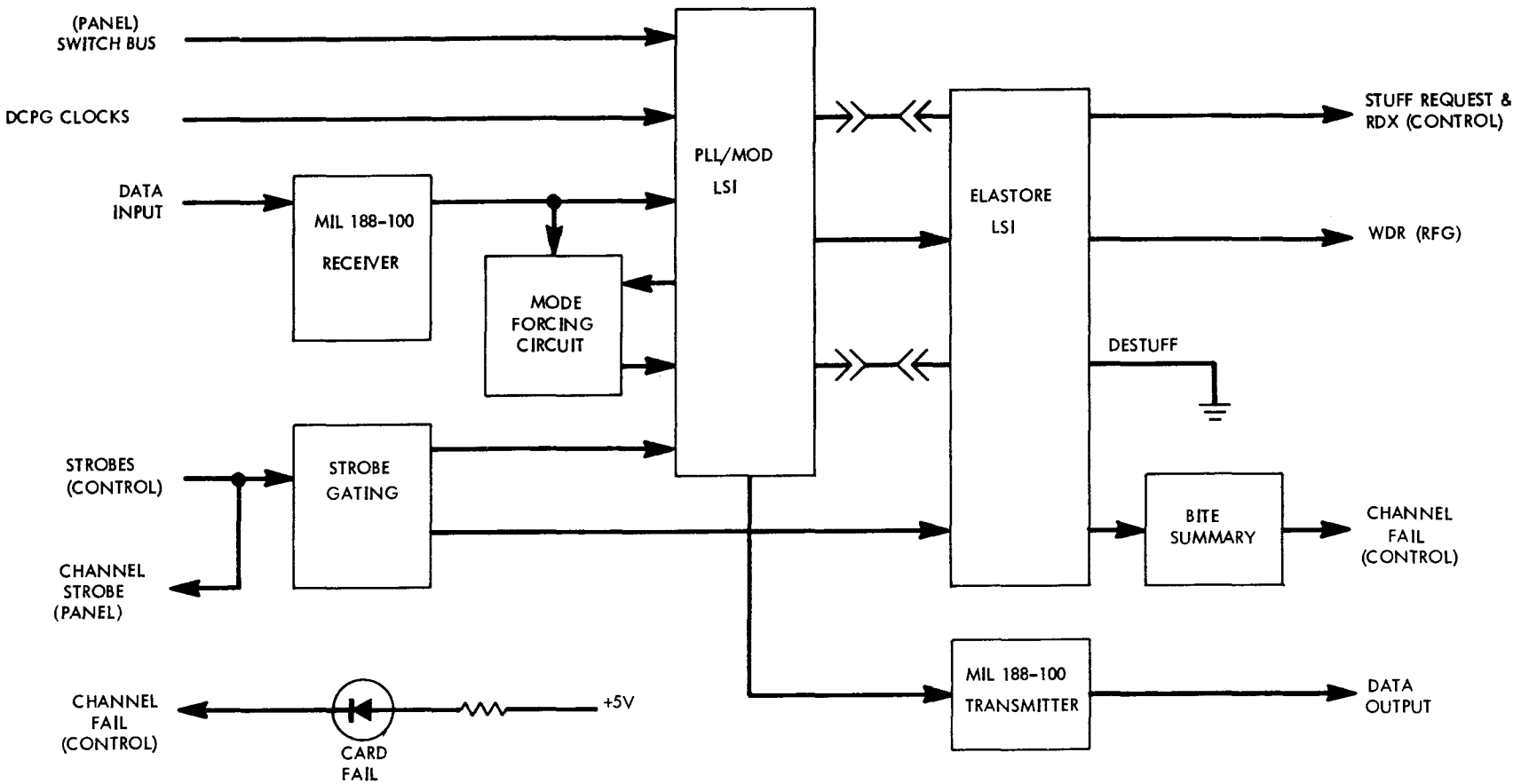
1-12. TDDM CHANNEL MODULES (20A2/20A3)

Functions required for each channel interface are repeated on individual channel cards (modules). Each channel is functionally independent of the mode of operation of all other modules. All functions common to the overall operation of the multiplexing and demultiplexing functions are grouped together onto the common modules. The channel modules and their interfaces to the common logic (modules 20A5 and 20A6) are designed so that each of the 12 channel slots can accept either a Digital Data Channel Module (20A2) or FSK Data Channel module (20A3) in any order or mix. Signals used by both types of modules are used in the same manner, requiring no changes in the common logic to accommodate both types of modules. Those signals unique to one type, i.e., FSK timing signals, are always present at the module location but used only by the card type requiring them.

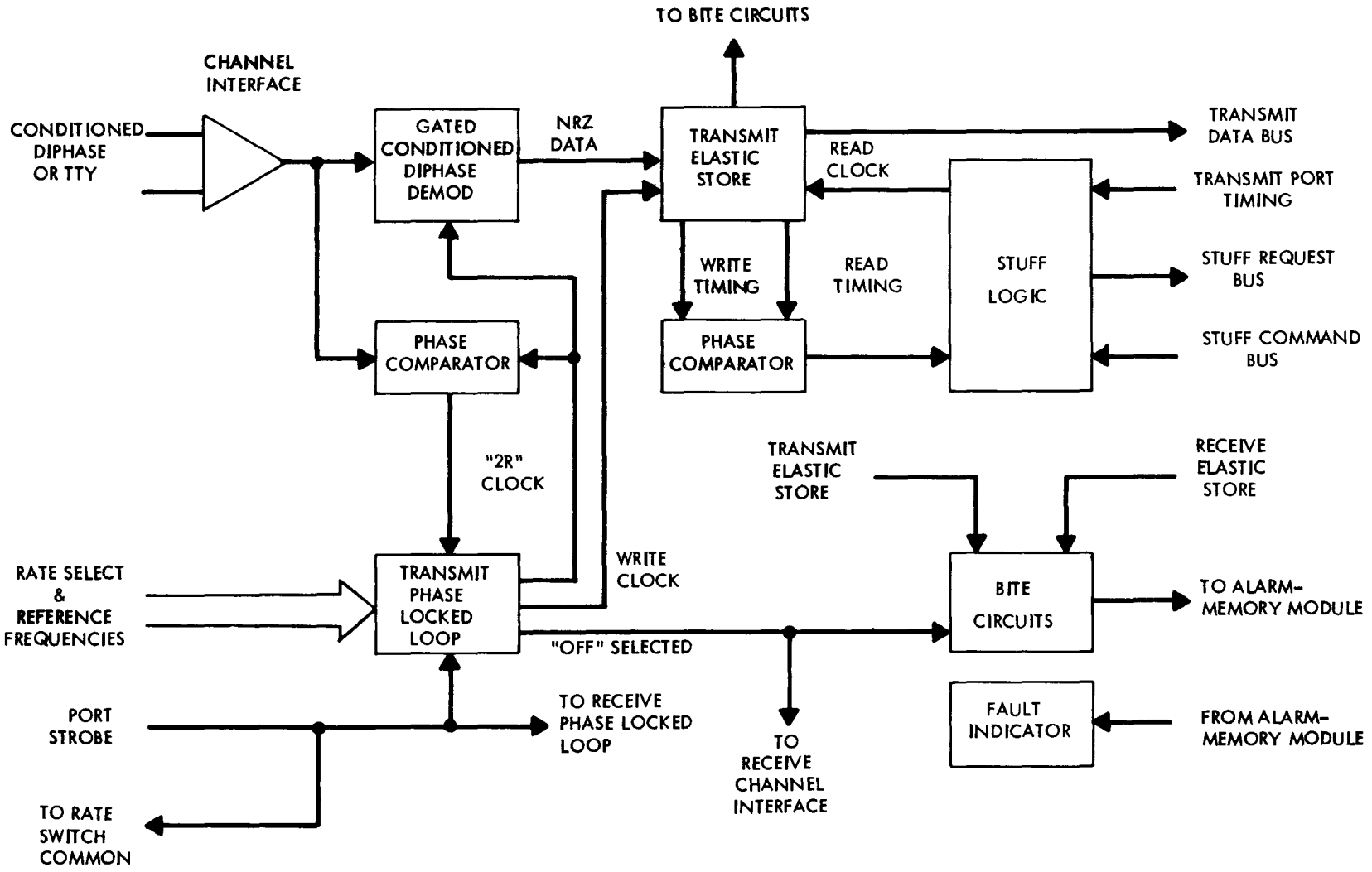
a. Digital Data Channel Module (20A2). The Digital Data Channel module provides from one to 12 of the channel interfaces to the group data buses of the TDDM. The interface is either conditioned diphase (CDP) at 600, 1200, 2400, 4800, or 9600 bits per second or teletype (TTY) at 45.5 to 150 baud processed at 1200 bits per second. The module accepts strobe pulses from the common control which controls its operation including the multiplexing and demultiplexing of group signals. Thumbwheel (Rate/Mode) switch data is loaded into module registers to program CDP or TTY and the bit rate under control of the strobes. The module also contains BITE circuitry to alert the common control of a failure and a light-emitting diode to indicate that the module has failed.

(1) Transmit Function Block Diagram. The transmit function block diagram shows that a phase comparator is used to compare CDP data with the 2R clock (twice the bit rate) generated by the transmit phase-locked loop (PLL). The output of the phase comparator selects either a high frequency reference (307.2 kHz + 108.6 ppm) or a low frequency reference (307.2 kHz -108.6 ppm) according to the phase error. Selection is made by dividing the selected reference clock. The CDP demodulator outputs NRZ data which, when strobed by the controller, are clocked into a transmit elastic store by the bit rate clock. A stuff request is returned to the controller module when the elastic store is less than half full. This results in a stuff command from the controller module which causes a data bit from the elastic store to be used twice. For TTY, the CDP demodulation function is omitted and the bit rate clock is at 1200 Hz, which occurs from alternating between the two reference clocks. The result is multiple sampling of the TTY having a maximum baud rate of 150.

DIGITAL DATA CHANNEL MODULE (20A2) BLOCK DIAGRAM

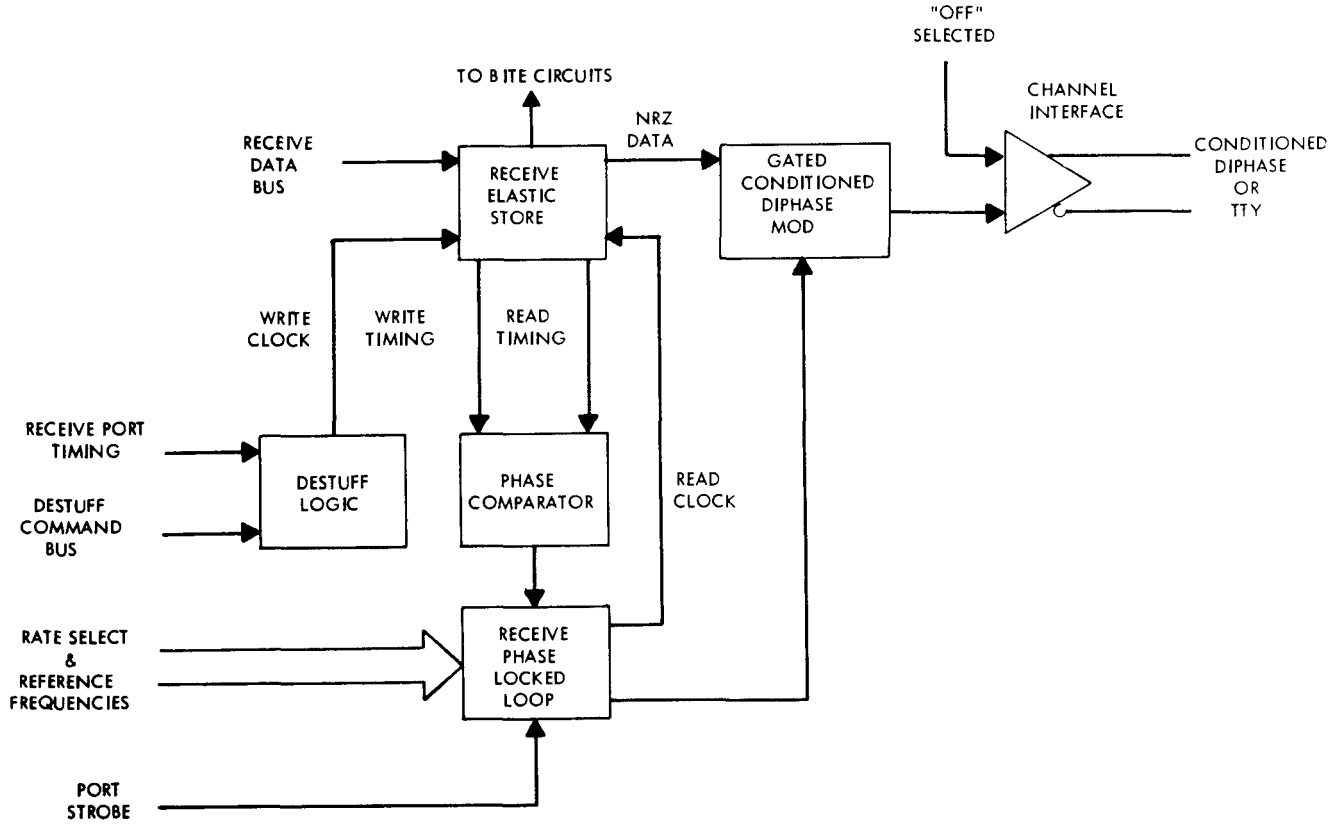


TRANSMIT FUNCTION BLOCK DIAGRAM



(2) Receive Function. The receive function uses the same frequency references as in the transmit function. A strobe from the controller resets the receive elastic store to midpoint. A phase comparator detects elastic store greater or less than half full to decide which frequency to use. The bit rate clock is obtained by dividing down the selected reference frequency.

RECEIVE FUNCTION BLOCK DIAGRAM



b. FSK Data Channel Module (20A3). The FSK Data Channel module provides from one to twelve of the TDDM channel interfaces. The interface (analog) is phase coherent as follows:

Modulator Output- 1232.5 and 1317.5 Hz nominal carrier frequencies, +1 dBm nominal balanced output, 600 ohms. Rates from 0-150 b/s. (See table 1-1.)

Demodulator Input- 1232.5 and 1317.5 Hz nominal, 600 ohms nominal balanced input. Rates from 0-150 b/s. (See table 1-2.)

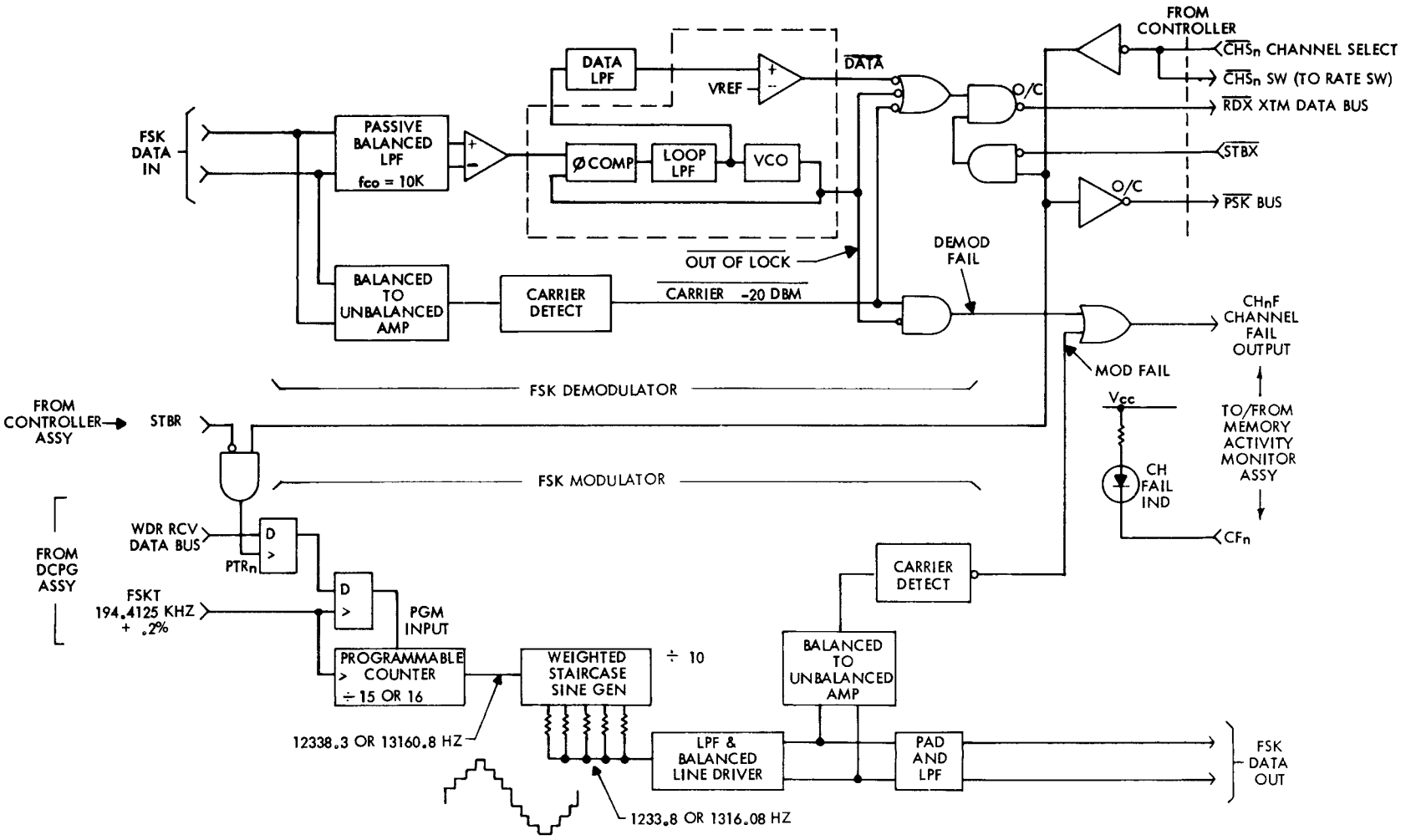
FSK TTY signals are compatible with the TH-22/TG terminal operating via up to five miles of cable. The FSK Data Channel module converts FSK signals into the equivalent of full-baud NRZ TTY data signals. These signals are multiple-sampled at 1200 Hz and multiplexed into the TDDM data stream the same as CDP TTY signals. Internal interfaces are as shown in table 1-3.

(1) FSK Demodulator. The FSK demodulator combines a bipolar comparator with a monolithic phase-locked loop to recover TTY from the binary FM-ed carrier. The XR2211 phase-locked loop demodulator IC phase locks a self-contained Voltage Controlled Oscillator (VCO) to the FSK carrier frequency, the control voltage of which is filtered and sliced to recover the data.

The incoming FSK signal, ranging from +4 dBm to -30 dBm, is coupled through a surge arrestor to a low pass filter-attenuator. This filter reduces out-of-band noise and transients before the signal is center-sliced in a voltage comparator. A cutoff frequency of 100 kHz satisfies the input impedance requirement of 600 ohms ±10, -20 percent. The surge arrestor, low pass filter-attenuator, and voltage comparator are all balanced (to ground) to obtain $\geq$26 dB common mode rejection. Signals within the clamp limits of the surge arrestors (±8 volts) are scaled by the attenuator to be maintained within the operating range of the voltage comparator. The output of the comparator is also scaled and ac-coupled to interface with the phase-locked loop IC. The VCO used in the emitter-coupled multi-vibrator uses temperature-compensated current-source charging and discharging paths. Square waves and 900 phased linear triangular waves are simultaneously generated in the complex VCO structure. The VCO squarewave output drives the main phase detector in phase with the incoming carrier, as maintained by the phase detector error voltage.

The loop is set up as a second order type 1 loop. The loop bandwidth is about 350 Hz, and the damping is about 0.8. These parameters allow fast slewing capability of the loop with minimal bias distortion of the data up to 150 b/s without making the loop overly sensitive to noise. The noise performance of this asynchronous system can be improved by using a lower cutoff receive filter (the loop bandwidth is the receive filter), but with this, intersymbol interference and bias distortion increase.

FSK CHANNEL MODULE (20A3) BLOCK DIAGRAM



A second order low pass filter, external to the loop, is used to filter the control voltage for data extraction, thus providing good carrier rejection (the carrier amplitude is quite high and would produce jitter with only a single pole filter). This filter cutoff of 300 Hz is for carrier rejection since most of the noise filtering is done by the main loop filter.

The data filter output is sliced with an internally-referenced comparator with some hysteresis to remove any remaining carrier components. The sliced data is gated off the module with the channel select and transmit strobe inputs as shown. The data output (RDX on the block diagram) is an open collector gate. Gating logic is CMOS and LSTTL.

The phase-locked loop (PLL) contains a second phase comparator and additional circuitry which are used to detect an out-of-lock condition for a BITE signal. This signal is gated with a "no-carrier present" signal to inhibit a fault output when the FSK input is not present. The carrier detection circuitry is a rectifying level sensor with a threshold at -20 dBm. The absence of a carrier or an out-of-lock condition also inhibits data (produces a steady mark) to the demodulator output.

(2) FSK Modulator. The FSK modulator circuitry combines low-power SCHOTTKY and linear integrated circuits for an optimum speed-power balance. The data switched divider approach to FSK signal generation produces carrier frequency stability derived from a crystal-controlled timing source external to the FSK board. Operating the switched divider at a divide of 150 or 160 times the carrier rate and allowing the divider to only change ratio synchronous with the timing input assures phase coherency and very low jitter. Synchronous operation is accomplished by retiming the data with the 197.4125 kHz clock and wiring the programmable divider to only enable the preset inputs when the "end of count" pulse occurs.

The output of the programmable divider is then divided by ten in a Johnson decade counter. The divide ratios and clock frequency combine to produce a minimal-hardware divide chain with carrier frequencies less than 0.2 Hz from the nominal 1232.5 and 1317.5 Hz.

The Johnson Counter produces five phases at the nominal carrier frequencies simultaneously. Resistors tap the output stages to produce five weighted current sources which, along with a fixed current, are summed in an operational amplifier. This forms a low-cost sine wave generator with suitable output amplitude control and negligible frequency drift. The result is a sine-wave at mark or space frequency with a spectrum and wave shape. The complementary signal required to produce a balanced output is generated in an inverting, unity gain, operational amplifier. These two signals are resistively attenuated and further filtered before being transmitted to the surge arrestor and output connector. The FSK signals produced by this circuitry measure +1 dBm into 600 ohms with a high

TABLE 1-1. MODULAR PERFORMANCE

Item	Requirement
Frequency: Mark Space	1317.5 ±3 Hz 1232.5 ±3 Hz
Output Level	0.0 ±2 dBm (1)
Output Impedance	600 ohms +10 -20%
Mark-to-Space: Amplitude Variation	1 dB
Bias Distortion: Contribution of Modulator	(2)
Input Clock Requirement	197.4125 Hz ±.01% (2) Accepts duty factors from 10 to 90%

(1) Derived from TH-22 Input Level Requirement (-22 dBm) and 10 dB Cable Loss.

(2) System requirement is 20% Maximum Bias Distortion for total TDDM Link. Total Link distortion is 12.5% + Modulator Distortion for Demodulator Distortion less than 12.5%.

TABLE 1-2. DEMODULATOR PERFORMANCE

Item	Requirement
Allowable Input Carrier Frequencies: Mark Space	1317.5 ±3 Hz 1232.5 ±3 Hz
Input Impedance	600 +10 -20% from 1 kHz to 2 kHz
Longitudinal Balance	26 dB
Sensitivity: BITE Disconnected	-12 dBm (1)
Good Carrier Threshold	-20 dBm
Noise Performance	System operable over 5 miles of WF-16 and 1000 feet of CX 4566 S/N = 28 dB calculated in this mode.
Input Bias Distortion	5% Peak
Contribution of Demodulator (Distortion)	(2)

(1) Derived from TH-22 Output Level Specification and Cable Loss.

(2) System requirement is 20% Average Bias Distortion for total TD-1069 Link. Total Link distrotion is 12.5% + Modulator Distortion for Demodulator Distortion less than 12.5%.

TABLE 1-3. INTERNAL INTERFACES

INTERFACE	SYMBOL	TYPE	COMMENT
Inputs:			
Demodulator BITE Disable	$\overline{DBD}$	LSTTL	Allows testing of sensitivity
Receive Data Bus	WDR	LSTTL	Input to FSK modulator. Data sampled into FSK card on positive transition of CHS_n, when RSTROBE is high.
Receive Strobe	$\overline{STBR}$	LSTTL	Receive data timing bus, 32 kHz active low.
Transmit Strobe	$\overline{STBS}$	LSTTL	Transmit data timing bus, 32 kHz active low.
Channel Select	$\overline{CHS_n}$	LSTTL	One of twelve lines, 1200 Hz negative going pulse within RSTROBE and XSTROBE pulses, at mid-bit of WDR and RDX.
FSK Timing Bus	FSKT	LSTTL	Input port for 197.4125 kHz ±.01% pulse train.
LED Input	$\overline{LED\ CH_n}$	N/A	Requires 20 mA sink current.
Outputs:			
Transmit Data Bus	$\overline{RDX}$	O/C	Output of FSK demodulator. Active (on-line) when channel select and XSTROBE inputs are low. Presents steady mark if loop is out of lock or FSK input is below -20 dBm.

TABLE 1-3. INTERNAL INTERFACES (Continued)

INTERFACE	SYMBOL	TYPE	COMMENT
Outputs: (Continued)			
Channel Select Switch	CHS_nSW	N/A	Jumpered to CHS_n. Allows control to detect when no channel card is present.
FSK Bus	$\overline{FSK}$	o/c	Goes low when channel is polled to indicate presence of FSK card.
Channel Fail	CH_NF	LSTTL	BITE Summary of Board Faults. External equipment faults are inhibited. Active high.

side frequency (normal marking) of 1316.83 Hz ±0.2 Hz. The carrier exhibits about 5 percent THD, and the output level between mark and space is less than 0.5 dB. The mark-to-space and space-to-mark distortion contributed by the complete modulator-filter is less than 1 percent.

Preceding the FSK modulator is a latch which extracts data from the receive data bus (WDR) input port of the board. Data is sampled on the positive transition of receive strobe (STBR) when the channel select line is low.

The transmitted carrier is monitored with a full wave rectifying level detector with a threshold at -20 dBm. The output of the detector (MOD FAIL) is OR'd with the demodulator BITE signal and exits from the board as a summary alarm.

c. FSK Compatibility. When one TDDM unit has a FSK Data Channel module in one channel and another has a Digital Data Channel module in the same numbered channel, compatibility between the two units must be provided. Through the use of dummy stuffing, erroneous error conditions are prevented from occuring in the receive path of the Digital Data Channel Card.

By generating a dummy stuff request signal in the transmit side of the FSK Data Channel, at the appropriate rate, elastic store overflow conditions will not occur. The transmit side is that part of the data channel module which processes data from the channel side input to be multiplexed into the group transmit signal.

The highest rate that the NRZ TTY signal can be sampled by the FSK Channel module is as follows:

(1) 1200 Hz + 781.6 ppm + 30 ppm = 1200.974 Hz

Where 1200 Hz + 781.6 ppm is the minimal internal rate selected for a stuff only routine. The additional + 30 ppm allows for maximum internal oscillator offset.

At the receiving TDDM with a Digital Channel Module tracking the TTY signal, if the internal oscillator should be at a worst-case 30 ppm below nominal frequency, then the maximum rate that the digital phase-locked loop (PLL) can reach is:

(2) (307,233 Hz = 30 ppm) 256 = 1200.0929 Hz

The minimum required stuff rate, then, is:

(1) - (2) = 0.8811 Hz

A stuff rate of 0.926 Hz has been selected, and must now be analyzed for proper operation at the other worst-case combination of clock tolerances; i.e. when the transmit TDDM is 30 ppm low and the

receiving TDDM is 30 ppm high. The 1200 Hz sampling clock is then:

(3) 1200 Hz + (781.6 - 30) ppm = 1200.902 Hz.

At the receiving TDDM, the lowest rate that the digital PLL can track is:

(4) (307,167 Hz + 30 ppm) 256 = 1199.90709 Hz.

Comparing (3) and (4), and (3) - (4) = 0.99491 Hz.

The selected fixed stuff rate of 0.926 Hz for the FSK Data Channel Module will work for all combinations of oscillator tolerances at the transmit and receive ends. The overhead control channel format, for stuff/destuff command capability, allows for approximately three stuff commands per second for each internal 600 bps channel (or 6 stuffs per second for a 1200 bps data input). A fixed stuff rate of one per second is suited to the FSK Data Channel module.

1-13. OVERVOLTAGE ABSORBER (20A8)

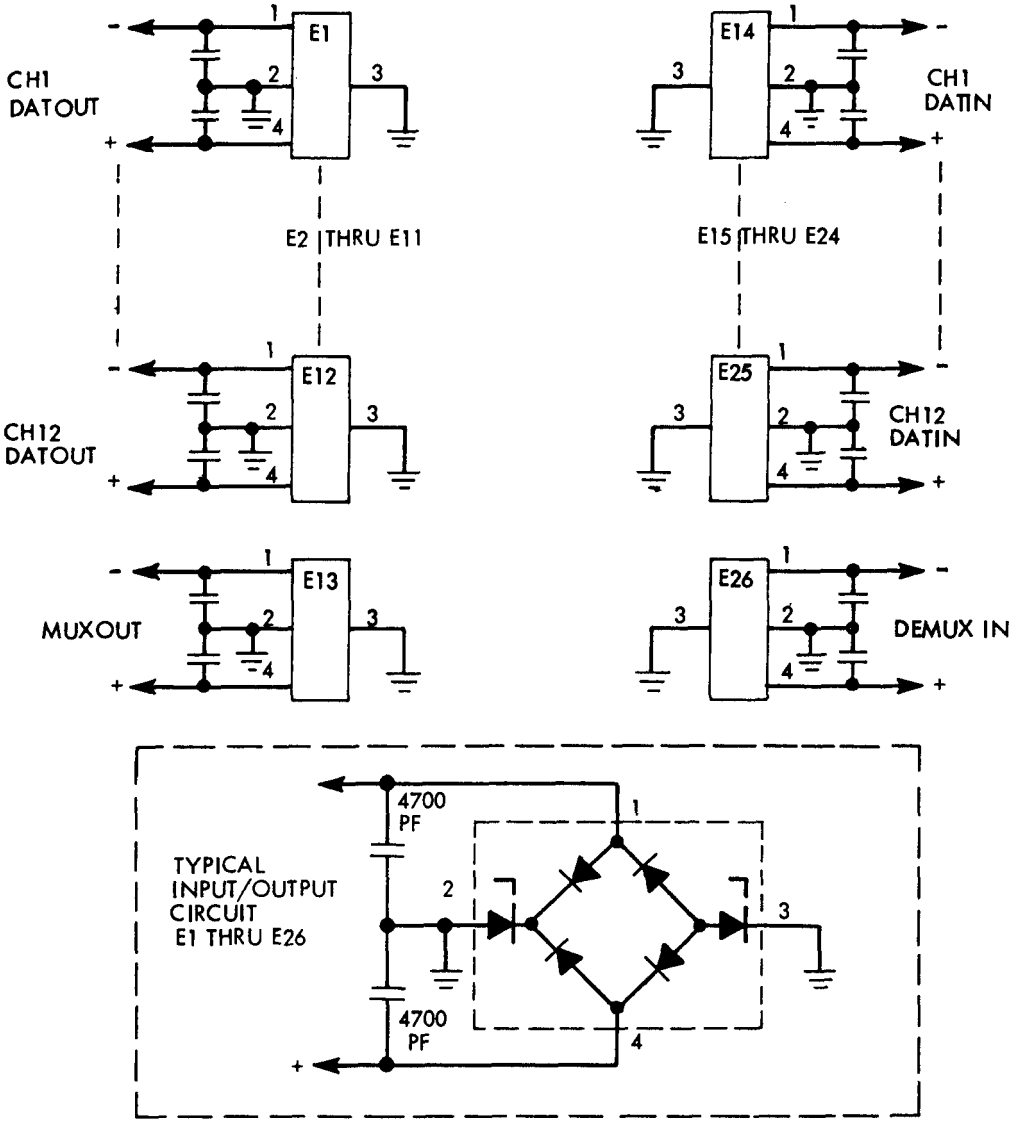
The Overvoltage Absorber module (20A8) provides input surge protection for all 12 channels and group MUX traffic. Fast-avalanche type bipolar diodes are used to shunt fast risetime surge currents to ground. The module also employs 4700 pF shunt capacitors (C1 through C52) from each line to ground for EMI/EMC emissions control. All channel and MUX/DEMUX pairs are routed from the chassis rear connectors to their location in the backplane, using shielded twisted pair cables, where they are bridged by transient suppressors. The Overvoltage Absorber module is captivated to prevent accidental removal. Removal and securing procedures for the Overvoltage Absorber module are described in TM 11-5805-638-12.

1-14. COMMON CONTROL (20A5/20A6)

The purpose of the Common Control is to derive timing from the Digital Clock Pulse Generator (DCPG) module (20A4) and provide signals to the 12 channel modules which will multiplex and demultiplex the 32 kHz group transmit and receive digital traffic. The Common Control performs functions which fall into the following five categories:

- Transmit Multiplexing
- Receive Demultiplexing
- Frame Synchronization
- Automatic Channel Assignment (ACA)
- Built-in Test Equipment (P-

OVERVOLTAGE ABSORBER MODULE (20A8)



The logic for the Common Control is contained on two printed wiring boards (PWB's): The Digital Controller (20A5) and The Alarm-Memory (20A6). The following block diagram illustrates the relationship of the functional blocks, of both modules, in a manner showing the overall control subsystem. The diagram indicates the functional partitioning on the two boards.

The Digital Controller module performs all of the Common Control functions. The Alarm-Memory module contains the control codes and random access memory (RAM) used by the Digital Controller. The logic for the BITE and alarm functions is contained in the Alarm-Memory module.

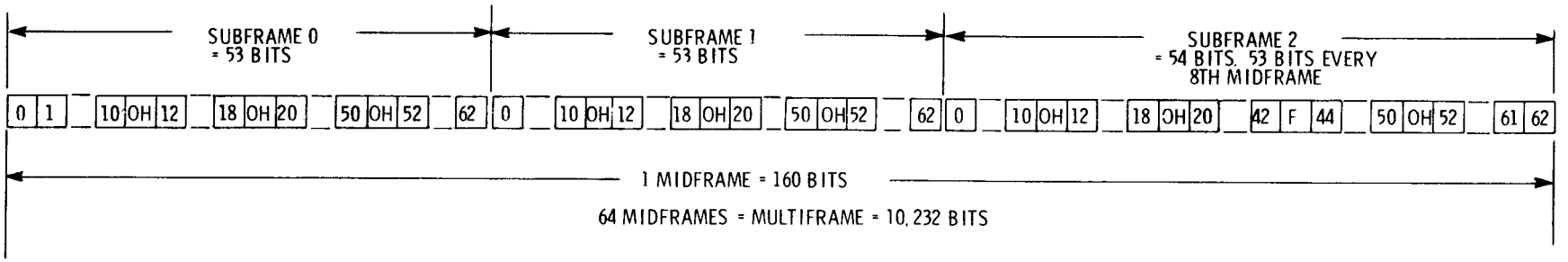
The Alarm Memory module provides a programmed digital sequencer which executes a series of instructions according to specific tasks to be performed. The heart of the digital sequencer is the Program Memory which supplies a series of digital codes to supporting logic elements. The logic elements are then able to execute algorithms in a manner which multiplexes and demultiplexes the 32 kHz digital group traffic. The Executive Routine of the digital sequencer performs a systematic acquisition of inputs in a polling sequence which determines the task to be performed at any given time.

The Common Control operates in three principal modes: 1) Power-up, 2) Normal, and 3) Automatic Channel Assignment (ACA). In the Power-up mode, the Common Control initializes those internal registers requiring known starting states or which might be adversely affected by a power interruption of 0.5 seconds or more. Once initialized, the ACA algorithm is performed. At this point the Normal mode is entered during which the transmit multiplex, receive demultiplex, frame synchronization and BITE operations are performed. In this mode the ALARM ACK/TEST pushbutton switch (front panel) may be operated as a lamp and audible alarm test without interfering with normal operation. When the operator wishes to make a channel rate change, the ASSIGN pushbutton is activated which begins the ACA mode (ACA algorithm performed). After this operation the Common Control returns to the Normal mode.

a. Transmit Multiplexing. The Common Control supplies strobes to 12 channel modules. This causes one of the 12 data sources to be gated onto a single open-collector group MUX bus. The group MUX bus is then accepted by the Common Control where overhead bits are inserted and the combined MUX stream is conditioned diphase (CDP) modulated before transmission.

A framing format is generated when the Common Control monitors the 32 kHz group transmit clock. The Common Control then logically decides which channel or overhead bit is to be gated into the MUX stream of any given time slot. The overhead format occupies fixed time slots in the framing format, and its purpose is to synchronize receive TDDM to the exact time slot and frame count of the transmit TDDM. It also identifies the absence or presence of a stuff bit.

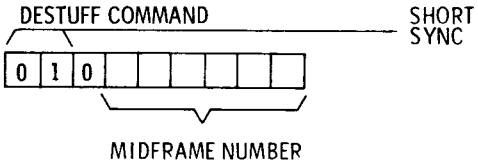
32.0 KB/S DATA FORMAT

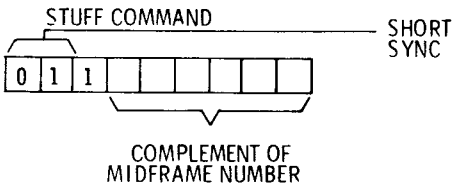


OH = OVERHEAD BIT-9 PER MIDFRAME
F = FILL BIT- THE FILL BIT OF EVERY 8TH 16TH 24TH 32ND 40TH 48TH 56TH & 64TH MIDFRAME IS MISSING

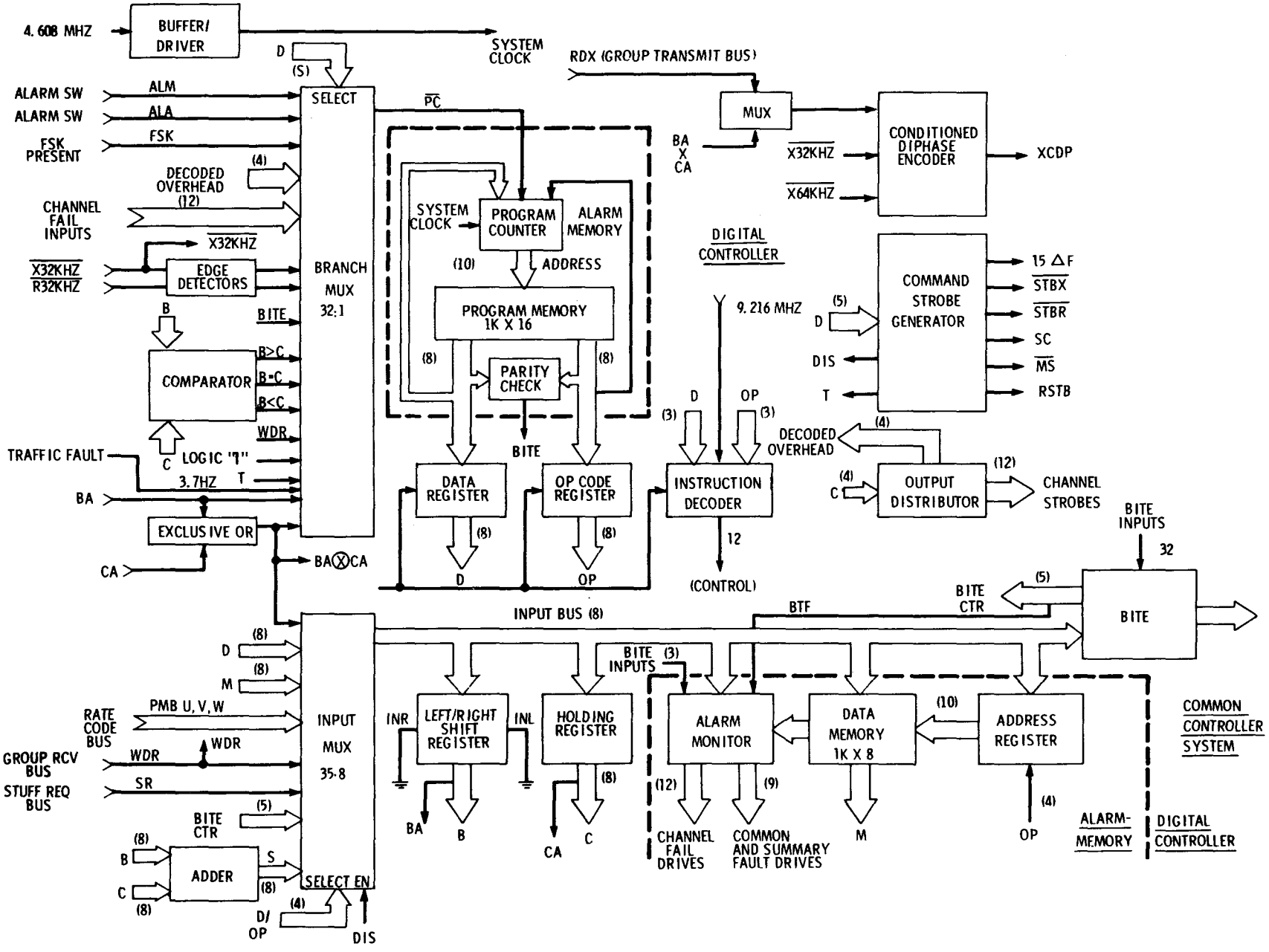
NOTE: TIME SLOTS 7, 15, 23, 27, 31, 39, 47, 55, 59 AND 63. ARE REMOVED FROM EVERY SUBFRAME. TIME SLOT 43 IS REMOVED FROM EVERY SUBFRAME 0 AND SUBFRAME 1.

OVERHEAD FORMAT





COMMON CONTROL (20A5 AND 20A6) FUNCTIONAL BLOCK DIAGRAM



Generation of the specified format implies maintenance of three binary counters: the six-bit Time Slot Counter (TSC), the two-bit Subframe Counter (SFC) and the six-bit Midframe Counter (MFC). Whenever the ACA algorithm is performed (para 1-14,d.).a four-bit Time Slot (TS) code is deposited into 192 consecutive memory locations (time slot file). The TSC/SFC refers to these locations in sequence as each edge of the 32 kHz transmit clock is sensed. The TSC/SFC is maintained by the transmit sequence in a single memory location and the MFC in a second location. Once the 32 kHz sensor is reset by the transmit sequence, the TSC/SFC is incremented and the view TSC/SFC number is used to access the time slot file. The resulting TS code directs the transmit sequence to a specific operation before generating the group strobe. The TS coding is as follows:

TS CODE		DEFINITION
MSB	LSB	RESET CODE
00	00	CHANNEL 1
00	01	
00	10	
00	11	
01	00	
01	01	
01	10	
01	11	
10	01	
10	10	
10	11	
11	00	CHANNEL 12
11	01	SKIP
11	10	FILL
11	11	OVERHEAD (OH)

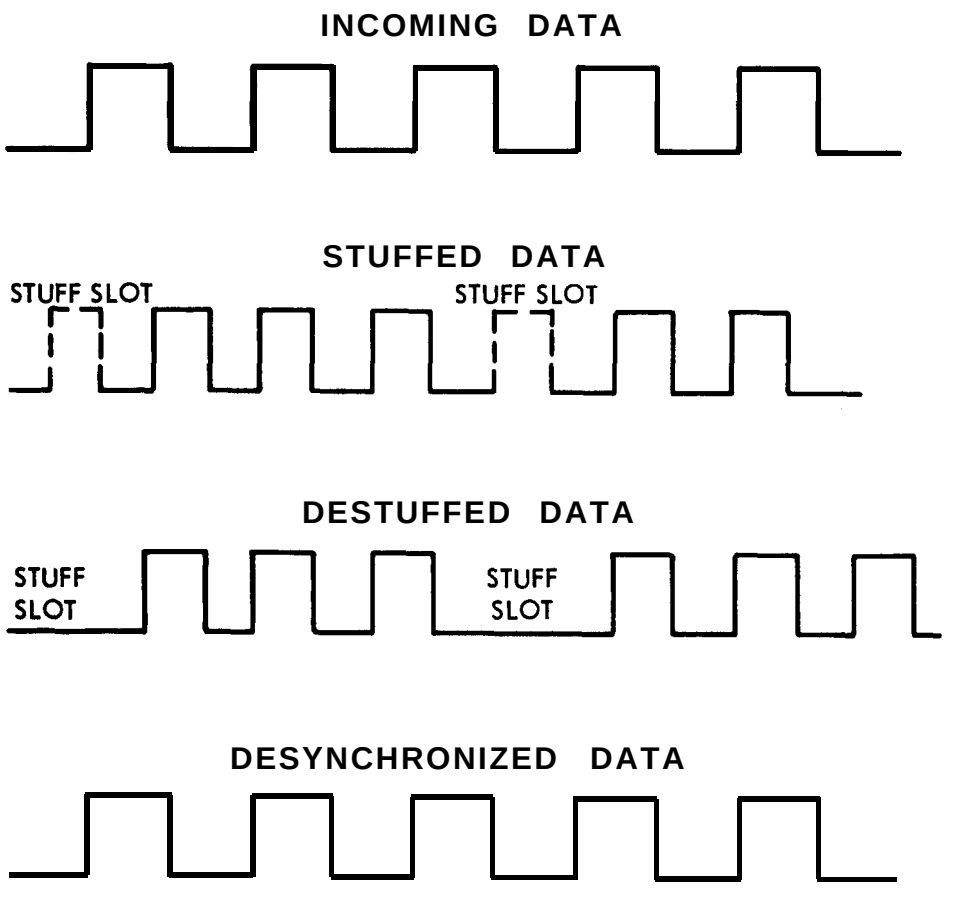
In general, the decode of the TSC/SFC counters will determine which source is to be gated onto the MUX stream for any given time slot. If channel data is to be gated, the Common Control generates a combination of two strobes (group strobe) to the channel cards. One strobe defines one discrete channel of the 12 possible channels. The second strobe identifies the strobe as being the transmit MUX function. When an overhead bit is to be generated, the channel strobes are automatically withheld.

The Common Control generates stuff commands to the individual channel modules. A stuff command is a control sent with the two previously mentioned strobes. It causes a channel to gate the same data generated during its prior channel time slot.

NOTE

Stuff bits are used to control the data transfer rate. To prevent the read clock from running past the write clock, the outputs are compared by a clock comparator (see page 1-25).

STUFFING MEANS THAT EXTRA TIME SLOTS ARE ADDED TO INCOMING BIT STREAMS (AS NEEDED) TO RAISE THEIR BIT RATES TO A FIXED MULTIPLEXING RATE. SINCE THESE TIME SLOTS CONTAIN NO INFORMATION, THEY MUST BE REMOVED (DESTUFFED) AFTER THE SIGNALS ARE SEPARATED (DEMULTIPLEXED).



A PHASE-LOCKED LOOP RESTORES THE DATA (DESYNCHRONIZES) TO ITS ORIGINAL STATE AFTER STUFFED SLOTS HAVE BEEN REMOVED.

The stuff command is sent to bring about a stuff request on the single open-collector Stuff Request Bus. It is gated onto the bus by a channel module, during one of its allocated time slots, indicating that the channel elastic storage is about to become empty.

The Common Control generates the overhead (OH) format in a specific manner so that the stuff bit is recognized at a remote receive TDDM. When the MFC equals TSC for the requesting channel, the six bits of the MFC are sent (in complement form) in the long sync code overhead format. Also, the control bit of the overhead format is sent as a logic 1. Together with the generation of a stuff command, in the next midframe, the resulting stuff bit is transmitted. Restuffing at the remote end is then a matter of: 1) determining when the received MFC in the overhead format appears in complemented form, and 2) withholding the appropriate timing strobe during the following midframe.

The overhead channel occupies time slots 11, 19, and 51 (see page 1-21) of the subframe. Channel allocations of the data format are based on the coding of channels and time slots. Channel numbers 0 through 49 are available for assignment to the 24 ports. Channels 50, 51 and 52 are permanently assigned to the overhead channel. Channels 54 through 63 are not used (see page 1-29). Channel 53 is used about every third midframe to obtain division of the 32 kb/s total data rate to the desired channel data rate. Channel numbers are made to correspond to time slot numbers. By representing the numbers in binary and reversing them so that the most significant bit (MSB) of a channel number is also the least significant bit (LSB) of the corresponding time slot number. The time slot numbers refer to the sequence by which the time slots are assigned.

There are three subframes per midframe, and 64 midframes per multiframe (0 through 63). The third subframe in each midframe has 54 bit periods (except for 31 and 63). The other subframes have 53 bit periods. Subframe lengths are varied by skipping time slot 43 as required. This adjusts the data rate of each channel to 600.46896 b/s. To eliminate a fourth subframe, the last location of the third subframe contains a reset code which causes the TSC/SFC to reset.

If a channel data bit is to be generated, the Common Control supplies a transmit strobe from the Command Strobe Generator and one of 12 discrete channel strobes from the Output Distributor. The applicable channel card then gates its data onto the external open collector group transmit bus (RDX). If an overhead data bit is to be generated, the appropriate bit is obtained internally within the Common Control. RDX data and overhead (OH) data are then multiplexed together and applied to the Conditioned Diphase Modulator prior to transmission (see block diagram).

b. Receive Demultiplexing. Receive demultiplexing is the reverse process of transmit multiplexing and requires that the destination of data from the 32 kHz group DEMUX data stream be determined for

each time slot. In order to do this the Common Control performs frame synchronization, a process which aligns the local timing counters (TSC, SFC, and MFC) according to the received overhead format within the DEMUX data stream. Once frame synchronization has been achieved, the Common Control decodes the TSC/SFC for each period of the 32 kHz group receive clock and provides a combination of two strobes to the channel modules (20A2, 20A3). The first strobe defines one discrete channel of the 12 possible channels. The second strobe identifies the strobe as being the receive function. When an overhead bit time occurs, the channel strobes are automatically withheld.

Destuff commands are used for the receive function. The destuff operation is accomplished by withholding the previously mentioned two strobes, which causes the stuffed bit to be ignored by the appropriate channel module. Restuffing occurs during the midframe following the one in which the six bits of the MFC of the overhead format (LONG SYNC CODE) are received in complement form.

The receive sequence is entered each time a new edge of the 32 kHz receive clock is sensed. Receive processing includes frame synchronization which consists of aligning the local TSC, SFC and MFC, according to the sync format received from the DEMUX data stream. Time slot codes, which direct data to the appropriate channels, are generated by accessing the data memory. The distinction between the Transmit and Receive access is separate time slot and subframe counters. The TSC/SFC is incremented for each 32 kHz receive clock in the same manner as in the Transmit Function.

The operating program of the digital sequencer monitors each transition of the 32 kHz group-receive clock and determines which channel data bit or overhead data bit was received from the demodulated group DEMUX traffic (WDR) by accessing the data memory. If a channel data bit is received, the operating program supplies a receive strobe from the Command Strobe Generator and one of 12 discrete channel strobes from the Output Distributor. The appropriate channel module then gates data from the WDR bus into its receive elastic store. If an overhead bit was received, the operating program will store the information for synchronization and control purposes.

c. Frame Synchronization. Frame synchronization is the process of aligning the local framing generation to the data format generated at a remote TDDM and is accomplished in the Common Control by searching for the SHORT SYNC CODE. The short sync code is comprised of a "0" and "1" in time slots 11 and 19 respectively of subframe 0. Time slot 51 is the stuff/destuff control bit. When this bit is "0", no stuffing is indicated and the true form of the MFC is present as the long sync code in bits 11, 19, and 51 of subframes 1 and 2. When stuffing is indicated by a logic 1 in the stuff/destuff control bit, the midframe number is presented in complemented form in the long sync code. The six-bit midframe number proceeds in straight binary fashion to synchronize the local MFC.

Frame synchronization and bit count integrity are accomplished within 300 msec 90 percent of the time following the application of a signal to the DEMUX input.

d. Automatic Channel Assignment (ACA). Automatic Channel Assignment (ACA) is a method of allocating time slots, for a time division multiplexer, to evenly distribute sampling of any particular channel. The benefit of even distribution is that format jitter and elastic storage are minimized at the channel level.

The ACA algorithm, as it applies to the Common Control, is performed in the following manner under power-up or an operator-initiated rate change.

1) Three-bit rate code for each channel is acquired by strobing each of the 12 thumbwheels, one at a time.

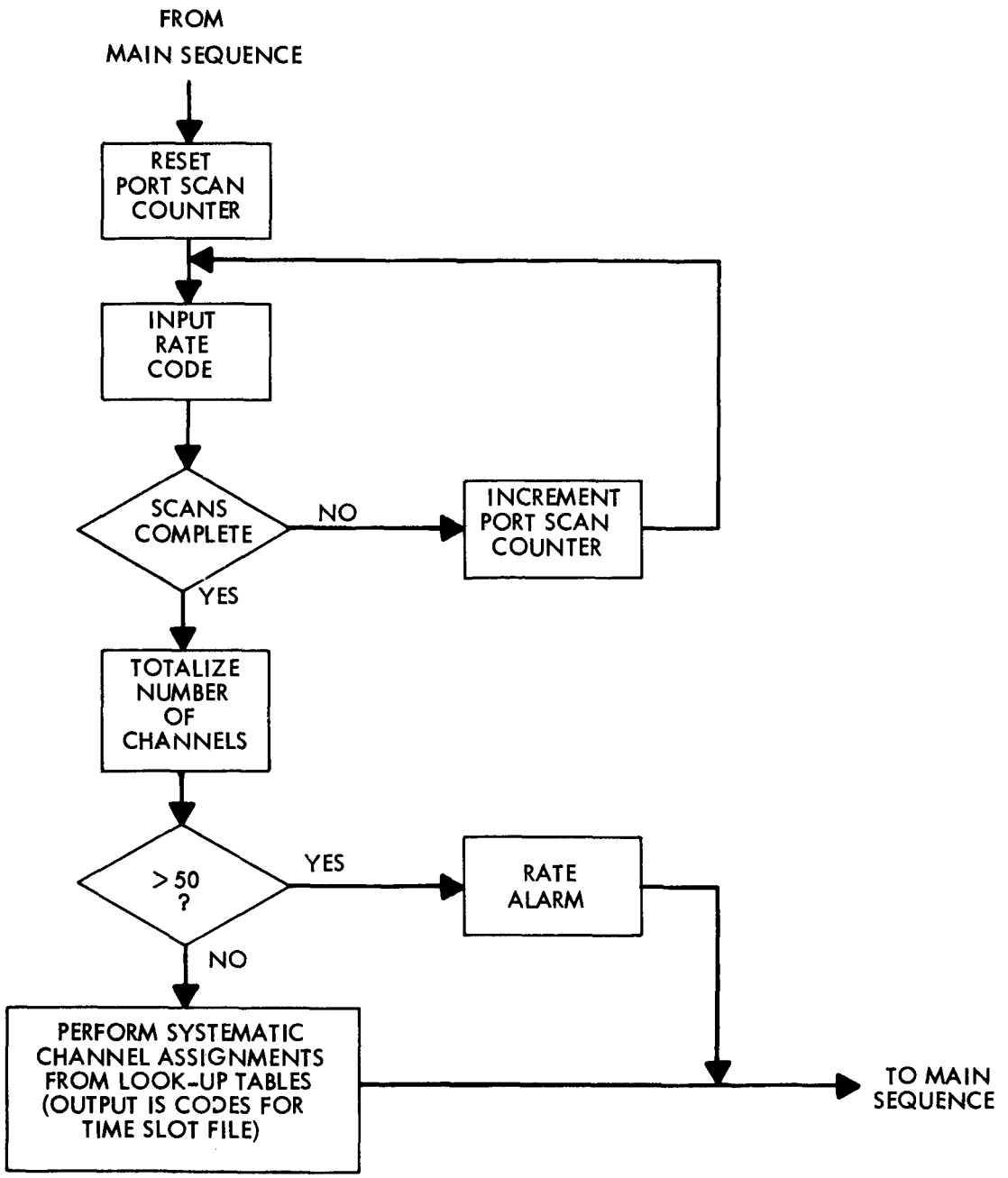
2) Channels are systematically sorted and assigned, according to data rate, with the highest rates being assigned first. In the case of the 9.6 kbps channel, the 16 time slot numbers are obtained by reversing the bit significance of binary numbers 0 through 15. The Time Slot Chart shows that the appropriate time slot numbers are: 0, 32, 16, 48, 8, 40, 24, 56, 4, 36, 20, 52, 12, 44, 28 and 60. If the next channel was also a 9.6 kbps rate, the binary numbers 16 through 31 would be reversed. If the next channel were a 4.8 kbps rate, 8 positions would be required and the binary numbers 16 through 23 would be reversed. This process is continued until the time slots for all 12 channels are assigned.

3) A maximum of 50 positions are available for channel time slot allocations (see Time Slot Chart). If the accumulated channel rates cause assignments in excess of the 50 positions, the rate budget of 30 kbps has been exceeded and the Common Control alerts the operator by lighting the RATE ALARM lamp. In this case all the slots are unassigned.

The ACA sequence is entered either upon activating the ASSIGN pushbutton or during power turn-on.

The ACA sequence causes all 12 channel thumbwheel switches to be scanned and then read through the input MUX. The acquired rates are first examined to determine whether or not the aggregate data rate programmed on the thumbwheel switches exceeds the budget of 30 kbps. If the budget is exceeded, the channel programming is inhibited and the RATE alarm is activated; if not, systematic channel assignments are made and codes for each time slot are deposited into the memory.

ACA SEQUENCE BLOCK DIAGRAM



TIME SLOT CHART

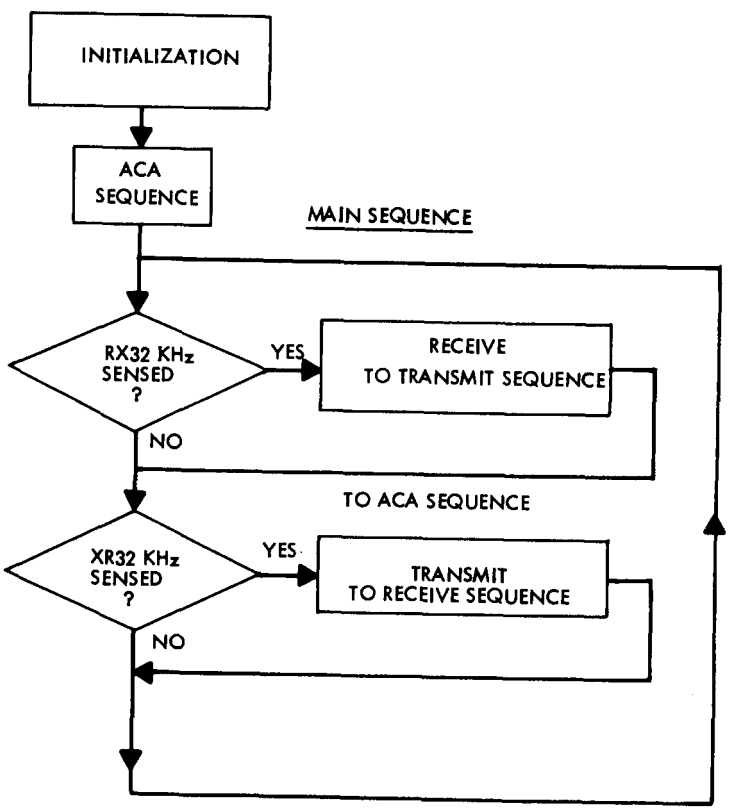
TIME SLOT LSB MSB / POSITION NUMBER MSB LSB ABCDEF	POSITION NUMBER	TIME SLOT NUMBER	
000000	0	0	AVAILABLE FOR DATA
000001	1	32	
000010	2	16	
000011	3	48	
000100	4	8	
000101	5	40	
000110	6	24	
000111	7	56	
001000	8	4	
001001	9	36	
001010	10	20	
001011	11	52	
001100	12	12	
001101	13	44	
001110	14	28	
001111	15	60	
010000	16	2	
010001	17	34	
010010	18	18	
010011	19	50	
010100	20	10	
010101	21	42	
010110	22	26	
010111	23	58	
011000	24	6	
011001	25	38	
011010	26	22	
011011	27	54	
011100	28	14	
011101	29	46	
011110	30	30	
011111	31	62	
100000	32	1	
100001	33	33	
100010	34	17	
100011	35	49	
100100	36	9	
100101	37	41	
100110	38	25	
100111	39	57	
101000	40	5	
101001	41	37	
101010	42	21	
101011	43	53	
101100	44	13	
101101	45	45	
101110	46	29	
101111	47	61	
110000	48	3	
110001	49	35	
110010	50	19	OVERHEAD (3)
110011	51	51	
110100	52	11	
110101	53	43	SPARE-1/3 NOT USED-2/3
110110	54	27	NOT USED (10)
110111	55	59	
111000	56	7	
111001	57	39	
111010	58	23	
111011	59	55	
111100	60	15	
111101	61	47	
111110	62	31	
111111	63	63	

The ACA algorithm incorporates the following requirements:

- Assignments are not made for any channel programmed to OFF position.
- Removed channel module automatically programmed OFF.
- Proper assignment occurs with up to 11 modules removed.
- TTY subscribers with transmission speeds up to 150 bps assigned a 1200 bps channel rate on MUX data stream.
- For FSK module, dialed rates other than OFF or TTY are not assignable and RATE indicator will flash.

e. Built-in Test Equipment (BITE). The TDDM uses Built-in Test Equipment (BITE) to monitor system/module failures. The Common Control circuitry governs the BITE function of the TDDM. For a detailed description see paragraph 1-17.

f. Executive Routine. At power up, the Executive Routine initializes those memory registers requiring known starting states and then causes the ACA sequence to be entered. At the end of the ACA sequence the normal polling sequence is entered. The transmit and receive sensors are tested for logical true condition. When either sensor is true, the respective-sequence (transmit or receive) is entered.



1-15. DIGITAL CLOCK PULSE GENERATOR (20A4)

The Digital Clock Pulse Generator (DCPG) module is one of three common boards. The DCPG module performs all TDDM timing functions and contains the group input and output interface circuits. Additional functions performed are as follows:

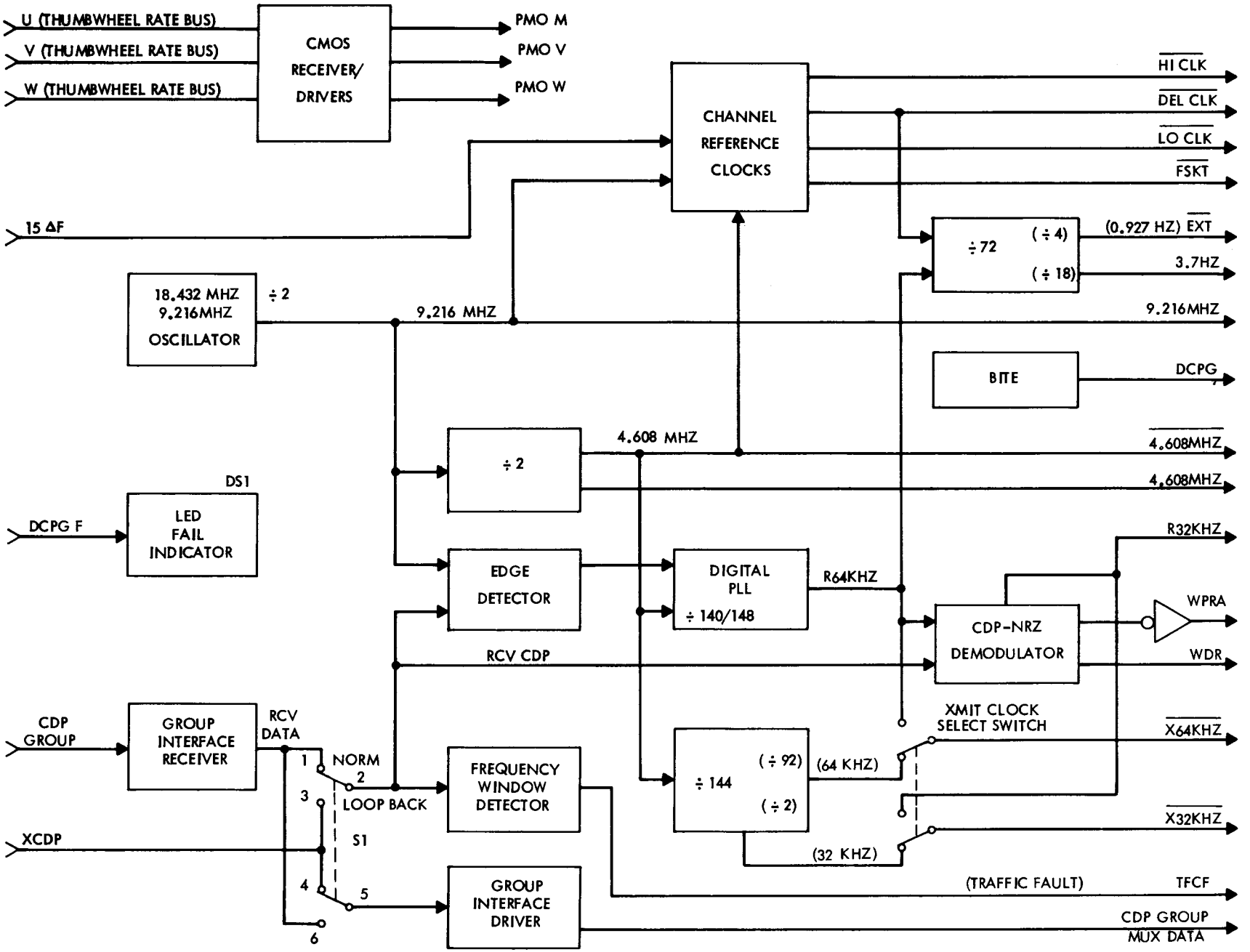
- Generates 10 clock frequencies from 0.927 Hz to 9.216 MHz from a crystal source.
- Regenerates 64 kHz and 32 kHz clocks from a conditioned diphase (CDP) source at 32 kbps. Regeneration is done with a digital phase-locked loop (PLL).
- Demodulates a conditioned diphase signal into NRZ, 32 kbps.
- Interfaces 32 kbps conditioned diphase data from LSTTL levels to a balanced line, and vice versa.
- Provides traffic fault and BITE outputs.

a. 9.216 MHz Oscillator. A 9.216 MHz master clock is generated, by the oscillator, by dividing a 18.432 MHz by 2 (within the oscillator module). The 9.216 MHz is further divided by 2 to produce 4.608 MHz.

b. Edge Detector and Digital PLL. The edge detector detects changes in receive conditioned diphase (RCDP) and operates as a phase comparator for the digital phase-locked loop (PLL). The detector's output sets the divide ratio of a programmable counter to either 140 or 148. This offsets the R64 kHz frequency to maintain proper phase between RCDP and R64 kHz. The R32 kHz output is provided by dividing R64 kHz by 2.

c. Channel Reference Clocks. The Channel Reference Clocks generate timing signals HICLK, LOCLK, DELCLK and FSK timing (FSKT). The HICLK signal is generated by dividing the 9.216 MHz clock by 15 (except by 14 every 1/500.4 seconds). An external signal (15 f) sets a latch every 1/500.4 seconds. A HI latch eventually reaches the counter presets changing the divide ratio to 14. The LOCLK operation is similar except that the preset is changed to 16 every 1/500.4 seconds. DELCLK is obtained by phase comparing HICLK and LOCLK; the frequency difference equals DELCLK. The FSK timing (197.398) is derived from the 9.216 MHz by counters. Transmit clocks are obtained either from the 4.608 MHz (divide by 144) or from R64 MHz and R32 kHz depending on the setting of the timing select switch. The 3.7 Hz and 0.927 Hz (EXT) signals are generated by dividing DELCLK (66.72 Hz) by 18 and then by 4.

DIGITAL CLOCK PULSE GENERATOR (20A4) BLOCK DIAGRAM



d. CDP Demodulator. The conditioned diphase demodulator processes RCDP into NRZ format using the regenerated R64 kHz for timing. The demodulated data is designated WDR and is output from the board.

NRZ DATA

CONDITIONED DIPHASE DATA

e. Group Interface Circuit. The Group Interface Circuit is used in conjunction with the loopback switch and Bite circuit.

(1) Group Interface Driver. Logic gates of the Group Interface Driver generate a positive and complemented signal which, in turn, produces a balanced signal. Output signals of the gates are rail-to-rail, within 30 mV. The absolute level reference is the 5V power supply ±5 percent.

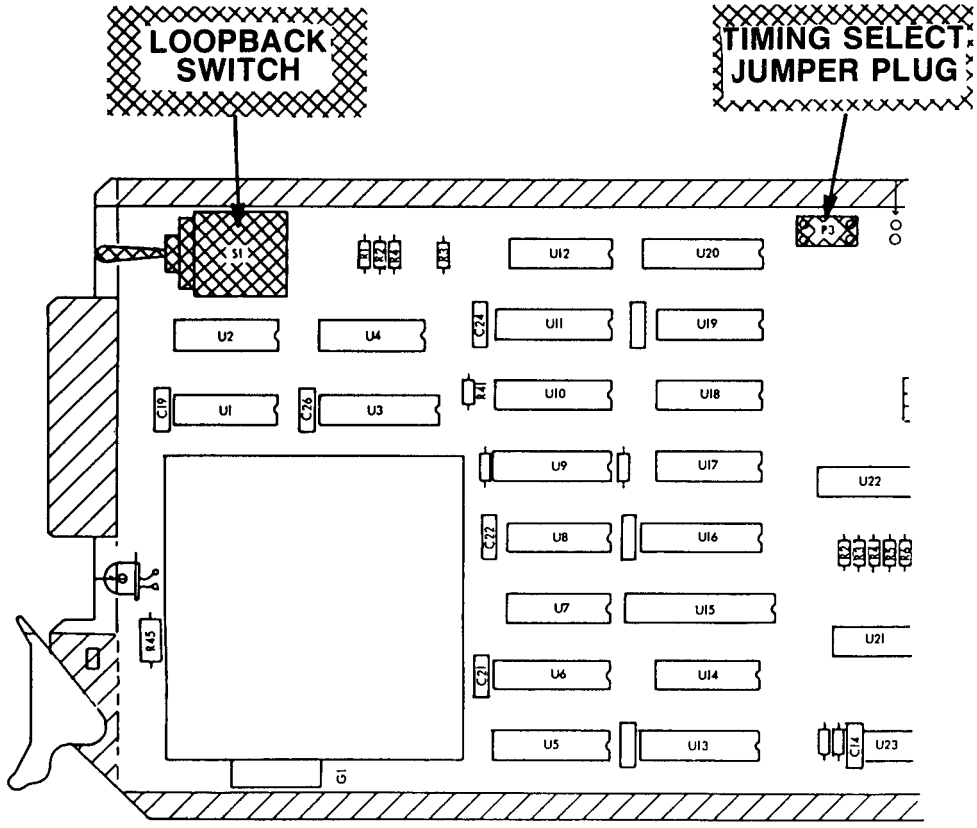
(2) Group Interface Receiver. The Group Receiver has a 40 dB longitudinal balance requirement. The input amplifier operates linearly as a balanced to unbalanced converter with a cutoff frequency of 120 kHz. A single-ended equalizer is used eliminating any 1% capacitors.

f. Loopback Switch. A two-position loopback switch is provided on the DCPG module which, when set to ON (up), provides the following functions:

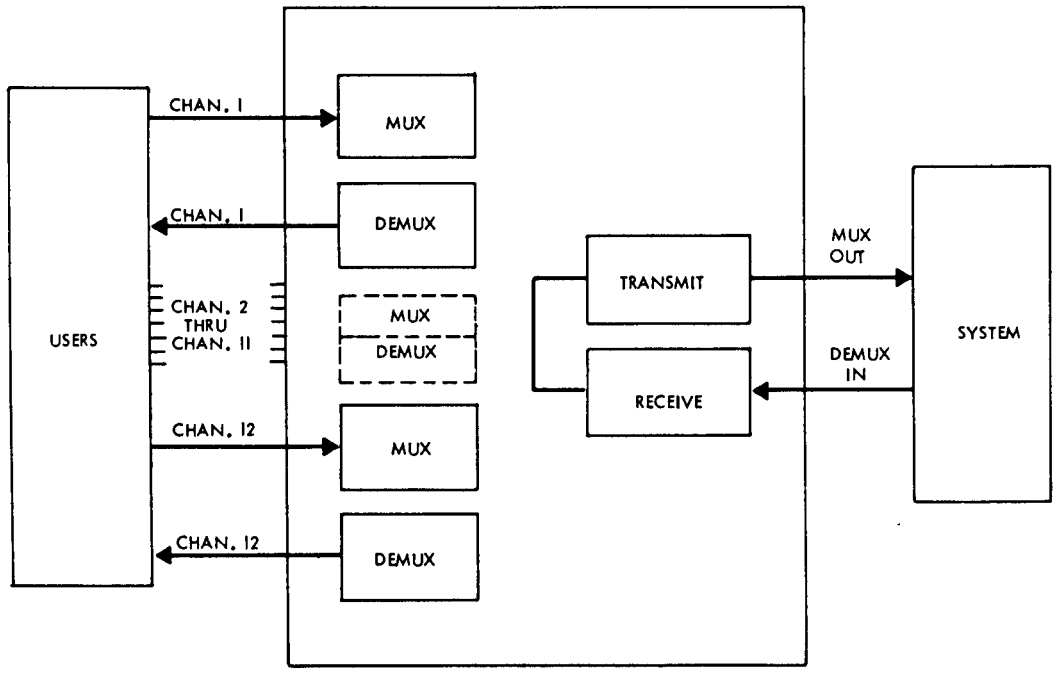
- Loops the CDP group DEMUX data to the CDP group MUX data.
- Loops the transmit CDP signal to the Write Data Receive (WDR) Bus after demodulating.

g. Transmit Clock Selection. Transmit timing can either be generated internally from the crystal oscillator or derived from the group DEMUX data. A two-position jumper plug is provided on the DCPG for this reason. The plug positions are labeled “INT” (internal) and and “REC” (received).

h. BITE Circuit. The BITE circuit operates by monitoring seven critical points on the DCPG for activity. This is done by an 8 x 1 multiplexer and a counter. The counter-is shifted by activity on the multiplexer output, changing the multiplexer address.



LOOPBACK MODE



1-16. POWER SUPPLY (20A1) BLOCK DIAGRAM DESCRIPTION

There are no complex mechanical assemblies in the TDDM Power supply. The power supply circuitry consists of a 1 ampere circuit breaker (CB1), filters (FL1 and FL2), thermal switch (S1), power indicators (DS1 & DS2), and transformer and regulator circuits. The 115 Vac input is filtered and applied to the primary of the transformer through the circuit breaker (CB1) and thermal switch (S1). Input ac voltage is indicated by the POWER lamp (DS1). Output dc voltage is indicated by the DC OUTPUT indicator (DS2). A detailed functional block diagram for the TDDM power supply is shown on the following page. Schematics are provided in the back of this manual (see FO-1 and FO-2).

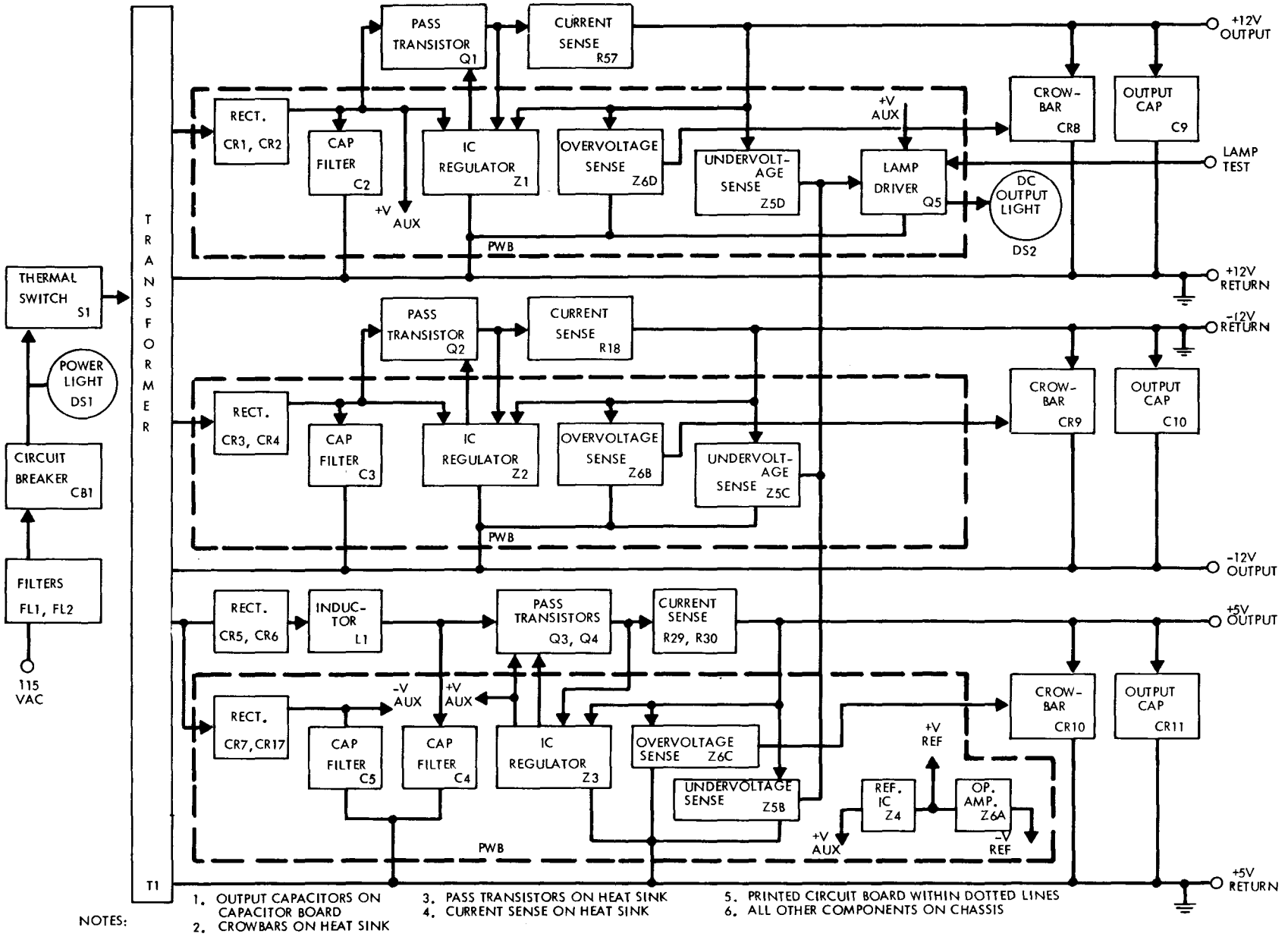
a. Voltage Regulation. The TDDM Power Supply provides dc operating voltages to the chassis and modules. Voltage regulation is accomplished by controlling the current flow to the primary of transformer T1. The Power Supply converts the input 115 Vac into three regulated dc voltages: +12 V, -12 V, +5 V. These three dc voltages are used to operate the Control, Timing and Data modules, and the Switch Assembly.

b. Dc Outputs. There are three secondary windings on the transformer. The +12 V secondary provides low voltage (27 Vat) which is fullwave rectified by CR1 and CR2 and filtered by capacitor C2. The resulting unregulated +20 Vdc is used as the positive auxiliary voltage and is applied through the pass transistor (Q1) which controls the current through it to maintain a constant +12 V output. This +12 V output is passed through a current sense resistor (R57) and is then filtered by the output capacitor (C9) before going to the P1 output pins. The IC regulator (21) uses the +12 V as a means of controlling and regulating the output. The overvoltage sense (Z6D) uses the +12 V to cause crowbar (CR8) to turn on if the output goes too high. The undervoltage sense (Z5D) uses it to turn off the lamp driver (Q5) which turns off the dc output light (DS2) should the output go too low.

The -12 V regulator circuit is identical to the +12 V circuit except for the following:

- The positive output line is grounded and the negative line is the output (-12 V).
- The divider resistors R49, R51, R48 and R50 are reversed due to the negative voltage.
- CR15 is changed to a 12 V zener. It is referenced to the negative 12 V output instead of ground.

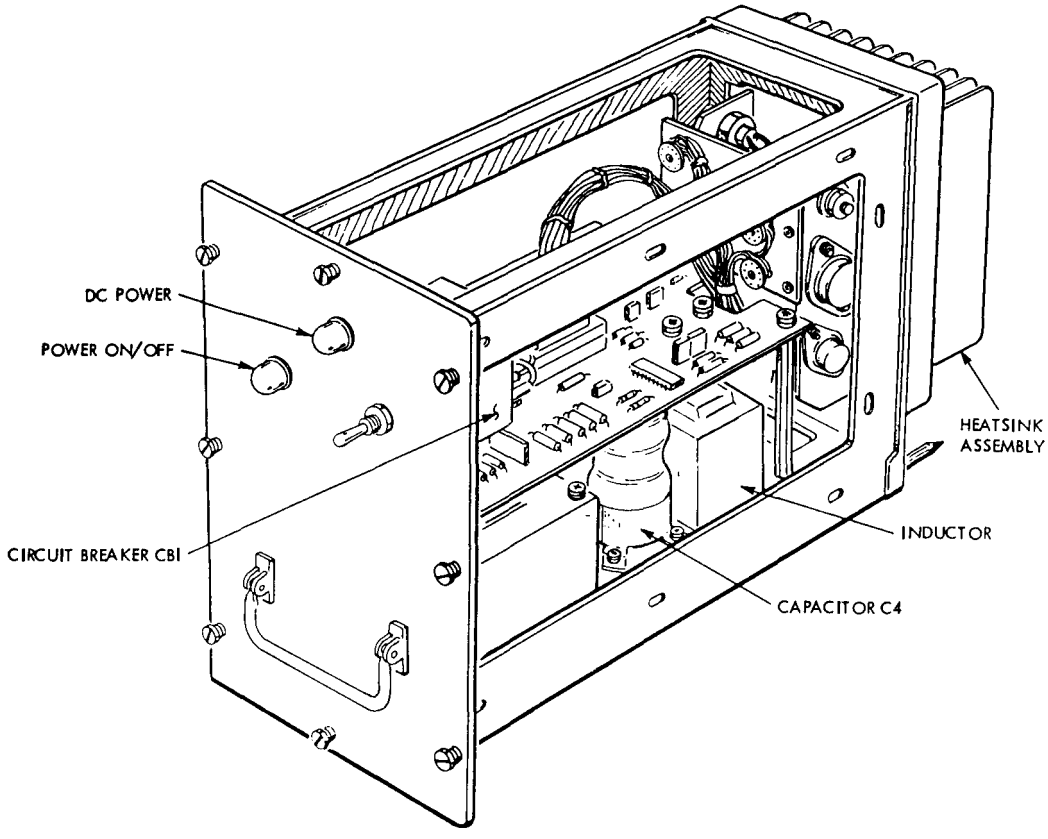
POWER SUPPLY FUNCTIONAL BLOCK DIAGRAM (20A1)



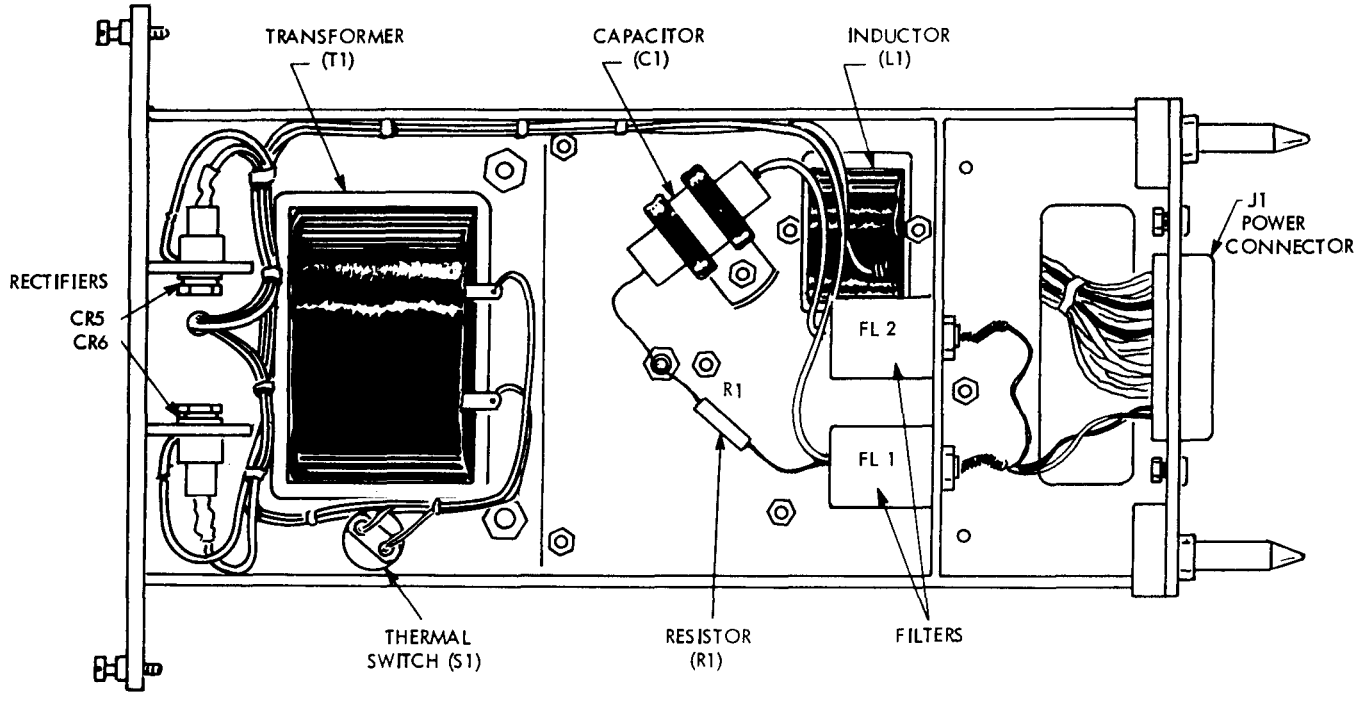
NOTES:

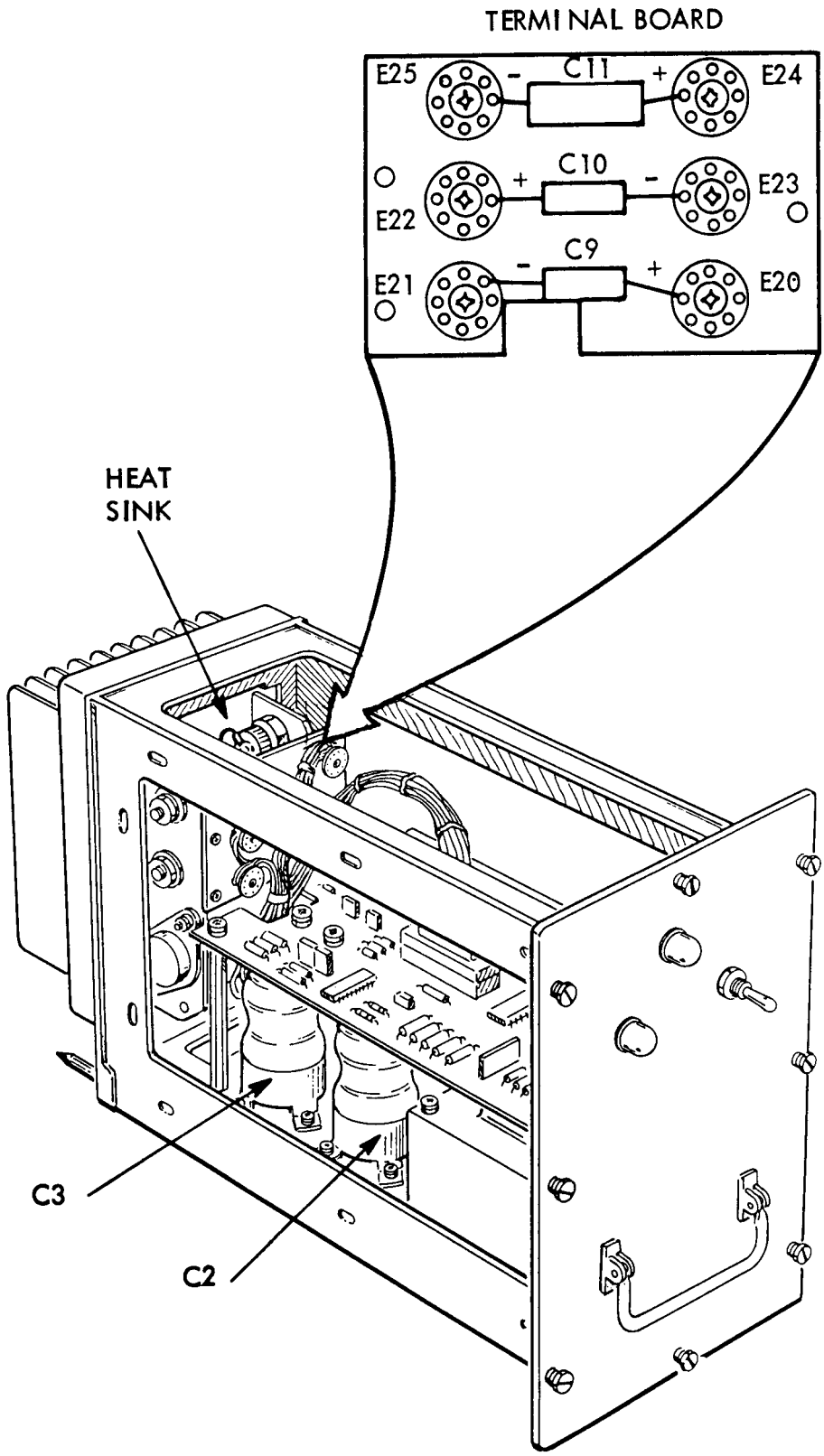
1. OUTPUT CAPACITORS ON CAPACITOR BOARD
2. CROWBARS ON HEAT SINK
3. PASS TRANSISTORS ON HEAT SINK
4. CURRENT SENSE ON HEAT SINK
5. PRINTED CIRCUIT BOARD WITHIN DOTTED LINES
6. ALL OTHER COMPONENTS ON CHASSIS

POWER SUPPLY (RIGHT SIDE) OPEN



POWER SUPPLY (BOTTOM VIEW)




TERMINAL BOARD
E25
C11
E24
E22
C10
E23
E21
C9
E20
HEAT SINK
C3
C2

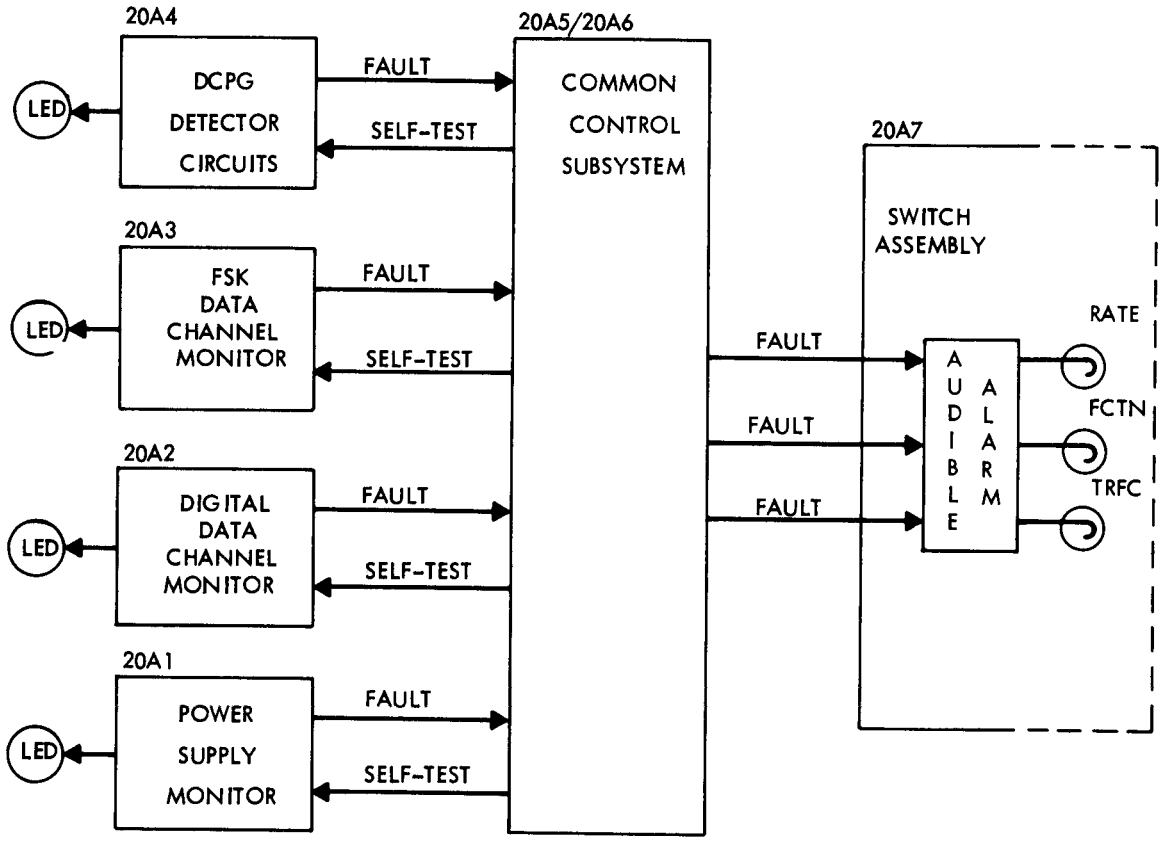
The +5 V regulator circuit uses the third secondary output. Here the low voltage output is rectified by CR5 and CR6 and filtered by inductor L1 and capacitor C4 to approximately +7 Vdc. This filtered, unregulated dc voltage is applied through a transient protecting inductor to the pass transistor (Q3) collector which controls the current to maintain a constant +5 V output voltage. The current from the Q3 emitter passes through the parallel current sense resistors (R29, R30) to the output capacitor (C11) and to the P1 output pins. The +5 V regulator circuit uses voltage from +V_{AUX} for power since it is higher than the +5 V unregulated dc. To provide the negative auxiliary voltage (-V_{AUX}), the +5 V secondary is applied to rectifiers CR7 and CR17 and capacitor filter C5. As with the +12 V secondary, the +5 V secondary uses overvoltage and undervoltage circuits for protection against too high or too low outputs.

1-17. BUILT-IN TEST EQUIPMENT (BITE) DESCRIPTION

The TDDM uses Built-in Test Equipment (BITE) to indicate system and/or module failure. The BITE indicators consist of the Functional (FCTN), Traffic (TRFC) and Rate Overload (RATE) lamps, and an audible alarm. Additional, each module has a fault lamp (LED) that lights red to indicate a failure on the module. The digital nature of the equipment demands the use of monitors to make go-no-go decisions as to the operating condition of that portion of the circuit being monitored. These monitors are provided along the traffic signal path of the TDDM and are used to check for external loss of traffic signals and internal circuit failures. The Common Control circuitry governs the BITE function of the TDDM (see para 1-14 Common Control).

a. Traffic Failure Operation. The receive data signal is monitored by the receive traffic monitor circuit. The output signal of the monitor circuit is applied to the fault summary logic through a delay circuit to prevent false alarms from a momentary fault condition. When a traffic failure occurs, the TRFC lamp lights and the audible alarm sounds. Pressing the ALARM ACK/TEST pushbutton sends a signal to the fault summary logic which silences the audible alarm (the TRFC lamp remains lighted). When the traffic signal is restored, the audible alarm sounds again and the ALARM ACK/TEST pushbutton must be pressed again to silence it. The fault summary logic interlocks traffic and functional failure signal logic processing so only the TRFC lamp lights if both traffic and functional failures occur at the same time.

BITE FUNCTIONAL BLOCK DIAGRAM



b. Functional Fault Operation. The BITE circuitry on the Digital Data Channel (20A2) FSK Data Channel (20A3) Digital Clock Pulse Generator (20A4) modules, and the power supply provides a self-monitoring capability.

When a fault is detected, a fault signal is sent to the Common Control Subsystem (20A5/20A6). The Common Control then performs a self-test to assure that a fault exists in the module providing the fault signal. If a fault does exist, an error signal is sent by the Common Control to the LED on the faulty module. The error signal lights the appropriate LED, sets off the audible alarm and lights the ALARMS indicator(s). There is a two-second delay introduced between fault detection and alarm activation to avoid false alarms caused by momentary failures.

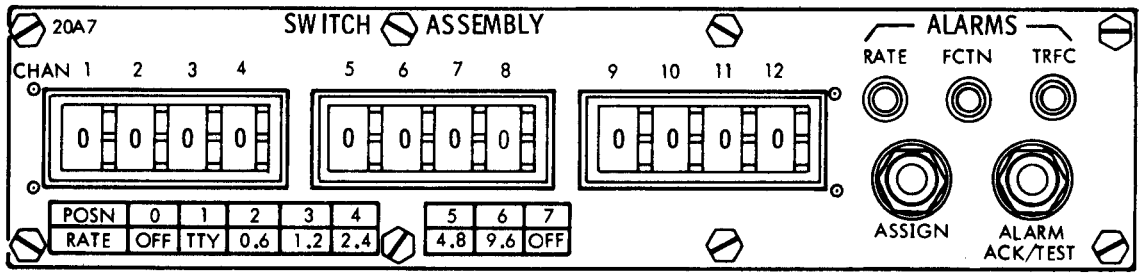
When an error condition is corrected, the Common Control automatically causes all indications and drive signals to return to a normal state.

c. Reset Function. When a functional failure occurs, the FCTN lamp lights and the audible alarm sounds. pressing the ALARM ACK/TEST pushbutton silences the audible alarm (the FCTN lamp remains lit). Pressing the ALARM ACK/TEST button again then steps all counters associated with 1st-level activity scanners, so the counter that stopped is stepped to the next input. It then cycles normal and will stop again when the scan cycle returns to the failed signal; it will stop sooner at another point if two faults exist. The audible alarm sounds again and can be silenced by pressing the ALARM ACK/TEST pushbutton. The FCTN lamp remains lighted until the fault is corrected because the functional failure indication is stored in the Memory Alarm (20A6) module. This capability of restarting a stopped activity detector allows a more thorough and positive check of symptoms by allowing the operator to determine whether more than one signal failed or whether the first failure indication was a result of the failure of another signal.

In some instances, several modules not having functional faults may give a fault indication as a result of a fault on one module. When this occurs, the reset function provides the means of determining which module is the real source of the failure. Pressing the ALARM ACK/TEST pushbutton, after the fault alarm sounds, silences the alarm; pressing it again restarts the fault scan cycle. If only one module is involved in the failure: upon restart, the fault scan cycle will continue until it returns to the failed module and it will stop again. If more than one module is involved the fault scan cycle will halt sooner.

1-18. SWITCH ASSEMBLY (20A7)

The Switch Assembly consists of 12 thumbwheel (rate/mode) switches, three alarm lamps, two pushbutton switches and an audible alarm.

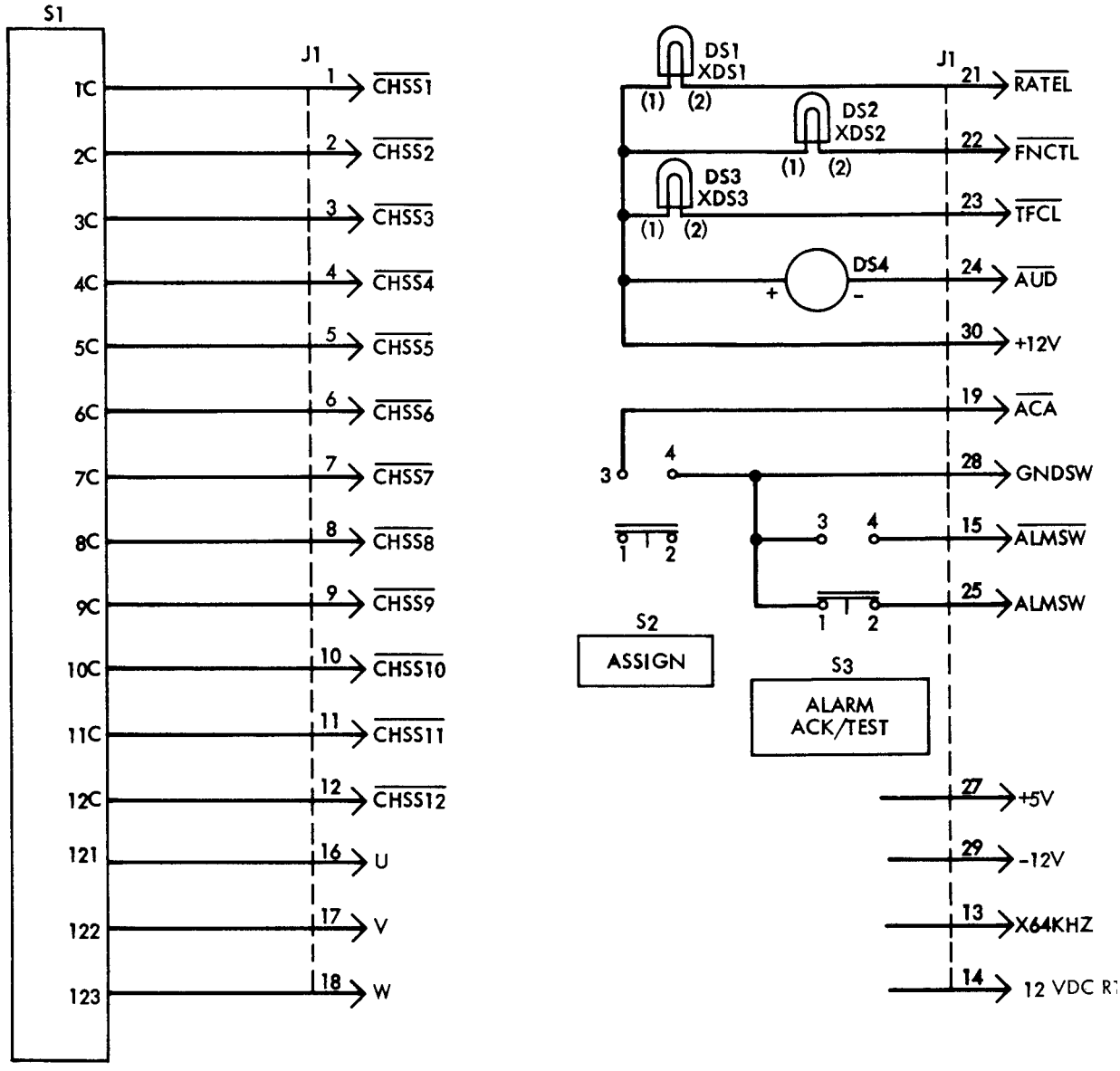


a. Thumbwheel Switches. The Switch Assembly thumbwheel switch is a printed circuit rotary type switch. Each switch uses three isolation diodes to prevent coding interference from the other unselected thumbwheels. The positions dialed on the 12 thumbwheel switches are encoded onto a 3-bit bus and buffered by the DCPG card. This allows the Common Control to read the selected data rates. Buffered output codes are defined as follows:

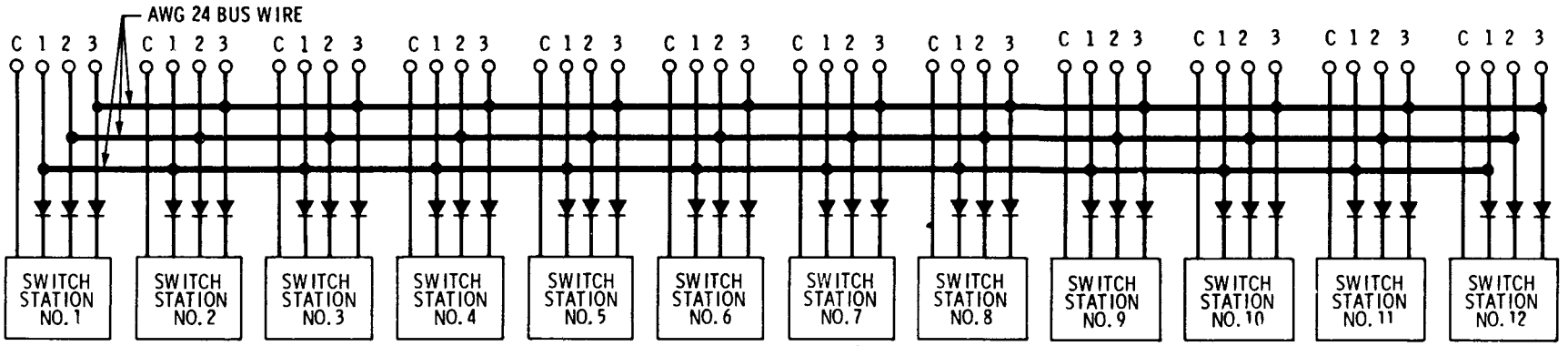
Dial Position	Rate Kb/s	U Bus	V Bus	W Bus
0	OFF	0	1	0
1	1.2 (TTY)	0	0	0
2	0.6	0	1	1
3	1.2	0	0	1
4	2.4	1	0	1
5	4.8	1	0	0
6	9.6	1	1	0
7	OFF	0	1	0

The contacts of the selected thumbwheel cause the appropriate rate code to appear on the 3-bit bus through the isolation diodes. All "ones" means an open circuit, i.e., channel module is missing, and is the same as "OFF".

SWITCH ASSEMBLY (20A7) SCHEMATIC DIAGRAM

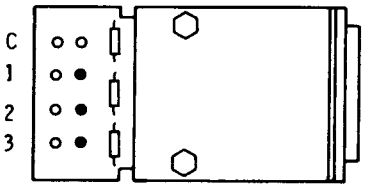


THUMBWHEEL SWITCH WIRING DIAGRAM



SWITCH CIRCUIT CONFIGURATION

TRUTH TABLE SWITCH STATIONS 1 THROUGH 12						
			OUTPUT			
			COMMON C CONNECTED TO TERMINALS VIA DIODE			
DIAL SETTING	POSITION MARKING	STOPS	1	2	3	
0	0	NONE	●		●	
1	1	↑	●	●	●	
2	2		●			
3	3		●	●		
4	4			●		
5	5			●	●	
6	6	↓			●	
7	7	NONE	●		●	

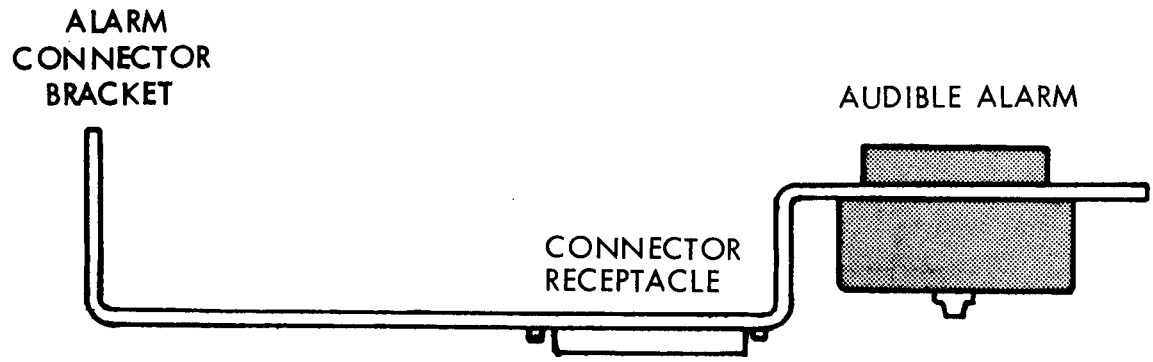


b. Alarm Lamps. The three indicator lamps, located on the ALARMS (see below) portion of the Switch Assembly, are: RATE, FCTN (functional), and TRFC (traffic). When a fault occurs either the TRFC or FCTN lamp will light. Data rates are examined through the Common Control circuit to determine whether or not the rate programmed on the thumbwheel switches exceeds 30 kbps. If exceeded, channel programming is inhibited and the RATE lamp is activated.

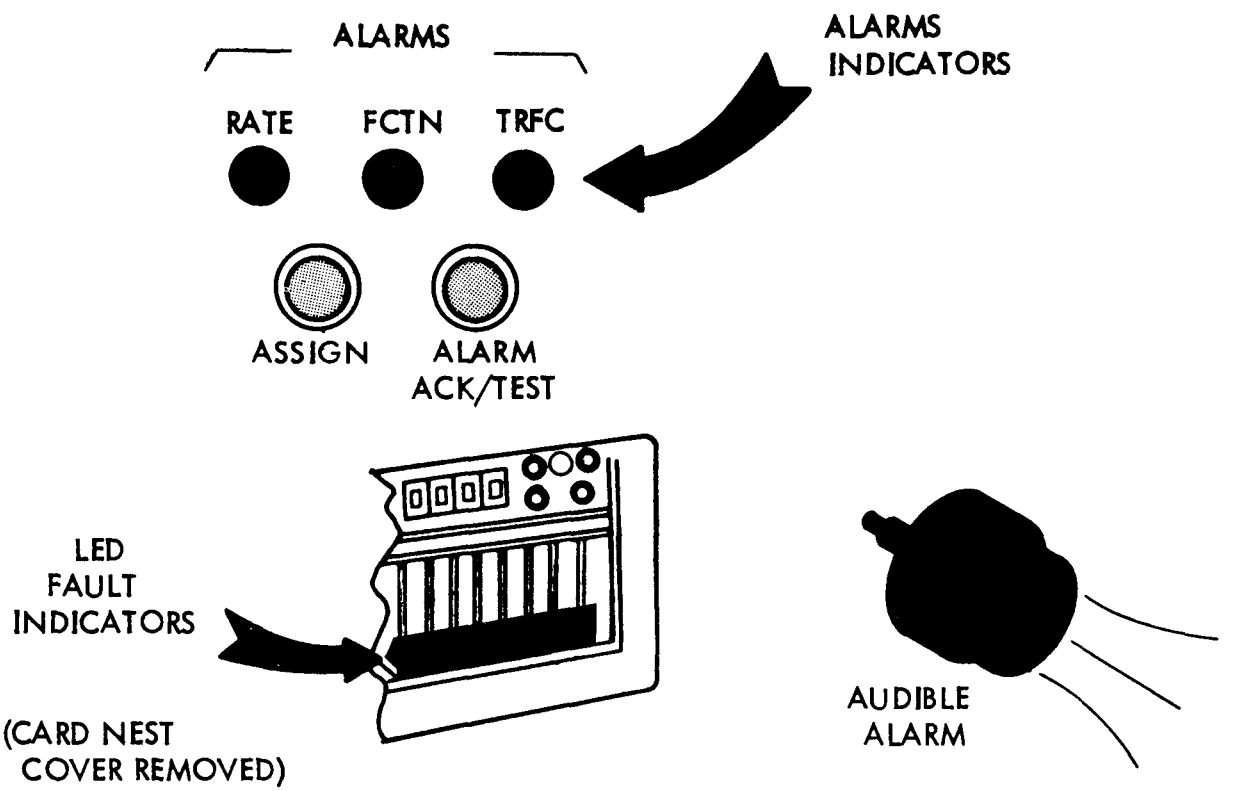
c. Pushbutton Switches. Below the three ALARM lamps are the ASSIGN and ALARM ACK/TEST pushbutton switches. When channel rates are selected by the thumbwheel switches, the ASSIGN pushbutton switch must then be pressed to activate the channels. The ALARM ACK/TEST pushbutton is used to test the three indicator lamps and module fault indicators. When depressed, all lamps should light if no fault exists. It is also used to silence the audible alarm after the fault has been corrected.

d. Audible Alarm. The audible alarm assembly is not visible when the Switch Assembly is in place on the TDDM. With the Switch Assembly removed from the chassis, the audible alarm is located on the alarm-connector bracket (see below) immediately behind the indicator lamps. The alarm activates during a fault situation. When the fault is corrected it sounds again until the ALARM ACK/TEST pushbutton is pressed.

ALARM-CONNECTOR BRACKET



ALARM	INDICATOR	REASON FOR ALARM
Rate Overload exceed (RATE)	Red Light	Programmed data rates overload exceeded 30 kbs, or misassignment of switches associated with FSK channels.
Functional (FCTN)	Red Light	Fault in any one of the PWB's or in the power supply.
Traffic (TRFC)	Red Light	Lack of activity at the DEMUX input with respect to the expected 32 kb/s conditioned diphase signal.
PWB Fault	Light Emitting Diodes (Red)	Located on each module, within the main frame, indicating a fault condition on that assembly. These can only be seen when the card nest cover is removed.
Audible Alarm	Solid State Auditory Device	Indicates by sound any or all of the above malfunctions, except rate alarm.



CHAPTER 2

DIRECT SUPPORT MAINTENANCE

Section I. GENERAL INFORMATION

2-1. SCOPE

This chapter covers direct support troubleshooting, maintenance and test procedures for the TDDM. Section I lists the tools and test equipment necessary to perform direct support manitenance. Troubleshooting and test procedures are described in Section II; maintenance procedures are covered in Section III.

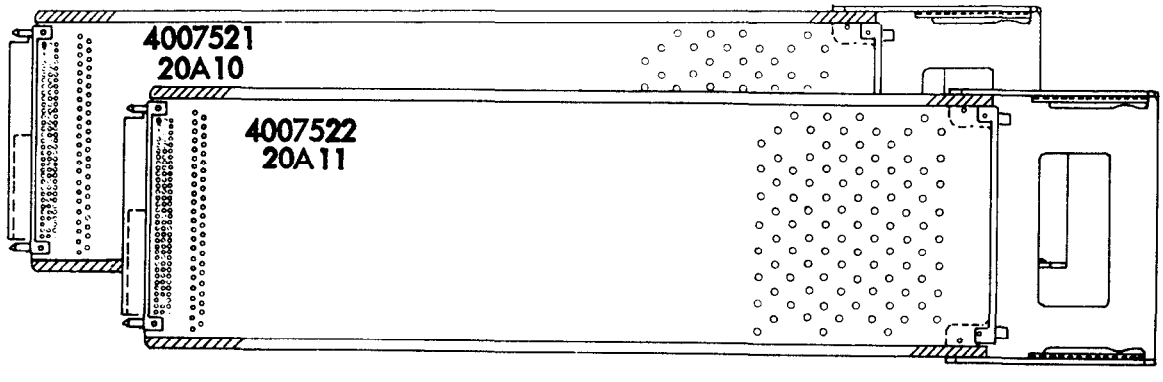
2-2. REPAIR PARTS, TOOLS AND TEST EQUIPMENT

Repair Parts: Refer to TM 11-5805-638-20P.
Tools and test equipment: Refer to TM 11-5805-638-12, Appendix B, for a complete listing of tools and test equipment required for test and repair of this equipment.

	NATIONAL STOCK NO.
Tool Kit, Electronic Equipment TK-101/G	5180-00-064-5178
Tool Kit, Electronic Equipment TK-105/G	5180-00-610-8177

TEST EQUIPMENT

Digital Multimeter AN/USM-486 with 85 RF probe
Extender Card 4007521 66-PIN (not provided with TDDM)
Extender Card 4007522 99-PIN (not provided with TDDM)



Section II. TROUBLESHOOTING

2-3. TROUBLESHOOTING INFORMATION

This section supplements the troubleshooting procedures found in the Operator and Organizational Maintenance Manual TM 11-5805-638-12. Direct support troubleshooting requires a limited amount of troubleshooting since modules 20A2 through 20A6 and 20A8 are replaced by organizational maintenance and repaired at depot level. The areas of responsibility for direct support are as follows:

- Test for defective chassis (20A9) and backplane. Replace if defective
- Check cable harness assemblies for defects. Replace if defective.
- Test Power Supply for defect. Replace if defective.

Location of defective components and/or wiring may be accomplished by following standard continuity and resistance measurement procedures, using the appropriate schematics or wiring diagrams.

2-4. TROUBLESHOOTING AIDS

Troubleshooting has three steps: (1) sectionalization, (2) localization, and (3) isolation.

- Sectionalization means tracing the fault to a module or assembly.
- Localization means tracing the fault to a subassembly within a module or assembly.
- Isolation means pinpointing the specific part or connection causing the trouble.

PROCEDURES

1. Visual Signs	Meter readings, dust, dirt, moisture; check for loose parts/connections.
2. Operate Unit	Operational test (see TM 11-5805-638-12)
3. Charts	Use available troubleshooting charts. Not all symptoms are listed in charts so use only as a guide.
4. Test Point Data	(See para 2-7). Use with troubleshooting chart.

2-5. SYMPTOM INDEX

Use this index to quickly find procedures in the troubleshooting chart.

TROUBLESHOOTING SYMPTOM	PROCEDURE NO.	PAGE
Alarms Indicator Lit	4	2-6
Audible Alarm Sounding	4	2-6
DC Output Lamp Not Lit	3	2-6
On-Off Switch Trips Off	1	2-4
Power Lamp Not Lit	2	2-5

CAUTION

DO NOT connect nor disconnect the ac power cable, harness cables, or power supply module (20A1) while the POWER switch on the front of the TDDM is set to the ON position.

2-6. TROUBLESHOOTING TABLE

Use the troubleshooting table to localize and isolate trouble. The table supplements the operational checks and may be used in conjunction with the applicable diagrams and/or schematics within this manual.

WARNING

Dangerous voltages are present in the Power Supply when 115 Vac is applied.

The troubleshooting table has Malfunction, Test or Inspection, and Corrective Action columns. The Malfunction (symptom) column is keyed to the Symptom Index (see para. 2-5). To use the chart, read down the symptom column of the Troubleshooting symptom Index until the condition is found. Locate the item on the Troubleshooting Chart and perform the corrective action(s) indicated.

Instructions for tests are provided in paragraph 2-7. Instructions for removal and/or replacement of components are provided in Section III, paragraph 2-8.

TABLE 2-1. TROUBLESHOOTING

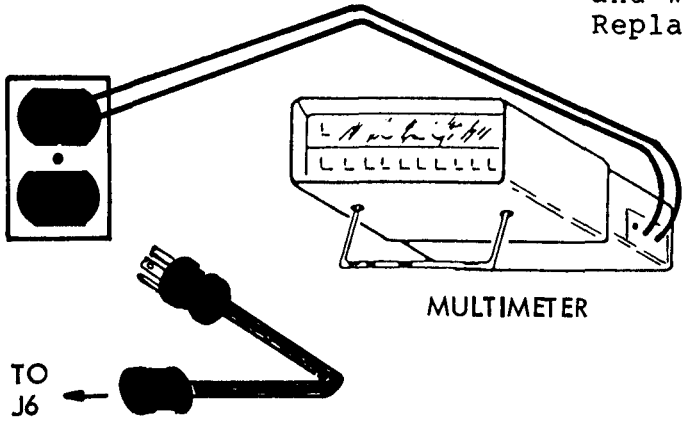
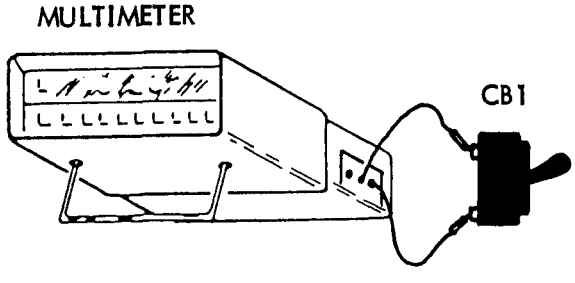
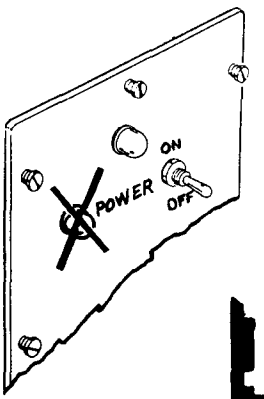
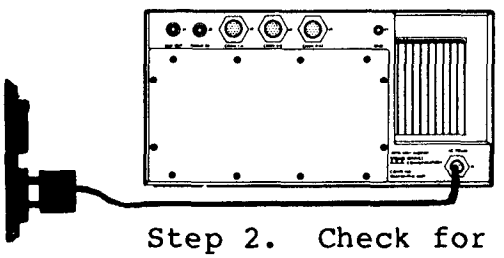
MALFUNCTION	TEST OR INSPECTION	CORRECTIVE ACTION
1. ON-OFF SWITCH TRIPS OFF	**CAUTION** DO NOT HOLD ON-OFF SWITCH IN ON POSITION.	
	Step 1. Ensure proper voltage to AC Power Connection (J6).	If multimeter indicates less than required 115 Vac check power cable and wall receptacle. Replace the faulty item.
		
	Step 2. With power removed, check circuit breaker (CB1) continuity.	If no continuity, replace Power Supply. Tag suspect Power Supply and refer to general support maintenance.
		

TABLE 2-1. TROUBLESHOOTING (CONTINUED)

	MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION
2	POWER LAMP NOT LIT

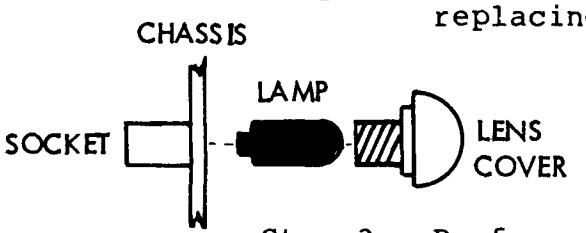


Step 1. Ensure that power cable is plugged into wall receptacle or power source.



If power cable is loose or out of receptacle, plug in and check to see that it holds securely in place.

Step 2. Check for POWER lamp failure by replacing the lamp.



Step 3. Perform continuity checks on: circuit breaker (CB1), thermal switch (S1), filters (FL1 & FL2), and connector (J1).

Refer findings to general support maintenance and forward Power Supply for repair.

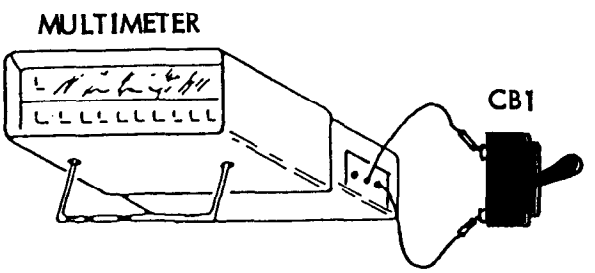
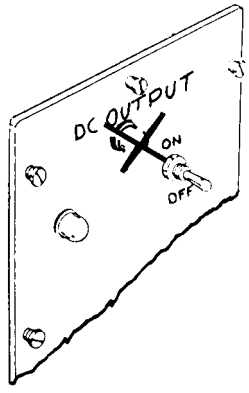


TABLE 2-1. TROUBLESHOOTING (CONTINUED)

MALFUNCTION	TEST OR INSPECTION	CORRECTIVE ACTION
3. DC OUTPUT LAMP NOT LIT.		Step 1. Replace DC OUTPUT Lamp. (See procedure for POWER lamp.) Step 2. Check dc outputs with multimeter. (See para 2-7.) Refer findings to general support maintenance and forward power supply for repair.
4. ALARMS INDICATOR(S) LIT AND/OR AUDIBLE ALARM SOUNDING (SEE NOTE).		

NOTE

Operational maintenance replaced module(s) with lit fault indicator(s) but did not correct fault.

Step 1. With power off, look for loose cable harness connection.

Ensure that all cable harness assemblies are secure in their connectors.

NOTE

The Switch Assembly harness is secured to the connector by a screw lock assembly. Ensure that both screws have been tightened.

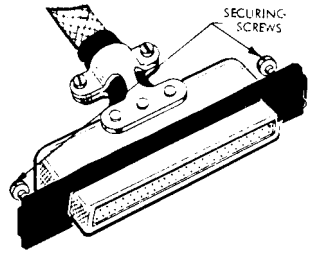
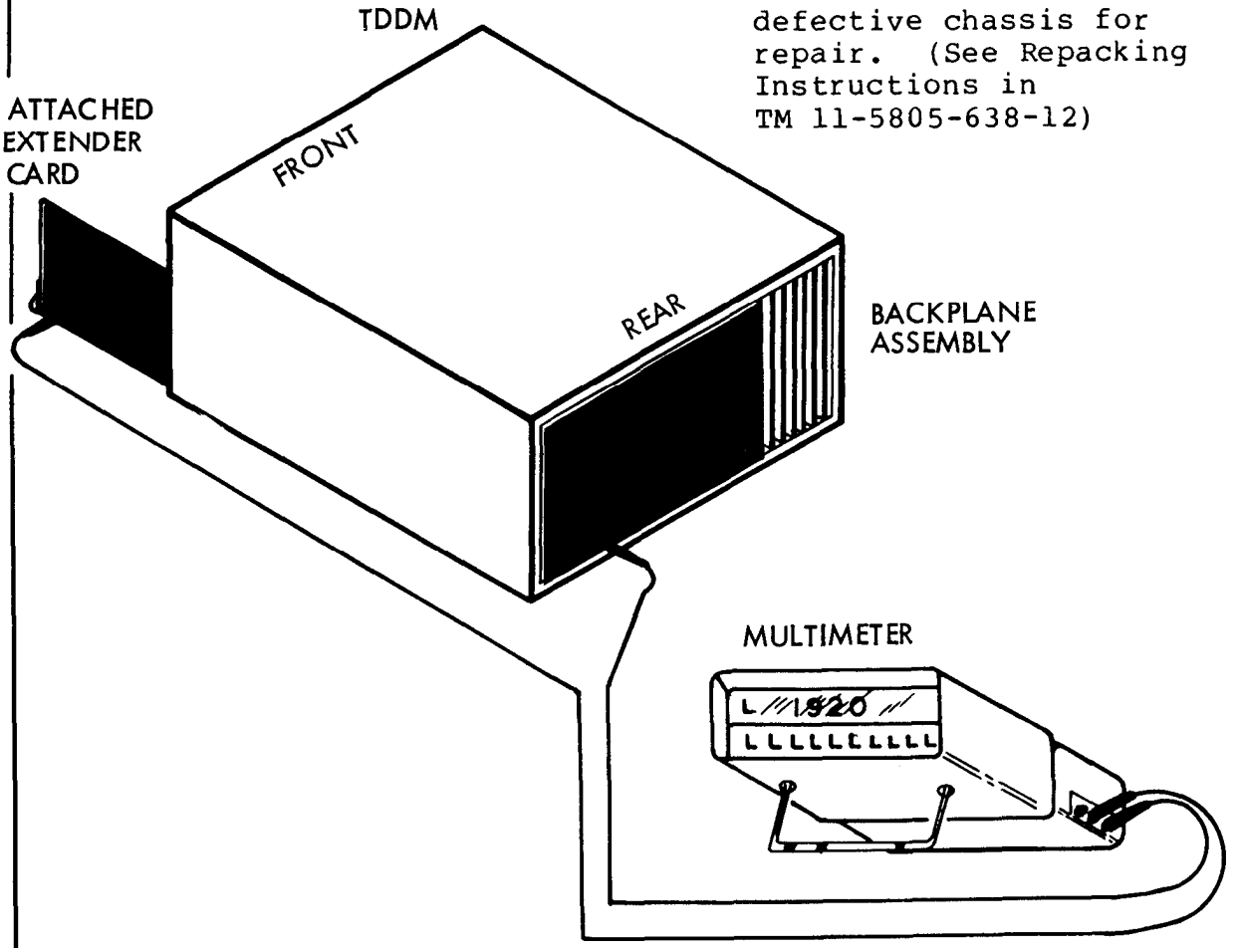


TABLE 2-1. TROUBLESHOOTING (CONTINUED)

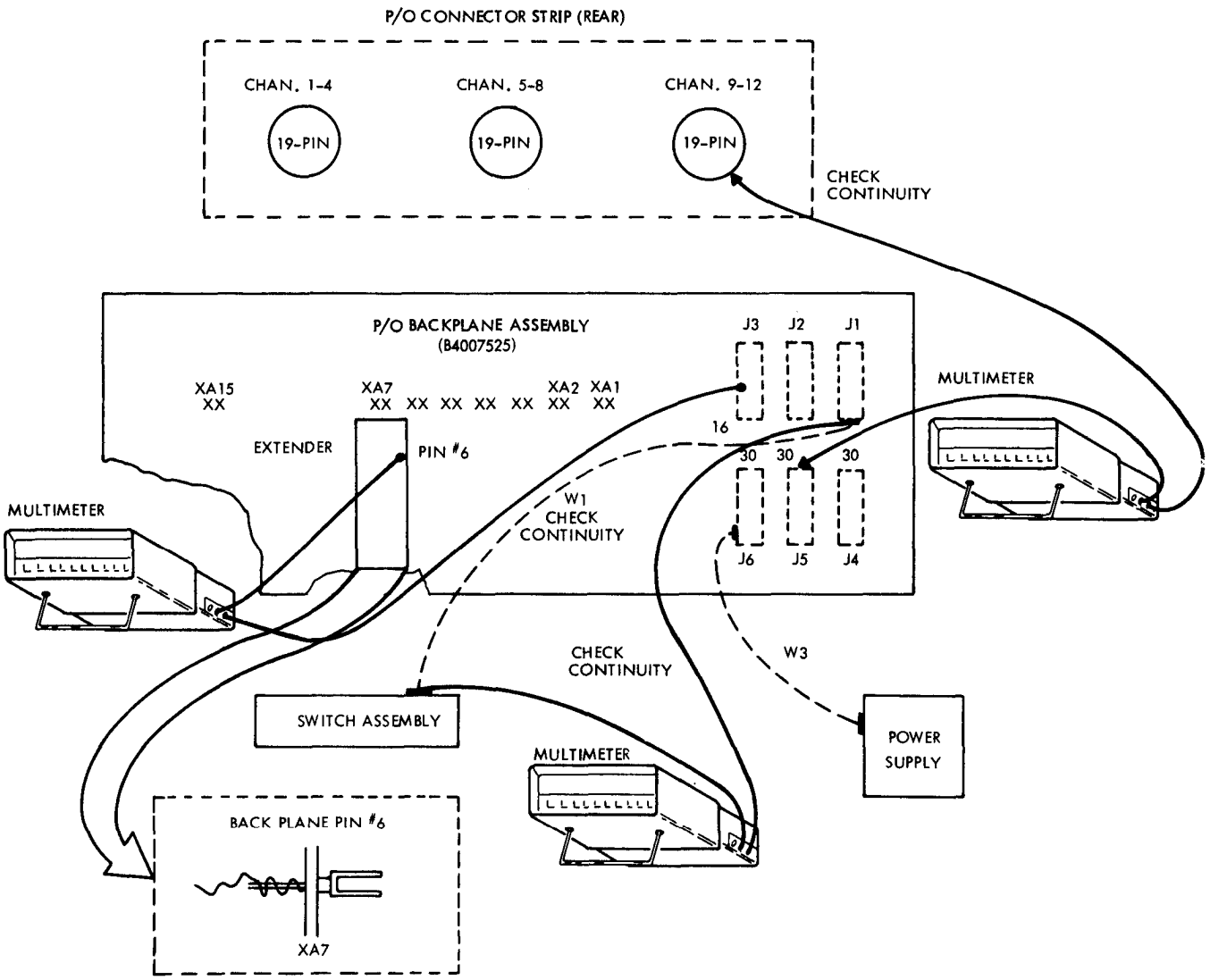
MALFUNCTION	TEST OR INSPECTION	CORRECTIVE ACTION
4. (Contd.)	Step 2. Check cable harnesses (W1 - W5) for continuity. Replace defective cable harness (see page 2-11). Forward defective cables to general support maintenance. Step 3. Measure chassis wiring for continuity. Use PWB Extender ITT DCD 4007521 (66-pin) or 4007522 (99-pin) as needed.	If chassis is found to be defective, replace it and refer findings to depot maintenance. Forward defective chassis for repair. (See Repacking Instructions in TM 11-5805-638-12)



2-7. TEST POINTS

1. CHASSIS (20A9)	FLUKE DIGITAL MULTIMETER 8030, CARD EXTENDER, ITT-DCD 4007521, 4007522	
No test points	Check for backplane and connector failures	Continuity

2. WIRING HARNESSES	FLUKE DIGITAL MULTIMETER 0830A	
No test points	Check for faulty wire or connector	Continuity



Section III. MAINTENANCE PROCEDURES

2-8. REMOVAL AND REPLACEMENT PROCEDURES

CAUTION

Do not attempt to remove or replace Power Supply or cable harnesses while the power cable is connected to the 115 Vac power source.

CAUTION

During removal and replacement, care should be used to prevent accidental damage to the equipment. Check carefully for loose hardware and/or connections.

Removal procedures at the direct support maintenance level consist of: 1) chassis, and 2) cable harness assemblies (W1 through W5) only. However, to replace the chassis it is necessary to remove all modules and assemblies. Module and assembly removal and replacement procedures are detailed in TM 11-5805-638-12.

a. Chassis Removal and Replacement. Chassis replacement requires that all modules (20A2 - 20A6, and 20A8), Switch Assembly (20A7), and Power Supply (20A1) be removed from the defective chassis.

REMOVE

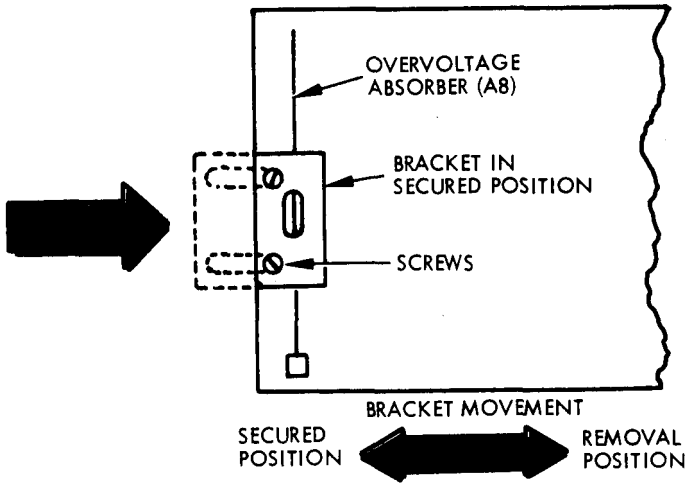
MODULES 20A2-20A6 AND 20A8

- Loosen 12 captive screws around outside edge of front card nest cover.
- Remove card nest cover.
- Pull outward on module extractor and then press down to separate module from connector.
- Pull module straight out through card guide.

NOTE

The Overvoltage Absorber module (20A8) is secured by a special bracket locking device.

- Loosen two bracket screws and slide bracket to the right.



REPLACE

- Slide the Overvoltage Absorber module slowly along card guide until it engages backplane.
- Push card extractor up until module is secure.
- Slide the bracket to the left and tighten both bracket screws.
- Slide the other modules in along card guides.
- Replace card nest cover and secure with 12 captive screws.

REMOVE

POWER SUPPLY (20A1)

- Set ON/OFF Power switch to OFF position.
- Loosen eight captive screws around outside edge of front of Power Supply.
- Grasp handle and pull Power Supply straight out.

REPLACE

- Slide the Power Supply along the chassis guides until rear connectors engage backplane.
- Secure Power Supply in chassis by tightening the eight captive screws.

REMOVE

SWITCH ASSEMBLY (20A7)

- Set Power Supply ON/OFF Power Switch to OFF position.

- Loosen eight captive screws around outer edge of Switch Assembly.
- Pull Switch Assembly straight out.
- Loosen two screws (screw lock assembly) securing connector (P7) and disconnect cable harness (W1) of Switch Assembly.

REPLACE

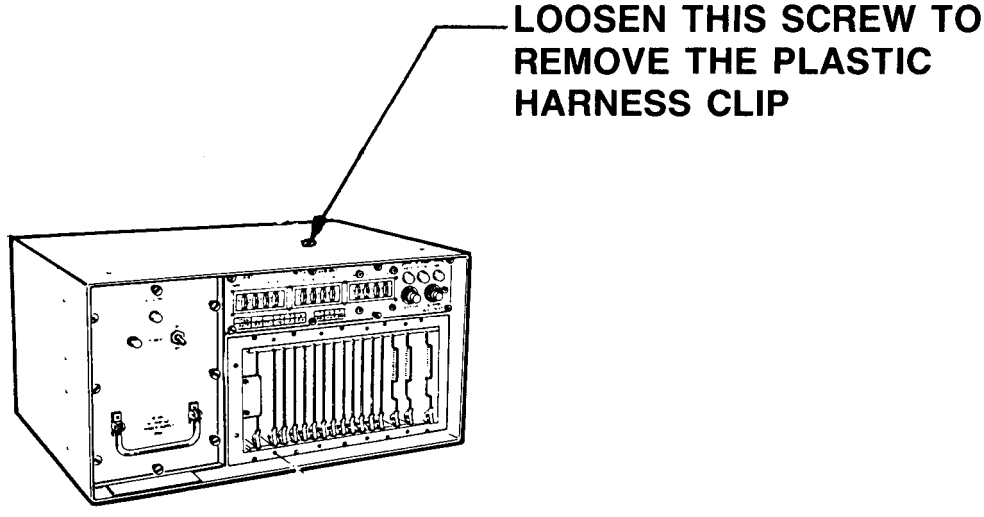
- Connect cable harness (W1) to rear of Switch Assembly and secure by tightening two screws.
- Line up the Switch Assembly with the chassis and carefully set in place.
- Secure Switch Assembly to chassis by tightening eight captive screws around the outer edge.

b. Harness Assembly Removal and Replacement. There are five cable harness assemblies used within the TDDM. They are as follows:

W1 - Switch Assembly Cable Harness
W2 - Channel/MUX Cable Harness
W3 - Power Supply Cable Harness
W4 - Channel Cable Harness
W5 - Channel/DEMUX Cable Harness

NOTE

The cable harnesses are tied down with plastic ties to avoid contact with components. These ties must be removed to effect removal of the harnesses. Also, the entire harness assembly is secured to the top of the TDDM cabinet by a plastic clip. This clip must be removed before attempting to remove cable harnesses.



REPLACE

- Plug the P3 and P6 connectors into their respective connector receptacles. Ensure that connectors are firmly in place.
- Plug the XA1 connector into the backplane assembly and secure with screws (2), washers (2), and hex nuts (2).
- Push the J6 connector through the chassis opening and secure with hex nut.

REMOVE

CHANNEL HARNESS ASSEMBLY (W4)

- Remove hex nut from J4 connector receptacle and pull through chassis opening.
- Unplug the P4 connector.

REPLACE

- Plug the P4 connector into the J4 connector receptacle. Ensure that connector is firmly in place.
- Push the J4 connector receptacle through the chassis opening and secure with hex nut.

REMOVE

CHANNEL/DEMUX HARNESS ASSEMBLY (W5)

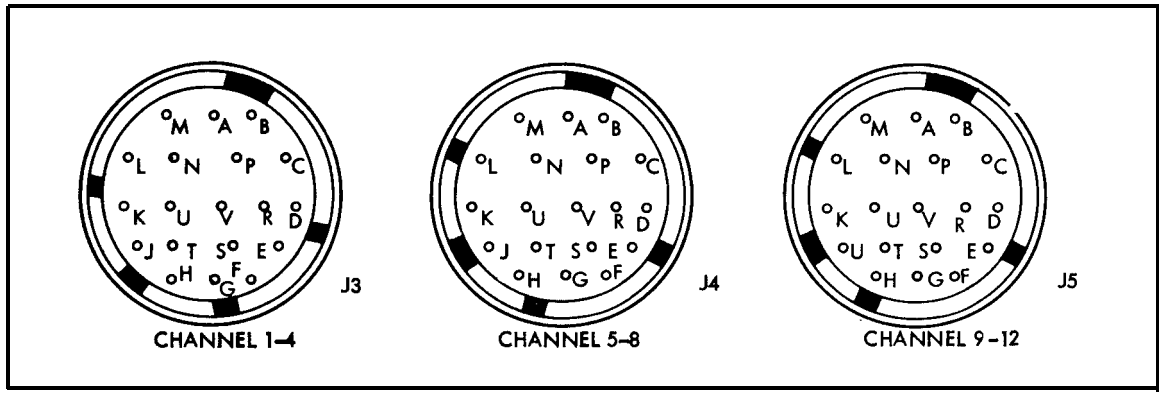
- Remove hex nuts from J2 and J5 connector receptacles and pull through chassis openings.
- Unplug the P5 connector.

REPLACE

- Plug the P5 connector into the J5 connector receptacle. Ensure that connector is firmly in place.
- Push the J2 and J5 connector receptacles through the respective chassis openings and secure them by replacing hex nuts.

PART OF CONNECTOR STRIP

(REAR OF TDDM)



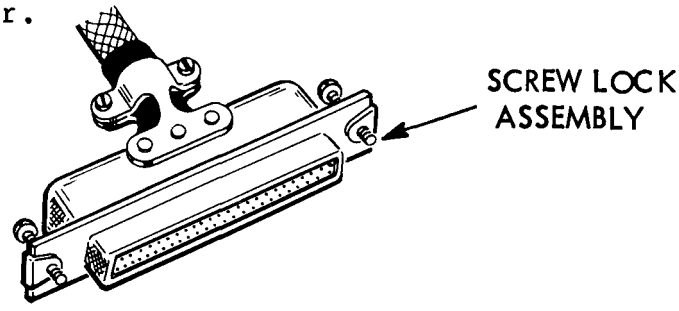
PIN DESIGNATION	DESCRIPTION
A	HIGH CHANNEL N IN
B	LOW CHANNEL N IN
C	HIGH CHANNEL N OUT
D	LOW CHANNEL N OUT
J	HIGH CHANNEL (N+1) IN
K	LOW CHANNEL (N+1) IN
L	HIGH CHANNEL (N+1) OUT
M	LOW CHANNEL (N+1) OUT
E	HIGH CHANNEL (N+2) IN
F	LOW CHANNEL (N+2) IN
G	HIGH CHANNEL (N+2) OUT
H	LOW CHANNEL (N+2) OUT
N	HIGH CHANNEL (N+3) IN
P	LOW CHANNEL (N+3) IN
R	HIGH CHANNEL (N+3) OUT
S	LOW CHANNEL (N+3) OUT
T	NC
U	CHASSIS GROUND
V	NC

LEGEND

N=1 FOR CHANNEL 1-4 CONNECTOR
N=5 FOR CHANNEL 5-8 CONNECTOR
N=9 FOR CHANNEL 9-12 CONNECTOR

SWITCH ASSEMBLY CABLE HARNESS (W1)

- Remove two screws from P7 connector screw lock assembly.
- Unplug Pl connector.



REPLACE

- Plug the P1 connector into the J1 connector receptacle. Ensure that connector is firmly in place.
- Plug the P7 connector into the J1 connector receptacle on the back of the Switch Assembly. Secure the connection by replacing and tightening the two screws in the screw lock assembly.

REMOVE

CHANNEL/MUX CABLE HARNESS (W2)

- Remove hex nuts from J1 and J3 connector receptacles and pull through chassis openings.
- Unplug P2 connector.

REPLACE

- Plug the P2 connector into the J2 connector receptacle. Ensure that connector is firmly in place.
- Push the J1 and J3 connector receptacles through the respective chassis openings and secure them by replacing hex nuts.

REMOVE

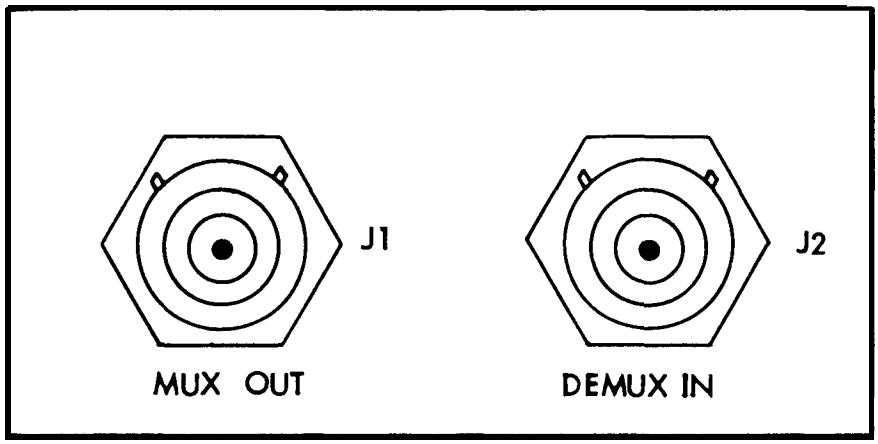
POWER SUPPLY CABLE HARNESS (W3)

- Remove hex nut from J6 connector receptacle and pull through chassis opening.
- Remove screws (2), washers (2), and hex nuts (2) from XA1 Connector.
- Unplug connectors P3 and P6.

MUX DEMUX BNC CONNECTORS

(UPPER LEFT REAR)

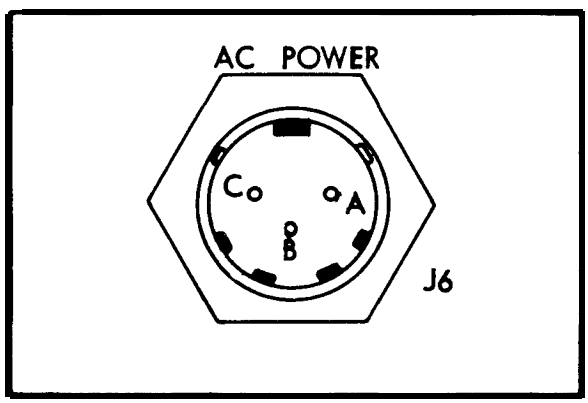
BJ-79



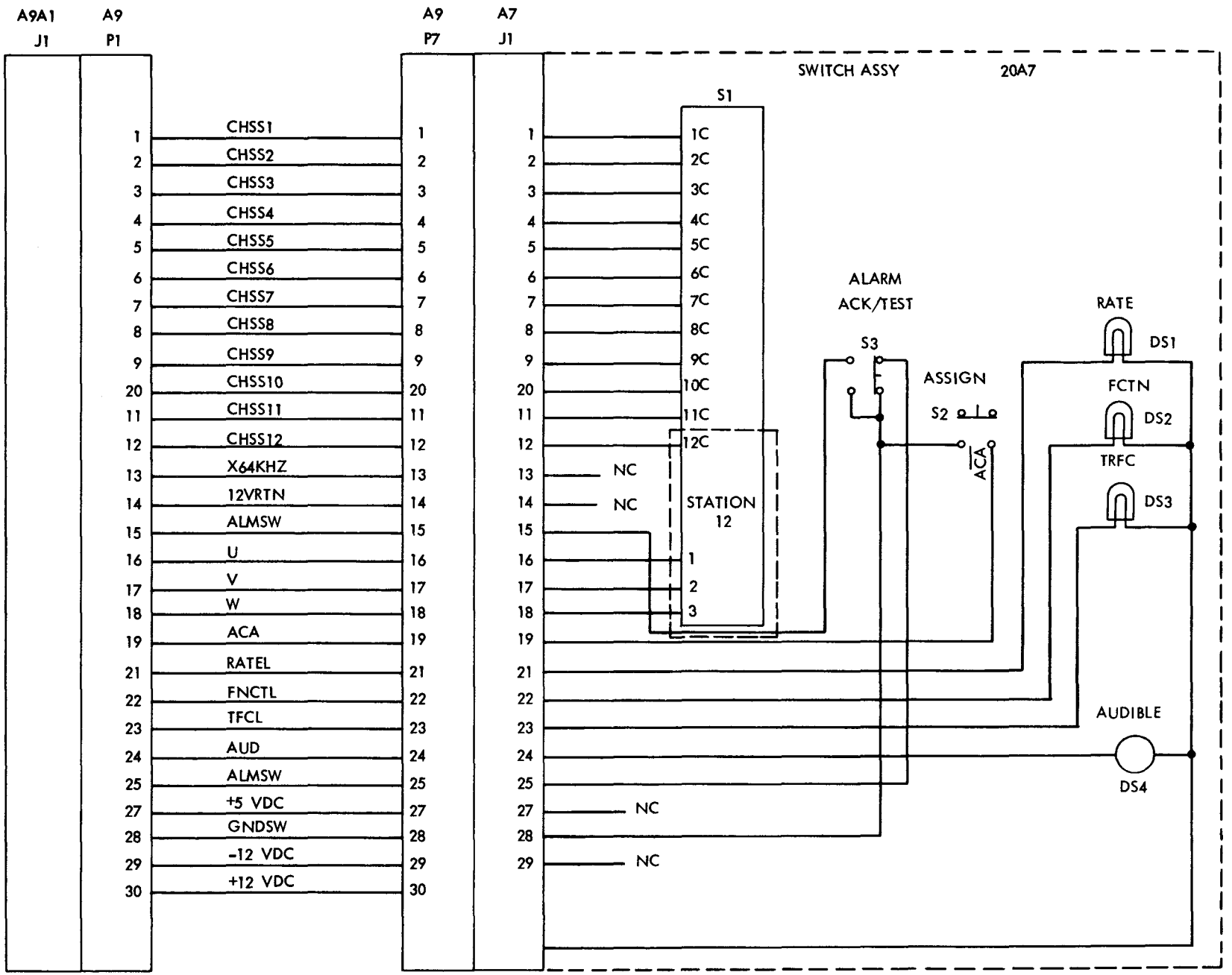
3-PIN AC POWER CONNECTOR

(LOWER RIGHT REAR)

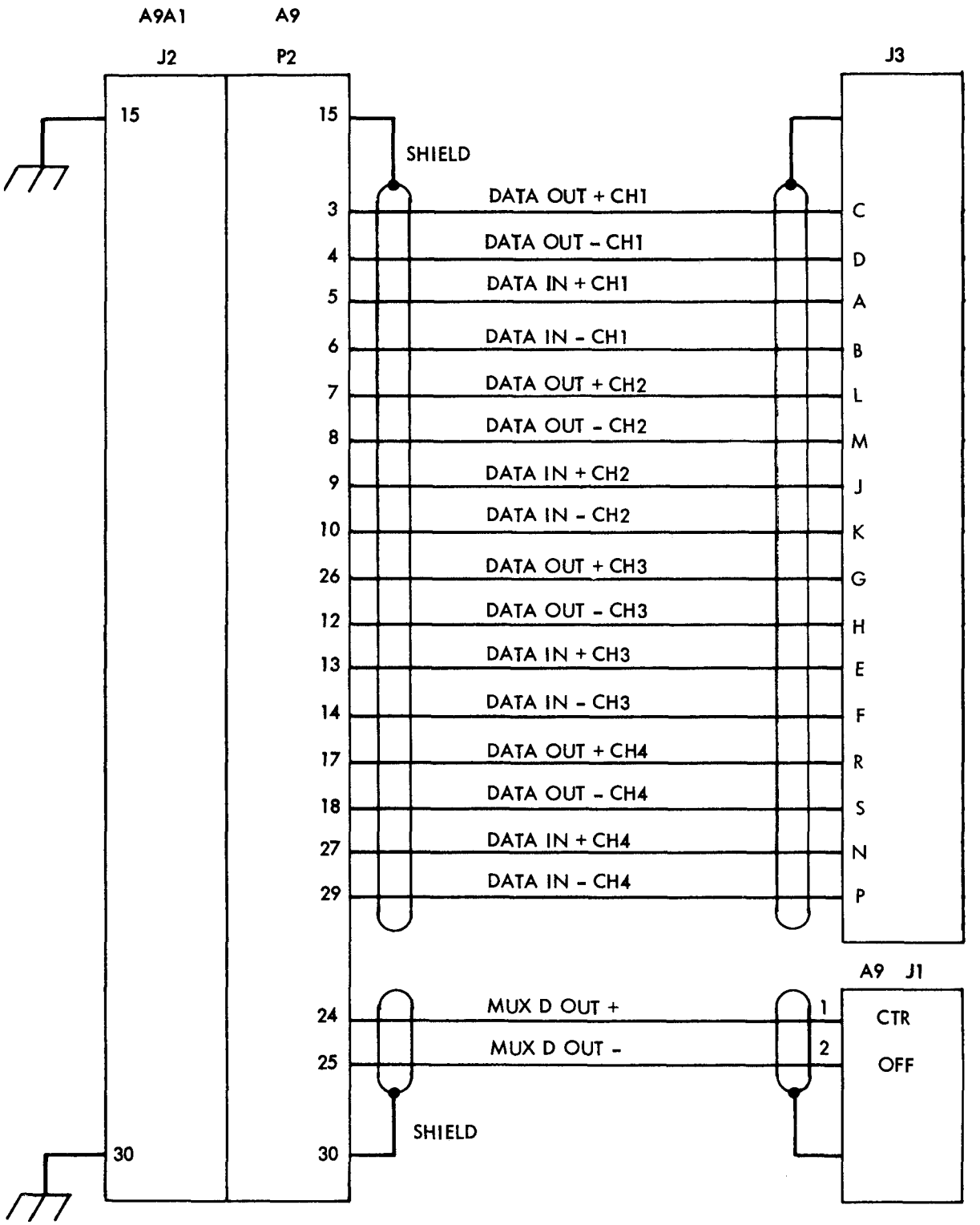
MS3114E12-3P



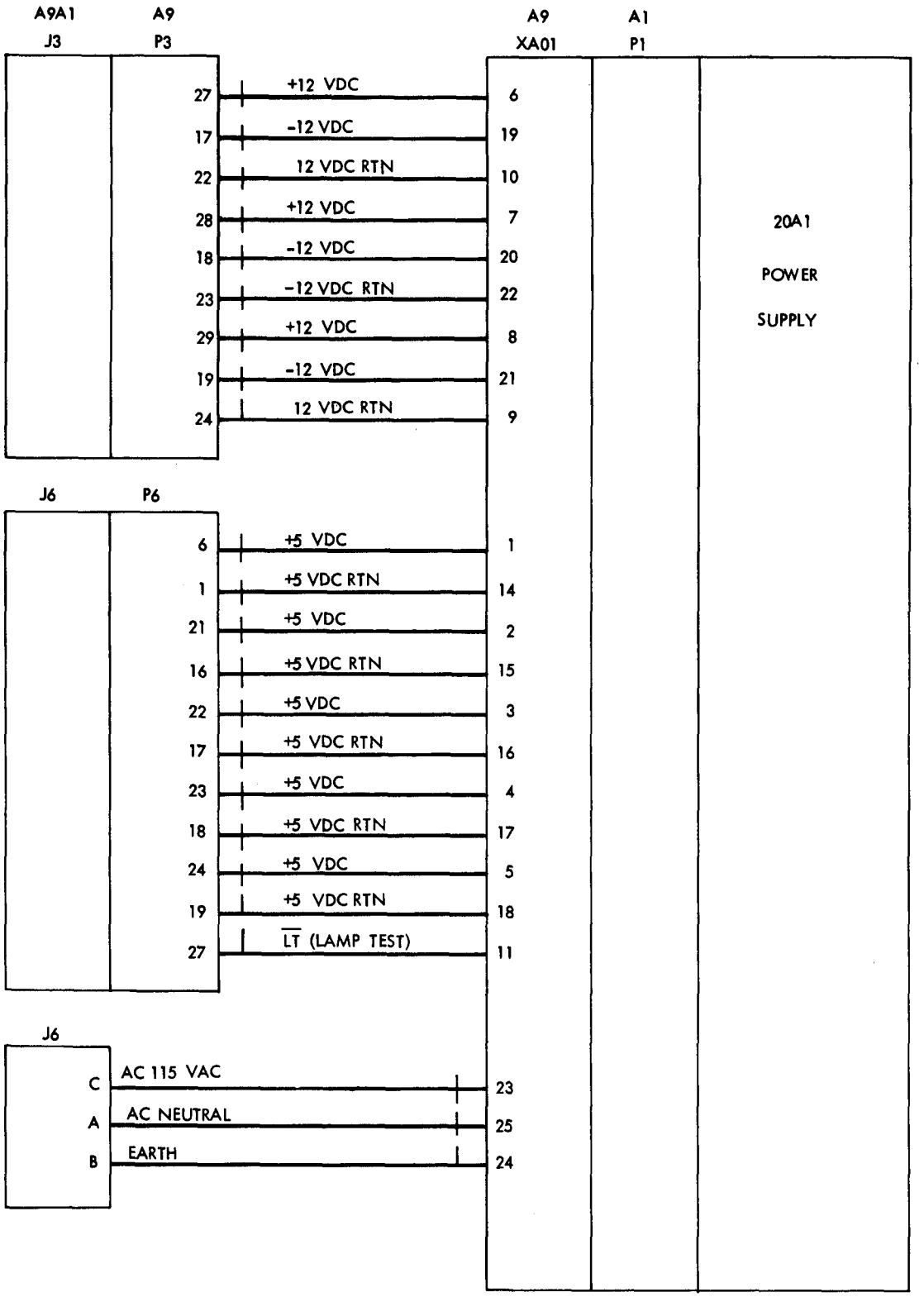
SWITCH ASSEMBLY CABLE HARNESS (W1)



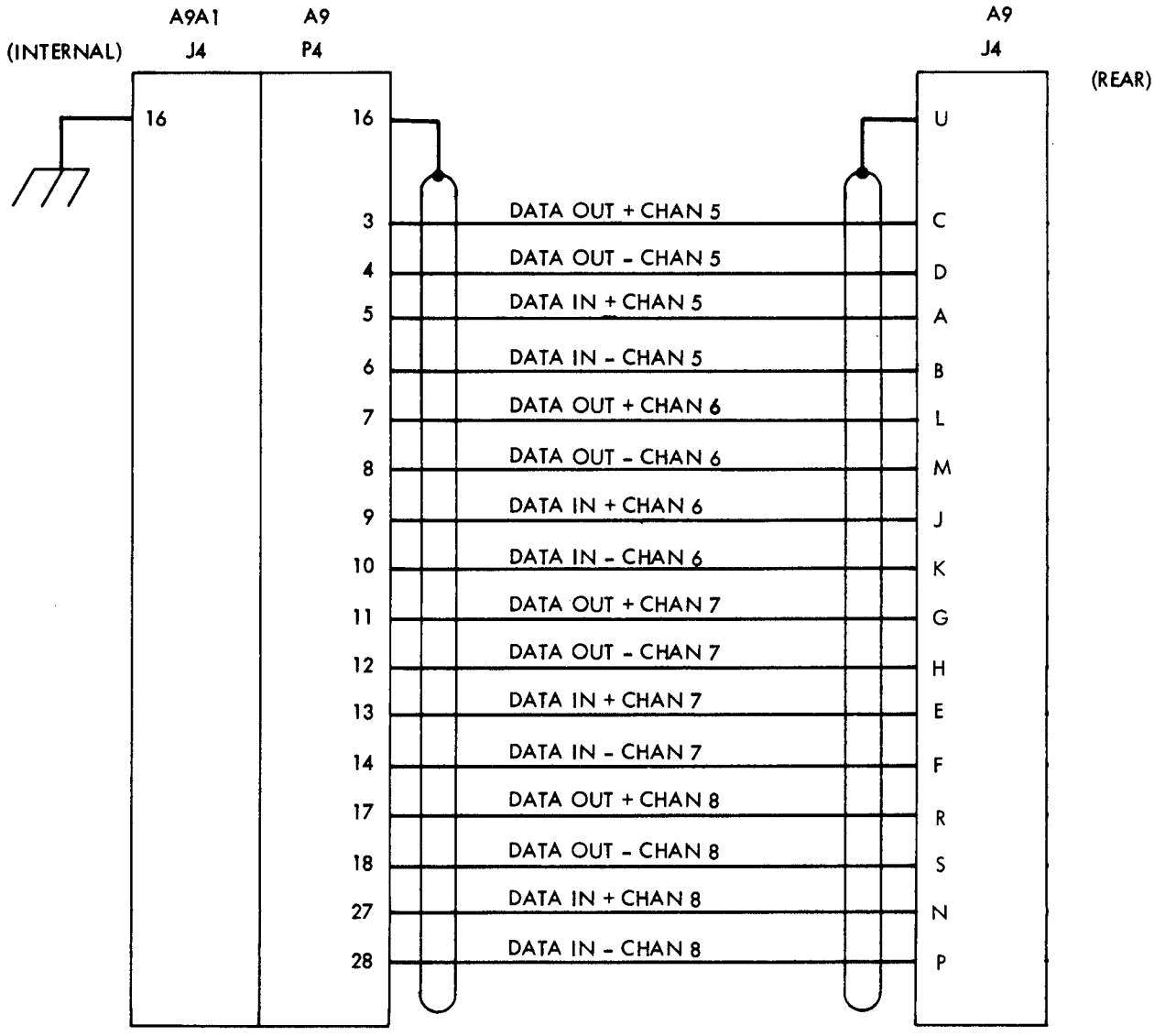
CHANNEL/MUX CABLE HARNESS (W2)



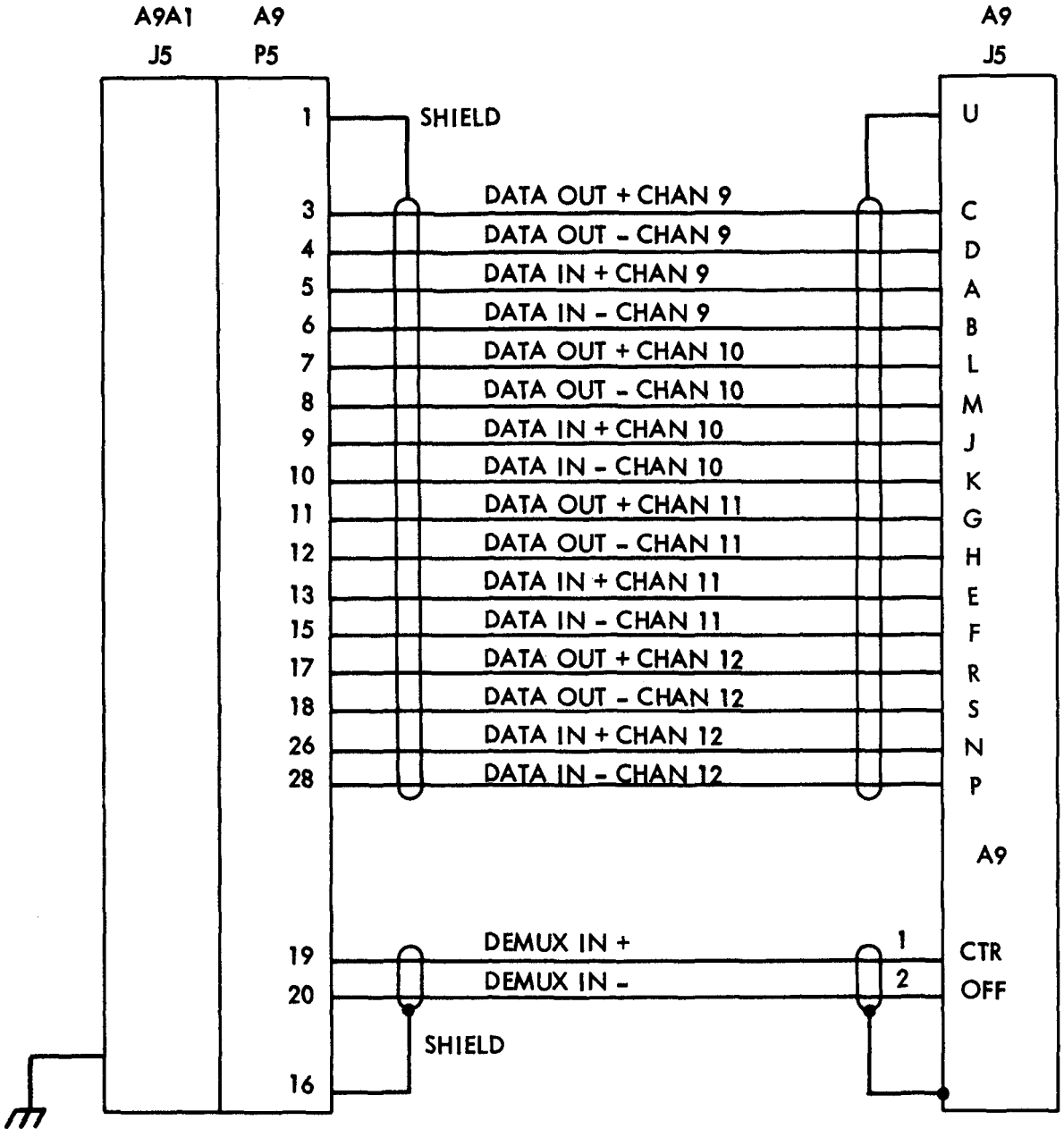
POWER SUPPLY CABLE HARNESS (W3)



CHANNEL CABLE HARNESS (W4)



CHANNEL/DEMUX CABLE HARNESS (W5)



CHAPTER 3

GENERAL SUPPORT MAINTENANCE

Section I. GENERAL INFORMATION

3.1. GENERAL

This chapter covers general support troubleshooting, maintenance, and test procedures for the TDDM. Section I lists the tools and test equipment needed to perform general support maintenance. Section II describes the troubleshooting and test procedures. Section III covers the maintenance procedures.

3-2. REPAIR PARTS, TOOLS, TEST EQUIPMENT, AND MATERIALS

General support maintenance requires the same repair parts, tools, test equipment and materials as listed for direct support (see para 2-2) with the addition of the following:

SPECIAL TOOLS

	NATIONAL STOCK NO.
Bendix Wrench Set (MS3114E Conn.) #11-6266-8-1 1/16″0, # 11-6266-10-1 3/16″0	
Wrap-N-Strap Tool P1602A	

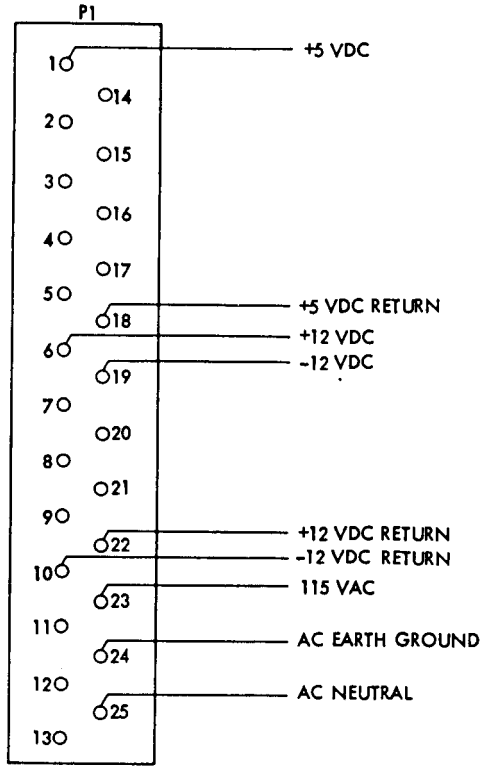
TEST EQUIPMENT

Power Supply HP 6002A	
Repair Facility PRC 350C	9490-00-031-4541
Switch Assembly Test Set ITT-DCD 1475707	

PARTS

Power Supply Load Resistors (MIL-R-39009B)
- 20 ohms-10 W, ±5% Type RER M Level
- 24 ohms-10 W, ±5% Type RER M Level
- 1.3 ohms-20 W, ±5% Type RER M Level

POWER SUPPLY TEST CABLE



The Power Supply Test Cable is to be constructed to permit operation of the Power Supply for testing, troubleshooting, and adjustment.

- Cable: Three-foot lengths of No. 24 AWG single-conductor stranded cable.

- Connector: Female side of M24308/4-3 connector to mate with Power Supply connector J1.

Section II. TROUBLESHOOTING

3-3. TROUBLESHOOTING INFORMATION

The general support troubleshooting chart supplements the direct support troubleshooting chart. See Chapter 2, Section II for troubleshooting definitions and procedures. Test point and voltage and resistance charts are also included to facilitate trouble-shooting. Specifically, the areas of responsibility for general support maintenance are as follows:

- Test defective Power Supply (20A1). Repair as needed.
- Test defective Switch Assembly (20A7). Repair as needed.
- Repair cable harness (W1 through W5) found to be defective by direct support maintenance.

3-4. BENCH TEST SETUP AND TEST CONDITIONS

Perform all checks in the troubleshooting chart with the Power Supply and test equipment as shown below. Read all instructions carefully before starting the troubleshooting procedures so you will understand what is to be accomplished.

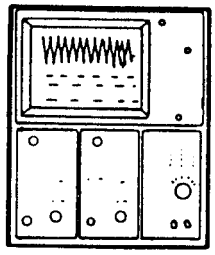
POWER CONNECTIONS

Connect pin 23 and 25 of the test cable to 115 V, 60/400 Hz. The power source must supply at least 5 amperes.

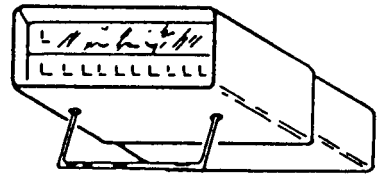
WARNING

When the power supply is connected to the 115 Vac power source, high voltage is present at exposed chassis components when the power supply covers are removed. DEATH or SERIOUS injury may result from contact.

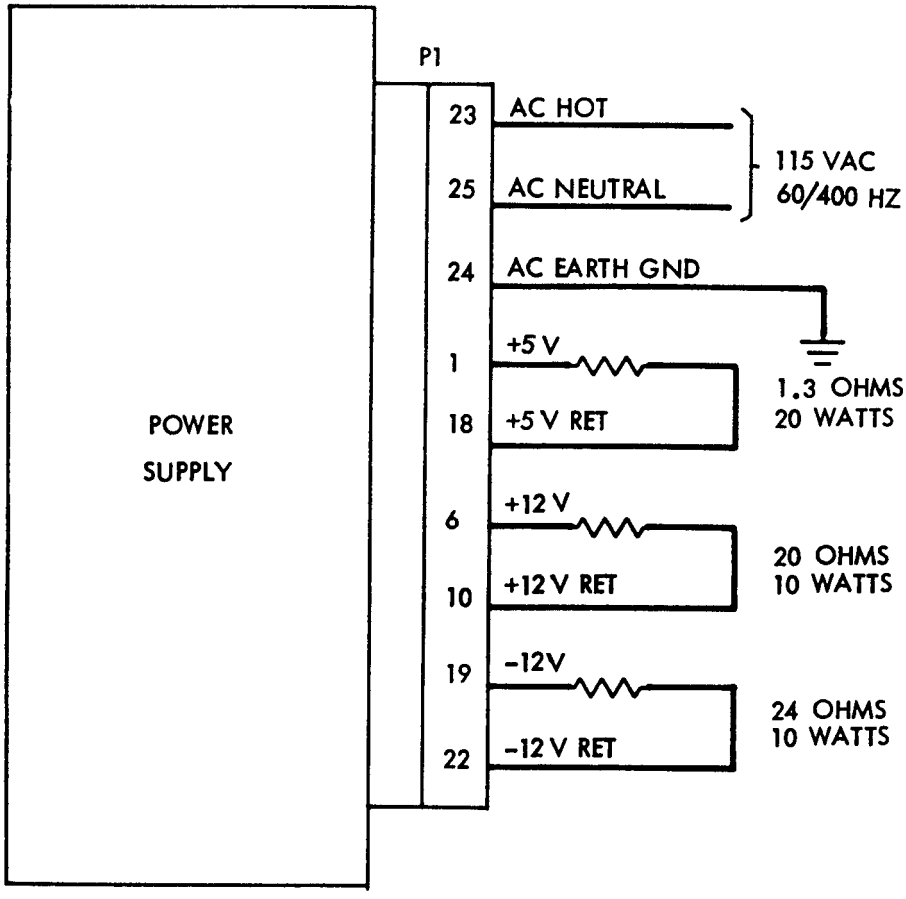
POWER SUPPLY TEST SETUP



OSCILLOSCOPE



DIGITAL
MULTIMETER



3-5. SYMPTOM INDEX

Use this index to quickly find procedures in the troubleshooting table.

TABLE 3-1. TEST POINTS

MODULE UNDER TEST POWER SUPPLY		TEST EQUIPMENT DIGITAL MULTIMETER/OSCILLOSCOPE	
TEST POINT	DESCRIPTION	DC VOLTAGE(V)	RIPPLE(V_{P-P})
TP1	+12 V UNREGULATED (+V AUX)	18.05	0.35
TP2	+12 V 723 OUTPUT	13.05	0
TP3	+12 V CURRENT SENSE	12.36	0
TP4	-12 V UNREGULATED	5.65	0.25
TP5	-12 V 723 OUTPUT	0.97	0
TP6	-12 V CURRENT SENSE	0.29	0
TP7	+ 5 V UNREGULATED	6.79	0.20
TP8	+ 5 V 723 OUTPUT	6.9	0
TP9	+ 5 V CURRENT SENSE	5.46	0
TP10	-V AUX	-12.05	0.45
TP11	+ 5 V SHUTDOWN	18.05	0.35
TP12	+ 5 V CROWBAR	0	0
TP13	+12 V CROWBAR	0	0
TP14	-12 V CROWBAR	-12.02	0

POWER SUPPLY PWB A1

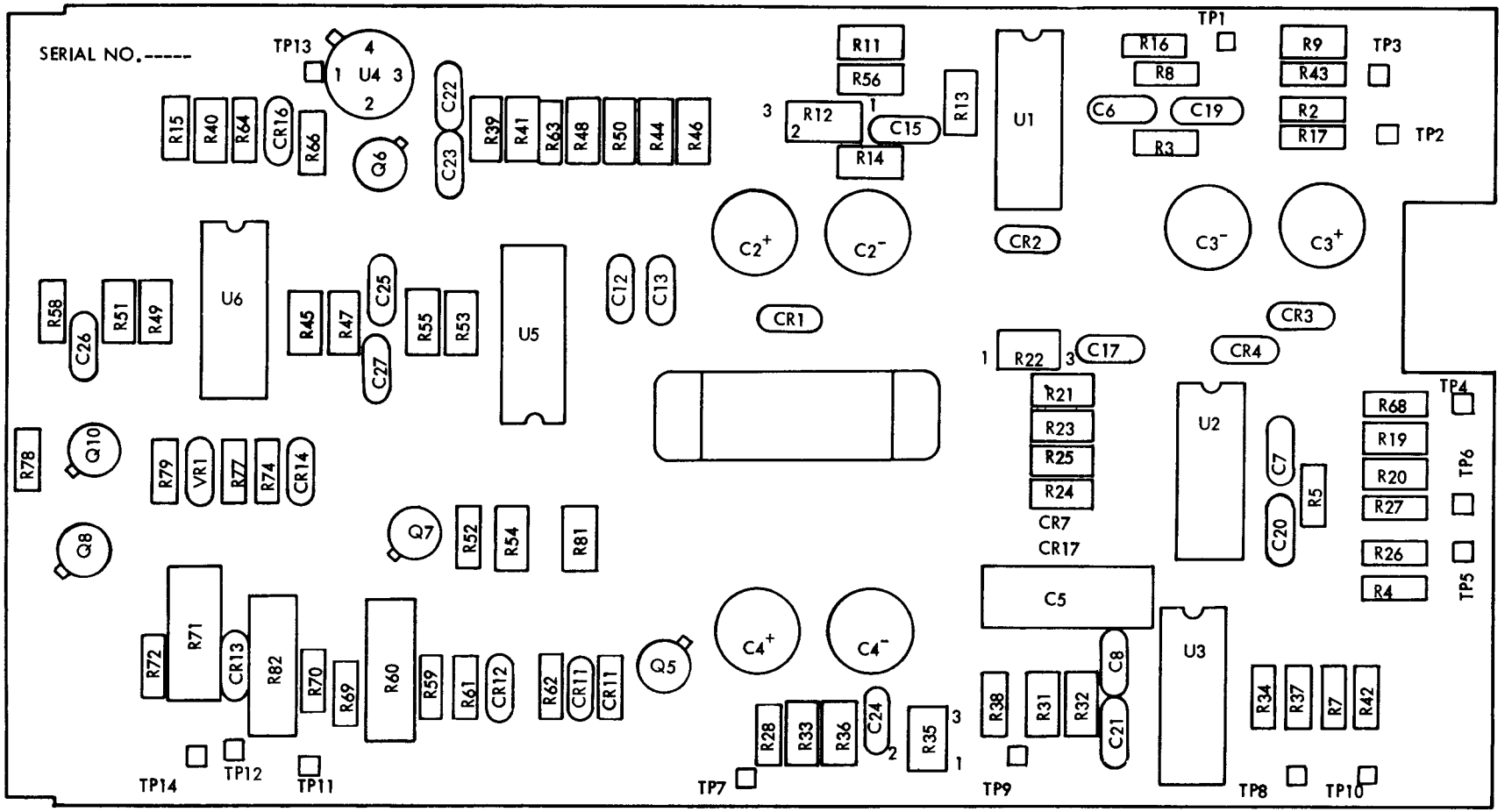


TABLE 3-2. TROUBLESHOOTING

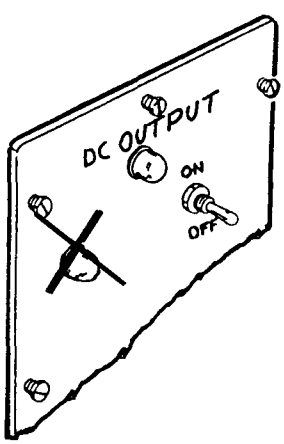
	MALFUNCTION	TEST OR INSPECTION	CORRECTIVE ACTION
1.	CIRCUIT BREAKER CB1 TRIPS OFF	Step 1. Check for shorted C2, C3, C4, CR5, or CR6.	Replace faulty component.
		Step 2. Check for shorted Q1, Q2 Q3, or Q4.	Replace faulty component.
		Step 3. Troubleshooting PWB A1, using resistance measurements.	Replace faulty component.
2.	POWER INDICATOR NOT LIT (Power applied to Power Supply and CB1 on)	Measure ac voltage across DS1 terminals.	a. If voltage across DS1 terminal is 115 Vac, replace DS1 lamp. b. If 115 Vac is not present, check for open CB1, FL1, FL2, or J1 (Pin 23). Replace defective part.
3.	No +5, +12, -12 V Outputs 	Measure ac voltage between terminals 1 and 2 of T1. If less than 108 Vac, check S1 for open. Replace if faulty.	

TABLE 3-2. TROUBLESHOOTING (CONTINUED)

	MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION
3.	+5 VDC OUTPUT IS NOT WITHIN 50 mV of +5 Vdc Step 1. Measure dc voltage at TP7. a. If voltage at TP7 is less than 6 Vdc, measure ac voltage between terminals 9 and 11 of T1. If less than 5 Vac, replace T1. b. Check for faulty CR5 or CR6. Replace faulty component. Step 2. Measure dc voltage at TP1. If voltage at TP1 is less than 15 Vac, measure ac voltage betwen pins 3 and 5 of T1. If less than 10 Vac, replace T1. Step 3. Measure dc voltage across R29. If voltage across R29 is greater than 350 mVdc, measure total resistance of R29 and R30. If not 0.077 ohm, replace faulty component. Step 4. Measure dc voltage between TP8 and TP9.

TABLE 3-2. TROUBLESHOOTING (CONTINUED)

	MALFUNCTION / TEST OR INSPECTION	CORRECTIVE ACTION
3.	(Continued)	If voltage between TP8 and TP9, is greater than 1 Vdc, check for open R6, Q3, or Q4. Replace faulty component.
	Step 5. Troubleshoot PWB A1, using voltage and resistance measurements.	Replace faulty component.
4.	+5 VDC OUTPUT RIPPLE VOLTAGE EXCEEDS 20 mVrms	
	Step 1. Measure ripple voltage TP1.	a. If over 1.0 Vp-p, replace C4. b. If over 2.0 Vp-p, replace C2.
	Step 2. Troubleshoot PWB A1, using voltage and resistance measurements.	Replace faulty component.
5.	+12 VDC OUTPUT IS NOT WITHIN 240 mV of +12 Vdc	
	Step 1. Measure dc voltage at TP1.	If voltage at TP1 is less than 15 Vdc, measure ac voltage between terminals 3 and 5 of T1. If less than 10 Vac, replace T1.

TABLE 3-2. TROUBLESHOOTING (CONTINUED)

	MALFUNCTION	TEST OR INSPECTION	CORRECTIVE ACTION
5.	(Continued)	Step 2. Measure dc voltage across R57.	If voltage at R57 is greater than 375 mVdc, replace R57.
		Step 3. Measure dc voltage between TP2 and TP3.	If voltage between TP2 and TP3 is greater than 0.6 Vdc, replace Q1.
		Step 4. Troubleshoot PWB A1, using voltage and resistance measurements.	Replace faulty component.
6.	+12 Vdc OUTPUT RIPPLE VOLTAGE EXCEEDS 20 mVrms.		
		Step 1. Measure ripple voltage at TP1.	If ripple voltage at TP1 is greater than 2 Vp-p, replace C2.
		Step 2. Troubleshoot PWB A1, using voltage and resistance measurements.	Replace faulty component.

TABLE 3-2. TROUBLESHOOTING (CONTINUED)

	MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION
7.	-12 VDC OUTPUT IS NOT WITHIN 240 mV of -12 Vdc Step 1. Measure dc voltage between TP4 and -12 Vdc output. If less than 15 Vdc, measure ac voltage between terminals 6 and 8 of T1. If less than 10 Vac, replace T1 . Step 2. Measure dc voltage across R18. If greater than 325 mVdc, replace R18. Step 3. Measure dc voltage between TP5 and TP6. If greater than 0.6 Vdc, replace Q1. Step 4. Troubleshoot PWB A1, using voltage and resistance measurements. Replace faulty component.
8.	-12 VDC OUTPUT RIPPLE VOLTAGE EXCEEDS 20 mVrms Step 1. Measure ripple voltage between TP5 and -12 Vdc output. If greater than 1.5 Vp-p, replace C3.

TABLE 3-2. TROUBLESHOOTING (CONTINUED)

	MALFUNCTION TEST OR INSPECTION	CORRECTIVE ACTION
8.	(Continued) Step 2. Troubleshoot PWB A1, using voltage and resistance measurements.	Replace faulty component.
9.	ALARMS INDICATORS LIT AND/OR AUDIBLE ALARM SOUNDING. Step 1. Direct support maintenance found cable harness assembly W1 to be defective. Check for loose or broken pins, receptacle or wire.	Repair cable harness by replacing defective plug or jack end or faulty wire.
10.	CHANNELS NOT RESPONDING TO ASSIGN SWITCH. Step 1. Check operation of switch assembly with continuity tests using multimeter.	a. Assign switch. Check for continuity between pins 19 and 28 of J1 with ASSIGN switch depressed. If ASSIGN switch does not function properly, replace it and repeat continuity test. b. ALARM ACK/TEST switch. Check for continuity between pins 15 and 28 of J1 with ALARM ACK/TEST switch depressed. Check for continuity between pins 25 and 28 of J1 with ALARM ACK/TEST switch in normal position. If ALARM ACK/TEST switch does not function properly, replace it and repeat test.

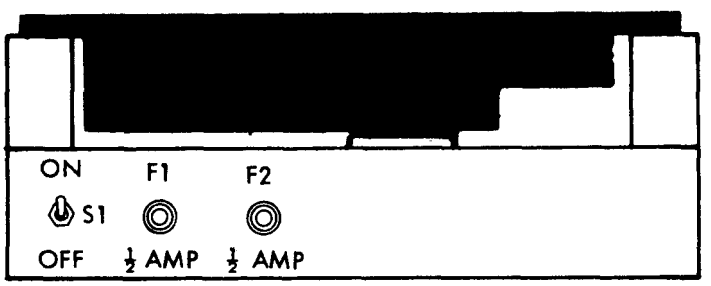


TABLE 3-2. TROUBLESHOOTING (CONTINUED)

MALFUNCTION	TEST OR INSPECTION	CORRECTIVE ACTION
10. (Continued)	c. Thumbwheel switch segment. Check for continuity between pin C and pins 1, 2, and 3 of the suspect segment as shown in truth table. If thumbwheel switch does not function properly replace it and repeat test.	

Dot in truth table indicates continuity. Blank indicates no continuity.

TRUTH TABLE
SWITCH STATIONS 1 THROUGH 12

DIAL SETTING	POSITION MARKING	STOPS	OUTPUT: COMMON C CONNECTED TO TERMINALS VIA DIODE 1	2	3	
0	0	NONE	•		•	
1	1	↑	•	•	•	
2	2		•			
3	3		•	•		
4	4			•		
5	5			•	•	
6	6	↓			•	
7	7	NONE	•		•	

Connect common (-) lead of multimeter to terminal C.

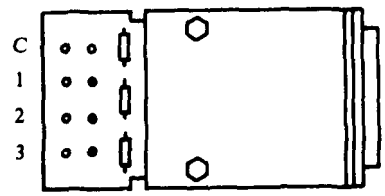
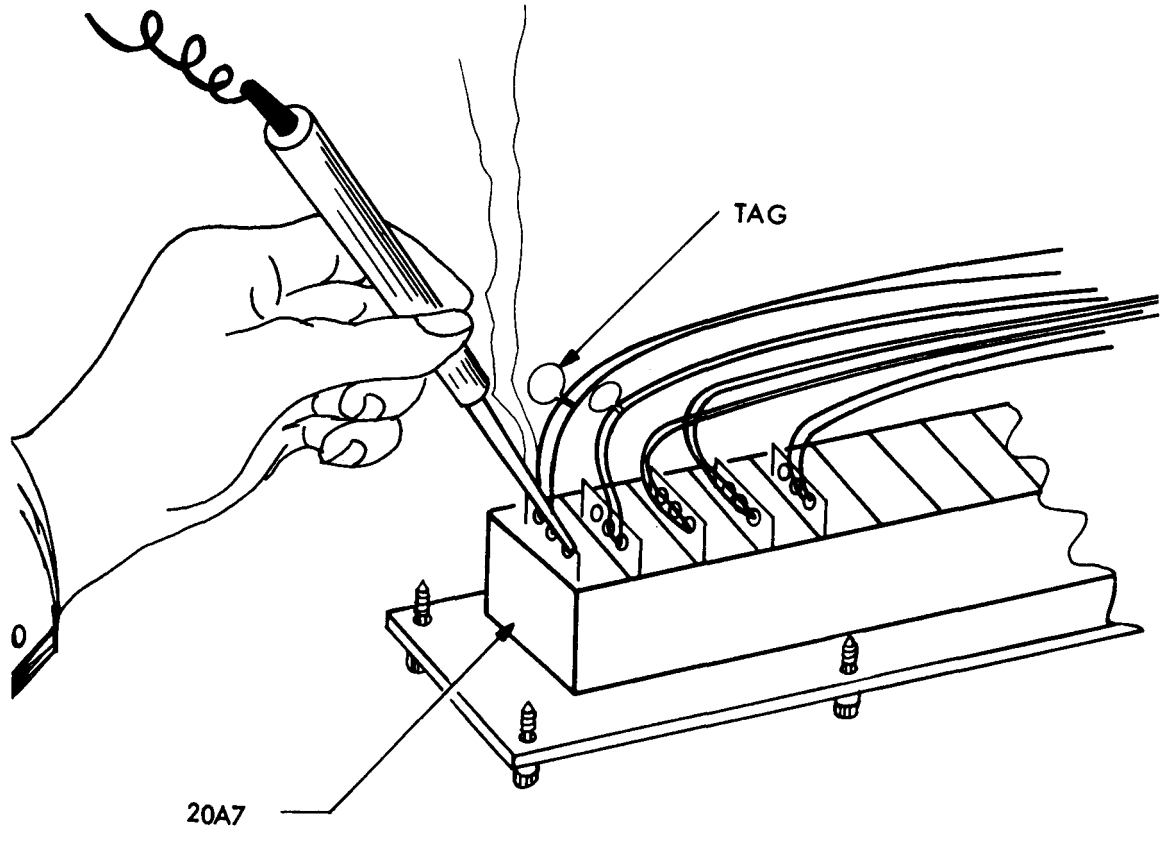


TABLE 3-2. TROUBLESHOOTING (CONTINUED)

MALFUNCTION	TEST OR INSPECTION	CORRECTIVE ACTION
10.	(Continued)	

CAUTION

Before unsoldering connections, wires should be tagged for ease of replacement.



3-6. VOLTAGE AND RESISTANCE MEASUREMENTS

Voltages and resistances at the various test points, pins, and terminals are given in the following table. Use the table to supplement the information given in the troubleshooting table and to troubleshoot PWB A1.

TABLE 3-3. VOLTAGE AND RESISTANCE

TERMINAL	Voltage			Resistance	
	Volts	Volts (P-P)	Conditions	(Ohms)	Conditions
P1-1 to 5	5.02 dc	0	Ref. to E20	6 K	Neg. on P1-14
P1-6 to 8	-12.01 dc	0	Ref. to E20	3.4 K	Neg. on P1-9
P1-9, 10	0	0	Ref. to E25	2.9 K	Neg. on P1-6
P1-11	0.17 dc	0	Ref. to E25	3.5 K	Pos. on P1-14
P1-14 to 18	0	0	Ref. to E25	5.3 K	Neg. on P1-1
P1-19 to 21	-12.01 dc	0		2.9 K	Neg. on P1-22
P1-22	0	0	Ref. to E25	9 K	Neg. on P1-19
P1-23	115 ac	325	Ref. to P1-25	7.5 K	Neg. on P1-25
P1-24	0	0	Ref. to Chassis	0.1 K	Neg. on Chassis
P1-25	115 ac	325	Ref. to P1-23	7.5 K	Neg. on P1-23
TP1	18.05 dc	0.35	Ref. to E25	11 K	Neg. to E25
TP2	13.05 dc	0	Ref. to E25	15 K	Neg. to E25
TP3	12.36 dc	0	Ref. to E25	15 K	Neg. to E25
TP4	5.6 dc	0.25	Ref. to E25	20 K	Neg. to E25
TP5	0.97 dc	0.25	Ref. to E25	11 K	Neg. to E25
TP6	0.29 dc	0	Ref. to E25	10 K	Neg. to E25
TP7	6.79 dc	0.20	Ref. to E25	25 K	Neg. to E25
TP8	6.90 dc	0	Ref. to E25	17 K	Neg. to E25
TP9	5.46 dc	0	Ref. to E25	16 K	Neg. to E25
TP10	-12.05 dc	0.45	Ref. to E25	15 K	Neg. to E25
TP11	18.05 dc	0.35	Ref. to E25	3.7 K	Neg. to E25
TP12	0	0	Ref. to E25	10 K	Neg. to E25
TP13	0	0	Ref. to E25	8.5 K	Neg. to E25
TP14	-12.02 dc	0	Ref. to E25	2.9 K	Neg. to E25
T1-1 to T1-2	113.7 ac	320	Ref. to E25	5.2 K	Neg. to E25
T1-3 to T1-5	30.95 ac	37	Ref. to E25	1.7 K	Neg. to E25
T1-6 to T1-8	29.65 ac	35	Ref. to E25	1.7 K	Neg. to E25
T1-9 to T1-11	18.9 dc	23	Ref. to E25	0.25 K	Neg. to E25

TABLE 3-3. VOLTAGE AND RESISTANCE (CONTINUED)

TERMINAL	Voltage			Resistance	
	Volts	Volts (P-P)	Conditions	(Ohms)	Conditions
Q1 Coll.	18.05 dc	0.35	Ref. to E25	1 K	Neg. to E25
Q1 Base	13.05 dc	0	Ref. to E25	2.9 K	Neg. to E25
Q1 Emit.	12.36 dc	0	Ref. to E25	2.3 K	Neg. to E25
Q2 Coll.	5.65 dc	0.25	Ref. to E25	11 K	Neg. to E25
Q2 Base	0.97 dc	0	Ref. to E25	1 K	Neg. to E25
Q2 Emit.	0.29 dc	0	Ref. to E25	0.5	Neg. to E25
Q3 Coll.	6.75 dc	0.25	Ref. to E25	70 K	Neg. to E25
Q3 Base	6.30 dc	0	Ref. to E25	6 K	Neg. to E25
Q3 Emit	5.46 dc	0	Ref. to E25	6 K	Neg. to E25
Q4 Coll.	15.55 dc	0.50	Ref. to E25	1 K	Neg. to E25
Q4 Base	6.90 dc	0	Ref. to E25	3.5 K	Neg. to E25
Q4 Emit.	6.30 dc	0	Ref. to E25	6 K	Neg. to E25
Q5 Coll.	0.17 dc	0	Ref. to E25	1 K	Neg. to E25
Q5 Base	0.77 dc	0	Ref. to E25	3 K	Neg. to E25
Q5 Emit.	0	0	Ref. to E25	0	Neg. to E25
Q6 Coll.	12.01 dc	0	Ref. to E25	3.6 K	Neg. to E25
Q6 Base.	0	0	Ref. to E25	1.1 K	Neg. to E25
Q6 Emit.	0	0	Ref. to E25	9	Neg. to E25
Q7 Coll.	0	0	Ref. to E25	500	Neg. to E25
Q7 Base	18.05 dc	0.40	Ref. to E25	3 K	Neg. to E25
Q7 Emit.	18.05 dc	0.40	Ref. to E25	1 K	Neg. to E25
Q8 Coll.	18.05 dc	0.40	Ref. to E25	3.6 K	Neg. to E25
Q8 Base	0	0	Ref. to E25	6.5 K	Neg. to E25
Q8 Emit.	0	0	Ref. to E25	0	Neg. to E25
Q10 Coll.	0	0	Ref. to E25	300	Neg. to E25
Q10 Base	-12.02 dc	0	Ref. to E25	3 K	Neg. to E25
Q10 Emit	-12.02 dc	0	Ref. to E25	3 K	Neg. to E25
Z1-2	12.52 dc	0.01	Ref. to E25	3.8 K	Neg. to E25
Z1-3	12.01 dc	0	Ref. to E25	3.1 K	Neg. to E25
Z1-4	3.58 dc	0	Ref. to E25	4.2 K	Neg. to E25
Z1-5	3.58 dc	0	Ref. to E25	2.6 K	Neg. to E25
Z1-6	7.17 dc	0	Ref. to E25	3.5 K	Neg. to E25
Z1-7	0	0	Ref. to E25	0	Neg. to E25
Z1-10	13.05 dc	0	Ref. to E25	2.9 K	Neg. to E25
Z1-11	17.80 dc	0.35	Ref. to E25	1 K	Neg. to E25
Z1-12	17.80 dc	0.35	Ref. to E25	1 K	Neg. to E25
Z1-13	14.47 dc	0	Ref. to E25	4.2 K	Neg. to E25

TABLE 3-3. VOLTAGE AND RESISTANCE (CONTINUED)

TERMINAL	Voltage			Resistance	
	Volts	Volts (P-P)	Conditions	(Ohms)	Conditions
Z2-2	+0.44 dc	0.01	Ref. to E25	500	Neg. to E25
Z2-3	0	0	Ref. to E25	0	Neg. to E25
Z2-4	-8.44 dc	0	Ref. to E25	6.1 K	Neg. to E25
Z2-5	-8.45 dc	0	Ref. to E25	6.9 K	Neg. to E25
Z2-6	-4.90 dc	0	Ref. to E25	7.0 K	Neg. to E25
Z2-7	-12.02 dc	0	Ref. to E25	3 K	Neg. to E25
Z210	+0.96 dc	0	Ref. to E25	900	Neg. to E25
Z2-11	+5.40 dc	0.25	Ref. to E25	13 K	Neg. to E25
Z2-12	+5.40 dc	0.25	Ref. to E25	13 K	Neg. to E25
Z2-13	+2.30 dc	0	Ref. to E25	11 K	Neg. to E25
Z3-2	5.59 dc	0	Ref. to E25	6 K	Neg. to E25
Z3-3	5.07 dc	0	Ref. to E25	6 K	Neg. to E25
Z3-4	5.07 dc	0	Ref. to E25	6 K	Neg. to E25
Z3-5	5.07 dc	0	Ref. to E25	4.3 K	Neg. to E25
Z3-6	7.24 dc	0	Ref. to E25	3.5 K	Neg. to E25
Z3-7	0	0	Ref. to E25	0	Neg. to E25
Z3-10	6.88 dc	0.01	Ref. to E25	3.6 K	Neg. to E25
Z3-11	17.95 dc	0.35	Ref. to E25	1 K	Neg. to E25
Z3-12	17.95 dc	0.35	Ref. to E25	1 K	Neg. to E25
Z3-13	8.08 dc	0.01	Ref. to E25	4.7 K	Neg. to E25
Z4-1	17.95 dc	0.35	Ref. to E25	1 K	Neg. to E25
Z4-2	2.50 dc	0	Ref. to E25	3.2 K	Neg. to E25
Z4-3	0	0	Ref. to E25	0	Neg. to E25
Z5-1, 13, and 14	6.68 dc	0.10	Ref. to E25	7.5 K	Neg. to E25
Z5-2	0	0	Ref. to E25		Neg. to E25
Z5-3	17.90 dc	0.35	Ref. to E25	1 K	Neg. to E25
Z5-4, 9	-2.50 dc	0	Ref. to E25	15 K	Neg. to E25
Z5-5, 6, and 10	2.50 dc	0	Ref. to E25	3.2 K	Neg. to E25
Z5-7	2.78 dc	0	Ref. to E25	8.2 K	Neg. to E25
Z5-8	-2.78 dc	0	Ref. to E25	8.2 K	Neg. to E25
Z5-11	2.71 dc	0	Ref. to E25	7.5 K	Neg. to E25
Z5-12	-11.96 dc	0.45	Ref. to E25	2 K	Neg. to E25
Z6-1, 5	-2.50 dc	0	Ref. to E25	15 K	Neg. to E25
Z6-2	0	0	Ref. to E25	13 K	Neg. to E25
Z6-3	0	0	Ref. to E25	5 K	Neg. to E25
Z6-4	17.90 dc	0.35	Ref. to E25	1 K	Neg. to E25
Z6-6	-2.32 dc	0	Ref. to E25	8.5 K	Neg. to E25
Z6-7	-9.70 dc		Ref. to E25	18 K	Neg. to E25
Z6-8	-9.70 dc	0.45	Ref. to E25	3.7 K	Neg. to E25
Z6-9, 13	2.50 dc	0	Ref. to E25	3.2 K	Neg. to E25
Z6-10	2.3 dc	0	Ref. to E25	2 K	Neg. to E25
Z6-11	-11.96 dc	0.45	Ref. to E25	6.7 K	Neg. to E25
Z6-12	2.31 dc	0	Ref. to E25	2 K	Neg. to E25
Z6-14	-9.70 dc	0.45	Ref. to E25	3.2 K	Neg. to E25

Section III. MAINTENANCE PROCEDURES

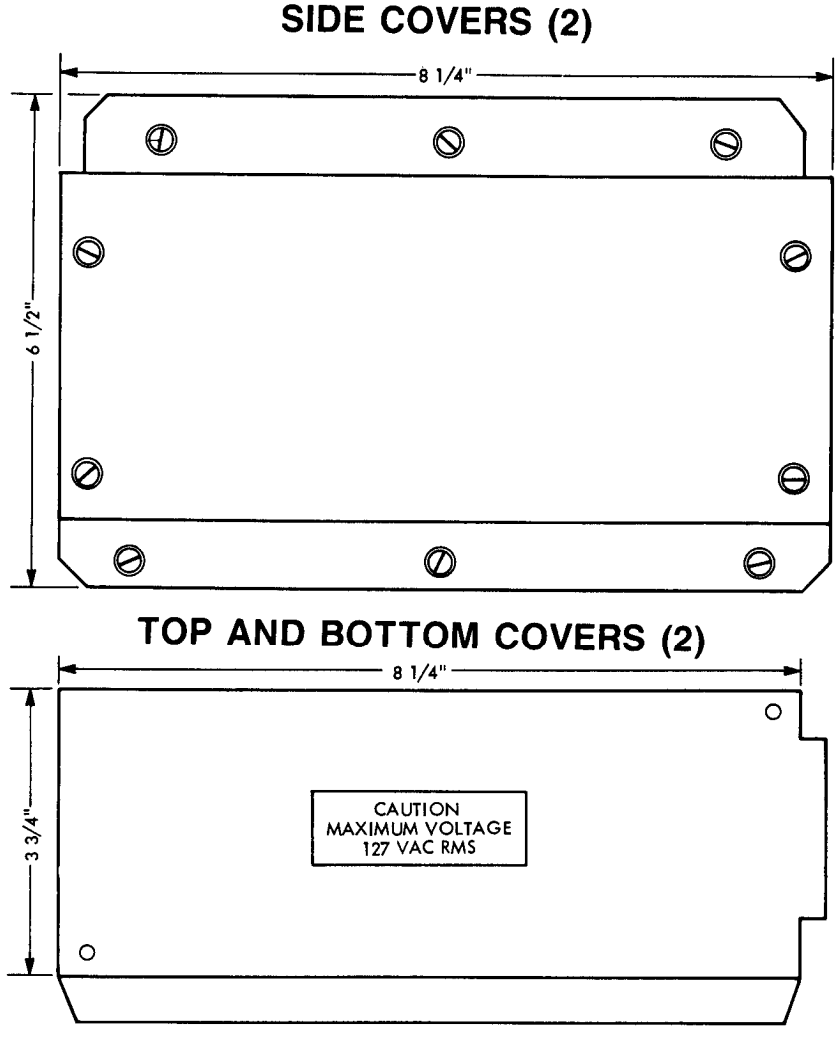
3-7. PARTS REMOVAL AND REPLACEMENT PROCEDURES

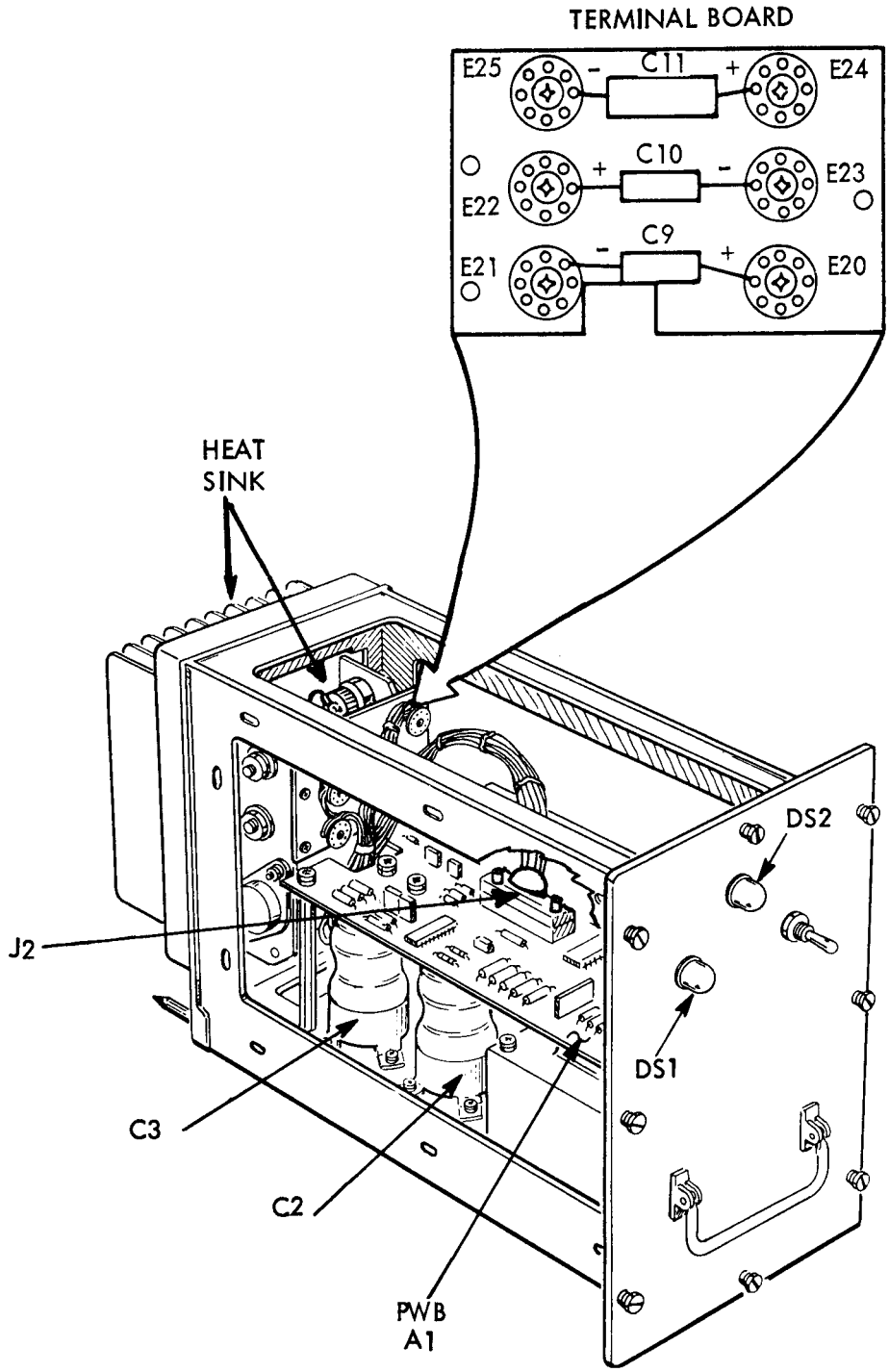
Parts removal and replacement procedures at the general support level are applicable to the Power Supply and the Switch Assembly.

a. Power Supply (20A1)

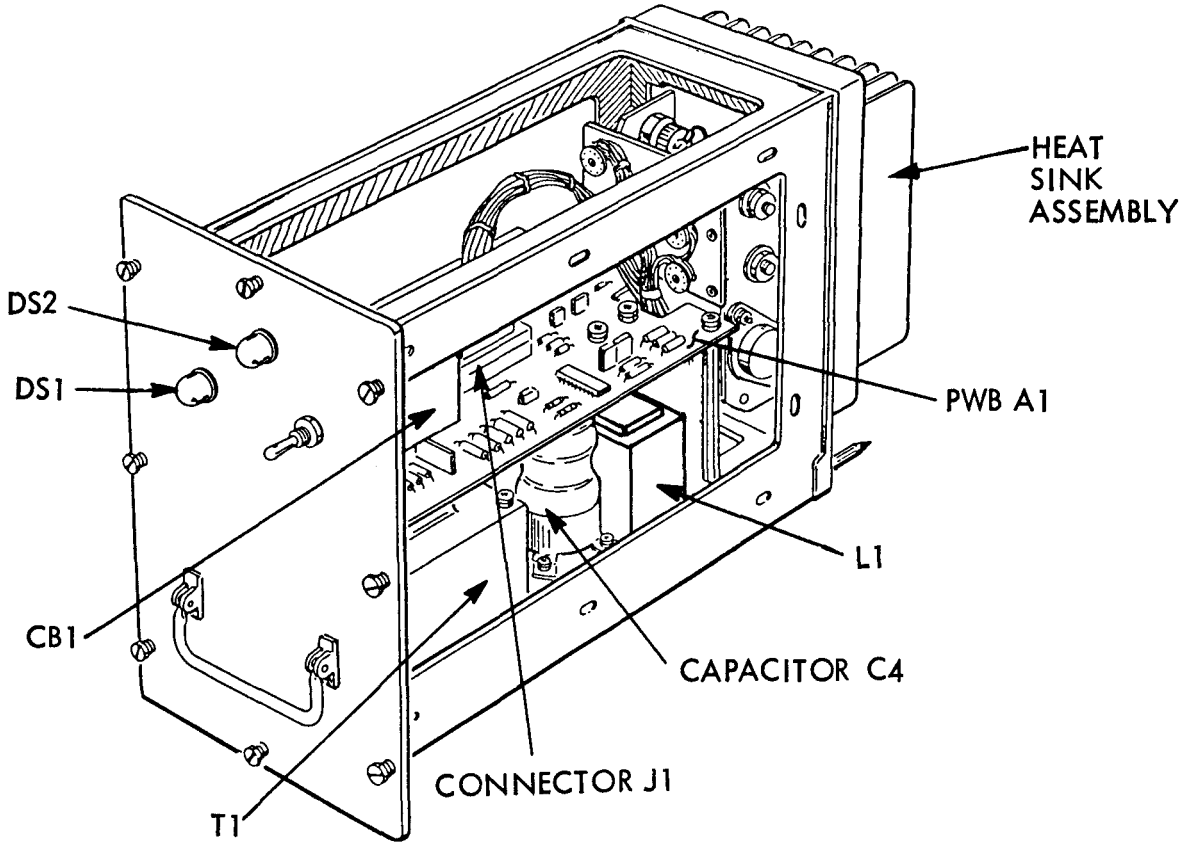
NOTE

To gain access to all components in the power supply, remove the two side covers by loosening the twenty (20) captive screws securing the covers to the chassis. When necessary, the top and bottom covers may then be removed by simply pulling them off the chassis. When maintenance has been completed, first reinstall the top and bottom covers (they are interchangeable) and then the side covers (these are also interchangeable). Tighten all screws.

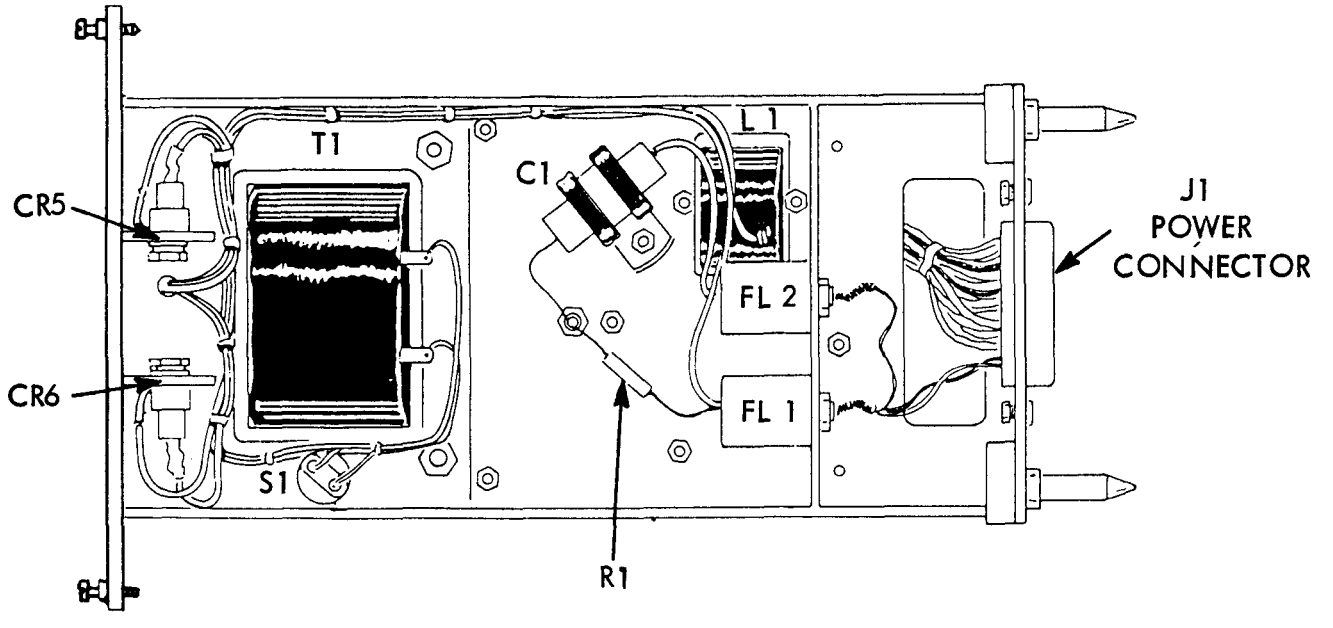



TERMINAL BOARD
E25
C11
E24
E22
C10
E23
E21
C9
E20
HEAT SINK
DS2
J2
DS1
C3
C2
PWB A1

POWER SUPPLY (RIGHT SIDE VIEW)



POWER SUPPLY (BOTTOM VIEW)



CIRCUIT BREAKER CB1, AND LAMPS DS1 AND DS2

REMOVE

- Tag, push back insulating tubing, and unsolder all wires to faulty component.
- For circuit breaker CB1, remove nut on outside of front panel and pull circuit breaker out of its mounting hole from inside of panel. On lamp DS1 or DS2, remove nut on the inside front panel and pull lamp socket out of its mounting hole from outside of panel.

REPLACE

- Install circuit breaker and tighten mounting nut.
- Resolder all wires and push insulating tubing firmly onto terminals.

PRINTED WIRING BOARD (PWB) A1

REMOVE

- Loosen two J2 connector screws alternately, three turns each screw, until screws disengage.
- Remove three stand-off screws and washers, two stand-off nuts and washers, and six capacitor screws and washers.
- Move board back and out through either side of chassis.

REPLACE

- With notch on board facing the rear of the Power Supply, insert board through either side of chassis, and align it with stand-offs. Install (but do not tighten) stand-off washers, screws, and nuts, and capacitor washers and screws. Tighten all screws and nuts.
- Install connector J2 by tightening each screw, alternately, three turns at a time until both screws are tight.

CAPACITORS C2, C3, AND C4

REMOVE

- Remove printed wiring board A1 as described above.
- Loosen clamp screw of faulty capacitors and lift capicator out of clamp.

REPLACE

- Install capacitor in clamp so that mounting holes at top of capicators are approximately aligned with long axis of the Power Supply. Do not tighten clamp screws.
- Reinstall PWB A1 as described above, realigning capicators if necessary, before installing capicator washers and screws. Tighten capacitor clamp screws.

TRANSFORMER T1 AND INDUCTOR L1

REMOVE

- Remove PWB A1 as described above.
- Tag and unsolder all wiring to faulty component; remove its mounting hardware, and lift component from chassis.

REPLACE

- Install component in chassis and resolder all leads.
- Reinstall PWB A1 as described previously.

FILTERS FL1 AND FL2, CAPACITOR C1, SWITCH S1, RESISTOR R1, DIODES CR5 AND CR6, AND CONNECTOR J1

REMOVE

- Tag and unsolder all wires to faulty component.
- Remove mounting hardware. Filters FL1 and FL2 and diodes CR5 and CR6 are mounted with nuts and washers; connectors J1 and capacitor C1 are mounted with nuts, washers, and screws; resistor R1 is terminal mounted, and switch S1 screws into the chassis. To remove S1, clamp its outer edge with a pliers and unscrew it counterclockwise.

REPLACE

- Install component on chassis and resolder all wires. Resistor R1 must be installed close to the chassis with a layer of heat sink compound between it and the chassis. Install diodes CR5 and CR6 with a coating of heat sink compound between the diode side of the assembly and the chassis.

CAPACITORS C9, C10, AND C11

NOTE

These components are located on the terminal board mounted to the heat sink at the rear of the Power Supply.

REMOVE

- Loosen two J2 connector screws alternately, three turns each until screws disengage.
- Remove the four heat sink mounting screws located on four corners of heat sink fin assembly. Pull heat sink assembly out of power supply chassis to gain access to terminal board.
- Unsolder and remove faulty component. Scrape off old heat sink compound from board.

REPLACE

- Apply a layer of heat sink compound (see Appendix B) to board surface. Solder component to its terminals, with body of the component pressed against heat sink compound.
- Push heat sink assembly into Power Supply and replace the four mounting screws.
- Install connector J2 by tightening each screw alternately, three turns each, until both screws are tight.

RESISTORS R6, R10, R18, R29, R30, R57, R67, R76, AND R80, CAPICATORS C14, C16, AND C18, TRANSISTORS Q1, Q2, Q3 AND Q4, DIODES CR8, CR9, AND CR10, AND INDUCTOR L2

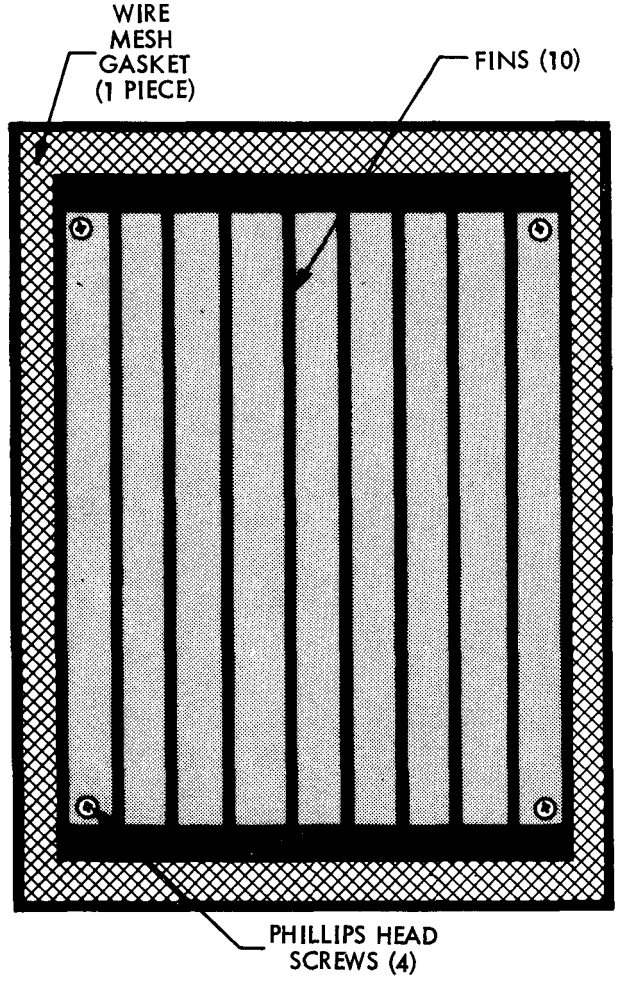
NOTE

These components are all located on the heat sink assembly.

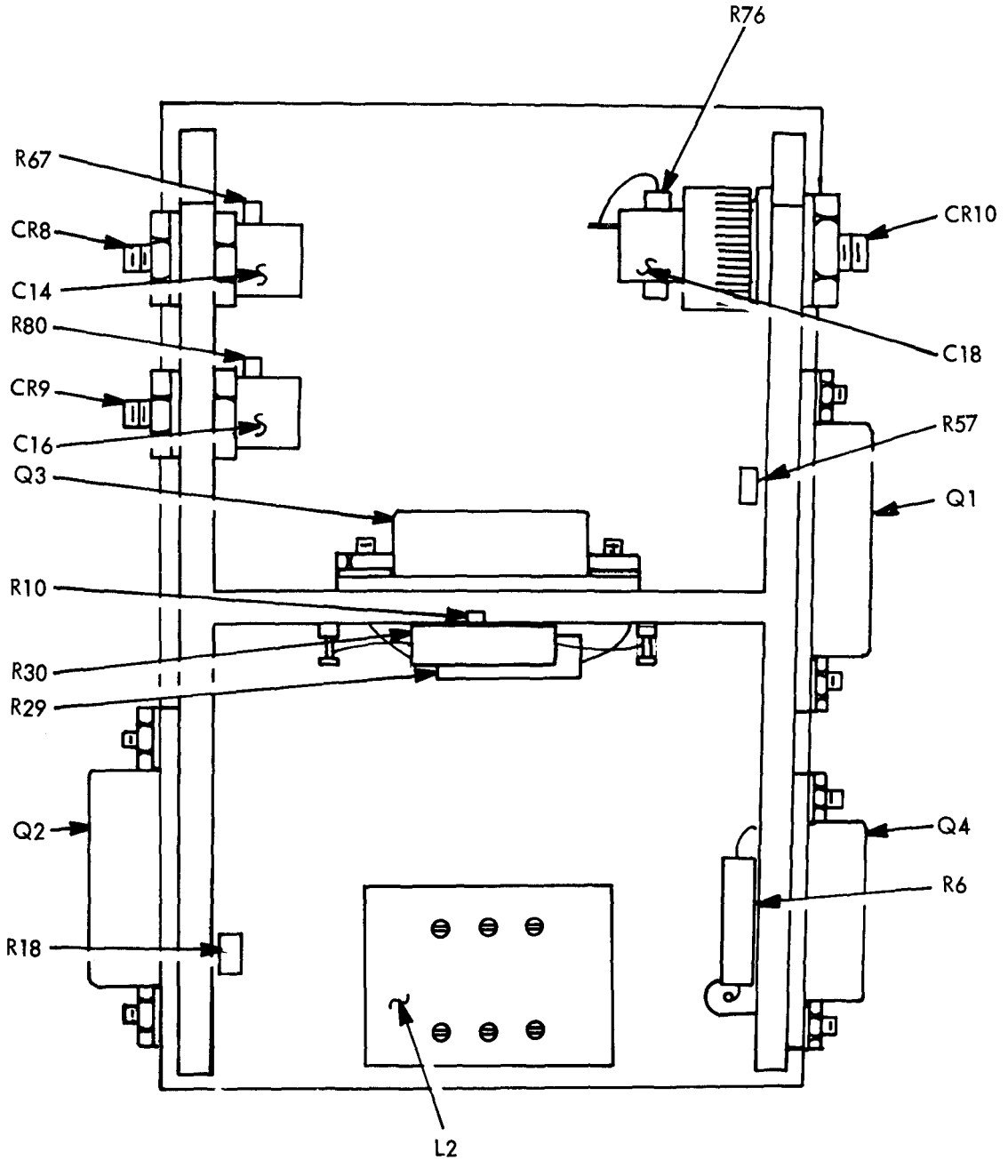
REMOVE

- Loosen two J2 Connector screws alternately, three turns each screw, until the connector disengages.
- Remove four heat sink mounting screws located on four corners of heat sink fin assembly. Pull heat sink assembly out of the Power Supply chassis.

HEAT SINK (EXTERNAL VIEW)



HEATSINK ASSEMBLY (COMPONENT SIDE)



- Remove the three mounting screws and washers holding terminal board to heat sink, and pull board away from heat sink to gain access to components.
- Tag and unsolder all wires to faulty component.
- Remove faulty component: resistors and capacitors are terminal unmounted; transistors are mounted with nuts, washers, and screws; diodes are mounted with nuts and washers; and the inductor is mounted by four screws accessible from the fin side of the heat sink.

REPLACE

- Scrape off all old heat sink compound (see Appendix B). Mount component using heat sink compound where applicable. Resolder all wires to the component.
- Reinstall terminal board to heat sink with the three mounting screws and washers. Reinstall heat sink to chassis with the four mounting screws.
- Install Connector J2 by tightening each screw alternately, three turns each, until both screws are tight.

b. Switch Assembly (20A7)

AUDIBLE ALARM DS4

REMOVE

- Tag and unsolder all wires.
- Unscrew knurled cap on underside of DS4 and remove DS4 from frame.

REPLACE

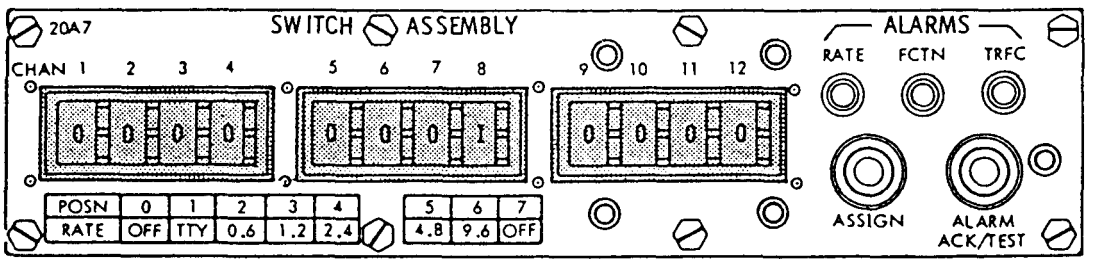
- With cap removed from DS4, insert DS4 in frame and install cap.
- Resolder all wires.

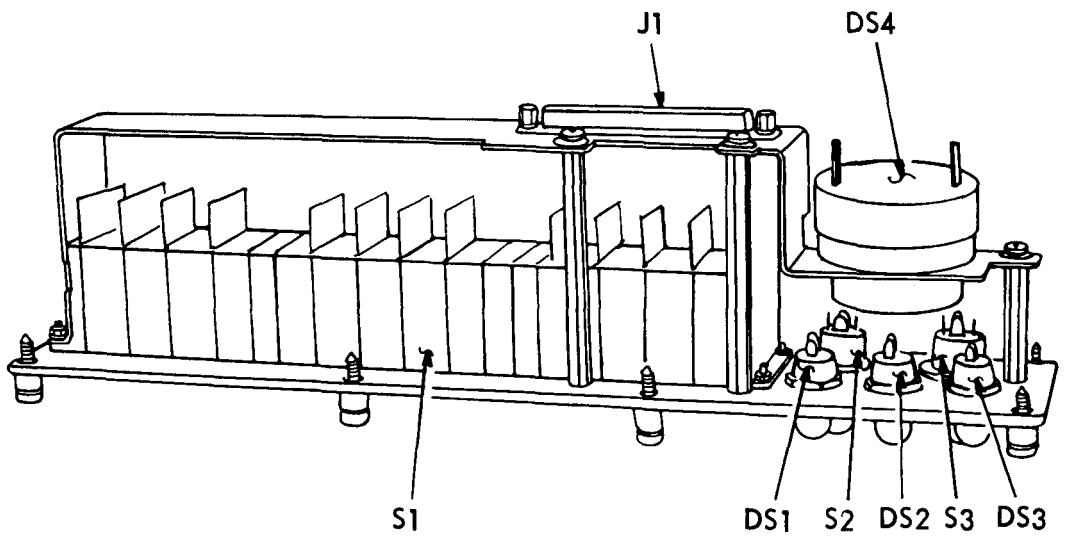
CONNECTOR J1, RATE/MODE ASSEMBLY (S1), SWITCHES S2 AND S3, AND LAMPS DS1, DS2, AND DS3

REMOVE

- Remove five standoff screws and two nuts, washers, and screws holding bracket to front panel. Pull bracket away from frame to expose switches, lamps and underside of connector J1.
- Tag and unsolder all wires from faulty component.

SWITCH ASSEMBLY





- Remove component: connector J1 is mounted to the bracket with two standoff screws, washers, and nuts; Rate/Mode assembly S1 is mounted to the front panel with four screws, nuts and washers (two have already been removed); switches S2 and S3 are mounted to the front panel with nuts and washers on the outside of the panel; and lamps DS1, DS2, and DS3 are mounted to the front panel with nuts and washers on the inside of the panel.

REPLACE

- Install component and tighten mounting hardware.
- Resolder all wires.
- Reinstall bracket and tighten all mounting hardware.

3-8. POWER SUPPLY (20A1) ADJUSTMENT PROCEDURES

Make adjustments after performing maintenance. These procedure determine if the Power Supply has been properly repaired and can be returned to use.

With the power supply setup for test make the following adjustments:

1. Adjust R35 for a +5 Vdc ±50 mV output.
2. Adjust R12 for a +12 Vdc ±240 mV output.
3. Adjust R22 for a -12 Vdc ±240 mV output.

3-9. CABLE HARNESS ASSEMBLY (W1-W5) REPAIR

Cable harness assembly repair consists of replacing connectors, connector contacts, individual wires, and complete harnesses where individual wire replacement is not practical. The following procedures describe the removal and replacement of wires for each of the various connector types. Refer to the following cable diagrams for wire destinations, color coding, and harness dress requirements.

REMOVAL

1. Connector P7
   - Remove two end-mounting screws and straps, loosen clamp screws, and pull connector cover back from connector.
   - Remove wire and contact using extraction/insertion tool M81969/14-02.

2. Connector XA1.

   - Remove wire and contact using extraction/insertion tool M81969/14-02.

3. Connectors P1 through P6

   - Remove wire and contact by pressing on contact locking tab with a suitable pointed tool and pulling the wire and contact out of the connector body.

4. Connectors J1 and J2.

   - Unscrew nut (1) and remove body assembly (8) and insert (7).
   - Unsolder and remove shield (6).
   - Remove dielectric (5), notched insert (10), washer (9), cone dielectric (3), cone (2), and nut (1).
   - Unsolder pin (1) from wire.

5. Connectors J3 through J6

   - Unsolder jam nut and pull grommet back.
   - Unsolder wire from connector pin.

REPLACE

1. Connector P7.

   - Strip wire insulation back 3/16 inch.
   - Using positioner M22520/2-08 and crimp tool M22520/2-01, crimp contact wire.
   - Using extraction/insertion tool M81969/14-02, insert contact in connector socket.
   - Push connector cover up against connector and tighten clamp screws.
   - Reinstall end straps and screws.

2. Connector XA1.

   - Strip wire insulation back 3/16 inch.

- Using positioner M22520/2-08 and crimp tool M22520/2-01, crimp contact to wire.
- Using extraction/insertion tool M81969/14-02, insert contact in connector socket.

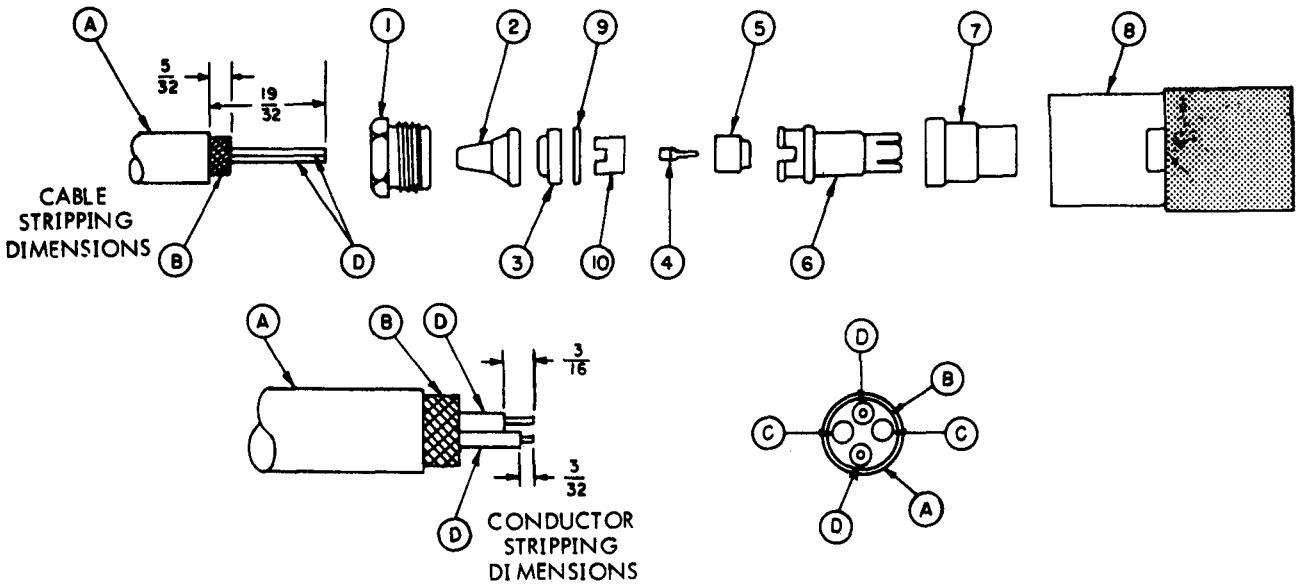
3. Connectors P1 though P6

- Strip wire insulation back 3/16 inch.
- Using crimp tool AMP 90202-2, crimp contact to wire.
- Insert contact in connector socket with locking tab facing outside of connector. Push contact all the way in until it locks in socket.

4. Connectors J1 and J2.

- Place nut (1) on cable.
- Strip outer jacket (A) back 19/32 inch. Strip braid (B) back 14/32 inch.
- Comb out braid and bend outward to allow free entry of cone (2).
- Cut filler (C) out.
- Push cone dielectric (3) into cavity of cone (2).
- Insert cone assembly over conductors (D) and under edge of braid (B). The tapered cone will flair out braid and jacket. Continue to push cone under braid until braid is flush with edge of cone.
- Install insulating washer (9) over the conductors and seat it against cone dielectric (3).

CONNECTORS J1 AND J2 ASSEMBLY DETAILS



1. NUT
2. CONE
3. CONE DIELECTRIC
4. PIN
5. DIELECTRIC
6. SHIELD
7. INSERT
8. BODY ASSY
9. INSULATING WASHER
10. NOTCHED INSERT

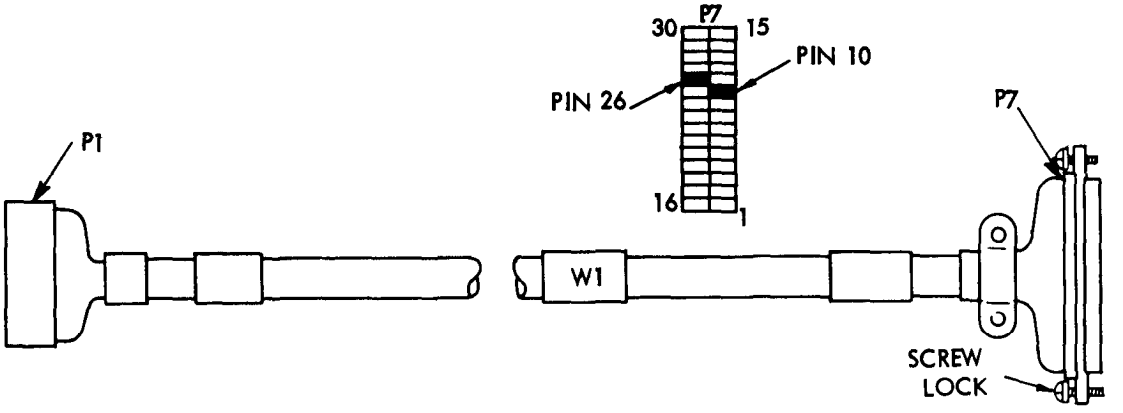
A. OUTER JACKET
B. BRAID
C. FILLER
D. CONDUCTOR

- Cut both conductors (D) 0.35 inch long, measured from surface of insulating washer (9).
- Using digital multimeter, determine which conductor is connected to pin 20 of P2. Strip insulation of this conductor back 0.1 inch. Strip other conductor back 0.2 inch.
- Tin conductor with 0.1 inch stripped insulation.
- Push notched insert (10) over tinned conductor, with other conductor folded at a right angle to allow notched insert (10) to seat flat against insulating washer (9).
- Solder pin (4), seated against notched insert (10), to tinned conductor.
- Slip dielectric (5) over pin (4). Slip shield (6) over the pin assembly and set it against washer (9).
- Wrap the conductor, folded at right angle between the shield ridges and solder, neatly (do not allow solder to extend above ridges).
- Push insert (7) over shield (6), and seat against insulating washer (9).
- Bring nut (1) up onto tapered portion of cable.
- Place connector body assembly (8) over insert (7) and engage nut (1).
- Wrench tighten nut (1) to 30.40 in. lbs. torque.

5. Connectors J3 through J6.

- Strip wire insulation back 3/16 inch (J3, J4, and J5) or 5/16 inch (J6). Tin wire.
- Solder wire to connector pin.
- Push grommet into connector. Screw in and tighten jam nut.

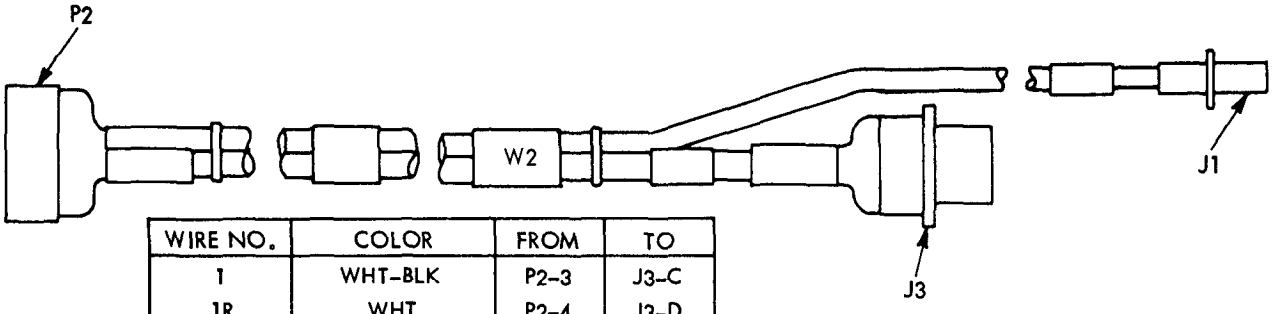
CABLE HARNESS ASSEMBLY W5 WIRE COLOR CODE AND DESTINATIONS



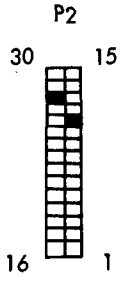
WIRE NO.	COLOR	FROM	TO
1	WHT-BLK-BRN	P1-1	P7-1
2	WHT-BLK-RED	P1-2	P7-2
3	WHT-BLK-ORN	P1-3	P7-3
4	WHT-BLK-YEL	P1-4	P7-4
5	WHT-BLK-GRN	P1-5	P7-5
6	WHT-BLK-BLU	P1-6	P7-6
7	WHT-BLK-VIO	P1-7	P7-7
8	WHT-BLK-GY	P1-8	P7-8
9	WHT-BLK	P1-9	P7-9
11	WHT-BRN	P1-11	P7-11
12	WHT-RED	P1-12	P7-12
13	WHT-BRN-RED	P1-13	P7-13
14	BLK	P1-14	P7-14
15	WHT-ORN	P1-15	P7-15

WIRE NO.	COLOR	FROM	TO
16	BRN	P1-16	P7-16
17	ORN	P1-17	P7-17
18	YEL	P1-18	P7-18
19	BLU	P1-19	P7-19
20	GY	P1-20	P7-20
21	WHT-GY	P1-21	P7-21
22	WHT-BLU	P1-22	P7-22
23	WHT-GRN	P1-23	P7-23
24	WHT-YEL	P1-24	P7-24
25	GRN	P1-25	P7-25
27	VIO	P1-27	P7-27
28	WHT-VIO	P1-28	P7-28
29	WHT	P1-29	P7-29
30	RED	P1-30	P7-30

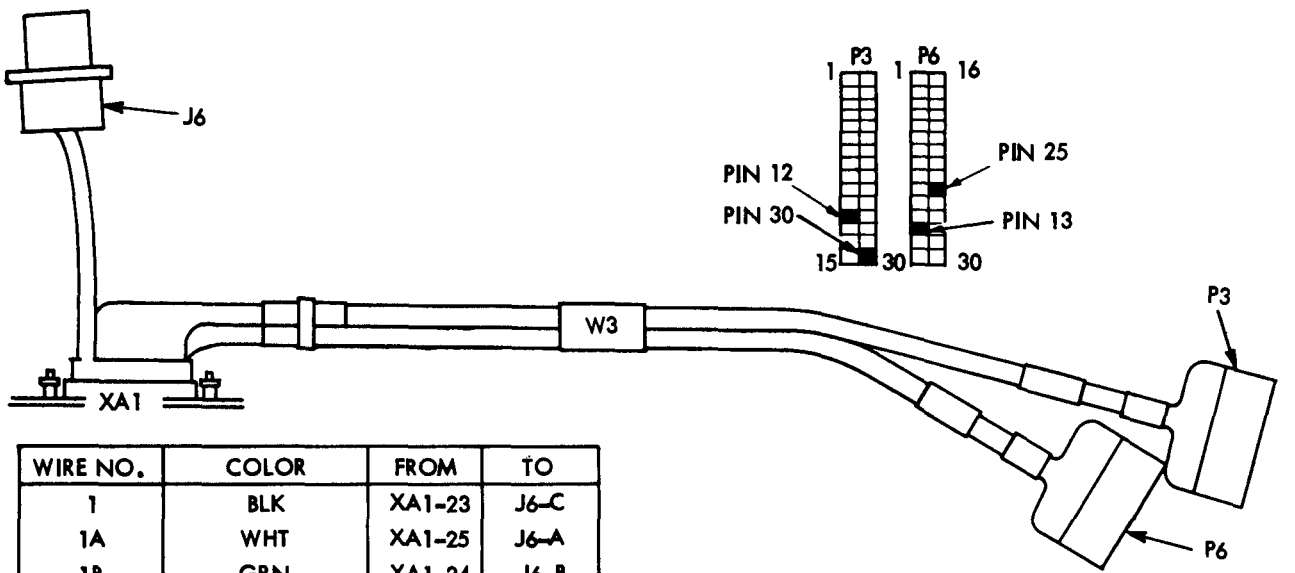
CABLE HARNESS ASSEMBLY W2 WIRE COLOR CODE AND DESTINATIONS



WIRE NO.	COLOR	FROM	TO	
1	WHT-BLK	P2-3	J3-C	
1R	WHT	P2-4	J3-D	
2	WHT-RED	P2-5	J3-A	
2R	WHT	P2-6	J3-B	
3	WHT-GRN	P2-7	J3-L	
3R	WHT	P2-8	J3-M	
4	WHT-BLU	P2-9	J3-J	
4R	WHT	P2-10	J3-K	
5	GRN	P2-26	J3-G	
5R	WHT	P2-12	J3-H	
6	ORN	P2-13	J3-E	
6R	WHT	P2-14	J3-F	
7	YEL	P2-17	J3-R	
7R	WHT	P2-18	J3-S	
8	BLU	P2-27	J3-N	
8R	WHT	P2-29	J3-P	
9	BLK	P2-15	J3-U	
10	WHT-ORN	P2-24	J1-PIN	
10R	WHT	P2-25	J1-RING	BARE STRAND
11	BLK	P2-30	J1-1	



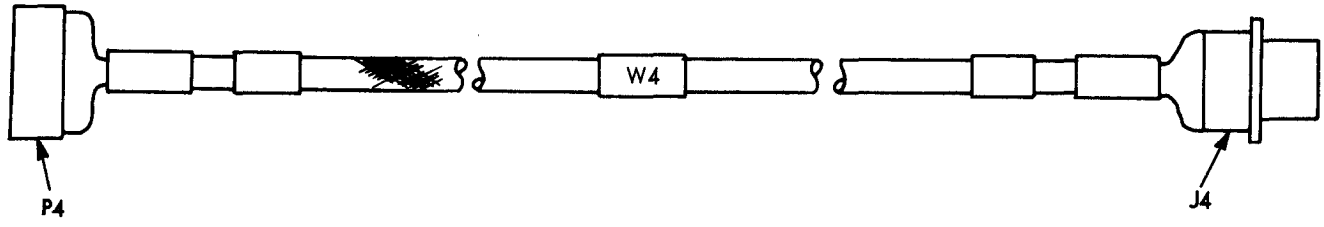
CABLE HARNESS ASSEMBLY W3 WIRE COLOR CODE AND DESTINATIONS

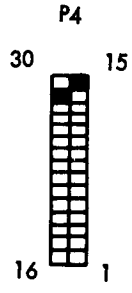


WIRE NO.	COLOR	FROM	TO
1	BLK	XA1-23	J6-C
1A	WHT	XA1-25	J6-A
1B	GRN	XA1-24	J6-B
3	RED	XA1-6	P3-27
3A	WHT	XA1-19	P3-17
3B	BLK	XA1-10	P3-22
4	RED	XA1-7	P3-28
4A	WHT	XA1-20	P3-18
4B	BLK	XA1-22	P3-23
5	RED	XA1-8	P3-29
5A	WHT	XA1-21	P3-19
5B	BLK	XA1-9	P3-24
6	VIO	XA1-1	P6-6
6A	WHT-VIO	XA1-14	P6-1

WIRE NO.	COLOR	FROM	TO
7	VIO	XA1-2	P6-21
7A	WHT-VIO	XA1-15	P6-16
8	VIO	XA1-3	P6-22
8A	WHT-VIO	XA1-16	P6-17
9	VIO	XA1-4	P6-23
9A	WHT-VIO	XA1-17	P6-18
10	VIO	XA1-5	P6-24
10A	WHT-VIO	XA1-18	P6-19
11	BLU	XA1-11	P6-27

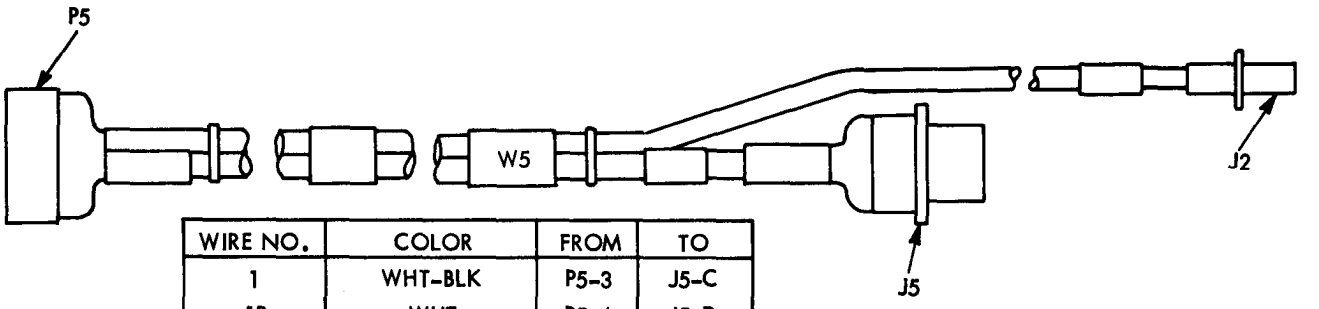
CABLE HARNESS ASSEMBLY W4 WIRE COLOR CODE AND DESTINATIONS



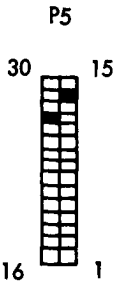


WIRE NO.	COLOR	FROM	TO
1	WHT-BLK	P4-3	J4-C
1R	WHT	P4-4	J4-D
2	WHT-RED	P4-5	J4-A
2R	WHT	P4-6	J4-B
3	WHT-GRN	P4-7	J4-L
3R	WHT	P4-8	J4-M
4	WHT-BLU	P4-9	J4-J
4R	WHT	P4-10	J4-K
5	GRN	P4-11	J4-G
5R	WHT	P4-12	J4-H
6	ORN	P4-13	J4-E
6R	WHT	P4-14	J4-F
7	YEL	P4-17	J4-R
7R	WHT	P4-18	J4-S
8	BLU	P4-27	J4-N
8R	WHT	P4-28	J4-P
9	BLK	P4-16	J4-U

CABLE HARNESS ASSEMBLY W5 WIRE COLOR CODE AND DESTINATIONS



WIRE NO.	COLOR	FROM	TO	
1	WHT-BLK	P5-3	J5-C	
1R	WHT	P5-4	J5-D	
2	WHT-RED	P5-5	J5-A	
2R	WHT	P5-6	J5-B	
3	WHT-GRN	P5-7	J5-L	
3R	WHT	P5-8	J5-M	
4	WHT-BLU	P5-9	J5-J	
4R	WHT	P5-10	J5-K	
5	GRN	P5-11	J5-G	
5R	WHT	P5-12	J5-H	
6	ORN	P5-13	J5-E	
6R	WHT	P5-15	J5-F	
7	YEL	P5-17	J5-R	
7R	WHT	P5-18	J5-S	
8	BLU	P5-26	J5-N	
8R	WHT	P5-28	J5-P	
9	BLK	P5-1	J5-U	
10	WHT-ORN	P5-19	J2-PIN	
10R	WHT	P5-20	J2-RING	BARE STRAND
11	BLK	P5-16	J2	



APPENDIX A
REFERENCES

A-1. PUBLICATION INDEXES

The following index should be consulted frequently for latest changes or revisions of references given in this appendix and for new publications relating to material covered in this manual.

Consolidated Index of Army Publications and Blank Forms . . . . . DA Pam 310-1

The Army Maintenance Management System (TAMMS) . . . . . DA Pam 738-750

Index of Modification Work Orders . . . . DA Pam 750-10

A-2. FORMS AND RECORDS

The following forms and records pertain to this material.

Discrepancy in Shipment Report . . . . SF 361

Report of Discrepancy (ROD) . . . . SF 364

Quality Deficiency Report . . . . . SF 368

Recommended Changes to Publications and Blank Forms . . . . . DA Form 2028

A-3. OTHER PUBLICATIONS

The following publications contain information pertinent to this material and associated equipment.

Painting and Preservation of Supplies Available for Field Use for Electronics Command Equipment . . . . . SB 1l-573

Preservation, Packaging, Packing and Marking Materials, Supplies and Equipment Used by the Army . . . . . SB 38-100

Operator's and Organizational Maintenance Manual: Multiplexer Time Division, Digital TD-1069/G (NSN 5805-01-028-8425) . . . . **TM 11-5805-638-12**

Hand Receipt Covering Contents of Components of End Item (CDEI), Basic Issue Items (BII), and Additional Authorization List (AAL) for Multiplexer, Time Division, Digital TD-1069/G (NSN 5805-01-028-8425) . . . . . **TM 11-5805-638-12-HR**

Organizational Maintenance Repair Parts and Special Tools List for Multiplexer, Time Division, Digital TD-1069/G (NSN 5805-01-028-8425) . . . . **TM 11-5805-638-20P**

APPENDIX A (CONTINUED)

Direct Support and General Support Repair Parts
and Special Tools List for Multiplexer,
Time Division Digital TD-1069/G . . . . . TM 11-5805-638-34P

Administrative Storage of Equipment . . . . . TM 740-90-1

Procedures for Destruction of Electronics Materiel to
Prevent Enemy Use (Electronics Command) . . . . . **TM 750-244-2**

First Aid for Soldiers . . . . . FM 21-11

APPENDIX B

EXPENDABLE SUPPLIES AND MATERIALS LISTS

Section I. INTRODUCTION

B-1. SCOPE

This appendix lists expendable supplies and materials you will need to operate and maintain the TD-1069/G. These items are authorizes to you by CTA 50-970, Expandable Items (Except Medical, Class V, Repairs Parts, and Heraldic Items).

B-2. EXPLANATION OF COLUMNS

a. Column 1 - Item Number. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material (e.g., “Use cleaning compound, item 1, App. E").

b. Column 2 - Level. This column identifies the lowest level of maintenance that requires the listed item.

C-Operator/Crew
O-Organizational
F-Direct Support
H-General Support

c. Column 3 - National Stock Number. This is the National Stock number assigned to the item; use it to request or requisition the item.

d. Column 4 - Description. Indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the part number followed by the Federal Supply Code for Manufacturer (FSCM) in parentheses, if applicable.

e. Column 5 - Unit of Measure (UM). Indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea. in. pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy your requirements.

Section II. EXPENDABLE SUPPLIES AND MATERIALS LIST

(1) ITEM NO.	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION PART NO. AND FSCM	(5) UNIT OF MEAS
1	H		3-foot lengths of No. 24 AWG single-conductor Stranded cable	FT
2	H		Connector M24308/4-3 (Female)	
3	H		Heat Sink Compound	OZ
4	F,H	6850-00-105-3084	Cleaning Compound (TRICHLOROTRIFLUOROETHANE)	OZ
5	F,H	7920-00-924-5700	Cleaning Cloth	YD

GLOSSARY
ABBREVIATIONS

ac	Alternating current
ACA	Automatic Channel Assignment
ACK	Acknowledge
ALM	Alarm
BITE	Built-in Test Equipment
bps	Bits per second
CDP	Conditioned Diphase
CHAN	Channel
CHFN	Channel fail LED indicator drive signal
CHSN	Channel select, one of 12 digital lines (lower case n for FSK)
CHSSN	Channel select, switch strobe not
CLK	Clock timing and distribution signal
CMOS	Complementary metal-oxide semi-conductor
CTR	Counter
DATIN	Digital Data Input signal
DATOUT	Digital Data Output signal
dBm	Decibels milliwatt
dc	Direct Current
DCPG	Digital Clock Pulse Generator
DELCLK	66.7 Hz clock, when HICLK and LOCLK are in Phase
DEMOD	Demodulation
DEMUX	Demultiplex

ABBREVIATIONS (CONTINUED)

ELASTORE	Elastic Store
EMI	Electromagnetic Interference
FCTN	Functional
FM	Frequency Modulation
FSK	Frequency Shift Keying
FSKT	Frequency Shift Keying timing
HICLK	High Clock Frequency
Hz	Hertz
J	Jack or electrical receptacle with female contacts
kb/s	Kilobits per second
kHz	Kilohertz
km	Kilometers
LSB	Least Significant Bit
LED	Light Emitting Diode
LOCLK	Low Clock Frequency
LSTTL	Large Scale Transistor-to-Transistor Logic
mHz	Megahertz
MSB	Most Significant Bit
MUX	Multiplex
mV	Millivolt(s)
mW	Milliwatt(s)
NRZ	Nonreturn-to-zero
NC	Not connected
OH	Overhead
PLL	Phase Locked Loop
PMBU, PMBV, PMBW	Programmable Mode Bus; 3-wire binary coded switch bus (U/V/W)
PMCS	Preventive Maintenance Check/ Service

ABBREVIATIONS (CONTINUED)

PWB	Printed Wiring board e.g. module
PWR	Power
Q	Transistor designator
RAM	Random Access Memory
RCV	Receive
RDX	Read Data Transmit
ROD	Report of Discrepancy
RSTB	Reset BITE
RSTROBE	Receive Strobe Timing signal
S	Switch designation
SFC	Subframe Counter
STBR	Strobe Receiver
STBX	Strobe Transmit
TAMMS	The Army Maintenance Management System
TFCF	Traffic Fault
TMDE	Test, Maintenance, Diagnostic Equipment
TRFC	Traffic
TSC	Time Slot Counter
TTY	Teletype
U	Integrated Circuit component designator
Vac	Volts alternating current
VCO	Voltage Controlled Oscillator
WDR	Write Data Receive
XCDP	Transmit Conditioned Diphase
XMIT	Transmit

GLOSSARY

BAUD - Unit of signaling speed derived from the duration of the shortest code element. Speed in bauds is the number of code elements per second.

BIT - Abbreviation for Binary Digit. A unit of information equal to one binary decision.

BYTE - Number of bits comprising a data word.

CONDITIONED DIPHASE - A format used in digital data transmission.

CLOCK - A reference source of timing information for a machine or system.

DEMULTIPLEX - The process of separating two or more signals previously combined by a compatible multiplexer.

RESTUFFING - The process of removing the stuffed slots to restore data to its original frequency (see STUFFING below).

DUPLEX CIRCUIT - A communication circuit that can simultaneously transmit and receive.

FAULT - A reproducible malfunction; i.e. a malfunction that occurs consistently under the same circumstances.

FREQUENCY SHIFT KEYING - A form of frequency modulation in which the modulating wave shifts the output frequency between predetermined values and the output wave has no phase discontinuity.

MARK - In telegraphy, a closed circuit condition. Equivalent to a binary one.

MIDFRAME - A portion of the data stream (160 bits). Sixty-four (64) midframes equals one multiframe.

MULTIPLEX - The process of combining two or more signals so that they can be transmitted on a single channel.

SPACE - In telegraphy, an open circuit condition. Equivalent to a binary zero.

STROBE - A sample pulse used to gate the output of a memory sense amplifier into a trigger in a register.

STUFFING - The process of adding extra time slots to incoming bit streams to raise their bit rates to a fixed multiplexing rate.

INDEX

INDEX (CONTINUED)

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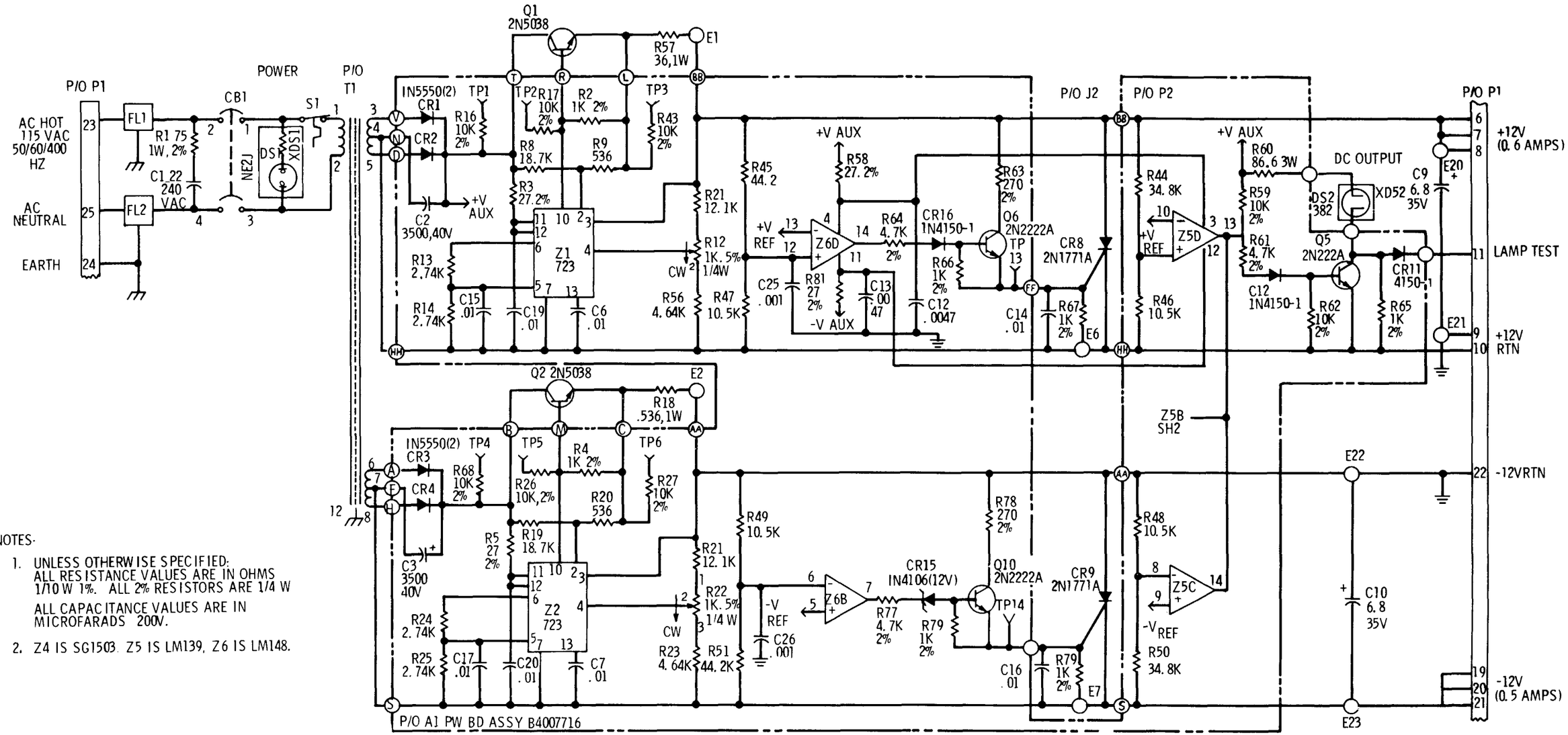
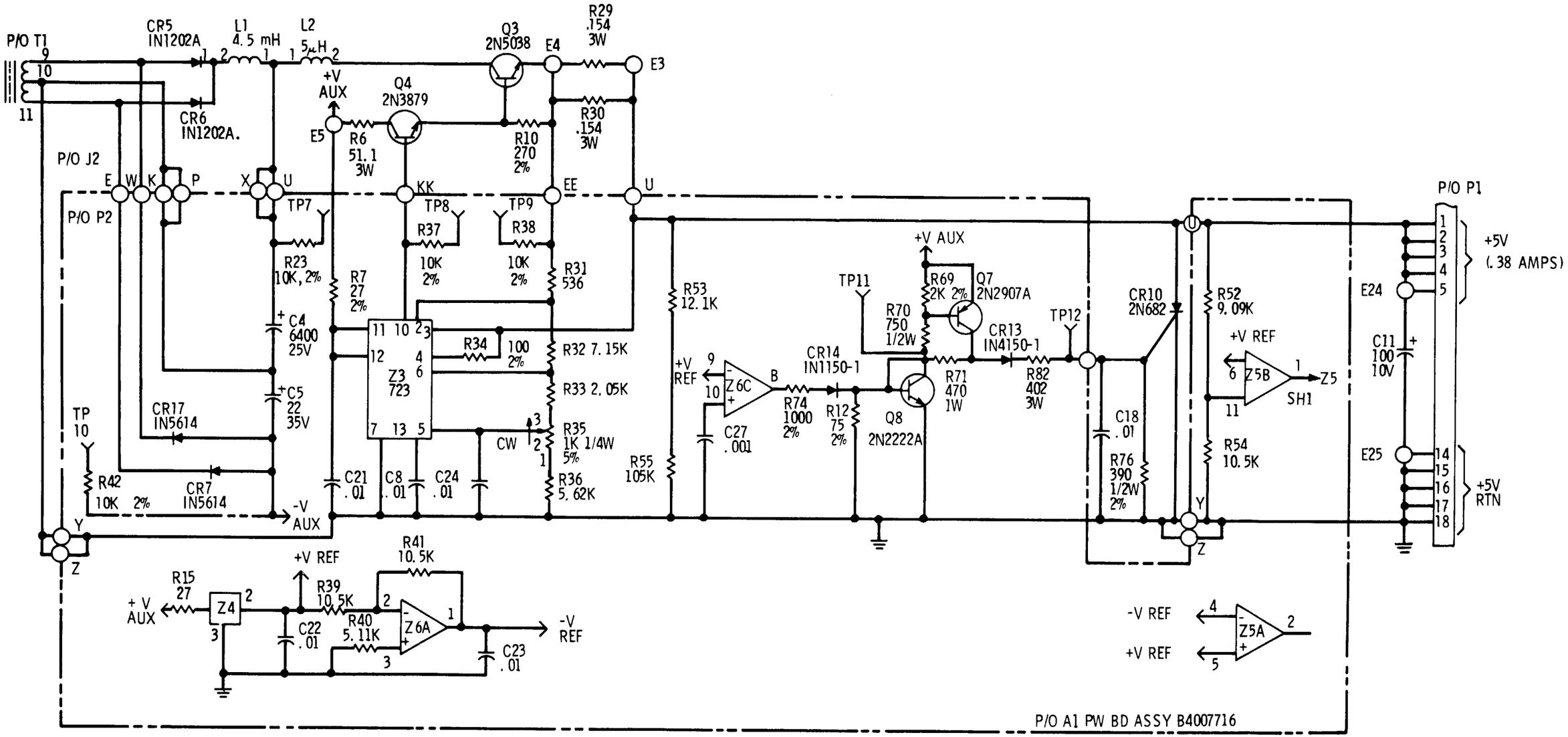


NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS 1/10 W 1%. ALL 2% RESISTORS ARE 1/4 W
   ALL CAPACITANCE VALUES ARE IN MICROFARADS 200V.
2. Z4 IS SG1503. Z5 IS LM139, Z6 IS LM148.

POWER SUPPLY SCHEMATIC DIAGRAM (SHEET 1 OF 2)



POWER SUPPLY
SCHEMATIC DIAGRAM
(SHEET 2 OF 2)

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