

TM 11-5805-367-35/3

DEPARTMENT OF THE ARMY TECHNICAL MANUAL

DS, GS, AND DEPOT MAINTENANCE MANUAL

MULTIPLEXERS

TD-352/U

AND TD-353/U

This copy is a reprint which includes current
pages from Changes 1 through 5.

HEADQUARTERS, DEPARTMENT OF THE ARMY
14 FEBRUARY 1967

WARNING

Be careful when working on the 115-volt ac line connections. Serious injury or death may result from contact with these points.

DON'T TAKE CHANCES!

CHANGE

No.5

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 1 April 1987

**DS,GS, AND DEPOT MAINTENANCE MANUAL
MULTIPLEXERS TD-352/U (NSN 5805-00-900-8199)
AND TD-353/U (NSN 5805-00-900-9153)**

TM 11-5805-367-35/3, 14 February 1967, is changed as follows:

1. Remove old pages and insert new pages as indicated below. New or changed material is indicated by a vertical bar in the margin of the page. Added or revised illustrations are indicated by a vertical bar adjacent to the identification number.

<i>Remove pages</i>	<i>Insert pages</i>
i and i	i and ii
iii through vi.....	iii through vi
1-1/(1-2 blank)	1-1/(1-2 blank)
3-13/(3-14 blank)	3-13/(3-14 blank)
6-1 and 6-2	6-1 and 6-2
A-1 and A-2	A-1 and A-2
None.....	Figure FO 6-45.1
None.....	Figure FO 6-53.1
Figure FO 6-59	Figure FO 6-59

2. File this change sheet in the front of the publication for reference purposes.

This publication is required for official use or for administrative or for operational purposes only. Distribution is limited to US Government Agencies. Other requests for this document must be referred to Commander, US Army Communications-Electronics Command and Fort Monmouth,ATTN: AMSEL-ME-P, Fort Monmouth, NJ 07703-5000.

By Order of the Secretary of the Army:

JOHN A. WICKHAM, JR.
General, United States Army
Chief of Staff

Official:

R.L. DILWORTH
Brigadier General, United States Army
The Adjutant General

DISTRIBUTION:

To be distributed in accordance with DA Form 12-51 literature requirements for TD-202/U, TD-203/U, TD-206/U, TD-352/U, and TD-353.

CHANGE

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 3 February 1984

No.4

**DS, GS, AND DEPOT MAINTENANCE MANUAL
MULTIPLEXERS TD-352/U (NSN 5805-00-900-8199)
AND TD-353/U (5805-00-985-9153)**

TM 11-5805-367-35/3, 14 February 1967, is changed as follows:

1. New or changed material is indicated by a vertical bar in the margin.
2. A new or changed illustration is indicated by a vertical bar next to the figure number.
3. Remove old pages and insert new pages as indicated below.

Remove pages

Insert pages

i and ii	i, ii and ii.1/(ii.2 blank)
1-1	1-1/(1-2 blank)
2-29 and 2-30.....	2-29 and 2-30
2-33 and 2-34.....	2-33 and 2-34
3-11 and 3-12.....	3-11 and 3-12
4-3 and 4-4.....	4-3 and 4-4
4-91 through 4-94.....	4-91 through 4-94
5-1 and 5-2.....	5-1 and 5-2
5-5 through 5-12.....	5-5 through 5-12.3/(5-12.4 blank)
5-23 and 5-24.....	5-23 and 5-24
A-1	A-1/(A-2 blank)

4. File this change in front of the publication for reference purposes.

By Order of the Secretary of the Army:

JOHN A. WICKHAM JR.
General, United States Army
Chief of Staff

Official:

ROBERT M. JOYCE
Major General, United States Army
The Adjutant General

DISTRIBUTION:

To be distributed in accordance with DA Form 12-51C requirements for TD-352/U and TD-353/U.

**DS, GS, AND DEPOT MAINTENANCE MANUAL
 MULTIPLEXERS TD-352/U (NSN 5805-00-900-8199)
 AND TD-353/U (5805-00-985-9153)**

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5000. A reply will be sent direct to you

Chapter	1. INTRODUCTION	Paragraph	Page
	Scope.....	1-1	1-1
	Consolidated index of Army publications and blank forms	1-2	1-1
	Maintenance forms, records and reports.....	1-3	1-1
	Deleted.....	1-4	1-1
	Reporting equipment improvement recommendations (EIR)	1-5	1-1
	Differences between semiconductor subassemblies	1-6	1-1
Chapter	2. FUNCTIONING		
Section	I. Block Diagram Analysis, Multiplexer TD-352/U		
	General	2-1	2-1
	Transmit circuits for TD-352/U.....	2-2	2-1
	Receive circuits for TD-352/U.....	2-3	2-2
	Monitoring and alarm circuits for TD-352/U	2-4	2-3
	Fault locator circuits for TD-352/U	2-5	2-4
	Power supply circuits for TD-352/U.....	2-6	2-4
	II. Block Diagram Analysis, Multiplexer TD-353/U		
	General	2-7	2-4
	Transmit circuits for TD 353/U	2-8	2-4
	Receive circuits for TD-353/U.....	2-9	2-8
	Monitoring and alarm circuits for TD-353/U	2-10	2-10
	Fault locator circuits for TD 353/U	2-11	2-10
	Power supply circuits for TD-3532U.....	2-12	2-10
	III. Module Schematic Analysis		
	Gate module 01.....	2-13	2-10
	Sampler module 08	2-14	2-13
	Flip flop module 09.....	2-15	2-14
	NAND gate module 11.....	2-16	2-14
	Emitter follower module 15	2-17	2-15
	Matrix module 16.....	2-18	2-15
	Matrix module 17.....	2-19	2-19
	Flip flop module 18.....	2-20	2-19
	Oscillator module 22.....	2-21	2-19
	Gate module 23.....	2-22	2-21
	Clamping flip flop module 25	2-23	2-21
	Pulse shaper module 30.....	2-24	2-22
	Amplifier module 31	2-25	2-23

	Paragraph	Page
Amplifier module 32	2-26	2-24
Pulse amplifier module 33.....	2-27	2-24
Gate module 35	2-28	2-25
Detector module 36.....	2-29	2-26
Sampler module 37.....	2-30	2-26
Sampler module 38.....	2-31	2-26
Decision circuit module 42	2-32	2-37
IV. Panel Schematic Analysis		
Regulated power supply panel 1A1/2A1.....	2-33	2-29
Double modem panel.1A2/2A2	2-34	2-38
Pen output circuits, panel 1A3/2A3	2-35	2-40
Coder timing (h.t.), panel 1A5	2-36	2-41
Coder timing (m.t.), panel 2A5	2-37	2-42
Coder circuits, panel 1A6/2A6.....	2-38	2-43
Pam reshaper (hits, panel 1A7.....	2-39	2-46
Coder timing and Pam reshaper circuits, panel 2A7	2-40	2-50
Transmit timing No.1, panel 1A8	2-41	2-52
Transmit timing No.1, panel 2A8	2-42	2-56
Transmit timing No.2, panel 1A9	2-43	2-61
Transmit timing No.2, panel 2A9	2-44	2-63
Transmit timing No.3/receive timing No.2, panel 1A10	2-45	2-64
Transmit timing No.3/receive timing No.2, panel 2A10	2-46	2-67
Noise generator, panel 1A11/2A11.....	2-47	2-67
Receive input and framing, panel 1A12/2A12	2-48	2-68
Receive timing No.1, panel 1A13	2-49	2-71
Receive timing No.1, panel 2A13	2-50	2-74
Decoder No.1, panel 1A14/2A14.....	2-51	2-78
Decoder No.2, panel 1A15.....	2-52	2-80
Decoder No.2, panel 2A15	2-53	2-82
Monitoring and alarm, panel 1A16/2A16	2-54	2-84
Transmit fault locator, panel 1A17	2-55	2-86
Transmit fault locator, panel 2A17.....	2-56	2-87
Receive fault locator, panel 1A18	2-57	2-88
Receive fault locator, panel 2A18	2-58	2-89
Unregulated power supply, panel 1A19/2A19.....	2-59	2-90
Chapter 3. DIRECT SUPPORT MAINTENANCE		
Section I. Troubleshooting at Direct Support		
General.....	3-1	3-1
Use of troubleshooting charts.....	3-2	3-1
Continuity checks.....	3-3	3-1
Mechanical maintenance	3-4	3-2
Test equipment, tools, and materials required.....	3-5	3-2
Multiplexer TD-352/U troubleshooting procedure.....	3-6	3-2
Multiplexer TD-353/U troubleshooting procedure.....	3-7	3-6
II. Alignment		
General.....	3-8	3-10
Switch settings and preliminary procedures.....	3-9	3-11
Preliminary coder adjustment (panel 1A6/2A6)	3-10	3-11
Decoder alignment (panel 1A 15 or 2A 15).....	3-11	3-11
Multiplexer TD-352/U pam level adjustment (panels 1A2/2A2 and 1A6/2A6).....	3-12	3-12
Multiplexer TD-353/U pam level adjustment(panels 1A1/2A1,1A6/2A6,and 1A7) ...	3-13	3-12
Final decoder alignment (panel 1A15 or 2A15).....	3-14	3-13
Chapter 4. GENERAL SUPPORT MAINTENANCE		
Section I. Introduction		
Scope of general support maintenance procedures.....	4-1	4-1

	Paragraph	Page
Organization of troubleshooting procedures	4-2	4-1
Use of troubleshooting charts.....	4-3	4-1
Use of waveforms	4-4	4-2
Test equipment and tools required	4-5	4-2
II. Troubleshooting at General Support		
Panel 1A1/2A1, troubleshooting	4-6	4-2
Panel 1A2/2A2, troubleshooting	4-7	4-8
Panel 1A3/2A2, troubleshooting	4-8	4-11
Panel 1A5, troubleshooting	4-9	4-13
Panel 2A5, troubleshooting	4-10	4-16
Panel 1A6/2A6. troubleshooting	4-11	4-18
Panel 1A7, troubleshooting	4-12	4-24
Panel 2AT, troubleshooting.....	4-13	4-26
Panel 1A8, troubleshooting.....	4-14	4-30
Panel 2A8, troubleshooting.....	4-15	4-33
Panel 1A9, troubleshooting.....	4-16	4-38
Panel 2A9, troubleshooting	4-17	4-40

	Paragraph	Page
Panel 1A10, troubleshooting	4-18	4-42
Panel 2A10, troubleshooting	4-19	4-48
Panel 1A11/2A11 troubleshooting.....	4-20	4-53
Panel 1A12/2A12, troubleshooting.....	4-21	4-54
Panel 1A13, troubleshooting	4-22	4-57
Panel 2A13, troubleshooting	4-23	4-65
Panel 1A14/2A14, troubleshooting.....	4-24	4-70
Panel 1A15, troubleshooting	4-25	4-75
Panel 2A15, troubleshooting	4-26	4-77
Panel 1A16/2A16, troubleshooting.....	4-27	4-78
Panel 1A17, troubleshooting	4-28	4-80
Panel 2A17, troubleshooting	4-29	4-84
Panel 1A18, troubleshooting	4-30	4-88
Panel 2A18, troubleshooting	4-31	4-92
Panel 1A19/2A19, troubleshooting.....	4-32	4-96
III. Alignment		
General	4-33	4-98
Panel 1A1/2A1, - 5.2 volt regulated output voltage adjustment	4-34	4-98
Panel 1A6/2A6, capacitor C1 adjustment.....	4-35	4-98
Chapter 5. GENERAL SUPPORT TESTING PROCEDURES		
General	5-1	5-1
Test equipment, materials, and other equipment	5-2	5-1
Modification work orders	5-3	5-1
Physical tests and inspection	5-4	5-2
Performance tests (TD-352/U)	5-5	5-5
Summary of performance standard (TD-352/U)	5-6	5-13
Performance tests (TD-353/U)	5-7	5-17
Summary of performance standard (TD-353/U)	5-8	5-25
6. DEPOT OVERHAUL STANDARDS		
Applicability of depot overhaul standards	6-1	6-1
Deleted	6-2	6-1
Deleted	6-3	6-1
APPENDIX A REFERENCES		A-1

LIST OF ILLUSTRATIONS

Fig.#	Title	Page
2-1	Multiplexer TD.352/U transmit fault locator circuits, block diagram	2-5
2-2	Multiplexer TD-352/U receive fault locator circuits, block diagram	2-6
2-3	Multiplexers TD.352/U and TD.353/U power supply circuits, block diagram	2-7
2-4	Multiplexer TD-353/U transmit fault locator circuits, block diagram	2-11
2-5	Multiplexer TD-353/U receive fault locator circuits, block diagram	2-12
2-6	Gate module 01, schematic diagram	2-13
2-7	Sampler module 08, schematic diagram	2-14
2-8	Flip-flop module 09, schematic diagram	2-15
2-9	NAND gate module 11, schematic diagram	2-16
2-10	Emitter-follower module 15, schematic diagram	2-17
2-11	Matrix module 16, schematic diagram	2-18
2-12	Matrix module 17, schematic diagram	2-20
2-13	Matrix modules 16 and 17, AND gate form	2-21
2-14	Flip-flop module 18, schematic diagram	2-22
2-15	Oscillator module 22, schematic diagram.....	2-23
2-16	Gate module 23, schematic diagram	2-24
2-17	Clamping flip-flop module 25 or 125, schematic diagram	2-25
2-18	Clamping flip-flop module 25, external circuitry for one-and two-terminal outputs	2-26

LIST OF ILLUSTRATIONS-Continued

Fig.#	Title	Page
2-19	Pulse shaper module 30, schematic diagram.....	2-27
2-20	Audio preamplifier module 31, schematic diagram	2-28
2-21	Audio amplifier module 32, schematic diagram	2-29
2-22	Pulse amplifier module 33, schematic diagram	2-30
2-23	Dual AND gate module 35, schematic diagram	2-31
2-24	Detector module 36, schematic diagram.....	2-32
2-25	Receiver sampler module 37, schematic diagram	2-33
2-26	Transmit sampler module 38, schematic diagram	2-34
2-27	Decision circuit module 42, schematic diagram	2-35
2-27.1	NOR gate module 46, schematic diagram.....	2-36
2-27.2	Basic NAND gate	2-36.1
2-27.3	NAND gate SE101K, basic application and schematic diagram	2-36.2
2-27.4	High fan out dual NAND gate SE113K, basic application and schematic diagram	2-36.3
2-27.5	Flip-flop SE124K. basic application and schematic diagram	2-36.4
2-27.6	Line driver SE150K, basic application and schematic diagram	2-36.5
2-27.7	NAND gate module SE157K, basic application and schematic diagram	2-36.6
2-27.8	Monostable multivibrator SE160K, basic application and schematic diagram	2-36.7
2-27.9	NAND gates SE181K, basic application and schematic diagram	2-36.8
2-27.10	Flip-flop CS704K, basic application and schematic diagram	2-36.9
2-28	Automatic short circuit protection circuit, simplified schematic diagram	2-37
2-29①	Panel 1A6/2A6, idealized waveforms (part 1 of 2)	2-47
2-29②	Panel 1A6/2A6, idealized waveforms (part 2 of 2)	2-48
2-30	Panel 1A8. idealized waveforms	2-54
2-31	Panel 1A9, address pulse and aux address circuit, idealized waveforms.....	2-62
2-32	Delayed/undelayed timing signal gate circuit	2-72
2-32.1	Address inhibit circuit, idealized waveforms	2-80.1
4-1	Extender cable assembly	4-3
5-1	Multiplexer TD-352/U, performance test setup	Foldout
5-2	Multiplexer TD-353/U, performance test setup	Foldout
5-1	Panel 1A2/2A2, top view	6-2
6-2	Panel 1A8/2A2, top view	6-3
6-3	Panel 1A6, top view	6-4
6-4	Panel 2A6, top view.	6-5
6-5	Panel 1A6/2A6, top view	6-6
6-6	Panel 1A7, top view	6-7
6-7	Panel 2A7, top view	6-8
6-8	Panel 1-8, top view	6-9
6-9	Panel 2A8, top view	6-10
6-10	Panel 1A9, top view	6-11
6-11	Panel 2A9, top view	6-12
6-12	Panel 1A10, top view	6-13
6-13	Panel 2A10, top view	6-14
6-14	Panel 1A11/2A11, top view	6-16
6-16	Panel 1A12/2A12, top view	6-16
6-16	Panel 1A13, top view	6-17
6-17	Panel 2A13, top view	6-18
6-18.1	Panel 1A14A/2A14A, top view	6-18.1
6-18	Panel 1-14/2A14, top view	6-19
6-19	Panel 1A16, top view	6-20
6-20	Panel 2A16, top view	6-21
6-21	Panel 1A16/2A16, top view.	6-22
6-22	Panel 1A17, top view	6-23

LIST OF ILLUSTRATIONS-Continued

Fig.#	Title	Page
6-23	Panel 2A17, top view	6-24
6-24	Panel 1A18, top view	6-26
6-25	Panel 2A18, top view	6-26
6-26	Panel 1A29/2A19, top view	6-27
6-26.1	Panel 1A20/2A20, top view	6-28
6-27	Panel 1A7, troubleshooting - waveforms	6-29
6-28	Panel 1A8, troubleshooting waveforms	Foldout
6-29	Panel 1A22/2A11, troubleshooting waveforms	6-30
6-30	Panel 1A16/2A16, troubleshooting waveforms	6-31
6-31	Deleted	
6-32	Color coding markings for MIL STD resistors, inductors and capacitors	Foldout
6-33	Multiplexer TD-352/U transmit circuits, block diagram	Foldout
6-34	Multiplexer TD-352/U transmit timing, idealized waveforms	Foldout
6-35	Multiplexer TD-352/U receive circuits, block diagram	Foldout
6-36	Multiplexer TD-352/U receive timing, idealized waveforms	Foldout
6-37	Multiplexer TD-352/U monitor and alarm circuits, block diagrams	Foldout
6-38	Multiplexer TD-353/U transmit circuits, block diagram	Foldout
6-39	Multiplexer TD-353/U transmit timing, idealized waveforms	Foldout
6-40	Multiplexer TD-353/U receive circuits, block diagram	Foldout
6-41	Multiplexer TD-353/U receive timing, idealized waveforms	Foldout
6-42	Multiplexer TD-353/U monitor and alarm circuits, block diagram	Foldout
6-43	Panel 1A1/2A11 top view	Foldout
6-44	Panel 1A1/2A1, schematic diagram	Foldout
6-45	Panel 1A2A/2A2A, schematic diagram	Foldout
6-45.1	Panel 1A2/2A2A, schematic diagram	Foldout
6-46	Panel 1A2/2A2 or 1A2/2A2A, troubleshooting waveforms	Foldout
6-47	Panel 1A3/2A3, schematic diagram	Foldout
6-48	Panel 1A3/2A3, troubleshooting waveforms	Foldout
6-49	Panel 1A5, schematic diagram	Foldout
6-50	Panel 1A5, troubleshooting waveforms	Foldout
6-51	Panel 2A5 schematic diagram	Foldout
6-52	Panel 2A5 troubleshooting waveforms	Foldout
6-53	Panel 1A6/2A6, schematic diagram	Foldout
6-53.1	Panel 1A6A/2A6A, schematic diagram	Foldout
6-54 ^①	Panel 1A6/2A6, troubleshooting waveforms (part 1 of 3)	Foldout
6-54 ^②	Panel 1A6/2A6, troubleshooting waveforms (part 2 of 3)	Foldout
6-54 ^③	Panel 1A6/2A6, troubleshooting waveforms (part 3 of 3)	Foldout
6-55	Panel 1A7, schematic diagram	Foldout
6-56	Panel 2A7, schematic diagram	Foldout
6-57	Panel 2A7, troubleshooting waveforms	Foldout
6-58	Panel 1A8, schematic diagram	Foldout
6-59	Panel 2A8 schematic diagram	Foldout
6-60	Panel 2A8 troubleshooting waveforms	Foldout
6-61	Panel 1A9, schematic diagram	Foldout
6-62	Panel 1A9, troubleshooting waveforms	Foldout
6-63	Panel 2A9, schematic diagram	Foldout
6-64	Panel 2A9, troubleshooting waveforms	Foldout
6-65	Panel 1A10 schematic diagram	Foldout
6-66	Panel 1A10 troubleshooting waveforms	Foldout
6-67	Panel 2A10, schematic diagram	Foldout
6-68	Panel 2A10, troubleshooting waveforms	Foldout
6-69	Panel 1A11/2A11, schematic diagram	Foldout

LIST OF ILLUSTRATIONS-Continued

Fig.#	Title	Page
6-70	Panel 1A12/2A12, schematic diagram	Foldout
6-70.1	Panel 1A121, schematic diagram	Foldout
6-71 ^①	Panel 1A12/2A12, troubleshooting waveforms (part 1 of 2)	Foldout
6-71 ^②	Panel 1A12/2A12, troubleshooting waveforms (part 2 of 2)	Foldout
6-72	Panel 1A13, schematic diagram	Foldout
6-73	Panel 1A13, troubleshooting waveforms	Foldout
6-74	Panel 2A13, schematic diagram	Foldout
6-75	Panel 2A13, troubleshooting waveforms	Foldout
6-76	Panel 1A14/2A14, schematic diagram	Foldout
6-77 ^①	Panel 1A14/2A14, troubleshooting waveforms (part 1 of 2)	Foldout
6-77 ^②	Panel 1A14/2A14, troubleshooting waveforms (part 2 of 2)	Foldout
6-77.1 ^①	Panel 1A14A/2A14A, schematic diagram.	Foldout
6-77.2 ^②	Panel 1A14A/2A14A, troubleshooting waveforms (part 1 of 3)	Foldout
6-77.2	Panel 1A14A/2A14A, troubleshooting waveforms (part 2 of 3)	Foldout
6-77.2	Panel 1A14A/2A14A, troubleshooting waveforms (part 3 of 3)	Foldout
6-78	Panel 1A15, schematic diagram.....	Foldout
6-79	Panel 1A15, troubleshooting waveforms	Foldout
6-80	Panel 2A15, schematic diagram.....	Foldout
6-81	Panel 2A15, troubleshooting waveforms	Foldout
6-82	Panel 1A16/2A16, schematic diagram.....	Foldout
6-83	Panel 1A17, schematic diagram.....	Foldout
6-84	Panel 1A17, troubleshooting waveforms	Foldout
6-85	Panel 2A17, schematic diagram.....	Foldout
6-86	Panel 2A17, troubleshooting waveforms	Foldout
6-87	Panel 1A18, schematic diagram.....	Foldout
6-88	Panel 1A18, troubleshooting waveforms.....	Foldout
6-89	Panel 2A18, schematic diagram.....	Foldout
6-90	Panel 2A18, troubleshooting waveforms.....	Foldout
6-91	Panel 1A19/2A19, schematic diagram.....	Foldout
6-92 ^①	Multiplexer TD-352/U, location of parts (part 1 of 3)	Foldout
6-92 ^②	Multiplexer TD-352/U, location of parts (part 2 of 3)	Foldout
6-92 ^③	Multiplexer TD-352/U, location of parts (part 3 of 3)	Foldout
6-93 ^①	Multiplexer TD-352/U, schematic diagram (part 1 of 3)	Foldout
6-93 ^②	Multiplexer TD-352/U, schematic diagram (part 2 of 3)	Foldout
6-93 ^③	Multiplexer TD-352/U, schematic diagram (part 3 of 3)	Foldout
6-94 ^①	Multiplexer TD-352/U, wiring diagram (part 1 of 4)	Foldout
6-94 ^②	Multiplexer TD-352/U, wiring diagram (part 2 of 4)	Foldout
6-94 ^③	Multiplexer TD-352/U, wiring diagram (part 3 of 4)	Foldout
6-94 ^④	Multiplexer TD-352/U, wiring diagram (part 4 of 4)	Foldout
6-95 ^①	Multiplexer TD-353/U, location of parts (part 1 of 3)	Foldout
6-95 ^②	Multiplexer TD-353/U, location of parts (part 2 of 3)	Foldout
6-95 ^③	Multiplexer TD-353/U, location of parts (part 3 of 3)	Foldout
6-96 ^①	Multiplexer TD-353/U, schematic diagram (part 1 of 5)	Foldout
6-96 ^②	Multiplexer TD-353/U, schematic diagram (part 2 of 5)	Foldout
6-96 ^③	Multiplexer TD-353/U, schematic diagram (part 3 of 5)	Foldout
6-96 ^④	Multiplexer TD-353/U, schematic diagram (part 4 of 5)	Foldout
6-96 ^⑤	Multiplexer TD-353/U, schematic diagram (part 5 of 5)	Foldout
6-97 ^①	Multiplexer TD-353/U, wiring diagram (part 1 of 8)	Foldout
6-97 ^②	Multiplexer TD-353/U, wiring diagram (part 2 of 8)	Foldout

LIST OF ILLUSTRATIONS-CONTINUED

Fig.#	Title	Page
6-97③	Multiplexer TD-353/U, wiring diagram (part 3 of 8)	Foldout
6-97④	Multiplexer TD-353/U, wiring diagram (part 4 of 8)	Foldout
6-97⑤	Multiplexer TD-353/U, wiring diagram (part 5 of 8)	Foldout
6-97⑥	Multiplexer TD-353/U, wiring diagram (part 6 of 8)	Foldout
6-97⑦	Multiplexer TD-353/U, wiring diagram (part 7 of 8)	Foldout
6-97⑧	Multiplexer TD-353/U, wiring diagram (page 8 of 8)	Foldout
6-98	Panel 1A1/2A1, wiring diagram	Foldout
6-99	Panel 1A19/2A19, wiring diagram	Foldout

CHAPTER 1

INTRODUCTION

1-1. Scope

a. This manual covers direct and general support and depot maintenance for Multiplexers TD-352/U and TD353/U. It includes instructions for troubleshooting, testing, aligning, and repairing the equipment, replacing maintenance parts, and repairing specified maintenance parts. It also lists tools, materials, and test equipment required for direct and general support and depot maintenance. Detailed functions of the equipment are covered in paragraphs 2-1 through 2-9.

b. The complete technical instructions for this equipment include TM 11-5805-367-12.

c. Throughout this manual, reference to panel 1A6/2A6 also applies to panel 1A6A/2A6A. Reference to 1A14/2A14 also applies to panel 1A14A/2A14A and reference to panel 1A12/2A12 also applies to panel 1A12 unless otherwise specified. Reference to panel 1A2/2A2 also applies to 1A2A/2A2A.

1-2. Consolidated Index of Army Publications and Blank Forms.

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

1-3. Maintenance Forms, Records and Reports

a. *Reports of Maintenance and Unsatisfactory Equipment.* Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA PAM 738-750 as contained in Management Maintenance Update.

b. *Report of Packaging and Handling Deficiencies.* Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR-735-11-2/DLAR 4140.55/NAV-MATINST 4355.73B/AFR 400-54/MCO 4430.3H.

c. *Discrepancy in Shipment Report (DISREP)(SF361).* Fill out and forward Discrepancy in Shipment Report (DISREP)(SF361) as prescribed in AR55-38/NAVSUPINST 4610.33C/AFR 75-18MCO P4610.19D/DLAR 4500.15.

1-4. Deleted.

1-5. Reporting Equipment Improvement Recommendations (EIR)

If your multiplexer TD-352/U or TD-353/U needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-PA-MA-D, Fort Monmouth, NJ 07703-5000.

1-6. Differences Between Semiconductor Subassemblies

This paragraph contains information covering redesigned multiplexer subassemblies 1A2/2A2, 1A2A/2A2A, and 1A6A/2A6A used in the TD-352/U and TD-353/U Multiplexers. These redesigned subassemblies use silicon semiconductors in lieu of germanium devices. Subassemblies equipped with silicon semiconductors have a black anodized frame and are identified by the suffix letter A. For example, 1A6A denotes a silicon version and 1A6 denotes a germanium version of the same multiplexer subassembly. It is possible that multiplexers in the field might be equipped with a combination of germanium and silicon subassemblies. The germanium subassemblies and the silicon subassemblies can be used interchangeably.

Note

Unless otherwise noted in this manual, data relating to the subassemblies containing germanium semiconductors apply to the subassemblies containing the silicon subassemblies.

Silicon subassemblies are considered to be non-repairable and should be returned to depot for final disposition.

Change 5 1-1/(1-2 Blank)

CHAPTER 2

FUNCTIONING

Section I. BLOCK DIAGRAM ANALYSIS, MULTIPLEXER TD-352/U

2-1. General

In conjunction with other terminal equipment, Multiplexer TD-352/U delivers audio signals over radio relay or cable lines. The TD-352/U accepts 12 audio channels, samples each channel at an 8-kilocycle (kc) rate, and combines the resultant pulse amplitude modulated (pam) samples on a time division basis. It then codes the samples with a six-digit binary code and delivers the resulting pulse code modulated (pcm) output signal to either Multiplexer TD-202/U (radio interface unit) or TD-204/U (cable interface unit) for transmission. In the receive traffic direction, the TD-352/U accepts an incoming pcm pulse train from either the TD-202/U or TD-204/U and decodes it, thereby restoring the original Pam signals. The Pam signals are finally demodulated into the 12 audio channels.

2-2. Transmit Circuits for TD-352/U

(fig.6-33)

a. *Audio Circuits.* The audio input for each channel is applied to a separate pam modulator. Six double modem panels 1A2/2A2, each containing two modulator circuits, are used. In the modulators, the audio signals are sequentially sampled at an 8-kc rate by timing signals developed by the modem timing matrix in panel 2A10. In this manner, the sampled audio signals are placed on the common transmit pam line and applied to panel 2A7 in proper time sequence. In panel 2A7, the pam signals are resampled at a 96-kc rate and reshaped in the sample and store circuits. The 96-kc timing signal, TFF5, is also obtained from panel 2A10. At this point, a cupped noise signal, obtained from noise generator panel 1A11/2A11 is inserted to insure a random one-level code change on the pam line in the absence of any audio input. This masks low level random noise caused by crosstalk between channels and prevents interference with audio reception. The output of the sample and store circuits is amplified and then applied to the pam-pcm converter circuits on panel 1A6/2A6.

b. *Coding Circuits.* In panel 1A6/2A6, the pam signals are either amplified or attenuated, depending on their individual input amplitude. The amplifier-attenuator (componder) circuit compresses high-level pam samples relative to the low-level pam samples under control of the compander control and compander control signals developed on panels 2A5 and 1A6/2A6. The pam signal, properly attenuated or amplified, is then applied to the coder circuits on panel 1A6/2A6. The coder, a sequential feedback circuit, consists of a decision network, storage flip-flops, and ladder network with associated clamping flip-flops. The clamping flip-flops and ladder network form a digital-to-analog converter. The coder timing signals (T pulses) are generated on panel 2A7 using timing signal inputs from panel 2A8. Six T pulses (T1 through T6) are used to drive the clamping flip-flops in proper sequence. Panel 2A8 also supplies the necessary decision pulses for operation of the decision circuit. The output of the decision circuit is a six-bit binary pulse equivalent in amplitude to the input pam pulse after amplification or attenuation. The output of the decision circuit is stored in a flip-flop that supplies half-width pam with a digit rate of 1,152 kc, applied from coder panel 1A6/2A6 to output panel 2A5.

c. *Output Circuits.* The half-width pcm signal is applied to a shift register on panel 2A5 where it is retimed under the control of the parallel shift, shift 1, and shift 2 signals. The output of the panel 2A5 shift register is retimed full-width pcm (570 kc). The retimed pcm is next applied to panel 1A3/2A3 where the selected master (4-kc) or slave (2-kc) address is inserted. After address insertion, the pcm signal is applied through the output circuit to the front panel PCM OUT connector.

d. *Transmit Timing Circuits.* Panels 2A8, 2A9, and 2A10 comprise the transmit timing circuits. A crystal oscillator in panel 2A8 generates the basic 2,304-kc master clock signal from which all transmit timing signals in the TD-352/U are derived.

derived. In multichannel systems, the transmit timing signals of both master and slave multiplexers must be in synchronization. This condition is accomplished by synchronizing the basic clock in the multiplexer acting as the slave unit with a 576-kc signal obtained from the multiplexer acting as the master unit. The 576-kc signal used for this purpose originates in the master clock countdown circuits of panel 2A8 where it is termed TFF2 (576-kc). This signal is buffered in panel 2A9 and applied to a front panel output connector as the SYNC OUT XMTR signal. The 576-kc SYNC OUT XMTR signal from the master unit is applied to the SYNC IN connector on the slave unit. The SYNC IN signal is applied to an automatic switch circuit in panel 2A8 which synchronizes the output of the basic clock. When the TD-352/U is used in a 12-channel system, synchronization of the basic clock is unnecessary since all transmit timing signals in the unit are referenced to the master 2,304-kc signal. Principal among the transmit timing signals generated in the countdown circuit of panel 2A8 is the modem timing (384-kc) signal. This signal is used to drive a second countdown chain on panel 2A10, the outputs of which are applied to the modem timing matrix. The outputs of the matrix are the 8-kc modulator timing signals which control audio channel sampling-activity in modem panels 1A2/2A2. Other transmit timing signals are used in the pam sample and store, and coder timing circuits of panel 2A7; the pam-pcm conversion circuits of panels 1A6/2A6 and 2A5; and the pcm address and output circuits of panel 1A3/2A3. A timing diagram, using idealized transmit timing signal waveforms, is shown in figure 6-34.

2-3. Receive Circuits for TD-352/U

(fig 6-35)

a. Pcm Input, Decoding, and Demodulating Circuits. The pcm input signal is applied to the front panel PCM IN connector and is fed to three sampler gates in panel 1A12/2A12. In 12-channel operation, the input signal consists of one pcm train and contains a 4-kc address. In 24-channel operation, the input signal consists of two interleaved pcm signal trains, one with a 4-kc address and one with a 2-kc address. The address is inserted in the pcm signal by operating the ADDRESS switch in the unit at the transmitting terminal to MASTER (4-kc) or SLAVE (2-kc), depending on whether the multiplexer is acting as a master or slave unit in the transmitting system. In 12-channel systems the ADDRESS switch is always in the MASTER position. The pcm train, which will be decoded, is determined by the setting of the ADDRESS switch in the unit at the receiving terminal. This signal is always sampled in sampler gate A and is designated pcm A. The other train, designated pcm B, is sampled in sampler gate B and is delivered directly to the front panel ALT PCM connector without being decoded. The pcm signal is also fed to sampler gate C for extraction of the address signal. Timing A, B, and C signals, from the receive timing circuits, are responsible for the operation of the sampler gates. The pcm A output of sampler gate A is reshaped and sent to decoder panel 1A14/2A14 through-either the auxiliary unit or an internal delay line in panel 2A15. The delay line compensates for the delay introduced by the auxiliary unit. In panel 1A14/2A14, the pcm signal is converted from a digital to an analog signal. The pcm signal is then shifted into a six-stage serial register by the 576-kc decoder clock signal generated in panel 2A13. The last digit of the 12th channel has a 2- or 4-kc frame sync signal. This signal is removed (becomes inaudible) when the pcm is shifted from the serial to the parallel set of registers by the address digit gate. The decoder pam output is fed to expander panel 2A16, which expands the peaks of the signal. The pam expander output corresponds to the pam signal fed into the transmit coder circuit (para 2-2b). The decoder pam output is sent to the demodulator section of double modem panels 1A2/2A2 where it is sampled and stored to lengthen the pulse, filtered, and amplified. The amplified outputs are 600-ohm, balanced audio output signals and are applied to the front panel AUDIO CHAN receptacle. Demodulator timing signals from panel 2A10 control the sample and store circuits in panels 1A2/2A2.

b. *Receiver Timing.* The 576-kc timing in signal enters the front panel receptacle and is fed to a frequency doubler in panel 2A13. The 1,152-kc doubler output is fed to a pulse inhibitor. A skip pulse is also fed to the inhibitor from the skip-pulse gate on panel 1A12/2A12. When an out-of-frame condition occurs, the skip pulse causes one

pulse at a time to be dropped from the 1,152-kc input until the multiplexer frames in. The modified 1,152-kc output train is fed to the timing signal countdown circuits, where most of the timing signals for the receive section are generated. Timing A and timing B signals, which sample the incoming pcm signal, are generated here also. The 1,152-kc signal is counted down to provide the 8-kc timing signal C, which is sent to sampler gate C on panel 1A12/2A12. When the unit is in frame, the timing C pulse coincides with the frame pulse in the incoming pcm train. When the unit is in frame, the timing C signal samples the incoming pcm signal at the address digit rate. This information is fed to one side of an address comparator circuit. A local 2- or 4-kc signal, selected through the ADDRESS switch, is fed to the other side of the comparator. When the unit is in frame, a number of 2- or 4-kc identical square wave pulses will exist on each side of the comparator, thereby causing no output to be generated. This action prevents the skip-pulse gate from generating skip pulses and the phase of the timing in signal is not changed. If the unit is not in frame, the address digit will not be detected in sampler gate C and a 2- or 4-kc square wave will not be generated. A different signal will now exist on the two sides of the comparator circuit. When this condition exists, a signal is sent to the skip-pulse gate, causing it to pass one pulse of the 8-kc RFF9 signal to the 1,152-kc clock pulse inhibitor circuit in panel 2A13. The skip pulse drops out one pulse from the 1,152-kc signal, causing the phase of the receive timing signals to change by a time corresponding to one-digit width in the 24-channel operation. Therefore, this action continues until the timing C signal is coincident with the address digit. Therefore, when the timing C signal samples the proper address digit in the incoming pcm train, the skip pulses cease and the receive section of the TD-352/U is framed to the incoming pcm signal. The clock timing and countdown circuits also feed a 384-kc modem timing signal to panel 2A10. Panel 2A10 on the receive side is interchangeable with the 2A10 panel on the transmit side of the unit and performs the same functions (para 2-2d). The receive section timing diagram is shown in figure 6-36.

2-4. Monitoring and Alarm Circuits for TD-352/U

(fig.6-37)

Alarm and monitoring circuits located on panel 1A16/2A16 provide visual and audible indications of incoming traffic framing failure and for monitoring the audio signal channels. Loss of the incoming pcm signal, or an out-of-frame condition, activates the tragic alarms and frame detector circuits, causing the FRAME indicator lamp (located on the front panel) to light and the buzzer to sound. Loss of frame due to an internal unit fault will also cause the FRAME lamp to light and the buzzer to sound. The 1,100-cycle per second (cps) test tone oscillator (nonsynchronous with system) generates a test tone for the purpose of aligning and testing the audio channel modems (panels 1A2/2A2). This is done by adjusting the OSC ADJUST knob on the service facility panel while observing the indication on the front panel TEST ALIGN meter. During normal operation, the BUZZER switch is ON and the FRAME lamp is extinguished. During normal operation, no alarm control signal is generated. If the TD-352/U drops out of frame, the alarm timing and the alarm control signals are applied to panel 1A16/2A16. This causes the FRAME lamp to light and relay K1 to energize, causing the buzzer to sound. Operating the BUZZER OFF switch (S2) connects the relay driver to the other output of the frame detector; silencing the buzzer. Loss of frame also causes a squelch signal to be sent to panels 1A14/2A14 and 2A15, preventing the pcm in signal from passing through to the demodulators while the unit is out of frame. This eliminates a disagreeable sound on the audio channels while the unit is out of frame. However, when the unit is in frame again, the flip-flop reverts to its original position, causing the buzzer to sound again. Operating the BUZZER OFF switch sets the relay to the deenergized condition and silences the buzzer. The microphone and earphone amplifiers on panel 1A16/2A16 are used in conjunction with Headset-Microphone H-91A/U. A bridging circuit is used to switch the headset in and out of a channel to prevent loading of the modem. These circuits are used for communicating over any channel selected by the SERV SEL

switch. In the audio measure circuits on panel 1A16/2A16, the audio output from any modem selected by the SERV SEL switch is amplified, buffered, and applied to the TEST ALIGN meter for alignment purposes.

2-5. Fault Locator Circuits for TD-352/U

(figs.2-1 and 2-2)

All the receive fault locator circuits and one transmit fault locator circuit (coder pam) are contained on panel 2A18. The remaining transmit fault locator circuits are on panel 2A17. Each fault locator circuit samples one or more critical signal outputs from a panel. These signals are buffered, amplified, retimed if necessary, detected and then combined so they may be fed to the TEST ALIGN meter as one signal representing the overall operation of a panel. The fault locator circuits provide a green TEST ALIGN meter reading when the panel is good. When one or more signals from a panel are absent, the combined output of the fault locator circuit is slightly lower and the TEST METER reads out of the green area, indicating a faulty panel. In practice, the outputs of all fault locator circuits are first fed to the SERV SEL switch, which controls application of the individual fault locator signals to the TEST ALIGN meter.

2-6. Power Supply Circuits for TD-352/U

(fig.2-3)

a. General. The unregulated and regulated power supply subassemblies, panels 1A19/2A19 and 1A1/2A1 are two separate units. Alternating current (ac) power at 115 volts \pm 5, 50-60 cycles per second (cps), is applied to panel 1A19/2A19, and the unregulated pulsating direct current (dc) outputs are applied to panel 1A1/2A1, where they are regulated and distributed to the transmit and receive circuits. Six regulated output circuits are provided, one of which is a highly regulated -5.2-volt supply for the coder and decoder circuits. If a short circuit occurs in any of the regulated output lines, a circuit is activated to cut off all voltage regulators. After the short circuit is removed, power is restored by operating the front panel AC POWER switch to OFF momentarily.

b. Operations. There are five similar series-type voltage regulators. For positive voltages, the negative side of the regulator circuit is grounded. For negative voltages, the positive side of the regulator circuit is grounded. The -5.2-volt supply is obtained by additional regulation from the -12-volt supply. The primary 115-volt ac input to panel 1A19/2A19 is fed to transformer T1. The five outputs from transformer T1 are applied to full-wave rectifiers and individually filtered through inductance-capacitance (1c)-type filters. The 1c filter outputs are applied to subassemblies on panel 1A1/2A1, where they are regulated in series-type current regulator circuits. Each of the regulator outputs is controlled by a differential amplifier, which compares variations in the regulated output voltage to a reference voltage. If a short circuit condition occurs, the short circuit protector cuts off the -12-volt supply which, in turn, cuts off all other regulated supplies. The -5.2-volt circuit is also disabled when the -12-volt supply is cut off. The 28-volt ac output from transformer T1 is used to energize the relay in the buzzer circuit and to light the FRAME indicator lamp.

Section II. BLOCK DIAGRAM ANALYSIS, MULTIPLEXER TD-353/U

2-7. General

In conjunction with other terminal equipment, Multiplexer TD-353/U delivers audio signals over radio relay or cable lines. The TD-353/U accepts 48 audio channels, samples each channel at an 8-kc rate, and combines the resultant pam samples on a time division basis. It then codes the samples with a six-digit binary code and delivers the resulting pcm output signal to either Multiplexer TD-203/U (radio interface unit) or TD-204/U (cable interface unit) for transmission. In the receive traffic direction, the TD-353/U accepts an incoming pcm pulse train from either the TD-203/U or TD-204/U and decodes it, thereby restoring the original pam signals. The pam signals are finally demodulated into the 48 audio channels.

2-8. Transmit Circuits for TD-353/U

(fig.6-38)

a. Audio Circuits. The audio input for each channel is applied to a separate pam modulator.

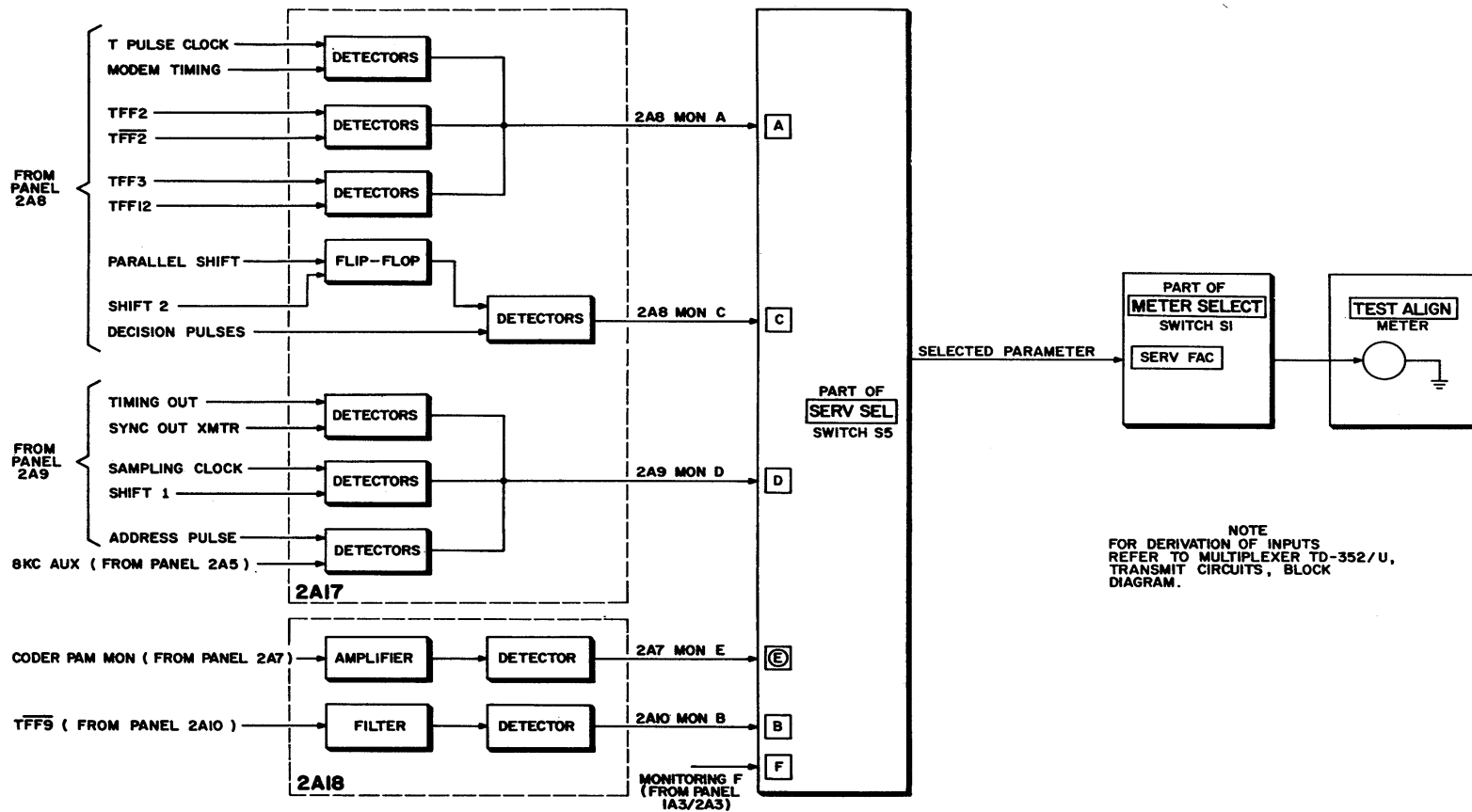


Figure 2-1. Multiplier TD-352/U transmit fault locator circuits, block diagram.

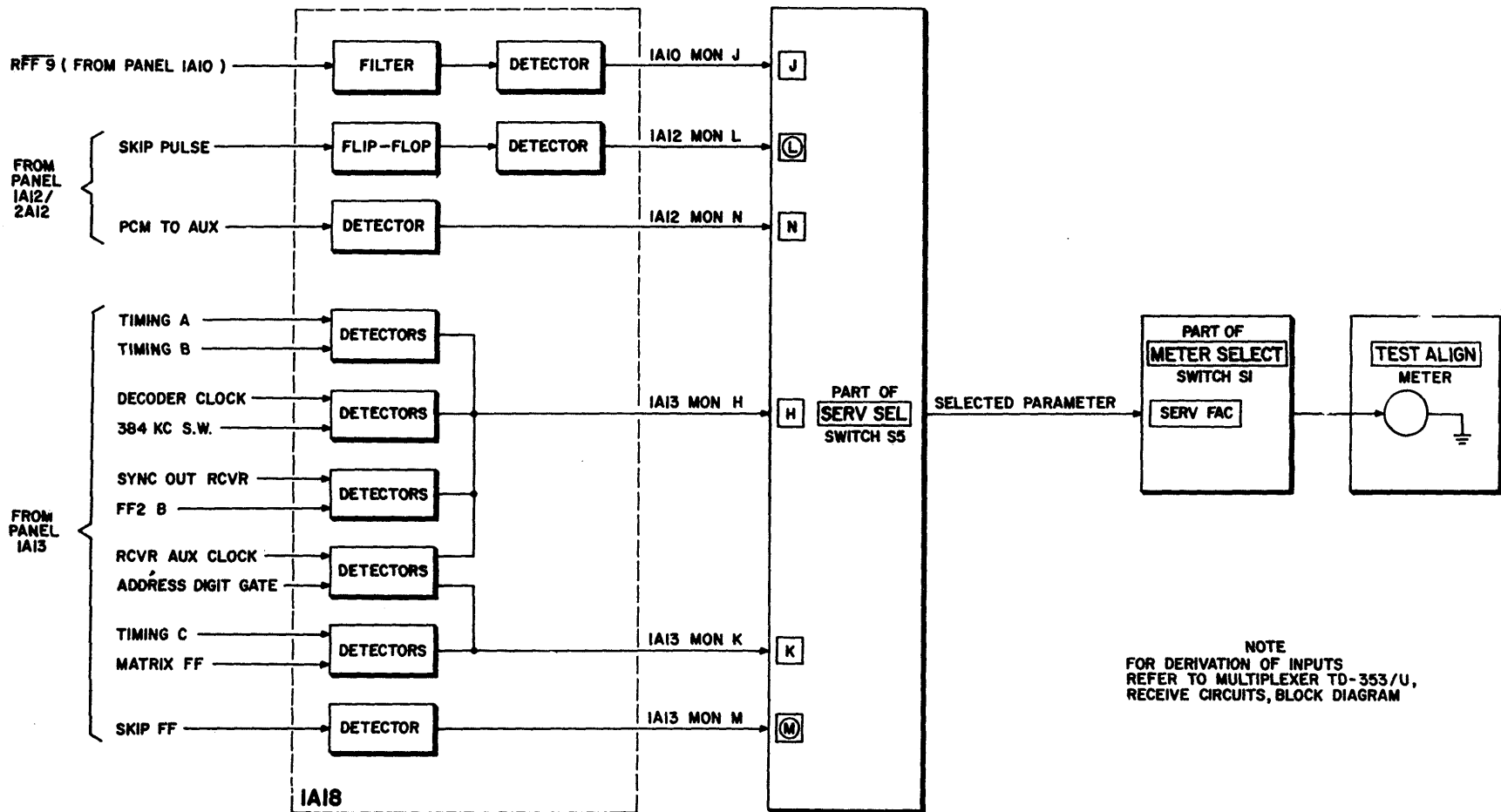


Figure 2-2. Multiplexer TD-352/U receive fault locator -circuits, block diagram.

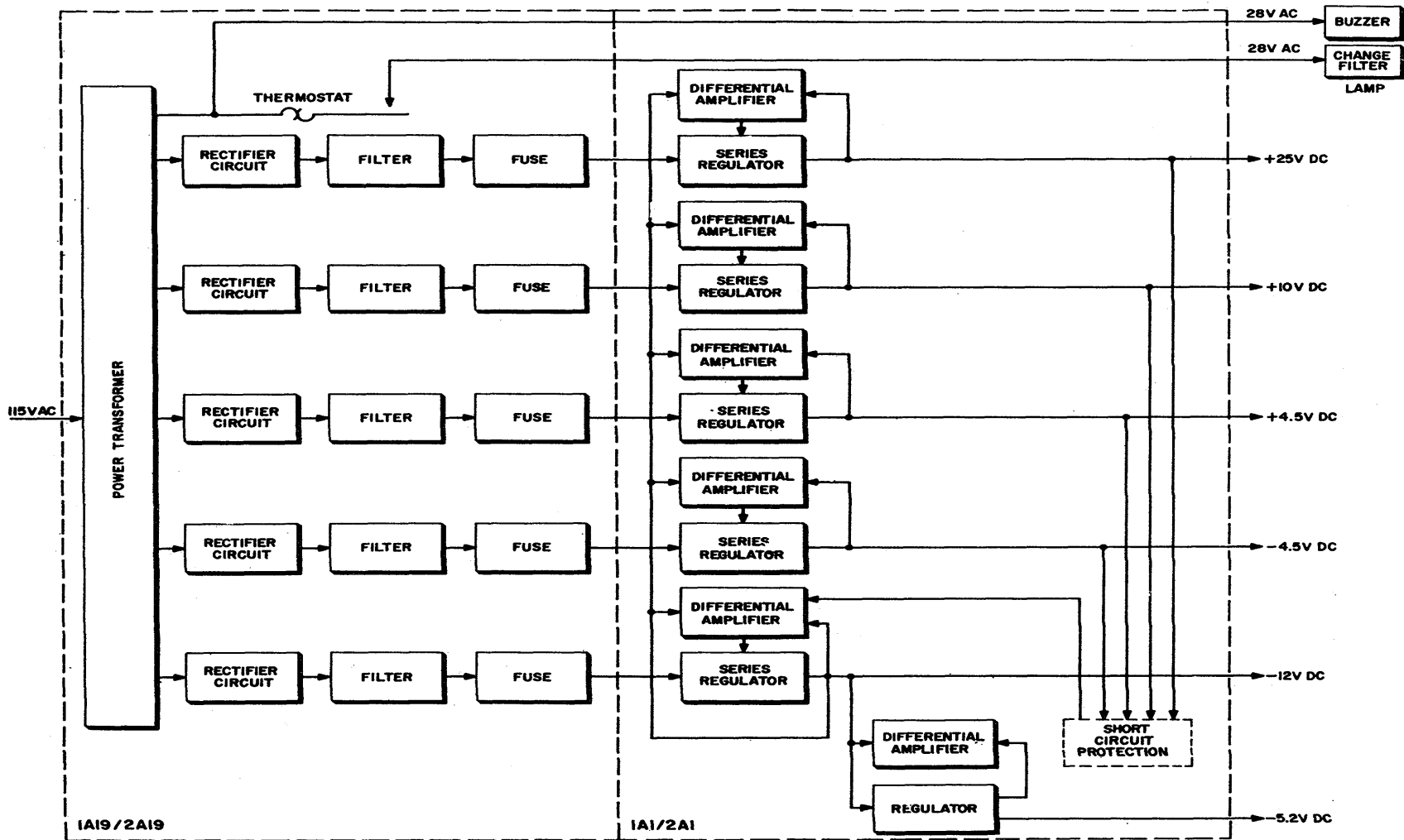


Figure 2-3. Multiplexers TD-352/U and TD-353/U power supply circuits, block diagram

Twenty-four double modem panels 1A2/2A2, each containing two modulator circuits, are used. In the modulators, the audio signals are sequentially sampled at an 8-kc rate by timing signals developed by the modem timing matrix in panel 1A10. In this manner, the odd and even channels are sampled and the pam signals placed on their respective transmit pam lines and applied to panel 1A7 in proper time sequence. In panel 1A7, the odd and even channel pam signals are alternately sampled and stored under control of two 192-kc timing signals generated in panel 1A9. A clipped noise signal, obtained from noise generator panel 1A11/2A11, is inserted on both pam lines to insure a random one-level code change on the pam line in the absence of any audio input. This also masks low level and random noise caused by crosstalk between channels, and prevents interference with audio reception. The outputs of the two sample and store circuits are alternately amplified and then applied to the pam-pcm converter circuits on panel 1A6/2A6.

b. Coding Circuits. In panel 1A6/2A6, the pam signals are either amplified or attenuated, depending on their individual input amplitude. The amplifier-attenuator (compander) circuit compresses high-level pam samples relating to the low-level pam samples under control of the compander control and compander control signals developed on panels 1A5 and 1A6/2A6. The pam signal, properly attenuated or amplified, is then applied to the coder circuits on panel 1A6/2A6. The coder, a sequential feedback circuit, consists of a decision network, storage flip-flops, and a ladder network with associated clamping flip-flops. The clamping flip-flops and ladder network form a digital-to-analog converter. The coder timing signals (T pulses) are generated on panel 1A5 using the P1 timing signal output of panel 1A8. Six T pulses (T1 through T6) are used to drive the clamping flip-flops in proper sequence. Panel 1A8 also supplies the reshaped clock signal from which the decision pulses on panel, 1A5 are generated. The output of the decision circuit is a six-bit binary pulse equivalent in amplitude to the input pam pulse after amplification or attenuation. The output of the decision circuit is stored in a flip-flop that supplies a pcm output signal at a digit rate of 2,304 kc. This signal is applied to output panel 1A3/2A3.

c. Output Circuits. On panel 1A3/2A3, the selected master (4-kc) or slave (2-kc) address is inserted, and the pcm signal is applied through the pcm output circuit to the front panel PCM OUT connector.

d. Transit Timing Circuits. Panels 1A8, 1A9, and 1A10 comprise the transmit timing circuits. A crystal oscillator in panel 1A8 generates the master clock signal from which all transmit timing signals in the TD-353/U are derived. In multichannel systems, the transmit timing signals of both master and slave multiplexers must be in synchronization. This is accomplished by synchronizing the basic clock in the multiplexer acting as the slave unit with a 2,304-kc signal obtained from the multiplexer acting as the master unit. The 2,304-kc signal used for this purpose originates in the master clock countdown circuits of panel 1A8 where it is termed SYNC OUT XMTR. The SYNC OUT XMTR signal from the master unit is applied to the SYNC IN connector on the slave unit. The SYNC IN signal is applied to an automatic switch circuit in panel 1A8 which synchronizes the output of the basic clock. When the TD-353/U is used in a 48-channel system, synchronization of the basic clock is unnecessary since all transmit timing signals in the unit are referenced to the master clock signal. Principal among the transmit timing signals generated in the countdown circuit of panel 1A8 is the FF3B xmtr (384-kc) signal. This signal is buffered in panel 1A9 and termed the modem timing signal. This signal is used to drive a second countdown chain on panel 1A10, the outputs of which are applied to the modem timing matrix. The outputs of the matrix are the 8-kc modulator timing signals which control audio channel sampling activity in modem panels 1A2/2A2. Other transmit timing signals are used in the pam sample and store circuits of panel 1A7, the pam-pcm conversion circuits of panels 1A6/2A8 and 1A5, and the pcm address and output circuits of panel 1A3/2A3. A timing diagram, using idealized transmit timing signal waveforms, is shown in figure 6-39.

2-9. Receive Circuits for TD-353/U

(fig. 6-40)

- a. *Pcm Input, Decoding, and Demodulating Circuits.* The pcm input signal is applied to the front panel PCM IN connector and is fed to three

sampler gates in panel 1A12/2A12. In 48-channel operation, the input signal consists of one pcm train and contains a 4-kc address. In 96-channel operation, the input signal consists of two interleaved pcm signal trains, one with a 4-kc address and one with a 2-kc address. The address is inserted in the pcm signal by operating the ADDRESS switch in the unit at the transmitting terminal to MASTER (4-kc) or SLAVE (2-kc), depending on whether the multiplexer is acting as a master or slave unit in the transmitting system. In 48-channel systems, the ADDRESS switch is always in the MASTER position. The pcm train which will be decoded is determined by the setting of the ADDRESS switch in the unit at the receiving terminal. This signal is sampled in sampler gate A and is designated pcm A. The pcm signal is also fed to sampler gate C for extraction of the address signal. Timing A and C signals from the receive timing circuits are responsible for the operation of the sampler gates. (Timing signal B and sample gate B are not used in this unit.) The pcm A output of sampler gate A is reshaped and sent to decoder panel 1A14/2A14 through either the auxiliary unit or an internal delay line in panel 1A15. The delay line compensates for the delay introduced by the auxiliary unit. In panel 1A14/2A14, the pcm signal is converted from a digital to an analog signal. The pcm signal is then shifted into a six-stage serial register by the decoder clock signal generated in panel 1A13. The last digit of the 48th channel has a 2- or a 4-kc frame sync signal. This signal is removed (becomes inaudible) when the pcm is shifted from the serial to the parallel set of registers by the address digit gate. The decoder pam output is fed to expander panel 1A15, which expands the peaks of the signal. The pam expander output corresponds to the pam signal fed into the transmitter circuit (para 2-8b). The decoder pam output is sent to the demodulator section of double modem panels 1A2/2A2 where it is sampled and stored to lengthen the pulse, filtered, and amplified. The amplified outputs are 600-ohm, balanced audio output signals and are applied to the front panel AUDIO CHAN receptacle. Demodulator timing signals from panel 1A10 control the sample and store circuits in panels 1A2/2A2.

b. Receiver Timing. The 2,304-kc timing in signal enters the front panel receptacle and is fed to the signal shaping and delay circuits on panel 2A13. The delayed and undelayed timing signals of this circuit are applied to a gating circuit that operates under the control of the skip pulse output of panel 1A12/2A12. When an out-of-frame condition occurs, the skip pulse causes the delayed and undelayed signals to be interchanged. This drops the timing signals back until the multiplexer frames in. The timing signal countdown circuits generate most of the timing signals for the receive section. The timing A signal, which samples the incoming pcm signal, is generated here also. The timing in signal is counted down to provide the 8-kc timing signal C, which is sent to sampler gate C on panel 1A12/2A12. When the unit is in frame, the timing A pulse coincides with the frame pulse in the incoming pcm train. When the unit is in frame; the timing C signal samples the incoming pcm signal at the address digit rate. This information is fed to one side of an address comparator circuit. A local 2- or a 4-kc signal selected through the ADDRESS switch, is fed to the other side of the comparator. When the unit is in frame; a number of 2- or 4-kc identical square wave pulses will exist on each side of the comparator, thereby causing no output to be generated. This action prevents the skip-pulse gate from generating skip pulses and the phase of the timing in signal is not changed. If the unit is not in frame, the address digit will not be detected in sampler gate C and a 2- or 4-kc square wave will not be generated. A different signal will now exist on the two sides of the comparator circuit. When this condition exists, a signal is sent to the skip-pulse gate, causing it to pass one pulse of the 8-kc RFF9 signal to the delayed-undelayed gate circuit on panel 1A13. When the timing C signal is coincident with the address digit, the skip pulses cease and the receive section of the TD-353/U is framed to the incoming pcm signal. The clock timing and countdown circuits also apply a 384-kc timing signal to panel 1A14/2A14, where it is reshaped and fed to panel 1A10 as the modem timing signal. Panel 1A10 on the receive side is interchangeable with the 1A10 panel on the transmit side of the unit and performs the same functions (para 2-8d). The receive section timing diagram is shown in figure 6-41.

2-10. Monitoring Alarm Circuit. for TD-353/U

(fig. 6-42)

Alarm and monitoring circuits located on panel 1A16/2A16 provide visual and audible indications of incoming traffic framing failure and for monitoring the odd and even audio signal channels. Loss of the incoming pcm signal, or an out-of-frame condition, activates the traffic alarms and frame detector circuits, causing the FRAME indicator lamp (located on the front panel) to light and the buzzer to sound. Loss of frame due to an internal unit fault will also cause the FRAME lamp to light and the buzzer to sound. The 1,100-cps test tone oscillator (nonsynchronous with system) generates a test tone for the purpose of aligning and testing the odd and even audio channel modems (panels 1A2/2A2). This is done by adjusting the OSC ADJUST knob on the service facility panel while observing the indication on the front panel TEST ALIGN meter. During normal operation, the BUZZER switch is ON and the FRAME lamp is extinguished. During normal operation no alarm control signal is generated. If the TD-353/U drops out of frame, the alarm timing and the alarm control signals are applied to panel 1A16/2A16. This causes the FRAME lamp to light and relay K1 to energize, causing the buzzer to sound. Operating the BUZZER OFF switch (S2) connects the relay driver to the other output of the frame detector, silencing the buzzer. Loss of frame also causes a squelch signal to be sent to panels 1A14/2A14 and 1A15, preventing the pcm in signal from passing through to the demodulators while the unit is out of frame. This eliminates a disagreeable sound on the audio channels while the unit is out of frame. However, when the unit is in frame again, the flip-flop reverts to its original position, causing the buzzer to sound again. Operating the BUZZER OFF switch sets the relay to the deenergized condition and silences the buzzer. The microphone and earphone amplifiers on panel 1A16/2A16 are used in conjunction with Headset-Microphone H-91A/U. A bridging circuit is used to switch the headset in and out of a channel-prevent loading of the modem. These circuits are used for communicating over any odd or even channel selected by the SERV SEL switches. In the audio measure circuits on panel 1A16/2A16, the audio output from any modem selected by the SERV SEL switches is amplified, buffered, and applied to the TEST ALIGN meter for alignment purposes.

2-11. Fault Locator Circuit for TD-353/U

(figs. 2-4 and 2-5)

All receive fault locator circuits are contained on panel 1A18. The transmit fault locator circuits are on panel 1A17. The operation of the fault locator circuits for the TD-353/U is similar to that described for the TD-352/U (para 2-5).

2-12. Power Supply Circuits for TD-353/U

The power supply circuits for the TD-353/U are identical with the power supply circuits described for the TD-352/U (para 2-6).

Section III. MODULE SCHEMATIC ANALYSIS

Note. In discussion pertaining to pulse levels, a negative-going pulse is defined as starting at 0-volt and decreasing toward -4.5 volts and a positive-going pulse is defined as starting at -4.5 volt and increasing toward 0 volt. Also, where there are differences in circuit parameters because the module is used in both the TD-352/U and TD-353/U, the value for the TD-353/U (high traffic) is given first followed by the value for the TD-352/U (medium traffic) in parentheses.

2-13. Gate Module 01

(fig. 2-6)

Gate module 01 performs a logical AND function for two positive-going input signals and produces one balanced output gate signal which is used to control the operation of an external bridge-type switching circuit. The input signals are applied, through pins 2 and 3, to the AND gate, consisting of diodes CR1 and CR2, and resistor R1. When the two input signals are in coincidence, the positive and negative excursions of the combined signal turn transistor Q1 on and off therefore switching the signal into the primary winding of output pulse transformer T1. In the TD-352/U, the parameters of the two input signals are such that the output signal appearing across pins 9 and 6 of the module is 5.2 microseconds (μsec) in duration, at a pulse repetition rate of 125 μsec . In the TD-353/U, the parameters of

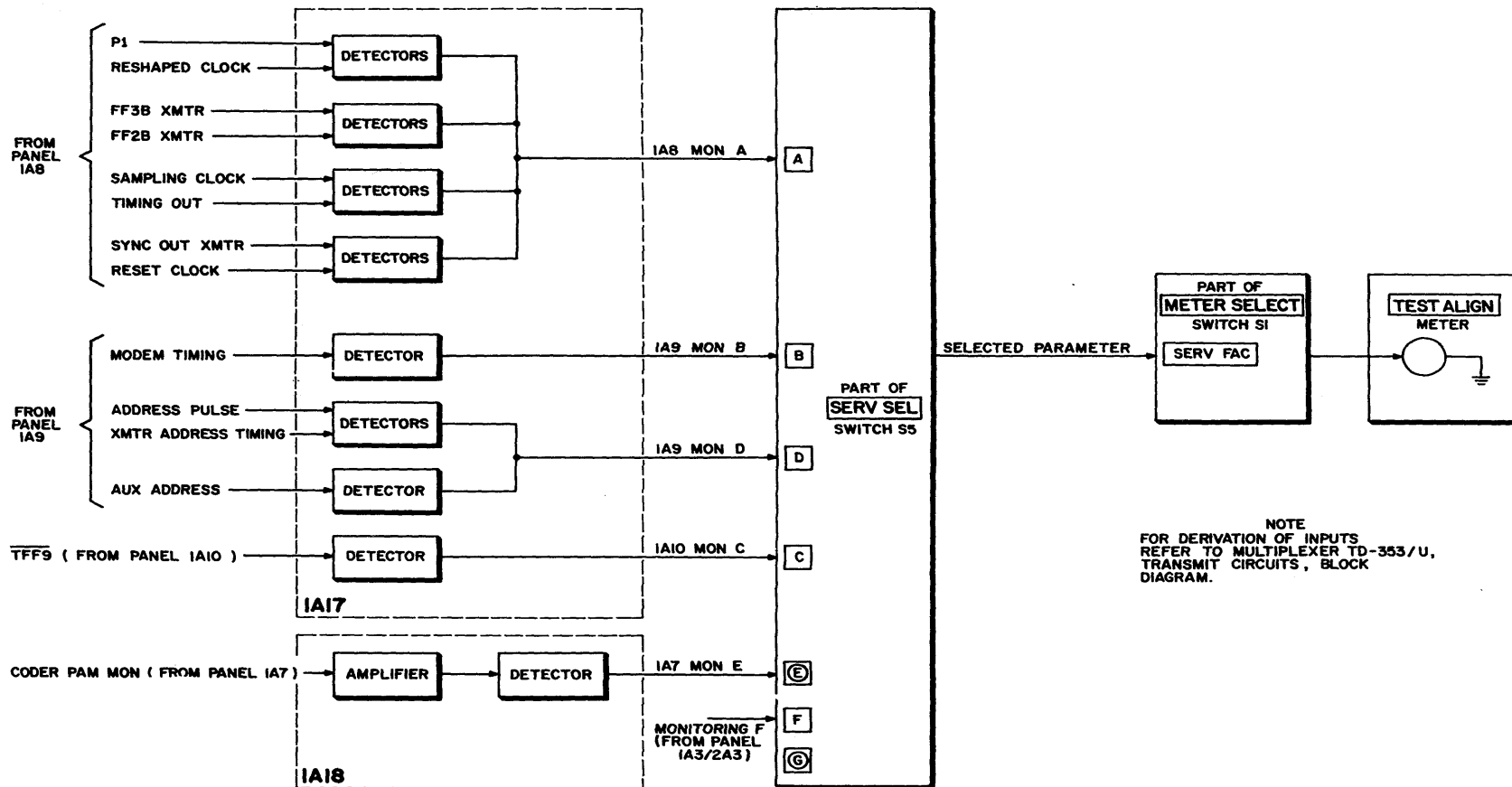


Figure 2-4. Multiplexer TD-353/U transmit fault locator circuits, block diagram.

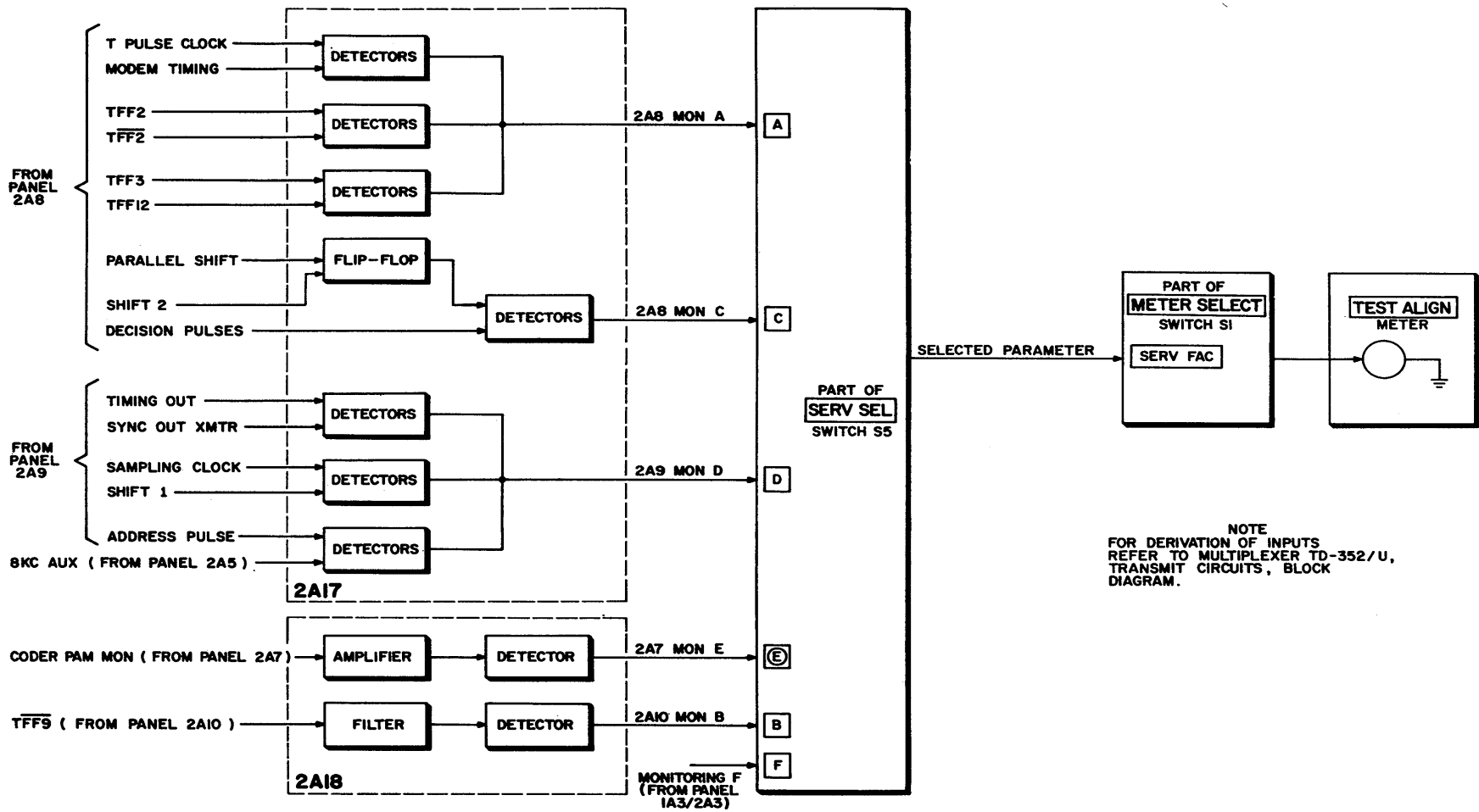


Figure 2-5. Multiplexer TD-353/U receive fault locator circuits, block diagram.

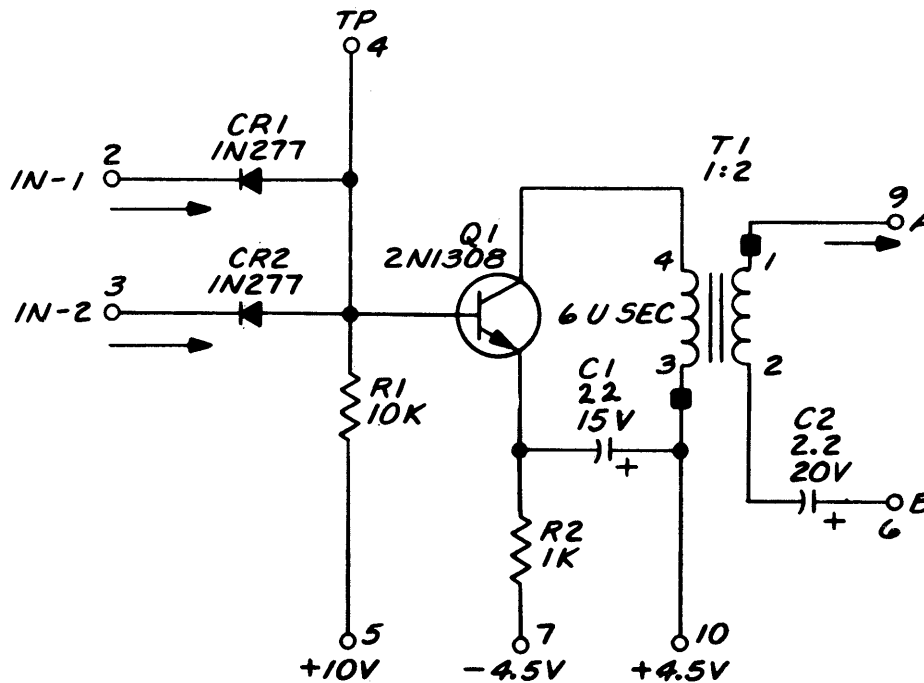
the two signals, when gated, provide an output signal which is 2.6 μ sec in duration, at a pulse repetition rate of 125 μ sec.

2-14. Sampler Module 08

(fig.2-7)

a. *Function.* The inputs to sampler module 08 are the signal to be sampled and a gate signal which controls the time of the sampling period. The signal to be sampled (in-1) consists of a random-frequency, square wave pulse train varying between 0 and -2.0 volts. The gate signal (in-2) is a train of 100-nanosecond (μ sec) pulses at an amplitude of -4.5 volts and a pulse repetition rate of 2,304 mc (576 kc). The output signals appear at pins 6 and 10, and consist of positive-going 100-nsec pulses which are in synchronization with the input gating signal. When a gating pulse occurs, an output will appear at either pin 6 or 10, but not both. If the sampled signal is at 0-volt level, the output pulse will appear at pin 10. If the sampled signal is at -2.0-volt level, the output pulse will appear at pin 6.

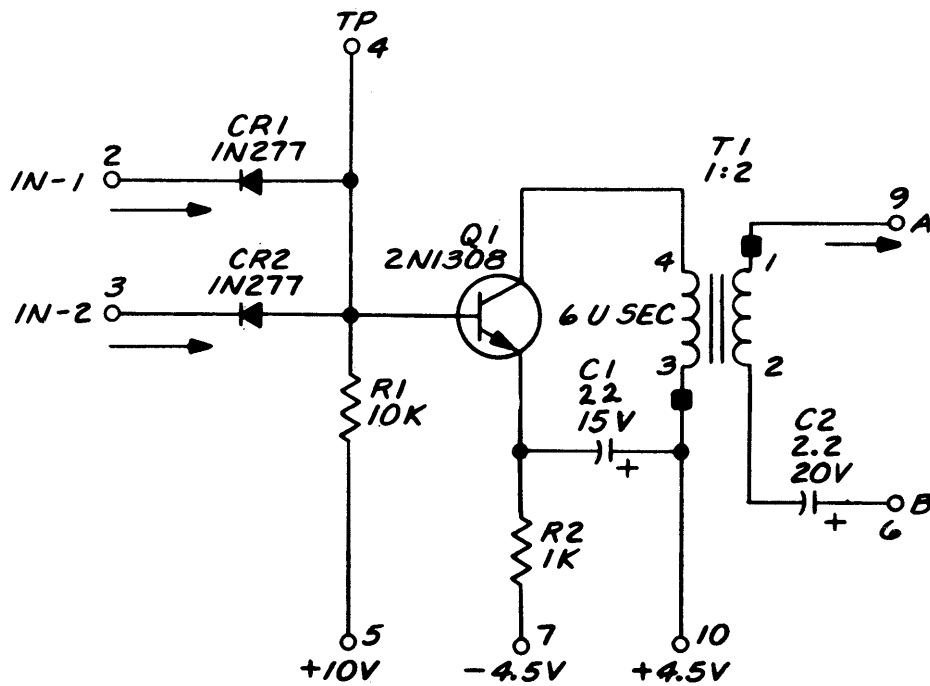
b. *Circuit Description.* The module consists of gated switch transistor Q1, pulse complementary output transistor Q2, and transistor Q3. Switch transistor Q1 controls the time at which transistors Q2 or Q3 can conduct. The collectors of transistors Q2 and Q3 are clamped to -4.5 volts by diodes CR3 and CR4, respectively. A voltage divider network, consisting of resistors R6 and R7, holds the base of transistor Q3 at approximately -1.05 volts at all times. Capacitor C2 reduces digital crosstalk which may appear as a ripple voltage at the base of transistor Q3. Voltage divider resistors R1 and R2, plus the low forward impedance of diode CR1, hold the base of transistor Q1 at a quiescent +1.0 volt, which keeps transistor Q1 cut off. The high reverse impedance of diode CR1 prevents shunting of incoming negative signals. Diode CR2 (normally conducting) and transistor Q1 (normally cut off) operate together as a current switch, providing more rapid conduction through



NOTE
RESISTANCES ARE IN OHMS, CAPACITANCES
ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-18

Figure 2-6. Gate module 01, schematic diagram.



NOTE
RESISTANCES ARE IN OHMS, CAPACITANCES
ARE IN UF, UNLESS OTHERWISE INDICATED.

TM5805-367-35/3-19

Figure 2-7. Sampler module 08 schematic diagram.

transistor Q1 when it conducts. With no input gating signal at pin 2, regardless of the signal level at input pin 7, transistors Q1, Q2, and Q3 remain cut off. With a gating signal applied to input pin 2, transistor Q1 conducts, causing transistor Q2 or transistor Q3 to conduct also, depending on which transistor has the more negative base.

2-15. Flip-Flop Module 09

(fig.2-8)

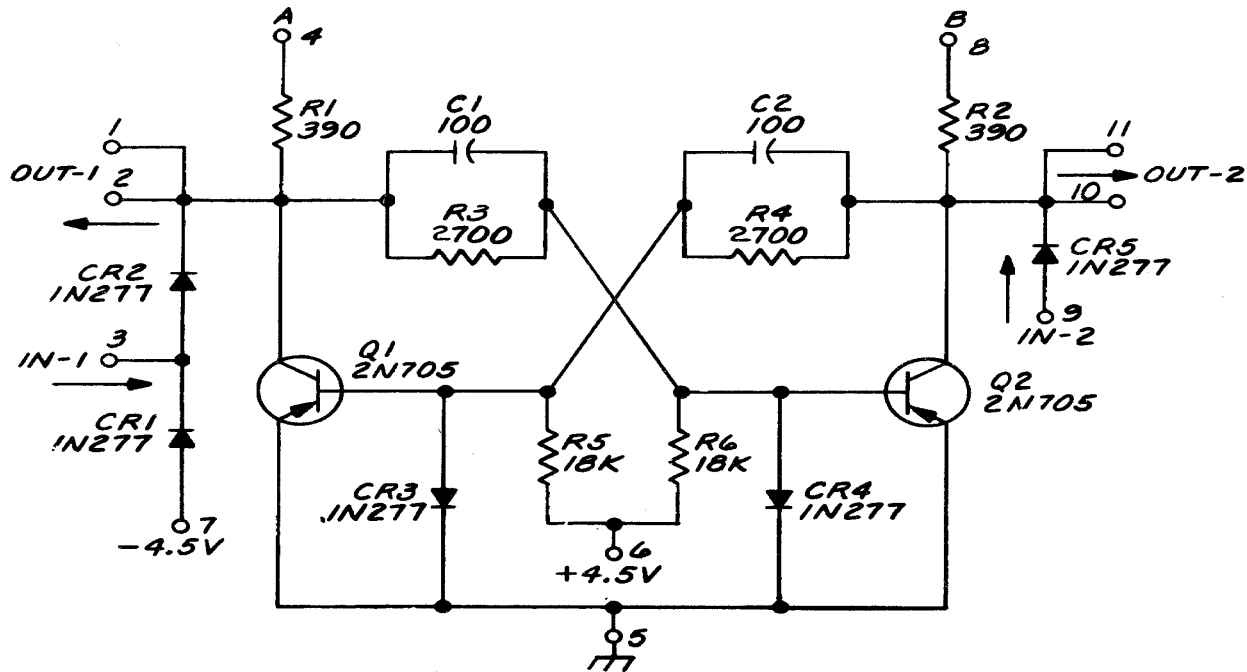
a. *Function.* Flip-flop module 09 is a high-speed bistable multivibrator, capable of switching states at a 2.3 mc rate in response to 4.5-volt positive-going trigger pulses applied to the collector of the cutoff-transistor. These pulses are fed to the collector through input triggering circuits from input pins 3 and 9. Outputs are taken from the collector of either transistor and are available to external circuitry through output pins 2 and 10. When the output at one pin is -0.2 volt, the output at the opposite pin is -4.3 volts.

b. *Circuit Description.* The module consists of multivibrator transistors Q1 and Q2, steering diodes CR2 and CR5, and trigger loading diode CR1. The bases of transistors Q1 and Q2 are clamped slightly positive by diodes CR3 and CR4, respectively. Both set-reset input triggering are complemented input triggering are used to switch the multivibrator.

2-16. NAND Gate Module 11

(fig.2-9)

a. *Function.* NAND gate module 11 generates positive-going 4.5-volt pulses under control of



NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-20

Figure 2-8. Flip-flop module 09 schematic diagram.

three gate input signals. The positive-going pulses appear at the anode of steering diode CR1. The cathode of diode CR1 is connected to the input circuit of an external flip-flop.

b. *Circuit Description.* The module consists of series-connected switching transistors Q1, Q2, and Q3, controlled by the respective gate input signals appearing at pins 5, 7, and 10. These input signals are negative-going square waves of different frequencies which are derived by flip-flop countdown circuits and coincide in phase.

2-17. Emitter Follower Module 15

(fig. 2-10)

a. *Function.* Emitter follower module 15 contains four identical buffer circuits, each operating independently, and are used to provide isolation and to prevent loading of various circuits.

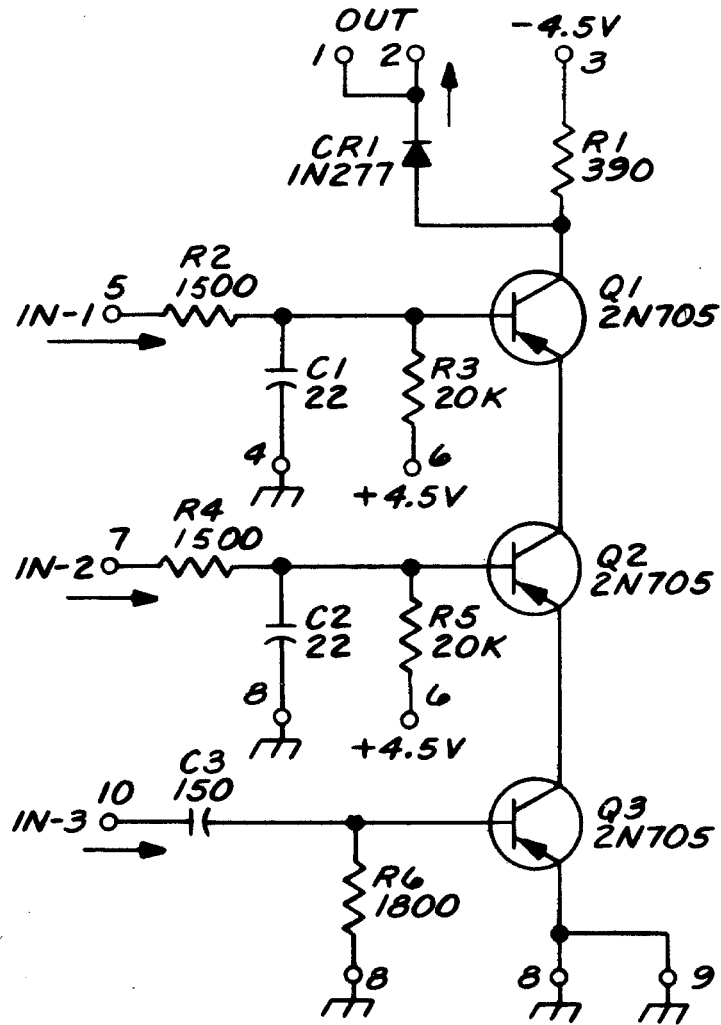
b. *Circuit Description.* The module consists of buffer transistors Q1, Q2, Q3, and Q4. Input signals to the buffers are negative-going square-pulse signals of various frequencies.

2-18. Matrix Module 16

(fig. 2-11)

a. *Function.* Matrix module 16 accepts six square-pulse input signals of various frequencies, all having amplitude levels of 0 or -4.5 volts. These signals are combined in a matrix of eight three-input AND gates, producing eight negative going square-pulse output signals on eight separate lines.

b. *Circuit Descriptions.* The module consists of 24 diodes and 8 resistors. The resistors and diodes form eight conventional three-input AND gates.



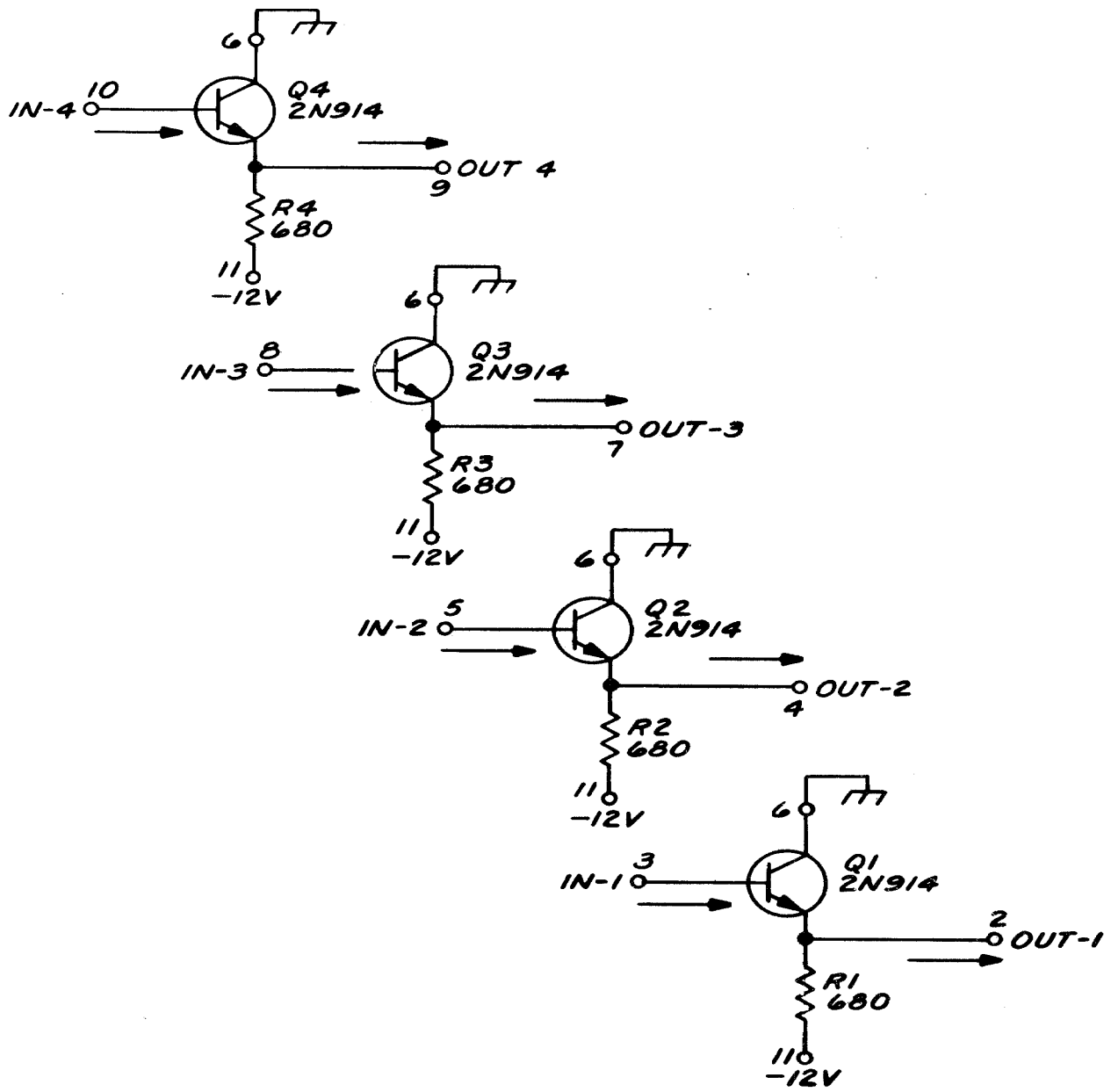
NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-21

Figure 2-9. NAND gate module 11, schematic diagram.

Two signals are gated in diodes CR1 through CR8. The output of these gates is gated in another two-input AND gate consisting of diodes CR9 through CR24. The eight AND gates operate identically. The components forming the eight AND gates are listed below with the module input and output terminals associated with each gate.

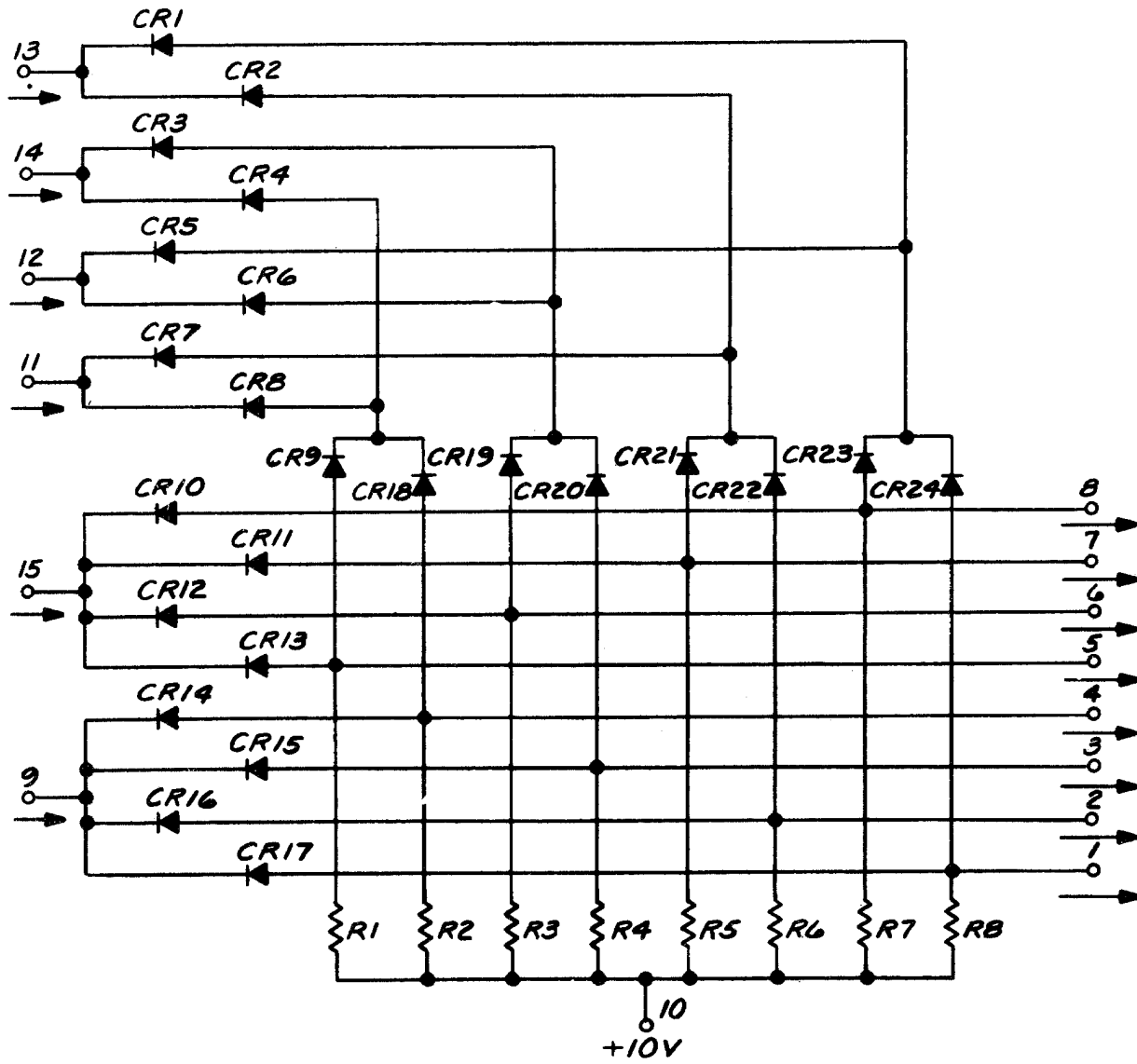


NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-22

Figure 2-10. Emitter-follower module 15, schematic diagram.



NOTE

VALUE OF ALL RESISTORS IS 6800 OHMS, 1/4 WATT.
ALL DIODES ARE TYPE IN277,

TM 5805-367-35/3-23

Figure 2-11. Matrix module 16, schematic diagram.

Input (module terminals)	AND gate components	Output (module terminals)
12, 13, 15	CR5, CR1, CR10, CR23, R7	8
11, 13, 15	CR7, CR2, CR11, CR21, R5	7
12, 14, 15	CR6, CR3, CR12, CR19, R3	6
11, 14, 15	CR8, CR4, CR13, CR9, R1	5
11, 14, 9	CR8, CR4, CR14, CR18, R2	4
12, 14, 9	CR6, CR3, CR15, CR20, R4	3
11, 13, 9	CR7, CR2, CR16, CR22, R6	2
12, 13, 9	CR5, CR1, CR17, CR24, R8	1

2-19. Matrix Module 17

(fig. 2-12)

a. *Function.* Matrix module 17 accepts six negative-going square-pulse input signals of various frequencies. These signals are combined in a matrix of six three-input AND gates, producing six square-pulse output signals on six separate lines.

b. *Circuit Description.* Matrix module 17 consists of 18 diodes and 6 resistors. The resistors and diodes form six conventional three-input AND gates. Two signals are gated in diodes CR1 through CR8. The output of these gates is gated in another two-input AND gate consisting of diodes CR9 through CR18. The six AND gates operate identically. A simplified schematic diagram of one gate is shown in figure 2-13. The components forming the six AND gates are listed below with the module input and output terminals associated with each gate.

Input (module terminals)	AND gate components	Output (module terminals)
12, 13, 15	CR5, CR1, CR10, CR17, R5	8
11, 13, 15	CR7, CR2, CR11, R4	7
11, 14, 15	CR8, CR4, CR12, CR9, R1	5
11, 14, 9	CR8, CR4, CR13, CR16, R2	4
12, 14, 9	CR6, CR3, CR14, R3	3
12, 13, 9	CR5, CR1, CR15, CR18, R6	1

2-20. Flip-Flop Module 18

(fig. 2-14)

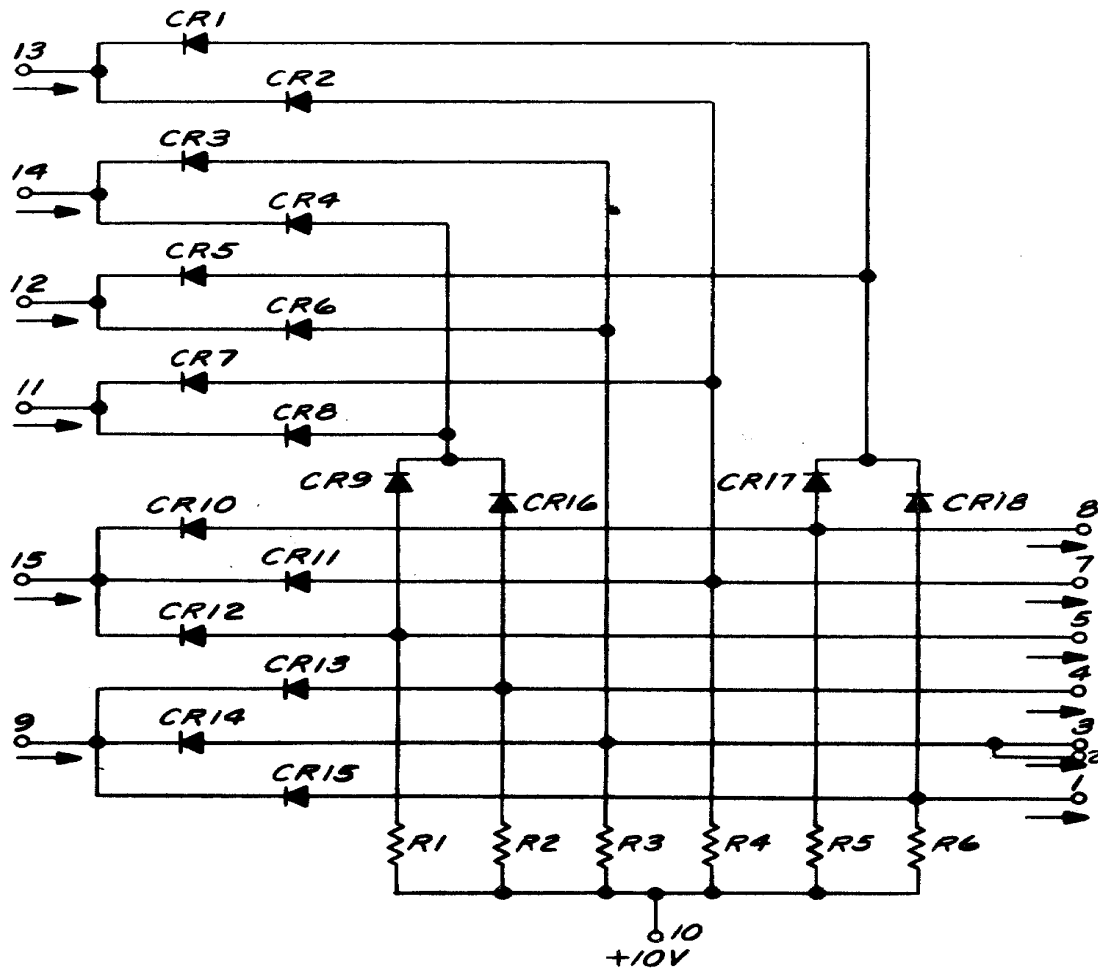
a. *Function.* Flip-flop module 18 is a bistable multivibrator with provisions for set-reset or complemented input triggering. The multivibrator switches states in response to input trigger pulses. These trigger pulses are applied to the base of either transistor through external input triggering circuits on pin 5 or 8. In addition, a -4.5-volt positive-going pulse applied to pin 3 will switch the flip-flop when pins 1 and 11 are tied to pins 2 and 10, respectively. Outputs are taken from either collector and are applied to external circuits through pins 2 and 10. When the output at one pin is 0 volt, the output of the opposite pin is -4.5 volts.

b. *Circuit Description.* The module consists of multivibrator transistors Q1 and Q2 and a complemented input triggering- circuit consisting of two biased steering gates. The inputs to both steering gates are through pin 3. The collectors of transistors Q1 and Q2 are clamped at -4.5 volts by diodes CR1 and CR2, respectively.

2-21. Oscillator Module 22

(fig. 2-15)

a. *Function.* Oscillator module 22 generates positive-going pulses occurring at a 2,304-kc



NOTE

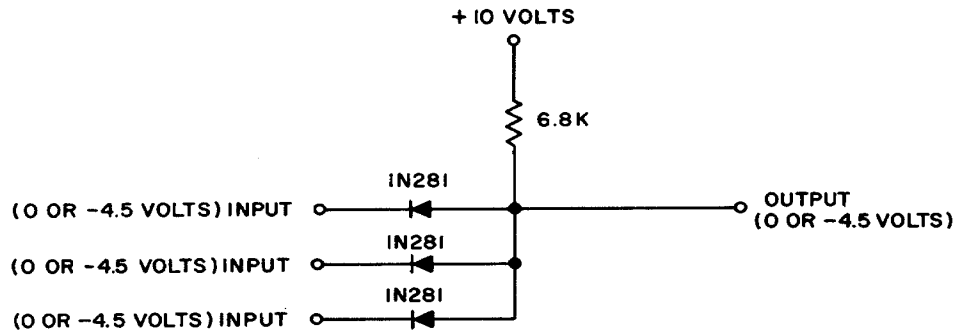
VALUE OF ALL RESISTORS IS 6800 OHMS, 1/4 WATT.
ALL DIODES ARE TYPE IN277,

TM 5805-367-35/3-24

Figure 2-12. Matrix module 17, schematic diagram.

(516-kc) rate. The pulses are 7 volts in amplitude with a 100-nsec duration and are applied to pin 5.

b. *Circuit Description.* The module consists of oscillator transistors Q1 and Q2 and buffer transistor Q3. The oscillator is controlled by an external crystal connected across pins 1 and 3. The frequency of the external crystal is 2,304 kc (576 kc). Transistor Q1 is connected to a buffer circuit that supplies feedback to the oscillator circuit and isolates the output. Transistor Q2 is a peaked amplifier having a voltage gain greater than one and provides the basic feedback and output signal. The inductance of coil L2 in the collector circuit of transistor Q2 provides a high impedance to the signal appearing at the collector. Capacitor C2 and resistors R4 and CR5, form a bias network that holds the base of transistor Q2 at +2.76 volts. Capacitor C2 reduces any



TM 5805-367-35/3-25

Figure 2-13. Matrix modules 16 and 17, AND gate form.

ripple that may appear at the base of transistor Q2. Inductor L1, connected between the -4.5-volt line and the collector of transistor Q3, and capacitor C1 form a filter that prevents the oscillator from inducing a ripple signal into the -4.5-volt power supply.

2-22. Gate Module 23

(fig. 2-16)

a. Function. Gate module 23 accepts up to four gate signals and one control signal. These signals combine to generate an output train of positive-going pulses the duration (100 or 200 nsec) of which is determined by the width of the control input signal, and the pulse repetition rate of which is determined by the rate of the gate input signals. The control signal is applied to pin 2, and the gate inputs (three or four in number, depending on module application) are applied to pins 8 (G1), 9 (G2), 10 (G3), and 11 (G4), respectively. The output is taken from pin 4.

b. Circuit Description. The module consists of OR gate diodes CRT, CR2, and CR3; resistor R4; buffer transistor Q1; switch transistor Q2; and buffer transistor Q3. Transistor Q1 is used as a buffer with an external load connected to its emitter. In module applications requiring four gate inputs, pin 11 (G4) is connected to the cathode of the external diode. The input to the fourth gate is the anode of the external diode. Resistors R1 and R2 form a voltage divider that establishes the voltage at the base of transistor Q2 during saturation or cutoff.

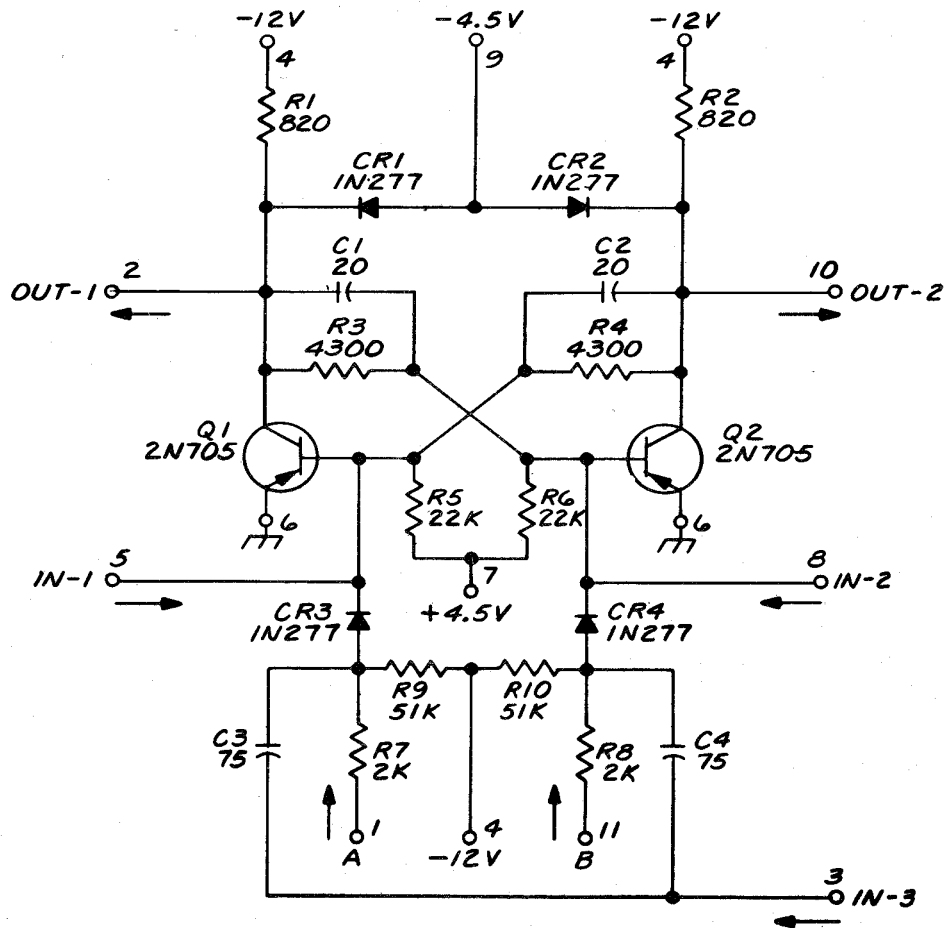
2-23. Clamping Flip-Flop Module 25 or 125

(fig. 2-17)

a. Function. Clamping flip-flop module 25 provides bistable multivibrator output with stable states of 0 and -5.2 volts. The -5.2-volt level is held to within ± 0.1 volt by clamping circuits. The output switches states in response to 4.5-volt positive-going input pulses. The pulses are fed from external circuitry through pin 3, 4, 10, or 11 to the base of the low-output (saturated) transistor. The output is taken from the collector of transistors Q1 and/or Q2, and is available to external circuitry through pins 6 and/or 7.

b. Circuit Description. The flip-flop consists of multivibrator transistors Q1 and Q2, -5.1- to -5.3-volt clamp transistor Q3, diode CR3, and steering diodes CR1 and CR2. These circuits are used in conjunction with external circuitry in two applications discussed below. The -5.1- to -5.3-volt clamp circuit (Q3, CR3) insures that when transistor Q1 is cut off, the collector of transistor Q1 will clamp to -5.2 volts ± 0.1 . In this condition, diode CR3 is biased off, and transistor Q3 is saturated and becomes the load for the collector of transistor Q1. When transistor Q1 is saturated, diode CR3 is conducting, transistor Q3 is cut off, and R7 becomes the load resistor for the collector of transistor Q1.

(1) In one application, the external circuitry



NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-26

Figure 2-14. Flip-flop module 18, schematic diagram.

is connected to pin 6, as shown in A, figure 2-18. This circuitry provides transistor Q2 with a collector load, power, and a clamp. In this arrangement, output is obtained from pin 7.

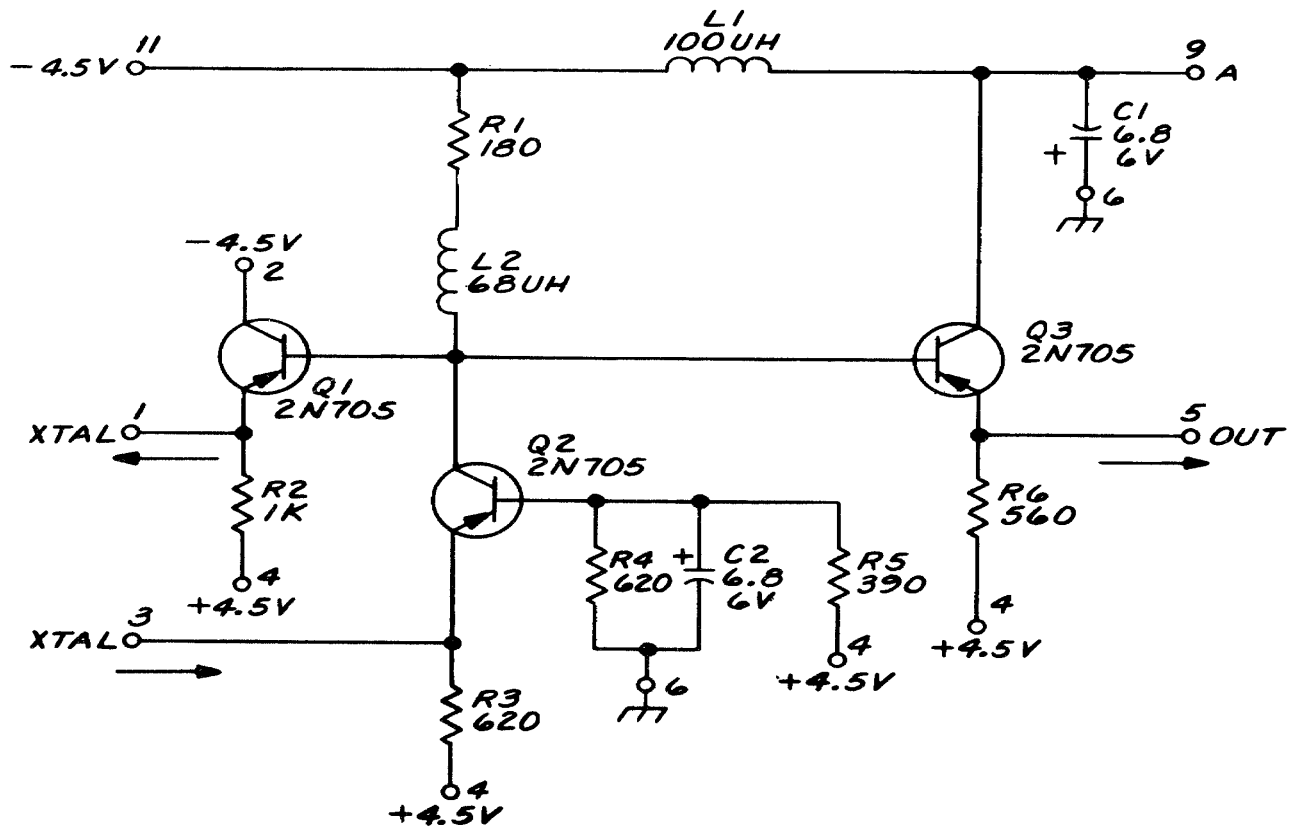
(2) In the other application, the external circuitry is connected to pins 6 and 7, as shown in B, figure 2-18.

This circuitry provides transistor Q2 with a collector load, power, and a -5.1- to -5.3-volt clamp. In this arrangement, output is obtained from pins 6 and 7.

2-24. Pulse Shaper Module 30

(fig. 2-19)

a. *Function.* The input to pulse shaper module 30 is a negative square-pulse signal having a frequency of from 8-kc to 2.3-mc and at an amplitude of approximately 4.5 volts. The output of the pulse shaper is a sharp, positive pulse of fixed duration, in synchronization with the negative edge of the input signal. The output pulse is 100 nsec in duration and with a level of 4.5 or 9.0 volts.



NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES
ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-27

Figure 2-15. Oscillator module 22, schematic diagram.

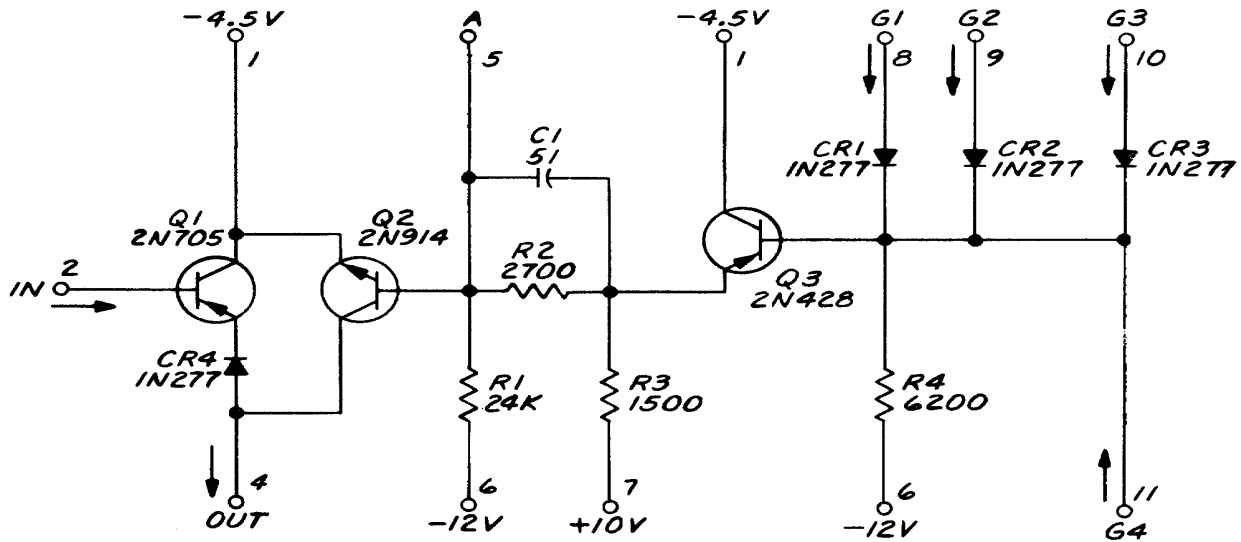
b. Circuit Description. The module consists of emitter follower transistor Q1, differentiator capacitor C1, resistors R2 and R3, pulse amplifier transistor Q2, and output driver transistor Q3. The output is applied to external circuitry from either the collector of transistor Q2 or the emitter of transistor Q3.

2-25. Amplifier Module 31

(fig. 2-20)

a. Function. Amplifier module 31 is used as the first stage of a three-stage audio-feedback amplifier. In conjunction with the other two stages it provides a gain of approximately five over the range of 0.3- to 3.5-kc when the external feedback circuit is connected. The module also provides a filtered -11.7-volt source for the collector of transistor Q1 and the collector of an external amplifier. The 11.7-volt power is connected to pins 4 and 5 for external use.

b. Circuit Description. The input signal to the module is applied through pin 2 to the base of amplifier transistor Q1, and the output, which is taken from the collector of transistor Q1 is at pin 3. Resistors R3 and R4 provide the feedback path for transistor Q1. Degenerative voltage



NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-28

Figure 2-16. Gate module 23, schematic diagram.

feedback is applied to the emitter circuit of transistor Q1 through pins 10 and 8 and appears across resistor R4. Resistor R5, and capacitor C2 limit the emitter current of transistor Q1, therefore providing the proper operating point for the transistor.

2-26. Amplifier Module 32

(fig. 2-21)

a. *Function.* Amplifier module 32 is used as the second stage of a three-stage audio-feedback amplifier.

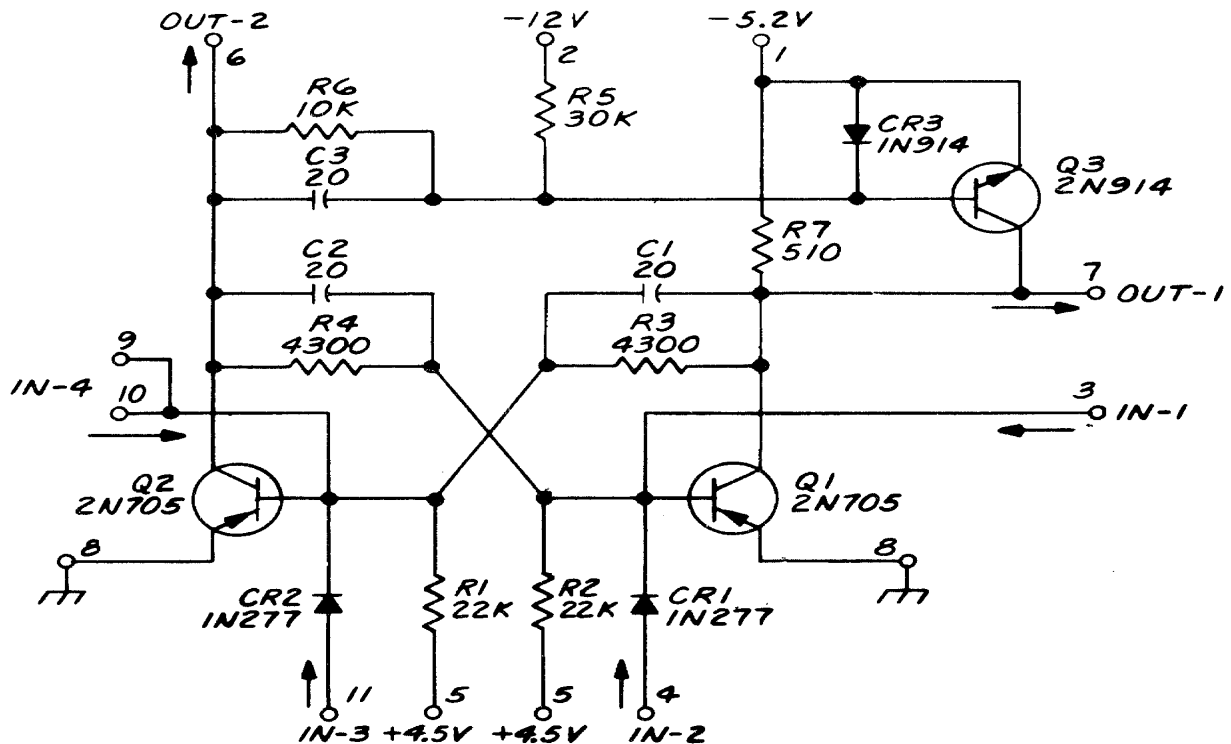
b. *Circuit Description.* The input signal to amplifier module 32 is applied through pin 3 to dc blocking capacitor C1 and then to the base of transistor Q1. The output signal appears at pin 10 and is taken from the collector of transistor Q1. Capacitor, C2, connected between the collector and base of transistor Q1, provides high frequency (above 3.5 kc) negative feedback, preventing any circuit oscillations. Resistor R3 and capacitor C3 limit the emitter current of transistor Q1. Resistors R1 and R4 provide biasing voltages.

2-27. Pulse Amplifier Module 33

(fig. 2-22)

a. *Function.* Pulse amplifier module 33 provides a fixed-amplitude in response to an input consisting of 100-nsec, 2.0-volt positive pulses. This input signal is applied to pin 2. Amplified outputs are available at pins 1 and 9. The output at pin 1 is a 4.5-volt inverted input signal. The output at pin 9 is a 60-nsec, 4.5-volt pulse.

b. *Circuit Description.* The pulse amplifier module is a two-stage circuit consisting of amplifier transistors Q1 and Q2. The collector of transistor Q1 is clamped to -4.5 volts by diode CR3. This provides a negative 4.5-volt fixed amplitude output. Transistor Q2 is a peaked amplifier since the inductance of coil L1 in the collector circuit provides high impedance to the pulse appearing in that circuit. With the col-



NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES
ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-29

Figure 2-17. Clamping flip-flop module 25 or 125, schematic diagram.

lector of Q2 clamped to -4.5 volts by diode CR1, a positive 4.5-volt fixed-amplitude output is provided. Diode CR2, which conducts between input pulses, and transistor Q2, which is cut off between input pulses, operate as a current switch. The current switch provides a uniform width pulse at the collector of transistor Q2. Pins 3 and 7 are externally connected to ground potential, and pin 8 has no external connection.

2-28. Gate Module 35

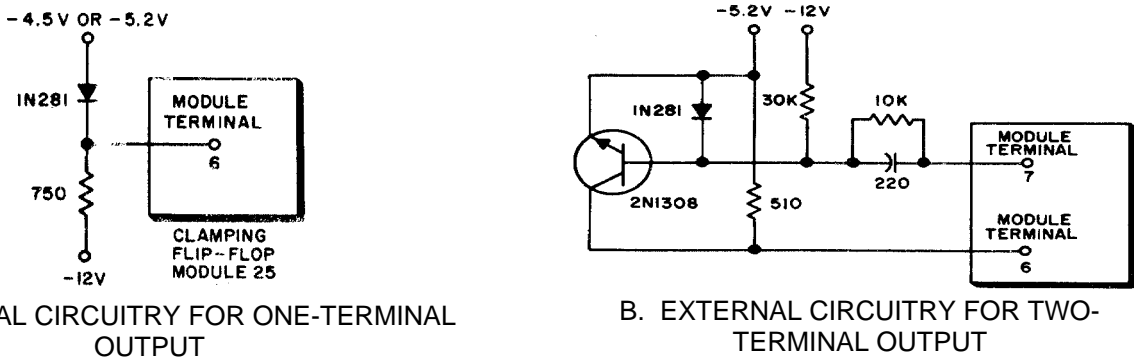
(fig. 2-23)

a. *Function.* Gate module 35 is used to decrease the pulse width of two input signals by an amount equal to the pulse width of a third input signal.

b. *Circuit Description.*

(1) Gate module 35 comprises two identical AND gate circuits: one consisting of diodes CR1 and CR2, resistor R1, and buffer transistor Q1; and the other consisting of diodes CR3 and CR4, resistor R3, and buffer transistor Q2. The first circuit is used to decrease the width of pulses contained in the signal applied to pin 2 (in-1). The second circuit performs the same function for the signal applied to pin 10 (in-2). The input signals applied to pin 2 and pin 10 are 2.6- μ sec positive-going pulses of -4.5 and 0 volts at a 48-kc pulse repetition rate.

(2) The third or controlling input signal, applied to the module through pin 9 (in-3),



NOTE
 RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.
 TM 5805-367-35/3-30

Figure 2-18. Clamping flip-flop module 25, external circuitry for one-and two-terminal outputs.

determines the decrease in pulse width of the two inputs described in (1) above. This third signal consists of a 384-kc train of 225-nsec negative-going pulses. Outputs are obtained from the module at pin 3 (out-1) and pin 8 (out-2). Each output consists of a train of 2.375-usec positive-going pulses at a 48-kc rate.

2-29. Detectors Module 36

(fig. 2-24)

a. *Function.* Detectors module 36 provides two separate and identical circuits, each used to convert input pulse signals to a positive dc level. The dc level is used to bias a diode which is part of an external AND gate circuit.

b. *Circuit Description.* The module consists of peak detector diodes CR1 and CR2, capacitors C1 and C2, and buffer transistor Q1, plus a second identical and separate circuit consisting of peak detector diodes CR3 and CR4, capacitors C3 and C4, and buffer transistor Q2. Input signals are applied to the circuits through pins 2 and 10. These inputs consist of negative-going pulse trains of various frequencies and pulse durations. Outputs are taken from pins 6 and 7.

2-30. Sampler Module 37

(fig. 2-25)

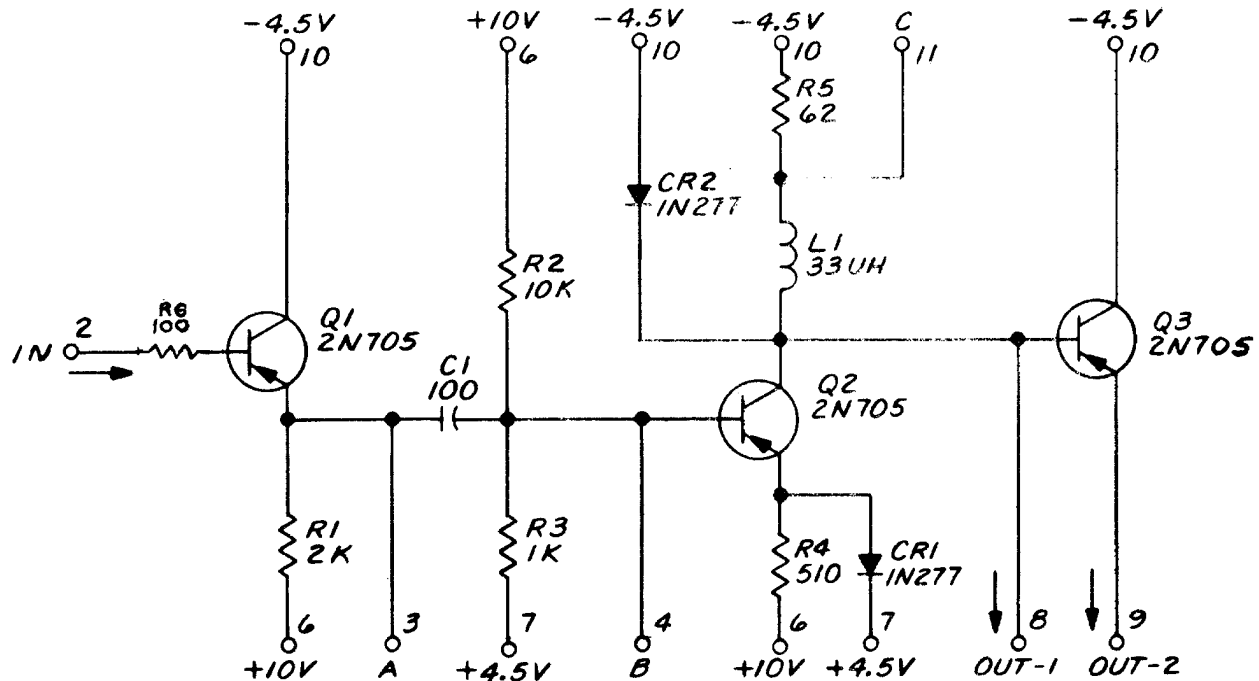
a. *Function.* Sampler module 37 provides a means of gating samples of a random-like pam input signal to form an unfiltered coherent audio output signal. This is accomplished using two input signals: a gating signal and the pam signal to be sampled. The gating signal is a train of 2.6-,usec (5.2-usec) pulses occurring at 125-usec intervals and is obtained from the secondary of an external transformer. The pulses are positive going at one end of the transformer, and negative going at the other end. The positive pulses are applied to pin 3, the negative to pin 6. When a pulse appears, clamping diodes CR5 and CR6 open and the bridge diodes conduct during the 2.6-,usec (5.2-usec) interval. The signal to be sampled appears at pin 4 and varies among 64 predetermined levels in a random manner and at 2.6-usec (5.2-usec) intervals. The start of a gating pulse is synchronous with the start of pulse amplitude level.

b. *Circuit Description.* Module 37 consists of bridge diodes CR1 through CR4, buffer transistor Q1, and transistor Q2. Diode CR5 clamps the anodes of diodes CR1 and CR3 to -4.5 volts. Diode CR6 clamps the cathodes of diodes CR2 and CR4 to +4.5 volts. Buffer transistor Q1 operates conventionally and is always conducting. Transistor Q2 operates in conjunction with external circuitry to form an audio amplifier. This amplifier provides a gain of approximately 3.3 over the range: 0.3- to 3.5-kc. An external 4,300-picofarad (pf) capacitor is connected to the base of transistor Q1 through pin 5. This capacitor serves as a means of storing the sampled pulse-amplitude level between gating pulses.

2-31. Sampler Module 38

(fig. 2-26)

a. *Function.* Sampler module 38 provides a means of gating samples of an audio signal to



NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES
ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-31

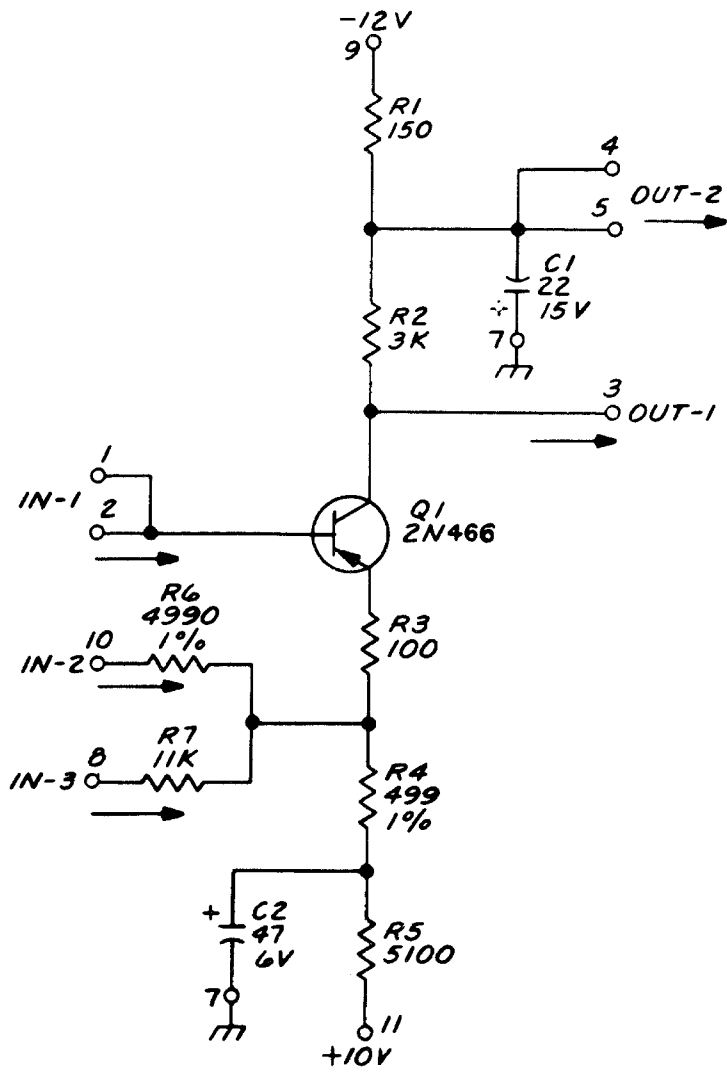
Figure 2-19. Pulse shaper module 30, schematic diagram.

form portions of a pam-time division multiplex (tdm) signal at the output. This is accomplished with two input signals: a gating signal and a signal to be sampled. The gating signal is a train of 2.6-usec (5.2-usec) pulses, occurring at 125-usec intervals and is obtained from the secondary of an external transformer. The pulses are positive going at one end of the transformer and negative going at the other end. The positive pulses are applied to pin 3, the negative to pin 6. This opens clamping diodes CR5 and CR6, and the bridge diodes conduct during the 2.6-usec (5.2-usec) interval. The frequency of the signal to be sampled varies from 0.3- to 3.5-kc and its input level is 2.0 volts root mean square (rms). This signal appears at pin 7. The output signal, which consists of pam samples of the audio input signal, appears at pin 4.

b. Circuit Description. The module consists of buffer transistor Q1 and switching-bridge diodes CR1 through CR4. Diodes CR5 clamps the anode of diodes CR1 and CR3 to 4.5 volts. Diode CR6 clamps the cathodes of diodes CR2 and CR4 to +4.5 volts. Buffer transistor Q1 operates conventionally and is always conducting.

2-32. Decision Circuit Module 42 (fig. 2-27)

a. Function. Decision circuit module 42 provides two output signals, each consisting of a train of 100-nsec, 4-volt positive-going pulses. These pulse trains are produced under control of three input signals: a train of decision pulses, a pam signal, and a ladder reference signal, applied to pins 3, 1, and d 2, respectively. The output signals are complementary and are applied to external circuitry through pins 4 and 5. Pulses at output pin 4 represent logic 1's, and pulses at output pin 5 represent logic 0's. These pulses are generated in

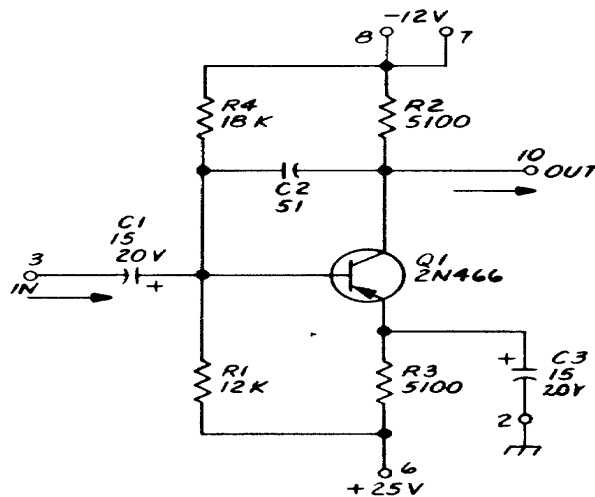


NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-32

Figure 2-20. Audio preamplifier module 31, schematic diagram.



NOTE
RESISTANCES ARE IN OHMS, CAPACITANCES
ARE IN UF, UNLESS OTHERWISE INDICATED.

EL8RC001

Figure 2-21. Audio amplifier module 32, schematic diagram.

synchronization with in-coming decision pulses. During any given decision pulse, an output pulse appears at either pin 4 or 5, but not at both. When the pam current level at pin 1 is less than the reference ladder current at pin 2, a logic 1 is generated at pin 4. When the pam current exceeds the reference ladder current, a logic 0 is generated at pin 5. Decision pulses are generated in groups of six, with a group repetition rate of 96 kc, a pulse repetition rate of 1,152 kc, and a pulse duration of 100-nsec (for medium traffic).

b. Circuit Description. The module consists of differential feedback amplifier transistors Q2 and Q4 and pulse buffer transistors Q1 and Q3. Buffer transistor Q1 isolates the collector of transistor Q2 from the base input circuit of transistor Q4 and from external circuitry connected to pin 4. Buffer transistor Q3 isolates the collector of transistor Q4 from the base input circuit of transistor Q2 and from external circuitry connected to pin 5. An external 0.01-microfarad (uf) capacitor is connected between pin 8 and ground to reduce ripple at the junction of resistors R1, R2, and R9, maintaining a steady -11.9 volts. In the presence of a decision pulse, differential feedback amplifier transistors Q2 and Q3 operate similarly to a flip-flop: they will assume one of two states, depending on the relative input current levels at pins 1 and 2.

2-32.1. Gate Module 46 (fig.2-27.1)

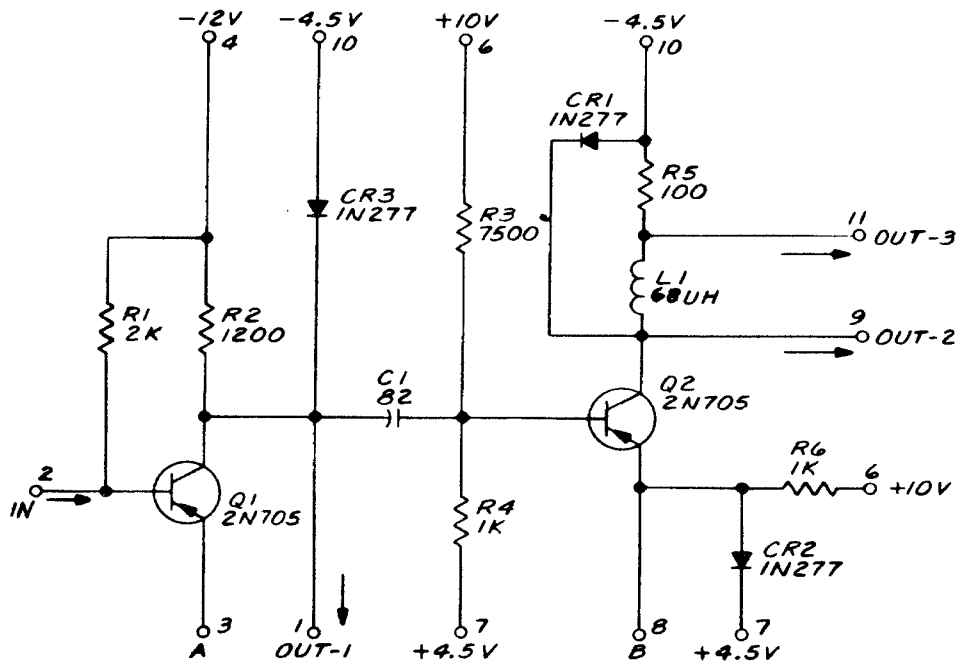
Gate module 46 is identical to Gate Module 23 except for the addition of diode CR5 in module 46. Diode CR5 provides additional emitter bias for transistor Q2. Otherwise the operation of module 46 is identical to module 23.

2-32.2. Integrated Circuit Modules

a. General.

(1) Eight integrated module types are used in various quantities in panel 1A14A/2A14A of the TD-352/U and TD-353/U. The integrated circuit element used in each type of module consists of a circuit built into a single chip of silicon by a planar process. This chip is mounted in a ten-lead TO-5 package.

(2) The circuits in all modules are high-speed low-power integrated arrays of various configurations of a basic NAND gate shown in figure 2-27.2. As shown, the NAND circuit comprises a diode AND gate and a transistor inverter. Each AND gate input drives the cathode of one diode. The gate output drives the base of the transistor inverter which provides an output at the collector in accordance with the truth table in figure 2-27.2. When the gate input is at -4.5 volts (logic 0 (zero) level) the diode conducts. When the gate input is at ground potential (logic 1 (one) level) the diode is cut off. When all gate inputs are at ground potential the gate output and transistor base are held near ground potential. This maintains the transistor conducting, giving a



NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-42

Figure 2-22. Pulse amplifier module 33, schematic diagram.

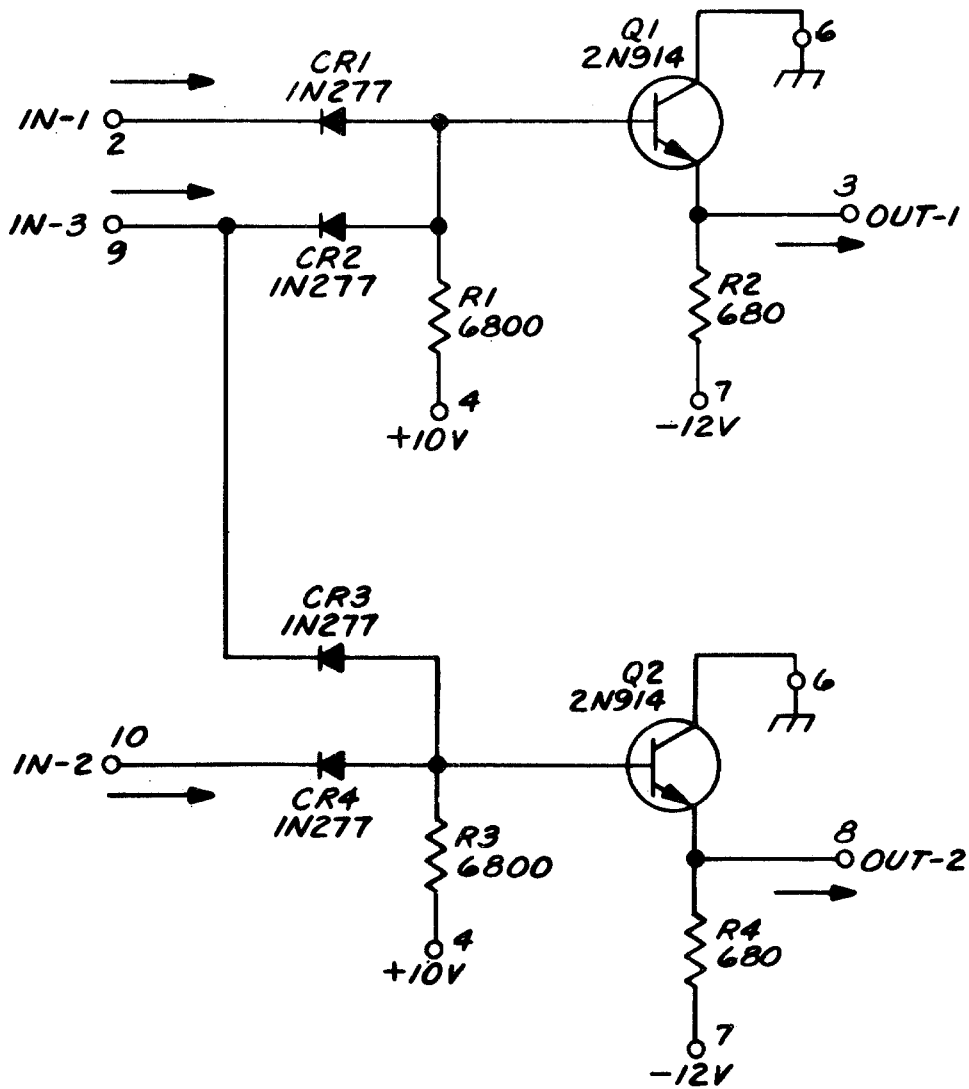
4.5 volt output (logic 0) at the collector. If -4.5 volts (logic 0) is applied to any gate input the corresponding diode conducts setting the gate output and transistor base at -4.5 volts. This keeps the transistor cut off, giving ground potential (logic 1) at the transistor collector. Thus the NAND gate output is a logic 1 if any gate input is at the logic 0 level, or a logic 0 if, and only if, all the gate inputs are logic 1.

b. *NAND Gate SE 101K* (fig. 2-27.3). NAND gate SE101K comprises a four input NAND gate with inputs applied via pins 7 through 10. In addition to the diode inputs, the gate node is accessible externally via pin 2 to expand gate fan-in. An external resistor is connected to pin 3 to provide the collector load for the inverter transistor. Output is taken from pin 3.

c. *High Fan-out Dual NAND Gate SE113K* (fig. 2-27.4). High fan-out dual NAND gate SE113K consists of two identical 3 input NAND gates. In each gate the node drives the high fan-out inverter through a two stage emitter-follower. Input to one gate is via pins 3, 4, and 5; output is via pin 2. Input to the other gate is via pins 7, 8, and 9; output is via pin 10.

d. *Flip-flop SE124K* (fig. 2-27.5). Flip-flop SE124K is a bistable multivibrator used as a clocked set-reset storage element. The flip-flop changes state in response to negative clock pulses applied at the T input. The outputs at Q and Q are determined by the levels present at the S and C inputs and are in accordance with the truth table in figure 2-27.5.

e. *Line Driver (Buffer) SE150K* (fig. 2-27.6). Line driver (buffer) SE150K comprises a two input NAND gate used for driving a heavy dc load. The gate node drives a multistage inverter buffer circuit having a two transistor pull-up pull-down output stage. Gate inputs are via pins 8 and 10; output is via pin 3.

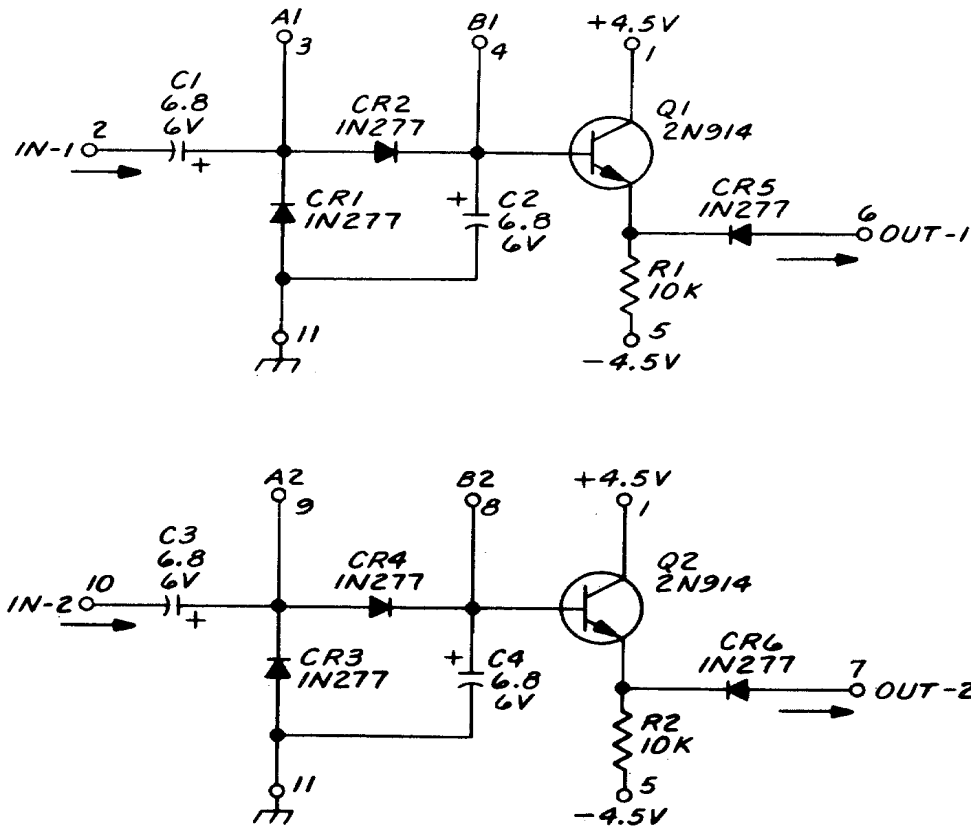


NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-35

Figure 2-23. Dual and gate module 35, schematic diagram.



NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES
ARE IN UF, UNLESS OTHERWISE INDICATED.

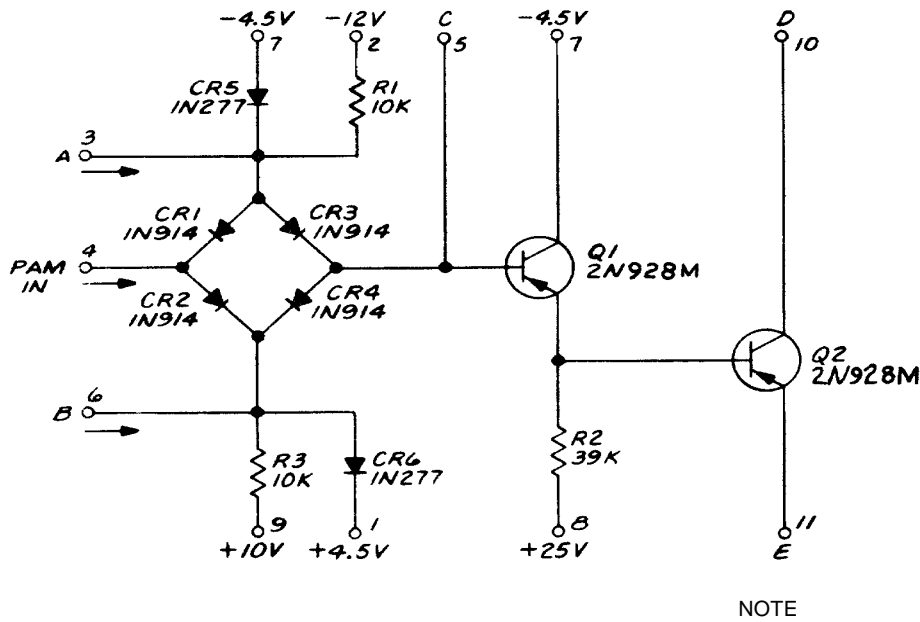
TM 5805-367-35/3-36

Figure 2-24. Detectors module 36, schematic diagram.

f. Dual NAND Gate (Buffer) SE157K (fig. 2-27.7). Dual NAND gate (buffer) SE157K consists of two identical 3 input NAND gates. In each gate, the node drives a three stage inverter buffer circuit having a two transistor, pull-up pull-down output stage. Input to one gate is via pins 3, 4, and 5; output is via pin 2. Input to the other gate is via pins 7, 8, and 9; output is via pin 10.

g. Monostable Multivibrator SE160K (fig. 2-27.8). Monostable multivibrator SE160K is used as a gated pulse shaper producing complementary buffered outputs appearing at pins 7 and 10. The circuit is triggered at the gated input (pin 9) on the negative-going edge of the input pulse. Upon being triggered, the input at pin 7 falls to the 0 level while that at pin 10 rises to the 1 level. Ninety microseconds or less later, with the exact time determined by a fixed internal timing resistor and capacitor and the external resistance connected at pin 3, the outputs at pins 7 and 10 start to switch. The output at pin 7 rises to the 1 level while pin 10 output falls to the 0 level.

h. NAND gates SE181K (fig. 2-27.9). NAND gate SE181K consists of four identical single input NAND gates. Input and



NOTE
RESISTANCES ARE IN OHMS, CAPACITANCES
ARE IN UF, UNLESS OTHERWISE INDICATED.

EL8RC002

Figure 2-25. Receive sampler module 37, schematic diagram.

output terminals are as shown in figure 2-27.9.

i. Flip-flop CS704K. (fig. 2-27. 10). Flip-flop is a bistable multivibrator used as a clocked set-reset storage element. The circuit is identical to the SE124K circuit except that CS704L has a split clock input, has no direct reset input, and contains some different input pin connections.

Section IV. PANEL SCHEMATIC ANALYSIS

2-33. Regulated Power Supply, Panel 1A1/2A1
(fig. 6-44)

a. General.

- (1) Regulated power supply panel 1A1/2A1 provides six series regulator circuits: one for each of the five unregulated output voltages (+ 10, - 4.5, +4.5, +25, and -12 volts) of panel 1A19/2A19, and a sixth (- 5.2 volts) using a portion of the -12-volt supply. These regulated voltages furnish all the operative dc power for either the TD-352/U or the TD353/U.
- (2) The six regulator circuits are of conventional design and consist of a differential amplifier, driver, and series regulator. Automatic short circuit protection is also incorporated.

b. Circuit Analysis.

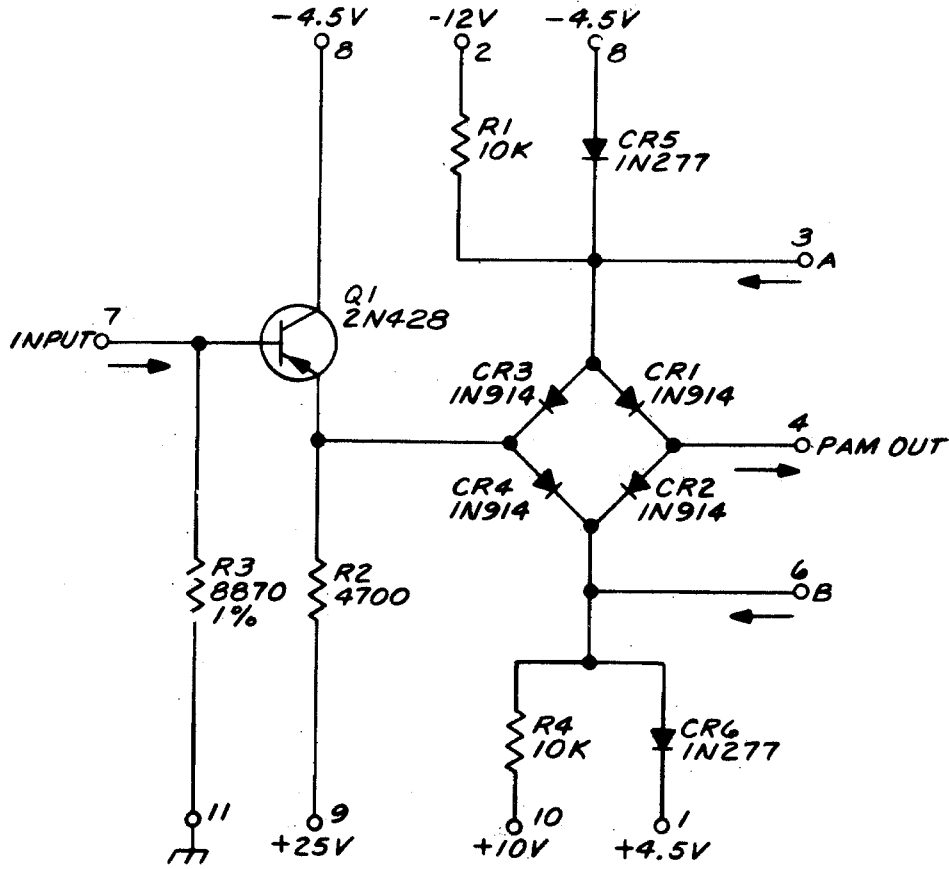
- (1) General. Unregulated dc input voltages are applied through jack J1 to the various series regulator circuits. The procedures given in (2), (3), and (4) below give a detailed description of the -4.5-volt regulator, which is typical of the other five regulators. This is followed by a discussion of the overload and protection circuits. The regulated output voltages are applied from the regulator circuits, through jack J1, to external circuitry. The input and output voltages and terminal designations of the six series voltage regulators are as follows:

TM 11-5805-367-35/3
C2

Series voltage regulator circuit	Input (vdc)	Input terminals, jack J1		Output (vdc)	Output terminal jack J1
		Positive terminal	Negative terminal		
+10 v	13.5	4	3	+10	4
-4.5 v	7	Ground	12	-4.5	22
+4.5 v	7.5	6	5	+4.5	6
+25 v	34	2	1	+25	2
-12 v	16	Ground	8	-12	20
-5.2 v	b -2	Ground	-12 V(B) c	-5.2	24

a Output voltages are between indicated output terminal and ground.
b Supplied by -12-volt series voltage regulator output terminal.

c -12 volt series voltage regulator output terminal.

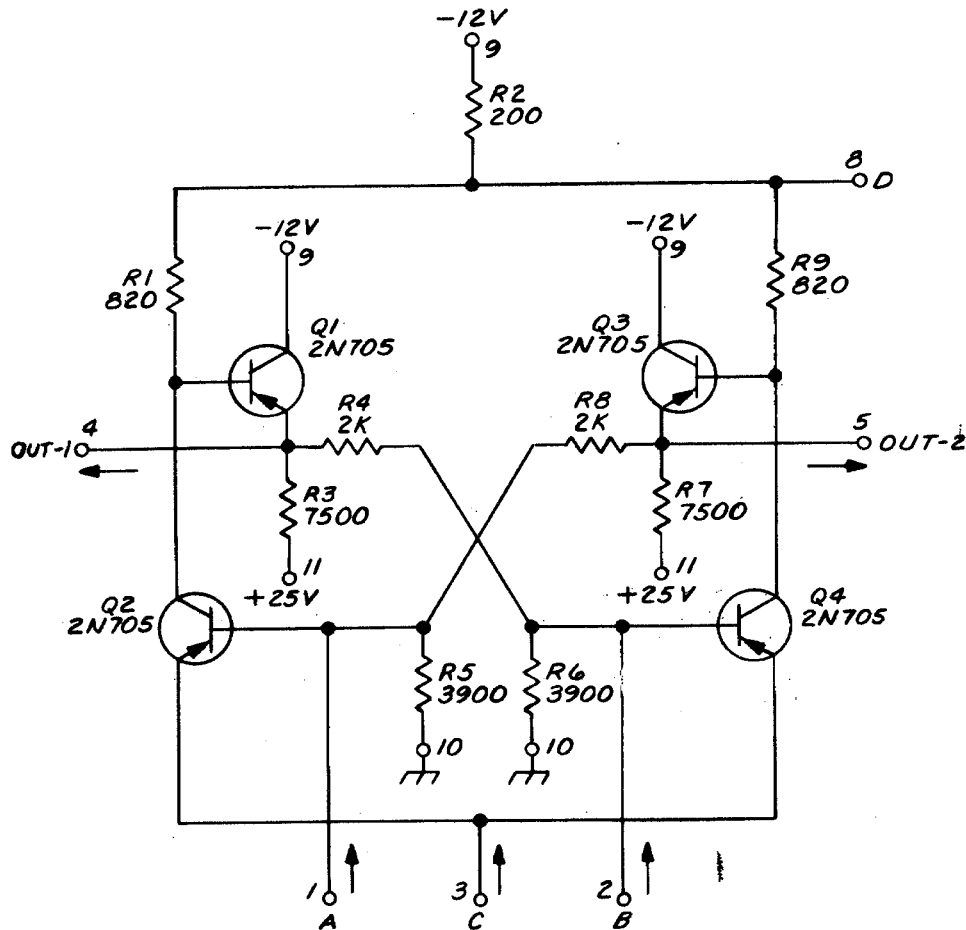


NOTE

RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-38

Figure 2-26. Transmit sampler module 38 schematic diagram.



NOTE

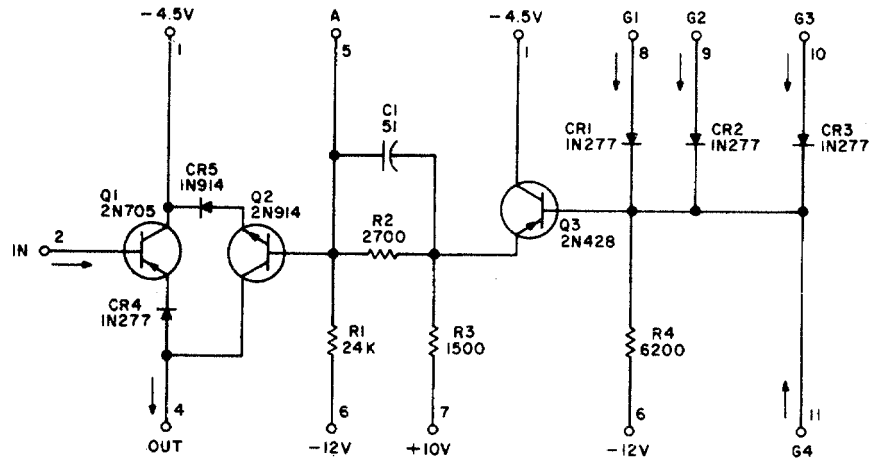
RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF, UNLESS OTHERWISE INDICATED.

TM 5805-367-35/3-39

Figure 2-27. Decision circuit module 42, schematic diagram.

(2) Series regulated circuit.

- (a) Input power to the -4.5-volt regulator is a -7.0-volt unregulated supply applied through terminal 12 (W2) of jack J1 to the collector of transistor Q6. The output of the regulator is taken from the emitter of transistor Q6 and appears at terminal 22 of jack J1. The output voltage is controlled by the current flow through transistor Q6 which, in turn is controlled by the voltage applied to its base. If the base voltage of transistor Q6 is at -4.5 volts, the output line will also be at -4.5 volts.
- (b) Breakdown diode VR2, resistor R14, and potentiometer R12 form a voltage divider, the output of which serves as a reference voltage in controlling the regulator output voltage. The reference voltage is stable and free of fluctuations in the -4.5-volt line because it obtains its power from the -12volt regulated supply. Break-down diode VR2 adds to the stability by regulating the voltage applied across potentiometer R12



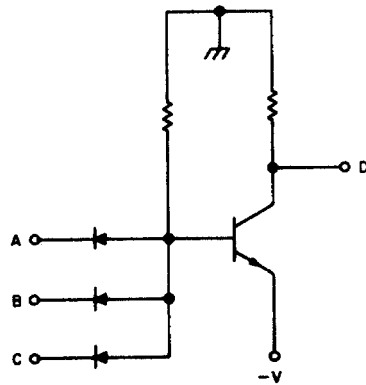
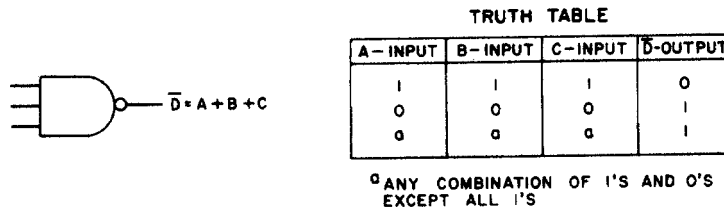
NOTES:

1. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
2. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS

TM 5805-367-35/3-C2-1

Figure 2-27.1. NOR gate module 46, schematic diagram

- (c) The output of the reference voltage divider is applied to the base of transistor Q8, which is one side of a conventional two-input differential amplifier. The second input to the differential amplifier is obtained from a voltage divider consisting of resistors R18 and R19, which are connected in series across the -4.5-volt regulator output. The junction of the two resistors in the divider is connected to the base of transistor Q9, which is the other side of the differential amplifier. Since the voltage divider is connected across the output of the regulator, any variations in the regulated output line produced by changing load conditions will cause a proportional voltage variation across the voltage divider. Therefore, the two inputs to the differential amplifier are a reference voltage, which remains constant, and the output of the voltage divider, which varies with changing output voltage conditions. If the voltage on the base of transistor Q9, (divider voltage) is more negative than the voltage on the base of transistor Q8 (reference voltage), conduction through transistor Q9 will increase and conduction through transistor Q8 will decrease. If the voltage on the base of transistor Q9 is more positive (less negative) than the base of transistor Q8, then the reverse condition will exist. The output of the differential amplifier appears at the collector of transistor Q9, and is connected to the base of transistor Q7, which acts as a buffer and driver. The output of transistor Q7 is taken from the emitter and is connected to the base of series regulator transistor Q6. Transistor Q6 determines the output voltage of the regulator because it acts as a variable

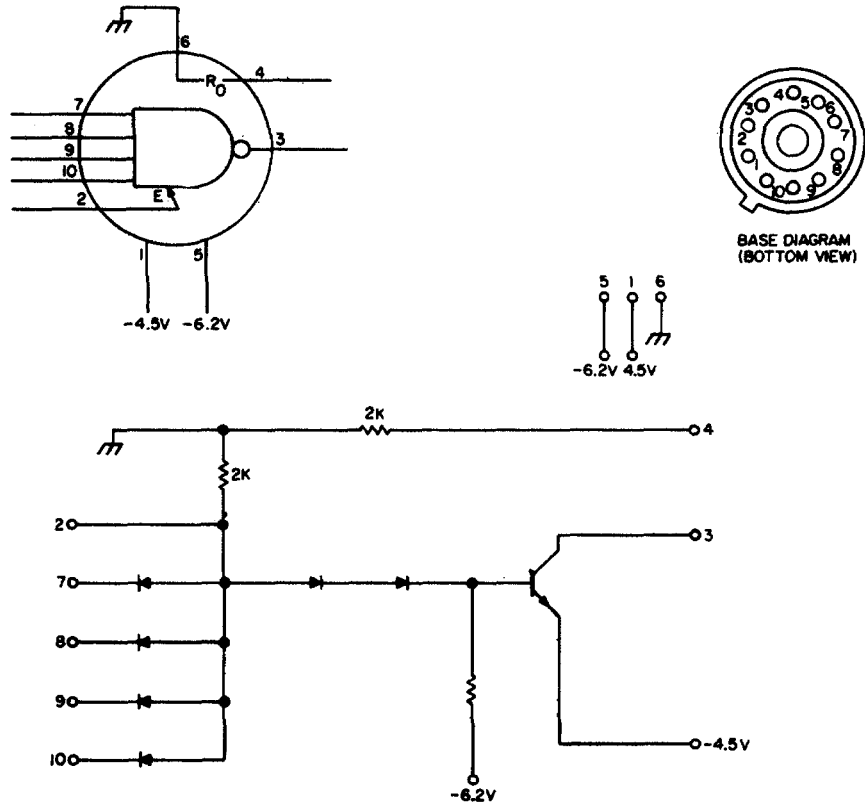


TM 5805-367-35/3-C-2-2

Figure 2-27.2. Basic NAND gate

resistance in series with the output line.

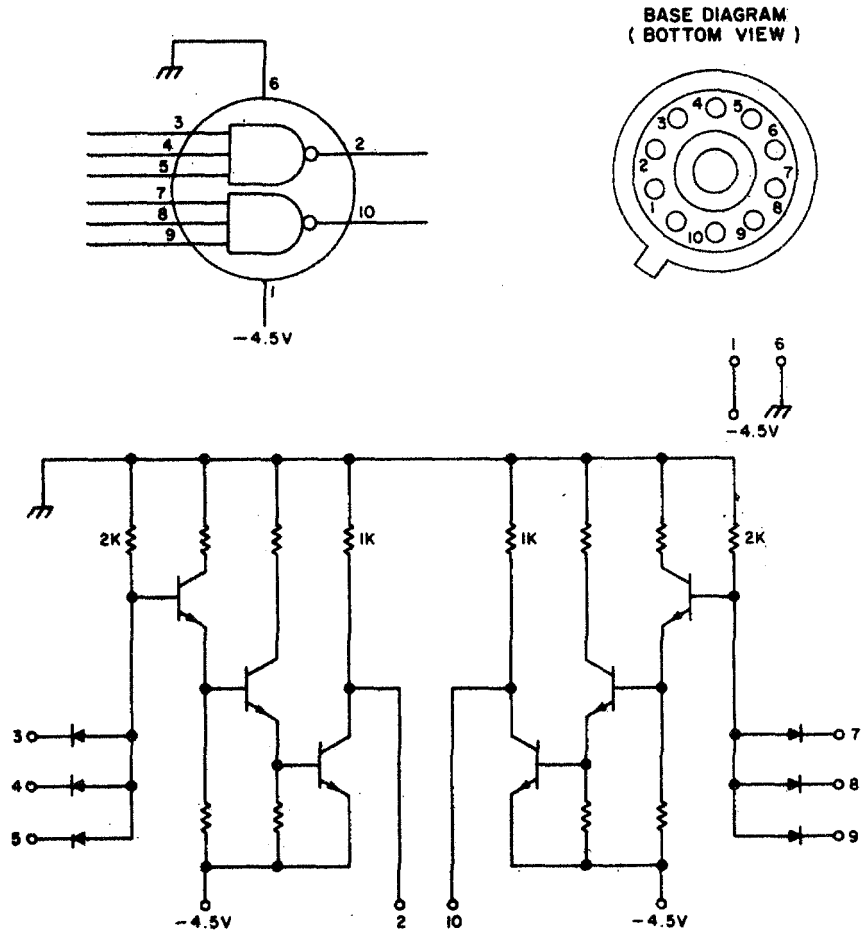
1. *Voltage increase.* When the voltage on the regulated output line increases, a proportional increase in voltage appears across the voltage divider (resistors R18 and R19) and is applied directly to the base of transistor Q9. If the base of transistor Q9 is more negative than the base of transistor Q8, transistor Q9 will conduct more heavily, causing its collector voltage to lower. This lower negative voltage is applied through driver transistor Q7 to the base of series regulator transistor Q6, causing it to conduct less and therefore lowering the voltage on its emitter. The decrease in the output voltage will be sufficient to cancel the voltage increase, thereby maintaining a constant -4.5-volt output.
2. *Voltage decrease.* When the output of the regulator is below -4.5 volts, the circuit operates as described in 1 above, except that the lower negative voltage causes transistor Q9 to conduct less. The higher negative collector voltage on Q9, in turn, causes transistor Q6 to conduct more heavily, increasing the output to -4.5 volts.



TM 5805-367-35/3-C2-3

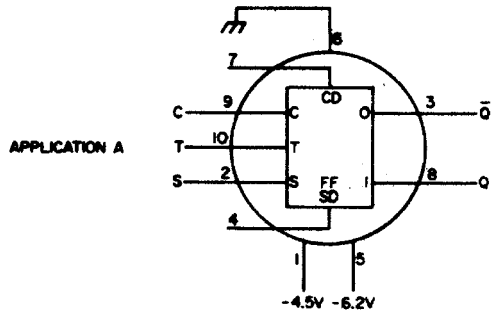
Figure 2-27.3. NAND gate SE101K, basic application and schematic diagram

- (3) *-5.2-volt series voltage regulator over- protection.* A fault in the -5.2volt series voltage regulator circuit can drive series regulator transistor Q31 into saturation. This would normally cause, the output voltage at terminal 24 of jack J1 to rise from -5.2 volts to nearly -12 volts, resulting in damage to externally connected circuits. To prevent damage, breakdown diode VR5 is included in the -5.2-volt series voltage regulator and acts to limit the maximum output voltage to -6.2 volts in the event of circuit failure.
- (4) *Automatic short circuit protection circuit.*
- (a) If the -12-volt power fails, the six series voltage regulators become inoperative because they require inputs from the -12-volt source. A short circuit across the output of one or more series voltage regulators (except for the -5.2-volt series voltage regulator) is detected by the automatic short circuit protection circuit. This circuit immediately cuts off the -12 volt series voltage regulator, cutting off all regulated dc power (including -5.2 volts) to external circuitry.

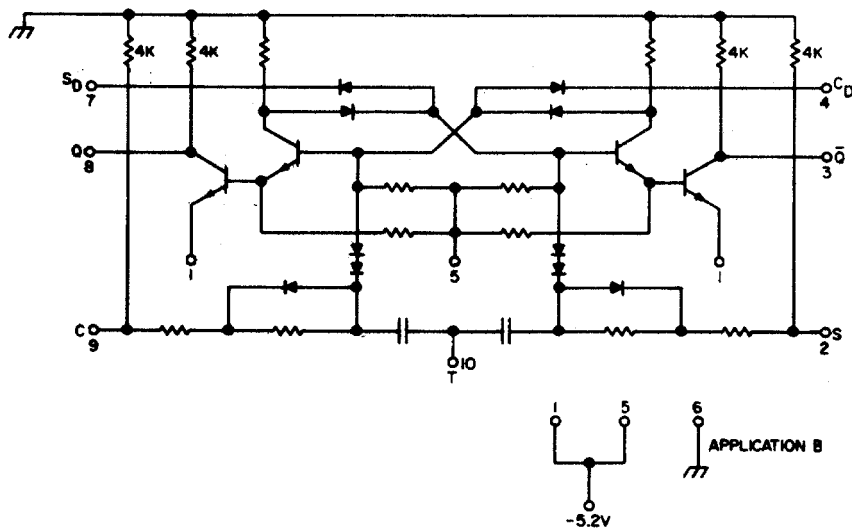
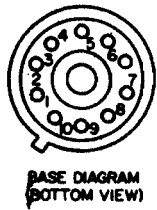
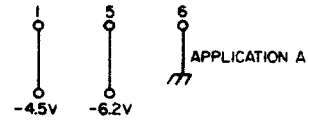
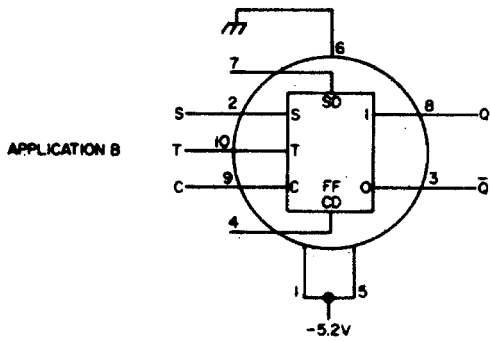


NOTE:
COMPONENT VALUES SHOWN ARE TYPICAL
TM 5805-367-35/3-C2-4

Figure 2-27.4. High fan-out dual NAND gate SE113K, basic application and schematic diagram

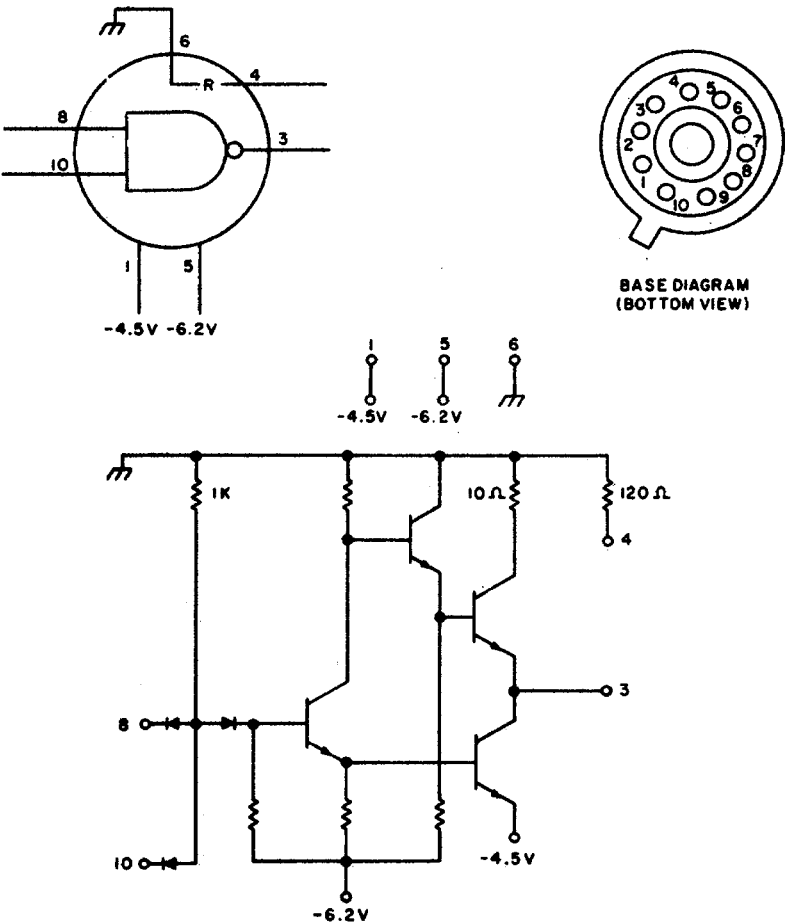


TRUTH TABLE			
S	C	Q	Q̄
0	0	INDETERMINATE	
0	1	0	1
1	0	1	0
1	1	NO CHANGE	



TM 5805-367-35/3-C2-5

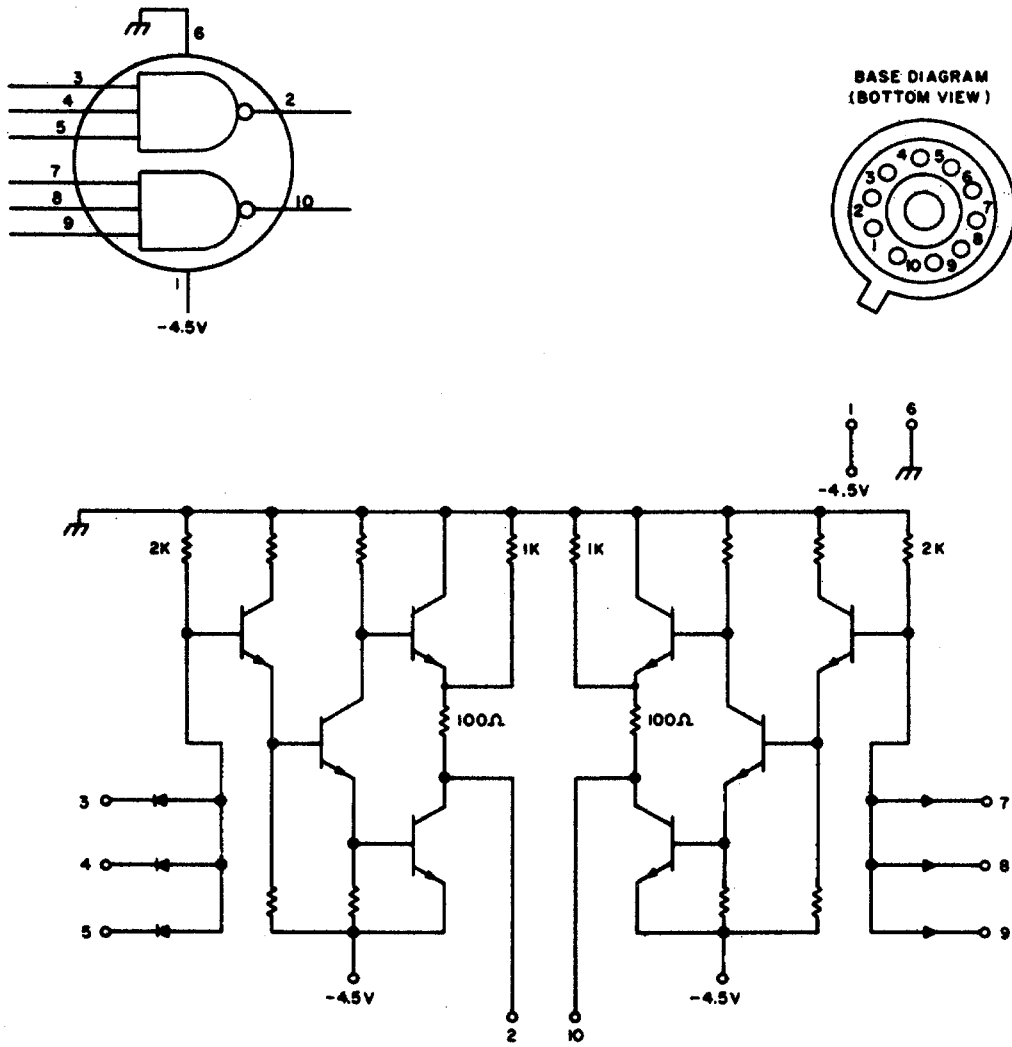
Figure 2-27.5. Flip-flop SE124K, basic application and schematic diagram



TM 5805-367-35/3-C2-6

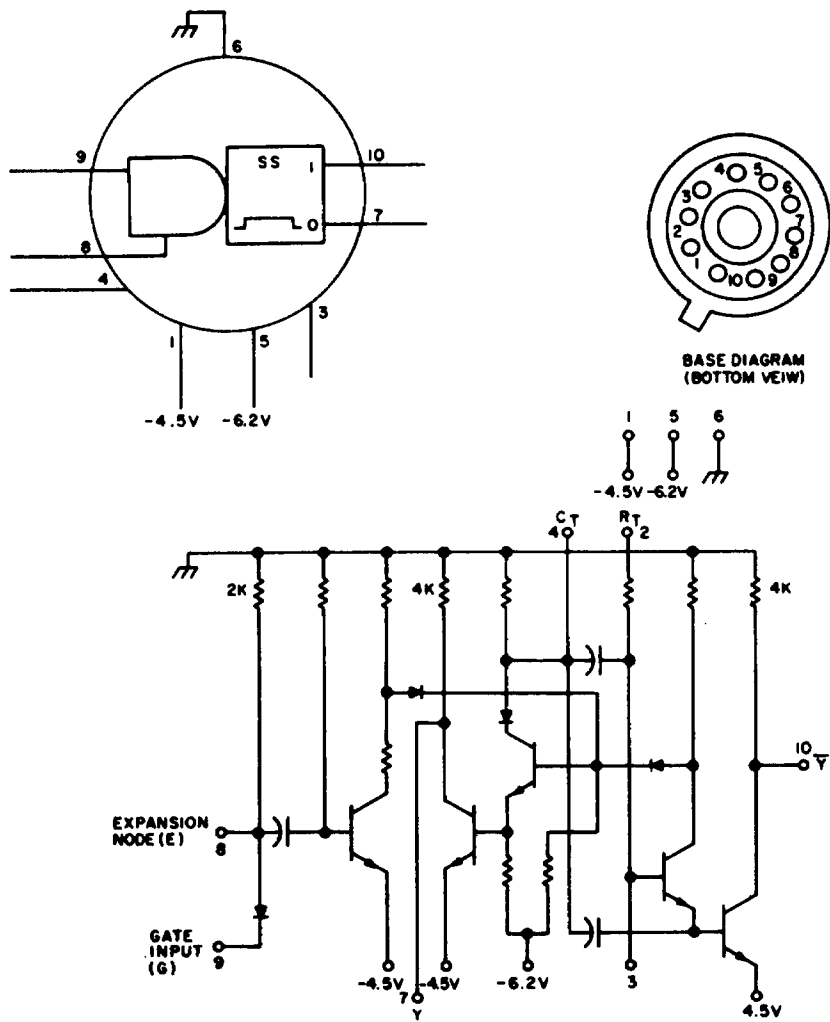
Figure 2-27.6. Line driver SE150K, basic application and schematic diagram

TM 11-5805-367-35/3
C2



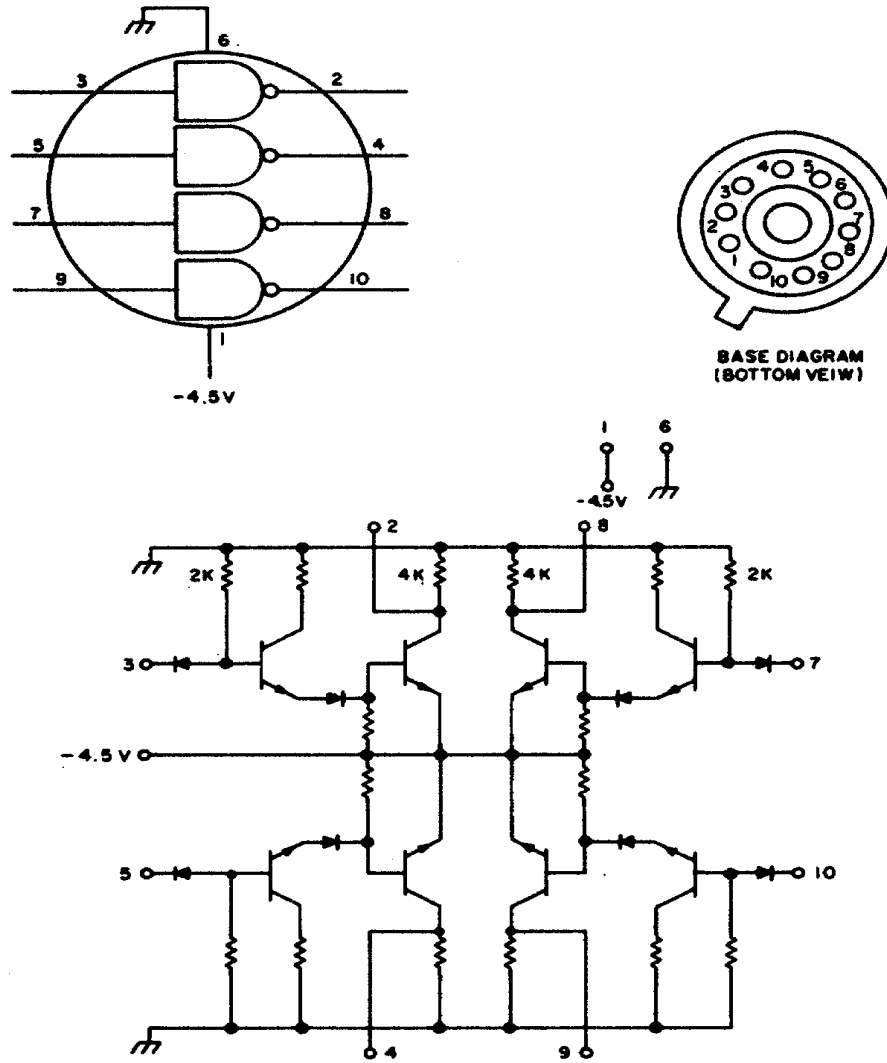
TM 5805-367-35/3-C2-7

Figure 2-27.7. NAND gate module SE157K, basic application and schematic diagram



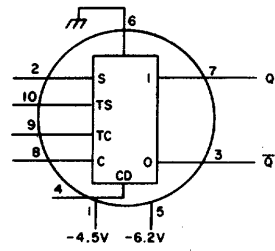
TM 5805-367-35/3-C2-8

Figure 2-27.8. Monostable multivibrator SE160K, basic application and schematic diagram



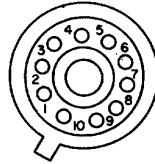
TM 5805-367-35/3-C2-9

Figure 2-27.9. NAND gates SE181K, basic application and schematic diagram

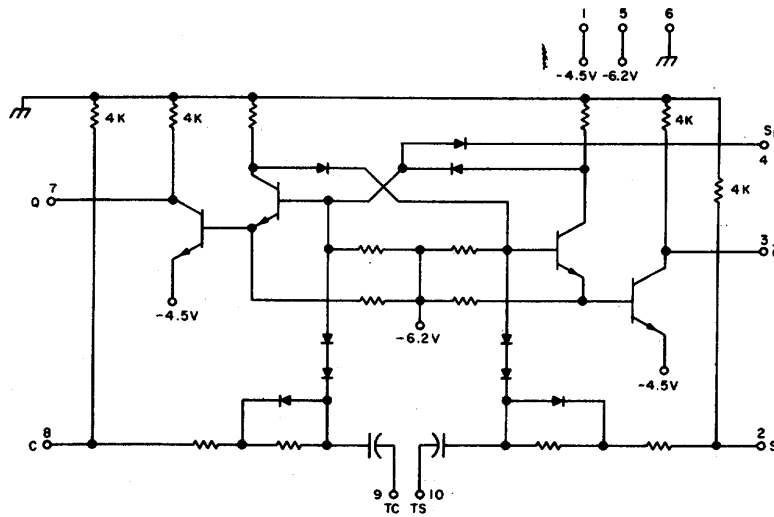


TRUTH TABLE					
TS	TC	S	C	Q	\bar{Q}
-	a	1	1	1	0
a	-	1	1	0	1
-	a	0	0	0	NO CHANGE
a	-	0	0	0	NO CHANGE

^a NEGATIVE TRIGGER PULSE



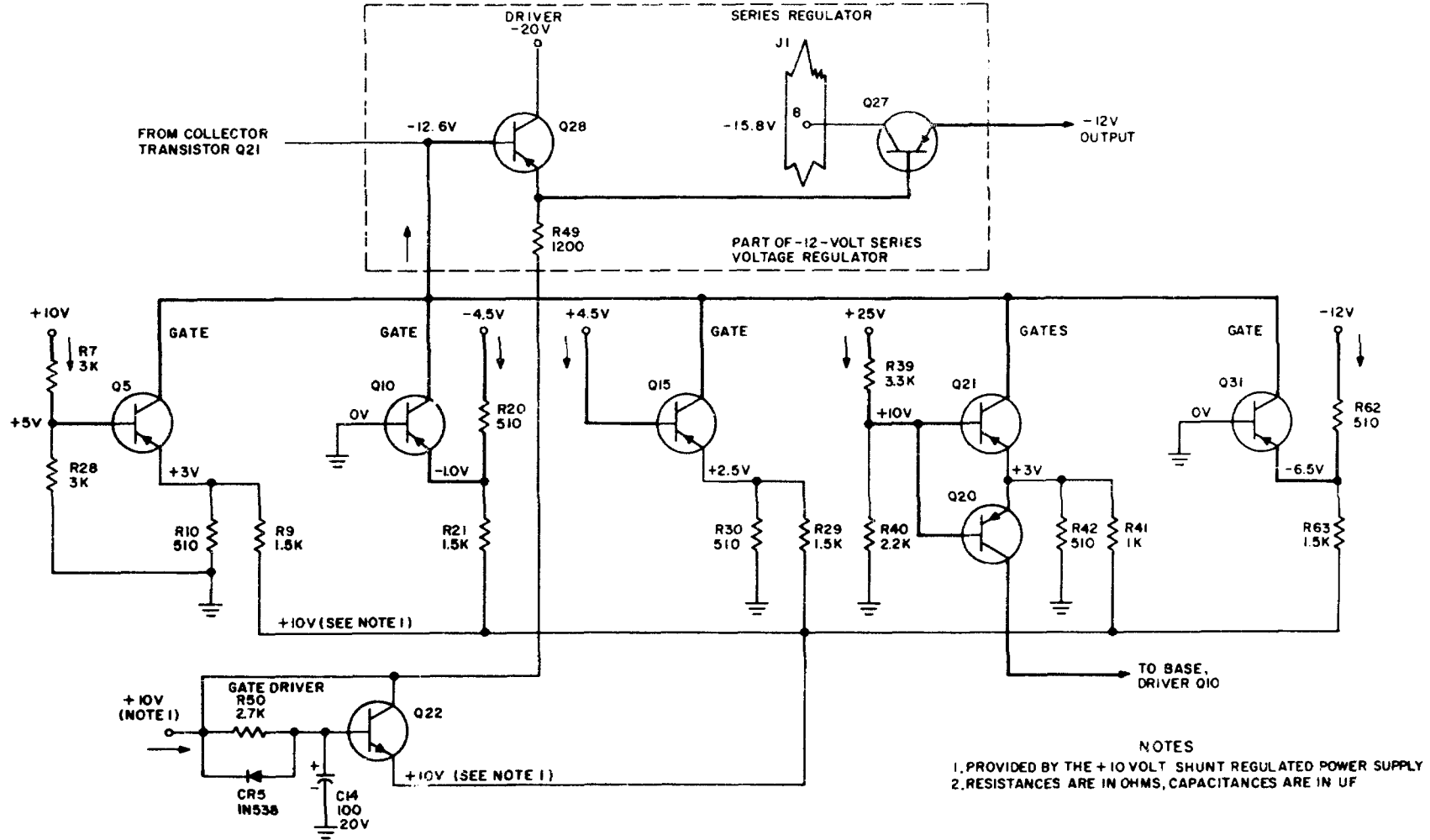
BASE DIAGRAM
(BOTTOM VIEW)



TM5805-367-35/3-C2-18

Figure 2-27.10. Flip-flop CS704K, basic application and schematic diagram

- (b) Figure 2-28 is a schematic diagram of the automatic short circuit protection circuit. This circuit controls driver transistor Q28. As an added means of protecting external circuitry, the automatic short circuit protection circuit provides a separate gate (transistor Q20) to control driver transistor Q17 of the +25-volt series voltage regulator. This gate insures rapid cutoff of the +25-volt power when a short occurs.
- (c) Gate driver transistor Q22 controls power from the +10-volt shunt regulated power supply to gate transistors Q5, Q10, Q15, Q20, Q21, and Q31. This power provides forward bias for the emitter-base junction of these gates. During normal operation, the gates are cut off and each of their emitter-base junctions is reverse-biased by one of the series voltage regulator outputs. The gates, when cut off, have no effect on the bases of driver transistor Q28 or Q17. The base of driver transistor Q28 is held at approximately -12.6 volts, controlled by the collector of transistor Q29 (part of differential amplifier transistors Q29 and Q30). This holds the emitter of driver transistor Q28 and the base of series regulator transistor Q27 at approximately -12.3 volts and the series regulator output at -12 volts.
- (d) The base of driver transistor Q17 is held at approximately -0.8 volt by the associated differential amplifier. This maintains the +25-volt series voltage regulator operating normally.
- (e) Assume that a short circuit occurs across the -4.5-volt series voltage regulator output, reducing it to 0 volt. With the -4.5-volt bias now removed from resistor R20, the emitter of gate transistor Q10 shifts positive. This positive shift forward biases the emitter-base junction of gate transistor Q10, causing it to turn on and approach saturation. This action shifts the voltage at the base of driver transistor Q28 from -12.6 volts to approximately +2 volts. The +volt level causes the emitter of driver transistor Q28 and the base of series regulator transistor Q27 to shift to approximately +1.7 volts, cutting off series regulator transistor Q27 and driving the -12-volt series voltage regulator output toward 0 volt. This action causes the remaining five series voltage regulator outputs to shift toward 0 volt.
- (f) With the +25-volt bias at resistor R39 now decreasing, the emitter-base junction of gate transistor Q20 shifts from reverse to forward bias, causing gate transistor Q20 to turn on and approach saturation. When the +25 volts at R39 decreases to 0 volt, the collector of gate transistor Q20 and the base of driver transistor Q17 shift from -0.6 volt to approximately +2 volts. The action of gate transistor Q20 now insures rapid cutoff of the +25-volt power.
- (g) When the -12-volt power decreases to 0 volt, all series voltage regulators are disabled and their outputs reduced to 0 volt.
- (h) To restore normal operation to the series voltage regulators after removing the short circuit across the -4.5-volt series voltage regulator output, it is necessary to momentarily defeat the automatic short circuit protection circuit. This is accomplished by briefly interrupting the main power to the unit.
- (i) When the main power is removed, capacitor C14, connected between the base of gate driver transistor Q22 and ground, is rapidly discharged through diode CR5 and the +10-volt shunt regulated supply. When power is reapplied, capacitor C14 starts to charge through resistor R50. Because of the increase in resistance capacitance (rc) chargetime (compared to the discharge time), capacitor C14 charges slower than it discharged. During this chargetime, the six series voltage



TM5805-367-35/3-43

Figure 2-28. Automatic short circuit protection circuit, simplified schematic diagram.

regulators attain normal operation and full output voltage. This immediately reverse biases all gates, cutting them off before bias power from the emitter of gate driver transistor Q22 can attain its operating value of + 10 volts and again disable the series voltage regulators.

2-34. Double Modem Panel 1A2/2A2

(fig. 6-45)

a. *General.* Each 1A2/2A2 panel provides modulation and demodulation for two 2-way audio channels. When there is a difference in pulse repetition rates, frequencies, voltages, or figure references depending on whether the panel is used in Multiplexer TD-352/U or TD-353/U, the information for the TD-353/U is given first, followed by a parenthetic reference applicable to the TD-352/U. The interrelationships between the panel input and output signals are shown in figures 6-38 and 6-40 (figs. 6-33 and 6-35).

- (1) Each demodulating circuit accepts a 0.3 to 3.5-kc audio signal at a level of -4 decibels (referred to 1 milliwatt in 600 ohms) (dbm) and converts it to a train of 2.5-microsecond (5.2-microsecond) pam samples occurring at an 8-kc rate. These samples assume the instantaneous peak amplitude of the audio signal at the time of sampling and can be any value from +2.8 to -2.8 volts at the modulating circuit output.
 - (2) Each demodulating circuit samples a tdm-pam signal and extracts a train of 2.6-microsecond (5.2-microsecond) sam pies at an 8-kc rate. These audio samples have peak amplitudes at any one of 64 levels between -1.24 and + 1.24 volts. The demodulating circuits convert these samples to a 0.3- to 3.5-kc audio signal, with a nominal 0.5-volt rms level at the demodulator output. This output is adjustable up to 1.5 volts.
 - (3) The double modem consists of two identical assemblies, MDM1 (modem 1) and MDM2 (modem 2), each containing modulating and demodulating circuits.
 - (4) The MDM1 modulator circuit consists of input transformer T1, PAM potentiometer R1 and resistor R2, sampler Z1 (module 38), and gate Z2 (module 01).
 - (5) The MDM1 demodulator circuit consists of gate Z3 (module 01), sampler Z4 (module 37), low-pass filter FL1, AG potentiometer R7, feedback amplifiers Z5 (module 31) and Z6 (module 32), buffer transistor Q1, and output transformer (2),.
 - (6) The MDM2 modulator circuit consists of input transformer T3, PAM potentiometer R11 and resistor R12, sampler Z7 Z7 (module 38), and gate Z8 (module 01).
 - (7) The MDM2 demodulator circuit consists of gate Z9 (module 01), sampler Z10 (module 37), low-pass filter FL2, AG potentiometer R17, feedback amplifiers Z11 (module 31) and Z12 (module 32), buffer transistor Q2, and output transformer T4.
- b. *Theory.* Since assemblies MDM1 and MDM2 are identical, the following discussion applies to both.
- (1) *Modulator section.*
 - (a) The audio signal is applied through terminals 1 and 2 of jack J5 to the balanced primary of transformer T1. Transformer T1 steps up the audio signal by a factor of 4.
 - (b) At terminal 3 of transformer T1, the dc level of the audio signal is set to a value between 0 and - 0.45 volt by PAM potentiometer R1. This dc level adjustment insures that, when no audio signal is present at terminals 1 and 2 of jack J5, the pam output at terminal 4 of sampler Z1 (module 38 para 2-31) will be at 0 volt.
 - (c) The audio signal at terminal 3 of transformer T1 is applied to terminal 7 of sampler Z1. Capacitor C1 is a low-pass filter that attenuates all signals above 50 kc.
 - (d) Two timing signals are also applied to the modulator section. One timing signal, consisting of 4.5-volt positive going pulses of 2.6-microsecond (5.2 microsecond) duration occurring at 20.8-microsecond intervals, is coupled through terminal 11 of jack J7 to terminal 2 of gate Z2 (module 01, para 2-13). The other timing signal, consisting of 4.5-volt positive-going pulses of 20.8-microsecond duration occurring at 125-microsecond intervals, is coupled through terminal 12 of jack J5 to terminal 2 of gate Z2.

- (e) The audio signal to terminal 7 of sampler Z1 is normally cut off from reaching terminal 4 of sampler Z1 and modulator output terminal 9 of jack -J5. When the two timing signals to gate Z2 are simultaneously at a positive level, a bias signal is produced across terminals 9 and 6 of gate Z2. This bias signal occurs once every 125 microseconds for a duration of 2.6 microseconds (5.2 microseconds) and is applied across terminals 3 and 6 of sampler Z1. Terminals 7 and 4 of sampler Z1 are now electrically shorted together, causing the audio signal to be applied to terminal 9 of jack J5.
 - (f) After 2.6 microseconds (5.2 microseconds), the timing signal at terminal 2 of gate Z2 shifts negative, sharply cutting off the bias signal from gate Z2 to sampler Z1. Terminals 4 and 7 of sampler Z3 again appear open circuited, therefore removing the incoming audio signal from the modulator output at terminal 9 of jack J5. When succeeding gated bias signals occur, new audio samples are gated to the modulator output.
- (2) *Demodulator section.*
- (a) A tdm-pam signal is fed through terminal 7 of jack J5 to terminal 4 of sampler Z4 (module 37, para 2-30). Two timing signals are supplied to the demodulator section simultaneously. One timing signal, consisting of 4.5-volt positive-going pulses of 2.6-microsecond (5.2-microsecond) duration occurring at 20.8-microsecond intervals, is coupled through terminal 8 of jack J5 to terminal 3 of gate Z3. The other timing signal, consisting of +4.5volt positive-going pulses of 20.8 microsecond duration occurring at 125-microsecond intervals, is coupled through terminal 21 of jack J5 to terminal 2 of gate Z3.
 - (b) Between samplings, the tdm-pam signal appearing at terminal 4 of sampler Z4 is prevented from reaching terminal 10 of sampler Z4. During this time, capacitor C2 (connected between terminal 5 of sampler Z4 and ground) stores the last pam sample as a dc voltage.
 - (c) When the two timing signals to gate Z3 are simultaneously at a positive level, a bias signal is produced across terminals 6 and 9 of gate Z3. This signal occurs once every 125 microseconds for a duration of 2.8 microseconds (5.2 microseconds) and is applied across terminals 3 and 6 of sampler Z4.
 - (d) When a bias signal occurs, terminals 4 and 5 of sampler Z4 are shorted together. The voltage across capacitor C2 now assumes the level of the pam signal appearing at terminal 4 of sampler Z4. After 2.6 microseconds (5.2 microseconds), the timing signal at terminal 2 of gate Z3 shifts sharply negative, cutting off the bias signal from gate Z5 to sampler Z4. Terminals 4 and 5 of sampler Z4 again appear open-circuited, removing the incoming pam signal from storage capacitor C2. The stored voltage across capacitor C2 now remains almost constant (due to the high rc discharge time of C2), until succeeding bias signals are applied to sampler Z4. When the succeeding bias signals occur, new pam samples are gated to the output of sampler Z7. These samples serially form an unfiltered, coherent audio signal.
 - (e) The voltage across capacitor C2, representing the pam sample, is amplified in sampler Z4 and fed-out of terminal 10 to low-pass filter FL1. Low-pass filter FL1 limits the high frequency response of the pam samples to 3.5 kc, removing the steplike character of the signal and leaving audiofrequency voltages only.

- (f) The audio signal is coupled from lowpass filter FL1 to AG potentiometer R7. This control is adjusted to produce a 0.1414-volt rms level (at its wiper arm) which is applied to terminal 2 of amplifier Z5 (module 31, para 2-25). The audio signal is amplified in amplifier Z5 and fed from terminal 3 of amplifier Z5 to terminal 3 of amplifier Z6 (module 32, para 2-26). Module Z6 amplifies the audio signal, which then appears at terminal 10 of amplifier Z6 with a 1.0-volt rms level. The audio output of amplifier Z6 is coupled through buffer transistor Q1 and appears at its emitter at the same 1.0-volt rms level.
- (g) The signal is coupled from buffer transistor Q1 to the output circuitry and, in addition, is fed back to amplifier Z5 along two parallel paths. Both feedback signals stabilize the gain through amplifiers Z5 and Z6.
- (h) The signal from buffer transistor Q1 to the output circuitry is divided between resistor CR9, and the primary of output transformer (2). A 0.5-volt rms signal appears across the primary of output transformer (2). The stepped-up signal which appears across the secondary of output transformer (2), is coupled to terminals 3 and 4 of jack J5 as a balanced signal.
- (i) The 1.0-volt rms audio signal, appearing at the junction of capacitor C7 and resistor CR9,, is also fed through resistor CR10 and terminal 5 of jack J5 to output-level-measuring circuits for monitoring purposes.

2-35. Pcm Output Circuits, Panel 1A3/2A3

(fig. 6-47)

a. *General.* Panel 1A3/2A3 pcm output circuits inserts the address information as the last digit of each frame in the pcm pulse train to be transmitted.

b. *Address Insertion.* Pcm A pulses are applied from the coder via terminal 4 of jack J6 to diode CR1 in AND gate CR1-CR2. The address pulse at terminal 30 of jack J6 occurs at the same time as the last digit in the pcm frame. The address pulse is inverted by transistor Q9 and applied to AND gate diode CR2. This pulse inhibits the AND gate, effectively blanking out the last digit of the pcm frame. The pcm output of the AND gate, with the last digit blank, is buffered by transistor Q1 and applied to diode CR4 in OR gate CR4-CR6.

c. *Development of Transmit 2-kc or 4-kc Address Signal.* The transmit 2-kc or 4-kc address digit- to be inserted at the end of each frame of the pcm pulse train is derived from an 8-kc signal. The application of this input signal to panel 1A3/2A3 is controlled by the ADDRESS switch. When the switch is set to the SLAVE position, the 8-kc signal is applied to terminal 17 of J6. From this point the signal is applied to pin 3 of flip-flop Z1 (module 18, para 2-20). This module divides the signal by two, producing a 4-kc signal at pins 10 and 11. This 4-kc signal is applied to pin 3 of a second flip-flop Z2 (module 18, para 2-20) where it is again divided by 2 to produce the desired 2-kc signal required for gating with the address pulse. The output of flip flop Z2 appearing at pins 10 and 11 is applied to diode CR6. which is part of the transmit address digit gate consisting of CR6. and CR9 (d below). When the ADDRESS switch is set to the MASTER position, the 8-kc signal is applied to terminal 24 of J6. From this point the signal is applied to pins 5 and 8 of flip-flop Z2 via steering diodes CR10 and CR11 respectively. Flip-flop Z2 divides the 8-kc signal by 2, producing at pins 10 and 11 the desired 4-kc-signal required for gating with the address pulse. This signal is also applied to diode CR6. in the transmit address digit gate.

d. *Transmit Address Digit Gate.* The transmit address digit gate consists of diodes CR6. and CR9. The inputs to this diode AND gate are the address signal which is applied to CR6. and is either a 2-kc or 4-kc signal, and the address pulse applied to CR9 from terminal 30 of J6. This gate produces an output only when the address pulse and either the 2-kc or 4-kc address signal are coincident, which occurs at the end of each frame. The gate output is the transmit address digit which is buffered by transistor Q4 and applied to diode CR6 in OR gate CR4-CR6. This gate inserts the transmit address digit in the last digit position of the pcm frame.

e. *Final Development of Pcm Output.* The pcm A signal with the transmit address digit is buffered by transistor Q2. From the output of transistor Q2, the signal takes two paths, one to diode CR13 in AND gate CR13-CR14, and the other through inverter transistor Q3 to diode CR15 in AND gate CR14-CR15. The sampling clock at terminal 3 of jack J6 is connected to diode CR12 in AND gate CR12-CR13, enabling this AND gate whenever the pcm A signal is positive, and to diode CR14 in AND gate CR14-CR16, enabling this AND gate whenever the inverted pcm A signal is positive.

The sampled pcm A signal is buffered by transistor Q5 and applied to terminal 3 of flip-flop Z3; the sampled inverted pcm A signal is buffered by transistor Q6 and applied to terminal 8 of flip-flop Z3. The output at terminals 1 and 2 of flip-flop Z3, which is the retimed pcm A signal with transmit address, is applied via driver transistor Q7 and buffer transistor Q8 to terminal 1 of jack J6 as the pcm out signal.

f Monitoring F Signal. A portion of the output of flip-flop Z2 appearing at pins 10 and 11 is applied to terminal 14 of J6 through resistor R3. This signal is termed MONITOR F and gives an indication of address digit activity by causing the front panel TEST ALIGN meter pointer to register in the green area when the meter selector switch is set to SERV FAC and the SERV SEL switch is set to the F position.

2-36. Coder Timing (HT), Panel 1A5

(fig. 6-49)

a. General. Coder timing panel 1A5 is used in conjunction with coder panel 1A6/2A6 to convert the pam signal to a pcm signal. There are three separate circuits on the panel: one for generating the decision pulses, one for generating timing signals T1 through T6, and one for generating the compander control signals. In addition, a T6B signal is developed from the T6 signal. All of the outputs of panel 1A5 are applied to coder panel 1A6/2A6. The procedures given in b, c, and d below describe the development of the various outputs of panel 1A5.

b. Development of Decision Pulses Signal. The reshaped clock signal is a continuous train of pulses at a 2.304-mc rate and is applied from terminal 5 of jack J4 to the base of emitter follower transistor Q1. The output of transistor Q1 is delayed 0.1 μ sec by delay line DL1 and is then buffered by transistor Q2. The signal is next inverted by transistor Q3 and applied to buffer transistor Q4. The output of transistor Q4 is thus a delayed, inverted, and buffered version of the reshaped clock signal. This signal is applied from transistor Q4 through resistor R39 to terminal 9 of jack J4 and is designated as the decision pulses signal.

c. Development of T1 Through T6 and $\overline{T6B}$ Signals. The P1 signal, a 384-kc positive-going pulse train, is applied from terminal 28 of jack J4 to diode CR4, which is part of a two-input AND gate consisting of diodes CR4 and CR12. The input to diode CR12 is the coder clock signal. When the coder clock signal and the P1 signals coincide, which will occur for approximately 100 nsec (or the pulse width of the coder clock signal), the signal is applied to the base of buffer transistor Q8. Diode CR13 functions to insure that only the P1 signal is applied to the AND gate. Any extraneous signals are grounded out through diode CR13. The output of buffer transistor Q8 is applied through capacitor C11 and diode CR5 to pin 8 of flip-flop Z1 (module 18, para 2-20). The coder clock signal is applied to pin 3 of flip-flop Z1. When the output of transistor Q8 and the coder clock signal coincide, flip-flop Z1 is triggered, producing a positive-going signal on pin 2. This signal is applied through buffer transistor Q13 to terminal 27 of jack J4 as the leading edge of the T2 signal. The flip-flop will remain in the same state until the next coder clock pulse is applied to pin 3 of flip-flop Z1. At that time, the flip-flop reverts back to its original condition and the signal on pin 2 will be -4.5 volts. This is applied through transistor Q13 to terminal 27 as the trailing edge of the T2 signal. The result is a 0.43- μ sec signal which coincides with the coder clock signal. The output from pin 2 of flip-flop Z1 is also applied to pin 11 of flip-flop Z2 (module 18). Its complement on pin 10 of flip-flop Z1 is applied to pin 1 of flip-flop Z2. The coder clock signal is applied to pin 3 of flip-flop Z2. Flip-flop Z2 develops the T3 signal in essentially the same as flip-flop Z1 developed T2, except that the inputs to pins 1 and 8 are from flip-flop Z1. When pin 2 of flip-flop Z1 goes to -4.5 volts, pin 10 goes to 0 volt and this 0-volt signal is applied to pin 1 of flip-flop Z2. When a coder clock signal coincides with the signal applied to pin 1 of flip-flop Z2, a positive-going signal is produced.

at pin 2 Of flip-flop Z2 and applied to terminal 26 of jack J4 as the leading edge of the T3 signal. When the next coder clock signal is applied to pin 3, the flip-flop reverses states, producing the trailing edge of the T3 signal. Flip-flops Z3, Z4, Z5, and Z6 operate identically to form signals T4, T5, T6, and T1, respectively. The T6 signal is also applied to the compander control circuits (d below) and to inverter transistor Q9. The output of inverter transistor Q9 is applied to flip-flop Z7 (d below) and through buffer transistor Q10 to terminal 19 of jack J4 as the $\overline{T6B}$ signal.

d. *Development of $\overline{\text{Compander Control}}$ and $\overline{\text{Compander Control}}$ Signals.* The compander control circuits control the bridge circuits on panel 1A6/ 2A6 which, in turn, determine whether the pam signal is to be amplified or attenuated. The main input to the compander control circuits is the *compander reset* signal on terminal 13 of jack J4, which comes from the compander control circuits on panel 1A6/2A6. This signal indicates whether the amplifier or attenuator should pass the signal, while the bridge circuit on panel 1A6/2A6 does the actual controlling. The signal from terminal 13 is applied through resistor R20 to diode CR6. It forms one part of an AND gate with capacitor C16. When this signal is a logic 1 (ground level), the diode will pass the coder clock signal which is present, therefore resetting the flip-flop. Also applied to flip-flop Z7 (at pin 3) is the $\overline{T6B}$ signal, which is derived from the T6 signal as described in c above. The $\overline{T6B}$ signal appears at the beginning of the coding cycle. It sets flip-flop Z7 in the state that allows the pam signal to pass through the amplifier on panel 1A6/2A6. The outputs of flip-flop Z7 are on pins 2 and 10 and complement each other. These flip-flop outputs are applied to a differential amplifier consisting of transistors Q11 and Q12. The outputs of the differential amplifier are applied to buffer transistors Q15 and Q16 and then to terminal 17 of jack J4 as the *compander control* signal, and to terminal 15 of jack J4 as the *compander control* signal.

2-37. Coder Timing (M.T.), Panel 2A5

(fig. 6-51)

a. *General.* Coder timing panel 2A5 is used in conjunction with various other panels to convert the pam signal to a pcm signal. There are two main circuits on the panel: one generates the compander control signals which are applied to panel 2A6, and one generates pcm A and pcm B which are applied to panel 2A3. In addition, $\overline{T6B}$ is developed, and a third circuit on the panel develops the 8-kc aux signal.

b. *Development of $\overline{\text{Compander Cont}}$ and $\overline{\text{Compander Cont}}$ Signals.* The compander control circuits control the bridge circuit on panel 1A6/2A6 which, in turn, determines whether the pam signal is to be amplified or attenuated. The main input to the compander circuits is the *compander reset* signal which is applied to terminal 31 of jack J6 from panel 1A6/2A6. This signal will indicate whether the amplifier or attenuator should pass the pam signal, while the bridge circuit on panel 1A6/2A6 does the actual controlling. The signal from terminal 31 is applied through resistor R1 to diode CR1 and forms one part of an AND gate with capacitor C1. When this signal is a logic 1 (ground level), the diode will pass the coder clock signal which is present on terminal 30 of jack J6, therefore resetting the flip-flop. In addition to the compander reset signal, the $\overline{T6B}$ signal is applied to flip-flop Z1. The $\overline{T6B}$ signal is developed from the T6 signal, which is applied to terminal 22 of jack J6. From terminal 22, the signal is applied through inverter transistor Q2 and buffer transistor Q1 to pin 3 of flip-flop Z1. This signal occurs at the beginning of the coding eyelet It sets flip-flop Z1 in the state that allows the pam signal to pass through the amplifier on the 1A6/2A6 panel. The outputs of flip-flop Z1 are on pins 2 and 10 and complement each other. The flip-flop outputs are applied to a differential amplifier consisting of transistors Q3 and Q4. The output of differential amplifier transistor Q3 is applied through buffer transistor Q8 to terminal 23 of jack J6 as the *compander cont* signal. The output of differential amplifier transistor Q4 is applied through buffer transistor Q9 to terminal 29 of jack J6 as the *compander cont* signal.

c. *Development of Pcm A and Pcm B Signals.* The pcm A and pcm B signals are developed from five input signals: FF9-1, FF-0, shift 1, shift 2, and parallel shift, all applied to jack J6. The FF9-1 and FF-0, signals are applied from panel 1A6/2A6 and indicate whether each pcm bit is a logic 1 or a logic 0. The shift 2 and parallel shift signals are applied from panel 2A8 and are developed as described in paragraph 2-42. The shift 1 signal is applied from panel 2A9 and is developed as described in paragraph 2-44. The

complete circuit consists of six flip-flops, five located on panel 2A5 (flip-flops Z2 through Z6) and one located on panel 1A6/2A6 (Z2). The signals are developed from the output of the decision circuit, and are applied to pins 1 and 8 of flip-flop Z2 on panel 1A6/2A6 (fig. 6-53). Flip flop Z2 is one of three flip-flops into which the first three bits of the six-bit pcm train are loaded. The output of flip-flop Z2 is on pins 2 and 10 and is applied to terminals 2 and 28 of jack J18 and designated the *FF9-1* or *Pcm A* and *FF-0*, or *Pcm B* signals. These signals are applied through terminals 10 and 2 of jack J6 on panel 2A5 (fig. 6-51) to pins 1 and 11 of flip-flop Z4. The output of flip-flop Z4 is on pins 2 and 10 and is applied to pins 1 and 11 of flip-flop Z6. The pcm bits are serially shifted into these three Flip flops by the shift 1 signal from terminal 4 of jack J6. When flip-flops Z2 (panel 1A6/2A6) (fig. 6-53), Z4, and Z6 are loaded with the first three bits, the parallel shift signal is applied to terminal 3 (fig. 6-51) of flip-flops Z2, Z3, and Z5. This signal parallel shifts the three bits in flip-flops Z2 (1A6/2A6), Z4, and Z6 into flip-flops Z2, Z3, and Z5, respectively. At this time, the fourth, fifth, and sixth bits are loaded into flip-flops Z2 (1A6/2A6), Z4, and Z6 the same as the first three bits. The first three bits are serially shifted out of Flip flops Z2, Z3, and Z5 by the shift 2 signal and applied from pins 2 and 10 of flip-flop Z5 to terminals 1 and 13, respectively. The pcm A signal appears at terminal 1, and the pcm B signal-at terminal 13. When the first three bits are shifted out, the parallel shift signal is again applied to shift the fourth, fifth, and sixth bits from flip-flops Z2 (1A6/2A6), Z4, and Z6 to flip-flops Z2, Z3, and Z5. These signals are then shifted out of the circuit the same as the first three bits. This process is repeated for each six-bit pcm signal. Because of the rate at which the shift 2 pulses occur (576 kc), the output pcm pulses are twice as wide as the input pcm pulses.

d. *Development of 8-Kc Aux Signal.* The *8-kc aux* signal is developed from the *address pulse*, *sampling clock*, and *address pulse* signals which are applied to terminals 20, 19, and 17, respectively, of jack J6. These signals trigger flip-flop Z7 (module 18) to produce a pulse similar to the input address pulse shifted by the sampling clock at pin 10 of flip-flop Z7. The signal is 1.736 μ sec wide and occurs every 125 μ sec. The signal is buffered by transistors Q5 and Q6, which are connected in parallel, and applied through capacitor C17 and resistor R21 to output buffer transistor Q7. The output of buffer transistor Q7 is applied to terminal 18 of jack J6 and designated *8-kc aux*. This signal is applied to the TO AUX connector for use by an auxiliary unit.

e. *Development of T6B Signal.* The $\overline{T6B}$ signal is developed from the T6 signal which is applied from terminal 22 of jack J6 to inverter transistor Q2. The output of transistor Q2 is applied through buffer transistor Q1 to terminal 27 of jack J6 and designated $\overline{T6B}$. The $\overline{T6B}$ signal is also applied to pin 3 of flip-flop Z1 as described in b above.

2-38. Coder Circuits, Panel 1A6/2A6

(fig. 6-53)

a. *General.* The coder circuits operate to convert the pam signal into a pcm signal compatible with Multiplexers TD-352/U and TD-353/U. Four main coder circuits are located on panel 1A6/2A6: the amplifier/attenuator circuit, decision circuit, compander control circuit, and ladder network. These are described in b through e below.

b. *Amplifier/Attenuator Circuits.* The main input to the panel is the *coder pam* signal on terminal 31 of jack J18. This signal is applied to two feedback dc amplifiers with a common input. Both amplifiers are dc amplifiers with gains of 6.67 and 0.333, respectively (the ratio of gain between the amplifier and attenuator being 20 to 1). The *coder pam* signal is applied to the amplifier through resistor R1, part of a feedback network (consisting of resistors R1 and R2 and capacitor C1) which controls the gain of the amplifier. From resistor R1, the signal is applied to the base (pin 2) of transistor Q1 which amplifies the signal and applies it to amplifier transistor Q2. From transistor Q2, the signal is applied through buffer transistor Q3 to the bridge circuit. Located in the base circuit of one transistor Q1 is potentiometer CR6, labeled CCL. Its function is to shift the output of the amplifier to center it midway in the coding range, that is, between levels 31 and 32. The *coder pam* signal is applied to the attenuator through resistor R22, which together with resistor R21 is part of a feedback network controlling the gain of the circuit. From resistor R22, the signal is applied to the differential

amplifier stages composed of transistors Q6 and Q7. From transistor Q6 the signal is applied through diode VR1 to buffer transistor Q8. From buffer transistor Q8, the signal is applied to the bridge circuit. ID, the base circuit of Q7 is a potentiometer R26 labeled CA. Its function is to center the attenuator with respect to the amplifier output so that all pcm levels are obtained. The attenuator is switched in when the pam amplitude is between pcm levels 0 to 15 or 48 to 63. The amplifier is switched in when the pam amplitude is between pcm levels 16 to 47. The CA potentiometer shifts the output of the attenuator so that a continuous transition is made between levels occurring in the amplify region and attenuate region. Therefore, it is adjusted so that pcm levels 16 and 16 and 47 and 48 are obtained. The bridge circuit contains two separate bridges: one consisting of diodes CR7 through CR10 in the amplifier line, and one consisting of diodes CR12 through CR15 in the attenuator line. The *compander control* and $\overline{\text{compander control}}$ signals, which are complements of each other, are applied through steering diodes CR16 through CR19 to control the current flow in the two bridge circuits. If the *compander control* signal is negative and the $\overline{\text{compander control}}$ signal is positive, steering diodes CR16 and CR19 will conduct, therefore applying a negative voltage at the junction of diodes CR7 and CR8. and a positive voltage at the junction of diodes CR9 and CR10. This causes the bridge circuit to be cut off, preventing the amplifier signal from getting through. Steering diodes CR17 and CR18 are cut off so that the attenuator signal is allowed to pass through transistor Q8, capacitor C6, and resistor R33 to buffer transistor Q9, from where it is applied to the decision circuit (c below). If the *compander control* signal is positive and the $\overline{\text{compander control}}$ signal is negative, steering diodes CR17 and CR18 conduct and CR16 and CR19 are cut off so the bridge in the amplifier line is conducting and the signal from transistor Q3 is applied through capacitor C6 and resistor R33 to buffer transistor Q9 for application to the decision circuit.

c. *Decision Circuit.* The decision circuit consists of pulse shaper transistors Q4 and Q5, differential amplifier transistors Q10 and Q11, and decision circuit module Z1 (module 42, para 2-32). The decision circuit develops the pcm signal by applying the output of the decision circuit on pins 4 and 5 of Z1 to pins 3 and 8 of flip-flop Z2 (module 18), depending on whether the signal from the amplifier/attenuator circuits or the ladder circuits is higher in amplitude. The *decision pulses* are applied through terminal 8 of jack J18 to the pulse shaper circuit, consisting of transistors Q4 and Q5. From the pulse shaper circuit the decision pulses are applied to pin 3 of decision circuit Z1. The input to pin 3 is the main input to the decision circuit; the two inputs applied to the module from the differential amplifier will act to apply this input either to pin 4 or 5 of decision circuit Z1, depending on which input is higher. The signal from the amplifier/attenuator circuit is applied to the base of differential amplifier transistor Q10, and the signal from the ladder network is applied to differential amplifier transistor Q11, If the signal applied to the differential amplifier from the ladder network is higher than that applied from the attenuator/amplifier circuit, transistor Q10 will conduct, causing decision circuit Z1 to apply no pulse to pin 4 and a pulse to pin 5 in coincidence with the decision pulses. These signals are applied to pins 3 and 8, respectively, flip-flop Z2 (module 18, para 2-20). If the attenuator/amplifier signal is higher than the ladder network signal, the opposite occurs.

d. *Companding Control Circuits.* The companding control circuits operate to generate the compander reset signal which is applied to panel 1A5 or 2A5 to generate the compander control and $\overline{\text{compander control}}$ signals (b above). The circuit consists of buffer transistors Q15, Q16, and Q17 and AND gates diodes CR30 through CR35. Basically, the circuit consists of two 3-input AND gates. If either AND gate has three logic 1 (0-volt) inputs, an output is applied to buffer transistor Q15 or Q16, for application to terminal 4 of jack J18 as the *compander reset* signal. The pcm A and pcm B signals are applied from the decision circuit to AND gates diodes CR30 and CR33, respectively. For the development of these signals refer to c above. Two signals are applied from clamping flip-flop Z3 (in the ladder network), which essentially indicate if the first decision was a logic 1 (pcm A) or a logic 0 (pcm B). If it was a logic 1, a logic 1 signal is applied from terminal 7 of module Z3 through buffer transistor Q17 to AND gate diode CR31. If it was a logic 0, a logic 1 signal is applied from

terminal 6 of module Z3 to AND gets diode CR34. The T2, signal is applied from terminal 11 of jack J18 to an AND gate diode in each gets (CR32 and CR35). The compander circuits operate to compress the pcm signal if it exceeds a predetermined limit. This limit is equal to a level indicated by the first two bits of the pcm train (11 or 00, the upper limit and lower limits, respectively). The compander circuits are designed to produce a logic 1 signal if either one of these conditions is met. The AND gate consisting of diodes CR30, CR31, and CR32 produces an output if the first two bits are logic 1's, the AND gate consisting of diodes CR33, CR34, and CR35 produces an output if the first two bits are logic 0's. If there is an output from either of the gates, the *compander reset* signal is a logic 1. This will cause the bridge in the amplifier/attenuator circuits to pass the attenuated signal. However, the AND gates in the compander circuits do not operate until signal T2 (or after the second decision is made). Therefore, initially the bridge circuit will always pass the amplified signal. If the *compander reset* signal is a logic 1, once the bridge is in the attenuate position it will remain there until coding of that channel is completed. In the gate consisting of diodes CR30, CR31, and CR32, if the input to diode CR30 from the decision circuit is a logic 1 during time T2, (indicating that pcm A is a logic 1) and the input to diode CR31 from the ladder network is a logic 1 (indicating that pcm A was logic 1 during time T1) when the T2 signal is applied to diode CR32 a logic 1 is applied to buffer transistor Q15. The output of transistor Q15 is applied to terminal 4 of jack J18 as the *compander reset* signal. In the second gate (consisting of diodes CR33, CR34, and CR35), if the input to diode CR33 is a logic 1 during time T2 (indicating that pcm A is a logic 0) and the input to diode CR34 is a logic 1 (indicating that pcm A was a logic 0 during time T1) when the T2 signal is applied, an output is applied from the AND gate to buffer transistor Q16. The output of transistor Q16 is applied to terminal 4 of jack J18 as the *compander reset* signal.

e. *Ladder Network*. The ladder network consists of a series of binary weighted resistors and associated components. If the input to the first leg of the ladder network is 1 volt the output is $\frac{1}{2}$ volt, and if the input to the second leg is 1 volt the output is $\frac{1}{4}$ volt, and so on. Since there are six legs in the ladder, the total number of discrete levels available (using the outputs from the ladder network in every possible combination) is 64. In actual practice, -5.2 volts is applied to each leg, so that the output from the first resistor is -2.6 volts, from the second -1.3 volts, and so on. The output from the ladder network is shifted 2.6 volts by a level shifter consisting of resistors R39 through R42, capacitor C6, and breakdown diode VR2. Because of the level shift, level 32 (the 32d of the 64 possible levels) is equal to 0 volt when the signal is applied to the decision circuit. The voltages applied to each of the six resistors are cumulative. Generally, the voltage is applied to each resistor in the network as long as the total voltage from the ladder does not exceed the voltage level of the pam signal applied to the decision circuit. If the ladder voltage exceeds the pam level, the voltage is removed from the resistor that raised the ladder voltage above the pam level, This occurs for signals T1, T2, T3, T4, and T5 (resistors R43, R45, R45, R47, and R48, respectively). During time T6 there is always a voltage applied to resistor R49 in the ladder network because this is the last decision to be made; all-that is to be determined is whether the pam signal is above or below the ladder voltage. The result of the operation of the ladder network is that after the coding operation is completed, the output of the ladder network is the one level of the 64 levels that is closest to the pam signal. The circuitry that applies the voltage to the ladder network is described in (1) through (4) below.

- (1) *Development- of T1 level*. The first level in the ladder network is developed by resistor R43. The voltage is applied to this resistor from clamping flip-flop Z3 (module 25). Initially, module Z3 is triggered by the T6 signal applied to pin 14; this causes a 0-volt level at pin 7 which is connected to resistor R43. The signal from resistor R43 is applied through the level shifter to one side of the differential amplifier in the decision circuit. The pam signal is applied to the-other side. If the pam input is higher than the ladder network signal, then the decision circuit develops a logic 1 at pin 10 of flip-flop Z2

(pcm A) and a logic 0 at pin 2 (pcm B). The signal from pin 2 is applied to the AND gate consisting of diodes CR39 and CR40. The *coder clock* signal is also applied to this AND gate. Since the signal applied from module Z2 is a logic 0, the output of the AND gate is also a logic 0. At this time, 0 volt is still applied to resistor R43; to remove it, module Z3 must be triggered at pin 4 by a logic 1. A signal is applied to pin 4 only when there is an output from the AND gate consisting of CR39 and CR40 and when the T1 signal is applied to resistor R93. When the pam signal is higher than the ladder network signal, there is no input to this gate and module Z3 is not triggered. As a result, during time T1 the first bit of the pcm signal will be a logic 1. If the ladder network is higher than the pam signal, then the signal applied to the AND gate from the decision circuit is a logic 1. When the other input to the gate is a logic 1 (*coder clock*), there is a logic 1 output from the AND gate which is applied through capacitor C34 to pin 4 of module Z3, when the T1 signal is also present. This signal will trigger module Z3, removing 0 volt from resistor R43; this voltage level in turn is applied to the decision circuit, causing the first pcm bit to be a logic 0.

- (2) *Development of T2, level.* Initially, 0 volt is applied to resistor R45. As soon as the first decision is completed, -5.2 volts is applied to resistor R45 and the second decision is made. If the first decision was a logic 1, a logic 0 is applied to pin 6 of module Z3. This signal is applied to diode CR36 of an OR gate consisting of diodes CR36 and CR37. The other input to the OR gate (at diode CR37) is the T2, signal. The output of the OR gate is applied to inverter transistor Q19 and buffer transistor Q18. From buffer transistor Q18, the signal is applied to inverter transistor Q14 and current clamp Q13, from which it is applied to resistor R45 in the ladder network. Therefore, during time T2,, -5.2 volts is applied to resistor R45. Now the second decision is made, and one of four situations can arise depending on the first decision.
- (3) *Development of T3 through T5 levels.* The T3 through T5 levels are developed essentially the same as the T1 pulse ((1) above). Initially, each clamping flip-flop is triggered to apply a 0 volt to the resistor connected to pin 7 of each module by the T6B signal previous to the one being generated. For example, module Z4 generates the T3 level for application to the decision circuits. Before the decision circuits generate a signal to control it, the T2, signal applied to pin 11 triggers module Z4 which applies a 0-volt signal to resistor R45. After the decision circuit generates a signal, that signal is applied through the AND gate consisting of CR39 and CR40, where it is gated with the coder clock signal and applied to pin 4 of each module. Also applied to each module is the T3 signal for module Z4, the T4 signal for module Z5, and the T5 signal for module Z6. These signals are applied to pin 4 of each module, also. Since each of these modules was initially in the zero state and applying -5.2 volts to the ladder resistors, the pcm B signal must be logic 1 and the coder clock signal and the correct T signal must be present, for the module to switch and remove the -5.2 volts from the ladder network.
- (4) *Development of T6 level.* The T6 level is developed from the T6B signal applied to terminal 15 of jack J18. The signal is applied through current clamp Q21, Q22 to resistor R49 and is at -5.2 volts (a logic 0). This signal is a logic 1 only during time T6.

f. *Idealized Waveforms.* Idealized waveforms for the panel are shown in figure 2-29.

2-39. Pam Reshaper (H.T.), Panel 1A7 (fig. 6-55)

a. *General.* Pam reshaper panel 1A7 is part of the transmit section of the TD-353/U. The function of the panel is to alternately sample one channel, while it is storing and feeding to the coder the

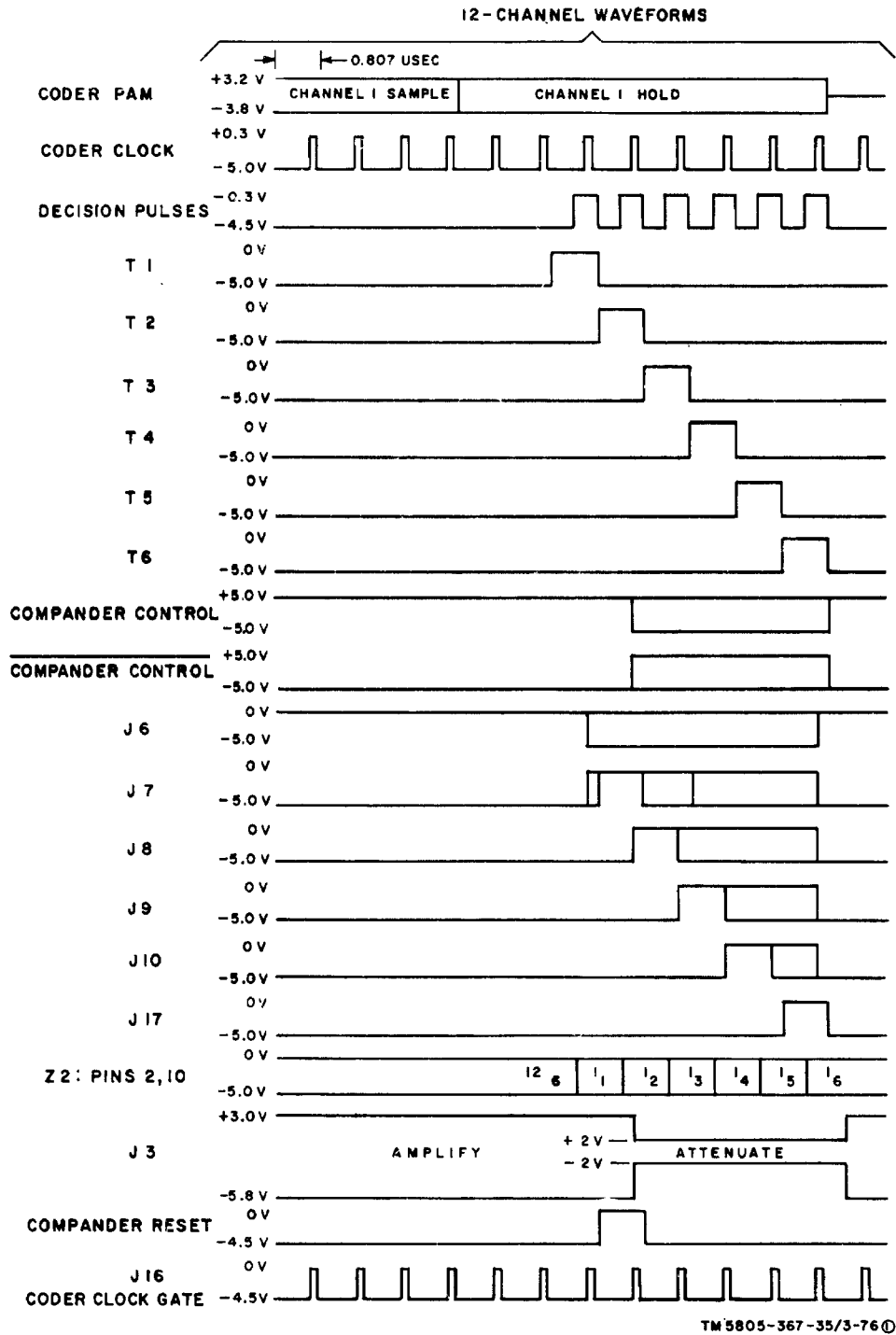


Figure 2-29①. Panel 1A6/2A6, idealized waveforms (part 1 of 2).

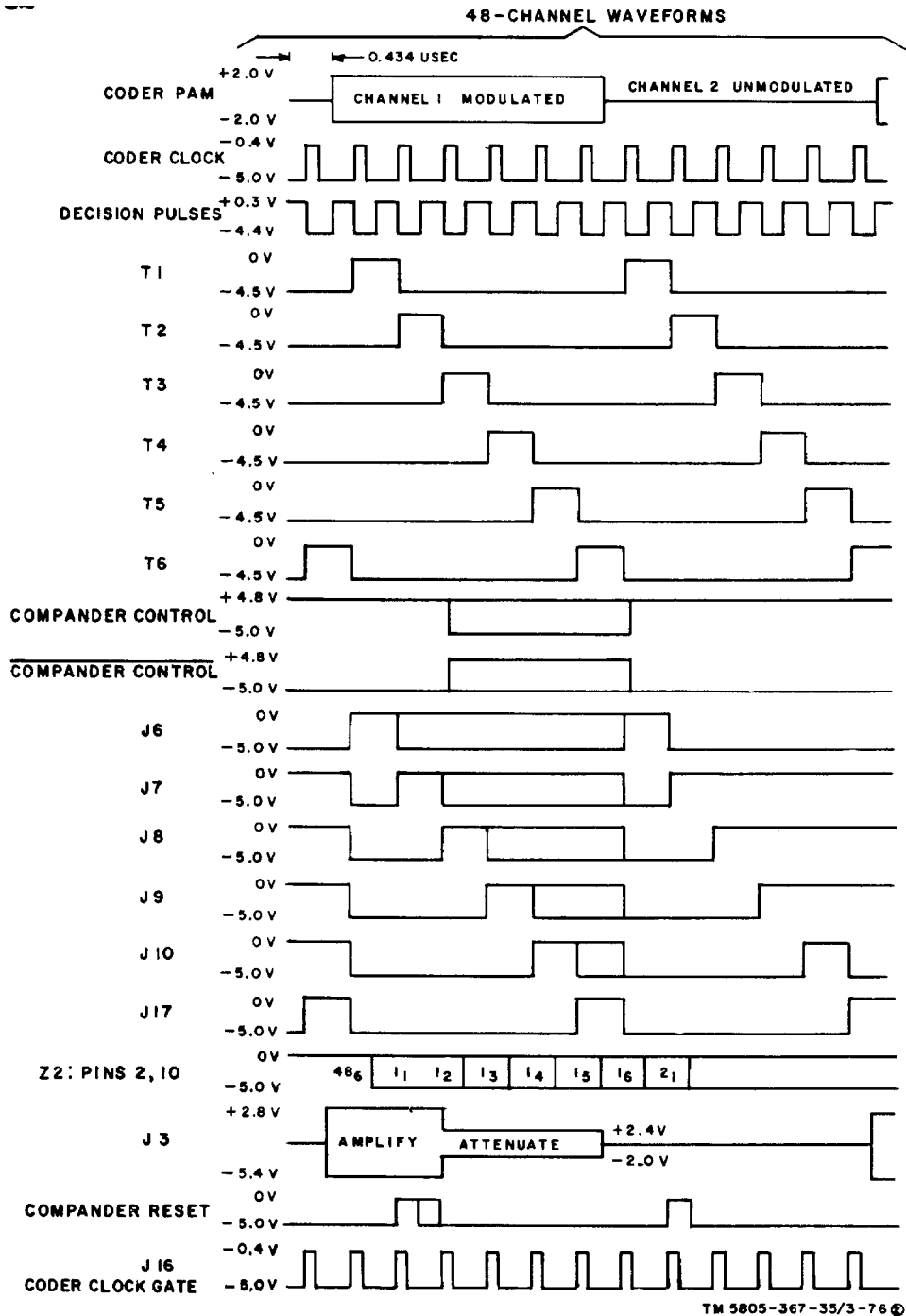


Figure 2-29. Panel 1A6/2A6, idealized waveforms (part 1 of 2).

sample from the previous channel. The circuit then reverses and feeds to the coder the sampled channel and proceeds to sample a new channel. There are two similar circuits on the panel, one for the odd channels and one for the even channels. At any one time, when one circuit is sampling, the other is feeding out the previously stored sample.

b. *Transmit Pam (Even Channels)*. One of the two principal inputs to the panel is the *transmit pam (even channels)* signal which is applied to

terminal 25 of jack J4. This signal consists of a wavetrain of pam pulses with a 2.6- μ sec width and a rate of 142 kc. The transmit pam signal is not flat as it enters the panel. To reduce the possibility of errors in the coder, the signal must be flat before being coded. To accomplish this, a capacitor is charged to the final value of the sampled signal, and this level is held constant throughout the coding cycle.

- (1) The pam input signal is applied through resistor R1 to the base of buffer transistor Q1 along with the clipped noise signal which is applied from terminal 24 of jack J4 through resistor R2 to the base of transistor Q1. This signal is buffered through transistor Q1 and applied to a bridge network consisting of diodes CR1, CR2, CR3, and CR4. The bridge acts as a switch. When it conducts, it rapidly charges capacitor C2 to the final value of the transmit pam signal. When the bridge cuts off, it presents a high impedance to the capacitor so that the stored charge takes a long time to leak off. The switching of the bridge network is controlled by the FF4 signal, which causes it to bridge alternately to conduct and cut off. The FF4 signal is applied from the secondary of transformer T1 across the bridge, and consists of 192-kc square waves. The development of this signal is described in *c* below. During the 2.6- μ sec positive excursions of the FF4 signal, the bridge network conducts and samples the pam signal entering at the junction of diodes CR1 and CR4. Capacitor C2, which receives the output of the bridge network, stores the output for the required 2.6- μ sec interval. The pam pulses charge the capacitor at a rapid rate, but once the bridge is turned off, the capacitor will discharge at a slow rate. This delay in the discharge will tend to hold the amplitude of the stored signal on capacitor C2 at a constant level during the coding process. To overcome any imbalance in the bridge circuit, a feedback circuit (*d* below) is provided.
- (2) The potential across capacitor C2 is applied to buffer transistors Q2 and Q3. The output of the emitter of transistor Q3 is divided into two branches: one branch provides a feedback signal to the base of transistor Q9 (*d* below), and the other branch (the principal one) goes to gate transistor Q4. Transistor Q4 operates in conjunction with gate transistor Q5 to either pass or not pass the pam signal to transistor Q10. This is controlled by the FF4 signal which enters the circuit at the base of transistor Q5 (*c* below). The bias for the base of transistor Q5 is provided by the output of transistor Q6 and varies from +4.5 to -4.5 volts. The gate circuit passes the pam signal during the positive-going excursions of the FF4 signal applied to the base of transistor Q5. The output, from the emitters of transistors Q4 and Q5, is applied through capacitor C5 to the base of buffer transistor Q10. The bias on the base of buffer transistor Q10 is controlled by ECL potentiometer R30. This potentiometer is adjusted to minimize the dc differences between the odd channel pcm and the even channel pcm signals.
- (3) The output of transistor Q10 is taken from the emitter and is combined with the pam (odd) signal (*e* below). The combined pair is coupled through capacitor C31 to the base (pin 2) of differential amplifier transistor Q17, which consists of two matched transistors in one case. The output of the differential amplifier is from pin 6 of transistor Q17 (the collector of the second transistor) and is applied through breakdown diode VR3 to the base of buffer transistor Q18. The output of the buffer transistor is from the emitter and is applied to terminal 22 of jack J4 as the *coder pam* signal. The output is also applied through resistor R61 to terminal 26 of jack J4 as the *coder pam mon* signal. The output signal will consist of a continuous train of pulses alternating between even channels and odd channels.

c. FF4 Signal. The FF4 signal is applied through terminal 15 of jack J4 to the base of buffer transistor Q7. The output of the buffer is from the emitter and is applied to two circuit points. One branch is coupled through capacitor C6 to the base of driver transistor Q8. The output from the driver is coupled from the emitter through capacitor C10 to pin 3 of transformer T1. The secondary of the transformer (pins 1 and 2) is connected across the bridge circuit as described in *b* above. A feedback circuit is also added to the input of the bridge circuit as described in *d* below. The other output from buffer transistor Q7 is applied to the base of inverter transistor Q6. The output of transistor Q6 is an inverted and amplified version of the input and is applied to the base of transistor Q5 as described in *b*(2) above.

d. *Feedback Signal.* The feedback network keeps diodes CR2 and CR3 in the bridge circuit cut off by the same amount, regardless of the voltage stored on capacitor C2. If one were cut off more than the other, then (particularly at high temperatures) the leakage current through one diode would exceed that through the other and would charge or discharge capacitor C2 to an erroneous level. One branch of the output from transistor Q3 is applied to the base of transistor Q9. The output of transistor Q9 is from the emitter and is applied to a voltage divider consisting of resistors R24 through R27. Two outputs are tapped from the voltage divider which are regulated by breakdown diode VR1. The outputs are applied to the bridge network through diodes CR9 and CR10. These diodes isolate the voltage divider from the transformer signal when it is applied. Breakdown diode VR1 (across the voltage divider) keeps the bridge cut off by 6 volts. The voltage divider output signal varies with the signal to the base of transistor Q9 to keep the cutoff voltage across the bridge diodes the same.

e. *Transmit Pam (Odd Channels) Signal.* The *transmit pam (odd channels)* signal is applied to the panel through terminal 5 of jack J4 and is processed the same as the *transmit pam (even channels)* signal. The timing signal for the transmit pam (odd channels) signal is the FF4 signal which enters the panel through terminal 9 of jack J4. After processing, the transmit pam (odd channels) signal is applied from the emitter of buffer transistor Q22 through capacitor C31 to pin 2 of transistor Q17, where it is combined with the *transmit pam (even channels)* signal as described in b(3) above.

f. *Clipped Noise Signal.* The *clipped noise* signal enters the panel at terminal 24 of jack J4 and is added to both *transmit pam* signals through resistors R2 and R36. The signal is applied through resistor R37 to terminal 23 of jack J4 and designated *noise genmon*.

2-40. Coder Timing and Pam Reshaper Circuits, Panel 2A7

(fig. 6-56)

a. *General.* The coder timing and pam reshaper circuits panel is used in the transmit portion of Multiplexer TD-352/U. The coder timing portion provides most of the timing signals for coder No. 2 panel 2A6. The pam reshaper section reshapes the pam signal applied to panel 2A6.

b. *Transmit Pam Input.* The *transmit pam* input applied to terminal 23 of jack J11 consists of relatively wide (5.2 μ sec) pulses. A large portion of the audio wave shape is picked off by the sampler circuit to represent the amplitude of the pam pulse. Since the amplitude of the pam signal is irregular, it must be flattened so that it may be coded properly. To provide a pam flat-topped signal that does not vary more than 0.1 percent in amplitude during coding, the transmit pam input is sampled by a bridge network consisting of diodes CR43, CR44, CR45, and CR46. The pam input is sampled during the initial 5.2- μ sec period and then stored for an additional 5.2 μ sec by capacitor C34. The sampling is accomplished by applying a train of 96-kc square wave pulses (TFF5 signal) through buffer transistor Q22 to driver transistor Q23, the output of which is coupled to transformer T1. The output of transformer T1 is applied across the bridge circuit causing it to turn on and off every 5.2 μ sec). To offset any unbalance in cutoff voltage across bridge diodes CR45 and CR46, a feedback circuit is provided. The feedback signal is developed across transistor Q26 and applied to buffer transistor Q27 through resistor R67. The emitter of transistor Q27 is applied to a voltage divider consisting of resistors R62, R63, R64, and R65, the output of which is connected across the bridge through diodes CR47 and CR48. When the feedback voltage across transistor Q26 varies, the voltage applied to the bridge through diodes CR47 and CR48 also varies to offset the unbalance in cutoff voltage across diodes CR45 and CR46. The output of the bridge is applied through capacitor C34 to buffer transistors Q25 and Q26. The output of transistor Q26 is applied to a highgain amplifier consisting of dual transistor Q28 and buffer Q29. The output at the emitter of buffer Q29 is applied to terminal 31 of jack J11 as the *coder pam* signal, and through resistor R78 to terminal 28 of jack J11 as the *coder pam mon* signal.

c. *Coder Timing Signals.* Five basic signals are used to develop the coder timing signals: FF2 on terminal 12 of jack J11, FF3 on terminal 10, FF4 on terminal 11, FF5 on terminal 13 and T pulse clock on terminal 17. These signals are applied directly or through flip-flops to various AND and OR gates to form the T1 through T6, T1', T6', coder clock, and FF5B signals.

- (1) *Coder clock Signal.* The T pulse clock signal on terminal 17 is applied to buffer transistor Q1 and then to pulse shaper transistor Q2. Transistor Q2 reshapes the waveform and applies it to complementary buffer transistors Q3 and Q4. The output of the buffer transistors is applied to terminal 18 as the *coder clock* pulse and is also used to generate the T1' and T6' signals ((4) below).
- (2) *T1 signal.* The T1 signal is formed by applying four signals to an OR gate consisting of diodes CR7, CR6., CR9, and CR10. As long as one of the inputs to the OR gate is at 0 volt, the output is 0 volt, but if all four signals are at -4.5 volts, the output will be -4.5 volts. The inputs to the OR gate are $\overline{FF2}$ from flip-flop Z1, pin 10 (module 18, para 2-20) to diode CR7; $\overline{FF4}$ from flip-flop Z2, pin 10 (module 18) to diode CR8; FF3 from flip-flop Z3, pin 10 (module 18) to diode CR9; and FF5 through complementary buffer transistors Q20 and Q21. The output of the OR gate is applied through amplifier and inverter transistor Q7 and buffer transistor Q8 to terminal 9 of jack J11 as the T1 signal. This signal is also used to form the T1' signal as described in (4) below.
- (3) *T6 through T6 signals.* These signals are formed essentially the same as the T1 signal, except for different inputs to different OR gates. The inputs used to form signals T2, through T6 are listed in the chart below:

Signal	Input
T2	FF2 from pin 2 of Z1 to diode CR3. $\overline{FF3}$ from pin 10 of Z3 to diode CR5. $\overline{FF4}$ from pin 10 of Z2 to diode CR4.
T3	FF5 from buffer transistors Q20, Q21 to diode CR6. $\overline{FF2}$ from pin 10 of Z1 to diode CR13. FF3 from pin 2 of Z3 to diode CR15. $\overline{FF4}$ from pin 10 of Z2 to diode CR14
T4	FF5 from buffer transistors Q20, Q21 to diode CR16. FF2 from pin 2 of Z1 to diode CR20. $\overline{FF3}$ from pin 10 of Z3 to diode CR22. FF4 from pin 2 of Z2 to diode CR21.
T5	FF5 from buffer transistors Q20, Q21 to diode CR23. $\overline{FF2}$ from pin 10 of Z1 to diode CR26. FF3 from pin 2 of Z3 to diode CR27. FF4 from pin 2 of Z2 to diode CR28.
T6	FF5 from buffer transistors Q20, Q21 to diode CR29. FF2 from pin 2 of Z1 to diode CR30, FF3 from pin 2 of Z3 to diode CR32. FF4 from pin 2 of Z2 to diode CR31. FF5 from buffer transistors Q20, Q21 to diode CR33.

- (4) *T1' and T6' signals.* The T1' signal is formed -by gating the coder clock and T1 signals together in an AND-gate consisting of diodes CR17 and CR18. The output of the AND gate is applied to buffer transistor Q9 and then to terminal 15 of jack J11 The T6' signal is formed by gating the coder clock and T6 signals together in an AND gate consisting of diodes CR34 and CR35. The output of the AND gate is applied to buffer transistor Q16 and then to terminal 19 of jack J11.
- (5) *FF5B signal.* The FF5B signal is essentially a buffered version of the FF5 signal applied to terminal 13 of jack J11. The FF5B signal is applied to terminal 16 of jack J11 for application to external circuits.

2-41. Transmit Timing No. 1, Panel 1 A8

(fig. 6-58)

a. *General.* Transmit timing No. 1, panel 1A8 provides the miscellaneous timing signals for the transmitting operations of the TD-353/U. The miscellaneous frequencies are developed from the output of a crystal-controlled master oscillator within the panel or from a synchronizing signal from another TD-353/U, when two such units are used in conjunction with one another during 96-channel operation. The TD-353/U providing the synchronizing for another unit is called the master multiplexer; the dependent unit is called the slave multiplexer.

b. *Types of Basic Timing Operation.*

- (1) *Master unit.* Whenever a TD-353/U is used as a master unit during 48- or 96 channel operation, the master oscillator is the primary source for transmitter timing. One of the outputs of the timing circuits is a 2,304-kc signal, which is used as the timing source for the slave unit. The timing signal is applied from the SYNC OUT XMTR connector of the master unit to SYNC IN connector of the slave unit.
- (2) *Slave unit.* When the slave unit receives a 2,304-kc timing signal from the master unit, the output from the master oscillator in slave unit 1A8 panel is automatically cut off as the primary source of transmitter timing. The incoming timing signal becomes the primary source of transmitter timing.
- (3) *Drop-and-insert (d/i operation).* When two TD-353/U units are used in conjunction with one another during d/i operation, both units operate as slave units. One unit receives its timing signal by connecting its SYNC IN to the SYNC OUT RCVR of the second unit. The second unit receives its timing by connecting its SYNC IN to the SYNC OUT RCVR of the first unit.

c. *Master Oscillator.* The master oscillator consists of crystal oscillator Z1 (module 22, para 2-21), crystal Y1, and amplifier transistor Q1. Crystal oscillator module Z1 operates at 2,304 kc, its exact frequency being determined by the 2,304-kc series-resonant mode of crystal Y1. The output of crystal oscillator Z1 appears at pin 5 of Z1 and is a train of 100- μ sec 7-volt positive going pulses occurring at a 2,304-kc rate. This signal is applied to amplifier transistor Q1 where the pulses are amplified to 9 volts peak-to-peak (+4.6 to -4.5 volt), inverted, and applied to the base of gate transistor Q2, and (if there is no SYNC IN signal) through diodes CR2 and CR3 to pulse shaper module Z2 (module 30, para 2-24). Diode CR2 is in the emitter circuit of transistor Q2 to protect the emitter-base junction from exceeding its rated back-bias voltage.

d. *Slave Circuit.*

- (1) The slave circuit consists of inverter transistor Q6, buffer transistor Q5, and buffer transistor Q4. When the 1A8 panel is operating in a slave unit, the sync in signal (100- μ sec, 2-volt positive going pulses occurring at a 2,304-kc rate) is applied as an input signal to terminal 29 of jack J6. This signal is coupled through capacitor C10 to the base of inverter transistor Q6. Transistor Q6 inverts the incoming pulses, and they are applied to the base of buffer transistor Q5 as negative-going pulses which vary between +4.5 and -4.5 volts. The output of buffer transistor Q5 is applied to OR gate diode CR5 and the base of buffer transistor Q4. Diode CR5 is part of an OR gate circuit consisting of diodes CR3 and CR5. Diode CR3 normally conducts

the signal from the master oscillator circuit to pulse shaper Z2; however, if there is a sync in signal applied to the circuit, diode CR3 is cut off and diode CR5 conducts the sync in signal to pulse shaper Z2 instead. Diode CR3 is cut off by the sync in signal by applying the sync in signal through buffer transistor Q4 to the base circuit of gate transistor Q3. Capacitor C5 charges to a positive value with respect to the emitter of transistor Q3. Therefore, transistor Q3 conducts and causes the input to diode CR3 to be at -4.2 volts. This back biases diode CR3 and prevents it from conducting.

- (2) The inverted sync in signal at the emitter of buffer transistor Q4 is coupled through capacitor C7 to a clamping circuit consisting of diode CR4. and resistor CR9,. The clamping circuit clamps the negative peak of the sync in signal to ground. The signal is then fed through resistor CR9, to terminal 19 of jack J6 as the sync in monitor signal.

e. Development of Master Clock Signal. Pulse shaper Z2 (module 30, para 2-24) develops the final master clock signal from which all the timing outputs of panel 1A8 (except sync in monitor) are derived. The input to pin 2 of pulse shaper Z2 is a train of 100- μ sec, negative-going 2,304-kc pulses. The output is a train of positive-going pulses on pins 8 and 9 occurring synchronous with the leading edge of the input pulses. This output signal is applied to buffer transistor Q7 and buffer transistor Q12. From transistor Q12 the signal is applied to terminal 17 as the reset clock signal. From transistor Q7 the signal is developed as shown in f below.

f. Flip-Flop Z3 Trigger Circuit. This Circuit consists of buffer transistor Q7, pulse shaper Q8, delay line DL1, buffer transistor Q9, and flip-flop Z3 (module 18, para 2-20). The circuit develops the reshaped clock signal which is used with its complement to generate the remaining timing signals from panel 1A8.

- (1) The master clock signal from pulse shaper Z2 (A, fig. 2-30) is applied to the base of buffer transistor Q7. The output of transistor Q7 (fig. 6-58) is coupled through capacitor C11 to pulse shaper transistor Q8. Transistor Q8 is normally cut off; however, a positive-going pulse applied to its emitter will turn the transistor on, causing a positive pulse of 4.5-volt amplitude to be applied from the collector of transistor Q8 to the out terminal of delay line DL1 and to the base of buffer transistor Q9.
- (2) The positive 4.5-volt pulse from transistor Q8 travels down delay line DL1 and arrives at the in terminal 0.1 μ sec after leaving the out terminal. At this point, the in terminal is shorted to ground. This will cause the pulse to be reflected back down the delay line. The reflected pulses are inverted by the delay line and arrive back at the out terminal as negative pulses delayed an additional 0.1 μ sec from those at the in terminal of the delay line. The total delay between the pulses going into the out terminal of the delay line and those reflected back out of the out terminal is 0.2 μ sec. The combined waveform (B, fig. 2-30) is applied to the base of buffer transistor Q9.
- (3) The signal at the base of transistor Q9 is a train of alternately positive and negative pulses, with the negative pulses occurring 0.2 μ sec after the positive pulses (B. fig. 2-30). This signal is buffered by transistor Q9 (fig. 6-58) and coupled through capacitor C12 to terminal 5 of flip-flop Z3 (module 18, para 2-20).
- (4) The positive and negative pulses at terminal 5 of flip-flop Z3 trigger the module, resulting in complement square wave outputs at terminals 10 and 2 (C and D, respectively, fig. 2-30).
- (5) The output at terminal 10 of flip-flop Z3 (fig. 6-58) is applied to three points: to buffer transistor Q11, from which it is applied to terminal 13 of jack J6 as the reshaped clock signal; to the base of buffer transistor Q10; and to terminal 2 of gate Z6.
- (6) The output at pin 2 of flip-flop Z3 is coupled- through capacitor C23 to terminals 3 and 9 of flip-flop Z7, the first stage of the countdown circuit.

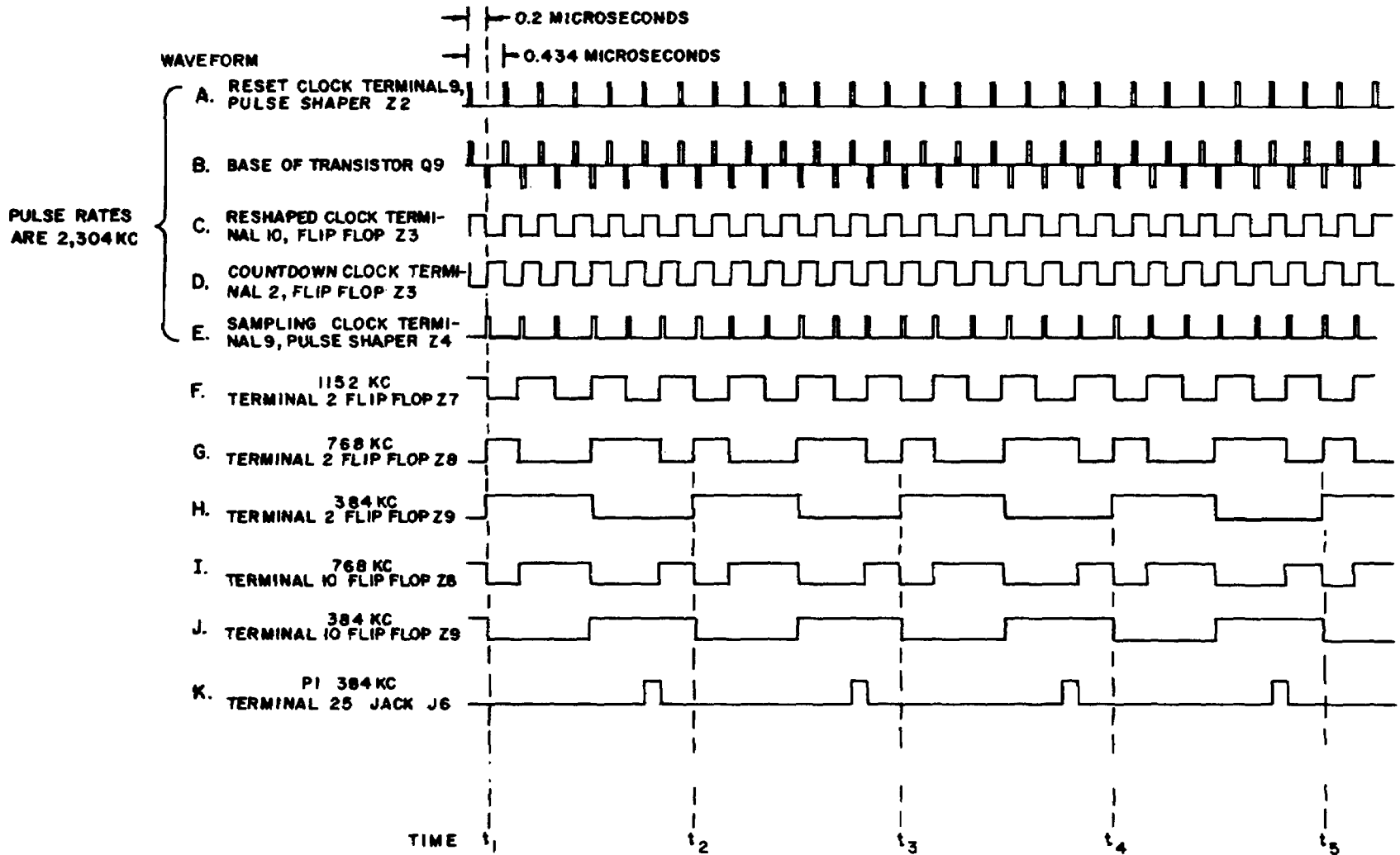


Figure 2-30. Panel 1A8, idealized waveforms.

g. *Development of Sampling Clock, Timing Out, and Sync Out Xmtr Signals.*

- (1) *Sampling clock signal.* The signal applied to the base of buffer transistor Q10 from flip-flop Z3 is buffered by transistor Q10 and applied to pin 2 of pulse shaper Z4 (module 30). The negative-going portion of the signal from transistor Q10 triggers the pulse shaper Z4 module. The output of pulse shaper Z4 is a train of 100- μ sec positive-going pulses occurring synchronous with the negative edge of the input signal. The output is from pin 9 (E, fig. 2-30). This signal is applied to three circuit points: buffer transistors Q13 (fig. 6-58) and Q14 which feed terminal 26 of jack J6 as the *sampling clock* signal, a biasing network consisting of capacitor C13 and resistors R23 and R24, and a biasing network consisting of capacitor C14 and resistors R27 and R28.
- (2) *Timing out signal.* The output of pulse shaper Z4 is applied through a biasing network consisting of capacitor C13 and resistors R23 and R24 to buffer transistor Q15. The output of transistor Q15 is applied to terminal 11 as the *timing out* signal. This signal is essentially the same as that shown for the output of pulse shaper Z4 (E, fig. 2-30).
- (3) *Sync out xmtr signal.* The output of pulse shaper Z4 (fig. 6-58) is applied through a biasing network consisting of capacitor C14 and resistors R27 and R28 to buffer transistor Q16. The output of transistor Q16 is applied to terminal 31 of jack J6 as the *sync out xmtr* signal. The signal is also essentially the same as that shown for terminal 9 of pulse shaper Z4 (E, fig. 2-30).

h. *Countdown Circuit.*

- (1) *General.* The countdown circuit basically consists of flip-flop Z7 (module 09, para 2-15), flip-flop Z8 (module 09), flip-flop Z9 (module 09), AND inhibitor Z10 (module 11, para 2-16), and their associated buffers. The countdown circuit divides the 2,304-kc input frequency by 6 to produce a 384-kc square wave output signal. Intermediate signals generated in the countdown circuit are used as gate signals for other circuits.
- (2) *Flip-flop Z7.* The input to the countdown chain is the clock signal from flip flop Z3 (D, fig. 2-30). This signal is applied to toggle input terminals 3 and 9 of flip-flop Z7 (module 09, para 2-15). Flip-flop Z7 will divide the 2,304-kc input signal in half and the output signal will be 1,152-kc square wave pulses (F, fig. 2-30). The output of flip-flop Z7 (fig. 6-58) is applied to two circuits: buffer transistor Q17 (for application to gate Z6 and AND inhibitor Z10) and through capacitor C24 to complement input triggering terminals 3 and 9 of flip-flop Z8.
- (3) *AND inhibitor Z10.*
 - (a) The output of flip-flop Z8 (module 09, para 2-15) would normally be a 576-kc square wave. However, to obtain a total division-by-6 in the countdown circuit, a feedback circuit is incorporated which causes flip-flop Z8 to divide by 1½ instead of by 2. Flip-flop Z8 produces a 768-kc wavetrain with pulses of unequal duration.
 - (b) The feedback circuit consists of AND inhibitor Z10 (module 11, para 2-16), driven by gate signals through buffers from the countdown flip-flops.
 - (c) The gate signals applied to AND inhibitor Z10 cause a positive-going inhibit signal occurring at a 384-kc rate to be generated at the AND inhibitor output on pin 2. This pulse train is fed back to flip-flop Z8, inhibiting the normal divide-by-2 operation to produce division by 1½ of the 1,152-kc input to the flip-flop.
 - (d) The gate input waveforms to AND inhibitor Z10 are as listed in the chart below. An inhibit signal is produced at terminal 2 of AND inhibitor Z10 when the gate inputs at pins 5 and 7 are at a negative peak (-4.5 volts) and a negative shift occurs at pin 10.

AND inhibitor input pin	Gate. input signals (fig. 2-30)
5 -----	Waveform G.
7 -----	Waveform H.
10 -----	Waveform F.

(e) In figure 2-30, just before time t_1 , waveforms G and H are at a negative peak. At time t_1 , a negative shift is produced in waveform F. This causes the inhibit signal to appear at pin 2 of AND inhibitor Z10. This positive going inhibit signal is applied to pin 2 of flip-flop Z8 and through capacitor C25 to complement input trigger pins 3 and 9 of flip-flop Z9. This causes both flip-flops to change states just after time t_1 (G and H, fig. 2-30). The inhibit signal is generated at a 384-kc rate at times t_2 , t_3 , t_4 , and t_5 .

(4) *Flip-flop Z8.*

- (a) Flip-flop Z8 (module 09) is triggered by the 1,152-kc square wave at pins 3 and 9. As previously explained, flip-flop Z8 is triggered also by the 384-kc inhibit signal, which is applied to pin 2 of the flip-flop. These input triggers cause flip-flop Z8 to divide the 1,152-kc square wave by $1\frac{1}{2}$. The output of the flip-flop is a 768kc wavetrain with pulses of unequal duration. This signal appears as complement outputs at pins 2 and 10 of the flip-flop (G and H, respectively, fig. 2-30).
- (b) The output at pin 2 is applied to two circuit points: through capacitor C25 to toggle input pins 3 and 9 of flip flop Z9, and through buffer transistor Q18 to pin 5 of AND inhibitor Z10.
- (c) The output at pin 10 is fed through buffer transistor Q19 to two circuit points: terminal 10 of jack J6 (where it is designated *FF2B XMTR* and fed out of the panel) and pin 9 of GATE Z6.

(5) *Flip-flop Z9.*

- (a) Flip-flop Z9 (module 09, para 2-15) is triggered by the 768-kc wavetrain input at toggle input pins 3 and FF2B. The flip-flop divides the input by 2, producing a 384-kc square wave. This signal appears as complement outputs at pins 2 and 10 of the flip flop (H and J, respectively, fig. 2-30).
- (b) The output at pin 2 is fed through BUFFER transistor Q20 to three circuit points: terminal 5 of jack J6 (where it is designated *FF3B XMTR* and fed out of the panel), pin 10 of gate Z6, and pin 7 of AND inhibitor Z10.

i. *Gate Z6.*

- (1) Gate Z6 (module 23, para 2-22) is used to produce the P1 signal which is applied to terminal 25 of jack J6. This signal is a train of 200-nsec positive-going pulses occurring at a 384-kc rate (K, fig. 2-30).
- (2) The inputs to pins 8, 9, and 10 of gate Z6 are gating signals (F, I, and H, respectively, fig. 2-30). The signals are used to control the input signal applied to pin 2. When the three gate signals are simultaneously at a negative peak (-4.5 volts), the signal at pin 2 is conducted to pin 4 and out to terminal -25 of jack J6 as the *P1* signal.

2-42. Transmit Timing No. 1, Panel 2A8
(fig. 6-59)

a. *General.* Transmit timing No. 1, panel 2A8, provides the miscellaneous timing signals for the transmitting operations of Multiplexer TD-352/U. The miscellaneous frequencies are developed from the output of a crystal-controlled master oscillator within the panel or from a synchronizing signal from another TD-352/U when two such units are used in conjunction with one another during 24 channel operation. The TD-352/U providing the synchronizing for another unit is called the master multiplexer; the dependent unit is called the slave multiplexer.

b. *Types of Operation.*

(1) *Master unit.* Whenever a TD-352/U is used as a master unit during 12- or 24 channel operation, the master oscillator is the primary source for transmitter timing. One of the outputs of the timing circuits is a 576-kc signal which is used as the timing source for the slave unit. The timing signal is applied from the SYNC OUT XMTR connector of the master unit to SYNC IN connector of the slave unit.

- (2) *Slave unit.* When the slave unit receives a 576-kc timing signal from the master unit, a feedback loop of the slave unit oscillator is automatically opened to prevent master operation. The 576-kc timing input is applied to the oscillator circuit and oscillator crystal Y1 generates the fourth harmonic of the 576-kc signal. The fourth harmonic (2,304 kc) is filtered out and applied to the succeeding stages as in master operation.
- (3) *Drop-and-insert (d/i) operation.* When two TD-352/U units are used in conjunction with one another during d/i operation, both units operate as slave units. One unit receives its timing signal by connecting its SYNC IN to the SYNC OUT RCVR of the second unit. The second unit receives its timing by connecting its SYNC IN to the SYNC OUT RCVR of the first unit.
- c. *Oscillator operation.* The frequency of the oscillator circuit is controlled by a quartz crystal with a mechanical resonant frequency of 2,304 kc. Procedures given in (1), (2), and (3) below give a detailed operation of the oscillator circuit in the various modes.
- (1) *Oscillator components.* Crystal Y1 operates in the series-resonant mode with transistor Q1. Gate transistor Q2 is inserted in the feedback circuit to prevent feedback to the crystal when the self-generating characteristics of the oscillator are not required. Coil L1 and capacitor C3 prevent oscillations from entering the -4.5-volt dc power supply, and the network consisting of coil L2 and resistor R1 peaks the output of transistor Q1. Capacitor C2 passes the lower frequencies to ground.
- (2) *Master oscillator operation.* The bias for the base of transistor Q1 is provided by the voltage divider consisting of resistors R2 and R3. The emitter of transistor Q1 is connected to one side of crystal Y1. When power is applied to the circuit, an initial surge of current from the +4.5volt dc source flows through resistor R4, transistor Q1, coil L2, resistor R1, and coil L1 to the -4.5-volt dc source to start the circuit oscillating. A positive going voltage is produced at the collector and is applied to the bases of gate transistor Q2 and buffer transistor Q4. The path through transistor Q4 is the output path, and the path to transistor Q2 is the feedback path. Transistors Q2 and Q3 operate as an inhibit gate circuit. Transistor Q3 is normally cut off for master operation; therefore, during this mode transistor Q2 will act like an emitter follower. The positive-going input at the base of transistor Q2 is produced at the emitter and is applied through diodes CR3 and CR1 to one side of crystal Y1. Diode CR3 is in the emitter circuit of transistor Q2 to protect the emitter-base junction from exceeding its back-bias voltage. This input to crystal Y1 acts as feedback to sustain operation. When the output from the other side of crystal Y1 to the emitter of transistor Q1 begins to go negative, the cycle described above is reversed and all the voltages go in a negative direction. The cycle is repeated synchronous with the mechanical vibration of crystal Y1.
- (3) *Slave oscillator operation.* When a TD362/U is used as a slave unit, the oscillator is externally synchronized by the 576-kc sync in signal applied at terminal 17 of jack J9. This signal is applied to pin 2 of pulse amplifier Z4 (module 33, para 2-27). One output of pulse amplifier Z4 is on pin 1 and is a train of negative-going spike pulses; another output is on pin 9 and is a train of positive going spike pulses. Both signals have a 576-kc rate. The output at pin 1 is used to develop a signal which inhibits the feedback in the oscillator circuit and will override the self-generating characteristics of the oscillator. The output at pin 9 is used to excite crystal Y1 and is applied to it through transistor Q9 and diode CR2. For master operation, the feedback signal keeps the crystal vibrating; for slave operation, the 576-kc input keeps the crystal vibrating. The fourth harmonic of the 576-kc frequency (2,304 kc) is developed at the emitter of transistor Q1, amplified at the collector, and applied to the base of transistor Q4. This signal is the same as that produced by the self-generating method during master operations.

(4) *Inhibiting gate.* The input to the inhibiting gate circuit is from pin 1 of pulse amplifier Z4 and is applied to the base of buffer transistor Q10. With no input from pulse amplifier Z4, the base of transistor Q10 is at 0 volt and the base of transistor Q11 is at -4.5 volts. Since transistor Q11 is an emitter follower, the -4.5-volt potential on its base is coupled to its emitter. However, because of an internal voltage drop in the transistor, the emitter voltage will be -4.2 volts. The current flow from the emitter of transistor Q11 is from the emitter through resistors R7 and R8 to the -12-volt source. Since the junction of resistors R7 and R8 is connected to the base of transistor Q3, the junction voltage (-5.6 volts) is applied to bias transistor Q3. As a result of these biases, transistors Q10 and Q11 are conducting and transistor Q3 is cut off. When the train of negative-going spike pulses appears at the base of transistor Q10, transistor Q10 acts as an emitter follower, and the signal is applied to the emitter without change of polarity. The signal passes through capacitor C9 and is applied to the base of buffer transistor Q11 and appears at its emitter. The point between resistors R17 and R8 is driven more positive, as a result of the clamping action of capacitor C9, resistor R16, and transistor Q11. Therefore, the point between resistors R8 and R7 goes more positive, causing the base of transistor Q3 to become more positive and transistor Q3 to conduct. Capacitor C4 stores a charge to maintain the bias between pulses. When transistor Q3 conducts, it shorts out the output of transistor Q2 and diode CR3 so that the anode of diode CR3 assumes a -4.5-volt potential. The -12-volt dc signal applied to resistor R5 causes the junction of diodes CR1 and CR2 to follow the more positive potential at the anodes of diodes CR1 and CR2. Because the potential at the anode of diode CR1 is -4.5 volts and the potential at the anode of diode CR2 goes to 0 volt with each positive-going pulse of the 576-kc output of transistor Q9, diode CR2 conducts and a positive-going pulse is applied to the crystal to sustain the oscillation.

d. *Countdown Chain Input.* The 2,304-kc pulse output of the oscillator is applied through transistor Q4 to pins 3 and 9 of flip-flop Z1 (module 09, para 2-15). From the 2,304-kc pulse output, flip-flop Z1 produces two complementary squarewave signal trains with a 1,152-kc frequency.

(1) *1,152-kc outputs.* The two 1,152-kc outputs of flip-flop Z1 are designated TFF1 and $\overline{\text{TFF1}}$.

(a) *TFF1 output.* The TFF1 output is taken from pin 10 of flip-flop Z1 and is applied through buffer transistor Q16 and buffer transistor Q25 to terminal 1 of jack J11. Another branch of this output is passed through a delay circuit consisting of transistors Q17, Q18, and delay line DL2, where the signal is delayed 0.2 μ sec. The output of the delay network is applied to terminal 4 of jack J11 and designated *T pulse clock*.

(b) *$\overline{\text{TFF1}}$ output.* The complement of the TFF1 signal is taken from pin 2 of flip-flop Z1 and passed through buffer transistor Q12 to terminal 20 of jack J9, where the signal is designated $\overline{\text{TFF1}}$. Another branch of the signal, applied to the base of gate transistor Q28, is described in *k* below.

(2) *Forward feed.* The input to the next stage of the countdown chain is taken from pin 10 of flip-flop Z1 and is passed through capacitor C5 to terminals 3 and 9 of flip-flop Z2 (module 09).

e. *Flip-Flop Z2 Outputs.* Flip-flop Z2 divides the 1,152-kc input by 2 to provide a 576-kc square wave output. Flip-flop Z2 also acts as the first flip-flop of a divide-by-6 countdown chain, as shown in f below.

- (1) *TFF2 output.* One output is taken from pin 10 of flip-flop Z2 and applied to buffer transistor Q8. The output of transistor Q8 is divided into three branches. One branch goes to pin 10 of AND gate Z6 (module 11, para 2-16); a second branch is applied to pin 2 of pulse shaper Z8 (module 30, para 2-24); the third branch of the signal is applied to terminal 2 of jack J9 and designated TFF2.
- (2) *TFF2 output.* The complement signal of TFF2 is taken from pin 2 of flip-flop Z2, applied through buffer transistor Q7 to terminal 19 of jack J9, and designated TFF2.
- (3) *Forward feed.* The signal input for the next stage of the countdown chain is taken from pin 10 of flip-flop Z2 and applied to pins 3 and 9 of flip-flop Z3 (module 09, para 2-15).

f. *Divide by-6 Countdown Chain.* The divide by -6 countdown chain consists of three flip-flop modules and an AND gate module. Flip-flops Z2 and Z3 (module 09, para 2-15) are located on panel 2A8, and the last flip-flop in the chain (flip-flop Z1, module 09) is located on panel 2A10. The divide-by-6 circuit operates to reduce a 1,152-kc square wave input to a 192-kc square wave output. The circuit also produces intermediate signals in the countdown process. The circuit operates as described below.

- (1) *General.* The division by 6 is accomplished by using a countdown chain in which the outputs of some stages are fed back into the circuit. Normally, the flip-flops would divide the input signal by 2 and apply it to the output circuit. However, by feeding the outputs of succeeding stages into an AND gate circuit (Z6) and applying the output of the AND gate to the inputs of the flip-flops, it is possible to get a division by 1 1/2. The total effect of the circuit is division by two in 2 flip-flops and a division by 1 1/2 in one flip-flop, for an overall division by 6 of the total input frequency.
- (2) *Inputs to flip-flops and AND gate.*

Module	Pin	Input signal
Z2 -----	3	1,152 kc from flip-flop Z1 (2A8).
Z3 -----	3	576 kc from flip-flop Z2.
Z1 (2A10) -----	3	384 kc from AND gate Z6.
Z6 -----	5	192 kc from flip-flop Z1 (2A10).
Z6 -----	7	384 kc from flip-flop Z3.
Z6 -----	10	576 kc from flip-flop Z2.

- (3) *Outputs of divide-by-6 countdown chain.* The main output from panel 2A8 for the divide-by-6 countdown chain is from pin 10 of flip-flop Z3 and is applied through buffer transistor Q5 as the *TFF3* signal. This signal is applied to panel 2A10 through terminal 23 of jack J6 for application to flip-flop Z1 for completion of the countdown function. The other signals produced by the countdown chain are the $\overline{TFF3}$ signal, which is applied from pin 2 of flip-flop Z3 through buffer transistor Q6 to terminal 21 of jack J9, and the *TFF2* and $\overline{TFF2}$ signals. The $\overline{TFF2}$ signal is applied from pin 2 of flip-flop Z2 through buffer transistor Q7 to terminal 19 of jack J9. The *TFF2* signal is applied from pin 10 of flip-flop Z2 through buffer transistor Q8 to terminal 2 of jack J9. In addition to these outputs from the panel, the *TFF3* signal is also applied to pin 2 of pulse shaper Z9 and pin 3 of flip-flop Z7.

g. *Synchronization of Countdown Chain.* As the signal passes through the countdown process, undesirable delays are introduced which could produce a phase shift between the input and output signals. To offset this phase shift when a TD-352/U is operated as a slave unit, the externally produced sync in, signal is injected into the countdown at various points. The *sync in* signal will reset the various flip-flops in the countdown-chain so that the output is in phase with the *sync in* signal.

- (1) *Origin of synchronizing signal.* The synchronizing signal is taken from pin 1 of pulse amplifier Z4 and is applied to the base of delay circuit transistor Q13.
- (2) *Delay circuit.* The 576-kc train of negative-going pulses is applied from the emitter of transistor Q13 through resistor R23 to delay line DL1. The negative 4.5-volt signal travels down delay line DL1 and arrives at the in terminal 0.1 μ sec after leaving the out terminal. At this point, the in terminal is shorted to ground. Since the characteristic impedance of the delay line is high, this will cause the pulse to be reflected back down the delay line. The reflected pulses are inverted by the delay line and arrive back at the out terminal as positive pulses delayed 0.1 μ sec more than those at the in terminal of the delay line. The pulses going into the out terminal are delayed a total of 0.2 μ sec more than those reflected back from the out terminal. The delayed signal is applied to buffer transistor Q14. The output of the buffer is applied to diode CR6. At this point, the signal consists of alternately negative and positive pulses with the positive going pulses occurring 0.2 μ sec after the negative-going pulses. Diode CR6 will only pass the positive-going pulses; therefore, only the delayed signal will reach inverter transistor Q18, which is in the output circuit of the delay circuit. Diode CR7 acts as a termination to insure that the negative-going signal is not passed through the circuit. The 0.2 μ sec delay produced by this circuit insures that enough time has elapsed in the countdown circuits before they are reset by the synchronizing pulses. The delay circuit output is applied through inverter transistor Q15 to pin 5 of pulse shaper Z5 (module 30, para 2-24). The negative-going input pulses to the pulse shaper are inverted and spiked and applied to output pins 8 and 9. From pin 8, the pulses are applied to pin 10 of flip-flop Z1, and from pin 9, they are applied to pin 10 of flip-flop Z2. These pulses will reset the flip-flops at a 576-kc rate. The 576-kc rate will reset every other cycle of operation of flip-flop Z1 and every cycle of operation of flip-flop Z2.

h. Development of FF12 Signal. The *FF12* signal is developed by flip-flop Z7 (module 18, - para 2-20). Two inputs are applied to flip-flop Z7: a 384-kc square wave signal from the emitter of buffer transistor Q6 is applied to pin 3, and a 192-kc signal (*TFF4*) is applied from terminal 11 of jack J9 through diode CR13 to pin 8. The output is a 192-kc signal taken from pins 1 and 2, which are tied together, and applied to terminal 31 of jack J9 as the *FF12* signal. In addition, the signal is also supplied to gate transistor Q20.

i. Development of Shift 9 Signal. The *shift 2* signal is developed in the gate circuit consisting of transistors Q19 and Q20. The input to gate transistor Q20 is a 192-kc signal as developed in *h* above. The input to gate transistor Q19 is the *FF2* signal from buffer transistor Q8, which is first applied to pin 2 of pulse shaper Z8 (module 30, para 2-24) and then from pin 9 of the pulse shaper to transistor Q19. The two signals are gated together, and the output of the gate circuit is applied to terminal 24 of jack J9 as the *shift 2* signal.

j. Development of Parallel Shift Signal. The *parallel shift* signal is developed by the gate circuit consisting of transistors Q21 and Q22. The input to gate transistor Q21 is a 192-kc signal from pin 1 of flip-flop Z7; this is the complement of the 192-kc signal described in *i* above. The input to gate transistor Q22 is a 576-kc signal from pin 9 of pulse shaper Z8. The two signals are gated together, and the output of the gate circuit is applied through buffer transistors Q24 and Q25 to terminal 30 of jack J9 as the *parallel shift* signal.

k. Development of Coder Decision Signal. The *coder decision* signal is developed in the gate circuit consisting of transistors Q27 and Q28. The input to gate transistor Q28 is the *FF1* signal, which is a 1,152-kc square wave taken from buffer transistor Q12. The input to gate transistor Q27 is the *FF5B* signal which is applied externally to terminal 29 of jack J9. In the gate circuit, six pulses are blanked out of the 1,152-kc square wave signal by each of the 192-kc square waves. The resultant signal consists of six pulses of the 1,152kc signal, then no signal for a period equivalent to six pulses of the 1,152-kc signal, after which this cycle is repeated. The output of the gate signal is taken from the emitters of the gate transistors and applied to terminal 22 of jack J9 as the *coder decision* signal.

I. Development of Modem Timing Signal. The *modem timing* signal is developed from the 384-kc TFF3 signal. The 384-kc signal is applied from buffer transistor Q6 and to pin 2 of pulse shaper Z9 (module 30, para 2-24). The output of pulse shaper Z9 is a wavetrain of positive-going 384-kc pulses which are applied through buffer transistor Q26 to terminal 28 of jack J9 as the *modem timing* signal.

2-43. Transmit Timing No. 2, Panel 1 A9

(fig. 6-61)

a. General. Transmit timing No. 2 panel 1A9 provides miscellaneous timing signals for the transmit section of the TD-353/U. The procedures given in *b* through *f* below give a detailed description of how the various outputs are formed. The interrelationships between the input and output signals are shown in figure 6-38. This diagram helps explain the function of the panel in the transmit section of Multiplexer TD-353/U.

b. Development of Modem Timing Signal. The FF3B xmtr signal appearing at terminal 19 of jack J5 is applied to pin 2 of the input of pulse shaper Z1 (module 30, para 2-24). -This signal is a 384-kc square wave; its negative level triggers pulse shaper Z1. The output of the pulse shaper is taken from pin 9 and consists of 100-nanosecond positive-going pulses at a 384-kc rate. This signal is applied through buffer transistor Q1 to terminal 22 of jack J5 as the *modem timing* signal.

c. Address Pulse and Auxiliary Address Circuit. The address pulse and aux address circuit consists of flip-flop Z4 (module 18, para 2-20); flip-flop Z5 (module 09, para 2-15); AND gate diodes CR9, CR10, CR11, and CR12; and buffer transistors Q6, Q7, Q8, Q9, Q10, and Q11.

(1) Development of address pulse output signal.

(a) The FF9 signal appearing at terminal 2 of jack J5 is fed through capacitor C6 and steering diode CR7 to pin 5 of flip-flop Z4. This signal is an 8-kc square wave (C, fig. 2-31). Simultaneously, the *reshaped clock* signal appearing at terminal 3 of jack J5 is fed through buffer transistor Q6, capacitor C7, and steering diode ORB to pin 8 of flip-flop Z4. This signal is a 2,304-kc train of 100-nanosecond positive-going pulses (A, fig. 2-31).

(b) The pulses at pins 5 and 8 of flip-flop Z4 drive the flip-flop, causing a train of positive-going pulses (E, fig. 2-31) to appear at pin 10 and a complementary signal (D, fig. 2-31) to appear at pin 2 of the flip-flop. The signal at pin 10 of the flip-flop is applied to terminal 14 of jack J5, where it is designated as the *address pulse* signal, and to diode CR12. The signal at pin 2 of flip-flop Z4 is applied to diode CR9. Diodes CR12 and CR9 are used in the aux address gate circuit described below.

(2) Development of aux address output signal.

The sampling clock signal appearing at terminal 15 of jack J5 is fed to diodes CR10 and CR11 as a gate signal. This signal is a 2,304-kc train of 100-nanosecond positive-going pulses (B, fig. 2-31).

(a) *AND gate CR9, CR10, and R18.* This circuit operates as a conventional AND gate, with the voltage at the base of buffer transistor Q7 following the more negative gate input signal. The input signals to diodes CR9 and CR10 (D and B, fig. 2-31) are gated, forming a train of 2,304-kc pulses having one pulse blanked every 125 microseconds. This signal (G, fig. 2-31) appears at the base of buffer transistor Q7 and is fed through transistor Q7 and capacitor C8 to pin 9 of flip flop Z5.

(b) *AND gate CR11, CR12, and R19.* This circuit also operates as a conventional AND gate, with the voltage at the base of buffer transistor Q8 following the more negative gate input signal. The input signals to diodes CR11 and CR12 (E and B, respectively, fig. 2-31) are gated, forming a train of 8-kc pulses. This signal (F, fig. 2-31) appears at the base of buffer transistor Q8 and is fed through transistor Q8 and capacitor C9 to pin 3 of flip-flop Z5.

WAVEFORM

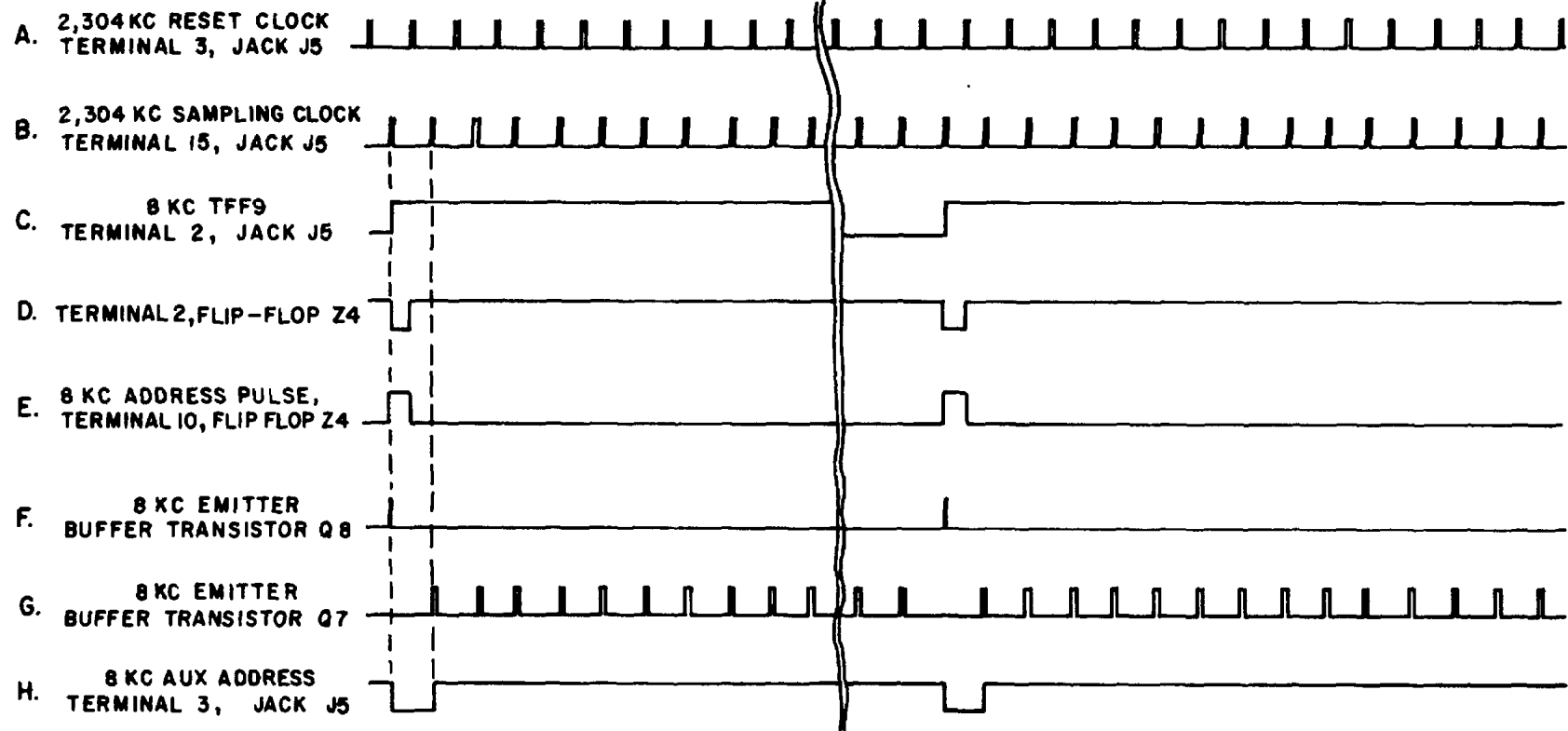


Figure 2-31. Panel 1A9, address pulse and aux address circuit idealized waveforms.

(c) *Flip-flop Z5.* The pulses at pins 3 and 9 of flip-flop Z5 drive the flip-flop, causing a train of 8-kc negative-going pulses to appear at pin 10. This pulse train is fed through a parallel circuit, consisting of buffer transistors Q9 and Q10, to dc shifting network resistors R23 and R24 and capacitor C10. The parallel transistors are required to provide adequate driving current for the input circuit of of buffer transistor Q11. The pulse train is coupled from the emitter of buffer transistor Q11 to terminal 18 of jack J5, where it is designated as the *aux address* signal (H, fig. 2-31).

d. *Development of Transmit Pam (Even Channels) Signal.* The FF4. input signal, a 192-kc square wave appearing at terminal 29 of jack J5, is fed through buffer transistor Q12 to the base of inverter transistor Q13.

(1) When the FF4 input signal is at a negative peak (-4.5 volts), transistor Q13 is conducting. At this time, any signal at terminal 30 of jack J5 is shorted to ground potential through transistor Q13. When the FF4 input signal is at a positive peak (0 volt), transistor Q13 is cut off. At this time, any signal at terminal 30 of jack J5 is unaffected by circuitry in panel 1A8.

(2) The collector of transistor Q13 is connected through terminal 30 of jack J5 to the pam samples from the even numbered audio channels. These pam samples occur only when transistor Q13 is cut off. This action helps eliminate unwanted channel crosstalk between adjacent even-numbered channels.

e. *Development of Transmit Pam (Odd Channels) Signal.* The FF4 input signal (opposite in polarity to TFF4) is a 192-kc square wave and appears at terminal 28 of jack J5. It is fed through buffer transistor Q14 to the base of inverter transistor Q15.

(1) When the FF4 input signal is at a negative peak (-4.5 volts), transistor Q15 is conducting. At this time, any signal at terminal 31 of jack J6 is shorted to ground potential through transistor Q15. When the FF4 input signal is at a positive peak (0 volt), transistor Q15 is cut off. At this time, any signal at terminal 31 of jack J5 is unaffected by circuitry in panel 1A8.

(2) The collector of transistor Q15 is connected through terminal 30 of jack J5 to the pam samples from the odd-numbered audio channels. These pam samples occur only when transistor Q15 is cut off. This action helps eliminate unwanted channel crosstalk between adjacent odd-numbered channels.

f. *Development of Transmit Address Timing Output Signal.* The FF9 input signal, an 8-kc square wave appearing at terminal 17 of jack J5, is fed through buffer transistor Q16 to terminal 16 of jack J5, where it is designated as the transmit address timing signal.

2-44. Transmit Timing No. 2, Panel 2A9

(fig. 6-63)

a. *General.* Transmit timing No. 2 panel 2A9 provides miscellaneous timing signals for the transmit section of the TD-353/U. The procedures given in b through e below give a detailed description of how the various outputs are formed. The interrelationships between the input and output signals are shown in figure 6-33. This diagram helps explain the function of the panel in the transmit section of Multiplexer TD-352/U.

b. *Development of Shift No. 1 Signal.* A 1,152-kc signal, designated *TFF1*, is applied from terminal 25 of jack J7 to pin 2 of pulse shaper Z1 (module 30, para 2-24). The output of pulse shaper Z1 at pin 9 in conjunction with gating transistor Q1 forms a wavetrain of five positive-going trigger pulses occurring at a group rate of 96 kc. This signal is applied to terminal 24 of jack J7 as the shift No. 1 signal. A 96-kc signal, designated T6, is applied from terminal 27 of jack J7 to pin 5 of flip-flop Z3. A 96-kc signal, shifted in time from T6 and designated T1, is applied from terminal 23 of jack J7 to pin 8 of flip-flop Z3. The output of Z3 at pin 10 is an asymmetrical 96-kc gating signal. It is applied from the output of flip-flop Z3 to the base of Q1 to turn it on and off. The application of the -4.5-volt gate signal from flip flop Z3 causes transistor Q1 to cut off for a period of 4.34 μ sec. This allows five trigger pulses from pulse shaper Z1 to reach the shift No. 1 output terminal. The gate signal then switches to 0-volt level, causing transistor Q1 to conduct for 6.06 μ sec, blocking the next seven trigger pulses from being applied to the output. The resultant output is a series of five positive-going pulses at a 1,152-kc rate, having a group rate of 96 kc.

c. *Development of Timing Out, Sync Out Xmtr, and Sampling Clock Signals.* A 576-kc signal ($\overline{TFF2}$) is applied from terminal 16 of J7 to pin 2 of pulse shaper Z2 (module 30, para 2-24). The output of pulse shaper Z2 is a wavetrain of 576-kc positive-going trigger pulses appearing at pin 9. The output of pulse shaper Z2 is applied to three circuit points to provide a variety of output signals as listed below:

- (1) *Timing out signal.* The signal from pin 9 of pulse shaper Z2 is applied through buffer transistor Q3 to terminal 31 of jack J7, where it is designated as the *timing out* signal. When terminated in a 91-ohm load, the output is a 576-kc signal of -2.0- to 0-volt pulses.
- (2) *Sync out xmtr signal.* The signal from pin 9 of pulse shaper Z2 is applied through buffer transistor Q4 to terminal 7 of jack J7 and designated the *sync out xmtr* signal. This signal is the same as the timing out signal.
- (3) *Sampling clock signal.* The signal from pin 9 of pulse shaper Z2 is applied through buffer transistor Q8 to terminal 14 of jack J7, where it is designated as the *sampling clock* signal. It is used to retime the pcm signal before transmission to external equipment.

d. *Development of Address Pulse and Address Pulse Signals.* A 192-kc signal, designated *parallel shift*, is applied from terminal 30 of jack J7 to pin 5 of flip-flop Z4 (module 18, para 2-20). An 8-kc signal from gate transistors Q10 and Q11 ((2) below) is applied to pin 8 of flip-flop Z4. The output from flip-flop Z4 appears at pins 2 and 10. The output on pin 2 is a train of 8-kc positive going pulses 1.73 μ sec wide, which are applied to terminal 29 of jack J7 as the address pulse signal. The output on pin 10 is a train of 8-kc negative going pulses (the complement of signal on pin 2), which are applied to terminal 18 as the address pulse signal.

- (1) The *parallel shift* pulse has a repetition rate of 192 kc and is applied to pin 5 of Z4. This sets the flip-flop output at pin 10 to a 0-volt level.
- (2) The 8-kc signal applied to pin 8 of flip flop Z4 is derived from a gate circuit consisting of transistors Q10 and Q11. A signal designated *M21* is applied from terminal 3 of jack J7 through inverter transistor Q9 and diode CR7 to the base of gate transistor Q10 as one of the inputs. The *FF5B* signal from terminal 1 of jack J7 is applied through diode CR6. to the base of transistor Q10. The $\overline{TFF6}$ signal from terminal 13 of jack J7 is applied to buffer Q28 and then through diode CR9 to the base of transistor Q10. The T1 signal from terminal 23 of jack J7 is applied to the base of transistor Q11. These signals are gated together by transistors Q10 and Q11. the result is an 8-kc pulse occurring at time T1'. This resets flip-flop Z4.

e. *Development of 8 Kc Address Signal.* An 8kc Signal. designated *TFF9* is applied from terminal 22 of jack J7 to buffer transistor Q24. The output of transistor Q24 is applied to terminal 26 of jack J7 and designated the *8-kc address* signal.

2-45. Transmit Timing No. 3/Receive Timing No. 2, Panel 1A10 (fig. 6-65)

a. *General.* Transmit timing No. 3/receive timing No. 2 panel 1A10 divides the 384-kc *modem timing* signal into various submultiple frequencies used in the transmit and receive sections of the TD-353/U. The prefixes T and M (transmit and modulate) are used with the timing signal designators when the panel is used in the transmit section of the multiplexer. The prefixes R and D (receive and demodulate) are used with the timing signal designators when the panel is used in the receive section of the multiplexer. The frequencies of the timing signals generated are: 192 kc, 96 kc, 48 kc, 24 kc, 16 kc, and 8 kc. The frequency division is accomplished by a conventional countdown chain consisting of flip-flops Z1 through Z6 (module 18, para 2-20) and associated gate circuits. Flip-flops Z1 through Z4 are divide by -2 circuits, and flip-flops Z5 and Z6 and the sixth gate Q11. Q12) form a divide-by-3 circuit. The gate circuits and their associated buffer transistors (Q1 through Q12) are used to retime the outputs of each of the flip-flops after each frequency division. This is done to prevent accumulation of delays in the countdown circuitry and to insure proper formation of the output signal matrix. Procedures given in *b* through *i* below describe how the various outputs are formed. The interrelationships between the input and output signals are shown in figure 6-38.

b. *Development of TFF4 (or RFF4) and $\overline{TFF4}$ (or $\overline{RFF4}$) Outputs.* A 384-kc input pulse, designated modem timing, is applied through terminal 29 of jack J13 to the of buffer transistor of each gate circuit and also to pin 3 of flip-flop Z1. flip flop Z1 (module 18, para 2-20) divides the input frequency by a factor of 2. The output, pin 2, is applied to terminal 14 of jack J13 as the *TFF4* (or *RFF4*) signal. The complement of this signal is obtained from pin 10 of flip-flop Z1, and is applied to terminal 27 of jack J13 as the (*TFF2*) (or *RFF4*) signal. The *TFF4* (or *RFF4*) signal is also applied to each OR gate (diodes CR1, CR3, CR6, CR10, and CR15) and to gate transistor Q2. The signals from pins 2 and 10 of flip-flop Z1 are also applied to pins 9 and 15, respectively, of diode matrix Z9.

c. *Development of TFF6 (or RFF5) and, $\overline{TFF5}$ or $\overline{RFF5}$) Outputs.* When coincidence occurs in the first gate (transistor Q2), a 192-kc pulse is produced at the junction of the emitter of transistor Q1 and the collector of transistor Q2. This signal is applied to pin 3 of flip-flop Z2. Flip-flop Z2 (module 18, para 2-20) divides the input by 2 and applies a 96-kc signal from pin 2 of the flip-flop to terminal 17 of jack J13. This is designated as the *TFF5* (or *RFF5*) signal. The complement of this signal appears at pin 10 and is applied to terminal 20 of jack J13 as the *TFF3* (or *RFF5*) signal. The signal from pin 10 is also applied to each OR gate (diodes CR2, CR4, CR7, CR11 and CR16). The signals from pins 2 and 10 are also applied to pins 11 and 12, respectively, of diode matrix Z9.

d. *Development of TFF6 (or RFF5) Output.* When coincidence occurs in the second gate (transistor Q4), a 96-kc pulse is produced at the junction of the emitter of transistor Q3 and the collector of transistor Q4. This signal is applied to pin 3 of flip-flop Z3. Flip-flop Z3 (module 18, para 2-20) divides the input by 2 and applies a 48-kc signal from pin 10 of the flip-flop to terminal 21 of jack J13, where it is designated as the *TFF6* (or *RFF6*) signal. This signal is also applied to OR gate diodes CR5, CR6, CR12, and CR17. The signals from pins 2 and 10 are also applied to pins 14 and 13, respectively, of diode matrix Z9.

e. *Development of TFF8 (or RFF8) Output.* When coincidence occurs in the third gate (transistor Q6), a 48-kc signal is produced at the junction of the emitter of transistor Q5 and the collector of transistor Q6. This signal is applied to pin 3 of flip-flop Z4. Flip-flop Z4 (module 18, para 2-20) divides the input by 2 and applies a 24-kc signal from pin 10 of the flip-flop to the third and fourth OR gates (diodes CR9 and CR13). The complement of this signal is applied from pin 2 of the flip-flop to the fifth OR gate (CR19). The signals from pins 2 and 10 are also applied to pins 9 and 15, respectively, of diode matrix Z7. When coincidence occurs in the fourth gate (transistor Q8), a 24-kc signal is produced at the junction of the emitter of transistor Q7 and the collector of transistor Q8. This signal is applied to pin 3 of flip-flop Z5. The 8-kc signal from the last gate (f below) is also applied to flip-flop Z5 (module 18, para 2-20) through capacitor C11 and diode CR21. Normally, a 12-kc signal would be developed at the output of flip-flop Z5. However, the feedback signal applied to pin 5 causes a wavetrain of nonidentical pulses with alternate negative-going edges having a period of 16 kc. This output is applied from pin 2 of flip-flop Z5 to terminal 5 of jack J13, where it is designated as the *FFF8* (or *RFF8*) signal. This signal is also applied to pin 11 of diode matrix Z7. The complement of this signal is applied from pin 10 of the flip-flop to the last two OR gates (CR14 and CR18).

f. *Development of TFF9 (or RFF9) and $\overline{TFF9}$ (or $\overline{RFF9}$) Outputs.* When coincidence occurs in the fifth gate (transistor Q10), a 16-kc pulse is produced at the junction of the emitter of transistor Q9 and the collector of transistor Q10. This signal is applied to pin 3 of flip-flop Z6. The 8-kc fixed-phase output of the last gate (transistor Q12) is also applied to flip-flop Z6 through pin 8, to insure that the output is the correct phase. Flip-flop Z6 (module 18, para 2-20) divides the input by 2 and applies an 8-kc pulse from pin 2 of the flip-flop to terminal 11 of jack J13, where it is designated as the *TFF9* (or *RFF9*) signal. This signal is also applied to the last OR gate (diode CR20). The complement of this signal is applied from. pin 10 of the flip-flop to terminal 9 of jack J13 and is designated *TFF9* (or *RFF9*). This signal is also applied to pin 13 of diode matrix Z7.

g. *Development of M21 Through M26 (or D21 Through D26) Signals.* Diode matrix Z7 (module 17, para 2-19) accepts six-inputs (two each from flip-flops Z4, Z5, and Z6) and combines them in a matrix of six 3-input AND gates. The output of each gate is a wavetrain of 20.8- μ sec positive going pulses occurring at an 8-kc rate. The pulses in the different outputs occur in sequence starting with signal M21 or D21 (that is, the leading edge of M22 or D22 occurs at the time of the trailing edge of M21 or D21, etc.). From diode matrix Z7, the M21 or D21 and M23 or D23 pulses. are applied to the output terminals through buffer transistors Q14 and Q13, respectively. The M22 or D22, M24 or D24, M25 or D25 and M26 or D26 signals are fed through buffer module Z8 (module 15, para 2-17) to the output. The outputs and their terminals are listed below:

Designation	Diode matrix Z7 output pin	Jack 13 output terminal
M21 or D21 -----	8	13
M22 or D22 -----	1	1
M23 or D23 -----	7	12
M24 or D24 -----	3	4
M25 or D25 -----	5	10
M26 or D26 -----	4	7

h. *Development of M11 Through M18 (or D11 Through D18) Signals.* Diode matrix Z9 (module 16, para 2-18) accepts six inputs (two each from flip-flops Z1, Z2, and Z3) and combines them in a matrix of eight 3-input AND gates.

- (1) The matrix outputs at pins 2 through 7 are wavetrains of 2.375- μ sec pulses occurring at a 48-kc rate. The pulses in these wavetrains occur in sequence and are 225 μ sec apart.
- (2) The matrix outputs at pins 1 and 8 are wavetrains of 2.6- μ sec, positive-going pulses occurring at a 48-kc rate. Pulses in these wavetrains occur in sequence. When the trailing edge of a pulse at pin 8 occurs, the leading edge of the pulse at pin 1 occurs.
- (3) Six of the eight matrix outputs (pins 2 through 7) are also gated with an additional signal by diodes CR23 through CR28. When panel 1A10 is used in the receive section of the TD-353/U, this additional signal is a train of 225-nanosecond, negative-going pulses occurring at a 384-kc rate. The signal appears at terminal 8 of jack J13 and is designated as the *modem gate timing* signal. When this panel is used in the transmit section of the TD-353/U, terminal 8 of jack J13 is grounded.
- (4) The eight outputs from diode matrix Z9 are applied through buffer modules Z10 and Z11 (module 15, para 2-17) to the terminals listed below:

Designation	Diode matrix Z9 output pin	Buffer	Jack J13 output terminal
M or D11 -----	8	Z10	26
M or D12 -----	1	Z11	16
M or D13 -----	7	Z10	25
M or D14 -----	2	Z11	16
M or D15 -----	6	Z10	24
M or D16 -----	3	Z11	18
M or D17 -----	5	Z10	22
M or D18 -----	4	Z11	19

i. *Development of M11 and M12 Outputs.* The M11 and M12 signals are identical with the D'11 and D'12 outputs except that the pulses in the M11 and M12 trains are 2.375 μ sec in duration versus 2.6 μ sec for M'11 and M'12. The leading edges of the M11 and M12 outputs are synchronous with the leading edges of pulses in the D'11 and M'12 outputs.

- (1) *Development of M11 Output.* The M11 signal is developed by gating the M'11 signal, with the 384-kc modem gate timing signal appearing at signal terminal 8 of jack J13. This is accomplished by gate Z12 (module 35, para 2-28). The resultant signal is applied from pin 3 of gate Z12 to terminal 3 of jack J13 and designated M11.
- (2) *Development of M12 Output.* The M12 signal is developed by gating the M'12 signal with the 384-kc modem timing gate appearing at terminal 8 of jack J13.

This is accomplished by gate Z12 (module 35, para 2-28). The resultant signal is applied from pin 8 of gate Z12 to terminal 6 of jack J13 and designated *M12*.

2-46. Transmit Timing No. 3/Receive Timing No. 2, Panel 2A10
(fig. 6-67)

a. *General.* Transmit timing No. 3/receive timing No. 2 panel 2A10 divides the 384-kc *modem timing signal* into various submultiple frequencies used in the transmit and receive sections of the TD-352/U. The prefixes T and M (transmit and modulate) are used with the timing signal designators when the panel is used in the transmit section of the multiplexer. The prefixes R and D (receive and demodulate) are used with the timing signal designators when the panel is used in the receive section of the multiplexer. The frequencies of the timing signals generated are: 192 kc, 96 kc, 48 kc, 24 kc, 16 kc, and 8 kc. The frequency division is accomplished by a conventional countdown chain consisting of flip-flops Z1 through Z6 (module 18, para 2-20) and associated gate circuits. Flip-flops Z1 through Z4 are divide-by-2 circuits. Flip flops Z5 and Z6 and the sixth gate (Q12) form a divide-by-3 circuit. The gate circuits and their associated buffers (transistors Q1 through Q12) are used to retime the outputs of each of the flip-flops after each frequency division. This is done to prevent accumulation of delays in the countdown circuitry and to insure proper formation of the output signal matrix. The circuits on panel 2A10 are essentially the same as the circuits described for panel 1A10 in paragraph 2-45, except for the use of different signal designations and the deletion of some circuits because there are fewer channels in the TD-352/U. The interrelationships between the input and output signals are shown in figure 6-33.

b. *Development of TFF4 (or RFF4) and $\overline{TFF4}$ (or $\overline{RFF4}$) Outputs.* The *TFF4* (or *RFF4*) signal and its complement, $\overline{TFF4}$ (or $\overline{RFF4}$), are developed as described in paragraph 2-45b.

c. *Development of TFF5 (or RFF5) and $\overline{TFF5}$ (or $\overline{RFF5}$) Outputs.* The *TFF5* (or *RFF5*) signal and its complement, $\overline{TFF5}$ (or $\overline{RFF5}$), are developed as described in paragraph 2-45c.

d. *Development of TFF6 (or RFF6) and $\overline{TFF6}$ (or $\overline{RFF6}$) Outputs.* The *TFF6* (or *RFF6*) signal is developed in the manner as described in paragraph 2-45d. Its complement, the $\overline{TFF6}$ (or $\overline{RFF6}$) signal, appears at pin 2 of flip-flop Z3 and is applied to terminal 19 of jack J13.

e. *Development of TFF8 (or RFF8) Output.* The *TFF8* (or *RFF8*) signal is developed as described in paragraph 2-45e.

f. *Development of TFF9 (or RFF9) and $\overline{TFF9}$ (or $\overline{RFF9}$) Outputs.* The *TFF9* (or *RFF9*) signal and its complement, $\overline{TFF9}$ (or $\overline{RFF9}$) are developed as described in paragraph 2-45f.

g. *Development of M21 through M26 (or D21 through D26) Outputs.* The *M21* through *M26* (or *D21* through *D26*) signals are developed as described in paragraph 2-45g.

h. *Development of M11 and M12 Outputs.* The *M11* and *M12* signals are wavetrains of 5.2- μ sec of positive-going pulses occurring at a 48-kc rate. The pulses of *M11* occur midway between the pulses *M12*; therefore, the two signals are not in phase. The *M11* and *M12*; signals are developed as follows:

(1) *Development of M11 Output.* A 96-kc output from pin 11 of flip-flop Z2 and a 48-kc output from pin 11 of flip-flop Z3 are gated in diode AND gate CR23 and CR24. The output of the AND gate is applied through buffer transistor Q14 to terminal 24 of jack J13 and designated *M11*.

(2) *Development of M12 Output.* A 96-kc output from pin 11 of flip-flop Z2 and a 48-kc output from pin 1 of flip-flop Z3 are gated in diode AND gate CR21 and CR22. The output of the AND gate is applied through buffer transistor Q13 to terminal 25 and designated *M11* or *D12*.

2-47. Noise Generator, Panel 1A11/2A11
(fig. 6 69)

a. *General.* Noise generator panel 1A11/2A11 provides a clipped, random-noise output signal containing frequencies from below 15 to above 500 kc and with amplitude peaks between 0 and -4.5 volts. The circuit consists of a noise source Q1, an eight stage amplifier (Q2 through Q9), and an output circuit (Q10, Q11, and Q12). The interrelationships between the input and output signals are shown in figures 6-33 and 6-38. These diagrams help describe the function of panel 1A11/2A11 in the transmit section of Multiplexers TD-352/U and TD-353/U.

b. *Operating Principles.* Noise source buffer transistor Q1 operates as a conventional grounded-collector amplifier. Noise voltage, produced by normal conduction through transistor Q1 and resistor R1, is applied to an eight stage amplifier consisting of transistors Q2 through Q9. The total gain of the amplifier is 120 decibels (db), and the output at the emitter of Q9 is a noise signal with amplitude of about 7 volts peak to peak. Coupling capacitor C7, between the second and third stages of the amplifier, provides amplitude equalization and high-pass filtering for the noise signal. Diodes CR1 and CR2 prevent possible damage to polarized capacitors C19 and C24, respectively, if the wrong voltage is applied to them from a defective transistor. The output from the eight stage amplifier is applied to a differential amplifier consisting of transistors Q10 and Q11. Here, the random noise signal is amplified and clipped to a peak-to-peak amplitude ranging between (0 and -4.5 volts. This signal is buffered by transistor Q12 and then applied to terminal 19 of jack J5, where it is designated as the clipped noise signal.

2-48. Receive Input and Framing, Panel 1A12/2A12

(fig. 6-70)

a. *General.* Panel 1A12/2A12 is used in the receive input section of both the TD-352/U and TD-353/U. When a difference exists in pulse repetition rates, frequencies, voltages, or figure references depending on whether the panel is used in Multiplexer TD-352/U or TD-353/U, the information for the TD-353/U is given first, followed by a parenthetic reference to the TD352/U. During 48-channel (12-channel) operation, the panel receives and regenerates a single pcm binary train. During 96-channel (24 channel) operation, the panel receives, separates, and regenerates two interleaved 48-channel (12 channel) pcm binary trains. The panel also generates a skip pulse that is applied to panel 1A13 (2A13) to frame the locally generated receiver timing signals with the incoming pcm. Panel 1A12/2A12 also generates signals used in the framing alarm circuits of panel 1A16/2A16. The interrelationships between the input and output signals are shown in figure 6-41 (fig. 636). These diagrams help describe the function of 1A12/2A12 panel in the receive section of the two multiplexers.

b. *Separation of Pcm.* The pcm in signal is applied to panel 1A12/2A12 at terminal 14 of jack J11. The pcm in signal has the rates and pulse widths listed in the chart below. From terminal 14, the pcm in signal is applied to pin 7 of sampler modules Z1, Z3, and Z5 (module 08, para 2-14). The timing signal for sampler Z1 appears at terminal 18 of jack J11. and is designated *timing A*. This signal consists of a train of positive-going spike pulses with a rate of 2,304 kc (576 kc) and is applied, through dc shifting network resistors R1 and R2 and capacitor C1, to the base of inverter transistor Q1. Transistor Q1 inverts the signal and applies the output to pin 2 of sampler Z1. The timing signal for sampler Z3 appears at terminal 2 of jack J11. and is designated *timing B*. The *timing A* and *timing B* signals are similar, except for their phase relationship; *timing B* signal pulses occur halfway between the pulses of the *timing A* signal, or approximately 0.22 , μsec (0.87 μsec) after the pulses of the *timing A* signals. The *timing A* and *timing B* signals sample the same pulse in 48-channel (12-channel) operation; however, only the output of the *timing A* circuit is used. In 96-channel 24 channel operation, the *timing A* signal samples the pulses in one binary train, while the *timing B* signal samples the pulses in the other train of the interleaved pair. The timing for sampler Z5 is discussed in e(2) below.

Rate (kc)	Number of channels operating	Pulse width (sec)
12	576	1.73
24	1,152	.87
48	2,304	.43
96	4,608	.22

c. *Development of Sampled Pcm and Pcm to Aux Outputs.* The outputs of sampler Z1 are the pcm logic 1 pulses (pin 10) and the logic 0 pulses (pin 6). These outputs are present only during the time that the *timing A* signal is present at pin 2. When this occurs, these outputs are applied to pins 9 and 3 of flip-flop Z2 (module 09, para 2-15). In flip flop Z2, the logic 1 and logic 0 pulses are used to regenerate the binary train. The regenerated output is applied from pin 10 of flip-flop Z2 through buffer transistor Q4 to terminal 10 of jack J11 where it is designated as the *sampled pcm* signal. The regenerated output from pin 10 is also applied to the bases of output driver transistors Q2 and Q3. The output of these transistors, connected in parallel to increase the current-carrying capacity of the circuit, is applied through a dc-shifting network to the base of output buffer transistor Q5. The output of transistor Q5 is applied to terminal 4 of jack J11, where it is designated as the *pcm to aux* signal.

d. *Development of Alt Pcm Out Output.* The output of sampler Z3 is developed the same as the output of sampler Z1, with the exception that the output of sampler Z3 is delayed 0.2 μ sec by delay line DL1. This output is applied to terminal 1 of jack J11 and is designated as the *alt pcm out* signal.

e. *Development of Skip-Pulse Output.* Panel 1A12/2A12 contains a circuit for framing the receive timing section of the multiplexer to the incoming pcm signal. This function is controlled by a skip-pulse circuit which is described in (1) through (4) below.

(1) *General.* The sampler circuit will select the correct binary train of an interleaved pair only when its timing signal is correctly phased with the incoming pcm signal. A skip pulse generated in panel 1A12/2A12 is used to shift the timing signals generated in panel 2A13 1A13 until correct phasing is attained. The skip pulse is developed in an exclusive OR circuit by comparing a constant reference signal with the pcm address signal. Circuit operation is normal when the reference signal is of opposite phase to the address signal. When an out-of-phase condition exists, the circuit will generate skip pulses until the correct address pulse is found. This circuit is described in more detail in (3) below. The output of the exclusive OR circuit is applied to the skip-pulse gating circuit ((4) below) as a negative error signal. The other input to this circuit is an 8-kc reference signal derived from the FF9 signal. The gate circuit passes the 8-kc reference signal whenever 8 or 10 consecutive error signals are present. In addition, an *alarm control* signal is generated by applying the signal from the skip-pulse gate circuit to control a differential amplifier, the output of which is applied through an inverter to terminal 29 of jack J11. ((4) below). The complement of the reference signal applied to the exclusive OR circuit is also applied through a buffer transistor to terminal 5 of jack J11. as the *alarm timing signal* ((4) below).

(2) *Inputs to exclusive OR circuit.*

(a) *Address signal input.* The *pcm in* signal from terminal 14 of jack J11. is applied to pin 7 of sampler Z6 (module 08, para 2-14). The other input to the sampler is the *timing C* signal which consists of positive-going 8-kc spikes. This signal is applied from terminal 19 of jack J11. through pulse shaper Q27 to buffer transistor Q26. The pulse shaper transistor sharpens the *timing C* signal and removes any noise spikes. The output of buffer transistor Q26 is applied to pin 2 of sampler Z6 through inverter Q21. The output of buffer Q26 is also applied to terminal 20 of jack J11. and designated as the *receive address* signal (b) below). In sampler Z6, the 8-kc timing pulses sample the pcm signal until the address pulses are found. The outputs of sampler Z5 appear at pins 6 and 10 and are applied to pins 9 and 3, respectively, of flip-flop Z6 (module 09, para 2-15). Flip-flop Z6 produces a 4-kc square wave when the transmit and receive sections are operating with a 4-kc address and the receive section is in frame. Flip-flop Z6 produces a 2-kc square wave if the transmit and receive sections are operating with a 2-kc address and the receiver is in frame. If the receive section is not in frame, with either address, the output of Z5 will be a train of random rectangular pulses. The output of flip flop Z6 is taken from pin 10 and is applied to buffer transistor Q22 as one of the inputs to the exclusive OR gate.

- (b) *Reference signal input.* The constant reference signal for the exclusive OR circuit is a 2-kc or 4-kc signal, depending on the position of ADDRESS switch S8, mounted on the service facility panel. If the desired pcm signal contains a 2-kc address signal, the ADDRESS switch is operated to the SLAVE position. If the desired pcm signal contains a 4-kc address, the ADDRESS switch is operated to the MASTER position. When the ADDRESS switch is in the MASTER position, the 8-kc train of positive going output pulses from terminal 20 of jack J11 (receive address signal) is applied back into terminal 8 of jack J11 through the external ADDRESS switch. From terminal 8, the 8-kc receive address signal (now called 4-kc RCVR address) is applied to pins 3 and 9 of flip-flop Z8 (module 09, para 2-15). Flip-flop Z8 develops a 4-kc square wave at pin 2 and a complementary signal at pin 10. The output from pin 2 is applied to buffer transistor Q25 as the reference input to the exclusive OR gate. The complementary signal on pin 10 is applied through buffer transistor Q28 to terminal 5 of jack J11 as the alarm timing signal. When the ADDRESS switch is in the SLAVE position, the 8-kc receive address signal output from terminal 20 of jack J11 is applied through the external ADDRESS switch back into terminal 9 of jack J11. From terminal 9, the signal (now called 2-kc rcvr address) is applied to pins 3 and 9 of flip-flop Z7 (module 09). Flip-flop Z7 produces a 4-kc square wave (at pin 2), which is applied through diodes CR13 and CR14 to pins 2 and 10 of flip-flop Z8. Flip-flop Z8 then divides the 4-kc input by 2 and applies a 2-kc signal from pin 2 of the flip-flop to buffer transistor Q25 as the reference input to the exclusive OR circuit.
- (3) *Operation of exclusive OR circuit.* As described in (2) above, the inputs to the exclusive OR circuit are an address signal and a constant reference signal. These signals are applied to buffer transistors Q22 and Q25, respectively. The exclusive OR circuit, consisting of transistors Q23 and Q24, produces an output signal of -4.5 volts only when the two input signals are in phase. When the signals are out of phase, the output is 0 volt. When the two inputs from buffer transistors Q22 and Q25 are both at a 0-volt level, both transistors in the exclusive OR circuit are cut off; because there is no current flow, the collectors are at a -4.5-volt level. This level is applied through buffer transistor Q15 as the output. If both inputs to Q22 and Q25 are at a -4.5volt level, the transistors in the exclusive OR circuit will be cut off. This happens because the input to the base of each transistor is also applied to the emitter of the other transistor, biasing the transistors into cutoff, and the signal applied to the bases is not sufficient to make the transistors conduct. In this case, the output at the collectors is again at -4.5 volts. If one input is at a 0-volt level and the other is at a -4.5volt level, one transistor will conduct and the other will be cut off. The current flow through the conducting transistor will cause the collectors of the exclusive OR gate to go to the 0-volt level, which is applied to buffer transistor Q15. A summary of these exclusive OR circuit conditions follows:

Address input, base of Q22	Reference input, base of Q25	Collectors output, Q23 and Q24
0	-4.5	0
-4.5	0	0
-4.5	-4.5	-4.5
0	0	-4.5

- (4) *Skip-pulse gating circuit.* The output circuit used to develop the skip pulse consists of AND gate diodes CR6 and CR7; buffer transistors Q14, Q15, and Q17; inverter transistor Q16; storage capacitor C17; and differential amplifier transistors Q18 and Q19. The output of the exclusive OR circuit represents one single error. Since single random errors would continually tend to drive the unit into the alarm condition, the skip pulse is produced only after 8 or 10 consecutive errors. Random errors do not appreciably affect the operation of the unit, but if 8 or 10 errors occur, the unit is definitely out-of-frame. The circuit controlling this function operates as follows. The negative-going output of the exclusive OR circuit is applied through buffer transistor Q15 to storage capacitor C17. The stored voltage on the capacitor controls the operation of differential amplifier Q18, Q19, which controls the output of AND gate diodes CR6 and CR7. The two inputs to the AND gate diodes are the error signal from the exclusive OR circuit (applied through transistor Q15 to AND gate diode CR7) and the RFF9 signal (applied to AND gate diode CR6 through the following circuit). The RFF9 signal is an 8-kc pulse which is applied from terminal 17 of jack J11 to buffer transistor Q11. The output of - transistor Q11 is applied through buffer transistor Q12 to pulse shaper Q13. The output of pulse shaper Q13 is a train of 8-kc spikes and is applied through buffer transistor Q14 to AND gate diode CR6. The AND gate diodes pass the 8-kc spike pulse signal to the base of buffer transistor Q26 when the negative error signal is present. When the error signal is applied to the AND gate, it is also applied to capacitor C17. If the error is a single pulse, capacitor C17 will not charge to a sufficient level to drive normally cutoff differential amplifier transistor Q18 into conduction, and the charge on C17; will leak off. However, if there is a train of 8 to 10 error pulses, the resulting charge on capacitor C17 will drive transistor Q18 into conduction. When this occurs, transistor Q16 (in series with Q18) will also conduct, passing the error signal applied to its base to output buffer transistor Q17. The signal at the emitter of transistor Q17 is applied to terminal 25 of jack J11 and is designated as the *skip-pulse* signal. The complement of the control signal from the differential amplifier is applied from the collector of transistor Q19, through inverter transistor Q20, to terminal 29 of jack J11 where it is designated as the *alarm control* signal.

2-49. Receive Timing No. 1, Panel 1A13

(fig. 6-72)

a. *General.* Panel 1A13 provides timing signals for the receive section of the TD-353/U. The main input to the panel is the timing in signal which appears at terminal 1 of jack J6 and consists of a 2,304-kc train of positive-going spike pulses. The timing signals supplied by panel 1A13 are developed from this signal and the *skip pulse* (terminal 15) and *receive address* (terminal 10) signals discussed in *b* through *f* below. The interrelationships between the input and output signals are shown in figure 6-41.

b. *Skip-Pulse Circuit.*

- (1) The timing in signal is applied to the base of buffer transistor Q1 and inverter transistor Q2. The output of transistor Q1 is detected by R4 and CR6 and applied to terminal 9 of jack J6 as the *timing in monitor* signal. The output of transistor Q2 is applied through delay circuit L3, L4 to pin 2 of pulse shaper Z3 (module 30, para 2-24). The output appearing at pin 9 of module Z3 is a 2,304-kc positive-going spike pulse signal and is applied to the bases of gate transistors Q4 and Q11. The output appearing at pin 3 of pulse shaper Z5 is a 2,304-kc negative-going spike pulse signal and is applied to pin 2 of pulse shaper Z5 (module 30) through delay line DL1. The delay line introduces a 0.2- μ sec delay in the negative-going signal, causing it to occur approximately midway between the pulses of the positive-going signal.

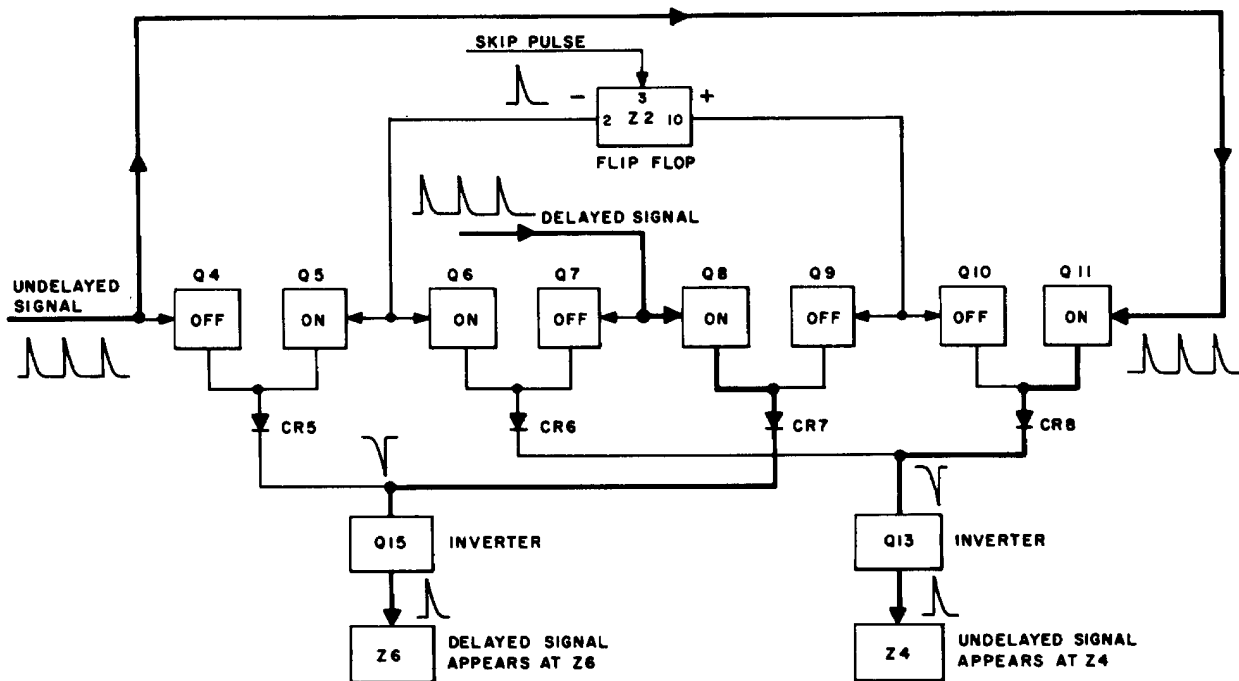
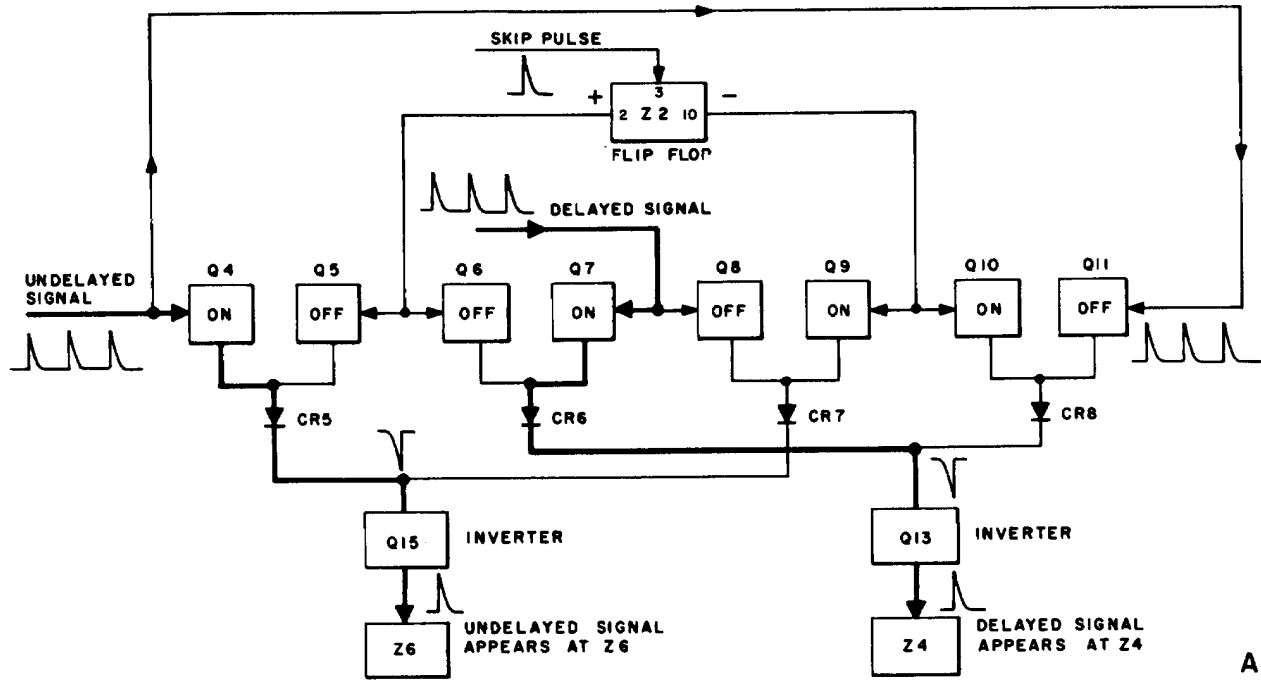


Figure 2-32. Delayed/undelayed timing signal gate circuit.

The output of pulse shaper Z6 is applied from pin 9 to the bases of gate transistors Q7 and Q8. Transistors Q4 through Q8 effectively operate as a double-pole, double-throw switch (fig. 2-32), which delivers the output of pulse shapers' Z3 and Z5 to pulse shapers Z4 and Z6.

- (2), The gate circuit, consisting of transistors Q4 through Q11. acts to automatically shift the timing back a half bit (0.2 μ sec) each time the circuit receives a skip pulse. A skip pulse is applied to the panel when the unit drops out of frame (para 2-48e). By dropping the timing back a half bit, the square wave address signal developed by the timing pulses is shifted along its base. The process repeats itself until the resulting address signal coincides with the pcm train. The shifting of the timing train is accomplished by applying the undelayed and delayed timing signals from modules Z3 and Z5 to the gate circuit, which applies them to the two output circuits and interchanges them each time a skip pulse is applied to the gate circuit.
- (3) The skip-pulse signal is applied to the panel through terminal 15 of jack J6 to pulse amplifier Z1 (module 33, para 2-27). The output of module Z1 appears at pin 9 and is applied to pin 3 of flip flop Z2 (module 18, para 2-20). This signal is positive-going and controls the state of the flip-flop. In one state, the signal causes a positive voltage to appear at pin 2 and a negative voltage to appear at pin 10. The positive voltage is applied to the bases of transistors Q5 Q6 and cuts them off. When transistors Q5 and Q6 are cut off, transistors Q4 and Q7 conduct. The negative voltage at pin 10 of flip-flop Z2 is applied to the bases of transistors Q9 and Q10, turning them on. When transistors Q9 and Q10 are conducting, transistors Q8 and Q11 are cut off. In this condition (A, fig. 2-32), transistors Q4 and Q7 act as emitter followers. Transistor Q4 passes the undelayed timing signal through inverter Q15 to pulse shaper Z6, and transistor Q7 passes the delayed timing signal through inverter Q13 to pulse shaper Z4. When the next skip pulse changes the state of flip-flop Z2 so that pin 2 is negative and pin 10 is positive, transistors Q5 and Q6 will conduct, turning transistors Q4 and Q7 off. Transistors Q8 and Q10 will be turned off and transistors Q8 and Q11 will be turned on. The undelayed timing signal will therefore be conducted to pulse shaper Z4 and the delayed signal to pulse shaper Z6 (B. fig. 2-32).
- (4) One of the outputs of the gating circuit is applied to inverter transistor Q13, and one is applied to inverter transistor Q16. The output from inverter transistor Q13 is applied through buffer transistor Q14 to terminal 17 of jack J6 and is designated as the *decoder clock* signal. In addition, the output of transistor Q14 is applied to pin 2 of pulse shaper Z4 (module 30, para 2-24). The output of module Z4 appears at pin 9 and is applied through buffer transistor Q15 to terminal 18 FF4 jack J6, where it is designated as the *receive aux clock* signal. Also, the output of module Z4 is applied to terminal 22 of jack J6 as the *timing A* signal and to pin 2 on gate modules Z10 and Z11 (module 23, para 2-22). The output from inverter transistor Q16 is applied to pin 2 of pulse shaper Z6 (module 30, para 2-24). The output of module Z6 appears at pin 9 and is applied through transistor Q17 to terminal 2 of jack J6, where it is designated as the *sync out rcvr* signal. The output of module Z6 is also applied to terminal 19 of jack J6 as the *timing B* signal and to pins 3 and 9 of flip-flop Z7 (module 09, para 2-15).

c. *Development of address Digit Gate Signal.* The address digit gate signal is produced by gating the M17 and M26 signals together in an AND gate consisting of diodes CR24 and CR23. The M17 signal is applied to terminal 26 of jack J6 and consists of a train of 48-kc positive-going pulses, 2.6- μ sec wide. The D26 signal consists of a train of 8-kc positive-going pulses, 20.8- μ sec wide. The result of the gating action is that the 8-kc pulse blanks out five of every six FF4 the 48-kc pulses. The resulting positive-going signal is applied to the base of inverter transistor Q18. The output of inverter transistor Q18 is applied through buffer transistor Q29 to terminal 24 of jack J6 and is designated as the *address digit gate* signal. The output of transistor Q18 is also applied to pin 11 of module Z10.

d. *Divide-By-6 Countdown Chain.* Flip-flops Z7, Z8, and Z9 operate in conjunction with AND inhibitor Z12 as a divide-by-6 countdown chain. The countdown chain operates similar to the one described in paragraph 2-42f. The input to the countdown chain is 2,304 kc, and a 384-kc output is taken from pin 2 of flip-flop Z9. This signal is applied through buffer transistor Q26 to terminal 21 of jack J6 and designated as the 384-kc s.w. signal. The signal from pin 10 of flip-flop Z8 is applied through buffer transistor Q24 to terminal 20 of jack J6 and designated as the RFF2B signal. Other outputs of the countdown chain are described in e and f below.

e. *Development of Timing C Signal.* The timing C signal is developed by gate Z10 (module 23, para 2-22). The output of gate Z10, pin 4, is applied through buffer transistor Q28 to terminal 30 of jack J6 and is designated as the timing C signal. This signal consists of a wavetrain of positive going spike pulses at an 8-kc rate. The chart below shows the source of the inputs to gate Z10.

Signal	Source	Input pin of gate Z10
384-kc square wave	Pin 10, flip-flop Z9 ^a	8
768-kc rectangular wave	Pin 2, flip-flop Z8 ^a	9
1,152-kc square wave	Pin 10, flip-flop Z7 ^a	10
Address digit gate	Inverter transistor Q18	11
2,304-kc spike pulses	Pin 9, pulse shaper Z4	2

^a Through associated buffer transistors shown in figure 6-72.

f. *Development of Matrix FF4 Signal.* The matrix FF4 signal is developed by gate Z11 (module 23, para 2-22). Matrix FF4 signal is a series of narrow pulses which occur at a 384-kc rate. The chart below shows the source of the inputs to gate Z11.

Signal	Source	Input pin of gate Z10
1,152-kc square wave	Pin 2, flip-flop Z7 ^a	8
768-kc rectangular wave	Pin 2, flip-flop Z8 ^a	9
384-kc square wave	Pin 10, flip-flop Z9 ^a	10
2,304-kc spike pulses	Pin 9, pulse shaper Z4	2

^a Through associated buffer transistors shown in figure 6-72.

2-50. Receive Timing No. 1, Panel 2A13

(fig. 6-74)

a. *General.* Panel 2A13 provides tuning signals for the receive section of Multiplexer TD-362/U. The interrelationships of the input and output signals are shown in figure 8-38.

b. *Basic Timing Signal Input.* Most of the timing signals generated by panel 2A13 are developed from the timing in signal which appears at terminal 2 of jack J6 and consists of a 576-kc train of positive-going spike pulses. This signal is applied to delay line DL1 as described in c below. It is also applied through resistor R1 to a peak detector where a dc monitoring signal is developed. This signal is applied to terminal 23 of jack J6 where it is designated as the timing in monitor signal.

c. *Development and Phasing of 1,152-kc Pulse.* The 576-kc timing in signal is applied to delay line DL1 where a 0.2-μsec delay is introduced. The output of delay line DL1 is coupled through capacitors C3 and C4 to the base of inverter transistor Q1. The output of transistor Q1 is coupled through capacitor C5 to the base of delay circuit transistor Q2. Transistor Q2 conducts each time a pulse is applied to its base, producing positive-going pulses at its collector.

- (1) *Frequency doubling.* The positive-going pulses at the collector of transistor Q2 cause current to flow in delay line DL2. Diode CR4 presents an open circuit to the negative reflections of the output of delay DL2. The positive reflections from delay DL2, however, join the original signal, therefore doubling the frequency. The resultant output is an 1,152-kc train of positive-going spike pulses, coupled through capacitor C6 to the base of inverter transistor Q3.

(2) *Pulse shaper Z1.* The pulses at the base of transistor Q3 are amplified, inverted, and applied to pin 2 of pulse shaper Z1 (module 30, para 2-24). Pulse shaper Z1 produces a train of 1,152-kc positive going spike pulses at pin FF2B. During normal operation, inhibitor transistor Q4 is shut off and permits the output of pulse shaper Z1 (pin 9) to pass to pins 3 and 9 of flip-flop Z2 (module fig, para 2-15). If the circuit is out of frame, transistor Q4 is turned on to inhibit the output of pulse shaper Z1 (pin 9) by shorting it to -4.5 volts. Refer to *m* below for development of the inhibit signal. The output, pin 8, of pulse shaper Z1 is applied to pin 8 of flip-flop Z5 (module 18, para 2-20). Flip-flop Z5 is part of the skip-pulse circuit (0 below).

d. Divide-By-6 Countdown Chain. Most of the timing outputs from the panel are developed from frequencies developed in the divide-by-6 circuit. (Refer to paragraph 2-42f for a similar divide-by-8 circuit.) The divide-by-8 circuit consists of AND gate Z8 (module 11, para 2-18), flip-flops Z2 and Z7 (module 09, para 2-15), and flip-flop Z1 on panel 2A10. The input to the divide-by-8 circuit is 1,152 kc and the output is 192 kc. The inputs and the outputs to the circuit are described in (1) through (5) below.

(1) *Basic input frequency.* The basic input frequency to the divide-by-8 circuit is a train of 1,152-kc positive-going spike pulses from pin 9 of pulse shaper Z1 (*c* above).

(2) *Inputs to AND gate Z6.* AND gate Z6 module in the countdown chain has three inputs as described in (a), (b) and (c) below.

(a) *576-kc input.* A branch of the 576-kc square wave output of buffer transistor Q12 is applied to pin 10 of AND gate Z6. This is developed from the 1,152kc signal applied to flip-flop Z2.

(b) *384-kc input.* A 384-kc signal is applied from the emitter of buffer transistor Q16 to pin 7 of AND gate Z6.

(c) *192-kc input.* A 192-kc signal is developed by flip-flop Z1 on panel 2A10, which is part of the countdown chain. The 192-kc input to AND gate Z6 is applied from pin 2 of flip-flop Z1 to terminal 14 of jack J13 on panel 2A10. This signal is designated $\overline{RFF4}$ and is applied to terminal 15 of jack J9. From terminal 15, the signal is applied to pin 5 of AND gate Z6.

(3) *576-kc output of countdown chain.* The input to flip-flop Z2 is at 1,152 kc and the output on pins 2 and 10 is at 576 kc. The output from pin 10 is used to develop the *decoder clock* and $\overline{RFF1}$ signals (*e* and *f* below) and the *timing A* and *rcvr aux clock* signals (*g* and *h* below). The output from pin 2 is used to develop the *timing B* and *sync out rcvr* signals (*j* and *k* below), and the $\overline{RFF1}$ signal (*i* below).

(4) *384-kc output of countdown chain.* The output of pin 2 of AND gate Z6 is applied to pin 2 of flip-flop Z7, which is similar to flip-flop Z2 and divides the input by 2. The output of Z7, which is a 384-kc signal is taken from pins 2 and 10. The output from pin 10 is applied through buffer transistor Q13 to terminal 13 of jack J6 where it is designated as the $\overline{RFF2}$ signal. The output from pin 10 is also applied through capacitor C14 and resistors R38 and R39 to the base of pulse shaper transistor Q14. The network at the collector of transistor Q14 reshapes the input, while diode CR13 removes any negative overshoot in the signal, leaving a 384-kc positive-spike output. This output is applied through buffer transistor Q15 to terminal 14 of jack J6 and is designated as the *modem timing* signal. The output from pin 2 of flip-flop Z7 is applied through buffer transistor Q16 to terminal 27 of jack J6 where it is designated $\overline{RFF2}$. Another output from transistor Q16 is applied to pin 7 of AND gate Z6 as part of the feedback circuit, and to pin 2 of pulse shaper Z8 as described in *m* below.

(5) *190-kc output of countdown chain.* The 192-kc outputs of the Divide-By-6 chain are obtained from flip-flop Z1 on panel 2A10 (para 2-46).

e. *Development of Decoder Clock Signal.* Flip flop Z2 (module 09, para 2-15) produces a 576-kc square wave output at pin 10 and a complementary signal at pin 2 (*d* above). The output from pin 10 is applied to the base of driver transistor Q6. The output of transistor Q6 is taken from the emitter and is applied to delay line DL3, where the signal is delayed 0.15 μ sec. The output of delay line DL3 is applied through buffer transistor Q7 to terminal 31 of jack J6 where it is designated as the *decoder clock* signal.

f. *Development of $\overline{RFF1}$ Signal.* The 576-kc square wave output at pin 10 of flip-flop Z2 is also applied through buffer transistor Q5 to terminal 24 of jack J6 where it is designated as the $\overline{RFF1}$ signal.

g. *Development of Timing A Signal.* The 576-kc output from the emitter of transistor Q5 is also applied to pin 2 of pulse shaper Z3 (module 30, para 2-24). Pulse shaper Z3 converts the square wave signal to a train of 576-kc positive-going spike pulses. This signal is taken from pin 9 of pulse shaper Z3 and is applied to terminal 30 of jack J6 where it is designated as the *timing A* signal.

h. *Development of Receive Aux Clock Signal.* The output at pin 9 of pulse shaper Z3 is also applied to the base of gate transistor Q8 through resistor R20, capacitor C10, and diode CR9. Transistors Q8, Q9, and Q10 form a squelch circuit, which controls the application of the *rcvr aux dock* signal to terminal 11 of jack J6 in conjunction with the alarm on signal appearing at terminal 16 of jack J6. The *alarm on* signal is applied to the base of transistor Q9. When the alarm on signal is at +10 volts, which is the case when there is no alarm, Q9 will conduct, applying a negative going signal- to the base of Q8. Transistor Q8 will then conduct, applying the signal from pulse shaper Z3 through buffer transistor Q10 to terminal 11 of jack J6 where it is designated as the *rcvr aux clock* signal. When the *alarm on* signal is at 0-volt which is the case when there is an alarm, Q9 is cut off. A positive going signal is therefore applied to the base of transistor Q8 which, in turn, cuts off and inhibits the signal applied to its emitter from reaching buffer transistor Q10. In this case, there is no *rcvr aux clock* signal at terminal 11 of jack J6

i. *Development of $\overline{RFF1}$ Signal.* The 576-kc square wave output of pin 2 of flip-flop Z2 is applied- through of buffer transistor Q12 to terminal 10 of jack J6 where it is designated as the $\overline{RFF1}$ signal.

j. *Development of Timing B Signal.* The 576-kc square wave output of buffer transistor Q12 is also applied to pin 2 of pulse shaper Z1. (module 30, para 2-24). Pulse shaper Z9 converts the square wave to a train of 576-kc positive-going pulses. The output appearing at pin 9 of pulse shaper Z9 is applied to terminal 26 of jack J6 where it is designated as the *timing B* signal.

k. *Development of Sync Out rcvr Signal.* The 576-kc pulse output at pin 9 of pulse shaper Z1. is also applied through buffer transistor Q21 to terminal 28 of jack J6 where it is designated as the *sync out rcvr* signal.

l. *Development of Monitoring M Signal.* The monitoring M signal gives a visible indication that the receive section is searching for the address signal when the unit is out of frame. This signal is developed from the output of pin 10 of flip-flop Z1. which is -4.5 volts during normal operation. When a skip pulse appears at pin 8 of flip-flop Z1. pin 10 goes to ground potential until a pulse from pin 8 of pulse shaper Z1 resets the flip-flop. The output from pin 10 of flip-flop Z1. is applied through buffer transistor Q20 to a peak detector. The dc output of the peak detector is applied through resistor R56 to terminal 9 of jack J6 where it is designated as the *monitoring M* signal.

m. *Development of timing A.* The *timing C* signal is a wavetrain of positive-going trigger pulses at an 8-kc rate. The train is developed by eliminating pulses from the 384-kc output of flip flop Z7. The 384-kc signal from the flip-flop is applied to pin 2 of pulse shaper Z8 (module 30, para 2-24). The output of pulse shaper Z8 is a pulse which repeats every 125 μ sec and is applied directly to terminal 25 of jack J6 as the *timing C* signal. However, the signal is applied to terminal 25 only when the inhibiting circuit ((1) below) operates to allow it to pass. The inhibiting circuit allows only every 48th pulse to pass;

therefore, the resulting frequency of the timing C signal is 8 kc.

- (1) The inhibiting circuit contains a two-input AND gate consisting of diodes CR18 and CR19; a three-input AND gate consisting of diodes CR15; CR16; and CR17; and transistors Q17, Q18, and Q19. The circuit accepts four input signals; RFF4 (192 kc), RFF5 (96 kc), D26 (8 kc), and RFF6 (48 kc). It produces an 8-kc signal which is inverted and used as a blanking signal to inhibit the output of pulse shaper Z8.
- (2) The inputs to the AND gate consisting of diodes CR18 and CR19 are the D26 signal appearing at terminal 21 of jack J8 and the RFF6 signal appearing at terminal 22 of jack J8. The D26 signal is an 8-kc wavetrain of positive going pulses with a duration of 20.8 usec. The RFF6 signal is a 48-kc wavetrain of positive-going pulses with a duration of 10.4 usec. The output of the AND gate is an 8-kc wavetrain with a pulse duration of 10.4 usec. This signal is applied to diode CR17 which is part of the three-input AND gate ((3) below).
- (3) The inputs to the AND gate consisting of diodes CR15, CR16, and CR17 are the RFF4 signal appearing at terminal 15 of jack J8, the RFF5 signal appearing at terminal 24 of jack J8, and the output of the first AND gate described in (2) above. There is an output from the AND gate whenever all three inputs are in coincidence; this occurs at an 8-kc rate for duration of 2.6 usec for each pulse. The output of the AND gate is applied through a dc-shifting network, consisting of resistors R47 and R48 and capacitor C23, to the base of inverter transistor Q18. The inverted output of transistor Q18 is clamped to a -4.5-volt level by diode CR20 and then applied through a dc-shifting network, consisting of resistors R50 and R51 and capacitor C24, to the base of inverter transistor Q19. The inverted output of transistor Q19 is applied to pin 9 of pulse shaper Z8 to inhibit its output. When the input to transistor Q19 is at a -4.5-volt level, the output of pulse shaper Z8 is allowed to pass to terminal 26 of jack J8. When the output of transistor Q19 is at a 0-volt level, the output of pulse shaper Z8 is clamped to -4.5 volts and there is no output.

n. Development of Address Digit Gate. The output of the AND gate consisting of diodes CR18 and CR19 mentioned in *m* above is also used to develop the address digit gate signal. The output of the AND gate is applied through buffer transistors Q17 and Q22 to terminal 17 of jack J8, where it is designated as the *address digit gate* signal.

O. Skipping Operation. As explained in paragraph 2-48, address signals are incorporated in the pcm signal to assure that the timing signals are coincident with their related pcm signals. If noncoincidence occurs, one of the address signals develops skip pulses to shift the timing until coincidence does occur. The positive-going *skip pulse* enters the panel at terminal 7 of jack J8 and is applied through a dc-shifting network, consisting of resistors R28 and R29 and capacitor C11, to the base of inverter transistor Q11. The output of transistor Q11 is applied to pin 2 of pulse shaper Z4 (module 30, para 2-24). The output of pulse shaper Z4 appears at pin 9 and is applied through capacitor C12 and diode CR11 to pin 5 of flip-flop Z5 (module 18, para 2-20). During normal operation the output of flip-flop Z5 keeps the base of transistor Q4 biased at cutoff (- 4.5 volts), allowing the 1,152-kc square wave signal (*c* above) to pass unaffected. When a *skip pulse* is applied to terminal 7 of jack J8, flip-flop Z5 changes state and applies a 0-volt potential to the base of transistor Q4. This turns transistor Q4 on and one pulse of the 1,152-kc signal is short circuited to -4.5-volt supply. As a result, there is one missing pulse in the train entering pins 3 and 9 of flip-flop Z2. The next pulse from pin 8 of pulse shaper Z1 is applied to pin 8 of flip-flop Z5 and immediately resets the flip-flop. This cuts off transistor Q4 so that only one pulse of the 1,152-kc train is blanked for each *skip pulse*. By eliminating one pulse at a time from the 1,152-kc train, the timing is shifted one pulse width, or 0.86 usec. The shifting is repeated until the correct coincidence is established and no more skip pulses are applied to the panel.

2-51. Decoder No. 1, Panel 1A14/2A14

(fig. 6-76)

a. *General.* Decoder No. 1 panel 1A14/2A14 operates in conjunction with decoder No. 2 panels 1A15 (TD-353/U) and 2A15 (TD-352/U) to convert the incoming pcm signal to a pam signal. This operation also restores the original dynamic range to those portions of the signal that are compressed by the compander at the point of origin. Where there are differences in operating frequencies or figure references, depending on whether the panel is used in Multiplexer TD-353/ U or TD-352/U, the information for the TD-353/ U is given first, followed by a parenthetic reference applicable to the TD-352/U, The interrelationships of the input and output signals are shown in figure 6-41 (fig. 6-36).

b. *Serial Shift Register.* The primary input to panel 1A14/2A14 is the *decoder pcm* signal, which is applied to terminal 31 of jack J10. This signal has a 2,304-kc (576-kc) rate and pulse width of 0.434 usec (1.732 usec) and normally varies between -2.0 and 0 volts. From terminal 31, the signal is applied through a dc-shifting network, consisting of resistors R3 and R4 and capacitor C3, to the base of driver transistor Q1. During normal operation, gate driver transistor Q2 is saturated, driving transistor Q1 into conduction. The output of gate transistor Q1 is applied through differentiating capacitor C4 to pin 8 of flip-flop Z2 (module 18, para 2-20). Flip-flops Z2 through Z7 make up a conventional serial shift register.

- (1) *Serial shift.* The pcm data is fed into the shift register with the aid of the *decoder clock* signal, which is applied through terminal 26 on jack J10 to pin 2 of pulse shaper Z1 (module 30, para 2-24). In pulse shaper Z1, this 2,304-kc (576-kc) square wave input is converted to a train of positive-going pulses at the same frequency. This signal is applied to pin 3 of each of shift-register flip-flops Z3 through Z7. The pcm signal is also applied directly to flip-flop Z2 from transistor Q1. The 2,304-kc (576-kc) serial shift pulses sample the pcm signal in the flip-flops and cause the pcm pulses to feed into the register until the most significant digit (msd) is stored in flip-flop Z7, and least significant digit (lsd) is in flip-flop Z2. The time required for shifting the data into the serial shift register is approximately 2.6 (10.4) usec
- (2) *Parallel shift.* When the most significant digit has reached flip-flop Z7, the data in the serial register is parallel-shifted into the register consisting of flip-flops Z8 through Z13. Parallel shifting is accomplished by a 384-kc (96-kc) signal, which is designated *FF5* or *384-kc s.w.* and enters the panel at terminal 22 of jack J10. This signal is applied to pin 2 of pulse shaper Z14, which then develops a wavetrain of positive-going pulses with a 384-kc (96-kc) rate. The output is taken from pin 9 of pulse shaper Z14 and applied to the bases of buffer transistors Q3 and Q4. Transistors Q3 and Q4 operate in push-pull fashion; the signal at their emitters is applied to pins 4 and 11 of shift register flip-flops Z9, Z10, Z11, and Z13 and to pin 3 of flip-flop Z12. The 384-kc (96-kc) pulse shaper Z14 output signal is also applied to the two address inhibit gate circuits ((3) below). The 384-kc (96-kc) parallel readout pulse transfers the data in the serial shift register to the parallel shift register. The most significant digit is now in flip flop Z13 and the next most significant digit is in flip-flop Z12. The binary information is held in the parallel shift register for 2.6 usec (10.4 usec) while the data is read out into a summing circuit. The summing network consists of a resistive ladder containing resistors R40, R41, R42, R44, R45, R47, R48, and R50 through R54. The pam output is obtained from the junction of resistors R53 and R54 and is applied to terminal 1 of jack J10, where it is designated as the *decoder pam signal* and applied to panel 1A15 (2A15). Four additional signals are sent to panel 1A15 (2A15) to control the pam decoder amplifier/attenuator circuits (para 2-53). These signals are taken from the last two flip-flops of the parallel shift register and are applied to the terminals of jack J10 as follows:

Signal designation	From	To
A-----	Pin 7 of Z13-----	Terminal 3 of J10
\bar{A} -----	Pin 6 of Z13-----	Terminal 4 of J10
B-----	Pin 10 of Z12-----	Terminal 2 of J10
B-----	Pin 2 of Z12-----	Terminal 5 of J10

- (3) *Elimination of address pulses.* If the 2- or 4-kc address pulses were permitted to remain in the pcm signal, they would cause an annoying hum in the audio output. This condition is prevented by removing the address pulses before the pcm signal enters the parallel shift register. The logic 1 pulses of the address signal are removed, so that when the operation is completed, each 288th (72d) pulse of each frame is a logic 0 pulse. This function is accomplished by the use of complementary *address inhibit 1* and *address inhibit 2* signals. The pulse width of these signals is 2.6 usec (10.4 usec) and they occur at an 8-kc rate, or every 125 usec. The *address inhibit 1* signal appears at terminal 9 of jack J10 and is applied through resistor R11 to the base of gate transistor Q5. The *address inhibit 2* signal appears at terminal 7 of jack J10 and is applied through resistor R34 to the base of gate transistor Q7. Transistors Q5 and Q6 form a two-input gate circuit, and transistors Q7 and Q8 function similarly. The 384-kc (96-kc) parallel shift pulses are applied to the bases of transistors Q6 and Q8 as the second input to these gates. In each gate circuit, the first 47 (11) parallel shift pulses of a frame are permitted to transfer the least significant digit from flip-flop Z2 to dip-flop Z8. The 48th (12th) parallel shift pulse, however, is rerouted by the gate circuits and applied as a reset pulse to flip-flop Z8 to blank out any logic 1 address pulse that may be present. If the address pulse is already at logic 0, the shift pulse is ineffective. The 47 (11) parallel shift pulses are applied from the emitter of transistor Q6 through capacitor C11 and C12 to pins 4 and 11 on flip-flop Z8. When a positive-going *address inhibit 1* pulse is applied to the base of gate transistor Q5, the transistor conducts, causing its collector (also connected to the emitter of Q6) to go to a potential of -4.5 volts. With -4.5 volts applied to the emitter of transistor Q6, that transistor is cut off long enough to blank one pulse from the parallel shift signal. At the same time, the negative going complementary pulse of *address inhibit 2* signal is applied to the base of transistor Q7, cutting it off. Therefore, transistor Q8 conducts, and the parallel shift pulse appearing at its emitter is applied through capacitor C25 to pin 3 of flip-flop Z8. This resets the flip-flop if it is not already in the desired state.
- (4) *Squelch circuit.* During normal operation, +10 volts dc is applied from terminal 25 of jack J10 through a dc-shifting network, consisting of resistors R6 and R8 and capacitor C5, to the base of gate transistor Q2. This voltage keeps transistor Q2 turned on and the base of transistor Q1 at ground potential. With the base of transistor Q1 at ground potential, it conducts and the decoder pcm signal appearing at its collector is applied to the serial shift register circuits. If the receive section drops out of frame the +10 volts is removed and a zero potential squelch signal is applied to terminal 25 of jack J10, turning transistor Q2 off. This places the base of transistor Q1 at -4.5 volts, cutting it off and preventing the *decoder pcm* signal from being applied to the serial shift register circuits. Objectionable noise is prevented from entering the audio circuits by removing the *decoder pcm* signal during the time the receiver drops out of frame.
- (5) *High traffic modem timing signal.* In addition to being used as the parallel readout signal, the 384-kc (96-kc) signal from pin 9 of pulse shaper Z14 is applied to terminal 21 of jack J10, where it is designated as the high traffic modem timing signal.

2-52. Decoder No. 2, Panel 1 A15

(fig. 6-78)

a. *General.* Decoder No. 2 panel 1A15 is used in conjunction with panel 1A14/2A14 in Multiplexer TD-353/U. In panel 1A15, the outer portions of the pam signal are expanded to compensate for any compression at the point of signal origin. This function is accomplished under control of signals developed in panel 1A14/2A14. Decoder No. 2 panel also develops the *address inhibit 1* and 2 signals, the 384-kc *modem gate timing* signal, the *main pcm* signal, and the *pcm from aux monitor* signal. The interrelationships of the input and output signals are shown in figure 6-41.

b. *Decoder Pam Signal.* The *decoder pam* signal enters panel 1A15 at terminal 25 of jack J9 and is applied to the bases of gate transistors Q5 and Q10. Depending upon the collector outputs of gate transistors Q4 and Q9 (c below), the signal passes through either transistor Q5 or Q10. The signal path through transistor Q10 is not attenuated. When transistor Q5 is conducting, however, the pam signal is first attenuated by a ratio of 20 to 1 in the network consisting of resistors R10 and R11. The pam signal is then applied either from transistor Q5 to gate transistor Q6 or from transistor Q10 to gate transistor Q11. Transistors Q6 and Q11 form an OR gate. When there is an attenuated pam signal at the base of transistor Q6, it conducts and the signal is applied through buffer transistor Q12 to terminal 23 of jack J9, where it is designated as the *receive pam* signal. When there is an unattenuated pam signal at the base of transistor Q11 it conducts and the signal is similarly applied through transistor Q12 to terminal 23 of jack J9.

c. *Gate Circuits.* When the pam decoder signal is applied to panel 1A15 a decision is made in the gating circuits as to whether or not the signal should be attenuated. A *pam decoder* signal with level from 16 to 47 is applied to the attenuator circuit; levels above 47 and below 16 are applied through the unattenuated circuit. In the attenuated circuit, the signal passes through a 20-to-1 attenuator where the signals are compressed to a level proportionate to that which existed before companding.

- (1) Application of the *pam decoder* signal to the attenuated or unattenuated circuit is controlled by transistor gates Q1, Q7, Q2, and Q8. Four signals developed on panel 1A14/2A14 are applied to transistors Q1, Q2, Q7, and Q8 on panel 1A15. These signals are designated as *A*, \bar{A} , *B*, and \bar{B} and are applied to terminals 29, 27, 28, and 31, respectively, of jack J9. Signal *A* represents the most significant digit (msd) of the signal being decoded; signal \bar{A} as its complement. Signal *B* represents the next most significant digit of the signal being decoded, and \bar{B} is its complement. Signals *A*, \bar{A} , *B* and \bar{B} are applied to the bases of transistors Q1, Q8, Q2, and Q7, respectively. The first two digits of all levels from 16 to 47 are either 0, 1 or 1, 0. This property is the key for identifying the levels to be attenuated. When the level of the signal being decoded has either one of these two combinations of digits (that is, signals *A* and *B* in opposite states), the gate circuit produces an output that steers the decoded signal through the attenuator.
- (2) Assume that a signal with a level of 47 is presented to the gates. The two most significant digits for level 47 are 1 and 0. Signal *A* (msd) is a logic 1, a positive going signal. Signal *B* (the next msd) is a logic 0; however, its complement signal \bar{B} is a positive-going signal. Since positive-going signals *A* and \bar{B} arrive simultaneously at the bases of transistors Q1 and Q7, both transistors conduct and set the collector of transistor Q1 at a -4.5-volt potential. This -4.5-volt potential is applied to the base of inverter transistor Q3 and to the base of gate transistor Q9. Transistor Q9 conducts and applies a +4.5-volt potential to the base of gate transistor Q11 and to the emitter of gate transistor Q10, cutting off both transistors. This prevents passage of the unattenuated signal to the output circuit. Transistor Q3 also conducts, its collector goes to +4.5 volts, and a more positive bias is applied to the base of gate transistor Q4. This cuts off transistor Q4 and allows gate transistor Q5 to conduct.

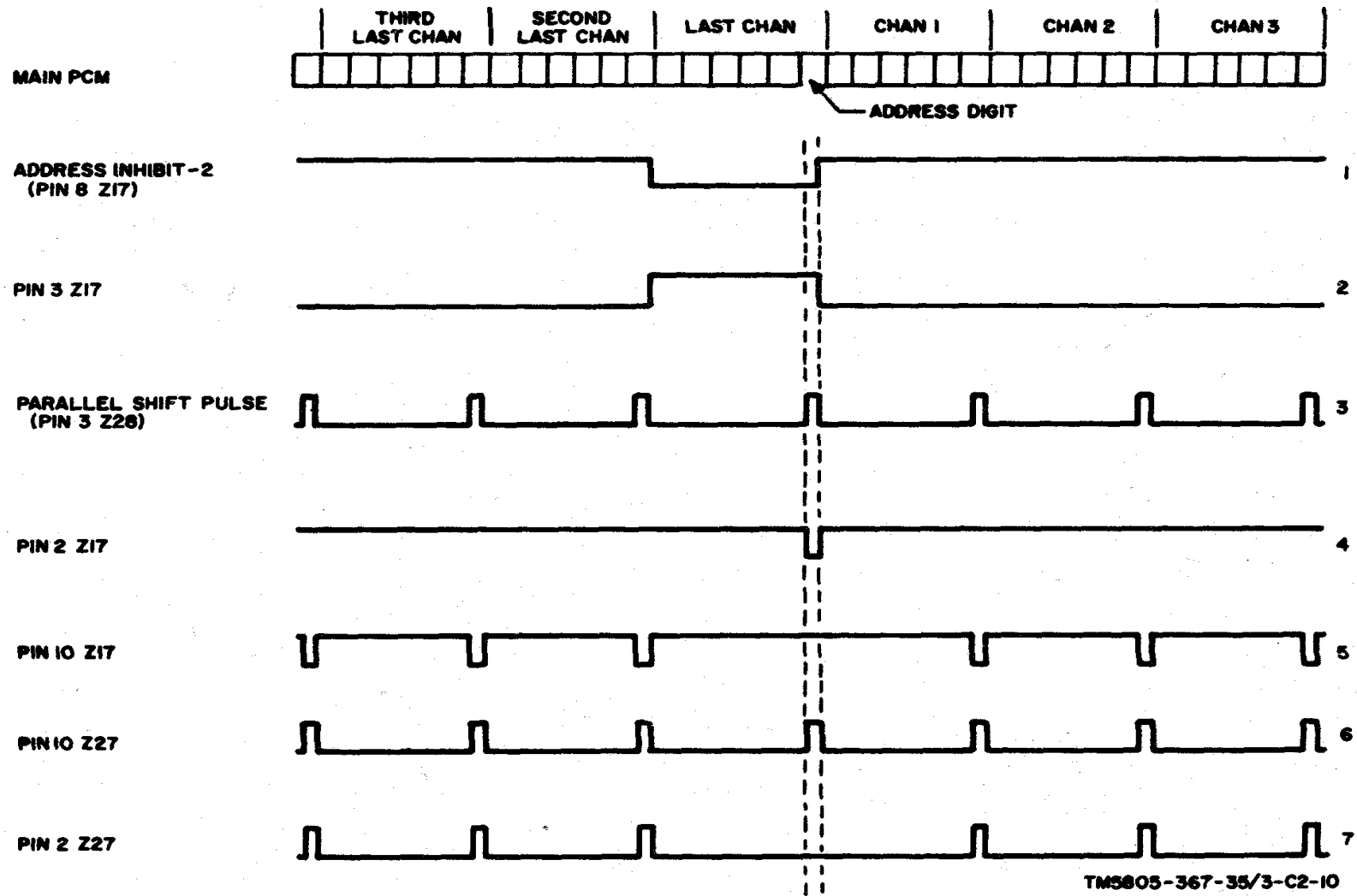


Figure 2-32.1. Address inhibit circuit, idealized waveforms

2-51 .1 Decoder No. 1 Panel 1A14A/2A14A
(fig. 6-76.1)

a. *General.* Decoder No. 1 panel 1A14A/2A14A operates in conjunction with decoder panel 1A15 (TD-353/U) and 2A25 (TD-352/U) to convert the incoming pcm signal to a pam signal. Where there are differences in operating frequencies or figure references, depending on whether the panel is used in Multiplexer TD-353/U or TD-352/U, the information for the TD-353/U is given first, followed by a parenthetical reference applicable to the TD-352/U. The interrelationships of the input and output signals are shown in figure 6-41 (fig. 6-36). The decoder is basically a digital-to-analog converter. The 6-bit pulse code being decoded, consisting of some sequence of 6 binary digits ("1's" and "0's"), is serially read into a six flip-flop shift register. A parallel readout pulse then occurs which shifts all the digits into what is basically a six flip-flop parallel shift register. The parallel shift register stores and reads out the pulse code digits while the next 6-bit pulse code is being read into the serial shift register. Depending on the digits in the parallel shift registers, each register drives a voltage clamp either to a precision dc reference voltage or to ground potential. The six voltage clamps parallel-feed their dc output to steps on a resistive ladder network with binary weighting on its inputs. The ladder network combines the inputs, forming the analog pam sample at its output. To match the decoder expanding characteristic closer to the coder compressing characteristic, two additional clamps are fed into the resistive ladder. Each clamp has the binary weighting of one-half pam level at the ladder output. When level 15 occurs, one of the clamps goes from a logic "1" to a "0", subtracting a one-half pam level from the ladder output; when level 48 occurs, the other clamp goes from a logic "0" to a "1", adding a one half pam level to the ladder output. Each clamp is controlled by gates which have the correct output at the correct time for pcm codes 15 and 48. Address inhibit circuitry removes the address digit by inhibiting the least significant flip-flop in the parallel shift register during readout to the ladder network of the last word in each frame. Variable resistor R5 establishes the correct time delay between the *decoder clock* signal at terminal 26 of jack J8, and the signal at J3; variable resistor R106 establishes the correct time delay between the *384 kc sw (FF5)* signal and the signal at jack J7 of the panel. Switch S1 is operated to MT when panel 1A14A/2A14A is used in the TD-352/U and to HT in the TD-353/U. In addition to the pam output, the 1A14A/2A14A panel provides five other outputs; four (*A*, *A̅ B* and *B̅*) to drive the decoder pam amplifier/attenuator circuits in the 1A15 and 2A15 panel, and one to provide the high traffic modem timing.

b. *Serial Shift Registers.*

- (1) *Decoder pcm.* A 2,304 kc (576 kc) full width pcm train (see *main pcm* waveform fig. 6-41) (fig. 6-36) varying nominally between -2.0 and 0 volts feeds into the panel via terminal 31 of jack J8 to pulse shaper Q5, Q6. The pulse shaper restores the pcm pulse form and shifts the incoming "1" and "0" digits to their proper logic level of 0 and -4.5 volts, respectively. Pcm output from Q6 feeds through an inverter from pin 3 to pin 2 in Z12 and is applied to two branches. One branch feeds back through a second inverter in Z12 from pin 5 to pin 4 and then is applied directly to one-shot Z9. The second branch is applied to pin 9 of one-shot Z13. Complement pcm trains are now formed at the inputs of one-shots Z9 and Z13. Any negative going edge of a pulse appearing in one or the other complement pcm trains trigger Z9 or Z13 to generate a positive going output pulse. The outputs of Z9 and Z13 are applied to the set and complement-trigger inputs of the first register Z10.
- (2) *Squelch.* During normal operation a +10 volt dc level is applied from terminal 25 of jack J8 through voltage dividing resistor R42 to the base of Q9. This saturates Q9, maintaining its collector at -4.5 volts. The -4.5volt potential at the collector of Q9, connected to the set (S-pin 2) and clear (C-pin 8) gates of Z10, maintains these gates enabled, allowing the decoder pcm to pass through Z10 to the remaining serial shift register flip-flops. If the receive section of the TD-352/U or TD-353/U

associated with the 1A14A/2A14A drops out of frame, the +10 volts is removed and a zero potential squelch signal is applied to terminal 10 of J8, turning off transistor Q9. This places the collector of Q9 at ground and disables the set and clear gates in Z10, preventing Z10 from being triggered. Thus any random pulses appearing on the pcm decoder line are prevented from being applied to the shift register, preventing objectionable noise from entering the audio circuits.

- (3) *Decoder clock.* A 2,304 kc (576 kc) train of sharp negative going pulses (see *decoder clock* waveform fig. 6-41) (fig. 6-36) varying nominally between -4.5 and 0 volts feeds into the panel via terminal 26 of jack J8 to pulse shaper Q1, Q2. The pulse shaper restores the clock pulse form and dc level and applies the output to one-shot Z1. Z1 is triggered on the leading edge of the negative pulse, generating a positive pulse output which is applied to pin 9 of Z2. Variable resistor R5 sets the output pulse to the required width, insuring that one-shot Z2 will be triggered at the proper time. One-shot Z2 is triggered by the trailing edge of the positive pulse appearing at pin 9, generating a positive pulse which feeds through complement buffer Q3, Q4, to the trigger input of flip-flops Z3 through Z7.
- (4) *Serial read-in.* Flip-flops Z2 through Z7, and Z10 comprise a conventional serial shift register. The pcm data is serially read through flip-flop Z10 into the remaining five flip-flops as follows: After the first pcm digit appears at the output of flip-flop Z10 the trailing edge of the first clock pulse appears at the trigger input (T) of the shift registers, transferring the state of Z10 to the second flip-flop, Z3. The second clock pulse occurs 0.43 usec (1.74 μ sec) after the first, transferring the state of flip-flop Z3 to flip-flop Z4, and that of flip-flop Z10 to flip-flop Z3. In like manner the remainder of the pcm word is serially read into the shift register with the third, fourth, and fifth shift clock pulses, such that after the fifth clock pulse, a 6-digit pcm word has been stored in the shift register with the most significant digit in flip-flop Z7 and the least significant digit in flip-flop Z10.

c. *Parallel Shift Registers.*

- (1) *Parallel shift pulse.* A 384-kc (96 kc) full width pulse train (see *384 kc sw* waveform fig. 6-41) ($\overline{\text{RFF5}}$ waveform fig. 6-36), varying nominally between -4.5 and 0 volts, feeds into the panel via terminal 22 of jack J8 to pulse shaper Q10, Q11. The pulse shaper restores the form and dc level of the signal and applies the output to switch S1 and one-shot Z26. With switch S1 operated to HT the output of pulse shaper Q10, Q11 is applied to one-shot Z26. One-shot Z26 is triggered on the negative going pulse transitions, generating a positive going pulse output which feeds through switch S1 to one-shot Z16. Variable resistor R106 adjusts the output pulse width of Z26 to insure correct delay of the high-traffic parallel shift pulse at jack J7 with respect to the input signal at terminal 22 of jack J8. With switch S1 operated to MT the output of pulse shaper Q10, Q11 is fed through switch S1 to one-shot Z16. One-shot Z16 is triggered by the negative trailing edge of its input pulse, generating a positive going pulse which feeds serially through an inverter in Z15 (in, pin 7; out, pin 8) and through single-input NAND gate Z28, thus forming the parallel shift pulse (see *decoder parallel shift* waveform fig. 6-41) (fig. 6 36).
- (2) *Parallel shift.* Just before the sixth serial shift pulse occurs on the decoder clock line, the trailing edge of a 384-kc positive pulse from NAND gate Z28 is applied to parallel shift register flip-flops Z22 through Z25 and from Z27 to parallel shift register flip-flop Z21. This transfers the pcm digits in the serial shift register to the parallel shift register with the most significant digit in flip-flop Z25 and the least significant in flip-flop Z21. The pcm digits are stored for 2.6 usec (10.4 usec) while the data is read into a summing circuit. During this period, another pcm word is read into the serial shift register flip-flops.
- (8) *Elimination of address digits* (fig. 2-32.1). If the 2-or 4-kc address digits were permitted to remain in the pcm signal, they would cause an annoying hum in the audio output. This condition is prevented by removing the address digit in the least significant digit of the last channel in each frame before it

C2, TM 11-5805-367-35/3

enters parallel shift register flip-flop Z21. The logic "1" digits of the address signal are removed so that the least significant digit position in the last channel in each frame always contains a logic "0." This is accomplished as follows: An 8-kc train of negative going pulses (see *address inhibit 2* waveform fig. 6-41. (fig. 6-36) varying nominally between -4.5 and 0 volts feeds into the panel via terminal 7 of jack J8 to pulse shaper Q16, Q17. The pulse shaper restores the form and dc level of the signal, feeds it through buffer transistor Q18, from where the signal is applied to two branches. One branch inverts the signal through assembly Z15 (in, pin 5; out, pin 4) and applies the resulting positive going pulse output to pin 3 of dual NAND gate Z17 (waveform 2); the second branch is applied to pin 8 of dual NAND gate Z17. The trigger (T) input (waveform 7) to parallel shift register flip-flop Z21 is generated by gating the parallel shift pulse (waveform 3) with *address inhibit-2* signal (waveform 1) in dual NAND gate Z17, and inverting the resulting signal (waveform 5) in dual NAND gate Z27. The direct clear (CD) input (waveform 4) to parallel shift register flip-flop Z21 is generated by gating the parallel shift pulse (waveform 3) with *address inhibit-2* signal (waveform 2) in dual NAND gate Z17, and buffering the resulting signal in buffer transistor Q12. During all channels except the last, the trigger (T) input to flip-flop Z21 from pin 2 of NAND gate Z27 is identical to the parallel shift pulse signal, allowing flip flop Z21 to operate as a standard parallel shift register. The direct clear (CD) input remains at the "1" level producing no affect on flip-flop Z21. During the last channel, the parallel shift pulse to the trigger (T) input of flip-flop Z21 is inhibited in NAND gate Z17 preventing reading of the address digit from flip-flop Z10 to flip flop Z21. At the same time a negative going pulse to the direct clear (CD) input resets flip flop Z21, clearing it of any previous data and causing its associated voltage clamp transistor Q21 to always produce a logic "0" output to the resistive ladder network during the address digit.

(4) *Digital-to-analog conversion circuit.*

- (a) The pcm digits, once read into the parallel shift register flip-flops Z21 through Z25, are converted to their equivalent pam level (analog signal) in this circuit as follows: The "1" and "0" outputs of flip-flops Z21 through Z24 are connected to voltage clamp transistors Q21 through Q24, respectively. The "1" and "0" outputs of flip-flop Z25 are connected to voltage clamp transistors Q26 and Q25, respectively. The voltage clamp transistors are each connected to a different step on resistive ladder network R79, R80, R84, R85, R89, R90, R94, R95, R99, R100, and R104. When a flip-flop is set during operation, the associated voltage clamp produces a precision -5.2-volt reference to its ladder network step; when a flip-flop is cleared, the associated voltage clamp produces ground potential. An exception to this is flip-flop Z25, connected to drive voltage clamp transistors Q25 and Q26 so that they are always in the opposite condition. Thus when flip-flop Z25 is set, voltage clamp transistors Q26 and Q25 produce a precision -5.2-volt reference and ground potential respectively to their ladder network steps, and a ground potential and -5.2-volt reference respectively when flip-flop Z25 is cleared.
 - (b) The resistive ladder network binary-weights the voltage clamp inputs to produce an analog voltage output as follows. When provided with a -5.2-volt input from the associated voltage clamp, each step on the ladder adds a voltage to the ladder output that decreases in binary fashion from the most significant ladder step at the output of clamp Q26 to the least significant ladder step at the output of Q21, so that the ratios between these voltages are 32:16:8:4:2:1. When a clamp is providing ground potential to a ladder step, the step adds no voltage to the ladder output. The ladder sums its binary weighted inputs, forming the analog pam sample output at terminal 1 of jack J8.
- (5) *Level 15 and 48 matching circuit.* This circuit functions to match the decoder pam levels generated for pulse codes 15 and 48 to the coder quantizing steps associated with these codes. Matching is accomplished by detecting receipt of codes 15 and 48 in the serial shift register and adding one-half pam level to the decoder pam in the ladder network when the code is 48, and subtracting one-half pam level when the code is 15.

The circuit operation follows: The "1" and "0" outputs of serial shift register flip-flops Z3 through Z7, and Z10 are connected to NAND gates Z11 and Z14 as indicated in the table below.

NAND gates inputs	Serial shift register flip-flop output terminals					
	Z7	Z6	Z5	Z4	Z3	Z10
Z11	1	1	0	0	0	0
Z14	0	0	1	1	1	1

Flip-flops Z19 and Z20, connected as storage elements in the parallel shift register, are each driven by a direct and inverted output from NAND gates Z11 and Z14 respectively, and are triggered by the regenerated parallel shift pulse from pin 10 of Z27 (waveform 6, fig. 2-32.1). Flip-flops Z19 and Z20, with their respective voltage clamp transistors Q19 and Q20, are connected to the resistive ladder network. During receipt of any pulse code except 15 and 48, and when storing the last bit of a word into the top shift register, the serial shift register outputs maintain a logic "1" output from NAND gates Z11 and Z14, and a logic 0 from their associated inverters. These outputs are applied to flip-flop Z19 and Z20 as shown in condition 1 of the table below.

Conditions	Pulse code in serial shift registers	Parallel shift register inputs			
		Z19		Z20	
		S	C	S	C
1	Any pulse code except 15 and 48.	0	1	1	0
2	Pulse Code 15	1	0	1	0
3	Pulse Code 48	0	1	0	1

Under condition 1 when a parallel shift pulse occurs, flip-flop Z19 is cleared and Z20 is set, driving voltage clamp transistor Q19 to ground and Q20 to -5.2 volts. Flip-flops Z19 and Z20 thus reference the ladder output, and provide a means of subtracting one-half pam level from the ladder during receipt of pulse code 15 and adding one-half pam level to the ladder during receipt of pulse code 48. This addition and subtraction process takes place as follows: During receipt of pulse code 15, the serial shift register produces all logic "1" inputs to NAND gate Z11 at the time that the last bit of a word is being stored in the top shift register, producing a logic 0 output from Z11, and all logic 0 inputs to NAND gate Z14, keeping the same logic "1" output. These outputs and their inverted replica are applied to flip-flops Z19 and Z20 as shown in condition 2 of the preceding table. Under this condition, when a parallel shift pulse occurs the output of flip-flop Z19 goes to a logic 0 at ladder resistor R67, consequently subtracting the required one-half pam level from the ladder output. During receipt of pulse code 48, the serial shift register produces all logic "1" inputs to NAND gate Z14 at the time that the last bit of a word is being stored in the top shift register, producing a logic 0 output from Z14, and all logic 0 inputs to NAND gate Z11, keeping the same logic "1" output. These outputs and their inverted replica are applied to flip-flops Z19 and Z20 as shown in condition 3 of the preceding table. Under this condition, when a parallel shift pulse occurs, the output of flip-flop Z20 goes to a logic "1" at ladder resistor R73, consequently adding the required one-half pam level to the ladder output.

C2, TM 11-5805-367-35/3

- (6) *Development of A, \bar{A} , B, \bar{B} .* The A, \bar{A} , B, and \bar{B} signals are generated in this panel for use in the companding circuits in panel 1A15 or 2A15.
- (a) The most significant digit of the parallel shift register, taken from the "1" output of flip-flop Z25, is inverted through inverter assembly Z12 and applied to terminal 3 of jack J8 where it is designated \bar{A} . The second most significant digit of the parallel shift register, taken from the "0" output of flip-flop Z25, is inverted through inverter assembly Z12 and applied to terminal 4 of jack J8 where it is designated A.
 - (b) The "1" and "0" outputs from the second most significant digit of flip-flop Z6 in the serial shift register are applied to the S and C inputs respectively of flip-flop Z8. flip flop Z8, triggered by the parallel shift pulse, applies its "1" and "0" output to terminals 5 and 2 respectively of jack J8, where they are designated \bar{B} and B. respectively.
- (7) *Development of H. T. modem timing.* For high-traffic applications only, the negative going edge of the 384 kc parallel shift pulse signal from pin 3 of NAND gate Z28 is used to trigger pulse-shaper Z18, generating a train of sharp, positive going pulses which is fed through buffer transistor Q15 to terminal 21 of jack J10, where it is designated *H.T. Modem Timing*.

When transistor Q5 conducts, the *decoder pam* signal is applied to the base of gate transistor Q6. Since the base of transistor Q6 is now more negative than the +4.5-volt potential placed on the base of transistor Q11 transistor Q6 conducts and applies the attenuated pam signal to the output circuit (*b* above).

- (3) Assume that a signal with a level of 16 is presented to the gating circuits. The first two most significant digits are 0 and 1. Signal *B* is a logic 1, and is positive going Signal *A* is a logic 0; however, its complement signal \bar{A} is positive-going. Signal *B* at the base of gate transistor Q2 and signal \bar{A} at the base of gate transistor Q8 cause the two transistors to conduct and produce the same results as described in (2) above for level 47.
- (4) Now assume a signal above level 47 or below level 16. The first two most significant digits for these levels are 1,1 or 0,0, respectively. In the case of a signal above level 47, signals *A* and *B* are positive-going; however, signals \bar{A} and \bar{B} are zero. Since only one of the inputs to transistors Q1 and Q7 is positive-going, these transistors do not conduct. The same is true for the inputs to transistors Q2 and Q8. As a result, both gate circuits are cut off and a +10 volt potential is applied to transistors Q3 and Q4, cutting off both. This causes transistor Q4 to conduct, placing a +4.5volt potential at the base of transistor Q6 and the emitter of Q5, cutting off both transistors. This also causes transistor Q10 to conduct and to apply the pam signal to the base of gate transistor Q11. Since the voltage on the base of transistor Q11 is more negative than that on the base of transistor Q6, transistor Q11 will conduct and apply the unattenuated pam signal through buffer transistor Q12 to terminal 23 of jack J9 where it is designated as the receive pam signal.

d. Squelch Circuit. The *squelch* signal is applied to terminal 24 of Jack J9 and consists of a + 10-volt signal during normal operation and a 0-volt signal when the unit is out of frame. When the + 10-volt signal is applied to terminal 24, diodes CR1 and CR5 conduct, beak-biasing diodes CR2 and CR6 so that transistors Q3 and Q4 operate normally. When the *squelch* signal goes to 0 volt, diodes CR1 and CR5 are back-biased and diodes CR2 and CR6 conduct. This keeps the bases of transistors Q3 and Q9 at a 0-volt level. Transistors Q3 and Q9 therefore conduct and the circuit operates the same as if one of the two gating circuits (consisting of transistors Q1 and Q7, and Q2 and Q8) were conducting (*c* above). When this occurs the signal is steered through the attenuated path. Therefore, when the squelch signal is 0 volt, all levels of the pam signal are always applied through the attenuated path, reducing the chance of unwanted noise reaching the output circuits where the unit is out of frame.

e. Pam Center Adjust Control. The potential at the bases of transistors Q5 and Q10 is controlled by CTR potentiometer R16. This control is adjusted so that the center half of the pam signal falls within its allotted range. If the potentiometer is not properly adjusted, level 16 will overlap level 15, or level 47 will overlap level 48. Since this adjustment is critical, the transistor base voltage supply (+18 volts dc) is partially regulated to provide more stability. The +18-volt supply is obtained from a network consisting of resistor R42; capacitor C21; and breakdown diodes CR17, CR18, and CR19. The input to the network is +25 volts, which enters the panel at terminal 11 of jack dc The +25-volt supply is applied across a voltage divider consisting of resistor R42 and the three breakdown diodes. The output of the divider is controlled by the breakdown voltage of the three breakdown diodes, which is 18 volts.

f. Development of Address Inhibit 1 and A Signals. The *address digit gate* signal is applied to the panel through terminal 5 of jack J9 and consists of a train of positive-going square pulses with a duration of 2.6 usec and a frequency of 8 kc. The signal is applied through resistor R26 to delay line DL1 where it is delayed by 0.3 usec. From the delay line, the signal is applied through buffer transistor Q13 to slicer transistor Q14. Slicer transistors Q14 and Q16 operate similar to a differential amplifier. The base of transistor Q16 is biased at a ground potential. The slicer circuit produces a push-pull output. One output consists of a train of positive-going square pulses and in applied from the collector of transistor Q14

to terminal 7 of jack J9 and designated *address inhibit 1*. The other output consists of a train of negative-going square pulses and is applied from the collector of transistor Q15 to terminal 6 of jack J9 and designated *address inhibit 2*. These pulses are used in panel 1A14/2A14 to inhibit the address pulses, preventing them from entering the last channel.

g. Development of Main pam Signal. The *sampled pcm* signal, which is a pcm signal that has been sampled and restored, is applied to the panel through terminal 3 of jack J9. From terminal 3, the signal is applied through delay line DL2, where it is delayed 0.4 usec, to buffer transistor Q20. From transistor Q20 the signal is applied to terminal 1 of jack J9 where it is designated as the *main pcm* signal.

h. Development of Pcm from Aux Monitor Signal. The *pam from aux* signal is applied from terminal 8 of jack J9 to buffer transistor Q19. The output of transistor Q19 is dc shifted by a network consisting of capacitor C22 and diode CR20. The dc level produced by the network is applied through resistor R45 to terminal 9 of jack J9 where it is designated *pcm from aux monitor*. This signal is applied to the front panel TEST ALIGN meter switching circuit for measurement purposes.

i. Development of 884 Kc Modem Gate Timing. The 384-kc modem gate timing signal is developed in a flip-flop consisting of transistors Q16 and Q17. One input to the flip-flop is the *modem timing signal*, which consists of a train of positive-going trigger pulses with a 384-kc rate. This signal enters the panel at terminal 17 of jack J9 and is applied to transistor Q16. The other input to the flip-flop is the *matrix FF* signal, which consists of pulses gated at a 384-kc rate. This signal enters the panel at terminal 13 of jack J9 and is applied through buffer transistor Q18 to transistor Q17. The modem timing signal sets the flip-flop, and the *matrix FF* signal resets it. The output of the flip-flop is taken from the collector of transistor Q17 and applied to terminal 20 of jack dc where it is designated *384-kc modem gate timing*. This signal consists of a wavetrain of square pulses with a 384-kc rate.

2-53. Decoder No. 2, Panel 2A15

(fig. 6-80)

a. General. Decoder No. 2 panel 2A15 is used in conjunction with panel 1A14/2A14 in Multiplexer TD352/U. In panel 2A15, the outer portions of the pam signal are expanded to compensate for any compression at the point of signal origin. This function is accomplished under the control of signals developed in panel 1A14/2A14. Decoder No. 2 panel also develops the *address inhibit 1 and 2* signals, the *main pcm signal*, the *pcm from aux monitor* signal, and the *rcvr aux address* or *rcvr frame pulse* signal. The interrelationships of the input and output signals are shown in figure 6-36.

b. Decoder Pam Signal. The *decoder pam* signal enters panel 2A15 at terminal 25 of jack J9 and is applied to the bases of gate transistors Q7 and Q9. Depending on the collector outputs of gate transistors Q6 and Q8 (*c* below), the signal passes through either transistor Q7 or transistor Q9. The signal path through transistor Q9 is not attenuated. When transistor Q7 is conducting, however, the pam signal is first attenuated by a ratio of 20 to 1 in the network consisting of resistors R10 and R11. The pam signal is then applied from either transistor Q7 to gate transistor Q10 or from transistor Q9 to gate transistor Q11. Transistors Q10 and Q11 form an OR gate. When there is an attenuated pam signal at the base of transistor Q10, it conducts and the signal is applied through buffer transistor Q12 to terminal 23 of jack J9 where it is designated *receive pam*. When there is an unattenuated pam signal at the base of transistor Q11, it conducts and the signal is similarly applied through transistor Q12 to terminal 23 of jack J9.

c. Gate Circuits. When the *pam decoder* signal is applied to panel 2A15, a decision is made in the gating circuits as to whether or not the signal should be attenuated. A *pam decoder* signal with a level of 16 to 47 is applied to the attenuator circuit; levels above 47 and below 16 are applied through the unattenuated circuit. In the attenuated circuit the signal passes through a 20 to 1 attenuator where the signals are compressed to a level proportionate to that which existed before companding.

- (1) Application of the *pam decoder* signal to the attenuated or unattenuated circuit is controlled by transistor gates Q1, Q3 and Q2, Q4. Four signals developed on panel 1A14/2A14 are applied to transistors Q1 through Q4 on panel 2A15. These signals are designated as A, \bar{A} , B, and \bar{B} and are

applied to terminals 28, 27, 28, and 31, respectively, of jack J8. Signal A represents the most significant digit (msd) of the signal being decoded: signal \bar{A} is its complement. Signal B represents the next most significant digit of the signal being decoded, and \bar{B} is its complement. Signals A , \bar{A} , B , and \bar{B} are applied to the bases of transistors Q1, Q4, Q2, and Q3, respectively. The first two digits of all levels from 16 to 47 are either 0, 1 or 1, 0, this property is the key for identifying the levels to be attenuated. When the level of the signal being decoded has either one of the two combinations of digits (that is, signals A and B in opposite states), the gate circuit produces an output that steers the decoded signal through the attenuator.

- (2) Assume that a signal with a level of 47 is presented to the gates. The two most significant digits for level 47 are 1 and 0. Signal A (msd) is a logic 1, a positive going signal. Signal B (the next (msd) is a logic 0 however, its complement signal \bar{B} is a positive-going signal. Since positive-going signals A and B arrive simultaneously at the bases of transistors Q1 and Q3, both transistors conduct and set the collector of transistor Q1 at a -4.5-volt potential. This -4.5-volt potential is applied to the base of inverter transistor Q5 and to the base of gate transistor Q8. Transistor Q8 conducts and applies a +4.5-volt potential to the base of gate transistor Q11 and to the emitter of gate transistor Q5 cutting off both transistors. This prevents passage of the unattenuated signal to the output circuit. Transistor Q5 also conducts, its collector goes to +4.5 volts, and a more positive bias is applied to the base of transistor Q6. This cuts off transistor Q4 and allows transistor Q7 to conduct. When transistor Q7 conducts, the decoder pam signal is applied to the base of transistor Q10. Since the base of transistor Q10 is now more negative than the +4.5-volt potential placed on the base of transistor Q11, Q10 will conduct and apply the attenuated pam signal to the output circuit (*b* above).
- (3) Assume that a signal with a level of 16 is presented to the gating circuits. The first two most significant digits are 0 and 1. Signal B is a logic 1 and is positive-going. Signal A is a logic 0 however, its complement signal \bar{A} is positive-going. Signal B at the base of gate transistor Q2 and signal A at the base of gate transistor Q4 cause the two transistors to conduct and produce the same results as described in (2) above for level 47.
- (4) Now assume a signal above level 47 or below level 16. The first two most significant digits for these levels are 1,1 or 0,0, respectively. In the case of a signal above level 47, signals A and B are positive-going; however, signals \bar{A} and \bar{B} are zero. Since only one of the inputs to transistors Q1 and Q3 is positive-going, these transistors do not conduct. The same is true for the inputs to transistors Q2 and Q4. As a result, both gate circuits are cut off and a + 10-volt potential is applied to transistors Q5 and Q8, cutting off both. This causes transistor Q6 to conduct and place a +4.5-volt potential at the base of transistor Q10 and the emitter of transistor Q7, cutting both transistors off. This also causes transistor Q9 to conduct and apply the pam signal to the base of gate transistor Q11. Since the voltage on the base of transistor Q11 is more negative than that on the base of transistor Q10, transistor Q11 will conduct and apply the unattenuated pam signal through buffer transistor Q12 to terminal 23 of jack J9, where it is designated as the *receive pam* signal.

d. Squelch Circuit. The squelch signal is applied to terminal 24 of jack J9 and consists of a +10-volt signal during normal operation and a 0-volt signal when the unit is out of frame. When the +10-volt signal is applied to terminal 24, diodes CR1 and CR4 conduct, back-biasing diodes CR2 and CR5 so that transistors Q5 and Q8 operate normally. When the *squelch* signal goes to 0 volt, diodes CR1 and CR4 are back-biased

and diodes CR2 and CR5 conduct. This keeps the bases of transistors Q5 and Q8 at a 0-volt level. Transistors Q5 and Q8 therefore conduct and the circuit operates the same as if one of the two gating circuits (consisting of transistors Q1 and Q3, and Q2 and Q4) were conducting (c above). When this occurs, the signal is steered through the attenuated path. Therefore, when the *sqelch* signal is 0 volt, all levels of the pam signal are always applied through the attenuated path, reducing the chance of unwanted noise of reaching the output circuits when the unit is out of frame.

e. *Pam Center Adjust Control.* The potential at the bases of transistors Q7 and Q9 is controlled by the CTR potentiometer R19. This control is adjusted so the center half of the pam signal falls within its allotted range. If the potentiometer is not properly adjusted, level 16 will overlap level 15, or level 47 will overlap level 48. Since this adjustment is critical, the transistor base voltage supply (+18 volts dc is partially regulated to provide more stability. The +18-volt supply is obtained from a network consisting of resistor R31; capacitor C11; and breakdown diodes CR1, CR2, and CR3. The input to the network is +25 volts, which enters the panel at terminal 19 of jack J9. The +25-volt supply is applied across a voltage divider consisting of resistor R31 and the three breakdown diodes. The output of the divider is controlled by the breakdown voltage of the three breakdown diodes, which is 18 volts.

f. *Development of Address Inhibit A and A Signals.* The address digit gate signal is applied to the panel through terminal 7 of jack J9 and consists of a train of positive-going square pulses with a duration of 2.6 usec and a frequency of 8 kc. The signal is applied through resistor R26 to delay line DL1, where it is delayed by 0.3 usec. From the delay line, the signal is applied through buffer transistor Q13 to slicer transistor Q14. Slicer transistors Q14 and Q15 operate similar to a differential amplifier. The base of transistor Q15 is biased at a ground potential. The slicer circuit produces a push-pull output. One output consists of a train of positive-going square pulses and is applied from the collector of transistor Q14 to terminal 8 of jack J9 and designated *address inhibit 2*. The other output consists of a train of negative-going square pulses and is applied from the collector of transistor Q15 to terminal 1 of jack J9 and designated *address inhibit 1*. These pulses are used in panel 1A14/2A14 to inhibit the address pulses, preventing them from entering the last channel.

g. *Development of Main pcm Signal.* The *sampled pcm signal*, which is a pcm signal that has been sampled and restored, is applied to the panel through terminal 3 of jack J9. From terminal 3, the signal is applied through delay line DL2, where it is delayed 0.4 usec. to buffer transistor Q21. From transistor Q21 the signal is applied to terminal 6 of jack A where it is designated as the main pcm signal.

h. *Development of pcm From Aux Monitor Signal.* The *pcm from aux* signal is applied from terminal A of jack J9 to buffer transistor Q20. The output of transistor Q20 is dc shifted by a network consisting of capacitor C21 and diode CR11. The dc level produced by the network is applied through resistor R45 to terminal 10 of jack J9 where it is designated *pcm from aux monitor*. This signal is applied to the front panel TEST ALIGN meter switching circuit for measurement purposes.

i. *Development of Rcvr Aux Address (or Rcvr Frame Pulse) Signal.* The receive address signal appearing at terminal 17 of jack A is buffered by transistor Q18 and applied to terminal 15 of jack J19 as *the rcvr aux address or rcvr frame pulse* signal.

2-54. Monitoring and Alarm, Panel 1A16/2A16

(fig. 6-82)

a. *General.* Monitoring and alarm panel 1A15 2A16 provides various circuits for monitoring and troubleshooting Multiplexers TD-352/U and TD353/U. Included are a pcm in monitor circuit, a 1,100-cps test tone used for testing and aligning panels 1A2/2A2, associated microphone and earphone amplifier circuits, a squelch circuit, and the frame alarm circuit.

b. *Development of Traffic pcm in Mon Signal.* The high or medium traffic pcm in mon signal is developed from the pcm in signal applied to terminal 28 of jack J7. From terminal 28, the *pcm in* signal is applied through buffer transistor Q1 to a level restorer circuit consisting of capacitor C1 and diode CRT. As long as a train of pulses is applied to the level restorer, it will produce a dc level which is applied through resistor R3 to terminal 29 and designated *H traffic pcm in mon*. This output is used with Multiplexer TD-353/U

only. For the TD-352/U, the output of the level restorer is applied through resistor R4 to terminal 30 of jack J7 and designated *med traffic pcm in mon*. These outputs are displayed on the TEST ALIGN meter when the METER SELECT switch is at PCM IN.

c. *Development of Test Tone Signal.* The *test tone* signal is a 1,100-cps audio signal that can be applied to double modem panels 1A2/2A2 for test purposes. The 1,100-cps *test tone* signal is generated by a resistance-capacitance phase-shift oscillator consisting of transistors Q2, Q3, and Q4. Oscillation is sustained by a feedback circuit consisting of three resistance-capacitance networks which shift the phase by 180°. The feedback signal is coupled from the emitter of transistor Q3 through the phase shifting network and transistor Q4 to the base of transistor Q2. The bias for the base of transistor Q2 is provided by a voltage divider consisting of resistors R5 and R6. When power is first applied, the surge of current through resistors R5 and R6 starts the circuit oscillating. Transistor Q3 acts as a buffer to isolate transistor Q2 from the output circuit. The output circuit from the emitter of transistor Q3 contains a lowpass filter, consisting of inductors L1 and L2 and capacitor C5, which removes any harmonics that might be in the output of transistor Q3. The output is applied to terminal 31 of jack J7 and is designated as the *test tone* signal. From terminal 31, the signal is applied to OSC ADJUST potentiometer R1 located on the service facility panel of the multiplexer. The signal is taken from the arm of the potentiometer and applied back to panel 1A16/2A16 as the *test tone adjust* signal at terminal 25 of jack J7. This adjusted test tone signal is applied through buffer transistor Q5 to the primary winding of transformer T1 and to a monitoring circuit. The secondary winding of transformer T1 is applied to terminals 14 and 19 of jack J7 and designated *test tone out No. 1* and *test tone out No. 2*, respectively. The monitoring circuit consists of capacitors C11 and C12, diodes CR2 and CR3, and resistor R18. The monitoring signal is applied from resistor R18 to terminal 20 and designated *test tone monitoring*.

d. *Development of Alarm and Relay Signals.* When the unit drops out of frame because of faulty circuits or loss of the pcm signal, this panel develops signals that control visual (FRAME indicator) and audio (buzzer) alarm circuits. A *squelch* signal is generated simultaneously to prevent objectionable noise from reaching the output circuits. These control signals are developed from the *alarm timing* and *alarm control* signals applied to terminals 9 and 8, respectively, of jack J7. The circuit basically consists of a three-input OR gate difference amplifier and a flip-flop circuit. The difference amplifier consists of transistors Q11, Q12, and Q13. The input to the base of transistor Q13 is a constant signal of approximately -2.0 volts. This signal is supplied by a voltage divider consisting of resistors R33 and R34, and allows transistor Q13 to conduct. The *alarm control* signal applies a -4.5-volt signal to the base of transistor Q12. This keeps transistor Q12 cut off when the *alarm control* signal is present. The *alarm timing* signal is applied through a peak detector, consisting of capacitor C26 and diodes CR8 and CR9, to the base of Q11. This keeps transistor Q11 cut off when the alarm timing signal is present. During normal operation, both *alarm control* and *alarm timing* signals are always present and only transistor Q13 conducts. Transistor Q13 therefore applies a negative potential to flip-flop transistor Q10 which, in turn, conducts and produces a +10-volt signal at its collector. This signal is applied to terminal 10 as the alarm 0 signal and to terminal 11 as the *squelch* signal. Since transistor Q10 is conducting, flip-flop transistor Q9 is cut off and therefore applies a 0-volt signal, through driver transistor Q6, to terminal 17 as the *converter lockout relay* signal and, through driver transistors Q7 and Q8, to terminal 18 as the *alarm relay* signal. The alarm on signal at terminal 16 is not used. When the *alarm control* and *alarm timing* signals go to 0 volt, indicating that the unit is out of frame, transistors Q12 and Q11 conduct. Transistor Q13 is therefore cut off and the flip-flop reverses state so that a 0-volt potential is now applied to terminals 10 and 11 and a +10-volt potential is applied to terminals 17 and 18.

e. *Development of Detected Audio Measure Signal.* Selection of the particular audio output channel to be monitored is determined by the positions of the SERV SEL and CHAN 1-12 selector switches on the TD-352/U, and by the SERV SEL, EVEN CHAN, and ODD CHAN selector switches on the TD-353/U. These switches route the output level measuring signals from the demodulator circuits on panel 1A2/2A2, through

the 2 WIRE/4 WIRE control switch, to terminal 26 on jack J7 of panel 1A16/2A16. From this point, the signal, termed *audio measure*, is applied to the primary winding of transformer T1 through buffer transistor Q17. The signal across the secondary winding of transformer T1 is then applied to a peak detector consisting of diodes CR10 and CR11 and capacitor C35. The positive charge stored by capacitor C35 is applied to terminal 15 of jack J7, where the dc level is designated as the *detected audio measure* signal. This signal is displayed on the front panel TEST ALIGN meter as required for monitoring, adjustment, and alignment purposes.

f. *Talk-Monitor Circuits.* The monitoring and alarm panel also provides earphone and microphone amplifier circuits. When a headset microphone combination such as the H-91A/U is connected to the front panel TALK MONITOR connector, the output of the microphone is connected to terminal 4 of jack J7. From this point, the signal, termed *mike*, is applied to transistors Q14 and Q15 where it is amplified and then applied through buffer transistor Q16 to transformer T2. Transformer T2 changes the unbalanced mike signal to the balanced signal required by the modulator circuits of panels 1A2/2A2. The output of the transformer is applied through resistors R46 and R47 to terminals 7 and 6, where the signals are designated *mike out No. 1* and *mike out No. 2*, respectively. Selection of the particular channel to be modulated by the mike output signal is determined by the positions of the SERV SEL and CHAN 1-12 selector switches on the TD352/U, and by the SERV SEL, EVEN CHAN, ODD CHAN, and MEASURE/PHONEODD/PHONE-EVEN selector switches on the TD-353/U. In the receive traffic direction, a portion of any demodulated audio output I channel from panels 1A2/2A2 is applied to I terminals 3 and 2 of jack J7 through the same selector switches. The signals appearing at terminals 3 and 2 are designated *earphone ampl in No. 1* and *earphone ampl in No. 2*, respectively, and are connected to matching transformer T4, which converts the balanced input signal to an unbalanced signal. The signal is then coupled to amplifier transistor Q18 through capacitor C36, and the output of Q18 is applied through capacitor C39 to terminal 1 of jack J7 where it is designated *earphone ampl out*. From terminal 1, the signal is applied to the front panel TALK MONITOR connector.

2-55. Transmit Fault Locator, Panel 1A17

(fig. 6-83)

a. *General.* There are five fault locator circuits for the transmit section of the TD-353/U. Four of the circuits (1A8 *mon A*, 1A9 *mon B*, 1A10 *mon C*, and 1A9 *mon D*) are contained on panel 1A17. The fifth circuit (1A7 *mon E*) is contained on receive fault locator panel 1A18 (para 2-57) but is operationally part of the transmit fault locator system.

b. *Development of 1A8 Mon A Signal.*

- (1) The fault locator circuit for panel 1A8 consists of four type 36 detector modules (para 2-29), each containing two identical peak detector circuits. Eight signal outputs from panel 1A8 are applied to the four detector modules, and the resulting dc outputs are combined in an AND gate. This produces one output, termed *1A8 mon A*, which is representative of the panel operation. This output is applied to the SERV SEL switch from which it can be switched to the TEST ALIGN meter circuit for monitoring purposes.
- (2) When all eight input signals are present, the level of the *1A8 mon A* signal is sufficiently high to cause the TEST ALIGN meter pointer to register in the green area of the meter dial. The loss of one or more input signals, however, results in a lower level *1A8 mon A* signal. The TEST ALIGN meter will indicate this faulty condition by registering out of the green area.
- (3) Of the eight input signals applied to the *1A8 mon A* circuit detectors, two signals (*FF2B xmtr* and *FF3B xmtr*) are fed directly to their associated detectors 1,000-ohm resistors. The P1, reshaped clock, sampling clock, and reset clock input signals are buffered before application to the detectors. The *timing out* and *sync out xmtr* signals are buffered and then amplified to a level which can be switched for detection. The following is a summary of the input signals, their input terminals, the associated buffer and amplifier stages (where applicable). And the pins to which the signals are applied.

Input signal	Appears at terminal	Buffered by transistor	Amplified by transistor	Applied to
<i>P1</i> -----	23	Q3 -----	-----	Pin 2, module Z2.
<i>Reshaped clock</i> ----	28	Q4 -----	-----	Pin 10, module Z2.
<i>FF3B xmtr</i> -----	24	-----	-----	Pin 2, module Z3.
<i>FF2B xmtr</i> -----	30	-----	-----	Pin 10 module Z3
<i>Sampling clock</i> ----	25	Q5 -----	-----	Pin 2, module Z4.
<i>Timing out</i> -----	20	Q6 -----	Q7 -----	Pin 10, module Z4.
<i>Sync out-xmr</i> -----	18	Q9 -----	Q10 -----	Pin 2, module Z5.
<i>Reset clock</i> -----	17	Q8 -----	-----	Pin 10 module Z5.

c. *Development of 1A9 Mon B Signal.* There are two fault locator circuits for panel A 1A9 mon B and 1A9 mon D (e below). The 1A9 mon B circuit has a single input, which is the modem timing signal appearing at terminal 7 of jack J21. This signal is first buffered and then applied through capacitor C19 to a peak detector network consisting of diodes CR12 and CR13, and capacitor C20. The dc output of the detector is applied through resistor R80 to terminal 8 of jack J21 where it is designated as the 1A9 mon B signal. This signal is also switched into the TEST ALIGN meter circuit through the SERV SEL switch. When the 1A9 mon B output signal is present (panel 1A9 good), it causes the meter pointer to register in- the green area; when this signal is absent, the meter registers out of the green area, which is the panel-bad indication.

d. *Development of 1A10 Mon C Signal.* The TFF9 signal from panel 1A10 is monitored both for its presence and correct frequency. The signal, appearing at terminal 27 of jack J21, has, a frequency of 8 kc and is first applied to a narrow bandpass filter consisting of capacitor C4 and inductor L1. The filter removes any frequencies other than 8 kc and passes the signal to a peak detector circuit consisting of diode CR5 and capacitor C5. The resulting dc level is applied through resistor R37 to terminal 16 of jack J21 where it is designated as the 1A10 mon C signal. This signal is also switched into the TEST ALIGN meter circuit through the SERV SEL switch as described for the foregoing fault locator output signals.

e. *Development of 1A9 Mon D Signal.* The 1A9 mon D signal is developed from the *address pulse, xmtr address timing, and aux address* signals from panel 1A9. The *address pulse*, appearing at terminal 2 of jack J21, is first buffered by transistor Q12 and then applied to flip-flop Z6 (module 09, para 2-15). Flip-flop Z. divides the frequency of the address pulse by 2 before application to pin 2 of detector module Z7. The xmtr address timing signal appears at terminal 11 of jack J21 and is applied directly to pin 10 of module Z7. The aux address signal appears at terminal 15 of jack J21 and is buffered by transistor Q8 and detected in module Z1. The two outputs of module Z7 and one output of module Z1 are combined and appear at terminal 29 of jack J21 as the IA, mon D signal. The level of this signal when all three signals are present is sufficient to cause a green TEST ALIGN meter reading as described for the other transmit fault locator circuits. When one signal is absent, the 1A9 mon D signal level decreases enough to cause the TEST ALIGN meter to read out of the green area.

2-56. Transmit Fault Locator, Panel 2A17
(fig. 6-85)

a. *General.* There are five fault locator circuit for the transmit section of the T-352/U. Three of these circuits (2A8 mon. A, 2A8 mon C, and 2A9 mon D) are contained on panel 2A17. The fourth and fifth circuits (2A10 mon. B and 2A7 mon. E) are contained on receive fault locator panel 2A18 (para 2-58), but they are operationally part of the transmit fault locator system.

b. *Development of 2A8 Mon A Signal.*

- (1) There are two fault locator circuits for panel 2A8: *2A8 mon A* and *2A8 mon C* (c below). The *2A8 mon A* circuit consists of three type 6-36) detector modules (para 2-29), each of which contains two identical peak detector circuits. Six signal outputs from panel 2A18 are applied to the three detector modules, and the resulting dc outputs are combined in an AND gate. This produces one output, representative of all six input signals, which is termed the *2A8 mon A* signal. This output is applied to the SERV SEL switch from which it can be switched to the TEST ALIGN meter circuit for monitoring purposes.
- (2) When all six input signals are present, the level of the *2A8 mon A* output signal is high enough to cause the TEST ALIGN meter pointer to register in the green area of the meter dial. The loss of one or more input signals causes a lower level output signal and- the TEST ALIGN meter indicates a faulty panel by registering out of the green area.
- (3) The inputs to the *2A8 mon A* fault locator circuit are the *T pulse clock*, *modem timing*, *TFF2*, *TFF2*, *TFF3*, and *TFF12* signals. These appear at terminals 27, 28, 21, 30, 22, and 23, respectively, of jack J21. The *T pulse dock* and *modem timing* signals are buffered by transistors Q1 and Q2 before application to pins 2 and 10, respectively, of detectors module Z1. the *TFF2* and *TFF2* signals are applied directly to pins 2 and 10, respectively, of detectors module Z3. The dc outputs of modules Z1, Z2, and Z3 are combined and appear at terminal 31 of jack J21 where they are designated as the *2A8 mon A* signal.

c. *Development of 2A8 Mon C Signal.* The second fault locator circuit for panel 2A8 is derived from three input signals: *parallel shift*, *shift 2*, and *decision pulses*. These signals appear at terminals 4, 3, and 5, respectively, of jack J21. Since the *parallel shift* and *shift A* signals are of insufficient duration to correctly charge capacitor C2 in detector module Z5, the signals are first used to trigger intermediate flip-flop stage Z4. When both signals are triggering flip-flop Z4, there will be an output signal of sufficient duration for detection in module Z5. If one of the inputs to module Z4 is removed because of a fault in panel 2A8, the input to pin 2 of module Z5 will be dc In this case, there will be no output from the detector circuit. The *decision pulses* signal is applied to the second detector circuit in module Z5, and the outputs of both detectors are combined to form the *2A8 mon C* signal which appears at terminal 6 of jack J21. This signal is applied to the TEST ALIGN meter circuit through the SERV SEL switching facility. When all three input signals are present, the level of the *2A8 mon C* signal is high enough to cause the TEST ALIGN meter to read in the green area. When one or more signals are absent, the output signal level decreases enough to cause the TEST ALIGN meter to read out of the green area.

d. *Development of 2A9 Mon D Signal.* The fault locator circuit for panel 2A9 is derived from six input signals, five generated on panel 2A9 and one (*8-kc aux*) generated on panel 2A5. Although the *8-kc aux* signal circuit is physically contained on panel 2A5, it is actuary part of panel 2~ transmit timing circuits. The six input signals are applied to detector modules Z6, Z7, and Z9. All signals are first buffered. The *timing out*, *sync out xmtr*, and *8-kc Aux signals* are also amplified to a level suitable for detection. The six outputs of modules Z6, Z7, and Z9 are combined into the *2A9 mon D* output which appears at terminal 29 of jack J1. This signal is applied to the TEST ALIGN meter circuit through the SERV SKI' switch as described for the other monitoring signals.

2-57. Receive Fault Locator, Panel 1A18

(fig. 6-87)

Receive fault locator panel 1A18 processes the receive signals of the TD-353/U for monitoring purposes the same as transmit fault locator panel 1A17 processes the transmit signals (para 2-55). The only difference is that in panel 1A1B, the *coder pam mon* signal applied to terminal 11 of jack J17 is applied to an amplifier transistor (Q11) before application to a buffer transistor. There are 17 inputs to the panel, and 8 monitoring signals are developed. The inputs, buffer and amplifier transistors, and detector modules used to develop the various signals are given below.

Input signal	Applied to panel at terminal	Detector module and pin number	Buffer transistor	Amplifier transistor	Output signal	Output terminal
<i>Timing A</i> -----	24	Z1, pin 2 -----	Q1 -----	-----	1A13 MON H ----	29
<i>Timing B</i> -----	28	Z1, pin 10-----	Q2 -----	-----		
<i>Decoder Clock</i> -----	25	Z2, pin 2 -----	Q3 -----	-----		
<i>384 KC S. W</i> -----	30	Z2, pin 10-----	-----	-----		
<i>Sync out rcvr</i> -----	20	Z3, pin 2 -----	Q4 -----	Q5 -----		
<i>FF2B</i> -----	21	Z3, pin 10-----	-----	-----	1A13 MON K ----	9
<i>Rcvr aux clock</i> -----	18	Z4, pin 2 -----	Q6 -----	Q7 -----		
<i>Address digit gate</i> -----	17	Z4, pin 10-----	Q8 -----	-----		
<i>Timing C</i> -----	12	Z6, pin 2 -----	Q9 -----	-----	1A7 MON E -----	10
<i>Matrix FF</i> -----	13	Z6, pin 10-----	Q10-----	-----		
<i>Coder pam mon</i> -----	11	-----	Q12-----	Q11-----	1A13 MON M-----	7
<i>Skip FF</i> -----	8	-----	-----	-----	1A10 MON J-----	16
<i>RFF9</i> -----	27	-----	Q13-----	-----	1A12 MON L-----	1
<i>Skip Pulse</i> -----	2	-----	Q14-----	-----	1A12 MON N ----	6
<i>Pcm to aux</i> -----	4	-----	Q15-----	-----		

In addition to the components called out in the chart, there are two flip-flop modules (Z5 and Z7) which are used to increase pulse duration to enable a peak detector to charge to a dc level.

2-58. Receive Fault Locator, Panel 2A18

(fig.6-89)

Receive fault locator panel 2A18 processes the receive signals of the TD-352/U for monitoring purposes the same as the transmit fault locator, panel 2A17, processes the transmit signals. Since the description of this panel is essentially the same as for panel 2A17, no detailed description is given. The detector, which monitors the RFF9 signal on this panel, is used in both the receive and transmit circuits and the *coder pam mon* signal, which is also monitored on this panel, is used in the transmit circuits only. There are 17 inputs to panel 2A18 which develop 7 monitoring signals. The inputs, buffer and amplifier transistors, and detector modules used to develop the various signals are given in the chart, below. In addition to the components called out in the chart there are two flip-flop modules (Z6 and Z7) which are used to increase pulse duration to enable a peak detector to charge to a dc level. The *coder pam mon* signal is also applied through amplifier transistor Q15 before application to its buffer transistor.

Input signal	Applied to panel at terminal	Detector module and pin number	Buffer transistor	Amplifier transistor	Output signal	Output terminal
<i>Timing A</i> -----	24	Z1, pin 2-----	Q1-----	-----	2A13 MON H-----	29
<i>Timing B</i> -----	28	Z1, pin 10-----	Q2-----	-----		
<i>Rcvr aux clock</i> -----	18	Z2, pin 2-----	Q3-----	Q4-----		
<i>Sync out rcvr</i> -----	20	Z2, pin 10-----	Q5-----	Q6-----		
<i>Decoder clock</i> -----	21	Z3, pin 2-----	-----	-----		
<i>Modem timing</i> -----	25	Z3, pin 10-----	Q7-----	-----		
<i>RFF2</i> -----	30	Z4, pin 2-----	-----	-----		
<i>Skip Pulse</i> -----	2	-----	Q11 ----	-----	2A12 MON L ----	9
<i>Timing C</i> -----	12	Z8, pin 2-----	Q12 ----	-----	2A13 MON K-----	10
<i>Address digit gate</i> -----	13	Z8, pin 10-----	Q13 ----	-----	2A10 MON B OR J	
<i>RFF9</i> -----	27	-----	Q14 ----	-----	2A7 MON E -----	7
<i>Coder pam mon</i> -----	11	-----	Q16 ----	Q15 -----	-----	16
<i>Alt pcm out</i> -----	6	Z9, pin 2-----	Q17 ----	-----	2A12 MON N-----	1
<i>Pcm to aux</i>	5	Z9, pin 10-----	Q18 ----	-----	-----	6

2-59. Unregulated Power Supply, Panel 1A19/2A19

(fig. 6-91)

a. General.

- (1) Unregulated power supply panel 1A19/ 2A19 accepts 115-volt 0 ape power and converts it to unregulated dc voltages and stepped-down ac voltages.. These voltages provide the power necessary to operate Multiplexers TD-353/U and T-352/U.
- (2) The chart below lists the loaded voltages provided by this power supply, the output terminals of jack J1 across which each voltage appears, and the use of each voltage.

Voltage	Positive terminals	Negative terminals	Used to drive
13.5 volts dc-----	9 and 22-----	8	+10-volt series voltage regulator.
7 volts dc -----	18 -----	17	-4.5-volt series voltage regulator.
7.5 volts dc -----	11 and 23 -----	10	+4.5-volt series voltage regulator.
34 volts dc -----	7 and 25-----	6	+25-volt series voltage regulator.
16 volts dc -----	15 -----	13	-12-volt series voltage regulator.
28 volts, 60 cps-----	1,2, ^a and 19-----	3	Miscellaneous circuits.
39 volts, 60 cps-----	14 -----	16	-20-volt shunt-regulated supply and +10-volt shunt-regulated supply.

^a Voltage is present at terminal 2, only when temperature rise causes thermal switch S1 to close.

- (3) Breakdown diodes CR11, CR12, and CR13, mounted on the chassis of panel 1A19/2A19, are shunt regulators for external dc power supplies. The chassis of panel 1A19/2A19 provides heat dissipation for these breakdown diodes; they have no functional relationship to panel 1A19/2A19 power supply.

b. Circuit Description.

- (1) This power supply consists of B single power transformer having multiple secondary windings, feeding five separate

dc power supplies. Also, the secondary windings deliver 39-volt 60-cps and 28 volt 60-cps power to external circuits.

- (2) The dc power supplies are conventional, each consisting of a full-wave rectifier, filter, and a fused output line. The dc power supplies that provide 7 volts and 16 volts have signal ground return. The remaining three dc power supplies are floating.

c. Theory.

- (1) Primary 115-volt 60-cps power, appearing across terminals 4 and 5 of jack J1, is applied to the primary (terminals 1 and 2) of transformer T1. The power is coupled through transformer T1 and appears across its five secondary windings, stepped down to various voltage values as shown in figure 6-90.
- (2) A full-wave rectifier circuit, connected across each winding, rectifies the ac power and converts it to negative dc voltages at the plates of each diode rectifier pair. These voltages are coupled through separate filter networks which remove most of the ripple from the dc voltages. These voltages are applied to external circuits through jack J1, as indicated in *a(l)* above.
- (3) Thirty-nine-volt 60-cps and 34-volt cps power is obtained across separate secondary windings. The latter voltage is reduced to 28 volts by resistors R1 and R2, before connection at jack J1.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE

Section I. TROUBLESHOOTING AT DIRECT SUPPORT

3-1. General

Some direct support maintenance may be performed while the units are operating in a system, but detailed troubleshooting is usually performed with the unit removed to the test bench after the symptom has been confirmed. Check all indications thoroughly to obtain a complete symptom before referencing the troubleshooting charts.

3-2. Use of Troubleshooting Charts

a. The direct support troubleshooting charts for the TD-352/U and TD-353/U are given in paragraphs 3-6 and 3-7, respectively. They include symptoms and probable causes that may persist after corrective actions such as panel substitution, fuse and lamp replacement, etc. have been tried at the organizational category.

Note. Although individual plug-in panels undergo troubleshooting procedures only at the general support maintenance category, the multiplexer can be restored to operation at the organizational category by using substitute panels. If this fails, the direct support troubleshooting procedures will restore the multiplexers to full operation because they include all unit circuitry except the plug-in panels.

b. Before using the direct support troubleshooting charts, check the following items thoroughly:

- (1) Be sure that panels substituted at the organizational category were fully operational (that is, not marginal) and that the identical trouble symptom persisted after installation of a substitute panel.
- (2) If operation of the unit is marginal, check all adjustments authorized at the organizational category. If marginal trouble persists, perform the direct support alignment procedures given in paragraphs 3-8 through 3-14. If realignment does not correct the trouble, proceed to the troubleshooting charts.
- (3) Check for signs of obvious physical damage.
 - (a) Cut cable harness.
 - (b) Broken wiring connections.
 - (c) Damaged parts.
- (4) Check the seating of plug-in panels in their mating connectors on the unit chassis.

c. After replacement of parts in direct support troubleshooting procedures, both organizational category adjustments and direct support alignment must be performed.

d. When a procedure calls for the multiplexer to be looped-back, this means that one jumper cable must be connected between the front panel pcm OUT and pcm IN connectors, and another cable between the TIMING OUT and TIMING IN connectors. These connections are required for direct support troubleshooting on the test bench. They are not necessary if the unit is being checked during operation in a system loop.

e. In some instances, the use of a modulated channel is required. This can be obtained using the internal 1,100-cps test tone and the switch settings described in TM 11-5805-367-12.

f. To check the operation of the various filters, waveforms must be presented on an oscilloscope. The expected waveforms are shown at the Rcvr of this manual. The methods given for checking waveforms in the general support maintenance procedures, chapter 4, are also applicable to the direct support procedures.

g. An electrical test panel (extender panel) will provide easy access to connectors on the unit chassis for measurement purposes.

3-3. Continuity Checks

Warning: Failure to disable ac power to the unit during continuity checks also constitutes a hazard to maintenance personnel and transistorized circuits.

a. If trouble is not corrected by any of the foregoing procedures, the wiring continuity must be checked. To do this systematically, the operating principles of the multiplexer as discussed in chapter 2 must be thoroughly understood.

TM 11-5805-367-35/3

Otherwise, each lead in the chassis will have to be checked, even though most connections may not apply to the trouble concerned.

b. Chassis wiring diagrams for Multiplexers and TD-353/U can be found at the rear of this manual (figs. 6-94 and 6-97).

3-4. Mechanical Maintenance

a. Mechanical adjustments and lubrication are not required on either unit. The locations of all chassis-mounted parts are shown in diagrams in chapter 6, and removal and replacement procedures are routine.

b. If an individual lead of the wiring harness is to be replaced because it is open, cut, burned, or too short to resolder when broken from connection points, the new lead should be connected, properly routed, and laced atop the existing wiring harness. Cut the old lead short and snub the ends into the harness. Do not attempt to remove defective leads or undo harness lacing.

3-5. Test Equipment, Tools, and Materials Required

The following test equipment and materials are required for direct support troubleshooting. This same equipment can be used for the direct support alignment procedures given in paragraphs 3-8 through 3-14.

a. *Test Equipment.*

- (1) Oscilloscope AN/USM-140A (or AN/USM-281C).
- (2) Signal Generator SG-71/FCC.
- (3) Multimeter TS-352/U.
- (4) Voltmeter, Electronic ME-30B/U.
- (5) Voltmeter TS-443/U.
- (6) Multimeter ME-26B/U.

b. *Materials.*

- (1) Capacitor, 0.1 FF nonpolar.
- (2) Resistor, 600 ohms, 1%.
- (3) Resistor, 91 ohms.
- (4) Potentiometer, Precision, 2,000 ohms. |
- (5) Electrical Test Panel.

c. *Tools.*

- (1) Tool Kit, Electronic Equipment TK105/G.
- (2) Tool Equipment TE-123 or Tool Kit, Radio Repair TK-115/G.

3-6. Multiplexer TD-352/U Troubleshooting Procedure

a. *Troubleshooting Chart.*

Item No.	Symptom	Probable trouble	Correction
1	No 116 volt, 50-60 cps ac power to multiplexer input connections and fuses checked good at organizational category).	a. Inductor open in FL1 ----- b. S3 defective . -----	a. Check FL1. b. Check S3.

Item No.	Symptom	Probable trouble	Correction
1	No 115 volt, 50-60 cps ac power to multiplexer (input connections and fuses checked good at organizational category).	a. Inducator open in FL1 b. S3 defective	a. Check FL1. b. Check S3.
2	AC POWER fuses keep blowing, all other sources of short circuit eliminated (all panels removed).	a. Feedthrough capacitors in filter FL1 or FL8 short circuit b. B1 short circuit ----- c. C1 short circuit -----	a. Check FL1 and FL8. b. Check B1. c. Check C1.
3	Ac power is present in multiplexer, but replacement indicator will not light.	R3 in FL8 open circuit -----	Check FL8.
4	Blower motor does not operate.	a. C1 open circuit ----- b. B1 defective -----	a. Check C1. b. Check B1.
<i>Note.</i> In items 5 through 10, the opened signal connectors must be terminated in a 91-ohm load.			
5	Loss of pcm in input at terminal 14 of J32	FL64 or FL65 open circuit	Check for signal at P3 (essentially pcm in signal shown at terminal 14 on panel 1A12/2A12). If present, check FL65. If absent, check FL64.
6	No pcm out signal at J3	FF3B or FL69 open circuit	Check for signal at P11 (essentially pcm out signal shown at terminal 1 on panel 1A3/2A3). If present, check FL68. If absent, check FL69.
7	Loss of timing in input at terminal 2 of J33.	FL66 or FL67 open circuit	Check for signal at P7 (essentially timing in signal shown at terminal 2 on panel 2A13. If present, check FL67. If absent, check FL66.
8	No timing out signal at J4	FL70 or FL71 open circuit	Check for signal at P15 (essentially timing out signal shown at terminal 31 on panel 2A9). If present, check FL70. If absent, check FL71.
9	No alt pcm out signal at J5	FL72 or FL73 open circuit	Check for signal at P19 (essentially alt Pcm out signal shown at terminal 1 on panel 1A12/2A12). If present, check FL72. If absent, check FL73.
10	Loss of sync in input at terminal 17 of J25	FL74 or FL75 open circuit	Check for signal at P23 (essentially sync in signal shown at terminal 17 of panel 2A8). If present, check FL75. If absent, check FL74.
11	No earphone output signal at terminal A of talk monitor connector J12.	FL10 open circuit	Check FL10
12	Loss of mike input signal at terminal 4 of J37.	FL10 open circuit .	Check FL9.
13	No reading on TEST ALIGN meter for any position of METER SELECT switch.	a. FL11 or FL12 open circuit. b. M1 defective	a. Check FL11 and FL12. b. Check M1.

Item No.	Symptom	Probable trouble	Correction
14	Buzzer will not sound and FRAME indicator will not light.	K1 defective	Check K1.
15	FRAME indicator lights, but buzzer will not sound	a. DS5 defective b. S2 defective	a. Check DS5. b. Check S2.
16	+28 volt supply keeps blowing fuses (all panels removed).	Short circuit feed through capacitor in FL13.	Check FL13.
17	No test tone output from panel 1A16/2A16, improper or erratic gain of output signal, or gain is fixed and cannot be adjusted.	R1 defective	Check R1.
18	No scope sync output at J42	R8 open circuit	Check R8.
19	Erroneous aux input signal at terminal 31 of J35 and terminal 9 of 736.	R2 open circuit	Check R2.
20	Erroneous audio measure signal at terminal 26 of J37 when S6 is set to 2 WIRE position.	R5 open circuit	Check R5.
21	Loss of audio in or audio out signals on any of 12 channels.	One or more filters open circuit.	Check appropriate filters using chart in b below.

b. Audio Channel Input and Output Connections and Associated Filters.

Channel No.	Audio in No. 1		Audio in No. 1		Audio in No. 2		Audio in No. 2	
	Measured at terminals 1 and 2 of connector	Check filters	Measured at terminals 3 and 4 of connector	Check filters	Measured at terminals 30 and 31 of connector	Check filters	Measured at terminals 28 and 29 of connector	Check filters
1 -----	J29	FL51,	J29-----	FL53,	-----	-----	-----	-----
2 -----	J17 -----	FL52	J17-----	FL54	-----	-----	-----	-----
3 -----	-----	FL38,	-----	FL40,	J29 -----	FL26,	J29	FL28,
4 -----	-----	FL39	-----	FL41	-----	FL27	J17	FL29
5 -----	J30 -----	-----	J30-----	-----	J17 -----	FL14,	-----	FL16,
6 -----	J18 -----	FL55	J18-----	FL57,	-----	FL15	-----	FL17
7 -----	-----	FL56	-----	FL58	-----	-----	-----	-----
8 -----	-----	FL42,	-----	FL44,	J30 -----	FL30,	J30	FL32,
9 -----	J31 -----	FL43	J31-----	FL45	-----	FL31	J18	FL33
10 -----	J19 -----	-----	J19-----	-----	J18 -----	FL18,	-----	FL20,
11 -----	-----	FL59,	-----	FL61,	-----	FL19	-----	FL21
12 -----	-----	FL60	-----	FL62	-----	-----	-----	-----
		FL46,		FL48,	-----	-----	-----	-----
		FL47		FL49	J31 -----	FL34,	J31	FL36,
		-----		-----	-----	FL35	J19	FL37
		-----		-----	J19 -----	FL22,	-----	FL24,
		-----		-----	-----	FL23	-----	FL25

3-7. Multiplexer T-353/U Troubleshooting Procedure

a. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
1	No 115-volt, 50-60 cps ac power to multiplexer (input connections and fuses checked good at organizational category).	a. Inductor open in FL1 b. S3 defective	a. Check FL1. b. Check S3.
2	AC POWER fuses keep blowing, all other sources of short circuit eliminated (all panels removed).	a. Feedthrough capacitors in FL1 or FL8 short circuit. b. B1 short circuit c. C1 short circuit	a. Check FL1 and FL8. b. Check B1. c. Check C1.
3	Ac power is present in multiplexer, but replacement indicator will not light.	R3 in FL8 open circuit	Check FL8.
4	Blower motor does not operate.	a. C1 open circuit b. B1 defective	a. Check C1. b. Check B1.
<i>Note.</i> In items 4 through 9, the opened signal connections must be terminated in 91-ohm loads.			
5	Loss of <i>pcm in</i> input at terminal 14 of J45.	FL212 or FL213 open circuit.	Check for signal at P3 (essentially pcm in signal shown at terminal 14 of panel 1A12/2A12). If present, check FL213. If absent, check FL212.
6	No <i>pcm out</i> signal at J3	FL216 or FL217 open circuit.	Check for signal at P11 (essentially pcm out signal shown at terminal 7 of panel 1A3/2A3). If present, check FL216. If absent, check FL217.
7	Loss of <i>timing in</i> input at terminal 1 of J46.	FL214 or FL215 open circuit.	Check for signal at P7 (essentially timing in signal shown at terminal 1 of panel 1A13). If present, check FL215. If absent, check FL214.
8	No <i>timing out</i> signal at J4	FL218 or FL219 open circuit.	Check for signal at P15 (essentially timing out signal shown at terminal 11 of panel 1A8). If present, check FL218. If absent, check FL219.
9	Loss of <i>sync in</i> input at terminal 29 of J29.circuit.	FL220 or FL221 open	Check for signal at P19 (essentially sync in signal shown at terminal 29 of panel 1A8). If present, check FL221. If absent, check FL220.
10	No earphone output signal at terminal A of TALK MONITOR connector J12.	FL10 open circuit:	Check FL10.
11	Loss of mike input signal at terminal 4 of J50.	FL9 open circuit	Check FL9.

Item No.	Symptom	Probable trouble	Correction
12	No reading on TEST ALIGN meter for any position of METER SELECT switch.	a. FL11 or FL12 open circuit b. M1 defective	a. Check FL11 and FL12. b. Check M1.
13	Buzzer will not sound and FRAME indicator will not light.	K1 defective	Check K1.
14	FRAME indicator lights, but buzzer will not sound.	a. DS5 defective b. S2 defective	a. Check DS5. b. Check S2.
15	+28-volt supply keeps blowing fuses (all panels removed).	Shorted feedthrough capacitor in FL13.	Check FL13.
16	No test tone output from panel 1A16/2A16, improper or erratic gain of output signal, or gain is fixed and cannot be adjusted.	R1 defective	Check R1.
17	No SCOPE SYNC output at J62.	R8 open circuit	Check R8.
18	Erroneous aux input signal at terminal 31 of J48 and terminal 8 of J49.	R2 open circuit	Check R2.
19	Erroneous audio measure signal at terminal 26 of J50 when S6 is set to 2 WIRE position.	R5 open circuit	Check R5.
20	Loss of audio in or audio out signals on any of 48 channels.	One or more filters open circuit	Check appropriate filters using chart in b below.

b. Audio Channel Input and Output Connections and Associated Filters.

Channel No.	Audio in No. 1		Audio in No. 1		Audio in No. 2		Audio in No. 2	
	Measured at terminals 1 and 2 of connector	Check filters	Measured at terminals 3 and 4 of connector	Check filters	Measured at terminals 30 and 31 of connector	Check filters	Measured at terminals 28 and 29 of connector	Check filters
1 -----	J51 -----	FL120,	J51 -----	FL118,	-----	-----	-----	-----
2 -----	J30 -----	FL121	J30 -----	FL119	-----	-----	-----	-----
3 -----	-----	FL138,	-----	FL156,	J51 -----	FL116,	J51 -----	FL154,
4 -----	-----	FL139	-----	FL157	-----	FL117	-----	FL155
5 -----	J52 -----	-----	J52 -----	-----	J30 -----	FL136,	J30 -----	FL171,
6 -----	J31 -----	FL135	J31 -----	FL206	-----	FL137	-----	FL172
7 -----	-----	FL153	-----	FL207	-----	-----	-----	-----
8 -----	-----	FL190	-----	FL192	-----	-----	-----	-----
9 -----	J53 -----	FL191	-----	FL193	J52 -----	FL208	J52 -----	FL210
10 -----	J32 -----	-----	-----	-----	J31 -----	FL209	J31 -----	FL211
11 -----	-----	FL133	J53 -----	FL131	-----	FL174	-----	FL172
12 -----	-----	FL134	-----	FL132	-----	FL175	-----	FL173
13 -----	J54 -----	FL151	J54 -----	FL183,	-----	-----	-----	-----
14 -----	J32 -----	FL152	J32 -----	FL201	-----	-----	-----	-----
15 -----	-----	-----	-----	FL186,	-----	-----	-----	-----
16 -----	-----	-----	-----	FL187	J54 -----	FL202,	J54 -----	FL204,
17 -----	J55 -----	FL144,	J55 -----	FL126,	-----	FL203	-----	FL205
18 -----	J34 -----	FL145	J34 -----	FL127	J33 -----	FL168,	J33 -----	FL166,
19 -----	-----	FL182,	-----	FL180,	-----	FL169	-----	FL167
20 -----	-----	FL200	-----	FL181	-----	-----	-----	-----
21 -----	J56 -----	-----	-----	-----	J55 -----	FL108,	J55 -----	FL106,
22 -----	J35 -----	FL104,	J35 -----	FL140,	J34 -----	FL109	J34 -----	FL107
23 -----	-----	FL105	-----	FL141	-----	FL124,	-----	FL122,
		FL160,		FL178,		FL125		FL123
		FL161		FL179		-----		-----
		-----		-----	J56 -----	FL158,	J56 -----	FL176,
						FL159		FL177

b. Audio Channel Input and Output Connections and Associated Filters-Continued

Channel No.	Audio in No. 1		Audio in No. 1		Audio in No. 2		Audio in No. 2	
	Measured at terminals 1 and 2 of connector	Check filters	Measured at terminals 3 and 4 of connector	Check filters	Measured at terminals 30 and 31 of connector	Check filters	Measured at terminals 28 and 29 of connector	Check filters
24 -----	-----	-----	-----	-----	J35 -----	FL162, FL163	J35-----	FL142, FL143
25 -----	J57 -----	FL30, FL31	J57-----	FL28, FL29	-----	-----	-----	-----
26 -----	J36 -----	FL66, FL67	J36-----	FL84, FL85	-----	-----	-----	-----
27 -----	-----	-----	-----	-----	J57 -----	FL26, FL27	J57-----	FL25, FL43
28 -----	-----	-----	-----	-----	J36 -----	FL64, FL65	J36-----	FL46, FL47
29 -----	J40 -----	FL44, FL45	J40-----	FL80, FL81	-----	-----	-----	-----
30 -----	J19 -----	FL62, FL63	J19-----	FL82, FL83	-----	-----	-----	-----
31 -----	-----	-----	-----	-----	J40 -----	FL98, FL99	J40-----	FL100 FL101
32 -----	-----	-----	-----	-----	J19 -----	FL102 FL103	J19-----	FL48 FL49
33 -----	J41 -----	FL23, FL24	J41-----	FL41, FL42	-----	-----	-----	-----
34 -----	J20 -----	FL60, FL61	J20-----	FL78, FL79	-----	-----	-----	-----
35 -----	-----	-----	-----	-----	J41 -----	FL21, FL22	J41-----	FL39, FL40
36 -----	-----	-----	-----	-----	J20 -----	FL58, FL59	J20-----	FL74, FL75
37 -----	J42 -----	FL56, FL57	J42-----	FL92, FL93	-----	-----	-----	-----
38 -----	J21 -----	FL112, FL113	J21-----	FL94, FL95	-----	-----	-----	-----
39 -----	-----	-----	-----	-----	J42 -----	FL110 FL111	J42-----	FL114 FL115
40 -----	-----	-----	-----	-----	J21 -----	FL96, FL97	J21-----	FL76, FL77
41 -----	J43 -----	FL19, FL20	J43-----	FL17, FL18	-----	-----	-----	-----
42 -----	J22 -----	FL37, FL38	J22-----	FL54, FL55	-----	-----	-----	-----
43 -----	-----	-----	-----	-----	J43 -----	FL15, FL16	J43-----	FL14, FL32
44 -----	-----	-----	-----	-----	J22 -----	FL52, FL53	J22-----	FL50, FL51
45 -----	J44 -----	FL33, FL34	J44-----	FL68, FL69	-----	-----	-----	-----
46 -----	J23 -----	FL70, FL71	J23-----	FL90, FL91	-----	-----	-----	-----

b. Audio Channel Input and Output Connections and Associated Filters-Continued

Channel No.	Audio in No. 1		Audio in No. 1		Audio in No. 2		Audio in No. 2	
	Measured at terminals 1 and 2 of connector	Check filters	Measured at terminals 3 and 4 of connector	Check filters	Measured at terminals 30 and 31 of connector	Check filters	Measured at terminals 28 and 29 of connector	Check filters
47 -----	-----	-----	-----	-----	J44 -----	FL86, FL87	J44-----	FL88, FL89
48 -----	-----	-----	-----	-----	J23 -----	FL72, FL73	J23-----	FL35, FL36

Section II ALIGNMENT

3-8. General

a. Direct support alignment procedures involve adjustments accessible on the handles of certain plug-in panels. There are two internal adjustments, one on panel 1A1/2A1 and one on panel 1A6/2A6, but these are authorized only for general support maintenance.

b. The procedures listed below should be used for direct support maintenance as explained in paragraphs 3-1 through 3-7, but they must be used also after any general support maintenance, especially when parts have been replaced in g. 1A6/2A6, 1A2/2A2, 1A7, 1A15 or 2A15.

c. Perform the alignment in the precise order given.

d. The alignment procedures are applicable both Multiplexers TD-352/U and TD-353/U, except where differences in reference designations of adjustment controls have been given.

e. The following is a summary of the controls to be adjusted:

Multiplexer	Panel	Reference designator	Nomenclature
TD-352/U and TD-353/U	1A6/2A6-----	R6 -----	CCL (common channel level adjust).
	1A2/2A2-----	R26-----	CA (compressor adjust).
TD-352/U only ----	2A15-----	R1,R11-----	PAM (pam level adjust).
	1A7-----	R19-----	CTR (pam center adjust).
TD-353/U only ----	1A15-----	R30-----	ECL (even channel level adjust).
	1A15-----	R16-----	CTR (pam center adjust).

3-9. Switch Settings and Preliminary Procedures

- a. Operate the TD-352/U front panel switches as follows:
 - (1) METER SELECT: OFF.
 - (2) AC POWER: OFF.
 - (3) BUZZER: OFF.
- b. Operate the TD-352/U or T-353/U side panel switches as follows:
 - (1) AUX: OUT.
 - (2) 2 WIRE-4 WIRE: 4 WIRE.
 - (3) ADDRESS: MASTER.
- c. Remove noise generator panel 1A11/2A11.
- d. Synchronize the oscilloscope; use the SCOPE SYNC output on the side panel of each multiplexer.
- e. Loop-back the timing and pcm signals.

3-10. Preliminary Coder Adjustment (Panel 1A6/2A6)

- a. Turn the test unit AC POWER switch OFF.
- b. Use modified Coder Adjust Panel. NSN 6625-00-668-9418, or modify an extender panel as follows:
 - (1) Disconnect the leads to terminal 26 and 31.
 - (2) Connect a 0.1 uf, or larger, nonpolar capacitor between terminals 30 and 31.
 - (3) Connect one side of a 2,000-ohm potentiometer 2 watts +3% Lin +0.2% to terminal 19 (+4.5 volts) and the other side to terminal 27 (-4.5 volts).
 - (4) Connect the center arm of the potentiometer to terminal 31. This provides a variable dc voltage input of at least +2.5 volts to the coder pam input of panel 1A6/2A6.
- c. Remove panel 1A6/2A6 from the test unit, insert the modified Coder Adjust Panel/modified extender panel into the test unit, and then insert panel 1A6/2A6 into the extender panel.
- d. Operate the test unit AC POWER switch to ON. Set switch S-1 on modified Coder Adjust Panel to the CCL position, and adjust CCL as follows:
 - (1) Set the side panel switch of TD-352/U to dc
 - (2) Adjust the CCL for a green reading on front panel meter.
- e. Adjust the oscilloscope for a horizontal sweep of 0.5 uSEC/CM.
- f. Connect the oscilloscope probe to the pcm OUT connector on front panel of the test unit.

NOTE

The least significant digit (lsd) of a channel is the most active digit observed when the potentiometer on the extender panel is rotated.

- g. Set switch S-1 on modified Coder Adjust Panel to the CA position. Rotate the extender panel potentiometer in both directions. AD levels should be observed on the oscilloscope as the coder pam input voltage is varied from -2.5 to +2.5 volts. If levels 101111 (47) and 110000 (48) are missing, adjust potentiometer R26 on panel 1A6/2A6 counterclockwise until they appear.
- h. Check to see that levels 001111 (15) and 010000 (16) are not missing. (Overcompensation of potentiometer R26 may cause loss of these two levels.) If levels 001111 (15) and 010000 (16) are missing, rotate potentiometer R26 clockwise until they appear.
- i. Repeat the procedures given in g and h above until all levels are present. Set switch S-1 on modified Coder Adjust Panel to CCL position, and check CCL adjustment again (paragraph 3-10d). Readjust if needed.
- j. Operate the test unit AC POWER switch to OFF and remove both panel 1A6/2A6 and the extender panel.

3-11. Decoder Alignment (Panel 1A15 or 2A15)

The following adjustment positions center code levels 010000 (16) through 101111 (47) with respect to the other levels.

- a. Modify the extender panel as follows:

- (1) Remove the capacitor from terminals 30 and 31.
- (2) Remove the potentiometer from terminals 19,27, and 31.
- (3) Leave terminals 26 and 31 disconnected.
 - b. Install panel 1A6/2A6 in the test unit; use this modified extender panel.
 - c. Operate the AC POWER switch to ON.
 - d. Apply a 1,000-cps, 4.5 volt peak-to-peak sine wave across terminals 31 and 30 (ground). (If coder alignment test panel is used, inject signal at terminals 26 and 30.)
 - e. Synchronize the oscilloscope with the 1,000-cps oscillator.
 - f. Connect the oscilloscope probe to receive pam output of the panel being aligned (jack J1 on either 1A15 or 2A15).
 - g. Adjust the pam center adjust (CTR) control of the panel being aligned (that is, R19 on 2A15, or R16 on 1A15 until the waveform presented on the oscilloscope has minimum discontinuity.
 - h. Operate the AC POWER switch to OFF and remove both panel 1A6/2A6 in the test unit.
 - i. Proceed with the pam level adjustment (para 3-12 or 3-13).

3-12. Multiplexer TD-352/U Pam Level Adjustment (Panda 1A2/2A2 and 1A6/2A6)

The TD-352/U pam level adjustment is made by adjusting PAM level potentiometers R1 and R11 on each modem panel 1A2/2A2 and CCL (common channel level) potentiometer R6 on coder panel 1A6/2A6. There are two modems per 1A2/2A2 panel. The potentiometers on the lower part of the panel handle are for the lower numbered channel, and the potentiometers on the upper part of the handle are for the higher numbered channel. For example, in the modem used for channels 2 and 4, the adjustments for channel 2 are on the lower part of the handle; those for channel 4, are on the upper part of the handle.

- a. Remove panel 2A7 and reinstall; use a standard extender panel.
- b. Operate the TD-352/U test unit AC POWER switch to ON.
- c. Connect the oscilloscope probe to terminal 23 on panel 2A7. Adjust the vertical deflection for 0.5 VOLT/CM or less and set the AC DC mode switch to dc
- d. Adjust any channels that are not 0 volts dc to 0.0 A 0.025 volts by means of the PAM adjustment potentiometers R1 and R11 on the 1A2/2A2 panels.
- e. Check position G on the aide panel switch and move the CCL adjustment on coder panel 1A6/2A6 until position G reads in the green region of the front panel meter. The meter indication should move up scale with clockwise rotation of the CCL potentiometer and down scale with counterclockwise rotation.
- f. Connect the oscilloscope probe to the pcm OUT connector on the front of the test unit and adjust any channel that is not between levels 011101 129) and 100010 134).
- g. Check that levels 15 and 48 are present per paragraph 3-10.
- h. Proceed with the final decoder alignment (para 3-14).

3-13. Multiplexer TD-353/U Pam Level Adjustment (Panels 1A1/2A1, 1A6/2A6, and 1A7)

The TD-353/U pam level adjustment is made by adjusting PAM level potentiometers R1 and R11 on each modem panel 1A2/2A2, and the CCL potentiometer R6 on coder panel 1A6/2A6, and ECL potentiometer R30 on panel 1A7. There are two modems per 1A2/2A2 panel. The potentiometers on the lower part of the panel handle are for the lower-numbered channel, and the potentiometers on the upper part of the handle are for the higher numbered channel. For example, in the modem used for channels 2 and 4, the adjustments for channel 2 are on the lower part of the handle; those for channel 4, are on the upper part of the handle.

- a. Remove panel 1A7 and reinstall; use a standard extender panel.
- b. Adjust the TD-353/U test unit AC POWER switch to ON.
- c. Connect the oscilloscope probe to terminal 25 in panel 1A7. Adjust the vertical deflection for 0.5 Volt/CM or less and the AC DC mode switch to DC.
- d. Adjust any even channels that are not 0 volts dc to 0.0 A 0.025 volts by means of the PAM adjustment potentiometers R1 and R11 on the 1A2/2A2 panels.
- e. Connect the oscilloscope probe to terminal 5 on panel 1A7. Adjust the vertical deflection for 0.5 VOLT/CM or less and the AC DC mode switch to DC.

- f. Adjust any odd channels as indicated in d above.
- h. Connect the oscilloscope probe to terminal 22 on panel 1A7. Adjust ECL potentiometer R30 on 1A7. so that the odd channels line up with the even channels to within +0.05 volts
- g. Check position G on the side panel switch and move the CCL adjustment on coder panel 1A6/2A6 until position G reads in the green region of the front panel meter. The meter indication should move up scale with clockwise rotation of the CCL potentiometer and down scale with counter clockwise rotation.
- i. Connect the oscilloscope probe to pcm OUT connector on the front of the test unit and adjust any channel that is not between levels 011101 (29) and 100010 (34).
- j. Check that levels 15 and 48 are present per paragraph 3-10.
- i. Proceed with the final decoder alignment (para 3-14).

NOTE

Modem panel 1A2/2A2 or 1A2/2A2A gain adjustments are performed as part of organizational maintenance (TM 11-5805-367-12).

3-14. Final Decoder Alignment (Panel 1A15 or 2A15)

- a. Select a channel that has a code level of 011111 (31) or 100000 (32), and terminate the output of that channel in a 600-ohm load.
 - b. Apply a 1,000-cps signal to the input of the selected channel, and adjust the input level of the audio oscillator to -4 dbm.
 - c. Note the output of the selected channel as measured on an ac vtvm; this should be -4 dbm.
 - d. Reduce the level of the audio input signal to -30 dbm and note the output voltage. This should be exactly 20 db down from the output obtained in c above. If not, adjust CTR (pam center adjust) potentiometer R19 (for panel 2A15) or potentiometer R16 (for panel 1A15) to obtain the correct reading.
- note.* Any adjustment of potentiometer R19 or R16 should be very slight. If excessive, repeat the preliminary adjustment (para 3-10), and then repeat the final adjustment.

CHAPTER 4 GENERAL SUPPORT MAINTENANCE

Section I. INTRODUCTION

Warning: When troubleshooting or making repairs in this equipment, be careful not to contact 115-volt ac connections. Use insulated test probes when making voltage measurements. Always disconnect the power cord from a unit before touching any of the internal parts.

4-1. Scope of General Support Maintenance Procedures

General support maintenance consists of troubleshooting, repairing, and testing defective plug-in panels returned by organizational maintenance personnel. Troubleshooting procedures for each type of plug-in panel of the TD-352/U and TD-353/U are provided in paragraphs 4-6 through 4-32. Repair procedures are covered in TB SIG 222. The testing of a repaired plug-in panel is accomplished by installing the plug-in panel in a TD-352/U or TD-353/U and performing the appropriate performance test (para 5-5 or 5-7).

Caution: When making repairs on the 1A14A/2A14A panel A 1, A e the Desoldering TM 11-5805-367-35/3 (FSN 3439-907-5806).

4-2. Organization of Troubleshooting Procedure'

a. *Sectionalization.* Sectionalizing faults in the TD-352/U or TD-353/U consists of tracing the source of the trouble to one or more plug-in panels, or to the unit chassis itself. This is normally done at the organizational category and in accordance with the procedures contained in TM 115805-367-12. If panel substitution at the organizational category does not sectionalize the trouble, the unit chassis must be subjected to the direct support procedures given in chapter 3. When a fault is sectionalized to a panel, either at the organizational category or as a result of further checks at the direct support maintenance that panel is sent to general support maintenance for localization of any trouble.

b. *Localization.* Localization of faults on the panels concerns tracing the source of trouble to the defective stage. This is done with the use of the troubleshooting charts (para s 4-5 through 4-31). A schematic diagram for each panel is included at the rear of this manual accompanied by waveforms for all points used to localize any fault listed in the corresponding troubleshooting chart. The general conditions for use of the charts are given in paragraph 4-3, and information relative to use of the waveforms is included in paragraph 4-4.

c. *Isolation.* Isolation of a faulty part in a defective stage is accomplished by making voltage and waveform measurements. A voltage and waveform chart is provided at the end of each panel troubleshooting chart.

Note. To isolate short circuits, it may be necessary to remove wires from terminals.

4-3. Use of Troubleshooting Charts

a. To localize a fault to a defective stage, install the panel on an electrical test panel (extender panel). Remove the corresponding panel in a TD-352/U or TD-353/U, and insert the extender/ faulty panel combination in place of the removed panel. The only exception to this procedure is the power supply panels, which require the use of extender cables. It is important that the notes pertaining to troubleshooting dual-type panels (that is, panels used in either the TD-352/U or TD-353/U, or used for transmit and receive functions) be strictly followed.

b. When a procedure calls for the bench test multiplexer to be looped-back, this means that one jumper cable must be connected between the front panel pcm OUT and pcm IN connectors, and another cable between the TIMING OUT and TIMING IN connectors.

c. In some instances the use of a modulated signal channel is required. This can be obtained using the internal 1,100-cps test tone and switch settings as described in TM 11-5805-367-12.

d. The probable cause and corrective action listed for any given symptom assumes that all previous symptoms are negative. This makes it unnecessary to list redundant information in each succeeding symptom. For example, if a panel

TM 11-5805-367-35/3

exhibits a symptom given as item 10, the symptoms of items 1 through 9 must be proved negative by test before the corrective action recommended for item 10 is followed.

e. If a dual-unit panel is to be investigated for faults, it must be checked completely in both TD-352/U and TD-353/U bench test units since differences exist in timing signal frequencies, input and output connections, etc.

A. Only terminal numbers of panel connectors are listed in the charts. The connector designator is stipulated to be that shown on the corresponding schematic diagram included at the rear of this manual.

g. Parts can be located by reference to the appropriate top panel view figure.

h. After replacement of any part, be sure that no other trouble exists.

i. When a panel is repaired, proceed as follows:

(1) Insert the panel in the TD-352/U or TD-353/U and check its alignment; use the procedures given in chapter 3, section II. If type 1A1/2A1 or 1A6/2A6 panels have been repaired, their alignment must first be checked (and adjusted, if necessary) in accordance with the procedures given in section III of this chapter.

(2) Perform the performance tests given in chapter 5.

4-4. Use of Waveforms

a. The principal factors that affect the waveforms are the oscilloscope grid values: sweep time and vertical sensitivity. Other conditions affecting the waveform obtained are given in the troubleshooting charts where applicable, and include the test requirements as listed in (1) through (4) below. These requirements must be met to obtain the expected waveform.

(1) Modulating frequencies used.

(2) TD-352/U or TD-353/U connections.

(3) Oscilloscope synchronization requirements. (4) TD-352/U or TD-353/U control switch settings.

b. The waveforms obtained on the oscilloscope should be compared with the reference waveforms. When a waveform is erroneous or absent, make a detailed check of the appropriate stage using the instructions given in the troubleshooting chart. Supplementary voltage and waveform data for the modules and transistors of the panel are also given after each chart for use in isolating faulty parts.

4-5. Test Equipment and Tools Required

a. Multiplexer TD-352/U (two required).

b. Multiplexer TD-353/U (two required).

c. Oscilloscope AN/USM-140A (or AN/USM-281C).

d. Multimeter TS-352/U.

e. Voltmeter, Electronic ME-30B/U.

f. Voltmeter TS-443/U.

g. Transistor Test Set TS-1836/U.

h. Headset-Microphone H-91A/U.

i. Signal Generator SO-71/FCC.

j. Multimeter ME-26B/U.

k. Tool Equipment TE-123.

l. Tool Kit, Electronic Equipment TK-105/G,

m. Cable Assembly, Radio Frequency CG-1040B/U (three required).

n. Extender Cable Assembly for panel 1A1/2A1 (fabricated as in fig. 4-1).

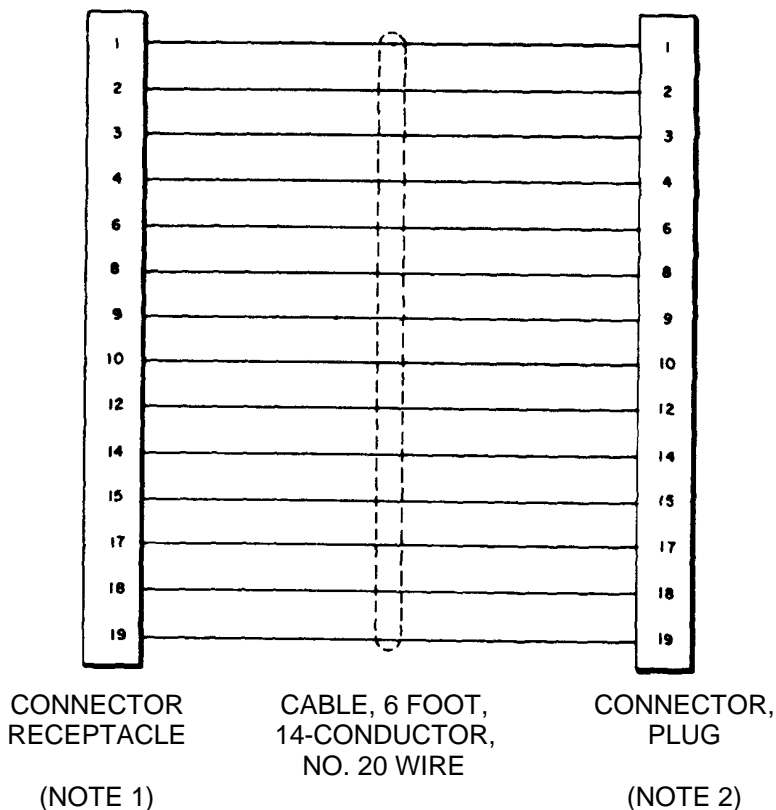
o. Extender Cable Assembly for panel 1A19/ 2A19 (fabricated as in fig. 4-1).

Section II. TROUBLESHOOTING AT GENERAL SUPPORT

4-6. Panel 1A1/2A1, Troubleshooting

a. Troubleshooting Chart Troubleshooting procedures for regulated power supply 1A1/2A1 are performed on the bench, with an extender cable between the test unit and power supply.

Fabricate the extender cable in accordance with figure 4-1. Connect the receptacle end of the cable to jack J1 on the rear of the power supply. When checking the power supply with the TD-352/U test unit, connect the plug end of the extender cable into jack J41 in panel 1A1/2A1, compartment. When checking the power supply with the TD353/U test unit, connect the plug end of the cable into jack J61 in panel 1A1 compartment.



NOTES

1. NSN 5935-00-687-2157
2. NSN 5935-00-577-0011

EL2RC001

Figure 4-1. Extender cable assembly.

Item No.	Symptom	Probable trouble	Correction
1	Panel causes fuse to blow in unregulated power supply 1A19/2A19.	Short circuit in regulator circuit associated with blown fuse.	<ol style="list-style-type: none"> a. Check for short in connector pins of appropriate unregulated input and regulated output terminals. b. Check for emitter-to-collector short in series-regulator transistors. c. Check for short circuits in other circuit parts that are connected directly across appropriate regulated output line and ground.
2	Regulated output voltage high and cannot be adjusted.	Associated voltage adjust circuit open.	<ol style="list-style-type: none"> a. Check appropriate voltage adjust potentiometer for open circuit. b. Check for emitter-to-collector short in differential amplifier transistor controlled by voltage adjust potentiometer.

Item No.	Symptom	Probable trouble	Correction
3	Simultaneous loss of all regulated output voltages. (Fuses in unregulated power supply are good.)	One or more individual regulator circuits defective.	Disconnect one end of the wire between-1A1/2A1-E41 and 1A1/2A1-E7. This will disable the short circuit protection circuit. All output voltages except those from the defective circuit will be restored. If all output voltages are missing, the trouble is in the -12 volt circuit. Refer to Item No. 4.
4	Erroneous -12 volt regulated output at terminal 20.	VR6, Q27, Q28, Q29, or Q30 defective.	<p>a. Check VR6 first. If good, proceed to b below</p> <p>b. Measure voltage at base of Q29 and Q30. If voltages are equal, try adjusting R58. If voltages remain equal, check continuity of circuit from base of Q29, through R58, to -12 volts and ground sides of regulator circuit. 5) Q29 and Q30 base voltages are not equal, check Q29, Q28, and Q27 for voltages listed in A below. If voltages are not approximately as given, check appropriate transistor.</p>

Item No.	Symptom	Probable trouble	Correction
5	Erroneous -4.5 volt regulated output at terminal 22.	Q6, Q7, Q8, or Q9, defective.	<p>a. First, check VR2. If good, proceed to b below.</p> <p>b. Measure voltage at base of Q8 and Q9. If voltages are equal, try adjusting R12. If voltages remain equal, check continuity of circuit from base of Q8 through R12, to -4.5 volts and ground sides of regulator circuit. If Q8 and Q9 base voltages are not equal, check Q8, Q7, and Q6 for voltages listed in c below. If voltages are not approximately as given, check appropriate transistor.</p>
6	Erroneous +4.5 volt regulated output at terminal 6.	VR3, Q11, Q12, Q13, Q9 defective.	<p>a. First, check VR3. If good, proceed to b below.</p> <p>b. Measure voltage at base of Q13 and Q14. If voltages are equal, try adjusting R22. If voltages remain equal, check continuity of circuit from base of Q13, through R22, to +4.5 volt and ground sides of regulator circuit. If Q13 and Q14 base voltages are not equal, check Q13, Q12, and Q11 for the voltages listed in d below. If voltages are not approximately as given, check appropriate transistor.</p>
7	Erroneous +10 volt regulated output at terminal 4.	VR1, Q1, Q2, Q3, or Q4 defective.	<p>a. First, check VR1. If good, proceed to b below.</p> <p>b. Measure voltage at base of Q3 and Q4. If voltages are equal, try adjusting R1. If voltages remain equal, check continuity of circuit from base of Q3, through R1, to +10 volts and ground sides of regulator circuit. If Q3 and Q4 base voltages are not equal, check Q3, Q2, and Q1 for voltages listed in e below. If voltages are not approximately as given, check appropriate transistor.</p>

Item No.	Symptom	Probable trouble	Correction
8	Erroneous +25 volt regulated output at terminal 2.	VR4, Q16, Q17, Q18, or Q19 defective.	<p>a. First, check VR4. If good, proceed to b below.</p> <p>b. Measure voltage at base of Q18 and Q19. If voltages are equal, try adjusting R32. If voltages remain equal, check continuity of circuit from base of Q18, through R32, to +25 volt and ground sides of regulator circuit. If Q18 and Q19 base voltages are not equal, check Q18, Q17, and Q16 for voltages listed in 1 below. If voltages are not approximately as given, check appropriate transistor.</p>
9	Erroneous -5.2 volt regulated output at terminal 24.	VR5, Q23, Q24, Q25, or Q26 defective.	<p>a. First, check VR6. If good, proceed to b below.</p> <p>b. Measure voltage at base of Q23 and Q24. If equal, try adjusting R53. If voltages remain equal, check continuity of circuit from base of Q25, through R53, to -5.2 volts and ground sides of regulator circuit. If Q23 and Q24 base voltages are not equal, check Q24, Q25, and Q26 for voltages listed in g below. If voltages are not approximately as given, check appropriate transistor.</p>

b. -12-Volt Regulator voltage with Respect to Ground.

Base of Q29 with respect to base of Q30	Collector Q29	Emitter Q28	Emitter Q27
Positive -----	-14 to -16 -----	-13.7 to -15.7 -----	-13.4 to -15.4
Negative -----	-6.0 -----	-5.7 -----	-5.4
Equal -----	-12.6 -----	-12.4 -----	-12.0

c. -4.5Volt Regulator Voltages with Respect to Ground

d.

e.

f. .

Base of Q8 with respect to base of Q9	Collector Q8	Emitter Q7	Emitter Q6
Positive -----	-6 to -8 -----	-5.7 to -7.7 -----	-5.4 to -7.4
Negative -----	-3.0 -----	-2.7 -----	-2.4
Equal -----	-4.5 -----	-4.9 -----	-4.5

d. +4.5-Volt Regulator Voltages with Respect to +4.5-volt Bus.

Base of Q13 with respect to base of Q14	Collector Q13	Emitter Q12	Emitter Q11
Positive -----	-6 to -8 -----	-5.7 to -7.7-----	-5.4 to -7.4
Negative-----	-3.0-----	-2.7-----	-2.4
Equal-----	-5.1-----	-4.8-----	-4.3

e. +10-Volt Regulator Voltages with Respect, to +10-Volt Bus.

Base of Q3with respect to base of Q4	Collector Q3	Emitter Q2	Emitter Q1
Positive -----	-12 to -15 -----	-11.7 to -14.7 -----	-11.4 to -14.4
Negative-----	-6-----	-5.7-----	-5.4
Equal-----	-10.6-----	-10.3-----	-10.0

f. +26-Volt Regulator Voltages with Respect to +25-Volt Bus.

Base of Q18ith respect to base of Q19	Collector Q18	Emitter Q17	Emitter Q16
Positive -----	-28 to -32 -----	-27.7 to -31.7 -----	-27.4 to -31.4
Negative-----	-12-----	-11.7-----	-11.4
Equal-----	-25.6-----	-25.3-----	-25.0

g. -5.2-Volt Regulator Voltages with Respect, to Ground.

Base of Q23with respect to base of Q24	Collector Q24	Emitter Q25	Emitter Q26
Positive -----	-7.1 -----	-6.8-----	-6.5
Negative-----	-.6-----	-.3-----	0
Equal-----	-5.5-----	-5.4-----	-5.2

h. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with intern 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Voltage measurements are as follows:

TM 11-5805-367-35/3

Transistor	Base	Emitter	Collector	Transistor	Base	Emitter	Collector
Q1-----	-0.3	0	-4.5	Q17-----	+0.8	+1.0	+0.9
Q2-----	-0.4	-0.3	-11.3	Q18-----	+19.0	+19.0	+0.8
Q3-----	+3.8	+4.0	+0.4	Q19-----	+18.8	+19.0	0
Q4-----	+3.8	+4.0	0	Q20-----	+10.0	+3.0	-0.5
Q5-----	+4.9	+2.3	-12.6	Q21-----	+10.0	+3.0	-12.6
Q6-----	-4.9	-4.5	-6.6	Q22-----	+9.5	+9.3	+9.9
Q7-----	-5.0	-4.9	-11.8	Q23-----	0	+0.2	-5.2
Q8-----	-2.9	-2.8	-4.5	Q24-----	0	+0.2	-5.5
Q9-----	-2.9	-2.8	-4.5	Q25-----	-5.5	-5.4	-5.7
Q10-----	0	-1.0	-12.6	Q26-----	-5.4	-5.2	-5.7
Q11-----	-0.2	0	-2.5	Q27-----	-12.4	-12.0	-15.2
Q12-----	-0.3	-0.2	-11.5	Q28-----	-12.6	-12.4	-19.5
Q13-----	+1.6	+1.7	0	Q29-----	-6.1	-6.0	-12.6
Q14-----	+1.6	+1.7	-0.3	Q30-----	-6.2	-6.0	-12.0
Q15-----	+4.5	+2.3	-12.6	Q31-----	0	-6.9	-12.6
Q16-----	-0.32	0	-7.3				

4-7. Panel 1A2/2A2, Troubleshooting

a. Troubleshooting pam For the following procedures the TD-352/U and TD-353/U test units must be looped-back and the channels modulated specifically as described for the individual symptoms. When parts such as PAM (R1 and R11) and AG (R7 and R17) controls are replaced, the panel must be adjusted and checked for nominal gain, using the internal test tone.

Item No.	Symptom	Probable trouble	Correction
1	No transmitter pam outputs or erroneous transmit pam output at terminal 9.	One or both modulator circuits defective.	<p>a. Set test unit SERV SEL and CHANNEL selector switches to apply internal test tone signal to first (lower-numbered) channel of position in which panel is being checked. (That is, if panel is being tested in channel 1, 3 position, apply test tone to channel 1 first.)</p> <p>b. Check transmit pam output at terminal 9. If present and correct, proceed to c below. If absent, check Z1 and Z2. If erroneous, check PAM adjustment R1; check R2, Z2, and T1 if trouble is not cleared.</p> <p>c. Set test unit CHANNEL selector switch to apply test tone signal to second (higher-numbered) channel of position in which panel is being checked. Check transmit pam output at terminal 9. If absent, check Z7 and Z8. If erroneous, check PAM adjustment R11; check R12, and T3 if trouble is not cleared.</p>

Item No.	Symptom	Probable trouble	Correction
2	No audio out No. 1 signal or erroneous audio out No. 1 signal across terminals 3 and 4 when test unit is switched so that test tone is modulating first (lower-numbered) channel of position in which panel is being checked.	<p>a. Z5, Z6, or Q1 defective.</p> <p>b. FL1 or R7 defective</p> <p>c. Amplifier in Z4 defective.</p> <p>d. Sampler in Z4 defective.</p> <p>e. Z3 defective</p>	<p>a. Check waveform at J3. If absent, proceed to b below. If absent, check Z5, Z6, and Q12. If signal is erroneous across terminals 3 and 4, feedback loop may be defective. An incorrect audio frequency response or high output level (defective AG control R7) is a symptom of this trouble. Check components in emitter circuit of Q1. If test unit audio gain adjustment procedure indicates demodulator is good, but there is still no output at terminals 3 and 4 of the panel, check R9 and T1.</p> <p>b. Check waveform at J2. If absent, proceed to e below. If present and correct, check FL1 and AG adjustment R7.</p> <p>c. Check waveform at pin 5 of Z4. If present, check amplifier in Z4. If absent, proceed to d below.</p> <p>d. Check waveform at pins 3 and/or 6 of Z4. If present, check sampler in Z7. If absent, proceed to e below.</p> <p>e. Z3 defective</p>
3	No audio out No. 2 signal or erroneous audio out No. 2 signal across terminals 28 and 29 when test unit is switched so that test tone is modulating second (higher-numbered) channel of position in which panel is being checked.	<p>Note. Since both demodulator circuits are identical, the probable troubles and corrective action for this symptom are identical with those given under item 2. Refer to figure 6-45 and substitute the appropriate parts reference designation numbers.</p>	

TM 11-5805-367-35/3

b. Module Terminal Voltages. The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements with the scope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) Channel of interest modulated with internal 1,100-cps test tone
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	2	3	4	5	6	7	8	9	10	11
Z1 -----	-----	12,13, fig. 6-46	9, 10, fig. 6-46	-----	14, 15, fig. 6-46	11, fig. 6- 46	-----	-----	-----	-----
Z2 -----	20,21, fig. 6-46	16,17, fig. 6-46	5, 6, fig. 6- 46	-----	14, 15, fig. 6-46	-----	-----	12, 13, fig. 6-46	-----	-----
Z3 -----	20,21, fig.6-46	16,17, fig. 6-46	5, 6, fig. 6- 46	-----	22, 23 fig. 6-46	-----	-----	18, 19, fig. 6-46	-----	-----
Z4 -----	-----	18,19, fig. 6-46	7, 8, fig. 6- 46	24, fig. 6- 46	22, 23 fig. 6-46	-----	-----	-----	1, fig. 6-46	+1.4
Z5 -----	0-----	-6.7 -----	-11.7 -----	-11.7-----	-----	-----	+0.5	-----	+0.5	-----
Z6 -----	-----	-6.7 -----	-----	-----	-----	-----	-----	-----	+2.5	-----
Z7 -----	-----	12,13, fig. 6-46	9, 10, fig. 6-46	-----	14, 15, fig. 6-46	11, fig. 6- 46	-----	-----	-----	-----
Z8 -----	20, 21, fig. 6-46	16,17, fig. 6-46	5, 6, fig. 6- 46	-----	14, 15, fig. 6-46	-----	-----	12, 13, fig. 6-46	-----	-----
Z9 -----	20, 21, fig. 6-46	16,17, fig. 6-46	5, 6, fig. 6- 46	-----	22, 23 fig. 6-46	-----	-----	18, 19, fig. 6-46	-----	-----
Z10-----	-----	18,19, fig. 6-46	7, 8, fig. 6- 46	24, fig. 6- 46	22, 23 fig. 6-46	-----	-----	-----	1, fig. 6-46	+1.4
Z11-----	0-----	-6.7	-11.7 -----	-11.7-----	-----	-----	+0.5	-----	+0.5	-----
Z12-----	-----	-6.7	-----	-----	-----	-----	-----	-----	+2.5	-----

4-8. Panel 1A3/2A3, Troubleshooting

a. Troubleshooting Chart. The following procedures must be performed with panel 1A3/2A3 installed in the TD-352/U and TD-353/U test units. The test units must be looped-back and one channel modulated.

Item No.	Symptom	Probable trouble	Correction
1	Loss of master (4 kc) address only. (Test unit is giving a FRAME alarm and TEST ALIGN meter does not read in green area with METER SELECT switch set to F.)	Z2 defective	Check Z2.
2	Loss of slave (2 kc) address only. (Test unit is giving a FRAME alarm and TEST ALIGN meter does not read in green area with METER SELECT switch set to F.)	Z1 defective	Check Z1.
3	No address (neither 2 kc nor 4 kc) in <i>pcm out</i> at terminal 1. (Test unit giving FRAME alarm.)	Q4, CR6, CR8, CR9, Q9, or CR2 defective.	Check waveform at J2. If absent, check Q4, CR8, and CR9. If present, check CR6, Q9, and CR2.
4	No <i>pcm out</i> or erroneous pcm out at terminal 1. (TEST ALIGN meter does not read in green area with METER SELECT switch set to PCM IN.)	CRT, Q1, CR4, Q2, Q3, CR12, CR13, Q5, CR14 CR15, Q6, Z3~Q7, or Q8 defective.	<p>a. Check waveform at J1. If absent, check CR1 and Q1. If present, proceed to <i>b</i> below.</p> <p>b. Check waveform at J3. If absent, check CR4, Q2, and Q3. If present, proceed to <i>c</i> below.</p> <p>c. Check waveforms at J9 and J5. If J4 is absent, check CR12, CR13, and Q5. If J5 is absent, check CR14, CR15, and Q6. If both waveforms are present, check Z3, Q7, and Q8.</p>

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with respect to ground with the ME-26 B/U and the figure references are to waveform measurements with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER unless instructed otherwise.
- (4) Pcm output terminated in 91-ohm load.
- (5) AUX A switch at OUT.
- (6) 2 WIRE-4 WIRE switch at 4 WIRE.
- (7) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1-----	1, 2, FIG. 6-48-----	1, 2, FIG. 6-48-----	-4.5
Q2-----	19, 20, FIG. 6-48-----	19, 20, FIG. 6-48-----	-4.5
Q3-----	19, 20, FIG. 6-48-----	0-----	5, 6, FIG. 6-48
Q4-----	3, 4, FIG. 6-48-----	3, 4, FIG. 6-48-----	-4.5
Q5-----	7, 8, FIG. 6-48-----	7, 8, FIG. 6-48-----	-4.5
Q6-----	9, 10, FIG. 6-48-----	9, 10, FIG. 6-48-----	-4.5
Q7-----	17, 18, FIG. 6-48-----	17, 18, FIG. 6-48-----	-4.5
Q8-----	17, 18, FIG. 6-48-----	11, 12, FIG. 6-48.	
Q9-----	8, FIG. 6-42-----		
	5, FIG. 6-64-----	0-----	21, 22, FIG. 6-48

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER unless instructed otherwise.
- (4) Pcm output terminated in 91-ohm load.
- (5) AUX switch at OUT.
- (6) 2 WIRE-4 WIRE switch at 4 WIRE.
- (7) Module terminal voltages are as follows:

Module	1	2	3	5	8	10	11
Z1-----	-2.4-----	-2.4-----	-2.1-----	-----	-----	15, fig. 6-48.	15, fig. 6-48.
Z2-----	-2.4-----	-2.4-----	15, fig. 6-48.	-2.1-----	-2.1 ^a -----	15, fig. 6-48.	15, fig. 6-48.
Z3-----	17, 18, fig. 6-48.	17, 18, fig. 6-48.	7, 8, fig. 6-48	-----	9, 10, fig. 6-48		

^a Measured at terminal 24.

4-9. Panel 1A5, Troubleshooting

a. Troubleshooting Chart. Modulate one channel using internal test tone.

Item No.	Symptom	Probable trouble	Correction
1	Simultaneous loss of all output signals (dead panel).	Q1, Q2, Q3, or Q4 defective ----	Check waveform at J2. If absent, check Q1 and Q2. If present, check Q3 and Q4.
2	No decision pulses output at terminal 9, but coder clock output at terminal 7 is present.	R34 defective -----	Check R34.
3	No coder clock output at terminal 7, but decision pulses output at terminal 9 is present.	Q5, Q5 or Q7 defective -----	Check waveform at J3. If absent, check Q5. If present, check Q6 and Q7.
4	Erroneous coder clock and decision pulses outputs.	DL1 defective -----	Check DL1.
5	Simultaneous loss of T1 through T6, T6B, compander control, and compander control output signals.	a. Z1 or CR5 defective ----- b. Q8, CR4, CR12, or CR13 defective.	a. Check waveform at emitter of Q8. IF present, check Z1 and CR5. If absent, proceed to b below. b. Check waveform at base of Q8. If present, check Q8. If absent, check CR4, CR12, and CR13.
6	Simultaneous loss of T1, T3 through T6, pcm compander control, and compander control outputs. (T2 at terminal 27 present.)	Z2 defective -----	Check Z2.
7	Simultaneous loss of T1, T4 through T6, T6B, compander control, and compander control outputs. (T2 at terminal 27 and T. at terminal 26 both present.)	Z3 defective -----	Check Z3.
8	Simultaneous loss of T1, T5, T6, T6B, compander control, and compander control outputs. (T2 T3, and T4 outputs at terminals .7. 26 and 25, respectively, all present.)	Z4 defective -----	Check Z4.
9	Simultaneous loss of T1, T6, pcm compander control, and compander control outputs. (T2 T3, T4, and A outputs at terminals 27, 26 25, and 24, respectively, all present.)	Z5 defective -----	Check Z5.
10	Loss of T1 output at terminal 22 only.	Z6 defective -----	Check Z6.
11	Simultaneous loss of T6B compander control outputs (terminals 19, 15, and 17, respectively). All other outputs present.	Q9 or Q10 defective -----	Check Q9 and Q10

Item No.	Symptom	Probable trouble	Correction
12	Simultaneous loss of <i>compander control</i> output at terminal 15 and <i>compander control</i> output at terminal 17. All other outputs present.	Z7 defective -----	Check Z7.
13	Loss of <i>compander control</i> output at terminal 15 only.	Q16 defective -----	Check Q16
14	Loss of <i>compander control</i> output at terminal 17 only.	Q15 defective -----	Check Q15.
15	Loss of both <i>compander control</i> output at terminal 17 and <i>compander control</i> output at terminal 15.	Q12 or Q11 defective -----	Check Q11 and Q12.
16	Loss of T6 output at terminal 23 only.	Q14 defective -----	Check Q14.
17	Loss of T2 output at terminal 27 only.	Q13 defective -----	Check Q13.

b. *Transistor Terminal Voltages.* The transistor terminal voltages given in the chart below were measured with respect to ground with the ME26B/U and the figure references are to waveform measurements with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1-----	-2.0-----	-1.7-----	-4.5
Q2-----	-1.6-----	-1.4-----	-4.5
Q3-----	+0.4-----	0-----	-2.4
Q4-----	+0.4-----	-2.1-----	-4.5
Q5-----	+0.9-----	+0.3-----	-3.5
Q6-----	+0.9-----	-3.5-----	-4.5
Q7-----	+0.9-----	-3.5-----	+4.5
Q8-----	19, fig. 6-50-----	20, fig. 6-50-----	-4.5
Q9-----	-0.03-----	0-----	-0.8
Q10-----	-0.03-----	-0.9-----	-4.5
Q11-----	18, fig. 6-50-----	-----	10, fig. 6-50
Q12-----	17, fig. 6-50-----	-----	9, fig. 6-50
Q13-----	-4.0-----	-3.6-----	-4.5
Q14-----	-4.0-----	-3.6-----	-4.5
Q15-----	18, fig. 6-50-----	10, fig. 6-50-----	+4.5
Q16-----	17, fig. 6-50-----	9, fig. 6-50-----	+4.5

c. *Module Terminal Voltages.* The module terminal voltages given in the chart below were measured with respect to ground with the ME26B/U and the figure references are to waveform measurements with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	2	3	10
Z1-----	-4.0-----	-----	-1.0
Z2-----	-4.0-----	-----	-1.0
Z3-----	-4.0-----	-----	-1.0
Z4-----	-4.0-----	-----	-1.0
Z5-----	-4.0-----	-----	-1.0
Z6-----	-4.0-----	-----	-1.0
Z7-----	17, FIG. 6-50	-0.9-----	18, fig. 6-50

4-10. Panel 2A5, Troubleshooting

a. Troubleshooting Chart. Loop-back and modulate the TD-352/U test unit

Item No.	Symptom	Probable trouble	Correction
1	No 8 kc aux output at terminal 18	Z7, Q5, Q6, or Q7 defective -----	Check waveform at base of Q7. If present, check Q7. If absent, check waveform at pin 10 of Z7. If still absent, check Z7. If present, check Q5 and Q6.
2	Simultaneous loss of $\overline{T6B}$ output at terminal 27, <i>compander control</i> output at terminal 23, and <i>compander control</i> output at 29.	Q1 or Q2 defective-----	Check Q1 and Q2
3	Loss of <i>compander control</i> output at terminal 23 and $\overline{\text{compander control}}$ output at terminal 29. (T6B output present.)	Z1, Q3, or Q4 defective -----	Check Z1, Q3, and Q4
4	No <i>compander control</i> output at terminal 23 only ($\overline{\text{compander control}}$ output present).	Q8 defective -----	Check Q8
5	No $\overline{\text{compander control}}$ output at terminal 29 (<i>compander control</i> output present).	Q9 defective -----	Check Q9
6	No <i>pcm A</i> or <i>pcm B</i> outputs at terminals 1 and 13, respectively.	a. Z4 defective ----- b. Z2, Z3, Z5, or Z6 defective	a. Check waveform at J4. If absent, check Z4. If present, proceed to <i>b</i> below b. Check waveform at J3. If absent, check Z6. If present, check Z2, Z3, and Z5.

b. *Transistor Terminal Voltages.* The transistor terminal voltages given in the chart below were measured with respect to ground with the ME- 26B/U and the figure references are to waveform measurements with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One Channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT
- (5) 2 WIRE-4 WIRE switch at A WIRE.
- (6) Terminal 18 terminated in 91-ohm load.
- (7) Transistor terminal volt are as follows:

Transistor	Base	Emitter	Collector
Q1-----	10, fig. 6-52 -----	10, fig. 6-52 -----	-4.5.
Q2-----	15, fig. 6-57 -----	0 -----	10, fig. 6-52.
Q3-----	11, fig. 6-52 -----	-----	9, fig. 6-52.
Q4-----	12, fig. 6-52 -----	-----	1, fig. 6-52.
Q5-----	19, fig. 6-52 -----	19, fig. 6-52 -----	-4.5.
Q6-----	19, fig. 6-52 -----	19, fig. 6-52 -----	-4.5.
Q7-----	19, fig. 6-52 -----	8, fig. 6-52 -----	
Q8-----	9, fig. 6-52 -----	9, fig. 6-52 -----	+4.5.
Q9 -----	1, fig. 6-52 -----	1, fig. 6-52 -----	+4.5.

c. *Module Terminal Voltages.* The module terminal voltages given in the chart below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Terminal 18 terminated in 91-ohm load.
- (7) Module terminal voltages area as follows:

Module	1	2	3	5	8	10	11
Z1 -----		11, fig. 6-52	10, fig. 6-52		18, fig. 6-57	12, fig. 6-52	
Z2 -----	5, fig. 6-52.	13, fig. 6-52.	18, fig. 6-60			14, fig. 6-52.	6, fig. 6-52.
Z3 -----	3, fig. 6-52	15, fig. 6-52	18, fig. 6-60	15, fig. 6-60	15, fig. 6-60	16, fig. 6-52	17, fig. 6-52
Z4 -----	5, fig. 6-52	3, fig. 6-52	13, fig. 6-64			17, fig. 6-52	6, fig. 6-52
Z5 -----	2, fig. 6-52	4, fig. 6-52	18, fig. 6-60	15, fig. 6-60	15, fig. 6-60	7, fig. 6-52	
Z6 -----	3, fig. 6-52	2, fig. 6-52	7, fig. 6-64			18, fig. 6-52	17, fig. 6-52
Z7 -----	5, fig. 6-64		4, fig. 6-64			15, fig. 6-52	9, fig. 6-64

4-11. Panel 1A6/2A6, Troubleshooting

a. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
1	No. FF9- 1 OR pcm A activity at terminal 2 (signal always at 0 volt or -4.3 volts).	Analog section , a. Q1, Q2, or Q3 defective b. Q6, Q7, or Q8 defective.	Modulate one channel using internal 1100 cps test tone. a. Check waveform et J5. If correct, check Q1, Q2, and Q3. If incorrect, proceed to b below. b. Check waveform at J2. If correct, check Q6, Q7, and Q8. If incorrect, proceed to c below.

Note. At the end of each coding cycle the network is reset to code level 100000 by the T6 and coder clock gate signals and the information given in the correction column is based on these conditions. Use a dual-trace oscilloscope, displaying the T6 signal as a reference on one trace and the signal under investigation on the other trace. Check the signal level when the trailing edge of the T6 pulse occurs. The idealized waveforms and timing relationships for the signals concerned are shown in figure 2-29.

		<i>Ladder Network</i>	
		c. Z3 defective	c. Check waveform at J5. If level is 0 volt, proceed to d below; if not, check Z3.
		d. Q13, Q14 , CR36, CR37, Q18, or Q19 defective.	d. Check at J7. If level is -5.0 volts, proceed to e below; if not, check waveform at J14. If level of signal at J14 is 0 volt, check Q13 and Q14 ; if not, check CR36, CR37, C18, and C19,
		e. Z4 defective	e. Check waveform at J8. If level is -5.0 volts, proceed to f below; if not, check Z4.
		f. Z5 defective	f. Check waveform at J9. If level is 6.0 volts, proceed to g below.
		g. Z6 defective	g. Check waveform at J10. If level is -5.0 volts, proceed to h below; if not, check Z6
		h. Q21 or Q22 defective	h. Check waveform at J17. If level 0 volt, proceed to i below; if not, check Q21 and Q22.
		i. CR39, CR40, or Q20 defective.	i. See that when cathode of CR39 goes to 0 volt, pulses in the coder clock signal at J16 are coincident with coder clock pulses appearing at terminal 9; if not, check CR39, CR40, and Q20. If signal at J16 is correct, proceed to j below.
		4-18	

a. Troubleshooting Chart-continued

Item No.	Symptom	Probable trouble	Correction
		<p>j. Q12 or VR2 defective</p> <p><i>Amplifier-attenuator and compandor control circuits</i></p> <p>k. CR14, CR15, or CR17 defective.</p> <p>l. CR12, CR13, or CR18 defective.</p> <p>m. CR7, CR8, or CR18 defective.</p> <p>n. CR9, CR10, or CR19 defective.</p>	<p>j. Check waveform at base of Q12. If erroneous, check Q12. If correct, check cathode of VR2, which should be 8 volts positive with respect to emitter of Q12; if not, check VR2. If both Q12 and VR2 check good, proceed to k below.</p> <p>Remove modulation and-</p> <p>k. Check waveform at J3. If correct, proceed to o below. If erroneous, check voltage at junction of CR14, CR15, and CR17 which should be about +3.5 volts; if not, check CR14, CR15, and CR17. If voltage is correct, proceed to l below.</p> <p>l. Check voltage at junction of CR12, CR13 and CR18 which should be about -4.9 volts; if not, check CR12, CR13, and CR18. If voltage is correct, proceed to m below.</p> <p>m. Check signal at junction of CR7, CR8 and CR18 which should be similar to that of J3 except that it is shifted 0.8 volt in a positive direction; if not, check CR7, CR8, and CR18. If signal information correct, proceed to n below.</p> <p>n. Check signal at junction of CR9, CR10, and CR19 which should be similar to that of J3 except that it is shifted 0.8 volt in a negative direction; if not, check CR9, CR10, and CR19.</p>

a. Troubleshooting Chart-Continued

Item No.	Symptom	Probable trouble	Correction
		<p><i>Amplifier-attenuator and compandor control circuits-Continued</i></p> <p>o. Q15, Q16, Q17, or CR 30 through CR 35 defective.</p> <p><i>Decision circuit</i></p> <p>p. Z2 defective</p> <p>q. Q9, Q10, or Q11 defective</p> <p>r. Q4, Q5, CR4, CR5, CR6, or Z1 - defective.</p>	<p>Reapply modulation and-</p> <p>o. Check waveform at emitter of Q17, which should be similar to wave form of J8 except that it is shifted 0.3 volt in a positive direction. If incorrect, check Q17. If correct, check CR30 through CR35, Q15 and Q18. If these diodes and transistors check good, proceed with <i>p</i> below.</p> <p>p. Check waveforms on pins 4 and 5 of Z1. If pulses are being presented to both pins, check Z2. If pulses are being presented to pin 4 or 5 only, proceed to <i>q</i> below. If there are no pulses at either pin 4 or 6, proceed to <i>r</i> below.</p> <p>i. Check waveform at J4 which should be similar to that of J3 except that it is shifted 0.8 volt in a negative direction; if not, check Q9. If correct check Q10 and Q11</p> <p>r. Check waveform at pin 3 of Z1. If incorrect, check Q4, Q6, CR4, CR5, and CR8. If correct, check Z1.</p>

Note. To observe the following symptoms modulate one channel of the test multiplexer; use the internal 1,100-cps test tone and monitor the pcm output signal by connecting an oscilloscope to the front panel PCM OUT connector. Synchronize the oscilloscope, from the 8-kc SCOPE SYNC output of the multiplexer. The sequence of digits, from the lsd to the led information (7) follows:

2	No lsd activity (digit 0)	Q21 or Q22 defective	Check waveform at J17. If absent, check Q21 and Q22.
3	No activity, digit 6	Z. or CR29 defective	Check waveform at pin 3 of Z6. If correct, check Z6. If incorrect, check CR29.

a. Troubleshooting Chart- Continued

Item No.	Symptom	Probable trouble	Correction
4	No activity, digit 4	Z5 or CR27 defective	Check waveform at pin 3 of Z5. If correct, check Z5. E incorrect, check CR27.
5	No activity, digit 3	Z4 or CR25 defective	Check waveform at pin 3 of Z4. If correct, check Z4. If incorrect, check CR25
6	No activity, digit 2	Q13, Q14 , Q18, Q19, CR36, or CR37 defective	Check waveform at J14. If correct, check Q13 and Q14 . If incorrect, Q18, Q18, Q19, and CR37.
7	No msd activity (digit 1)	Z3 defective	Check Z3.
8	Levels is 0 through 15 and 48 through 63 missing or incorrect in palm out signal	<p>a. Attenuator circuit defective</p> <p>b. Amplifier-attenuator control circuit defective.</p> <p>c. Compandor control. - circuit defective.</p>	<p>a. Check waveform at J2. If in check attenuator circuit as given in item l b above. If proceed to b below.</p> <p>b. check amplifier-attenuator circuit as given in items 1 k and 1/ above. If circuit checks good, proceed to c below.</p> <p>c. Check compandor control circuit as given in item 1 o.</p>
9	Levels 16 and 17 missing or incorrect in pcm out signal	<p>a. Amplifier circuit defective</p> <p>b. Amplifier-attenuator control circuit de-defective</p>	<p>a. Check waveform at J5. E in check amplifier circuit given in item la above. If correct, proceed to b below.</p> <p>b. Check amplifier-attenuator control circuit as given in items 1m and above.</p>
10	Transitions between 15 and 16, or 47 ant 48 missing from pcm out signal.	Panel misaligned	Perform alignment of compressor adjust control R26 as given in chapter 3
11	Any level missing other than those given in items 8, 9, and 10.	Clamping flip-flop circuits defective.	See that waveforms at J5 through J10 and J17 are clamped to -5.2 volts and ground; if not, check respective clamping circuits.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1 ^a			
Q2	34, 40, fig. 6-54		9, 10, fig. 6-54.
Q3	8, 10, fig. 6-54	9, 10, fig. 6-54	+ 10.0.
Q4	48 channel: -2.1 12 channel: 13 fig. 6-60.	45, 40, fig. 6-54	43, 44, fig. 6-54.
Q5	48 channel: +0.3 12 channel: +0.7.	45, 46, fig. 6-54	47, 48, fig. 6-54.

^a Q1: Pin 1: 39, 40, fig. 6-54.
Pin. 2: 0v.
Pin 6: 1, fig. 6-27; 21, fig. 6-57.
Pin 7: 41, 42, fig. 6-54.

c. *Module Terminal Voltages.*

Module	1	2	3	4	5	6	7	8	10	11
Z1 -----	51, 52, fig. 6-54.	56, 56, fig. 6-54.	47, 48, fig. 6-54.	65, 66, fig. 6-54.	65, 66, fig. 6-54.					
Z2 -----		37, 38, fig. 6-54.	65, 66, fig. 6-54.					65, 66, fig. 6-54.	29, 30, fig. 6-54.	
Z3 -----				25, 26, fig. 6-54.		21, 22, fig. 6-54.	11, 12, fig. 6-54.			See note 1 below
Z4 -----			See note 1 below	See note 2 below			15, 16, fig. 6-54.			See note 3 below
Z5 -----			See note 1 below	See note 4 below			17, 18, fig. 6-54.			See note 5 below
Z6 -----			See note 1 below	See note 6 below			37, 38, fig. 6-54.			See note 7 below

Notes

1. Check T6 and coder clock waveforms at terminals 14 and 9. If both are present and correct, input to pin 11 of Z3 and pin 3 of Z4, Z5, and Z6 can be considered correct.
2. Check T3 waveform at terminal 12 and waveform at emitter of Q20. If both are present and correct, input to pin 4 of Z4 can be considered correct.
3. Check T2 and coder clock waveform at terminals 11 and 9. If both are present and correct, input to pin 11 of Z4 can be considered correct.
4. Check T4 waveform at terminal 13 and waveform at emitter of Q20. If both are present and correct, input to pin 4 of Z5 can be considered correct.
5. Check T3 and coder clock waveforms at terminals 12 and 9. If both are present and correct, input to pin 11 of Z5 can be considered correct.
6. Check T5 waveform at terminal 16 and waveform at emitter Q20. If both are present and correct, input to pin 4 of Z6 can be considered correct.
7. Check T4 and coder clock waveforms at terminals 13 and 9. If both are present and correct, input to pin 11 of Z6 can be considered correct.

4-12. Panel 1A7, Troubleshooting

a. *Troubleshooting Chart.* Loop-back the TD-353/U test unit, and use the internal test tone to modulate odd or even channels in accordance with the symptoms described. In addition to the troubles listed, this panel can be a potential source of noise in the multiplexer system, which may be induced back into the voltage supply lines through the various stages. If the panel has been rejected because it is causing noise in the system, check all filtering components in the collector or emitter circuits of the applicable stages.

Item No.	Symptom	Probable trouble	Correction
1	No <i>noise gen mon</i> output at terminal 23.	CR11 or R37 defective	Check CR11 and R37.
2	No <i>coder pam</i> output at terminal 22 with modulation applied to both odd and even channels.	Q17, VR3, or Q18 defective	Check Q17 (specifically C31), VR3, and Q18.
3	No <i>coder pam</i> output at terminal 22 with modulation applied to even channels, but output is present with modulation applied to odd channels	<p>a. Q10 defective</p> <p>b. Q5, Q6, or Q7 defective</p> <p>c. Q4 defective</p> <p>d. Q2 or Q3 defective</p> <p>e. Q1 defective</p> <p>f. Q8, T1, CR1, CR2, , CR3 or CR4 defective.</p>	<p>a. Check waveform at J2. If present, check Q10. If absent, proceed to <i>b</i> below.</p> <p>b. Check waveform at base of Q5. If present, check Q5. If absent, check Q6 and Q7. If Q5 is good, proceed to <i>c</i> below.</p> <p>c. Check waveform at base of Q4. If present, check Q4. If absent, proceed to <i>d</i> below.</p> <p>d. Check waveform at base of Q2. If present, check Q2 and Q3. If absent, proceed to <i>e</i> below.</p> <p>e. Check waveform at emitter of Q1. If absent, check Q1. If present, proceed to <i>f</i> below.</p> <p>f. Check waveform at emitter of Q8. If absent, check Q8. If present, check T1 and CR1 through CR4.</p>

Item No.	Symptom	Probable trouble	Correction
4	No <i>coder pam</i> output at terminal 22 with modulation applied to odd channels, but output is present with modulation applied to even channels.	<p>a. Q22 defective</p> <p>b. Q15, Q16, or Q19 defective</p> <p>c. Q14 defective</p> <p>d. Q12 or Q13 defective</p> <p>e. Q11 defective</p> <p>f. Q20, T2, CR12, CR13, CR14, or CR15 defective.</p>	<p>a. Check waveform at J3. If present, check Q22. If absent, proceed to <i>b</i> below.</p> <p>b. Check waveform at base of Q15. If present, check Q15. If absent, check Q16 and Q19. If Q15 is good, proceed to <i>c</i> below.</p> <p>c. Check waveform at base of Q14. If present, check Q14. If absent, proceed to <i>d</i> below.</p> <p>d. Check waveform at base of Q12. If present, check Q12 and Q13. If absent, proceed to <i>e</i> below.</p> <p>e. Check waveform at emitter of Q11. If absent, check Q11. If present, proceed to <i>f</i> below.</p> <p>f. Check waveform at emitter of Q20. If absent, check Q20. If present, check T1 and CR12 through CR15.</p>
5	Demodulated output of multiplexer odd and even channels distorted using this panel.	R30 (even chan level adj) out of adjustment.	Check R30. Perform pam level adjustment.
6	<i>Coder pam</i> output of multiplexer even channels distorted.	Q9, R24 through R27, VR1, CR9, or CR10. defective	Check Q9, R24 through R27, VR1, CR9, and CR10.
7	<i>Coder pam</i> output of multiplexer odd channels distorted.	Q21, R67 through R70, VR2, CR20 or CR21. defective	Check Q21, R67 through R70, VR2, CR20, and CR21.
8	No <i>coder pam mon</i> output at terminal 26.	R61 defective	Check R61.
4-25			

b. *Transistor Terminal Voltages.*

(1) The transistor terminal voltages listed in (2) below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements with the oscilloscope under the following conditions:

- (a) Test multiplexer connected for loop back operation.
- (b) One channel modulated with internal 1,100-cps test tone.
- (c) ADDRESS switch at MASTER.
- (d) AUX switch at OUT.
- (e) 2 WIRE-4 WIRE switch at 4 WIRE.

(2) The transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector	Transistor	Base	Emitter	Collector
Q1 -----	4, fig. 6-27-	-0.75-----	+3.3.	Q12 -----	-0.75-----	-1.3 -----	+4.5.
Q2 -----	-0.75-----	-1.3 -----	+4.5.	Q13 -----	-1.3 -----	-2.0 -----	+4.4.
Q3 -----	-1.3-----	-2.0 -----	+4.4.	Q14 -----	-2.0 -----	-3.0 -----	-6.2.
Q4 -----	-2.0-----	-3.0 -----	-5.2.	Q15 -----	-0.4 -----	-3.0 -----	-5.2.
Q5 -----	-0.4-----	-3.0 -----	-5.2.	Q16 -----	+4.3 -----	+4.3-----	-0.4.
Q6 -----	+4.3-----	+4.3-----	-0.4.	Q17 ^a -----			
Q7 -----	-2.4-----	-2.1 -----	-4.5.	Q18 -----	+0.7 -----	1, fig. 6-27	+4.2.
Q8 -----	+1.9-----	-2.1 -----	0.	Q19 -----	-2.4 -----	-2.1 -----	-4.5.
Q9 -----	-1.9-----	+1.6-----	-4. 5.	Q20 -----	+1.9 -----	+2.1 4-----	0.
Q10-----	-0.2-----	+0.5-----	+6.9.	Q21 -----	-1.9 -----	-1.6 -----	-4.5.
Q11-----	4, fig. 6-27-	-0.75-----	+3.3.	Q22 -----	-0.2 -----	+0.5-----	+6.9.

^a Q17: Pin 1: +10
 Pin 2: 0
 Pin 3: .7
 Pin 5: .7
 Pin 6: 0
 Pin 7: +6.7

4-13. Panel 2A7, Troubleshooting

a. *Troubleshooting Chart.* Loop back the TD-352/U test unit and modulate one channel: use the internal test tone.

Item No.	Symptom	Probable trouble	Correction
1	No <i>coder clock</i> output at terminal 18.	a. Q3 or Q4 defective b. Q2 or Q1 defective	a. Check waveform at collector of Q2. If present, check Q3 and Q4. If absent, proceed to b below. b. Check waveform at emitter of Q1. If present, check Q2. If absent, check Q1.
2	No <i>FF5B</i> output at terminal 16.	Q20 or Q21 defective	Check Q20 and Q21.

Item No.	Symptom	Probable trouble	Correction
3	<i>T1</i> through <i>T6</i> outputs at terminals 9, 4, 6, 7, 8, and 14, respectively, simultaneously lost or erroneous.	Z1, Z2, or Z3 defective	Check output at pins 2 and 10 of Z1, Z2, and Z3.
4	No <i>T1</i> output at terminal 9 only.	Q7, Q8, or CR7 through CR10 defective.	Check waveform at J4. If present, check Q7 and Q8. If absent, check CR7 through CR10
5	No <i>T2</i> output at terminal 4 only.	Q5, Q6, or CR3 through CR6 defective.	Check waveform at J8. If present, check Q5 and Q6. If absent, check CR3 through CR6.
6	No <i>T3</i> output at terminal 6 only.	Q10, Q11 or CR13 through CR16 defective.	Check waveform at J6. If present, check Q10 and Q11. If absent, check CR13 through CR16.
7	No <i>T4</i> output at terminal 7 only.	Q12, Q13, or CR20 through CR23. defective.	Check waveform at J10. If present, check Q12 and Q13. If absent, check CR20 through CR23.
8	No <i>T5</i> output at terminal 8 only.	Q14, Q15, or CR26 through CR29. defective.	Check waveform at J5. If present, check Q14 and Q15. If absent, check CR26 through CR29.
9	No. <i>T6</i> output at terminal 14 only.	Q17, Q18, or CR30 through CR33. defective.	Check waveform at J3. If present, check Q17 and Q18. If absent, check CR30 through CR33.
10	No <i>T1'</i> output at terminal 15 only.	CR17, CR15 or Q9 defective.	Check signal at base of Q9. If absent, check CR17 and CR18. If present, check Q9.
11	No <i>T6'</i> output at terminal 14 only.	CR34, CR35, or Q16 defective.	Check signal at base of Q16. If absent, check CR34 and CR35. If present, check Q16.
12	No <i>noise gen mon</i> output at terminal 21.	CR49 or R73 defective	Check CR49 and R73.
13	No, or incorrect, <i>coder pam</i> output at terminal 31.	a. Q28, VR2, or Q24, - defective.	a. Check waveform at J9. If present, check Q28, VR2, and Q24, If absent, proceed to <i>b</i> below.

Item No.	Symptom	Probable trouble	Correction
		<p>b. Q25 or Q26 defective</p> <p>c. Q24, defective</p> <p>d. T1, C33, or CR43 through CR46. defective.</p> <p>e. Q22 or Q23 defective</p> <p>f. CR12, CR26, CR39, CR36, Q19, CR40, or CR41 defective.</p>	<p>b. Check waveform at base of Q25. If present, check Q25 and Q26. If absent, proceed to c below.</p> <p>c. Check waveform at emitter of Q24,. If absent, check Q24, If present, proceed to d below.</p> <p>d. Check waveform at J1. E present, check T1, C33, and CR43 through CR46. If absent, proceed to e below.</p> <p>e. Check waveform at base of Q23. If present, check Q23.-If absent, check Q22. If Q22 checks good, proceed with f below.</p> <p>f. Check signal at base of Q19. If absent, check CR12, CR25, CR39, and CR38, If present, check Q19, CR40, and CR41.</p>
14	Erroneous <i>coder pam</i> output at terminal 31.	Q27, R62 through R65, VR1, CR47, or CR48 Defective	Check Q27, R62 through R65, VR1, CR47, and CR48.
15	No <i>coder pam mon</i> output at terminal 28.	R78 defective	Check R78.

b. *Transistor Terminal Voltages*

(1) The transistor terminal voltages listed in (2) below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements using the oscilloscope under the following conditions:

- (a) Test multiplexer connected for loopback operation.
- (b) One channel modulated with internal 1,100-cps test tone.
- (c) ADDRESS switch at MASTER.
- (d) AUX switch at OUT.
- (e) 2 WIRE-4 WIRE switch at 4 WIRE.

(2) The transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1	-0.9	-0.6	-4.5.
Q2	-0.6		18, fig. 6-57.
Q3	18, fig. 6-57	18, fig. 6-57	+4.5.
Q4	18, fig. 6-57	18, fig. 6-57	-4.5.
Q5	-0.9 ^a	0	10, fig. 6-57.
Q6	10, fig. 6-57	10, fig. 6-57	-4.5.
Q7	-0.9 ^b	0	14, fig. 6-57.
Q8	14, fig. 6-57	14, fig. 6-57	-4.5.
Q9	16, fig. 6-57	16, fig. 6-57	+4.5.
Q10	0.9 ^c	0	11, fig. 6-57.
Q11	11, fig. 6-57	11, fig. 6-57	-4.5.
Q12	-0.9 ^d	0	12, fig. 6-57.
Q13	12, 6-57	12, fig. 6-57	-4.5.
Q14	-0.9 ^e	0	13, fig. 6-57
Q15	13, fig. 6-57	13, fig. 6-57	-4.5.
Q16	19, fig. 6-57	19, fig. 6-57	+4.5.
Q17	-0.9 ^f	0	15, fig. 6-57.
Q18	15, fig. 6-57	15, fig. 6-57	-4.5.
Q19		-4.5	-0.3
Q20	-2.4	-2.6	-4.5.
Q21	-2.4	-2.6	0.
Q22	-2.6	-2.3	-4.5.
Q23	+1.2	+1.5	0.
Q24	0	+0.3	-3.3.
Q25	+0.3	-0.3	+4.5.
Q26	-0.3	-1.0	-4.3.
Q27	-0.7	-0.4	-4.5.
Q28 ^g			
Q29	+0.7	0	+9.2.

^a Measure at J8.

^b Measure at J4.

^c Measure at J6

^d Measure at J10.

^e Measure at J5.

^f Measure at J3.

^g Q28: Pin 1: +10

Pin 2: 0.

Pin 3: -0.07.

Pin 4: -0.07.

Pin 5: 0.

Pin 6: +6.7.

c. Voltage Regulator VR1 Voltages

(1) Anode: -3.1.

(2) Cathode: +3.2.

d. Module Terminal Voltages.

(1) The module terminal voltages listed in (2) below were measured with respect to ground with the ME-26B/U under the following conditions:

(a) Test multiplexer connected for loopback operation.

(b) One channel modulated with internal 1,100 cps test tone.

(c) ADDRESS switch at MASTER.

(d) AUX switch at OUT.

(e) 2 WIRE-4 WIRE switch at 4 WIRE.

(2) The module terminal voltages are as follows:

Module	2	8	10
Z1-----	2. 4	See note 1 below	-2. 4
Z2-----	2. 4	See note 2 below	-2. 4
Z3-----	2. 4	See note 3 below	-2. 4

Notes

1. Measure at terminal 12 of panel:-2.4.
2. Measure at terminal 11 of panel:-2.4.
3. Measure at terminal 10 of panel:-2.4.

4-14. Panel 1A8, Troubleshooting

a. *Troubleshooting Chart.* There are two categories of faults within panel 1A8. The first is loss of, or erroneous, timing output signals that occurred when the panel was used in a TD-353/U operated as a simple 48-channel terminal or in a TD-353/U operated as a master unit in a larger terminal. The second category is synchronization troubles that were evident when the panel was used in a TD-353/U operated as a slave unit. Items 1 through 13 in the troubleshooting chart below localize faults in the first category. Items 14 and 15 are concerned with synchronization faults. Since a panel used in a slave unit may also have timing signal generator circuit troubles, be sure that symptoms 1 through 13 are not present before proceeding to localize any synchronization faults.

Item No.	Symptom	Probable trouble	Correction
	1 Dead panel (loss of all timing output signals including reset clock at terminal 17).	Z1, Q1, Q2, or Z2 defective	<p>a. First try injecting the SYNC OUT XMTR output of a second TD-353/U test unit into SYNC IN input of the TD-353/U in which this panel is being checked.</p> <p>b. If any or all output signals are restored, disconnect external sync in signal to test unit and check Z1, Q1, and Q2.</p> <p>c. If panel is still dead with external SYNC IN signal applied, check sync in monitor waveform at terminal 19. If present, check Z2.</p> <p>d. If sync in monitor signal is absent (and monitor signal clamping circuit CR4, R9 checks good) and sync in circuitry Q3 through Q6 is defective, proceed to item 14. (In this case, corrections a through c above are void and the 2,304-kc</p>

Item No.	Symptom	Probable trouble	Correction
2	Loss of a timing output signals except reset clock at terminal 17.	Q7, Q8, DL1, Q9, or Z3 defective.	master oscillator signal must be traced from Z1 to the output of Z2, stage-by-stage.) Trace 2,304-kc master oscillator signal from input of Q7 to output of Z3, stage-by-stage
3	Loss of reset clock output at terminal 17 only.	Q12 defective	Check Q12.
4	Loss of reshaped clock output at terminal 13 only.	Q11 defective	Check Q11
5	Simultaneous loss of <i>sync out xmtr</i> output at terminal 31, <i>timing out</i> output at terminal 11, and <i>sampling clock</i> output at terminal 26	Q10 or Z4 defective	Check Q10 and Z4.
6	No <i>sync out xmtr</i> output at terminal 31 only.	Q16 defective	Check Q16.
7	No <i>timing out</i> output at terminal 11.	Q15 defective	Check Q15.
8	No <i>sampling clock</i> output at terminal 26.	Q13 or Q14 defective	Check Q13 and Q14 .
9	Simultaneous loss of $\overline{P1}$ output at terminal 25, $\overline{FF2B}$ <i>xmtr</i> output at terminal 10 and $\overline{FF3B}$ <i>xmtr</i> output at terminal 5.	Z7 or Z8 defective	Check waveform at J3. If absent check Q17, then Z7. If present, check Z6
10	No $\overline{P1}$ output at terminal 25 only ($\overline{FF2B}$ <i>xmtr</i> and $\overline{FF3B}$ <i>xmtr</i> good).	Z6 defective	Check Z6.
11	No $\overline{FF2B}$ <i>xmtr</i> output at terminal 10 of ($\overline{P1}$ and $\overline{FF3B}$ <i>xmtr</i> good).	Q19 defective	Check Q19.
12	No $\overline{FF3B}$ <i>xmtr</i> output at terminal 5 only ($\overline{P1}$ and $\overline{FF2B}$ <i>xmtr</i> good).	Q20 or Z. defective	Check Q20 and Z9.

Item No.	Symptom	Probable trouble	Correction
13	Erroneous $\overline{FF2B}$ xmtr signal at terminal 10 (576 kc) and $FF3B$ xmtr signal at terminal 5 (288 kc).	Q18 or Z10 defective	Check Q18 and Z10.
<p><i>Note.</i> An external 2,304-kc signal is required to complete the remaining troubleshooting procedures for panel 1A8. Obtain this signal from the SYNC OUT XMTR output of a second TD-353/U test unit. Also, you must simultaneously monitor the SYNC IN input signal (terminal 29) and one of the timing output signals of the panel on a dual-channel oscilloscope. The <i>reset clock</i> output (terminal 17) is recommended as the output signal to monitor because it has a 2,304-kc pulse repetition rate. Synchronize the oscilloscope; use the SCOPE SYNC output of the second TD-353/U test unit.</p>			
14	Timing output signals drifting with respect to phase of <i>sync in</i> signal at terminal 29.	Sync in input circuit inoperative.	Check CR5, Q5, and Q6, in that order.
15	Incorrect frequency of <i>reset clock</i> output signal at terminal 17.	CR3, Q3, and/or Q4 - defective. (Q2 not cut off and both master oscillator and <i>sync in</i> signal are driving timing circuits.)	Check <i>sync in monitor</i> signal at terminal 19. If present, check Q3 and CR3. If absent, first check CR4 and R9 (monitor signal clamping circuit). If this circuit is good, check Q4.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector	Transistor	Base	Emitter	Collector
Q1 -----	+3.6 -----	+3.8 -----	+2.3.	Q11 -----	-2.3 -----	-2.0 -----	-4.5.
Q2 -----	+2.3 -----	+1.9 -----	-4.5.	Q12 -----	-3.3 -----	-3.2 -----	-4.5.
Q3 ^a -----	-4.1 -----	-4.5 -----	-4.3.	Q13 -----	-3.3 -----	-3.1 -----	+4.5.
Q4 ^a -----	+1.4 -----	-0.1 -----	-4.5.	Q14 -----	-3.3 -----	-3.1 -----	-4.5.
Q5 ^a -----	+1.5 -----	+1.4 -----	-4.5.	Q15 ^b -----	-1.8 -----	-1.6 -----	-2.6.
Q6 ^a -----	+4.2 -----	+4.5 -----	+1.4.	Q16 ^c -----	-1.7 -----	-1.6 -----	-2.6.
Q7 -----	-3.3 -----	-3.1 -----	-4.5.	Q17 -----	-1.5 -----	-1.2 -----	-4.5.
Q8 -----	+4.5 -----	+3.6 -----	10, fig. 6-28.	Q18 -----	-1.7 -----	-1.3 -----	-4.5.
Q9 -----	10, fig. 6-28.	10, fig. 6-28---	-4.5.	Q19 -----	1, fig. 6-28. -	-1.5 -----	-4.5.
Q10 -----	-2.3 -----	-1.9 -----	-4.5.	Q20 -----	-33 -----	-1.4 -----	-4.5.

^a Checked with sync in input of test multiplexer obtained from sync out xmtr output of second test multiplexer. Oscilloscope synchronized from SYNC OUT connector of second test multiplexer.

^b Terminal 11 terminated in 91 ohm load.

^c Terminal 31 terminated in 91 ohm load.

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements with the AN/USM-140 under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	2	4	5	7	8	9	10
Z1 -----			-2.9 -----			4.4 -----	
Z2 -----	+2.1 -----				-3.5 -----	-3.3 -----	
Z3 -----	2.4 -----						-2.3
Z4 -----	1.9 -----				3.6 -----	-3.3 -----	
Z6 -----	-2.3 -----	fig. 7, 6-28			-1.2 -----	-1.5 -----	-1.5.
Z7 -----	1.5 -----						1.7.
Z6 -----	1.7 -----						1, fig. 6-28.
Z9 -----	1.8 -----						1.8.
Z10 -----	-1.7 -----		-1.3 -----	-1.5 -----			-1.2.

4-15. Panel 2A8, Troubleshooting

a. *Troubleshooting Chart.* There are two categories of faults within panel 2A8. The first is loss of, or erroneous, timing output signals that occurred when the panel was used in a TD-352/U operated as a simple 12-channel terminal or in a TD-352/U operated as a master unit in a larger terminal. The second category is synchronization troubles that were evident when the panel was used in a TD-352/U operated as a slave unit. Items 1 through 16 in the troubleshooting chart below localize faults in the first category. Items 17 through 19 are concerned with synchronization faults. Since a panel used in a slave unit may also have timing signal generator circuit troubles, be sure that symptoms 1 through 16 are not present before proceeding to localize any synchronization faults.

Item No.	Symptom	Probable trouble	Correction
1	Dead panel (simultaneous loss of all output signals).	Q1, Q2, Q3, Q4, Q24, Q30, or Z1 defective.	Check waveform at J8. If present, check Q29, Q30, and Z1. If absent, or erroneous, check Q1, Q2, and Q3.
2	Loss of $\overline{TFF1}$ output at terminal 20 only.	Q12 defective	Check Q12.
3	No <i>coder decision</i> output at terminal 22.	Q27 and Q28 defective	Check Q27 and Q28.
4	Loss of $TFF1$ output at terminal 1 only.	Q16 or Q25 defective	Check for presence of T-pulse clock waveform at terminal 4. If present, check Q25. If absent, check Q16.
5	No, or erroneous, <i>T-pulse clock</i> output at terminal 4.	Q17, DL2, or Q18 defective	If no waveform, check Q17 and Q18. If erroneous waveform, check DL2.
6	Simultaneous loss of $TFF2$ (terminal 2), $\overline{TFF2}$ (terminal 19), $TFF3$ (terminal 23), and $\overline{TFF3}$ (terminal 21) outputs.	Z2 defective	Check Z2.
7	Loss of $\overline{TFF2}$ output at terminal 19 only.	Q7 defective	Check Q7.
8	Loss of $TFF2$ output at terminal 2 only.	Q8 defective	Check Q8.
9	Simultaneous loss of $\overline{TFF3}$ (terminal 23) and $TFF3$ (terminal 21) outputs.	Z3 defective	Check Z3.
10	Erroneous $TFF3$ and $\overline{TFF3}$ outputs (288-kc signals).	Z6 defective	Check Z6.
11	No $TFF3$ output at terminal 23 only.	Q5 defective	Check Q5.
12	No $\overline{TFF3}$ output at terminal 21 only.	Q6 defective	Check Q6.
13	No <i>modem timing</i> output at terminal 28 (J10).	Z9 or Q26 defective	Check Z9 or Q26.
14	No $FF12$ output at terminal 31 (J5).	Z7 defective	Check Z7.
15	No <i>parallel shift</i> output at terminal 30.	Z6, Q21, Q22, Q23, or Q24 defective.	Check waveform at J4. If present, check Q23 and Q24. If absent, check waveform at J4. If signal is present at this point, check Q21 and Q22; if absent, check Z6.

Item No.	Symptom	Probable trouble	Correction
16	No shift 2 output at terminal 24.	Q19 or Q20 defective	Check Q19 and Q20.
<p><i>Note.</i> An external 576-kc SYNC IN signal is required to complete the remaining troubleshooting procedures for panel 2A8. Obtain this signal from the SYNC OUT XMTR output of a second TD-352/U test unit. Also, simultaneously monitor in <i>sync in</i> input signal (terminal 17) and the selected timing output signal of the panel on a dual-channel oscilloscope. <i>TFF2</i>, at terminal 2, is recommended as the output signal to monitor since it has a pulse repetition rate of 576 kc. Synchronize the oscilloscope; use the SCOPE SYNC output of the second TD-352/U test unit.</p>			
17	Timing output signals (<i>TFF2</i>) drift with respect to external <i>sync in</i> input signal at terminal 17.	Master oscillator feedback loop not inhibited by <i>sync in</i> input circuitry. Master oscillator not being excited by <i>sync in</i> signal.	Check waveform at J3. If present, check Q11, Q3, CR1, and CR3. If absent, check Q10 and Z4. If Q10 and Z4 are good, check Q9 and CR2.
18	Timing output signals out of phase with respect to external terminal <i>sync in</i> input signal at terminal 17.	Delayed <i>sync in</i> signal circuit defective	Check waveform at J1. If absent, check back through Q15, CR5, CR7, Q14, DL1, and Q13. If present, check waveforms at J6. If this waveform is absent, check Z5 and CR8; if present and only <i>TFF1</i> is out of phase, check CR9 and CR10. Also, check CR11 and CR12.
19	No <i>sync in monitor</i> output at terminal 27.	Defective <i>sync in</i> signal detector circuit.	Check CR4 and CR6.
<hr/>			

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the 4-26B/U and the figure references are to waveform measurements with the AN/USM-140 under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Translator	Base	Emitter	Collector
Q1-----	+3.6-----	+3.4-----	-2.7.
Q2-----	-2.7-----	-3.2-----	-4.5.
Q3-----	-6.4-----	-4.5-----	-2.8.
Q3 ^a -----	-3.7-----	-4.5-----	-4.2.
Q4-----	+1.5-----	0-----	-4.5.
Q5-----	14, fig. 6-60-----	-1.6-----	-4.5.
Q6-----	12, fig. 6 00-----	-1.6-----	-4.5.
Q7-----	-18 4-----	-1.5-----	-4.5.
Q8-----	-1.8-----	-1.5-----	-4.5.
Q9 ^a -----	24, fig. 6-60-----	24, fig. 6-60-----	-4.5.
Q10 ^a -----	2, fig. 6-60-----	2, fig. 6-60-----	-4.5.
Q11 ^a -----	20, fig. 0-00-----	20, fig. 6-60-----	-4.5.
Q12 ^a -----	-1.7-----	-1.5-----	-4.5.
Q13 ^a -----	2, fig. 6-00-----	2, fig. 6-60-----	-4.5.
Q14 ^a -----	21, fig. 4--00-----	21, fig. 6-60-----	-4.5.
Q15 ^a -----	22, fig. 0-80-----	0-----	1, fig. 6-60.
Q16-----	-1.5-----	-1.2-----	-4.5
Q17-----	-1.2-----	-1.2-----	-4.5
Q18-----	-1.8-----	-0.9-----	-4.5
Q14-----	3, fig. 6-60-----	3, fig. 6-60-----	-4.6
Q20-----	-1.7-----	-3.1-----	15, fig. 6-60.
Q21-----	-3.2-----	-3.8-----	5, fig. 0-00.
Q22-----	3, fig. 6-60-----	5, fig. 6-60-----	-4.5.
Q23-----	5, fig. 6-60-----	5, fig. 6-60-----	-4.5.
Q24-----	5, fig. 6-60-----	5, fig. 6-60-----	+4.5.
Q25-----	-1.2-----	-1.0-----	-4.5.
Q26-----	16, fig. 6-60-----	16, fig. 6-60-----	+4.5.
Q27-----	-2.6 ^b -----	-4.5-----	13, fig. 6-60.
Q28-----	-1.5-----	13, fig.6-60-----	-4.5.
Q29-----	0-----	0-----	-2.9.
Q30-----	-2.9-----	-2.6-----	-4.5.

^a Checked with sync in input of test multiplexer obtained from SYNC OUT XMTR output of second test multiplexer. Oscilloscope synchronized from SYNC OUT connected OUT own of second test multiplexer.

^b Measured at terminal 29.

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME--26B/U and the figure references are to waveform measurements using the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	1	2	3	5	7	8	9	10	11
Z1 -----		-1.7	-2.6				-2.6	-1.5.	
Z2 -----		-1.8	-1.5				-1.5	-1.8.	
Z3 -----		12, fig. 6-60	-1.8				-1.8	14, fig.6-60	
Z4 ^a -----	2, fig. 6-60	23, fig. 6-60					24, fig. 6 60		
Z5 ^a -----		1, fig. 6-60				4, fig. 6-60	4, fig. 0.6		
Z6 -----		14, fig. 6-60		-2.4	-1.6			-1.5.	
Z7 -----	-1.7	-1.7	-1.6			-2.4 ^b		-3.2	-3.2.
Z8 -----		-1.5				3, fig. 6-60	3, fig. 6-60		
Z9 -----			-1.6			16, fig. 6-60	16.,fig. 6-60		

^a. Checked with sync in input of test multiplexer obtained from sync out xmtr output of second test multiplexer. Oscilloscope synchronized from SYNC OUT connector of second test multiplexer.

^b. Measured at terminal 11 of panel.

4-16. Panel 1A9, Troubleshooting

a. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
1	No modem timing output at terminal 22.	Z1 or Q1 defective	Check waveform at base of Q1. If present, check Q1. If absent, check Z1 (assert tally that of modem timing at terminal 22).
2	No address pulse output at terminal 14.	Z4 or Q6 defective	Check waveform at emitter of Q6. (essentially that of reshaped clock at terminal 3). If waveform present, check Z4. If absent, check Q6.
3	No <i>aux address</i> output or low-amplitude <i>aux address</i> output at terminal 18.	a. Q9, Q10, or Q11 defective b. Z5 defective c. Q8, CR11 or CR12 defective. d. Q7, CR9, or CR10 - defective..	a. Check waveform at pin 10 Z5 (essentially that of <i>aux address</i> output at terminal 18). If present, check Q9, Q10, and Q11. If absent, proceed to b below. b. Check waveform at emitter of Q8. If absent or incorrect, proceed to c below. If present, check pin 4- of Z5. If waveform at pin 4- information absent or incorrect, proceed to d below. If present, check Z5. c. Check Q8, CR11, and CR12. d. Check Q7, CR9, and CR10.
4	No <i>transmit pam</i> output or incorrect <i>transmit pam</i> (even channels) output at terminal 30.	Q12. or Q13 defective	Check Q12. and Q13.
5	No <i>transmit pam</i> output or incorrect <i>transmit pam</i> (odd channels) output at terminal 31.	Q14 or Q15 defective	Check Q14 and Q15.
6	No <i>transmit address</i> timing output at terminal 16.	Q16 defective	Check Q16.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with respect to ground with the ME -26B/U and the figure references are to waveform measurements using the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation 4-
- (2) Channels modulated with internal 1,100cps test tone as specified in chart.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector	Transistor	Base	Emitter	Collector
Q1 -----	6, fig. 6-62	6, fig. 6-62	+4.5.	Q12 -----	-2.4 -----	-2.1 -----	-4.5.
Q6 -----	-2.0-----	-1.7 -----	-4.5.	Q13 ^b -----	+ 1.2-----	0-----	8, fig. 6-62.
Q7 -----	9, fig. 6-62 --	9, fig. 6-62--	-4.5.				
Q8 -----	10, fig. 6-62	10, fig. 6-62	-4.5.	Q14 -----	-2.4 -----	-2.1-----	-4.5.
Q9 -----	11, fig. 6-62	11, fig. 6-62	-4.5.	Q16 ^c -----	-1.2 -----	0-----	8, fig. 6-62
Q10-----	11, fig. 6-62	11, fig. 6-62	-4.5.				
Q11 a ----	11, fig. 6-62	3, fig. 6-62. -		Q16 -----	-2.4 -----	-2.1-----	-4.5.

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are T6 waveform measurements using the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) ADDRESS switch at MASTER.
- (3) AUX switch at OUT.
- (4) 2 WIRE-4 WIRE switch at 4 WIRE.
- (5) Module terminal voltages are as follows:

Module	2	3	5	8	9	10
Z1 -----	-1.6			6, fig. 6-62	6, fig. 6-62	
Z4 -----	5, fig. 6-62 ^a		-2.4 ^b	-1.7 ^c		5, fig. 6-62.
Z5 -----		10, fig. 6-62			9, fig. 6-62	11, fig. 6-62.

^a Waveform should be inverse of that shown.

^b Measure at terminal 2 of panel.

^c Measure at emitter of Q6.

4-17. Panel 2A9, Troubleshooting

a. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
1	No <i>shift No. 1</i> output at terminal 24.	Z1, Z3, or Q1 defective	Check waveform at pin 10 of Z3. If present, check Z1 and Q1. If absent, check Z3.
2	Simultaneous loss of <i>timing out</i> signal at terminal 31, <i>sync out xmtr</i> signal at terminal 7, and <i>sampling clock</i> sign&1 at terminal 14.	Z2 or Q2 defective	Check Z2 and Q2.
3	Loss of <i>timing out</i> signal at terminal 31 only.	Q3 defective	Check Q3.
4	Loss of <i>sync out xmtr</i> signal at terminal 7 only.	Q4defective	Check Q4.
5	Loss of <i>sampling clock</i> signal at terminal 14 only.	Q8 or CR6 defective	Check Q8 and CR5.
6	No <i>address pulse</i> output or incorrect <i>address pulse</i> output at terminal 29.	a. Z4 defective b. Q10 or Q11 defective c. Q9, Q28, CR7, CR8, or CR9 defective.	a. Check waveform at J1. If check Z4. If incorrect, proceed to b below. b. Check waveform at junction of CR7 and CR9. If correct, check Q10 and Q11. If incorrect, proceed to c below. c. Check waveform at collector of Q9. If incorrect, check Q9. If correct, check Q28, CR7, CR8, and CR9.
7	No or incorrect <i>8-kc address</i> output at terminal 26.	Q24 or CR28 defective	Check Q24, and CR28.

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/4 and the figure references are to waveform measurements using the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Translator	Base	Emitter	Collector
Q1 -----	-2.1 -----	-4.5-----	7, fig. 6-64.
Q2 -----	2, fig. 6-64 -----	2, fig. 6-64-----	+4.5.
Q3 -----	2, fig. 6-64 -----	10, fig. 6-64	
Q4 -----	2, fig. 6-64 -----	3, fig. 6-64	
Q8 -----	2, fig. 6-64 -----	4, fig. 6-64-----	-4.5.
Q9 -----	16, fig. 6-68 -----	0 -----	-0.9.
Q10 -----	12, fig. 6-64 -----	-4.5-----	1, fig. 6-64
Q11 -----	16, fig. 6-57 -----	1, fig. 6-64-----	-4.5.
Q24 -----	-2.4 -----	-2.1-----	-4.5.
Q28 -----	-2.4 -----	-2.1-----	-4.5.

Terminal 31 terminated in

c. *Module Terminal.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	2	5	8	9	10
Z1 -----	-2.4-----	-----	-----	7, fig. 6-64	
Z2 -----	-2.4-----	-----	2, fig. 6-64 ---	2, fig. 6-64	
Z3 -----	-2.8-----	19, fig. 6-57.-	16, fig. 6-57 --	-----	-2.1.
Z4 -----	9, fig. 6-64----	18, fig. 6-59--	1, fig. 6-64----	-----	5, fig. 6-64

4-18. Panel 1A10, Troubleshooting

a. *Troubleshooting Chart.* Use a dual-channel oscilloscope for the following troubleshooting procedures, and keep a constant check on the synchronization of the various' timing signals, with respect to the *modem timing* signal at terminal 29.

Item No.	Symptom	Probable trouble	Correction
1	No <i>FF4</i> output or erroneous <i>FF4</i> output at terminal 27 (J8) and/or <i>FF4</i> output at terminal 14.	Z1 defective	Check Z1.
2	No <i>FF5</i> output or erroneous <i>FF5</i> output at terminal 20 (J5) and/or <i>FF5</i> output at terminal 17.	Q1, Q2, or Z2 defective	Check waveform at J3 which should be in synchronization with modern timing input (J2). If present check check Z2. If absent, check Q1 and Q2.
3	No <i>FF5</i> output or erroneous <i>FF5</i> output at terminal 21 (J9).	a. Z3 defective b. CRT, CR2, Q3, or Q4 defective.	a. Check waveform at J1 which should be in synchronization with modem timing (J2), <i>FF4</i> (J8), and <i>FF5</i> (J5) signals. If present, check Z3. 'If absent, proceed to b below. b. Check waveform at base of Q4, which should be essentially that of <i>FF5</i> (J5) gated with <i>FF4</i> (J8). If present, check Q4 and Q3. If absent, check CR1 and CR2.
4	No M11 output at terminal 26.	Q1 in Z10 defective. CR5, CR23, or CR1 in Z9 defective.	CR15 signal at pin 3 of Z10. If present, replace Z10. If absent, replace Z9.
5	No M13 output at terminal 25.	Q2 in Z10; CR11 CR21, CR7, or CR2 in Z9; or CR28 defective.	Check signal at pin 5 of Z10. If present, replace Z10. If absent, check CR28 first. If CR28 checks good, replace Z9.
6	No M15 output at terminal 24.	Q3 in Z10; CR12, CR19, CR6, or CR3 in Z9; or CR27 defective.	Check signal at pin 8 of Z10. If present, replace Z10. If absent, check CR27 first. If CR27 checks good, replace Z9.
7	No M17 output at terminal 22.	Q4 in Z10; CR13, CR9, CR8 or CR4 in Z4; or CR26 defective.	Check signal at pin 10 of Z10. If present, replace Z10. If absent, check CR26 first. If CR26 checks good, replace Z9.

Item No.	Symptom	Probable trouble	Correction
8	No <i>M18</i> output at terminal 19.	Q4 in Z11; CR14, CR19, CR8 or CR4 in Z9; or CR25 defective.	Check signal at pin 10 of Z11. If present, replace Z11. If absent, check CR25 first. If CR25 checks good, replace Z9.
9	No <i>M16</i> output at terminal 18.	Q3 in Z11, CR15, CR20, CR6 or CR3 in Z9; or CR29 defective.	Check signal at pin 8 of Z11. If present, replace Z11. If absent, check CR29. first. If CR29. checks good, re- place Z9.
10	No <i>M14</i> output at terminal 16.	Q2 in Z11; CR15 CR22, CR7 or CR2 in Z9; or CR23 defective.	Check signal at pin 5 of Z11. If present, replace Z11. If absent, check CR23 first. If CR23 checks good, replace Z9
11	No <i>M12</i> output at terminal 15.	Q1 in Z11. or CR17, CR29, CR5, or CR1 in Z9 defective.	Check signal at pin 3 of Z11. If present, replace Z11. If absent, replace Z9.
12	No <i>M11</i> output at terminal 3.	Z12 defective	Replace Z12.
13	No <i>M12</i> output at terminal 6.	Z12 defective	Replace Z12.
14	FF4, FF5, and FF5 outputs all good but simultaneous loss of following: <i>FF8</i> output at terminal 5 <i>FF9</i> output at terminal 9 <i>FF9</i> output at terminal 11 <i>M21</i> output at terminal 13 <i>M22</i> output at terminal 1 <i>M23</i> output at terminal 12 <i>M24</i> output at terminal 4 <i>M25</i> output at terminal 10 <i>M26</i> output at terminal 7	a. Z4 defective b. CR3, CR4, CR5, Q5, or Q6 defective.	a. Check waveform at J4, which should be in synchronization with modem timing (J2), <i>FF4</i> (J8), <i>FF5</i> (J5), and <i>FF5</i> (J9) signals. If present, check Z4. If absent, proceed to b below. b. Check waveform at base of Q6, which should be essentially that of <i>FF5</i> (J9) gated with <i>FF4</i> (J8) (J8), <i>FF5</i> (J5), and <i>FF5</i> (J9). If present, check Q6 and Q5. If absent, check CR3, CR4, and CR5.

Item No.	Symptom	Probable trouble	Correction
15	<p><i>FF4</i>, <i>FF5</i>, <i>FF5</i>, and $\overline{FF8}$ outputs all good but simultaneous loss of:</p> <p><i>TFF9</i> output at terminal 9T or <i>RFF9</i> output at terminal 11</p> <p><i>M21</i> output at terminal 13 <i>M21</i> output at terminal 1 <i>M23</i> output at terminal 12 <i>M24</i> output at terminal 4 <i>M25</i> output at terminal 10 <i>M26</i> output at terminal 7.</p>	<p>a. Z6 defective</p> <p>b. CR10, CR11, CR12, CR13, CR14, Q9, or Q10 defective.</p>	<p>a. Check waveform at J5, which should be in synchronization with modem timing (J2), <i>FF4</i> (J8), <i>FF5</i> (J5), <i>FF5</i> (J9), <i>FF8</i> (J11), and Z4 output (J10) signals. If present, check Z6. If absent, proceed to b below,</p> <p>b. Check waveform at base of Q10, which should be essentially that of <i>FF8</i> (J11) gated with <i>FF4</i> (J8), <i>FF5</i> (J5), <i>FF5</i> (J9), <i>FF8</i> (J11), and Z4 output (J10). If present, check Q10 and Q9. If absent, check CR10 through CR14.</p>
16	<p>No <i>FF8</i> output at terminal 5</p>	<p>a. Z6 defective</p> <p>b. CR6, CR7, CR8, CR9, Q7 or Q8 defective.</p>	<p>a. Check waveform at pin 3 of Z5, which should be essentially as shown for J10 and in synchronization with modem timing (J2), <i>FF4</i> (J8), <i>FF5</i> (J5), and <i>FF5</i> (J9) signals. If present, check Z5. If absent, proceed to b below.</p> <p>b. Check waveform at base of Q8, which should be essentially that of Z4 output (J10) gated with <i>FF4</i> (J8), <i>FF5</i> (J5), and <i>FF5</i> (J9). If present, check Q8 and Q7. If absent, check CR5, through CR9.</p>

Item No.	Symptom	Probable trouble	Correction
17	Erroneous <i>FF8</i> output at terminal 5, <i>TFF9</i> output at terminal 9, and to or <i>RFF9</i> output at terminal 11	<p>a. CR21, CR22, C7, C9, R24, R25, R26, or R27 defective.</p> <p>b. CR15 through CR20, Q11, or Q12 defective.</p>	<p>a. Check waveform at J7, which should be in synchronization with modem timing (J2), <i>FF4</i> (J8), <i>FF5</i> (J5), <i>FF6</i> (J9), Z4 output (J10) <i>FF8</i> (J11) and <i>FF9</i> (terminal 11) signals. If any signal is present (even though erroneous) check CR21, CR22, C7, C9, and R24 through R27. If no signal at J7, proceed to below.</p> <p>b. Check waveform at base of Q12, which <u>should</u> be essentially that of <i>FF9</i> (terminal 11) gated with all preceding timing signals as in previous items. If the waveform is present, check Q12 and Q11. If absent, check CR15 through CR20.</p>
18	No <i>M21</i> output at terminal 13.	CR16, CR8, CR20, or CR29 in Z7 defective. Q14 defective.	Check Q14 . If good, replace Z7.
19	No <i>M22</i> output at terminal 1.	Q1 in Z6 defective. CR15, CRT, CR29., or CR20 in Z7 defective.	Check signal at pin 1 of Z7. If present, replace Z6. If absent, replace Z7.
20	No <i>M23</i> output at terminal 12.	CR7., CR18, or CR23 in Z7defective. Q13 defective.	Check Q13. If good, replace Z7.
21	No <i>M24</i> output at terminal 4.	Q2 in Z6 defective. CR3, CR19, or CR22 in Z7 - defective.	Check signal at pin 3 of Z7. If present, replace Z6. If absent, replace Z7.
22	No <i>M25</i> output at terminal 10. Z7 defective.	Q4 in Z6 defective. CR5, CR9, CR17, or CR21 in absent, replace Z7.	Check signal at pin 5 of Z7. If present, replace Z6. If absent, replace Z7.
23	No <i>M26</i> output at terminal 7.	Q3 in Z6 defective. CR4, CR10, CR17, or CR21 in Z7 defective.	Check signal at pin 4 of Z7. If present, replace Z6. If absent, replace Z7.

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Translator	Base	Emitter	Collector
Q1-----	See note 1-----	14, fig. 6-66-----	-4.5.
Q2-----	-2.4-----	-4.5-----	14, fig. 6 66.
Q3-----	See note 1-----	1, fig. 6-66-----	-4.5.
Q4-----	-1.6 (see note 2)-----	-4.5-----	1, fig. 6-66.
Q5-----	See note 1-----	3, fig. 6-66-----	-4.5.
Q6-----	-1.0 (see note 3)-----	-4.5-----	3, fig. 6-66.
Q7-----	See note 1-----	32, fig. 6-66-----	-4.5.
Q8-----	-0.7 (see note 4)-----	-4.5-----	32, fig. 6-66.
Q9-----	See note 1-----	4, fig. 6-66-----	-4.5.
Q10-----	-0.45 (see note 5)-----	-4.5-----	4, fig. 6-66.
Q11-----	See note 1-----	5, fig. 6-66-----	-4.5.
Q12-----	-0.45 (see note 6)-----	-4.5-----	5, fig. 6-66.
Q13-----	-3.6-----	-4.3-----	0.
Q14-----	-3.6-----	-4.2-----	0.

Notes

1. For 1A10 panels used in receive side of TD-353/U, refer to 26, figure 6-77, for waveform at base of transistor. For 1A10 panels used in transmit side of TD-353/U, refer to 6, figure 6-62, for waveform at base of transistor.

2. Measure at junction of CRT, CR2, and R6.
3. Measure at junction of CR4, CR5, and R9.
4. Measure at junction of CR7, CR8, CR9, and R12.
5. Measure at junction of CR10, CR12, CR13, CR14, and R15.
6. Measure at junction of CR15, CR10, CR17, CR18, CR19, CR20, and R18.

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B1U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Z1	-2.4	-2.4	(^a)							-2.4	-2.4				
Z2	-2.4	-2.4	14, fig. 6-66.							-2.4	-2.4				
Z3	-2.4	-2.4	1, fig. 6-66.							-2.4	-2.4				
Z4	-2.4	-2.4	3, fig. 6-66.							-2.4	-2.4				
Z5	16, fig. 6-66.	16, fig. 6-66.	32, fig. 6-66.							29, fig. 6-66.	29, fig. 6-66.				
Z6	-2.4	-2.4	4, fig. 6-66.							-2.4	-2.4				
Z7	-3.6		-3.6	-3.6	-3.6		-3.6	-3.6	-3.6	-2.4		21, fig. 6-66.	29, fig. 6-66.	-2.4	-2.4
Z8		-4.2	-3.6	-4.2	-3.6		-4.2	-3.6	-4.2	-3.6					
Z9	-3.6	-3.6	-3.6	-3.6	-3.6	-3.6	-2.4	-3.6	-2.4		-2.4	-2.4	-2.4	-2.4	-2.4
Z10		-4.3	-3.6	-4.3	-2.4		-4.3	-3.6	-4.3	-3.6					
Z11		-4.3	-3.6	-4.3	-3.6		-4.3	-3.6	-4.3	-3.6					
Z12		-4.3	-4.6					-4.6		-4.3					

^a For 1A10 panels used in receive side of TD-353/U, refer to 26, figure 6-77 for waveform. For 1A10 panels used in transmit side of TD-353/U, refer to 6, figure 6-62 for waveform.

4-19. Panel 2A10, Troubleshooting

a. *Troubleshooting Chart.* Use a dual-channel oscilloscope for the following troubleshooting procedures, and keep a constant check on the synchronization-of the various timing signals, with respect to the modem timing signal at terminal 29.

Item No.	Symptom	Probable trouble	Correction
1	No T or $\overline{FF4}$ output, or erroneous T or $\overline{FF4}$ output at terminal 27 (J8) and/ or T or $\overline{FF4}$ output at terminal 14.	Z1 defective	Check Z1.
2	No T or $\overline{RFF5}$ output, or erroneous T or $\overline{FF5}$ output at terminal 20 (J5) and/or $\overline{FF5}$ output at terminal 17.	Q1, Q2, or Z2 defective	Check waveform at J3, which should be in synchronization with modem timing input (J2). If present, check Z2. If absent, check Q1 and Q2.
3	No T or $\overline{FF5}$ output, or erroneous T or $\overline{FF5}$ output at terminal 21 (J9) and/or T or $\overline{FF6}$ output at terminal 19.	a. Z3 defective b. CRT, CR2, Q3, or Q4 defective.	a. Check waveform at J1, which should be in synchronization modem timing (J2), to or $\overline{FF4}$ (J8), and to or $\overline{FF5}$ (J5) signals. If present, check Z3. If absent, proceed to b below. b. Check waveform at base of Q4, which should be essentially that of to or $\overline{FF5}$ (J5) gated with to or $\overline{FF4}$ (J8). If present, check Q4 and Q3. If absent, check CR1 and CR2.
4	No $\overline{M11}$ or $\overline{D11}$ output at terminal 24.	CR23, CR24. or Q14 defective.	Check CR23, CR29. and Q14 .
5	No $\overline{M12}$ or $\overline{D12}$ output at terminal 25.	CR21, CR22, or Q13 defective.	Check CR21, CR22, and Q13.
6	$\overline{FF4}$, $\overline{FF5}$, and $\overline{FF5}$ outputs all good but simultaneous loss of following: T or $\overline{FF8}$ output at terminal 5. T or $\overline{FF9}$ output at terminal 9. T or $\overline{FF9}$ output at terminal 11.	a. Z4 defective b. CR3, CR4, CR5, Q5, or Q6 defective.	a. Check waveform at J4, which should be in synchronization with modem timing (J2), to or $\overline{FF4}$ (J8), to or $\overline{FF5}$ (J5), and to or $\overline{FF5}$ (J9) signals. If present, check Z4. If absent, proceed to b below. b. Check waveform at base of Q6, which should be essentially that of T or $\overline{RFF6}$ (J9) gated with T or $\overline{FF4}$ (J8), to or $\overline{FF5}$ (J5), and T or $\overline{RFF6}$ (J9). If present, check

Item No.	Symptom	Probable trouble	Correction
7	<p><i>M21</i> or <i>D21</i> output at terminal 13. <i>M22</i> or <i>D22</i> output at terminal 1. <i>M23</i> or <i>D23</i> output at terminal 12. <i>M24</i> or <i>D24</i> output at terminal 4. <i>M25</i> or <i>D25</i> output at terminal 10. <i>M26</i> or <i>D26</i> output at terminal 7.</p> <p>T or <i>FF4</i>, T or <i>FF5</i>, T or <i>FF5</i>, and T or <i>FF8</i> outputs all good but simultaneous loss of following: T or <i>FF9</i> output at terminal 9. T or <i>FF9</i> output at terminal 11.</p> <p><i>M21</i> or <i>D21</i> output at terminal 13. <i>M22</i> that of to or <i>FF8</i> (<i>J11</i>) terminal 1. <i>M23</i> or <i>D23</i> output at terminal 12. <i>M24</i> or <i>D24</i> output at terminal 4. <i>M25</i> or <i>D25</i> output at terminal 10. <i>M26</i> or <i>D26</i> output at terminal 7.</p>	<p>a. Z6 defective</p> <p>b. CR10, CR11, CR12, CR13, CR14, Q9, or or <i>D22</i> output at</p>	<p>Q6 and Q5. If absent, check CR3, CR4, and CR5.</p> <p>a. Check waveform at J5, which should be in synchronization with modem timing (J2), to or <i>FF4</i> (J8), to or <i>FF5</i> (J5), to or <i>FF5</i> (J9), to or <i>FF8</i> (J11), and Z4 output (J10) signals. If present, check Z6. If absent, proceed to b below.</p> <p>b. Check waveform at base of Q10, which should be assert tally gated with to or <i>FF4</i> (J8), to or <i>FF5</i> (J5), to or <i>FF5</i> (J9), to or <i>FF8</i> (J11), and Z4 output (J10). If present, check Q10 and Q9. If absent check CR10 through CR14.</p>
8	<p>No T or <i>FF8</i> output at terminal 5.</p>	<p>a. Z6 defective</p> <p>b. CR6, CR7, CR8, CR9, Q7, or Q8 defective.</p>	<p>a. Check waveform at pin 3 of Z5, which should be in synchronization with to or <i>FF4</i> (J8), to or <i>FF5</i> (J5), to or <i>FF5</i> (J9), and modem timing (J2) signals. If present, check Z5. If absent, proceed to b below.</p> <p>b. Check waveform at base of Q8, which should be essentially that of Z4 output (J10) gated with T or <i>FF4</i> (J8),</p>

Item No.	Symptom	Probable trouble	Correction
9	Erroneous to or $\overline{FF8}$ output at terminal 5, to or $FF9$ output at terminal 9, and to or $\overline{FF9}$ output at terminal 11.	<p>a. CR25, CR26, C15, C17, R28, R29, R30, or R31 defective.</p> <p>b. CR15, CR16, CR17, CR18, CR19, CR20, Q11, or Q12 defective.</p>	<p>to or $FF5$ (J5), and to or $FF5$ (J9). If present, check Q8 and Q7. If absent, check CR6 through CR9.</p> <p>a. Check waveform at J7, which should be in synchronization with modem timing (J2), to or $FF4$ (J8), to or $FF5$ (J5), to or $FF5$ (J9), Z4 output (J10), T or $FF8$ (J11), and T or $FF9$ (terminal 11) signals. If any signal is present (even though erroneous), check CR25, CR20, C15, C17, and R26 through R30. If no signal at J7, proceed to b below.</p> <p>b. Check waveform at base of Q12, which should be essentially that of to or $\overline{FF9}$ (terminal 11) gated with all preceding timing signals as in previous items. If the waveform is present, check Q12 and Q11. If absent, check CR15 through CR20.</p>
10	No M21 or D21 output at terminal 13.	CR15, CR8, CR20, or CR29. in Z7 defective. Q15 defective.	Check Q15. If good, replace Z7.
11	No M23 or D22 output at terminal 1.	CR16, CRT, CR29., or CR20 in Z7 defective. Q1 in Z6 defective.	Check signal at pin 1 of Z7. If present, replace Z6. If absent, replace Z7.
12	No M23 or D23 output at terminal 12.	CR7, CR18, or CR23 in Z7 defective. Q16 defective.	Check Q16. If good, replace Z7.
13	No M24 or D24 output at terminal 4.	CR3, CR19, or CR22 in Z7 defective. Q2 in Z6 defective.	Check signal at pin 3 of Z7. If present, replace Z6. If absent, replace Z7.
14	No M25 or D25 output at terminal 10.	Q4- in Z6 defective. CR5, CR9, CR17, or CR21 in Z7 defective.	Check signal at pin 5 of Z7. If present, replace Z6. If absent, replace Z7.
15	No M26 or D26 output at terminal 7.	Q3 in Z6 defective. CR4, CR10, CR17, or CR21 in Z7 defective.	Check signal at pin 4 of Z7. If present, replace Z6. If absent, replace Z7.

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measure meets made with the oscilloscope under | the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at MASTER.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Translator	Base	Emitter	Collector
Q1-----	See note 1 below -----	2, fig. 6-68-----	-4. 5.
Q2-----	-2.4 -----	-4.5-----	2, fig. 6 68.
Q3-----	See note 1 below -----	1, fig. 6-68-----	-4.5.
Q4-----	-1.8 (see note 2) -----	-4.5-----	1, fig. 6-68.
Q5-----	See note 1 below -----	3, fig. 6-68-----	-4.5.
Q6-----	-1.0 (see note 3) -----	-4.5-----	3, fig. 6-68.
Q7-----	See note 1 -----	24, fig. 6-68 -----	-4.5.
Q8-----	-0.7 (see note 4) -----	-4.5-----	24, fig. 6-68.
Q9-----	See note 1 -----	4, fig. 6-68-----	-4.5.
Q10-----	-0.45 (see note 5)-----	-4.5-----	4, fig. 6-68.
Q11-----	See note 1 -----	5, fig. 6-68-----	-4.5.
Q12-----	-0.45 (see note 6)-----	-4.5-----	5, fig. 6-68.
Q13-----	-3.3 -----	-3.5-----	0.
Q14-----	-3.3 -----	-3.5-----	0.
Q15-----	-3.7 -----	-3.9-----	0.
Q16-----	-3.7 -----	-3.9-----	0.

Notes

1. For 2A10 panels used in receive aide of TD-352/U, refer to 27, figure 6-?7 for waveform at base of transistor. For 2A10 panels used in transmit side of TD-352/U, refer to 16, figure 6-60 for waveform at base of transistor.

2. Measure at junction of CRT, CR7, and R6.
3. Measure out junction of CR3, CR4, CR6, and T9.
4. Measure at junction of CR6, CR7, CR8, CR9, and R12.
5. Measure at junction of CR10, CR12, CR13, CR14, and CR15.
6. Measure at junction of CR16, CR16, CR17, CR18, CR15 CR20, and R18.

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	1	2	3	4	5	7	8	9	10	11	12	13	14	15
Z1	-2.4	-2.4	(^a)						-2.4	-2.4				
Z2	-2.4	-2.4	2, fig. 6-68.						-2.4	-2.4				
Z3	-2.4	-2.4	1, fig. 6-68.						-2.4	-2.4				
Z4	-2.4	-2.4	3, fig. 6-68.						-2.4	-2.4				
Z5	-2.4	-2.4	24, fig. 6-68.		5, fig. 6-68				-2.4	-2.4				
Z6	-2.4	-2.4	4, fig. 6-68.				5, fig. 6-68		-2.4	-2.4				
Z7	-3.7		-3.7	-3.7	-3.7		-3.7	-2.4	-2.4	-2.4	-2.4	-2.4	-2.4	-2.4
Z6		-4.3	-3.7	-4.3	-3.7	-4.3	-3.7	-4.3	-3.7					

^a For 2A10 panels used in receive side of TD-352/U, refer to 27, fig. 6-77 for waveform. For 2A10 panels used in transmit side of TD-352/U, refer to 16, fig. 6-60.

4-20. Panel 1A11/2A11, Troubleshooting

a. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
1	No <i>clipped noise</i> output at terminal 10. (No reading on TEST ALIGN meter with METER SELECT switch set to NOISE GEN.)	<p>a. Noise source buffer Q1; or voltage/ current amplifier stage Q2/Q3, Q4/Q5, Q6/Q7, or Q8/Q9 defective</p> <p>b. Clipped noise output circuit Q10, Q11, or Q12 defective.</p>	<p>a. Check signal at J1. If present, proceed to <i>b</i> below. If present but insufficient gain, proceed to item 2. If absent, check Q1. Collect or Q1 will measure -12 volts if transistor is open, and GEN.) volts if shorted. If Q1 checks good (collect or at -8 volts), check signal at emitters of buffers Q3, Q5, and Q7. If signal information absent at any emitter, check transistor and preceding amplifier. Be sure to check coupling capacitors C19 and C24, and their protective diodes CR1 and CR2, respectively. If signal is present up to emitter of Q7, check Q8 and Q9.</p> <p>b. Check signal at J2. If absent, check C29. If present, Check signal at J3. If signal information present, check Q12. If absent, check Q11 and Q10.</p>
2	Low clipped noise output at terminal 10. (TEST ALIGN meter does not read in green area with METER SELECT switch set to NOISE GEN.)	Low gain in voltage/ current amplifier stage Q2/Q3, Q4/Q5, Q6/Q7, or Q8/Q9	Overall gain of amplifier should be about 120 db and signal at J1 (emitter of Q9). about 7 volts peak to-peak. Check signal at emitters of Q7, Q5, and Q3 to isolate defective voltage/current amplifier stage, then both transistors of that stage.

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows 4

Transistor	Base	Emitter	Collector	Transistor	Base	Emitter	Collector
Q1 -----	>+1.4 -----	>1.7-----	-8.0.	Q7 -----	-5.1 -----	-4.8 -----	-11.4.
Q2 -----	0 -----	+0.25-----	-5.4.	Q8 -----	0-----	-0.30-----	-5.7.
Q3 -----	-5.4-----	-5.1 -----	-11.4.	Q9-----	-5.7 -----	-5.4 -----	-11.2.
Q4 -----	0 -----	+0.25-----	-2.5.	Q10 -----	0-----	-1.8 -----	-4.5.
Q5 -----	-2.5-----	-2.3 -----	-11.4.	Q11 -----	0-----	-1.8 -----	-2.4.
Q6 -----	0 -----	+0.25-----	-5.1.	Q12 -----	-2.4 -----	-2.3 -----	-4.5.

4-21. Panel 1A1 2/2A12 of 1A121 Troubleshooting.

a. *Troubleshooting Chart.*

Item No.	Symptom	Probable trouble	Correction
1	Simultaneous loss of <i>sampled pcm</i> output at terminal 10 and <i>pcm</i> to AUX output at terminal 4.	Q1, Z1, and/or Z2 defective	Check waveform at J5. , check Z2. If absent, check Z1 and Q1.
2	Loss of sampled palm output at terminal 10 only.	Q4 defective	Check Q4.
3	Loss of <i>pcm</i> to AUX output at terminal 4 only.	Q2, Q3, and/or Q5 defective	Check Q2, Q3, and Q5.
4	No <i>alt pcm</i> out at terminal 1	Q6, Z3, Z4, Q7, DL1, Q8, Q9 or Q10 defective.	a. Check waveform at J9. If present, check Q8, Q9, and Q10. If absent, proceed to b below. b. Check waveform at J7. If present, check Z4, Q7, and DL1. If absent, check Z3 and Q6.
5	No <i>receive address</i> output at terminal 20.	Q26 or Q27 defective	Check Q26 and Q27.
6	No <i>alarm timing</i> output (2 kc or 4 kc) at terminal 5.	Q28 defective	Check Q28.
7	No 4-kc <i>alarm timing</i> output at terminal 5.	Z6 defective	Check Z6
8	No 2-kc <i>alarm timing</i> output at terminal 5.	Z7 defective	Check Z7.

a. Troubleshooting Chart- Continued ..

Item No.	Symptom	Probable trouble	Correction
9	Simultaneous loss of <i>skip pulse</i> output at terminal 25 and <i>alarm control</i> output at terminal 29.	Defect in one or more of the following circuits: a. Pcm address (Q21, Z5, Z6 and/or Q22). b. Reference address (Q25) c. Address exclusive OR gate (Q23, Q24, and/or Q15). d Skip pulse generator (Q11, Q12, Q13, and/or Q14). e. Skip pulse gate (CR6, CR7, C17, Q16) defective. f. Differential amplifier Q18, Q19, and Q20 defective.	a. Check waveform at J1. If absent, check Q25. If present, proceed to b below. b. Check waveform at J8. If absent, check Q21 and Z5. If present, proceed to c below. c. Check waveform at J3. If absent, check Z6 and Q22. If present, proceed to d below. d. Check waveform at J4. If absent, check Q11, Q12, and Q13. If present, check Q14 . If Q14 is good, check CR6, CR7, C17, and Q16. e. Check waveform at J10. If absent, check Q23 and Q24, If present, check Q15. If Q15 checks good, proceed to f below- f. Check waveform at J2. If absent, check Q18 and Q19. If present, check Q20.
10	No <i>skip pulse</i> output at terminal 25 (alarm control output is good).	Q17 defective	Check Q17.
11	No <i>alarm control</i> output at terminal 29 (skip pulse output is good).	Q18, Q19, and/or Q20 - defective.	Check waveform at J2. If present, check Q20. If absent, check Q18 and Q19.

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for Loop back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are follows:

Translator	Base	Emitter	Collector
Q1	See note 1	0	23, 24, fig. 6-71.
Q2	18, 19, fig. 6-71	18, 19, fig. 6-71	-4.5.
Q3	18, 19, fig. 6-71	18, 19, fig. 6-71	-4.5.
Q4	18, 16, fig. 6-71	16 19, fig. 6-71	-4.5.
Q5 (see note b.)	18, 16, fig. 6-71	14, 15, fig. 6-71	
Q8	See note 2	0	25, 26, fig. 6-71.
Q7	33, 34, fig. 6-71	33, 34, fig. 6-71	-4.5.
Q8	10, 11, fig. 6-71	10, 11, fig. 6-71	-4.5.
Q9	10, 11, fig. 6-71	T6 1-1, fig. 6-71	-4.5.
Q10 (see note 7)	10, 11, fig. 6-71	4	12, 13, fig. 6-71
Q11	-2.4	2.2	-4;5.
Q12	-2.2 4	2.0	-4.5.
Q13	2.0	+0.3	3, fig. 6-71
Q14	4- 3, fig. 6-71	3, fig. 6-71	-4.5.
Q15	-2.2 (see note 3)	4- -2.0 (see note 3)	-4.5.
	+0.2 (see note 4)	+0.2 (see note 4)	
Q10	27, fig. 6-71	0	22, fig. 6-71.
Q17	22, fig. 6-71	22, fig. 6-71	-4.5.
Q18	4- 1.0 (see note 3)	+ 1.3 (see note 3)	0.
	+2.7 (see note 4)	+ 1.7 (see note 4).	
Q19	+1.5	+1.3 (see note 3)	-3.8 (see note 3).
	+ 1.7 (see note 4)	-1.9 (see note 4).	
Q20	-0.3 (see note 3)	0	0 (see note 3).
	0 (see note 4)	-4.5 (see note 4).	
Q21	0	28, fig. 6-71	
Q22	-1.1 (see note 3)	-0.9 (see note 3)	-4.5.
	-0.6 (see note 4)	-0.4 (see note 4).	
Q23	-0.4 (see note 3)	-0.4	-4.5.
	+0.2 (see note 4).		
Q24,	0 (see note 3)	-0.9 (see note 3)	-4.5.
	0.1 (see note 4)	-0.4 (see note 4).	
Q26	9, fig. 6-71	9, fig. 6-71	-4.5.
Q27	0	See note 6	9, fig. 6-71
Q28	-2.0	-1.8 4	-4.5.

Notes

1. Input to base of Q1 is timing A signal at terminal 18.
2. Input to base of Q. information timing a signal at terminal 2.
3. Measured with palm IN connector removed (unit out of frame).
4. Measured with palm IN connector replaced (unit in frame).
5. Signal at emitter of Q27 is same as timing C signal at terminal 19.
6. Terminal 4 germinated in 91-ohm load.
7. Terminal 1 germinated in 91-ohm load.

c. Module Terminal Voltages. The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	2	3	5	8	9	10
Z1	23, 24, fig. 6-71.	.	29, 30, fig. 6-71.	20, 21, fig. 6-71.	.	4, 5, fig. 6-71.
Z2		29, 30, fig. 6-71.			4, 5, fig. 6-71.	18, is, fig. 6-71.
Z3	25, 26, fig. 6-71.		31, 32, fig. 6-71.	20, 21, fig. 6-71.		7, 8, fig. 6-71.
Z4		31, 32, fig. 6-71.			7, 8, fig. 6-71.	33, 34, fig. 6-71.
Z5	28, fig. 6-71.		35, fig. 6-71.	20, 21, fig. 6-71.		6, fig. 6-71.19,
Z6		6, fig. 6-71			35, fig. 6-71	a-1.8 b_ 3.5.
Z7	-2.0	9, fig. 6-71			9, fig. 6-71	
Z8	-1.8	17, fig. 6-71			17, fig. 6-71	-2.0.

- ^a Measured with PAM IN connector removed (unit out of frame).
- ^b Measured with PCM IN connector replaced (unit in frame).
- ^c Checked with SYNC IN input of test multiplexer obtained from SYNC OUT XMTR output of second test multiplexer. Oscilloscope synchronized from SYNC OUT connector of second test multiplexer.

4-22. Panel 1A13, Troubleshooting

a. Troubleshooting Chart. The TD-353/U test unit must be looped-back for the following procedure. Jacks J3 and J4 are major test points on the panel and are used to isolate trouble between the two principal circuits (that is, the timing in pulse shaping and timing A/timing B signal gating circuit, and the timing signal countdown circuit). Items 1 through 7 of the troubleshooting procedure cover those symptoms wherein there is a simultaneous loss of outputs from both jack J3 and jack J4, and no, or erroneous, output from either jack J3 or jack J4. When the timing A and timing B waveforms are present at jacks J3 and J4, respectively, any trouble in the timing signal countdown circuit can then be isolated by referring sequentially to the symptoms given in items 8 through 21. If the test unit still will not frame with the panel, the trouble is probably in the timing A/timing B switching flip-flop Z2 or its associated skip pulse amplifier Z1 (item 22).

Item No.	Symptom	Probable trouble	Correction
1	No timing A or timing B 2,304-kc timing signal at either J3 or J4 (with PCM IN connector either con-removed).	<p>a. Q2 or Z3 defective</p> <p>b. Z2 defective</p>	<p>a. Check waveform at J2, which should be delayed 0.1 μs with respect to timing in signal at terminal 1. If correct, proceed to b below. If absent, check Q2 and Z3.</p> <p>b. Check voltages at pins 2 and 10 of Z2. If pin 2 is positive (0 volt), pin 10 must be negative (-4.5 volts); or if pin 2 is negative (-4.5 volts), pin 10 must be positive (0 volt). If any other condition exists, Z2 is defective.</p>

Note. The symptoms given in items 2 and 3 below are probable when the voltages at pins 2 and 10 of flip-flop Z2 are positive (0 volt) and negative (-4.5. volts), respectively.

2	No timing A signal at J3, but timing B signal is present at J4.	<p>a. Z5 defective</p> <p>b. Q6, Q7, CR9, CR10, or CR11 defective.</p> <p>e. Q13 defective</p> <p>d. Q14 or Z4 defective</p>	<p>a. Check waveform at pin 9 of Z5. If present, proceed to correction Voltages. below. If absent, check Z5.</p> <p>b. Check waveform at cathode of CR11. If present, proceed to c below. If absent, check Q7 for open circuit or Q6 for short circuit. If Q6 and Q7 are good, check CR9, CR10, and CR11</p> <p>e. Check waveform at base of Q14 If present, proceed to d below. If absent, check Q13.</p> <p>d. Check waveform at pin 2of Z4. If present, check Z4. If absent, check Q14</p>
---	---	--	---

Item No.	Symptom	Probable trouble	Correction
3	No timing B signal et J4, but timing A signal is present at J3.	a. Q4, Q5, CR6, CR7, or CR8 defective. b. Q16 or Z6 defective	a. Check waveform at cathode of CR8. If present, proceed to b below. If absent, check Q4 for open circuit or Q5 for short circuit. If Q4 and Q5 are good, check CR6, CR7, and ORB. b. Check waveform at pin 2 of Z6. If present, check Z6. If absent, check Q16.
<p><i>Note.</i> The symptoms given in items 4 and 5 below are probable when the voltages at pins 2 and 10 of flip-flop Z2 are negative (-4.5 volts) and positive (0 volt), respectively.</p>			
4	No timing B signal at J4, but timing A signal is present at J3.	a. Z5 defective b. Q8, Q9, CR12, CR13, or CR14 defective. c. Q16 or Z6 defective	a. Check waveform at pin 9 of Z5. If present, proceed to b below. If absent, check Z5. b. Check waveform at cathode of CR14. If present, proceed to c below. If absent, check Q8 for open circuit or Q9 for short circuit. If Q8 and Q9 are good, check CR12, CR13, and CR14. c. Check waveform at pin 2 of Z6. If present, check Z6. If absent, check Q16.
5	No timing A signal at J3, but timing B signal is present at J4.	a. Q10, Q11, CR15, CR16, or CR17 defective. b. Q13 defective c. Q14 or Z4 defective	a. Check waveform at cathode of CR17. If present, proceed to b below. If absent, check Q11 for open circuit or Q10 for short circuit. If Q10 and Q11 are good, check CR15, CR16, and CR17. b. Check waveform at base of Q14. If present, proceed to c below. If absent, check Q13. c. Check waveform at pin 2 of Z4. If present, check Z4. If absent, check Q14.

Item No.	Symptom	Probable trouble	Correction
6	Erroneous undelayed 2,304-kc timing signal (observed at J4 when pins 2 and 10 of Z2 are positive (0 volt) and negative (-4.5 volts) respectively, or at J3 when pins 2 and 10 of Z2 are negative (-4.5 volts) and positive (0 volt) respectively).	Q2, L3, L4, C28, or Z3 defective.	Check waveform at J2 with respect to timing in signal at terminal 1. If timing relationship is erroneous, check Q2, L3, L4, and C28. If wave shape is erroneous, check Z3.
7	Erroneous delayed 2,304-kc timing signal (observed at J3 when pins 2 and 10 of Z2 are positive (0 volt) and negative (-4.5 volts) respectively, or at J4 when pins 2 and 10 of Z2 are negative (-4.5 volts) and positive (0 volt) respectively). erroneous, check DL1. If wave shape is erroneous, check Z5.	DL1 or Z5 defective	Check waveform at J3 (or J4 as applicable) with respect to undelayed timing signal at J2. The pulses in the waveform at J3 (or J4) should be delayed 0.2 us and should fall approximately midway between those observed at J2. If timing relationship is
8	No <i>sync out rcvr</i> output at terminal 2.	Q17 defective	Check Q17.
9	No <i>receive aux clock</i> output at terminal 18.	Q15 defective	Check Q15.
10	No <i>timing in monitor</i> output at terminal 9.	Q1, CRT, or CR4 defective	Check Q1, CR1, and CR4.
11	Simultaneous loss of: <i>Rcvr frame pulse</i> (terminal 12) <i>FF2B</i> (terminal 203) <i>384-kc s.w.</i> (terminal 21) <i>Matrix FF</i> (terminal 23) <i>Address digit gate</i> (terminal 24) <i>Timing C</i> (terminal 30).	Z7 defective	Check Z7.
12	<i>Timing C</i> output at terminal 30 and rear frame pulse at terminal 12 both erroneous (outputs at terminals 20, 21, 23, and 24 present).	Q22 defective	Check Q22.

Item No.	Symptom	Probable trouble	Correction
13	Simultaneous loss of FF output at terminal 20, 884-kc s.w. output at terminal 21, and address digit gate output-at terminal 24 (outputs at terminals 12, 23, and 30 erroneous).	Z8 defective	Check Z8.
14	Loss of FF2B output at terminal 20 only.	Q24 defective	Check Q24.
15	Simultaneous loss of 884-kc s.w. output at terminal 21 and address digit gate output at terminal 24 (output at terminal 20 is present; outputs at terminals 12, 23, and 30 are erroneous).	Q26 or Z9 defective	Check Q26 and Z9.
16	Following outputs all simultaneously erroneous: Rcvr frame pulse (terminal 12) FF2B (terminal 20) 884-kc s.w. (terminal 21) Matrix FF (terminal 23) Address digit gate (terminal 24) Timing a (terminal 30).	-a. Q23 defective b. Q27 or Z12 defective	a. Check waveform at emitter of Q23 ter of Q23 (essentially that of pin 2 of Z7). If present proceed to b below. If absent, check Q23. b. Check for presence of 576 kc signal at emitter of Q27. If no signal, check Q27. If present, check Z12.
17	Timing C output at terminal 30, Rcvr frame pulse output at terminal 12, and matrix FF output at terminal 23 simultaneously erroneous (outputs at terminals 20, 21, and 24 are good).	Q25 defective	Check Q25.
18	Loss of timing C output at terminal 30 and rcvr frame pulse output at terminal 12 only (outputs at terminals 20, 21, 23, and 24 all good).	Q28 or Z10 defective	Check Q28 and Z10.

Item No.	Symptom	Probable trouble	Correction
19	No matrix FF output at terminal 23 only (outputs at terminals 12, 20, 21, 23, and 24 all good).	Z11 defective	Check Z11.
20	No address digit gate output at terminal 24 (outputs at terminals 12, 23, and 30 erroneous; outputs at terminals 20 and 21 good).	Q18, CR23, or CR24 defective.	-Check Q18, CR23, and CR24.
21	No address digit gate output at terminal 24 only (outputs at terminals 12, 20, 21, 23, and 30 all good).	Q24, defective	Check Q24,
22	No <i>rcvr frame pulse</i> at terminal 12 (other outputs all good).	Q30 defective	Check Q30.
23	All timing signal outputs present and apparently good, but TD-353/U, test unit will not frame with this panel. (Timing A and timing B signal condition at J3 and J4 does not interchange when PAM IN connector is removed.)	Z1 or Z2 defective	With PAM IN connector removed, check waveform at J1. If absent or erroneous, Check Z1. If present, check Z2. The polarity of the voltages at pins 2 and 10 of Z2 should change each time a <i>skip pulse</i> appears at J1.
24	No <i>skip FF</i> output at terminal 7. No TEST ALIGN hairline meter reading with SERV SEL switch set to M and METER SELECT switch set to SERV FAC.	Q12 defective	Check Q12.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measured meets made with the oscilloscope under I the following conditions:

- (1) Test multiplexer connected for loop-back operation Voltages. (0 Voltages. Voltages.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector	Transistor	Base	Emitter	Collector
Q1 -----	6, fig. 6-73-	6, fig. 6-73 --	-4.5.	Q15 ^b -----	-2.4-----	-1.7 -----	-2.7.
Q2 -----	6, fig. 6-73	0-----	-1.4.	Q16 -----	-1.0-----	-0.8 -----	-1.7.
Q4 ^a -----	-3.4-----	-3.7 -----	-4.5.	Q17 ^c -----	-1.8-----	-1 7 -----	-2.7.
Q5 ^a -----	-2.4-----	-3.3 -----	-4.5.	Q18 -----	17, fig. 6-73	0-----	5, fig. 6-73
Q6 ^a -----	-2.4-----	-3.0 -----	-4.6.				
Q7 ^a -----	-3.3-----	-3.7 -----	-4.5.	Q22 -----	-1.8 -----	-1.5 -----	-4.5.
Q8 ^a -----	-3.3-----	-3.7-----	-4.5.	Q23 -----	-1.7 -----	-1.4 -----	-4.5.
Q9 ^a -----	-2.4-----	-3.5-----	-4.5.	Q24 -----	-1.8 -----	-1.5 -----	-4.5.
Q10 ^a -----	-2.4-----	-3.3 -----	-4.5.	Q25 -----	-1.8 -----	-1.5 -----	-4.5.
Q11 ^a -----	-3.4-----	-3.7-----	-4.5.	Q28 -----	-1.8 -----	-1.5 -----	-4.5.
Q12 ^a -----	-2.4-----	-2.1-----	-4.5.	Q27 -----	-1.7 -----	-1.4-----	-4.5.
Q13-----	-1.0-----	-0.8 -----	-1.7.	Q28 -----	16, fig. 6-73	16, fig. 6-73	-4.5.
Q14 -----	-1.7-----	-1.6-----	-4.5.	Q24,-----	5, fig. 6-73	-15, fig. 6-73	-4.4.

^a PCM IN connector removed for these measurements (unit out Or frame).

^b Terminal 18 terminated In 91 ohm load.

^c Terminal 2 terminated in 91-ohm load.

c. Module Terminal Voltages. The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	1	2	3	4	8	9	10	11
Z1 (see note 1)		See note 2.				1, fig. 6-73.		
Z2 (see note 1)	-2.4	-2.4	1, fig. 6-73.				-2.4	-2.4.
Z3		-1.4	1.2		3.7	3.4		
Z4		-1.6			3.8	3.6		
Z5		1.0			3.6	3.3		
Z6		1.7			3.8	3.5		
Z7		-1.7	-3.5			-3.5	-1.8	
Z8		1.7	1.7			1.7	-1.8	
Z9		1.8	1.7			1.7	-1.5	
Z10		-3.6		16, fig. 6-73.	-1.5	-1.4	-1.5	5, fig. 6-73.
Module	2	4	5	7	8	9	10	
Z11	-3.6	14, fig. 6-73.			-1.5	-1.4	-1.5	
Z12	-1.7		-1.4	-1.5			-1.4	

Notes

1. PCM IN connector removed (unit out of frame).
2. Signal at pin 2 of Z1 is essentially the same as *skip pulse* input at terminal 15.

4-23. Panel 2A13, Troubleshooting

a. Troubleshooting Chart. The TD-352/U test unit must be looped-back for the following procedure and one channel modulated with the internal test tone.

Item No.	Symptom	Probable trouble	Correction
1	Simultaneous loss of all timing output signals. (TEST ALIGN meter does not read in green area for H and K positions of SERV SEL switch, and TD-352/U test unit gives continuous frame alarm.)	a. Z2 defective b. DL1, Q1, Q2, DL2, Q3, Q4, or Z1 defective.	a. Check waveform at J2. If present, check Z2. If absent or erroneous, proceed to <i>b</i> below. b. Check waveform at J7. If absent or erroneous, check frequency doubler circuit from input of DL1 through Q1, Q2, and DL2, to output of inverter Q3. If J7 waveform is present, check Z1; if Z1 is good, check for shorted Q4.
2	No <i>decoder clock</i> output or erroneous decoder clock output at terminal 31 only.	Q6, DL3, or Q7 defective	Check Q6, DL3, and Q7.
3	Simultaneous loss of $\overline{RFF1}$ output at terminal 29, timing A output at terminal 30, and <i>Rcvr aux</i> clock at terminal 11 only.	Q5 defective	Check Q5.
4	No <i>timing A</i> output or erroneous timing A output at terminal 30 only.	Z3 defective Check Z3.	
5	No <i>Rcvr aux</i> clock output at terminal 11 only.	Q9, Q8, CR9, or Q10 - defective.	Check Q10, Q8, CR8, and Q9.
6	<i>Rcvr aux</i> clock output at terminal 11 will not squelch when PAM IN connector is removed.	Q9 defective	Check Q. for short circuit.
7	Simultaneous loss of <i>RFF1</i> output at terminal 10, modem timing output at terminal 14, $\overline{RFF2}$ output at terminal 13, <i>RFF2</i> output at terminal 27, <i>timing B</i> output at terminal 26, and <i>sync out rcvr</i> output at terminal 28.	Q12 defective	Check Q12.

Item No.	Symptom	Probable trouble	Correction
8	<i>Timing B</i> output at terminal 26 and <i>sync out rcvr</i> output at terminal 28 simultaneously lost or erroneous.	Z9 defective	Check Z9.
9	No <i>sync out rcvr</i> output at terminal 28 only.	Q21 defective	Check Q21.
10	Simultaneous loss of <i>modem timing</i> output at terminal 14, $\overline{RFF2}$ output at terminal 13, and <i>RFF2</i> output at terminal 27 only.	Z7 defective	Check Z7.
11	No <i>modem timing</i> output or erroneous <i>modem timing</i> output at terminal 14 only.	Q14 or Q15 defective	Check waveform at J6. If present, check Q15. If absent or erroneous, check Q14
12	No $\overline{RFF2}$ output at terminal 13 only.	Q13 defective	Check Q13.
13	No <i>RFF2</i> output at terminal 27 only.	Q16 defective	Check Q16.
14	Modem timing output at terminal 14, $\overline{RFF2}$ output at terminal 14, <i>RFF2</i> output at terminal 27, and timing a output at terminal 25 simultaneously erroneous.	Z6 defective	Check Z6.
15	No address digit pulse output at terminal 17.	CR18, CR19, Q17, or Q22 defective.	Check waveform at J4. If present, check Q17 and Q22. If absent, check CR18 and CR19.
16	No timing C output at terminal 25.	CR15, CR16, CR17, Q18, or Q19 defective.	Check waveform at J5. If present check Q19. If absent, check Q18 and CR15 through CR17.
17	Erroneous <i>timing C</i> output at terminal 25.	Z8 defective	Check Z8.

Item No.	Symptom	Probable trouble	Correction
18	TD-352/U test unit recovers correctly when PCM IN connector is removed and then replaced, but there is no <i>monitoring</i> M output (<i>skip-pulse</i> activity) at terminal 9. (No TEST ALIGN meter reading with SERV SEL switch set to M and when PCM IN connector is replaced.)	C26, CR21, or Q20 defective	Check CR21, C26, and Q20.
19	Audio output of TD-352/U test unit is garbled using this panel, although all timing signal outputs are apparently good; unit is not giving a frame alarm; and pcm activity is not squelched. (In this symptom, test unit is, in fact, out of frame due to defective timing signal skip circuit in panel 2A13.) open circuit. If no skip-	<p>a. Q4 defective</p> <p>b. Z5, Z4, or Q11 defective</p>	<p>a. Set SERV SEL switch to M and METER SELECT switch to SERV FAC. Remove and then replace PCM IN connector while observing TEST ALIGN meter. <i>Skip -pulse</i> activity should be noted (meter reading in green area). If this observation is correct, check Q4 for pulse activity is observed proceed to b below.</p> <p>b. Remove and then replace PCM IN connector while checking waveform at J3. (Synchronize oscilloscope from J10 on panel 1A12/2A12 for this presentation.) If waveform is erroneous, check Z4. If absent, check Q11 and Z4. If present and correct, check Z5.</p>
20	No <i>timing in monitor</i> output at terminal 23. (TEST ALIGN meter does not read in green area with METER SELECT switch set to TIMING IN.)	C1, CR1, CR2, or C2 defective.	Check C1, CRT, CR2, and C2.

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1-----	See note below -----	0-----	20, fig. 6-75.
Q2-----	20, fig. 6-75-----	-----	21, fig. 6-75.
Q3-----	21, fig. 6-75-----	-0.3-----	6, fig. 6-75.
Q4-----	-6.0-----	-4.5-----	1, fig. 6-75.
Q5-----	-1.8-----	-1.5-----	-4.5.
Q6-----	-1.8-----	-1.6-----	-4.5.
Q7-----	-1.6-----	-1.3-----	-4.5.
Q8-----	+0.1-----	22, fig. 6-75-----	23, fig. 6-75.
Q9-----	+0.3-----	0-----	+0.1.
Q10-----	23, fig. 6-75-----	9, fig. 6-75-----	
Q11-----	7, fig. 6-75-----	0-----	24, fig. 6-75.
Q12-----	-2.0-----	-1.7-----	-4-5.
Q13-----	-1.9-----	10, fig. 6-75-----	-4.5.
Q14-----	10, fig. 6-75-----	+4.5-----	11, fig. 6-75.
Q15-----	11, fig. 6-75-----	11, fig. 6-75-----	+4.5.
Q16-----	15, fig. 6-75-----	-1.6-----	-4.5.
Q17-----	3, fig. 6-75-----	3, fig. 6-75-----	0.
Q18-----	27, fig. 6-75-----	-4.5-----	13, fig. 6-75.
Q19-----	13, fig. 6-75-----	-4.5-----	13, fig. 6-75.
Q20-----	25, fig. 6-75-----	25, fig. 6-75-----	-4.5.
Q21-----	14, fig. 6-75-----	16, fig. 6-75-----	
Q22-----	3, fig. 6-75-----	12, fig. 6-75-----	-4.5.

Note. Waveform at base of Q1 is essentially that of terminal 2 only delayed 0.2 µsec.

c. *Module Terminal Voltages.* module terminal voltages listed below were measured with respect to ground with the M E-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	2	3	5	7	8	9	10
Z1 -----	6, fig. 6-75.	-----	-----	-----	1, fig. 6-75 --	1, fig 6-75. --	
Z2 -----	-20-----	6, fig. 6-75.	-----	-----	-----	6, fig. 6-75. -	-1.8.
Z3 -----	-15-----	-----	-----	-----	18, fig. 6-75.	18, fig. 6-75.	
Z4 -----	24, fig.6-75	-----	-----	-----	-----	2, fig. 6-75.	
Z5 -----	26, fig.6-75	-----	2, fig. 6-75.	-----	1, fig. 6-75.--	-----	25, fig. 6-75
Z6 -----	15, fig.6-75	-----	-2.4 -----	-1.6-----	-----	-----	-1.7.
Z7 -----	15, fig.6-75	-1.7 -----	-----	-----	-----	- 1.7-----	-1.9.
Z8 -----	-1.6-----	-----	-----	-----	-----	13, fig. 6-75.	
Z9 -----	-1.7-----	-----	-----	-----	14, fig. 6-75.	14, fig. 6-75.	

4-24. Panel 1A14/2A14, Troubleshooting

a. *Troubleshooting Chart.* This panel must be checked in both TD-352/U and TD-353/U test units. The units must be looped-back and modulated, except as directed in item 5.

Item No.	Symptom	Probable trouble	Correction
1	Simultaneous loss of <i>decoder pam</i> output at terminal 1; <u>B</u> and <u>B</u> outputs at terminals 2 and 5 respectively; and <u>A</u> and <u>A</u> outputs at terminals 3 and 4, respectively.	<p>a. Q1, Q2, or Z2 defective</p> <p>b. Z1 defective</p> <p>c. Z14, Q3, or Q4 defective</p>	<p>a. Check waveform at J2. If absent, check Q1 and Q2. If present, check waveform at J1. If this waveform is absent, check Z2. If present, proceed to b</p> <p>b. Check Z1. If good, proceed to c below.</p> <p>c. Check Z14, Q3, and Q4. If good trouble is either in serial or parallel shift registers; proceed with item 2.</p>
2	No <u>B</u> or <u>B</u> outputs at terminals 2 and 5, respectively.	<p>a. Q3, Q4, Z1, or Z12 defective.</p> <p>b. Z6, defective</p> <p>c. Z5 defective</p> <p>d. Z3 or Z4 defective</p>	<p>a. Check waveforms at J8, J6, and J9. If all present check Z12. If waveforms are present at J8 and J9, but not at J6, proceed with b below. If waveform at J8 is absent, check for presence of ht modem timing output at terminal 22. If this waveform is present, check Q3 and Q4; if absent, proceed with item 3. If waveform at J9 is absent, check Z1.</p> <p>b. Check waveform at J5. If present, check Z6. If absent, proceed with c below.</p> <p>c. Check waveform at J4. If present, check Z5. If absent, proceed with d below.</p> <p>d. Check waveform at J3. If present, check Z4. If absent, check Z3.</p>
3	No <u>FFS</u> or 384-kc s.w. input at terminal 22.	Z14, Q3 or Q4 defective	Check Z14, Q3, and Q4.
4	No <u>A</u> or <u>A</u> outputs at terminals 3 and 4, respectively.	a. Z7, Z13, or Q9 defective.	a. Check waveform at J7. If present, check Z13 and Q9. If absent, check Z7. If Z7 checks good, proceed with b below

Item No.	Symptom	Probable trouble	Correction
5	Low level 2- or 4-kc tone in channel 12. (4-kc tone if ADDRESS switch is in MASTER position; 2-kc tone if ADDRESS switch is in SLAVE position.)	b. Z11 defective c. Z10 defective d. Z9 defective e. Z8 defective. f. Q7 and/or Q8 defective Q5, Q6, Q7, Q8, or Z8 defective.	b. Check waveform at pin 7 of Z11. If absent, check Z11. If present, proceed with c below. c. Check waveform at pin 7 of Z10. If absent, check Z10. If present, proceed with d below. d. Check waveform at pin 7 of Z7. If absent, check Z9. If present, proceed to e below. e. Check waveform at pin 7 of Z8. If absent, check Z8. If present, proceed to f below. f. See that led is at -4.5 volts. If not, check Q7 and Q8. Check waveform at emitter of Q6. If absent, check Q5, Q6, Q7, and Q8. If present, check Q8.
6	Panel checks apparently good, but demodulated output of multiplexer is still distorted.	One or more flip-flop modules have marginal defect.	Remove internal modulation from test unit and insert varying dc levels into coder pam input of panel 1A6/2A6. Using a dual-channel oscilloscope, monitor signal at terminal 31 and J1 of panel 1A14/2A14. Signal at J1 should follow that at terminal 31, with appropriate delay. If not, replace Z1. If signal at J1 checks good, repeat this procedure for J3, J4, J5, J6, and J7, replacing any module with marginal operation. If Z2 through Z7 check good, see that output (pin 7) of Z8 through Z13 clamps to -5.0 and 0 volts.

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation
- (2) One channel modulated with internal 1,100 cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1-----	0-----	28, 29, fig. 6-77-----	28, 30, fig. 6-77.
Q2-----	+ 0.2-----	0-----	0.
Q3-----	26, 27, fig. 6-77-----	26, 27, fig. 6-77-----	-4.5.
Q4-----	26, 27, fig. 6-77-----	26, 27, fig. 6 - 77 ----	-4.5.
Q5-----	6, fig. 6-79 ----- 3, fig. 6-81	-4.5 -----	31, 32, fig. 6-77.
Q6-----	26, 27, fig. 6 - 77 ----	31, 32, fig. 6 - 77 ----	-4.5.
Q7-----	5, fig. 6-79 ----- 6, fig. 6-81	-4.5 -----	33, 34, fig. 6-77.
Q8-----	26, 27, fig. 6 - 77 ----	33, 34, fig. 6-77-----	-4.5.
Q9 -----	22, 40, fig. 6 - 77 ----	-5.2 -----	23, 40, fig. 6 - 77.

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	1	2	3	4	6	7	8	9	10	11
Z1 ----	-----	-1.3 ----	-----	-----	-----	-----	17, 18, --- fig. 6- 77.	17, 18, fig. 6- 77.	-----	-----
Z2 ----	-----	See note - 1 be- low.	-----	-----	-----	-----	3, 4, fig. - 6-77.	-----	1, 2, fig. 6-77.	-----
Z3 ----	See note 1 be- low.	See note 2 be- low.	17, 18, fig. 6- 77.	-----	-----	-----	-----	-----	5, 6, fig. - 6-77.	1, 2, fig. 6-77.
Z4 ----	5, 6, fig. - 6-77.	See note 3 be- low.	17, 18, fig. 6- 77.	-----	-----	-----	-----	-----	7, 8, fig. - fig. 6- 77.	See note 2 be- low.
Z5 ----	7, 8, fig. - 6-77.	See note 4 be- low.	17, 18, fig. 6- 77.	-----	-----	-----	-----	-----	9, 10, fig. 6-77.	See note 3 be- low.
Z6 ----	9, 10, fig. 6-77.	See note 5 be- low.	17, 18, fig. 6- 77.	-----	-----	-----	-----	-----	11, 12, -- fig. 6- 77.	See note 4 be- low.
Z7 ----	11, 12, --- fig. 6- 77.	See note 6 be- Low.	17, 18, fig. 6- 77.	-----	-----	-----	-----	-----	13, 14, -- fig. 6- 77.	See note 5 be- low.
Z8 ----	-----	-----	32 33 -- fig. 6- 77.	See note-- 7 be- low.	See note 9 be- low.	35, 36, --- fig. 6- 77.	-----	-----	-----	See note 8 be- low.
Z9 ----	-----	-----	-----	See note-- 10 be- low.	See note 12 be- low.	37, 40, --- fig. 6- 77.	-----	-----	-----	See note 11 be- low.
Z10----	-----	-----	-----	See note-- 13 be- low.	See note 15 be- low.	38, 40, --- fig. 6- 77.	-----	-----	-----	See note 14 be- low.
Z11----	-----	-----	-----	See note-- 16 be- low.	See note 18 be- low.	39, 40, --- fig. 6-a 77.	-----	-----	-----	See note 17 be- low.

Module	1	2	3	4	6	7	8	9	10	11
Z12-----	11, 12,--- fig. 6- 77.	24, 25, -- fig. 6- 77.	26, 27, fig. 6- 77.	-----	-----	-----	-----	-----	20, 21, -- fig. 6- 77.	See note 5 be-, low. See note 20 be" low.
Z13-----	-----	-----	-----	See note--- 19 be- low.	See note 21 be- low.	22, 40, --- fig. 6- 77.	-----	-----	-----	
Z14-----	-----	-2.4 -----	-----	-----	-----	-----	26, 27, --- fig. 6- 77.	26, 27 fig. 6- 77.		

Notes

1. Waveform is same as that shown for Z2: pin 10 except that it is of opposite polarity.
2. Waveform is same as that shown for Z3: pin 10 except that it is of opposite polarity.
3. Waveform is same as that shown for Z4: pin 10 except that it is of opposite polarity.
4. Waveform is same as that shown for Z5: pin 10 except that it is of opposite polarity.
5. Waveform is same as that shown for Z6: pin 10 except that it is of opposite polarity.
6. Waveform is same as that shown for Z7: pin 10 except that it is of opposite polarity.
7. Input to Z8: pin 4 can be considered correct if signals at Z2: pin 10 and collector of Q5 are correct.
8. Input to Z8: pin 11 can be considered correct if signals at Z2: pin 2 and collector of Q5 are correct.
9. Waveform is same as that shown for Z8: pin 7 except that it is of opposite polarity.
10. Input to Z9: pin 4 can be considered correct if signals at Z3: pin 2 and emitter of Q3 are correct.
11. Input to Z9: pin 11 can be considered correct if signals at Z3: pin 10 and emitter of Q3 are correct.

12. Waveform is same as that shown for Z9: pin 7 except that it is of opposite polarity.
13. Input to Z10: pin 4 can be considered correct if signals at Z4: pin 2 and emitter of Q3 are correct.
14. Input to Z10: pin 11 can be considered correct if signals at Z4: pin 10 and emitter of Q3 are correct.
15. Waveform is same as that shown for Z10: pin 7 except that it is of opposite polarity.
16. Input to Z11 pin 4 can be considered correct if signals at Z5: pin 2 and emitter of Q3 are correct.
17. Input to Z11 pin 11 can be considered correct if signals at Z5: pin 10 and emitter of Q3 are correct.
18. Waveform is same as that shown for Z11 pin 7 except that it is of opposite polarity.
19. Input to Z13: pin 4 can be considered correct if signals at Z7: pin 2 and emitter of Q3 are correct.
20. Input to Z13: pin 11 can be considered correct if signals at Z7: pin 10 and emitter of Q3 are correct.
21. Waveform is same as that shown for Z13: pin 7 except that it is of opposite polarity.

4-24.1 Panel 1A14A/2A14A Troubleshooting

a. *Troubleshooting Chart.* This panel must be checked in both the TD-352/U and the TD-353/U test units. The units must be looped back and one channel modulated. In the TD-353/U, operate switch S1 on panel 1A14A/2A14A to HT, and to MT for the TD-352/U. Make certain variable resistors R5 and R106 are adjusted per paragraph 4-36.

Item No.	Symptom	Probable trouble	Correction
1.	Simultaneous loss of decoder pam output at terminal 1, B and <u>B</u> outputs at terminals 2 and 5 respectively, A and <u>A</u> outputs at terminals 3 and 4 respectively, and HT <i>modem</i> timing at terminal 21.	Q10, Q11, Z15, Z15, Z26, Z28 CR11, CR12, or S1 defective.	Check waveform at pin 8 of Z15. If present, check Z28. If absent, check waveform at pin 10 of Z16. If present, check the inverter at pin 8 of Z15. If absent, check waveform at pin 9 of Z16. If present, check Z16. If absent, check waveform at collector of Q11. If present and switch S1 is in MT position, check switch S1. If present and switch S1 is in HT position, check Z26 and switch S1. If absent, check Q10, Q11, CR11, and CR12.
2	Simultaneous loss of decoder pam output at terminal 1, B and <u>B</u> outputs at terminals 2 and 5 respectively, and A and <u>A</u> outputs at terminals 3 and 4 respectively.	a. Q5, Q6, CR3, Q9, Z9, Z10, Z12, or Z13 defective. b. Q1, Q2, Q3, Q4, Z1, or Z2 defective.	a. Check waveform at pin 7 of Z10. If present, proceed to b below. If absent, check waveform at pins 9 and 10 of Z10. If both waveforms are absent, check Q5, Q6, CR3, and the pin 2 inverter in Z12. If the waveform at pin 10 of Z10 only is absent, check Z13; if the waveform at pin 9 of Z10 only is absent, check Z9 and the pin 4 inverter in Z12. If waveforms are present at pins 9 and 10 of Z10, check squelch stage Q9. b. Check waveform at J3. If present, proceed to next step. If absent, check waveform at pin 10 of Z2. If present, check Q8 and Q4. If absent, check waveform at pin 10 of Z1. If present, check Z2.

Item No.	Symptom	Probable trouble	Correction
3	Simultaneous loss of B and \bar{B} outputs at terminals 2 and 5 respectively, A and \bar{A} outputs at terminals 8 and 4 respectively, and an incorrect <i>decoder pam</i> output at terminal 1.	Z3, Z4, Z5, or Z5, defective	If absent, check waveform at the collector of Q2. If present, check Z1. If absent, check Q1 and Q2. Check for waveform at pin 3 of Z6, Z5, Z4 and Z3, in that order. When waveform is first recovered, check flip-flop driven by that output.
4	Loss of A and \bar{A} outputs at terminals 3 and 4 respectively, and an incorrect <i>decoder pam</i> output at terminal 1.	Z7 or Z26 defective	Check waveform at J2. If present, check Z26. If absent check Z7.
5	Incorrect decoder pam output at terminal 1; distortion.	a. Z26, Q25, Q26 defective b. Z11, Z23, Z24, Q22, Q23, and Q24 defective.	a. Check pins 2 and 9 of Z265 for pcm waveform and find modulated channel. Trigger pulse at pin 10 will fall within the first bit of the PCM channel and will cause output at pins 8 and 8 to vary between 0 and -5. volts for 2.6 μ sec (H. T.), or 10.4 μ sec (M. T.). If no signal is present at pins 8 or 8, check Z26. If signals at pins 8 and 3 are not clamping to ground, check Q26 and Q26 respectively. b. Check pins 2 and 9 of Z24, Z23, Z22 for PCM waveform and find modulated channel. Trigger pulse at pin 10 will fall within the third bit of the PCM channel at Z24, within the fourth bit at Z28, within the fifth bit at

Item No.	Symptom	Probable trouble	Correction
6	Distortion at low signal levels.	Z19, Z20, Z11, Z14, Z15, Z17, Z27, Q19, Q20 defective. c. Z21, Z27, Z17, Q16, Q17, Q18 defective.	Z22, and will cause the respective outputs at pin 3 to vary between 0 and -6.2 volts for 2.6 μ sec (H. T.) or 10.6 μ sec (M. T.). If no signal is present at pin 3 of respective module, check that module. If signal at pin 3 of module is not clamping to ground, check the respective clamping transistors Q24, Q23, or Q22. c. Check pins 2 and 9 of Z21 for PCM waveform and find modulated channel. Check pin 10 for trigger pulse which will fall within the sixth bit of the modulated PCM channel; if present, it will cause a signal at pin 3 to vary between 0 and -5.2 volts for 2.6 μ sec (H. T.) or 10.4 μ sec (M. T.). If no signal is present at pin 3, check Z21. If signal at pin 3 is not clamping to ground, check Q21. If signal is absent at pin 10 of Z21, check pin 3 of Z27. If present at pin 3 of Z27, check pin 3 gated Z27; if absent, check pin 7 of Z17. If present at pin 7 of Z17, check pin 8 of Z17; if present, check pin 10 gate of Z17. If signal is absent at pin 8 of Z17, check Q16, Q17, and Q18. Place coder panel 1A6/2A6 on extension panel; disconnect PAM to coder lead and insert dc into coder. DC level should be variable between

Item No	Symptom	Probable trouble	Correction
			<p>+2.5 and -2.5 volts. Connect one oscilloscope probe to PCM OUT at front panel of unit and vary dc level into coder over total coder level range. Adjust CA potentiometer on 1A6/2A6 if level 15 or 48 is missing, then check the following. For any PCM code except 15, pin 3 of Z19 shall be at 0 volts; for code 15, pin 3 of Z19 shall be at -5.2 volts. If pin 3 of Z19 does not clamp to 0 volts, check Q19. If Z19 does not change state, check pins 10, 2, and 9 of Z19. If no signal is present at pin 10, check pin 9 of Z27; if absent, check pin 10 gate of Z27; if this signal is absent, check pin 3 of Z17. If signal is present at pin 3 of Z17, check pin 2 gate of Z17; if absent, check pin 4 gate of Z15. If signal is present at pin 10 of Z19, check pins 2 and 9. At code 15, pin 9 will have a negative going pulse between 0 volts and - 4.5 volts approximately 1 bit wide, and signal at pin 10 will coincide within the time period of this pulse. Pin 2 will have the inverse of the pulse at pin 9. If described pulse is absent at pin 9 of Z19, check Z11, CR7, and CR8. If pulse is present at pin 9 of Z19 but absent at pin 2, check pin 2 gate of Z15. For any PCM code except 48, pin 3 of Z20 shall be at -5.2 volts; for code 48, it shall be at 0 volts. If pin 3 of Z20 does not clamp to 0 volts, check Q20. If Z20 does not change state, check pins 2 and 9. At code 48, pin</p>

Item No.	Symptom	Probable trouble	Correction
7	LOSS of A or <u>A</u> outputs at terminals 3 and 4 respectively.	Z12 defective	2 will have a negative going pulse between 0 volts and -4.5 volts approximately 1 bit wide, and signal at pin 10 will coincide within the time period of this pulse. Pin 9 will have the inverse of this pulse at pin 2. If described pulse is absent at pin 2 of Z19, check Z14, CR5, and CR6. If pulse is present at pin 2 of Z20 but absent at pin 9, check pin 10 gate of Z15. Check Z12.
8	Loss of B and <u>B</u> outputs at terminals 2 and 5 respectively.	Z8 defective	Check Z8.
9	Loss of HT <i>modem timing</i> output at terminal 21.	Q15; or Z18 defective	Check Q16 or Z18.
10	Low level 2 or 4 kc tone in channel 48 (channel 12). (4 kc tone if ADDRESS switch is in MASTER position; 2 kc tone if ADDRESS switch is in SLAVE position.)	a. Q12, Z15, or Z17 defective b. Z17 defective c. Q16, Q17, or Q18 defective	a. Check waveform at pins 10 and 4 of Z21. If both are incorrect, proceed to c below. If waveform at pin 10 only is poor, proceed to b below. If waveform at pin 4 only is poor, check waveform at pin 2 of Z17; if correct, check Q12. If poor, check waveform at pin 3 of Z17; if correct, check the pin 2 gate of Z17. If incorrect, check the pin 4 inverter in Z15. b. Check pin 10 gate in Z17. c. Check waveform at base of Q18. If correct, check Q18. If incorrect, check Q16 and Q17.

b. Transistor Terminal Voltages. The transistor voltages listed below were measured with respect to ground with ME-26B/U; the figure references are to waveform measurements with

the oscilloscope made under the following conditions:

- (1) Test-multiplexer connected for loopback operation.
- (2) One channel modulated with internal 1100-cps test tone..
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages as follows:

Transistor	Base	Emitter	Collector
Q1	65, 66, fig. 6-77.2, or 0.0	67, 68, fig. 6-77.2, or -0.37 ± 0.03	-4.5
Q2	0.0	67, 68, fig. 6-77.2, or -0.37 ± 0.03	69, 70, fig. 6-77.2 or -1.8 ± 0.3
Q3	82, 83, fig. 6-77.2, or -3.8 ± 0.2	82, 83, fig. 6-77.2, or -3.8 ± 0.2	-4.16 ± 0.15
Q4	82, 83, fig. 6-77.2, or -3.8 ± 0.2	82, 83, fig. 6-77.2, or -3.8 ± 0.2	+4.4
Q5	1, 2, fig. 6-77.2	3, 4, fig. 6-77.2	-4.5
Q6	0.0	-----	5, 6, fig. 6-77.2
Q9	-3.7	-4.5	-4.3
Q10	73, 74, fig. 6-77.2; or -2.1 ± 0.4	75, 76, fig. 6-77.2, or -2.0 ± 0.3	-4.5
Q11	0.0	77, 78, fig. 6-77.2, or 0.87 ± 0.32	79, 80, fig. 6-77.2, or -2.3
Q12	25, 26, fig. 6-77.2	25, 26, fig. 6-77.2	+4.5
Q15	49, 50, fig. 6-77.2	49, 50, fig. 6-77.2	+4.5
Q16	51, 52, fig. 6-77.2, or +0.5	53, 54, fig. 6-77.2, or 0.1	-4.5
Q17	0.0	53, 54, fig. 6-77.2, or +0.1	55, 56, fig. 6-77.2, or -0.2
Q18	55, 56, fig. 6-77.2, or -0.2	55, 56, fig. 6-77.2, or 0.0	-4.5
Q19	39, 40, fig. 6-77.2	0.0	35, 36, fig. 6-77.2
Q20	41, 42, fig. 6-77.2	0.0	37, 38, fig. 6-77.2
Q21	57, 58, fig. 6-77.2	0.0	43, 44, fig. 6-77.2
Q22	59, 60, fig. 6-77.2	0.0	45, 46, fig. 6-77.2
Q23	59, 60, fig. 6-77.2	0.0	45, 46, fig. 6-77.2
Q24	59, 60, fig. 6-77.2	0.0	45, 46, fig. 6-77.2
Q25	59, 60, fig. 6-77.2	0.0	45, 46, fig. 6-77.2
Q26	59, 60, fig. 6-77.2	0.0	45, 46, fig. 6-77.2

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U; the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop back operation.
- (2) One channel modulated with internal 1100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages as follows:

Change 3 4-74,7

Z or Q NUMBER	1	2	3	4	5	6	7	8	9	10
Z1	-4.5	-----	-3.0±0.2	-----	-6.2	0	-----	-----	69, 70, fig. 6-77.2, or -1.8 ± 0.8	71, 72, fig. 6-77.2. or -8.6 ± 0.3
Z2	-4.5	-----	-3.0	-----	-6.2	0	-----	-----	69, 70, fig. 6-77.2, or -1.8 ± 0.3	82, 83 fig.. 6-77.2. or -3.8 ± 0.2
Z3	-4.5	INVERSE OF 13,14, fig. 6-77.2	16, 14, fig. 6-77.2	-----	-6.2	0	-----	INVERSE OF 16,, 14, fig. 6-77.2	13,14, fig. 6-77.2	82, 83, fig.. 6-77.2, or -3.8±0.2
Z4	-4.5	INVERSE OF 13, 14, fig. 6-77.2	16, 14, fig. 6-77.2	-----	-6.2	0	-----	INVERSE OF 13,14, fig. 6-77.2	13, 14, fig. 6-77.2	82, 83, fig. 6-77.2, or -3.8 ± 0.2
Z5	-4.5	INVERSE OF 13, 14 fig. 6.77.2	16. 14, fig. 6-77.2	-----	-6.2	0	-----	INVERSE OF 16, 14, fig. 6-77.2	13, 14, fig. 6-77.2	82, 83, fig.. 6-77.2, or -3.8±0.2
Z6	-4.5	INVERSE OF 13, 14, fig. 6-77.2	16, 14, fig. 6-77.2	-----	-6.2	0	-----	INVERSE OF 16, 14, fig. 6-77.2	13, 14, fig. 6-77.2	82, 83, fig. 6-77.2, or -3.8 ± 0.2
Z7	-4.5	INVERSE OF 13, 14, fig. 6-77.2	16, 14, fig. 6-77.2	-----	-6.2	0	-----	INVERSE OF 16, 14, fig. 6-77.2	13, 14, fig. 6-77.2	82, 83, fig. 6-77.2, or --3.8 ± 0.2
Z8	-5.2	INVERSE OF 13, 14, fig. 6-77.2	15, 16, fig. 6-77.2	-----	-6.2	0	-----	INVERSE OF 15, 16, fig. 6-77.2	13, 14, fig. 6-77.2	31, 32, fig.. 6-77.2
Z9	-4.5	-----	-----	-----	-6.2	0	-----	-----	INVERSE OF 7, 8, fig. 6-77.2	11, 12, fig. 6-77.2
Z10	-4.5	-4.3	13, 14,, fig. 6-77.2	-----	-6.2	0	13, 14, fig. 6-77.2	-4.3	11, 12, fig. 6-77.2	11, 12, fig. 6-77.2
Z11	-4.5	17, 18. fig. 6-77.2	19, 20, fig. 6-77.2	-----	-6.2	0	13, 14, fig. 6-77.2	13, 14 fig. 6-77.2	13, 14 fig. 6-77.2	13, 14 fig. 6-77.2
Z12	-4.5	7, 8, fig. 6-77.2	5, 6, fig. 6-77.2	INVERSE OF 7, 8. fig. 6-77.2	7, 8, fig. 6-77.2	0	-----	9, 10. fig. 6-77.2	-----	9, 10, fig. 6-77.2

Z13	-4.5	-----	-----	-----	-6.2	0	-----	-----	7, 8, fig. 6-77.2	11, 12, fig. 6-77.2
Z14	-4.5	17, 18, fig. 6-77.2	19, 20, fig. 6-77.2	-----	-6.2	0	INVERSE OF 13, 14, fig. 6-77.2	INVERSE OF 13, 14, fig. 6-77.2	INVERSE OF 13, 14, fig. 6-77.2	13, 14, fig. 6-77.2
Z15	-4.5	21, 22, fig. 6-77.2	19, 20, fig. 6-77.2	23, 24, fig. 6-77.2	55, 56, fig. 6-77.2	0	47, 48 fig. 6-77.2	61, 62, fig. 6-77.2	19, 20, fig. 6-77.2	21, 22, fig. 6-77.2
Z16	-4.5	-----	-----	-----	-6.2	0	-----	-----	79, 80, fig. 6-77.2	47, 48, fig. 6-77.2
Z17	-4.5	25, 26, fig.. 6-77.2	23, 24, fig. 6-77.2	31, 32, fig. 6-77.2	-----	0	31, 32, fig. 6-77.2	55, 56, fig. 77.2, or 0.0	-----	27, 28, fig. 6-77.2
Z18	-----	31, 32, fig. 6-77.2	-----	-----	-----	+10	+4.5	49, 60, fig. 6-77.2	49, 50, fig. 6-77.2	-4.5
Z19	-5.2	21, 22, fig. 6-77.2	35, 36, fig. 6-77.2	-----	-5.2	0	-----	-----	19, 20, fig. 6-77.2	29, 30, fig.. 6-77.2
Z20	-5.2	19, 20, fig. 6-77.2	3, 38, fig. 6-77.2	-----	-5.2	0	-----	-----	21, 22, fig. 6-77.2	29, 30 fig. 6-77.2
Z21	-5.2	82, 88, fig. 6-77.2, or -8.8±0.2	43, 44, fig. 6-77.2	25, 26, fig. 6-77.2	-5.2	0	-----	-----	13, 14, fig. 6-77.2	33, 34, fig. 6-77.2
Z22	-5.2	INVERSE OF 13, 14, fig. 6-77.2	46, 46, fig. 6-77.2	-----	-5.2	0	-----	-----	13, 14, fig. 6-77.2	33, 34 fig. 6-77.2
Z23	-5.2	INVERSE OF 13, 14, fig. 6-77.2	45, 46, fig. 6-77.2	-----	-5.2	0	-----	-----	13, 14, fig. 6-77.2	33, 34, fig. 6-77.2
Z24	-5.2	INVERSE OF 18, 14, fig. 6-77.2	45, 46, fig. 6-77.2	-----	-5.2	0	-----	-----	13, 14, fig.. 6-77.2	33, 34, fig. 6-77.2
Z25	-5.2	INVERSE OF 13, 14, fig. 6-77.2	45, 46, fig. 6-77.2	-----	-5.2	0	-----	INVERSE OF 13, 14, fig. 6-77.2	13, 14, fig. 6-77.2	33, 34, fig. 6-77.2
Z26	-4.5	-----	-----	-----	-6.2	0	-----	-----	13, 14, fig. 6-77.2	81, fig. 6-77.2
Z27	-4.5	33, 34, fig. 6-77.2	27, 28, fig. 6-77.2	-----	-----	0	-----	27, 28, fig. 6-77.2	25, 26, fig. 6-77.2	29, 30, fig. 6-77.2
Z28	-4.5	-----	31, 32, fig. 6-77.2	-----	-6.2	0	-----	61, 62, fig. 6-77.2	-----	-----

4-25. Panel 1A15, Troubleshooting

a. *Troubleshooting Chart.* Loop-back and modulate the TD-353/U test unit for this procedure.

Item. No.	Symptom	Probable trouble	Correction
1	No <i>main pcm</i> output at terminal 1.	Q20 defective	Check Q20.
2	Erroneous <i>main pcm</i> output at terminal 1.	DL2 defective	Check DL2.
3	No <i>384-kc modem gate timing</i> output at terminal 20.	Q16, Q17, or Q18 defective	Check waveform at emitter of Q18. If absent, check Q18. If present, check flip-flop Q16, Q17.
4	No <i>pcm from aux monitor</i> output at terminal 9.	Q19 or CR20 defective	Check waveform at emitter of Q19, If absent, check Q19, If present, check CR20.
5	No <i>address inhibit 1</i> output at terminal 7 or <i>address inhibit 2</i> output at terminal 6.	Q13, Q14, or Q15 defective	Check waveform at emitter of Q13, If absent, check Q13, If present, check Q14 and Q15
6	Erroneous <i>address inhibit 1</i> and <i>2</i> outputs at terminals 7 and 6, respectively.	DL1 defective	Check DL1.
7	No <i>receive pam</i> output at terminal 23.	a. Q12 defective b. Q6 and/or Q11 defective c. Q19 Q2, Q7, and/or Q8 defective. d.. Q3, Q4, or Q5 defective	a. Check waveform at J2. If present, check Q12 If absent, proceed to b below. b. Check waveform at base of Q6 and Q11. If no waveform at either base, check waveform at J7. If no waveform at J7, proceed to c below. If waveform is present at J7 and also at base of Q11 (but not at base of Q6), proceed to d below. If waveform is present at J7 and also at base of Q6 (but not at base of Q11) proceed to e below. If waveforms appear good at bases of both Q6 and Q11 but not at J2, check Q6 and Q11 c. Check operation of A-A/B-B gate circuit Q19 Q2, Q7, and Q8. d. Check waveform at collector of Q3. If present, check Q4 and Q5. If absent. check Q3.

a. Troubleshooting Chart -Continued

Item. No.	Symptom	Probable trouble	Correction
8	Dc level of receive pam output at terminal 23 does not shift when CTR pam center adjust) potentiometer R16 is adjusted.	e. Q9 or Q10 defective VR1, VR2, VR3, or R16 defective.	e. Check Q9 and Q10. Check for +18 volts at terminal 1 of R16. If present, check R16. If absent, check VR1, VR2, and VR3.

b. Transistor Terminal Voltage. The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/4 and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1-----	12, fig. 6-79-----	18, fig. 6-79-----	3, fig. 6-79.
Q2-----	11, fig. 6-79-----	19, fig. 6-79-----	3, fig. 6-79.
Q3-----	14, fig. 6-79-----	+4.5-----	15, fig. 6-79.
Q4-----	15, fig. 6-79-----	+4.5-----	16, fig. 6-79.
Q5-----	17, fig. 6-79-----	16, fig. 6-79-----	+4.5.
Q6-----	16, fig. 6-79-----	2, fig. 6-79-----	-4.5.
Q7-----	13, fig. 6-79-----	-4.5-----	18, fig. 6-79.
Q8-----	10, fig. 6-79-----	-4.5-----	19, fig. 6-79.
Q9-----	20, fig. 6-79-----	+4.5-----	21, fig. 6-79.
Q10-----	21, fig. 6-79-----	21, fig. 6-79-----	+4.5.
Q11-----	21, fig. 6-79-----	2, fig. 6-79-----	-4.5.
Q12-----	2, fig. 6-82-----	1, fig. 6-79-----	-4.5.
Q13-----	22, fig. 6-79-----	22, fig. 6-79-----	-4.5.
Q14-----	22, fig. 6-79-----	-----	6, fig. 6-79.
Q15-----	0-----	-----	5, fig. 6-79.
Q16-----	7, fig. 6-79-----	0-----	8, fig. 6-79.
Q17-----	14, fig. 6-73-----	0-----	8, fig. 6-79.
Q18-----	14, fig. 6-73-----	14, fig. 6-73-----	-4.5.
Q19-----	-----	-----	-4.5.
Q20-----	23, fig. 6-79-----	23, fig. 6-79-----	-4.5.

4-26. Panel 2A15, Troubleshooting

a. *Troubleshooting Chart.* Loop-back and modulate the TD-352/U test unit for this procedure.

Item. No.	Symptom	Probable trouble	Correction
1	No <i>main pcm</i> output at terminal 6.	Q21 defective	Check Q21.
2	Erroneous <i>main pcm</i> output at terminal 6.	DL2 defective	Check DL2.
3	No <i>rcvr aux address</i> output at terminal 15.	Q18 defective	Check Q18.
4	No <i>pcm from aux monitor</i> output at terminal 10.	Q20 or CR11 defective	Check waveform at emitter of Q20. If absent, check Q20. If present, check CR11
5	No <i>address inhibit 1</i> output at terminal 1 or <i>address inhibit 2</i> output at Terminal 8.	Q13, Q14, or Q15 defective	Check waveform at emitter of Q13. If absent, check Q13. If present, check Q14 and Q15.
6	Erroneous <i>address inhibit 1</i> and 2 outputs at terminals 1 and 8, respectively.	DL1 defective	Check DL1.
7	No <i>receive pam</i> output at terminal 23.	<p>a. Q12 defective</p> <p>b. Q10 and/or Q11 defective.</p> <p>c. Q1, Q2, Q3, and/or Q4 defective.</p> <p>d. Q5, Q6, or Q7 defective</p> <p>e. Q8 or Q9 defective</p>	<p>a. Check waveform at J2. If present, check Q12. If absent, proceed to b below.</p> <p>b. Check waveform at base of Q10 and Q11. If no waveform at either base, check waveform at J7. If no waveform at J7, proceed to c below. If waveform is present at J7 and also at base of Q11 (but not at base of Q10), proceed to d below. If waveform is present at J7 and also at base of Q10 (but not at base of Q11), proceed to e below. If waveforms appear good at bases of both Q10 and Q11 but not at J2, check Q10 and Q11</p> <p>c. Check operation of <u>A-A/B-B</u> gate circuit Q1, Q2, Q3, and Q4.</p> <p>d. Check waveform at collector of Q5. If present, check Q6 and Q7. If absent, check Q5.</p> <p>e. Check Q8 and Q9.</p>

a. *Troubleshooting Chart*-Continued

Item. No.	Symptom	Probable trouble	Correction
8	Dc level of <i>receive pam</i> output at terminal 23 does not shift when CTR (pam center adjust) potentiometer R19 is adjusted.	VR1, VR2, VR3, or R19 defective.	Check for +18 volts at terminal 1 of R19. If present, check R19. If absent, check VR1, VR2, and VR3.

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch to OUT.
- (5) 2 WIRE-4 WIRE switch to 4 WIRE:.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1-----	11, fig. 6-81-----	15, fig. 6-81-----	2, fig. 6-81.
Q2-----	13, fig. 6-81-----	16, fig. 6-81-----	2, fig. 6-81
Q3-----	14, fig. 6-81-----	-4.5-----	15, fig. 6-81
Q4-----	10, fig. 6-81-----	-4.5-----	16, fig. 6-81
Q5-----	17, fig. 6-81-----	+4.5,-----	18, fig. 6-81
Q6-----	18, fig. 6-81-----	+4.5-----	19, fig. 6-81
Q7-----	20, fig. 6-81-----	19, fig. 6-81-----	+4.5.
Q8-----	21, fig. 6-81-----	+4.5-----	22, fig. 6-81
Q9-----	9, fig. 6-81-----	22, fig. 6-81-----	+4.5.
Q10-----	19, fig. 6-81-----	19, fig. 6-81-----	-4.5.
Q11-----	22, fig. 6-81-----	22, fig. 6-81-----	-4.5.
Q12-----	1, fig. 6-81-----	12, fig. 6-81-----	-4.5.
Q13-----	23, fig. 6-81-----	23, fig. 6-81-----	-4.5.
Q14-----	23, fig. 6-81-----	24, fig. 6-81-----	6, fig. 6-81
Q15-----	0-----	24, fig. 6-81-----	3, fig. 6-81
Q18-----	8, fig. 6-81-----	7, fig. 6-81-----	-----
Q20-----	+0.3-----	+0.6-----	-4.5.
Q21-----	25, fig. 6-81-----	25, fig. 6-81-----	-4.5.

4-27. Panel 1A16/2A16, Troubleshooting

a. *Troubleshooting Chart.* The following procedures must be performed with panel 1A16/2A16 installed in both TD-352/U and TD-353/U test units. The test units must be looped-back (except for items 10 and 11) and one channel modulated.

Item. No.	Symptom	Probable trouble	Correction
1	No <i>h traffic pcm in mon</i> output at terminal 29 and no <i>med traffic pcm in mon</i> output at terminal 30. (TEST ALIGN meter on both TD-352/U and TD-353/U test units do not read in green area with METER SELECT switches set to PCM IN.)	Q1, C1, or CR1 defective	Check waveform at J4. If absent, check Q1. If present, check C1 and CR1
2	Simultaneous loss of <i>test tone</i> out across terminals 14 (No.1) and 19 (No.2), and <i>test tone monitoring</i> output at terminal 20.	Q2, Q3, Q4 and/or Q5 defective.	Check waveform at J6. If present, check Q5. If absent, check waveform at J1. If waveform at this point is absent, check Q2, Q3, and Q4. If J1 waveform is present, check R19, C5, R11, L1, C6, L2, and R12.
3	Loss of <i>test tone monitoring</i> output at terminal 20 only.	Detector circuit defective	Check C11, CR2, CR3, C12, and R18.
4	Loss of <i>test tone out</i> across terminal) 14 (No. 1) and 19 (No. 2) only.	T1 defective	Check T1.
5	No <i>detected audio measure</i> output at terminal 15.	Q17 detector circuit defective	Check C34 CR10, CR11 C35, and R49. If good, check Q17 and C33. If trouble persists, check T1.
6	No <i>earphone ampl</i> out at terminal 1.	Q18 or T4 defective	Check Q18, and if trouble persists, T4.
7	No <i>mike out</i> across terminals 7 (No. 1) and 6 (No. 2).	Q14, Q15, Q16, or T2 defective.	Check waveform at J2. If absent, check Q14, Q15, and Q16. If present, check C32, CR12, and R45. If trouble persists, check T2.
<i>Note.</i> Disconnect the pcm in to the test units for the following procedure.			
8	No <i>alarm relay</i> output at terminal 18, <i>alarm off</i> output at terminal 10, and <i>scquelch</i> output at terminal 11. (FRAME alarm buzzer and indicator lamp either always On or always off.)	Q11 Q12, Q13, Q9, or Q10 defective.	Check waveform at J2. If incorrect, check Q11 and Q12. If correct, check waveform at J3. If this signal is incorrect check Q13. If Q11, Q12, and Q13 are good, check Q9 and Q10.

Item. No.	Symptom	Probable trouble	Correction
9	Loss of <i>alarm relay</i> output at terminal 18 only. (Buzzer always on or always off.)	Q7 or Q8 defective	Check Q7 and Q8.

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME -26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector	Transistor	Base	Emitter	Collector
Q1-----	1, fig. 6-30	1, fig. 6-30	-4.5. ----	Q10-----	+9.5 -----	+9.8-----	+2.7.
Q2-----	+6.0-----	+6.3----	+0.3.----	Q11-----	-3.1 -----	-2.3-----	+25.0.
Q3-----	+0.3-----	+0.6----	-4.6. ----	Q12-----	-4.5 -----	-2.3-----	+25.0.
Q4-----	+0.1-----	+0.35--	-4.5. ----	Q13-----	-2.1 -----	-2.3-----	-2.3.
Q5.-----	0-----	+0.3----	-4.5. ----	Q14-----	0.-----	-0.7-----	+5.4.
Q6-----	+1.5-----	+1.8----	0.-----	Q15-----	+5.4 -----	+5.7-----	-3.3.
Q7-----	+1.9-----	+2.2----	0.-----	Q16-----	-3.3 -----	-3.0-----	-12.0.
Q8-----	+2.2-----	+2.5----	0.-----	Q17-----	+0.1 -----	+0.4-----	-4.5.
Q9-----	+16-----	-----	+1.5.----	Q18-----	+2.6 -----	+2.9-----	+1.6.

a Remove panel 1A8 or 2A8 (as applicable) for this measurement..

4-28. Panel 1A17, Troubleshooting

a. *Troubleshooting Chart.* In the following procedure, a faulty type 36 module can be detected by measuring the voltage at pins 4 and 8 (approximately +2 volts dc) and at the emitters of transistors Q1 and Q2 (greater than 1.5 volts).

Item. No.	Symptom	Probable trouble	Correction
1	<p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 1A8 mon A output at terminal 31 or 1A9 mon D output at terminal 29 remain at +1.1 volts when panels 1A8 and 1A9 are removed from the test unit to simulate faults in those panels.</p> <p><i>Note.</i> + 1.1 volt at terminals 31 and 29 is the correct condition to obtain a good panel (green) indication with TEST ALIGN meter connected and SERV SEL switch in A and D positions. (However, the +1.1-volt reading must be measured with TEST ALIGN meter out of the circuit.) With this symptom, panel 1A17 is providing a good panel output even though panels 1A8 and 1A9 have been simulated faulty by their removal.</p>	<p>Defective 1A8 mon A output circuit CR2, or defective 1A9 mon D output circuit CR6.</p> <p><i>Note:</i> If only one detector circuit were working (and output circuit were good) the voltage at terminal 31 or 29 would decrease to provide a bad panel indication on the TEST ALIGN meter.</p>	<p>Check CR2 or CR6.</p>
2	<p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 1A8 mon A output at terminal 31 is less than + 1.1 volts with a good panel 1A8 installed in TD-353/U test unit. (When TEST ALIGN meter is connected it does not read in green area with SERV SEL</p>	<p>One or more defective detector circuits Z2 through Z5 and/or associated buffer or inverter stages.</p>	<ol style="list-style-type: none"> a. Check waveform at J10. If absent, check Q3. If present, check applicable side of Z2. If this side checks good, proceed to b below. b. Check waveform at J9. If absent, check Q4. If present, check applicable side of Z2. If this side checks good, proceed to c below. c. Check waveform at J12. If absent, check R12. If

Item. No.	Symptom	Probable trouble	Correction
3	<p>switch in A position. Therefore, panel 1A17 is providing a bad panel output when panel 1A8 is good.)</p> <p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 1A9 <i>mon D</i> output at terminal 29 is less than +1.1 volts with a good 1A9 panel installed in TD-353/U test unit. (When TEST ALIGN meter is connected it does not read in green area with SERV SEL switch-in D position. Therefore,</p>	<p>Detector circuits Z1, Z7, and/or associated buffer, inverter, and flip-flop stages defective.</p>	<p>present, check applicable side of Z3. If this side checks good, proceed to d below.</p> <p>d. Check waveform at J11. If absent, check R13. If present, check applicable side of Z3. If this side also checks good, proceed to e below.</p> <p>e. Check waveform at J14. If absent, check Q5. If present, check applicable side of Z4. If this side checks good, proceed to f below.</p> <p>f. Check waveform at J13. If absent, check Q7 and Q6, If present, check applicable side of Z4. If this side also checks good, proceed to g below.</p> <p>g. Check waveform at J3. If absent, check Q10 and Q9. If present, check applicable aide of Z5, If this side checks good, proceed to h below.</p> <p>h. Check waveform at J1. If absent, check Q8. If present, check applicable side of Z5,</p> <p>a. Check waveform at J2. If absent, check Q2 and Q1. If present, check applicable side of Z1. If Z1 checks good proceed to b below.</p> <p>b. Check waveform at J5. If absent, check Z6 and Q12 If present, check applicable side of Z7. If this side checks good, proceed to c below</p> <p>c. Check waveform at J7. If absent, check R38. If present, check applicable Side of Z7.</p>

Item. No.	Symptom	Probable trouble	Correction
4	panel 1A17 is providing a bad panel output when panel 1A9 is good.) No 1A10 <i>mon C</i> output at terminal 16. (TEST ALIGN meter does not read in green area with SERV SEL switch in C position.)	CR5 or Q11 defective	Check CR5 and Q11.
5	No 1A9 <i>mon B</i> output at terminal 8. (TEST ALIGN meter does not read in green area with SERV SEL switch in B position.)	CR12, CR13, or Q22 defective.	Check CR12, CR13, and Q22.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1 c,e-----	15, fig. 6-84-----	15, fig. 6-84-----	-4.5.
Q2 c,e-----	15, fig. 6-84-----	0-----	2, fig. 6-84.
Q3 a-----	19, fig. 6-84-----	19, fig. 6-84-----	+4.5.
Q4 a-----	-2.1 -----	-2.0 -----	+ 4.5.
Q5 a-----	-3.1 -----	-3.0 -----	+4.5.
Q6 a-----	-1.6 -----	-1.7 -----	+4.5.
Q7 a-----	-1.7 -----	0-----	-1.2.
Q8 a-----	-3.2 -----	-2.7 -----	+4.5.
Q9 a,f -----	17, fig. 6-84-----	17, fig. 6-84-----	+4.5.
10 a -----	-1.7-----	0-----	-1.2.
Q11 b-----	12, fig. 6-84-----	12, fig. 6-84-----	-4.5.
Q12 c-----	14, fig. 6-84-----	14, fig. 6-84-----	+4.5.
Q22d-----	13, fig. 6-84-----	13, fig. 6-84-----	+4.5.

a SERV SEL switch at A; METER SELECT switch at SERV FAC.
 b SERV SEL switch at C; METER SELECT switch at SERV FAC.
 c SERV SEL switch at D; METER SELECT switch at SERV FAC.

d SERV SEL switch at B; METER SELECT switch d SERV FAC.
 e Terminal 15 terminated in 9 Fohm load.
 f Terminal 18 terminated in 91-ohm load.

TM 11-5805-367-35/3

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements TD-352/U made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	2	3	6	7	9	10
Z1 b -----	2, fig. 6-84-	-----	<+1.0 a ----	-----	-----	
Z2 c -----	19, fig. 6-84	-----	<+1.0 a ----	<+1.0 a--	-----	-2.0.
Z3 c -----	-1.5-----	-----	-----	-----	-----	-1.5.
Z4 c -----	-3.0-----	-----	<+1.0 a ----	<+1.0 a--	-----	-1.2.
Z5 c -----	-1.2-----	-----	<+1.0 a ----	<+1.0 a--	-----	-2.7.
Z6 b -----	-----	14, fig. 6-84	-----	-----	14, fig. 6-84-	-2.0.
Z7 b -----	-2.0-----	-----	<+1.0 a ----	<+1.0 a--	-----	-2.0.

a All inputs present and correct.

b SERV SEL switch at D; METER SELECT at SERV FAC.

c SERV SEL switch at A; METER SELECT at SERV FAC.

4-29. Panel 2A17, Troubleshooting

a. *Troubleshooting Chart.* In the following procedure, a faulty type 36 module can be detected by measuring the voltage at pins 4 and 8 (approximately +2 volts dc and at the emitters of transistors Q1 and Q2 (greater than 1.5 volt).

Item. No.	Symptom	Probable trouble	Correction
1	<p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 2A9 mon D output at terminal 29, 2A8 mon A output at terminal 31, or 2A8 mon C output at terminal 6 remain at +1.1 volt when panels 2A9 and 2A8 are removed from the test unit to simulate faults in those panels.</p> <p><i>Note.</i> + 1.1 volt at terminals 29, 31 and 6 is the correct condition to obtain a good panel (green) indication with TEST ALIGN meter connected and SERV SEL switch set to D, A, and/or C. (However, the 1.1-volt reading must be</p>	<p>Defective 2A9 mon D output circuit CR7, 2A8 mon A output circuit CRT, and/or 2A3 mon C output circuit CR4.</p> <p><i>Note.</i> If only one detector circuit were working (and output circuits were good), the voltages at terminals 29, 31, and/or 6 would decrease to provide a panel-bad indication on the TEST ALIGN meter.</p>	<p>Check CR7, CR1, or CR4.</p>

Item. No.	Symptom	Probable trouble	Correction
2	<p>measured with TEST ALIGN meter out of the circuit.) With this symptom, panel 2A17 is providing a good panel output even though panels 2A9 and 2A8 have been simulated faulty by their removal.</p> <p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 2A9 mon D output at terminal 29 is less than +1.1 volts with a good 2A9 panel installed in TD-352/U test unit. (When TEST ALIGN meter is connected it does not read in green area with SERV SEL switch set to D. Therefore, panel 2A17 is providing a bad panel output when panel 2A9 is good.)</p>	<p>One or more defective detector circuits Z6, Z9, Z7 and/or associated buffer or inverter stages.</p>	<ul style="list-style-type: none"> a. Check waveform at J17. If absent, check Q4 and Q3. If present, check applicable side of Z6, If this side checks good, proceed to b below. b. Check waveform at J18. If absent, check Q6 and Q5. If present, check applicable side of Z6, If this side is also good, proceed to c below. c. Check waveform at J5. If absent, check Q15. If present, check applicable side of Z9. If this side checks good, proceed to d below. d. Check waveform at J20. If absent, check Q14 and Q13. If present, check applicable side of Z9. If this side also checks good, proceed to e below. e. Check waveform at J3. If absent, check Q7. If present, check applicable side of Z7. If this side checks good, proceed to f below. f. Check waveform at J4. If absent, check Q8. If present, check applicable side of Z7.

Item. No.	Symptom	Probable trouble	Correction
3	<p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 2A8 <i>mon A</i> output at terminal 31 is less than + 1.1 volt with a good 2A8 panel installed in TD-352/U test unit. (When TEST ALIGN meter is connected, it does not read in green area with SERV SEL switch set to A. Panel 2A17 provides a bad panel output when panel 2A8 is good.)</p>	<p>Detector circuits Z1, Z2, Z3, and/or associated buffers defective.</p>	<ol style="list-style-type: none"> a. Check waveform at J9. If absent, check Q1. If present, check applicable side of Z1. If this side checks good, proceed to b below. b. Check waveform at J10. If absent, check R8 and Q2. If present, check applicable side of Z1. If this side also checks good, proceed to c below. c. Check waveform at J11. If absent, check R9. If present, check applicable side of Z2. If this side checks good, proceed to d below. d. Check waveform at J12. If absent, check R19. If present, check applicable side of Z2. If this side also checks good, proceed to e below. e. Check waveform at J13. If absent, check R16. If present, check applicable side of Z3. If this side checks good, proceed to f below. f. Check waveform at J14. If absent, check R17. If present, check applicable side of Z3
4	<p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 2A8 <i>mon C</i> output at terminal 6 is less than + 1.1 volts with a good panel 2A8 installed in TD-352/U test unit. (TEST ALIGN meter does not read in green area with SERV SEL switch set to C. Therefore, panel 2A17 is providing a bad panel output when panel 2A8 is good.)</p>	<p>Detector circuit Z5 and/or associated flip-flop Z4 defective.</p>	<ol style="list-style-type: none"> a. Check waveform at J16. If absent, check Z4. If present, check R25 and applicable side of Z5. If this side checks good, proceed to b below b. Check waveform at J15. If absent, check R24, R26. If present, check applicable side of Z5.

b. *Transistor Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1a-----	0.9 -----	-1.0. -----	+ 4.5.
Q2a-----	5, fig. 6-86 -----	5, fig. 6-86 -----	+4.5.
Q3b -----	21, fig. 6-86-----	21, fig. 6-86-----	+4.5.
Q4b -----	21, fig. 6-86-----	0-----	12, fig. 6-86
Q5b -----	20, fig. 6-86-----	20, fig. 6-86-----	+4.5.
Q6b -----	20, fig. 6-86-----	0-----	13, fig. 6-86.
Q7b -----	1, fig. 6-86 -----	1, fig. 6-86 -----	+4.6.
Q8b -----	17, fig. 6-86-----	2, fig. 6-86 -----	+4.5.
Q13b-----	19, fig. 6-86-----	19, fig. 6-86-----	-4.5.
Q14b-----	19, fig. 6-86-----	0-----	14, fig. 6-86.
Q15b-----	15, fig. 6-86-----	3, fig. 6-86 -----	+4.5.

a SERV SEL switch at A; METER SELECT switch at SERV FAC.

b SERV SEL switch at D; METER SELECT switch at SERV FAC.

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	2	5	6	7	10
Z1b-----	-1.0-----	-----	<+1.0a -----	<+1.0a ---	5, fig. 6-86.
Z2b-----	-1.5-----	-----	<+1.0a -----	<+1.0a ---	-1.5.
Z3b-----	-1.6-----	-----	<+1.0a -----	<+1.0a ---	-3.2.
Z4d-----	-1.7-----	16, fig. 6-86	-----	-----	-3.4.
Z5d-----	-3.4-----	-----	<+1.0a -----	<+1.0a ---	10, fig. 6-86.
Z6c-----	12, fig. 6-86	-----	<+1.0a -----	<+1.0a ---	13, fig. 6-86
Z7c-----	1, fig. 6-86-	-----	< + 1.0a ----	<+1.0a ---	2, fig. 6-86.
Z9c -----	3, fig. 6-86-	-----	<+1.0a -----	<+1.0a ---	14,fig. 6-86

a All Inputs to panel present and correct.

b SERV SEL switch at A; METER SELECT switch at SERV FAC.

c SERV SEL switch at D; METER SELECT switch at SERV FAC.

d SERV SEL switch at C; METER SELECT switch at SERV FAC.

4-30. Panel 1A18, Troubleshooting

a. *Troubleshooting Chart.* In the following procedure, a faulty type 36 module can be detected by measuring the voltage at pins 4 and 8 (approximately +2 volts dc and at the emitters of transistors Q1 and Q2 (greater than 1.5 volt).

Item. No.	Symptom	Probable trouble	Correction
1	<p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 1A13 mon H output at terminal 29 or 1A13 mon K output at terminal 9 remain at +1.1 volt when panel 1A13 is removed from the test unit to simulate a fault in that panel.</p> <p><i>Note.</i> + 1.1 volt at terminals 29 and/or 9 is the correct condition to obtain a good panel (green) indication with TEST ALIGN meter connected and SERV SEL switch set to H and/or K. (However, the 1.1-volt reading must be measured with TEST ALIGN meter out of the circuit.) With this symptom, panel 1A18 is providing a good panel output even though panel 1A13 has been simulated faulty by its removal.</p>	<p>Defective 1A13 mon H output circuit CR1, or defective 1A13 mon K output circuit CR4.</p> <p><i>Note.</i> If only one of above mentioned detector circuit were working (and output circuits were also good), the voltage at terminal 29 and/or 9 would decrease to provide a 1A13 bad panel indication on the TEST ALIGN meter.</p>	<p>Check CR1 or CR4.</p>
2	<p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 1A13 mon H output at terminal 29 is less than +1.1 volt with a good panel 1A13 installed in TD-353/U test unit. (When TEST ALIGN meter is connected, it does not read in green area with SERV SEL switch at H. Therefore, panel 1A18</p>	<p>One or more defective detector circuits Z1 through Z4 and/or associated buffer or inverter stages.</p>	<p>a. Check waveform at J10. If absent, check Q1. If present, check applicable side of Z1. If this side of Z1 checks good, proceed to b below.</p> <p>b. Check waveform at J9. If absent, check Q2. If present, check applicable side of Z1. If this side checks good, proceed to c below.</p> <p>c. Check waveform at J16. If absent, check Q3. If present, check applicable side</p>

Item. No.	Symptom	Probable trouble	Correction
3	<p>is providing a bad panel output when panel 1A13 is good.)</p> <p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 1A13 <i>mon K</i> output at terminal 9 is less than +1.1 volt with a good panel 1A13 installed in TD-353/U test unit. (When TEST ALIGN meter is connected, it does not read in green area with SERV SEL switch at K. Therefore, panel 1A18 is providing a bad panel output when panel 1A13 is good.)</p>	<p>Detector circuits Z4, Z6, and/or associated buffer and flip-flop stages defective</p>	<p>of Z2. If this side checks good, proceed to d below.</p> <p>d. Check waveform at J11. If absent, check R9. If present, check applicable side of Z2. If this side checks good, proceed to e below.</p> <p>e. Check waveform at J13. If absent, check Q5 and Q4. If present check applicable side of Z3. If this side checks good proceed to f below.</p> <p>f. Check waveform at J12. If absent, check R19. If present, check applicable side of Z3. If this side also checks good, proceed to g below.</p> <p>g. Check waveform at J4. If absent, check Q7 and Q6. If present, check applicable side of Z4.</p> <p>a. Check waveform at J1. If absent, check Q8. If present, check applicable side of Z4. If this side checks good, proceed to b below.</p> <p>b. Check waveform at J5. If absent, check Z5 and/or Q9. If present, check applicable side of Z6, If this side checks good, proceed to c below.</p> <p>c. Check waveform at J7. If absent, check Q10 If present, check applicable side of Z6.</p>
4	<p>No 1A7 <i>mon E</i> output at terminal 10. (TEST ALIGN meter does not read in green area with SERV SEL switch at E.)</p>	<p>Peak detector CR5, CR6, or preceding amplifier Q11 and/or buffer Q12 stages defective.</p>	<p>Check waveform at J15. If present, check CR5, CR6, and associated parts. If absent, check Q12 and Q11</p>

Item. No.	Symptom	Probable trouble	Correction
5	No 1A13 <i>mon M</i> output at terminal 7. (TEST ALIGN meter does not read in green area with SERV SEL switch at M.)	CR7, R45, R46, or C13 defective.	Check CR7, R45, R46, and C13.
6	No 1A10 <i>mon J</i> output at terminal 16. (TEST ALIGN meter does not read in green area with SERV SEL switch at J.)	CR8 or Q13 defective	Check CR8 and Q13.
7	No 1A12 <i>mon L</i> output at terminal 1. (TEST ALIGN meter does not read in green area with SERV SEL switch at L.)	Peak detector CR9, CR10, or preceding flip-flop Z7, and/or buffer Q14 defective.	Check waveform at J6. If present, check CR9, CR10, and associated parts. If absent, check Z7 and Q14.
8	No 1A12 <i>mon N</i> output at terminal 6. (TEST ALIGN meter does not read in green area with SERV SEL switch at N.)	Peak detector CR11, CR12, or buffer Q15 defective.	Check CR11, CR12, and Q15.

b. Transistor Terminal Voltages. The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references were to waveform- measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE TD-352/U WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1 a-----	-3.6 -----	-3.59-----	+4.5.
Q2 a-----	-3.6 -----	-3.5 -----	+4.5.
Q3 a-----	-1.6 -----	-1.7 -----	+4.5.
Q4 a-----	-1.7 -----	-1.8 -----	+4.5.
Q5 a-----	-----	0-----	-1.2.
Q6 a-----	-1.7 -----	1.8 -----	+4.5.
Q7 a-----	-----	0-----	-1.4.
Q8 b-----	20, fig. 6-88-----	1, fig. 6-88 -----	+4.5.
Q9 b-----	18, fig. 6-88-----	18, fig. 6-88-----	+4.5.
Q10 b-----	19,fig. 6-86-----	5, fig. 6-88 -----	+4.5.
Q11 c -----	+0.3-----	+1.7-----	-6.0.
Q12 c -----	-6.0 -----	5.8 -----	-12.0.
Q13 d-----	12,fig. 6-88-----	12, fig. 6-88-----	-4.5.
Q14 e-----	15, fig. 6-88-----	15, fig. 6-88-----	-4.5.
Q15 f-----	16, fig. 6-88-----	6, fig. 6-88 -----	-4.5

a SERV SEL switch of H; METER SELECT switch at SERV FAC.
 b SERV SEL switch at K; METER SELECT switch at SERV FAC
 c SERV SEL switch at E; METER SELECT switch at SERV FAC.

d SERV SEL switch at J; METER SELECT switch at SERV FAC.
 e SERV SEL switch at L; METER SELECT switch at SERV FAC.
 f SERV SEL switch at N; METER SELECT switch at SERV FAC.

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	2	3	6	7	9	10
Z1 -----	-3.59-----	-----	+2.2a-----	+2.2-----	-----	-3.5.
Z2 -----	-1.7-----	-----	+2.2a-----	+2.2-----	-----	-1.5.
Z3 -----	-1.2-----	-----	+2.2a-----	+2.2-----	-----	-1.6.
Z4 -----	-1.4-----	-----	+2.2a-----	-----	-----	1, fig. 6 88.
Z5 -----	-----	18, fig. 6-88--	-----	-----	18, fig. 6-88-	3, fig. 6-88
Z6 -----	3, fig. 6-88-	-----	-----	-----	-----	5, fig. 6-88
Z7 -----	-----	15, fig. 6-88--	-----	-----	15, fig. 6-88-	4, fig. 6-88

a Inputs to panel present and correct..

4-31. Panel 2A18, Troubleshooting

a. *Troubleshooting Chart.* In the following procedure, a faulty type 36 module can be detected by measuring the voltage at pins 4 and 8 (approximately +2 volts dc) and at the emitters of transistors Q1 and Q2 (greater than 1.5 volts).

Item. No.	Symptom	Probable trouble	Correction
1	<p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 2A13 mon H output at terminal 31, 2A13 mon K output at terminal 10, or 2A12 mon N output at terminal 3 remain at + 1.1 volt when panels 2A13 and 2A12 are removed from the test unit to simulate faults in those panels.</p> <p><i>Note.</i> + 1.1 volt at terminals 31,10, and 3 is the correct condition to obtain a good panel (green) indication with TEST ALIGN meter connected and SERV SEL switch set to H, K, and/or N. (However, the 1.1-volt reading must be measured with TEST ALIGN meter out of the circuit.) With this symptom, panel 2A18 is providing good panel output even though panels 2A13 and 2A12 have been simulated faulty by their removal.</p>	<p>Defective 2A13 mon H output circuit CR1, 2A13 mon K output circuit CR9, or 2A12 mon N output circuit CR13.</p> <p><i>Note.</i> If only one of above mentioned detector circuits were working (and output circuits were good) the voltage at terminal 31, 10, and/or 3 would decrease to provide a bad panel indication on the TEST ALIGN meter.</p>	<p>Check CR1, CR9, and/or CR13.</p>
2	<p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 2A13 mon H output at terminal 31 is less than +1.1 volt with a good 2A13 panel installed in TD-352/U test unit. (When TEST ALIGN meter is connected, it does not read in green area</p>	<p>One or more defective detector circuits Z1 through Z4 and/or associated buffer or inverter stages.</p>	<p>a. Check waveform at J10. If absent, check Q1. If present, check applicable side of Z1. If this side checks good, proceed to b below.</p> <p>b. Check waveform at J9. If absent, check Q2. If present, check applicable side of Z1. If this side also checks good, proceed to c below.</p>

Item No.	Symptom	Probable trouble	Correction
3	<p>with SERV SEL switch at H. Therefore, panel 2A18 is providing a bad panel output when panel 2A13 is good.)</p> <p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 2A13 <i>mon K</i> output at terminal 10 is less than +1.1 volt with a good 2A13 panel installed in TD-352/U test unit. (When TEST ALIGN meter is connected, it does not read in green area with SERV SEL switch set to K. Therefore, panel 2A18 is providing a panel-bad output when panel 2A13 is good.)</p>	<p>Detector circuit Z8 and/or associated flip-flop and buffer circuits defective.</p>	<p>c. Check waveform at J4. If absent, check Q4 and Q3. If present, check applicable side of Z2. If this side checks good, proceed to d below.</p> <p>d. Check waveform at J16. If absent, check Q6 and Q5. If present, check applicable side of Z2. If this side also checks good, proceed to e below.</p> <p>e. Check waveform at J12. If absent, check R20. If present, check applicable side of Z3. If this side checks good, proceed to f below.</p> <p>f. Check waveform at J11. If absent, check Q7. If present, check applicable side of Z3. If this side is also good, proceed to g below.</p> <p>g. Check waveform at J13. If absent, check R26. If present, check applicable side of Z4.</p> <p>a. Check waveform at J5. If absent, check Z7 and Q12. If present, check applicable side of Z8. If this side checks good, proceed to b below.</p> <p>b. Check waveform at J7. If absent, check Q13. If present, check applicable side of Z8.</p>

Item. No.	Symptom	Probable trouble	Correction
4	<p>With TEST ALIGN meter disconnected (METER SELECT switch set to any position except SERV FAC), 2A12 <i>mon N</i> output at terminal 3 is less than +1.1 volt with a good 2A12 panel installed in TD-352/U test unit. (When TEST ALIGN meter is connected, it does not read in green area with SERV SEL switch set to N. Therefore, panel 2A18 is providing a panel bad output when panel 2A12 is good.)</p>	<p>Detector circuit Z9 and/or associated buffer stages defective.</p>	<p>a. Check waveform at J8. If absent, check Q17. If present, check applicable side of Z9. If this side checks good, proceed to b below. b. Check waveform at J17. If absent, check Q18. If present, check applicable side of Z9.</p>
5	<p>No 2A12 <i>mon L</i> output at terminal 1. (TEST ALIGN meter reads in green area with SERV SEL switch set to L.)</p>	<p>Peak detector CR7, CR8, flip-flop Z6, or buffer Q11 defective.</p>	<p>Check waveform at J6. If present, check CR7 and CR8. If absent, check Z6, and Q11.</p>
6	<p>No 2A10 <i>mon B or J</i> output at terminal 16. (TEST ALIGN meter does not read in green area with SERV SEL switch set to B or J.) NOTE. Approximately +0.29 volt at terminal 16 is the current condition to obtain in a good panel (green) indication with test align meter connected and SERV SEL switch set to B. (However 0.29 volt reading must be measured with test align meter out of the circuit.) With this condition, panel 2A18 is provided good panel output even though panel 2A10 has been simulated faulty by its removal.</p>	<p>CR10 or Q14 defective</p> <p>NOTE. CR 10. defective (NSN 5805-00-916-5964).</p>	<p>Check CR10 and Q14.</p>
7	<p>No 2A7 <i>mon E</i> output at terminal 9. (TEST ALIGN mEter does not read in green area with SERV SEL switch set to E.)</p>	<p>Peak detector CR12, CR11 and/or amplifier Q15, Q16, defective.</p>	<p>Check waveform at J15. If present, check CR12 and CR11. If absent, check Q15 and Q16.</p>

b. *Transistor Terminal Voltages.* The transistor terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements with the AN/USM-140 under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Transistor terminal voltages are as follows:

Transistor	Base	Emitter	Collector
Q1a -----	7, fig. 6-90 -----	7, fig. 6-90 -----	+4.5.
Q2a-----	6, fig. 6-90 -----	6, fig. 6-90 -----	+4.5.
Q3a -----	18, fig. 6-90-----	18, fig. 6-90-----	+4.5.
Q4a-----	18, fig. 6-90-----	0-----	1, fig. 6-90
Q5a-----	12, fig. 6-90-----	12, fig. 6-90-----	+4.5.
Q6a..-----	12, fig. 6-90-----	0-----	13, fig. 6-90
Q7a-----	20, fig. 6-90-----	8, fig. 6-90 -----	+4.5.
Q11b-----	15, fig. 6-90-----	15, fig. 6-90-----	-4.5.
Q12c-----	17, fig. 6-90-----	17, fig. 6-90-----	-4.5.
Q13c-----	4, fig. 6-90 -----	4, fig. 6-90 -----	+4.5.
Q14d-----	11, fig. 6-90-----	11, fig. 6-90-----	-4.5.
Q15e -----	+ 0.4-----	+ 0.7-----	-1.0.
Q16e -----	+ 0.7-----	- 0.7 -----	-12.0.
Q17fg-----	5, fig. 6-90 -----	5, fig. 6-90 -----	+4.5.
Q18fh-----	14, fig. 6-90-----	14, fig. 6-90 -----	+4.5.

a SERV SEL switch at H; METER SELECT switch at a SERV FAC.
 b PCM IN connector removed (unit out of frame). SERV SEL switch at L; METER SELECT switch at a SERV FAC.
 c SERV SEL switch at K; METER SELECT switch at SERV FAC.

d SERV SEL switch at J; METER SELECT switch at SERV FAC.
 e SERV SEL switch at E; METER SELECT switch at SERV FAC.
 f SERV SEL switch at N; METER SELECT switch at SERV FAC.
 g Terminal 6 terminated in 91 ohm load.
 h Terminal 6 terminated in 91-ohm load.

c. *Module Terminal Voltages.* The module terminal voltages listed below were measured with respect to ground with the ME-26B/U and the figure references are to waveform measurements made with the oscilloscope under the following conditions:

- (1) Test multiplexer connected for loop-back operation.
- (2) One channel modulated with internal 1,100-cps test tone.
- (3) ADDRESS switch at MASTER.
- (4) AUX switch at OUT.
- (5) 2 WIRE-4 WIRE switch at 4 WIRE.
- (6) Module terminal voltages are as follows:

Module	2	3	6	7	9	10
Z1b-----	7, fig. 6-90-	-----	<+1.0 a-----	<+1.0 a----	-----	6, fig. 6-90
Z2b-----	18, fig. 6-90	-----	<+1.0 a-----	<+1.0 a----	-----	13, fig. 6-90
Z3b-----	-1.3-----	-----	<+1.0 a-----	<+1.0 a----	-----	8, fig. 6-90.
Z4b-----	-1.6-----	-----	<+1.0 a-----	-----	-----	-----
Z6c-----	-----	15, fig. 6-90	-----	-----	15, fig. 6-90-	-2.0.
Z7d-----	-----	17, fig. 6-90	-----	-----	17, fig. 6-90-	-2.0.
Z8d-----	2, fig. 6-90-	-----	<+1.0 a-----	<+1.0 a----	-----	4, fig. 6-90.
Z9e-----	5, fig. 6-90-	-----	<+1.0 a-----	<+1.0 a----	-----	14, fig. 6-90

a All Inputs to panel present and correct.

b SERV SEL switch at H; METER SELECT switch at SERV FAC.

c SERV SEL switch at L; METER SELECT switch at SERV FAC.

PCM IN connector removed (unit out of frame).

d SERV SEL switch at K; METER SELECT switch at SERV FAC.

e SERV SEL switch at N; METER SELECT switch at SERV FAC.

4-32. Panel 1A19/2A19, Troubleshooting

a. *Troubleshooting Chart.* To troubleshoot unregulated power supply 1A19/2A19, connect the receptacle end of the extender cable (fig. 4-1) to jack J1 on the rear of the power supply and connect the plug end of the extender cable into jack J40 in the panel 2A19 compartment of the TD-352/U or jack J60 in the panel 1A19 compartment of the TD-353/U.

Item. No.	Symptom	Probable trouble	Correction
1	Power supply causes AC POWER fuses on front panel of test unit to blow.	Short circuit across primary winding of power transformer T1, or one or more shorted rectifier circuit diodes.	a. Check 115-volt ac power input terminals 4 and 5 for shorted connector pins. b. Check rectifier diodes.
2	Simultaneous loss of all output voltages (AC POWER fuses good).	Open primary winding on T1.	Check dc resistance across terminals 1 and 2 of T1. If reading exceeds about 1 ohm, winding is defective.
3	One or more rectified output line fuses keep blowing.	Short circuit across output terminals of inoperative line.	a. Check for shorted connector pins of appropriate terminals. b. Check filter capacitors.
4	No output from one or more rectified output lines.	Associated secondary winding of T1, rectifier diodes, or filter choke winding open.	Check dc resistance of chokes and T1 secondary windings with values given in b below.

b. Dc Resistance of T1 Secondary Windings and Chokes.

Part	Measure across terminals	Dc resistance in ohms
T1	1 and 2	0.8
	3 and 5	1.0
	6 and 8	.5
	9 and 11	.2
	12 and 14	.4
	15 and 17	.2
L1	1 and 2	1.57
	3 and 4	.75
	5 and 6	.75
	7 and 8	.55
	9 and 10	.27

Section III. ALIGNMENT

4-33. General

a. General support alignment procedures for the TD-352/U and TD-353/U involve the following four internal adjustments on the multiplexer panels.

Adjustment	Panel
-5.2V	1A1/2A1
Phase adjust C1	1A6/2A6
Phase adjust R5	1A14A/2A14A
Phase adjust R06	1A14A/2A14A

b. The procedures given in paragraph 4-34 must be used after repair of either panel 1A1/2A1 or 1A6/2A6. The procedures given in paragraph 4-36 should be performed before and after repair of panel 1A14A/2A14A.

Note. After making these adjustments and before proceeding to the unit performance test, the direct support alignment procedure must be performed.

4-34. Panel 1A1/2A1, -5.2-Volt Regulated Output Voltage Adjustment

- Remove panel 1A1/2A1 from the test unit, and place it on the bench.
- Connect the extender cable (fig. 4-1) between jack J1 on the panel and jack J41 (TD-362/U test unit) or jack J61 (TD-353/U test unit).
- Remove the button plug on the left side of panel 1A1/2A1. This provides access to the -5.2-volt adjustment, potentiometer R53.
- Connect the TS-443/U between the front panel -5.2-volt test point (-) and terminal 10 of jack J1 (ground).
- Adjust the TS-443/U to the range giving the highest scale reading for -5.2 volts.
- Adjust potentiometer R53 for -5.2 ± 0.01 volts dc output.
- Perform the direct support alignment procedures given in paragraph 3-10.

4-35. Panel 1A6/2A6, Capacitor C1 Adjustment

- Install panel 1A6/2A6 on the extender panel.
- Connect the oscilloscope probe to jack J5 and ground the probe to terminal 30 of panel 1A6/2A6.
- Adjust PAM potentiometer R1 or R11, of one modem panel 1A2/2A2 to provide a positive going pulse at J5.
- Adjust capacitor C1 on 1A6/2A6 to give minimum ringing on leading edge of pam pulse without lowering the risetime of the pulse.
- Perform the complete direct support alignment procedure given in chapter 3.

4-36. Panel 1A14A/2A14A Adjustments

Adjust resistors R5 and R106 as follows.

- Install 15, 1A14A/2A14A on panel.
- Connect one channel of the AN/USM-140 to terminal 26 of J8 and the other channel to jack J3. Ground the AN/USM-140 probes to terminal 6 or J8.
- Adjust R5 so that the signal at J3 trails the signal at terminal 26 of J8 by 340 ± 10 ns in the TD-352/U, or 320 ns in the TD-353/U. The delay between the signals is measured on their negative going edges at the 50 % point of their peak-to-peak amplitude.
- Connect one channel of the AN/USM-140 to terminal 22 of J8 and the other channel to J7.
- Operate switch S1 on the 1A14A/2A14A panel to N.T.
- Adjust R106 so that the signal at J7 trails the signal at terminal 22 of J8 by 360 ± 10 ns in the TD-352/U or TD/353/U. The delay between the signals is measured on their negative going edges at the 50% point of their peak-to-peak amplitude.

CHAPTER 5

GENERAL SUPPORT TESTING PROCEDURES

5-1. General

a. These testing procedures are prepared for use by Electronics Field Maintenance Shops and Electronics Service Organizations responsible for general support maintenance of electronic equipment to determine the acceptability of repaired electronic equipment. These procedures set forth specific requirements that repaired electronic equipment must meet before it is returned to the using organization. The testing procedures may also be used as a guide for the testing of equipment that has been repaired at direct support if the proper tools and test equipment are available. Perform the physical test and inspection (para 5-4) on the TD-352/U or TD-353/U. Refer to paragraphs 5-5 and 5-6 to perform the unit performance test on the TD-352/U. Refer to paragraphs 5-7 and 5-8 to perform the unit performance test on the TD-353/U.

b. Each test depends on the preceding test for certain operating procedures. Comply with the instructions preceding each chart before proceeding to the chart. Perform each test in sequence. Do not vary the sequence. For each step, perform all the actions required in the *Control settings* columns; then perform each specific test procedure, and verify it against its performance standard.

5-2. Test Equipment, Materials, and Other Equipment

a. *General.* All test equipment, materials, and other equipment required to perform the testing procedures given in this section are listed in the following charts and were authorized under TA 11-17 and TA 11-100(11-17).

b. *Test Equipment.*

Nomenclature	Federal stock No.	Technical manual
Multiplexer TD-352/U ^a (two reqd).	5805-900-8199	TM 11-5805-367-12.
Multiplexer TD-353/U ^b (two reqd).	5805-900-8200	TM 11-5805-367-12.
Signal Generator SG-71/FCC.	6625-669-0255.	TM 11-5088.
Headset-Micro phone H-91A/U.	5965-699-6871.	TM 11-5805-367-12.
Headset HS-33/U	5965-170-4814.	

^a TD-352/U test only.

^b TD-353/U test only.

c. *Materials.*

Materials	Federal stock No.
Cable Assembly, Radio Frequency CG-1040B/U (5 at three reqd). 22 AWG wire ----- Resistor, 600 ohms, 1%	5995-913-0509

d. *Other Equipment.* Electric Light Assembly MX-1292/PAQ, FSN 6695-537-4470, TM 11-5540.

5-3. Modification Work Orders

The performance standards listed in the tests (para 5-5 and 5-7) assume that no modification work orders have been performed. A listing of current modification work orders will be found in DA Pam 310-1.

5-4. Physical Tests and Inspections

- a. *Test Equipment and Materials.* Electric Light Assembly MX-1292/PAQ.
- b. *Test Connections and Conditions.*
 - (1) Do not make any connections to the equipment.
 - (2) When repairs are completed and before reassembly of the equipment, perform the checks given in c below.
 - (3) Connect the MX-1292/PAQ to a 115-volt, 60-cps source, and install the wide band transmission filter.
- c. *Test Procedure.*

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	N/A-----	Controls may be in any position.	<ul style="list-style-type: none"> a. Inspect front panel for evidence of physical damage, loose or missing parts, screws, or panel fasteners. b. Inspect connectors and plugs for cleanliness and evidence of physical damage. c. Remove and check all fuses for proper size and amperage rating. d. Check all filter capacitors for evidence of overheating. e. Check all resistors for evidence of overheating. f. Inspect all wiring and cabling for worn or frayed insulation. g. Inspect all metal surfaces for conditions of finish. Note. Touchup paint is recommended instead of refinishing whenever practical (TB SIG 364). 	<ul style="list-style-type: none"> a. Front panel is complete and not damaged. b. Connectors and plugs are clean and not damaged. c. Fuses are properly sized and rated as indicated on panel markings. d. Capacitors show no evidence of leakage. e. Resistors show no signs of discoloration due to overheating. f. Wiring and cabling are free of cuts and frays. g. All metal surfaces intended to be painted do not show bare metal. Panel lettering is legible.

2	N/A	Controls may be in any position.	Check the equipment for applicable modification work orders. (Refer to DA Pam 310-4 for a list of MWO's.)	If MWO is performed, MWO number appears on equipment.
3	<p><i>MX-1292/PAQ</i></p> <p>245V FOR M.V. LAMP: ON.</p>	Controls may be in any position.	<p>a. Expose equipment to direct rays of MK-1292/PAQ, and inspect condition of moisture-fungiproofing epoxy.</p> <p><i>Note.</i> Moisture-fungiproofing appears blue-green under rays of MX-1292/PAQ. Epoxy appears milky-white, but blue-gray if defective.</p> <p>b. Operate MX-1292/PAQ 245V FOR M.V. LAMP switch to OFF.</p>	<p>a. All components, wiring, and chassis surfaces are completely covered with moisture-fungiproofing epoxy with no evidence of it on connectors or switch contacts.</p> <p><i>Note.</i> Do not apply moisture-fungiproofing or epoxy to parts not originally treated with it.</p> <p>b. None.</p>

5-5. Performance Tests (TD-352/U)

(fig. 5-1)

a. Test Equipment and Materials.

- (1) Multiplexer TD-352/U (two required).
- (2) Signal Generator SG-71/FCC.
- (3) Headset-Microphone H-91A/U.
- (4) Headset HS-33/U
- (5) Cable Assembly, Radio Frequency, CG-1040B/U (three required).

(6) Voltmeter Meter ME-30B/U.

b. Test Connections and Conditions. Loop-back the TD-352/U pcm and timing connections as shown in figure 15, Do not connect the second TD-352/U test unit, SG-71/FCC, or H-91A/U. until told to do so.

Note 1. When testing panel 1A2/2A2, always install panel 1A2/2A2 in channel 1, 3 position.

Note 2. When testing panel 2A10, the procedures in steps 1 and 2 must be performed twice; once with panel 2A10 in the receive side of the TD-352/U and once with panel 2A10 in the transmit side of the TD-352/U.

c. Test Procedures.

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	<p><i>TD-352/U test unit:</i> AC POWER: OFF Install 1A6/2A6 coder panel in the coder align panel. Turn TD-352/U AC Power ON.</p>		<p><i>Transmit timing and transmit timing fault locator tests.</i></p> <ul style="list-style-type: none"> a. Adjust oscilloscope a horizontal swap of 0.5 μsec/cm and a vertical deflection of 2.0 V/cm. b. Connect oscilloscope probe to PCM OUT connector on front panel of test unit, and connect oscilloscope external trigger to Scope Sync connector on test unit. c. Adjust coder align panel potentiometer from -2.5 to +2.5 VDC. d. Turn TD-352/U test unit AC POWER to OFF. Remove coder align panel and reinstall 1A6/2A6 panel in test unit. Turn test unit AC Power ON. 	<ul style="list-style-type: none"> a. None b. None. c. Verify on oscilloscope a binary count from 0(000000) thru 63 (111111). If binary count is missing, assume 1A6/2A6 panel is inoperative. d. None

c. Test Procedure-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1.1	<p><i>TD-352/U test unit:</i> AC POWER: ON METER SELECT: SERV FAC ADDRESS: MASTER AUX: OUT 2 WIRE-4 WIRE: 4 WIRE CHAN I-12: OFF <i>Second TD-352/U:</i> AC POWER: OFF</p>		<p>a. Set SERV SEL switch (primary TD-352/U) to A. b. Set SERV SEL switch to C- c. Connect SYNC OUT XMTR output of second TD-352/U to SYNC IN input of primary TD-352/U test unit. d. Set AC POWER switch of second TD-352/U to ON. e. Set METER SELECT switch (primary TD-352/U) to SYNC IN. f. Set METER SELECT switch to SERV FAC. g. Set SERV SEL switch to A h. Set SERV SEL switch to C i. Set AC POWER switch of second TD-352/U to OFF. j. Set SERV SEL switch (primary TD-352/U) to D. k. Set METER SELECT switch to TIMING IN. l. Connect SYNC OUT XMTR output of primary TD-352/ if test unit to SYNC IN input of second TD-352/U. m. Set AC POWER switch of second TD-352/U to ON.</p>	<p>a. TEST ALIGN meter reads in green area. b. TEST ALIGN meter reads in green area. c. None. d. None. e. TEST ALIGN meter reads in green area. f. None. g. TEST ALIGN meter reads in green area. h. TEST ALIGN meter reads in green area. i. None. j. TEST ALIGN meter reads in green area. k. TEST ALIGN meter reads in green area. l. None. m. None.</p>

c. Test Procedures-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
			<p><i>n.</i> Set METER SELECT switch of second TD-352/U to SYNC IN.</p> <p><i>o.</i> Set AC POWER switch of second TD-352/U to OFF.</p> <p><i>p.</i> Set METER SELECT switch (primary TD-352/U) to SERV FAC.</p> <p><i>q.</i> Set SERV SEL switch to B</p> <p><i>r.</i> Set SERV SEL switch to OSC.</p> <p><i>s.</i> Adjust OSC ADJUST control for hairline indication on TEST ALIGN meter.</p> <p><i>t.</i> Set SERV SEL switch to CHAN 1-12 position.</p>	<p><i>n.</i> TEST ALIGN meter of second TD-352/U reads in green area.</p> <p><i>o.</i> None.</p> <p><i>p.</i> None.</p> <p><i>q.</i> TEST ALIGN meter reads in green area.</p> <p><i>r.</i> None.</p> <p><i>s.</i> None.</p> <p><i>t.</i> None.</p>

Step No	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
			<p>u. In sequence, set CHAN 1-12 switch to positions 1 through 12, observing TEST ALIGN meter reading for each position.</p> <p>r. Set CHAN 1-12 switch to 1</p>	<p>u. TEST ALIGN meter reads on or near hairline for each channel.</p> <p>r. None.</p>
2	No changes required		<p><i>Receive timing and receive timing fault locator tests</i></p> <p>a. Set SERV SEL switch (primary TD-352/U) to H.</p> <p>b. Set SERV SEL switch to K</p> <p>c. Set SERV SEL switch to J.</p> <p>d. Disconnect CG-1040B/U from PCM IN connector.</p> <p>e. Set SERV SEL switch to M</p> <p>f. Reconnect CG-1040B/U to PCM IN connector.</p> <p>g. Set METER SELECT switch to TIMING IN.</p> <p>h. Connect SYNC OUT RCVR output of primary TD-352/U test unit to SYNC IN input of second TD-352/U.</p> <p>i. See that METER SELECT switch of second TD-352/U is set to SYNC IN.</p> <p>j. Set AC POWER switch of second TD-352/U to ON.</p> <p>k. Set AC POWER switch of second TD-352/U to OFF</p>	<p>a. TEST ALIGN meter reads in green area.</p> <p>b. TEST ALIGN meter reads in green area.</p> <p>c. TEST ALIGN meter reads in green area.</p> <p>d. Buzzer sounds and FRAME indicator lights.</p> <p>e. TEST ALIGN meter reads in green area.</p> <p>f. Buzzer stops, FRAME indicator extinguishes, and TEST ALIGN meter reading drops to left of green area.</p> <p>g. TEST ALIGN meter reads in green area.</p> <p>h. None.</p> <p>i. None.</p> <p>j. TEST ALIGN meter of second TD-352/U reads in green area.</p> <p>k. None.</p>

Step No	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
3	<p>Same as step 1 except: SG-71/FCC Power ON: ON RANGE: X10 Tuning vernier: 110 AMPLITUDE:-4 dbm MOD. BAL.- BAL. UNBAL BAL.</p> <p><i>Note.</i> Precise setting of 1,100 cps not critical. (Dial setting is sufficient; frequency measurement not necessary.)</p>		<p><i>Modulator, sample and store, coder timing, coder pam monitor, noise generator, and noise generator monitor tests</i></p> <p>a. Set CHAN 1-12 switch to OFF and connect 1,100 cps BAL. OUTPUT of SG-71/FCC to pins A and B of AUDIO CHAN connector 1-4 (audio in 1 for channel 1).</p> <p>b. Set METER SELECT switch to SERV FAC.</p> <p>c. Set SERV SEL switch to E.</p> <p>d. Remove 1,100-cps tone.</p> <p>e. Reconnect 1,100-cps tone.</p> <p>f. Set METER SELECT switch to NOISE GEN.</p> <p>g. Connect 1,100-cps BAL. OUTPUT of SG-71/FCC to pins E and F of AUDIO CHAN connector 1-4 (audio in 2 for channel 3).</p> <p>h. Set METER SELECT switch to SERV FAC.</p> <p>i. See that SERV SEL switch is set to E.</p>	<p>a. None.</p> <p>b. None.</p> <p>c. TEST ALIGN meter reads in green area.</p> <p>d. TEST ALIGN meter reads out of green area.</p> <p>e. None.</p> <p>f. TEST ALIGN meter reads in green area.</p> <p>g. None.</p> <p>h. None.</p> <p>i. TEST ALIGN meter reads in green area.</p>
4	No changes required.		<p><i>Pcm in traffic detector, coder, pcm output, and transmit and receive address tests</i></p>	

		<p>a. Set METER SELECT switch to PCM IN.</p> <p>b. Disconnect CG-1040B/U from PCM IN connector.</p> <p>c. Reconnect CG-1040B/U to PCM IN connector.</p> <p>d. Set ADDRESS switch to SLAVE.</p> <p>e. Set METER SELECT switch to SERV FAC.</p> <p>f. Set SERV SEL switch to F</p> <p>g. Connect Headset HS-33/U to pins G and H of AUDIO CHAN connector 1-4 (audio out 2 for channel 3) and listen to 1-100-cps tone.</p> <p>h. Remove modulation and listen to channel.</p> <p>i. Reconnect modulation to pins A and B of AUDIO CHAN connector 1-4 (audio in 1 for channel 1).</p>	<p>a. TEST ALIGN meter reads in green area.</p> <p>b. No reading on TEST ALIGN meter.</p> <p>c. None.</p> <p>d. Test unit frames-in on SLAVE (2 kc) address; TEST ALIGN meter reads in green area Unit may go into alarm, but only momentarily.</p> <p>e. None.</p> <p>f. TEST ALIGN meter reads in green area.</p> <p>g. 1,100-cps tone is clear and free of distortion.</p> <p>h. Channel is free of random clicks.</p> <p>i. None.</p>
5	No changes required.	<p><i>Pcm input and pcm monitoring tests</i></p> <p>a. Set SERV SEL switch to L</p> <p>b. Disconnect CG-1040B/U from PCM IN connector.</p>	<p>a. None.</p> <p>b. TEST ALIGNMENT meter reads in green area, buzzer sounds, and FRAME indicator lights.</p>

Step No	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
			c. Reconnect CG-1040B/U to PCM IN connector. d. Set SERV SEL switch to N.	c. Buzzer stops, FRAME indicator extinguishes, and no reading on TEST ALIGN meter. d. TEST ALIGN meter reads in green area.
6	Adjust output of Sg-71/FCC to -4.0 dbm for steps b and f.		<i>Decoder, demodulator, and audio measure tests</i> a. Set SERV SEL switch to CHAN 1-12. b. Set CHAN 1-12 switch to OFF. c. Reconnect ME-30B/U and 600 ohm resistor to pins C and D of AUDIO CHAN connector 1-4 (AUDIO OUT-1 for channel 1). d. Reconnect Headset HS-33/U to pins C and D of AUDIO CHAN connector 1-4 and listen to 1,100 Hz tone. e. Remove 1100 Hz input to pins A and B and Headset HS-33/U from pins C and D of AUDIO CHAN connector 1-4.	a. None. b. None. c. ME-30B/U to read -4 ± 1 dbm <i>Note.</i> Performance is affected by setting of demodulator gain control. Test unit demodulators should be set to give hairline readings on TEST ALIGN meter in loop-back condition. If a type 1A2/2A2 panel is being checked after repair, its gain setting may not give hairline reading under loop-back conditions. d. Audio tone is clear and free of distortion. e. ME-30B/U reads less than -20 dbm

Step No	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
			<p>f. Connect 1100 Hz input to pins E and F of AUDIO CHAN connector 14 (AUDIO IN-2 for Channel 3)</p> <p>g. Reconnect ME-30B/U and 600 ohm resistor to pins G and H of AUDIO CHAN connector 1-4 AUDIO OUT-2 for Channel 3).</p> <p>h. None.</p> <p>i. Reconnect Headset HS-33/U to pins G and H of AUDIO CHAN connector 14 and listen to 1100 Hz tone</p> <p>j. Remove 1 100 Hz input to pins E and F and Headset HS-33/U from pins G and H of AUDIO CHAN connector 1-4.</p>	<p>f. None</p> <p>g. ME-30B/U reads 4+ 1 dbm</p> <p>h. None.</p> <p>i. Audio tone is clear and free of distortion.</p> <p>j. ME-30B/U reads less than. -20 dbm</p>

Step No	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
7	No changes required.		<p><i>NOTE:</i> Before performing this test, insure that the TEST ALIGN meter indicates within the green area when SERV SEL switch is in position-G; if the meter does not indicate within the green area adjust common channel level potentiometer (R6) on panel 1A6/2A6.</p> <p><i>Pcm from aux monitoring tests</i></p> <p>a. Disconnect loop-back cable between PCM IN and PCM OUT connectors.</p> <p>b. Connect lead between PCM OUT connector and pin C on the TO AUX connector.</p> <p>c. Set METER SELECT switch to PCM FROM AUX.</p> <p>d. Reconnect PCM IN to PCM OUT connector.</p>	<p>a. None.</p> <p>b. None.</p> <p>c. TEST ALIGN meter reads in green area.</p> <p>d. None.</p>
8	No changes required.		<p><i>Frame alarm and squelch tests</i></p> <p>a. Disconnect CG-1040B/U from PCM IN connector.</p> <p>b. Depress BUZZER OFF switch.</p> <p>c. Reconnect CG-1040B/U to PCM IN connector.</p> <p>d. Depress BUZZER OFF switch again.</p>	<p>a. FRAME indicator lights, buzzer sounds, and 1,100-cps tone on channel 1 ceases.</p> <p>b. Buzzer ceases, but FRAME indicator stays lighted, and tone stays off.</p> <p>c. FRAME indicator extinguishes and 1,100-cps tone resumes.</p> <p>d. Buzzer does not sound.</p>

Step No	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
9	Same as step 1, except second TD-352/U not required.		<p><i>Test tone and test tone monitor tests</i></p> <p>a. Disconnect SG-71/FCC Headset HS-33/U ME-30B/U, and 600 ohm resistor from AUDIO CHAN 1-4 connector.</p> <p>b. Set SERV SEL switch to OSC.</p> <p>c. Set METER SELECT switch to SERV FAC.</p> <p>d. Adjust OSC ADJUST control for hairline indication on TEST ALIGN meter.</p> <p>e. Reset SERV SEL switch to CHAN 1-12 position.</p> <p>f. Set CHAN 1-12 switch to position 1.</p>	<p>a. None.</p> <p>b. None.</p> <p>c. None.</p> <p>d. Meter pointer of TEST ALIGN meter can be set for hairline reading.</p> <p>e. None.</p> <p>f. TEST ALIGN meter reads on or near hairline. See note in step 6c above.</p>
10	No changes required.		<p><i>Microphone and earphone amplifier tests</i></p> <p>a. Connect Headset-Microphone H-91A/U to Talk MONITOR connector.</p> <p>b. Listen for internal 1,100-cps tone.</p> <p>c. Set SERV SEL switch to PHONE and hum or speak into microphone of H-91A/U.</p>	<p>a. None.</p> <p>b. 1,100-cps tone can be heard clear and undistorted on headset.</p> <p>c. Disconnect ME-30B/U from SG-71/FCC. Reconnect ME-30B/U to AUDIO CHAN 1-4, pins A and B. Observe pointer fluctuation on ME-30B/U while speaking into microphone of H-91A/U.</p>

11 TD-352/U test unit:
AC POWER: ON
METER SELECT:
SERV FAC
ADDRESS:
MASTER
AUX: OUT
Second TD-352/U:
AC POWER: ON

Channel gain adjustment

Note: Each panel 1A2/2A2 in the TD-352/U (TD-353/U) contains two channels. The channel number assigned to a panel are located on the frame below each panel. The lower number channel and its associated controls are physically located on the bottom half of the panel.

- a. Establish order-wire communication through the link (TM 11-5805-367-12, para 3-6).
- b. Adjust the TD-352/U OSC ADJUST control at both terminals for a center hairline indication on the TEST ALIGN meter.
- c. Operate the TD-352/U SERV SEL switch at both terminals to CHAN 1-12 (vertical up)

Note. The procedures given in (d) through (g) below must be performed simultaneously at both terminals. This is necessary because the signal used for the adjustment at one end of the link is generated at the other end of the link.

- d. Operate the TD-352/U 2 WIRE-4 WIRE switch at both terminals to the position corresponding to the type of line or trunk (2- or 4-wire) connected to channel 1.
- e. Operate the TD-352/U CHAN 1-12 switch at both ends of the link to 1.

Step No	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
			<p>f. Adjust the TD-352/U AG control for channel 1 at both ends of the link for a center hairline indication on the TEST ALIGN meter.</p> <p>g. Perform the procedures given in (d) through (f) above for each channel of the TD-352/U's.</p> <p>h. Perform cross-talk check in paragraph 5-5, step 12, a through e.</p>	
12	No changes required.		<p><i>Cross-talk check .</i> <i>Note.</i> This check is performed on the TD-352/U after each installation, prior to any operation, once each 24 hours of operation, and immediately after replacement of panel assemblies.</p> <p>a. Perform procedures in step 11, above prior to proceeding to next step.</p> <p>b. Operate the TD-352/U CHAN 1-12 switch at both ends of link to 1.</p> <p>c. Perform procedure b above for each channel of the TD-352/U.</p>	<p>b. Audio tone is clear on channel 1. No audio tone on other channels at both terminals.</p>

- | | | | |
|--|--|--|--|
| | | <p>d. If cross talk is heard, loosen plug-in panel retaining bars (TM 11-5805-367-35/3, fig. 3-10, 3-11), reseal all plug-in panels, then tighten plug-in panel retaining bars.</p> <p>e. Repeat step b. If cross talk is still present, remove the TD-352/U from system and return it to next higher level maintenance.</p> | |
|--|--|--|--|

5-6. Summary of Performance Standard (TD-352/U)

Step No.	Description	Performance standard	Test data
	<i>Transmit timing and transmit timing fault locator tests</i>		
1a	Panel 2A8 timing signals (SERV SEL switch: A). ' area.	TEST ALIGN meter reads in green area.	
1b	Panel 2A8 timing signals (SERV SEL switch: C). area.	TEST ALIGN meter reads in green area.	
1e	Panel 2A8 external sync in monitor (METER SELECT: SYNC IN).	TEST ALIGN meter reads in green area.	
1g	Panel 2A8 timing signals using external sync input (SERV SEL switch: A).	TEST ALIGN meter reads in green area.	
1h	Panel 2A8 timing signals using external sync input (SERV SEL switch: C).	TEST ALIGN meter reads in green area.	
1j	Panel 2A9 timing signals (SERV SEL switch: D).	TEST ALIGN meter reads in green area.	
1k	Panel 2A9 TIMING: OUT signal (METER SELECT switch: TIMING OUT).	TEST ALIGN meter reads in green area.	
1n	Panel 2A9 SYNC OUT XMTR signal (METER SELECT switch of second TD-352/U set to SYNC IN).	TEST ALIGN meter (of second TD-352/U) reads in green area.	
1q	Panel 2A10 timing signals (SERV SEL switch: B).	TEST ALIGN meter reads in green area.	
1u	Panel 2A10 modem timing signals (all channels modulated).	TEST ALIGN meter reads on or near hairline.	
	<i>Receive timing and receive timing fault locator tests</i>		
2a	Panel 2A13 timing signals (SERV SEL switch: H).	TEST ALIGN meter reads in green areas.	
2b	Panel 2A13 timing signals (SERV SEL switch: K).	TEST ALIGN meter reads in green area.	
2c	Panel 2A10 timing signals (SERV SEL switch: J).	TEST ALIGN meter reads in green area.	
2d	Panel 2A13 skip pulse activity -----	Buzzer sounds and FRAME indicator lights.	
2e	Panel 2A13 skip pulse monitoring (SERV SEL switch: M).	TEST ALIGN meter reads in green area.	
2f	Panel 2A13 framing -----	Buzzer stops, FRAME indicator extinguishes, no reading on TEST ALIGN meter.	
2g	Panel 2A13 TIMING IN monitor (METER SELECT switch: TIMING IN).	TEST ALIGN meter reads in green area.	
2j	Panel 2A13 SYNC OUT RCVR output(METER SELECT switch of second TD-352/U set to SYNC IN).	TEST ALIGN meter (of second TD-352/U) reads in green area.	

Step No.	Description	Performance standard	Test data
3c	<p><i>Modulator, sample and store, coder timing, coder pam monitor, noise generator, and noise generator monitor tests</i></p> <p>Panel 1A2/2A2 modulator channel 1, panel 2A7 coder pam monitor (SERV SEL switch: E).</p>	TEST ALIGN meter reads in green area.	
3d	Panel 2A18 coder pam fault detector (modulation removed).	TEST ALIGN meter reads out of green area.	
3f	Panel 1A11/2A11 noise generator (METER SELECT switch: NOISE GEN).	TEST ALIGN meter reads in green area.	
3i	Panel 1A2/2A2 modulator channel 3 (SERV SEL: E).	TEST ALIGN meter reads in green area.	
4a	<p><i>Pcm in traffic detector coder, pcm output, and transmit and receive address tests</i></p> <p>Panel 1A6/2A6 pam to pcm converter, panel 2A5 pcm retiming and comparator control, and panel 1A3/2A3 pcm output (METER SELECT: PCM IN).</p>	TEST ALIGN meter reads in green area.	
4b	Panel 1A16/2A16 pcm in traffic detector	No reading on TEST ALIGN meter.	
4d	Panel 1A3/2A3 address insertion and panel 1A12/2A12 address detection (ADDRESS switch from MASTER to SLAVE).	Test unit frames in TEST ALIGN meter reads in green area. Unit may go into alarm, but only momentarily.	
4f	Panel 1A3/2A3 transmit address monitor (SERV-SEL switch: F).	TEST ALIGN meter reads in green area.	
4g	Panel 1A6/2A6 pam-pcm conversion (modulated channel).	Test tone is clear and free of distortion.	
4h	Panel 1A6/2A6 pam-pcm conversion (unmodulated channel).	Channel is free of random clicks.	
5b	<p><i>Pcm input and pcm input monitoring test</i></p> <p>Panel 1A12/2A12 skip-pulse generator (PCM IN connector removed, SERV SEL switch: L).</p>	TEST ALIGN meter reads in green area. Buzzer sounds. FRAME indicator lights.	
5c	Panel 1A12/2A12 framing	Buzzer stops. FRAME indicator extinguishes. No reading on TEST ALIGN meter.	
5d	Panel 1A12/2A12 pcm input (SERV SEL switch: IN).	TEST ALIGN meter reads in green area.	

Step No.	Description	Performance standard	Test data
6c 6d 6e 6i 6j	<p><i>Decoder, demodulator, and audio measure circuits</i></p> <p>Panel 1A16/2A16 audio measure detector, channel 1.</p> <p>Panel 1A14/2A14 pcm to pam converter, panel 2A15 expander circuit, and panel 1A2/2A2 demodulator circuit (demodulated audio output monitored at AUDIO CHAN connector, channel 1).</p> <p>Panel 1A16/2A16 audio measure detector (modulating tone removed).</p> <p>Panel 1A2/2A2 audio measure, channel 3</p> <p>Panel 1A2/2A2 demodulated audio output monitored at AUDIO CHAN connector, channel 3.</p>	<p>TEST ALIGN meter reads on or near hairline.</p> <p>Audio tone is clear and free of distortion.</p> <p>No reading on TEST ALIGN meter.</p> <p>TEST ALIGN meter reads on or near hairline.</p> <p>Audio tone is clear and free of distortion.</p>	
7c	<p><i>Pcm from aux monitoring test</i></p> <p>Panel 2A15 pcm from aux monitor (METER SELECT switch: PCM FROM AUX).</p>	<p>TEST ALIGN meter reads in green area.</p>	
8a 8b 8c 8d	<p><i>Frame alarm and squelch test</i></p> <p>Panel 1A16/2A16 alarm and squelch circuit.</p> <p>Depress BUZZER OFF switch</p> <p>PCM IN signal connected</p> <p>Depress BUZZER OFF switch again</p>	<p>FRAME indicator lights, buzzer sounds, 1,100-cps tone ceases.</p> <p>Buzzer ceases, FRAME indicator remains lighted, and tone stays off.</p> <p>FRAME indicator extinguishes and 1,100-cps tone resumes.</p> <p>Buzzer does not sound.</p>	
9d 9f	<p><i>Test tone and test tone monitor test</i></p> <p>Panel 1A16/2A16 test tone oscillator (OSC ADJUST control adjusted).</p> <p>Panel 1A16/2A16 test tone monitor (CHAN 1-12 switch: 1).</p>	<p>TEST ALIGN meter pointer can be set for hairline reading.</p> <p>TEST ALIGN meter reads on or near hairline.</p>	
10b 10c	<p><i>Microphone and earphone amplifier test</i></p> <p>Panel 1A16/2A16 earphone amplifier (internal tone monitored).</p> <p>Panel 1A16/2A16 microphone amplifier (demodulated speech monitored on TEST ALIGN meter).</p>	<p>1,100-cps tone is clear and undistorted.</p> <p>TEST ALIGN meter pointer fluctuates between no and green area reading.</p>	

5-7. Performance Tests (TD-353/U)

(fig. 5-2)

a. Test Equipment and Materials.

- (1) Multiplexer TD-353/U (two required).
- (2) Signal Generator SG-71/FCC.
- (3) Headset-Microphone H-91A/U.
- (4) Headset HS-33/U.
- (5) Cable Assembly, Radio Frequency, type CG-1040B/U (three required).

b. Test Connections and Conditions. Loop-back the TD-353/U pcm and timing connections as shown in figure 5-2. Do not connect the second TD-353/U test unit, SG-71/FCC, or H-91A/U until told to do so.

Note 1. When testing panel 1A2/2A2, always install panel 1A2/2A2 in channel 1, 3 position.

Note 2. When testing panel 1A10, the procedures in steps 1 and 2 must be performed twice; once with panel 1A10, in the receive side of the TD-353/U and once with panel 1A10, in the transmit side of the TD-353/U.

c. Test Procedures.

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	<p><i>TD-353/U test unit:</i> AC POWER: ON METER SELECT: SERV FAC ADDRESS: MASTER AUX: OUT 2 WIRE-4 WIRE: 4 WIRE</p> <p><i>Second TD-353/U:</i> AC POWER: OFF</p>		<p><i>Transmit timing and transmit timing fault locator tests</i></p> <p>a. Set SERV SEL switch (primary TD-353/U) to A.</p> <p>b. Connect SYNC OUT XMTR output of second TD-353/U to SYNC IN input of primary TD-353/U test unit.</p> <p>c. Set AC POWER switch of second TD-353/U to ON.</p> <p>d. Set METER SELECT switch(primary TD-353/U) to SYNC IN.</p> <p>e. Set METER SELECT switch to SERV FAC.</p> <p>f. Set SERV SEL switch to A</p> <p>g. Set AC POWER switch of second TD-352/U to OFF.</p>	<p>a. TEST ALIGN meter reads in green area.</p> <p>b. None.</p> <p>c. None.</p> <p>d. TEST ALIGN meter reads in green area.</p> <p>e. None.</p> <p>f. TEST ALIGN meter reads in green area.</p> <p>g. None.</p>

c. Test Procedures-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
			<p><i>h.</i> Set SERV SEL switch to B -----</p> <p><i>i.</i> Set SERV SEL switch to D -----</p> <p><i>j.</i> Set METER SELECT switch to TIMING IN.</p> <p><i>k.</i> Connect SYNC OUT XMTR output of primary TD-353/U test unit to SYNC IN input of second TD-353/U.</p> <p><i>l.</i> Set AC POWER switch of second TD-353/U to ON.</p> <p><i>m.</i> Set METER SELECT switch of second TD-353/U to SYNC IN.</p> <p><i>n.</i> Set AC POWER switch of second TD-353/U to OFF.</p> <p><i>o.</i> Set METER SELECT switch to SERV FAC.</p> <p><i>p.</i> Set SERV SEL switch to C -----</p> <p><i>q.</i> Set SERV SEL switch to OSC</p> <p><i>r.</i> Adjust OSC ADJUST control for hairline indication on TEST ALIGN meter.</p> <p><i>s.</i> Set MEASURE-PHONE ODD-PHONE EVEN switch to MEASURE.</p> <p><i>t.</i> Set SERV SEL switch to ODD CHAN position.</p> <p><i>u.</i> In sequence, set ODD CHAN switch to positions 1 through 47, observing TEST ALIGN</p>	<p><i>h.</i> TEST ALIGN meter reads in green area.</p> <p><i>i.</i> TEST ALIGN meter reads in green area.</p> <p><i>j.</i> TEST ALIGN meter reads in green area.</p> <p><i>k.</i> None.</p> <p><i>l.</i> None.</p> <p><i>m.</i> TEST ALIGN meter of second TD-353/U reads in green area.</p> <p><i>n.</i> None.</p> <p><i>o.</i> None.</p> <p><i>p.</i> TEST ALIGN meter reads in green area.</p> <p><i>q.</i> None.</p> <p><i>r.</i> None.</p> <p><i>s.</i> None.</p> <p><i>t.</i> None.</p> <p><i>u.</i> TEST ALIGN meter reads on or near hairline for each channel.</p>

		<p>meter reading for each position.</p> <p>v. Set SERV SEL switch to EVEN CHAN position.</p> <p>w. In sequence, set EVEN CHAN switch to positions 2 through 48, observe TEST ALIGN meter reading for each position.</p>	<p>v. None.</p> <p>w. TEST ALIGN meter reads on or near hairline for each channel.</p>
2	No changes required.	<p><i>Receive timing and receive timing fault locator tests</i></p> <p>a. Set SERV SEL switch to H</p> <p>b. Set SERV SEL switch to K</p> <p>c. Set SERV SEL switch to J.</p> <p>d. Disconnect CG-1040B/U from PCM IN connector.</p> <p>e. Set SERV SEL switch to M</p> <p>f. Reconnect CG-1040B/U to PCM IN connector.</p> <p>g. Set METER SELECT switch to TIMING IN.</p> <p>h. Connect SYNC OUT RCVR output of primary TD-353/U test unit to SYNC IN input of second TD-353/U.</p> <p>i. See that METER SELECT switch of second TD-353/U is set to SYNC IN.</p> <p>j. Set AC POWER switch of second TD-353/U to ON.</p>	<p>a. TEST ALIGN meter reads in green area.</p> <p>b. TEST ALIGN meter reads in green area.</p> <p>c. TEST ALIGN meter reads in green area.</p> <p>d. Buzzer sounds and FRAME indicator lights.</p> <p>e. TEST ALIGN meter reads in green area.</p> <p>f. Buzzer stops, FRAME indicator out, TEST ALIGN meter reading drops to left of green area.</p> <p>g. TEST ALIGN meter reads in green area.</p> <p>h. None.</p> <p>i. None.</p> <p>j. TEST ALIGN meter of second TD-353/U reads in green area.</p>

Test Procedures-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
			k. Set AC POWER switch of second TD-353/U to OFF.	k. None.
3	<p>Same as step 1 except: SG-71/FCC Power ON: ON</p> <p>RANGE: X10 Tuning Vernier: 110 AMPLITUDE: -4 dbm MOD. BAL.-BAL. UNBAL. BAL</p> <p><i>Note.</i> Precise setting of 1,100 cps not critical. (Dial setting is sufficient; frequency measurement not necessary.)</p>		<p><i>Modulator, sample and store, coder timing, coder pam monitor, noise generator, and noise generator monitor tests</i></p> <p>a. Connect 1,100 cps BAL. OUTPUT of SG-71/FCC to pins A and B of AUDIO CHAN connector1-8 (audio in 1 for channel 1).</p> <p>b. Set METER SELECT switch to SERV FAC.</p> <p>c. Set SERV SEL switch to E</p> <p>d. Remove 1,100-cps tone</p> <p>e. Reconnect 1,100 cps tone</p> <p>f. Set METER SELECT switch to NOISE GEN.</p> <p>g Repeat steps a through f for channels 2 through 24.</p>	<p>a. None.</p> <p>b. None.</p> <p>c. TEST ALIGN meter reads in green area.</p> <p>d. TEST ALIGN meter reads out of green area.</p> <p>e. None.</p> <p>f. TEST ALIGN meter reads in green area.</p>

4	No changes required.	<p><i>Pcm in traffic detector, coder, pcm output and transmit and receive address tests</i></p> <ul style="list-style-type: none"> a. Set METER SELECT switch to PCM IN. b. Disconnect CG-1040B/U from PCM IN connector. c. Reconnect CG-1040B/U to PCM IN connector. d. Set ADDRESS switch to SLAVE. e. Set METER SELECT switch to SERV FAC. f. Set SERV SEL switch to F. g. Connect Headset HS-33/U to pins G and H of AUDIO CHAN connector 1-8(audio out 2 for channel 3) and listen to 1,100-cps tone. h. Remove modulation and listen to channel. i. Reconnect modulation to pins A and B of AUDIO CHAN connector 1-8 (audio in 1 for channel 1). j. Reconnect Headset HS-33/U to pins C and D of AUDIO CHAN connector 1-8 (audio out 1 for channel 1). 	<ul style="list-style-type: none"> a. TEST ALIGN meter reads in green area. b. No reading on TEST ALIGN meter. c. None. d. Test unit frames in on SLAVE(2 Kc) address; TEST ALIGN meter reads in green area. Unit may go into alarm, but only momentarily. e. None. f. TEST ALIGN meter reads in green area. g. 1,100-cps tone is clear and free of distortion. h. Channel is free of random clicks. i. None. j. None.
---	----------------------	--	--

Test Procedures-Continued

Step No	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
5	No changes required.		<p><i>Pcm input and pcm input monitoring tests</i></p> <p>a. Set SERV SEL switch to L.</p> <p>b. Disconnect CG-1040B/U from PCM IN connector.</p> <p>c. Reconnect CG-1040B/U to PCM IN connector.</p> <p>d. Set SERV SEL switch to N..</p>	<p>a. None.</p> <p>b. TEST ALIGN meter reads in green area, buzzer sounds and FRAME indicator lights.</p> <p>c. Buzzer stops, FRAME indicator extinguishes, and no reading on TEST ALIGN meter.</p> <p>d. TEST ALIGN meter reads in green area.</p>
6	No changes required.		<p><i>Decoder, demodulator, and audio measure tests</i></p> <p>a. Set SERV SEL switch to ODD CHAN position.</p> <p>b. Turn OSC ADJUST control fully counterclockwise (off).</p> <p>c. Set ODD CHAN switch to 1 MEASURE-PHONE ODD-PHONE EVEN switch to PHONE ODD.</p> <p>d. Listen to 1,100-cps tone on Headset HS-33/U</p> <p>e. Remove modulation</p>	<p>a. None.</p> <p>b. None.</p> <p>c. TEST ALIGN meter reads on or near hairline.</p> <p><i>Note.</i> Performance is affected by setting of demodulator gain control. Test unit demodulators should be set to give hairline readings on TEST ALIGN meter in loop-back condition. If a type 1A2/2A2 panel is being checked after repair, its gain setting may not give hairline reading under loop-back conditions.</p> <p>d. Audio tone is clear and free of distortion.</p> <p>e. No reading on TEST ALIGN meter.</p>

			<p><i>f.</i> Reconnect modulation <i>g.</i> Reconnect 1,100-cps BAL OUTPUT of SO-71/FCC to pins E and F of AUDIO CHAN connector 1-8 (audio in 2 for channel 3). <i>h.</i> Reconnect Headset HS-33/U to pins G and H of AUDIO CHAN connector 1-8 (audio out 2 for channel 3). <i>i.</i> Set ODD CHAN switch to 3 <i>j.</i> Listen to 1,100-cps tone on headset.</p>	<p><i>f.</i> None. <i>g.</i> None. <i>h.</i> None. <i>i.</i> TEST ALIGN meter reads on or near hairline. (See also note, step <i>c</i> above.) <i>j.</i> Audio tone is clear and free of distortion.</p>
7	No changes required.		<p><i>Pcm from aux monitoring tests</i> <i>a.</i> Disconnect loop-back cable between PCM IN and PCM OUT connectors. <i>b.</i> Connect lead between PCM OUT connector and pin C on the TO AUX connector. <i>c.</i> Set METER SELECT switch to PCM FROM AUX. <i>d.</i> Reconnect PCM IN to PCM OUT connector.</p>	<p><i>a.</i> None. <i>b.</i> None. <i>c.</i> TEST ALIGN meter reads in green area. <i>d.</i> None.</p>
8	No changes required.		<p><i>Frame alarm and squelch circuits</i> <i>a.</i> Disconnect C-G1040B/U from PCM IN connector. <i>b.</i> Depress BUZZER OFF switch. <i>c.</i> Reconnect CG-1040B/U to PCM IN connector. <i>d.</i> Depress BUZZER OFF switch again.</p>	<p><i>a.</i> FRAME indicator lights, buzzer sounds, and 1,100-cps tone on channel 1 ceases. <i>b.</i> Buzzer ceases, but FRAME indicator stays lighted and tone stays off. <i>c.</i> FRAME indicator extinguishes and 1,100-cps tone resumes. <i>d.</i> Buzzer does not sound.</p>

c. Test Procedures-Continued

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
9	Same as step 1, except second TD-353/U not required.		<p><i>Test tone and test tone monitor tests.</i></p> <p>a. Disconnect SG-71/FCC and Headset HS-33/U from AUDIO CHAN connector. b. Set SERV SEL switch to OSC c. Set METER SELECT switch to SERV FAC. d. Adjust OSC ADJUST control for hairline indication on TEST ALIGN meter. e. Set MEASURE-PHONE ODD-PHONE EVEN switch to MEASURE, and SERV SEL switch to ODD CHAN position. f. Set ODD. CHAN switch to position 1.</p>	<p>a. None. b. None. c. None. d. Meter pointer of TEST ALIGN meter can be set for hairline reading. e. None. f. TEST ALIGN meter reads on or near hairline. See note in step 6c above.</p>
10	No changes required.		<p><i>Microphone and earphone amplifier tests</i></p> <p>a. Connect Headset-Microphone H-91A/U to TALK MONITOR connector. b. Set MEASURE-PHONE ODD-PHONE EVEN switch to PHONE ODD and hum or speak into microphone. c. Connect SG-71/FCC to pins A and B of AUDIO CHANNELS 1-8. d. Listen for internal 1,100 cps tone.</p>	<p>a. None. b. None. c. TEST ALIGN meter pointer fluctuates between no and green area reading. d. 1,100-cps tone can be heard clear and undistorted on headset.</p>

5-8. Summary of Performance Standard (TD-353/U)

Step No.	Description	Performance standard	Test data
<i>Transmit timing and transmit timing fault locator tests</i>			
1a	Panel 1A8 timing signals (SERV SEL switch: A).	TEST ALIGN meter reads in green area.	
1d	Panel 1A8 external sync in monitor (METER SELECT: SYNC IN).	TEST ALIGN meter reads in green area.	
1f	Panel 1A8 timing signals using external sync input (SERV SEL switch: A).	TEST ALIGN meter reads in green area.	
1h	Panel 1A9 timing signals (SERV SEL switch: B).	TEST ALIGN meter reads in green area.	
1i	Panel 1A9 timing signals (SERV SEL switch: D).	TEST ALIGN meter reads in green area.	
1j	Panel 1A9 timing out signal (METER SELECT switch: TIMING OUT).	TEST ALIGN meter reads in green area.	
1m	Panel 1A9 sync out xmtr signal (METER SELECT switch of second TD-353/U set to SYNC IN).	TEST ALIGN meter (of second TD-353/U) reads in green area.	
1p	Panel 1A10, timing signals (SERV SEL switch: C).	TEST ALIGN meter reads in green area.	
1u	Panel 1A10, modem timing signals (all odd channels modulated).	TEST ALIGN meter reads on or near hairline.	
1w	Panel 1A10, modem timing signals (all even channels modulated).	TEST ALIGN meter reads on or near hairline.	
<i>Receive timing and receive timing fault locator tests</i>			
2a	Panel 1A13 timing signals (SERV SEL switch: H).	TEST ALIGN meter reads in green area.	
2b	Panel 1A13 timing signals (SERV SEL switch: E).	TEST ALIGN meter reads in green area.	
2c	Panel 1A10, timing signals (SERV SEL switch: J).	TEST ALIGN meter reads in green area.	
2d	Panel 1A13 skip-pulse activity -----	Buzzer sounds, FRAME indicator lights.	
2e	Panel 1A13 skip-pulse monitoring (SERV SEL switch: M).	TEST ALIGN meter reads in green area.	
2f	Panel 1A13 framing -----	Buzzer stops, FRAME indicator extinguishes, no reading on TEST ALIGN meter.	
2g	Panel 1A13 timing in monitor (METER SELECT switch: TIMING IN).	TEST ALIGN meter reads in green area.	

5-8. Summary of Performance Standard (TD-353/U)-Continued

Step No.	Description	Performance standard	Test data
2j	Panel 1A13 sync out rcvr output (METER SELECT switch of second TD-353/U set to SYNC IN). <i>Modulator, sample and store, coder timing, coder pam monitor, noise generator, and noise generator monitor tests</i>	TEST ALIGN meter (of second TD-353/U) reads in green area.	
3c	Panel 1A2/2A2 modulator channel 1, panel 1A7 coder pam monitor (SERV SEL switch: E).	TEST ALIGN meter reads in green area.	
3d	Panel 1A18 coder pam fault detector (modulation removed).	TEST ALIGN meter reads out of green area.	
3f	Panel 1A11/2A11 noise generator (METER SELECT switch: NOISE GEN).	TEST ALIGN meter reads out of green area.	
3i	Panel 1A2/2A2 modulator channel 3 (SERV SEL: E).	TEST ALIGN meter reads in green area.	
4a	<i>Pcm in traffic detector, coder, pcm output, and transmit and receive address tests</i> Panel 1A6/2A6 pam to pcm converter, panel 1A5 pcm retiming and comparator control, and panel 1A3/2A3 pcm output (METER SELECT: PCM IN).	TEST ALIGN meter reads in green area.	
4b	Panel 1A16/2A16 pcm in traffic detector	No reading on TEST ALIGN meter.	
4d	Panel 1A3/2A3 address insertion and Test unit frames in; panel 1A12/2A12 address detection (ADDRESS switch from MASTER to SLAVE).	TEST ALIGN meter reads in green area. Unit may go into alarm, but only momentarily.	
4f	Panel 1A3/2A3 transmit address monitor (SERV SEL switch: F).	TEST ALIGN meter reads in green area.	
4g	Panel 1A6/2A6 pam-pcm conversion (modulated channel).	Test tone is clear and free of distortion.	
4h	Panel 1A6/2A6 pam-pcm conversion (unmodulated channel).	Channel is free of random clicks.	
5b	<i>Pcm input and pcm input monitoring test</i> Panel 1A12/2A12 skip-pulse generator (SERV SEL switch: L).	TEST ALIGN meter reads in green area. Buzzer sounds. FRAME indicator lights.	
5c	Panel 1A12/2A12 framing-----	Buzzer-stops. FRAME indicator extinguishes. No reading on TEST ALIGN meter.	
5d	Panel 1A12/2A12 pcm input (SERV SEL switch: N).	TEST ALIGN meter reads in green area.	

5-8. Summary of Performance Standard (TD-353/U)-Continued

Step No.	Description	Performance standard	Test data
	<i>Decoder, demodulator, and audio measure circuits</i>		
6c	Panel 1A16/2A16 audio measure detector, channel 1.	TEST ALIGN meter reads on or near hairline.	
6d	Panel 1A14/2A14 pcm to pam converter, panel 1A15 expander circuit, and panel 1A2/2A2 demodulator circuit (demodulated audio output monitored at AUDIO CHAN connector, channel 1).	Audio tone is clear and free of distortion.	
6e	Panel 1A16/2A16 audio measure detector (modulating tone removed).	No reading on TEST ALIGN meter	
6i	Panel 1A2/2A2 audio measure, channel 3	TEST ALIGN meter reads on or near hairline.	
6j	Panel 1A2/2A2 demodulated audio output monitored at AUDIO CHAN connector, channel 3.	Audio tone is clear and free of distortion.	
	<i>Pcm from aux monitoring test</i>		
7c	Panel 1A15 pcm from aux monitor (METER SELECT switch: PCM FROM AUX).	TEST ALIGN meter reads in green area.	
	<i>Frame alarm and squelch test</i>		
8a	Panel 1A16/2A16 alarm and squelch circuit.	FRAME indicator lights, buzzer sounds, 1,100-cps tone stops.	
8b	Depress BUZZER OFF switch	Buzzer ceases, FRAME indicator remains lighted, and tone stays off.	
8c	PCM IN signal connected	FRAME indicator extinguishes and 1,100-cps tone resumes.	
8d	Depress BUZZER OFF switch again	Buzzer does not sound	
	<i>Test tone and test tone monitor test</i>		
9d	Panel 1A16/2A16 test tone oscillator (OSC ADJUST control adjusted).	TEST ALIGN meter pointer can be set for hairline reading.	
9f	Panel 1A16/2A16 test tone monitor (ODD CHAN switch: 1).	TEST ALIGN meter reads on or near hairline.	
	<i>Microphone and earphone amplifier test</i>		
10b	Panel 1A16/2A16 earphone amplifier (internal tone monitored).	1,100-cps tone is clear and undistorted	
10c	Panel 1A16/2A16 microphone amplifier (demodulated speech monitored on TEST ALIGN meter).	TEST ALIGN meter pointer fluctuates between no and green area reading.	

CHAPTER 6

DEPOT OVERHAUL STANDARDS

Refer to DMWR 11-5805-367/3 for depot repair and overhaul procedures.

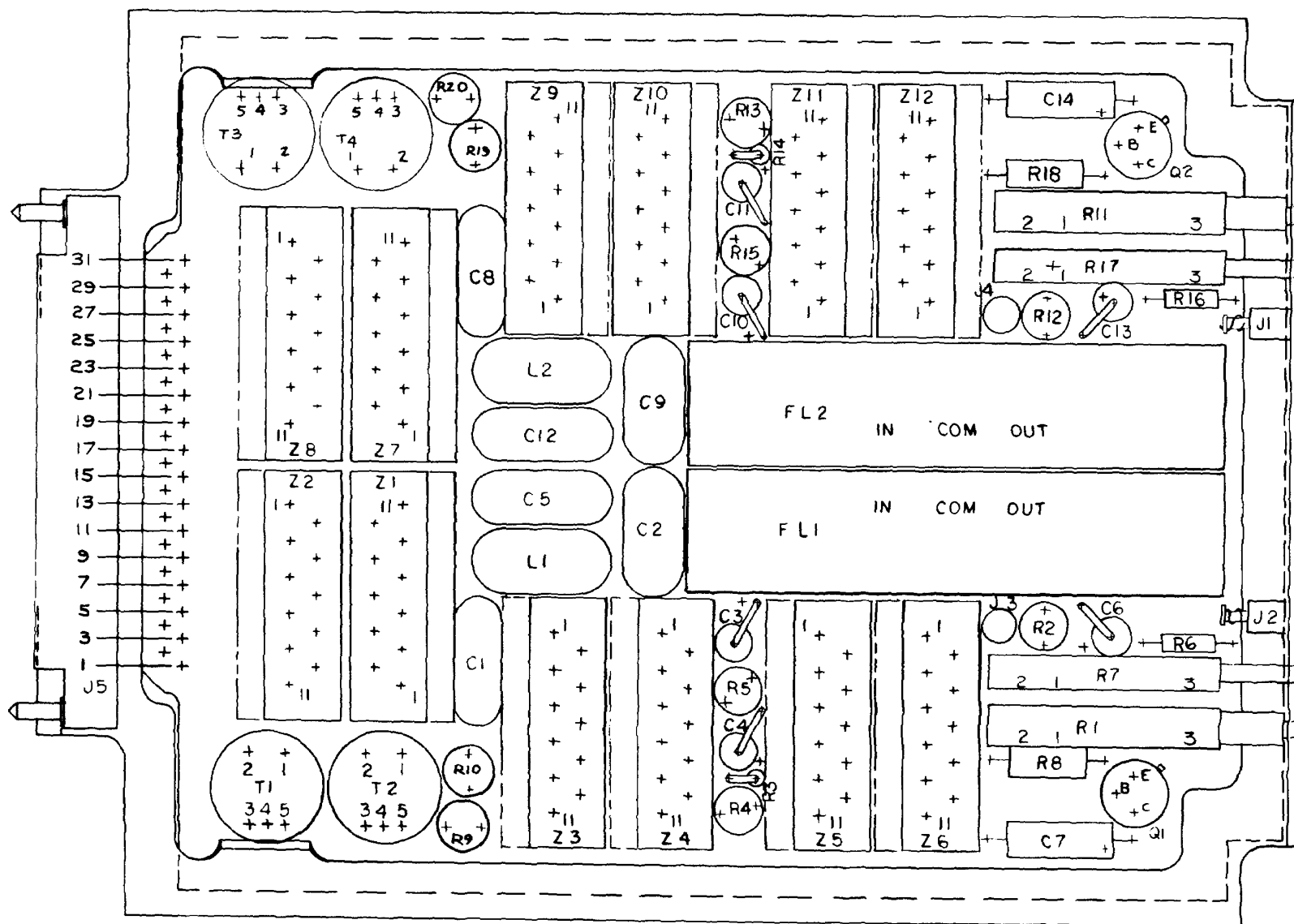


Figure 6-1. Panel 1A2/2A2, top view.

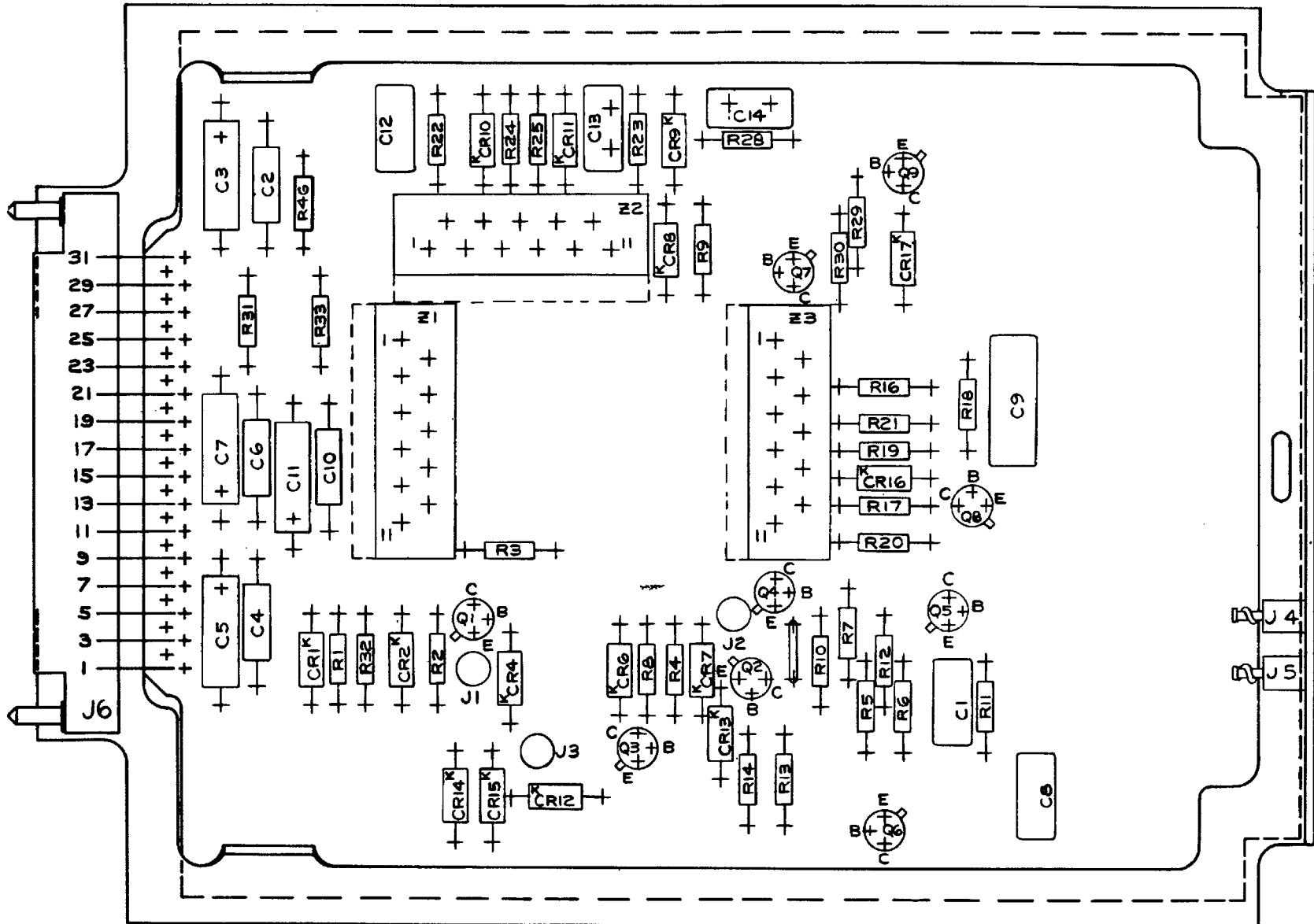


Figure 6-2. Panel 1A3/2A3, top view.

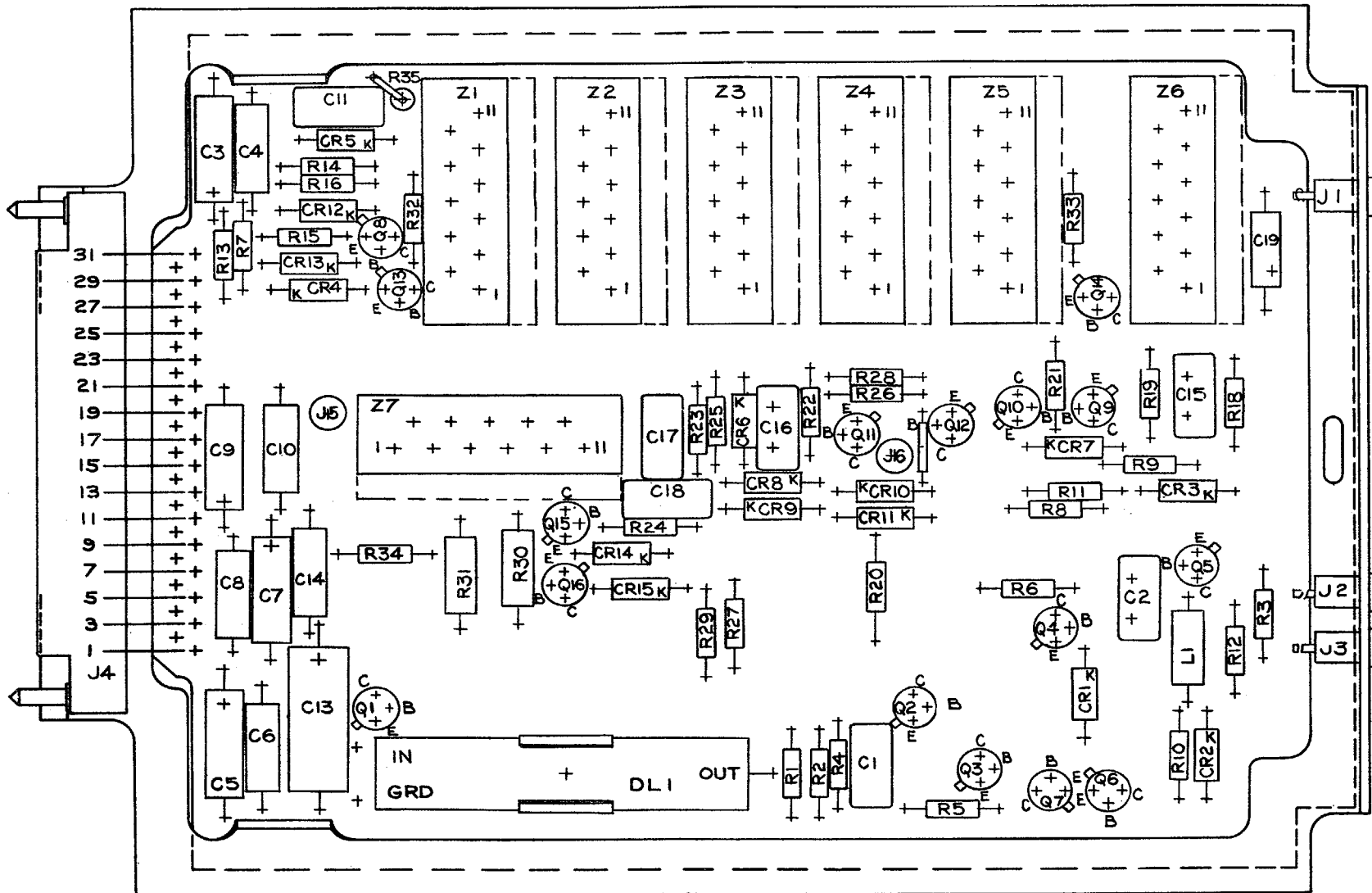


Figure 6-3. Panel 1A5, top view.

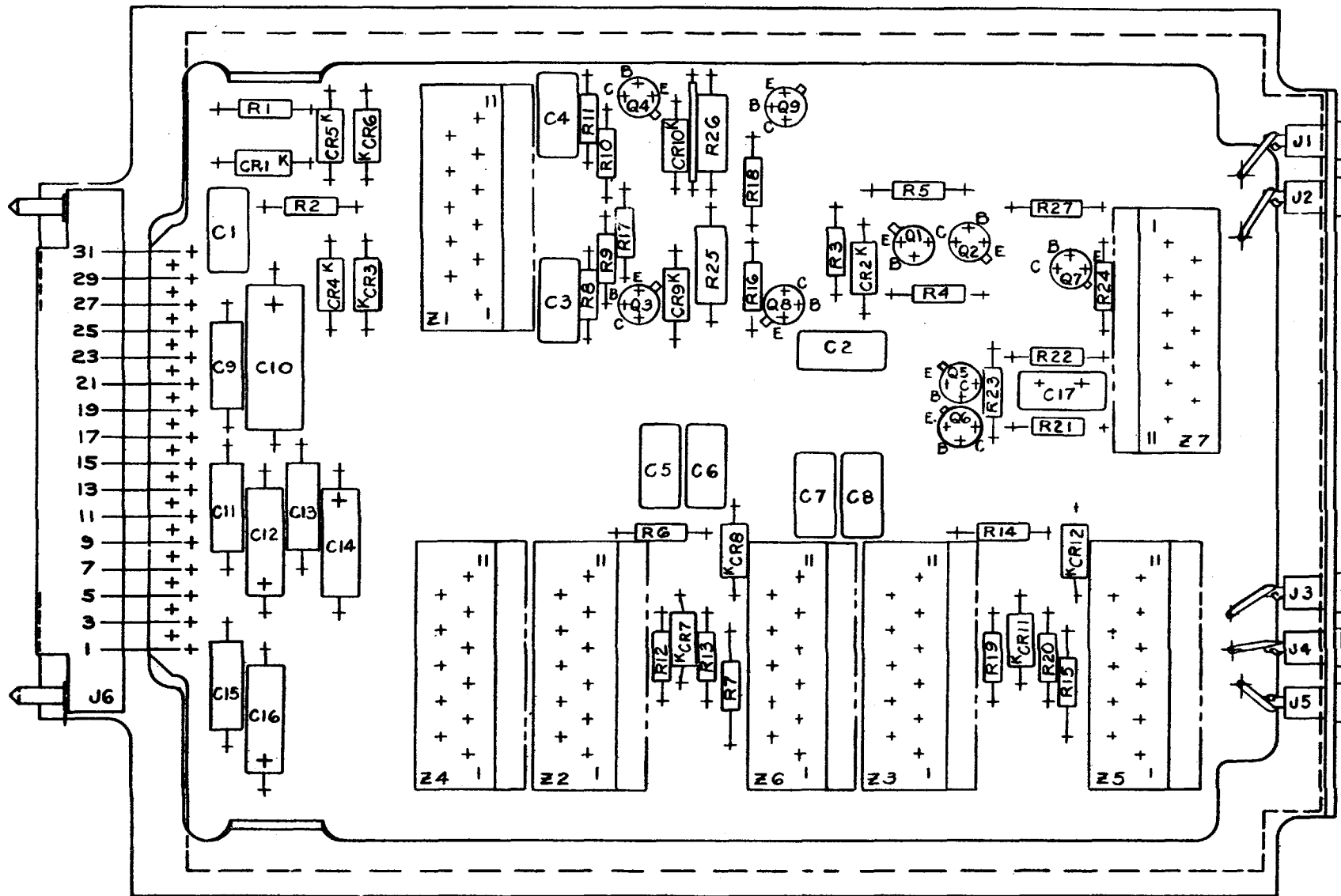
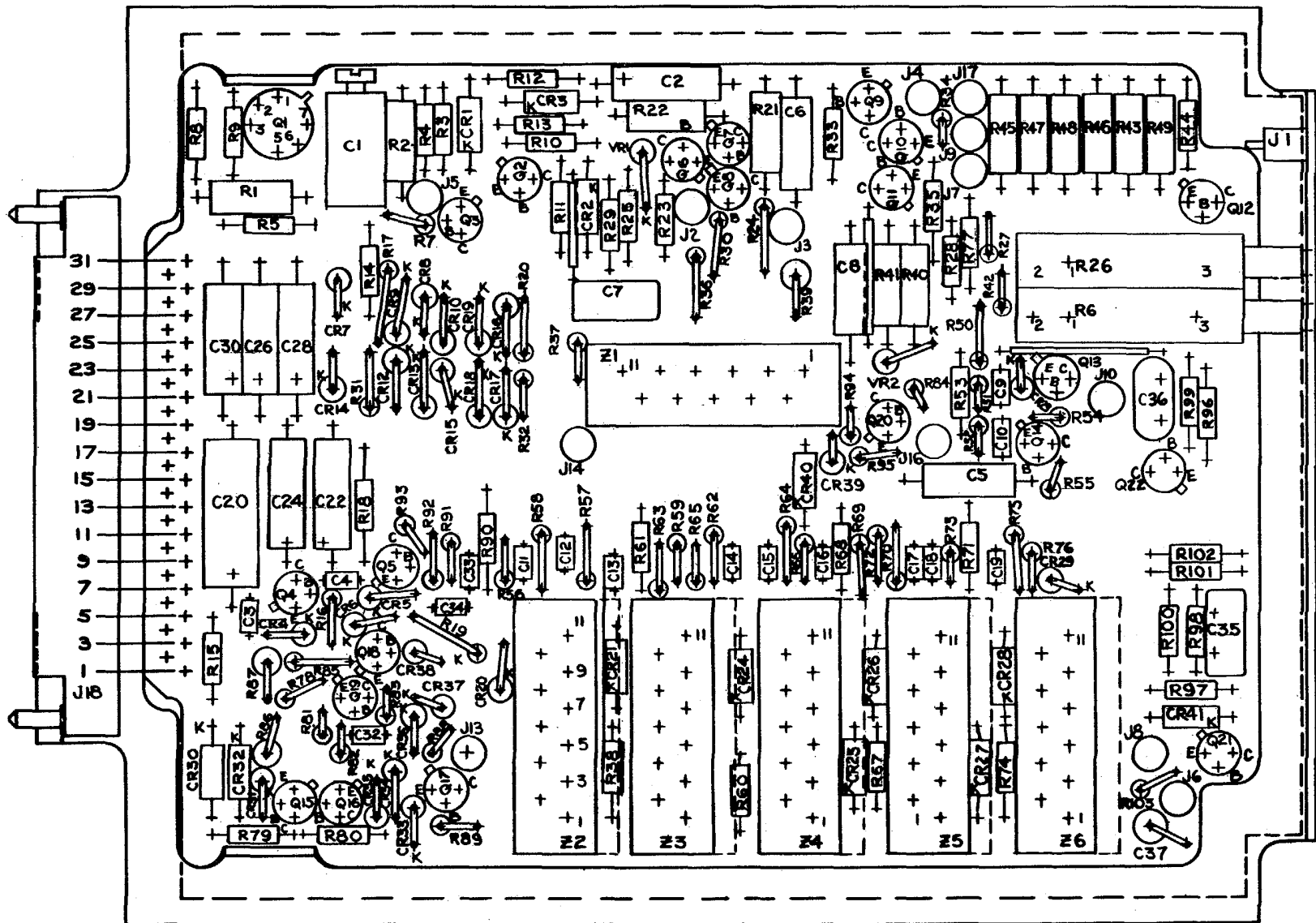


Figure 6-4. Panel 2A5, top view.



NOTE: WHEN REPLACING CAPACITOR C1 INSTALL A 3/8" BY 1/2" SPACER BETWEEN THE CAPACITOR AND THE LAND AREA.

EL2RC001

Figure 6-5. Panel 1A6/2A6, top view.
Change 3 6-6

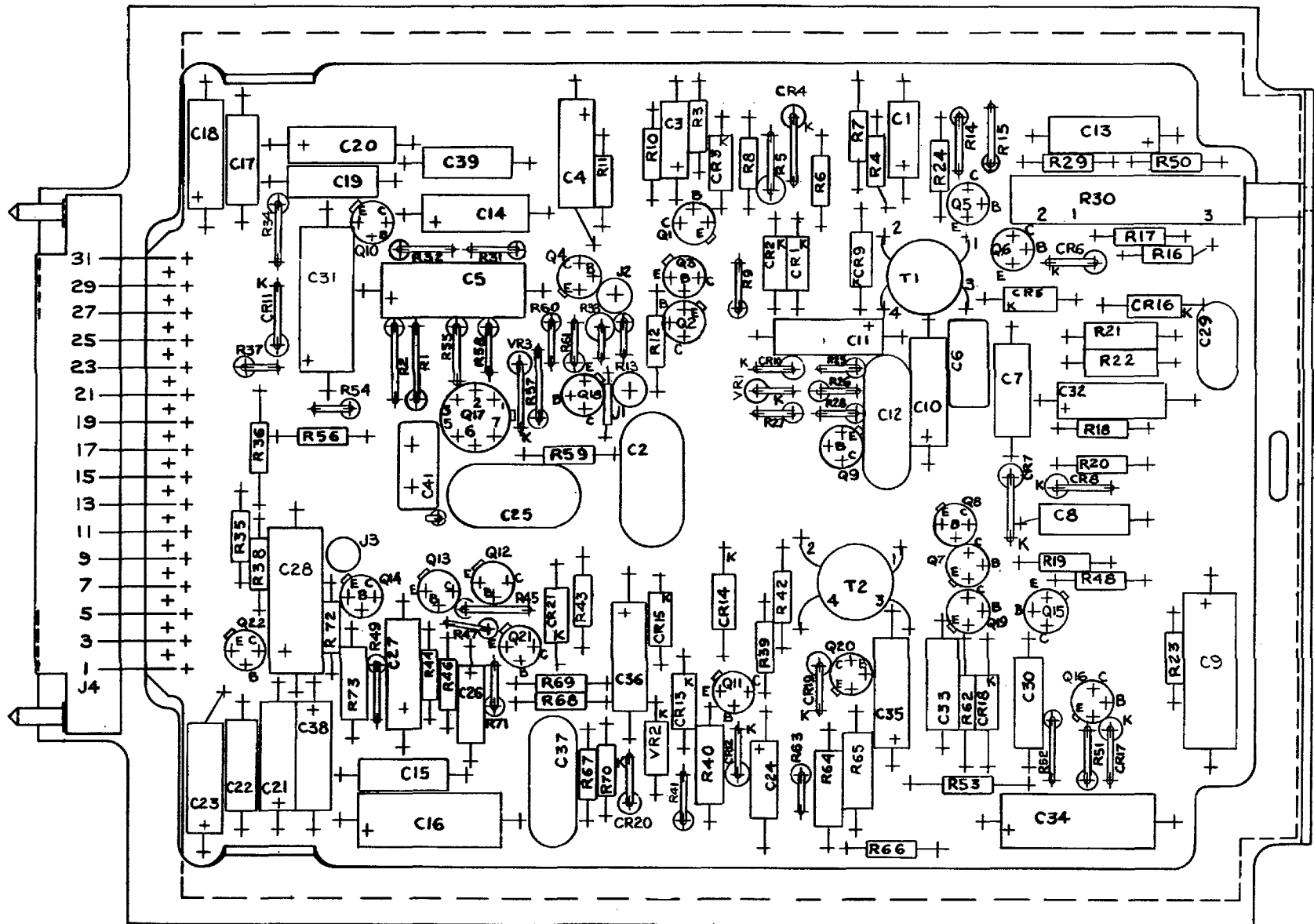


Figure 6-6. Panel 1A7, top view.

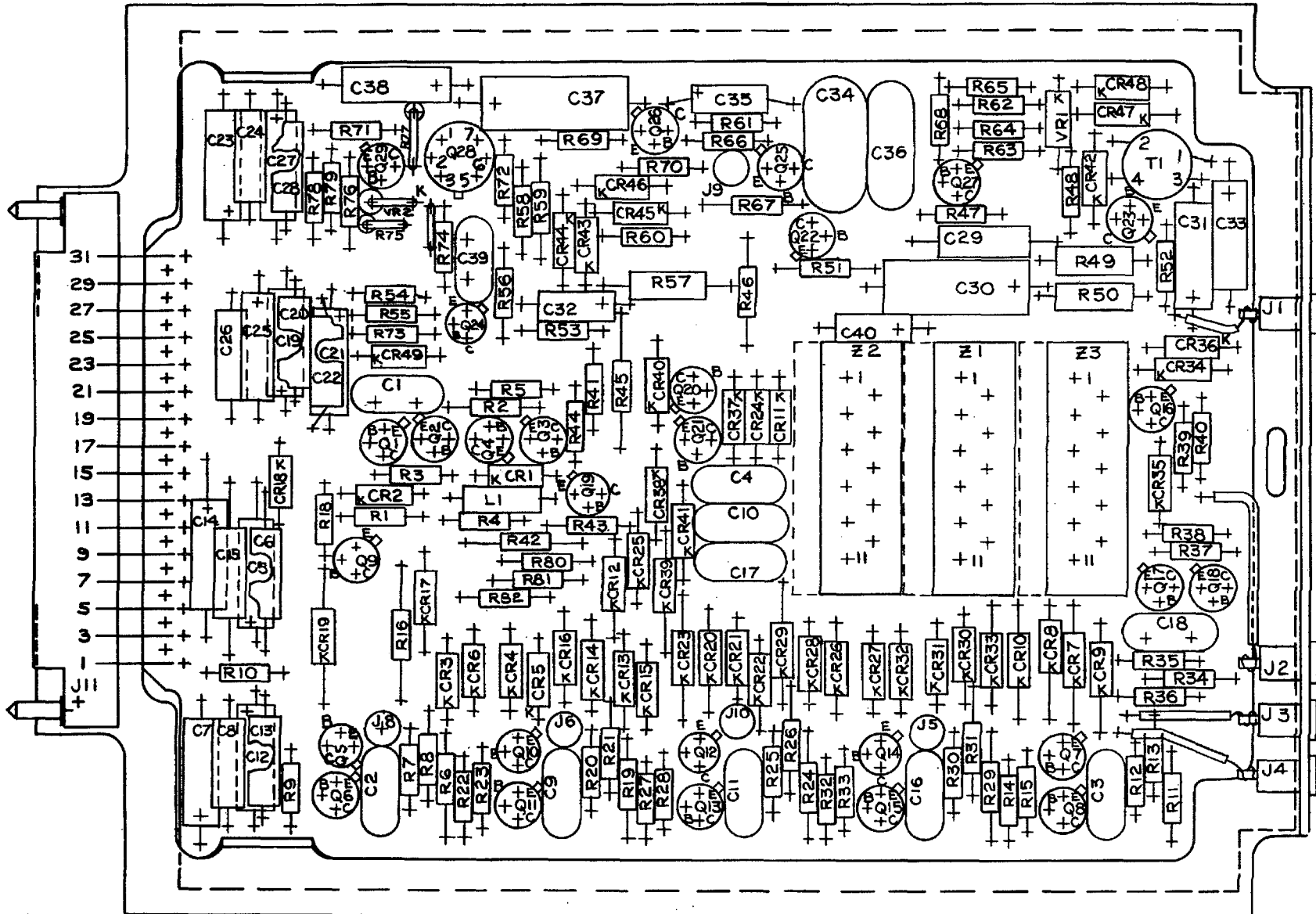


Figure 6-7. Panel 2A7, top view.

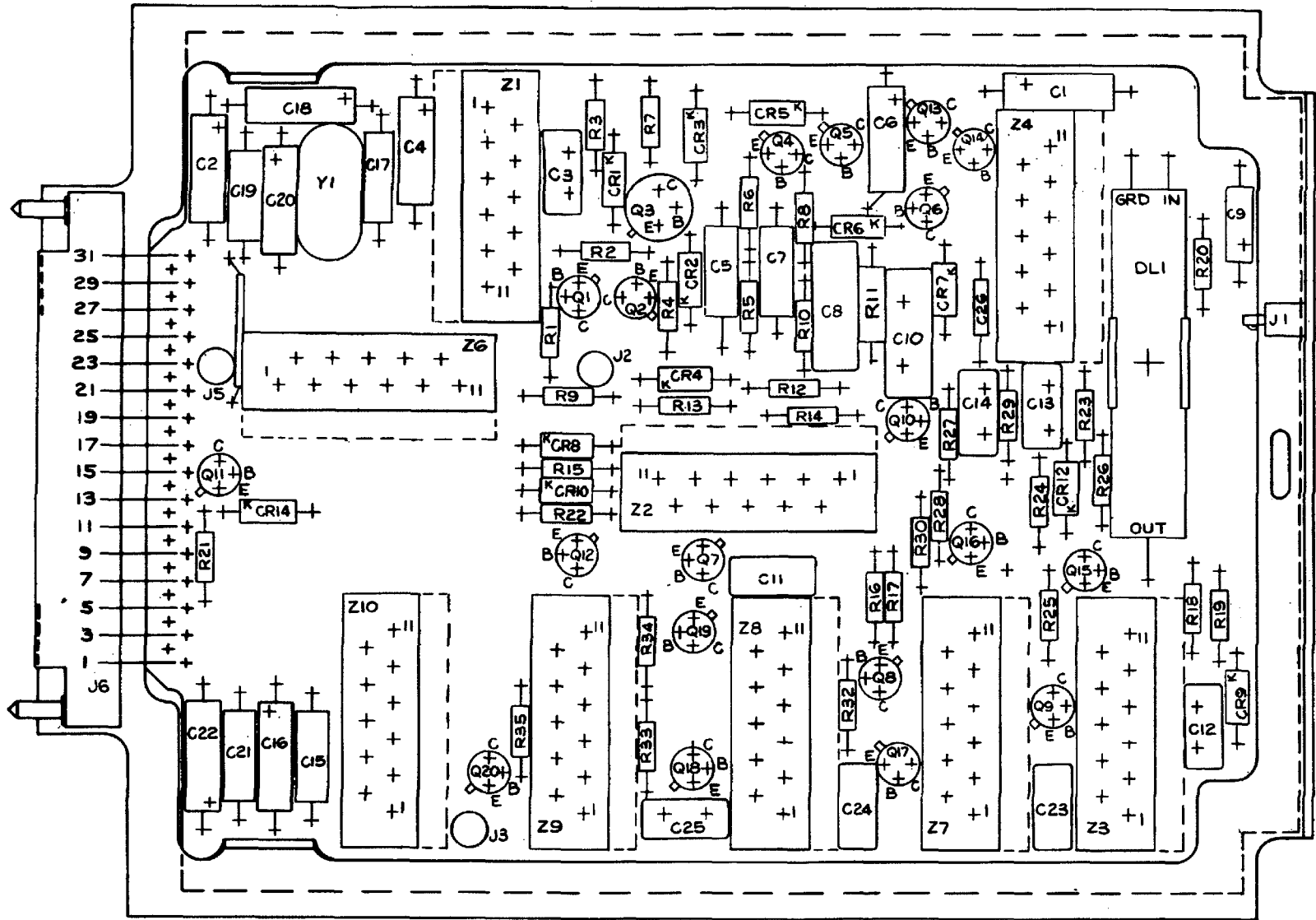


Figure 6-8. Panel 1A8, top view.

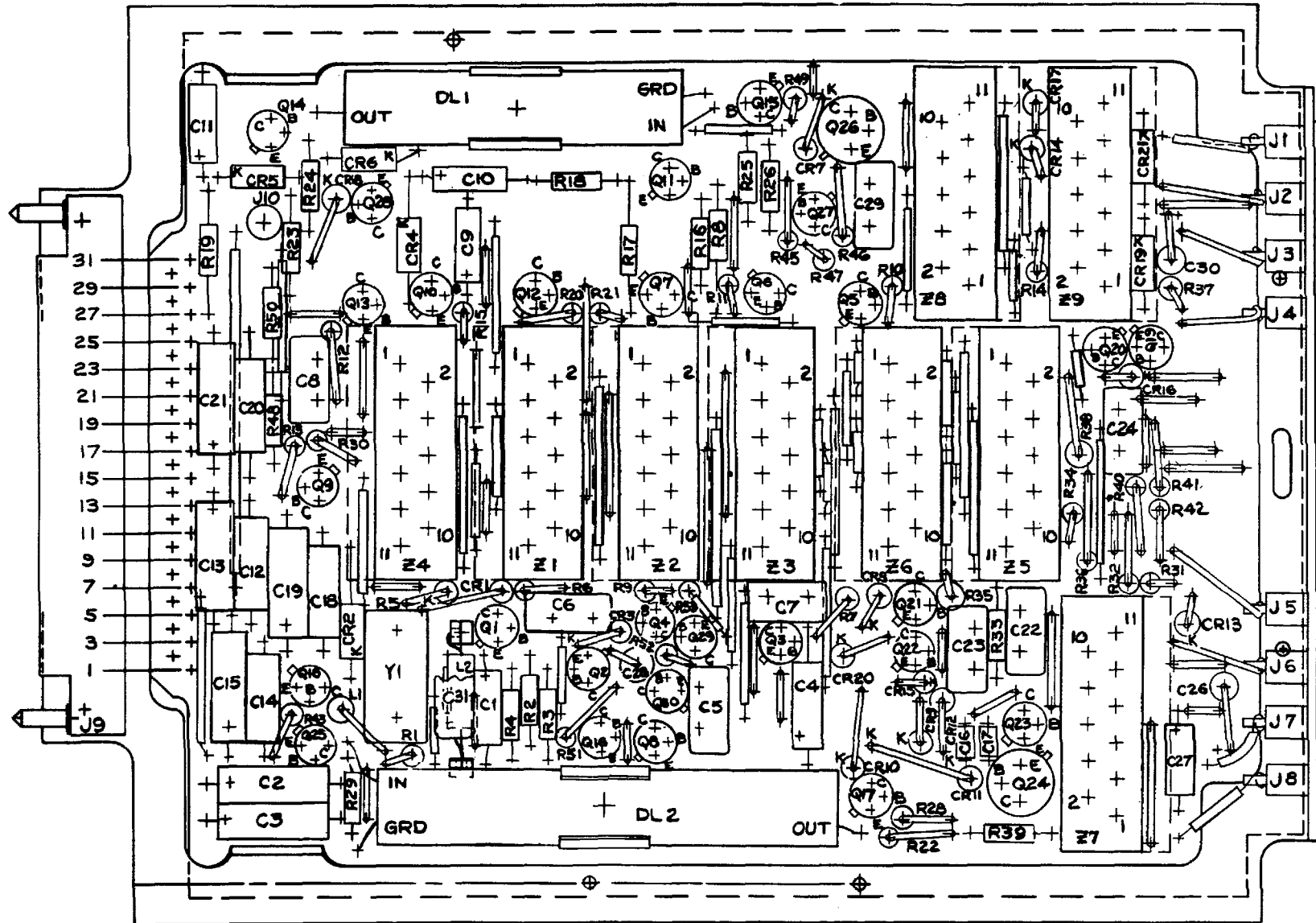


Figure 6-9. Panel 2-8, top view.
6-10

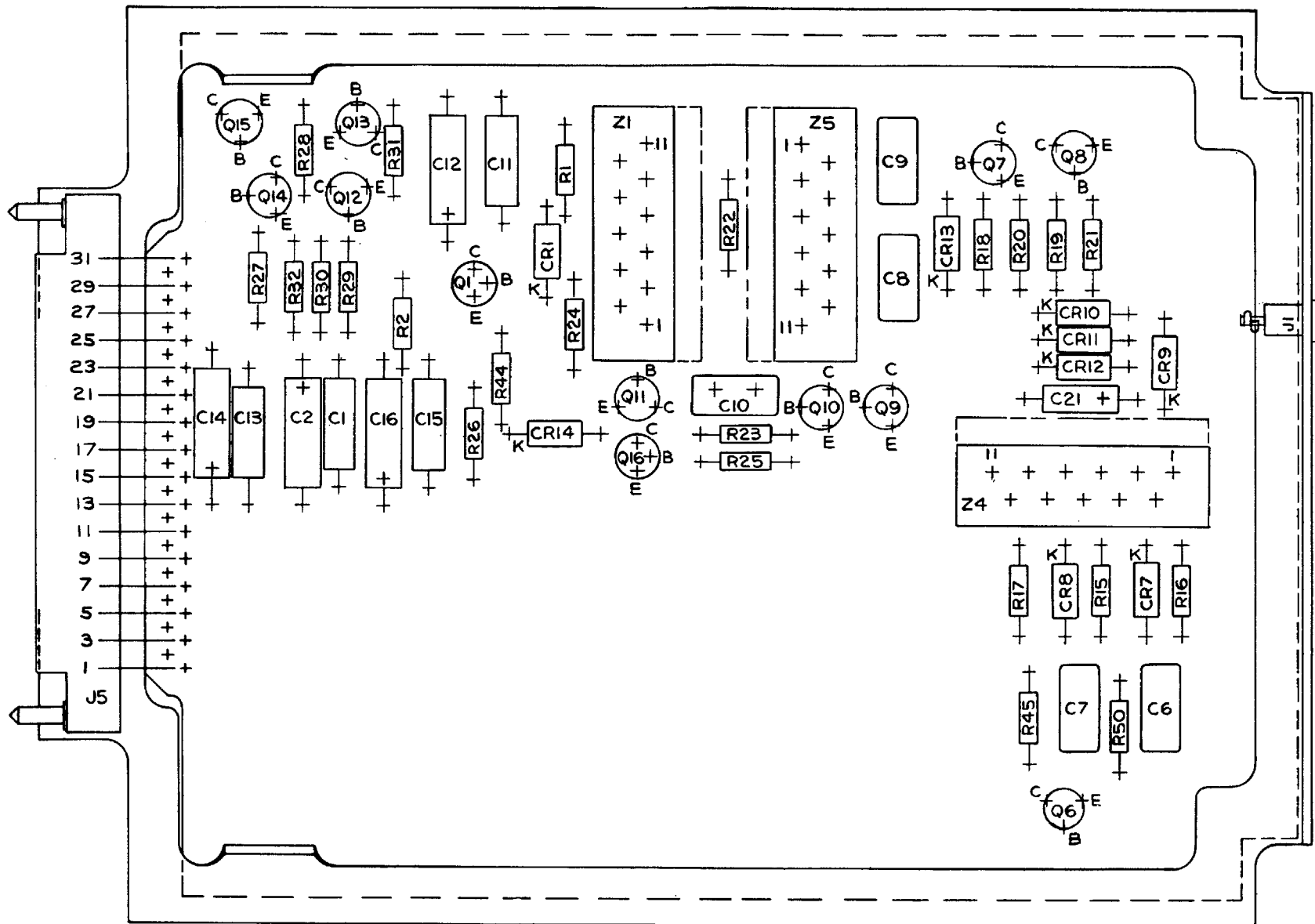


Figure 6-10. Panel 1A9, top view.
6-11

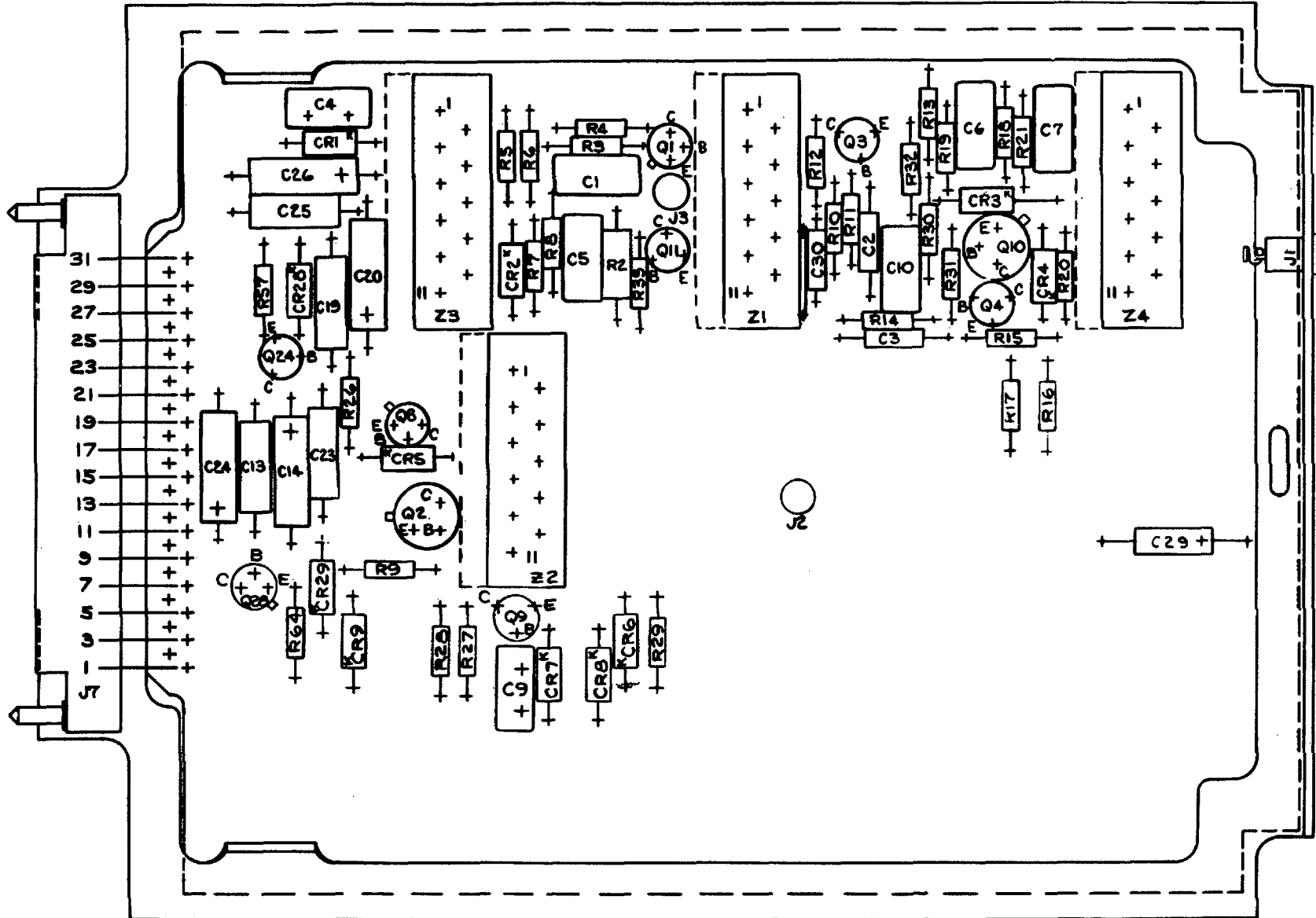


Figure 6-11. Panel 2A9, top view.
6-12

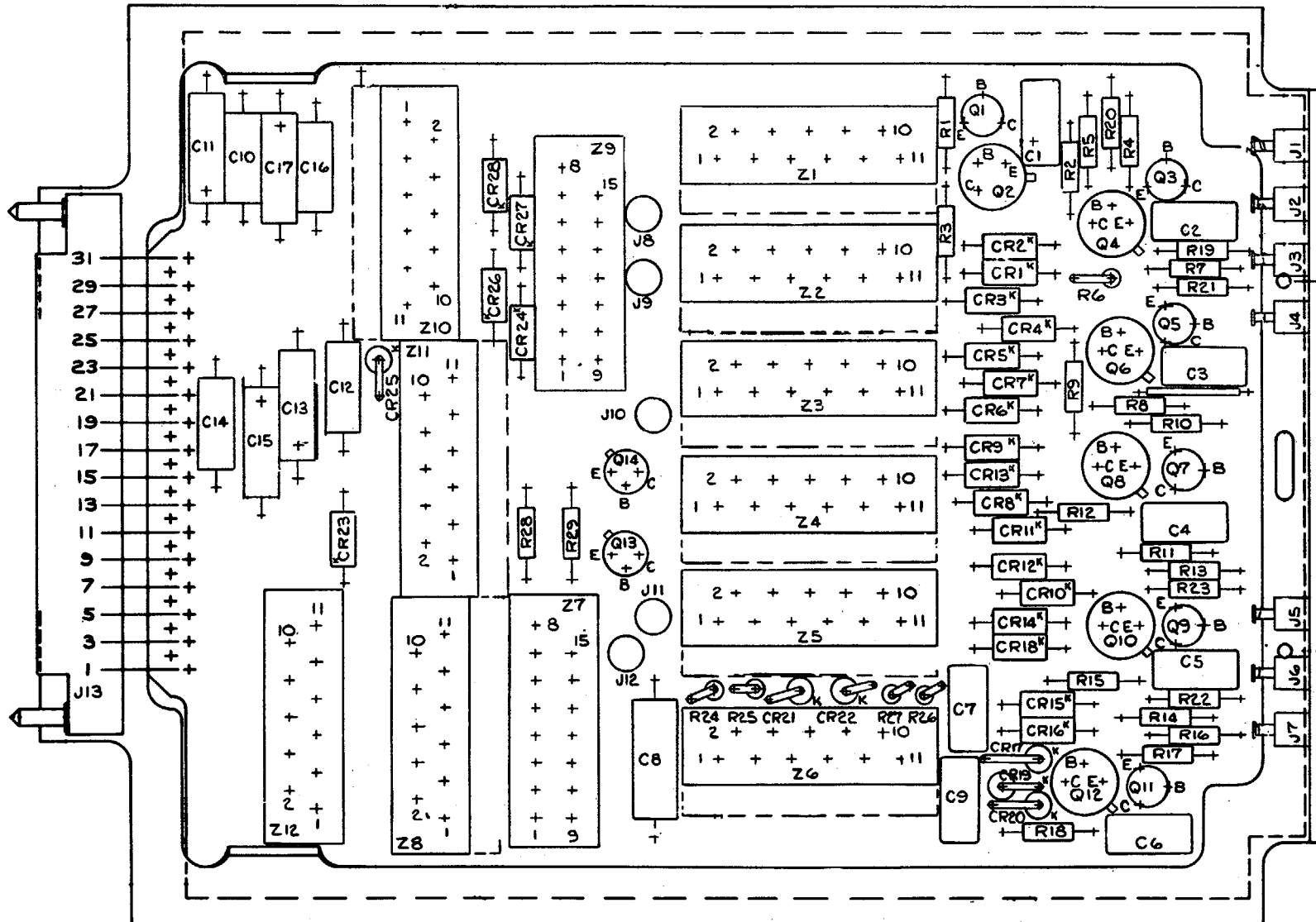


Figure 6-12. Panel 1A10, top view.
6-13

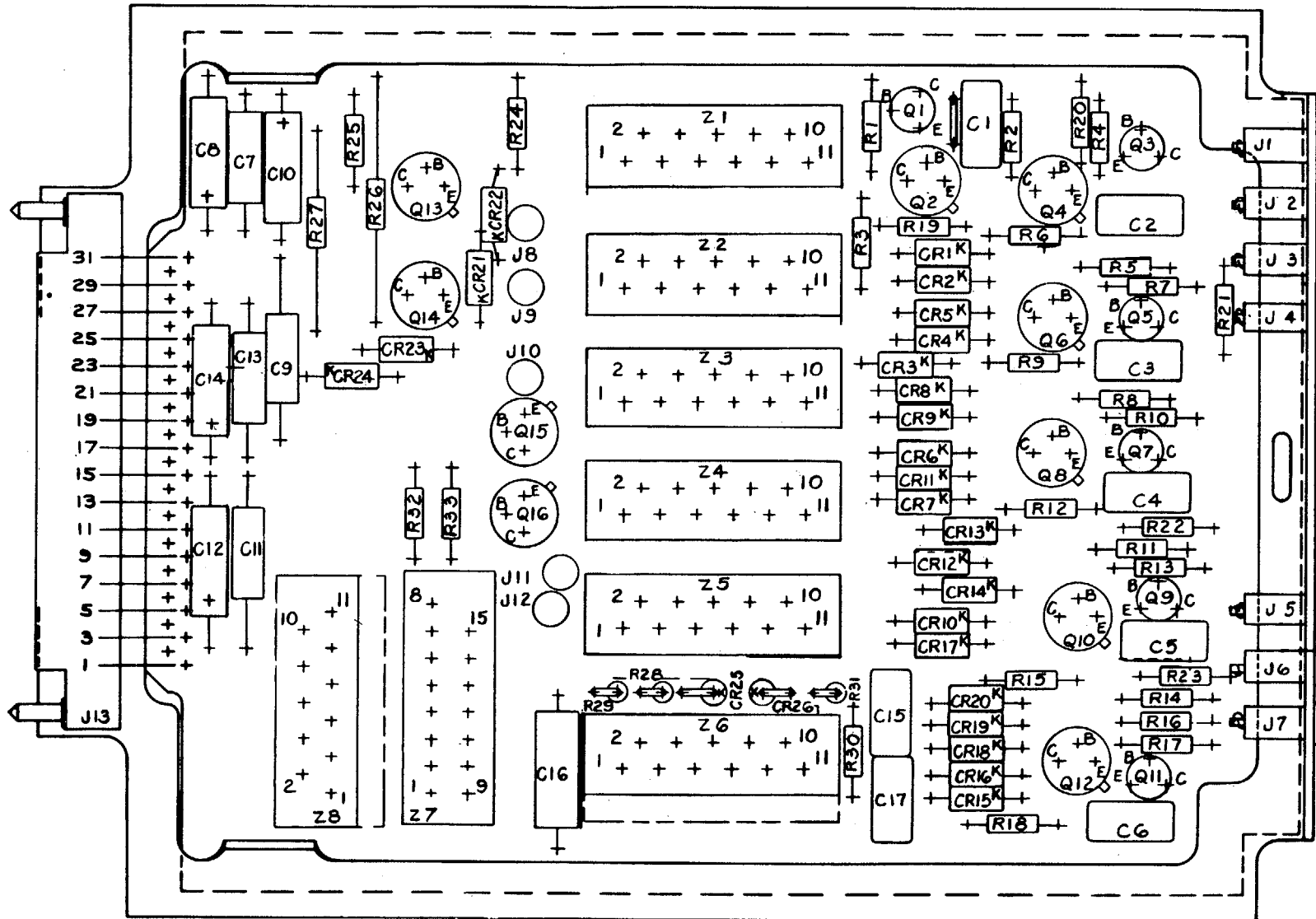


Figure 6-13. Panel 2A10, top view.

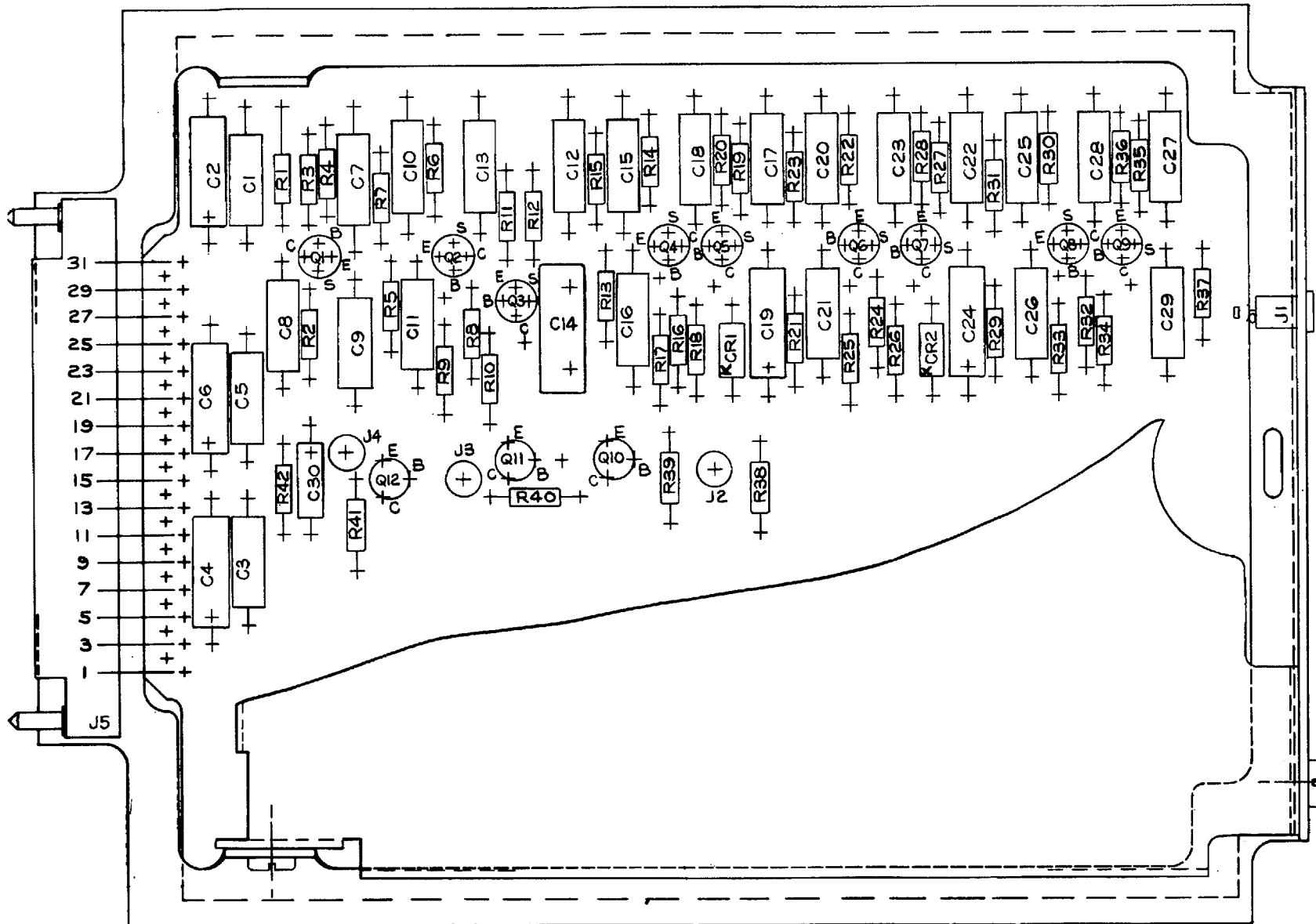


Figure 6-14. Panel 1A11/2A11, top view.

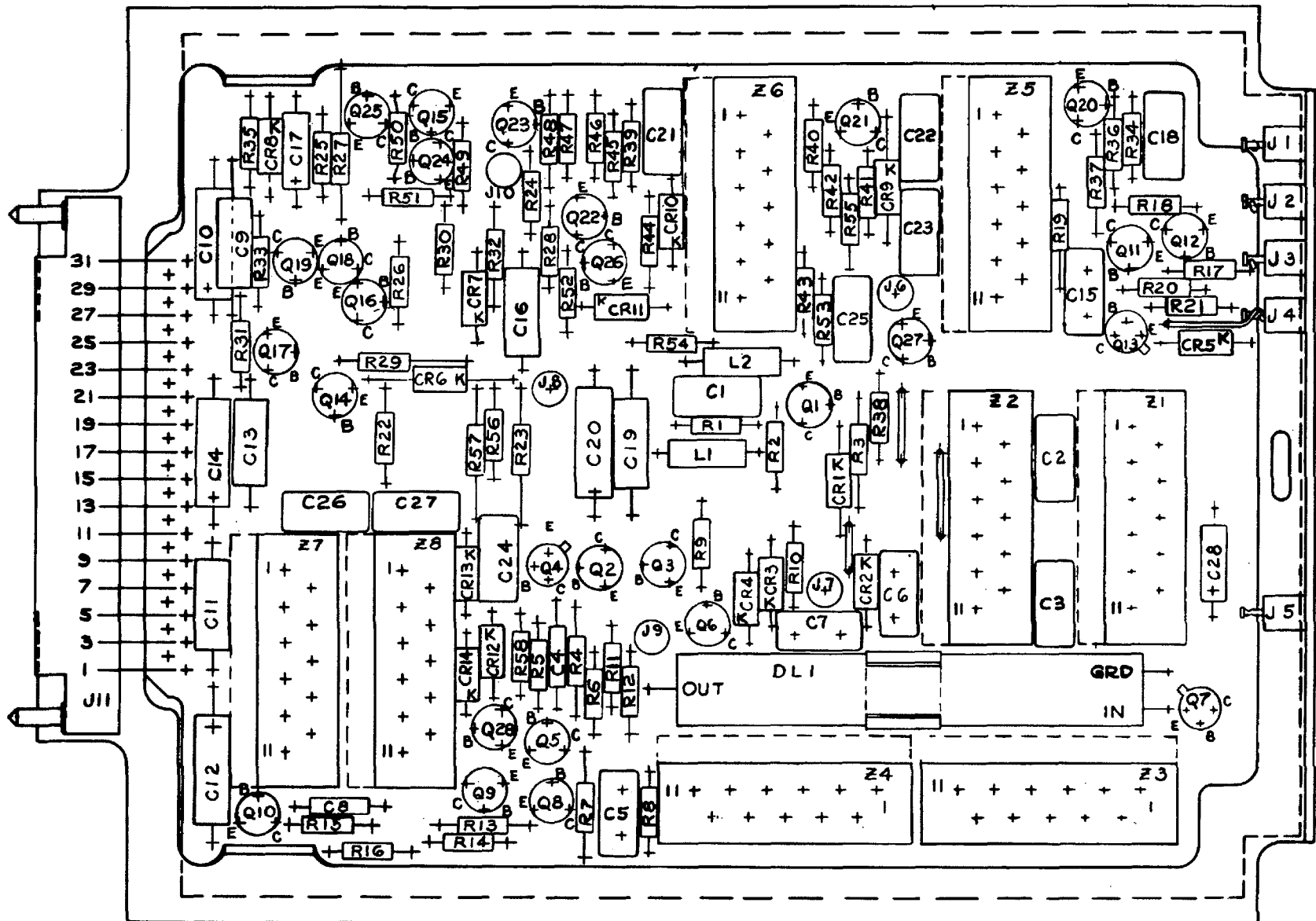


Figure 6-15. Panel 1A12/2A12, top view.
6-16

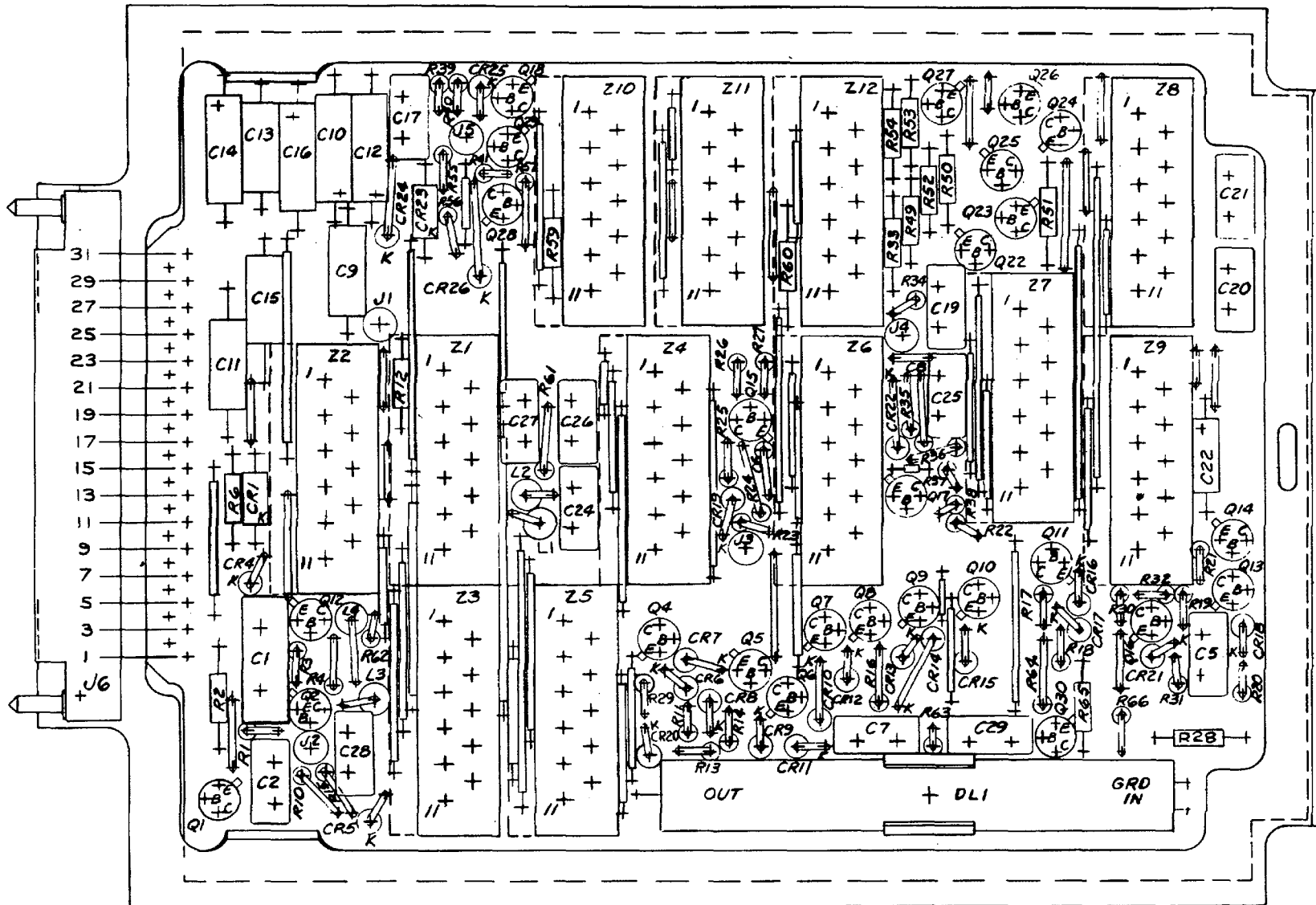


Figure 6-16. Panel 1A13, top view.
6-17

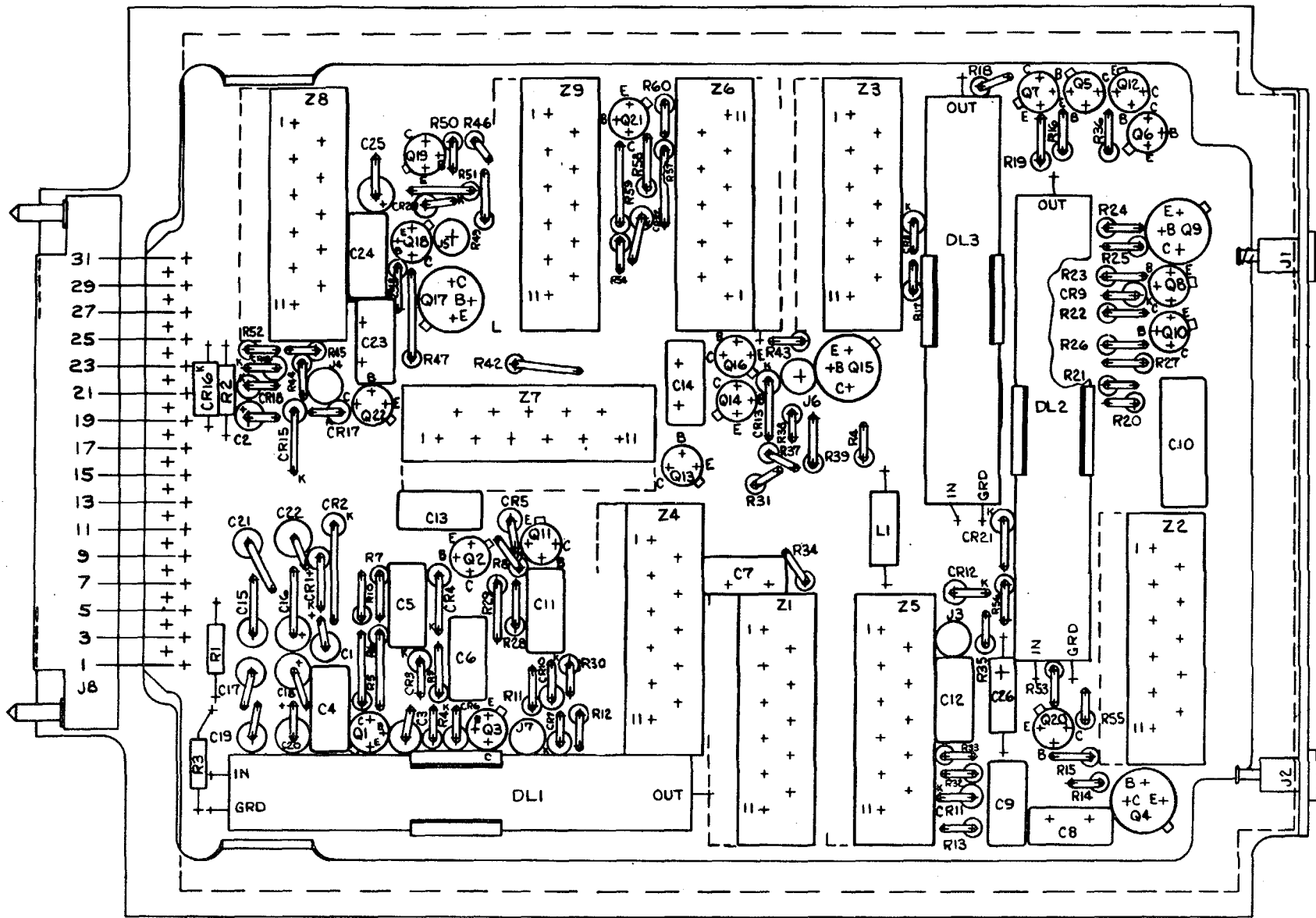


Figure 6-17. Panel 2A13, top view.

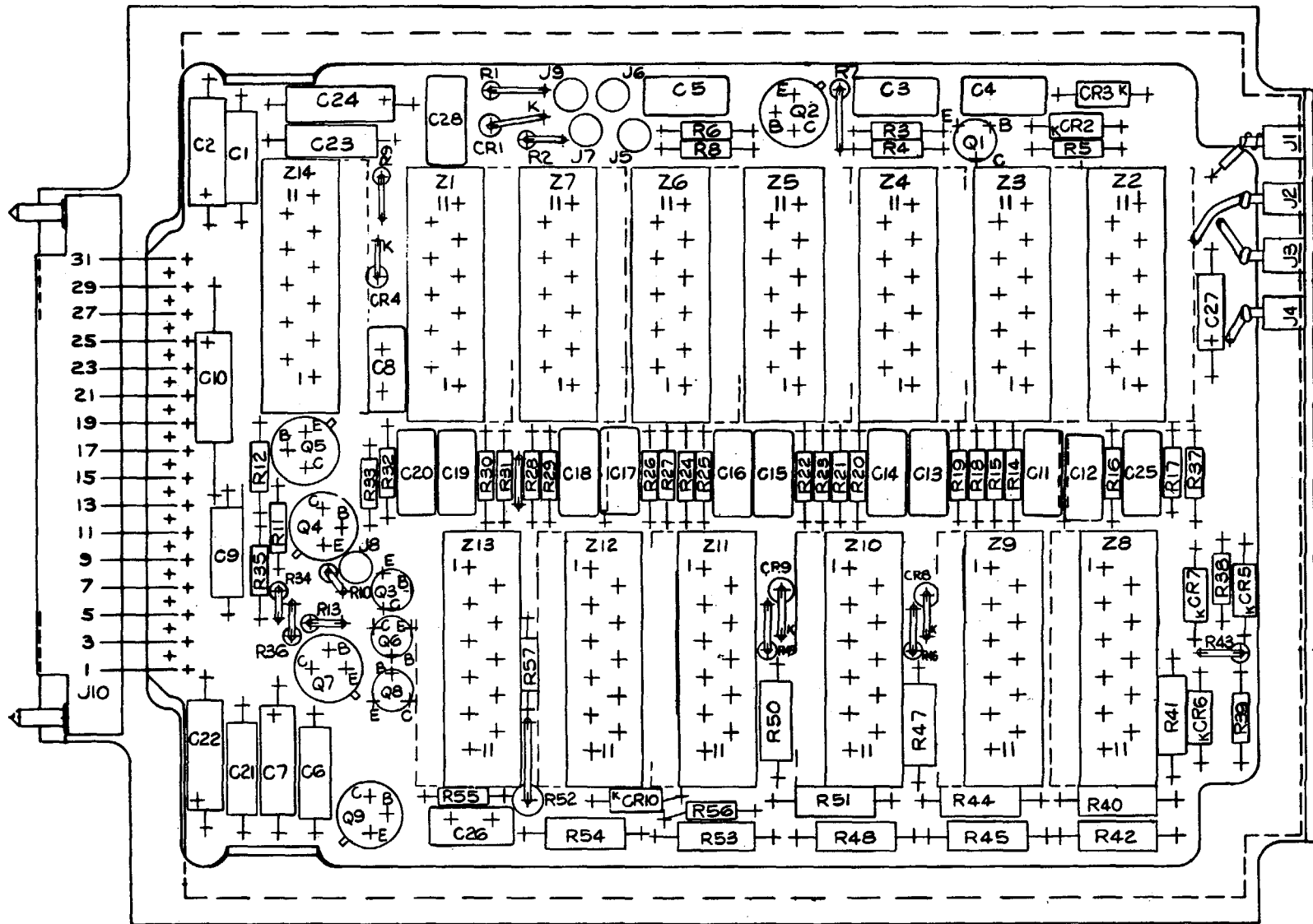


Figure 6-18. Panel 1A14/2A14, top view.

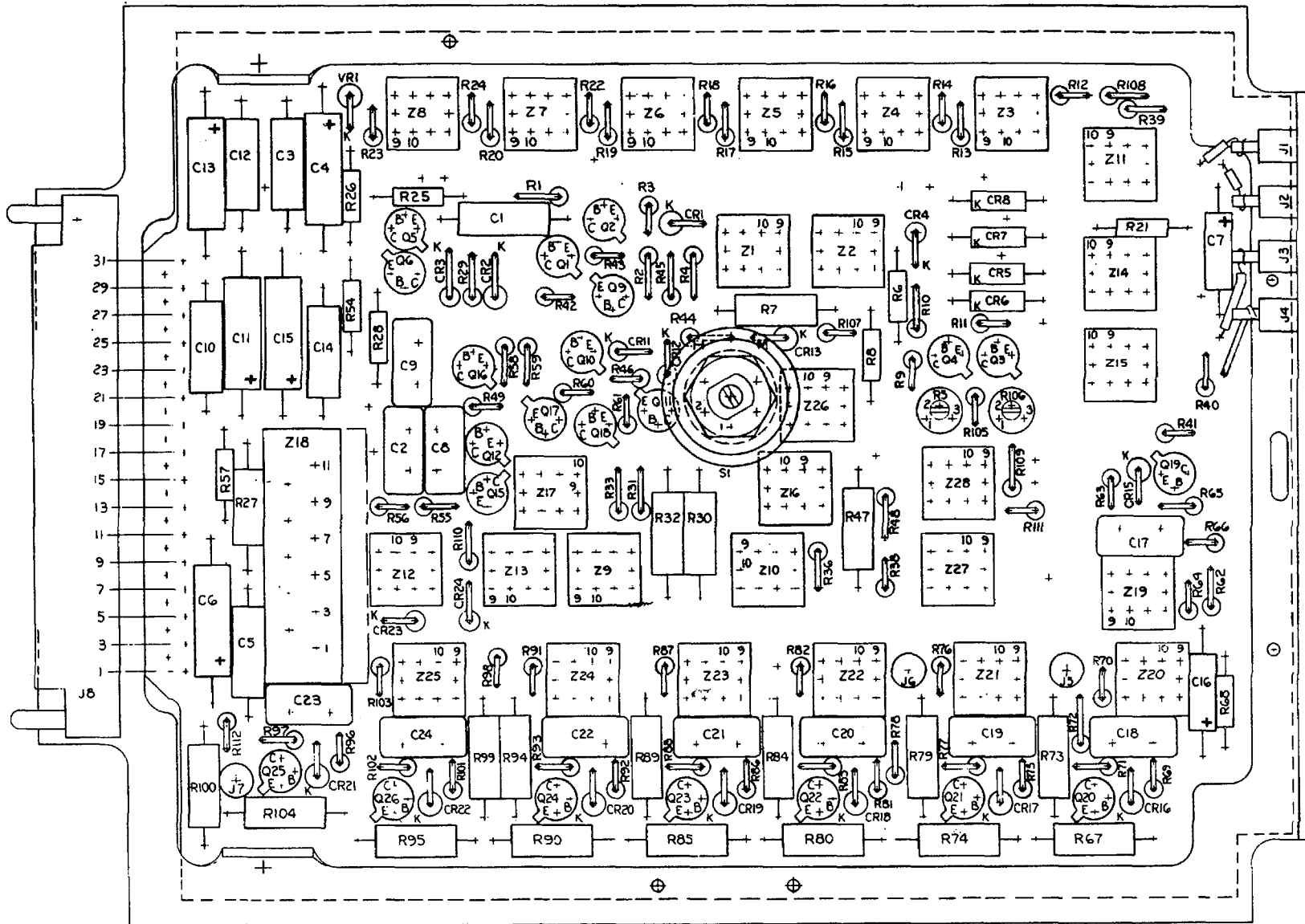


Figure 6-18.1. Panel 1A14A/2A14A, top view
6-18.1

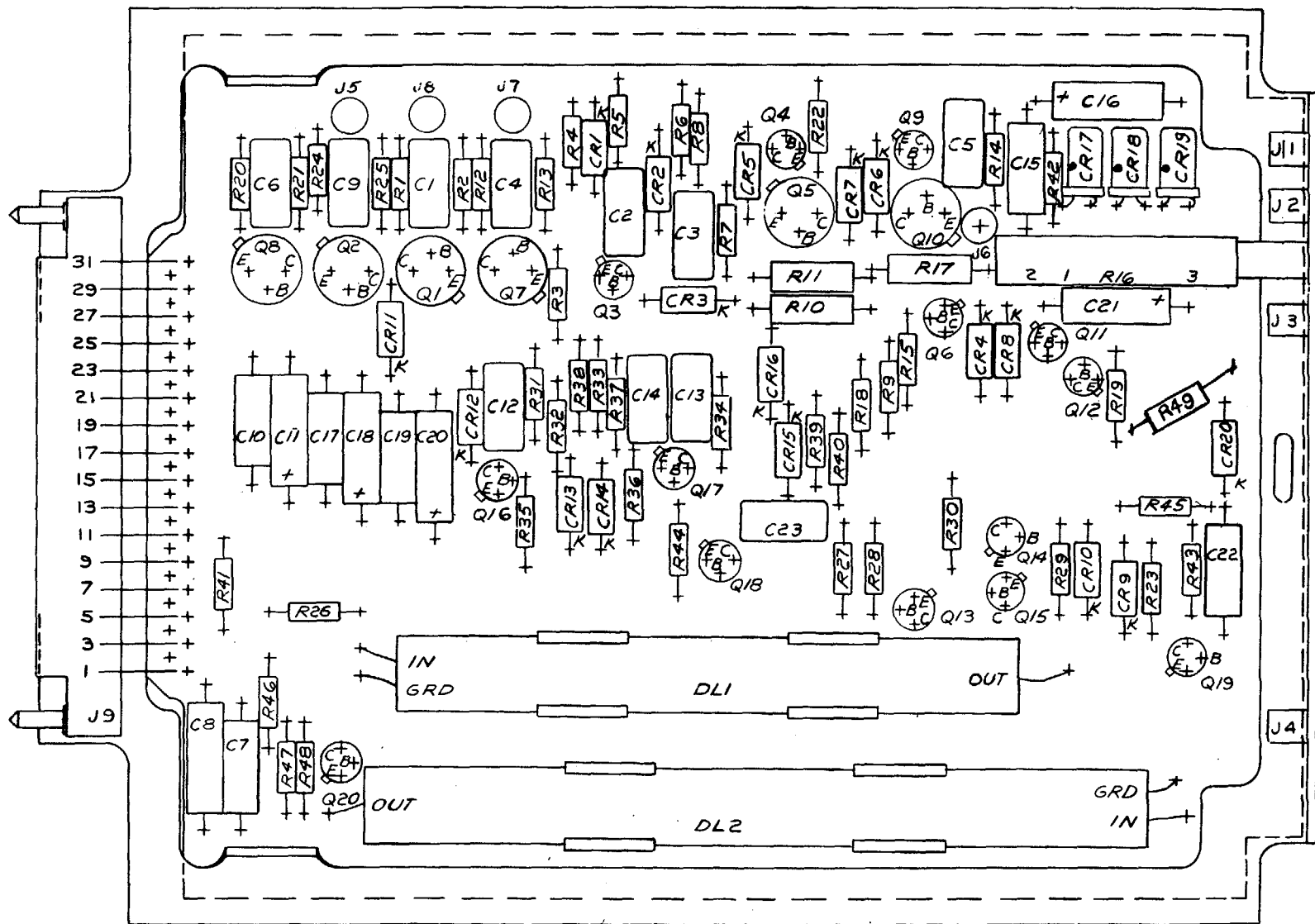


Figure 6-19. Panel 1A15, top view.

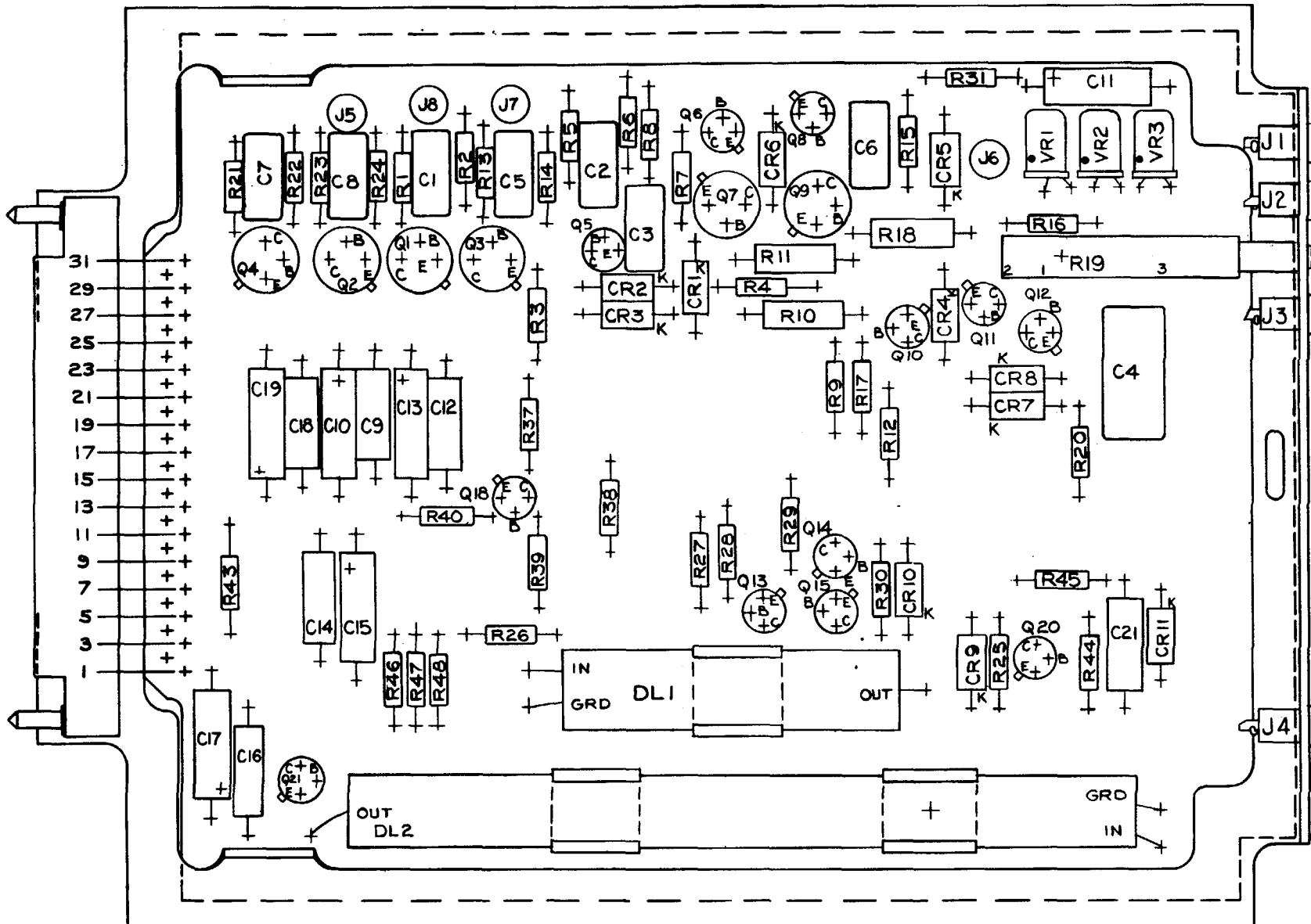


Figure 6-20. Panel 2A15, top view.

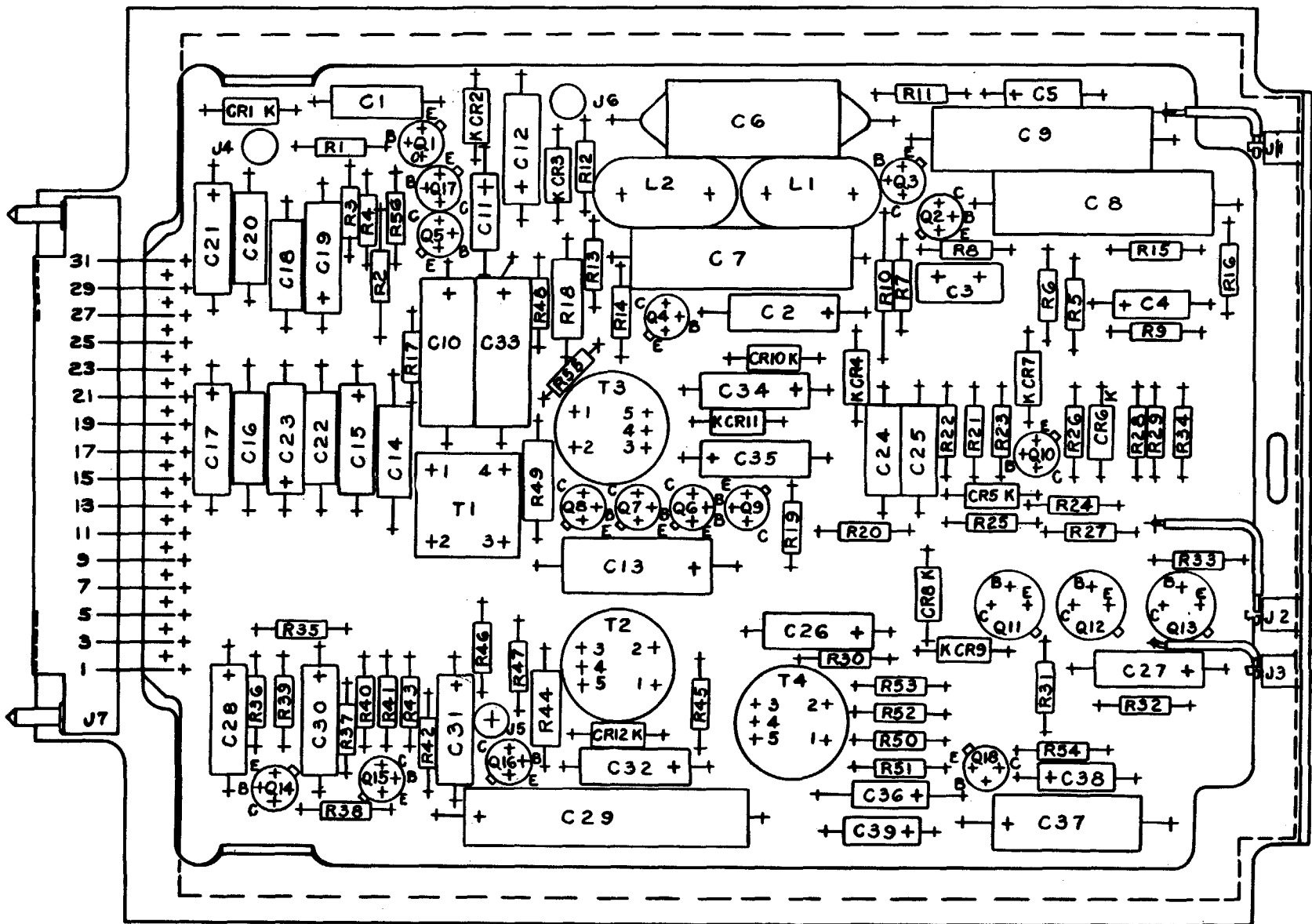


Figure 6-21. Panel 1A16/2A16, top view.

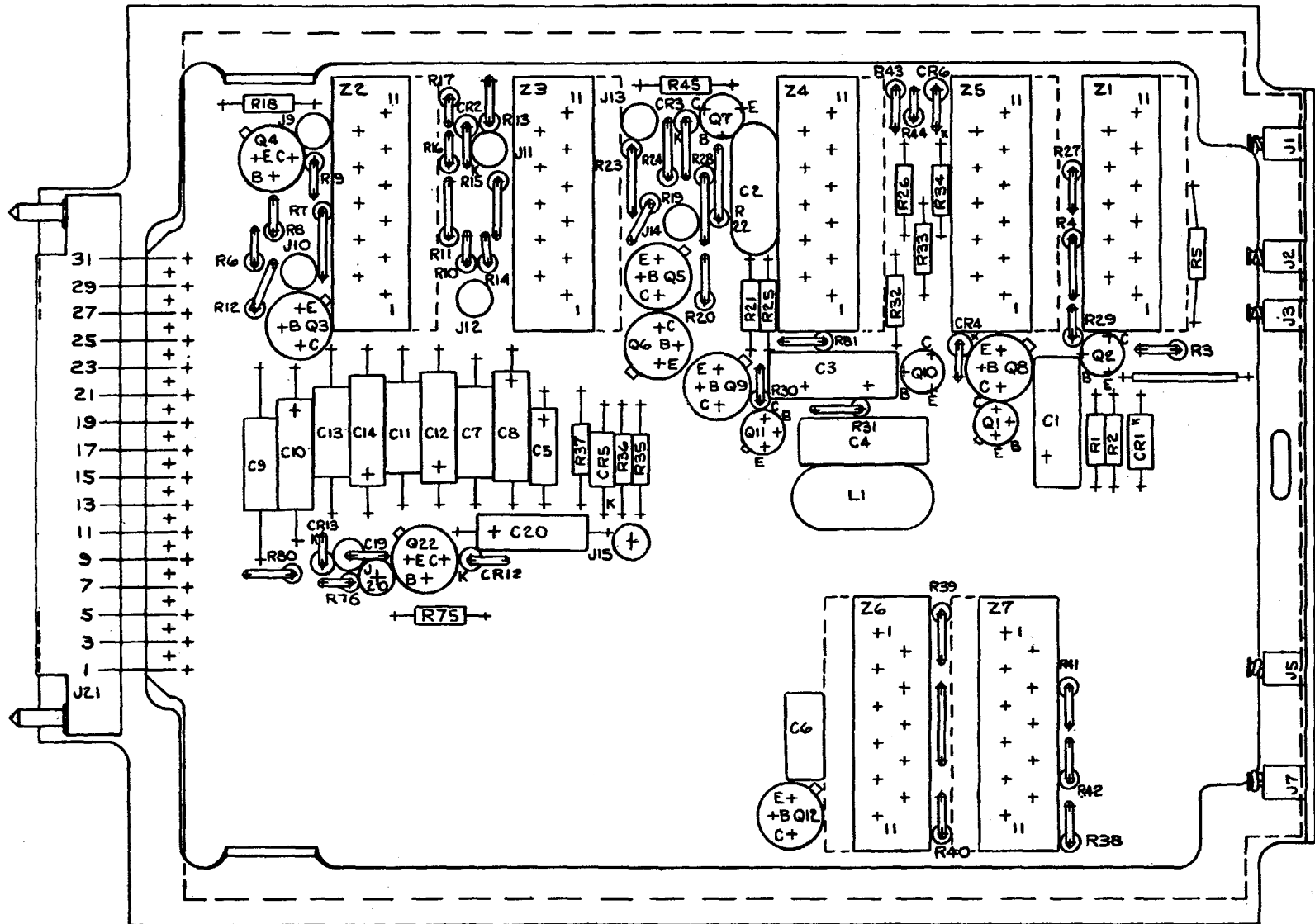


Figure 6-22. Panel 1A17, top view.

TM5805-367-35/3-111

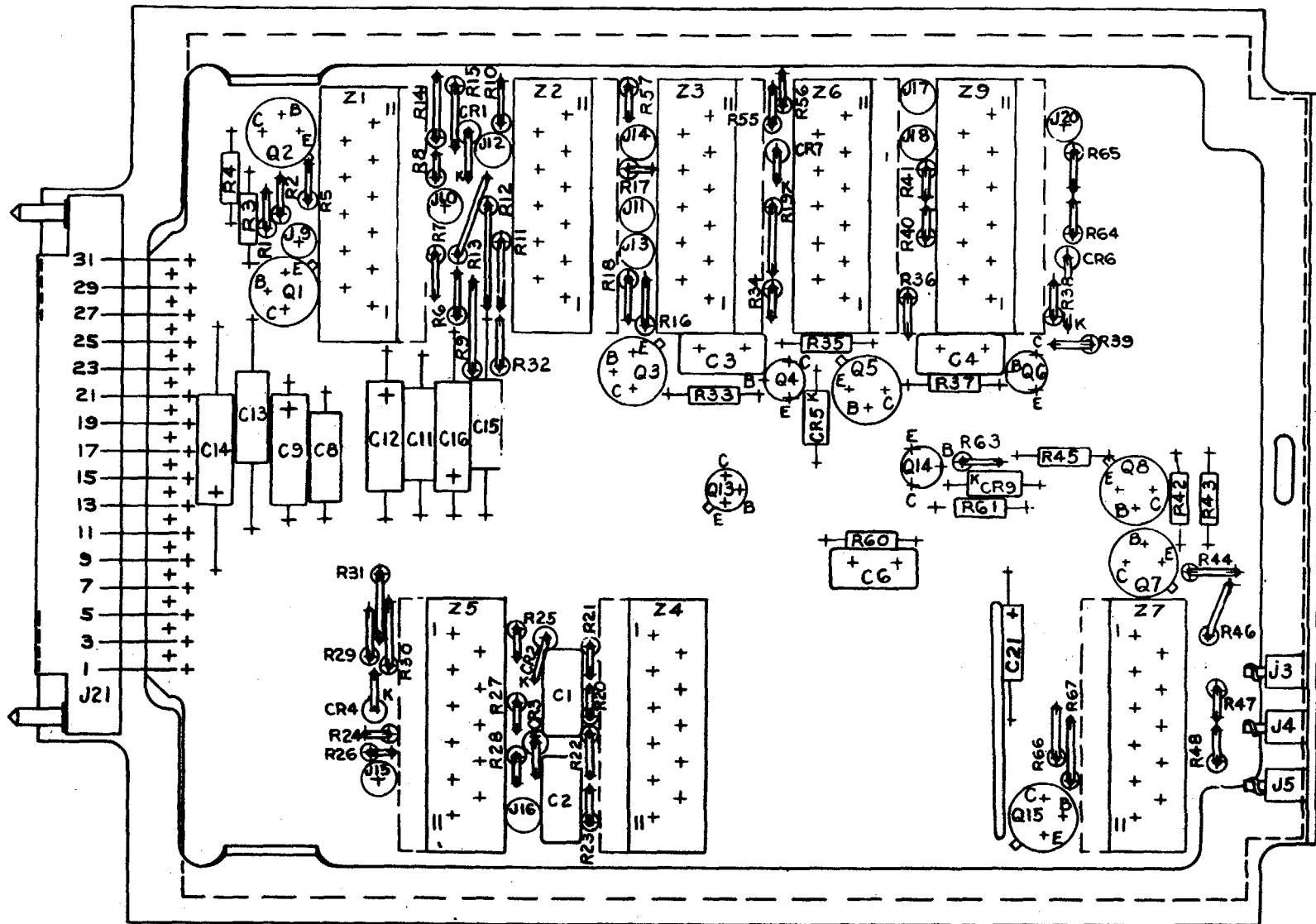


Figure 6-23. Panel 2A17, top view.

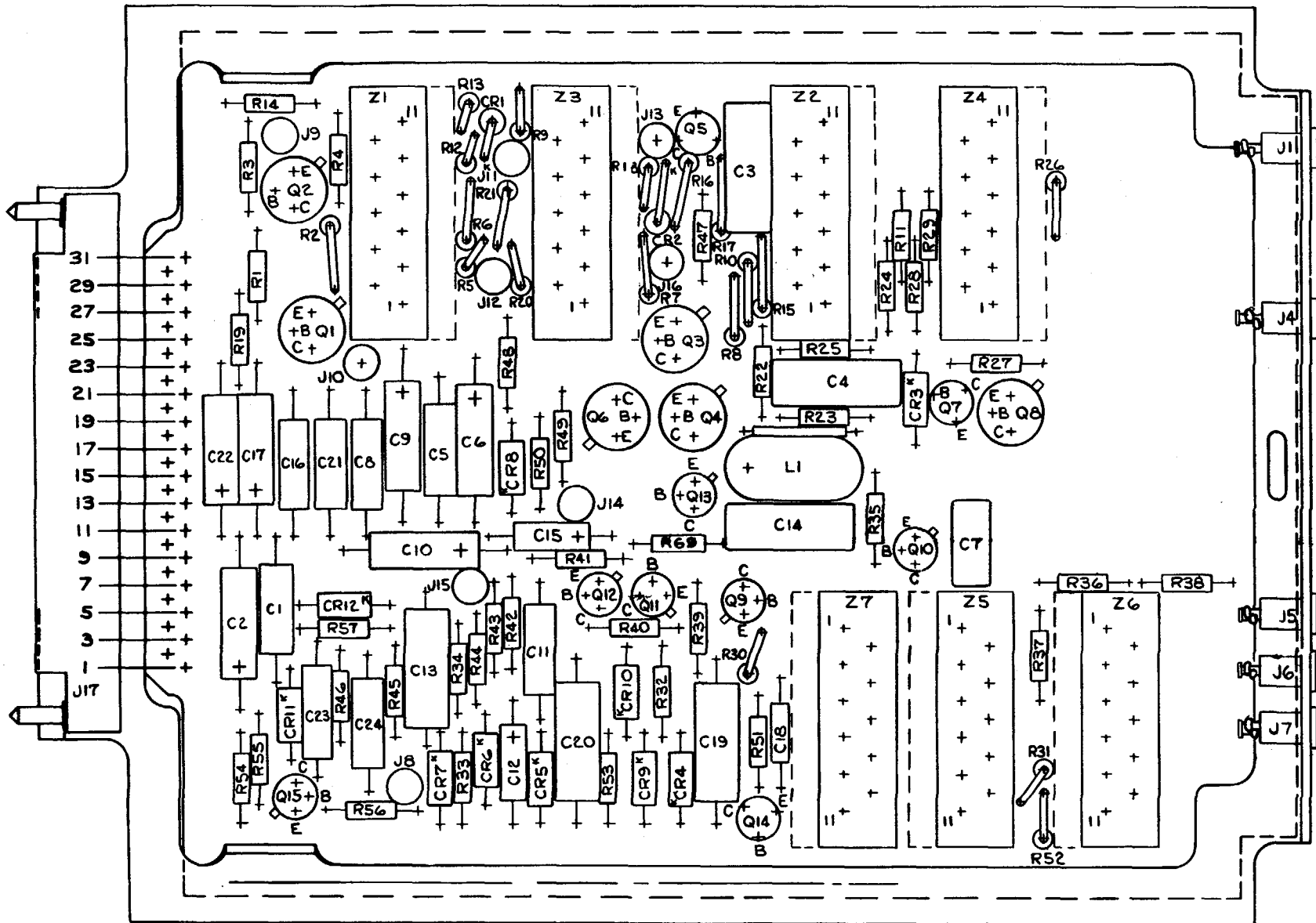


Figure 6-24. Panel 1A18, top view.

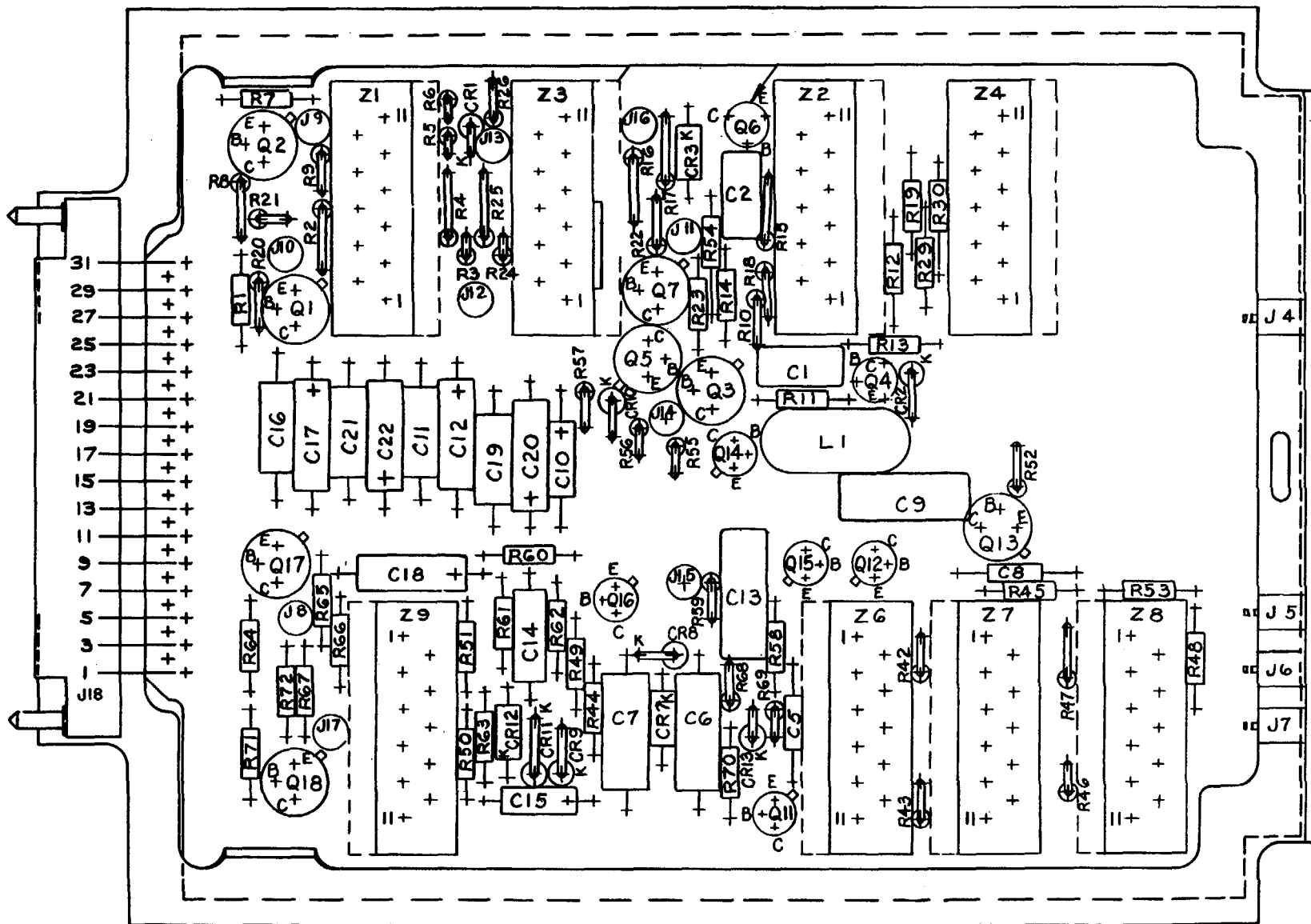


Figure 6-25. Panel 2A18, top view.

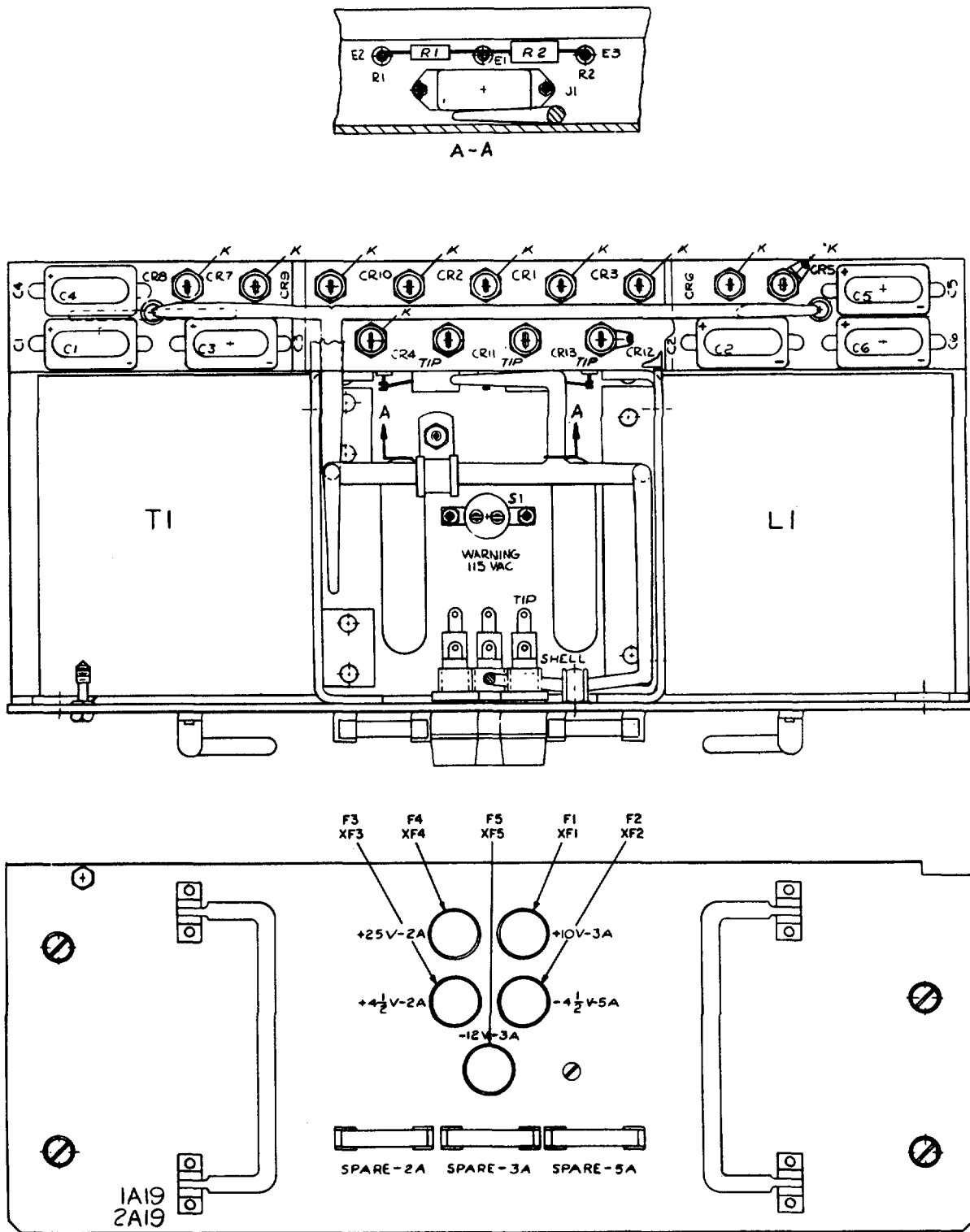
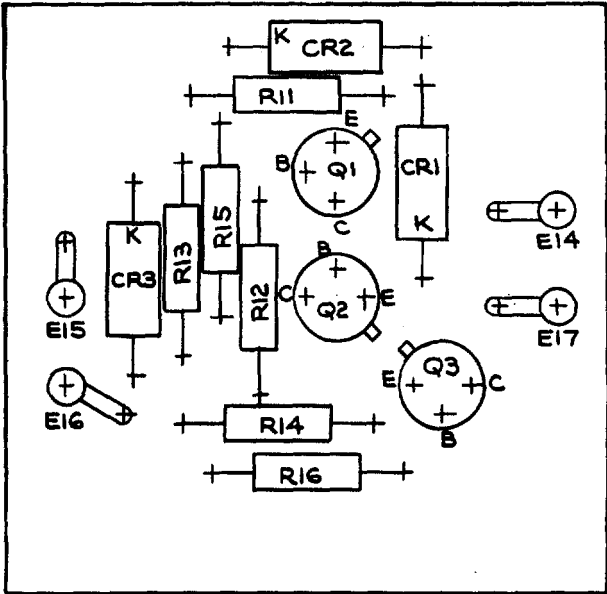


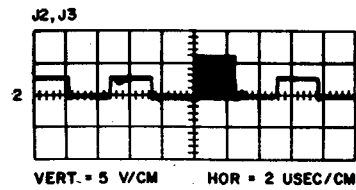
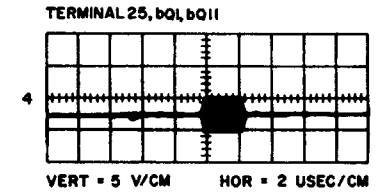
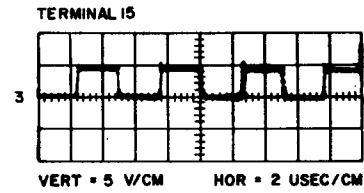
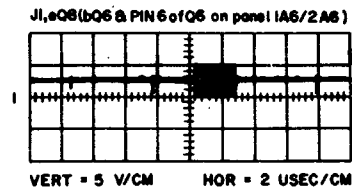
Figure 6-26. Panel 1A19/2A19, top view.

TM5805-367-35/3-123



TM5805-367-35/3-C1-2

Figure 6-26.1. Panel 1A20/2A20, top view.

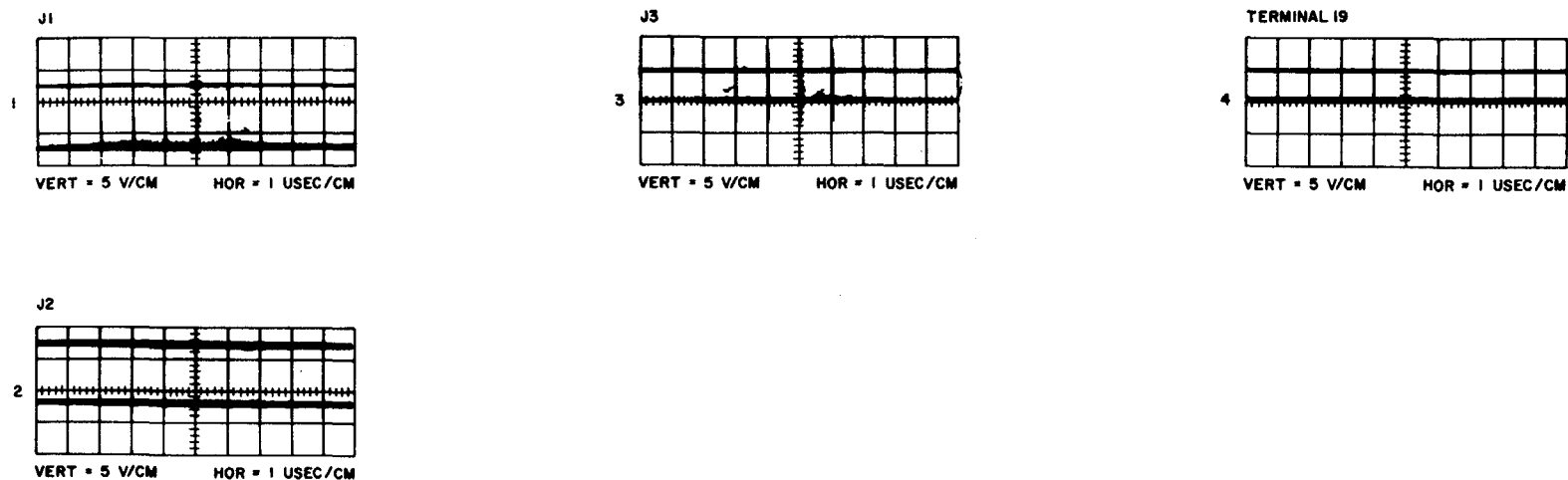


CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

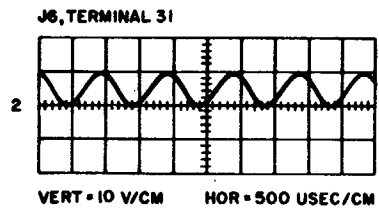
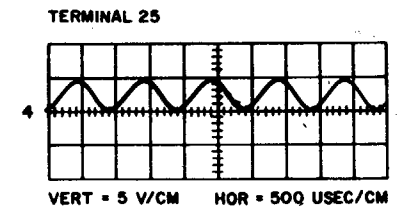
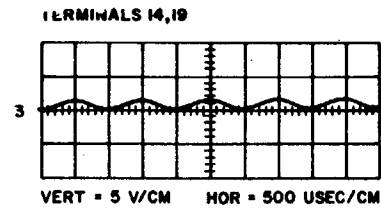
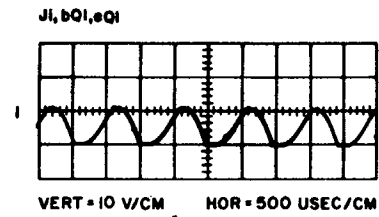
TM5805-367-35/3-61

Figure 6-27. Panel 1A7, troubleshooting waveforms.



- CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS
1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
 2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
 3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
 4. ADDRESS SWITCH AT MASTER.
 5. AUX SWITCH AT OUT.
 6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.
- TM5805-367-35/3-88

Figure 6-29. Panel 1A11/2A11, troubleshooting waveforms.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

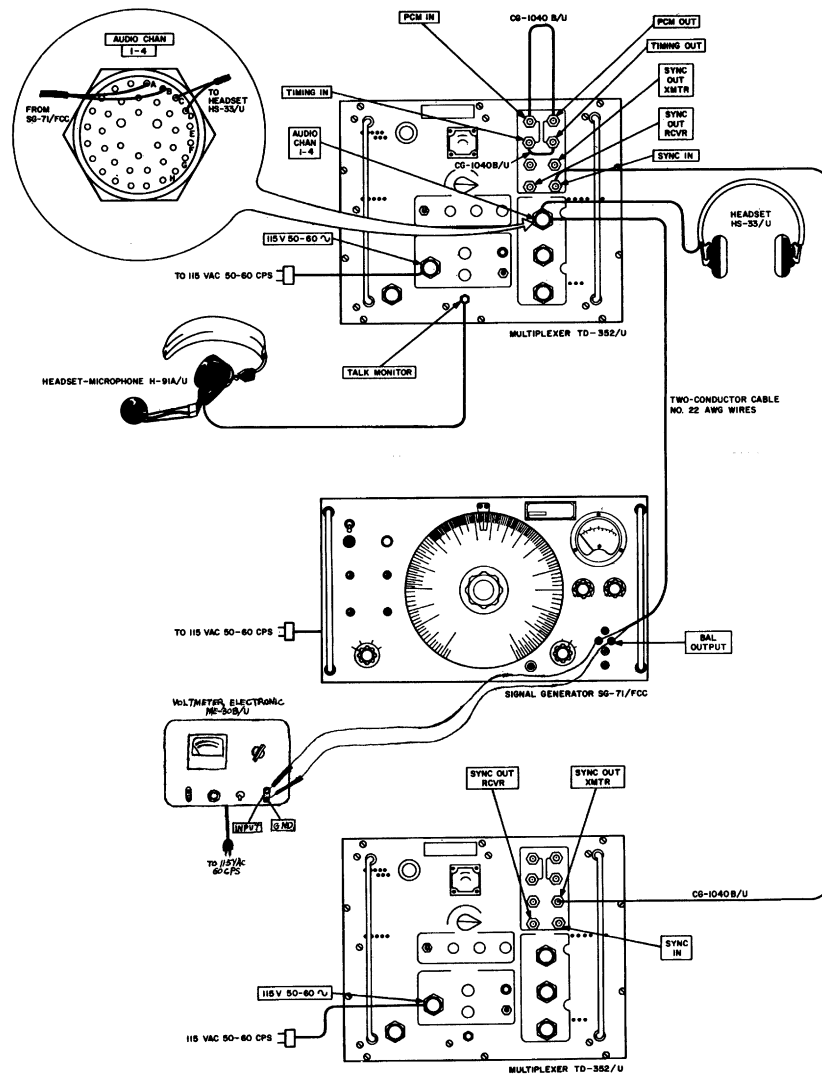
TM5805-367-35/3-110

Figure 6-30. Panel 1A16/2A16, troubleshooting waveforms.

APPENDIX A

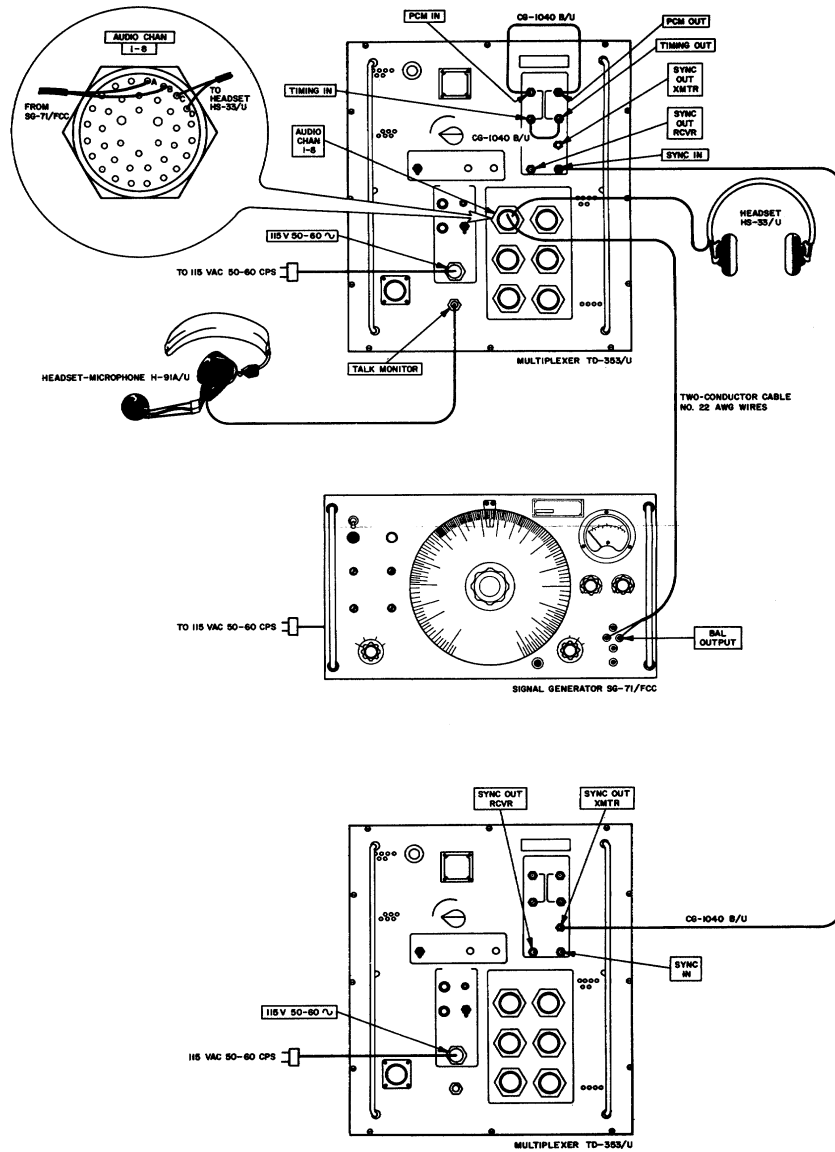
REFERENCES

DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms
TB SIG 222	Solder and Soldering
TB SIG 355-1	Depot Inspection, Standard for Repaired Signal Equipment
TB SIG 355-2	Depot Inspection, Standard for Refinishing Repaired Signal Equipment
TB SIG 355-3	Depot Inspection, Standard for Moisture and Fungus Resistant Treatment
TM 11-664	Theory and Use of Electronic Test Equipment
TM 11-4000	Troubleshooting and Repair of Radio Equipment
TM 11-6625-366-10	Operator's Manual for Multimeter TS-352B/U (NSN 6625-00-553-0142)
TM 11-5540	Electric Light Assembly MX-1292/PAQ (NSN 6995-00-378-5449)
TM 11-5805-367-12	Operator's and Organizational Maintenance Manual Multiplexers, TD-202/U (NSN 5805-00-884-2176), TD-203/U (5805 00-884-2177), TD-204/U (5805-00-900-8200), TD-352/U (5805-00-900-8199) and TD-353/U (5805-00-985-9153) Restorers, Pulse Form, TD-206/G (5805-00-868-8078) and TD-206B/G (5805-01-020-2251) and Converters, Telephone Signal, CV-1548/G (5805-00-069-8795) and CV-1548A/G (5805-00-069-8795)
TM 11-5805-367-20P-3	Organizational Maintenance Repair Parts and Special Tool Lists; Multiplexers TD-352/U and TD-353/U (NSN 5805-00-900-8199 and 5805-00-985-9153)
TM 11-5805-367-34P-3	Direct Support and General Support Maintenance Repair Parts and Special Tools Lists (Including Depot Maintenance Repair Parts and Special Tools) for Multiplexers TD-352/U and TD-353/U (NSN 5805-00-900-8199 and 5805-00-985-9153)
TM 11-6625-200-15	Operator's, Organizational, Direct Support, General Support, and Depot Maintenance Manual: Multimeters ME-26A/U (NSN 6625-00-360-2493), ME-26B/U, ME-26C/U (6625-00-646-9409), ME-26D/U, (6625-00-913-9781)
TM 11-6625-320-12	Operator's and Organizational Maintenance Manual: Voltmeter, Meter ME-30A/U and Voltmeters, Electronic ME-30B/U, ME-30C/U, and ME-30E/U
TM 11-6625-414-50	Depot Maintenance Manual: Voltmeter TS-443/U
TM 11-6625-535-15	Operator's, Organizational, Direct Support, General Support and Depot Maintenance Manual: Oscilloscope AN/USM-140A
TM 11-6625-539-15	Operator's Organizational, Field and Depot Maintenance Manual: Transistor Set, TS-1836/U
TM 11-6625-648-12	Operator's and Organizational Maintenance Manual: Test Set, Telephone, AN/PTM-7 (NSN 6625-00-902-7574)
DMWR 11-5805-367/3	Depot Maintenance Work Requirement Multiplexers TD-352/U (NSN 5805-00-900-8199) and TD-353/U (NSN 5805-00-985-9153)



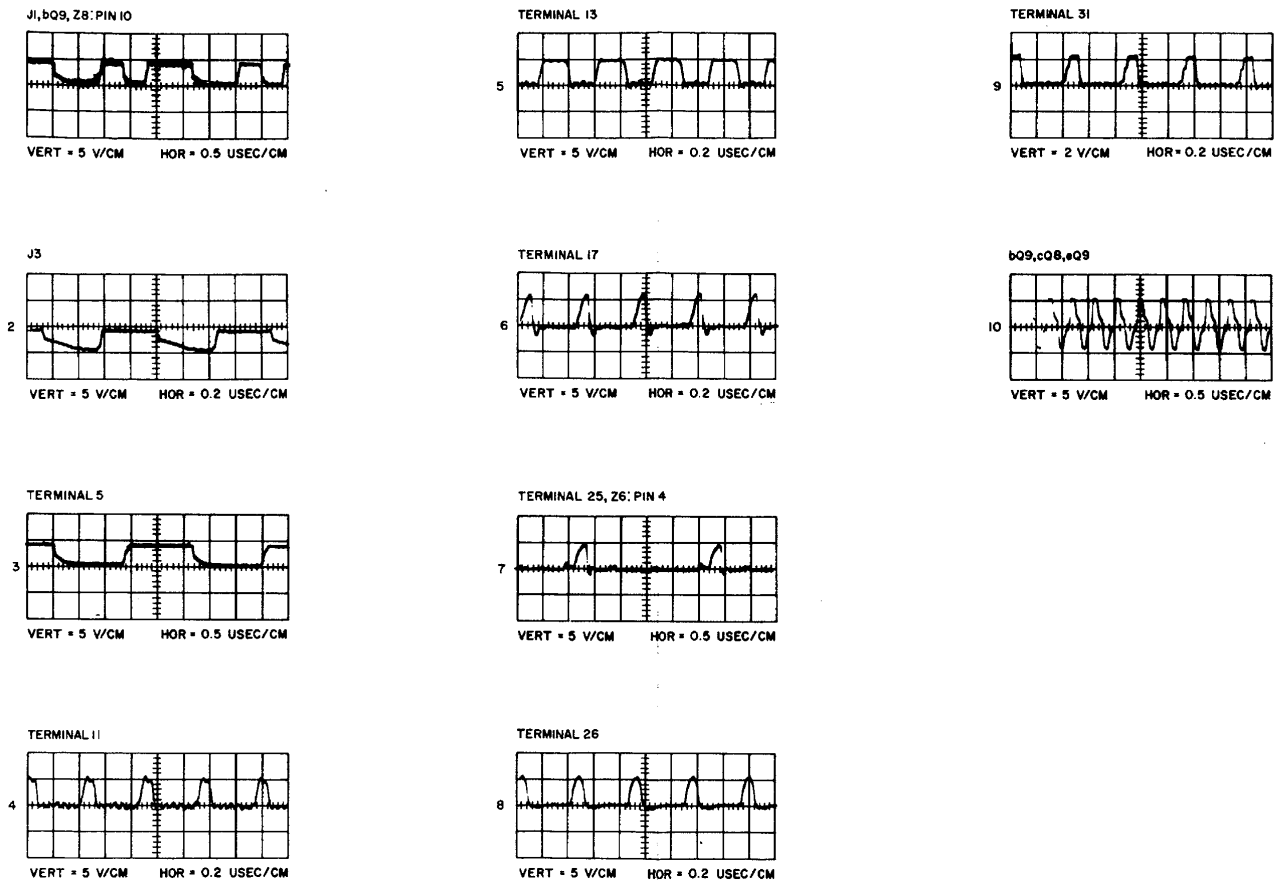
TM5805-367-35/3-128

Figure 5-1. Multiplexer TD-352/U, performance test setup.



TM5805-367-35/3-129

Figure 5-2. Multiplexer TD-353/U, performance test setup.

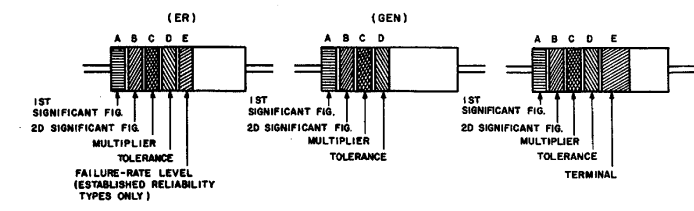


CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

TM5805-367-35/3-67

Figure 6-28. Panel 1A8, troubleshooting waveforms.



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS. COLOR CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE 1
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

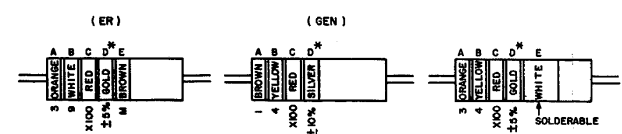
BAND A	BAND B	BAND C	BAND D	BAND E
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR
BLACK	0	BLACK	0	BROWN
BROWN	1	BROWN	1	RED
RED	2	RED	2	ORANGE
ORANGE	3	ORANGE	3	YELLOW
YELLOW	4	YELLOW	4	GREEN
GREEN	5	GREEN	5	BLUE
BLUE	6	BLUE	6	PURPLE (VIOLET)
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7	GRAY
GRAY	8	GRAY	8	WHITE
WHITE	9	WHITE	9	

COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	1	BROWN	±10 (COMP. TYPE ONLY)	BROWN	M=1.0	
BROWN	10	RED	±2	RED	P=0.1	
RED	100	ORANGE	±3	ORANGE	S=0.01	
ORANGE	1,000	YELLOW	±5 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)	YELLOW		
YELLOW	10,000	SILVER		SILVER		SOLDERABLE
GREEN	100,000	GOLD		GOLD		
BLUE	1,000,000	RED		RED		
PURPLE (VIOLET)		WHITE		WHITE		
GRAY	0.01					
WHITE	0.1					

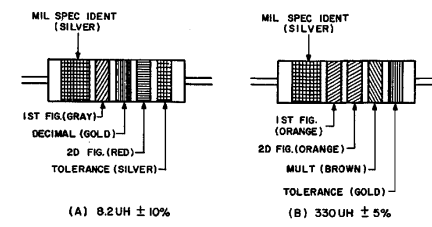
BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)
 BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.
 BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)
 BAND D — THE RESISTANCE TOLERANCE.
 BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1/2 TIMES THE WIDTH OF OTHER BANDS AND INDICATES TYPE OF TERMINAL.
 RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)
 SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:
 2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



COMPOSITION-TYPE RESISTORS FILM-TYPE RESISTORS
 * IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.
 A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS. B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.



COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF THE CODING FOR AN 8.2UH CHOKES IS GIVEN. AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED.

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE		20	
SILVER		10	
GOLD		DECIMAL POINT	5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.

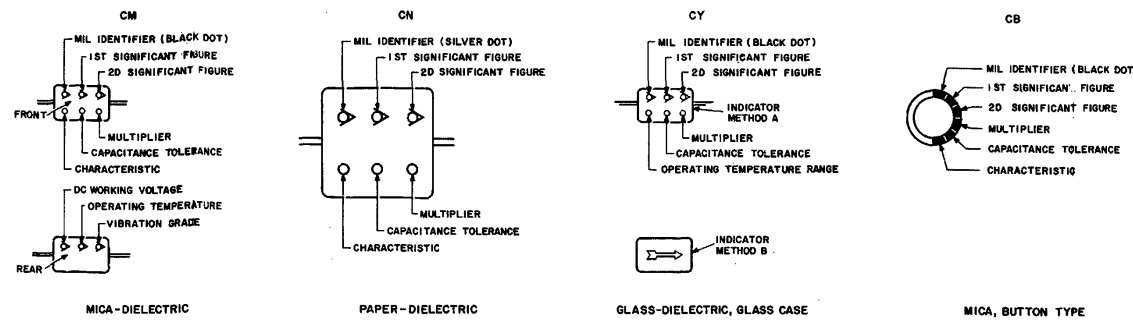


TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER	CAPACITANCE TOLERANCE			CHARACTERISTIC			DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE	
					CM	CN	CY	CM	CN	CB				
BLACK	CM, CN, CY, CB	0	0	1										
BROWN		1	1	10				B	E	B				
RED		2	2	100	±2%			C						
ORANGE		3	3	1,000	±30%			D	D	300				
YELLOW		4	4	10,000				E						
GREEN		5	5		±5%			F		500				
BLUE		6	6											
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1		±5%	±5%							
SILVER	CN			0.01	±10%	±10%	±10%							

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER	CAPACITANCE TOLERANCE	MIL CAPACITANCE ID
BLACK	0	0	0	1	±2.0 UUF	CC
BROWN	-30	1	1	10	±1%	
RED	-80	2	2	100	±2%	±0.25 UUF
ORANGE	-180	3	3	1,000		
YELLOW	-280	4	4			
GREEN	-380	5	5		±4%	±0.5 UUF
BLUE	-470	6	6			
PURPLE (VIOLET)	-750	7	7			
GRAY		8	8	0.01*		
WHITE		9	9	0.1*	±10%	
GOLD	+100			0.1		±1.0 UUF
SILVER				0.01		

- THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
- LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-250, MIL-C-1072B, AND MIL-C-10900C RESPECTIVELY.
- LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
- TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.
- OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

Figure 6-32. Color code markings for MIL STD resistors, inductors.

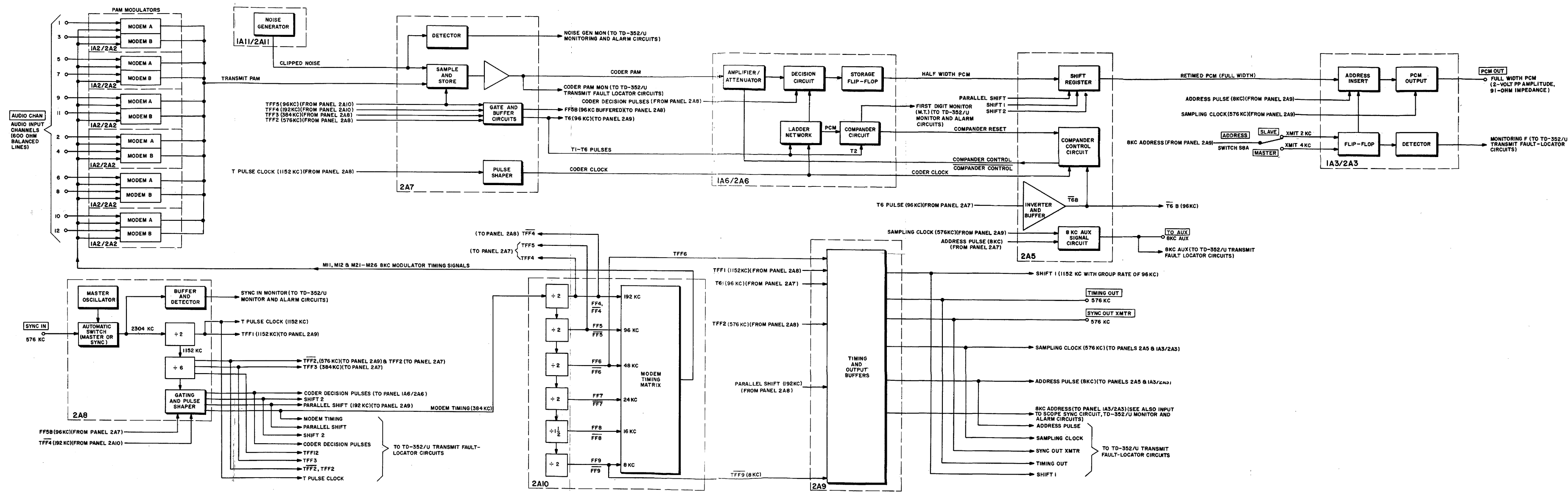
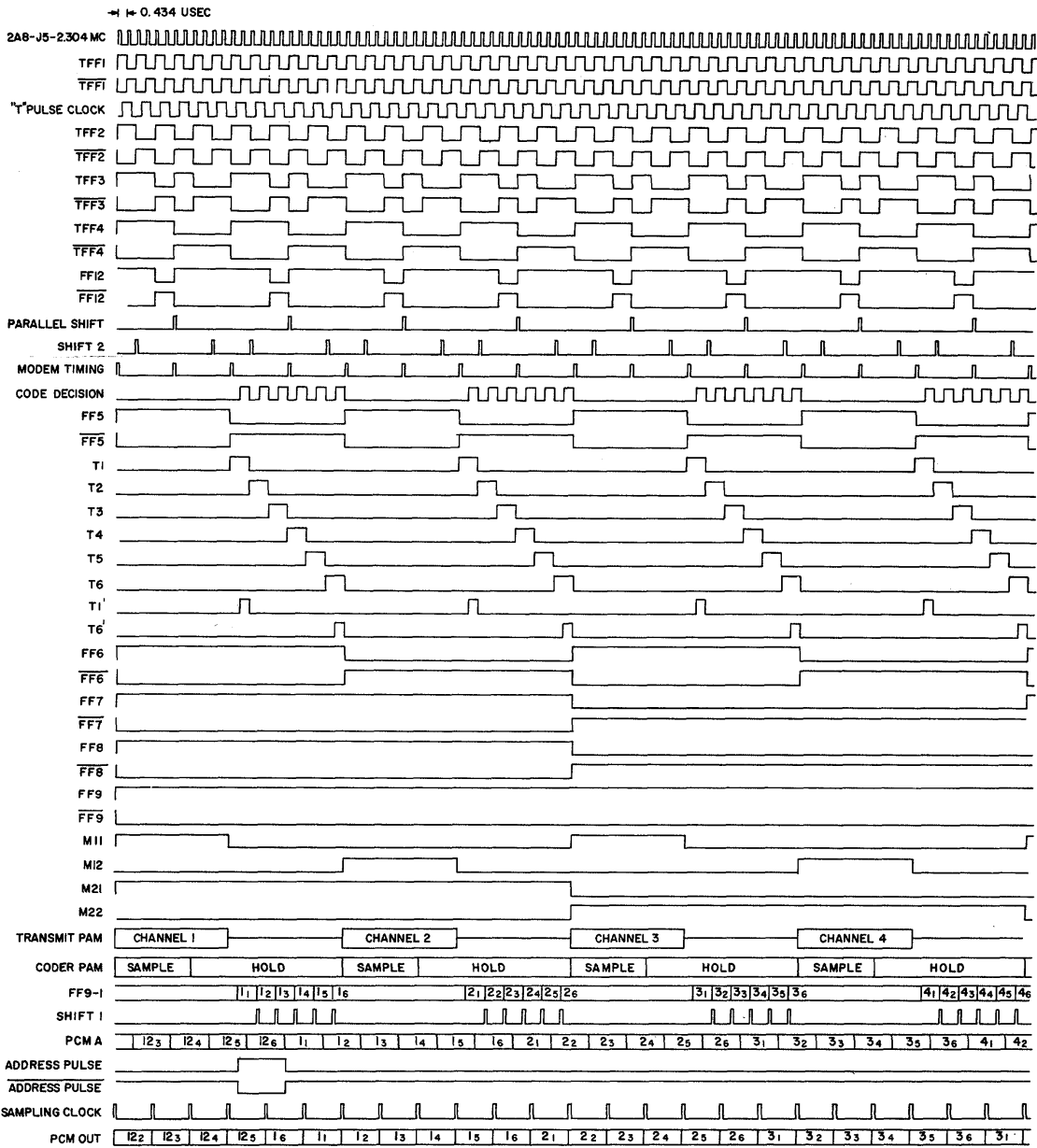


Figure 6-33. Multiplexer TD-352/U transmit circuits, block diagram.



TM5805-367-35/3-4

Figure 6-34. Multiplexer TD-352/U transmit timing, idealized waveforms.

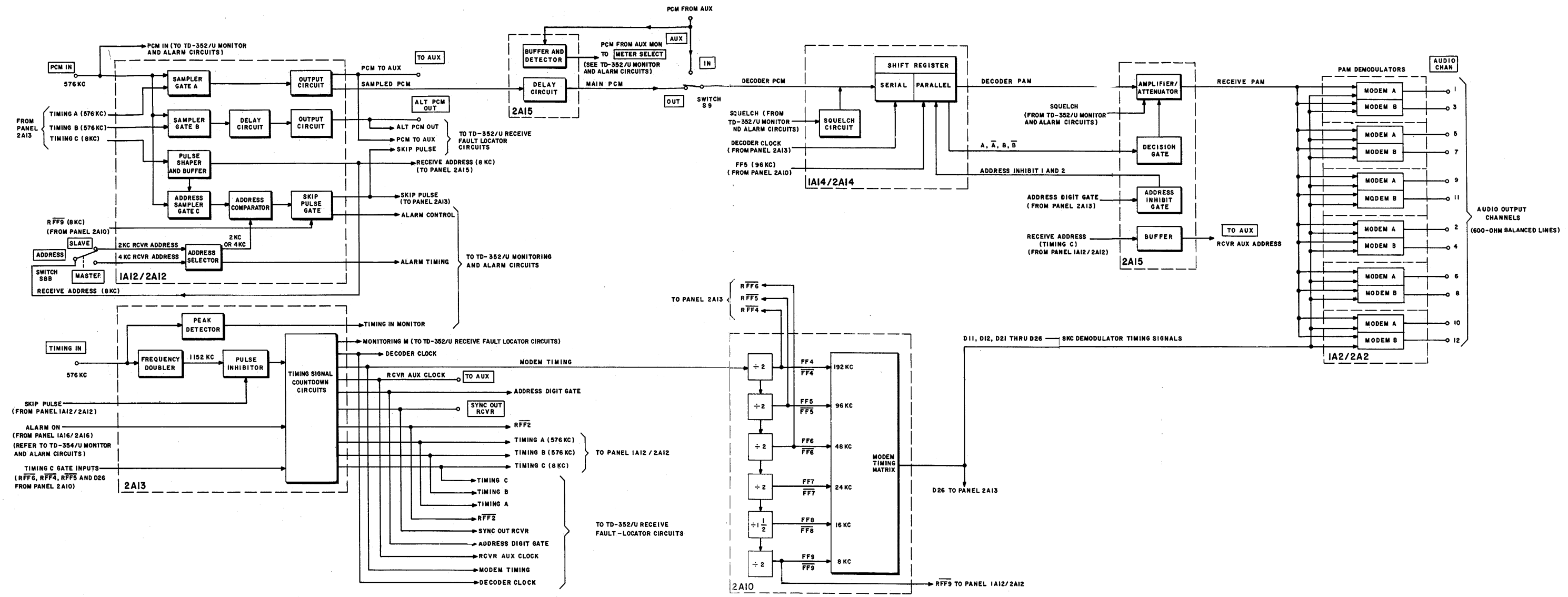


Figure 6-35. Multiplexer TD-352/U receive circuits, block diagram.

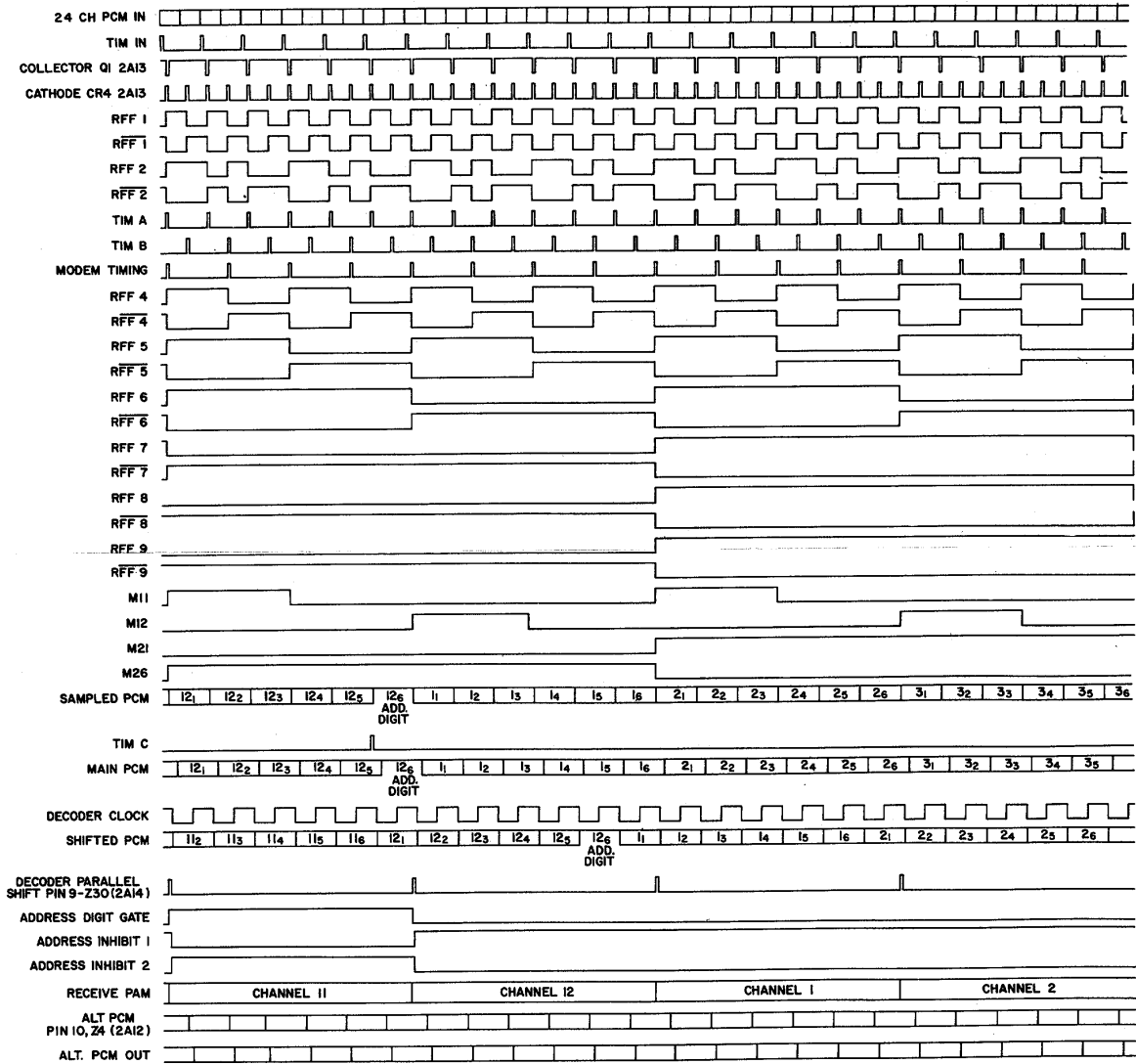


Figure 6-36. Multiplexer TD-352/U receive timing, idealized waveforms.

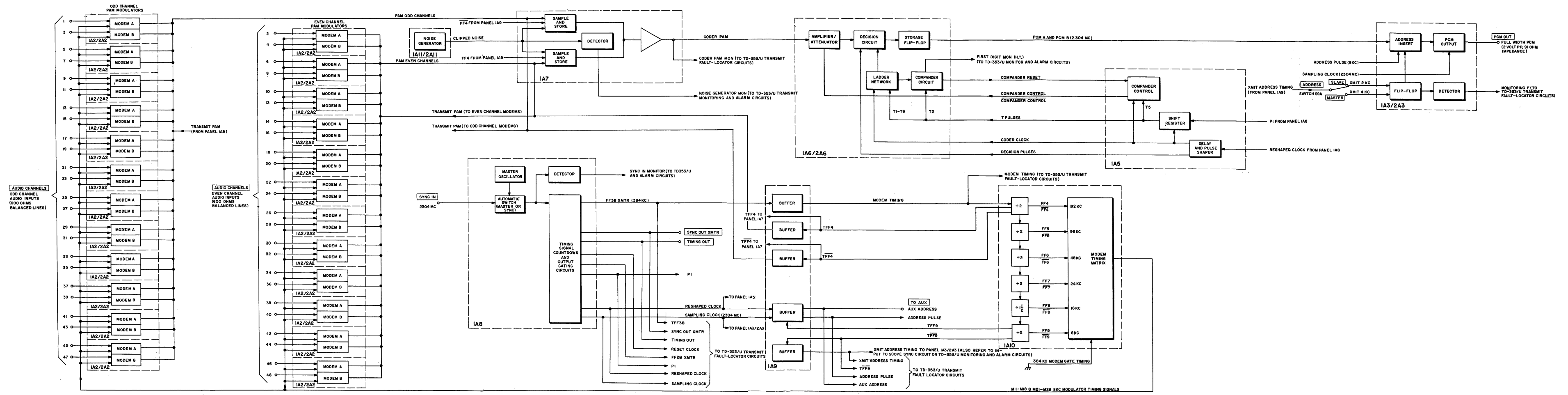


Figure 6-38. Multiplexer TD-353/U transmit circuits, block diagram.

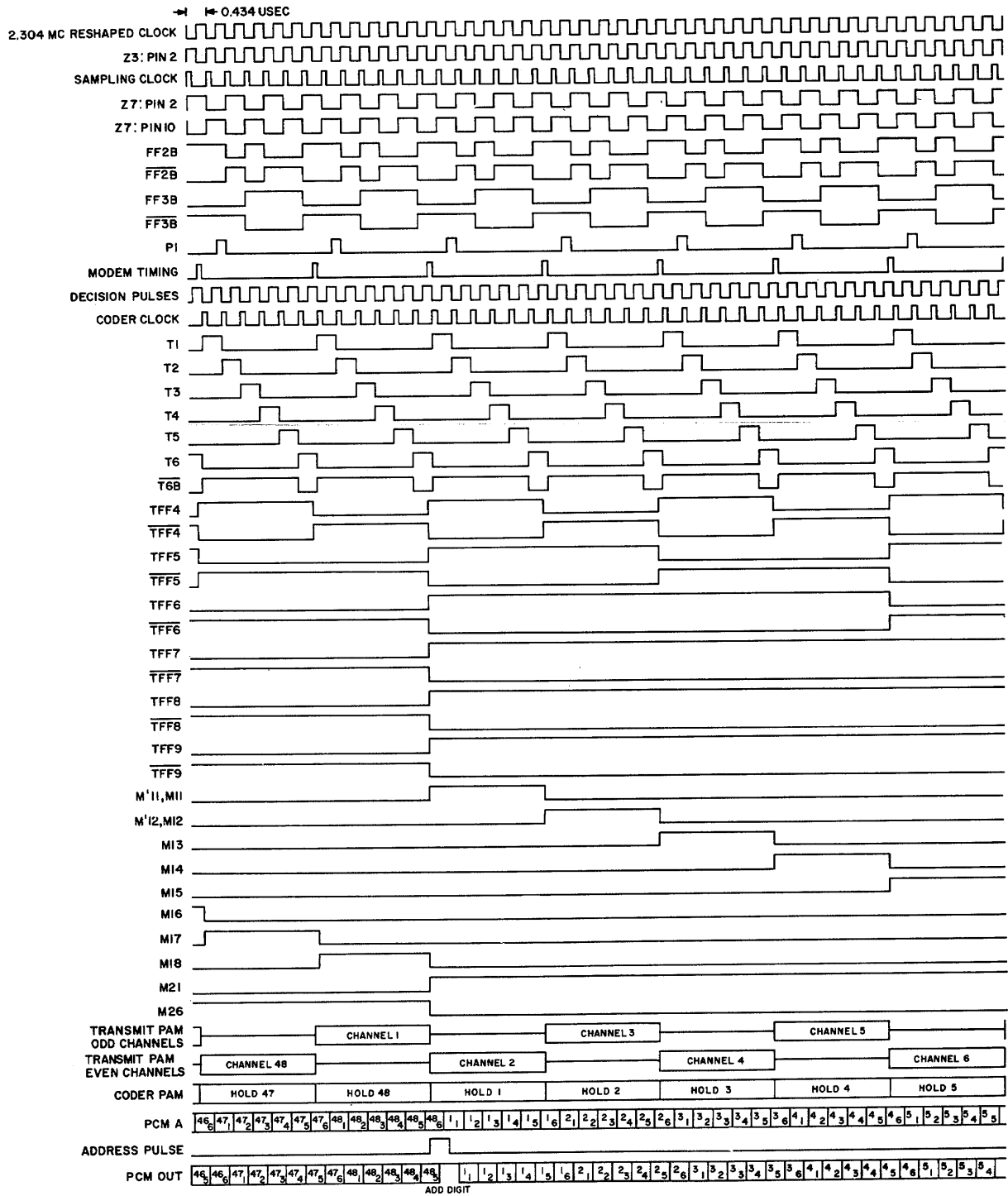


Figure 6-39. Multiplexer TD-353/U transmit timing, idealized waveforms.

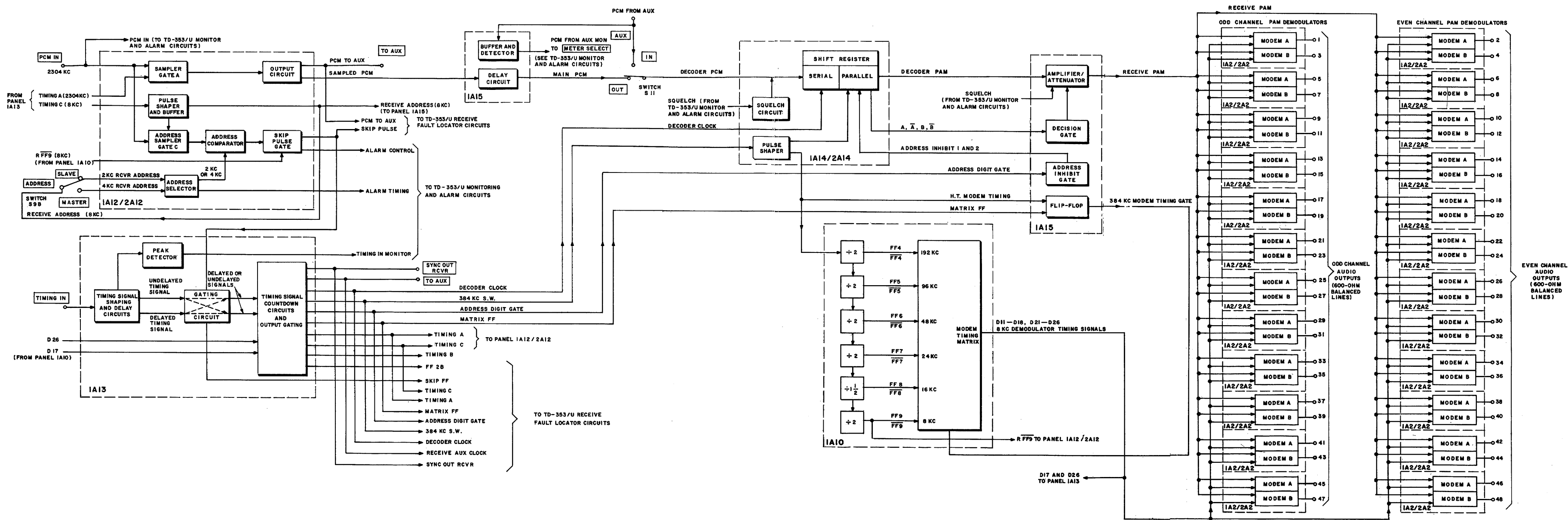


Figure 6-40. Multiplexer TD-353/U receive circuits, block diagram.

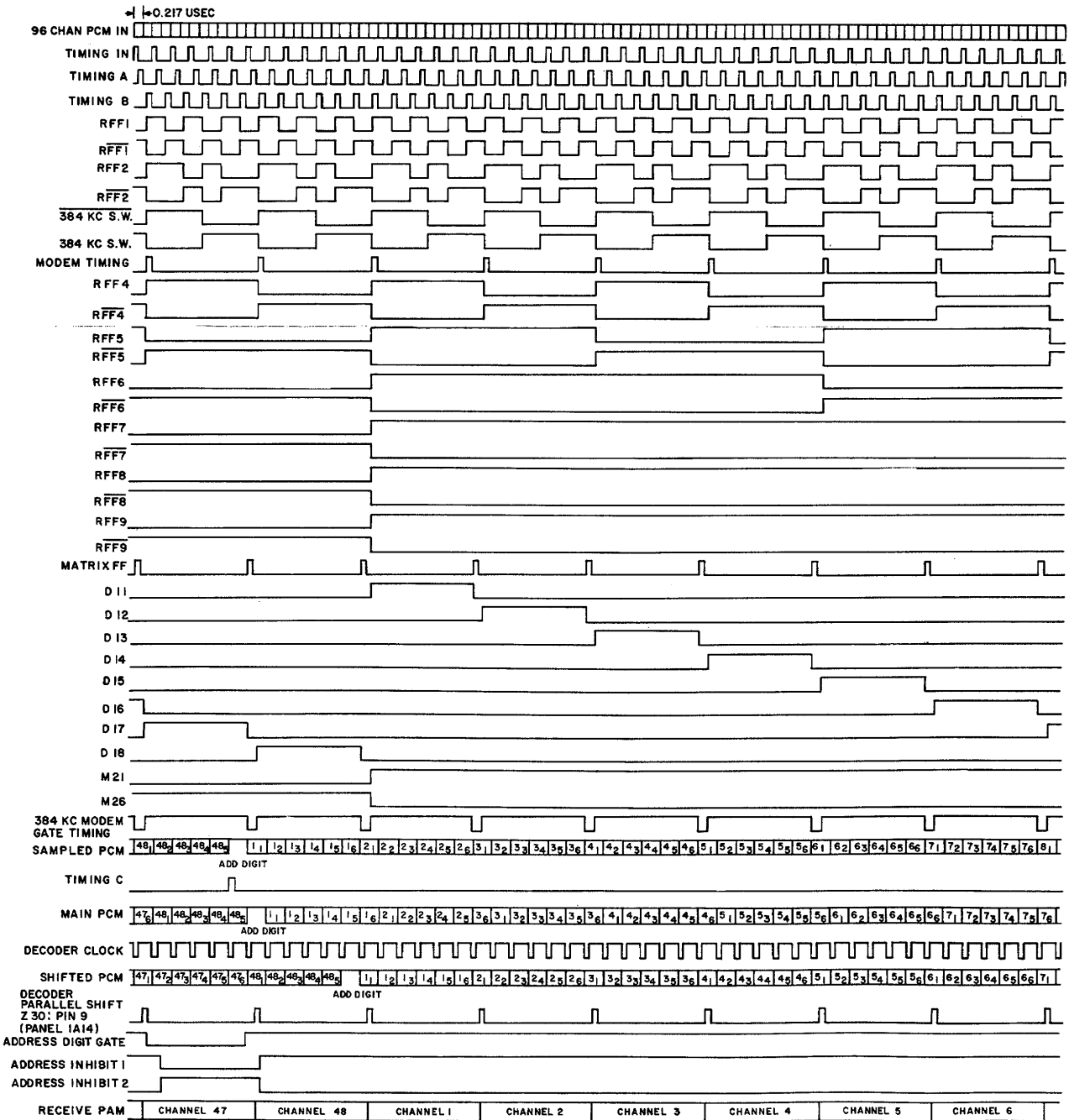


Figure 6-41. Multiplexer TD-353/U receive timing, idealized waveforms.

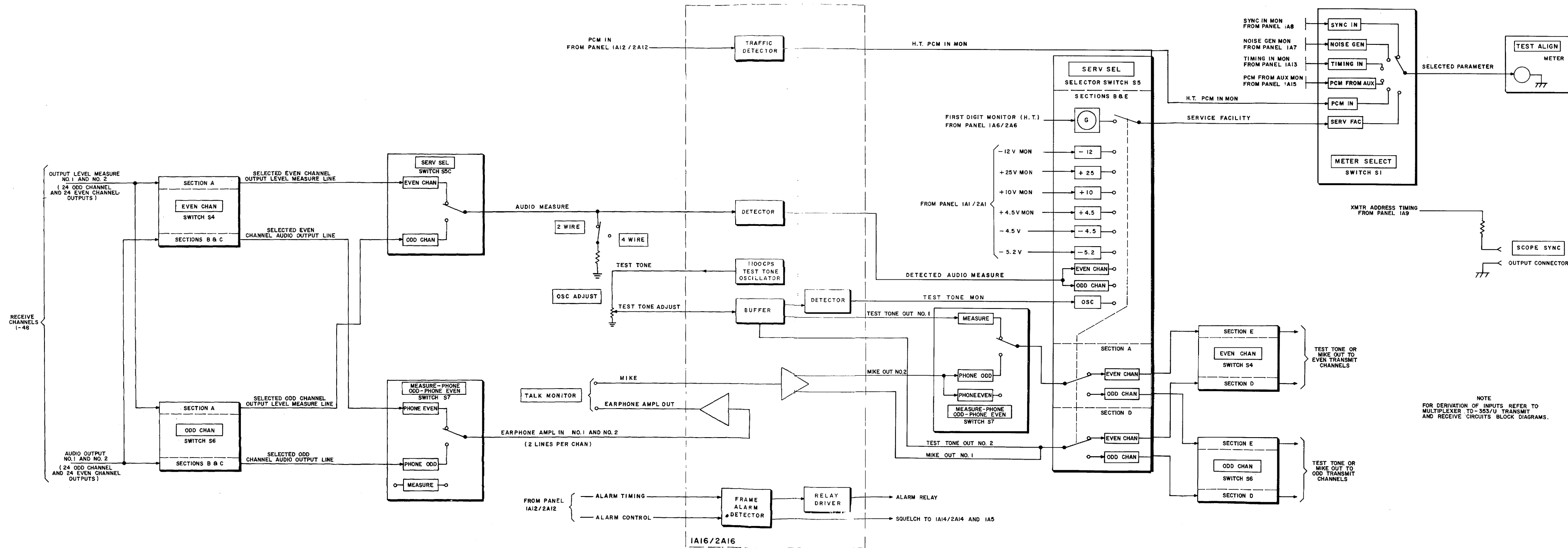


Figure 6-42. Multiplexer TD-353/U, monitor and alarm circuits, block diagram.

Change 3

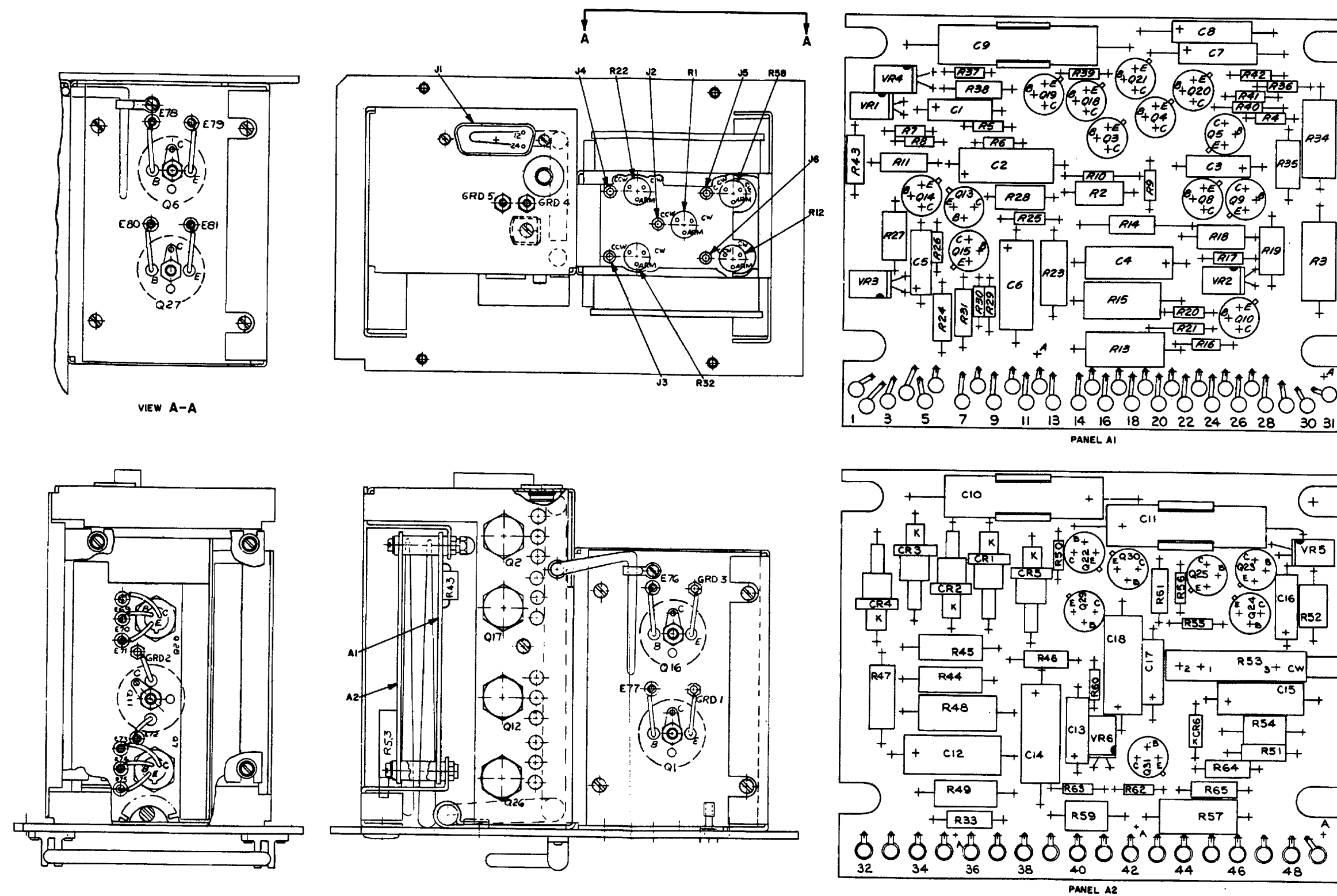
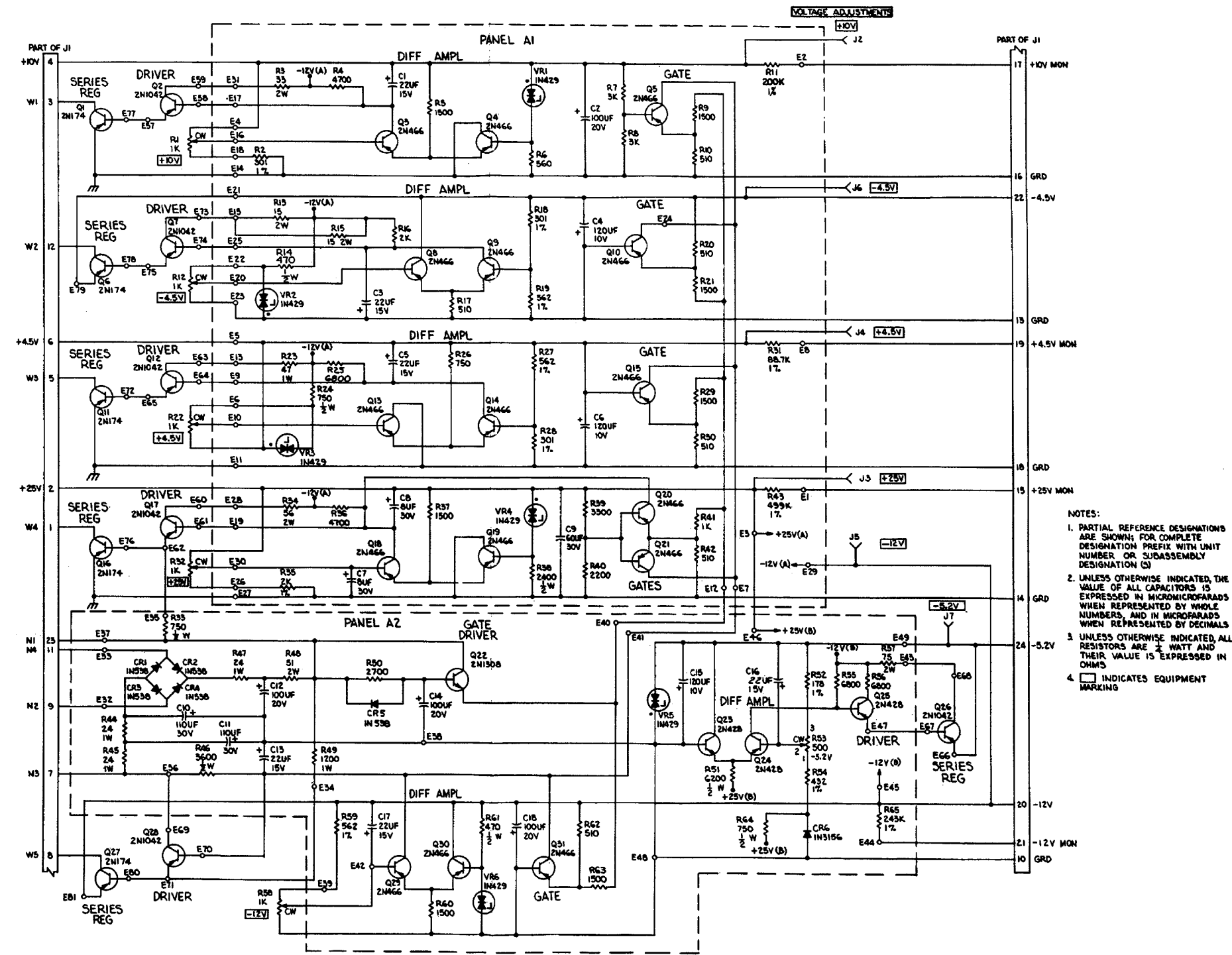


Figure 6-43. Panel 1A1/2A1, top view.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S).
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS.
 3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE 1/2 WATT AND THEIR VALUE IS EXPRESSED IN OHMS.
 4. □ INDICATES EQUIPMENT MARKING.

Figure 6-44. Panel 1A1/2A1, schematic diagram.

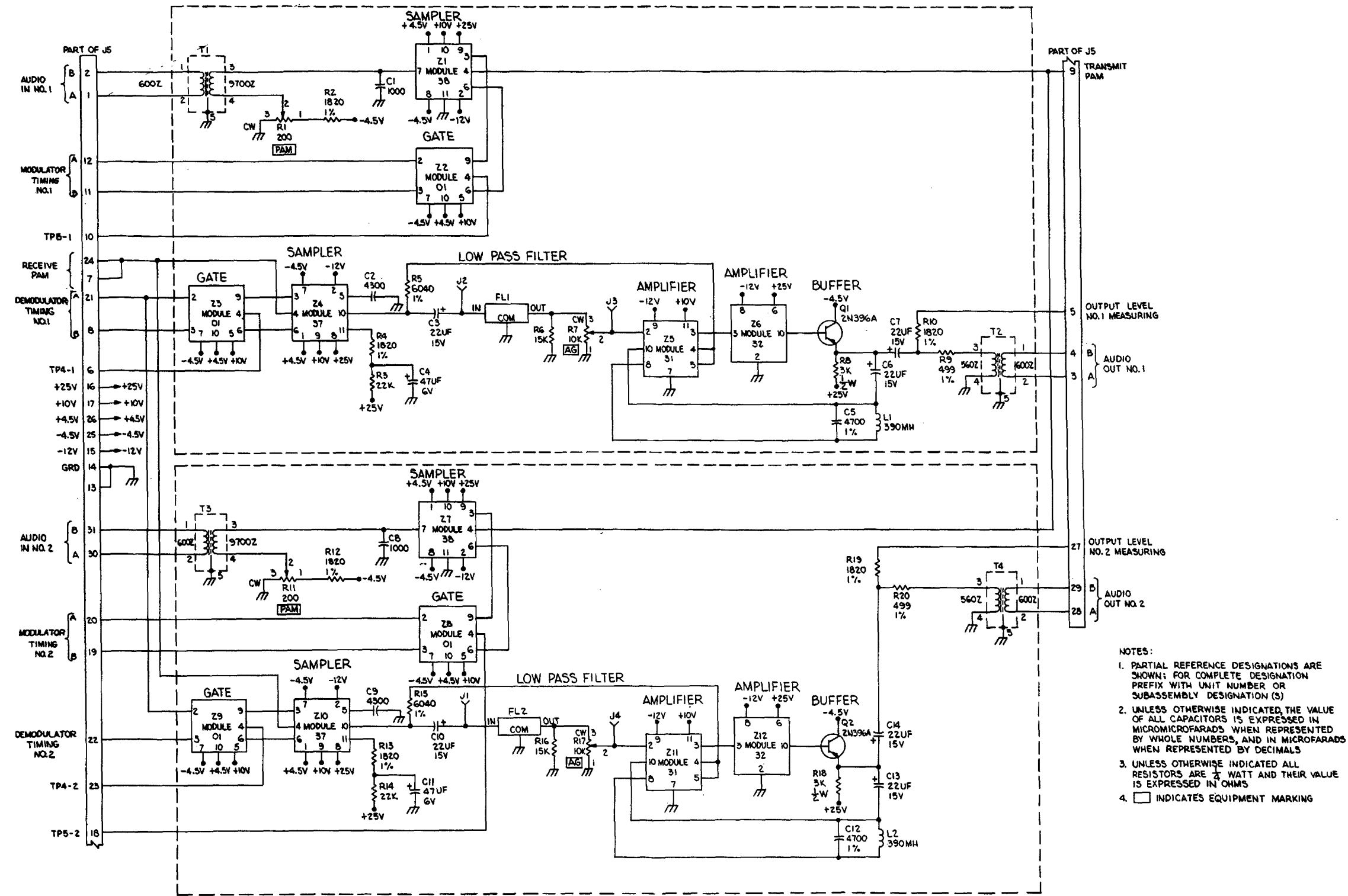


Figure 6-45. Panel 1A2/2A2, schematic diagram.

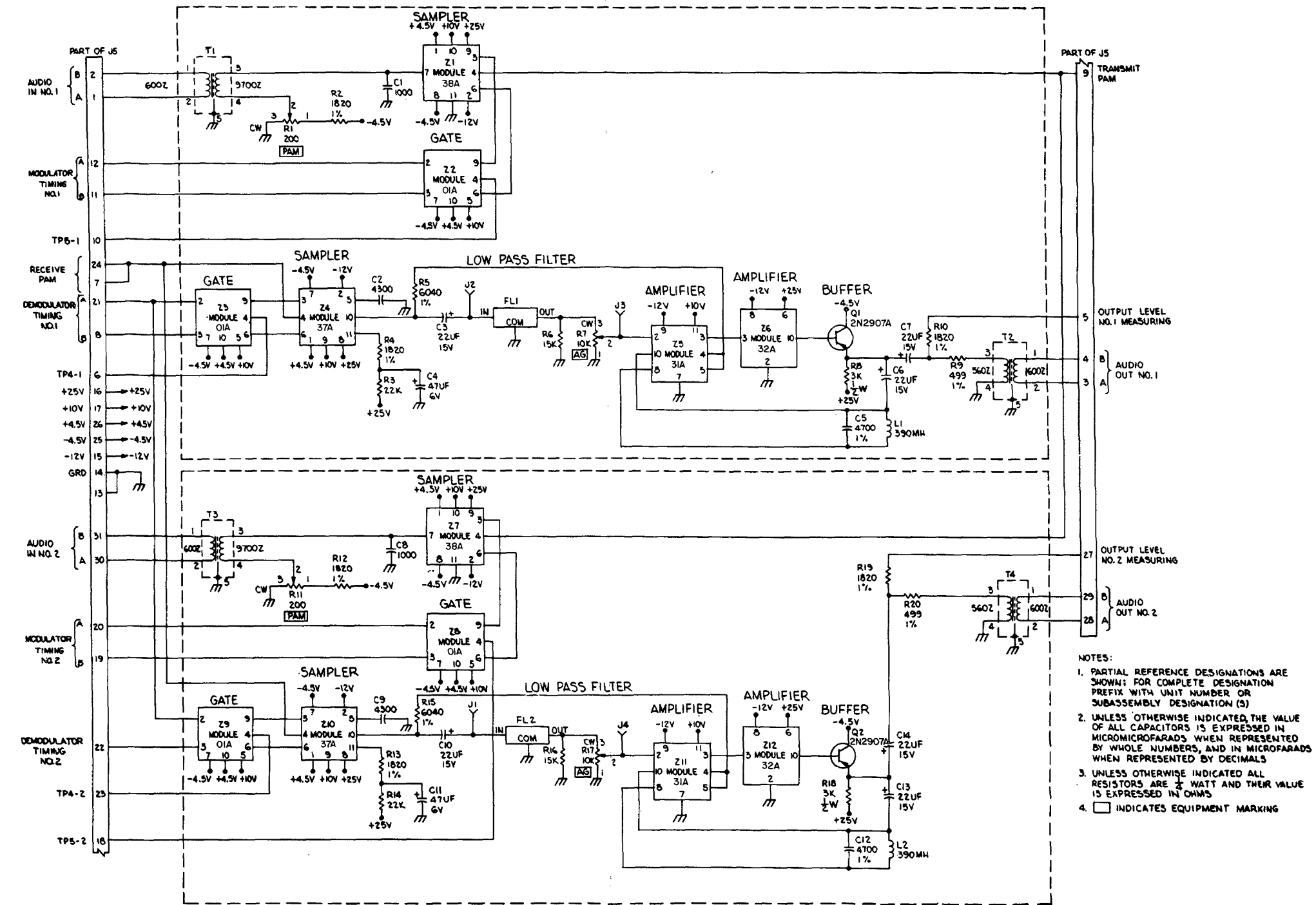
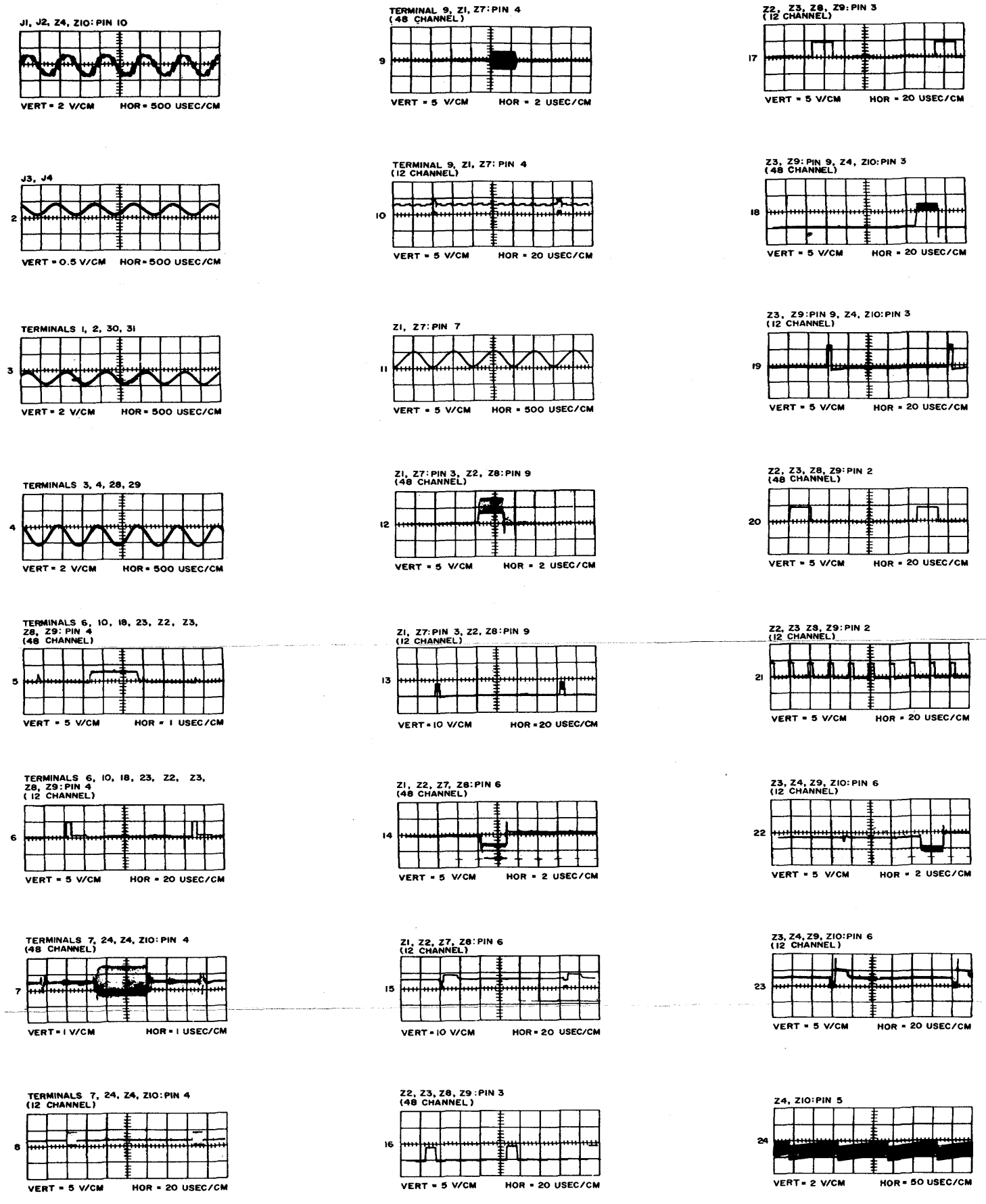
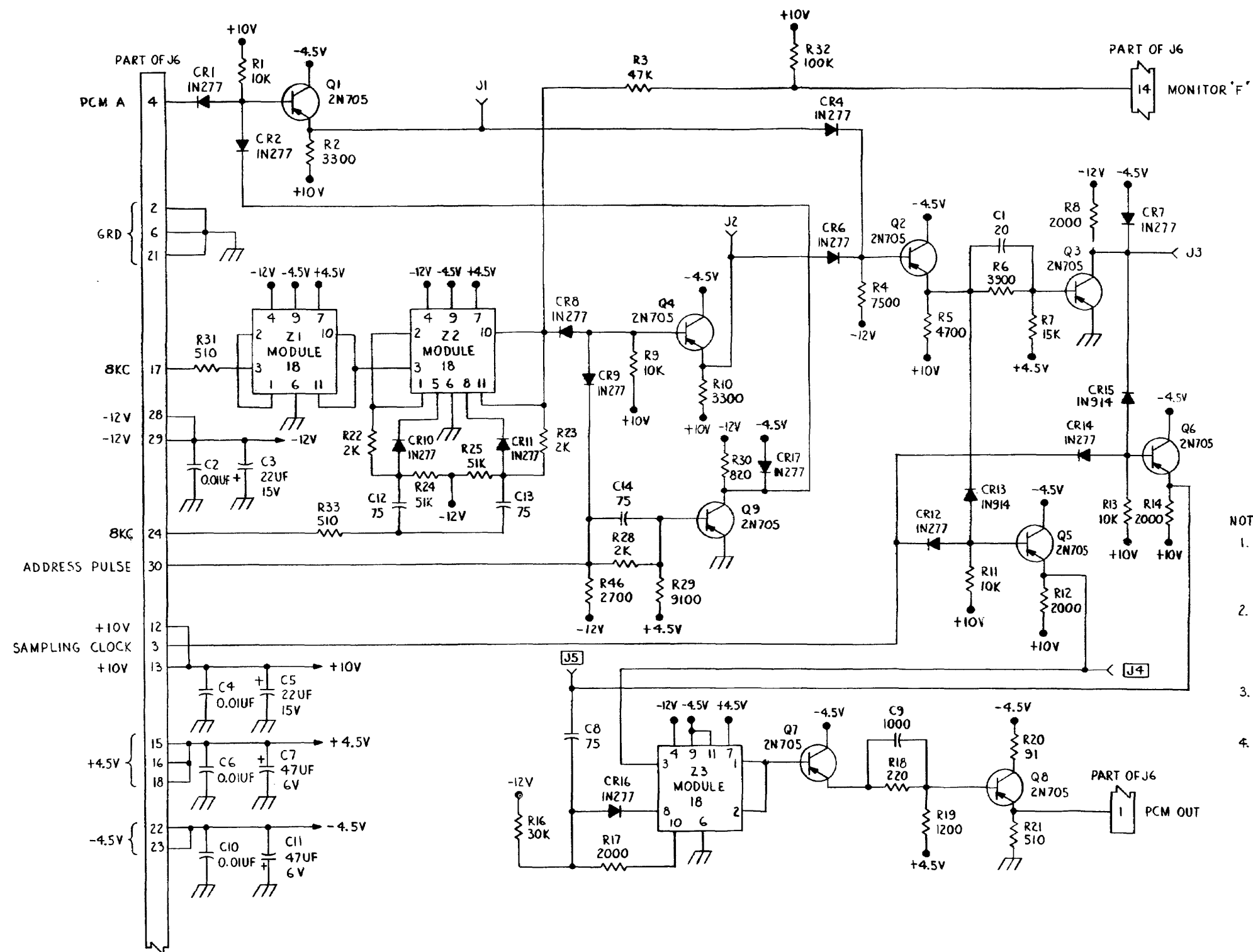


Figure 6-45.1 Panel 1A2A/2A2A, Schematic Diagram.



- CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS
1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
 2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
 3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
 4. ADDRESS SWITCH AT MASTER.
 5. AUX SWITCH AT OUT.
 6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.
- TM5805-367-35/3-46

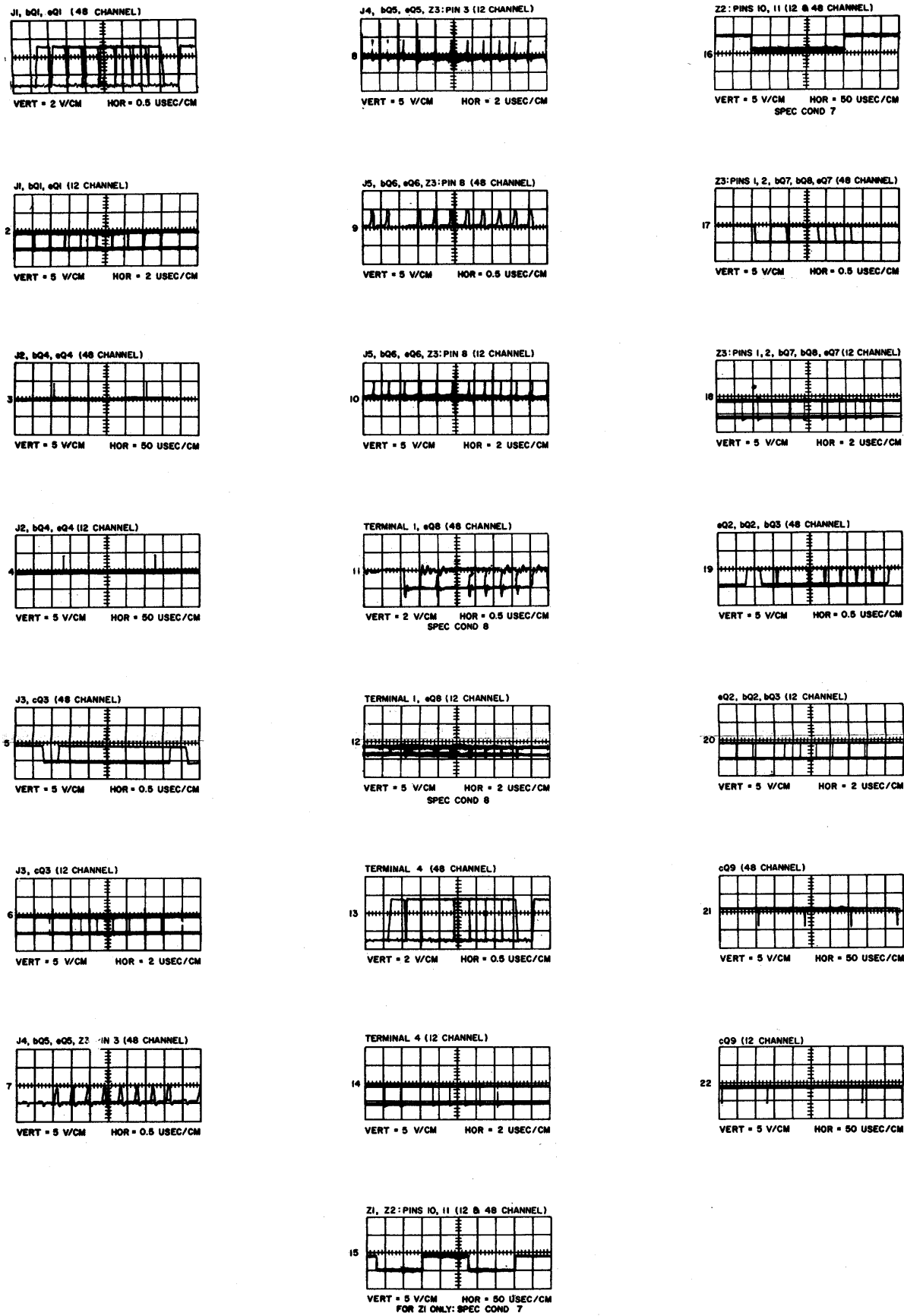
Figure 6-46. Panel 1A2/2A2, troubleshooting waveforms.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS.
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE $\frac{1}{4}$ WATT AND THEIR VALUE IS EXPRESSED IN OHMS.
 4. INDICATES EQUIPMENT MARKING.

Figure 6-47. Panel 1A3/2A3, schematic diagram
Change 3

EL2RC004



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATION

A. GENERAL.

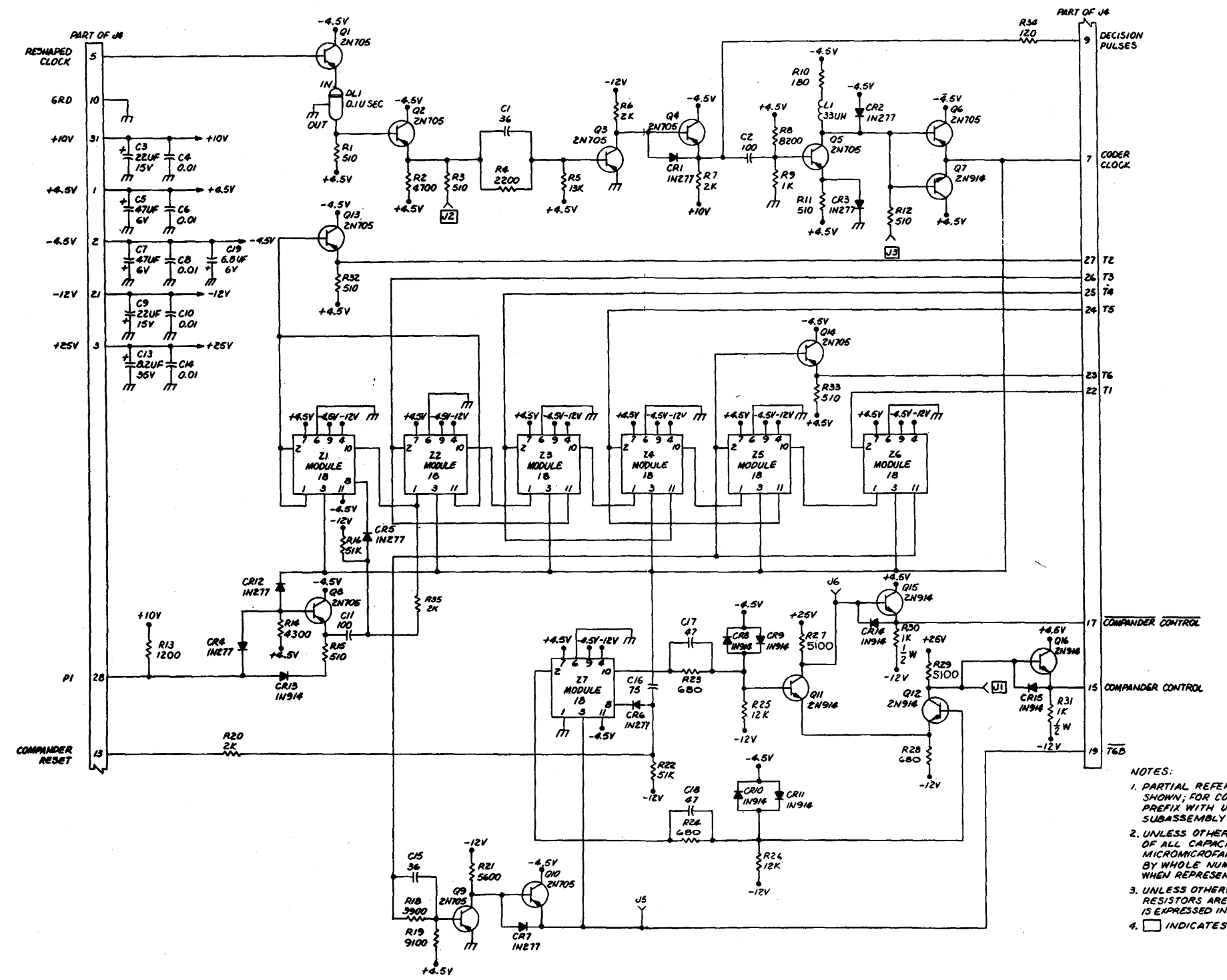
THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY REFERENCES GIVEN BENEATH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK SHOWN.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. TEST MULTIPLEXER ADDRESS SWITCH SET TO MASTER UNLESS INSTRUCTED OTHERWISE.
5. AUX SWITCH SET TO OUT.
6. 2 WIRE-4 WIRE SWITCH SET TO 4 WIRE..

B. SPECIAL

7. TEST MULTIPLEXER ADDRESS SWITCH SET TO SLAVE.
8. PCM OUTPUT TERMINATED IN 91-OHM LOAD..

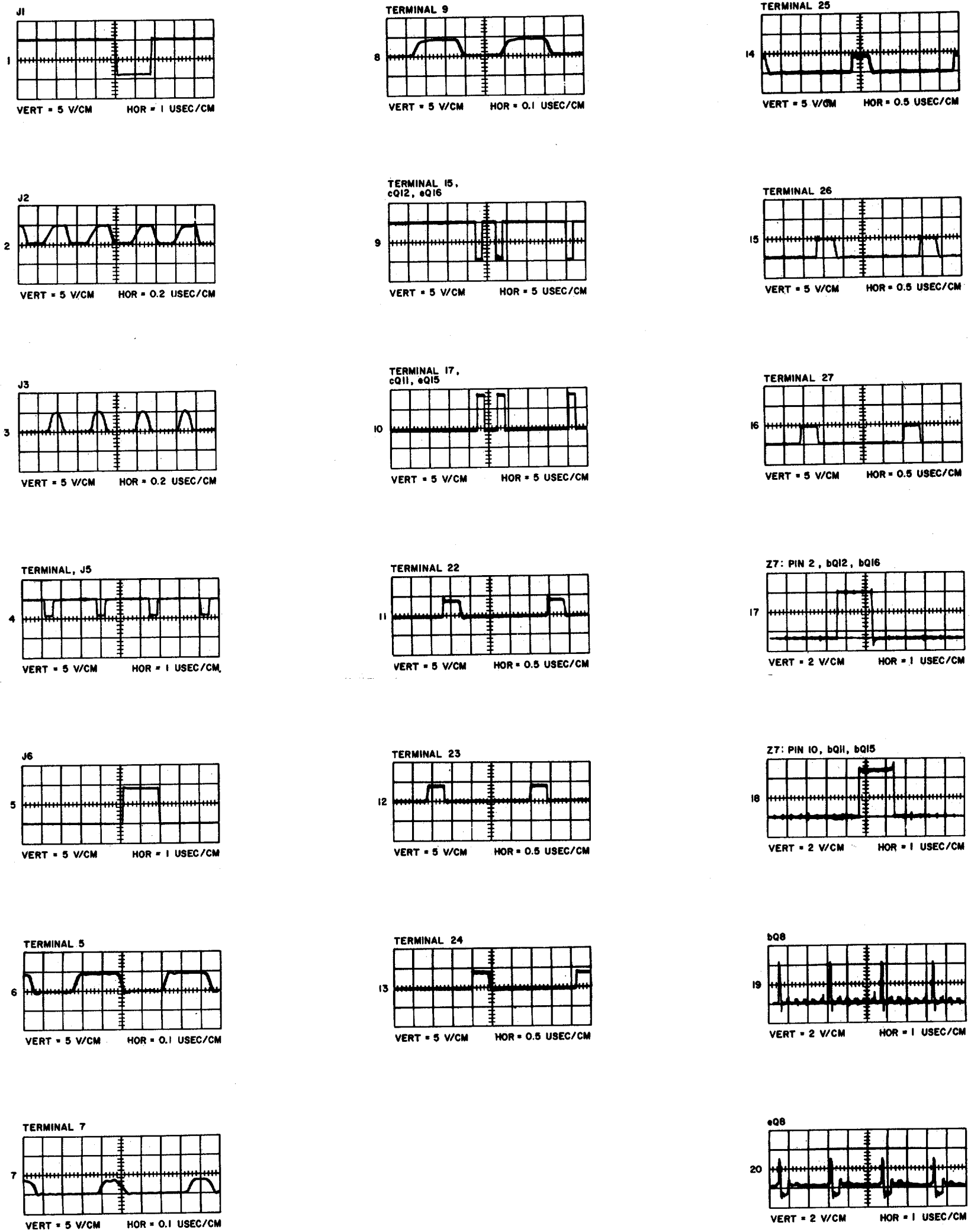
Figure 6-48. Panel 1A3/2A3, troubleshooting waveforms.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

TM5805-367-35/3-51

Figure 6-49. Panel 1A5, schematic diagram.



- CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS
1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK SHOWN.
 2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
 3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
 4. ADDRESS SWITCH AT MASTER
 5. AUX SWITCH SET TO OUT.
 6. 2 WIRE-4 WIRE SWITCH SET TO 4 WIRE.

Figure 6-50. Panel 1A5, troubleshooting waveforms.

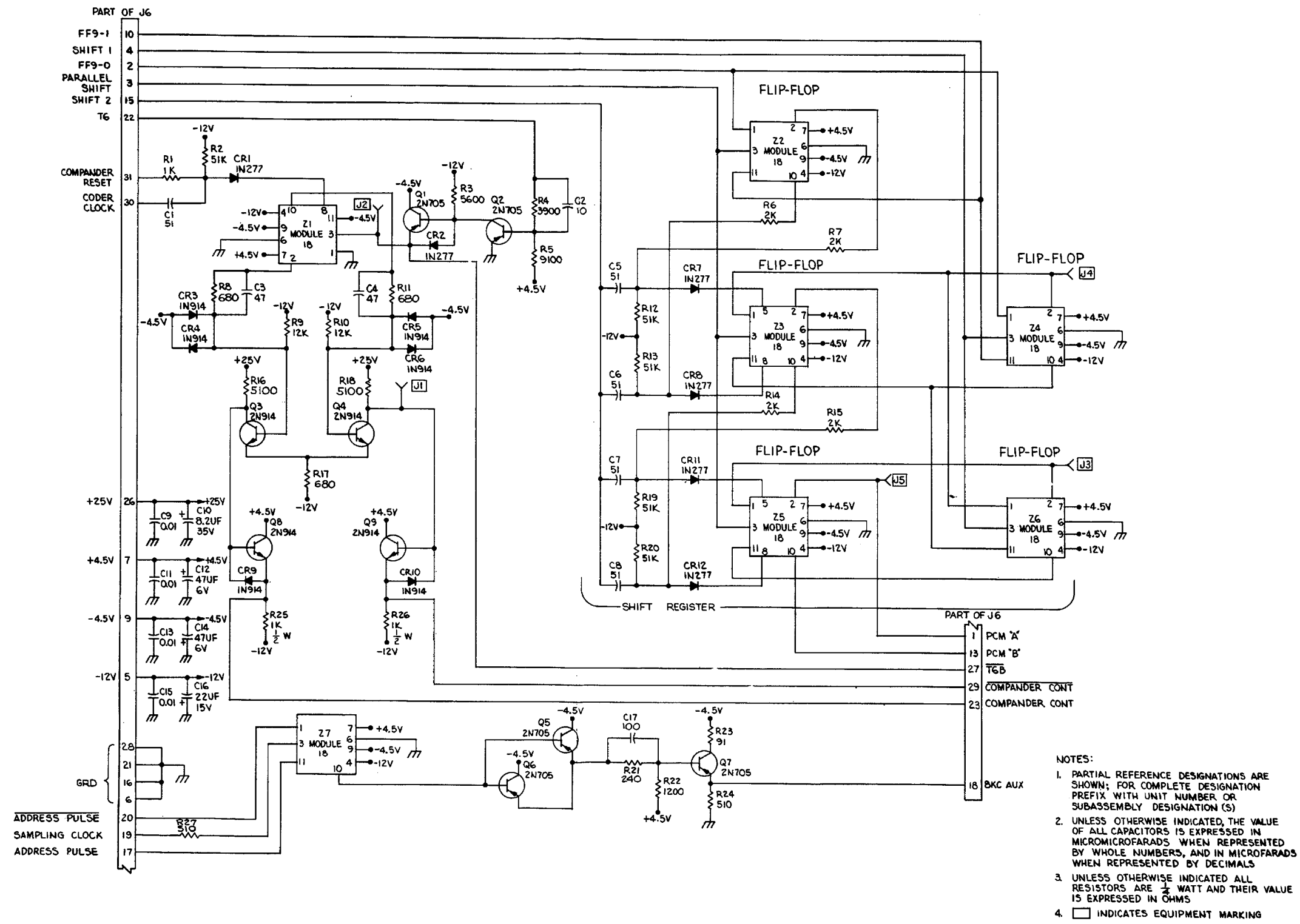
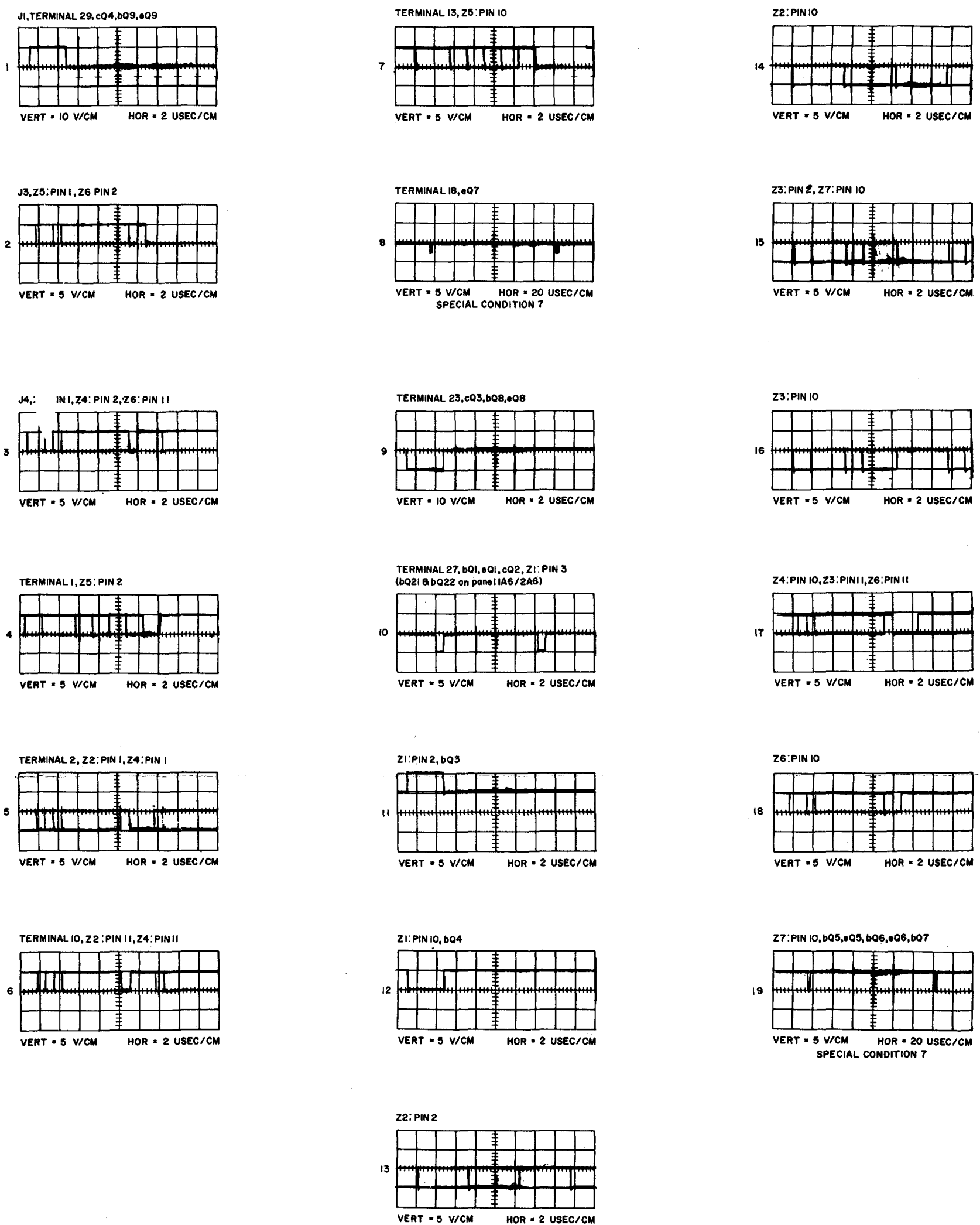


Figure 6-51. Panel 2A5, schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A GENERAL.

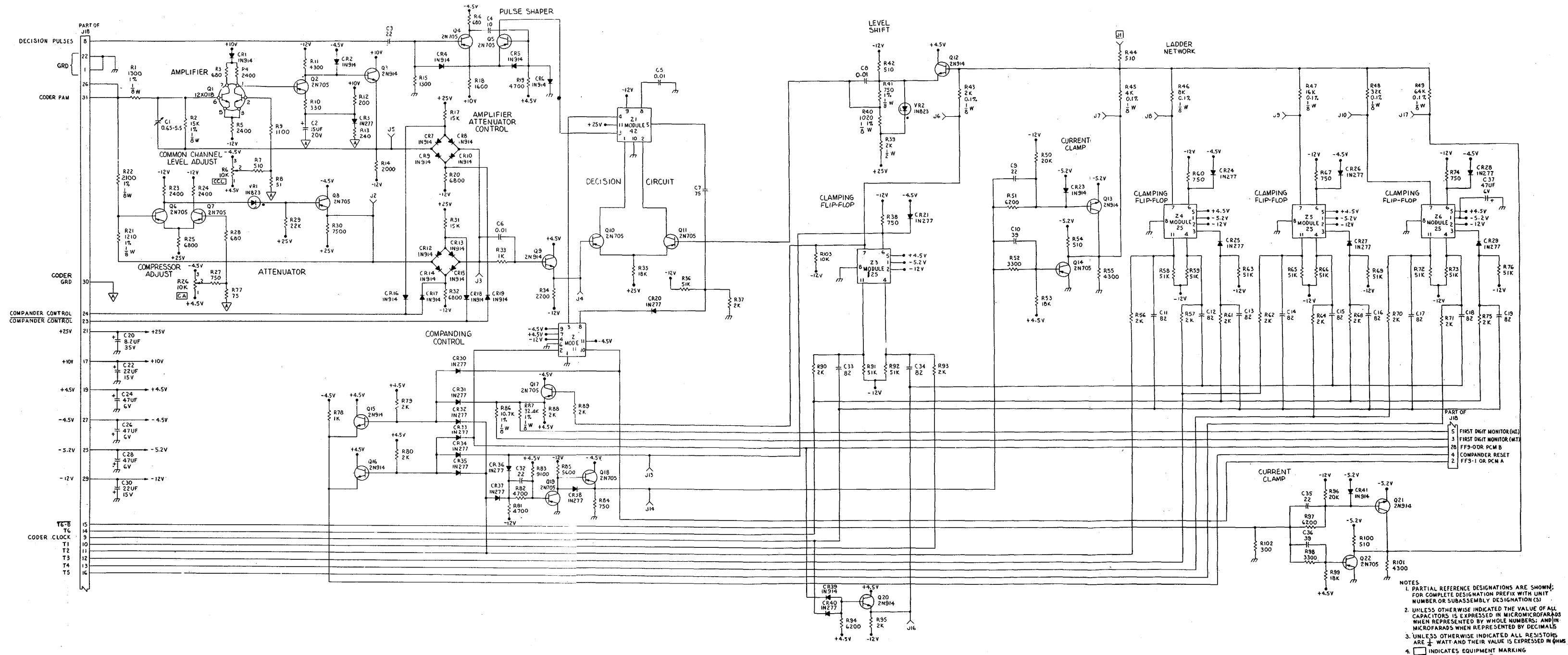
THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY REFERENCES WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK SHOWN.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH SET TO MASTER
5. AUX SWITCH SET TO OUT.
6. 2 WIRE-4 WIRE SWITCH SET TO 4 WIRE.

B SPECIAL

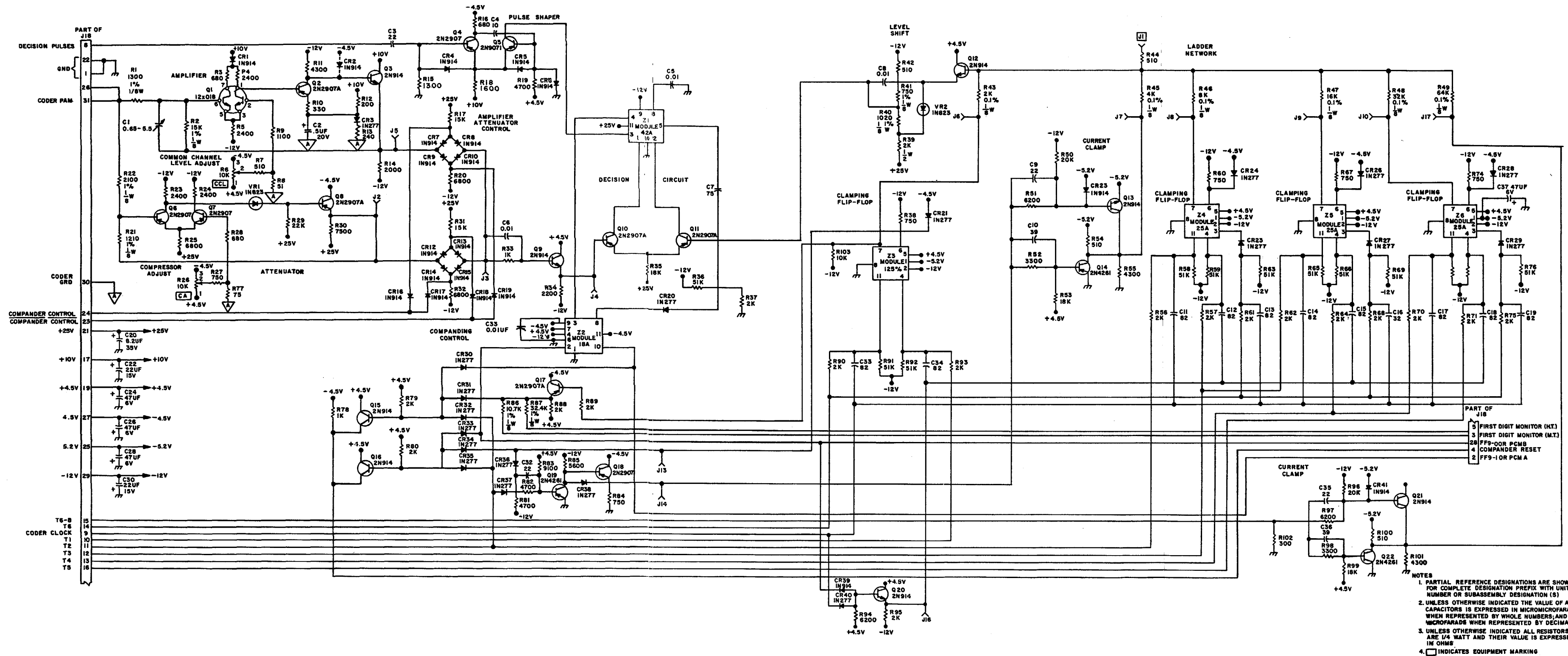
7. TERMINAL 18 TERMINATED IN 91-OHM LOAD.

Figure 6-52. Panel 2A5, troubleshooting waveforms.



NOTES
 1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS; AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

Figure 6-53. Panel 1A6/2A6, schematic diagram.



NOTES
 1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS; AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

Figure 6-53.1 Panel 1A6A/2A6A, schematic diagram

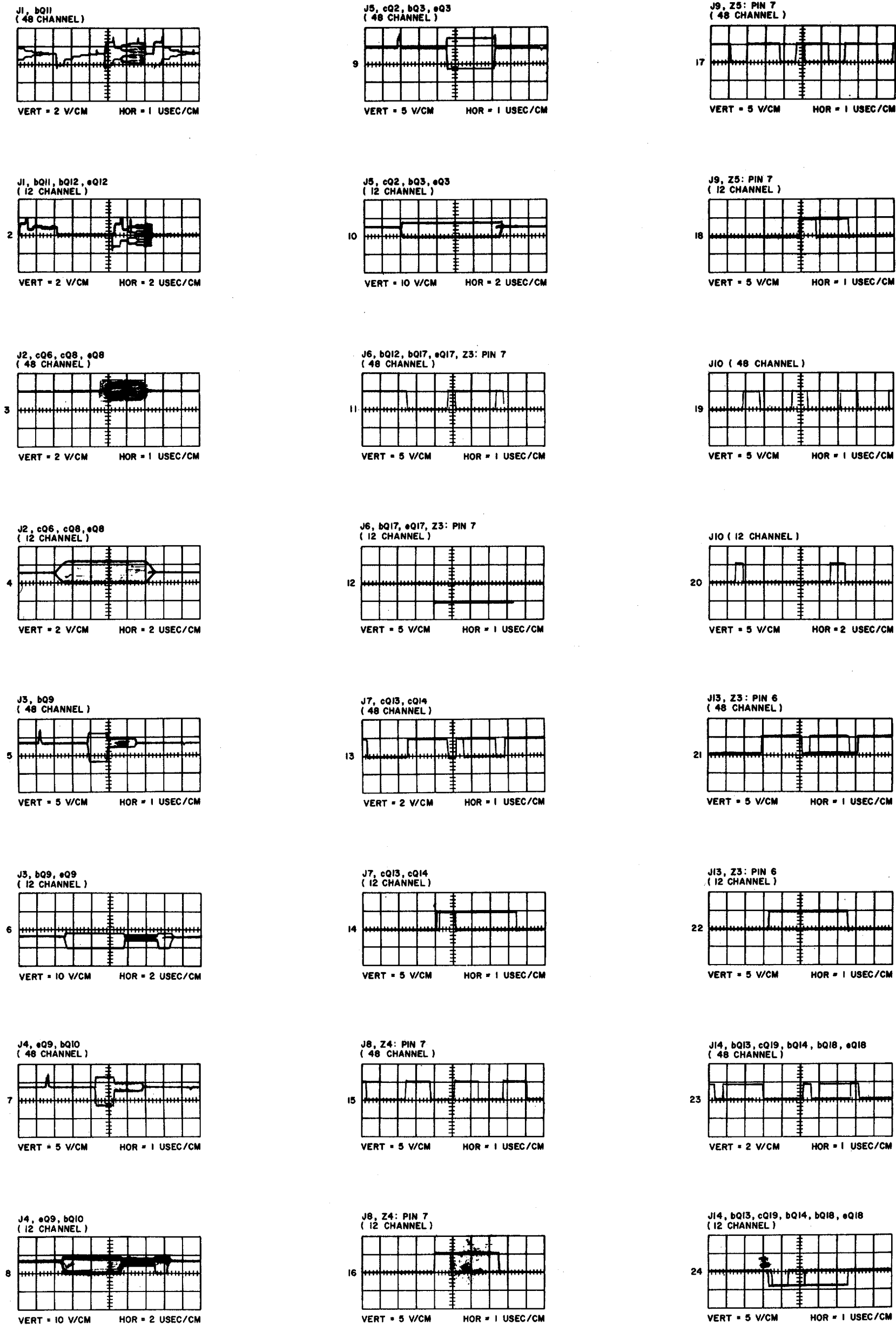


Figure 6-54①. Panel 1A6/2A6, troubleshooting waveforms (part 1 of 3).

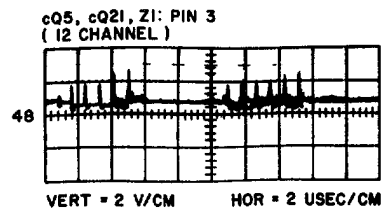
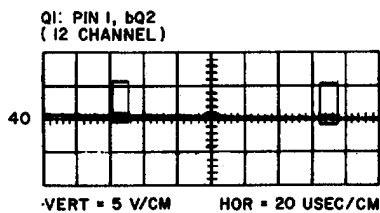
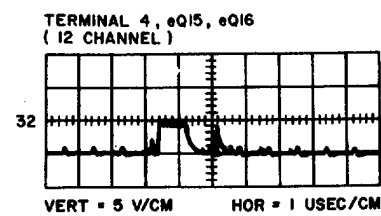
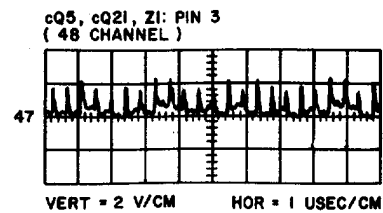
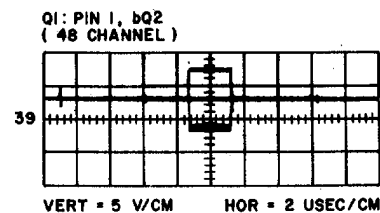
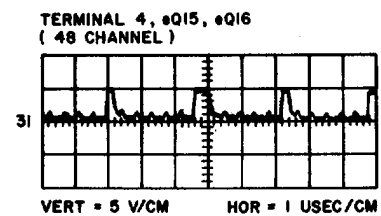
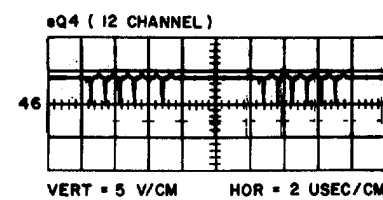
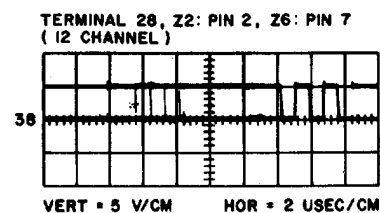
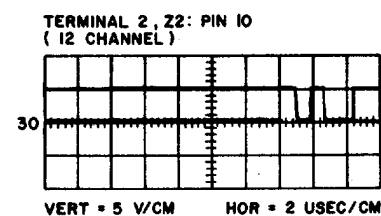
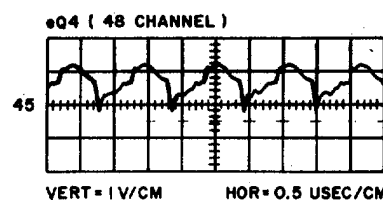
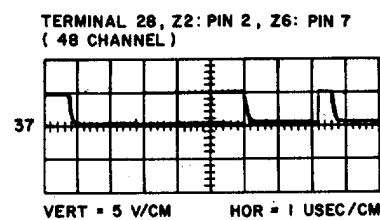
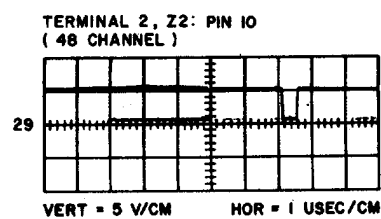
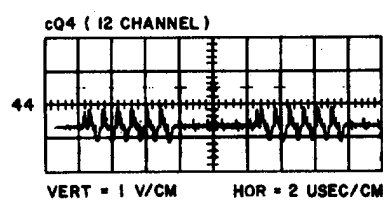
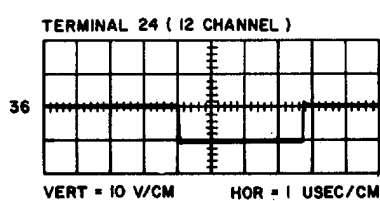
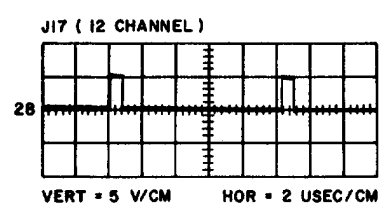
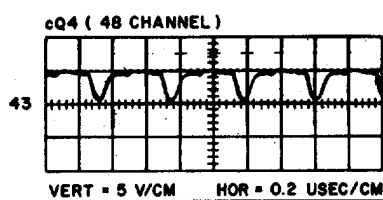
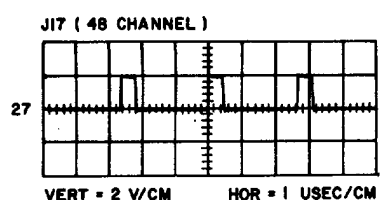
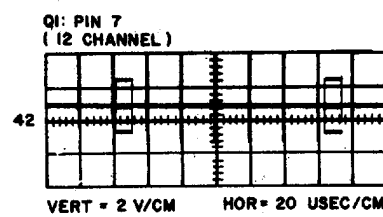
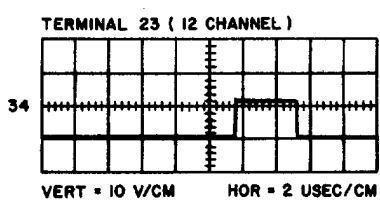
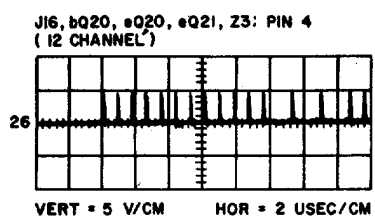
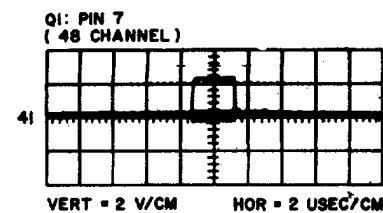
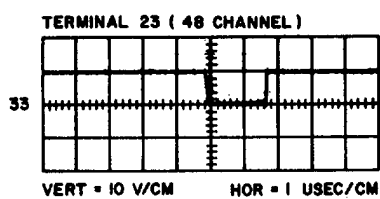
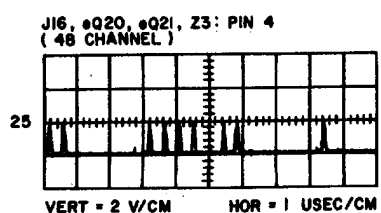
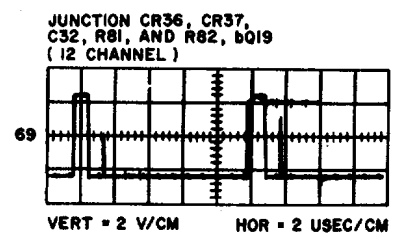
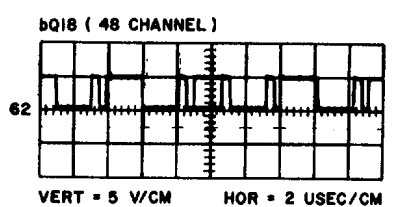
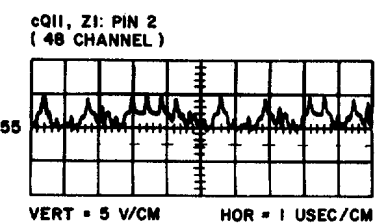
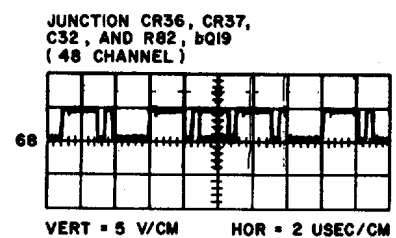
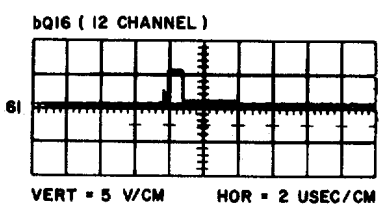
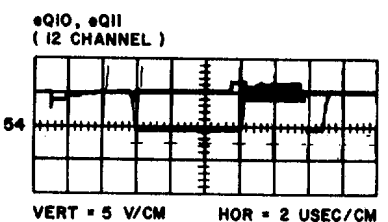
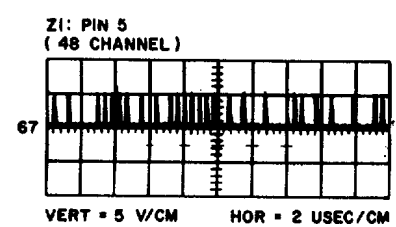
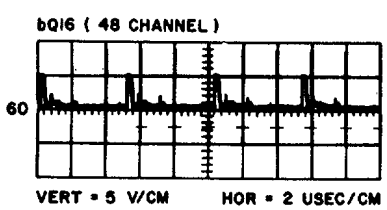
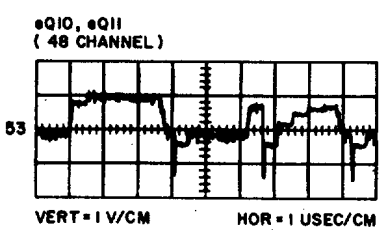
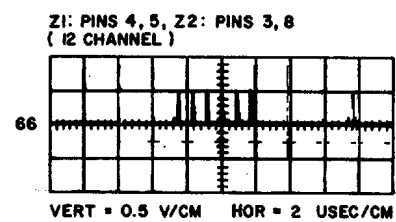
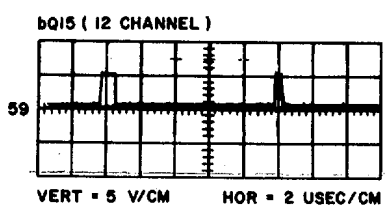
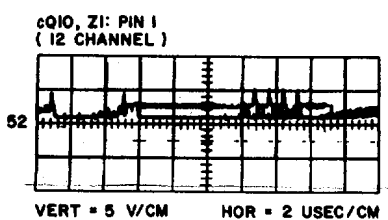
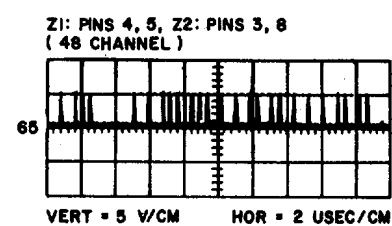
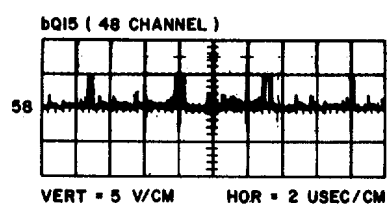
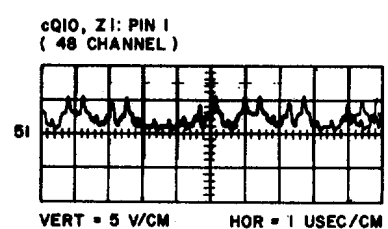
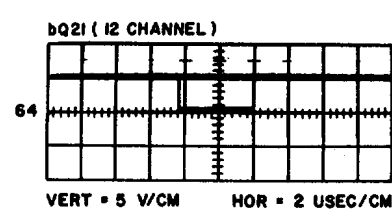
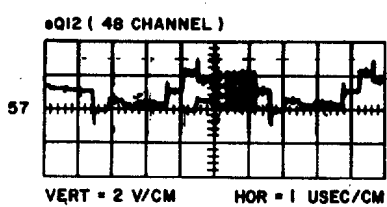
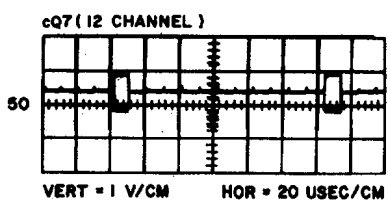
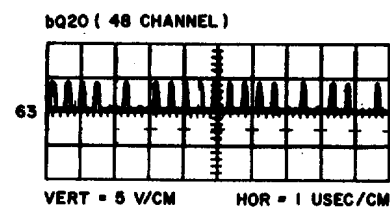
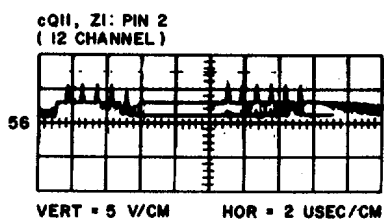
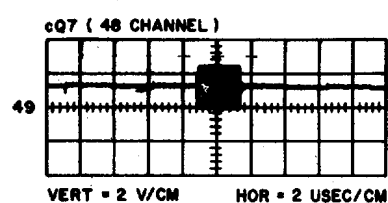


Figure 6-54②. Panel 1A6/2A6, troubleshooting waveforms (part 2 of 3).



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

Figure 6-54³. Panel 1A6/2A6, troubleshooting waveforms (part 3 of 3).

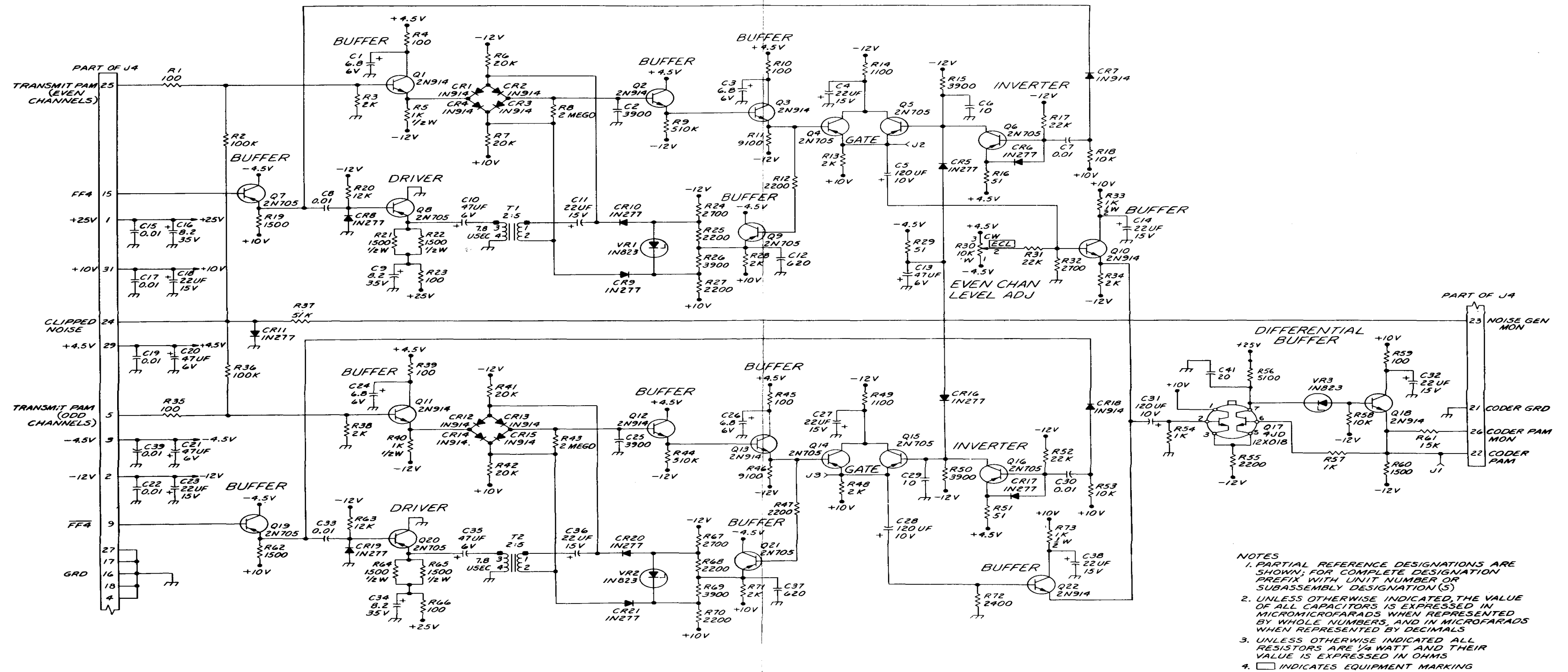
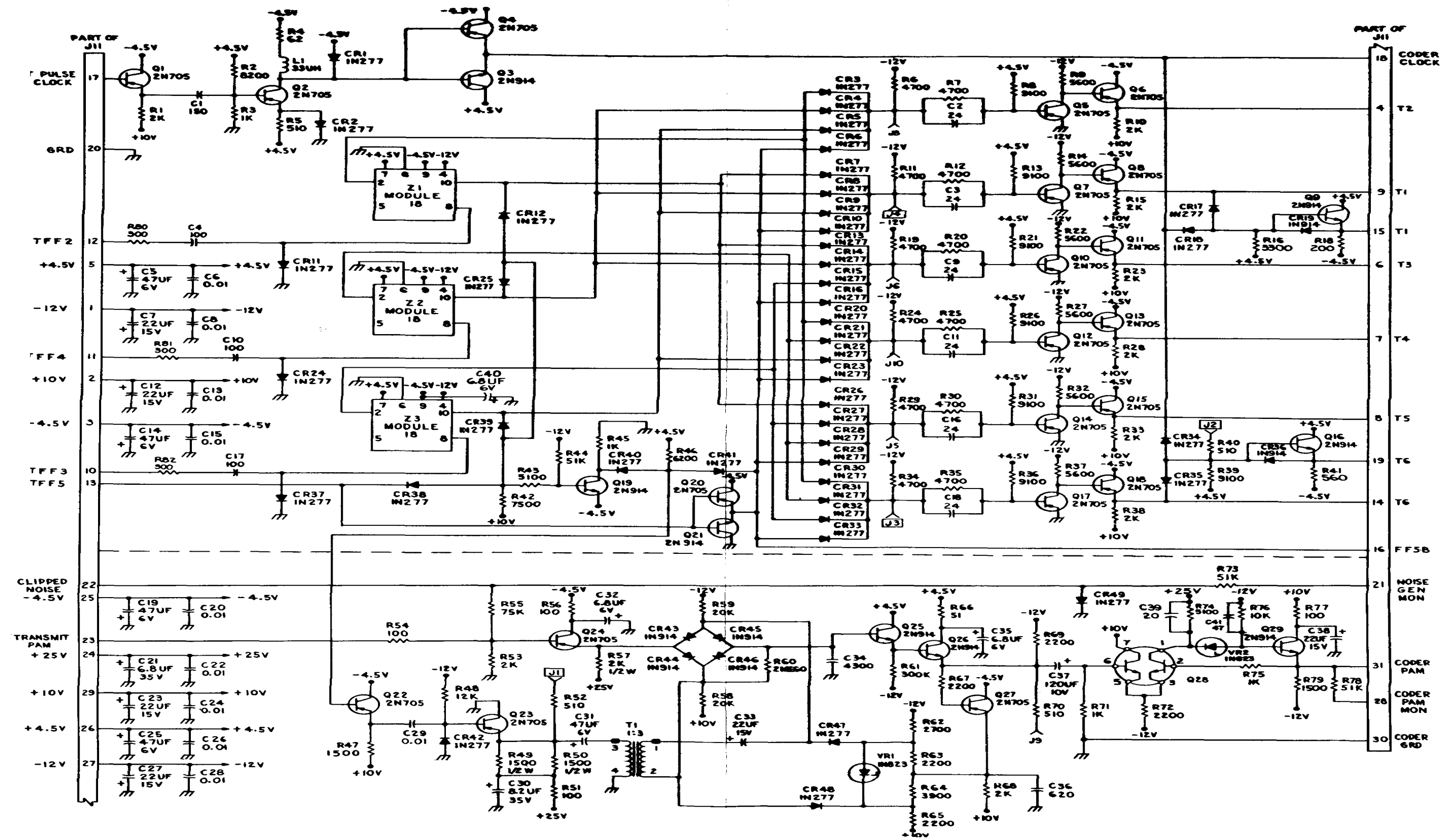
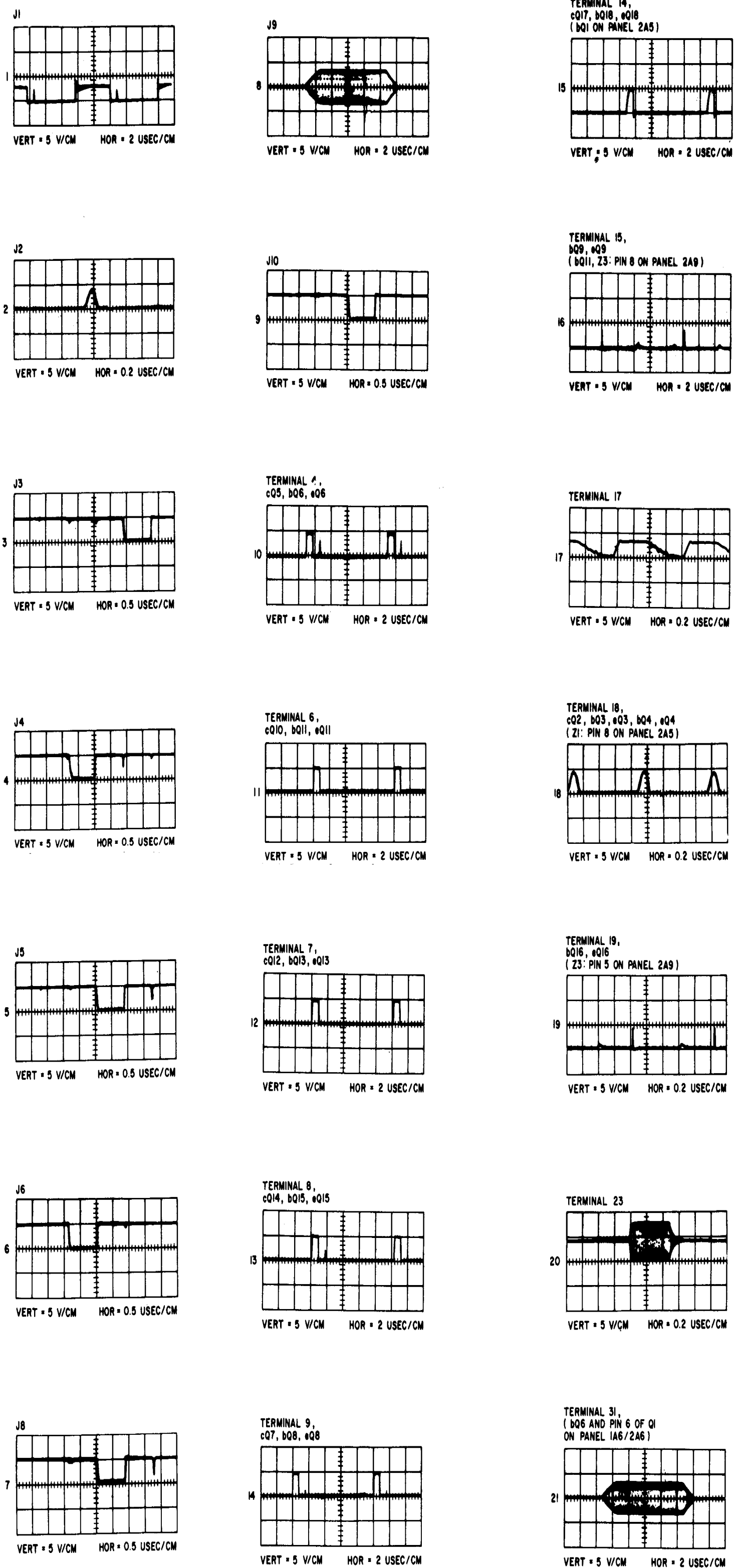


Figure 6-55. Panel 1A7, schematic diagram.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTOR VALUES ARE $\frac{1}{2}$ WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING
 5. LOWER PORTION OF BOARD HAS OWN POWER LEADS

Figure 6-56. Panel 2A7, schematic diagram.

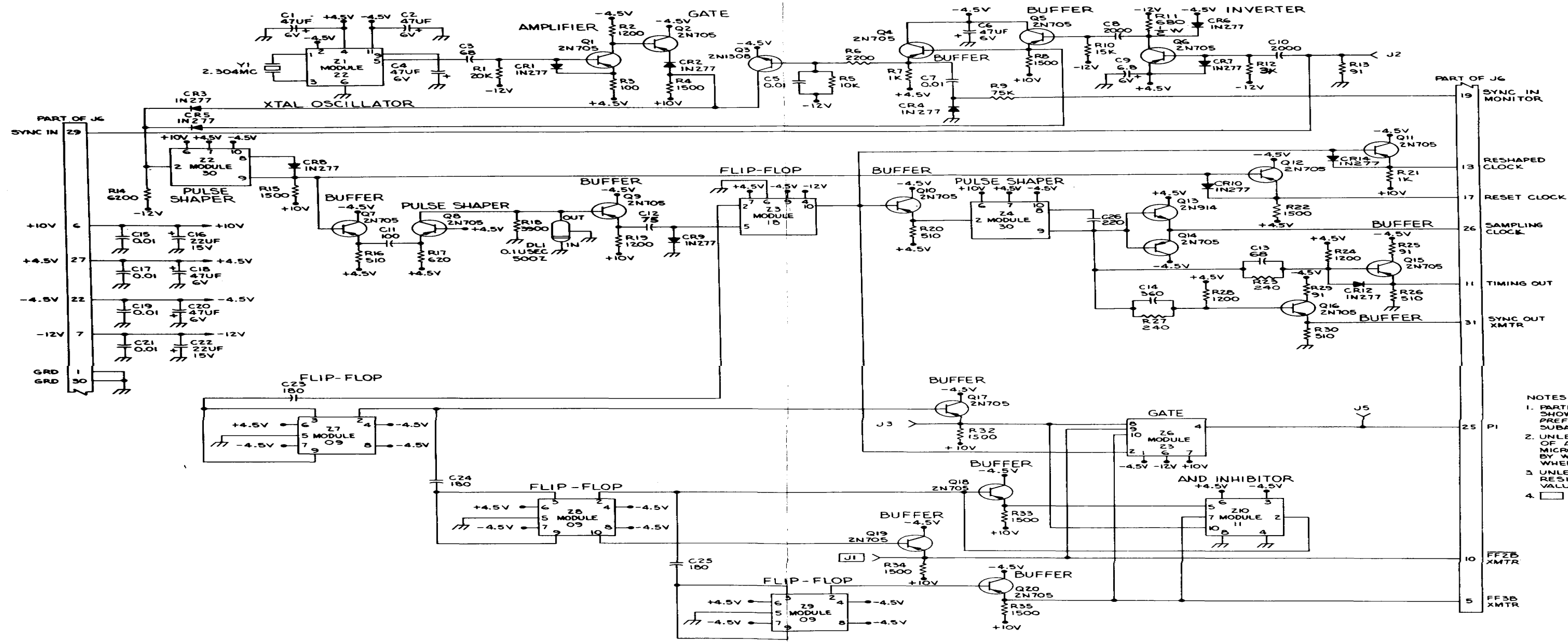


CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

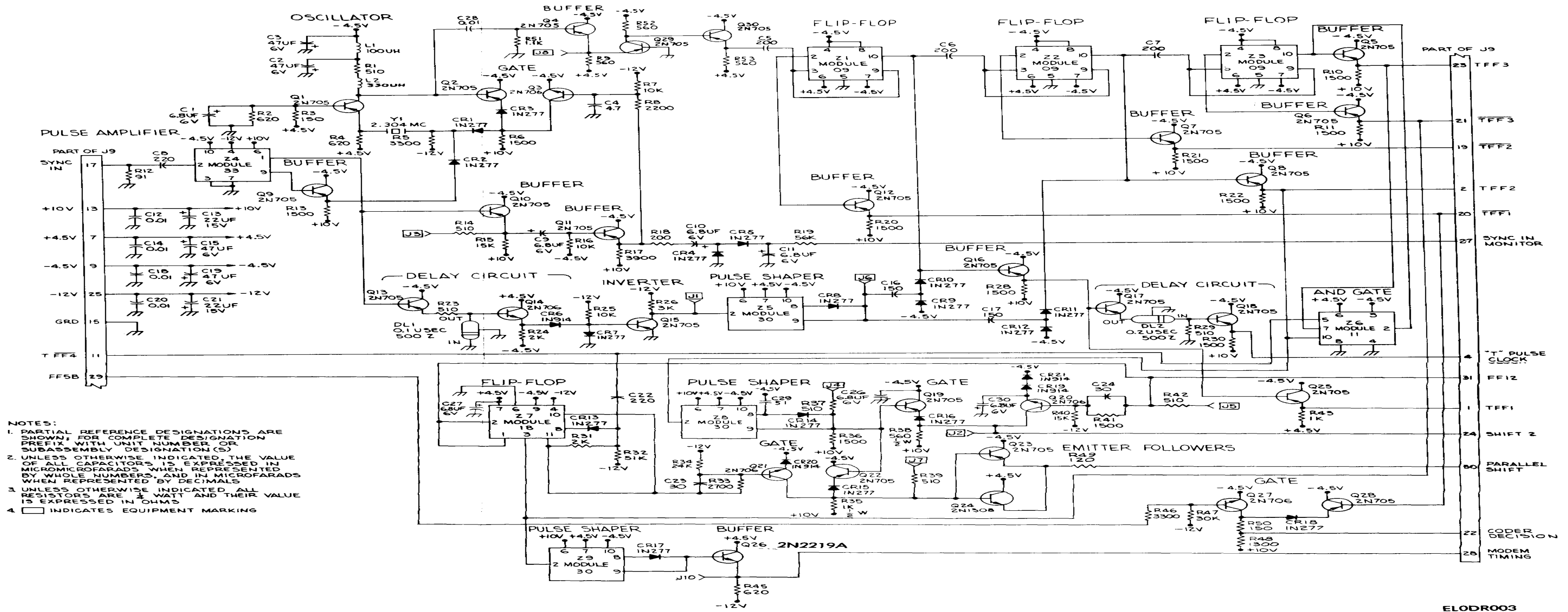
TM 11-5805-367-35/3-64

Figure 6-57. Panel 2A7, troubleshooting waveforms.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING

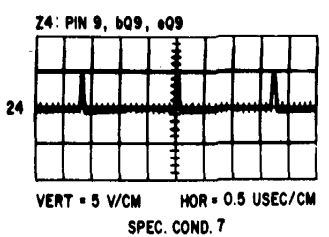
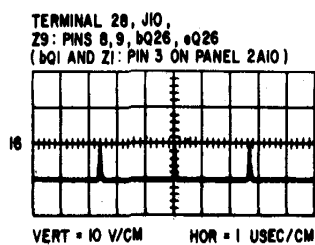
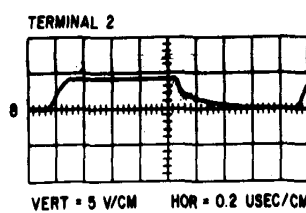
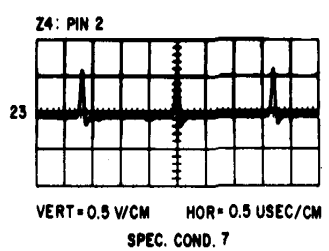
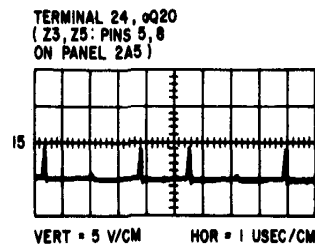
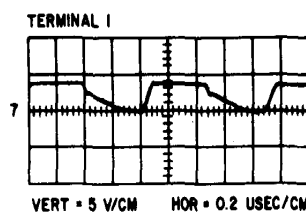
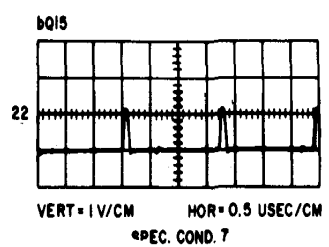
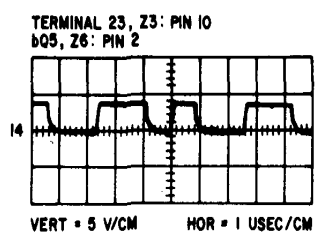
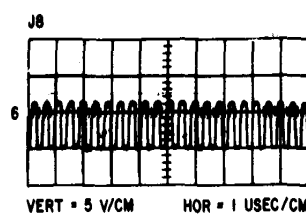
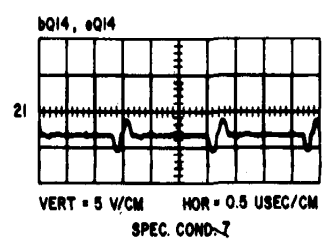
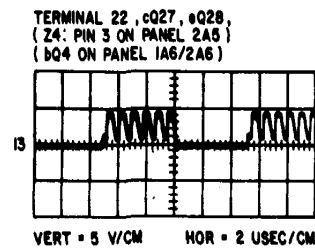
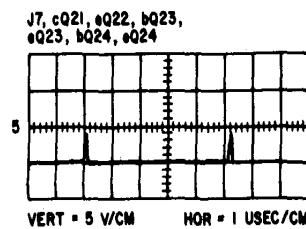
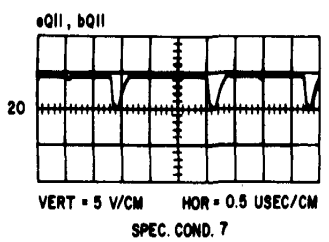
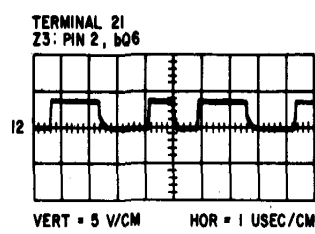
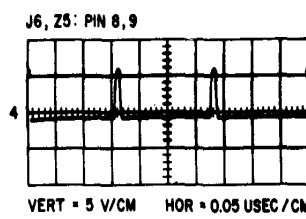
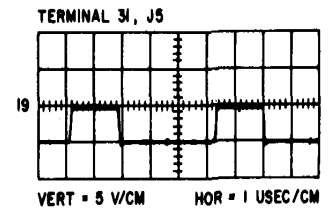
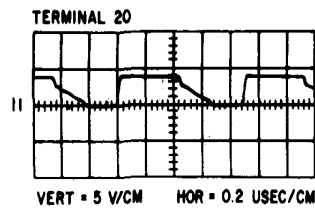
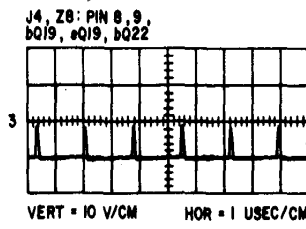
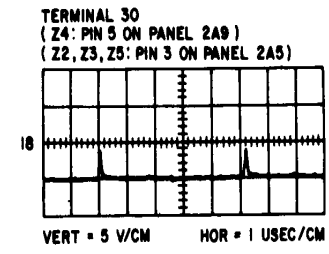
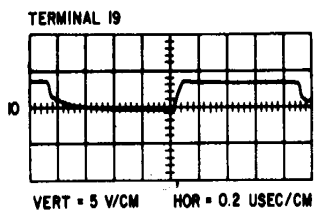
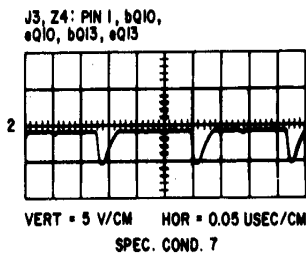
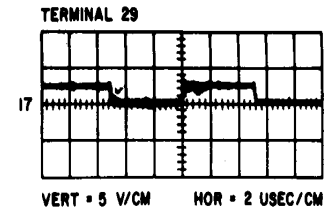
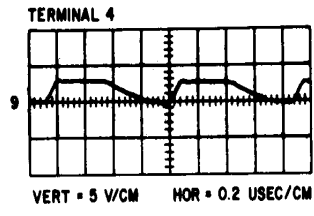
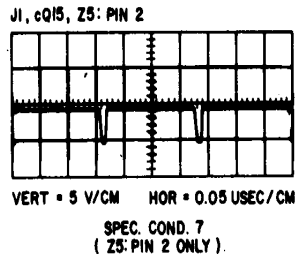
Figure 6-58. Panel 1A8, schematic diagram.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE 1/2 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

ELODR003

Figure 6-59. Panel 2A8, schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

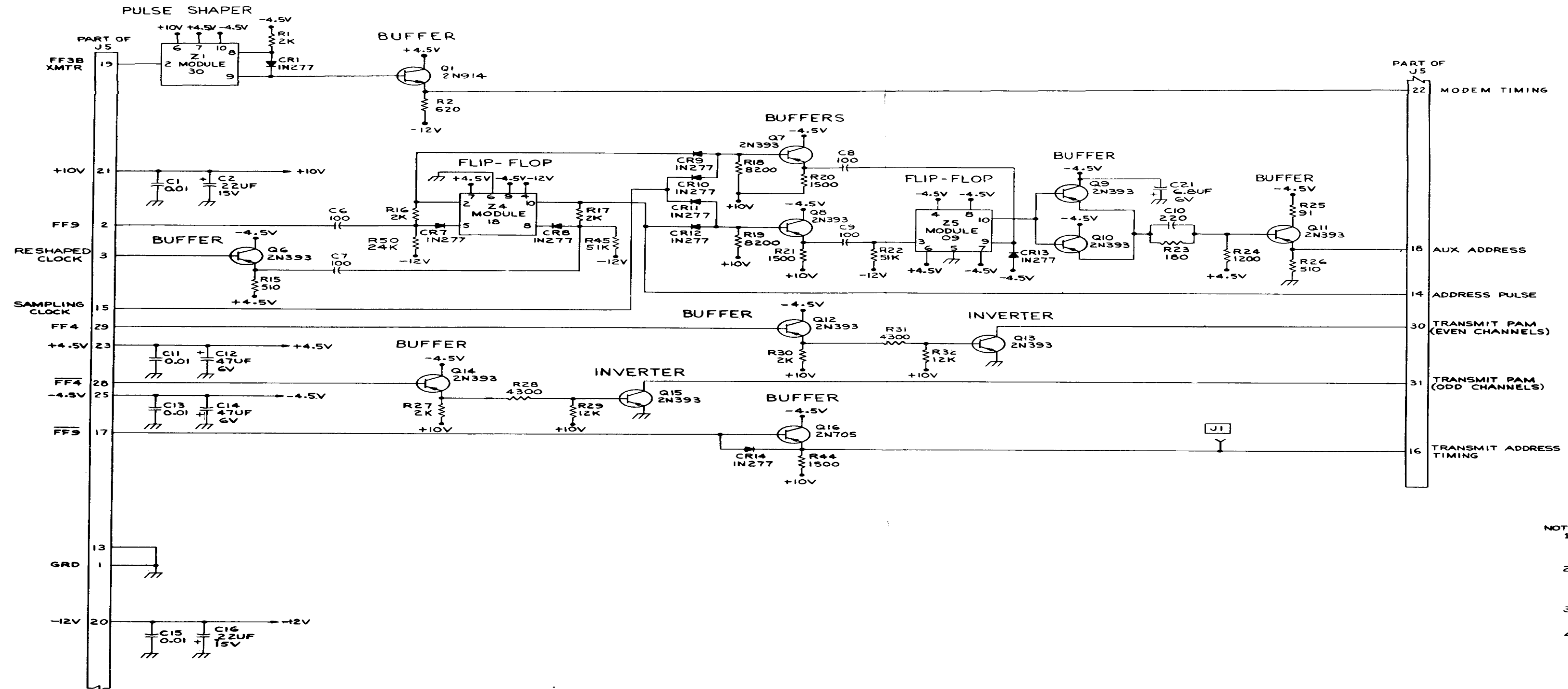
1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

B. SPECIAL.

7. CHECKED WITH SYNC IN INPUT OF TEST MULTIPLEXER OBTAINED FROM SYNC OUT XMTR OUTPUT OF SECOND TEST MULTIPLEXER. OSCILLOSCOPE SYNCHRONIZED FROM SYNC OUT CONNECTOR OF SECOND TEST MULTIPLEXER.

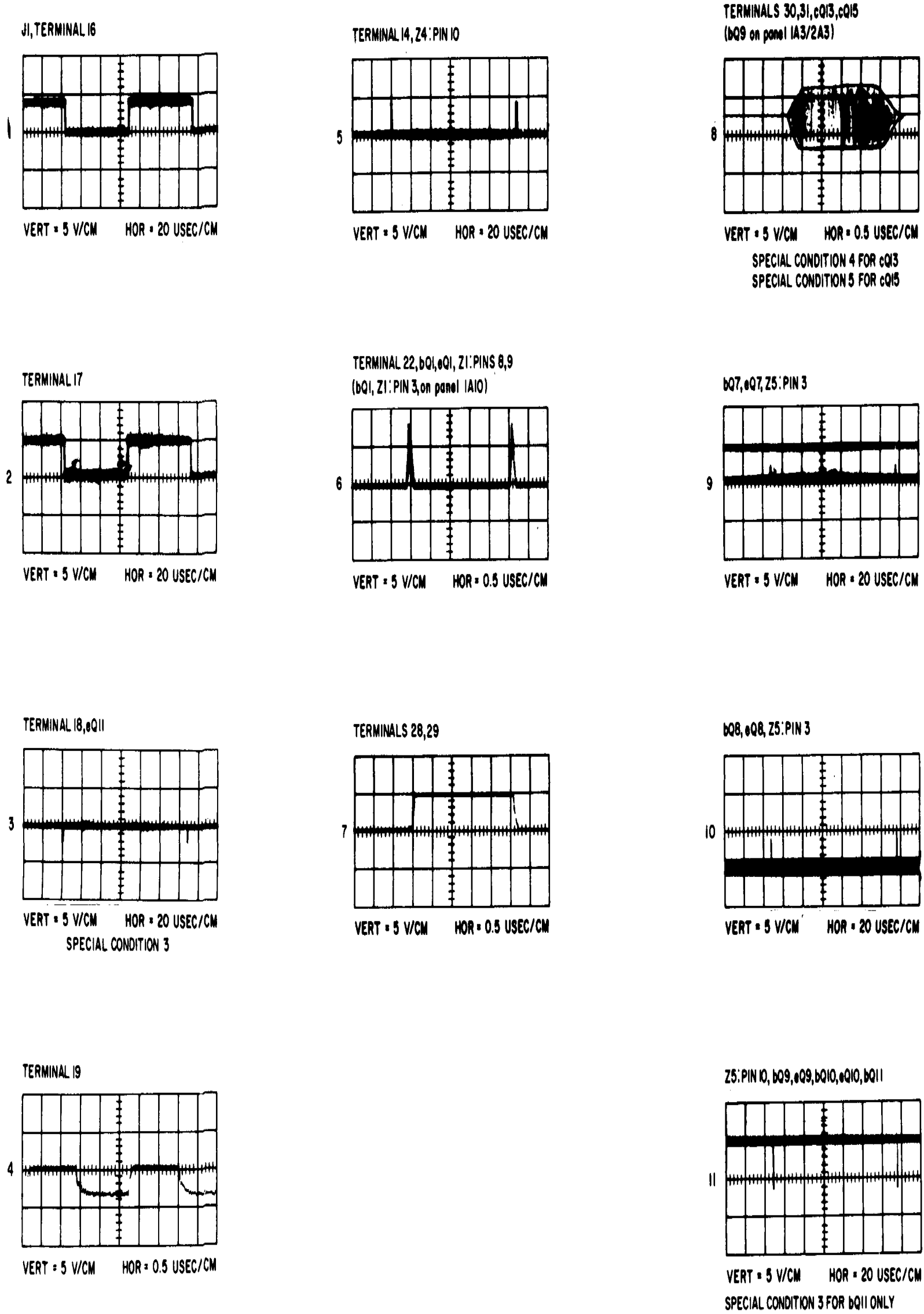
TN 5008-367-36/3-71

Figure 6-60. Panel 2A8, troubleshooting waveforms.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUB-ASSEMBLY DESIGNATION(S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THE VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

Figure 6-61. Panel 1A9, schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.

B. SPECIAL.

3. TERMINAL 18 TERMINATED IN 91-OHM LOAD.
4. MODULATE ONE EVEN CHANNEL.
5. MODULATE ONE ODD CHANNEL.

TM5805-367-35/3-74

Figure 6-62. Panel 1A9, troubleshooting waveforms.

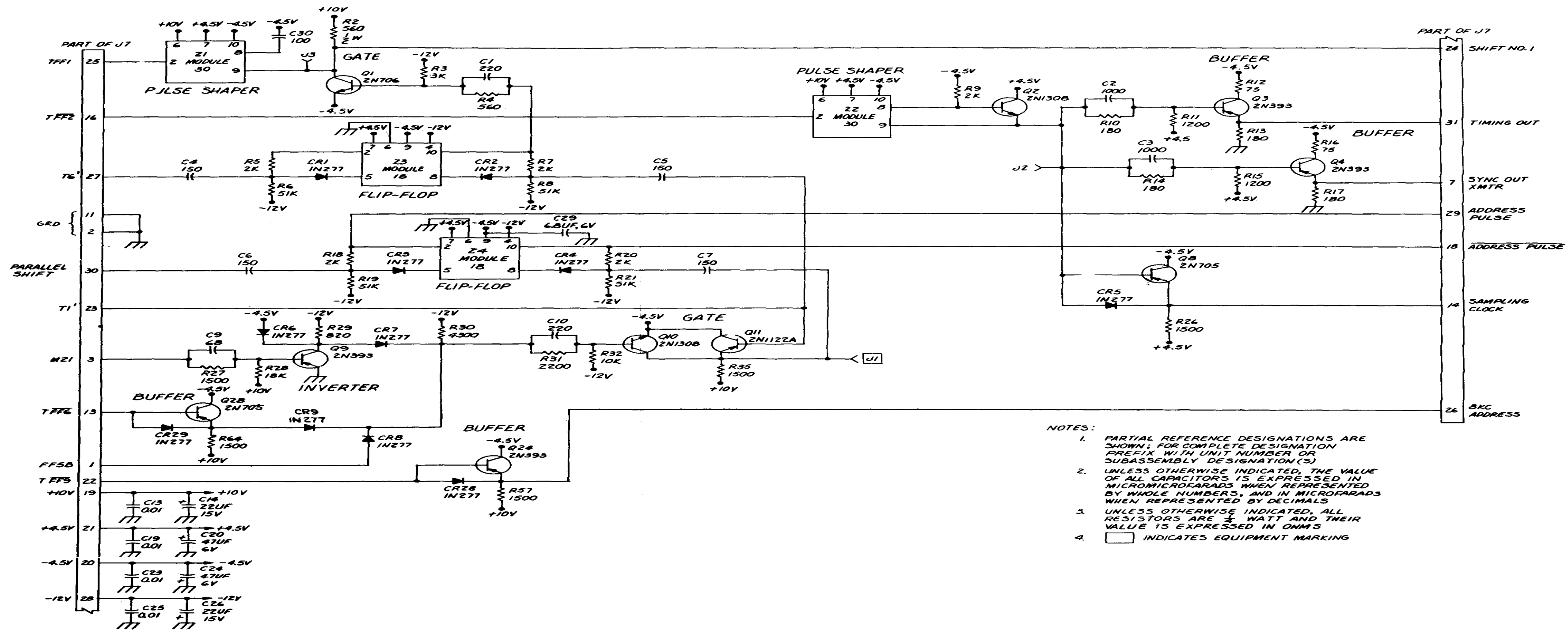
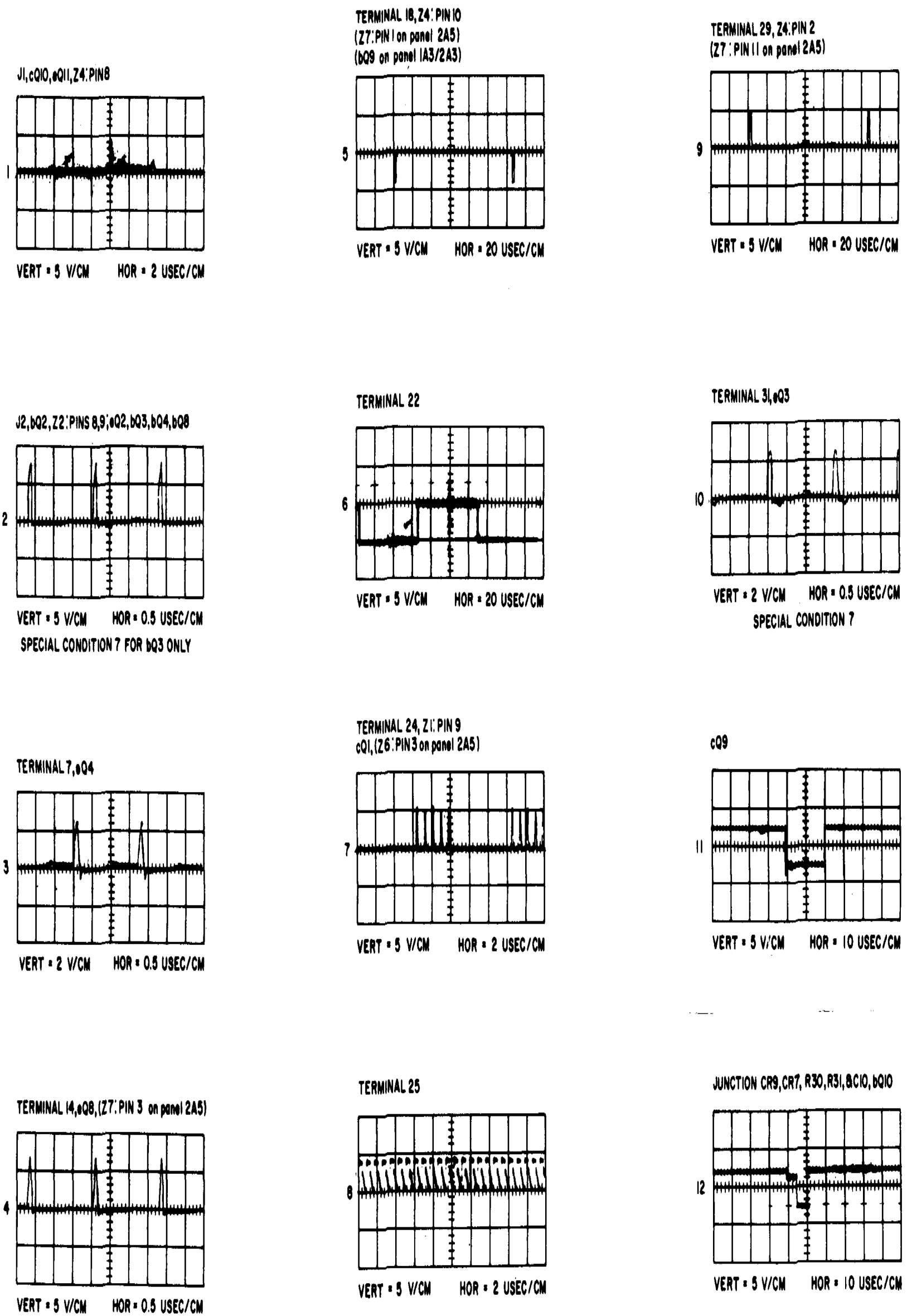


Figure 6-63. Panel 2A9, schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

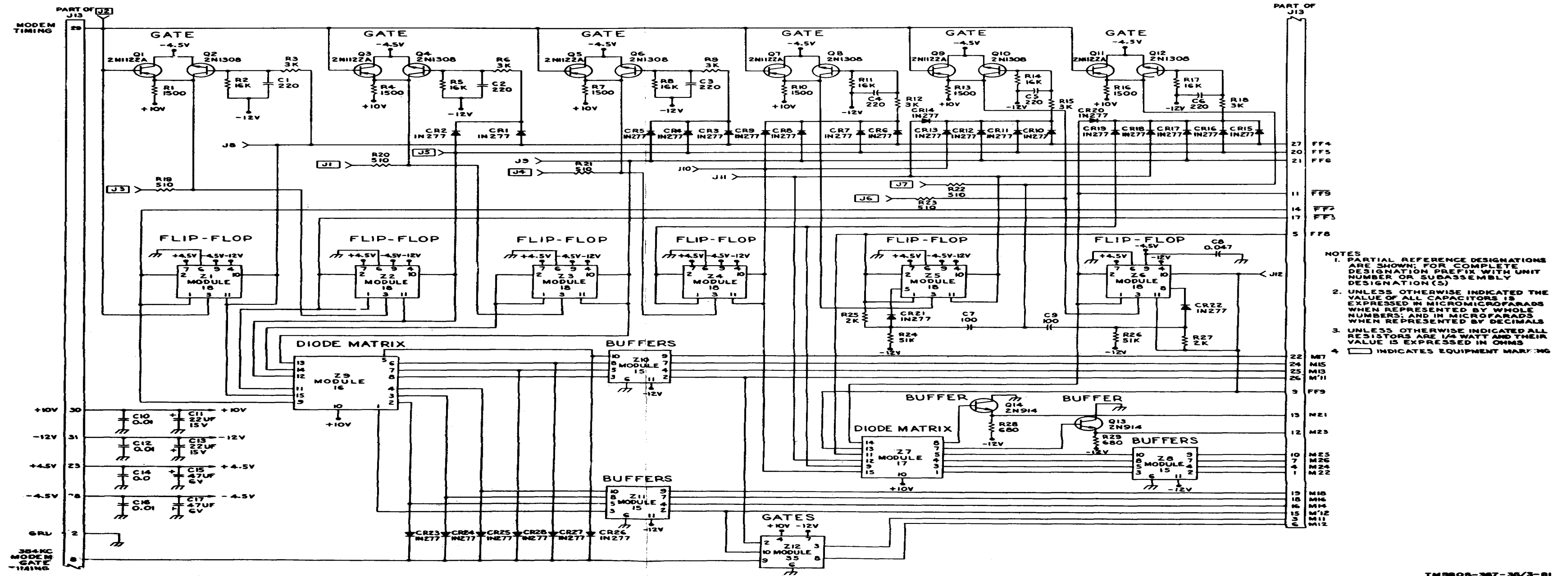
1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

B. SPECIAL.

7. TERMINAL 31 TERMINATED IN 91-OHM LOAD.

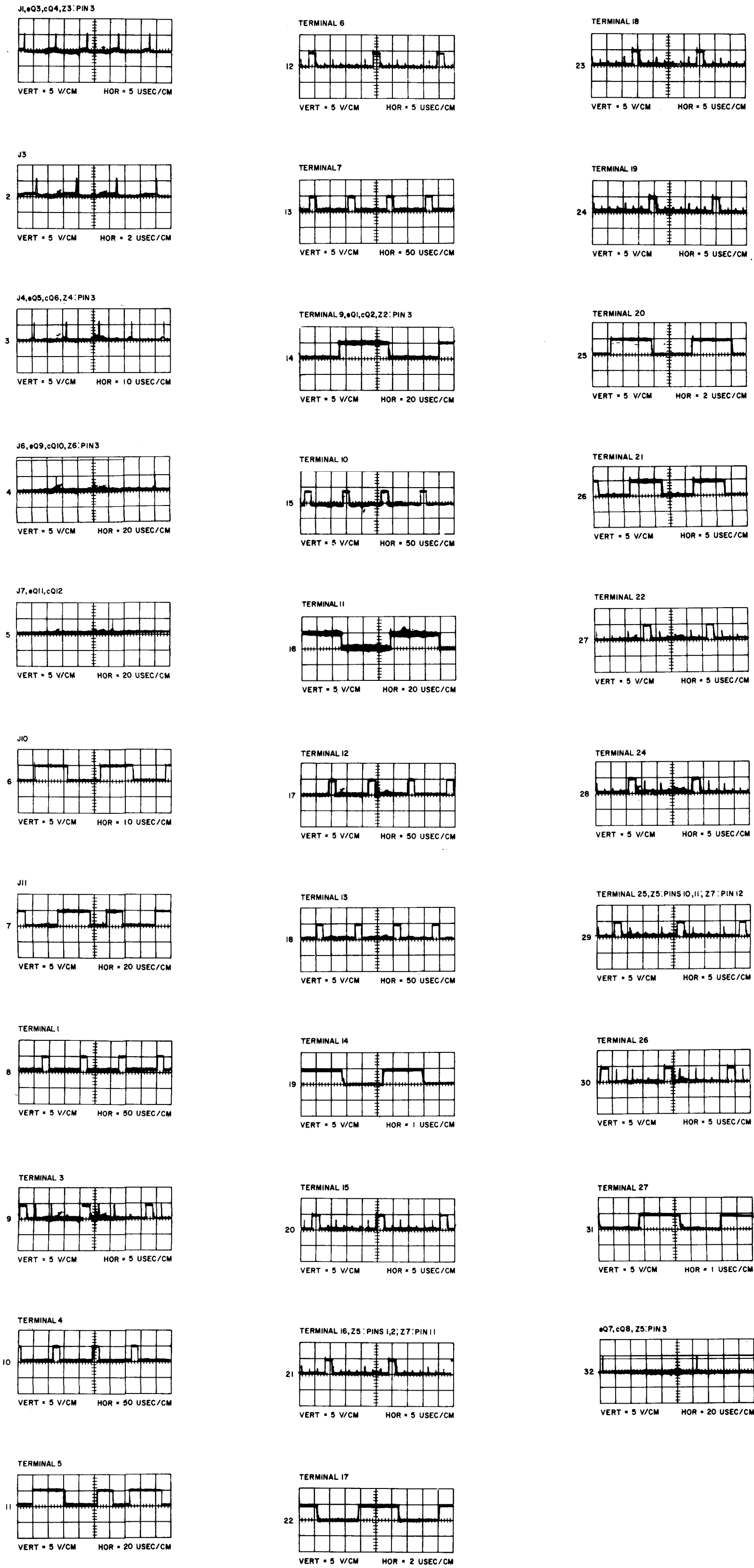
TM 11-5805-367-35/3-79

Figure 6-64. Panel 2A9, troubleshooting waveforms.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS; AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING

Figure 6-65. Panel 1A10, schematic diagram.

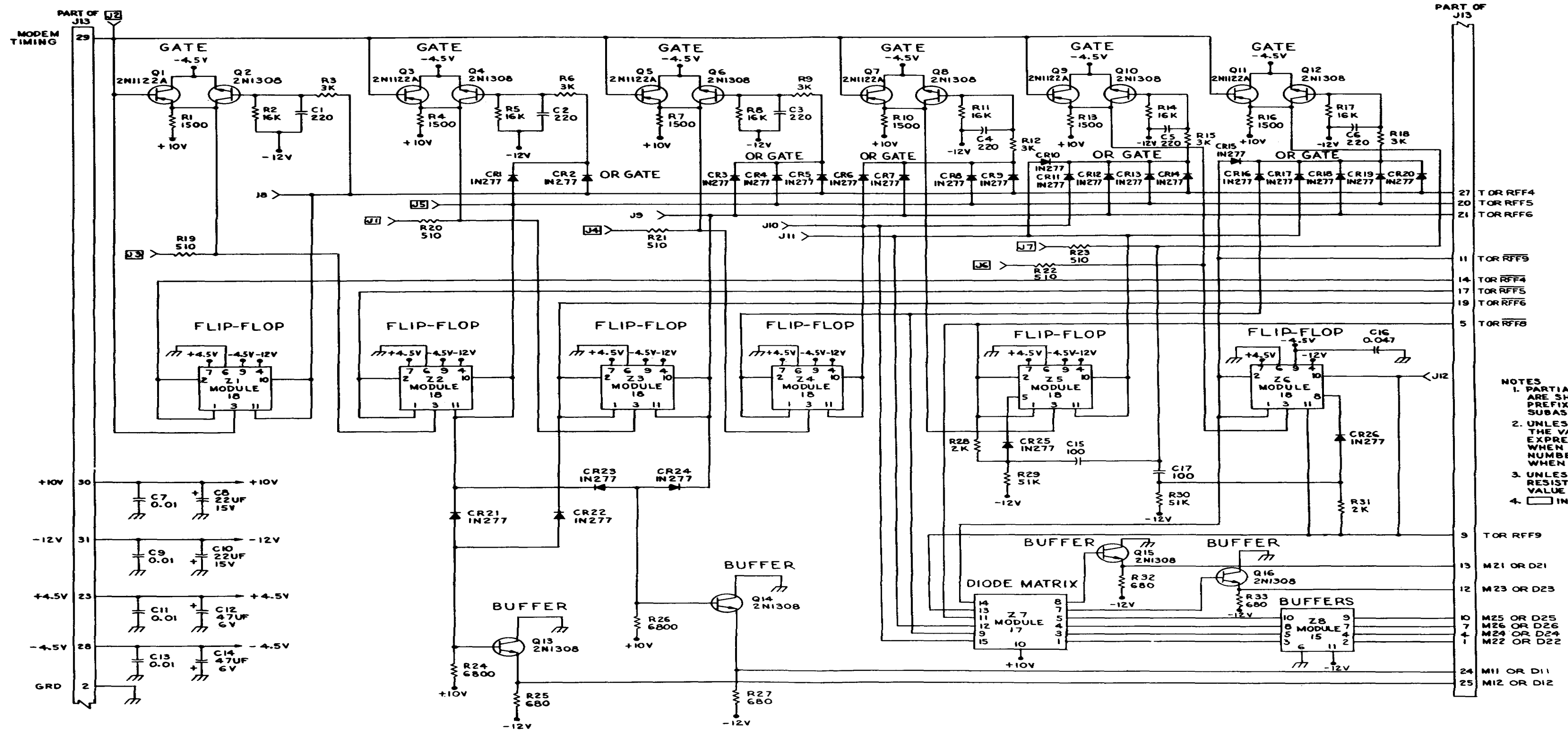


CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

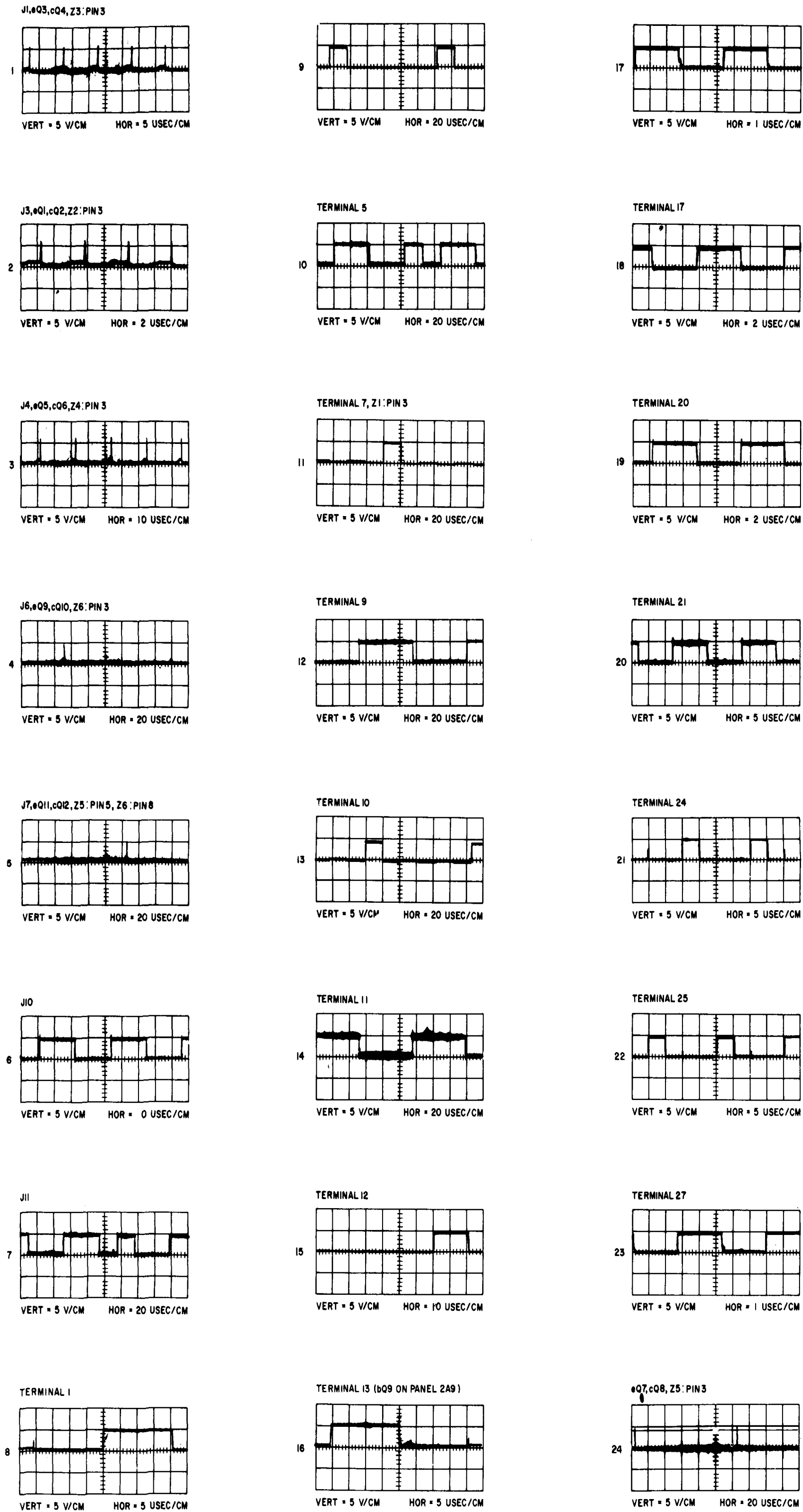
TM 5805-367-35/3-82

Figure 6-66. Panel 2A10, troubleshooting waveforms.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS; AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/2 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING

Figure 6-67. Panel 2A10, schematic diagram.

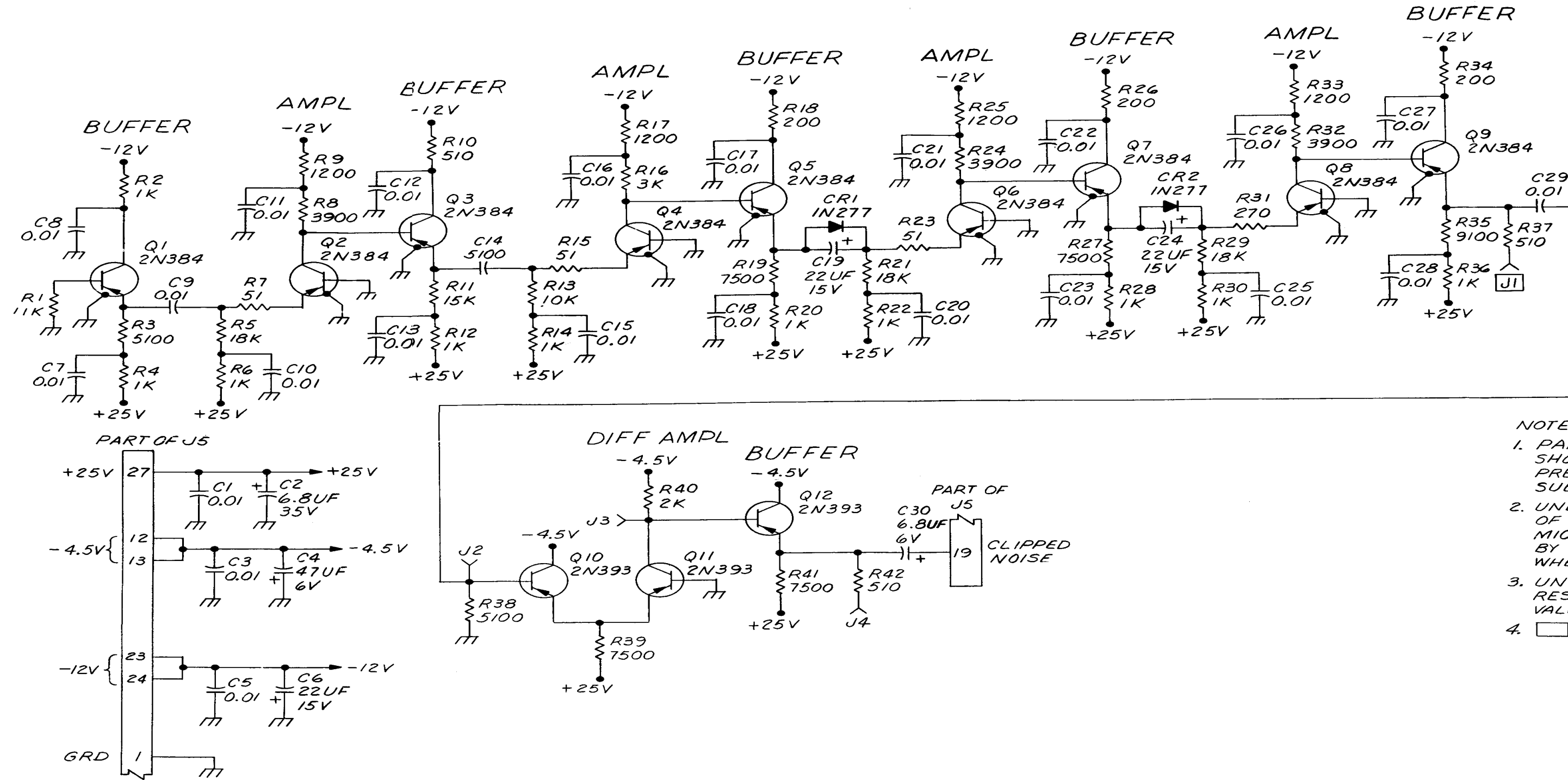


CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

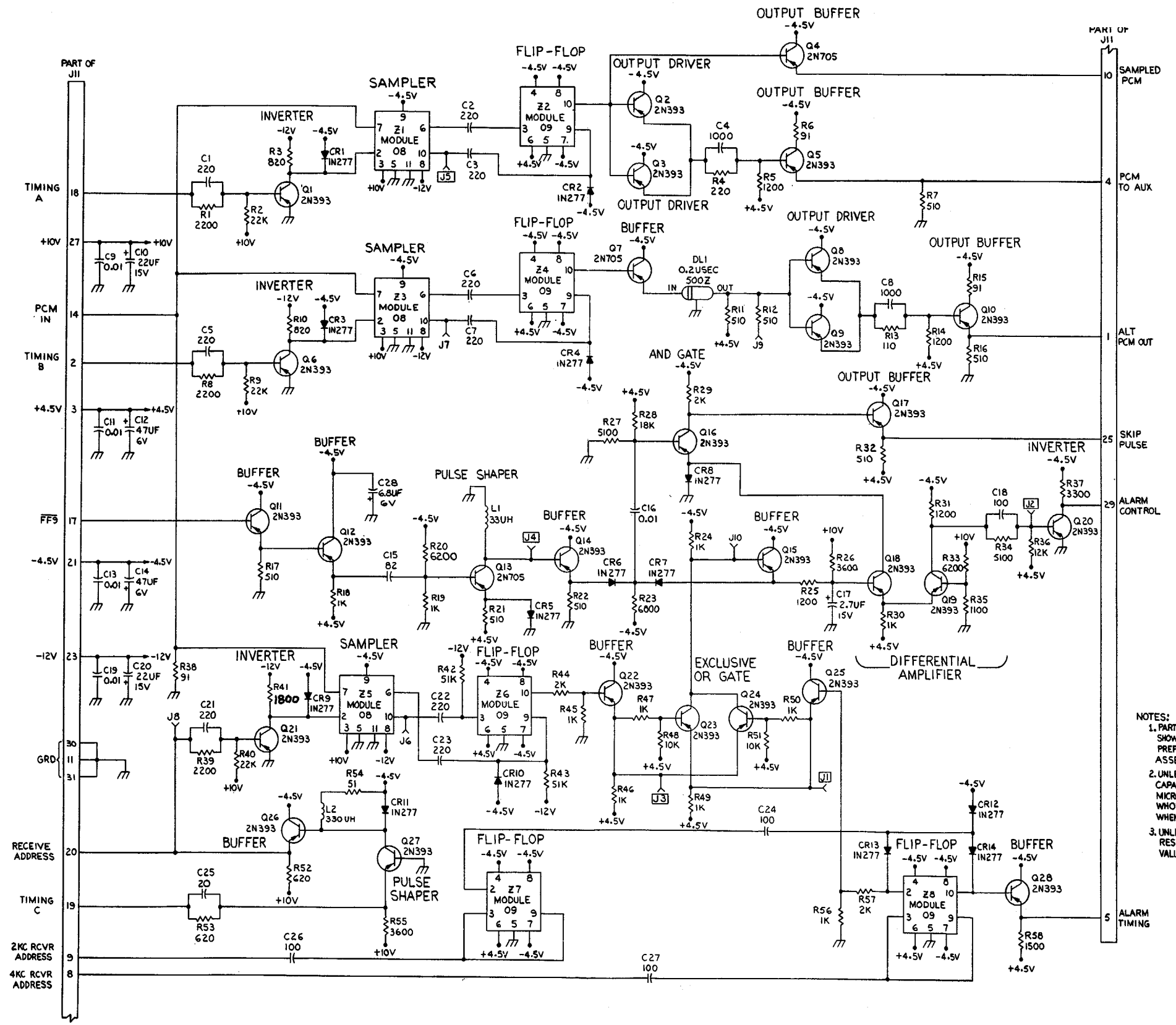
TM 5805-367-35/3-85

Figure 6-68. Panel 2a10, troubleshooting waveforms.



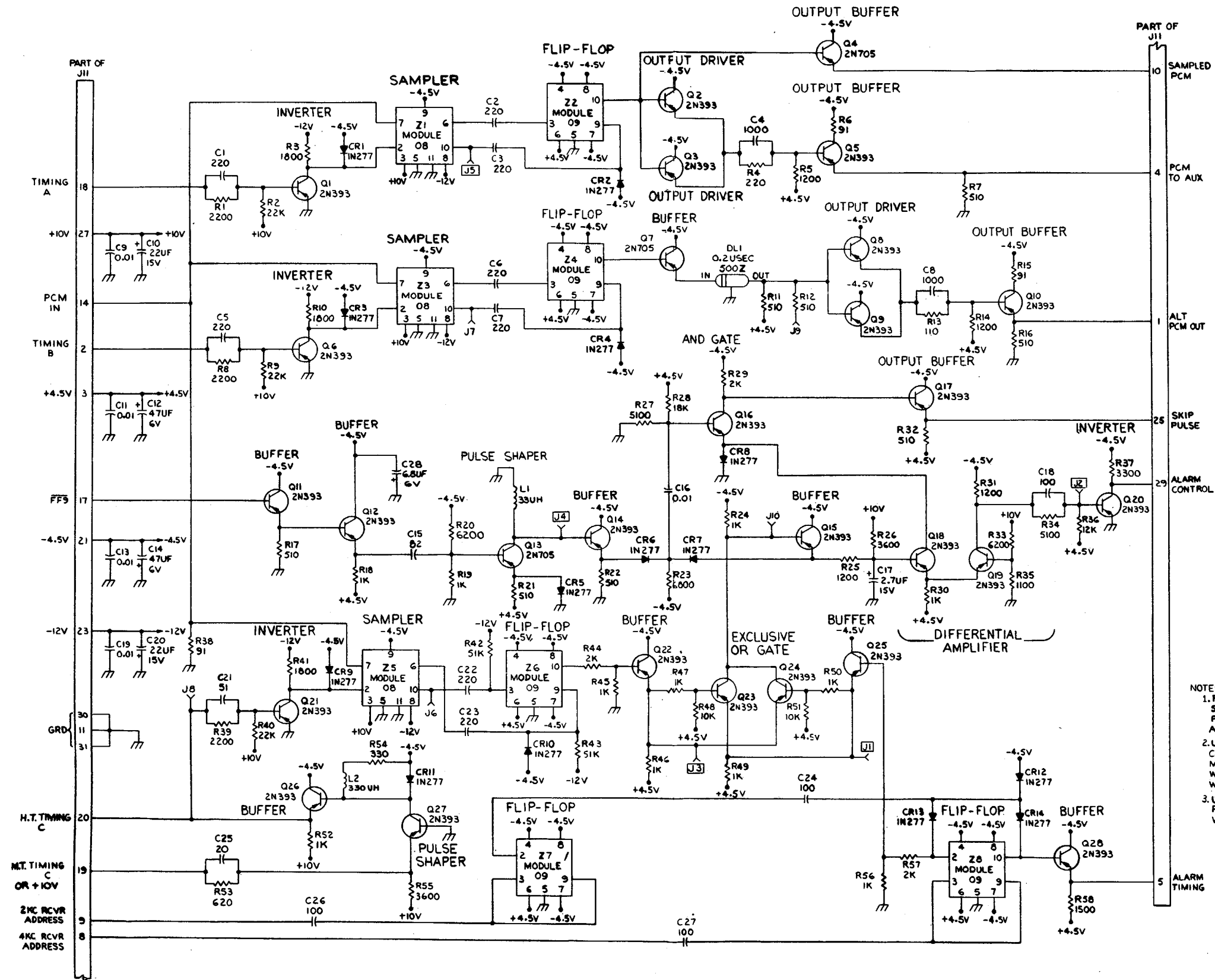
- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE $\frac{1}{4}$ WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING

Figure 6-69. Panel 1A11/2A11, schematic diagram.



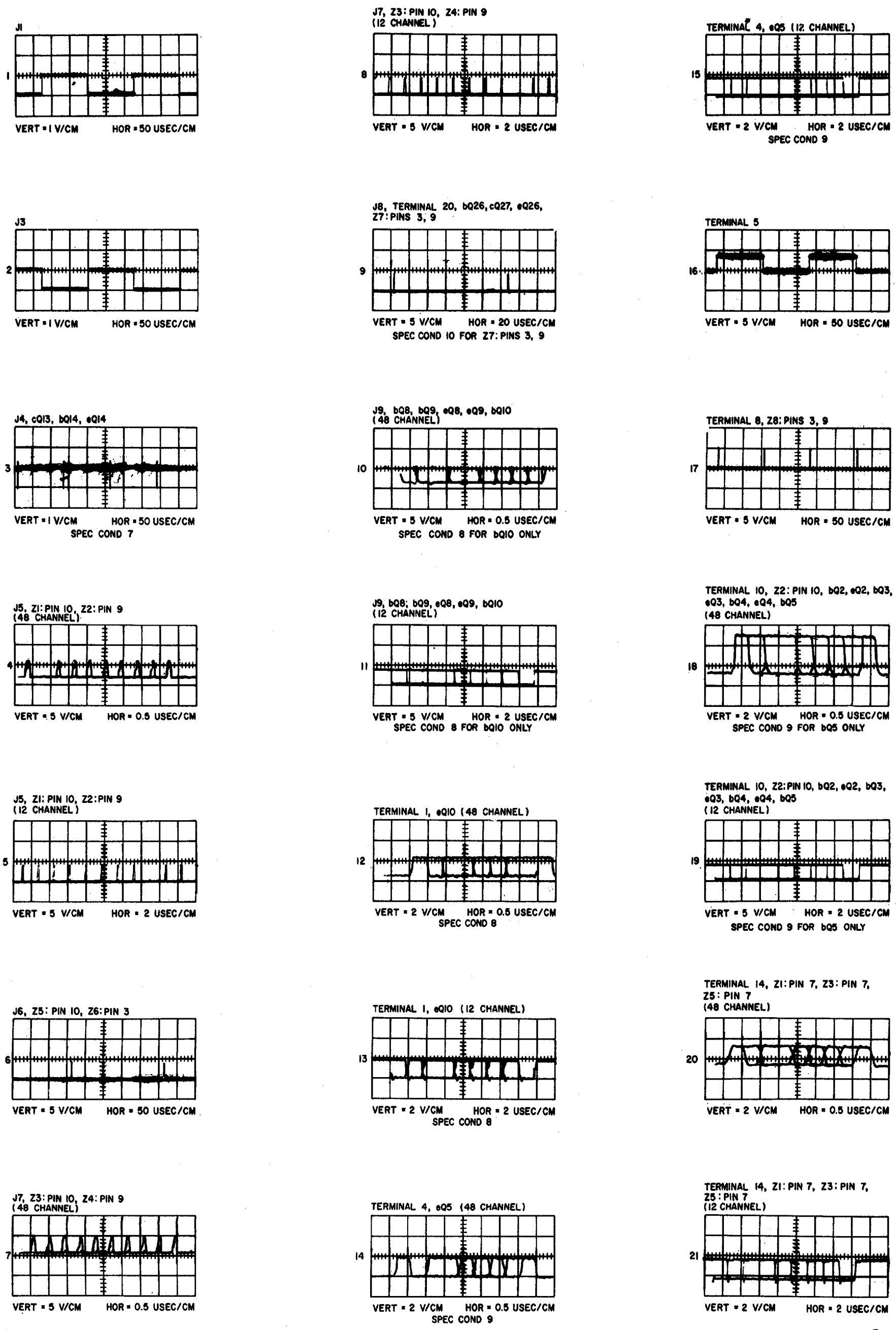
- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION. PREFIX WITH UNIT NUMBER OR SUB-ASSEMBLY DESIGNATION(S).
 2. UNLESS OTHERWISE INDICATED ALL CAPACITORS ARE EXPRESSED IN MICRO-MICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS.
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/2 WATT AND THEIR VALUE IS EXPRESSED IN OHMS.

Figure 6-70. Panel 1A12/2A12, schematic diagram.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUB-ASSEMBLY DESIGNATION (S).
 2. UNLESS OTHERWISE INDICATED ALL CAPACITORS ARE EXPRESSED IN MICRO-MICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS.
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/2 WATT AND THEIR VALUE IS EXPRESSED IN OHMS.

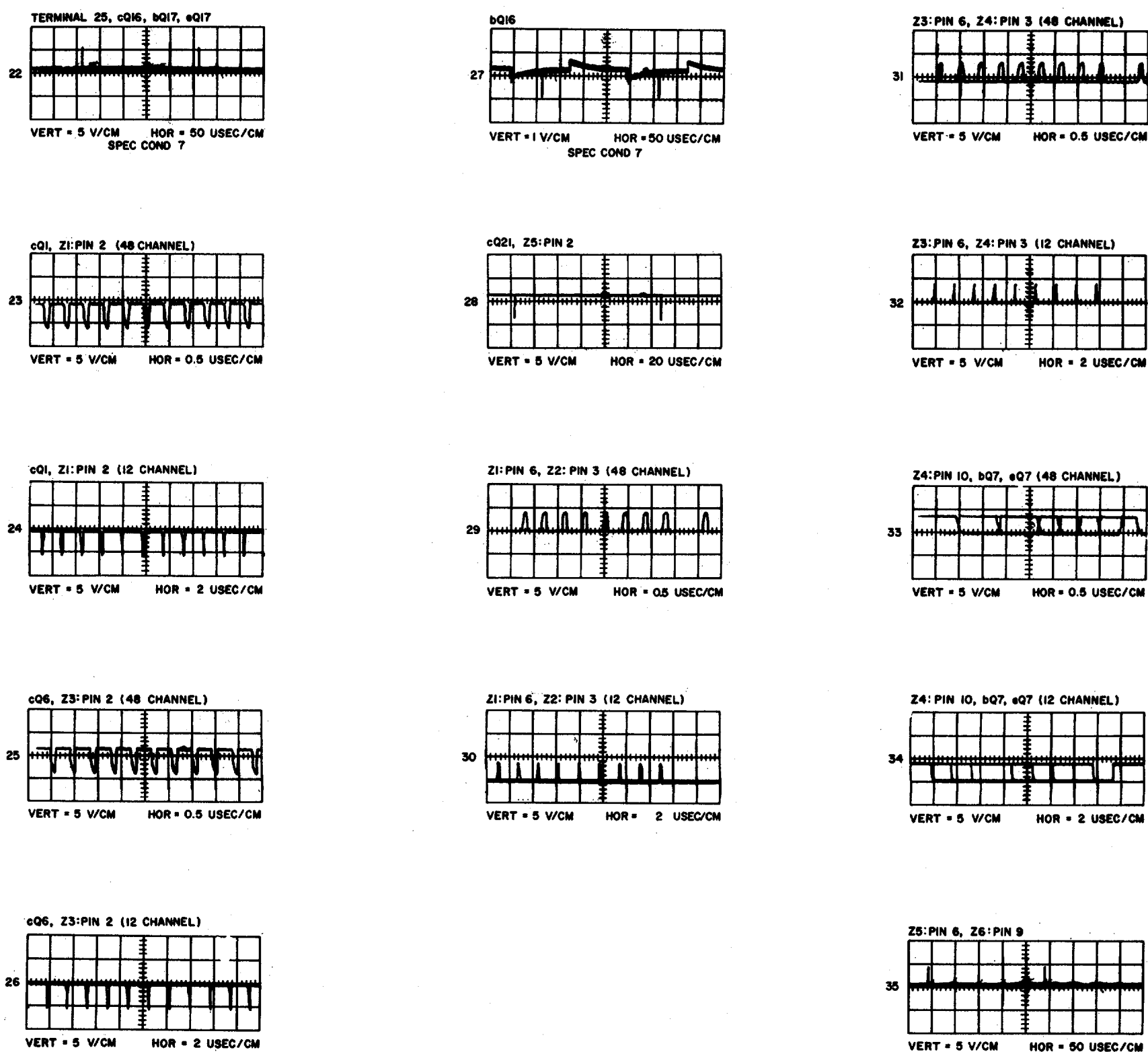
Figure 6-70.1. Panel 1A121, schematic diagram.



TM5805-367-35/3-91 ①

TM 11-5805-367-35/3

Figure 6-71①. Panel 1A12/2A12, troubleshooting waveforms (part 1 of 2).



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

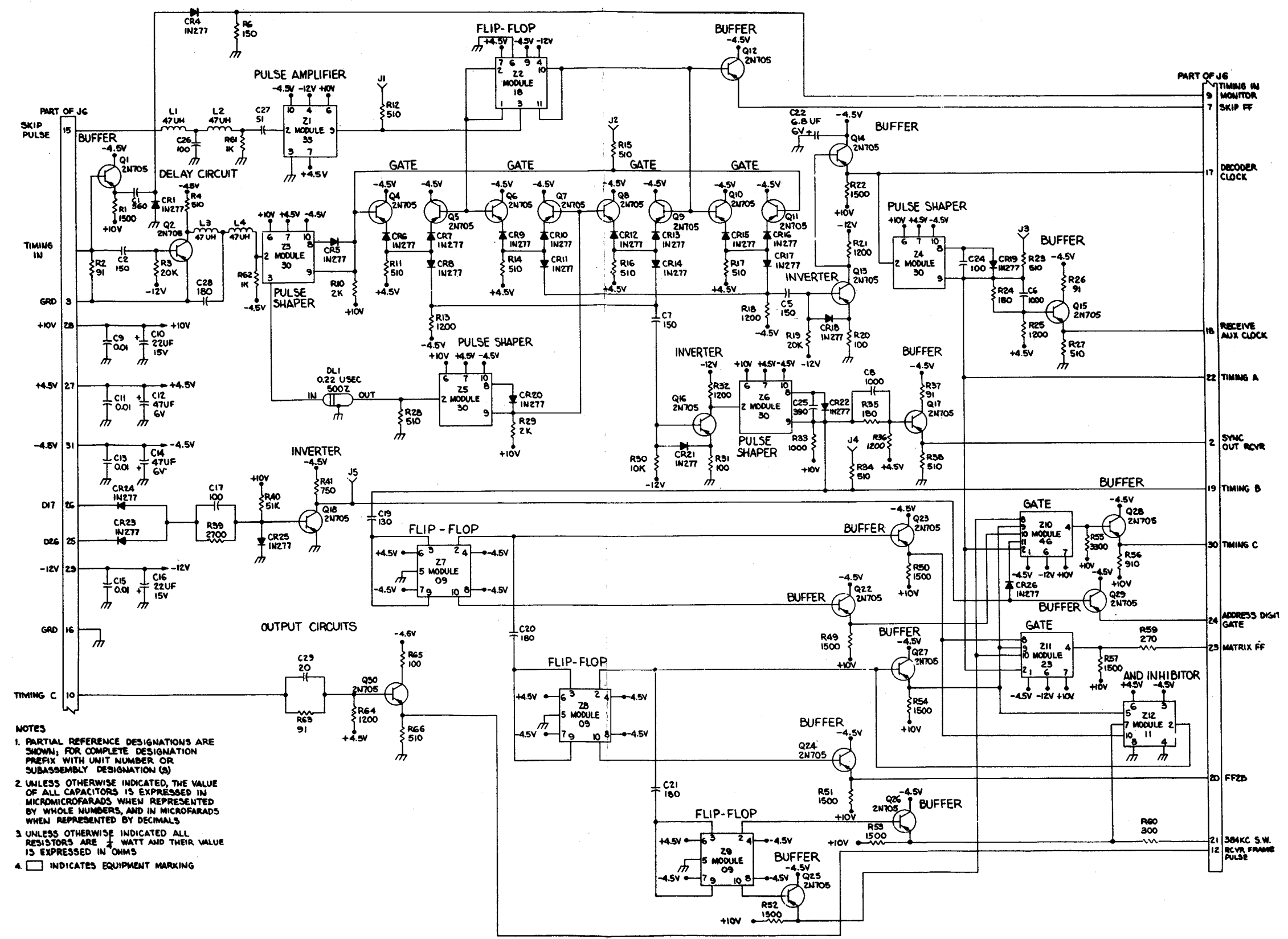
THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

B. SPECIAL.

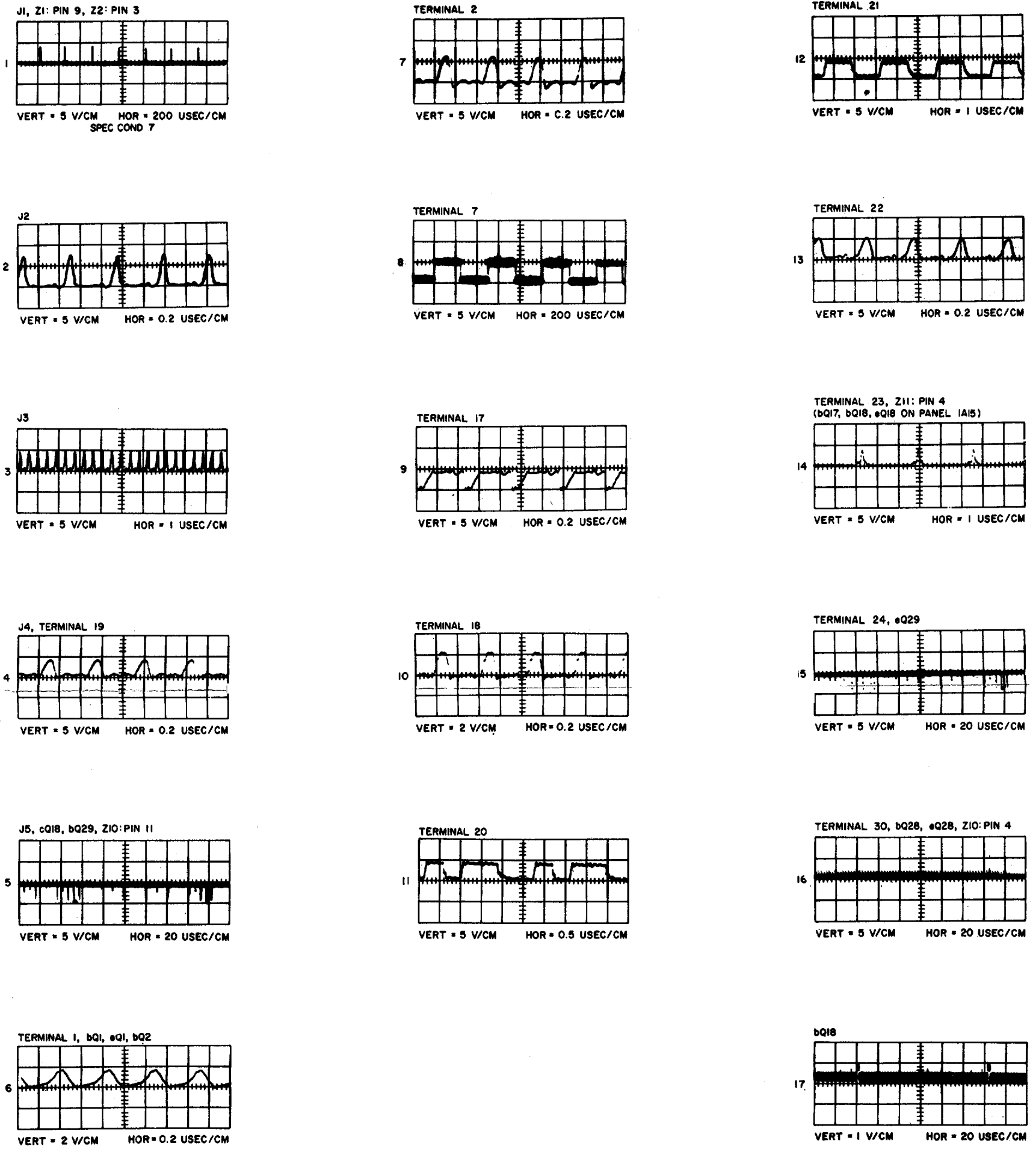
7. PCM IN CONNECTOR REMOVED (UNIT OUT OF FRAME).
8. TERMINAL 1 TERMINATED IN 91-OHM LOAD.
9. TERMINAL 4 TERMINATED IN 91-OHM LOAD.
10. CHECKED WITH SYNC IN INPUT OF TEST MULTIPLEXER. OSCILLOSCOPE SYNCHRONIZED FROM SYNC OUT CONNECTOR OF SECOND TEST MULTIPLEXER.

Figure 6-71②. Panel 1A12/2A12, troubleshooting waveforms (part 2 of 2).



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

Figure 6-72. Panel 1A13, schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THE ILLUSTRATIONS. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

B. SPECIAL.

7. PCM IN CONNECTOR REMOVED (UNIT OUT OF FRAME).

Figure 6-73. Panel 1A13, troubleshooting waveforms.

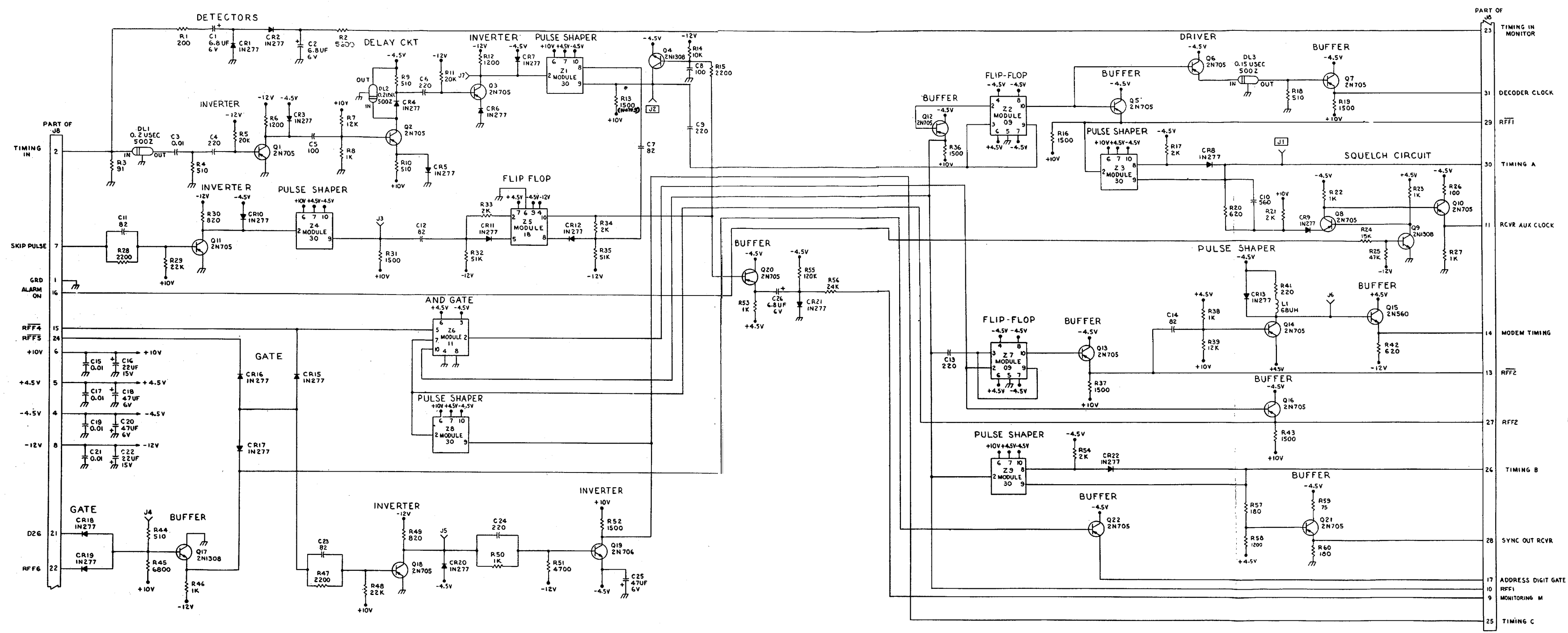
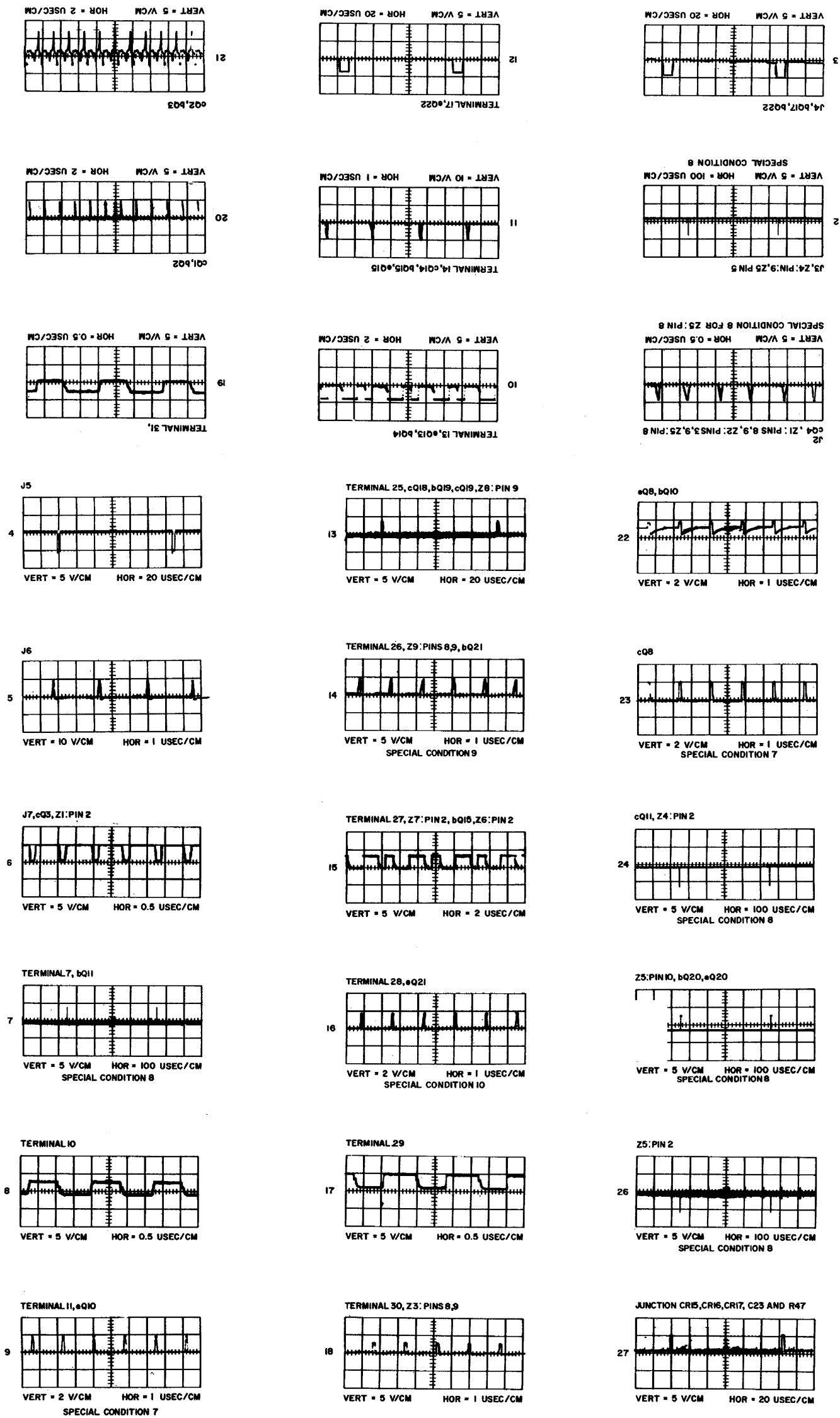


Figure 6-74. Panel 2A13, schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

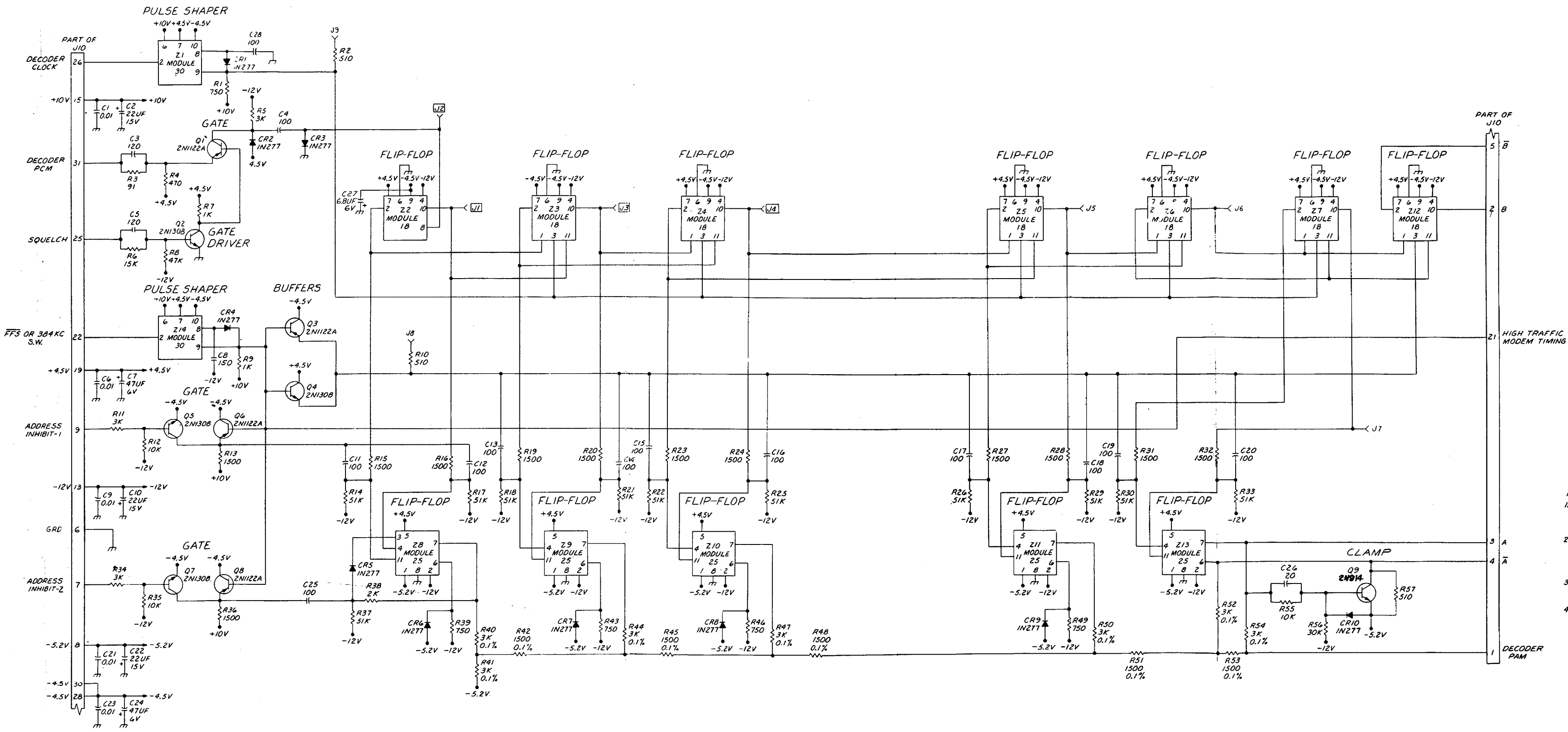
THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

B. SPECIAL.

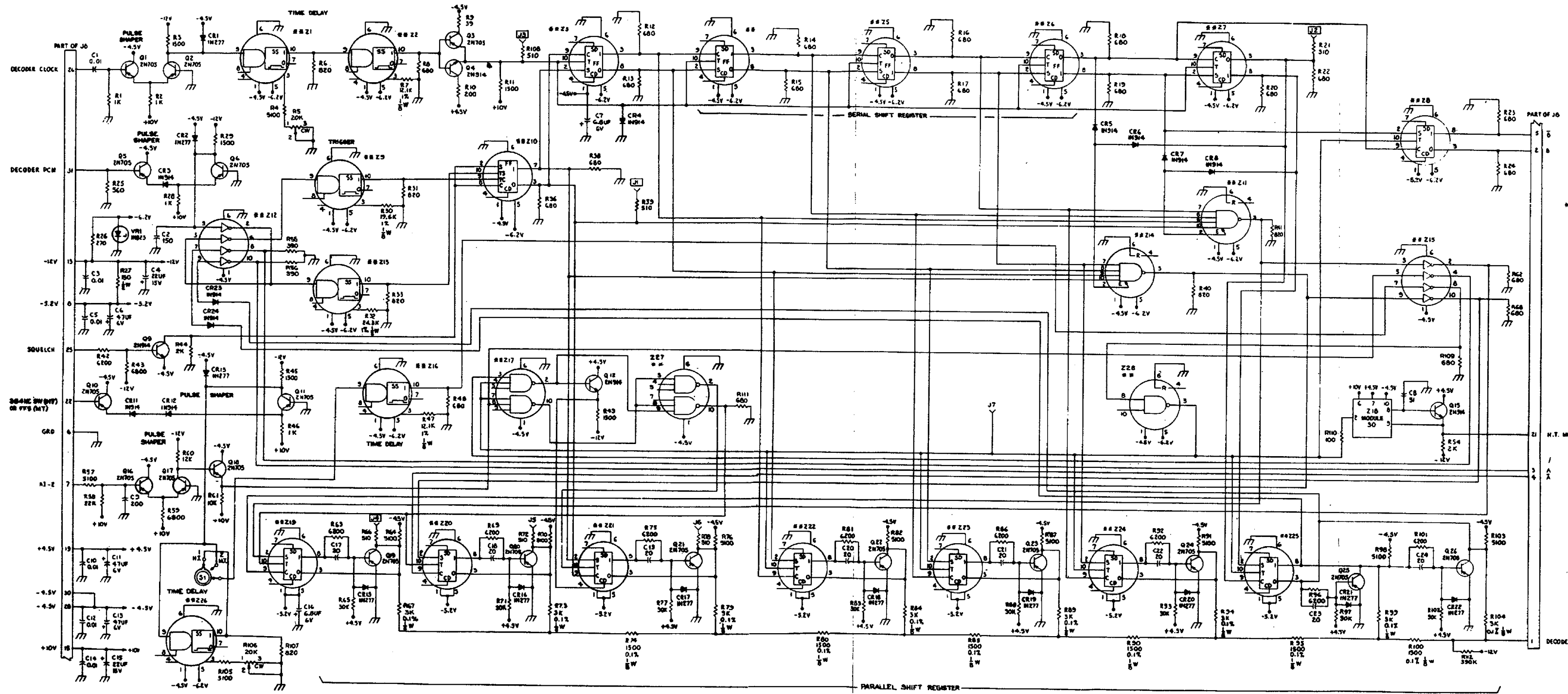
7. TERMINAL 11 TERMINATED IN 91-OHM LOAD.
8. PCM IN CONNECTOR REMOVED (UNIT OUT OF FRAME).
9. TERMINAL 26 TERMINATED IN 91-OHM LOAD.
10. TERMINAL 28 TERMINATED IN 91-OHM LOAD.

Figure 6-75. Panel 2A13, troubleshooting waveforms.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/2 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

Figure 6-76. Panel 1A14/2A14, schematic diagram.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION. PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION.
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS.
 3. UNLESS OTHERWISE INDICATED RESISTORS ARE .25 WATT AND THEIR VALUE IS EXPRESSED IN OHMS.
 4. □ INDICATES EQUIPMENT MARKING.
- ## 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994, 995, 996, 997, 998, 999, 1000.

Figure 6-77.1. Panel 1A14A/2A14A, schematic diagram.

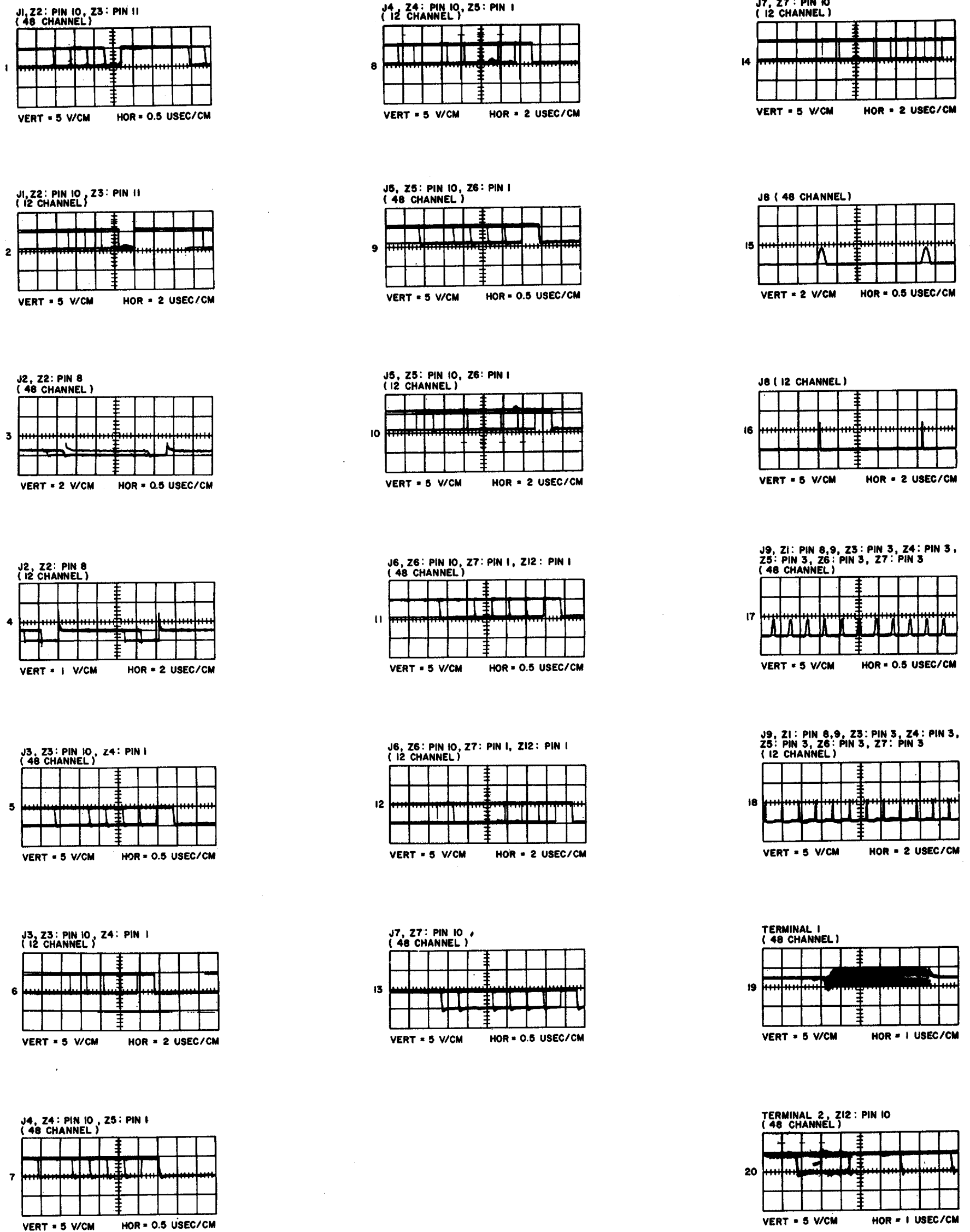
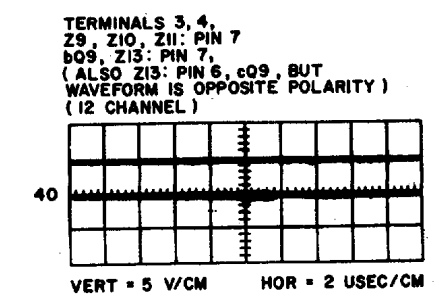
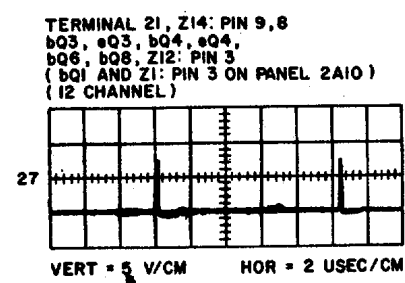
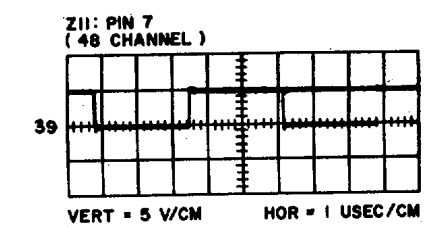
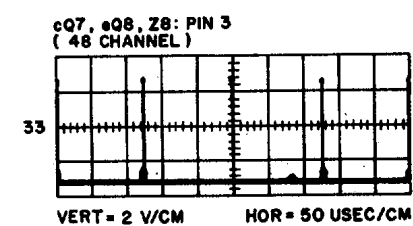
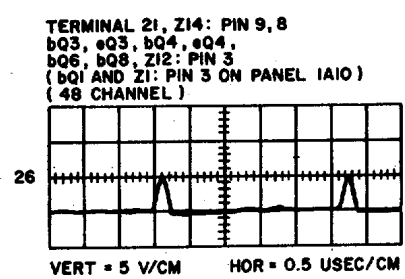
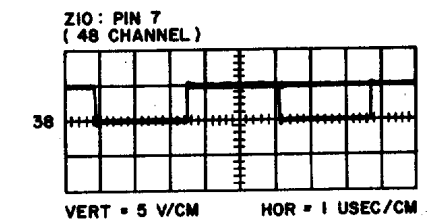
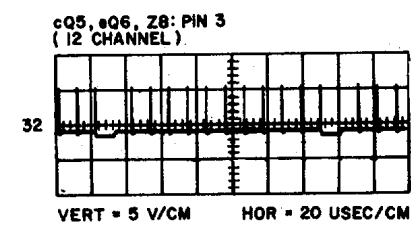
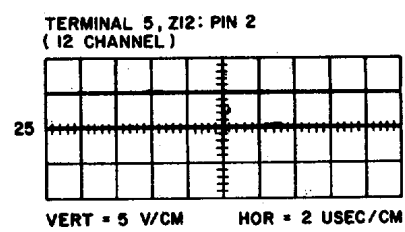
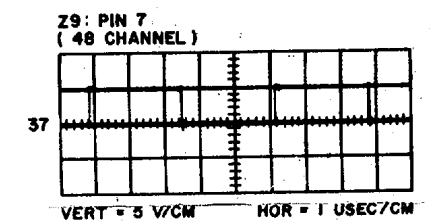
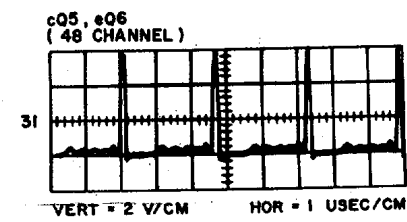
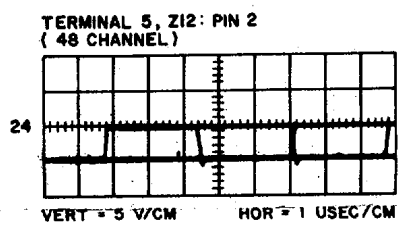
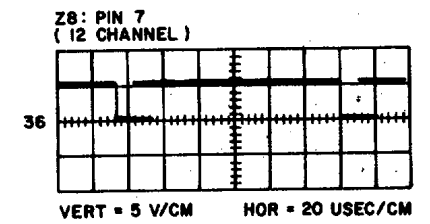
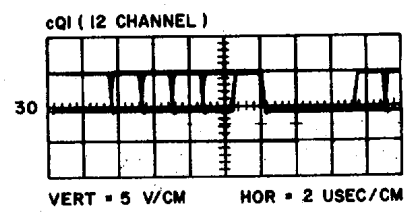
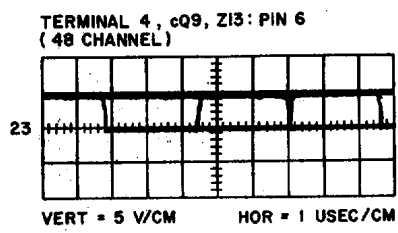
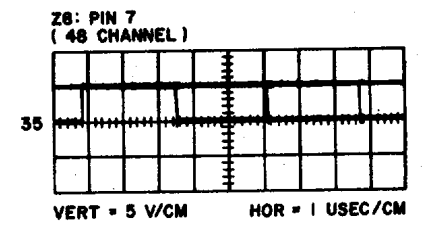
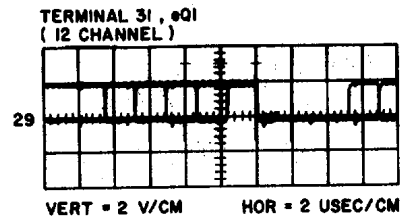
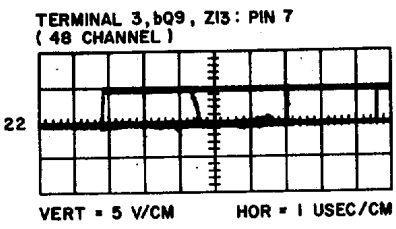
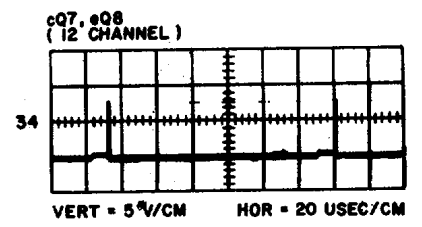
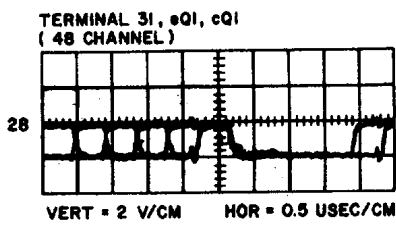
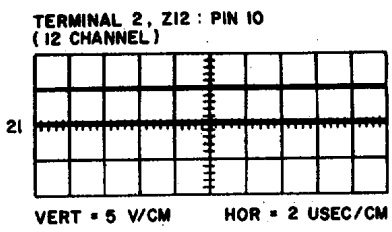


Figure 6-77①. Panel 1A14/2A14, troubleshooting waveforms.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

Figure 6-77. Panel 1A14/2A14, troubleshooting waveforms.

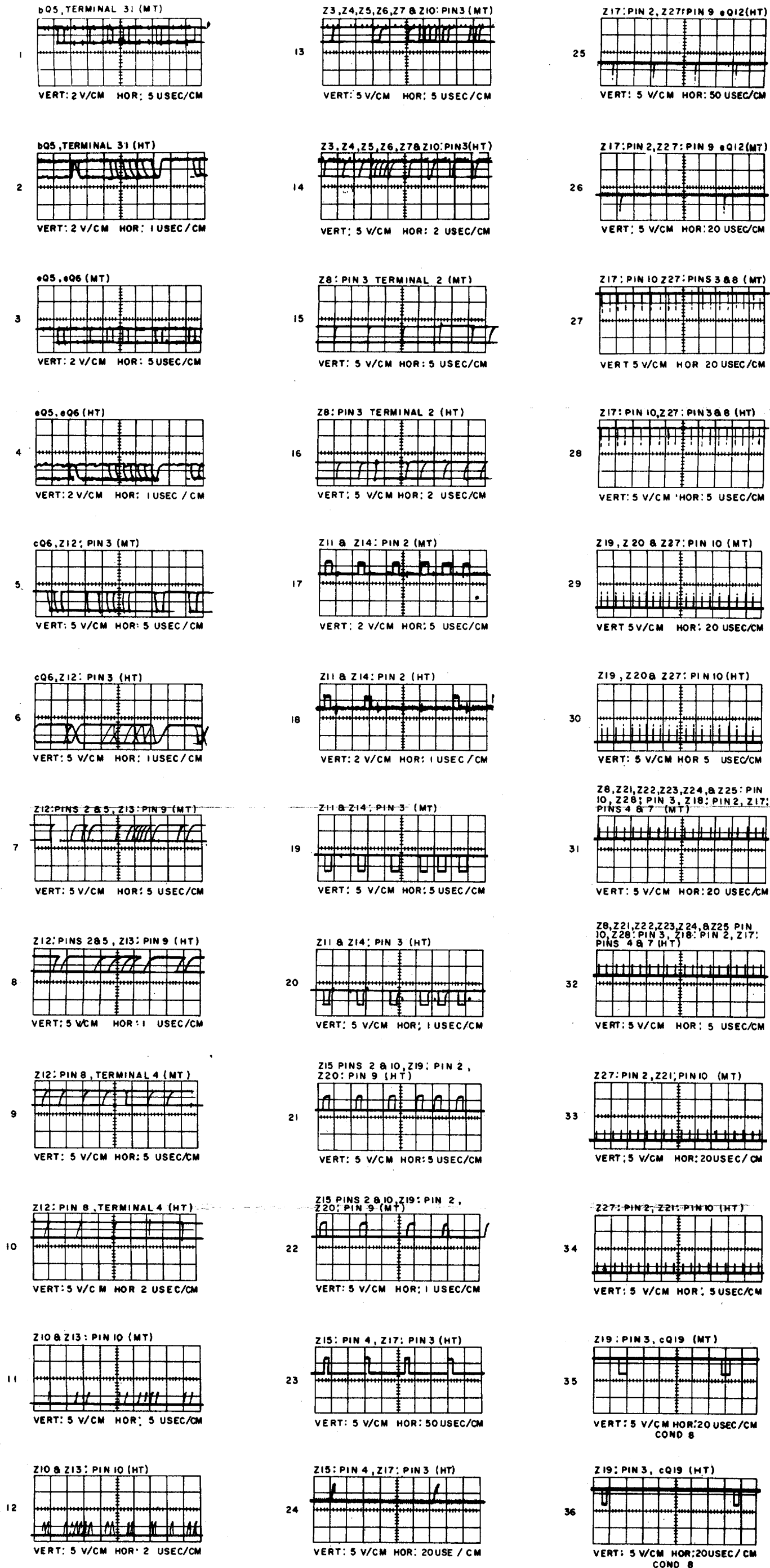


Figure 6-77.2①. (Sheet 1 of 3) Panel 1A14A/2A14A, troubleshooting waveforms.

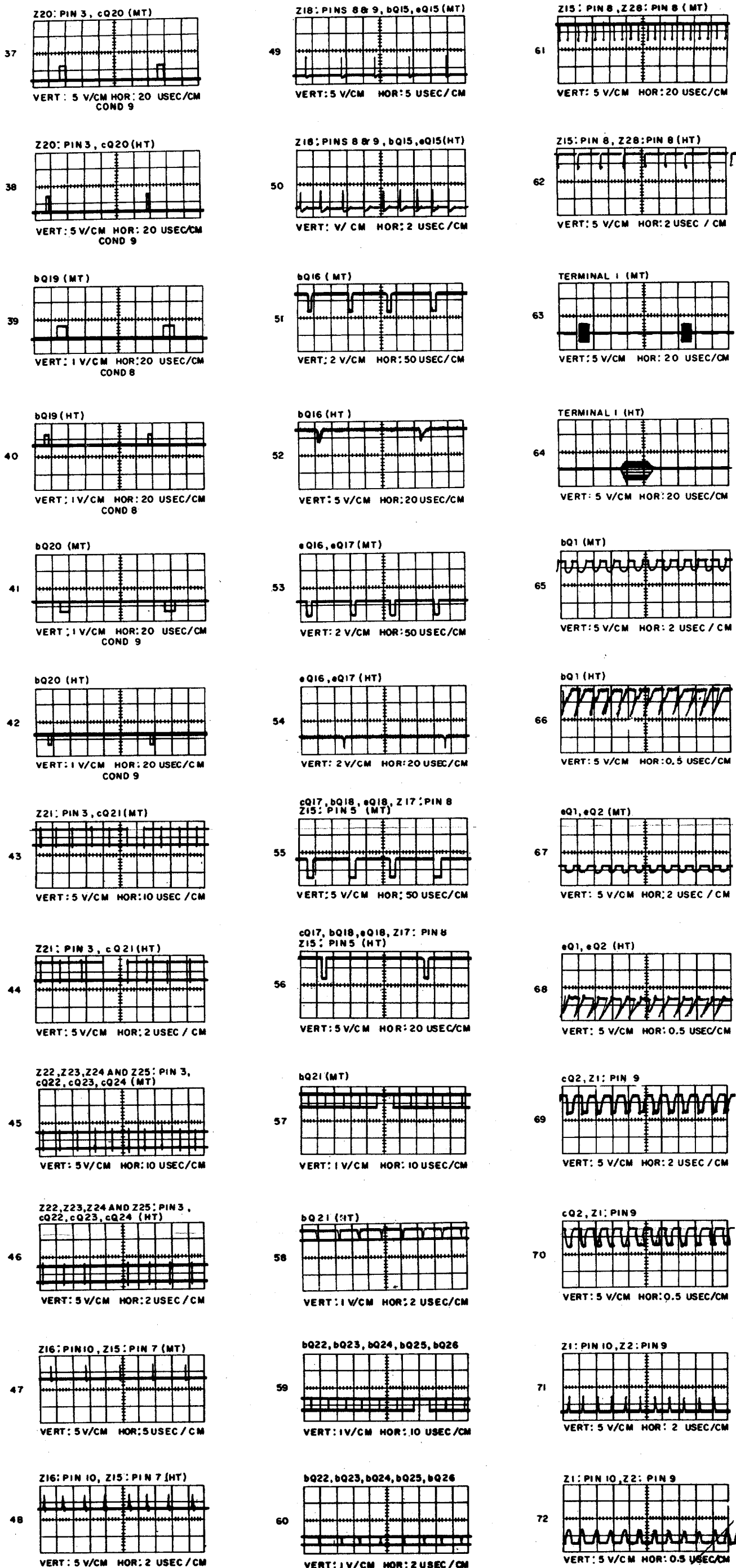
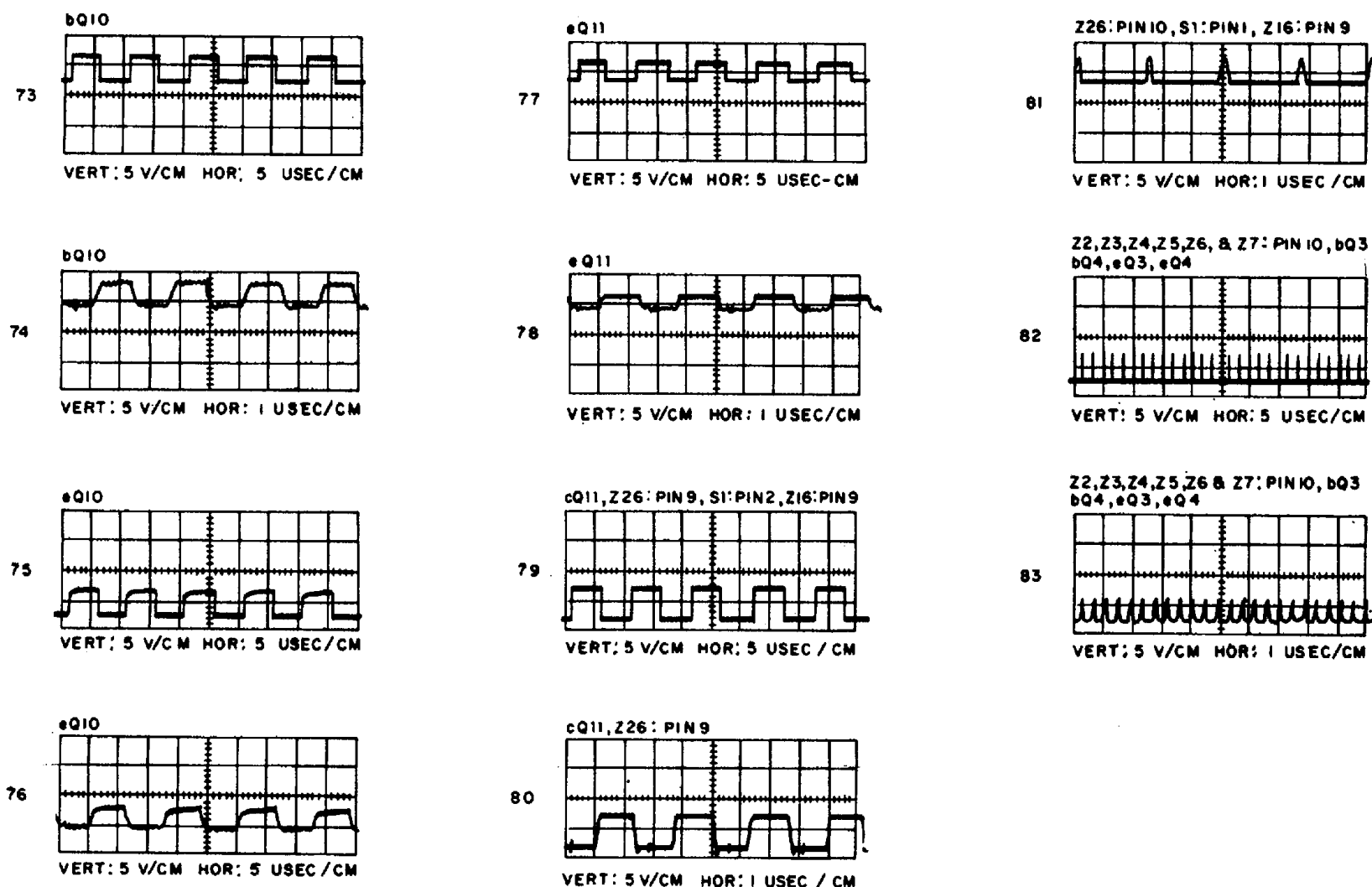


Figure 6-77.2² (Sheet 2 of 3). Panel 1A14A/2A14A, troubleshooting waveforms.

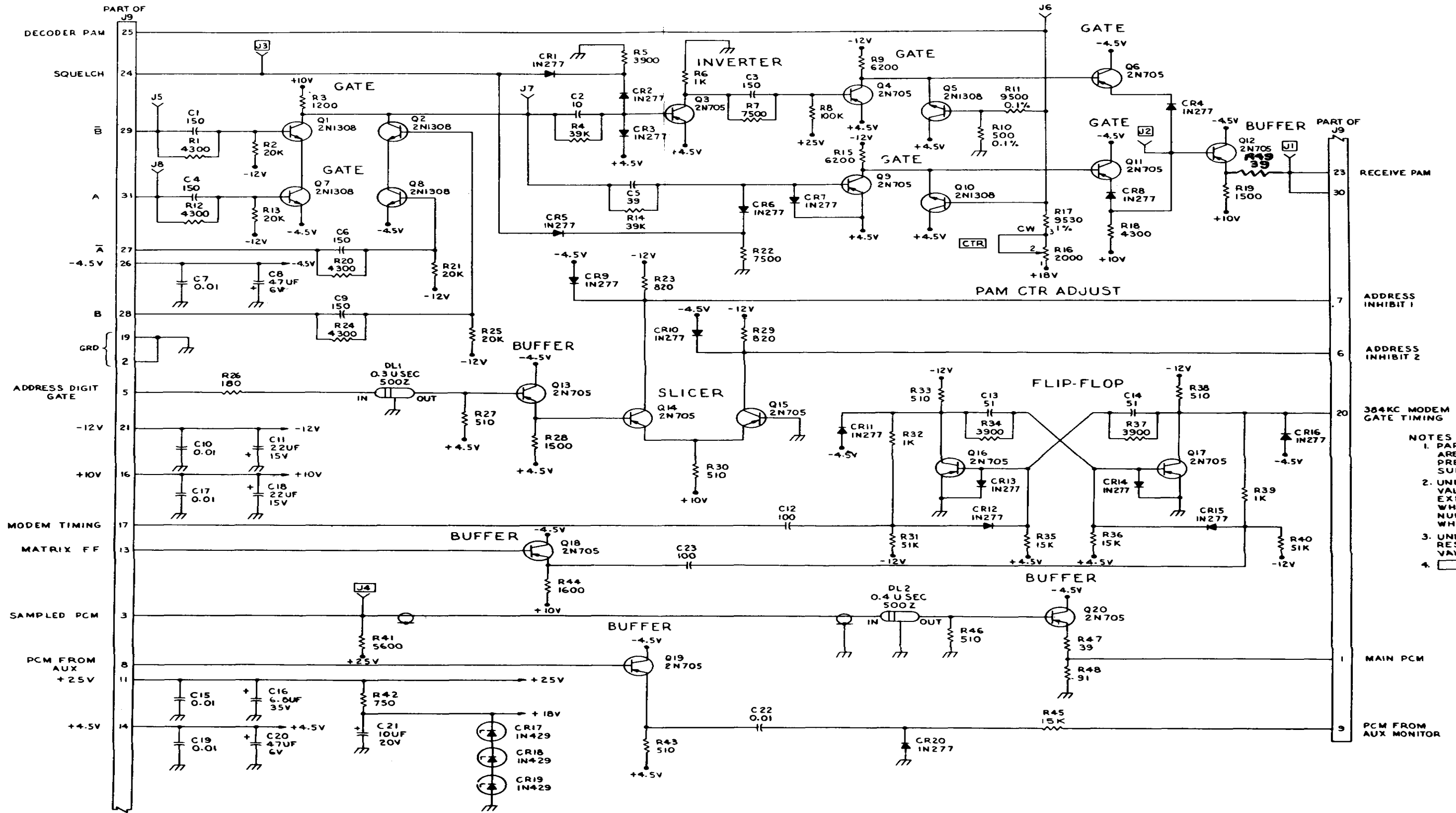


CONDITIONS FOR OBTAINING WAVEFORMS

NOTES 1 THROUGH 7 GIVEN BELOW ARE APPLICABLE TO ALL WAVEFORMS ON THIS ILLUSTRATION. NOTE — REFERENCES GIVEN WITH WAVEFORMS PERTAIN TO CONDITIONS LISTED BELOW WHICH ARE REQUIRED TO OBTAIN THAT WAVEFORM.

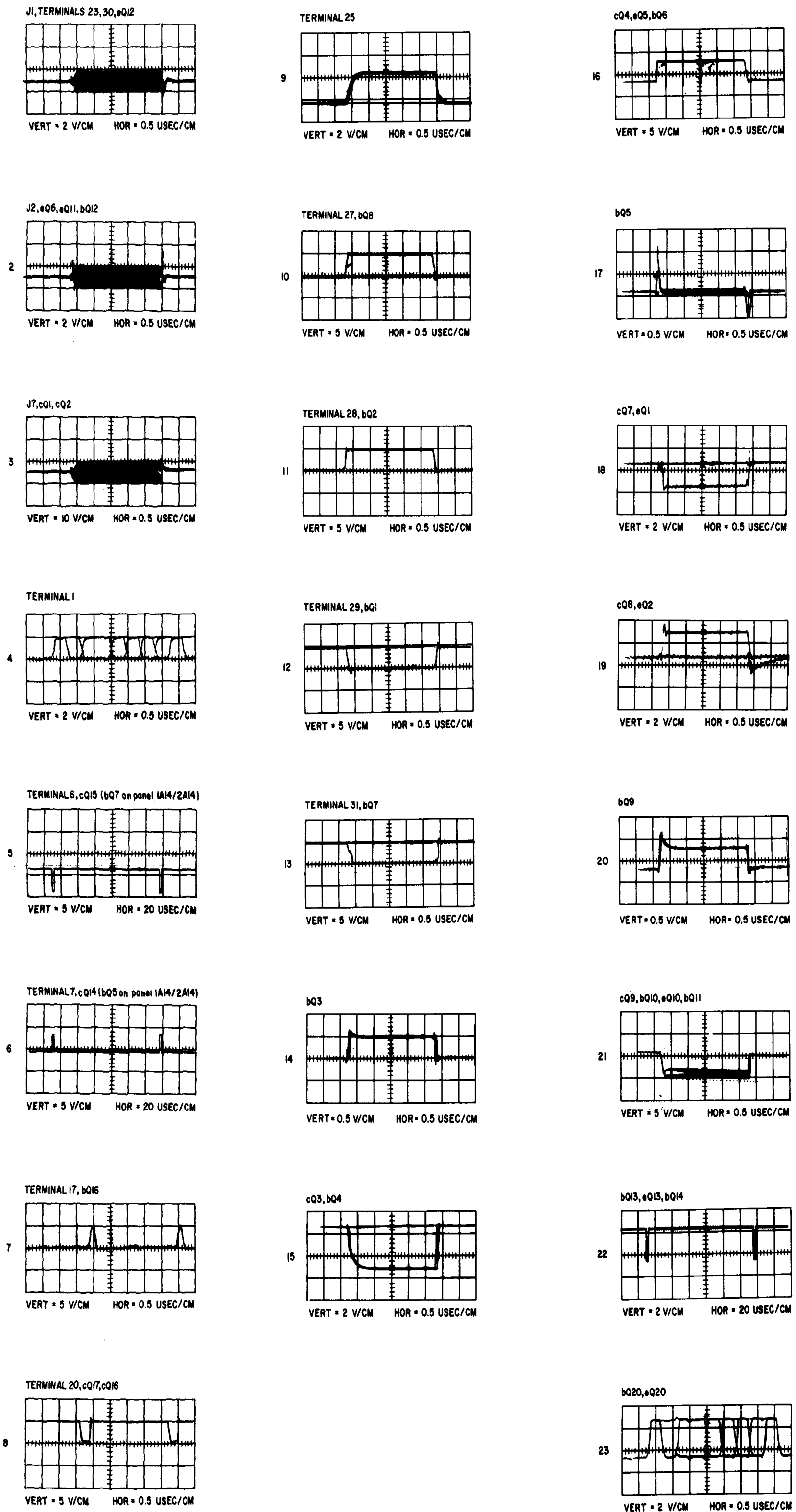
1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH OPERATED TO OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.
7. SWITCH S1 ON 1A14A/2A14A PANEL OPERATED TO HT WITH A TD-353/U, AND TO MT WITH A TD-352/U.
8. CODE LEVEL 15 MUST BE PRESENT FOR WAVEFORM.
9. CODE LEVEL 48 MUST BE PRESENT FOR WAVEFORM.

Figure 6-77.2 (Sheet 3 of 3). Panel 1A14A/2A14A, troubleshooting waveforms.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS; AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

Figure 6-78. Panel 1A15, schematic diagram.

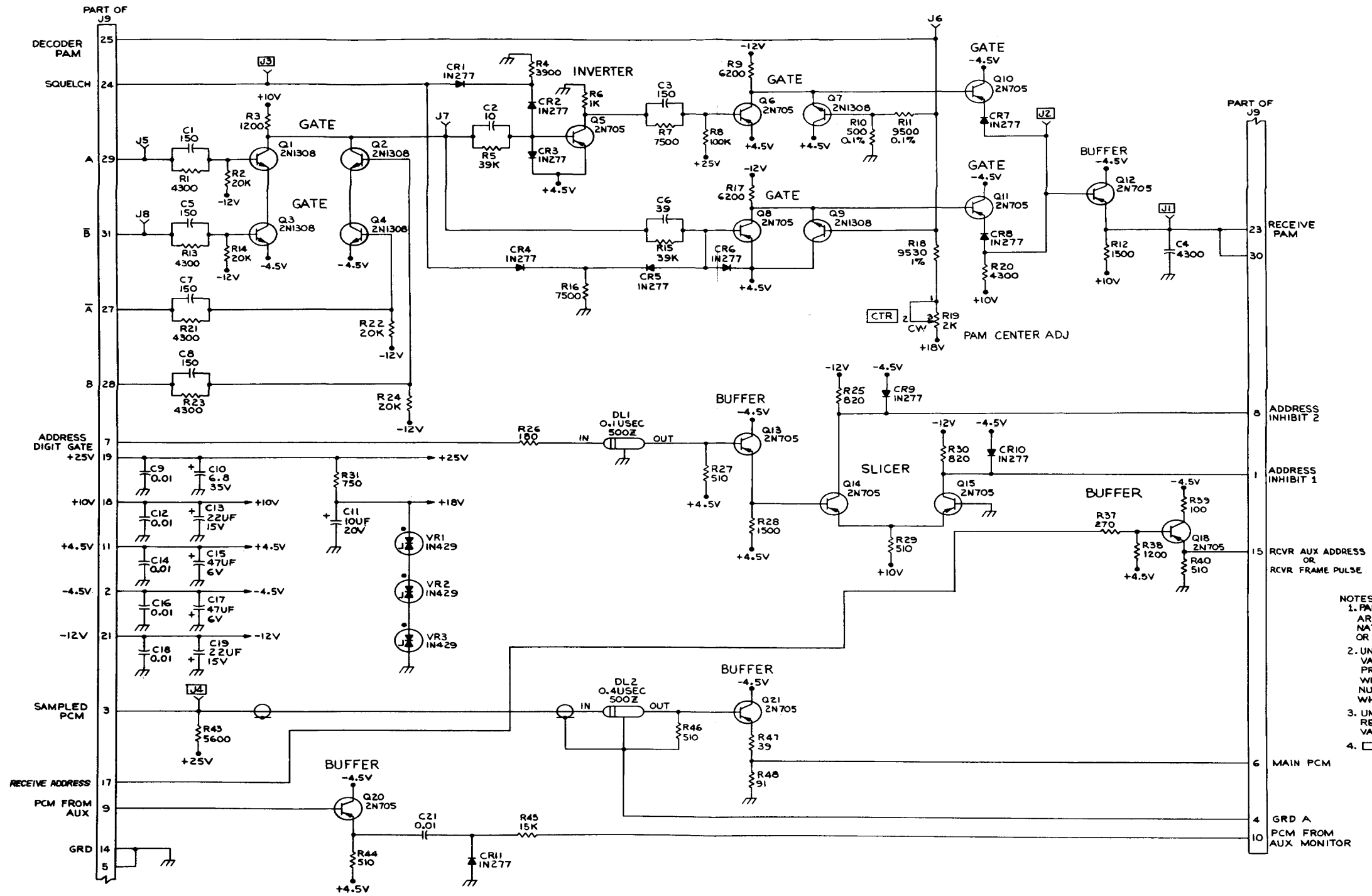


CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

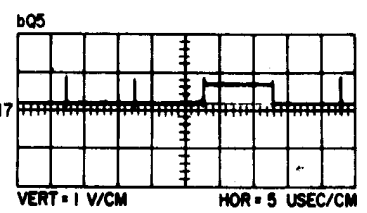
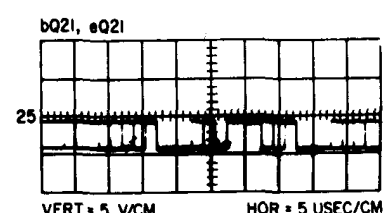
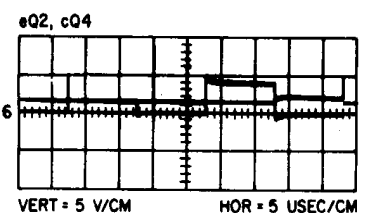
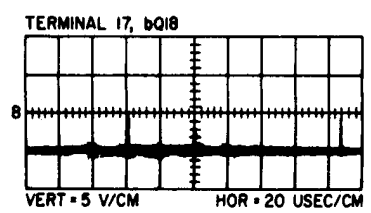
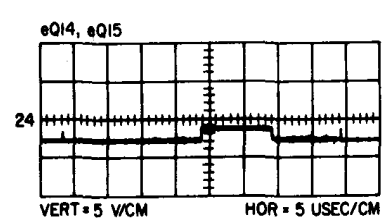
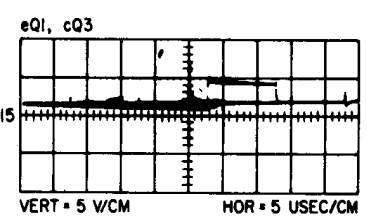
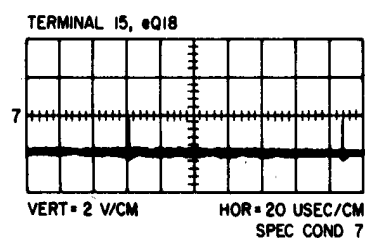
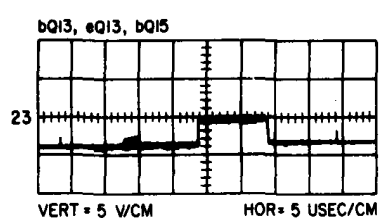
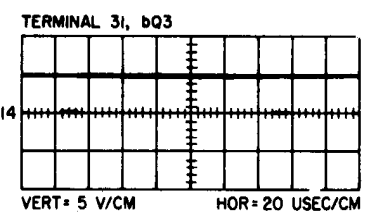
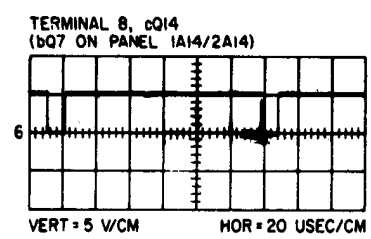
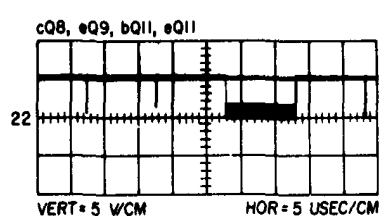
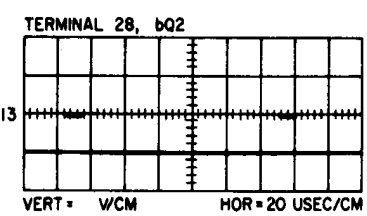
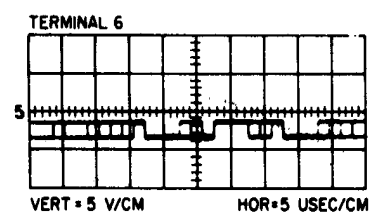
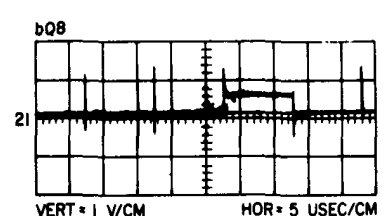
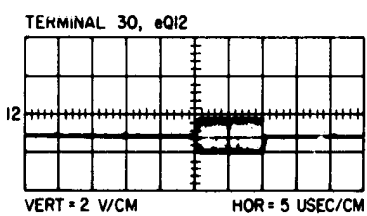
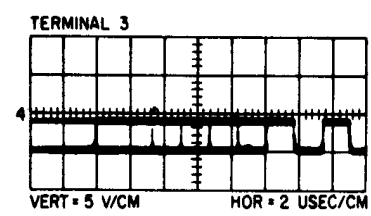
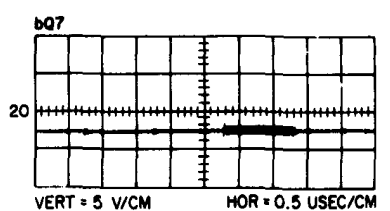
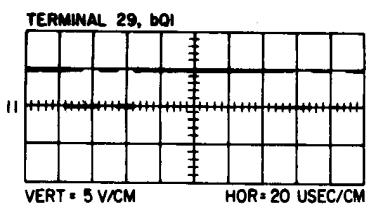
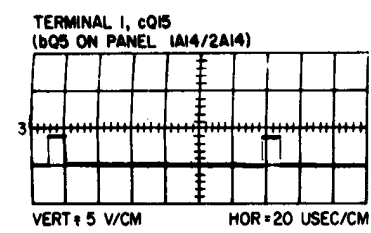
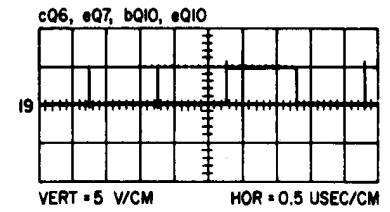
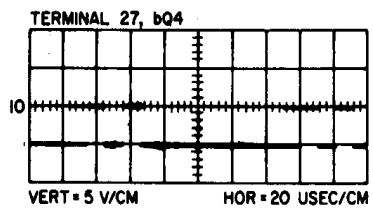
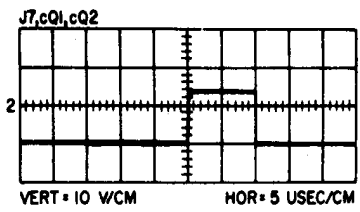
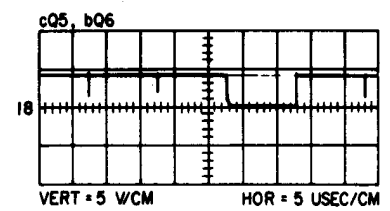
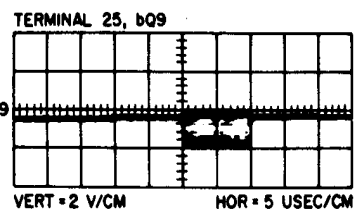
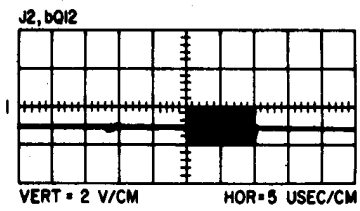
TM5805-367-35/3-104

Figure 6-79. Panel 1A15, troubleshooting waveforms.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/2 WATT AND THE VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

Figure 6-80. Panel 2A15, schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

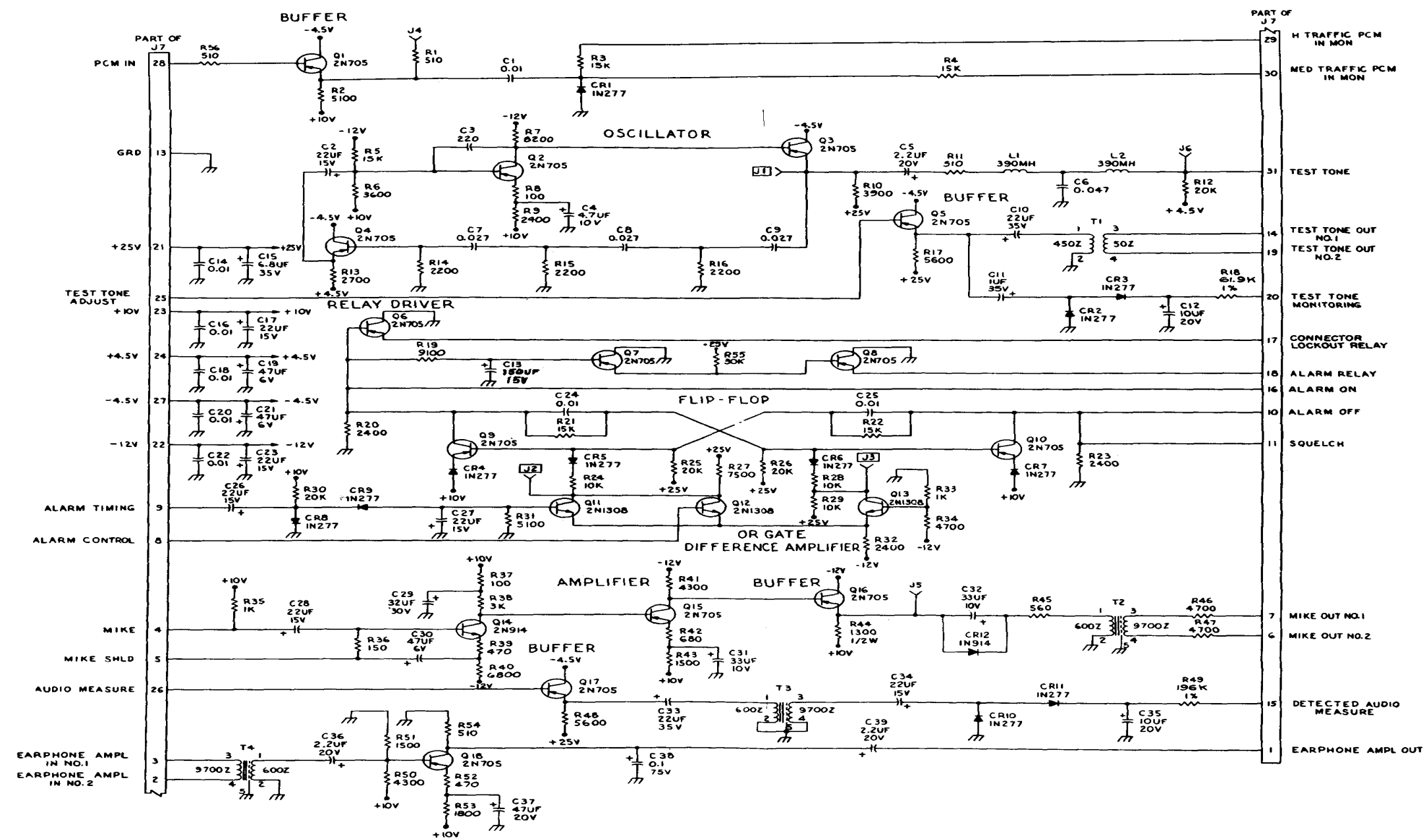
1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

B. SPECIAL.

7. TERMINAL 15 TERMINATED IN 91-OHM LOAD.

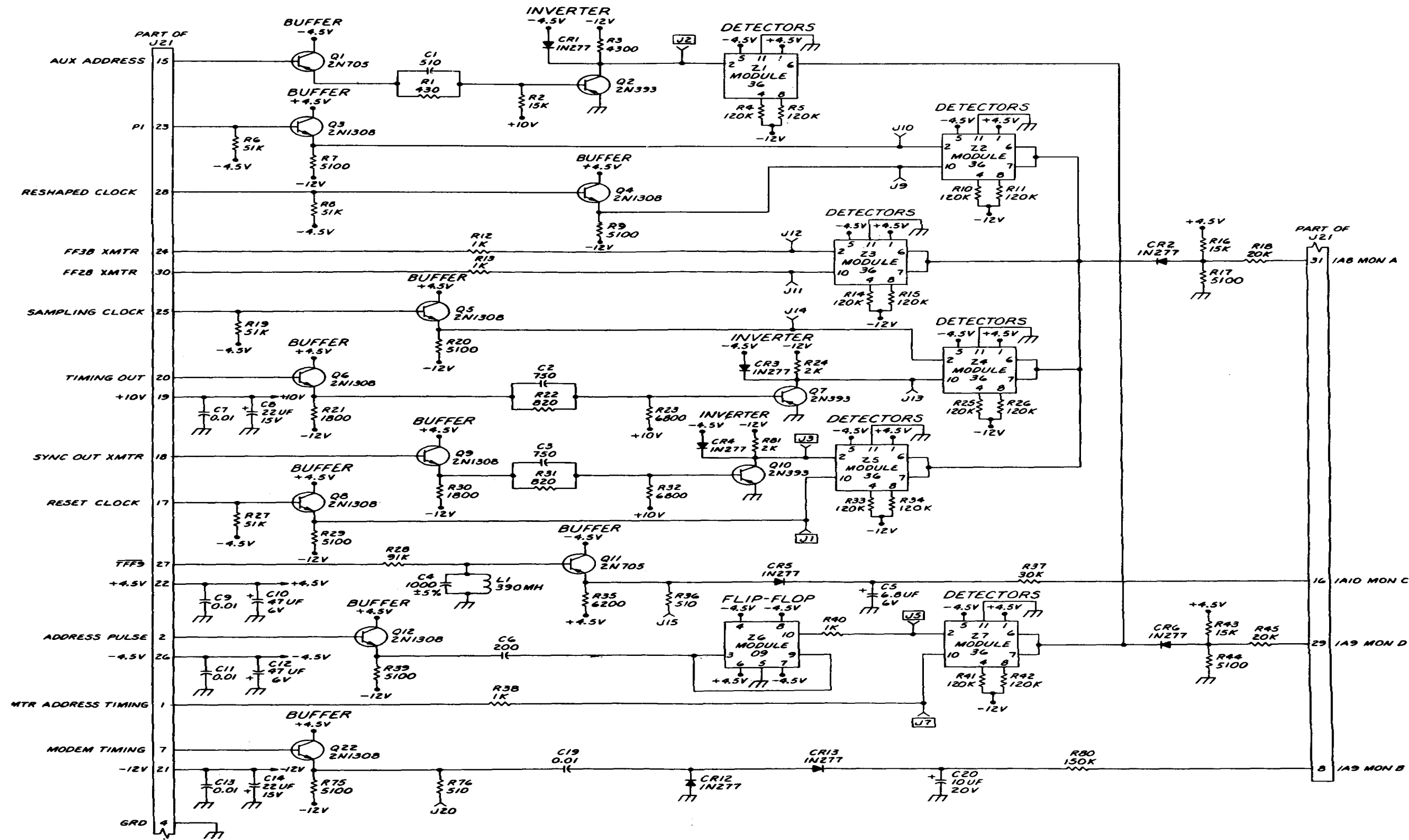
TM5805-367-36/3-107

Figure 6-81. Panel 2A15, troubleshooting waveforms.



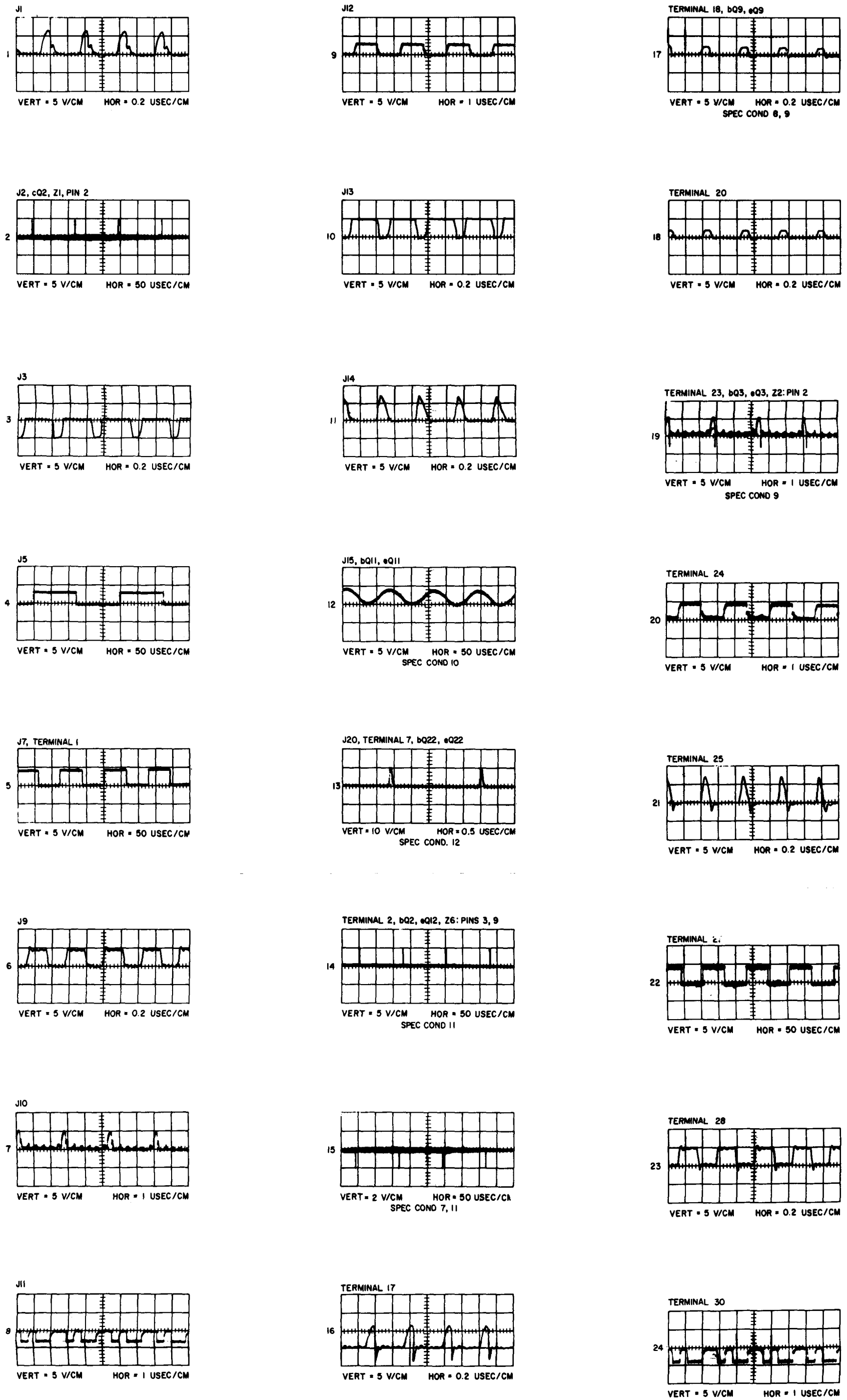
- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/2 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

Figure 6-82. Panel 1A16/@a16, schematic diagram.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKINGS

Figure 6-83. Panel 1A17, schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL

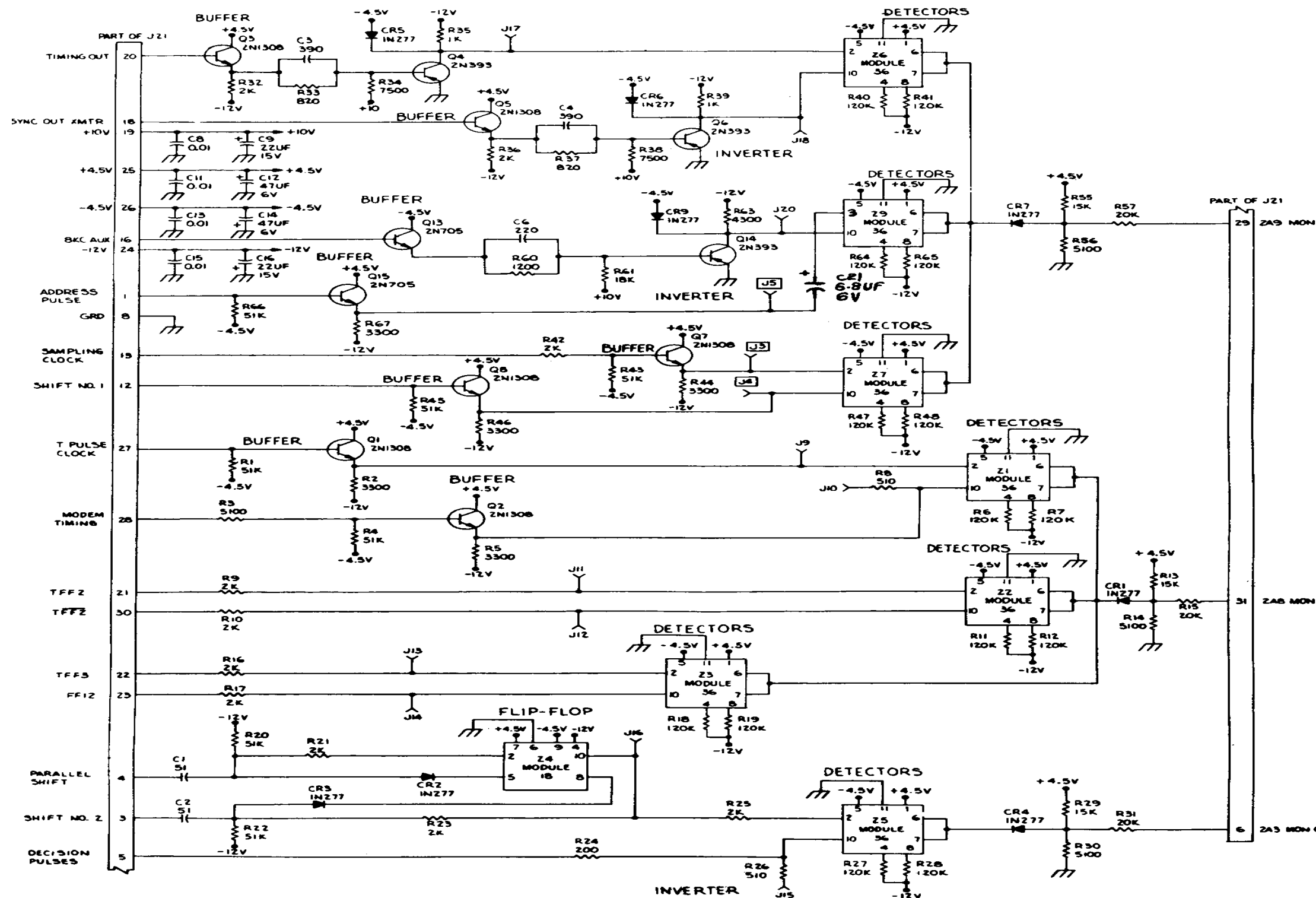
THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

B. SPECIAL

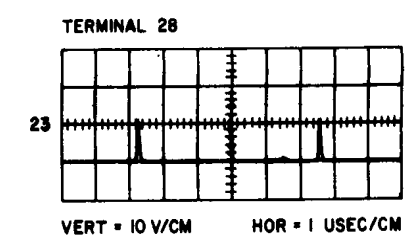
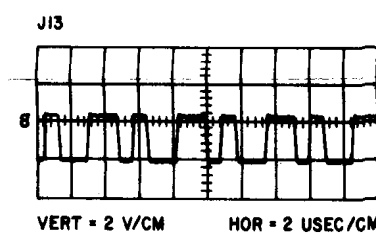
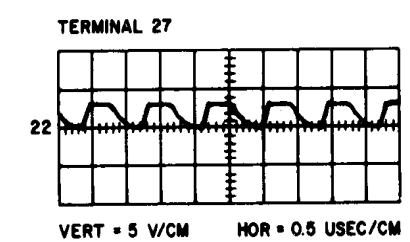
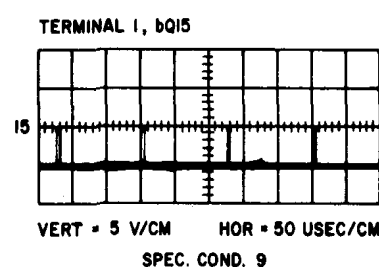
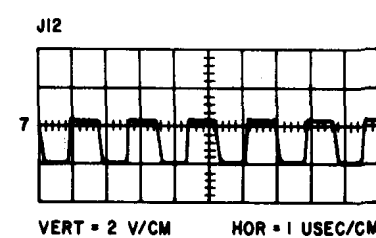
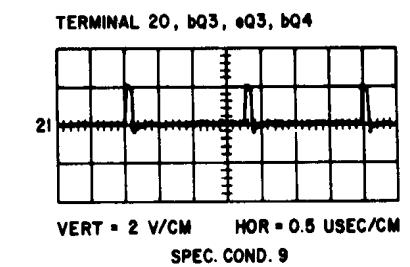
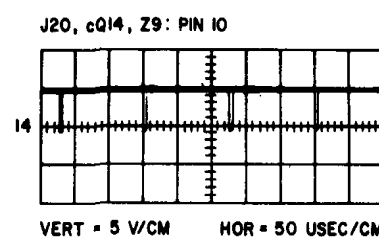
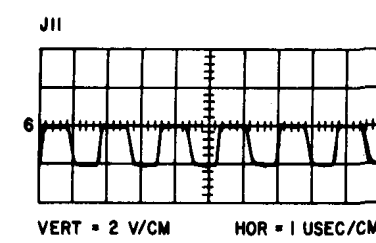
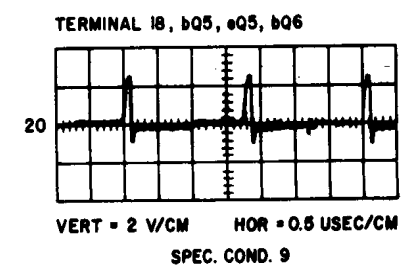
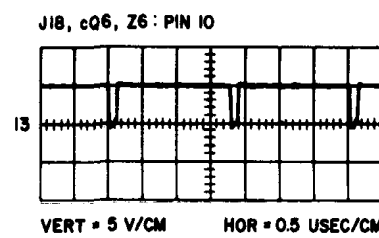
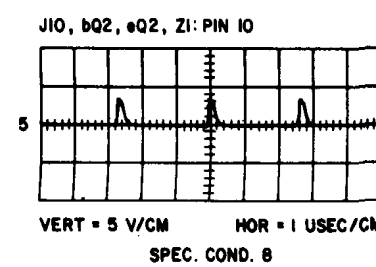
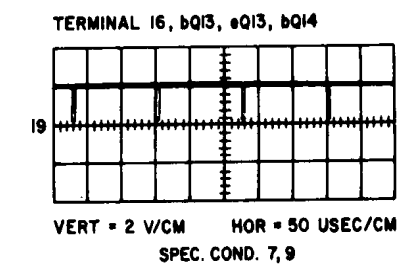
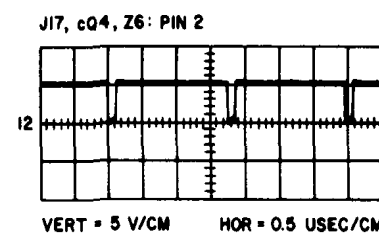
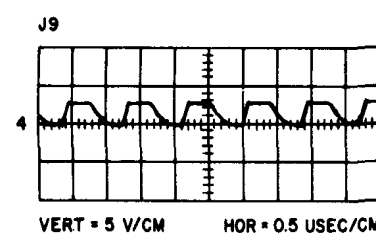
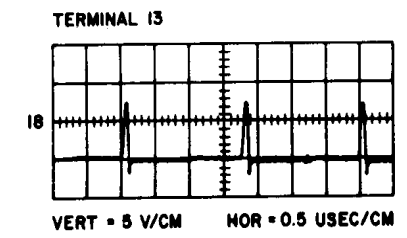
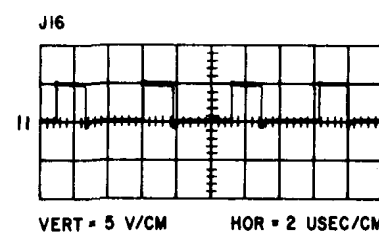
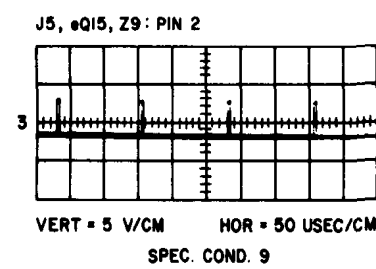
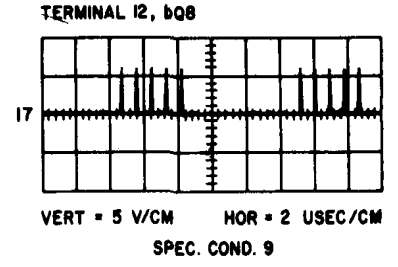
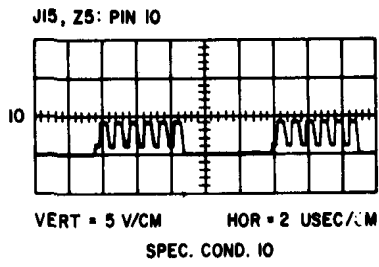
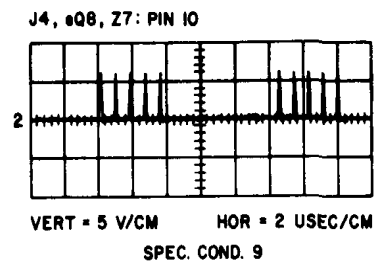
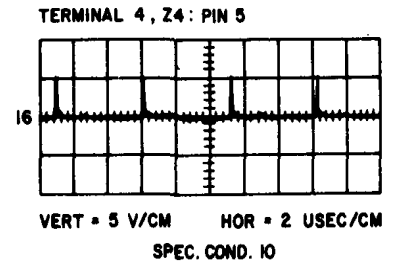
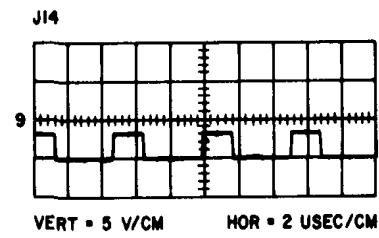
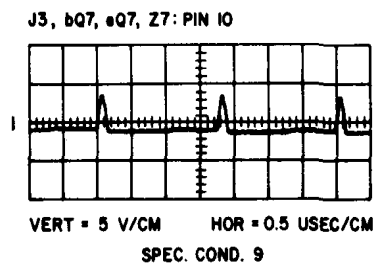
7. TERMINAL 15 TERMINATED IN 91-OHM LOAD.
8. TERMINAL 18 TERMINATED IN 91-OHM LOAD.
9. SERV SEL SWITCH AT A; METER SELECT SWITCH AT SERV FAC.
10. SERV SEL SWITCH AT C; METER SELECT SWITCH AT SERV FAC.
11. SERV SEL SWITCH AT D; METER SELECT SWITCH AT SERV FAC.
12. SERV SEL SWITCH AT B; METER SELECT SWITCH AT SERV FAC.

Figure 6-84. Panel 1A17, troubleshooting waveforms.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE 1/2 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING

Figure 6-85. Panel 2A17, schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL

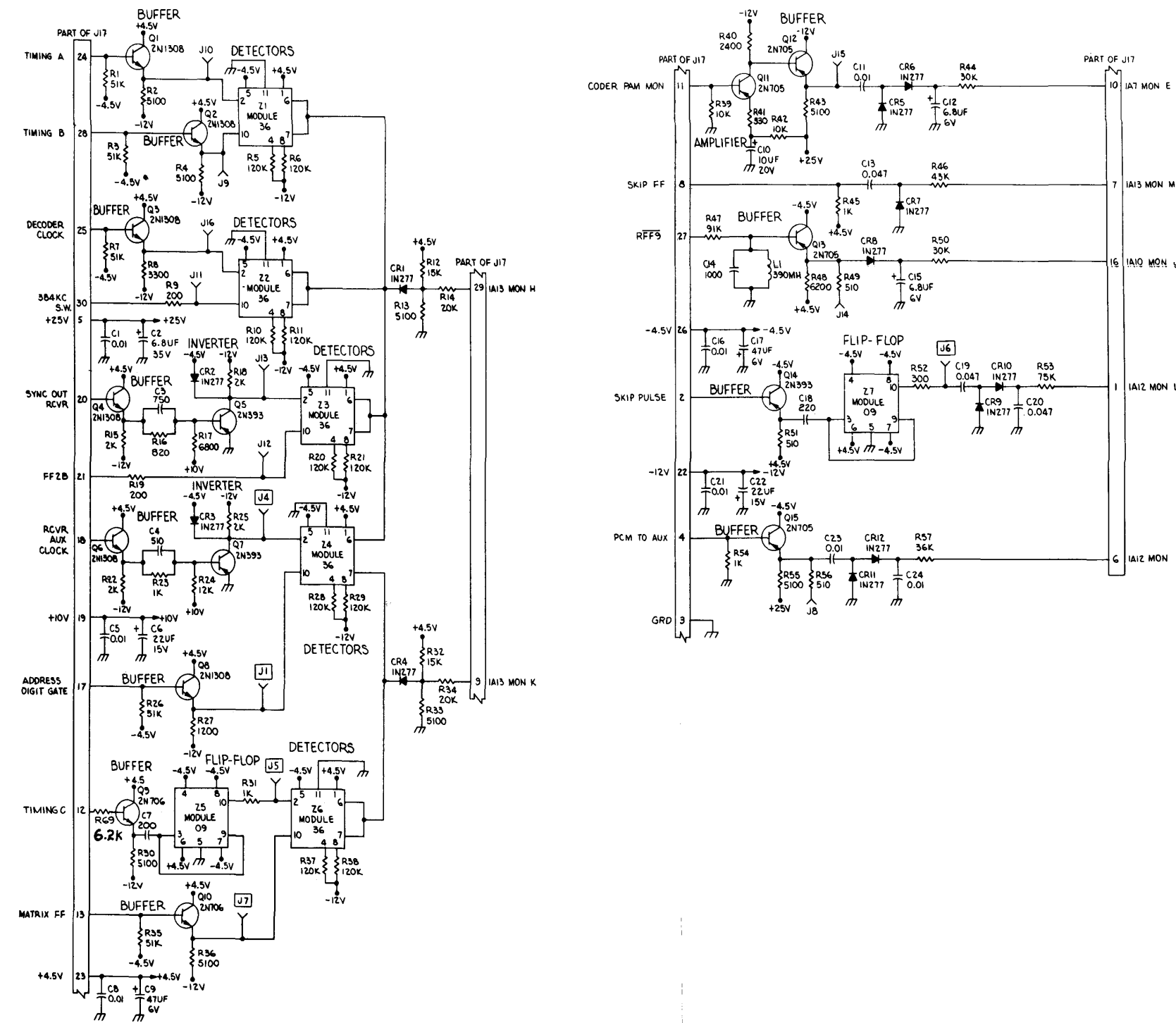
THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

B. SPECIAL

7. TERMINAL 16 TERMINATED IN 91-OHM LOAD.
8. SERV SEL SWITCH AT A; METER SELECT SWITCH AT SERV FAC.
9. SERV SEL SWITCH AT D; METER SELECT SWITCH AT SERV FAC.
10. SERV SEL SWITCH AT C; METER SELECT SWITCH AT SERV FAC.

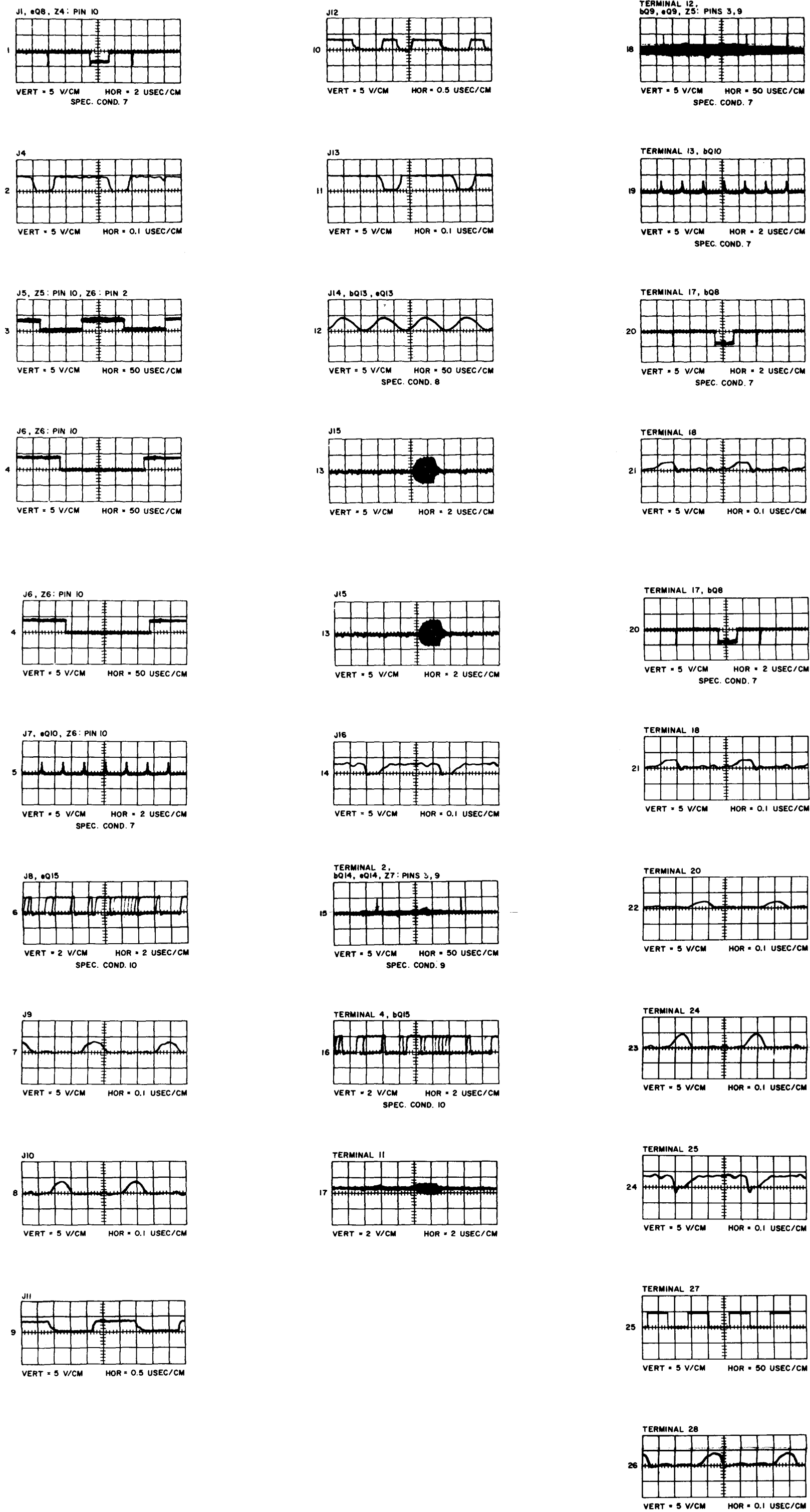
Figure 6-86. Panel 2A17, troubleshooting waveforms.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

TM5805-367-35/3-118

Figure 6-87. PANEL 1A18. Schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

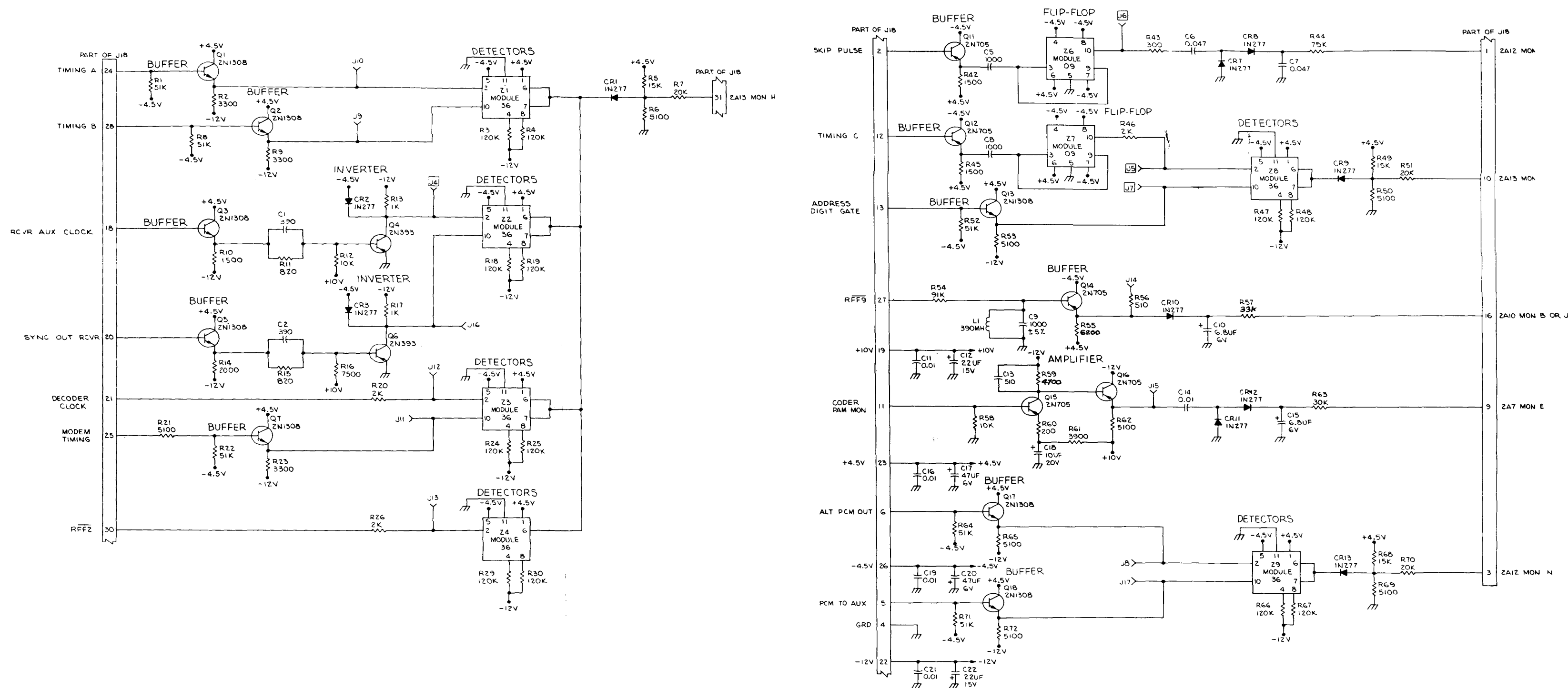
THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

B. SPECIAL.

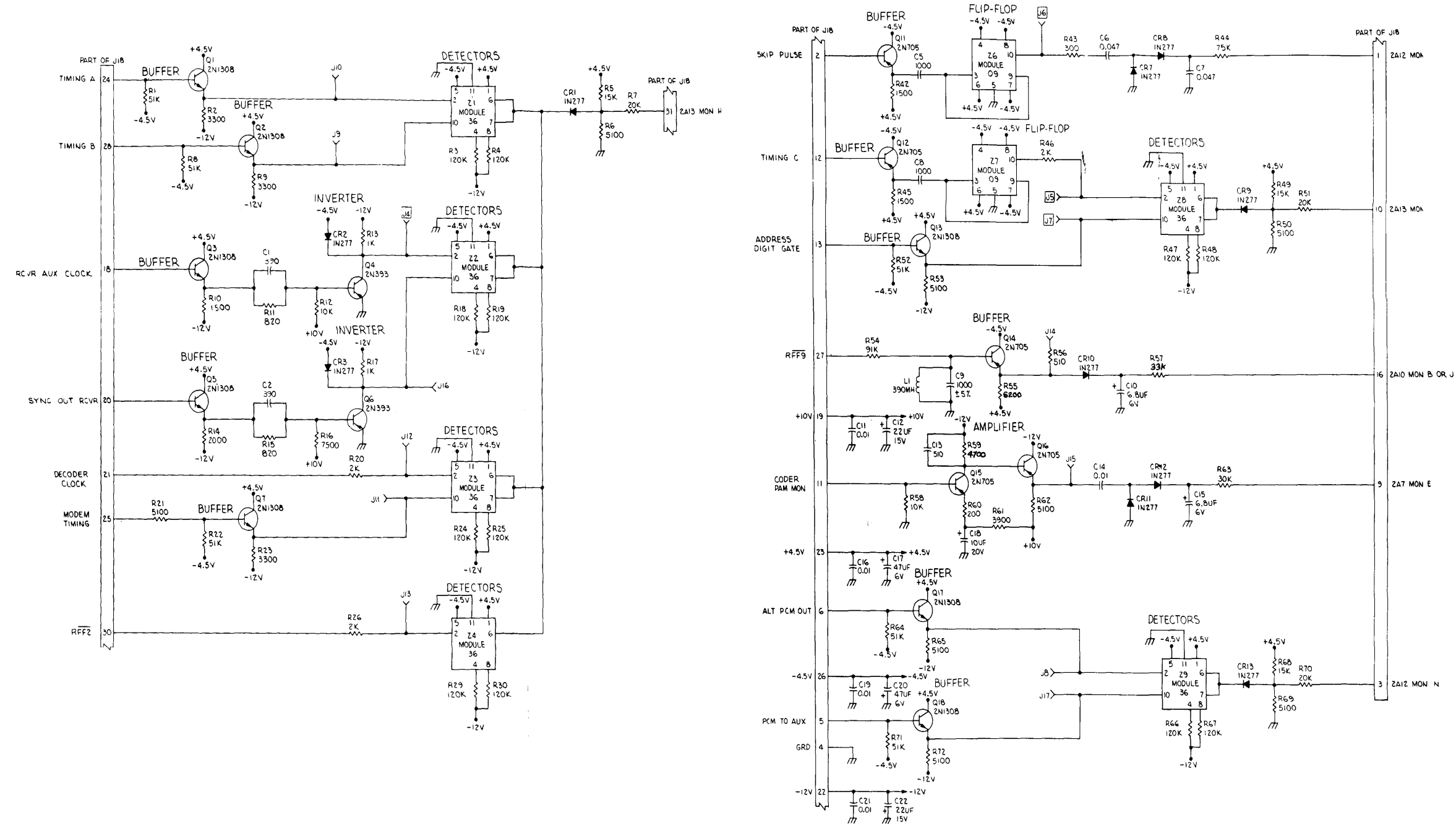
7. SERV SEL SWITCH AT K; METER SELECT SWITCH AT SERV FAC.
8. SERV SEL SWITCH AT J; METER SELECT SWITCH AT SERV FAC.
9. SERV SEL SWITCH AT L; METER SELECT SWITCH AT SERV FAC.
10. SERV SEL SWITCH AT N; METER SELECT SWITCH AT SERV FAC.

Figure 6-88. Panel 1A18, troubleshooting waveform.



- NOTES:
- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
 - UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 - UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/2-WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 - ☐ INDICATES EQUIPMENT MARKING

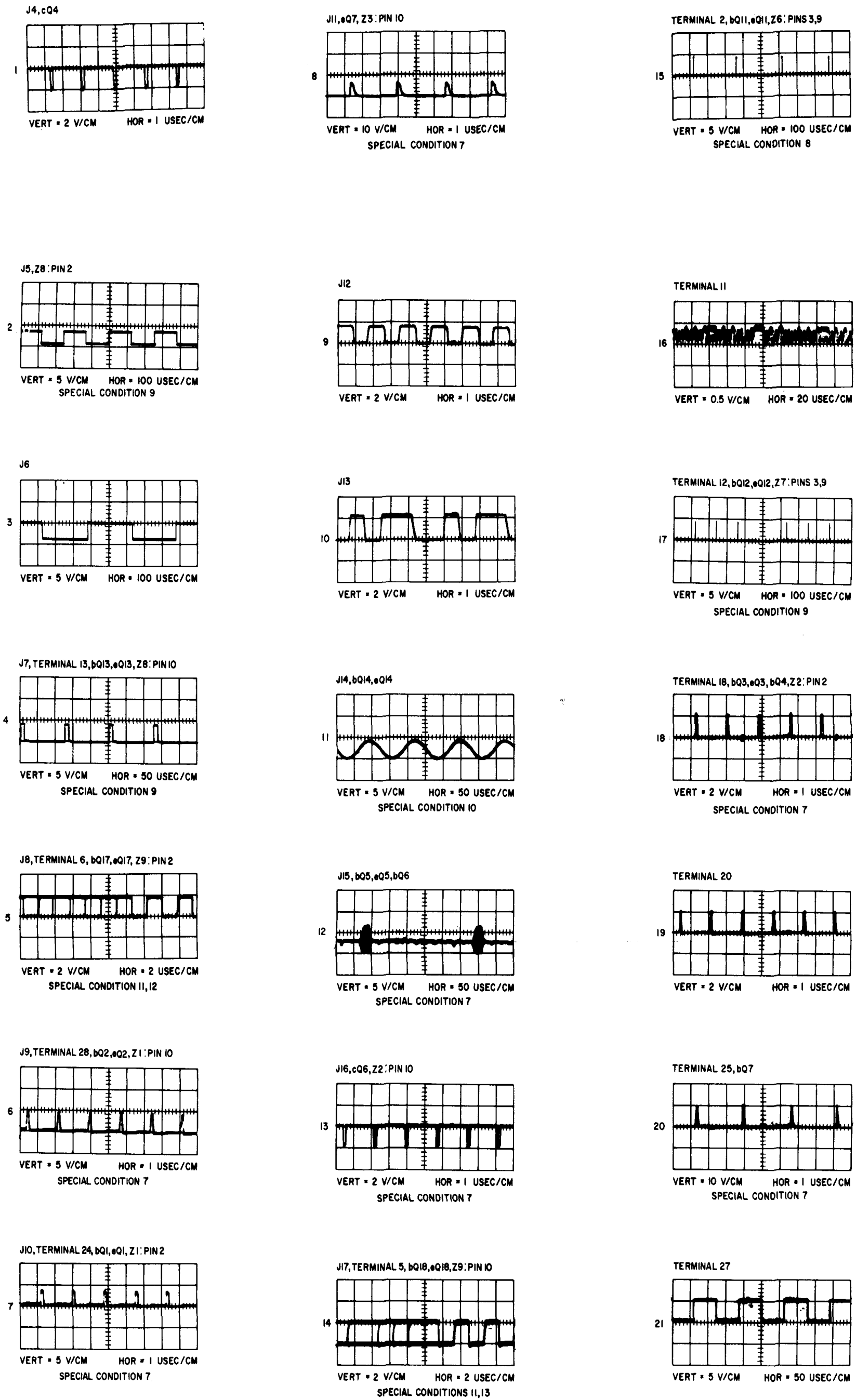
Figure 6-89. Panel 2A18, schematic diagram.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS.
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS.
 4. □ INDICATES EQUIPMENT MARKING.

TM5805-367-35/3-121

Figure 6-89. Panel 2A18, schematic diagram.



CONDITIONS FOR OBTAINING WAVEFORM PRESENTATIONS

A. GENERAL.

THE FOLLOWING CONDITIONS ARE APPLICABLE TO ALL WAVEFORMS SHOWN ON THIS ILLUSTRATION. CHECK ALSO ANY NUMBERED KEY REFERENCES GIVEN WITH THE WAVEFORM. THESE REFERENCES PERTAIN TO SPECIAL CONDITIONS LISTED BELOW AND WHICH ARE ALSO REQUIRED TO OBTAIN THE WAVEFORM SHOWN.

1. TEST MULTIPLEXER CONNECTED FOR LOOP-BACK OPERATION.
2. ONE CHANNEL MODULATED USING INTERNAL 1100 CPS TEST TONE.
3. OSCILLOSCOPE SYNCHRONIZED FROM SCOPE SYNC OUTPUT OF TEST MULTIPLEXER.
4. ADDRESS SWITCH AT MASTER.
5. AUX SWITCH AT OUT.
6. 2 WIRE-4 WIRE SWITCH AT 4 WIRE.

B. SPECIAL.

7. SERV SEL SWITCH AT H; METER SELECT SWITCH AT SERV FAC.
8. SERV SEL SWITCH AT L; METER SELECT SWITCH AT SERV FAC. PCM IN CONNECTOR REMOVED (UNIT OUT OF FRAME).
9. SERV SEL SWITCH AT K; METER SELECT SWITCH AT SERV FAC.
10. SERV SEL SWITCH AT J; METER SELECT SWITCH AT SERV FAC.
11. SERV SEL SWITCH AT N; METER SELECT SWITCH AT SERV FAC.
12. TERMINAL 6 TERMINATED IN 91-OHM LOAD.
13. TERMINAL 5 TERMINATED IN 91-OHM LOAD.

Figure 6-90. Panel 2A18, troubleshooting waveforms.

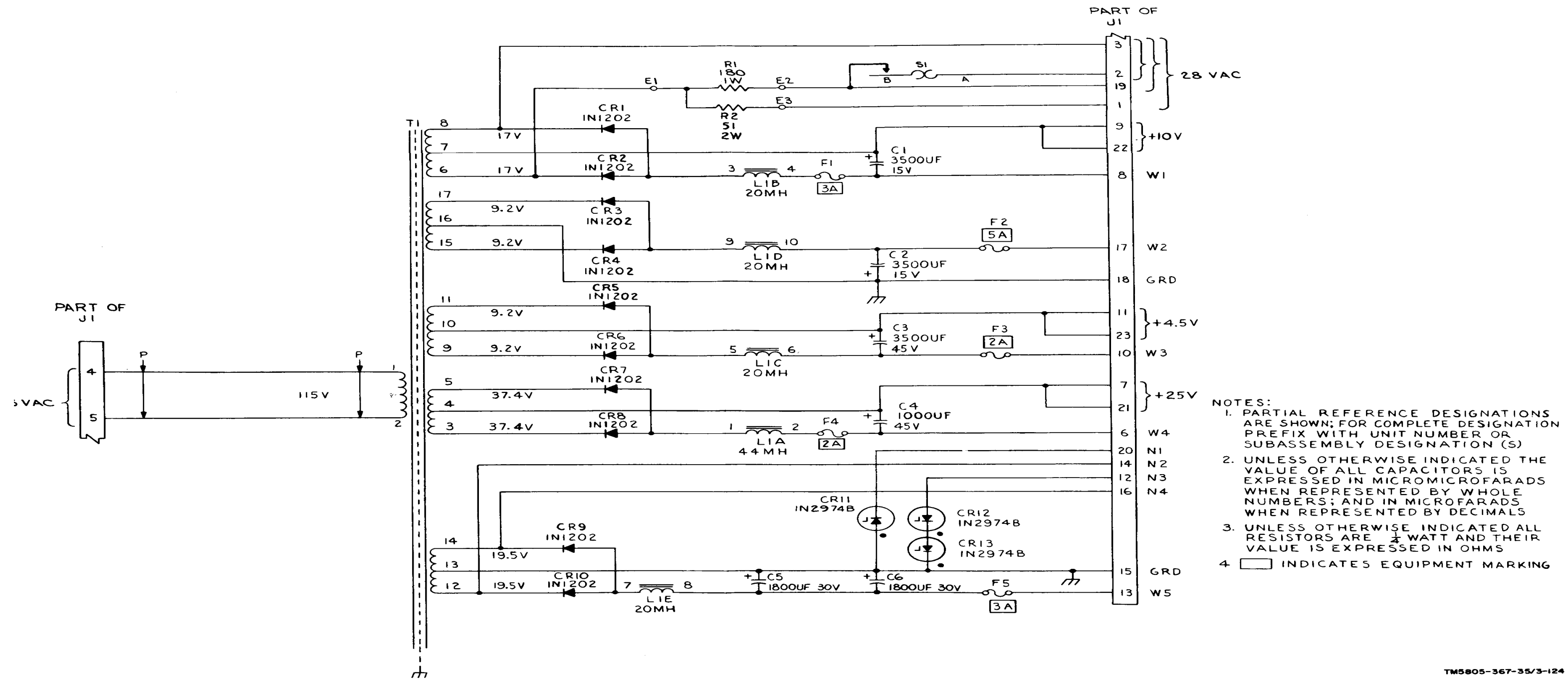
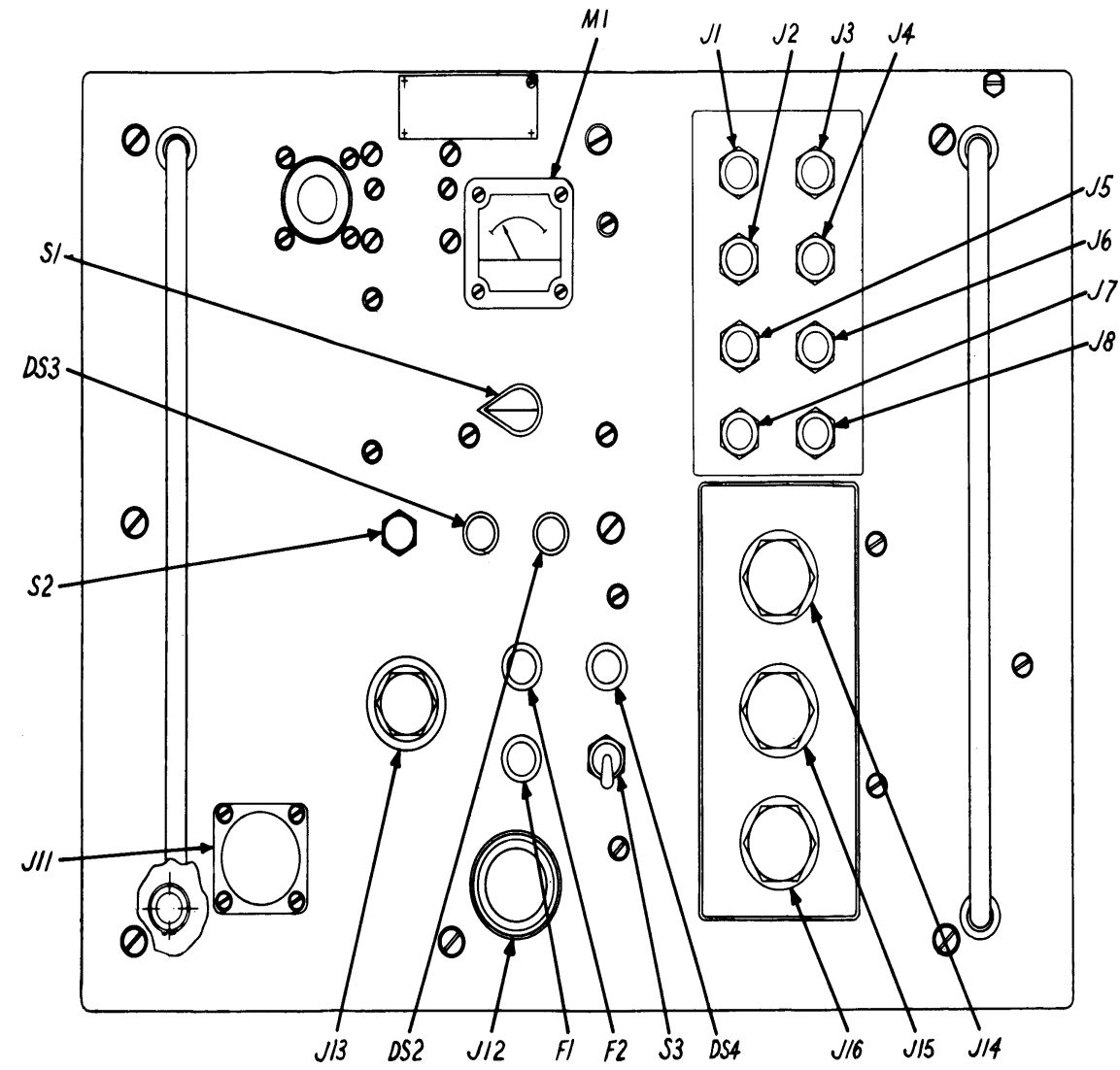
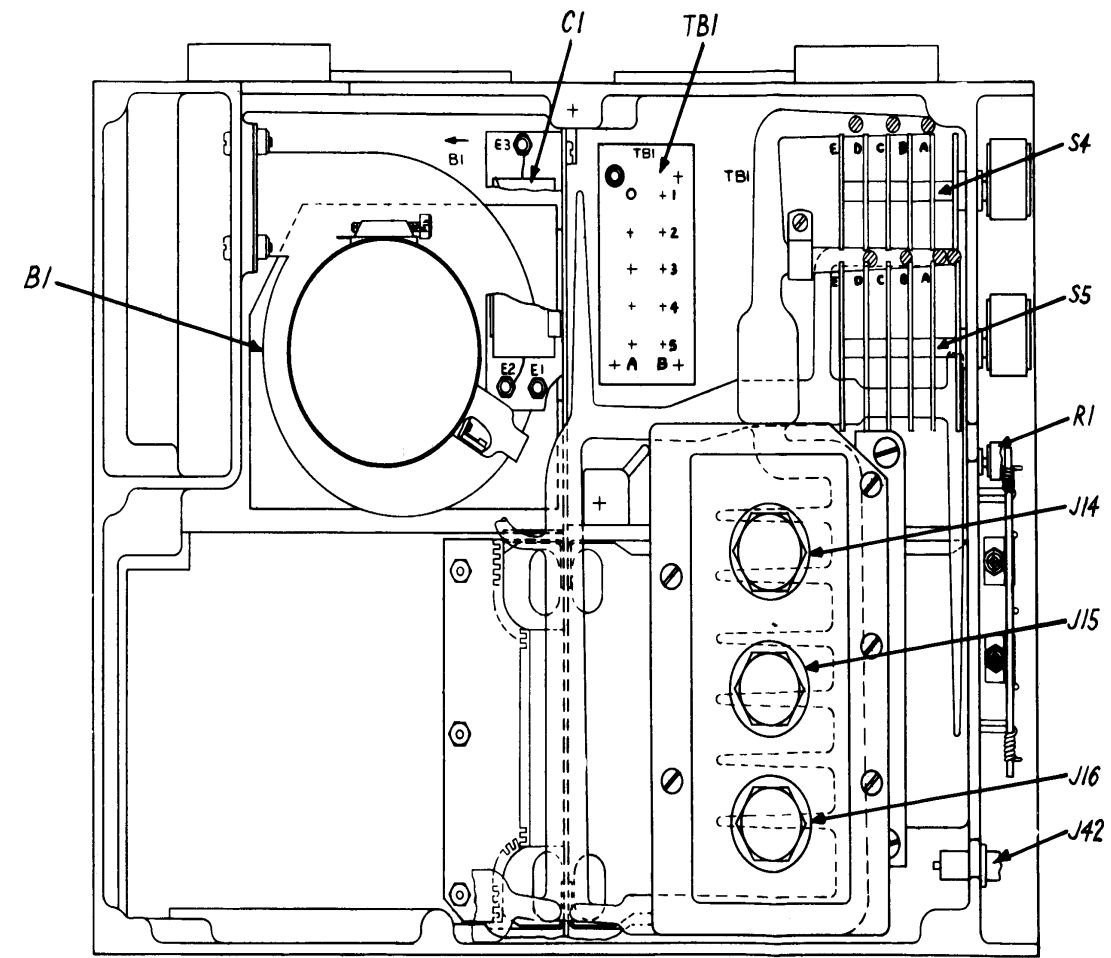


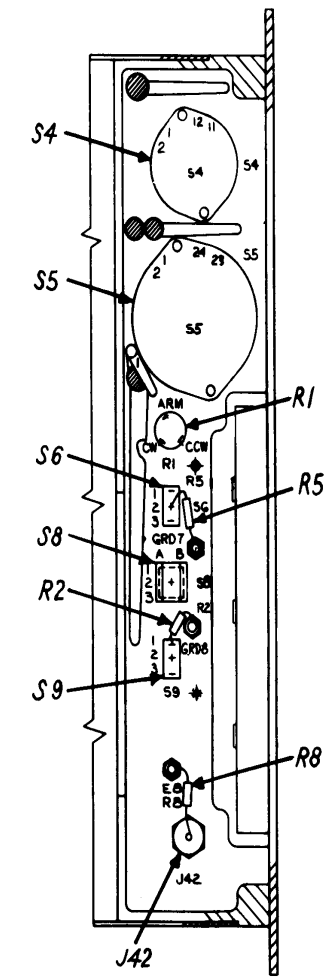
Figure 6-91. Panel 1A19/2A19, schematic diagram.



FRONT PANEL

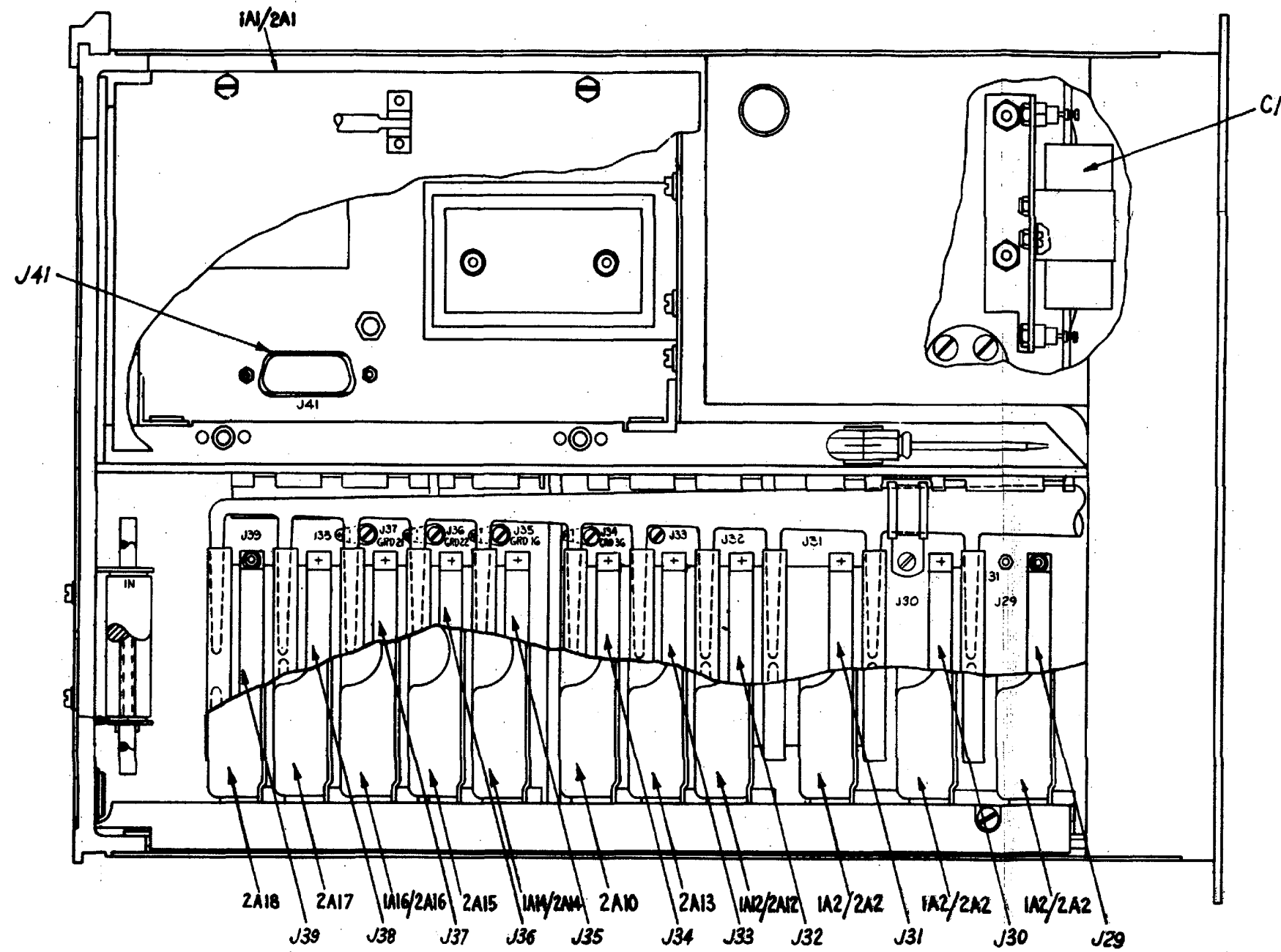


FRONT OF CHASSIS
(FRONT PANEL REMOVED)

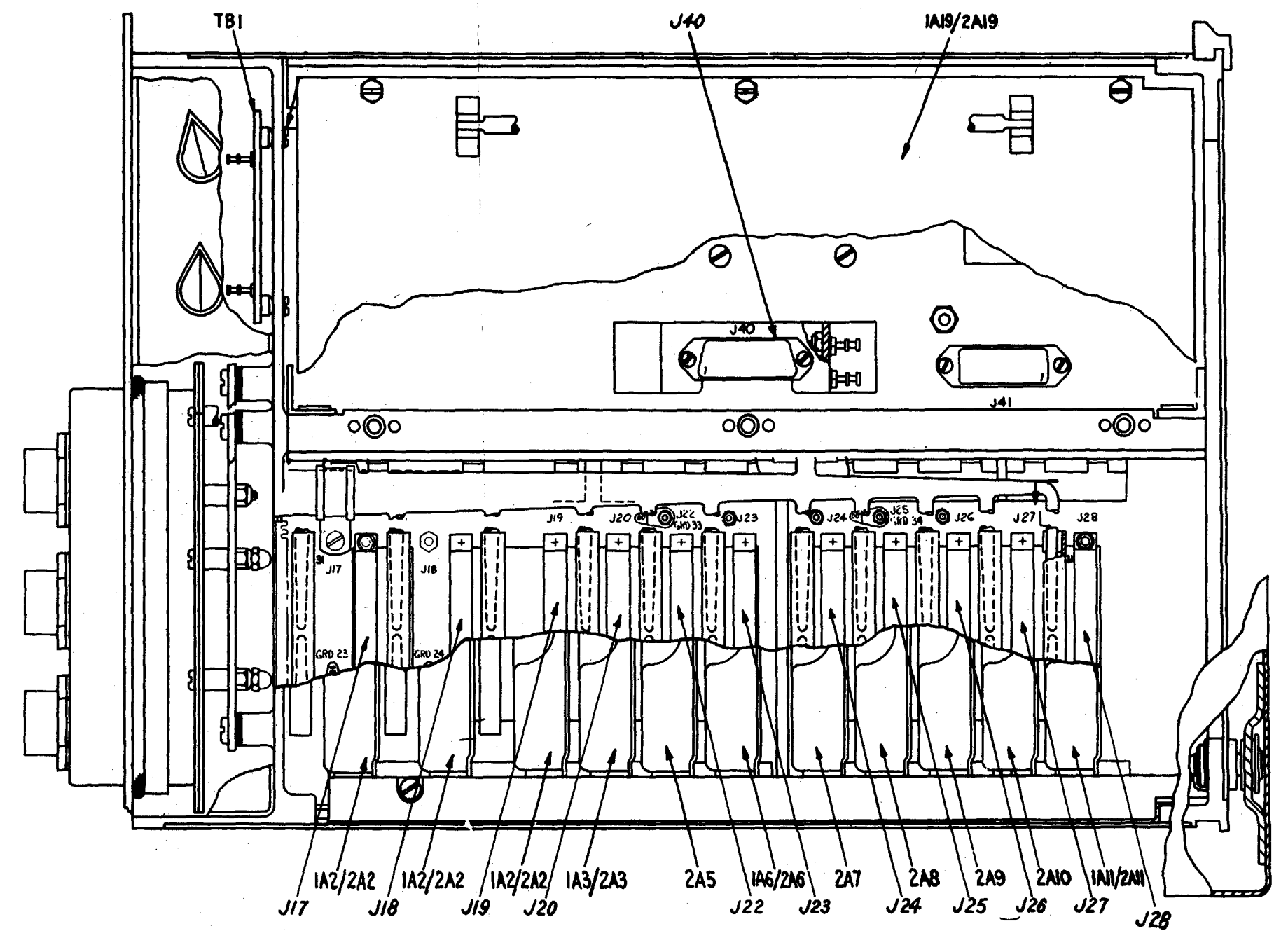


RIGHT SIDE PANEL
(REAR VIEW)
TM5805-367-35/3-130 ①

Figure 6-92①. Multiplexer TD-352/U, location of parts (part 1 of 3).
Panel 1A18, schematic diagram.



LEFT SIDE OF CHASSIS



RIGHT SIDE OF CHASSIS

TM5805-367-35/3-130 (2)

Figure 6-92②. Multiplexer TD-352/U, location of parts (part 2 of 3).

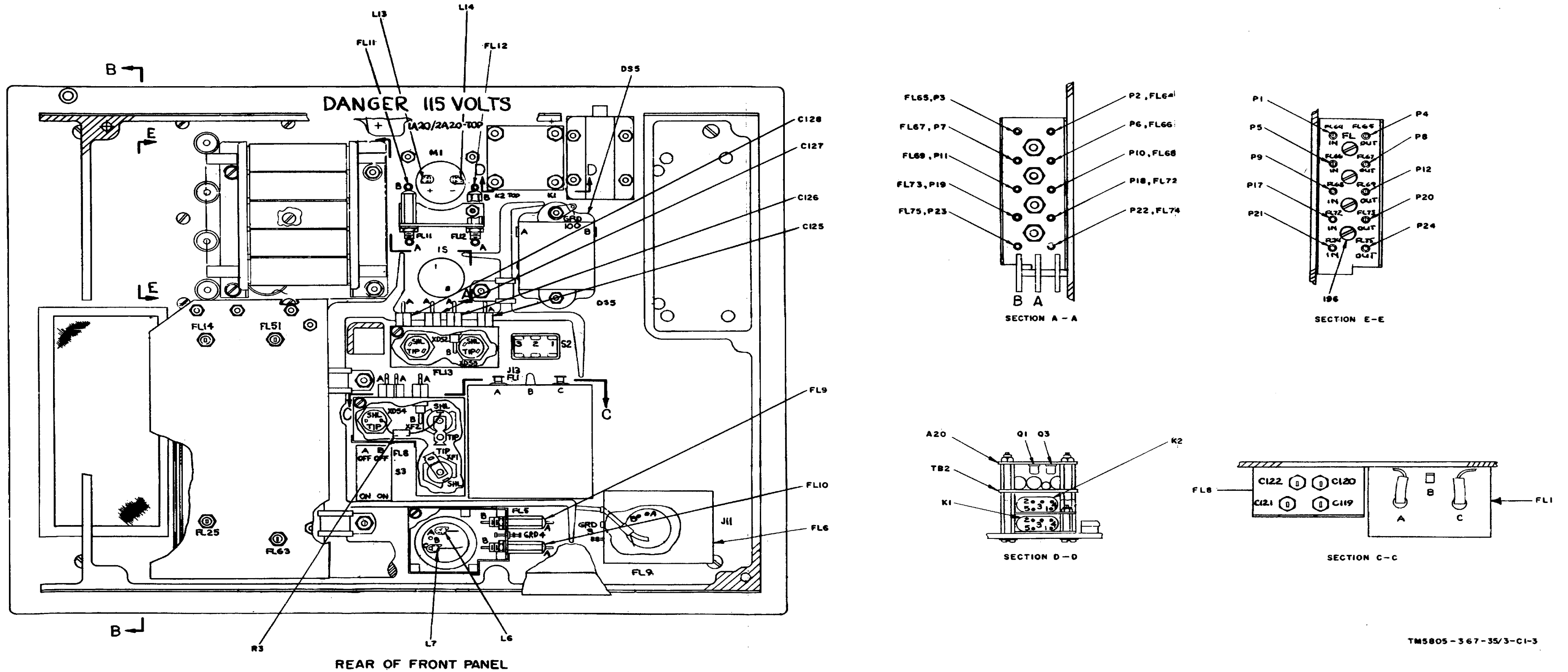


Figure 6-92. Multiplexer TD-352/U, location or parts (part 3 of 3).

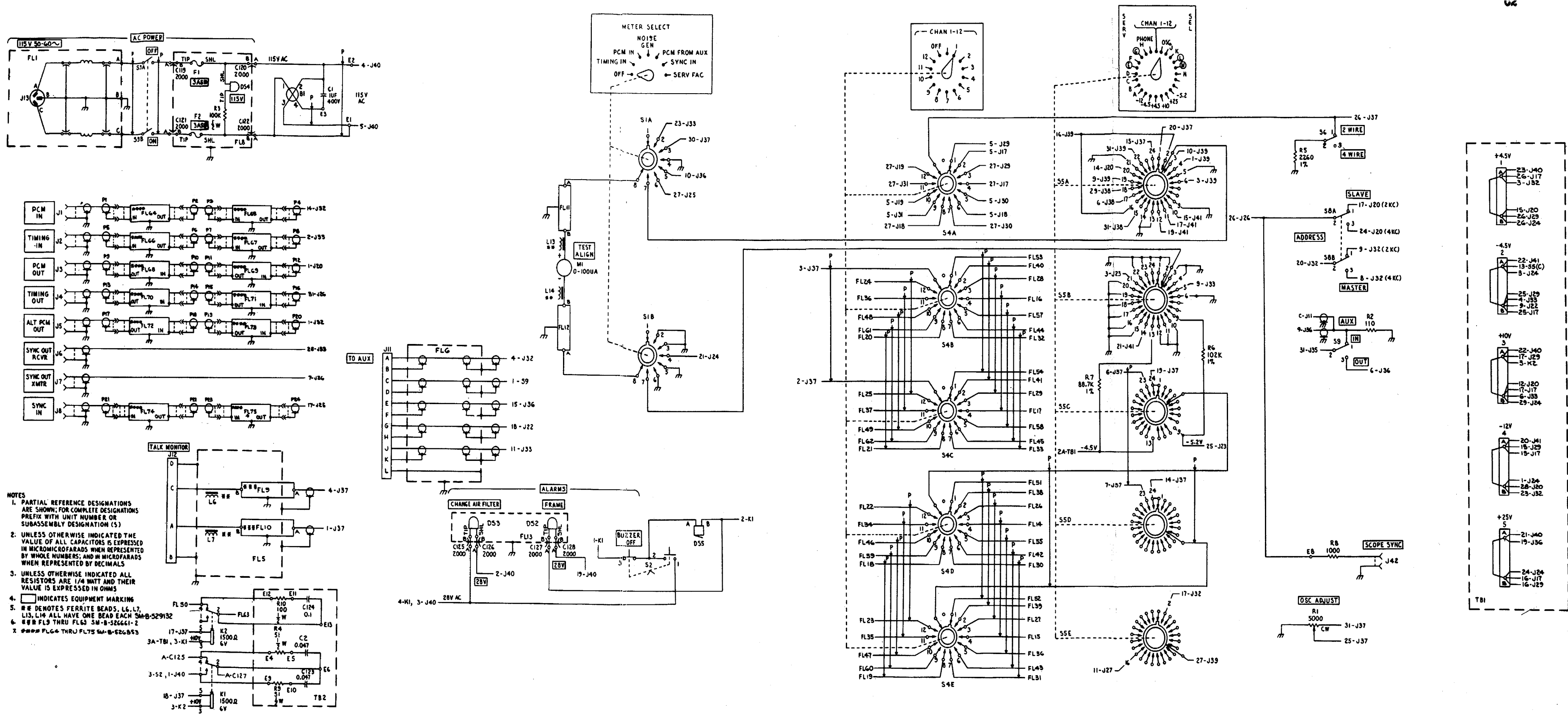


Figure 6-93①. Multiplexer TD-352/U, schematic diagram (part 1 of 3).

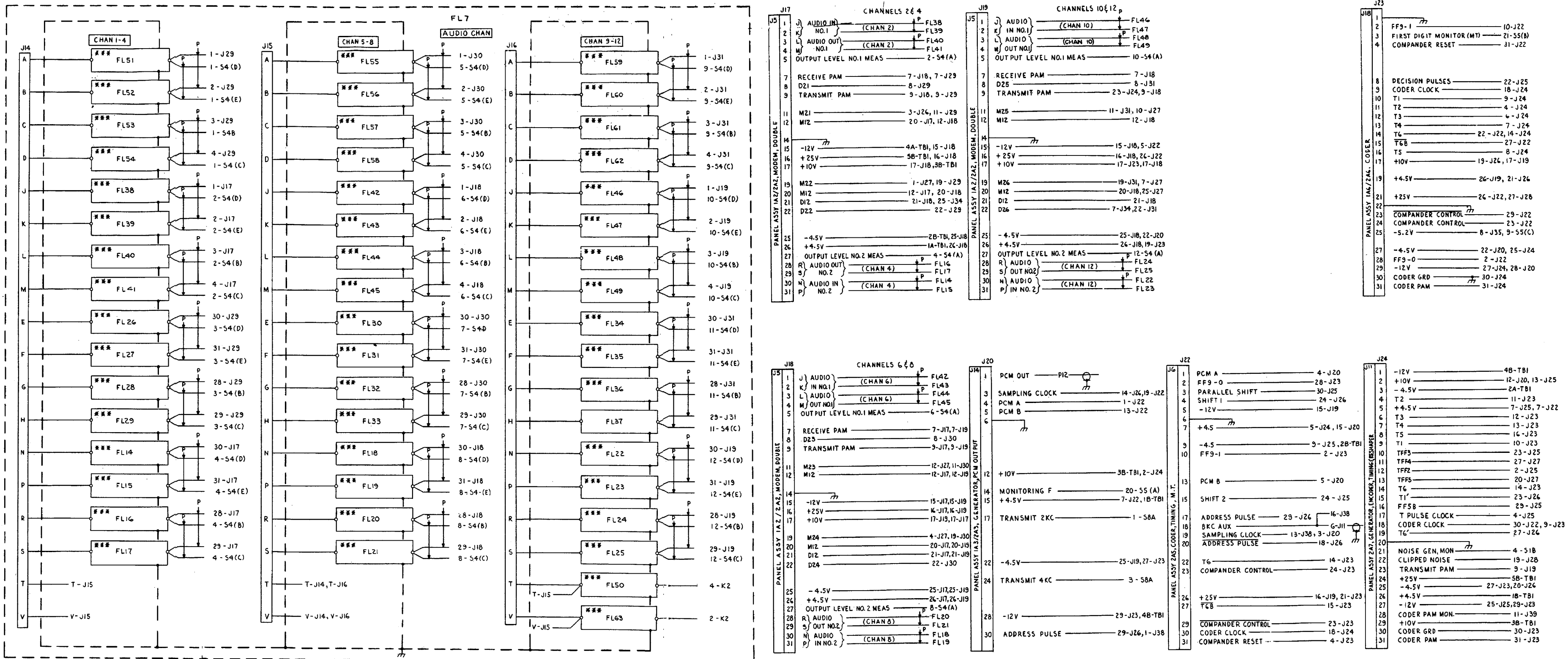


Figure 6-93. Multiplexer TD-352/U, schematic diagram (part 2 of 3).

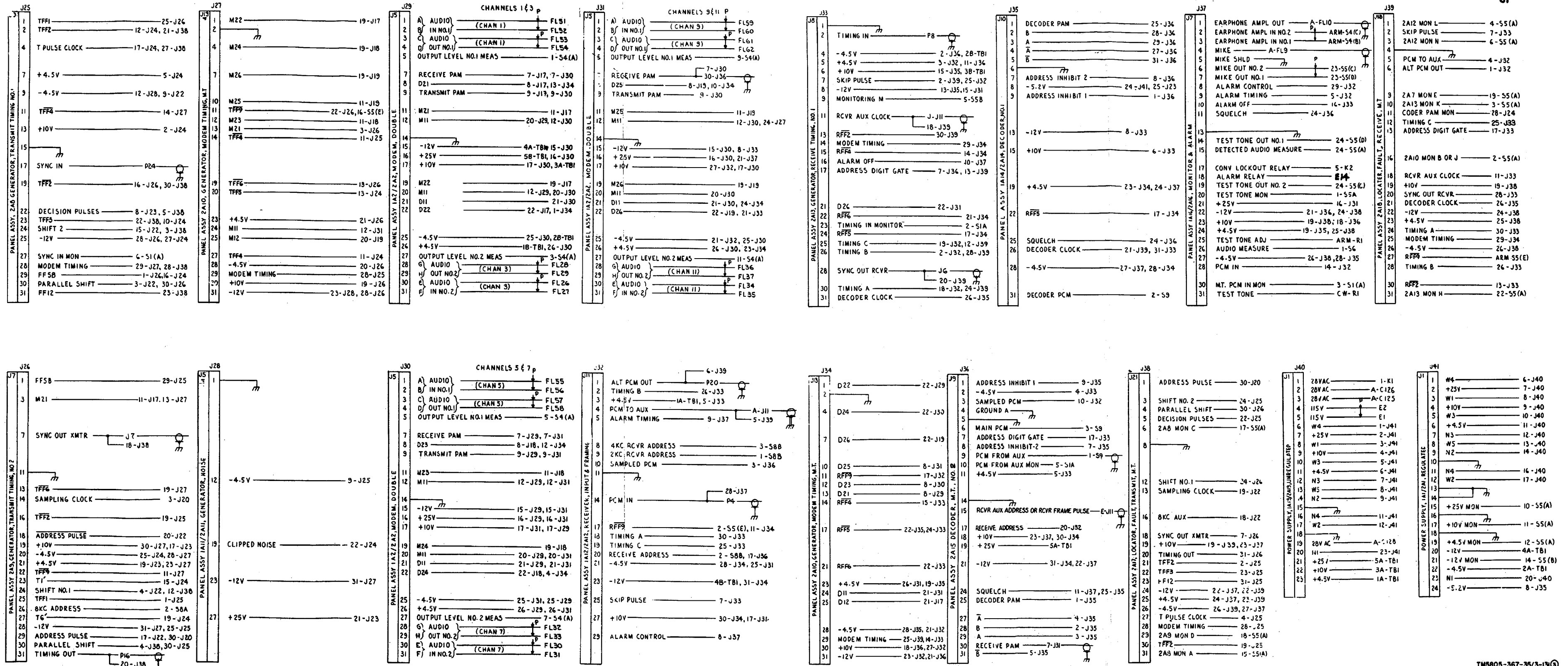


Figure 6-93. Multiplexer TD-352/U, schematic diagram (part 3 of 3).

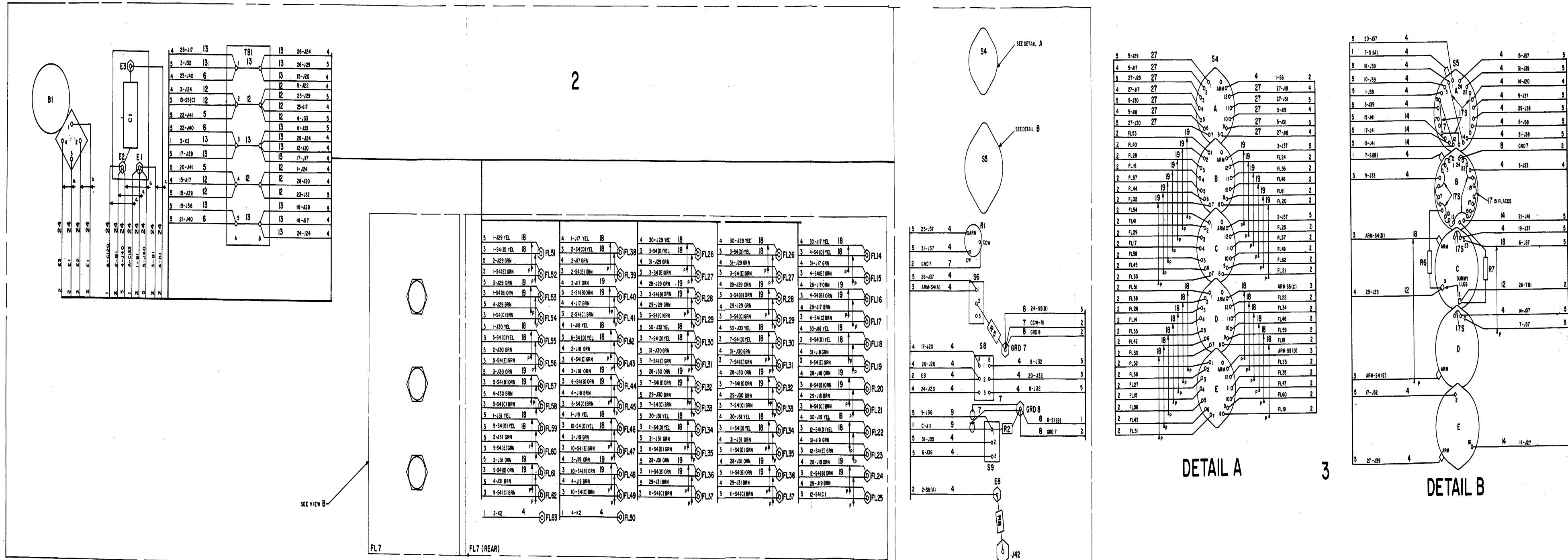
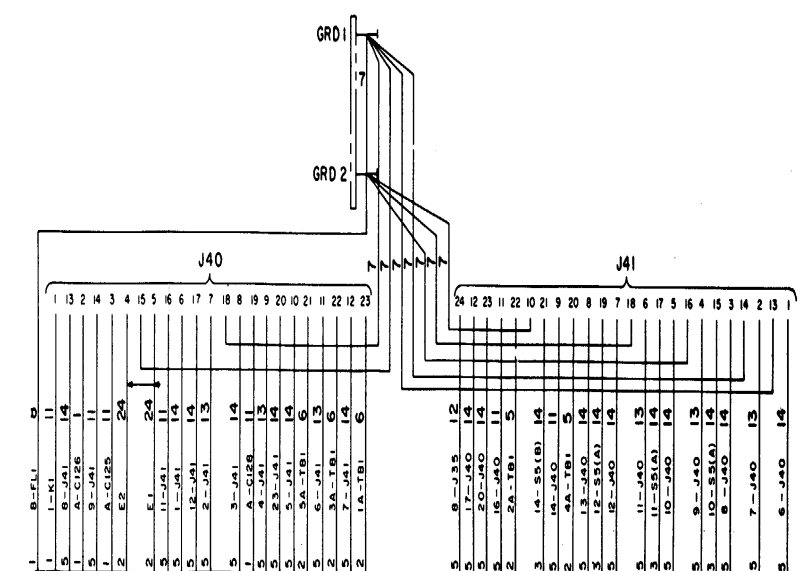
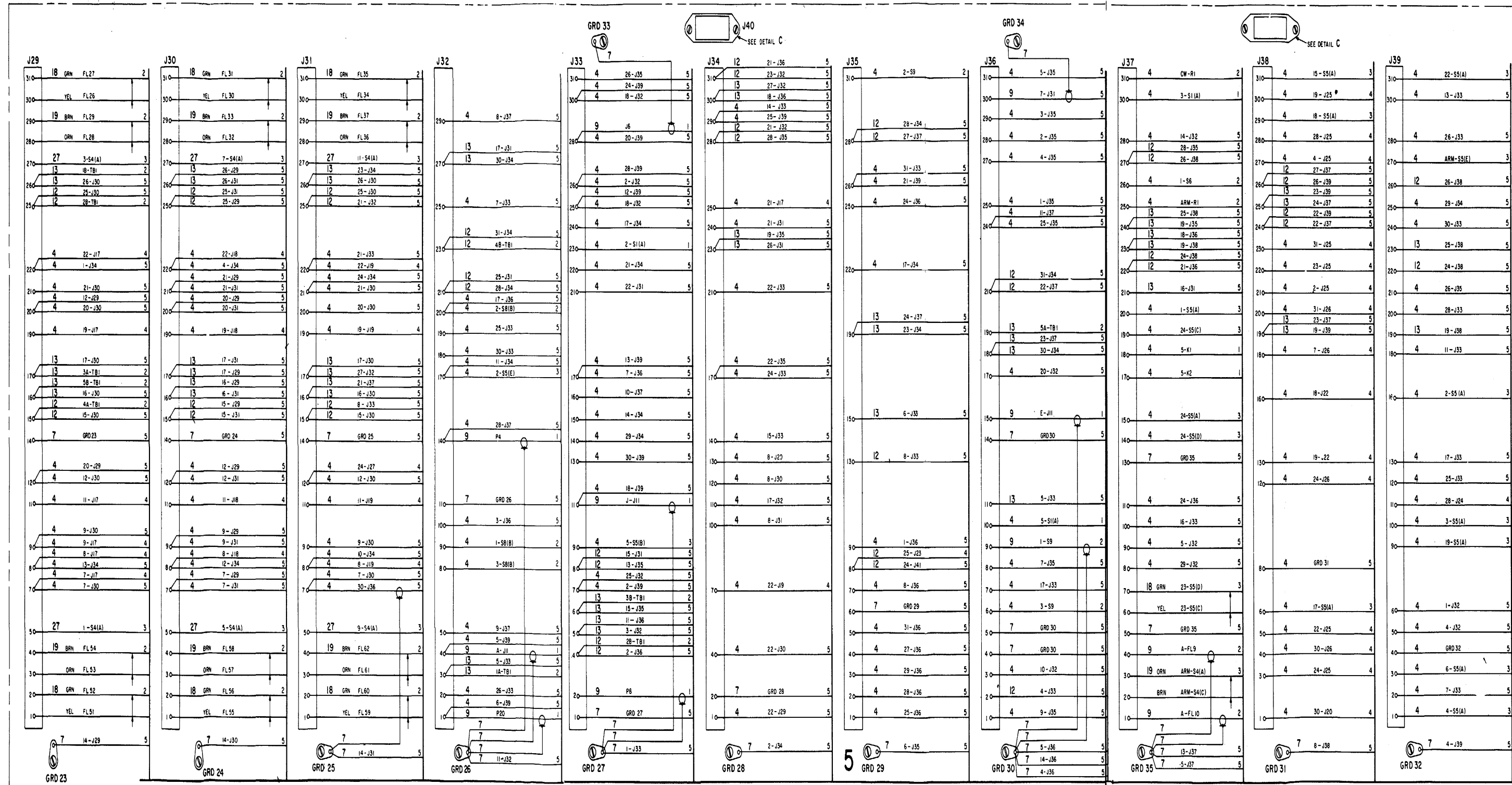


Figure 6-94. Multiplexer TD-352/U, wiring diagram (part 2 of 4).



DETAIL C

RIGHT SIDE VIEW

Figure 6-94. Multiplexer TD-352/U, wiring diagram (part 4 of 4).

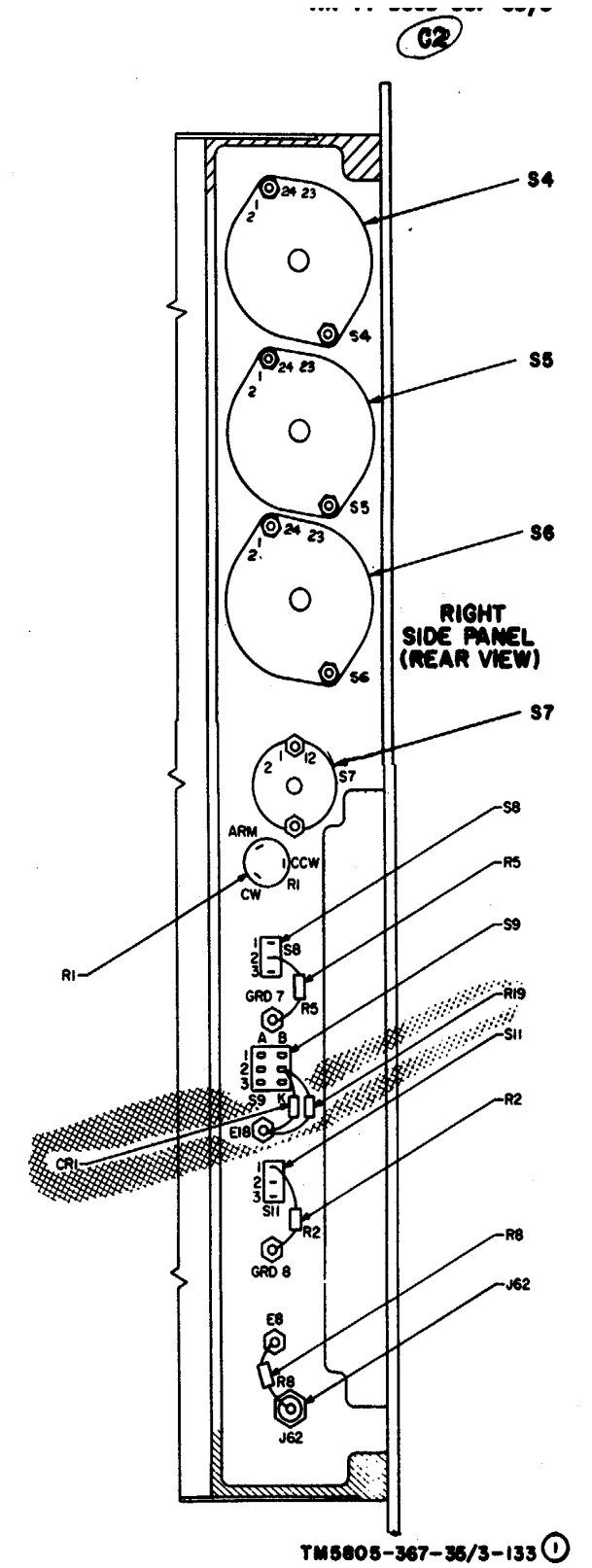
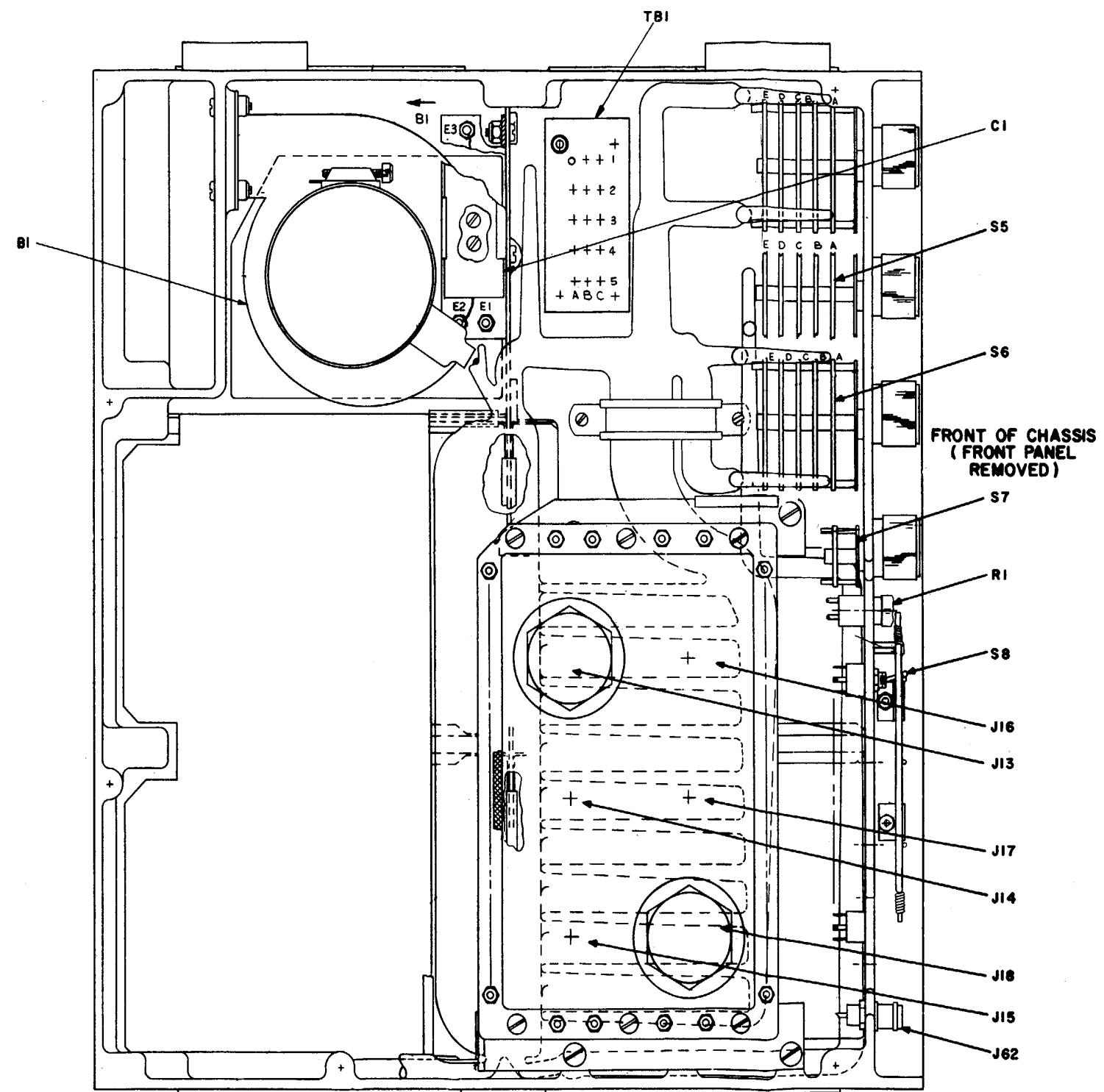
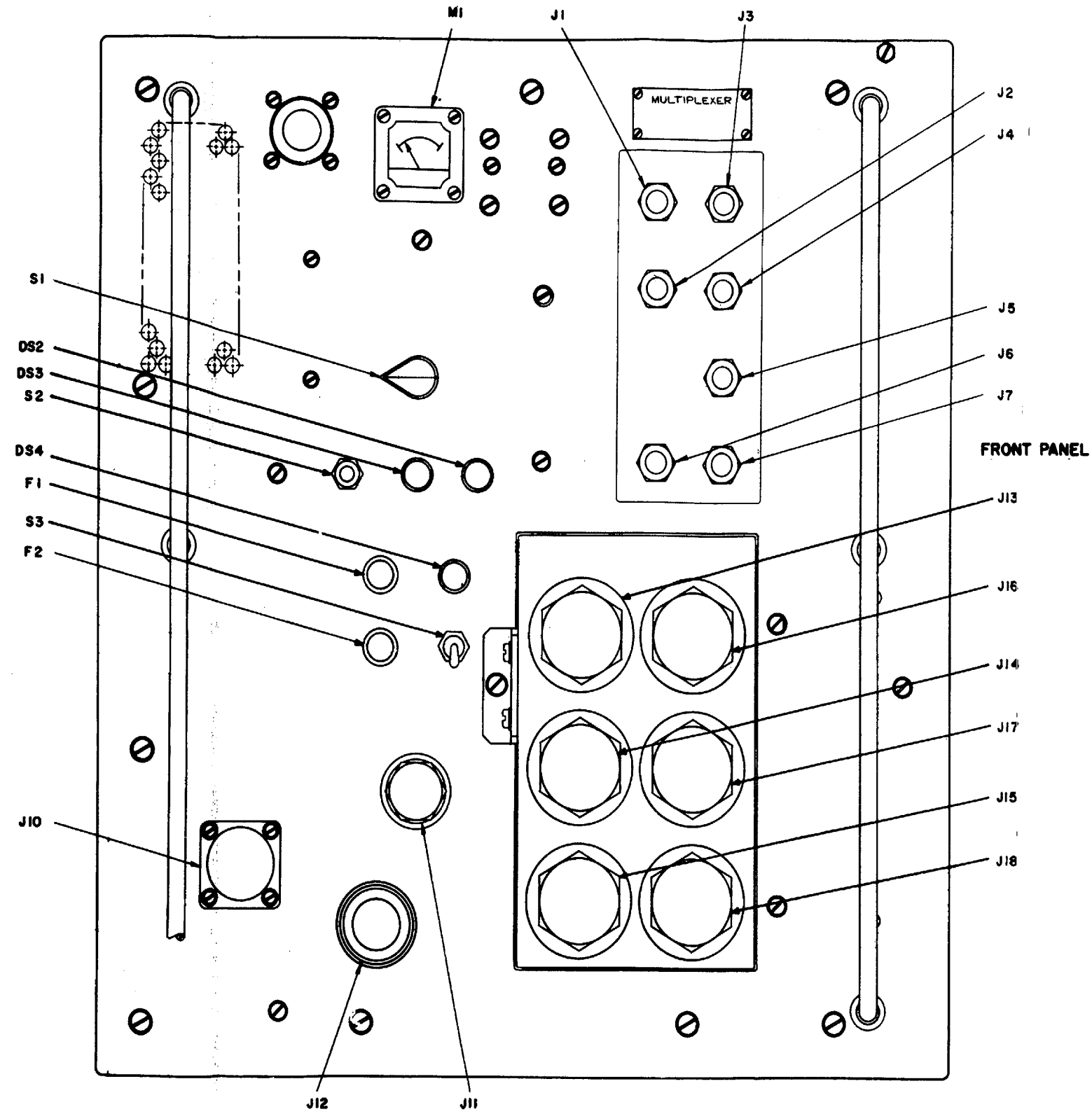
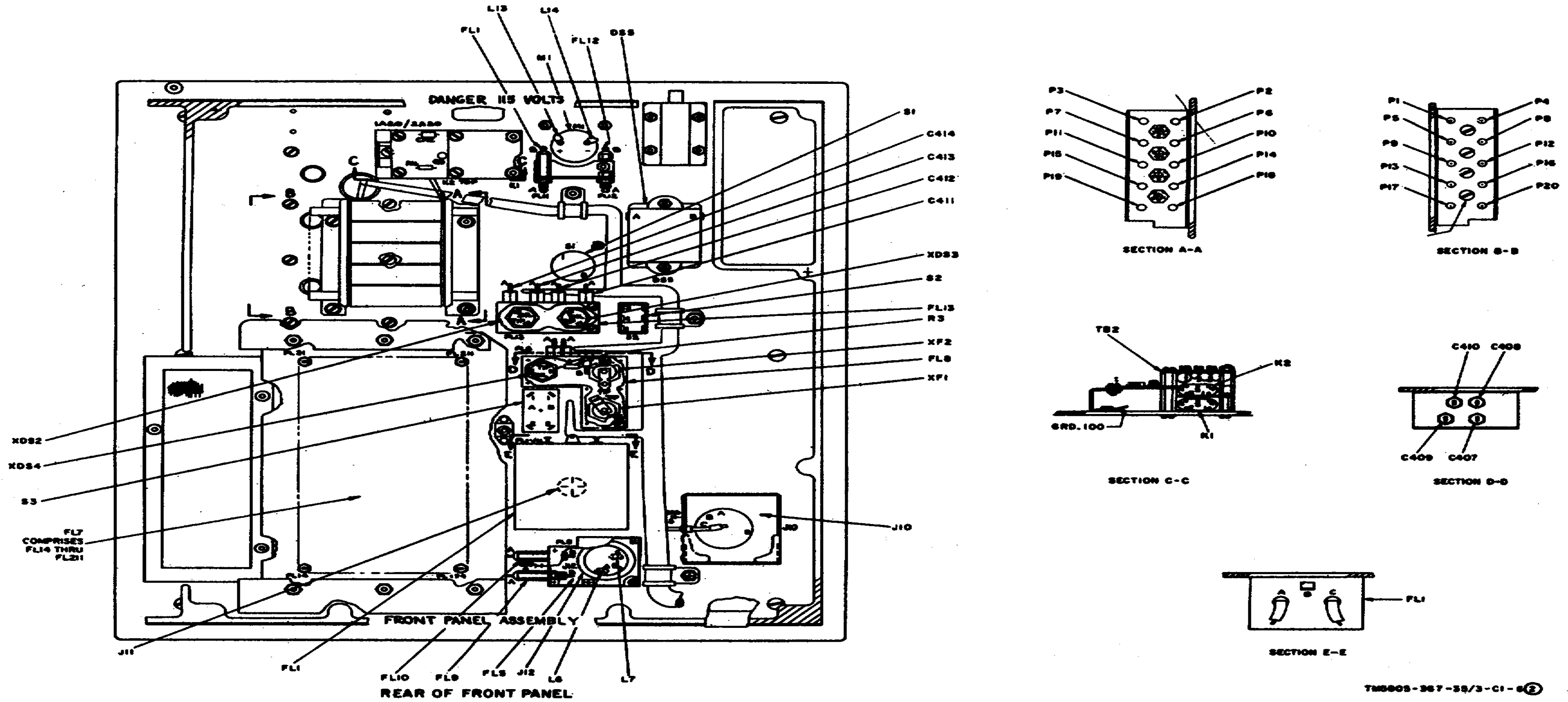
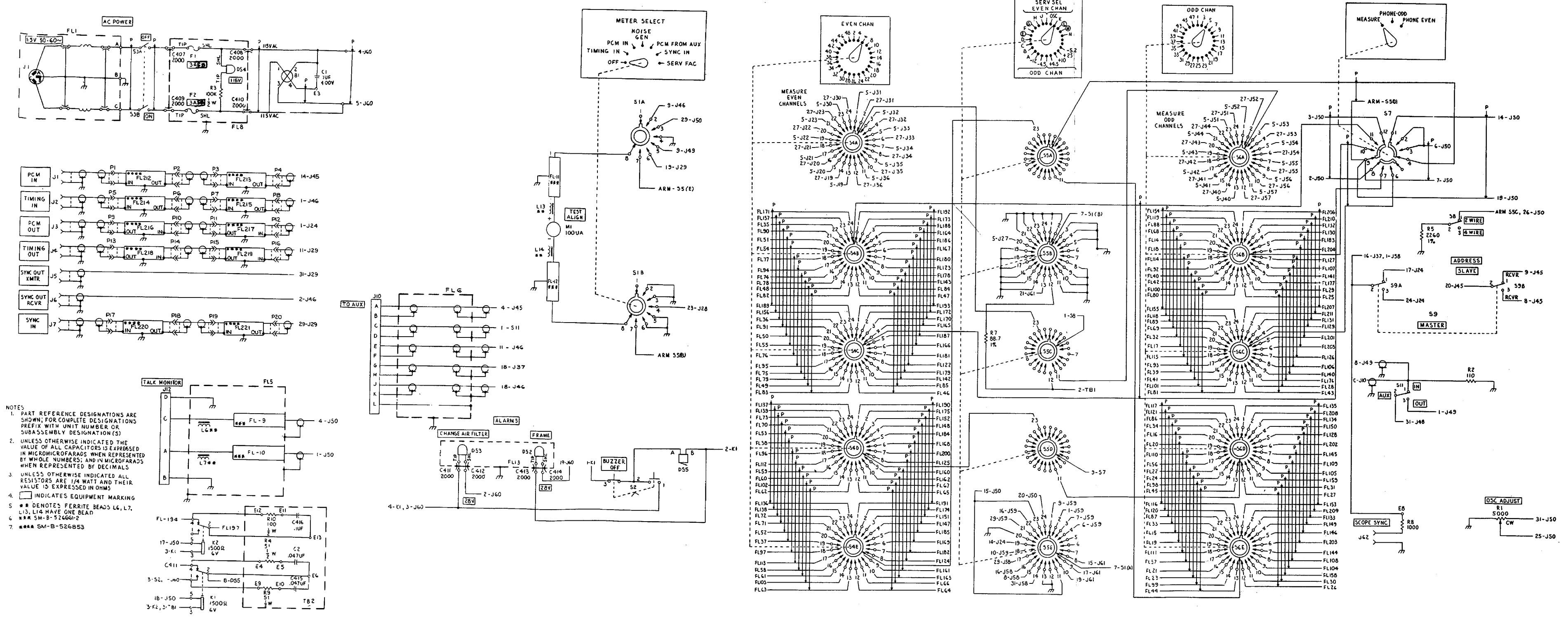


Figure 6-95①. Multiplexer TD-353/U, location of parts (part 1 of 3).



TM 11-5805-367-35/3-C1-62

Figure 6-95②. Multiplexer TD-353/U, location of parts (part 2 of 3).



- NOTES
1. PART REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS; AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING
 5. ****** DENOTES FERRITE BEADS L6, L7, L13, L14 HAVE ONE BEAD
 6. ******* SM-B-526661-2
 7. ******** SM-B-526653

Figure 6-96 ①. Multiplexer TD-353/U, schematic diagram (part 1 of 5).

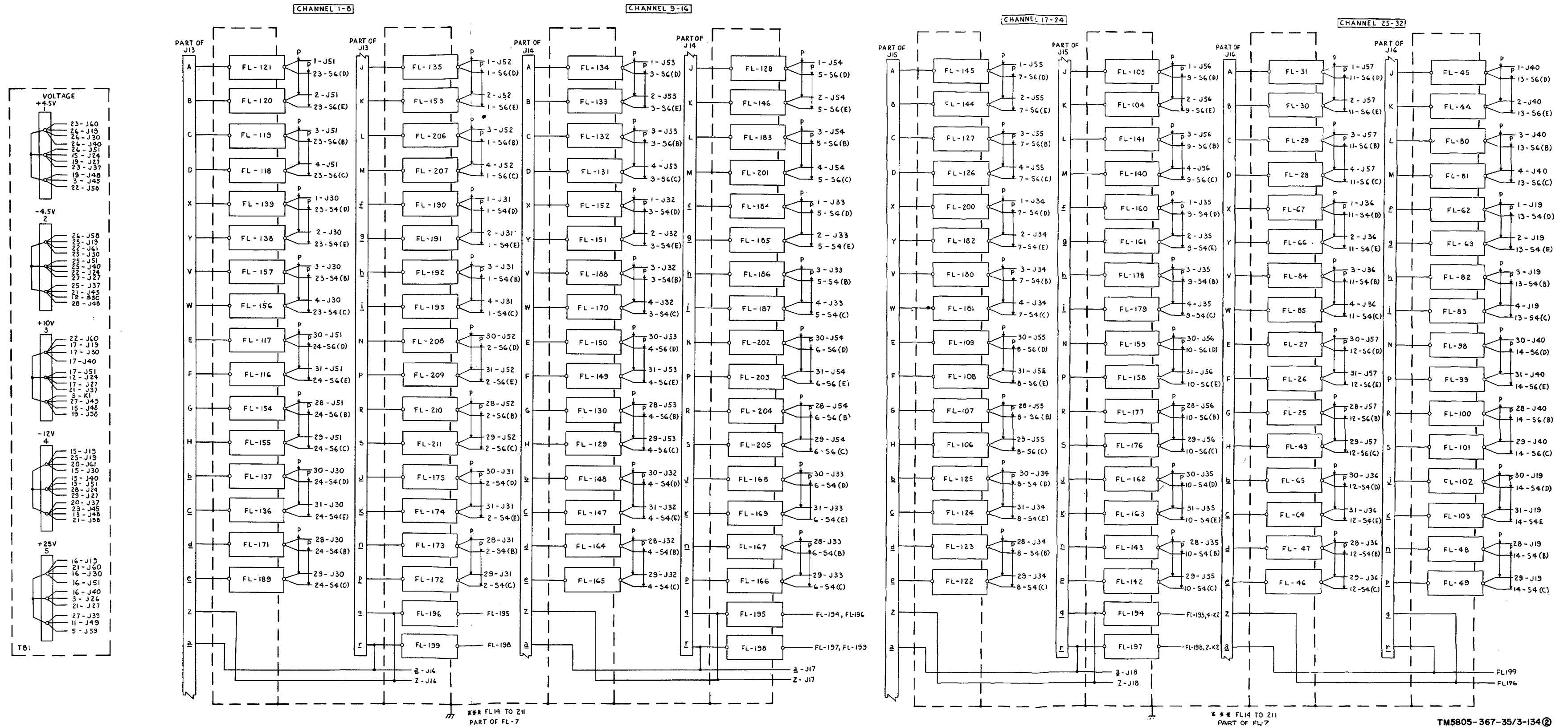


Figure 6-96 ②. Multiplexer TD-353/U, schematic diagram (part 2 of 5).

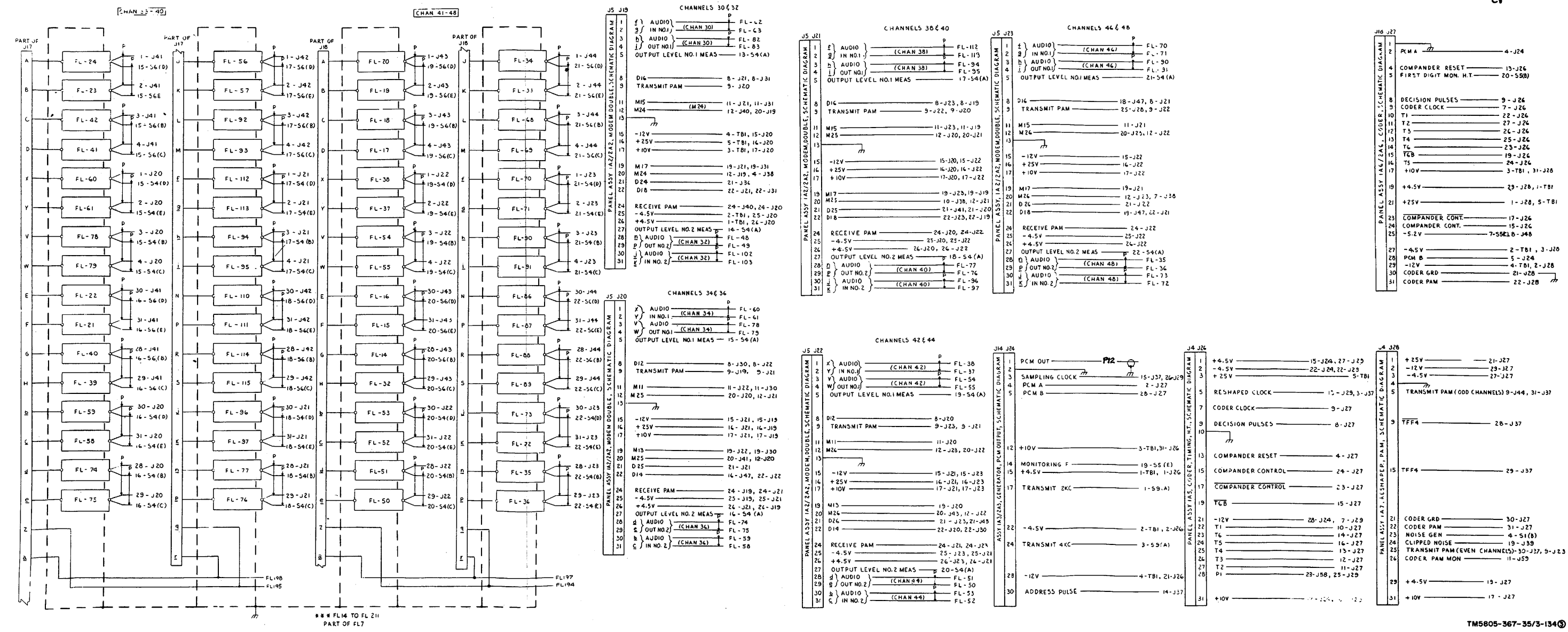


Figure 6-96③. Multiplexer TD-353/u, schematic diagram (part 3 of 5).

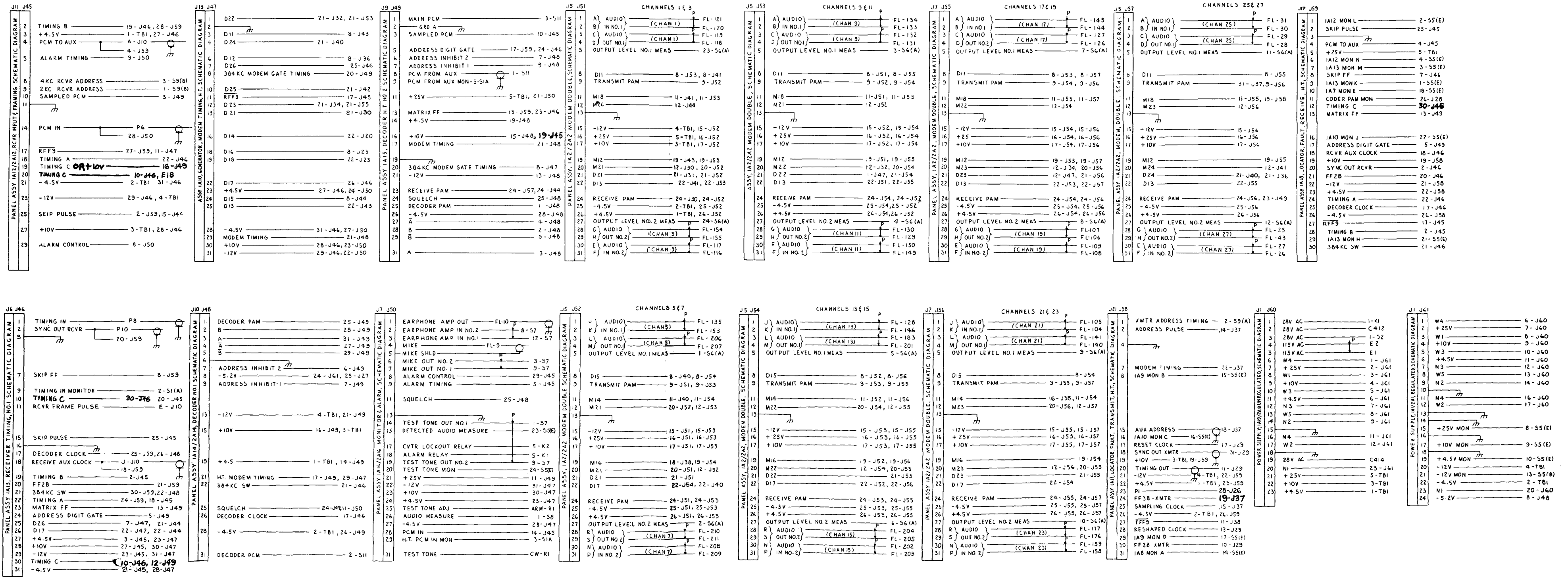
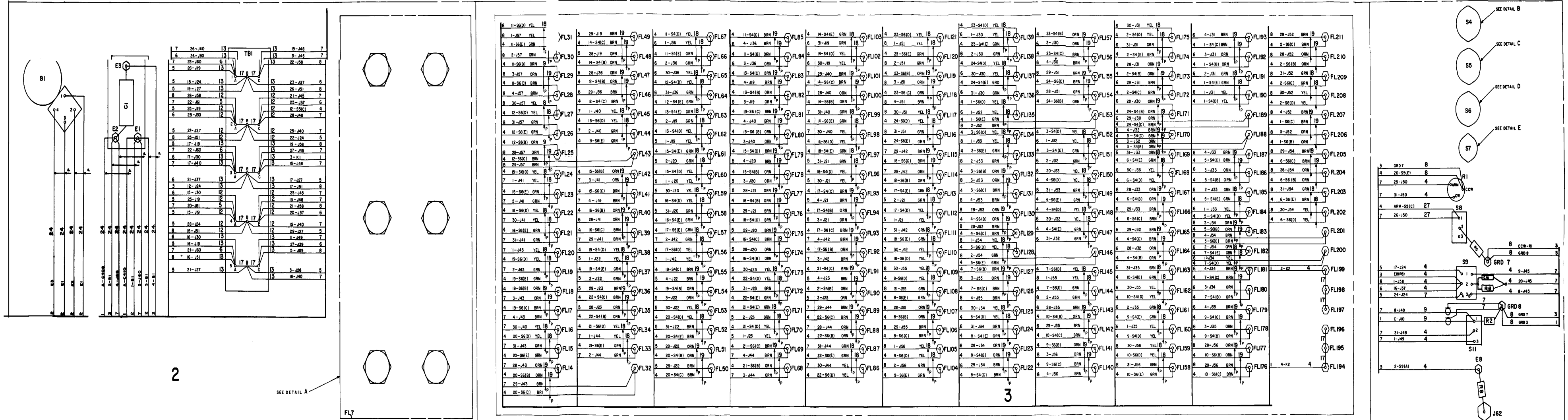
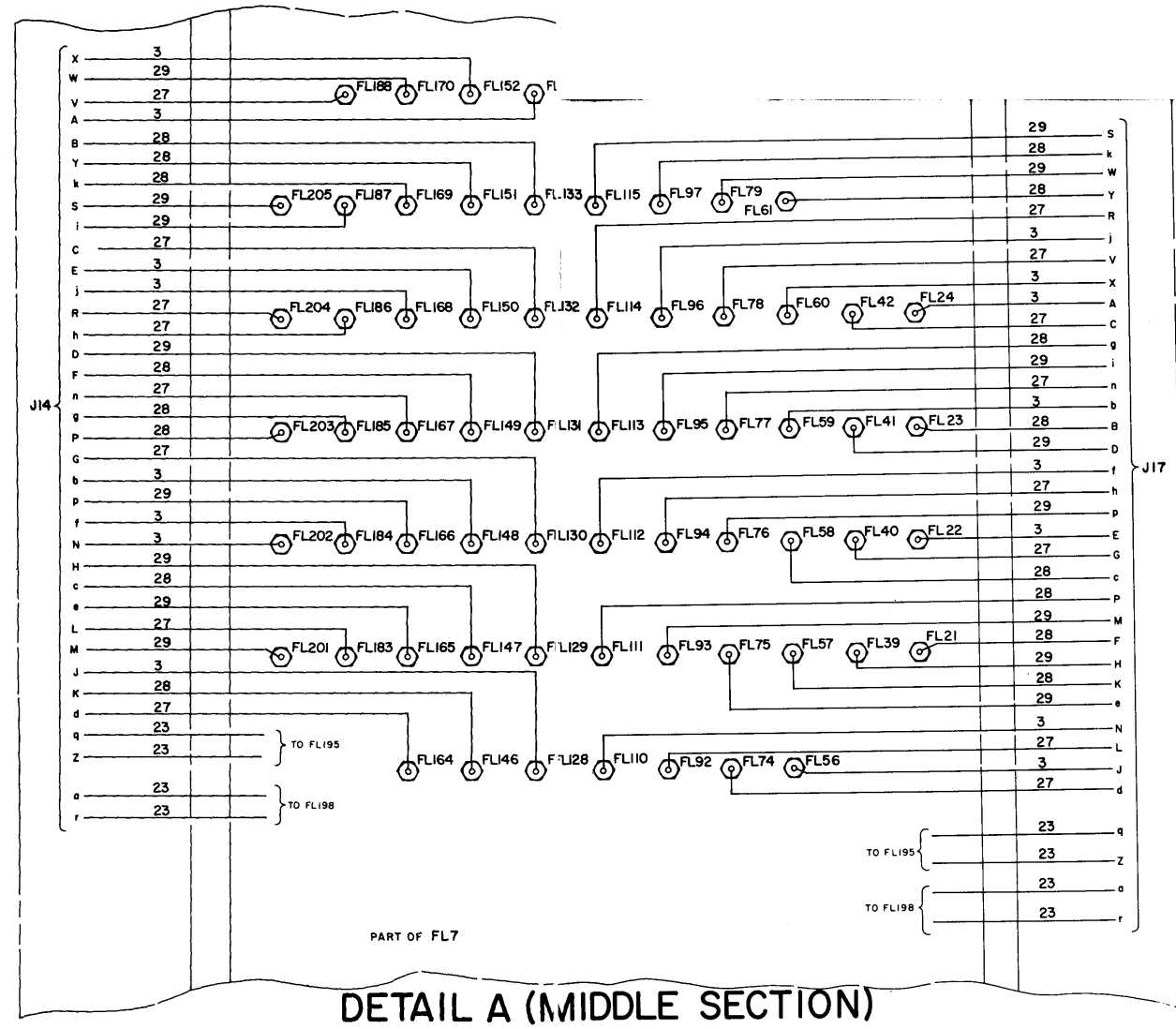


Figure 6-96. Multiplexer TD-353/U, schematic diagram (part 5 of 5).

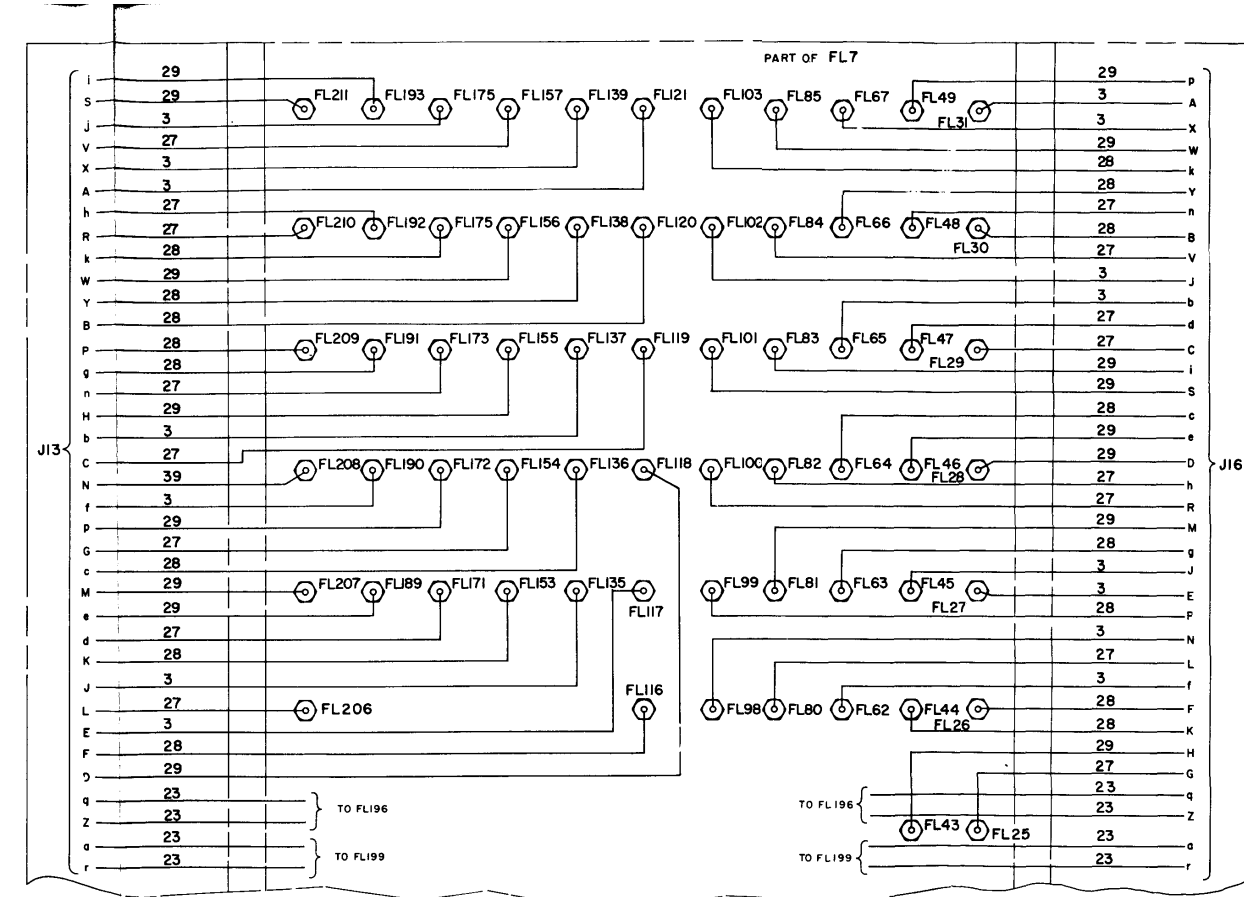


FRONT VIEW WITH FRONT PANEL REMOVED

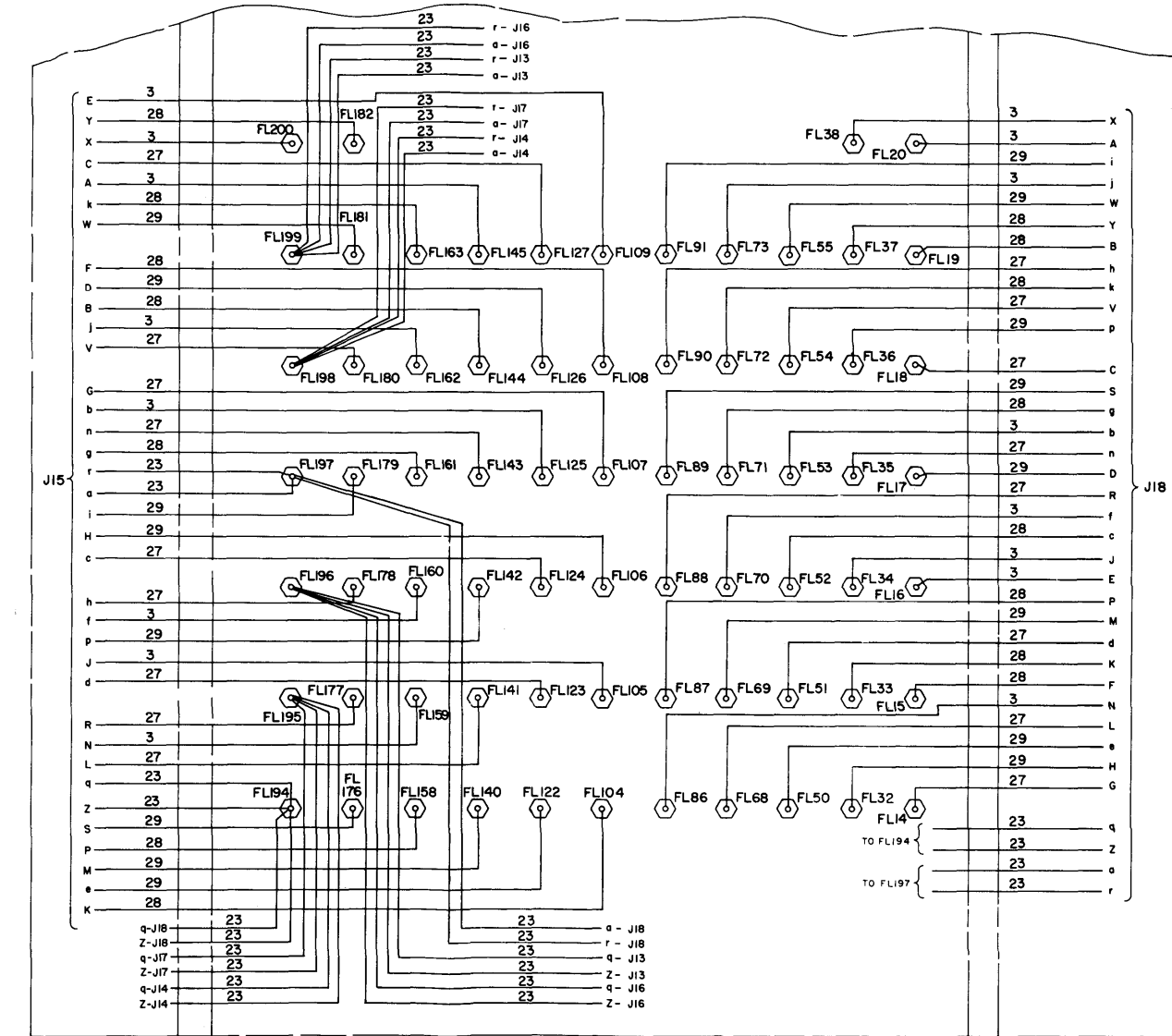
Figure 6-97. Multiplexer TD-353/U, wiring diagram (part 2 of 8).



DETAIL A (MIDDLE SECTION)

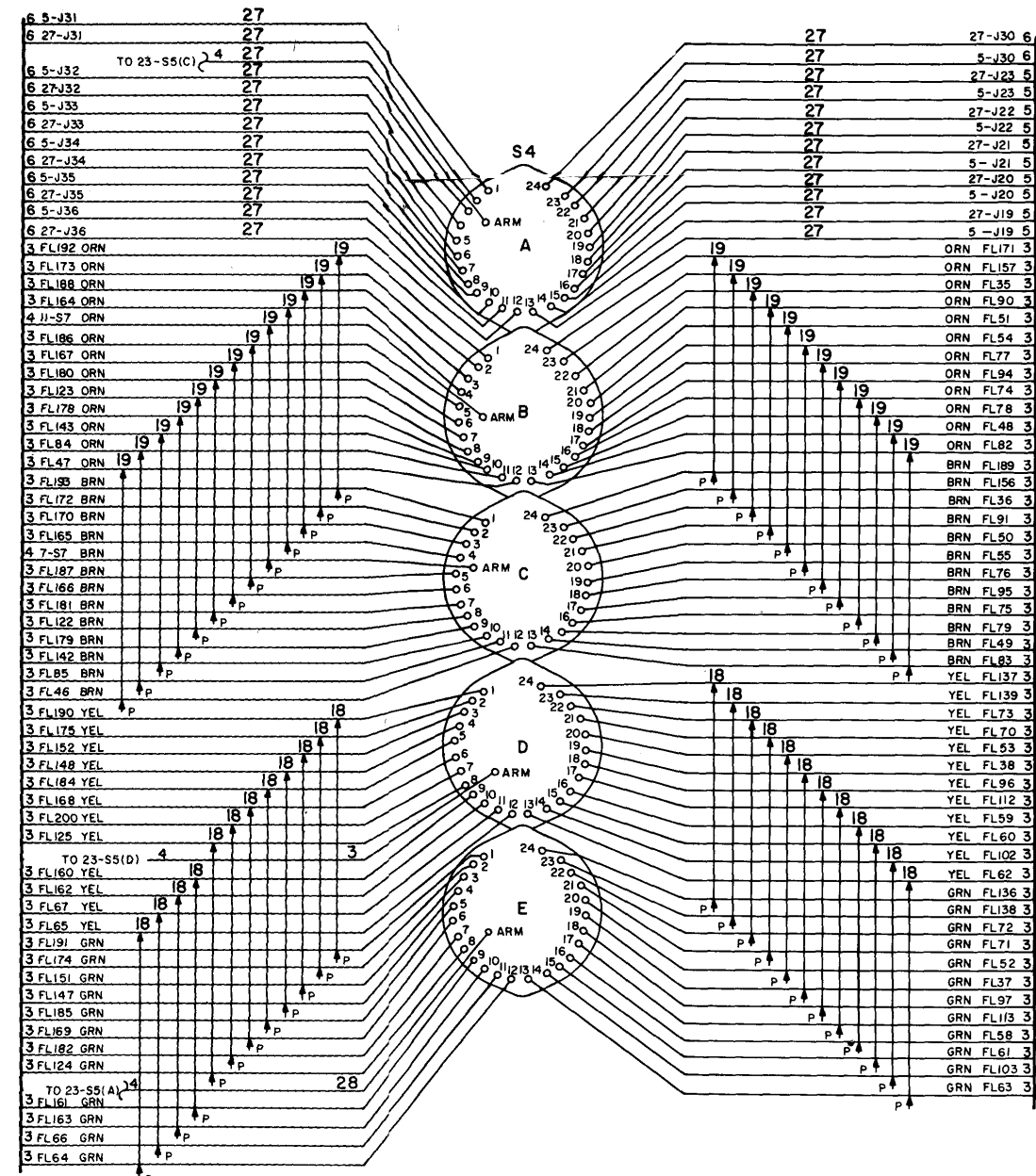


DETAIL A (TOP SECTION)

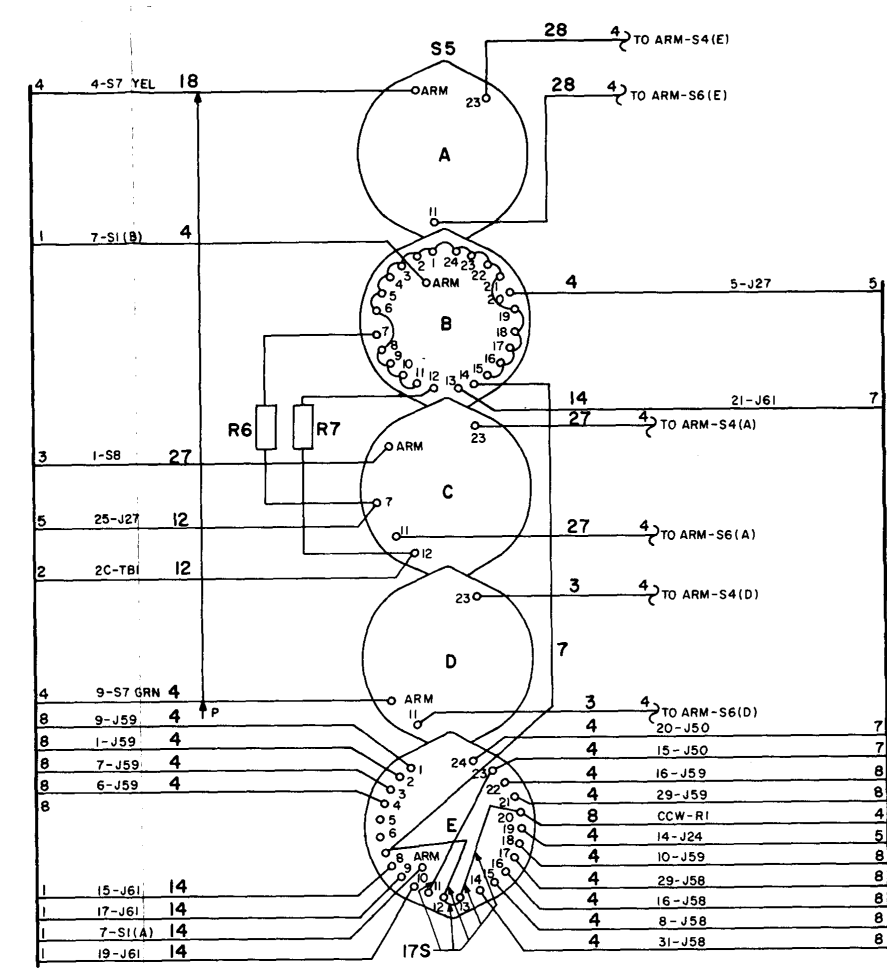


DETAIL A (BOTTOM SECTION)

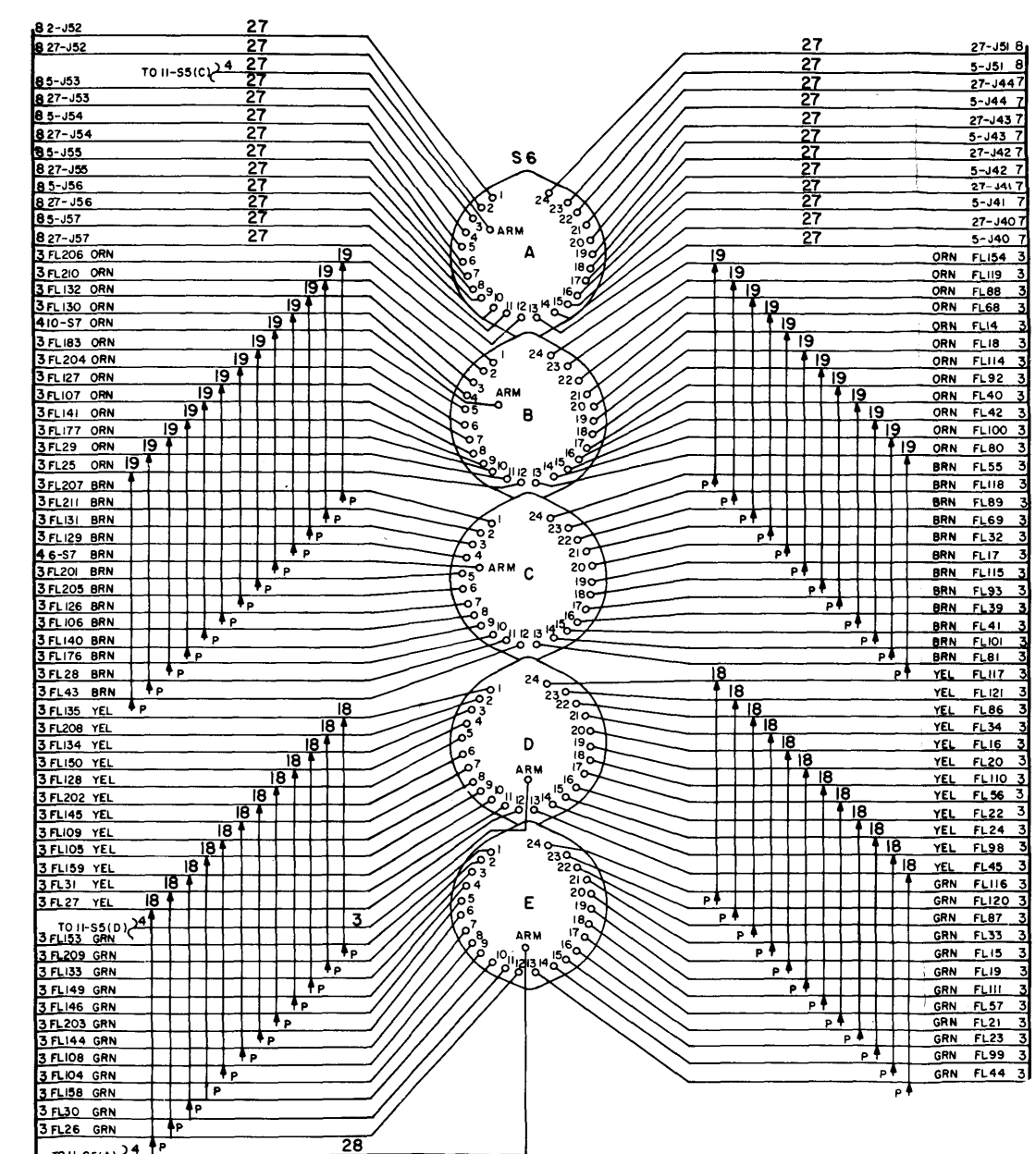
Figure 6-97. Multiplexer TD-353/U, wiring diagram (part 3 of 8).



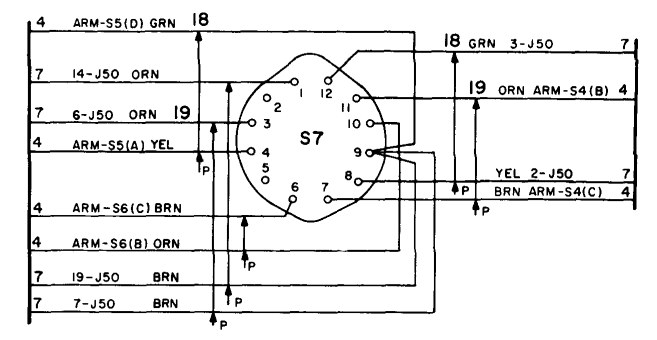
DETAIL B



DETAIL C

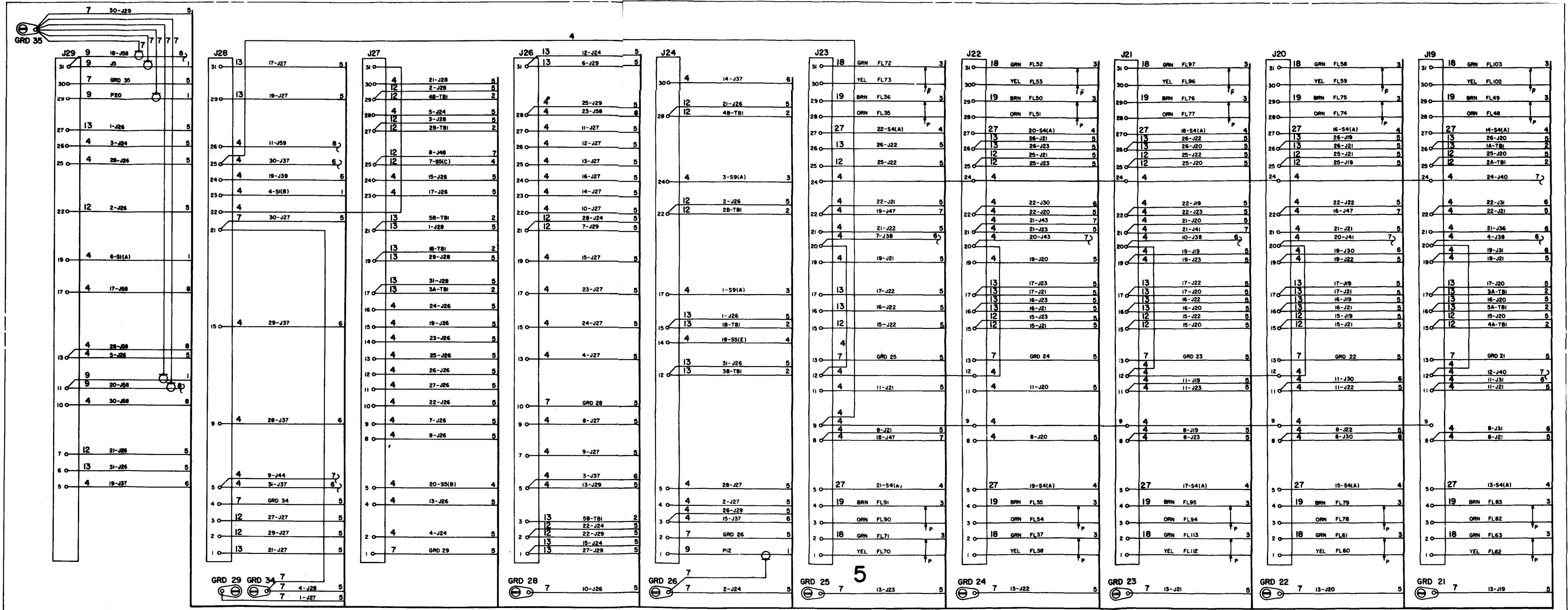


DETAIL D



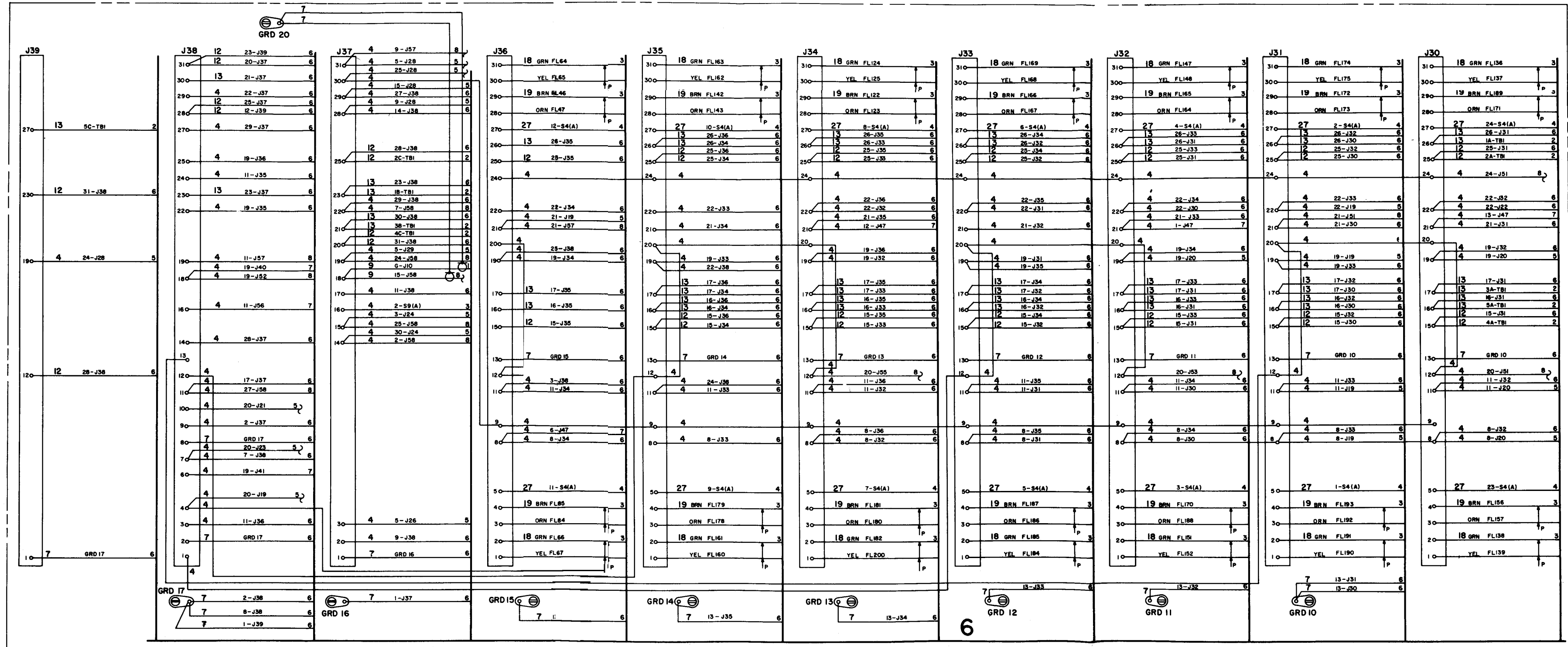
DETAIL E

Figure 6-974. Multiplexer TD-353/U, wiring diagram (part 4 of 8).



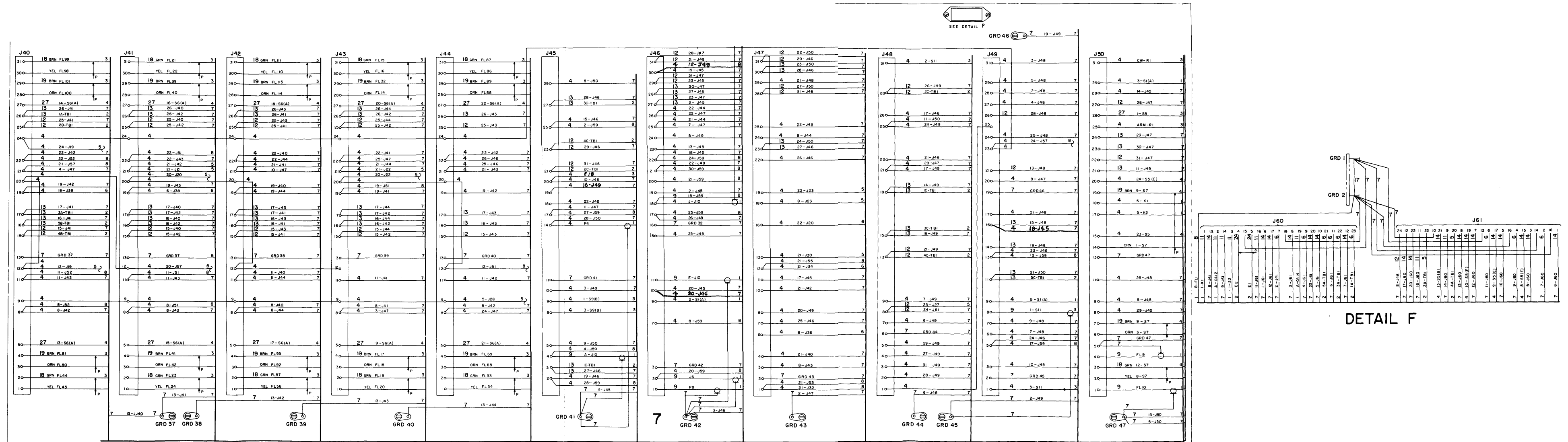
LEFT SIDE VIEW (TOP SECTION)

Figure 6-97. Multiplexer TD-353/U, wiring diagram (part 5 of 8).



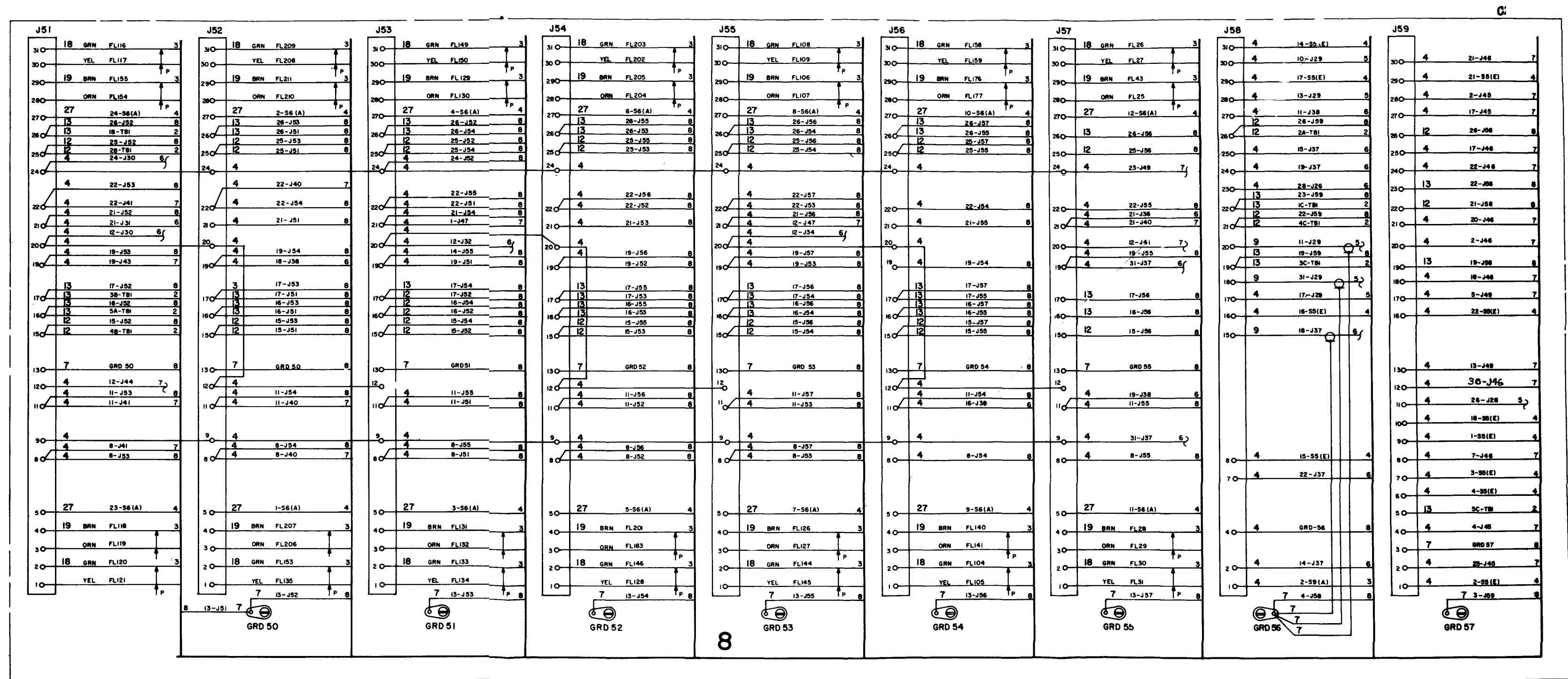
LEFT SIDE VIEW (BOTTOM SECTION)

Figure 6-97. Multiplexer TD-353/U, wiring diagram (part 6 of 8).



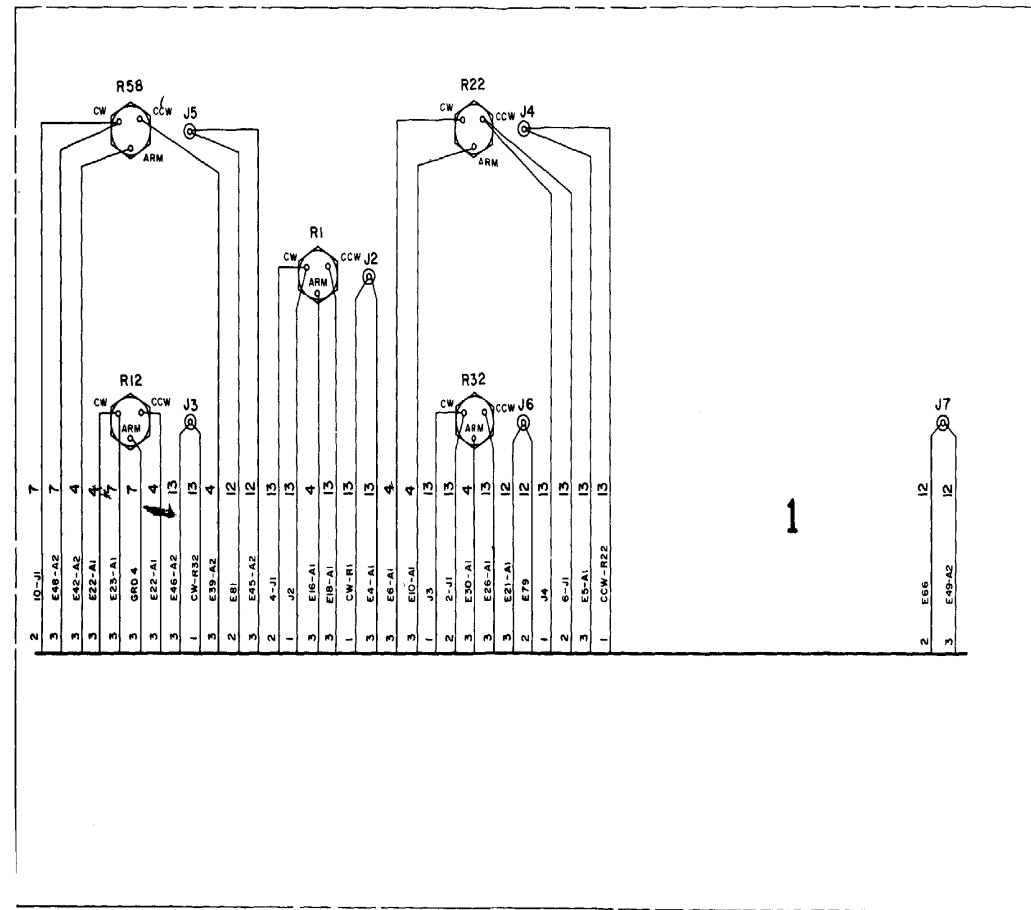
RIGHT SIDE VIEW (TOP SECTION)

Figure 6-97. Multiplexer TD-353/U, wiring diagram (part 7 of 8).

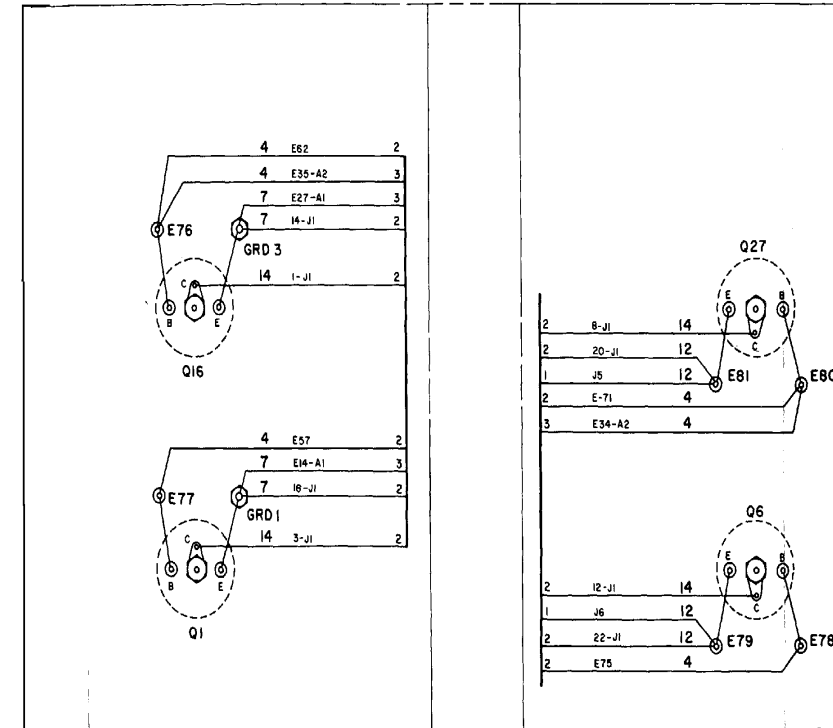


RIGHT SIDE (BOTTOM SECTION)

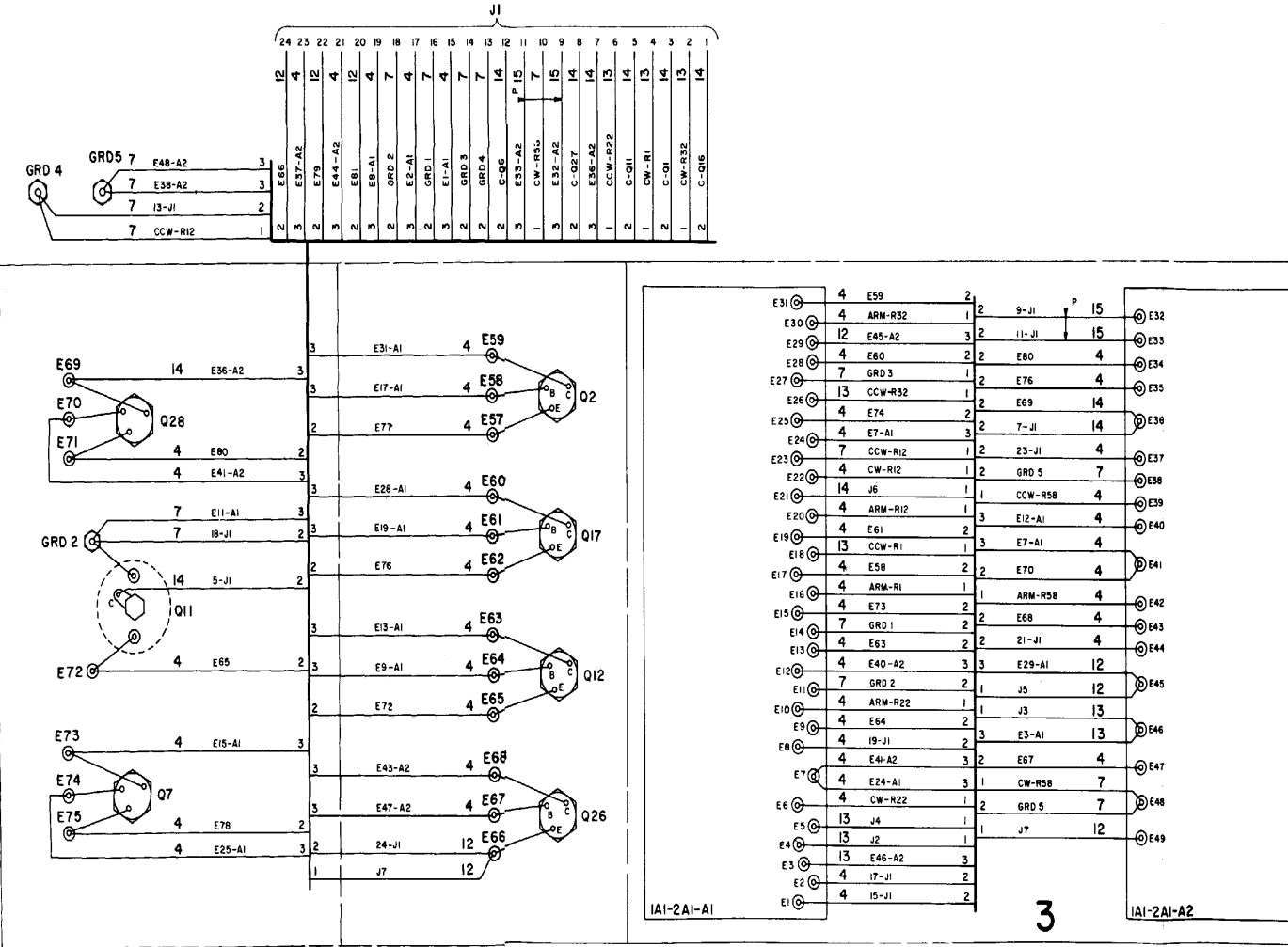
Figure 6-97. Multiplexer TD-353/U, wiring diagram (part 8 of 8).



REAR VIEW OF FRONT PANEL



TOP VIEW OF CHASSIS



BOTTOM VIEW OF CHASSIS

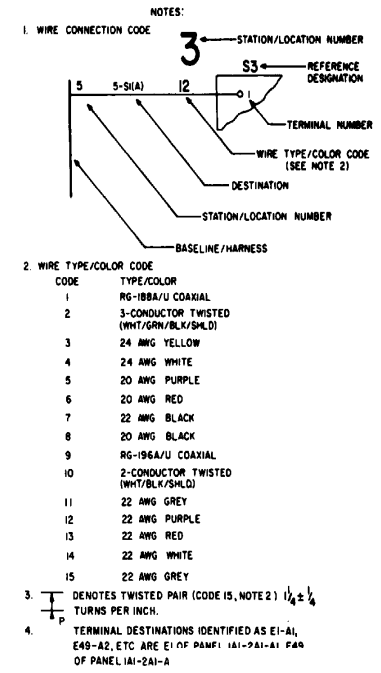
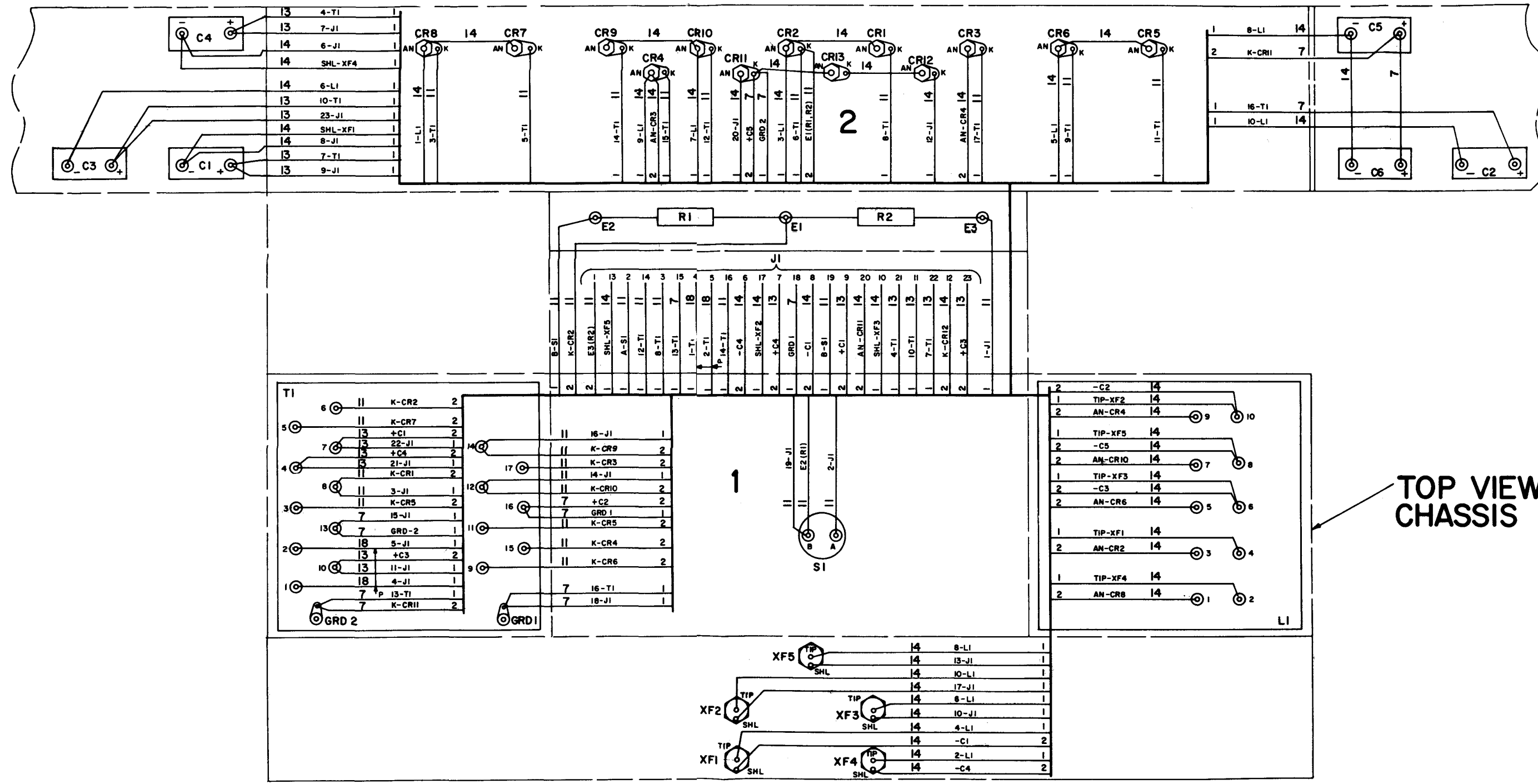


Figure 6-98. Panel 1A1/2A1, wiring diagram.



TOP VIEW OF CHASSIS

REAR VIEW OF FRONT PANEL

- NOTES:
- WIRE CONNECTION CODE
 - 1. WIRE CONNECTION CODE
 - 2. STATION/LOCATION NUMBER
 - 3. REFERENCE DESIGNATION
 - 4. TERMINAL NUMBER
 - 5. WIRE TYPE/COLOR CODE (SEE NOTE 2)
 - 6. DESTINATION
 - 7. STATION/LOCATION NUMBER
 - 8. BASELINE/HARNESS
 - WIRE TYPE/COLOR CODE

CODE	TYPE/COLOR
1	RG-188A/U COAXIAL
2	3-CONDUCTOR TWISTED (WHT/GRN/BLK/SHLD)
3	24 AWG YELLOW
4	24 AWG WHITE
5	20 AWG PURPLE
6	20 AWG RED
7	22 AWG BLACK
8	20 AWG BLACK
9	RG-196A/U COAXIAL
10	2-CONDUCTOR TWISTED (WHT/BLK/SHLD)
11	22 AWG GREY
12	22 AWG PURPLE
13	22 AWG RED
14	22 AWG WHITE
15	22 AWG YELLOW
16	18 AWG BARE WIRE
17	22 AWG BARE WIRE
18	20 AWG GREY
19	20 AWG PURPLE
20	20 AWG RED
21	20 AWG BLACK
22	20 AWG WHITE
23	20 AWG YELLOW
24	20 AWG PURPLE
25	20 AWG RED
26	20 AWG BLACK
27	20 AWG WHITE
28	20 AWG YELLOW
29	20 AWG PURPLE
30	20 AWG RED
31	20 AWG BLACK
32	20 AWG WHITE
33	20 AWG YELLOW
34	20 AWG PURPLE
35	20 AWG RED
36	20 AWG BLACK
37	20 AWG WHITE
38	20 AWG YELLOW
39	20 AWG PURPLE
40	20 AWG RED
41	20 AWG BLACK
42	20 AWG WHITE
43	20 AWG YELLOW
44	20 AWG PURPLE
45	20 AWG RED
46	20 AWG BLACK
47	20 AWG WHITE
48	20 AWG YELLOW
49	20 AWG PURPLE
50	20 AWG RED
51	20 AWG BLACK
52	20 AWG WHITE
53	20 AWG YELLOW
54	20 AWG PURPLE
55	20 AWG RED
56	20 AWG BLACK
57	20 AWG WHITE
58	20 AWG YELLOW
59	20 AWG PURPLE
60	20 AWG RED
61	20 AWG BLACK
62	20 AWG WHITE
63	20 AWG YELLOW
64	20 AWG PURPLE
65	20 AWG RED
66	20 AWG BLACK
67	20 AWG WHITE
68	20 AWG YELLOW
69	20 AWG PURPLE
70	20 AWG RED
71	20 AWG BLACK
72	20 AWG WHITE
73	20 AWG YELLOW
74	20 AWG PURPLE
75	20 AWG RED
76	20 AWG BLACK
77	20 AWG WHITE
78	20 AWG YELLOW
79	20 AWG PURPLE
80	20 AWG RED
81	20 AWG BLACK
82	20 AWG WHITE
83	20 AWG YELLOW
84	20 AWG PURPLE
85	20 AWG RED
86	20 AWG BLACK
87	20 AWG WHITE
88	20 AWG YELLOW
89	20 AWG PURPLE
90	20 AWG RED
91	20 AWG BLACK
92	20 AWG WHITE
93	20 AWG YELLOW
94	20 AWG PURPLE
95	20 AWG RED
96	20 AWG BLACK
97	20 AWG WHITE
98	20 AWG YELLOW
99	20 AWG PURPLE
100	20 AWG RED
 - 1. DENOTES TWISTED PAIR (CODE 24, NOTE 2) 11/4 ± 1/4 TURNS PER INCH.

Figure 6-99. Panel 1A19/2A19, wiring diagram.

By Order of the Secretary of the Army:

HAROLD K. JOHNSON,
*General, United States Army,
 Chief of Staff.*

Official:

KENNETH G. WICKHAM,
*Major General, United States Army,
 The Adjutant General.*

Distribution:

Active Army:


USASA (2)	USAESC (70)	Sig Sec, Gen Dep (5)
CNGB (1)	MDW (1)	Sig Dep (12)
CC-E (7)	Armies (2) except	Army Dep (2) except
Dir of Trans (1)	Seventh (5)	LBAD (14)
CofEngrs (1)	EUSA (5)	SAAD (30)
TSG (1)	Corps (2)	TOAD (14)
CofSptS (1)	USAC (3)	LEAD (7)
USACDCEA (1)	507th USASA Gp (5)	NAAD (5)
USACDCCBRA (1)	508th USASA Gp (5)	SVAD (5)
USACDCCEA (1)	318th USASA Bn (5)	ATAD (10)
USACDCOA (1)	319th USASA Bn (5)	SigFLDMS (2)
USACDCQMA (1)	USATC (2)	AMS (1)
USACDCTA (1)	Svc Colleges (2)	USAERDAA (2)
USACDCADA (1)	USASCS (5)	USAERDAW (13)
USACDCARMA (1)	USASESCS (5)	USACRREL (2)
USACDCAVNA (1)	USAADS (2)	Units organized under following
USACDCARTYA (1)	USAAMS (2)	TOE's (2 each):
USACDCSWA (1)	USAARMS (5)	1-307 11-347
USACDCCEA, Ft Huachuca (1)	USAIS (2)	7 11-357
USAARENBD (2)	USAES (2)	11-6 11-500(AA-AC)
USAAESWBD (5)	USATSCH (5)	11-35 11-587
USARADB (5)	WRAMC (1)	11-56 11-592
USAMC (5)	Army Pie Cen (2)	11-57 11-597
USCONARC (5)	USACDCEC (10)	11-97 17
ARADCOM (5)	Instl (2) except	11-98 31-105
ARADCOM Rgn (2)	Ft Gordon (10)	11-117 32-56
OS Maj Comd (4)	Ft Huachuca (10)	11-127 32-78
LOGCOMD (2)	Ft Carson (21)	11-155 32-500
USAMICOM (4)	Ft Knox (13)	11-157 37
USASTRATCOM (4)	Gen Dep (2)	11-158

NG: State AG (3).

USAR: None.

For explanation of abbreviations used, see AR 320-50.

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

 <p style="text-align: center;"><i>THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.</i></p>		SOMETHING WRONG WITH PUBLICATION	
		FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)	
		DATE SENT	
PUBLICATION NUMBER		PUBLICATION DATE	PUBLICATION TITLE
IN THIS SPACE, TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT.			
BE EXACT PIN-POINT WHERE IT IS			
PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.
PRINTED NAME, GRADE OR TITLE AND TELEPHONE NUMBER		SIGN HERE	

THE METRIC SYSTEM AND EQUIVALENTS

WEIGHT MEASURE

1 Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
 1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
 1 Kilometer = 1000 Meters = 0.621 Miles

WEIGHTS

1 Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
 1 Kilogram = 1000 Grams = 2.2 lb.
 1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
 1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
 1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
 1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
 1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

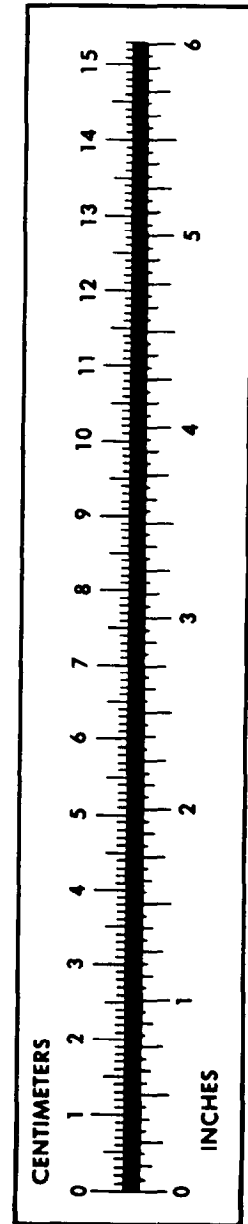
TEMPERATURE

$5/9(^{\circ}\text{F} - 32) = ^{\circ}\text{C}$
 212° Fahrenheit is equivalent to 100° Celsius
 90° Fahrenheit is equivalent to 32.2° Celsius
 32° Fahrenheit is equivalent to 0° Celsius
 $9/5^{\circ}\text{C} + 32 = ^{\circ}\text{F}$

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
its	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
ometers per Liter	Miles per Gallon	2.354
ometers per Hour	Miles per Hour	0.621



PIN : 021869-005