TECHNICAL MANUAL
OPERATOR'S, ORGANIZATIONAL,
AND DIRECT SUPPORT
MAINTENANCE MANUAL


INTERFACE UNIT J-4522/U
(NSN 5975-01-253-6144) (EIC: N/A)
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ORGANIZATIONAL MAINTENANCE PAGE

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## $+$

SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK


DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

## SAFETY SUMMARY

## WARNING

- Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required (para 5-14 through 5-18, 5-20, 5-21).
- Zinc chromate dust primer is highly toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate (para 5-22).
- Isopropyl alcohol is flammable and moderately toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate (para 5-22, 5-23).
- Whenever possible, shut off the power source before beginning work inside unit to prevent electrical shock (para 5-6).
- Adhesive, MIL-A-46016, type II, is flammable and slightly toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate (para $5-23$.


## HOW TO USE THIS MANUAL

HOW DO I FIND INFORMATION? To help you locate information, this manual has three types of indexes.
a. Front Cover. Use front cover index and black tabs at the edge of pages to quickly find the chapters of this manual shown on the cover.
b. Table of Contents. Entries within the main table of contents duplicate the entries on the front cover and are highlighted. This is in case the cover is torn off or soiled beyond legibility.
c. Chapter Indexes. These indexes are located in the front of each chapter. The listings are in the order of appearance.
2. HOW DO I GET FAMILIAR WITH THE EQUIPMENT? See chapter 1 for physical and functional descriptions.
3. DOES THE MANUAL CONTAIN OPERATOR INSTRUCTIONS? See chapter 2 ard 3 for applicability.
4. WHAT IS THE EXTENT OF ORGANIZATIONAL MAINTENANCE? See chapter 4. Normally, organizational maintenance is limited to quarterly preventive maintenance checks and services and replacement of defective line replaceable units (LRUs).
5. WHERE IS DIRECT SUPPORT MAINTENANCE COVERED? Seechapter 5.
6. ARE OTHER MANUALS REQUIRED? Refer to appendix A for a list. Obtain these manuals through supply channels.
7. WHAT TOOLS AND EQUIPMENT ARE REQUIRED? Turn to appendix B (Maintenance Allocation) for a listing.
8. HOW DO I GET SPARE PARTS? Refer to paragraph 5-3
9. WHAT ACTIONS ARE TAKEN IF MISTAKES ARE FOUND IN THE MANUAL? See the block on the table of contents for procedures.

C

## HOW TO USE THIS MANUAL - Continued

10. DO I NEED TO KNOW ANY SPECIAL SAFETY INSTRUCTIONS? Ensure you understand the information on page $A$ and $B$ before you operate or maintain the equipment.
11. WHAT OTHER FEATURES SHOULD I KNOW ABOUT THIS MANUAL? You should know the use of NOTES, CAUTIONS, AND WARNINGS. Definitions are:

## NOTE

An essential operating or maintenance procedure, caution, or statement which must be highlighted.

## CAUTION

An operating or maintenance procedure, practice, condition, statement, etc., which, if not strictly observed, could result in damage to, or destruction of, equipment or loss of mission effectiveness or long term health hazards to personnel.

## WARNING

An operating or maintenance procedure, practice, condition, statement, etc., which, if not strictly observed, could result in INJURY to or DEATH of personnel.

D

HEADQUARTERS,
No. 1

Operator's, Unit, And Direct Support Maintenance Manual<br>INTERFACE UNIT J-4522/U<br>(NSN 5975-01-253-6144) (EIC: N/A)

TM 11-5895-1279-13, 15 March 1992, is changed as follows:

1. The title of this manual is changed as indicated above.
2. Remove old pages and insert new pages as indicated below. New or changed material is indicated by a vertical bar in the margin of the page.

| Remove Pages | Insert Pages |
| :--- | :---: |
| $5-1$ through 5-6 | $5-1$ through $5-6$ |
| $5-15 /(5-16$ blank) | $5-15 /(5-16$ blank) |
| B-1 through B-6 | B-1 through B-6 |

3. File this change sheet in front of the publication for reference purposes.

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## OPERATOR'S, ORGANIZATIONAL, AND DIRECT SUPPORT MAINTENANCE MANUAL INTERFACE UNIT J-4522/U (NSN 5975-01-253-6144) (EIC: N/A)

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INTERFACE UNIT
J-4522/U
1-0

## CHAPTER 1

## INTRODUCTION

## CHAPTER CONTENTS <br> Page



Section I. GENERAL INFORMATION

1-1. SCOPE
Type of Manual: Operator's, Organizational, and Direct Support Maintenance
Model Number and Equipment Name: Junction Box J-4522/U. Throughout manual the Junction Box J-4522/U will be referred to as the Interface Unit.
Purpose of Equipment: Provides interface and control of major system units.

## 1-2. MAINTENANCE FORMS, RECORDS, AND REPORTS

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750, as contained in Maintenance Management Update.
b. Reporting of Item and Packaging Discrepancies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/SECNAVINST 4355.18/AFR 400-54/MCO 4430.3J.700-15/1.

## 1-2. MAINTENANCE FORMS, RECORDS, AND REPORTS - Continued

c. Transportation Discrepancy Report (TDR) (SF 361). Fill out and forward Transportation Discrepancy Report (TDR) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

## 1-3. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR)

If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design or performance. Put it on an SF 368 (Product Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ED-PH, Fort Monmouth, New Jersey 07703-5007. We'll send you a reply.

## 1-4. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS

Refer to the latest issue of DA Pam 25-30 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

## 1-5. ADMINISTRATIVE STORAGE

Administrative storage of equipment issued to and used by Army activities will have Preventive Maintenance Checks and Services (PMCS) performed before storing. When removing the equipment from administrative storage, the PMCS checks should be performed to assure operational readiness.

## 1-6. DESTRUCTION OF ARMY ELECTRONICS MATERIEL

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

## 1-7. REFERENCE INFORMATION

This listing includes the nomenclature cross reference list and list of abbreviations used in this manual.
a. Nomenclature Cross Reference List

| Common Name | Official Nomenclature |
| :---: | :---: |
| Airborne Subsystem (ABN SS) | AQL Airborne Subsystem |
| Computer processor (CP) | Computer Processor CP-1692/U |
| Control panel.................. | Control Panel C-11804/AQL |
| Frequency synthesizer | Synthesizer, Electrical Frequency O-1833/U |

## 1-7. REFERENCE INFORMATION - Continued

Common Name
IF processor (IFP) ................................................... Intermediate Frequency Processor
CV-4008/U.
IF switch (IFS) ............................................................. Intermediate Frequency Switch
SA-2542/U

## 1-7.

## REFERENCE INFORMATION - Continued

## Common Name

IFP control A
$\qquad$
(IFCTRLA) (A12)
F Processor Control -A CCA (A12)
(C5116778)
IFP control B (IFCTRLB) (A13) $\qquad$ IF Processor Control -B CCA (A13) (C5116783)
IU bus 1
(IUBUS1) (A20) $\qquad$ Interface Unit Bus 1 CCA (A20)
(C5116748)
IU bus 2
(IUBUS2) (A14)
Interface Unit Bus 2 CCA (A14)
(C5116753)
IU data link (IUDL) (A26)..........................................Interface Unit Data Link CCA
(A26) (SM-D-873900)
1553B1 interface (1553B1) (A27) ............................1553B1 Interface CCA (A27)
(SM-D-87S904)
1553B2 interface (1553B2) (A15) ............................ 1553B2 Interface CCA (A15)
(SM-D-873904)
IU navigation (IUNAV) (A16) ......................................
Mag tape interface (MTDIU) (A23)...........................
Motherboard (A28) ..................................................
NAV filter FL1 ..........................................................
Oscillator (OSC) (G1) $\qquad$ Oscillator, Rubidium Frequency, Sinewave, 10 MHz
Static random access
memory (SRAM) (A17, A21)
SRAM CCA (A17, A21) (C5116853)
Time-of-intercept (TOIA) (A1)
TOIA CCA (A1) (C5116758)
Time-of-intercept (TOIB) (A4)
TOIB CCA (A4) (C5116763)

## b. List of Abbreviations.



## 1-7. REFERENCE INFORMATION - Continued I

| IU |  |
| :---: | :---: |
| IUBUS | interface unit bus |
| IUDL ...........................................................interface unit-data link |  |
| IUNAV ............................................................interface unit-navigation |  |
| IUTS ...............................................................Interface unit test set |  |
| MTDIJ $\qquad$ magnetic tape-display interface unit |  |
| MTE ...............................................................Mission Test Equipment |  |
| OPINT .............................................................operator interrupt |  |
| PCU ...............................................................Power control unit |  |
| Q-C group ........................................................Quantizer-control group |  |
| RFA ...............................................................Radio frequency antenna |  |
| RDC ...............................................................Receiver digital control |  |
| SDR ................................................................Signal data recorder |  |
| SRAM .............................................................static random access memory |  |
| TOI ...............................................................time-of-intercept |  |
| TIC | universal time interval counter |

## 1-8. SAFETY, CARE, AND HANDLING

a. Safety. For artificial respiration, refer to FM 21-11. When lifting or handling heavy objects, use two persons to prevent possible back injury.
b. Care. Do not use the equipment as a step or a seat.
c. Handling. Do not drop the equipment or turn it over roughly. Avoid damage to connectors.

## Section II. EQUIPMENT DESCRIPTION

## 1-9. CHARACTERISTICS, CAPABILITIES, FEATURES

## CHARACTERISTICS

- MODULAR DESIGN
- RACK-MOUNTED
- HIGHLY RELIABLE

CAPABILITIES

- PROCESSES RAW PULSE DATA FOR TRANSMISSION TO CP
- CONTROLS RECEIVER OPERATION
- CONTROLS AQL AIRBORNE SUBSYSTEM (ABN SS) COMMUNICATION WITH:
- DATA LINK
- NAV SYSTEM
- MISSION TEST EQUIPMENT (MTE)


## FEATURES

- CONTAINS BOTH ROM AND RAM
- PROGRAMMABLE DMA CIRCUITRY
- OPERATES AUTOMATICALLY UNDER SOFTWARE CONTROL
- BUILT-IN TEST CIRCUITS


## 1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS

a. General Location. Refer to TM 11-5821-332-13.
b. Major Components.

## 1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS - Continued


(1)
(2) 1553B1 INTERFACE (1553B1) (A27).
(3) STATIC RANDOM ACCESS MEMORY (SRAM1) (A21).
(4) STATIC RANDOM ACCESS MEMORY (SRAM2) (A17).
(5) 1553B2 INTERFACE (1553B2) (A15).
(6) IFP CONTROL B (IFCTRLB) (A13).
(7) CP INTERFACE (CPIF) (All)
(8) DIGITIZER B (DIGB) (A7)
(9) DIGITIZER A1 (DIGA1) (A5)
(11) OSCILLATOR (OSC) (G1)
(12) NAV FILTER (FL1)

Provides air cooling
Controls 1553B interface

Provides memory storage

Provides memory storage

Controls 1553B interface

Controls IF processor interface

Controls pulse data interface
Provides analog-to-digital conversion
Provides analog-to-digital conversion
Regulates battery function

Outputs very stable clock signal
Filters input from nav set

## 1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS - Continued


(13)
(14)
(15)

MOTHERBOARD (A28)
TIME-OF-INTERCEPT (TOIA) (A1) signal

TIME-OF-INTERCEPT (TOIB) (A4) signal
(16)
(19)

IFP CONTROL A (IFPCTRLA) (A12).
DIGITIZER A2 (DIGA2) (A6)
DIRECTION-OF-ARRIVAL (DOA)
(A9) signal

IU BUS 2 (IUBUS2) (A14)
IU NAVIGATION (IUNAV) (A16)
DUAL BUS PROCESSOR (DBP) (A18).

IU BUS 1 (IUBUS1) (A20)
MAG TAPE INTERFACE (MTDIU)
(A23)
IU DATA LINK (IUDL) (A26)

Board into which CCA's are plugged
Calculates time-of-intercept of

Calculates time-of-intercept of

Provides analog-to-digital conversion
Calculates direction-of-arrival of

Controls IF processor interface

Controls bus 2
Controls navigation interface
Provides processing functions

Controls bus 1
Controls signal data recorder interface

Controls data link interface

## 1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS - Continued

c. External Interfaces.

(1) CONNECTOR J1.
(2) CONNECTOR J2.
(3) CONNECTOR J6.
(4) CONNECTOR J3.
(5) CONNECTOR J4.
(6) CONNECTOR J7.
(7) CONNECTOR J8.
(8) CONNECTOR J15.
(9) CONNECTOR J16.
(10) CONNECTOR J14.

Navigation
Signal data recorder (SDR)
Computer processor (CP)
Operator terminal
Global positioning system (GPS)
Left pod receiver digital control (RDC)

Right pod receiver digital control (RDC)

Computer processor (CP) 1553B
Computer processor (CP) 1553B
Right pod B (RPB)

## 1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS - Continued


(11)
(12)
(13)
(14)
(15)
(16)

CONNECTOR J20.
CONNECTOR J19.

CONNECTOR J13.
CONNECTOR J18.
CONNECTOR J17.
CONNECTOR J12.
CONNECTOR J11.
CONNECTOR J10.
CONNECTOR J9.
CONNECTOR J5.

Data link
$\pm 12$ volts power, -5.2 volts, +28 volts

Right pod A (RPA)
5 volts and ground
Battery
Left pod B (LPB)
Left pod A (LPA)
1553B receiver digital control (RDC)
1553B receiver digital control (RDC)
CRT test

## 1-11. EQUIPMENT DATA

a. Physical

Weight
Height
Width
Length
b. Functional

Input Power
c. Environmental

Temperature
Operating

Non-operating

Altitude
Operating
Non-operating
Humidity
Fungus
Salt fog
Sand and Dust
Vibration
$38.5 \mathrm{lb}(17.50 \mathrm{~kg})$
19.6 in ( 49.78 cm )
10.1 in ( 25.65 cm )
7.6 in ( 19.30 cm )
+5.0 Vdc @ 30 amp $-5.5 \mathrm{Vdc} @ 5 \mathrm{amp}$ +12.0 Vdc @ 1 amp -12.0 Vdc @ 1 amp +28.0 Vdc @ 2 amp

- 51 degrees $F(-46$ degrees $C$ ) to +131 degrees $F(+55$ degrees $C$ )
- 60 degrees $F(-51$ degrees $C$ ) to +185 degrees $F$ ( +85 degrees C )
$30,000 \mathrm{ft}(9,144 \mathrm{~m})$
40,000 ft (12,192 m)
0 to 98 percent
Fungus resistant
Prolonged exposure without degradation
Exposure without damage or degradation
Transportable by ground vehicle, watercraft, or aircraft


## Section III. TECHNICAL PRINCIPLES OF OPERATION

## 1-12. OVERVIEW I

(1) RADIO FREQUENCY ANTENNA (RFA). Intercepts rf emitter signals. Downconverts rf signals to produce phase and trigger if. Signal outputs.
(2) IF SWITCH (IFS). Filters RFA phase and trigger if. signals. Routes if. signals to IFP as directed by RDC.
(3) IF PROCESSOR (IFP). Processes if. signals for signal qualification and signal confirmation.
(4) CONTROL PANEL. Controls system PS. Also used to zeroize CP memory.
(5) INTERFACE UNIT (IU). Provides interface and control of major system units.
(6) COMPUTER PROCESSOR (CP). Performs data computation and signal processing functions for quantizercontrol group (Q-C group).
(7) SYSTEM PS. Provides primary power for Q-C group.
(8) RECEIVER PS. Provides power for receiver group.
(9) RECEIVER DIGITAL CONTROL (RDC). Provides digital control of receiver group and routing of data to Q-C group.
(10) FREQUENCY SYNTHESIZERS (FS). Generates phase lock loop local oscillator (LO) signals (three bands) to rapidly tune RFA.

1-12. OVERVIEW - Continued


## 1-13. DETAILED OPERATION

(1) OSCILLATOR (OSC) (G1). 10 MHz rubidium frequency standard used as clock.
(2) TIME-OF-INTERCEPT (TOIA) (AI), (TOIB) (A4). Produces time-of-intercept digital data.
(3) DIRECTION-OF-ARRIVAL (DOA) (A9). Calculates direction-of-arrival data.
(4) DIGITIZER (DIGA1) (A5), (DIGA2) (A6), (DIGB) (A7). Translates analog data into digital data.
(5) IFP CONTROL (IFPCTRLA) (A12), (IFPCTRLB) (A13). Controls digitizer bus operation.
(6) CP INTERFACE (CPIF) (A11). Controls pulse data interface between IU and CP.
(7) 1553B2 INTERFACE (1553B2) (A15). Controls interface between IU and RDC.
(8) NAV FILTER FL1. Isolates IU from nav set.
(9) IU NAVIGATION (IUNAV) (A16). Interface between IU and nav set.
(10) DIGITIZER BUS. 32-bit parallel bus used for pulse data processing.
(11) IU BUS 2 (IUBUS2) (A14). Controls data transfer between digitizer bus and bus 2.
(12) BUS 2. 16-bit parallel bus used primarily for receiver control.
(13) DUAL BUS PROCESSOR (DBP) (A18). Has INTEL 8086 microprocessor controls processing functions.
(14) STATIC RANDOM ACCESS MEMORY (SRAM2) (A17). Provides 256K SRAM data storage.
(15) STATIC RANDOM ACCESS MEMORY (SRAM1) (A21). Provides 256K SRAM data storage.
(16) IU BUS 1 (IUBUS1) (A20). Controls bus 1 operation. Has RS-232 interfaces with RDC and test equipment operator terminal.
(17) BUS 1. 16-bit parallel bus used primarily for communication with test equipment, CP, and data link.
(18) MAG TAPE INTERFACE (MTDIU) (A23). Controls communications between SDR and IU.
(19) IU DATA LINK (IUDL) (A26). Provides data link interface.
(20) 1553B1 INTERFACE (1553B1) (A27). Controls interface between IU and CP.
(21) BATTERY REGULATOR (BATREG) (A3). Controls battery back-up power to CP and IU SRAM. Recharges battery as needed when system power is applied.


1-13. DETAILED OPERATION - Continued
a. $\quad$ OSC (G1). Refer to OSC (G1) block diagram. OSC (G1) is a $10-\mathrm{MHz}$ rubidium frequency standard used as a very stable clock.

OSC (G1) accepts:

- +28 Vdc
- External output frequency adjustment (depot level only)

OSC (G1) outputs:

- $10-\mathrm{MHz}$ sinewave 0.5 volts root-mean-square (Vrms) in amplitude to TOIA


AOL-5520-01A

OSC (G1) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION -Continued

b. TOIA (A1). Refer to TOIA (A1) block diagram. TOIA (A1):

- Calculates five least significant bits of TOI word
- Measures pulse width of received pulse
- Generate interrupt
- Panel receives reset and control signals from IFPCTRLB (A13)

TOIA (A1) receives:

- $\quad$ 10-MHZ SINEWAVE from OSC (G1)
- TIME MARK from GPS
- DATA SIGNALS from GPS
- RECEIVER RESET SIGNALS and CONTROL SIGNALS from IFPCTRLB (A13)

TOIA (A1) outputs:

- TOI WORD (bits DO-4) to digitizer bus
- $\quad 6.25-\mathrm{MHZ} \mathrm{CLOCK}$ to TOIB (A4)
- PULSE WIDTH MEASUREMENT DATA (D16-28) to digitizer bus
- 1 -second INTERRUPT to CP via digitizer bus
- PWG ENABLE SIGNALS to IFPCTRLA (A12) and IFPCTRLB (A13)
(1) $10-\mathrm{MHz}$ SINEWAVE from OSC (G1) is input to TOIA (A1). The sinewave is converted to a $10-\mathrm{MHz}$ squarewave and input to phase-lock loop/voltage controlled oscillator (PLL/VCO), which outputs a very accurate $200-\mathrm{MHz}$ clock. The $200-\mathrm{MHz}$ clock is divided by two providing a $100-\mathrm{MHz}$ clock. The $100-$ MHz clock is applied to a 4 -bit counter which divides the clock by $2,4,8$, and 16 , providing $50 \mathrm{MHz}, 25$ $\mathrm{MHz}, 12.5 \mathrm{MHz}$, and 6.25 MHz . The $100-\mathrm{MHz}$ clock also becomes the least significant bits of the TOI word. Clock signals are latched through and converted to transistor-transistor logic (TTL) signal levels. The TTL clock signals are latched onto the digitizer bus along with $100-\mathrm{MHz}$ clock as bits DO-4 of TOI word. The $100-\mathrm{MHz}$ clock is bit $0,50-\mathrm{MHz}$ clock is bit 1 , and so on. The $6.25-\mathrm{MHz}$ clock is also routed to TOIB (A4) board where it clocks remaining TOI counters.
(2) $50-\mathrm{MHZ}$ CLOCK from the 4 -bit counter is applied to the 13 -bit counter as a clock input. CONTROL SIGNALS from IFPCTRLB (A13) are applied to the PWG enable circuitry in conjunction with the received pulse. PWG ENABLE enables the 13-bit counter at the beginning of the received pulse. The 13-bit counter produces a pulse train which is converted from emitter coupled logic (ECL) to TTL and applied to the 13-bit latch. At the end of the received pulse, PWG FINISHED is applied to the 13-bit latch to latch PULSE WIDTH MEASUREMENT DATA (D16-28) onto the digitizer bus. RESET disables the 13-bit counter and resets it to a zero count.
(3) TIME MARK and DATA SIGNALS from the GPS are input to TOIA (A1) and received by differential receivers. Both signals feed an interrupt generator which generates a 1second repeat signal, INTERRUPT, used to initiate CP update.
(4) Panel RECEIVER RESET SIGNALS and CONTROL SIGNALS from IFPCTRLA (A13) are applied to the PWG enable circuit. RECEIVER RESET SIGNALS stops and CONTROL SIGNALS starts the PWG enable circuit. PWG ENABLE SIGNALS are used in IFPCTRLA (A12) and IFPCTRLB (A13).


TOIA (A1) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION - Continued

c. TOIB (A4). Refer to the TOIB (A4) block diagram (sheet 1). TOIB (A4) contains counters which output the TOI word. TOIB (A4) also determines if a received signal is pulse doppler or a high frequency signal.

TOIB (A4) accepts:

- $\quad 6.25-\mathrm{MHZ}$ CLOCK from TOIA (A1)
- Counter startup values from software
- ENABLE AND DISABLE CONTROL from software
- Digitized log amplitude signals LAR0-6 from DIGB (A7)
- Reset, blanking, and doppler signals

TOIB (A4) outputs:

- TOI WORD bits DO-15 and bits D16-31 to digitizer bus
- DOPPLER INT to IUBUS1 (A20)
- LOG AMPLITUDE > THRESHOLD SIGNAL to IFPCTRLB (A13)
- TSTPWG to DIGB (A7)
- Data bits CMD5-7 to TOIA (A1)
(1) Two 16-bit counters and one 11-bit counter determine the signal TOI WORD. Each counter is clocked by $6.25-\mathrm{MHZ}$ CLOCK, and is loaded at startup with an initial value determined by software. Counters and latches are also enabled and disabled under software control. The counters either act independently, or all three counters can be configured as one 43 -bit counter. When a pulse is received, counters are stopped and the counter output represents TOI WORD. TOI WORD is then latched onto the digitizer bus as bits DO-15 and D16-31.
(2) Three of the 11-bit counter outputs (D6-8) are applied to a 3-bit latch. These outputs are transmitted to dual AND gates. Two AND gate outputs are buffered and latched. The latched output (TSTPWG) is sent to DIGB (A7).
(3) TOI WORD is also buffered and placed back on the 16 -bit bus. Bits DO-7 go to an 8 -bit latch number 1 . Three of the latch outputs are sent to the TOIA (AI) as CMD5-7. The five remaining bits (CMDO-4) are applied to programmable array logic (PAL) number 1. PAL number 1 generates presets for the 11-bit and 16-bit counters.


TOIB (A4) BLOCK DIAGRAM (SHEET 1 OF 2)

1-13. DETAILED OPERATION - Continued
(4) Refer to the TOIB (A4) block diagram (sheet 2). The 16-bit data (D0-15) are applied to a 7 bit latch. Latch outputs (D0-6) represent the offset data and are applied to an 8 -bit adder. At the same time, digitized $\log$ amplitude information (LAR0-6) from DIGB (A7) is applied to 8 -bit adder and magnitude comparator. The output from the adder represents the sum of the log amplitude data plus the offset data. The sum data are applied to 8 -bit latches numbered 2 and 3 . Output from latch number 2 (D0-7) is placed on the 16 -bit digitizer bus as the least significant byte of the TOI WORD (D0-15). Output from latch number 3 is applied to the magnitude comparator and compared with digitized $\log$ amplitude signals. The output from the magnitude comparator is latched and transmitted to the IFPCTRLB (A13) as LOG AMPLITUDE > THRESHOLD SIGNAL.
(5) Timing and interrupt control is handled by PAL number 2 in conjunction with two 8 -bit latches, a 4 -bit latch, and three counters. The 8 -bit latches latch data bits D815 and the 4 bit latch latches data bits Do3. Ripple carry outputs from the counters generate T1, T2, and T3. Timing signals are applied to PAL number 2. PAL number 2 sends to the counters CNT 1, CNT 2, and CNT 3. RESET, BLANKING, and DOPPLER signals from the IFPCTRLB (A13) are also applied to PAL number 2. These signals and the timing interact to generate interrupt flag (INT FLAG) and doppler interrupt (DOPPLER INT). The interrupt flag is applied to the IFPCTRLA (A12) and doppler interrupt is applied to IUBUS1 (A20).


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TOIB (A4) BLOCK DIAGRAM (SHEET 2 OF 2)

## 1-13. DETAILED OPERATION -Continued

d. DOA (A9). Refer to the DOA (A9) block diagram. DOA (A9) receives digitized phase signals from digitizers DIGA1 (A5) and DIGA2 (A6) and computes DOA for CP.

DOA (A9) receives:

- ADDRESS SIGNALS (DO-7) from IFPCTRLB (A13)
- Digitized PHASE SIGNALS BC, AC, and AD from DIGA1 (A5) and DIGA2 (A6)
- 16BIT DATA (D0-15) from RFA
- MULTIPLIER CONTROL SIGNALS from IFPCTRLA (A12)

DOA (A9) outputs:

- CORRECTED PHASE SIGNAL DATA (bits DO-23) to CP via digitizer bus
- DOA SIGNAL DATA D29-30 and D6-13 to CP via digitizer bus
(1) IFPCTRLB (A13) address input (8-bit) is buffered and addresses lower two RAM segments. The 8-bit address is also encoded and addresses the upper three RAM segments.
(2) 16-BIT DATA is buffered and sent to RAM segments. The upper three RAM segments provide storage for phase correction tables (ROM) received from processors in the RFA. The ROM data from RFA is routed through RDC. 8 -bit adders add phase corrections from RAM to each digitized phase signal from RFA. Corrected phase signals are buffered via 24-bit buffer and sent to the CP as bits DO-23. Corrected phase signals (DF1037) are sent to a $16 \times 16$-bit multiplier. All three corrected phase signals address two $16 \mathrm{~K} \times$ 6 PROM segments. PROM output addresses a $4 \mathrm{~K} \times 8$ PROM segment. PROM contains scaling factor data to compute DOA.
(3) The two most significant bits of PROM output (RELO-1) represent two most significant bits of DOA signal. Two bits are put on digitizer bus as bits D29-30. The five least significant bits of PROM output are fed to the $16 \times 16$-bit multiplier, controlled by MULTIPLIER CONTROL SIGNALS.
(4) Frequency and phase correction data from digitizer bus stored in two lower RAM segments are input to the $16 \times 16$-bit multiplier. Frequency data is multiplied by phase data in the multiplier, buffered, and output to digitizer bus as bits D6-13. The 8-bit DOA signal (D6-13) together with the two most significant bits (D29-30) represent DOA SIGNAL DATA.


## 1-13. DETAILED OPERATION -Continued



DOA (A9) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION Continued

e. DIFA1 (A5). Refer to the DIGA1 (A5) block diagram. DIGA1 (A5) digitizes analog phase signals from the IFP into 8 -bit digital words. Test signals are generated and digitized for automatically checking DIGA1 (A5).

DIGA1 (A5) receives:

- 16-BIT DATA (DO-15) from digitizer bus
- $\quad+12$ VDC from system power
- ANALOG PHASE SIGNALS (DFBCi and DFBCq, DFACi and DFACq) from IFP
- $\quad$ Right and left pod control signals from receiver group
- SAMPLE CLOCK from IFPCTRLA (A12)

DIGA1 (A5) outputs:

- Digitized PHASE BC SIGNALS (PPDF10-17) to DOA (A9)
- Digitized PHASE AC SIGNALS (PPDF20-27) to DOA (A9)
(1) DIGA1 (A5) receives 16-BIT DATA (DO-15) from digitizer bus. Data are buffered and latched into four 3-to- 8 decoders. The decoder outputs are applied to four high speed analog switching networks (analog switches). Five least significant bits of each decoder output are used as test control signals.
(2) The voltage divider/buffer network generates TEST LEVELS and VOLTAGE REFERENCE LEVELS. The voltage input to the voltage divider/buffer network is +12 Vdc. TEST LEVELS are applied to four analog switches. VOLTAGE REFERENCE LEVELS are applied to four analog-to-digital converters (A/D conv).
(3) High speed analog switching is used to multiplex between ANALOG PHASE SIGN[ALS and TEST LEVELS. Each analog switch has four sets of inputs. TEST LEVELS g . through analog switches when test control signals from 3 -to- 8 decoders are asserted. Analog phase signal inputs are switched through analog switches when right and left pod control signals are asserted. One signal set appears at each switch output at one time.
(4) Switch outputs are sent to differential drivers. Each differential driver output is an analog input to a 7 -bit A/D conv. SAMPLE CLOCK simultaneously clocks all four A/D conv when an analog signal is present at the input. A/D conv analog input is converted to an equivalent 7 -bit digital word which addresses two $16 \mathrm{~K} x$ 8 PROM. Each PROM contains scaling factor data for phase and test signals. Upper PROM outputs 8-bit digitized PHASE BC signals to DOA (A9). Lower PROM outputs 8 -bit digitized PHASE AC signals to DOA (A9).


## 1-13. DETAILED OPERATION-Continued



## 1-13. DETAILED OPERATION-Continued

f. DIGA2 (A6). Refer to the DIGA2 (A6) block diagram. DIGA2 (A6) digitizes analog phase and signals and analog fine-frequency signals from the IFP. Test signals are generated and digitized for DIGA2 (A6) board automatic checking.

DIGA2 (A6) receives:

- 16-BIT DATA from digitizer bus
- $\quad+12$ VDC from system power
- ANALOG PHASE SIGNALS (DFADi and DFADq) from the IFP
- ANALOG FINE-FREQUENCY PHASE SIGNALS (FRUi and FRUq) from IFP
- $\quad$ Right and left pod control signals from receiver group
- SAMPLE CLOCK and FRU SAMPLE CLOCK from IFPCTRLA (A12)

DIGA2 (A6) outputs:

- Digitized PHASE AD SIGNALS to DOA (A9)
- Digitized FINE-FREQUENCY SIGNALS (FRUO-7) to IFPCTRLA (A12)
- Digitized FINE-FREQUENCY DATA (D16D-D23D) to IFPCTRLB (A13)
(1) DIGA2 (A6) receives 16-BIT DATA from the digitizer bus. Data are buffered and latched into four 3-to-8 decoders. Five least significant bits of each decoder output are used as test control signals.
(2) The voltage divider/buffer network generates TEST LEVELS and VOLTAGE REFERENCE LEVELS. Voltage input to the voltage divider/buffer network is +12 Vdc. TEST LEVELS are applied to four analog switches. VOLTAGE REFERENCE LEVELS are applied to four A/D conv.
(3) High speed analog switching is used to multiplex between ANALOG PHASE SIGNALS and TEST LEVELS. Each analog switch has four sets of inputs. TEST LEVELS are input and go through the switches when test control signals from each 3-to-8 decoder are asserted. ANALOG PHASE SIGNALS and FINE-FREQUENCY PHASE SIGNALS are input and switched through the analog switches when right and left pod control signals are asserted. Only one signal set appears at each switch output at one time.
(4) Switch outputs are sent to differential drivers. Each differential driver output is analog input to a 7-bit A/D conv. SAMPLE CLOCK clocks two A/D conv with analog phase data. FRU SAMPLE CLOCK clocks the other two A/D conv with fine-frequency data. The AID conv analog input is converted to an equivalent 7-bit digital word which addresses two 16K x 8 PROM. Each PROM contains scaling factor data for phase, finefrequency, and test signals. Upper PROM output is an 8-bit digitized phase AD signal and lower PROM output is 8 -bit digitized FINE-FREQUENCY SIGNALS. The 8-bit digitized FINE FREQUECY DATA signal is also latched onto the digitizer bus for routing to the CP as bits $16-23$ by two separate 8 -bit latches. Only one latch is enabled at a time.

FROM
DIGITIZER BUS:


## 1-13. DETAILED OPERATION-Continued

g. DIGR (A7). Refer to the DIGB (A7) block diagram. DIGB (A7) selects and digitizes log amplitude (LA), signals from the IFP.

DIGB (A7) receives:

- DIFFERENTIAL LOG AMPLIFIER SIGNALS from the IFP
- PWG SIGNALS and PHASE REVERSAL TRIGGER SIGNALS from the IFP
- Right and left pod control signals
- $\quad+12$ VDC from system power
- SAMPLE CLOCK and TEST CONTROL SIGNALS from IFPCTRLA (A12)
- CW FLAG from the digitizer bus

DIGB (A7) outputs:

- Digitized LOG AMPLITUDE SIGNALS (LARO-6)
- 8-BIT DATA (D24-31) and 16-BIT DATA (DO-15) to digitizer bus
(1) Differential receivers receive DIFFERENTIAL LOG AMPLIFIER SIGNALS and PWG SIGNALS. The Largest LA signal is selected and routed as a 6-bit digital word. PWG SIGNALS are converted to TTL signal levels by ECL-to-TTL converters. The TTL level PWG signals are applied to a quad NAND gate and timing circuit. Timing circuit creates a window signal for the gates. PWG output signals from the quad NAND gate are applied to a 4-bit latch. These signals, along with the right and left pod control signals address a $2 \mathrm{~K} \times 8$ and a $2 \mathrm{~K} \times 4$ PROM. Four least significant bits of each PROM output select the largest LA signal for digitizing. The selected PROM outputs are applied directly to the analog switches or latched by the 2 -bit latch to the 1 of 4 multiplexer.
(2) Voltage divider/buffer network receives +12 Vdc and generates TEST LEVELS and VOLTAGE REFERENCE LEVELS. TEST LEVELS are routed to switching network and VOLTAGE REFERENCE LEVELS are routed to the A/D conv.
(3) High speed analog switching multiplexes analog LA signals and TEST LEVELS. The switching network has four input sets. TEST LEVELS inputs go through the switching network when TEST CONTROL SIGNALS are asserted. Analog LA signal inputs go through the switching network when the PROM output is asserted. The 4-bit word selects the largest LA signal. Only one signal set appears at the switching network output at one time.
(4) The switching network output goes through differential drivers and becomes an analog input to the 7 -bit A/D conv. SAMPLE CLOCK clocks the A/D conv when an analog signal is at the input. The A/D conv analog input is converted to an equivalent 7-bit digital word, the digitized LA signal. The LA signal is also latched onto the digitizer bus as bits D24-31 with bit 31 being latched onto bus as a logic low (0).
(5) PHASE REVERSAL TRIGGER SIGNALS are converted to TTL signal levels by ECL-to TTL converters. The multiplexer selects the PHASE REVERSAL TRIGGER SIGNAL with the largest LA, then sends it to the 12-bit counter as the clock input. The counter counts phase reversals on each received pulse. A pulse must be received to count the number of phase reversals. The counter output is fed into two 16-bit latches. CW FLAG is also applied to each latch to indicate if the received signal is continuous wave or pulse. The phase reversal count is latched onto the digitizer data bus as bits DO-12. CW FLAG is latched onto the digitizer data bus as bit D15. Bits D13 and 14 are latched onto the digitizer bus as logic lows (0). Bits D14 and D15 may also be placed on the digitizer bus by the 2-bit latch and a gated buffer. Only one latch or buffer is enabled at a time.

FROM IFP:
DIFFERENTIAL LOG
AMPLITUDE SIGNALS


## 1-13. DETAILED OPERATION-Continued

h. IFPCTRTA (A12). Refer to the IFPCTRLA (A12) block diagram (sheet 1). IFPCTRLA (A12) controls differential signals from IFP and routes them to SRU within IU.

IFPCTRLA (A12) receives:

- CW FLAG SIGNALS, PULSE WIDTH RESET SIGNALS, SIDEBAND FLAG SIGNALS, and START TRIGGER SIGNALS from the IFP in right and left pods
- MULTIPLEXER CONTROL SIGNALS
- DATA (DO-7) from the digitizer bus
- Address data (AD0-7) from the digitizer bus
- Digitized FINE-FREQUENCY SIGNALS (FRU0-7) from DIGA2 (A6)
- PWG ENABLE from TOIA (A1)
- FRU RETRIGGER (FRURTG) SIGNAL from IFPCTRLB (A13)
- READ/WRITE strobes from IFPCTRLB (A13)
- DATA STROBES from the digitizer bus (FRUXDB-/ and RTGXDB-/)

IFPCTRLA (A12) outputs:

- CW FLAG, PULSE WIDTH RESET, SIDE BAND FLAG and START TRIGGER to the digitizer bus
- FINE FREQ SIGNALS (D8-15) to digitizer bus
- READ/WRITE strobes to digitizer bus
- READ/WRITE LOAD ACKNOWLEDGE to digitizer bus
- TEST CONTROL SIGNALS to DIGB (A7)
- MULTIPLIER CONTROL SIGNALS to DOA (A9)
- SAMPLE CLOCK and FRU SAMPLE CLOCK to DIGA2 (A6)
- SAMPLE CLOCK to DIGA1 (A5) and DIGB (A7)
- Data D24-31 to CP
(1) Differential signals received from IFP in right and left pods are applied to differential receivers and fed into mutiplexers. Only one signal from each set appears at multiplexer output. MULTIPLEXER CONTROL SIGNALS control which signal appears at the multiplexer output depending on which receiver pod is active. CW FLAG SIGNALS indicates received signal is continuous wave. PULSE WIDTH RESET SIGNALS indicates received pulse does not meet requirements and should not be processed. SIDEBAND FLAG SIGNAL indicates received signal is upper sideband. START TRIGGER SIGNAL indicates analog signals are stable. SIDEBAND FLAG SIGNAL is also applied to 28 -bit buffers (sheet 2 ).
(2) Three least significant bits (D0-2) on digitizer bus are fed into the 3-to-5 decoder which generates TEST CONTROL SIGNALS used on DIGB (A7).
(3) Digitized FINE-FREQUENCY SIGNALS (FRU0-7) from DIGA2 (A6) are received and latched onto digitizer bus as bits D8-15.
(4) MULTIPLIER CONTROL SIGNALS control multiplier operation on DOA (A9), and are generated using delay lines and logic.
(5) FRURTG SIGNAL generates SAMPLE CLOCK and FRU SAMPLE CLOCK used on DIGA1 (A5), DIGA2 (A6), and DIGB (A7). These signals are generated using delay lines and are logic controlled by PWG ENABLE.


FROM
DIGITIZER
BUS: DATA


IFPCTRLA (A12) BLOCK DIAGRAM SHEET 1 OF 2)

## 1-13. DETAILED OPERATION-Continued

(6) Refer to the IFPCTRLA (A12) block diagram (sheet 2). Address data (AD0-7) from digitizer bus are buffered and sent to PAL number 1 and PAL number 2. PAL number 1 places READ STROBES B0, B2, and B4 and WRITE STROBES B0, B2, B4, and B6 on the digitizer bus. PAL number 2 places READ STROBES 96 and 9A, and WRITE STROBES 90,92, B8, BA, and BC on the digitizer bus. The PAL are enabled by read and write load commands from the control logic circuits.
(7) READ/WRITE STROBES and RAM ENABLE from IFPCTRLB (A13) are applied to the control logic circuits. Logical outputs are read and write load commands (for PAL number 1 and PAL number 2) and acknowledge signal to the digitizer bus.
(8) SIDEBAND FLAG SIGNAL from the multiplexer (sheet 1 ) is applied to 28 -bit buffers that have hardwired addresses. When data from the 8 -bit buffers is to be sent to the CP, DATA STROBES FRUXCB-/ or RTGXDB-/ from the digitizer bus is asserted. The buffer that receives the strobe sends the output data to the CP.


IFPCTRLA (A12) BLOCK DIAGRAM SHEET 2 OF 2)

## 1-13. DETAILED OPERATION-Continued

i. IFPCTRT.R (A13). Refer to the IFPCTRLB (A13) block diagram (sheet 1). IFPCTRLB (A13) performs timing and control functions for the IFP and is connected to the digitizer bus and bus 2.

IFPCTRLB (A13) receives:

- DATA (D16-24) from digitizer bus
- PANEL, SIDEBAND (SB), CLOCK, and ENABLE signals from digitizer bus
- DATA (DO-15) from bus 2
- ADDRESS (A0-7) from bus 2
- POWER ON RESET and RAW RECEIVER RESET from bus 2
- READ, WRITE, and ENABLE STROBES from bus 2
- PWG ENABLE (PWGEN) from bus 2
- DMA ACKNOWLEDGE from bus 2
- GO from bus 2
- LOG AMPLITUDE > THRESHOLD SIGNAL from TOIB (A4)

IFPCTRLB (A13) outputs:

- FRURTG to IFPCTRLA (A12)
- READ, WRITE, and ENABLE strobes to IFPCTRLA (A12)
- CONTROL FLAGS AND ENABLE COMMANDS to digitizer bus
- BUS 2 ACKNOWLEDGE (XACKB2) to DBP
- READ and WRITE OPERATIONS to IUBUS2 (A14)
- READ and WRITE STROBES to digitizer bus
- ABORT and START CLEAR SIGNALS to bus 2
- LOOK and LOOK ENABLE (LOOKEN) SIGNALS to bus 2
- DIRECT MEMORY ACCESS INTERRUPT to bus 1
- DMA REQUEST to digitizer bus and IFPCTRLA (A12)
- ADDRESS SIGNALS and CONTROL SIGNALS to digitizer bus
- RECEIVER RESET SIGNALS to IFP and TOIA (A1)
- FRURTG SIGNALS to IFP
(1) Address bits A0-7 from bus 2 (ADDRESS) are buffered onto the A1 bus. Address bits A11-2 are applied to decoder number one. A13-6 are applied to PAL number 1 which is used as a state machine. POWER ON RESET resets the state machine. READ, WRITE, and ENABLE STROBES from bus 2 and LOOK from PAL number 6 (sheet 3) are also applied to the state machine. When WRITE command (WT) is applied to decoder number 1, specific LOAD commands are generated and applied to 16-bit latches number 1 and 2 (sheet 2). 4-bit data S0-3 from the state machine are decoded by PAL number 2. Appropriate READ, WRITE, and ENABLE STROBES are sent to IFPCTRLA (A12), BUS 2 ACKNOWLEDGE (XACKB2) is sent to DBP, and READ and WRITE OPERATIONS SIGNALS are sent to IUBUS2 (A14). When PAL number 2 decodes a read operation is required, READ (RD) command is sent to decoder number 1. Based on address bits All2, decoder number 1 now sends READ commands to 16-bit transceiver number 1, 2, 3, or 4.


IFPCTRLB (A13) BLOCK DIAGRAM (SHEET 1 OF 4)

## 1-13. DETAILED OPERATION-Continued

(2) Refer to IFPCTRLB (A13) block diagram (sheet 2). Data bits DO-15 from bus 2 are directed through 16-bit transceiver number 1 onto DI bus. When LOAD command from decoder number 1 (sheet 1 ) is applied to 16 -bit latch number 1, data on the DI bus is latched to the digitizer bus and throughout the IFPCTRLB (A13) as ENABLE COMMANDS and CONTROL FLAGS. Latch number 1 is called the IFP command register.
(3) DMA request (RAM ENABLE) is generated for SRAM access. RAM ENABLE (IUN) (from 16-bit latch number 1) is one of the ENABLE commands that are applied to the digitizer bus and IFPCTRLA (A12). When DMA operation (SRAM access) is complete, DMA ACKNOWLEDGE from bus 2 is applied to PAL number 8 (sheet 4).
(4) Data on DI bus is latched onto the C bus by latch number 2 (the FRURTG register) when LOAD command from decoder number 1 (sheet 1 ) is asserted. Data on C bus is loaded into 16 -bit programmable down counter number 1. TIMER1 and TIMER2 (TMR1, 2) signals are applied to PAL number 7 (sheet 4). Data on the C bus is directed through 16bit transceiver number 2 when READ command from decoder number 2 (sheet 1 ) is asserted. The data then on DI bus is also directed through 16-bit transceiver number 1 by READ command and placed on bus 2 .
(5) DATA (bits D16-24) are input from the digitizer bus in parallel to PAL number 3 and 4. When LOOK command from PAL number 6 (sheet 3 ) is asserted, 10 -bit data is applied to 10 inverters. Inverter output is applied to 16 -bit transceiver number 3. 16-bit data ( 6 bits are hardwired low) are routed through the 16 -bit transceiver to the DI bus when READ command from decoder number 1 (sheet 1 ) is asserted. Data on the DI bus is directed through 16-bit transceiver number 1 by READ command and placed on bus 2 .
(6) The 16-bit down counter number 2 counts received pulse data (DO-15). D0-15 from DI bus are loaded into counter number 2 when LOAD command from decoder number 1 (sheet 1 ) is asserted. Counter number 2 begins counting when PULSE COUNT ENABLE (PEN) is received from PAL number 6 (sheet 3). PULSE COUNT CARRY from counter number 2 is applied to timing circuit. DMA INTERRUPT from the timing circuit to bus 1 asserts when pulse count reaches zero. Counter number 2 output on PC bus is directed through 16-bit transceiver number 4 when READ command from decoder number 1 (sheet 1 ) is asserted. DO-15 is also directed through transceiver number 1 to bus 2 by READ command.

1-13. DETAILED OPERATION-Continued


IFPCTRLB (A13) BLOCK DIAGRAM (SHEET 2 OF 4)

## 1-13. DETAILED OPERATION-Continued

(7) To control pulses in the IFP, START and ABORT signals are required. Refer to IFPCTRLB (A13) block diagram (sheet 3). To generate these pulses, LOG AMPLITUDE > THRESHOLD (LA> THRESHOLD) SIGNAL from TOIB (A4) and bus 2 is applied to PAL number 5 which is used as a state machine. GO from bus 2 is applied to logic gates number 1 which generates GO1. GO1 is applied to PAL number 5 and delay line number 1. GO CLEAR (GO CLR) from the delay line is applied back to the logic gates number 1. GO2 from the delay line is also applied to PAL number 5. From the digitizer bus, PANEL, SB, ENABLES, and CLOCK signals are latched by 8-bit latch number 3 to the OK field programmable logic array (FPLA). CONTROL FLAGS from latch number 1 are applied to OK FPLA and PAL number 6. OK FPLA generates ENABLE OK (ENOK) and RENABLE OK (RENOK) and feeds them back to latch number 3. RENOK is also applied to PAL number 5. FPLA requires a LOOK ENABLE (LOOKEN) from PAL number 6. PAL number 6 is discussed in the following paragraph. If the panel (left or right POD forward or aft) signal is correct and enabled and the sideband is set and enabled, the OK FPLA sends out SIDEBAND/PANEL OK (SPOK) to PAL number 5. When a pulse does not qualify for processing, ABORT is generated in PAL number 5 and applied to PAL number 6 and bus 2 . When a pulse does qualify for processing, START is generated in PAL number 5 and applied to PAL number 7 (sheet 4). CLEAR from logic gates number 2 resets PAL number 5.

PWG ENABLE (PWGEN) from bus 2 is applied to PAL number 6. When ABORT from PAL number 5 is not asserted, LOOKEN, START CLEAR, LOOK, and PEN are generated. LOOKEN is applied to FPLA an d bus 2. START CLEAR is applied to bus 2. LOOK is applied to sheets 1 and 2 circuits and bus 2 . PEN is applied to 16 -bit counter number 2 (sheet 2).
(8) Receiver reset control generates CLEAR, IFP RECEIVER RESET, and IFP FRURTG. POWER ON RESET from bus 2 is applied to logic gate number 3. RAW RECEIVER RESET from bus 2 is applied to delay line number 2, and CONTROL FLAGS from latch number 1 is applied to logic gates number 2. Delay line number 2 sends RRCV1 and RRCV2 to logic gates number 2. Logic gates number 2 develop PANEL RESET and RAW RECEIVER RESET. Both resets are converted to four sets of differential signals and sent to the IFP. RECEIVER RESETS are also sent to TOIA (A1). Logic gates number 2 also sends PANEL RESET to logic gate number 3. Logic gate number 3 generates CLEAR, and applies it to delay line number 3. Three delayed outputs from delay line number 3 are applied to logic gates number 2. Logic gates number 2 generate CLEAR and send it to PAL number 5 (sheet 3 ) to reset the circuit.

## 1-13.

 DETAILED OPERATION-ContinuedFROM BUS 2:
LA > THRESHOLD FROM TOIB (A4)


FROM
DIGITIZER BUS


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IFPCTRLB (A13) BLOCK DIAGRAM (SHEET 3 OF 4)

## 1-13. DETAILED OPERATION-Continued

(9) PAL number 7 and number 8 generate READ and WRITE STROBES for the digitizer bus, and FRURTG for the IFPCTRLA (A12). Refer to IFPCTRLB (A13) block diagram (sheet 4). CONTROL FLAGS from latch number 1 (sheet 1), START from PAL number 5 (sheet 3), and TMR1, and TMR2 from counter number 1 (sheet 2 ) are sent to PAL number 7. PAL number 7 generates FRURTG and sends it to IFPCTRLA (A12). It also generates four state output signals (Q14) and sends them to PAL number 8. PAL number 8 functions as a decoder, and decodes the Q1-4 inputs. PAL number 8 generates the READ and WRITE STROBES to control operations on the digitizer bus. One of the WRITE STROBES (DMA WRITE REQUEST) is applied back to PAL number 7. When DMA operation (SRAM access) is complete, DMA ACKNOWLEDGE from bus 2 is applied to PAL number 8.

1-13. DETAILED OPERATION-Continued


IFPCTRLB (A13) BLOCK DIAGRAM (SHEET 4 OF 4)

## 1-13. DETAILED OPERATION-Continued

i. CPIF (A11). Refer to the CPIF (All) block diagram. CPIF (All) controls differential pulse data transfer between IU and CP.

CPIF (A11) receives:

- 32-BIT DATA from the digitizer bus
- CONTROL SIGNALS and INTERRUPT SIGNALS from CP
- $\quad$ Address data (A1-7) from digitizer bus
- CPIF ENABLE from IUBUS2 (A14)

CPIF (A11) outputs:

- CONTROL SIGNALS to bus 2 and CPIF (All)
- $\quad$ CP INTERRUPT to IUBUS1 (A20)
- 4 CP COMMAND SIGNALS, CP COMMAND STROBE SIGNAL, AND CP CLOCK to the CP
-32-BIT DATA (DO-31) on DIFF BUS to the CP
(1) 32-BIT DATA (called beginning of look header) (BOL) from digitizer bus is applied to internal bus D. All of the control signals and enables to route the data through CPIF (All) are generated within CPIF (All) itself. Output from the 16 -bit latches is enabled on internal bus DI. Data on bus DI are enabled to the 32 -bit transceiver. The transceiver puts 32-bit data on internal bus DO and into differential drivers. The differential drivers send the 32-bit data (DIFF BUS) to the CP via internal bus DC which connects to the 32-bit differential bus.
(2) Additional 32-bit data called intercept word (IW) may follow the BOL but require holding to allow frequency retrigger (FRT) signals to be sent to the CP first. IW is then enabled from bus DI into FIFO. When CP is ready for IW, 32-bit data (IW) is put onto DO bus by FIFO and sent by differential drivers to CP the same as BOL.
(3) When 32-bit data (FRT) is sent to the CP, it is transmitted the same as BOL. End of look header (EOL) follows to complete data transfer.
(4) Data bits 28-31 of 32 -bit data word going to CP are address information and are enabled out of 16 -bit latch number 1 and buffer number 1 directly to multiplexers. CPIF control signals and data bits 28-31 control flow of 32bit data through CPIF (A11).
(5) CP status is sent to CPIF (A11) as 32-bit status word. Status word is sent via the 32-bit differential bus and CPIF internal bus DC to differential receivers number 1. At specific times; data bits DO-15 from bus D are also enabled into 16 -bit buffer number 1. The data controls transfer of CP status word as in paragraph (4). The status word out of differential receivers number 1 is put on bus DO and enabled through the 32 -bit transceiver to bus DI. From bus DI, data bits DO-15 are enabled through the 16-bit latch number 3 to bus D and the digitizer bus. Data bits DO-15 from the digitizer bus are sent to DBP (A18). From bus DI, data bits D16-31 are enabled through buffer number 3 to bus D and the digitizer bus. The digitizer bus is connected directly to bus 2 through IUBUS2 (A14). Status word is destined for DBP (A18) which can only receive 16-bit words. Data bits D16-31 were enabled into the 16-bit buffer number 2 and held. Now data bits D16-31 are enabled out of the 16 -bit buffer as DO-15 onto bus D and follow the same route as the first 16 -bits to DBP (A18).
(6) CPIF (A11) receives address bits A1-7 via the digitizer bus and CPIF ENABLE from IUBUS2 (A14). These signals are applied to the control signal generation circuits. CONTROL SIGNALS are used in CPIF (All) and bus 2.


## 1-13.



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CPIF (A11) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION-Continued

(7) INTERRUPT SIGNALS from the CP are applied to differential receivers number 2. The differential receivers outputs are applied to CP command, strobe, and interrupt signal generation circuit which generates the following outputs and transmits them to the computer processor through differential drivers number 2.

- CP INTERRUPT to IUBUS1 (A20)
- 4 CP COMMAND SIGNALS to the CP
- CP COMMAND STROBE SIGNAL to the CP
- CP CLOCK to the CP


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## 1-13. DETAILED OPERATION-Continued

k. 1553R2 (A15). Refer to the 1553B2 (A15) block diagram. Per MILSTD-1553B, command, status, and data words are 20 bits each: 16 data bits, 3 sync bits, and 1 parity bit. Command and status words are interchanged between RDC and IU via 1553B2 (A15) interface. The 1553B converts parallel data to serial data for transmission, or receives serial data and converts to parallel data.
(1) A 16-bit transceiver connects 16 -bit IUBUS2 (A14) data (DB00-15B2) to the bit processor; data (SIB00-15) flows in either direction. The bit processor detects bit errors with parity detection and converts data from parallel to serial or serial to parallel. The 1553 transceiver controls serial data input and output of the bit processor. The isolation transformer connects to and isolates the transceiver from the serial data bus.
(2) When 1553B2 (A15) interface is required for data transmission or receiving, 1553 ENABLE from IUBUS2 (A14) is applied to address generation control circuits. The address generation control circuits produce CONTROL SIGNALS for the address generation circuits. The address generation circuits provide address bits A0-19, which are applied to bus 2. 1553 REQUEST from the decoder PROM is sent to IUBUS2 (A14), which then returns 1553 ACKNOWLEDGE to 1553B2 (A15) interface. INIT resets state machine PROM addressing, causing required control signal generation. INIT resets the state machine PROM, causing address word CROMA0-7 to be applied to the decoder PROM which then generates output signals. These signals may consist of CONTROL SIGNALS, 1553 INTERRUPT, or 1553 REQUEST, depending upon the address word and latch output CMD4. CROMA0-7 is also applied as an input to the state machine, which causes it to output a different address word. This process continues until the next INIT is received.
(3) The hard-wired address input, RTA0-4, is applied to the bit processor and the RTA register. The output of the RTA register, SIB08-12, is applied to the SIB bus. SIB00-03 is applied to a register, which outputs several signals. They are bus high enable signal BHEN, read/write control signals IORC and IOWC, and 4 bits of address data (A16-19). The output signals are sent to bus 2 and are used to access SRAM. SIB00-15 are registered and output to a 16 -bit up counter as STAD01-15. This represents a start address that preloads the counter. The output of the counter is a 4-bit address (AO1-04) to bus 2 .
(4) A command word is applied to the 1553B2 (A15) as part of SERIAL DATA from the RDC. After it is routed to the bit processor via the isolation transformer and 1553 transceiver, it is placed on the SIB bus. SIB00-07 is applied to a latch. Latch output CMD4 is applied to the decoder PROM as part of the CROM address and is used as a bank select for the decoder PROM. When the bit processor detects a receive command word followed by a specified number of data words (DB00-15B2), a single status word on the SIB bus response is placed on the serial 1553B bus (after message validation). If more than one bit processor is placed on the 1553B bus, only the bit processor with a hard-wired address (RTAO-4) matching the 5 -bit address field of the command status word is active at any given time. Similarly, if the bit processor detects a transmit command word, the status word response is again placed on the 1553B interface bus; however, in this case, the status word is followed by a specified number of data words. The data words are formed by latching the contents of SRAM onto bus 2 for conversion to serial format within the bit processor. The process is concluded by transmitting the serial data to the RDC.


1553B2 (A15) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION-Continued

I. NAV FILTER FL1. Refer to the NAV filter FL1 block diagram. NAV filter FL1 isolates the IU from the navigation set.

NAV filter FL1 accepts:

- CLOCK from navigation system
- SYNC from navigation system
- DATA from navigation system
- +12 VDC

NAV filter FL1 outputs:

- CLOCK to IUNAV (A16)
- SYNC to IUNAV (A16)
- DATA to IUNAV (A16)
- $\quad$ Clock return to navigation system
- $\quad$ Sync return to navigation system
- Data return to navigation system
(1) NAV filter FL1 uses three identical networks of resistors, diodes, and linear microcircuits. The microcircuits are powered by a +12 VDC input to CLOCK, SYNC, and DATA signals. CLOCK, SYNC, and DATA SIGNALS received from Carousel Navigation System are filtered, converted from differential to unbalanced signals, and routed to IUNAV (A16).

1-13. DETAILED OPERATION-Continued


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NAV FILTER FL1 BLOCK DIAGRAM
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## 1-13. DETAILED OPERATION-Continued

m. IUNAV (A16). Refer to the IUNAV (A16) block diagram. IUNAV (A16) is an interface between IU and Carousel Navigation System.

IUNAV (A16) receives:

- Unbalanced NAV, CLOCK, SYNC, AND DATA SIGNALS from the navigation system via NAV filter FL1
- NAVIGATION ACKNOWLEDGE and NAVIGATION ENABLE from IUBUS2 (A14)

IUNAV (A16) outputs:

- NAVIGATION REQUEST to IUBUS2 (A14)
- CONTROL SIGNALS to bus 2
- NAV DATA (D0-16) to bus 2
- ADDRESS (A0-19) to bus 2
- NAV INTERRUPT to IUBUS1 (A20)
(1) Unbalanced NAV, CLOCK, SYNC, and DATA SIGNALS from NAV filter FL1 are applied to differential receivers and a multiplexer.
(2) Navigation data from differential receivers is applied to a 32 -bit serial-to-parallel shift register. 32-bit navigation data is latched through two 16 -bit latches and the 16 -bit bus into 16 -bit transceiver and onto bus 2 . The navigation data is also applied to a 16 -bit latch and a 4-bit latch. Navigation data from the navigation system writes to IU memory. The IU reads navigation data from memory and sends it to the CP at the start of a look operation.
(3) The 4-bit data from the 4-bit latch is applied directly to a 20 -bit buffer. The data from the 16 -bit latch is applied to a 15 -bit adder and is also wrapped around to be placed back on the 16 -bit bus through 16 -bit buffer.
(4) Navigation data also address a $512 \times 8$ PROM segment. This PROM segment contains data which, added to navigation data by the 15 -bit adder, generates addresses for SRAM2 (A17) board on bus 2. ADDRESS asserts when NAVIGATION ACKNOWLEDGE asserts. NAVIGATION INTERRUPT generates after data transfer to IU memory.
(5) IUNAV (A16) generates NAVIGATION REQUEST to IUBUS2 (A14), which sends NAVIGATION ACKNOWLEDGE and NAVIGATION ENABLE back. These signals together with navigation clock and sync signals generate control data flow and address generation signals.


## 1-13. DETAILED OPERATION-Continued



## 1-13. DETAILED OPERATION-Continued

n. IUBUS2 (A14). Refer to the IUBUS2 (A14) block diagram. IUBUS2 (A14) performs bus arbitration for bus 2. Data path connection circuit allows digitizer bus and bus 2 to become common bus.

IUBUS2 (A14) receives:

- 32-bit DATA (DO-31) from digitizer bus
- 16-bit DATA (D0-15) from bus 2
- CONTROL SIGNALS from bus 2
- DMA REQUEST and control signals (LOOK ENABLE and LOOK) from IFPCTRLB (A13)
- NAVIGATION REQUEST from IUNAV (A16)
- 1553 REQUEST from 1553B2 (A15)

IUBUS2 (A14) outputs:

- 32-bit DATA (DO-31) to digitizer bus
- 16-bit DATA (DO-15) to bus 2
- Bus 2 upper and lower parity bits to bus 2
- PARITY ERROR and BUS 2 ERROR to IUBUS1 (A20)
- ADDRESS DATA (AO-19) to SRAM (A17)
- NAVIGATION ENABLE to IUNAV (A16)
- 1553B1 ENABLE to 1553B1 (A27)
- 1553B2 ENABLE to 1553B2 (A15)
- CPIF ENABLE to CPIF (A11)
- ADDRESS to digitizer bus
- DMA INTERRUPT to IUBUS1 (A20)
- DMA ACKNOWLEDGE to IFPCTRLB (A13)
- NAVIGATION ACKNOWLEDGE to IUNAV (A16)
- 1553 ACKNOWLEDGE to 1553B2 (A15)
(1) Five transceivers communicate data between the digitizer bus and bus 2. 32-bit data from the the the digitizer bus are formatted onto bus 2 . Or, 16 -bit data from bus 2 are formatted onto the 32 -bit digitizer bus.
(2) The 12-bit down counter counts data words (DIO-11) stored in SRAM. A maximum of 4 K words can be stored for each received signal. The word count (WCO-11) is applied to the 16-bit buffer (4-bits always low), which applies the word count to the internal bus and 8-bit transceivers to send data (DIO-15) to DBP (A18) via bus 2.
(3) IUBUS2 (A14) receives requests for direct memory access (DMA), navigation data, and 1553 data. An acknowledge signal is generated for each request signal.
(4) Parity generation and checking circuits generate an upper parity bit and lower parity bit for data flow to SRAM upper and lower memory segments. PARITY ERROR is generated and sent to IUBUS1 (A20) when a parity error exists on bus 2.
(5) LOOK ENABLE and LOOK from IFPCTRLB (A13) and READ STATUS ENABLE from the enable generation circuits are received by a 16-bit transceiver used as a buffer. Thirteen buffer inputs are hard-wired low. The buffered data are placed on the internal bus and used as control signals.
(6) The 20-bit up counter generates 20 address bits for SRAM, enable generation, and address generation circuits. An address value from the internal bus is entered into the counter, which is clocked by an internal clock. When the counter reaches the value entered, an address is applied to the 6-bit and 20-bit buffers. The buffers apply the output address to SRAM (A17), enable generation circuits, and address generation circuits.


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## 1-13. DETAILED OPERATION-Continued

(7) Enable generation circuits generate NAVIGATION ENABLE, 1553B1 ENABLE, 1553B2 ENABLE, CPIF ENABLE, and READ STATUS ENABLE. NAVIGATION ENABLE allows IUNAV (A16) board to receive navigation data from the navigation system. 1553B1 and B2 ENABLE allows 1553B2 (A15) to control communications between the RDC and the IU. CPIF ENABLE allows CPIF (All) to transfer unprocessed pulse data to the CP. READ STATUS ENABLE allows control signals (LOOK ENABLE and LOOK) from IFPCTRLB (A13) to be placed on the internal bus.
(8) Address generation circuit generates ADDRESS to access CPIF (All) via digitizer bus when unprocessed pulse data is transferred to the CP. Pulse data from SRAM on bus 2 is accessed during DMA operation and sent to the CP via CPIF (All). Software-controlled DMA INTERRUPT to IUBUS1 (A20) asserts on memory access. Address generation circuits are controlled by DMA ACKNOWLEDGE.

## 1-13.

 DETAILED OPERATION -Continued

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IUBUS2 (A14) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION -Continued

o. DRP (A18). Refer to the DBP (A18) block diagram (sheet 1 of 2 , and sheet 2 of 2 ). DBP (AI8) controls data flow between bus 1 and bus 2. A microprocessor controls data flow and memory manipulation while a coprocessor computes numerics.
(1) The 12 MHz oscillator input to clock generator produces 4 MHZ CLOCK to the microprocessor, coprocessor, bus arbiter, and bus controller. RESET from the clock generator resets the microprocessor, coprocessor, and bus arbiter. 3-BIT BUS STATUS (SO-2) from the microprocessor is applied to the bus arbiter, bus controller, and 4-bit latch (sheet 2). 3-BIT BUS STATUS causes the bus arbiter to generate BUS 1 AND BUS 2 CONTROL SIGNALS. 3-BIT BUS STATUS also causes the bus controller to generate I/O READ/WRITE signals and MEMORY READ/WRITE signals. MEMORY READ/WRITE accesses SRAM when no other bus activity is present. I/O READ/WRITE tells an input or output device to read from or write to data bus. In addition, the bus controller generates INTAA1-B1 containing decoded interrupt information, which is sent to PAL number 3 on the IUBUS1 (A20) card. INTAB1 is also sent to the programmable interrupt controller as an interrupt acknowledge.
(2) When INTERRUPTS (INTO-7) are asserted, the programmable interrupt controller sends INTERRUPT SIGNAL to the microprocessor, which executes software to handle the interrupt. The interrupt controller has an 8-bit bi-directional data bus to the microprocessor address/data bus for address and data flow.
(3) The microprocessor has a 4-bit address/status bus (AD16-19) and a 16-bit bi-directional address/data bus (ADO-15) for address, status, and data flow. The address/status bus is the four most significant address lines for memory operations. During memory operations, status information is available on these lines.
(4) When a DBP card is ready to use the bus, BUS REQUEST is sent to either IUBUS1 (A20) or IUBUS2 (A14) via bus 1 or bus 2, respectively. When either IUBUS1 (A20) or IUBUS2 (A14) grants access to the bus, it sends BUS ACKNOWLEDGE to the requesting DBP card.
(5) Decoded cascade information is sent to IUBUS1 (A20) on the CASAO-2 or CASBO-2 lines, depending upon whether it is an output from the A13 or A14 card.


DBP (A18) BLOCK DIAGRAM (SHEET 1 OF 2)

## 1-13. DETAILED OPERATION Continued

(6) Address bits ADO-19 from the microprocessor are applied to the chip select generation circuitry via the 4-bit and 16-bit buses and latches. The chip select generation circuitry generates device-access chip selects for the programmable interrupt controller, serial communication interfaces, programmable interval counter (PIC), SRAM, EPROM, bus 1, and bus 2.
(7) Address data from the 4-bit and 16-bit latches are controlled by LATCH ENABLE from the bus controller. The 20 -bit address bus also addresses a $48 \mathrm{~K} \times 8$ SRAM and a $32 \mathrm{~K} \times 8$ EPROM. The 16-bit address/data bus allows 16bit data transfer between the microprocessor, bus 1, and bus 2. 16bit data (D00-15B1/B2) is transmitted or received by the 16-bit transceivers (2 and 3). Address data from the address/status bus are buffered by the 20-bit buffers, which are enabled by control signals from the bus arbiter.
(8) The 16-bit transceiver (1) transfers data (DOO-15RB) between the microprocessor and the RS-423 serial communication interface \& The serial communication interfaces provide noise-free data transfer for diagnostic program load and cathode ray tube (CRT) test. The PIC (used as a baud rate generator) sets serial interface data transfer rates. The PIC and serial interfaces receive 1.536 MHZ CLOCK from the 1.536 MHz oscillator (part of the DBP). Serial interface data transfer is set at 153.6 KHz . Transmit and receive control signals are software-controlled interrupts from each serial interface. The 16-bit address/data bus allows address and data flow between each serial interface, the PIC, SRAM, EPROM, the microprocessor address a data bus, and the programmable interrupt controller (sheet 1). The EPROM contains software that controls DBP (A18).


## 1-13. DETAILED OPERATION-Continued

p. SRAM2 (A17). SRAM2 (A17) and SRAM1 (A21) theory of operation is identical. Therefore only SRAM2 (A17) is described. Refer to the SRAM2 (A17) block diagram.
(1) Memory Configuration. The SRAM is configured as follows:

- The $256 \mathrm{~K} \times 9$-bit static RAM (SRAM) is divided into two parallel segments, an upper $128 \mathrm{~K} \times 9$-bit segment and a lower $128 \mathrm{~K} \times 9$-bit segment.
(2) Memory Access. The SRAM is accessed as follows:
- Seventeen-bit address A01-17B2 is buffered then split off into different functions.
- Address bits A01-14 address the internal $16 \mathrm{~K} \times 3$ bit memory banks on the $32 \mathrm{~K} \times 3$ bit SRAM. The upper/lower write enable signals determine which of the $128 \mathrm{~K} \times 9$ bit SRAM banks is selected.
- MEN-/ (memory enable) from bus 2 is buffered and applied to the decoder.
- The upper three bits of the address bus (A15-17) together with MEN-/ and POWER GOOD are used to generate the chip selects (CS00-07) for each $32 \mathrm{~K} \times 3$-bit segment of memory.
- CS00-07 are buffered and applied to the upper and lower SRAM as CS00-07B and CSOO-07A, respectively.
(3) Data Handling.
- Data are written into or read out of RAM via an 18 -bit bidirectional bus to/from bus 2 . This 18 -bit bus carries a 16-bit bidirectional data bus (DB00-07 and DB08-15) to/from bus 2 and two parity bits to/from IUBUS2 (A14).
- Each $128 \mathrm{~K} \times 9$-bit segment of memory outputs 8 -bits of data and one parity bit.
- Present are 16 -bit data, an upper parity bit, and a lower parity bit. The parity bits are used for error detection and correction during data transmission to or from another board. Upper/lower write enable signals are generated by BUS CONTROL SIGNALS from the DBP via bus 2 .
- Data read from memory (RD00-15) is first buffered before being put onto the data bus. Data on the data bus (WD00-15) is buffered before being written into memory.
(4) Battery Backup. The power to each SRAM in the IU is maintained by a battery in the BATREG (A3). In the event of a system power failure, this battery will ensure that data stored in the SRAM will not be lost. Data cannot be accessed, however, until system power is restored.


SRAM2 (A17) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION-Continued

q. IUBIS1 (A20). Refer to the IUBUS1 (A20) block diagram. IUBUSI (A20) controls processed data flow along bus 1.

IUBUS1 (A20) receives:

- 16-bit ADDRESS DATA (AO-15) from bus 1
- 16-bit DATA (D0-15) from bus 1
- CP1553 REQUEST from 1553B1 (A27)
- SDR REQUEST from MTDIU (A23)
- DATA LINK REQUEST from IUDL (A26)
- PARITY ERROR from IUBUS2 (A14)
- BUS 1 CONTROL SIGNALS from DBP (A18), MTDIU (A23), 1553B1 (A27), and IUDL (A26)
- BUS 2 ERROR from bus 2
- ZEROIZE SRAM from connector J19
- IO READ/WRITE SIGNALS from DBP (A18)
- 1.536 MHZ CLOCK from DBP (A18)
- CP1553 INTERRUPT from 1553B1 (A27)
- SDR INTERRUPT from MTDIU (A23)
- TRANSMIT/RECEIVE CONTROL from DBP (A18)
- DMA INTERRUPT from IUBUS2 (A14)
- NAV INTERRUPT from IUNAV (A16)
- 1553 INTERRUPT from 1553B2 (A15)
- CP INTERRUPT from CPIF (All)

IUBUS1 (A20) outputs:

- 16-bit DATA (D0-15) to bus 1
- SDR ENABLE to MTDIU (A23)
- SRAM ENABLE to SRAM (A17)
- CP1553 ENABLE to MTDIU (A23)
- DATA LINK ENABLE to IUDL (A26)
- CP1553 ACKNOWLEDGE to 1553B1 (A27)
- SDR ACKNOWLEDGE to MTDIU (A23)
- DATA LINK ACKNOWLEDGE to IUDL (A26)
- Bus 1 upper and lower parity bits to bus 1
- Bus 1 error to bus 1
- INTERRUPTS to DBP (A18)
(1) 16-bit ADDRESS DATA is buffered and encoded generating SRAM ENABLE, CP 1553 ENABLE, SDR ENABLE, and DATA LINK ENABLE. 16-bit ADDRESS DATA also generates chip selects for circuits on IUBUS1 (A20).
(2) IUBUS1 (AD0) controls 1553B1 (A27), IUDL (A26), and MTDIU (A23). CP1553, SDR, and data link access requests are applied to request acknowledge control circuits. Corresponding acknowledge signals are generated and returned.
(3) The 16-bit transceiver connects bus 1 to parity circuits, four programmable interrupt controllers, six programmable interval timers used as baud rate generators, and six serial interfaces. Parity generation and checking generates upper parity bit and lower parity bit corresponding to upper and lower memory segments on SRAM. PARITY ERROR indicates a parity error on bus 2, causing two bus error signals to assert and be read by software. PARITY ERROR INTERRUPT is also generated and controlled by software. Bus 1 signals control parity bit generation and checking on bus 1 .
(4) Four programmable interrupt controllers receive priority interrupts. Each controller output is a softwarecontrolled INTERRUPT to DBP (A18). IO READ/WRITE SIGNALS control the programmable interrupt controllers.


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IUBUS1 (A20) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION-Continued

(5) Six serial communication interfaces connect to RS 423 interfaces. One interface communicates with the operator terminal, two interfaces receive phase correction data from rf ROM in the RDC. The remaining three interfaces are spares. Each interface and programmable interval timer (baud rate generator) receives 1.536 MHZ CLOCK. IO READ/WRITE SIGNALS and software control each interface and the baud rate generator. The baud rate generator controls data flow speed.
(6) ZEROIZE SRAM asserts to clear SRAM. .The zeroize signal generates software controlled interrupt. Software clears each SRAM by filling SRAM with zeros.


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## 1-13.

DETAILED OPERATION -Continued
r. MTDIIT (A23). Refer to the MTDIU (A23) block diagram. MTDIU (A23) controls communications between the signal data recorder (SDR) and IU. Data flow is on 8-bit bidirectional data bus between IU and SDR Control signals are transferred on differential lines.

MTDIU (A23) receives:

- 8-BIT DATA from SDR
- SDR ENABLE from IUBUS1 (A20)
- SDR ACKNOWLEDGE from IUBUS1 (A20)
- CONTROL SIGNALS from SDR
- 16-bit DATA (DO-15) from bus 1
- CP1553 ENABLE from IUBUS1 (A20) MTDIU (A23) outputs:
- 8-BIT DATA to SDR
- SDR REQUEST, SDR INTERRUPT, and CONTROL SIGNALS to IUBUS1 (A20)
- CONTROL SIGNALS to SDR
- 16-bit DATA (D0-15) to bus 1
- 16-bit ADDRESS DATA (AO-15) to bus 1
(1) On power-up, MTDIU (A23) checks for SDR inputs. Differential CONTROL SIGNALS are applied to differential receivers. The output from the differential receivers is applied to latch circuits. Three PROM segments generate interface control signals. The first PROM segment generates control signals, SDR REQUEST, and SDR INTERRUPT for IUBUS1 (A20) PROM outputs are applied to the 24-bit latch. Control signals from the 24-bit latch are applied to differential drivers. Differential outputs are sent back to the SDRL These signals represent control, status, and command signals for data transfer control.
(2) Two other PROM segments control PROM addressing. PROM 8-bit data are latched and double buffered (8-bit and 16-bit) onto bus 1 and read by software. The SDR can control PROM addressing by sending addresses through the multiplexer.
(3) SDR REQUEST is sent to IUBUS1 (A20). IUBUS1 (A20) returns SDR ACKNOWLEDGE to enable the SDR interface data transfer to begin. The 20-bit counter generates addresses for data stored on SRAM. The acknowledge signal enables a buffer which sends addresses to SRAM via bus 1. SRAM data is transferred on bus 1 and brought into the 16-bit buffer. 8-bit data is latched and applied to differential drivers. Differential driver outputs are transferred to the SDR. The 16-bit counter counts data words transferred to the SDR.
(4) CP 1553 ENABLE indicates the CP 1553 interface is able to transfer data. Data transferred from SDR to IU also transfers to the CP via the 1553 interface. Control signal generation circuits control transfer.
(5) SDR INTERRUPT is asserted when data is to be transferred.


## 1-13.



MTDIU (A23) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION-Continued

s. IUDL (A26). Refer to the IUDL (A26) block diagram. IUDL (A26) interface through aircraft data link system, communicates between AQL system and ground systems.

IUDL (A26) receives:

- 16-bit DATA (D0-15) from bus 1 DATA LINK ACKNOWLEDGE and DATA LINK ENABLE from IUBUS1 (A20)
- 20-KHZ CLOCK, 1.15 MHZ CLOCK and SERIAL DATA from data link system
- CONTROL SIGNALS from software

IUDL (A26) outputs:

- DATA LINK REQUEST, CONTROL SIGNALS, and RECEIVE AND TRANSMIT DATA INTERRUPT to IUBUS1 (A20)
- SERIAL COMMUNICATIONS CONTROLLER INTERRUPT to bus 1
- 16-bit DATA (D0-15) to bus 1
- ADDRESS DATA (AO-15 and A16-19) to bus 1
- SERIAL DATA to data link
(1) SERIAL DATA is applied to differential receivers and the software-controlled serial communications controller. Received data is put into FIFO memory, buffered, and sent to bus 1 via the 16 -bit transceiver. Transmit data from bus 1 or RAM is buffered and put into FIFO memory. The serial communications controller takes data from FIFO and applies data to differential drivers for data link transmission.
(2) The serial communications controller controls IU and data link communications. The controller is clocked by a $4.9152-\mathrm{MHz}$ clock derived from the $4.9152-\mathrm{MHz}$ oscillator. The controller receives $20-\mathrm{KHZ}$ CLOCK, 1.
-MHZ CLOCK, and SERIAL DATA from data link system. The controller outputs SERIAL DATA to the data link system. Data from the data link system is converted to parallel data and sent to bus 1. Parallel data for transfer to the data link system is converted to serial data. The controller has a built-in test mode for system verification.
(3) To communicate, PROM generates DATA LINK REQUEST to IUBUS1 (A20). IUBUS1 (A20) responds with DATA LINK ACKNOWLEDGE and DATA LINK ENABLE, which address three PROM. SERIAL COMMUNICATIONS CONTROLLER INTERRUPT is generated at serial communications operation completion. Upper PROM outputs are applied to the multiplexer which addresses RAM segments. Middle PROM puts 8-bit address data on the internal bus. Lower PROM generates CONTROL SIGNALS, DATA LINK REQUEST signal, and receive and transmit data interrupts. CONTROL SIGNALS control data flow through IUDL (A26). Receive data interrupt asserts when data from data link system is put onto bus 1. Similarly, transmit data interrupt is asserted when data from bus 1 or RAM is sent to data link system.
(4) IUDL (A26) connects with bus 1 via the 16 -bit transceiver. RAM loads 16 -bit counter which generates 16 -bit address. Counter output (address bits DBAO-15) is placed on the internal bus. DBAO-7 are applied to 8 -bit latch. DBAO-3 are latched onto bus 1 as address bits (A16-19). DBA4-7 and the latched output (A20-23) are not used. DBAO-15 are latched by 16-bit latch to bus 1 as A0-15. Four of the least significant address bits (A01-04) are buffered and multiplexed to address RAM.
(5) The 8-bit transceiver routes control words between data link system and IU via the controller.


IUDL (A26) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION -Continued

t. 1553R1 (A27). Refer to the 1553B1 (A27) block diagram. Per MIL-STD-1553B, command, status, and data words are 20 bits each: 16 data bits, 3 sync bits, and 1 parity bit Command and status words-are interchanged between CP and IU via 1553B1 (A27) interface. The 1553B1 (A27) converts parallel data to serial data for transmission, or receives serial data and converts to parallel data.
(1) A 16-bit transceiver connects 16-bit IUBUS1 CA20) data (DB00-15B2) to the bit processor; data (SIB00-15) flows in either direction. The bit processor detects bit errors with parity detection and converts data from parallel to serial or serial to parallel. The 1553 transceiver controls serial data input and output of the bit processor. The isolation transformer connects to and isolates the transceiver from the serial data bus.
(2) When 1553B1 (A27) interface is required for data transmission or receiving, 1553 ENABLE from IUBUS1 (A20) is applied to address generation control circuits. The address generation control circuits produce CONTROL SIGNALS for the address generation circuits. The address generation circuits provide address bits AO-19, which are applied to bus 1. 1553 REQUEST from the decoder PROM is sent to IUBUS1 (A20), which then returns 1553 ACKNOWLEDGE to 1553B1 (A27) interface. INIT resets state machine PROM addressing, causing required control signal generation. INIT resets the state machine PROM, causing address word CROMAO-7 to be applied to the decoder PROM which then generates output signals. These signals may consist of CONTROL SIGNALS, 1553 INTERRUPT, or 1553 REQUEST, depending upon the address word. CROMAO-7 is also applied as an input to the state machine, which causes it to output a different address word. This process continues until the next INIT is received.
(3) The hard-wired address input, RTA0-4, is applied to the bit processor and the RTA register. The output of the RTA register, SIB08-12, is applied to the SIB bus. SIBO0-03 is applied to a register, which outputs several signals. They are bus high enable signal BHEN, read/write control signals IORC and IOWC, and 4 bits of address data (A16-19). The output signals are sent to bus 1 and are used to access SRAM. SIB00-15 are registered and output to a 16-bit up counter as STAD01-15. This represents a start address that preloads the counter. The output of the counter is a 4-bit address (AO1-04) to bus 1.
(4) A command word is applied to the 1553B1 (A27) as part of SERIAL DATA from the CP. After it is routed to the bit processor via the isolation transformer and 1553 transceiver, it is placed on the SIB bus. SIBO(007 is applied to a latch. Latch output CMD4 is applied to the decoder PROM. When the bit processor detects a receive command word followed by a specified number of data words (DB00-15B2), a single status word on the SIB bus response is placed on the serial 1553B bus (after message validation). If more than one bit processor is placed on the 1553B bus, only the bit processor with a hard-wired address (RTAO-4) matching the 5-bit address field of the command status word is active at any given time. Similarly, if the bit processor detects a transmit command word, the status word response is again placed on the 1553B interface bus; however, in this case, the status word is followed by a specified number of data words. The data words are formed( by latching the contents of SRAM onto bus 1 for conversion to serial format within the bit processor. The process is concluded by transmitting the serial data to the CP.


1553B1 (A27) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION -Continued

u. BATREG (A.3). Refer to the BATREG (A3) block diagram. BATREG (A3) charges the battery and monitors battery voltage. The +6 Vdc battery supplies battery backup for SRAM memory retention in CP and IU.

BATREG (A3) accepts:

- +28 VDC from system power supply
- +12 VDC from system power supply
- 16-bit address DATA AO-15 from bus 1

BATREG (A3) outputs:

- +5 Vdc normal or +4.5 Vdc backup power to CP and IU memory
- 800 mA constant current for charging +6 Vdc battery
- Power on reset (POR-/)
- POWER GOOD to SRAM (A17)
- Digitized BATTERY CONDITION data bit D10-15 to bus 1
(1) System power supply +28 Vdc input to BATREG (A3) is delayed two seconds and then energizes relay K2. Relay K2 applies ground to logic circuits indicating system power is on. The ground becomes POR-/ and is sent to IUBUS1 (A20). POWER GOOD is output and sent to each SRAM board when +28 volts is applied to BATREG (A3) indicating SRAM boards can be accessed. On/off regulator control and delay energizes relay K3 which applies +16 Vdc to constant current voltage regulator which applies 800 mA constant current to battery for charging. System power supply +12 Vdc is applied to +5 Vdc voltage regulator which powers memory in CP and IU under normal conditions.
(2) If system power should fail, the +6 Vdc battery powers the voltage regulator which maintains +4.5 Vdc output to power memory in CP and IU. Under normal system power, the IU can check battery voltage condition. The IU sends address/data bits and control data for encoding. Address encoding and logic circuitry energizes or deenergized relay K3 to charge battery, enables Comparator circuit to check battery voltage, reads battery voltage condition through voltage divider network, Comparator, buffers, and then outputs reading onto bus 1 .



## 1-75/(1-76 blank)

CHAPTER 2
OPERATING INSTRUCTIONS

Not Applicable.

2-1/(2-2 blank)

CHAPTER 3
OPERATOR MAINTENANCE

Not Applicable.

3-1/(3-2 blank)

CHAPTER 4
ORGANIZATIONAL MAINTENANCE

Not Applicable.

4-1/(4-2 blank)

## CHAPTER 5

## DIRECT SUPPORT MAINTENANCE

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## Section I. REPAIR PARTS, SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

## 5-1. COMMON TOOLS AND EQUIPMENT

For authorized common tools and equipment refer to the Modified Table of Organization and Equipment (MTOE) applicable to your unit.

## 5-2. SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

Refer to Maintenance Allocation (appx B] and TM 11-589501276-23P. A special test fixture must be locally fabricated (appx D). A stopwatch is also required.

## 5-3. REPAIR PARTS I

Repair parts are listed and illustrated in TM 11-5895-1279-23P.

## Section II. TROUBLESHOOTING

## 5-4. TEST EQUIPMENT REQUIRED I

Refer to paragraph(s) 5-1 and 5-2, and test setup diagram(s).

## 5-5. TEST CONNECTIONS

a. Make test setup.
b. Initial Conditions.
(1) Set IUTS ac ON/OFF switch to OFF.
(2) Push control panel POWER ON/OFF switch to OFF.

## NOTE

There are two different operator terminals used in this test setup. One is for system 4 (HP Terminal 2645N given in step (3) thru (6) below and the other for system 1 (HPTerminal 700/43 given in step (7) below):
(3) On operator terminal (HP MODEL 2645N ) set the controls as follows:

| Switch | Set To |
| :--- | :--- |
| CRT monitor | ON |
| DUPLEX | FULL |
| PARITY | NONE |
| BAUD RATE | 9600 |
| Function | disengaged |
| REMOTE | engaged |
| CAPS LOCK | engaged |

(4) Check that all operator terminal lamps, except TRANSMIT, are off.
(5) On operator terminal, press RESET TERMINAL button
(6) Proceed to step (8) below.
(7) On operator terminal (HP MODEL 700/43) proceed as follows:

CHANGE 1 5-2
a Turn operator terminal on.
b Enter setup mode by pressing SHIFT-SETUP.
c Select User Setup mode by pressing function key F1

## NOTE

Data is changed by selecting the appropriate data column using the arrow keys. The space bar will cycle through the available choices for each column.
d Verify the following settings:

| Time: Hour | Not Set |
| :--- | :--- |
| Minute | Not Set |
| Screen Saver | 15 Minutes |
| Screen Attr | Normal |
| Refresh Rate | 72 Hz |
| Cursor On | ON |
| Cursor Type | Blink Box |
| Smooth Scroll | Jump |
| Status Line | ON |
| On Line | ON LINE |

e Select System Setup mode by pressing function key F8.
f Verify the following settings:

| Screen Width | 80 |
| :--- | :--- |
| Multipage | OFF |
| Auto Page | OFF |
| Attr Extent | Line |
| Bgnd Attr | Dim |
| Compatibility | Adds VP/A2 |
| Enhanced Mode | OFF |
| Lead-in Char | ESC |
| EOM Char | NUL |
| Block Term | Us/Cr |
| Auto Scroll | ON |
| Auto Linefeed | OFF |
| Auto Wrap | ON |
| Monitor Mode | OFF |
| Graph Mode | OFF |
| Block Mode | Character |
| Protect Mode | OFF |

g Select Data Communications mode by pressing function key F8


TM 11-5895-1279-13

## 5-5. TEST CONNECTIONS - Continued

(9) Set digital delay/width generator switches:

```
Switch Position
POWER
IREM EN ENGAGED
TRIGGER MORE EXT TRIG
```

Position
ON
ENGAGED
EXT TRIG
(10) Set universal time interval counter (UTIC) switches:

Switch
LINE/STBY ON
FUNCTION
START COM/SEP
GATE
STAT
SAMPLE SIZE
(11) On test fixture, adjust battery potentiometer (pot.) to one-half scale.
(12) Proceed tt paragraph 5-6.

## 5-6. TEST PROCEDURE AND FAULT ISOLATION

a. Use following procedure. The procedure is arranged in four columns.

Column (1). Contains step number. Do not skip steps unless ACTION column (4) directs otherwise.
Column (2). Contains test operation to be performed.
Column (3). Contains normal indication to be observed when procedure has been performed.
Column (4). Prescribes corrective action.
b. Whenever a corrective action has been taken, perform steps 1 through 40 to verify repair.
c. If replacement of a part does not correct fault, reinstall original part before proceeding to next step.
d. Refer to applicable TM issued with the test equipment for operating instructions.

## 5-6. TEST PROCEDURE AND FAULT ISOLATION- Continued

e. Refer to following as required.
(1) FO-1. Component Locations.
(2) FO-2. Motherboard A28.
(3) Appendix C. Wire List.
(4) Appendix D. Illustrated List of Manufactured Items.

## WARNING

Whenever possible, shut off power source before working inside unit to prevent electrical shock.

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
|  | CAUTION |  |  |
|  | Be sure test connections and initial conditions required in paragraph 5-5 are performed before proceeding |  |  |
| 1. | On IUTS, set PROCESSOR SELECT switch to 9 . |  |  |
| 2. | On IUTS, set both ac and dc ON/OFF switches to ON. |  |  |
| 3. | On control panel, push POWER ON/OFF switch to ON. Wait 10 seconds. | IU fan operates | If not, go to step77. |

## CHANGE1 5-5

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

5.

FIGURE 5-2. MAIN MENU
On operator terminal, enter 7 <RETURN>.

TEST EXECUTION
menu ffig. 5-3)
displayed


FIGURE 5-3. TEST EXECUTION MENU

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

7.

On UTIC, adjust FREQ/PERIOD input trigger level until lamp blinks stop trigger lamp starts blinking.
8.

On operator terminal, adjust UTIC to read 2.000 microseconds as follows: UTIC
a. Increase
$+100$
Enter
$+10$
H
$+1$
b. Decrease
-100

-10 | Enter |
| :--- |
| C |
| P |
| $D$ |

FIGURE 5-4. PRI ALINEMENT MESSAGE
-1 D

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued


FIGURE 5-5. IU TEST SELECTION MENU

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued


5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
|  | NOTES <br> - Step 17 starts the IU test program. Prompts in step $18 \mathbf{a}, \mathbf{b}$, and $\mathbf{c}$ will appear during a normal test run. Watch for and follow screen instructions should any other prompts appear while test is running. <br> - If test halts on diagnostic test longer than $\mathbf{3 0}$ seconds, record failed test module number and goto step 49. |  |  |
| 17. | On operator terminal, enter 1 <RETURN> and start stopwatch. | Test data scrolls as test executes |  |
| 18. | Watch for the following messages: | a. PRESS OPINT TEN TIMES THEN PRESS SPACE ON CRT | a. Go to step 19. |
|  |  | b. MOVE RDC CABLE W7 TO IU CONNECTOR J7 THEN ENTER A CONTROL C | $\underline{\text { b }}$. Go to step 21. |
|  |  | c. MOVE RDC CABLE W7 TO IU 23. CONNECTOR J8 THEN ENTER A CONTROL C | c. Go to step 23. |
|  |  | d. NO HARD- <br> WARE ERRORS WERE DETECTED | d. Go to step 25. |
|  |  | e. XX TEST MODULES ENCOUNT ERED HARDWARE ZERO FAULT | e. Go to step 46. |
| 19. | On control panel, press COMPL (OPINT) key 10 times. |  |  |

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

27.

Connect DVM across test fixture pot.


## 5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 28. | Adjust test fixture pot. for +4.7 Vdc reading on DVM. | OFFF displayed |  |
| 29. | On operator terminal enter following: <br> a. OW 50,0002 <RETURN> |  |  |
|  | b. IW 50 <RETURN> |  | a. If not, aline A3 (para 5-7). Return to step 27. |
|  |  |  | b. If present go to step 30 . |
|  |  |  | c. If fault persists, replace and aline A3 para 5-10 and 5-7) Return to step 27. |
| 30. | Repeat steps 28 and 29 for following voltages: |  | a. If not, aline A3 (para 5-7). Return to step 27. |
|  |  | Display | b. If present, go to step 31. |
|  |  | 1FFF |  |
|  |  | 3 FFFF | c. If fault persists, replace |
|  |  | $\begin{aligned} & \text { 7FFF } \\ & \text { FFFF } \end{aligned}$ | and aline A3 (para 5-10 and 5-7). Repeat test procedure. |
| 31. | Adjust test fixture pot. for +5.4 Vdc on DVM. |  |  |
| 32. | Disconnect cable W15 from IU J6. |  |  |
| 33. | Disconnect DVM from test fixture pot. |  |  |
|  |  | -12 |  |

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 34. | Using DVM, check voltage on IU between J6-99(+) and J6-98(-). | $+5.05+.05 \mathrm{Vdc}$ | a. If not, aline A3 (para 5-7). Return to step 27. <br> b. If present, go to step 35. <br> c. If fault persists, replace and aline A3 para 5-10 and 5-7. Return to step 27. |
| 35. | Reconnect cable W15 to IU J6. |  |  |
| 36. | Reconnect DVM to test fixture pot. |  |  |
| 37. | Observe DVM voltage indication. When voltage drops to zero, stop time measurement and b. If within record time. limits, go to step 38. | 26 to 34 min | a. If not, go to step 51. |
| 38. | On operator terminal, enter: |  |  |
|  | a. OW 50,0004 <RETURN> <br> b. OW 50,0000 <RETURN > DVM rises | Voltage reading on |  |
|  | NOTE <br> Read and clearly understand next step before doing it. |  |  |
| 39. | Observe DVM and slowly turn test fixture pot. cw. Stop turning pot. at instant voltage goes to zero. | Voltage rises to a value between +6.9 and +7.1 Vdc , then drops to zero | a. If not, go to step 51. |
| 5-13 |  |  |  |

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 40. | End test: |  |  |
|  | a. Remove test setup power. |  |  |
|  | b. Remove IU from test setup. |  |  |
|  | c. If removed, install covers para 5-9. |  |  |
|  | PART II. FAULT ISOLATION |  |  |
|  | A. NENU DOES NOT APPEAR |  |  |
| 41. | Replace A18 (para 5-10). Repeat test procedure. | Menu displayed (fig. 5-5 | If replacing A18 does not correct fault, go to step42. |
| 42. | Check IU voltages: |  | a. If not, send IU to higher level maintenance. |
|  | b. Using DVM check voltage at: |  | $\underline{\text { b }}$. If present, go to step 43. |
|  | Test points (FO-2) Vdc |  |  |
|  | E4 (gnd) to E3 <br> E4 (gnd) to XA01.55 | $\begin{aligned} & +5+.15 \\ & +12+.15 \end{aligned}$ |  |
|  | E4 (gnd) to XA01.59 <br> E5 (gnd) to XA01.101 | $\begin{aligned} & -12+.15 \\ & -5+.15 \end{aligned}$ |  |
| 43. | Replace W5 (para 5-18. Repeat test procedure. | Menu displayed (fig. 5-5) | If replacing W5 does not correct fault, send IU to higher level maintenance. |



5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued


FIGURE 5-7. TYPICAL ERROR/NO ERROR MESSAGES

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
|  | NOTES <br> TASK NUMBERS of TEST MODULES that failed other than or in addition to test numbers 53 to 79 are FIRST priority IU errors. <br> - TASK NUMBERS 53 to 79 only, and any error message which indicates DIGA1, DIGA2, and/or DIGB bad, take SECOND priority over any other IU errors. <br> - TASK NUMBERS 53 to 79 only, and any error message which indicates DOA, TOIA, TOIB, and/or CTRLA bad, take THIRD priority over other IU errors. |  |  |
| 48. | Read error message. Note and record TASK NUMBER(s) and CCA(s) that failed. | a. TASK NUMBERS of TEST MODULES that failed <br> b. CCA(s) that failed | a. If any TASK NUMBER(s) other than or in addition to 53 to 79 fail, go to step 49 . <br> b. If any TASK NUMBER(s) 53 to 79 and DIGA1, DIGA2, and/or DIGB fail, aline front end (para 5-8). <br> c. If front end alinement fails, go to step 52 . <br> d. If any TASK NUMBER(s) 53 to 79 and DOA, TOIA, TOIB, and/or CTRLA fail, go to step 52. |

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 49. | Using table 5-1 <br> a. Locate failed TASK NUMBER in TASK NO. Column. |  | a. Replace by priority (1, 2, 3) suspected CCA(s) (para 5-10). Repeat test procedure. |
|  | b. In failed TASK NUMBER row, find numbers $(1,2,3)$ which identify suspect CCA(s). |  | b. If replacing and testing all suspect CCAs $(1,2,3)$ does not correct fault, go to step 50. |
| 50. | Using table 5-2 <br> a. Locate failed TASK <br> NUMBER in TASK NO. column. |  | a. Replace by priority (1, 2) suspected wire harness(es) and/or connectors) (para 5-13 through 5-21). Repeat test procedure. |
|  | b. In failed TASK NUMBER row, find numbers $(1,2)$ which identify suspect wire harness(es) and connector(s). |  | b. If fault persists, send IU to higher level maintenance. |
|  | D. VOLTAGE RISE/FALL TIME |  |  |
| 51. | Replace and aline A3 (para 5-10 an 5-7). Repeat test procedure. | 26 to 34 minutes | If fault persists, send IU to higher level maintenance. |
|  | 5-18 |  |  |

TABLE 5-1. TEST MODULE/CCA MATRIX

|  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |  |
| mances |  |  |  |  |  |  |  |  |  |  |  |
| 0.0.0. |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | ' |  |  |  |  |  |  |
| 12, 2.40 |  |  |  |  |  |  |  | , | , |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| \%r, |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | ' | 2 | - |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| \% |  |  |  |  |  |  |  |  |  |  |  |
| 0,1.2 |  |  |  |  |  |  |  | 2 |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | $\cdot 1$ |  |  | 2 |  |  |  | - |

TABLE 5-2. TEST MODULE/WIRE HARNESS MATRIX


5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
|  | E. TASK NUMBER(S) 53 TO 79 FAILED |  |  |
|  | NOTE |  |  |
|  | On operator terminal, cursor must be placed at end of last test run. This clears data from display memory. Failure to do so may cause subsequent displays to be distorted. |  |  |
| 52. | On operator terminal, press ROLL UP key until cursor is positioned at end of test run. | XX TEST MODULES ENCOUNTERED HARDWARE FAULT |  |
| 53. | On operator terminal, enter: |  |  |
|  | a. <RETURN> | a. IU TEST EXECUTION menu displayed (fiq. 5-6 |  |
|  | b. M <RETURN> | b. IU TEST SELECTION menu displayed (fig.5-5) |  |
|  | c. 2 <RETURN> | c. IU TEST EXECUTION menu displayed (fig. 5-6 |  |
| 54. | On operator terminal, enter 1 <RETURN>. | The first test result message displayed (fig.5-7) |  |

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued


FIGURE 5-8. TYPICAL NO ERROR DATA DISPLAY TEST
56.

Analyze ERROR message.

ERROR MESSAGES
a. DIGA1, DIGA2,

DIGB, and DOA-BAD
b. TOIA and

TOIB-BAD
a. Go to step 57 .
b. Go to step 62.

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 56. | Cont | c. DIGA1-BAD | c. Go to step 66. |
|  |  | d. DIGA2-BAD | d. Go to step 68. |
|  |  | e. DIGB-BAD | e. Go to step 69. |
|  |  | f. DOA-BAD | f. Go to step 67. |
|  |  | g. TOIA-BAD | g. Go to step 70. |
|  |  | h. TOIB-BAD | h. Go to step 71. |
|  |  | i. CTRLA-BAD | i. Go to step 72. |
|  |  | i. DIGB CTRLA, <br> TOIA, 73, and TOIB-BAD | i. Go to step |
|  |  | k. DIGA1, DIGA2, DOA, TOIA, TOIB, and CTRLA-BAD | k. Go to step 75. |
| 57. | Check A7 as follows: <br> a. Replace A7 para 5-10. <br> b. Aline front end para 5-8). <br> c. Perform steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original A7. Go to step 58. |
|  |  |  | b. If correct, go to step 25. |
| 58. | Check A9 as follows: <br> a. Replace A9 (para 5-10). | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original A9. Go to step 59. |

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 59. | b. Repeat steps 1 through 18. <br> Check A5 as follows: <br> a. Replace A5 para 5-10. <br> b. Aline front end para 5-8. <br> c. Perform steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | b. If correct, go to step 25 . <br> a. If not, reinstall original A5. Go to step 60. <br> b. If correct, go to step 25. |
| 60. | Check A6 as follows: <br> a. Replace A6 (para 5-10. <br> b. Aline front end para 5-8). <br> c. Perform steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If TASK NUMBERS that failed are from 53 to 67, reinstall A6. Send IU to higher level maintenance. <br> b. If TASK NUMBERS that failed are from 68 to 79 , reinstall A6. Go to step 61. <br> c. If correct, go to step 25. |
| 61. | Using table 5-2 <br> a. Locate failed TASK NUMBER in TASK NO. column. <br> b. In failed TASK NUMBER row, find numbers $(1,2)$ which identify suspect wire harness(es) and connector(s). |  | a. Replace by priority (1, 2) suspected wire harness(es) and/or connector(s) (para 5-13 Through 5-21). Repeat test procedure. <br> b. If fault persists, send IU to higher level maintenance. |

## 5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 62. | Check A1 as follows: <br> a. Replace AI para 5-10. <br> b. Repeat steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original <br> A1. Go to step 63. <br> b. If correct, go to step 25. |
| 63. | Check A4 as follows: <br> a. Replace A4 (para 5-10). <br> b. Repeat steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original A4. Go to step 64. <br> b. If correct, go to step 25. |
| 64. | Check W14 as follows: <br> a. Replace W14 (para 5-19). <br> b. Repeat steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original W14. Go to step 65. <br> b. If correct, go to step 25 . |
| 65. | Check OSC G1 as follows: <br> a. Replace OSC G1 (para 5-12). <br> b. Repeat steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original OSC G1. Send IU to higher level maintenance. <br> b. If correct, go to step 25 . |
| 66. | Check A5 as follows: <br> a. Replace A5 (para 5-10. <br> b. Aline front end (para 5-87). <br> c. Perform steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original A5. Go to step 67. <br> b. If correct, go to step 25. |
| 67. | Check A9 as follows: <br> a. Replace A9 (para 5-10). <br> b. Perform steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If TASK NUMBERS that failed are from 53 to 67 , reinstall A9. Send IU to higher level maintenance. |

## 5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 67. | Cont |  | b. If TASK NUMBERS that failed are from 68 to 79 , reinstall A9. Go to step 60. <br> c. If correct, go to step 25. |
| 68. | Check A6 as follows: <br> a. Replace A6 (para 5-10). <br> b. Aline front end (para 5-8). go to step 25. <br> c. Perform steps 1 through 18 . | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original A6. Go to step 66. <br> b. If correct, |
| 69. | Check A7 as follows: <br> a. Replace A7 (para 5-10. <br> b. Aline front end para 5-8. <br> c. Perform steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If TASK NUMBERS that failed are from 53 to 67 , reinstall A7. Send IU to higher level maintenance. <br> b. If TASK NUMBERS that failed are from 68 to 79 , reinstall A6. Go to step 59. <br> c. If correct, go to step 25. |
| 70. | Check A1 as follows: <br> a. Replace A1 (para 5-10). <br> b. Repeat steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original AI. Go to step 63. <br> b. If correct, go to step 25. |

## 5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 71. | Check A4 as follows: <br> a. Replace A4 (para 5-10. <br> b. Repeat steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original A4. Send IU to higher level maintenance. <br> b. If correct, go to step 25. |
| 72. | Check A12 as follows: <br> a. Replace A12 (para 5-10). <br> b. Repeat steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original A12. Send IU to higher level maintenance. <br> b. If correct, go to step 25. |
| 73. | Check A7 as follows: <br> a. Replace A7 (para 5-10). <br> b. Aline front end para 5-8. <br> c. Perform steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original A7. Go to step 74. <br> b. If correct, go to step 25. |
| 74. | Check A12 as follows: <br> a. Replace A12 (para 5-10). <br> b. Repeat steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original A12. Go to step 62. <br> b. If correct, go to step 25. |
| 75. | Check A12 as follows: <br> a. Replace A12 (para 5-10). <br> b. Repeat steps 1 through 18. | NO HARDWARE ERRORS WERE DETECTED | a. If not, reinstall original A12. Go to step 76. <br> b. If correct, go to step 25. |

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued


## 5-7. A3 ALINEMENT



FIGURE 5-9. A3 ADJUSTMENT POINTS
7.

On control panel, push POWER ON/OFF switch to ON.

## 5-7. A3 ALINEMENT - Continued



FIGURE 5-10. A3 PARTS LOCATION

5-7. A3 ALINEMENT - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 10. | Using DVM, check voltage between R1 (pin 1) and TP5 (gnd). | +6.5 Vdc | a. If not, adjust R8. <br> b. If adjustment fails, replace and aline A3 para 5-10 and 5-7. <br> c. If voltage is correct, go to step 11. |
| 11. | On control panel, push POWER ON/OFF switch to OFF. |  |  |
| 12. | Remove A3 from card extender. |  |  |
| 13. | Remove card extender from A3 slot. |  |  |
| 14. | Install A3 (bara 5-10). |  |  |
| 15. | Repeat test procedure (para 5-6). |  |  |

## 5-8. FRONT END ADJUSTHENTS/ALINEMENTS

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :--- | :--- | :--- | :--- |
| 1. | Remove top cover (para 5-9). <br> 2. <br> Locate and identify TP1, TP2, TP3, R3 and <br> R5 on A5, A6 and A7 (fig. 5-11). |  |  |

FIGURE 5-11. FRONT END ADJUSTMENT LOCATIONS

Using DVM, check voltages between following test points on both A5 and A6 (fig. 5-11):
a. TP1 - TP3 (gnd)
b. TP2 - TP3 (gnd)
$5.40+.01$
$5.00+.10$
replace failed CCA (para 5-10). Aline front end (para 5-8.

## 5-8. FRONT END ADJUSTNENTS/ALINENENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 4. | Using DVM, check voltages between following test points on A7 (fig. 5-11): <br> a. TP1 - TP3 (gnd) <br> b. TP2 - TP3 (gnd) <br> On operator te test run. This do so may cau | $\begin{aligned} & 5.00+.10 \\ & 5.40+.01 \end{aligned}$ <br> NOTE <br> al, cursor must be placed at end of last data from display memory. Failure to bsequent displays to be distorted. | a. If not, adjust R3. <br> b. If not, adjust R5. <br> c. If adjustment fails, replace A7 (para 5-10). Aline front end [para 5-8). |
| 5. | On operator terminal, press ROLL UP key until cursor is positioned at end of TEST RUN. | XX TEST MODULES ENCOUNTERED HARDWARE FAULT |  |
| 6. | On operator terminal, enter <RETURN>. | IU TEST EXECUTION menu displayed (fiq. 5-6) |  |
| 7. | On operator terminal, enter M <RETURN>. | IU TEST SELECTION menu displayed (fig. 5-5) |  |
| 8. | On operator terminal, enter $\mathrm{N}<$ RETURN $>$. | CCA MENU <br> displayed (fig. 5-12 |  |

## 5-8. FRONT END ADJUSTNENTS/ALINENENTS - Continued



FIGURE 5-12. CCA MENU
9.

On operator terminal, enter N < RETURN>

MODULE SELECTION MENU displayed (fig. 5-13)

PWR UP PASSED
$P R O C=I U$
hardware test package
hodule selection
FUNCTION: HOUULE SELECTION

EnTER 1 TO RESET CUSTOM TEST


FIGURE 5-13. MODULE SELECTION MENU 1

## 5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued



FIGURE 5-14. MODULE SELECTION MENU 2

On operator terminal, enter:
a. 1 <RETURN>
b. 53 <RETURN>
c. $90<$ RETURN>
d. 68 <RETURN>
e. 90 <RETURN>

MODULE SELECTION
MENU 2 redisplayed after each entry (fig. 5-14)

## 5-8.

FRONT END ADJUSTMENTS/ALINEMENTS - Continued


FIGURE 5-15. AVAILABLE OPTIONS MENU
13.
14.
15.

On operator terminal, enter:
a. $1<$ RETURN $>$
b. $5<$ RETURN $>$
c. $9<$ RETURN $>$

On operator terminal, enter M <RETURN>

On operator terminal, enter 8 <RETURN> .

AVAILABLE OPTIONS
menu redisplayed after each entry (fig. 5-15)

IU TEST SELECTION menu displayed (fig. 5-5
IU TEST EXECUTION menu displayed (fig. 5-6)

5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :--- | :--- | :--- | :--- |
| 16. | On operator terminal, enter <br> $1<$ RETURN $>$. | Test 53/68 display <br> begins scrolling on <br> screen[(fig. 5-16) |  |


| 00053: IFPDG1 :NO ERROR |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00090: | TEST | \#01 |  |  |  |  |  |  |  |  |  |
| DF 1 | DF2 | DF3 | FRU | LA | REL | DOA | PW | PRI | SB | CW | PNL |
| 6 A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | 04 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | 04 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 0.1 | 01 | 40 |
| 00068: IFPDG16 6 : DIGA1-BAD, DIGA2-*, DIGB-*, DOA-*, TOIA-*, TOI-*, CTRLA-*00090: TEST $\# 01$ |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| DF1 | DF2 | DF3 | FRU | LA | REL | D0A | PW | PRI | SB | CW | PNL |
| 6A | D4 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D9 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D9 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D9 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | 09 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6A | D9 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D9 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | 09 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | 09 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6A | D9 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D9 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6A | 09 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6A | D9 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | D9 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | 09 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6 A | 09 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |
| 6A | D9 | EB | 29 | 15 | 03 | 3964 | 0011 | 900 | 01 | 01 | 40 |

FIGURE 5-16. TEST 53/68 DISPLAY

5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 17. | Locate and identify following columns on displays (fig. 5-16). <br> DF1 <br> DF2 <br> DF3 <br> FRU <br> LA <br> In steps 18 through 20 observ required adjustments. | Each column contains series of hexadecimal values. Those values have a tolerance of $\pm 3$ bits. <br> EXAMPLE: $\begin{aligned} 6 A & -(67,68,69) \\ & +(6 B, 6 C, 6 D) \end{aligned}$ <br> NOTE <br> ta scrolling on screen while | making |
| 18. | Check values under following columns fig. 5-16: <br> Column <br> DF1 <br> DF2 | $\begin{aligned} & \text { Display } \\ & 6 \mathrm{~A}-(67,68,69) \\ & +(6 \mathrm{~B}, 6 \mathrm{C}, 6 \mathrm{D}) \end{aligned} \quad \begin{aligned} & \\ & \mathrm{D} 4-(\mathrm{D} 1, \mathrm{D} 2, \mathrm{D} 3) \\ & \quad+(\mathrm{D} 5, \mathrm{D}, \mathrm{D} 7) \end{aligned}$ | a. If not, adjust A5R3 (fig. 5-11. <br> b. If adjustment fails, replace A5 para 510). Aline front end (para 5-8). |
| 19. | Check values under following columns (fig. 5-16): $\frac{\text { Column }}{\text { DF3 }}$ <br> FRU | $\begin{aligned} & \quad \text { Display } \\ & \text { EB -(EB,E9,EA) } \\ & +(\mathrm{EC}, \mathrm{ED}, \mathrm{EE}) \\ & \\ & 29-(26,27,28) \\ & +(2 \mathrm{~A}, 2 \mathrm{~B}, 2 \mathrm{C}) \end{aligned}$ <br> 5-38 | a. If not, adjust A6R3 (fig. 5-11). <br> b. If adjustment fails, replace A6 para 5-10. Aline front end (para 5-8). |

5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 20. | Check values under LA column [fig. 5-16). | $\begin{array}{r} 15-(12,13,14) \\ \quad+(16,17,18) \end{array}$ | a. If not, adjust A7R3 (fig. (5-11). <br> b. If adjustment fails, replace A7 (para 5-10). Aline front end (para 5-8). |
| 21. | On operator terminal, hold down <CTRL> key and press C. | Scrollings stops |  |
| 22. | On operator terminal, enter: <br> a. <RETURN> | a. IU TEST EXECUTION menu displayed (fig. 5-6) |  |
|  | b. $\mathrm{M}<$ RETURN> | b. IU TEST SELECTION menu displayed (fig. 5-5 |  |
|  | c. $\mathrm{N}<$ RETURN $>$ | $\begin{aligned} & \text { c. CCA MENU } \\ & \text { displayed fig. } 5-12 \text { ( } \end{aligned}$ |  |
|  | d. $\mathrm{N}<$ RETURN $>$ | d. MODULE SELECTION \#1 menu displayed ffig. 5-13 |  |
| 23. | On operator terminal, <br> a. $\mathrm{N}<$ RETURN> | MODULE SELECTION enter: \#2 menu redisplayed after each entry (fig. 5-14) |  |
|  | c. $55<$ RETURN $>$ <br> d. $90<$ RETURN $>$ <br> e. $70<R E T U R N>$ <br> f. $90<$ RETURN> |  |  |
|  |  | 5-39 |  |

5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 24. | On operator terminal, enter: <br> a. $\mathrm{N}<$ RETIURN $>$ <br> b. $1<$ RETURN $>$ <br> c. $5<$ RETURN> <br> d. $9<$ RETURN $>$ | AVAILABLE OPTIONS menu redisplayed after each entry (fig. 5-15). |  |
| 25. | On operator terminal, enter: <br> a. $M<R E T U R N>$ <br> b. $8<$ RETURN $>$ <br> c. $1<$ RETURN $>$ | a. IU TEST SELECTION menu displayed (fig. 5-5 <br> b. IU TEST EXECUTION menu displayed (fig. 5-6 <br> c. Test 55/70 display begins ,=/ scrolling on screen (fig. 5-17 <br> NOTE |  |

In steps 26 through 28 observe data scrolling on screen while making required adjustments.
26.

Check values under following columns (fig. 5-17):

## Column

DF1

DF2

## Display

$95-(92,93,94)$ $+(96,97,98)$
$2 \mathrm{C}-(29,2 \mathrm{~A}, 2 \mathrm{~B})$
+(2D,2E,2F)
a. If not, adjust A5R3 (fig. 5-11.
b. If adjustment fails, replace A5 (para 5-10). Aline front end (para 5-8).

5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued


| 00055: IFPDG3 : NO ERROR |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00090: TEST \#03 |  |  |  |  |  |  |  |  |  |  |  |
| DF 1 | DF2 | DF 3 | FRU | LA | REL | OOA | PW | PRI |  |  |  |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | $\begin{aligned} & \text { PNL } \\ & \text { CO } \end{aligned}$ |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 |  |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | Co |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | co |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 01 | C0 |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | CO |
| 95 | ${ }^{2} \mathrm{C}$ | 16 | 55 | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | co |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | CO |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | CO |
| 95 95 | 2 C | 16 | 55 | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | co |
| 95 | 2 C | 16 | 55 55 | 40 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | CO |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | CO |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069 E | 1001 | 8000 8000 | 01 | 01 | CO |
| 95 | 2C. | 16 | 55 | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | CO |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069 E | 1001 | 80000 | 01 | 01 | CO |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | CO |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| DF1 | DF2 | DF3 | FRU | LA | REL | OOA | PW |  |  |  |  |
| 95 | 2 C | 16 | 55 | 40 | 03 | 069E | 1001 | 8000 | $01$ | $01$ | $\begin{aligned} & \text { NLL } \\ & \text { CO } \end{aligned}$ |
| 95 | 2 C | 10 | 4 F | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | CO |
| 95 | 2 C | 10 | 4F | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | CO CO |
| 95 | 2 C | 10 | 4 F | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | CO |
| 95 | 2 C | 10 | 4 F | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | C0 |
| 95 | 2 C | 10 | 4F | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | co |
| 95 95 | 2 C | 10 | 4 F | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | C0 |
| 95 | 2 C | 10 | 4 F | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | CO |
| 95 | 2 C | 10 | 4 F | 40 | 03 03 | 069E | 1001 | 8000 | 01 | 01 | CO |
| 95 | 2 C | 10 | 4 F | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | C0 |
| 95 | 2 C | 10 | 4F | 40 | 03 | 069E | 1001 | 8000 8000 | 01 | 01 | CO |
| 95 | 2 C | 10 | 4 F | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 01 | CO |
| 95 | 2 C | 10 | 4F | 40 | 03 | 069E | 1001 | 8000 8000 | 01 | 01 01 | CO |
| 95 | 2 C | 10 | 4F | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | C0 |
| 95 | 2 C | 10 | 4F | 40 | 03 | 069E | 1001 | 8000 | 01 | 01 | C0 |
| 95 | 2 C | 10 | 4F | 40 | 03 | 069 E | 1001 | 8000 | 01 | 01 | CO |

FIGURE 5-17. TEST 55/70 DISPLAY

## 5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 27. | Check values under following columns (fig. 5-17): |  |  |
|  | $\frac{\text { Column }}{\text { DF3 }}$ | $\begin{aligned} & \frac{\text { Display }}{16-(13,14,15)} \\ & \quad+(17,18,19) \end{aligned}$ | $\begin{aligned} & \text { a. If not, adjust A6R3 } \\ & \text { (fig. 5-11). } \end{aligned}$ |
|  | FRU | $\begin{array}{r} 55-(52,53,54) \\ +(56,57,58) \end{array}$ | b. If adjustment fails, replace A6 (para 5-10). Aline front end (para 5-8). |
| 28. | Check values under LA column fig. 5-17. | $\begin{array}{r} 40-(3 \mathrm{D}, 3 \mathrm{E}, 3 \mathrm{~F}) \\ \\ +(41,42,43) \end{array}$ | a. If not, adjust A7R3 (fig. 5-11. |
|  |  |  | b. If adjustment fails, replace A7 (para 5-10. Aline front end (para 5-8). |
| 29. | On operator terminal, hold down <CTRL> key and press C. | Scrolling stops |  |
| 30. | On operator terminal, enter: |  |  |
|  | a. <RETURN> | a. IU TEST <br> EXECUTION menu displayed (fig. 5-6 |  |
|  | b. M <RETURN> | b. IU TEST SELECTION menu displayed (fig. 5-5) |  |
|  | c. $\mathrm{N}<$ RETURN $>$ | $\begin{aligned} & \text { c. CCA MENU } \\ & \text { displayed ffig. } 5-12 \end{aligned}$ |  |
|  | d. $\mathrm{N}<$ RETURN $>$ | $\begin{aligned} & \text { d. MOD)ULE } \\ & \text { SELECTION \#1 (fig. 5-13 } \\ & \text { menu displayed } \end{aligned}$ |  |

5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 31. | On operator terminal, enter: <br> a. $\mathrm{N}<$ RETURN $>$ <br> b. $1<$ RETURN $>$ <br> c. $56<$ RETURN> <br> d. $90<R E T U R N>$ <br> e. $71<R E T U R N>$ <br> f. $90<$ RETURN> | MODULE <br> SELECTION \#2 menu redisplayed after each entry (fig. 5-14) |  |
| 32. | On operator terminal, enter: <br> a. $\mathrm{N}<$ RETURN $>$ <br> b. $1<$ RETURN $>$ <br> c. $5<$ RETURN $>$ <br> d. $9<$ RETURN $>$ | AVAILABLE OPTIONS menu redisplayed after each entry (fig. 5-15) |  |
| 33. | On operator terminal, enter: <br> a. $M<R E T U R N>$ <br> b. 8 <RETURN> <br> c. $1<$ RETURN> | a. IU TEST SELECZTION menu displayed (fig. 5-5 <br> b. IU TEST EXECUTION menu displayed (fig. 5-6 <br> c. Test 56/71 display begins scrolling on screen (fig. 5-18) |  |

5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :--- | :--- | :--- | :--- |
|  |  |  |  |


| 00056: IFPDG4 : DIGA1-BAD, DIGA2-*, DIGB-*, DOA-*, TOIA-*, TOI-*, CTRLA-* |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00090: | TEST | \#04 |  |  |  |  |  |  |  |  |  |
| DF1 | DF2 | DF3 | FRU | LA | REL | DOA | PW | PRI | SB | CW | PNL |
| AA | AA | 29 | 29 | 55 | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | D5 | 29 | 6 6 | 02 | $32 C 5$ | 1800 | 10000 | 01 | 01 | 80 |
| $A A$ | AA | D5 | 29 | 6A | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | D5 | 29 | 6 A | 02 | 32 C 5 | 1300 | 10000 | 01 | 01 | 80 |
| AA | AA | D5 | 29 | 6 A | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| $A \mathrm{~A}$ | AA | D5 | 29 | 6A | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 30 |
| AA | AA | D5 | 29 | 6A | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | D5 | 29 | 6 A | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| $A A$ | AA | D5 | 29 | 6 A | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | MA | D5 | 29 | 6A | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | A | 05 | 29 | 6 A | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | 05 | 29 | 6 A | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | D5 | 29 | 6 A | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | U5 | 29 | 6 A | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | MA | D5 | 29 | 6 6A | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | D5 | 29 | 6 A | 02 | $32 C 5$ | 1800 | 10000 | 01 | 01 | 80 |
| AA | $A A$ | D5 | 29 | 6A | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| 00071 : | IFPDGI | 19 : N0 | ROR |  |  |  |  |  |  |  |  |
| 00090: | TEST | \#04 |  |  |  |  |  |  |  |  |  |
| DF1 | DF 2 | DF 3 | FRU | LA | REL | DOA | PW | PRI | SB | CH | PNL |
| AA | AA | 29 | 29 | 55 | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | 05 | 29 | 58 | 02 | 32.5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | 05 | 29 | 58 | 02 | 32C5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | D5 | 29 | 58 | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | D5 | 29 | 58 | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | 05 | 29 | 58 | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | 05 | 29 | 58 | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | D5 | 29 | 58 | 02 | $32 C 5$ | 1800 | 10000 | 01 | 01 | 80 |
| AA | $A A$ | D5 | 29 | 58 | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | 05 | 29 | 58 | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | D5 | 29 | 53 | 02 | $32 C 5$ | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | 05 | 29 | 58 | 02 | 32 C 5 | 1800 | 10000 | 01 | 01 | 80 |
| $A A$ | AA | D5 | 29 | 58 | 02 | $32 \mathrm{C5}$ | 1800 | 10000 | 01 | 01 | 80 |
| $A A$ | AA | 05 | 29 | 58 | 02 | $32 C 5$ | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | 1.5 | 29 | 58 | 02 | 3205 | 1800 | 10000 | 01 | 01 | 80 |
| nA | AA | 05 | 29 | 58 | 02 | $32 C 5$ | 1800 | 10000 | 01 | 01 | 80 |
| AA | AA | 05 | 29 | 58 | 02 | $32 C 5$ | 1800 | 10000 | 01 | 01 | 80 |

FIGURE 5-18. TEST 56/71 DISPLAY

5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 34. | NOTE <br> In steps 34 through 36 observe data scrolling on screen while making required adjustments. |  |  |
|  | Check values under following columns fig. 5-18): |  |  |
|  | $\frac{\text { Column }}{\text { DF1 }}$ | $\begin{gathered} \text { Display } \\ A A-(A 7, A 8, A 9) \\ +(A B, A C, A D) \end{gathered}$ | a. If not, adjust A5R3 fig. 5-11. |
| 35. | DF2 | $\begin{aligned} & A A-(A 7, A 8, A 9) \\ & +(A B, A C, A D) \end{aligned}$ | b. If adjustment fails, replace A5 (para 5-10). Aline front end (para 5-8). |
|  | Check values under following columns (fig. 5-18): |  |  |
|  | $\frac{\text { Column }}{\text { DF3 }}$ | $\begin{gathered} \text { Display } \\ \text { D5 (D2,D3,D4) } \\ \text { +(D6,D7,D8) } \end{gathered}$ | a. If not, adjust A6R3 (fig. 5-11). |
|  | FRU | $\begin{gathered} 29-(26,27,28) \\ \quad+(2 A, 2 B, 2 C) \end{gathered}$ | b. If adjustment fails, replace A6 (para 5-10). Aline front end (para 5-8). |
| 36. | Check values under LA column fig. 5-18). | $\begin{aligned} & 55-(52,53,54) \\ & +(56,57,58) \end{aligned}$ | $\begin{aligned} & \text { a. If not, adjust A7R3 } \\ & \text { [fig. 5-11. } \end{aligned}$ |
|  | On operator terminal, hold down <CTRL> key and press C. |  | b. If adjustment fails, replace A7 (para 5-10). Aline front end para 5-8 |
| 37. |  | Scrolling stops |  |
|  |  |  |  |

5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 38. | On operator terminal, enter: <br> a. <RETURN> | a. IU TEST EXECUTION menu displayed (fig. 5-6) |  |
|  | b. IU TEST | b. $M<$ RETURN $>$ SELECTION menu displayed (fig. 5-5) |  |
|  | c. $\mathrm{N}<$ RETURN $>$ | displayed (fig. $5-12$ |  |
|  | d. $\mathrm{N}<$ RETURN $>$ | d. MODULE SELECTION \#1 menu displayed (fig. 5-13) |  |
| 39. | On operator terminal, enter: <br> a. $N<R E T U R N>$ <br> b. $1<$ RETURN> | MODULE <br> SELECTION \#2 <br> menu redisplayed after each entry (fig. 5-14) |  |
|  | c. 57 <RETURN> |  |  |
|  | d. $90<$ RETURN> |  |  |
|  | e. $69<R E T U R N>$ <br> f. $90<$ RETURN> |  |  |
| 40. | On operator terminal, enter: <br> a. $N<$ RETURN $>$ <br> b. $1<$ RETURN> | AVAILABLE OPTIONS menu redisplayed after each entry (fig. 5-15) |  |
|  | c. $5<$ RETURN $>$ <br> d. $9<$ RETURN $>$ |  |  |

5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued


5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :--- | :--- | :--- | :--- |
|  |  |  |  |


| :NO ERROR |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00090: | TEST | \#05 |  |  |  |  |  |  |  |  |  |
| DF 1 | DF2 | DF3 | FRU | LA | REL | DOA | PW | PRI | SB | CW | PNL |
| 2 C | 95 | 56 | 80 | 6 A | 03 | 378B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 6 A | 03 | 378B | 1001 | 8000 | 01 | 01 | 00 |
| 2C | 95 | 56 | 80 | 6 A | 03 | 378B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 6 A | 03 | 378B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 6 A | 03 | $378 B$ | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 6 A | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2C | 95 | 56 | 80 | 6 A | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 59 | 56 | 80 | 6 A | 03 | 378B | 1001 | 3000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 6 A | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2C | 95 | 56 | 80 | 6 A | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 30 | 6 A | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2C | 95 | 56 | 80 | 6 A | 03 | 378 B | 1001 | 3000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 6 A | 03 | 3788 | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 6 A | 03 | 3788 | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 6 A | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 6 A | 03. | 378B | 1001 | 3000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 6 A | 03 | 378 B | 1001 | 8000 | 01 | 01 |  |
| 00069: | IFPDG1 | : DIGAl-*, DIGA2-*, DIGE-BAD, DOA-* |  |  |  |  |  |  |  |  |  |
| 00090: | TEST | \#03 |  |  |  |  |  |  |  |  |  |
| DF l | DF2 | DF3 | FRU | LA | REL | DOA | PW | PRI | SB | CW | PNL |
| 2 C | 95 | 56 | 80 | 6 A | 03 | 378 B | 1001 | 3000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 3788 | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 3788 | 1001 | 8000 | 01 | 01 | 00 |
| 2C | 95 | 56 | 80 | 55 | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 378 B | 1001 | 3000 | 01 | 01 | 00 |
| 2C | 95 | 56 | 80 | 55 | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 3788 | 1001 | 8000 | 01 | 01 | 00 |
| 2C | 59 | 56 | 80 | 55 | 03 | 3788 | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 30 | 55 | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 378B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 378B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 378B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 378 B | 1001 | 3000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |
| 2 C | 95 | 56 | 80 | 55 | 03 | 378 B | 1001 | 8000 | 01 | 01 | 00 |

FIGURE 5-19. TEST 57/69 DISPLAY

## 5-8. FRONT END ADJUSTMENTS/ALINEMENTS - Continued

| STEP | PROCEDURE | INDICATIONS | ACTION |
| :---: | :---: | :---: | :---: |
| 43. | Check values under following columns (fig. 5-19): |  |  |
|  | $\frac{\text { Column }}{\text { DF3 }}$ | $\begin{array}{r} \text { Display } \\ 56-(53,54,55) \\ +(57,58,59) \end{array}$ | a. If not, adjust A6R3 fig. 5-11. |
|  | FRU | $\begin{array}{r} 80-(7 \mathrm{D}, 7 \mathrm{E}, 7 \mathrm{FF}) \\ +(81,82,83) \end{array}$ | b. If adjustment fails, replace A6 (para 5-10). Aline front end (para 5-8). |
| 44. | Check values under LA column (fig. 5-19. | $\begin{gathered} 6 \mathrm{~A}-(67,68,69) \\ \quad+(6 \mathrm{~B}, 6 \mathrm{C}, 6 \mathrm{D}) \end{gathered}$ | $\begin{aligned} & \text { a. If not, adjust A7R3 } \\ & \text { (fig. 5-11. } \end{aligned}$ |
|  |  |  | b. If adjustment fails, replace A7 (para 5-10). Aline front end (para 5-8). |
| 45. | On operator terminal, |  |  |
|  | a. Hold down <CTRL> key and press C. | a. Scrolling stops |  |
|  | b. Enter <RETURN> | b. IU TEST EXECUTION menu displayed (fig. 5-6 |  |
| 46. | Steps 18 through 45 interact. Repeat front end alinement (para 5-8) until NO ERROR messages appear. | NO ERROR messages | a. If fault persists, go to paragraph 5-6 step 46. |
|  |  |  | b. If correct, repeat test procedure (para 5-6). |
|  |  |  |  |

## Section III. MAINTENANCE

5-9. COVERS
NOTE
Procedure is the same for top and bottom cover.
a. Preliminary Procedures.
(1) Remove power from test setup.
(2) Remove IU from test setup.

b. Removal.
(1) If removing bottom cover, set IU upside down.

NOTE
If helicoil is stripped, replace helicoil insert(para 5-22).
(2) Remove 25 screws (1) and washers (2).
(3) Remove cover (3).
(4) Inspect gasket (4) for cracks or breaks. If damage, replace gasket[(para 5-23).

## 5-9. COVERS - Continued

c. Installation.
(1) Place cover (3) and gasket (4) in installed position.

NOTE
If helicoil is stripped, replace helicoil insert (para 5-22).
(2) Install 26 screws (1) and washers (2). Torque to 6-8 inch/pounds.

d. Follow-on Procedure. Perform test procedure (para 5-6).

## 5-10. CIRCUIT CARD ASSEMBLIES

NOTE
Procedure is the same for all circuit cards, except where noted.
a. Preliminary Procedure. Remove top cover(para 5-9).
b. Removal.
(1) If removing circuit card Al, disconnect W14P2 (2).
(2) Loosen cam locks (1).
(3) Using circuit card extractor, remove circuit card (3) from IU (4).


## 5-10. CIRCUIT CARD ASSEMBLIES - Continued

C. Installation.

## CAUTION

Carefully seat circuit card in card slot or circuit card connectors may be damaged.
(1) Insert circuit card (3) into IU (4).
(2) Tighten cam locks (1).
(3) If installing circuit card A1, connect W14P2 (2).

d. Follow-on Procedures.
(1) If A3 replaced, aline A3 (para 5-7).
(2) For all other circuit cards, perform test procedure (para 5-6).

## 5-11. NAV FILTER FL1

a. Preliminary Procedure. Remove top cover (para 5-9).
b. Removal.
(1) Loosen two jackscrews (5) on connector W1P2 (4).
(2) Disconnect connector W1P2 (4).
(3) Remove four screws (1) and washers (2).
(4) Remove FL1 (3).

C. Installation.
(1) Place FL1 (3) in installed position.
(2) Install four screws (1) and washers (2).
(3) Connect connector W1P2 (4) to FL1 (3).
(4) Tighten two jackscrews (5).
d. Follow-on Procedure. Perform test procedure (para 5-6.

## 5-12. OSCILLATOR G1

a. Preliminary Procedure. Remove top cover(para 5-9).
b. Removal.
(1) Set IU left side down on work bench.
(2) While supporting oscillator, remove four screws (1).
(3) Lower and rotate oscillator to access connectors P1 (3) and W14P1 (5).
(4) Loosen two jackscrews (4) on connector P1 (3).
(5) Disconnect connector PI (3) and W14P1 (5).
(6) Remove oscillator (2).

c. Installation.
(1) Connect connector P1 (3) and W14P1 (5) to oscillator (2).
(2) Tighten two jackscrews (4) on connector P1 (3).
(3) Position oscillator (2) in IU.
(4) Install four screws (1).
d. Follow-on Procedure. Perform test procedure (para 5-6).

## 5-13. CONNECTORS J2, J3, J4, J6, J7, J8, J11, J12, J13, OR J14

NOTES

- Procedure is the same for connectors $\mathrm{J} 2, \mathrm{~J} 3, \mathrm{~J} 4, \mathrm{~J} 6, \mathrm{~J} 7 \mathrm{~J} 8, \mathrm{~J} 11, \mathrm{~J} 12, \mathrm{~J} 13$, or J14.
- Connectors J17, J1i3, J19, and J20 are not replaceable by direct support maintenance.
a. Preliminary Procedure. Remove oscillator G1 (para 5-12).
b. Removal.
(1) Remove four screws (7) and washers (6), nutplate (2), ground lug (4), and connector (3) from front panel (5).
(2) Tag and remove wires (1).

c. Installation.
(1) Install wires (1) in connector (3) as tagged. Remove tags.
(2) Position connector (3) in rear of front panel (5).
(3) Position and hold ground lug (4) and nutplate (2) on rear of connector (3).
(4) Install four screws (7) and washers (6).
d. Follow-on Procedure. Install oscillator G1 (para 5-12).


## 5-14. CONNECTOR J5

a. Preliminary Procedure. Remove NAV FILTER FLI (para 5-11).
b. Removal.
(1) Remove two screws (9), washers (8), lockwashers (3), and nuts (4).
(2) Remove connector (1) and ground lug (6) from rear of front panel (7).
(3) Remove insulation sleeving (2) from wires (5).

WARNING
Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(4) Tag, unsolder, and remove wires (5).


## 5-14. CONNECTOR J5 -Continued

C. Installation.
(1) Position new length of insulation sleeving (2) on wires (5).

WARNING
Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(2) Resolder wires (5) as tagged. Remove tags.
(3) Position and shrink insulation sleeving (2).
(4) Position ground lug (6) and connector (1) on rear of front panel (7).
(5) Install two screws (9), washers (8), lockwashers (3) and nuts (4).

d. Follow-on Procedure. Install NAV filter FL1 para 5-11.

## 5-15. CONNECTORS J9, J10, J15, OR J16

NOTE
Procedure is the sane for $\mathrm{J} 9, \mathrm{~J} 10, \mathrm{~J} 15$, or J 316 .
a. Preliminary Procedure. Remove top cover(para 5-9).
b. Removal.
(1) Remove insulation sleeving (2) from wires (1).

WARNING
Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(2) Tag, unsolder, and remove wires (1).
(3) Remove nut (3) and washer (4).
(4) Remove connector (5). I


## 5-15. CONNECTORS J9, J1O, J15, OR J16 -Continued

c. Installation.
(1) Place connector (5) in installed position.
(2) Install nut (3) and washer (4).
(3) Place new lengths of insulation sleeving (2) on wires (1). v

WARNING
Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(4) Resolder wires (1) as tagged. Remove tags.
(5) Position and shrink-insulation sleeving (2).

d. Follow-on Procedure. Perform test procedure (para 5-6).

## 5-16. P1 CONNECTORS AT MOTHERBOARD A28

NOTE
Procedure is the same for all P1 connectors terminated at motherboard A28.
a. Preliminary Procedure. Remove top cover(para 5-9).
b. Removal.
(1) Loosen two captive screws (2).
(2) Disconnect connector (4).
(3) Remove insulation sleeving (3).

## WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(4) Tag, unsolder, and remove wires (1).
(5) Remove connector (4).


## 5-16. P1 CONNECTORS AT MOTHERBOARD 28 - Continued

c. Installation.
(1) Position new length of insulation sleeving (3) on wires (1).

## WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(2) Resolder wires (1) on connector (4) as tagged. Remove tags.
(3) Connect connector (4).
(4) Tighten two captive screws (2).

d. Follow-on Procedure. Install top cover(para 5-6).

## 5-17. WIRE HARNESS W1

NOTE
Procedure is same for all wires in wire harness W1.
a. Preliminary Procedure. Remove top cover(para 5-9).

b. Removal (Wire Harness).
(1) Loosen two captive screws (4) on connector W1P2 (6) at NAV filter FL1J2 (5).
(2) Disconnect connector W1P2 (6).
(3) Loosen two captive screws (1) on connector WIP1 (2) at motherboard A28J5 (3).
(4) Disconnect connector WIP1 (2).
(5) Remove W1 (7).

## 5-17. WIRE HARNESS W1 - Continued

c. Replacement (Wire).
(1) Remove insulation sleeving (4) from both ends of damaged wire (3).
(2) Remove cable ties (2), as required.

## WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(3) Tag, unsolder, and remove wire (3) from connectors WIP1 (1) and W1P2 (5).
(4) Dress ends of new length of wire (3).
(5) Position new lengths of insulation sleeving (4) on both ends of wire (3).
(6) Route wire (3) between connector WIP1 (1) and WIP2 (5).
(7) Resolder wire (3) to IJ1P1 (1) and W1P2 (5) as tagged. Remove tag.
(8) Repeat steps 1 through 8 for remaining damaged wires (3).
(9) Replace cable ties (2), as required.


## 5-17. WIRE HARNESS W1-Continued

d. Installation.
(1) Place W1 (7) in installed position.
(2) Connect WIP1 (2) to motherboard A28J5 (3).
(3) Tighten two captive screws (1).
(4) Connect W1P2 (6) to NAV filter (5).
(5) Tighten two captive screws (4).

e. Follow-on Procedure. Perform test procedure (para 5-6).

## NOTES

- Refer to appendix C to find how wire harness is terminated at the front panel and motherboard (A28).
- W3 from J19 to A28 is not replaceable at direct support maintenance.
- Procedure is the same for all wire harness removal, replacement of damaged wire(s), and wire harness reinstallation except where noted.
a. Preliminary Procedures.
(1) Remove top cover (para 5-9.
(2) If required for access, remove oscillator G1 (para 5-12).
b. Removal (Wire Harness).
(1) If replacing W3 jumper wire connecting J 3 to J 19 , go to paragraph c .
(2) If removing connector J5, go to step (5).
(3) Remove four screws (6) and washers (5), nutplate (1), ground lug (3), and J connector (2) from front panel (4).
(4) Go to step (7).



## 5-18. WIRE HARNESS W2 THROUGH W13, AND W15 - Continued

(5) Remove two screws (7), washers (6), lockwashers-s (2), and nuts (3).
(6) Remove connector J5 (1) and ground lug (4) from rear of front panel (5).

(7) See below. Loosen captive screws (3) and disconnect P connector(s) (4) from A28 (5).
(8) Remove cable ties (2), as required, to isolate wire harness (1).
(9) Remove wire harness (1).


## 5-18. WIRE HARNESS W2 THROUGH W13, AND W15 - Continued

c. Replacement (Wire).
(1) Cut and remove cable ties (2), as required.
(2) rag an( remove crimped ends of damaged wire (3) from J connector(s) (1).
(3) If working on W3 jumper connecting J3 to J19, go to step 6.
(4) Remove insulation sleeving (4), as required.

## WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(5) Tag, unsolder, and remove damaged wire (3) from P connector(s) (5).


## 5-18. WIRE HARNESS W2 THROUGH W13, AND W15 - Continued

(6) Dress both ends of replacement wire (3).
(7) Position replacement wire (3) in installed position.
(8) Install crimp contact(s) (6) wire (3).
(9) Install crimped ends of wire (3) in J connector(s) (1) as tagged.
(10) If working on W3 jumper connecting J3 to J19, go to step 12.
(11) Position new length of insulation sleeving (4) on wire (3).

## WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(12) Resolder wire (3) to $P$ connector(s) (5) as tagged. Remove tags.
(13) Position and shrink insulation sleeving (4).
(14) Check wire harness continuity.
(15) Install cable ties (2), as required.


## 5-18. WIRE HARNESS W2 THROUGH W13, AND W15 - Continued

d. Installation.
(1) If working on W 3 jumper connecting J 3 to J 19 , go to Follow-on Procedure, paragraph e.
(2) Connect P connector (2) to A28 (3).
(3) Tighten two captive screws (1).

(4) If installing connector J 5 , go to step 8 .
(5) See below. Position $J$ connector (2), ground lug (3), and nutplate (1) on rear of front panel (4).
(6) Install four screws (6) and washers (5).
(7) Go to step 10 .


## 5-18. WIRE HARNESS W2 THROUGH W13, AND W15 - Continued

(8) Position connector J5 (3) and ground lug (4) on rear of front panel (5).
(9) Install two screws (6), washers (7), lockwashers (1), and nuts (2).
(10) Install cable ties (3), as required.

d. Follow-on Procedures.
(1) If removed, install oscillator G1 (para 5-12).
(2) Perform test procedure (para 5-6.

## 5-19. WIRE HARNESS W14

a. Preliminary Procedure. Remove oscillator G1 (para 5-12).
b. Removal
(1) Disconnect W14P2 (2) from CCA AI (1).
(2) 2Remiove W14 (3).

c. Installation.
(1) Place W14 (3) in installed position.
(2) Connect W14P2 (2) to CCA AI (1).
d. Follow-on Procedure. Install oscillator G1 (para 5-12).

## 5-20. OSCILLATOR G1 TO MOTHERBOARD A28J6 WIRE HARNESS

## NOTE

Procedure is the same for either wire in wire harness.
a. Preliminary Procedures.
(1) Remove oscillator G1 (para 5-12).
(2) Remove bottom cover (para 5-9).
b. Removal.
(1) Set IU on left side down on workbench.
(2) Remove insulation sleeving (1) from J6 end of wire (3) as required.

## WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(3) Tag, unsolder, and remove bus bar (2) from connector J6 (4).
(4) Tag, unsolder, and remove two wires (3) from bus bar (2).
(5) Remove screw (7) and cable clamp (6).
(6) Remove cable ties (5) as required.
(7) Pull wire (3) through grommet (8).

(8) Remove insulation sleeving (2).

## WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(9) Unsolder and remove wire (3) from connector P1 (1).

c. Installation.
(1) Dress new length of wire (3).
(2) Install new lengths of insulation sleeving (2) on each end of wire (3).
(3) Solder wire (3) to connector P1 (1) as tagged.
(4) Position and shrink insulation sleeving (2).

## 5-20. OSCILLATOR G1 TO MOTHERBOARD A28J6 WIRE HARNESS - Continued

(5) Route wire (3) through grommet (8) to connector J6 (4).

## WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(6) Solder wires (3) to bus bar (2).
(7) Solder bus bar (2) to connector J6 (4) as tagged. Remove tag.
(8) Position insulation sleeving (1).
(9) Install cable ties (5) as required.
(10) Place cable clamp (6) in installed position.
(11) Install screw (7).

d. Follow-on Procedures.
(1) Install bottom cover (para 5-9.
(2) Install oscillator G1 (para 5-12).

## NOTES

- Procedure is same for twisted pair wiring to connector J9 or J15. Connector J10 is jumpered to J 9 . Connector J15 is jumpered to J16. Twisted pair wiring is removed as a unit.
- Refer to appendix for wire list.
a. Preliminary Procedure. Remove top cover (para 5-9).
b. Removal.


## NOTE

If jumper wires between connectors are damaged, repeat steps 1 and 2 . to remove wire, then go to installation.
(1) Remove insulation sleeving (2) from twisted pair (3).

WARNING
Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(2) Tag, unsolder, and remove twisted pair (3) from J connector (1).
(3) Set IU upside down on workbench.


## 5-21. WIRING TO CONNECTORS J9, J10, J15, OR J16. - Continued ]

(4) Remove insulation sleeving (2) from twisted pair (1).
(5) Using extraction tool, remove twisted pair (1) from pins (3) on A28 (4).

## NOTE

J9 twisted pair has one cable clamp instead of three.
(6) Remove three screws (6) and cable clamps (7).
(7) Remove cable ties (5), as required.
(8) Remove twisted pair (1).


## 5-21. WIRING TO CONNECTORS J9, J10, J15, OR J16 - Continued

c. Installation.

## NOTE

If only jumper wires between connectors were removed, go to step 12.
(1) Dress ends of twisted pair (2) to be attached to A28.
(2) Install new lengths of insulation sleeving (1).
(3) Position a twisted pair end (2) in pin connector (3).
(4) Using crimping tool, crimp pin connector (3).
(5) Repeat steps (3) and (4) for remaining twisted pair end (2).


## 5-21. WIRING TO CONNECTORS J9, J10, J15, OR J16-Continued

(6) Place twisted pair (1) in, installed position.
(7) Using insertion tool, instill twisted pair (1) on A23S (4) pins (3) as tagged. Remove tags.
(8) Slide insulation sleeving (2) down to cover pins (3).

(9) Install cable ties (5) as required.

NOTE
J9 twisted pair has one cable clamp instead of three.
(10) Place three cable clamps (7) in installed position.
(11) Install three screws (6).

## 5-21. WIRING TO CONNECTORS J9, J10, J15, OR J16 - Continued

(12) Set IU in normal upright position.
(13) Dress wire ends (3).
(14) Position new length of insulation sleeving (2) on wire ends (3).

## WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(15) Solder wires (3) to J connector(s) (1) as tagged. Remove tags.
(16) Position and shrink insulation sleeving (2).

d. Follow-on Procedure. Perform test procedure (para 5-6).

## 5-22. HELICOIL INSERTS

## a. Removal.

(1) Using removal tool, press and turn insert (1) counterclockwise.
(2) Remove insert (1). If insert cannot be removed, go to step 3.
(3) Using scribe, pry top thread of insert (1) away from housing hole (2).
(4) Using needle-nose pliers, turn insert (1) counterclockwise.
(5) Remove insert (1).


5-22. HELICOIL INSERTS - Continued
b. Installation.

## WARNING

Isopropyl alcohol is flammable and moderately toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate.
(1) Using pipe cleaner or swab, and isopropyl alcohol, clean housing hole (2).
(2) Place new insert (1) on insertion tool.

## WARNING

Zinc chromate dust primer is highly toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate.
(3) Coat insert (1) with zinc chromate dust primer.


## NOTE

## Top thread of insert should be below housing surface between $1 / 4$ and 1-1/2 turns.

(4) Using insertion tool, install insert (1) in housing hole (2) as follows:
(a) Aline insert threads with hole threads.
(b) Press insertion tool outer housing against hole housing (3).
(c) Turn insertion tool clockwise to thread insert into hole within limits given.
(5) Ensure insert (1) is between $1 / 4$ and $1-1 / 2$ turns below housing surface.
(a) If insert is installed within limits given, go to step (6).
(b) If insert is not installed within limits given, replace insert.
(6) Using tang removal tool, press and remove insert tang (4) from bottom of insert (1).
(7) Allow zinc chromate dust primer one hour to cure.

c. Follow-on Procedure. Install cover (para 5-9).

## 5-23. GASKET

NOTE
Procedure is the same for top or bottom cover gaskets.
a. Preliminary Procedure. Remove cover (para 5-9).
b. Removal.
(1) Scrape gasket (1) from cover (2).

## WARNING

Isopropyl alcohol is flammable and moderately toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate.
(2) Using isopropyl alcohol, clean cover (2) to remove gasket (1) and adhesive residue.


## 5-23. GASKET - Continued

c. Installation.

## WARNING

Adhesive, MIL-A-46016, type II, is flammable and slightly toxic to eyes,. skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate.
(1) Apply light, even coat of adhesive to mating surface of gasket (1) and cover (2).
(2) Install gasket (1) on cover (2).
(3) Allow adhesive to cure at room temperature for 2 hours.

d. Follow-on Procedure. Install cover (para 5-9).

## 5-24. FAN ASSEMBLY

a. Preliminary Procedures.
(1) Remove power from test setup.
(2) Remove IU from test setup.
b. Removal.
(1) While supporting fan assembly, remove eight screws (6) and washers (5).
(2) Separate fan assembly (4) from rear panel (1).
(3) Loosen two captive screws (3).
(4) Disconnect connector (2).


## 5-24. FAN ASSEMBLY - Continued

c. Installation.
(1) Connect connector (2).
(2) Tighten two captive screws (3).
(3) Position and hold fan assembly (4) on rear panel (1).
(4) Install eight screws (6) and washers (5). Torque to 6-8 inch pounds.

d. Follow-on Procedure. Perform test procedure (para 5-6).

## Section IV. PREPARATION FOR STORAGE OR SHIPMENT

## 5-25. STORAGE FACILITIES

a. Security of the stored equipment is required. The area used for storage must protect the equipment from being stolen.
b. The equipment in storage must be protected from the weather. Covered storage is required.

## 5-26. PROCEDURES

a. The equipment to be stored must be in good working order. Perform an Operational check on the equipment prior to storage (para 5-5).
b. When putting the equipment into administrative storage (1-45 days) use a storage area that is accessible. Equipment in administrative storage must be able to be removed from storage and put into operation on 24 hour notice.

## APPENDIX A <br> REFERENCES

## A-1. SCOPE

This appendix lists all forms, field manuals, technical manuals, and miscellaneous publications referenced in this manual. Only those publications available to, and required by the user are listed.

## A-2. FORMS

Recommended Changes to Publications and Blank Forms DA Form 2028DA Form 2028-2
Report of Discrepancy (ROD) ..... SF 364
Discrepancy in Shipment Report ..... SF 361
Quality Deficiency Report ..... SF 368
A-3. FIELD MANUALS
First Aid and Safety ..... FM-21-11
A-4. TECHNICAL MANUALS
Operator's, Organizational, and Direct Support
Maintenance Manual for
Airborne Relay Facility AN/ARW-83 (V)6 ..... TM 11-5821-332-13
Organizational, Operation, and MaintenanceInstructions with Illustrated Parts Breakdownfor Computer, Digital CP-I 849/UTM 11-5895-127613
Organizational and Direct Support
Repair Parts and Special Tools
List for Interface Unit J-4522/U. ..... TM 11-5895-1279-23P
Operator's, Organizational, and Direct SupportMaintenance Manual forPower Supply-Receiver PP-8184/UTM 11-5895-1280-13
Operator's, Organizational, and Direct Support
Maintenance Manual for
Control Panel C-11804/ALQ. ..... TM 11-5895-1281-13
Operator's, Organizational, and Direct Support Maintenance Manual for
Receiver Digital Control C-I 1634/U. ..... TM 11-5895-1283-13
Operator's, Organizational, and Direct Support Maintenance Manual for
Power Supply PP-8185/U ..... TM 11-5895-1285-13
Operator's, Organizational, and Direct Support
Maintenance Manual for
Test Set, Interface Unit TS-4221/U ..... TM 11-6625-3150-13
A-5 MISCELLANEOUS PUBLICATIONS
The Army Maintenance Management System ..... DA Pam 738-750
Consolidated Index of Army Publication and Blank Forms ..... DA Pam 25-30
Procedures for Destruction of Electronics
Maateriel to Prevent Enemy Use(Electronics Command)TM 750-244-2

## APPENDIX B <br> MAINTENANCE ALLOCATION CHART FOR <br> INTERFACE UNIT J-4522/U

## B-1. GENERAL

This appendix provides a summary of the maintenance operations for Interface Unit J-4522/U. It authorizes levels of maintenance for specific maintenance functions of repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

## B-2. MAINTENANCE FUNCTION

Maintenance functions will be limited to and defined as follows:
a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.
b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.
c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean(decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.
d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.
e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.
f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.
g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.
h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.
i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.
j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/ operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.
k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

## CHANGE 1 B-1

## B-3. COLUMN ENTRIES

a. Column 1, Group Number. Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.
b. Column 2, Component/Assembly. Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.
c. Column 3, Maintenance functions. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.
d. Column 4, Maintenance Level. Column 4 specifies, by the listing of a 'work time" figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated level of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance levels, appropriate "work time" figures will be shown for each level. The number of task-hours specified by the 'work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

## C - Operator/Crew, O - Unit Maintenance/Aviation Unit Maintenance, F - Direct Support/Aviation Intermediate Maintenance, H - General Support Maintenance, D - Depot Support Maintenance

e. Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.
f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in section IV, Remarks, which is pertinent to the item opposite the particular code.

## B-4. TOOL AND TEST EQUIPMENT REQUIREMENT\$ (Section III)

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.
b. Maintenance Level. The codes in this column indicate the maintenance level allocated the tool or test equipment.
c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.
d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.
e. Tool Number. This column lists the manufacturers part number of the tool followed by the Federal Supply Code for manufacturers ( 5 -digit) in parentheses.

## B-5. REMARKS

a. Reference Code. This code refers to the appropriate item in section II, column 6.
b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in section II

CHANGE 1 B-2

Section II. MAINTENANCE ALLOCATION CHART FOR
INTERFACE UNIT J-4522/U

| (1) <br> GROUP NUMBER | (2) <br> COMPONENT ASSEMBLY | (3) <br> MAINTENANCE | (4) <br> MAINTENANCE CATEGORY |  |  |  |  | (5) <br> TOOLS AND EQUIPMENT | (6) <br> REMARKS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | FUNCTION | C | 0 | F | H | D |  |  |
| 00 | INTERFACE UNIT | INSPECT <br> TEST <br> TEST <br> ALINE <br> REPAIR |  | 0.5 | $\begin{aligned} & 0.3 \\ & 1.4 \\ & 0.5 \\ & 1.5 \end{aligned}$ |  | 1.0 | $\begin{gathered} 10 \\ 1,4,10 \\ 1,2,3,4,5,6 \\ 7,8,9,10,12 \\ 5 \\ 10 \end{gathered}$ | $\begin{aligned} & \text { A, B } \\ & \text { C, D } \end{aligned}$ |
| 01 | CCA IU BUS | INSPECT <br> TEST REPAIR REPLACE |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 13 \\ & 10 \end{aligned}$ |  |
| 02 | CCA IU BUS 2 | INSPECT <br> TEST <br> REPAIR <br> REPLACE |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 13 \\ & 10 \end{aligned}$ |  |
| 03 | CCA TO1A | INSPECT <br> TEST REPAIR REPLACE |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 13 \\ & 10 \end{aligned}$ |  |
| 04 | CCA TO1B | INSPECT <br> TEST REPAIR REPLACE |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 13 \\ & 10 \end{aligned}$ |  |
| 05 | CCA 1553 IF | INSPECT <br> TEST REPAIR REPLACE |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 13 \\ & 10 \end{aligned}$ |  |
| 06 | CCA SRAM | INSPECT <br> TEST <br> REPAIR <br> REPLACE |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 13 \\ & 10 \end{aligned}$ |  |

Section II. MAINTENANCE ALLOCATION CHART
FOR
INTERFACE UNIT J-4522/U

| (1) <br> GROUP NUMBER | (2) <br> COMPONENT ASSEMBLY | (3) <br> MAINTENANCE FUNCTION | (4) <br> MAINTENANCE CATEGORY |  |  |  |  | (5) <br> TOOLS AND EQUIPMENT | (6) REMARKS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | C | 0 | F | H | D |  |  |
| 07 | CCA IU NAV | $\begin{aligned} & \text { INSPECT } \\ & \text { TEST } \\ & \text { REPLACE } \\ & \text { REPAIR } \end{aligned}$ |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 13 \\ & 11 \end{aligned}$ |  |
| 08 | CCA IUDL INSPECT | TEST <br> REPLACE <br> REPAIR |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{gathered} 04 \\ 0.5 \end{gathered}$ | $\begin{aligned} & 13 \\ & 11 \end{aligned}$ |  |
| 09 | CCA MTDIU | $\begin{aligned} & \text { INSPECT } \\ & \text { TEST } \\ & \text { REPLACE } \\ & \text { REPAIR } \end{aligned}$ |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 13 \\ & 11 \end{aligned}$ |  |
| 10 | CCA DBF | $\begin{aligned} & \text { INSPECT } \\ & \text { TEST } \\ & \text { REPLACE } \\ & \text { REPAIR } \end{aligned}$ |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 13 \\ & 11 \end{aligned}$ |  |
| 11 | CCA CP INTERFACE | INSPECT <br> TEST <br> REPLACE <br> REPAIR |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 13 \\ & 11 \end{aligned}$ |  |
| 12 | CCA DOAA | INSPECT <br> TEST <br> REPLACE <br> REPAIR |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 13 \\ & 11 \end{aligned}$ |  |
| 13 | CCA BATTERY REG | INSPECT <br> TEST <br> REPLACE <br> REPAIR |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 13 \\ & 11 \end{aligned}$ |  |
| 14 | CCA IFPCTRL | INSPECT <br> TEST <br> REPLACE <br> REPAIR |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 13 \\ & 11 \end{aligned}$ |  |
| 15 | CCA IFPCTRL B | INSPECT <br> TEST <br> REPLACE <br> REPAIR |  |  | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 13 \\ & 11 \end{aligned}$ |  |

B-4 CHANGE 1

## Section III. TOOL AND TEST EQUIPMENT REQUIREMENTS <br> FOR <br> INTERFACE UNIT J-4522/U

| TOOL OR TES $\dagger$ EQUIPMENT REF CODE | MAINTENANCE CATEGORY | NOMENCLATURE | NATIONAL/NATO STOCK NUMBER | $\overline{\mathrm{TOOL}}$ <br> NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| 01 | F | TAPE, LRU DIAGNOSTICS |  | 5034-2934 |
| 02 | F | DIGITAL DELAY WIDTH GENERATOR |  | 7085 |
| 03 | F | INTERFACE UNIT TEST SET |  | C5116272 |
| 04 | O,F | MISSION TEST EQUIPMENT |  | C5117754 |
| 05 | O,F | MULTIMETER | 6625-01-139-2512 |  |
| 06 | F | OSCILLOSCOPE | 6625-01-119-7314 |  |
| 07 | F | RECEIVER, DIGITAL CONTROL |  | C5116262 |
| 08 | F | RECEIVER, POWER SUPPLY |  | C5116264 |
| 09 | F | SYSTEM POWER SUPPLY |  | C5116268 |
| 10 | O,F | TOOL KIT, ELECT. EQUIP. TK-105/G | 5180-610-8177 |  |
| 11 | F | TERMINATION, 75 OHM |  | TNG1-1-75 |
| 12 | F | HELICOIL KIT | 5895-00-873-6874 |  |
| 13 | D | TEST SYSTEM |  | HP-7050 |

CHANGE 1 B-5

## Section IV. REMARKS

| REFERENCE <br> CODE | REMARKS |
| :---: | :--- |
| A | ORGANIZATIONAL MAINTENANCE LEVEL ACCOMPLISHES SYSTEM TESTS USING <br> BIT, MISSION TEST EQUIPMENT, AND CONTINUITY TESTS OF CABLES |
| B | DIRECT SUPPORT MAINTENANCE LEVEL ACCOMPLISHES THOSE TESTS REQUIRED <br> TO LOCATE FAULTY MODULES, COMPONENTS, WIRING AND CABLE PROBLEMS. <br> C <br> DIRECT SUPPORT MAINTENANCE LEVEL PROVIDES ORGANIZATIONAL <br>  <br> MAINTENANCE ASSISTANCE AS REQUIRED, AND REPAIR OF CHASSISIFRAME BY <br> REPLACEMENT OF METERS, SWITCHES, CONNECTORS, AND OTHER CHASSIS AND <br> FRONT PANEL MOUNTED PIECE PARTS AND SELECTED MODULES/CIRCUIT CARDS <br> AND CABLE ASSEMBLY REPAIR/REPLACEMENT. |
| DIRECT SUPPORT MAINTENANCE LEVEL REPAIR MINOR DAMAGE TO LRU CHASSIS <br> AND COVERS BY STRAIGHTENING, SANDING, AND SPOT PAINTING. |  |

* U.S.GOVERNMENT PRINTING OFFICE: 1997-509-116/60076

PIN: 069797-001
CHANGE 1 B-6

## SECTION II MAINTENANCE ALLOCATION CHART <br> FOR <br> INTERFACE UNIT <br> J-4522/0



## B-7

## SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS FOR <br> INTEFACE UNIT

| TOOL OR TEST EQUIPMENT REF CODE | MAINTENANCE CATEGORY | NOMENCLATURE | NATIONAL/NATO STOCK NUMBER | TOOL <br> NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| 01 | 0 | TAPE, LRD DIAGNOSTICS |  | 5034-2934 |
| 02 | F | DIGITAL DELAYIWIDTH GENERATOR |  | 7085 |
| 03 | F | INTERFACE UNIT TEST SET |  | C5116272 |
| 04 | 0 | MISSION TEST EQUIPMENT |  | C5117754 |
| 05 | O,F | MULTIMETER | 6625-01-139-2512 |  |
| 06 | F | OSCILLOSCOPE | 6625-01-119-7314 |  |
| 07 | F | RECEIVER DIGITAL CONTROL |  | C5116262 |
| 08 | F | RECEIVER POWER SUPPLY |  | C5116264 |
| 09 | F | SYSTEM POWER SUPPLY |  | C5116268 |
| 10 | O, F | TOOL KIT, ELECT. EQUIP. TK-105/G | 5180-00-610-8177 |  |
| 11 | O, F | TORQUE LIMITING SET |  | MMCARR 57 |
| 12 | F | TERMINATION 75 OHM |  | TNG1-1-75 |
| 13 | F | BELICOIL KIT | 5895-00-873-6874 |  |
| 14 | F | MAINTENANCE SUBSYSTEM |  | C5117753 |
| 15 | F | STOPWATCH |  | FELDMAR 6 |

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## PAGE B-11

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## Section IV. REMARKS

| REFERENCE <br> CODE | REMARKS |
| :---: | :--- |
| A | Organizational maintenance level accomplishes system tests using bit, mission test <br> equipment, and continuity tests of cables. <br> Direct support maintenance level accomplishes those tests required to locate faulty modules, <br> components, wiring and cable problems. |
| C | Direct support maintenance level provides organizational maintenance assistance as <br> required and repair of chassis/frame by replacement of meters, switches, connectors, and <br> other chassis and front panel mounted piece parts and selected modules/circuit cards and <br> cable assembly repair/replacement. |
| DDirect support maintenance level repairs minor damage to LRU chassis and covers by <br> straightening, sanding, and spot painting. |  |
| EDirect support will check the dual bus processor CCA to determine that the following <br> applicable microcircuits are installed: For the Marine Corps microcircuit USG shall carry the <br> part number 845035C0925 and USH shall carry the part number 845035C0926. For the <br> Army microcircuit USG shall carry the number C51 18219 and USH shall carry the number <br> C5118220. The depot shall change the microcircuits. |  |

## APPENDIX C WIRE LIST



[^1]W1

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 24 | ORG | P1-1 (A28J5) | P2-1 | +12 VA |
| 24 | ORG | P1-6 (A28J5) | P2-6 | +12 VB |
| 26 | WHT TW | P1-4 (A28J5) | P2-4 | NAVCLK |
| 26 | BLK PR | P1-8 (A28J5) | P2-8 | NAVCLK RTN |
| 26 | WHT TW | P1-5 (A28J5) | P2-5 | NAVD |
| 26 | BLK PR | P1-9 (A28J5) | P2-9 | NAVD RTN |
| 26 | WHT TW | P1-3 (A28J5) | P2-3 | NAVSNC |
| 26 | BLK PR | P1-7 (A28J5) | P2-7 | NAVSNC RTN |
|  | W2 |  |  |  |
| 24 | GRN | J2-55 | E1 | CHASSIS GND |
| 26 | BLK TW | J2-15 | P1-15 (A28J10) | DATF \$ |
| 26 | WHT PR | J2-14 | P1-14 (A28J10) | DATF * |
| 26 | BLK TW | J2-7 | P1-7 (A28J10) | DTIN \$ |
| 26 | WHT PR | J2-2 | P1-2 (A28J10) | DTIN * |
| 26 | BLK TW | J2-8 | P1-8 (A28J10) | DTOT \$ |
| 26 | WHT PR | J2-3 | P1-3 (A28J10) | DTOT * |
| 26 | BLK TW | J2-54 | P1-54 (A28J10) | FMTSELO \$ |
| 26 | WHT PR | J2-53 | P1-53 (A28J10) | FMTSELO * |
| 26 | BLK TW | J2-40 | P1-40 (A28J10) | FMTSEL1 \$ |
| 26 | WHT PR | J2-39 | P1-39 (A28J10) | FMTSEL1 * |
| 26 | BLK TW | J2-13 | P1-13 (A28J10) | SPARE1 \$ |
| 26 | WHT PR | J2-12 | P1-12 (A28J10) | SPARE1 * |
| 26 | BLK TW | J2-41 | P1-41 (A28J10) | SPARE2 \$ |
| 26 | WHT PR | J2-30 | P1-30 (A28J10) | SPARE2 * |
| 26 | BLK TW | J2-43 | P1-43 (A28J10) | SPARE3 \$ |
| 26 | WHT PR | J2-42 | P1-42 (A28J10) | SPARE3* |

W2 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 26 | BLK TW | J2-45 | P1-45 (A28J10) | SPARE4 \$ |
| 26 | WHT PR | J2-44 | P1-44 (A28J10) | SPARE4* |
| 26 | BLK TW | J2-11 | P1-11 (A28J10) | STAD \$ |
| 26 | WHT PR | J2-10 | P1-10 (A28J10) | STAD * |
| 26 | BLK TW | J2-16 | P1-16 (A28J10) | STAF \$ |
| 26 | WHT PR | J2-9 | P1-9 (A28J10) | STAF * |
| 26 | BLK TW | J2-4 | P1-4 (A28J10) | TCMDO \$ |
| 26 | WHT PR | J2-5 | P1-5 (A28J10) | TCMDO * |
| 26 | BLK TW | J2-24 | P1-24 (A28J10) | TDATOO \$ |
| 26 | WHT PR | J2-23 | P1-23 (A28J10) | TDATOO * |
| 26 | BLK TW | J2-32 | P1-32 (A28J10) | TDAT01 \$ |
| 26 | WHT PR | J2-25 | P1-25 (A28J10) | TDAT01 * |
| 26 | BLK TW | J2-27 | P1-27 (A28J10) | TDAT02 \$ |
| 26 | WHT PR | J2-26 | P1-26 (A28J10) | TDAT02 * |
| 26 | BLK TW | J2-29 | P1-29 (A28J10) | TDAT03 \$ |
| 26 | WHT PR | J2-28 | P1-28 (A28J10) | TDAT03* |
| 26 | BLK TW | J2-22 | P1-22 (A28J10) | TDAT04 \$ |
| 26 | WHT PR | J2-21 | P1-21 (A28J10) | TDAT04* |
| 26 | BLK TW | J2-34 | P1-34 (A28J10) | TDAT05 \$ |
| 26 | WHT PR | J2-33 | P1-33 (A28J10) | TDAT05 * |
| 26 | BLK TW | J2-36 | P1-36 (A28J10) | TDAT06 \$ |
| 26 | WHT PR | J2-35 | P1-35 (A28J10) | TDAT06 * |
| 26 | BLK TW | J2-38 | P1-38 (A28J10) | TDAT07 \$ |
| 26 | WHT PR | J2-37 | P1-37 (A28J10) | TDAT07 * |
| 26 | BLK TW | J2-1 | P1-1 (A28J10) | FRDY \$ |
| 26 | WHT PR | J2-6 | P1-6 (A28J10) | FRDY * |
| 26 | BLK TW | J2-18 | P1-18 (A28J10) | FRST \$ |
| 26 | WHT PR | J2-17 | P1-17 (A28J10) | FRST * |

C-3

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 22 | GRN | J3-55 | E2 | CHASSIS GND |
| 24 | BLK TW | J3-1 | P1-1 (A28J11) | DSPCLK \$ |
| 24 | WHT PR | J3-2 | P1-2 (A28J11) | DSPCLK* |
| 24 | BLK TW | J3-3 | P1-3 (A28J11) | DSPDOO \$ |
| 24 | WHT PR | J3-4 | P1-4 (A28J11) | DSPDOO * |
| 24 | BLK TW | J3-5 | P1-5 (A28J11) | DSPD01 \$ |
| 24 | WHT PR | J3-6 | P1-6 (A28J11) | DSPD01* |
| 24 | BLK TW | J3-7 | P1-7 (A28J11) | DSPD02 \$ |
| 24 | WHT PR | J3-8 | P1-8 (A28J11) | DSPD02 * |
| 24 | BLK TW | J3-9 | P1-9 (A28J11) | DSPD03 \$ |
| 24 | WHT PR | J3-10 | P1-10 (A28J11) | DSPD03* |
| 24 | BLK TW | J3-11 | P1-11 (A28J11) | DSPD04 \$ |
| 24 | WHT PR | J3-12 | P1-12 (A28J11) | DSPD04* |
| 24 | BLK TW | J3-13 | P1-13 (A28J11) | DSPD05 \$ |
| 24 | WHT PR | J3-14 | P1-14 (A28J11) | DSPD05* |
| 24 | BLK TW | J3-15 | P1-15 (A28J11) | DSPD06 \$ |
| 24 | WHT PR | J3-16 | P1-16 (A28J11) | DSPD06 * |
| 24 | BLK TW | J3-17 | P1-17 (A28J11) | DSPD07 \$ |
| 24 | WHT PR | J3-18 | P1-18 (A28J11) | DSPD07* |
| 24 | BLK TW | J3-19 | P1-19 (A28J11) | DSPD08 \$ |
| 24 | WHT PR | J3-20 | P1-20 (A28J11) | DSPD08* |
| 24 | BLK TW | J3-21 | P1-21 (A28J11) | DSPD09 \$ |
| 24 | WHT PR | J3-22 | P1-22 (A28J11) | DSPD09* |
| 24 | BLK TW | J3-23 | P1-23 (A28J11) | DSPHSNC \$ |
| 24 | WHT PR | J3-24 | P1-24 (A28J11) | DSPHSNC * |
| 24 | BLK TW | J3-25 | P1-25 (A28J11) | DSPVSNC \$ |
| 24 | WHT PR | J3-26 | P1-26 (A28J11) | DSPVSNC * |
| 24 | BLK TW | J3-32 | P1-32 (A28J11) | KBDAT \$ |
| 24 | WHT PR | J3-33 | P1-33 (A28J11) | KBDAT * |
| 24 | BLK TW | J3-28 | P1-28 (A28J11) | SPARE1 \$ |
| 24 | WHT PR | J3-27 | P1-27 (A28J11) | SPARE1* |
| 24 | BLK TW | J3-30 | P1-30 (A28J11) | SPARE2 \$ |
| 24 | WHT PR | J3-29 | P1-29 (A28J11) | SPARE2 * |

## W3 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :--- | :--- | :--- | :--- | :--- |
| 24 | BLK TW | J3-35 | P1-35 (A2311JI) | SPARE3 \$ <br> 24 |
| WHT PR | SPARE3 * |  |  |  |

## W3 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 22 | BLK | P2-4 (A28J6) | J19-U | +12 VDC RTN |
| 22 | VIO | P3-4 (A28J1) | J19-d | -5.2 VDC |
| 22 | VIO | P3-5 (A28J1) | J19-e | -5.2 VDC |
| 22 | VIO | P3-10 (A28J1) | J19-f | -5.2 VDC |
| 22 | BLK | P3-14 (A28J1) | J19-g | -5.2 VDC RTN |
| 22 | BLK | P3-13 (A28J1) | J19-h | -5.2 VDC RTN |
| 22 | BLK | P3-7 (A28J1) | J19-j | -5.2 VDC RTN |
| 22 | RED | P3-1 (A28J1) | J19-b | BATT + |
| 22 | BLK | P3-2 (A28J1) | J19-c | BATT - |
| 22 | GRN | J19-S (A28J1) | E12 | CHASSIS GND |
|  | W4 |  |  |  |
| 24 | GRN | J4-1 | E3 | CHASSIS GND |
| 26 | BLK TW | J4-5 | P1-5 (A28J16) | GPSD \$ |
| 26 | WHT PR | J4-4 | P1-4 (A28J16) | GPSD * |
| 26 | BLK TW | J4-7 | P1-7 (A28J16) | SPARE1 \$ |
| 26 | WHT PR | J4-6 | P1-6 (A28J16) | SPARE1* |
| 26 | BLK TW | J4-9 | P1-9 (A28J16) | SPARE2 \$ |
| 26 | WHT PR | J4-8 | P1-8 (A28J16) | SPARE2 * |
| 26 | BLK TW | J4-11 | P1-11 (A28J16) | SPARE3 \$ |
| 26 | WHT PR | J4-10 | P1-10 (A28J16) | SPARE3* |
| 26 | BLK TW | J4-13 | P1-13 (A28J16) | SPARE4 \$ |
| 26 | WHT PR | J4-12 | P1-12 (A28J16) | SPARE4* |
| 26 | BLK TW | J4-3 | P1-3 (A28J16) | TICK \$ |
| 26 | WHT PR | J4-2 | P1-2 (A28J16) | TICK * |


|  | W5 |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| AWG | COLOR | FROM | TO | REMARKS |
| 24 | GRN | J5-1 | E16 | CHASSIS GND |
| 24 | WHT | J5-2 | P1-2 (A2834) | TXD1 |
| 24 | WHT | J5-3 | P1-3 (A28J4) | RXD1 |
| 24 | BLK | J5-4 | P1-4 (A28J4) | GND1 |
| 24 | WHT | J5-5 | P1-5 (A28J4) | TXD2 |
| 24 | WHT | J5-6 | P1-6 (A28J4) | RXD2 |
| 24 | BLK | J5-7 | P1-7 (A28J4) | GND2 |
| 24 | WHT | J5-8 | P1-8 (A28J4) | TXD3 |
| 24 | WHT | J5-9 | P1-9 (A28J4) | RXD3 |
| 24 | BLK | J5-10 | P1-10 (A28J4) | GND3 |
| 24 | WHT | J5-11 | P1-II (A28J4) | TXD4 |
| 24 | WHT | J5-12 | P1-12 (A28J4) | RXD4 |
| 24 | BLK | J5-13 | P1-13 (A28J4) | GND4 |
| 24 | WHT | J5-14 | P1-14 (A28J4) | TXD5 |
| 24 | WHT | J5-15 | P1-15 (A28J4) | RXD5 |
| 24 | BLK | J5-16 | P1-16 (A28J4) | GND5 |
| 24 | WHT | J5-17 | P1-17 (A28J4) | TXD6 |
| 24 | WHT | J5-18 | P1-18 (A28J4) | RXD6 |
| 24 | BLK | J5-19 | P1-19 (A28J4) | GND6 |
| 24 | WHT | J5-20 | P1-20 (A28J4) | TXD7 |
| 24 | WHT | J5-21 | P1-21 (A28J4) | RXD7 |
| 24 | BLK | J5-22 | P1-22 (A28J4) | GND7 |
| 24 | WHT | J5-23 | P1-23 (A28J4) | TXD8 |

## C-7

|  | W5 (continued) |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| AWG | COLOR | FROM | TO | REMARKS |
| 24 | WHT | J5-24 | P1-24 (A28J4) | RXD8 |
| 24 | BLK | J5-25 | P1-25 (A28J4) | GND8 |
| 24 | WHT | J5-26 | P1-26 (A28J4) | DTR1 |
| 24 | WHT | J5-27 | P1-27 (A28J4) | CTS1 |
| 24 | GRN | J5-28 | E4 | CHASSIS GND2 |
| 24 | WHT | J5-29 | P1-29 (A28J4) | DTR2 |
| 24 | WHT | J5-30 | P1-30 (A28J4) | CTS2 |
| 24 | GRN | J5-31 | E4 | CHASSIS GND3 |
| 24 | WHT | J5-32 | P1-32 (A28J4) | DTR3 |
| 24 | WHT | J5-33 | P1-33 (A28J4) | CTS3 |
| 24 | GRN | J5-34 | E16 | CHASSIS GND4 |
| 24 | WHT | J5-35 | P1-35 (A28J4) | DTR4 |
| 24 | WHT | J5-36 | P1-36 (A28J4) | CTS4 |
| 24 | GRN | J5-37 | E16 | CHASSIS GND5 |
| 24 | WHT | J5-38 | P1-38 (A28J4) | DTR5 |
| 24 | WHT | J5-39 | P1-39 (A28J4) | CTS5 |
| 24 | GRN | J5-40 | E16 | CHASSIS GND6 |
| 24 | WHT | J5-41 | P1-41 (A28J4) | DTR6 |
| 24 | WHT | J5-42 | P1-42 (A28J4) | CTS6 |
| 24 | GRN | J5-43 | E4 | CHASSIS GND7 |
| 24 | WHT | J5-44 | P1-44 (A28J4) | DTR7 |
| 24 | WHT | J5-45 | P1-45 (A28J4) | CTS7 |

W5 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 24 | GRN | J5-46 | E4 | CHASSIS GND8 |
| 24 | WHT | JS-4 | P1-47 (A28J4) | DTR8 |
| 24 | WHT | J5-48 | P1-48 (A28J4) | CTS8 |
| 24 | WHT | J35-49 | P1-49 (A28J4) | OPINT |
| 24 | WHT | J5-50 | P1-50 (A28J4) | RESET |
|  | W6 |  |  |  |
| 26 | BLK TW | J6-2 | P1-26 (A28J8) | CPCLK \$ |
| 26 | WHT PR | J6-1 | P1-i (A28J8) | CPCLK * |
| 26 | BLK TW | J6-9 | P1-30 (A28J8) | CPCMDO \$ |
| 26 | WHT PR | J6-8 | P1-5 (A28J8) | CPCMDO * |
| 26 | BLK TW | J6-6 | P1-28 (A28J8) | CPCMD1 \$ |
| 26 | WHT PR | J6-5 | P1-3 (A28J8) | CPCMD1 * |
| 26 | BLK TW | J6-4 | P1-27 (.A28J8) | CPCMD2 \$ |
| 26 | WHT PR | J6-3 | P1-2 (A28J8) | CPCMD2* |
| 26 | BLK TW | J6-14 | P1-29 (A28J8) | CPCMD3 \$ |
| 26 | WHT PR | J6-7 | P1-4 (A28J8) | CPCMD3* |
| 26 | BLK TW | J6-13 | P1-32 (A28J8) | CPDOO \$ |
| 26 | WHT PR | J6-12 | P1-7 (A28J8) | CPDOO * |
| 26 | BLK TW | J6-24 | P1-33 (A28J8) | CPDO1 \$ |
| 26 | WHT PR | J6-15 | P1-8 (A28J8) | CPDO1 * |
| 26 | BLK TW | J6-17 | P1-34 (A28J8) | CPD02 \$ |
| 26 | WHT PR | J6-16 | P1-9 (A28J8) | CPD02 * |
| 26 | BLK TW | J6-19 | P1-35 (A28J8) | CPD03 \$ |
| 26 | WHT PR | J6-18 | P1-10 (A28J8) | CPD03 * |
| 26 | BLK TW | J6-21 | P1-36 (A28J8) | CPD04 \$ |
| 26 | WHT PR | J6-20 | P1-11 (A28J8) | CPD04 * |
| 26 | BLK TW | J6-23 | P1-37 (A28J8) | CPD05 \$ |
| 26 | WHT PR | J6-22 | P1-12 (A28J8) | CPD05 * |

W6 (continued)

| AWG | COLOR | FROM |
| :---: | :---: | :---: |
| 26 | BLK TW | J6-26 |
| 26 | WHT PR | J6-25 |
| 26 | BLK TW | J6-28 |
| 26 | WHT PR | J6-27 |
| 26 | BLK TW | J6-30 |
| 26 | WHT PR | J6-29 |
| 26 | BLK TW | J6-32 |
| 26 | WHT PR | J6-31 |
| 26 | BLK TW | J6-34 |
| 26 | WHT PR | J6-33 |
| 26 | BLK TW | J6-36 |
| 26 | WHT PR | J6-35 |
| 26 | BLK TW | J6-38 |
| 26 | WHT PR | J6-37 |
| 26 | BLK TW | J6-40 |
| 26 | WHT PR | J6-39 |
| 26 | BLK TW | J6-42 |
| 26 | WHT PR | J6-41 |
| 26 | BLK TW | J6-44 |
| 26 | WHT PR | J6-43 |
| 26 | BLK TW | J6-55 |
| 26 | WHT PR | J6-45 |
| 26 | BLK TW | J6-47 |
| 26 | WHT PR | J6-46 |
| 26 | BLK TW | J6-49 |
| 26 | WHT PR | J6-48 |
| 26 | BLK TW | J6-11 |
| 26 | WHT PR | J6-10 |
| 24 | BLK | J6-99 |
| 24 | WHT | J6-98 |

TO
P1-38 (A28J8)
P1-13 (A28J8)
P1-39 (A28J8)
P1-14 (A28J8)
P1-40 (A28J8)
P1-15 (A28J8)
P1-41 (A28J8)
P1-16 (A28J8)
P1-42 (A28J8)
P1-17 (A28J8)
P1-43 (A28J8)
P1-18 (A28J8)
P1-44 (A28J8)
P1-19 (A28J8)
P1-45 (A28J8)
P1-20 (A28J8)
P1-46 (A28J8)
P1-21 (A28J8)
P1-47 (A28J8)
P1-22 (A28J8)
P1-48 (A28J8)
P1-23 (A28J8)
P1-49 (A28J8)
P1-24 (A28J8)
P1-50 (A28J8)
P1-25 (A28J8)
P1-31 (A28J8)
P1-6 (A28J8)
P2-50 (A28.J9)
P2-25 (A28J9)

## REMARKS

CPD06 \$ CPD06 *

CPD07 \$ CPD07*

CPD08 \$ CPD08*

CPD09 \$ CPD09 *

CPD10 \$
CPD10*
CPD11 \$
CPD11 *
CPD12 \$
CPD12 *
CPD13 \$
CPD13*
CPD14 \$
CPDI4*
CPD15 \$
CPD15*
CPD16 \$
CPD16 *
CPD17 \$
CPD17*
CPD18 \$
CPD18 *
CPINT \$
CPINT *
BAT +
BAT -

W6 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 26 | BLK TW | J6-51 | P2-26 (A28J9) | CPD19 \$ |
| 26 | WHT PR | J6-50 | P2-1 (A28J9) | CPD19 * |
| 26 | BLK TW | J6-53 | P2-27 (A28J9) | CPD20 \$ |
| 26 | WHT PR | J6-52 | P2-2 (A28J9) | CPD20 * |
| 26 | BLK TW | J6-64 | P2-28 (A28J9) | CPD21 \$ |
| 26 | WHT PR | J6-54 | P2-3 (A28J9) | CPD21* |
| 26 | BLK TW | J6-57 | P2-29 (A28J9) | CPD22 \$ |
| 26 | WHT PR | J6-56 | P2-4 (A28J9) | CPD22 * |
| 26 | BLK TW | J6-59 | P2-30 (A28J9) | CPD23 \$ |
| 26 | WHT PR | J6-58 | P2-5 (A28J9) | CPD23 * |
| 26 | BLK TW | J6-61 | P2-31 (A28J9) | CPD24 \$ |
| 26 | WHT PR | J6-60 | P2-6 (A28J9) | CPD24 * |
| 26 | BLK TW | J6-63 | P2-32 (A28J9) | CPD25 \$ |
| 26 | WHT PR | J6-62 | P2-7 (A28J9) | CPD25 * |
| 26 | BLK TW | J6-66 | P2-33 (A28J9) | CPD26 \$ |
| 26 | WHT PR | J6-65 | P2-8 (A28J9) | CPD26 * |
| 26 | BLK TW | J6-68 | P2-34 (A28J9) | CPD27 \$ |
| 26 | WHT PR | J6-67 | P2-9 (A28J9) | CPD27 * |
| 26 | BLK TW | J6-70 | P2-35 (A28J9) | CPD28 \$ |
| 26 | WHT PR | J6-69 | P2-10 (A28J9) | CPD28* |
| 26 | BLK TW | J6-72 | P2-36 (A28J9) | CPD29 \$ |
| 26 | WHT PR | J6-71 | P2-11 (A28J9) | CPD29 * |
| 26 | BLK TW | J6-74 | P2-37 (A28J9) | CPD30 \$ |
| 26 | WHT PR | J6-73 | P2-12 (A28.J9) | CPD30 * |
| 26 | BLK TW | J6-76 | P2-38 (A28J9) | CPD31 \$ |
| 26 | WHT PR | J6-75 | P2-13 (A28J9) | CPD31 * |
| 26 | BLK TW | J6-80 | P2-40 (A28J9) | INTI \$ |
| 26 | WHT PR | J6-79 | P2-15 (A28J9) | INTI * |
| 26 | BLK TW | J6-78 | P2-39 (A28J9) | SPARE10 \$ |
| 26 | WHT PR | J6-77 | P2-14 (A28J9) | SPARE10 * |

W6 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 26 | BLK TW | J6-82 | P2-41 (A28J9) | SPARE2 \$ |
| 26 | WHT PR | J6-81 | P2-16 (A28J9) | SPARE2* |
| 26 | BLK TW | J6-92 | P2-42 (A28J9) | SPARE3 \$ |
| 26 | WHT PR | J6-83 | P2-17 (A28J9) | SPARE3* |
| 26 | BLK TW | J6-85 | P2-43 (A28J9) | SPARE4 \$ |
| 26 | WHT PR | J6-84 | P2-18 (A28J9) | SPARE4* |
| 26 | BLK TW | J6-87 | P2-44 (A28J9) | SPARE5 \$ |
| 26 | WHT PR | J6-86 | P2-19 (A28J9) | SPARE5* |
| 26 | BLK TW | J6-89 | P2-45 (A28J9) | SPARE6 \$ |
| 26 | WHT PR | J6-88 | P2-20 (A28J9) | SPARE6* |
| 26 | BLK TW | J6-91 | P2-46 (A28J9) | SPARE7 \$ |
| 26 | WHT PR | J6-90 | P2-21 (A28J9) | SPARE7* |
| 26 | BLK TW | J6-95 | P2-48 (A28J9) | SPARE8 \$ |
| 26 | WHT PR | J6-94 | P2-23 (A28J9) | SPARE8* |
| 26 | BLK TW | J6-97 | P2-49 (A28J9) | SPARE9 \$ |
| 26 | WHT PR | J6-96 | P2-24 (A28J9) | SPARE9* |
| 26 | GRN | J6-100 | E5 | CHASSIS GND |
|  | W7 |  |  |  |
| 24 | GRN | J7-5 | E6 | CHASSIS GND |
| 26 | BLK TW | J7-3 | P1-3 (A28J7) | LP-LKIU1 \$ |
| 26 | WHT PR | J17-2 | P1-2 (A28J7) | LP-LKIU1* |
| 26 | BLT TW | J17-12 | P1-12 (A28J7) | LP-LKIU2 \$ |
| 26 | WHT PR | J7-11 | P1-11 (A28J7) | LP-LKIU2 * |
| 26 | WHT TW | J17-7 | P1-6 (A28J7) | LP-RDIU \$ |
| 26 | BLK PR | J7-6 | P1-7 (A28J7) | LP-RDIU * |
| 26 | BLK TW | J7-10 | P1-7 (A28J7) | SPARE1 \$ |
| 26 | WHT PR | J7-1 | P1-1 (A28J7) | SPARE1* |
| 26 | BLK TW | J7-9 | P1-9 (A28J7) | SPARE2 \$ |
| 26 | WHT PR | J7-8 | P1-8 (A28J7) | SPARE2* |
| 26 | WHT TW | J7-4 | P1-4 (A28J7) | SPARE3* |
| 26 | BLK PR | J7-13 | P1-13 (A28J7) | SPARE3 \$ |

## C-12

W8

| AWG |
| :--- |
| 24 |
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| COLOR | FROM |
| :--- | :--- |
| GRN | $\mathrm{J} 8-5$ |
| BLK TW | $\mathrm{J} 83-3$ |
| WHT PR | $\mathrm{J} 8-?$ |
| BLK TW | $\mathrm{J} 8-12$ |
| WHT PR | $\mathrm{J} 8-11$ |
| BLK TW | $\mathrm{J} 8-6$ |
| WHT PR | $\mathrm{J} 8-7$ |
| BLK TW | $\mathrm{J} 8-10$ |
| WHT PR | $\mathrm{J} 8-1$ |
| BLK TW | $\mathrm{J8} 8$ |
| WHT PR | $\mathrm{J} 8-8$ |
| WHT TW | $\mathrm{J} 8-4$ |
| BLK PR | $\mathrm{J} 8-13$ |


| GRN | $\mathrm{J} 11-55$ |
| :--- | :---: |
| BLK TW | $\mathrm{J} 11-1$ |
| WHT PR | $\mathrm{J} 11-2$ |
| BLK TW | $\mathrm{J} 11-3$ |
| WHT PR | $\mathrm{J} 11-4$ |
| BLK TW | $\mathrm{J} 11-5$ |
| WHT PR | $\mathrm{J} 11-6$ |
| BLK TW | $\mathrm{J} 11-7$ |
| WHT PR | $\mathrm{J} 11-8$ |
| BLK TW | $\mathrm{J} 11-9$ |
| WHT PR | $\mathrm{J} 11-10$ |
| BLK TW | $\mathrm{J} 11-11$ |
| WHT PR | $\mathrm{J} 11-12$ |
| BLK TW | $\mathrm{J} 11-13$ |
| WHT PR | $\mathrm{J} 11-14$ |

## w9

E8
P1-1 (A28J2)
P1-2 (A28J2)
P1-3 (A28J2)
P1-4 (A28J2)
P1-5 (A28J2)
P1-6 (A28J2)
P1-7 (A28J2)
P1-8 (A28J2)
P1-9 (A28J2)
P1-10 (A28J2)
P1-11 (A28J2)
P1-12 (A28J2)
P1-13 (A28J2)
P1-14 (A28J2)

## W9 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 26 | BLK TW | J11-15 | P1-15 (A28J2) | LPA-FRUI \$ |
| 26 | WHT PR | J11-16 | P1-16 (A28J2) | LPA-FRUI * |
| 26 | BLK TW | J11-17 | P1-17 (A28J2) | LPA-FRUQ \$ |
| 26 | WHT PR | J11-18 | P1-18 (A28J2) | LPA-FRUQ * |
| 26 | BLK TW | J11-19 | P1-19 (A28J2) | LPA-FRURTRG \$ |
| 26 | WHT PR | J11-20 | P1-20 (A28J2) | LPA-FRURTRG * |
| 26 | BLK TW | J11-21 | P1-21 (A28J2) | LPA-LA \$ |
| 26 | WHT PR | J11-22 | P1-22 (A28J2) | LPA-LA * |
| 26 | BLK TW | J11-23 | P1-23 (A28J2) | LPA-PHRVTRG \$ |
| 26 | WHT PR | J11-24 | P1-24 (A28J2) | LPA-PHRVTRG * |
| 26 | BLK TW | J11-25 | P1-25 (A28J2) | LPA-PWG \$ |
| 26 | WHT PR | J11-26 | P1-26 (A28J2) | LPA-PWG * |
| 26 | BLK TW | J11-27 | P1-27 (A28J2) | LPA-PWRST \$ |
| 26 | WHT PR | J11-28 | P1-28 (A28J2) | LPA-PWRST * |
| 26 | BLK TW | J11-29 | P1-29 (A28J2) | LPA-RRST \$ |
| 26 | WHT PR | J11-30 | P1-30 (A28J2) | LPA-RRST * |
| 26 | BLK TW | J11-31 | P1-31 (A28J2) | LPA-SBFLG \$ |
| 26 | WHT PR | J11-32 | P1-32 (A28J2) | LPA-SBFLG * |
| 26 | BLK TW | J11-33 | P1-33 (A28J2) | LPA-STRG \$ |
| 26 | WHT PR | J11-34 | P1-34 (A28J2) | LPA-STRG * |
| 26 | BLK TW | J11-36 | P1-36 (A28J2) | SPARE1 \$ |
| 26 | WHT PR | J11-35 | P1-35 (A28J2) | SPARE1* |
| 26 | BLK TW | J11-38 | P1-38 (A28J2) | SPARE2 \$ |
| 26 | WHT PR | J11-37 | P1-37 (A28J2) | SPARE2* |
| 26 | BLK TW | J11-40 | P1-40 (A28J2) | SPARE3 \$ |
| 26 | WHT PR | J11-39 | P1-39 (A28J2) | SPARE3* |
| 26 | BLK TW | J11-42 | P1-42 (A28J2) | SPARE4 \$ |
| 26 | WHT PR | J11-41 | P1-41 (A28J2) | SPARE4* |
| 26 | BLK TW | J11-44 | P1-44 (A28J2) | SPARE5 \$ |
| 26 | WHT PR | J11-43 | P1-43 (A28J2) | SPARE5* |

## W9 (continued)

| AWG |
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| 26 |
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| COLOR | FROM |
| :--- | ---: |
| BLK TW | $\mathrm{J} 11-46$ |
| WHT PR | $\mathrm{J} 11-45$ |
|  |  |
| BLK TW | $\mathrm{J} 11-48$ |
| WHT PR | $\mathrm{J} 11-47$ |
| BLK TW | $\mathrm{J} 11-50$ |
| WHT PR | $\mathrm{J} 11-49$ |
|  |  |
| BLK TW | $\mathrm{J} 11-52$ |
| WHT PR | $\mathrm{J} 11-51$ |
| BLK TW | $\mathrm{J} 11-54$ |
| WHT PR | $\mathrm{J} 11-53$ |

J12-55

| GRN | $\mathrm{J} 12-55$ |
| :--- | :---: |
| BLK TW | $\mathrm{J} 12-1$ |
| WHT PR | $\mathrm{J} 12-2$ |
| BLK TW | $\mathrm{J} 12-3$ |
| WHT PR | $\mathrm{J} 12-4$ |
| BLK TW | $\mathrm{J} 12-5$ |
| WHT PR | $\mathrm{J} 12-6$ |
| BLK TW | $\mathrm{J} 12-7$ |
| WHT PR | $\mathrm{J} 12-8$ |
| BLK TW | $\mathrm{J} 12-9$ |
| WHT PR | $\mathrm{J} 12-10$ |


| BLK TW | J12-11 |
| :--- | :--- |
| WHT PR | J12-12 |

BLK TW WHT PR

J12-13
J12-14
BLK TW
WHT PR
J12-15
J12-16
BLK TW
J12-17
WHT PR

TO
P1-46 (A28J2)
P1-45 (A28J2)
P1-48 (A28J2)
P1-47 (A28J2)
P1-50 (A28J2)
P1-49 (A28J2)
P1-52 (A28J2)
P1-51 (A28J2)
P1-54 (A28J2)
P1-53 (A28J2)

## W10

| E9 | CHASSIS GND |
| :--- | :--- |
| P1-1 (A28J3) | LPB-CWFLG \$ |
| P1-2 (A28J3) | LPB-CWFLG * |
| P1-3 (A28J3) | LPB-DFADI \$ |
| P1-4 (A28J3) | LPB-DFADI * |
| P1-5 (A28J3) | LPB-DFADQ \$ |
| P1-6 (A28J3) | LPB-DFADQ * |
| P1-7 (A28J3) | LPB-DFBCI \$ |
| P1-8 (A28J3) | LPB-DFBCI * |
| P1-9 (A28J3) | LPB-DFBCQ \$ |
| P1-10 (A28J3) | LPB-DFBCQ * |
| P1-11 (A28J3) | LPB-DFACI \$ |
| P1-12 (A28J3) | LPB-DFACI * |
| P1-13 (A28J3) | LPB-DFACQ \$ |
| P1-14 (A28J3) | LPB-DFACQ * |
| P1-15 (A28J3) | LPB-FRUI \$ |
| P1-16 (A28J3) | LPB-FRUI * |
| P1-17 (A28J3) | LPB-FRUQ \$ |
| P1-18 (A28J3) | LPB-FRUQ * |

## W10 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 26 | BLK TW | J12-19 | P1-19 (A28J3) | LPB-FRURTRG \$ |
| 26 | WHT PR | J12-20 | P1-20 (A28J3) | LPB-FRURTRG * |
| 26 | BLK TW | J12-21 | P1-21 (A28J3) | LPB-LA \$ |
| 26 | WHT PR | J12-22 | P1-22 (A28J3) | LPB-LA * |
| 26 | BLK TW | J12-23 | P1-23 (A28J3) | LPB-PHRVTRG \$ |
| 26 | WHT PR | J12-24 | P1-24 (A28J3) | LPB-PHRVTRG * |
| 26 | BLK TW | J12-25 | P1-25 (A28J3) | LPB-PWG \$ |
| 26 | WHT PR | J12-26 | P1-26 (A28J3) | LPB-PWG * |
| 26 | BLK TW | J12-27 | P1-27 (A28J3) | LPB-PWRST \$ |
| 26 | WHT PR | J12-28 | P1-28 (A28J3) | LPB-PWRST * |
| 26 | BLK TW | J12-29 | P1-29 (A28J3) | LPB-RRST \$ |
| 26 | WHT PR | J12-30 | P1-30 (A28J3) | LPB-RRST * |
| 26 | BLK TW | J12-31 | P1-31 (A28J3) | LPB-SBFLG \$ |
| 26 | WHT PR | J12-32 | P1-32 (A23J3) | LPB-SBFLG * |
| 26 | BLK TW | J12-33 | P1-33 (A28J3) | LPB-STRG \$ |
| 26 | WHT PR | J12-34 | P1-34 (A28J3) | LPB-STRG * |
| 26 | BLK TW | J12-36 | P1-36 (A28J3) | SPARE1 \$ |
| 26 | WHT PR | J12-35 | P1-35 (A28J3) | SPARE1* |
| 26 | BLK TW | J12-38 | P1-38 (A28J3) | SPARE2 \$ |
| 26 | WHT PR | J12-37 | P1-37 (A28J3) | SPARE2 * |
| 26 | BLK TW | J12-40 | P1-40 (A28J3) | SPARE3 \$ |
| 26 | WHT PR | J12-39 | P1-39 (A28J3) | SPARE3* |
| 26 | BLK TW | J12-42 | P1-42 (A28J3) | SPARE4 \$ |
| 26 | WHT PR | J12-41 | P1-41 (A28J3) | SPARE4* |
| 26 | BLK TW | J12-44 | P1-44 (A28J3) | SPARE5 \$ |
| 26 | WHT PR | J12-43 | P1-43 (A28J3) | SPARE5* |
| 26 | BLK TW | J12-46 | P1-46 (A28J3) | SPARE6 \$ |
| 26 | WHT PR | J12-45 | P1-45 (A28J3) | SPARE6* |
| 26 | BLK TW | J12-48 | P1-48 (A28J3) | SPARE7 \$ |
| 26 | WHT PR | J12-47 | P1-47 (A28J3) | SPARE7* |

## W10 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 26 | BLK TW | J12-50 | P1-50 (A28J3) | SPARE8 \$ |
| 26 | WHT PR | J12-49 | P1-49 (A28J3) | SPARE8* |
| 26 | BLK TW | J12-52 | P1-52 (A28J3) | SPARE9 \$ |
| 26 | WHT PR | J12-51 | P1-51 (A28J3) | SPARE9* |
| 26 | BLK TW | J12-54 | P1-54 (A23J3) | SPARE10 \$ |
| 26 | WHT PR | J12-53 | P1-53 (A28J3) | SPARE10* |
|  | W11 |  |  |  |
| 24 | GRN | J13-55 | E10 | CHASSIS GND |
| 26 | BLK TW | J13-1 | P1-1 (A28J14) | RPA-CWFLG \$ |
| 26 | WHT PR | J13-2 | P1-2 (A28J14) | RPA-CWFLG * |
| 26 | BLK TW | J13-3 | P1-3 (A28J14) | RPA-DFADI \$ |
| 26 | WHT PR | J13-4 | P1-4 (A28J14) | RPA-DFADI * |
| 26 | BLK TW | J13-5 | P1-5 (A28J14) | RPA-DFADQ \$ |
| 26 | WHT PR | J13-6 | P1-6 (A28J14) | RPA-DFADQ * |
| 26 | BLK TW | J13-7 | P1-7 (A28J14) | RPA-DFBCI \$ |
| 26 | WHT PR | J13-8 | P1-8 (A28J14) | RPA-DFBCI * |
| 26 | BLK TW | J13-9 | P1-9 (A28J14) | RPA-DFBCQ \$ |
| 26 | WHT PR | J13-10 | P1-10 (A28J14) | RPA-DFBCQ * |
| 26 | BLK TW | J13-11 | P1-11 (A28J14) | RPA-DFACI \$ |
| 26 | WHT PR | J13-12 | P1-12 (A28J14) | RPA-DFACI * |
| 26 | BLK TW | J13-13 | P1-13 (A28J14) | RPA-DFACQ \$ |
| 26 | WHT PR | J13-14 | P1-14 (A28J14) | RPA-DFACQ * |
| 26 | BLK TW | J13-15 | P1-15 (A28J14) | RPA-FRUI \$ |
| 26 | WHT PR | J13-16 | P1-16 (A28J14) | RPA-FRUI * |
| 26 | BLK TW | J13-17 | P1-17 (A28J14) | RPA-FRUQ \$ |
| 26 | WHT PR | J13-18 | P1-18 (A28J14) | RPA-FRUQ* |
| 26 | BLK TW | J13-19 | P1-19 (A28J14) | RPA-FRURTRG \$ |
| 26 | WHT PR | J13-20 | P1-20 (A28J14) | RPA-FRURTRG * |
| 26 | BLK TW | J13-21 | P1-21 (A28J14) | RPA-LA \$ |
| 26 | WHT PR | J13-22 | P1-22 (A28J14) | RPA-LA * |

## W11 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 26 | BLK TW | J13-23 | P1-23 (A28J14) | RPA-PHRVTRG \$ |
| 26 | WHT PR | J13-24 | P1-24 (A28J14) | RPA-PHRVTRG * |
| 26 | BLK TW | J13-25 | P1-25 (A28J14) | RPA-PWG \$ |
| 26 | WHT PR | J13-26 | P1-26 (A28J14) | RPA-PWG * |
| 26 | BLK TW | J13-27 | P1-27 (A28J14) | RPA-PWRST \$ |
| 26 | WHT PR | J13-28 | P1-28 (A28J14) | RPA-PWRST * |
| 26 | BLK TW | J13-29 | P1-29 (A28J14) | RPA-RRST \$ |
| 26 | WHT PR | J13-30 | P1-30 (A28J14) | RPA-RRST * |
| 26 | BLK TW | J13-31 | P1-31 (A28J14) | RPA-SBFLG \$ |
| 26 | WHT PR | J13-32 | P1-32 (A28J14) | RPA-SBFLG * |
| 26 | BLK TW | J13-33 | P1-33 (A28J14) | RPA-STRG \$ |
| 26 | WHT PR | J13-34 | P1-34 (A28J14) | RPA-STRG * |
| 26 | BLK TW | J13-36 | P1-36 (A28J14) | SPARE1 \$ |
| 26 | WHT PR | J13-35 | P1-35 (A28J14) | SPARE1* |
| 26 | BLK TW | J13-38 | P1-38 (A28J14) | SPARE2 \$ |
| 26 | WHT PR | J13-37 | P1-37 (A28J14) | SPARE2 * |
| 26 | BLK TW | J13-40 | P1-40 (A28J14) | SPARE3 \$ |
| 26 | WHT PR | J13-39 | P1-39 (A28J14) | SPARE3* |
| 26 | BLK TW | J13-42 | P1-42 (A28J14) | SPARE4 \$ |
| 26 | WHT PR | J13-41 | P1-41 (A28J14) | SPARE4* |
| 26 | BLK TW | J13-44 | P1-44 (A28J14) | SPARE5 \$ |
| 26 | WHT PR | J13-43 | P1-43 (A28J14) | SPARE5* |
| 26 | BLK TW | J13-46 | P1-46 (A28J14) | SPARE6 \$ |
| 26 | WHT PR | J13-45 | P1-45 (A28J14) | SPARE6* |
| 26 | BLK TW | J13-48 | P1-48 (A28J14) | SPARE7 \$ |
| 26 | WHT PR | J13-47 | P1-47 (A28J14) | SPARE7* |
| 26 | BLK TW | J13-50 | P1-50 (A28J14) | SPARE8 \$ |
| 26 | WHT PR | J13-49 | P1-49 (A28J14) | SPARE8* |
| 26 | BLK TW | J13-52 | P1-52 (A28J14) | SPARE9 \$ |
| 26 | WHT PR | J13-51 | P1-51 (A28J14) | SPARE9* |
| 26 | BLK TW | J13-54 | P1-54 (A28J14) | SPARE10 \$ |
| 26 | WHT PR | J13-53 | P1-53 (A28J14) | SPARE10* |

## C-18

W12

| AWG | COLOR | FROM |
| :---: | :---: | :---: |
| 24 | GRN | J14-55 |
| 26 | BLK TW | J14-1 |
| 26 | WHT PR | J14-2 |
| 26 | BLK TW | J14-3 |
| 26 | WHT PR | J14-4 |
| 26 | BLK TW | J14-5 |
| 26 | WHT PR | J14-6 |
| 26 | BLK TW | J14-7 |
| 26 | WHT PR | J14-8 |
| 26 | BLK TW | J14-9 |
| 26 | WHT PR | J14-10 |
| 26 | BLK TW. | J14-11 |
| 26 | WHT PR | J14-12 |
| 26 | BLK TW | J14-13 |
| 26 | WHT PR | J14-14 |
| 26 | BLK TW | J14-15 |
| 26 | WHT PR | J14-16 |
| 26 | BLK TW | J14-17 |
| 26 | WHT PR | J14-18 |
| 26 | BLK TW | J14-19 |
| 26 | WHT PR | J14-20 |
| 26 | BLK TW | J14-21 |
| 26 | WHT PR | J14-22 |
| 26 | BLK TW | J14-23 |
| 26 | WHT PR | J14-24 |
| 26 | BLK TW | J14-25 |
| 26 | WHT PR | J14-26 |
| 26 | BLK TW | J14-27 |
| 26 | WHT PR | J14-28 |
| 26 | BLK TW | J14-29 |
| 26 | WHT PR | J14-30 |


| TO | REMARKS |
| :---: | :---: |
| E11 | CHASSIS GND |
| P1-1 (A28J13) | RPB-CWFLG \$ |
| P1-2 (A28J13) | RPB-CWFLG * |
| P1-3 (A28J13) | RPB-DFADI \$ |
| P1-4 (A28J13) | RPB-DFADI * |
| P1-5 (A28J13) | RPB-DFADQ \$ |
| P1-6 (A28J13) | RPB-DFADQ * |
| P1-7 (A28J13) | RPB-DFBCI \$ |
| P1-8 (A28J13) | RPB-DFBCI * |
| P1-9 (A28J13) | RPB-DFBCQ \$ |
| P1-10 (A28J13) | RPB-DFBCQ * |
| P1-II (A28J13) | RPB-DFACI \$ |
| P1-12 (A28J13) | RPB-DFACI * |
| P1-13 (A28J13) | RPB-DFACQ \$ |
| P1-14 (A28J13) | RPB-DFACQ * |
| P1-15 (A28J13) | RPB-FRUI \$ |
| P1-16 (A28J13) | RPB-FRUI * |
| P1-17 (A28J13) | RPB-FRUQ \$ |
| P1-18 (A28J13) | RPB-FRUQ * |
| P1-19 (A28J13) | RPB-FRURTRG \$ |
| P1-20 (A28J13) | RPB-FRURTRG * |
| P1-21 (A28J13) | RPB-LA \$ |
| P1-22 (A28J13) | RPB-LA * |
| P1-23 (A28J13) | RPB-PHRVTRG \$ |
| P1-24 (A28J13) | RPB-PHRVTRG * |
| P1-25 (A28J13) | RPB-PWG \$ |
| P1-26 (A28J13) | RPB-PWG * |
| P1-27 (A28J13) | RPB-PWRST \$ |
| P1-28 (A28J13) | RPB-PWRST * |
| P1-29 (A28J13) P1-30 (A28J13) | RPB-RRST \$ RPB-RRST * |

## W12 (continued)

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 26 | BLK TW | J14-31 | P1-31 (A28J13) | RPB-SBFLG \$ |
| 26 | WHT PR | J14-32 | P1-32 (A28J13) | RPB-SBFLG * |
| 26 | BLK TW | J14-33 | P1-33 (A28J13) | RPB-STRG \$ |
| 26 | WHT PR | J14-34 | P1-34 (A28J13) | RPB-STRG * |
| 26 | BLK TW | J14-36 | P1-36 (A28J13) | SPARE1 \$ |
| 26 | WHT PR | J14-35 | P1-35 (A28J13) | SPARE1* |
| 26 | BLK TW | J14-38 | P1-38 (A28J13) | SPARE2 \$ |
| 26 | WHT PR | J14-37 | P1-37 (A28J13) | SPARE2* |
| 26 | BLK TW | J14-40 | P1-40 (A28J13) | SPARE3 \$ |
| 26 | WHT PR | J14-39 | P1-39 (A28J13) | SPARE3* |
| 26 | BLK TW | J14-42 | P1-42 (A28J13) | SPARE4 \$ |
| 26 | WHT PR | J14-41 | P1-41 (A28J13) | SPARE4* |
| 26 | BLK TW | J14-44 | P1-44 (A28J13) | SPARE5 \$ |
| 26 | WHT PR | J14-43 | P1-43 (A28J13) | SPARE5* |
| 26 | BLK TW | J14-46 | P1-46 (A28J13) | SPARE6 \$ |
| 26 | WHT PR | J14-46 | P1-45 (A28J13) | SPARE6 * |
| 26 | BLK TW | J14-48 | P1-48 (A28J13) | SPARE7 \$ |
| 26 | WHT PR | J14-47 | P1-47 (A28J13) | SPARE7* |
| 26 | BLK TW | J14-50 | P1-50 (A28J13) | SPARE8 \$ |
| 26 | WHT PR | J14-49 | P1-49 (A28J13) | SPARE8* |
| 26 | BLK TW | J14-52 | P1-52 (A28J13) | SPARE9 \$ |
| 26 | WHT PR | J14-51 | P1-51 (A28J13) | SPARE9* |
| 26 | BLK TW | J14-54 | P1-54 (A28J13) | SPARE10 \$ |
| 26 | WHT PR | J14-53 | P1-53 (A28J13) | SPARE10* |

W13

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 24 | GRN | J20-14 | E13 | CHASSIS GND |
| 24 | BLK | J20-22 | P1-22 (A28J12) | GND-SIG-21 |
| 26 | BLK TW | J20-2 | P1-2 (A28J12) | (TST) DLRXCLK \$ |
| 26 | WHT PR | J20-3 | P1-3 (A28J12) | (TST) DLRXCLK * |
| 26 | BLK TW | J20-4 | P1-4 (A28J12) | (TST) DLTXCLK \$ |
| 26 | WHT PR | J20-5 | P1-5 (A28J12) | (TST) DLTXCLK * |
| 26 | BLK TW | J20-6 | P1-6 (A28J12) | DLRXCLK \$ |
| 26 | WHT PR | J20-7 | P1-7 (A28J12) | DLRXCLK* |
| 26 | BLK TW | J20-8 | P1-8 (A28J12) | DLRXD \$ |
| 26 | WHT PR | J20-9 | P1-9 (A28J12) | DLRXD * |
| 26 | BLK TW | J20-10 | P1-10 (A28J12) | DLTXCLK \$ |
| 26 | WHT PR | J20-11 | P1-11 (A28J12) | DLTXCLK* |
| 26 | BLK TW | J20-12 | P1-12 (A28J12) | DLTXD \$ |
| 26 | WHT PR | J20-13 | P1-13 (A28J12) | DLTXD * |
| 26 | BLK TW | J20-17 | P1-17 (A28J12) | SPARE1 \$ |
| 26 | WHT PR | J20-16 | P1-16 (A28J12) | SPARE1* |
| 26 | BLK TW | J20-19 | P1-19 (A28J12) | SPARE2 \$ |
| 26 | WHT PR | J20-18 | P1-18 (A28J12) | SPARE2 * |
| 26 | BLK TW | J20-21 | P1-21 (A28J12) | SPARE3 \$ |
| 26 | WHT PR | J20-20 | P1-20 (A28J12) | SPARE3 * |
| W14 ( Coax Cable) |  |  |  |  |
|  |  | G1J1 | A1J1 | 10 MHz REF |

W15

| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 22 | GRN | J17-A | E14 | CHASSIS GND |
| 22 | RED | J17-B | A28XA3-135 | BATT + |
| 22 | BLK | J17-C | A28XA3-131 | BATT - |
| 22 | WHT/RED | J17-D | P2-3 | FAN - |
| 22 | WHT/RED | J17-D | P2-4 | FAN + |
| 22 | WHT/BLK | J17-E | P2-7 | FAN RTN |
| 22 | WHT/BLK | J17-E | P2-8 | FAN RTN |
| 22 | WHT/RED | G1P1-1 | A28J6-1 | +28 VDC |
| 22 | WHT/RED | G1P1-1 | P1-7 | +28 VDC |
| 22 | WHT/RED | G1P1-7 | P1-1 | +28 VDC |
| 22 | WHT/BLK | G1P1-8 | A28J6-2 | +28 VDC RTN |
| 26 | BLK TW | J9-IS | A28XA15-81 | RDC BUS LO |
| 26 | WHT PR | J9-IC | A28XA15-82 | RDC BUS HI |
| 26 | BLK TW | J9-IS | J10-IS | RDC BUS LO |
| 26 | WHT PR | J9-IC | J10-IC | RDC BUS HI |
| 26 | BLK TW | J16-IS | A28XA27-81 | CP BUS LO |
| 26 | WHT PR | J16-IC | A28XA27-82 | CP BUS HI |
| 26 | BLK TW | J16-IS | J15-IS | CP BUS LO |
| 26 | WHT PR | J16-IC | J15-IC | CP BUS HI |
| 16 | GRN | J18-A | E15 | CHASSIS GND |
| 16 | BLK | J18-B | GND BUS | GND |
| 16 | BLK | J18-C | GND BUS | GND |
| 16 | BLK | J18-D | GND BUS | GND |


| AWG | COLOR | FROM | TO | REMARKS |
| :---: | :---: | :---: | :---: | :---: |
| 16 | RED | J18-E | +5V BUS | +5 VDC |
| 16 | RED | J18-F | +5V BUS | +5 VDC |
| 16 | RED | J18-G | +5V BUS | +5 VDC |
| 16 | RED | J18-H | +5V BUS | +5 VDC |
| 16 | RED | J18-J | +5V BUS | +5 VDC |
| 16 | RED | J18-K | +5V BUS | +5 VDC |
| 16 | RED | J18-L | +5V BUS | +5 VDC |
| 16 | RED | J18-M | +5V BUS | +5 VDC |
| 16 | BLK | J18-N | GND BUS | GND |
| 16 | BLK | J18-P | GND BUS | GND |
| 16 | BLK | J18-R | GND BUS | GND |
| 16 | BLK | J18-S | GND BUS | GND |
| 16 | BLK | J18-T | GND BUS | GND |
| 16 | BLK | J18-U | GND BUS | GND |
| 16 | RED | J18-V | +5V BUS | +5 VDC |
| 16 | RED | J18-W | +5V BUS | +5 VDC |
| 16 | RED | J18-X | +5V BUS | +5 VDC |
| 16 | RED | J18-Y | +5V BUS | +5 VDC |
| 16 | RED | J18-Z | +5V BUS | +5 VDC |
| 16 | BLK | J18-a | GND BUS | GND |
| 16 | BLK | J18-b | GND BUS | GND |
| 16 | BLK | J18-C | GND BUS | GND |
| 16 | BLK | J18-d | GND BUS | GND |
| 16 | RED | J18-e | +5V BUS | +5 VDC |
| 16 | BLK | J18-f | GND BUS | GND |

## C-23/(C-24 blank)

## APPENDIX D

ILLUSTRATED LIST OF MANUFACTURED ITEMS

## TEST FIXTURE FABRICATION

a. Parts Required.
(1) MS27467TIIB5S -
(2) RJS12R -
(3) M16878/4BFE2 -
(4) M16874/4BFEO -
(5) Solder

Connector
12-ohm 50W potentiometer
Wire, \#22 gauge, red
Wire, \#22 gauge, black

> MS2746T1185S
> MATES WITH J17


D-1
b. Assembly.
(1) Crimp red wire to connector pin B3.
(2) Crimp black wire to connector pin C .

## WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.
(3) Solder red wire to resistor CCW terminal.
(4) Solder black wire to resistor wiper terminal.


| REFERENCE <br> DESIGNATION | COMPONENTS | KEY |
| :---: | :--- | :---: |
| A1 | TOIA CCA | 1 |
| A3 | BATTERY REFULATOR CCA | 20 |
| A4 | TOIB CCA | 2 |
| A5 | DIGITIZER A1 CCA | 19 |
| A6 | DIGITIZER A2 CCA | 3 |
| A7 | DIGITIZER B CCA | 18 |
| A9 | DOAA CCA | 4 |
| A11 | CP INTERFACE CCA | 17 |
| A12 | IFPCTRL A CCA | 5 |
| A13 | IFPCTRL B CCA | 16 |
| A15 | INTERFACE UNIT BUS 2 CCA | 6 |
| A16 | I553B2 CCA | 15 |
| A17 | SRAM 2 CCA | 7 |
| A18 | DBP CCA | 14 |
| A20 | INTERFACE UNIT BUS 1 CCA | 8 |
| A21 | SRAM 1 CCA | 9 |
| A23 | ATIDU CCA | 13 |
| A26 | IU DL CCA | 10 |
|  | 1553B1 CCA | 12 |
|  |  | 11 |

FO-1. Component Locations (circuit Card Assemblies) (Sheet 1 of 4)


| REFERENCE DESIGNATION | COMPONENTS | KEY |
| :---: | :---: | :---: |
| J1 | CONNECTOR J1 | 1 |
| J2 | CONNECTOR J2 | 2 |
| J3 | CONNECTOR J3 | 3 |
| J4 | CONNECTOR J4 | 4 |
| J6 | CONNECTOR J6 | 5 |
| J7 | CONNECTOR J7 | 6 |
| J8 | CONNECTOR J8 | 7 |
| J15 | CONNECTOR J15 | 8 |
| J16 | CONNECTOR J16 | 9 |
| J14 | CONNECTOR J14 | 10 |
| J20 | CONNECTOR J20 | 11 |
| J19 | CONNECTOR J19 | 12 |
| J18 | CONNECTOR J18 | 13 |
| J13 | CONNECTOR J13 | 14 |
| J12 | CONNECTOR J12 | 15 |
| J17 | CONNECTOR J17 | 16 |
| J11 | CONNECTOR J11 | 17 |
| J10 | CONNECTOR J10 | 18 |
| J9 | CONNECTOR J9 | 19 |
| J5 | CONNECTOR J5 | 20 |



| REFERENCE <br> DESIGNATION | COMPONENTS | KEY |
| :---: | :--- | :---: |
| R3 | REFERENCE VOLTAGE POTENTIOMETER ADJUSTMENT POINT - DIG B (A7) | 1 |
| TP1 | TEST POINT 1 - DIG B (A7) | 2 |
| R5 | BIT VOLTAGE POTENTIOMETER ADJUSTMENT POINT - DIG B (A7) | 3 |
| TP2 | TEST POINT 2 - DIG B (A7) | 4 |
| TP3 | GROUND - DIG B (A7) | 5 |
| R3 | REFERENCE VOLTAGE POTENTIOMETER ADJUSTMENT POINT - DIG A2 (A6) | 6 |
| TP1 | TEST POINT 1 - DIG A2 (A6) | 7 |
| R5 | BIT VOLTAGE POTENTIOMETER ADJUSTMENT POINT - DIG A2 (A6) | 8 |
| TP2 | TEST POINT 2 - DIG A2 (A6) | 9 |
| TP3 | GROUND - DIG A2 (A6) | 10 |
| R3 | REFERENCE VOLTAGE POTENTIOMETER ADJUSTMENT POINT - DIG A1 (A5) | 11 |
| TP1 | TEST POINT 1 - DIG A1 (A5) | 12 |
| R5 | BIT VOLTAGE POTENTIOMETER ADJUSTMENT POINT - DIG A1 (A5) | 13 |
| TP2 | TEST POINT 2 - DIG A1 (A5) | 14 |
| TP3 | GROUND - DIG A1 (A5) | 15 |


$\left.\begin{array}{|c|l|c|}\hline \begin{array}{c}\text { REFERENCE } \\ \text { DESIGNATION }\end{array} & & \text { COMPONENTS }\end{array}\right]$ KEY

FO-1. Component Locations (Test and Adjust Points) (Sheet 4 of 4)


By Order of the Secretary of the Army:
GORDON R. SULLIVAN
General, United States Army
Chief of Staff
Official:
Nutal od
MILTON H. HAMILTON
Administrative Assistant to the Secretary of the Army 01322

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# THE METRIC SYSTEM AND EQUIVALENTS 

NEAR MEASURE

Centimeter $=10$ Millimeters $=0.01$ Meters $=0.3937$ Inches 1 Meter $=100$ Centimeters $=1000$ Millimeters $=39.37$ Inches 1 Kilometer $=1000$ Meters $=0.621$ Miles
'VEIGHTS
Gram $=0.001$ Kilograms $=1000$ Milligrams $=0.035$ Ounces $1 \mathrm{Kilogram}=1000 \mathrm{Grams}=2.2 \mathrm{lb}$.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

## LIQUID MEASURE

1 Milliliter $=0.001$ Liters $=0.0338$ Fluid Ounces
1 Liter $=1000$ Milliliters $=33.82$ Fluid Ounces

## SQUARE MEASURE

1 Sq. Centimeter $=100$ Sq. Millimeters $=0.155$ Sq. Inches 1 Sq. Meter $=10,000 \mathrm{Sq}$. Centimeters $=10.76$ Sq. Feet
1 Sq. Kilometer $=1,000,000 \mathrm{Sq}$. Meters $=0.386$ Sq. Miles

## CUBIC MEASURE

1 Cu. Centimeter $=1000 \mathrm{Cu}$. Millimeters $=0.06 \mathrm{Cu}$. Inches 1 Cu. Meter $=1,000,000 \mathrm{Cu}$. Centimeters $=35.31 \mathrm{Cu}$. Feet

## TEMPERATURE

$5 / 9\left({ }^{\circ} \mathrm{F}-32\right)={ }^{\circ} \mathrm{C}$
$212^{\circ}$ Fahrenheit is evuivalent to $100^{\circ}$ Celsius
$90^{\circ}$ Fahrenheit is equivalent to $32.2^{\circ}$ Celsius
$32^{\circ}$ Fahrenheit is equivalent to $0^{\circ}$ Celsius
$9 / 5 \mathrm{C}^{\circ}+32={ }^{\circ} \mathrm{F}$

## APPROXIMATE CONVERSION FACIORS

| to Change | TO | MULTIPLY BY |
| :---: | :---: | :---: |
| Inches | Centimeters | 2.540 |
| Feet | Meters. | 0.305 |
| Yards | Meters | 0.914 |
| Miles | Kilometers | 1.609 |
| Square Inches | Square Centimeters. | 6.451 |
| Square Feet | Square Meters | 0.093 |
| Square Yards | Square Meters | 0.836 |
| Square Miles | Square Kilometers | 2.590 |
| Acres | Square Hectometers | 0.405 |
| Cubic Feet | Cubic Meters ....... | 0.028 |
| Cubic Yards | Cubic Meters | 0.765 |
| Fluid Ounces | Milliliters. | 29.573 |
| its | Liters. | 0.473 |
| arts. | Liters. | 0.946 |
| , allons | Liters. | 3.785 |
| Ounces | Grams | 28.349 |
| Pounds | Kilograms | 0.454 |
| Short Tons | Metric Tons | 0.907 |
| Pound-Feet | Newton-Meters | 1.356 |
| Pounds per Square Inch | Kilopascals | 6.895 |
| Miles per Gallon........ | Kilometers per Liter | 0.425 |
| Miles per Hour | Kilometers per Hour . | 1.609 |
| TO CHANGE | TO | MULTIPLY BY |
| Centimeters | Inches | 0.394 |
| Meters. | Feet | 3.280 |
| Meters. | Yards | 1.094 |
| Kilometers | Miles | 0.621 |
| Square Centimeters | Square Inches | 0.155 |
| Square Meters... | Square Feet. . | 10.764 |
| Square Meters. | Square Yards | 1.196 |
| Square Kilometers. | Square Miles. | 0.386 |
| Square Hectometers | Acres ..... | 2.471 |
| Cubic Meters | Cubic Feet | 35.315 |
| Cubic Meters | Cubic Yards | 1.308 |
| Milliliters. | Fluid Ounces | 0.034 |
| Liters..... | Pints......... | 2.113 |
| Liters. | Quarts. | 1.057 |
| 'ers. | Gallons | 0.264 |
| ms. | Ounces | 0.035 |
| . Ograms | Pounds | 2.205 |
| Metric Tons. | Short Tons | 1.102 |
| Newton-Meters | Pounds-Feet | 0.738 |
| Kilopascals | Pounds per Square Inch | 0.145 |
| ${ }^{-1}$ ometers per Liter | Miles per Gallon....... | 2.354 |
| smeters per Hour. | Miles per Hour. . | 0.621 |

PIN: 069797-001


[^0]:    REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS
    You can help improve this manual. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms) or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-LM-LT, Fort Monmouth, New Jersey 07703-5007.

    In either case a reply will be furnished direct to you.

[^1]:    * CONNECTORS J17, J18, and $\mathbf{J 1 9}$ and associated cables are non-repairable at ds.

