TM 11-5805-637-34

TECHNICAL MANUAL

DIRECT SUPPORT AND GENERAL SUPPORT

MAINTENANCE MANUAL

BUFFER, DATA TD-1065/G

(NSN 5805-01-028-8364)

HEADQUARTERS, DEPARTMENT OF THE ARMY

16 APRIL 1981

WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT.

Be careful when working on the 115-volt ac line connections. SERIOUS INJURY or DEATH may result from contact with these connections.

CAUTION

Place POWER switch to OFF before removing or inserting circuit card assemblies.

CAUTION

Do not adjust variable controls on any circuit card assembly.

CAUTION

Many data buffer assemblies are secured with captive-type nuts. Do not attempt to turn nuts unless specifically instructed to do so.

CHANGE

No. 2

DEPARTMENTS OF THE ARMY
THE NAVY, AND THE AIR FORCE
Washington, DC, 1 August 1988

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL BUFFER, DATA TD-1065/G (NSN 5805-01-028-8364) AND TD-1065A/G (NSN 5805-01-182-3937) AND TD-1065B/G (NSN 5805-01-185-4194)

TM 1l-5805-637-34/EE169-JC-INM-010/TD 1065B/G/TO 31S5-2G-272, 16 April 1981, is changed as follows:

1. Title of manual is changed as shown above.

2. The Navy technical manual identification number (TMIN) has been added to this publication.

3. Remove old pages and insert new pages as indicated below. New or changed material is indicated by a vertical bar in the margin of the page. Added or revised illustrations are indicated by a vertical bar adjacent to the identification number.

Remove pages	*Insert pages*
i and ii	i and ii
1-1 and 1-2	1-1 and 1-2
2-5 and 2-6	2-5 and 2-6
2-11 through 2-20	2-11 through 2-20
3-1 through 3-16	3-1 through 3-16
A-1/(A-2 blank)	A-1/(A-2 blank)

4. File this change sheet in the front of the publication for reference purposes.

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To be distributed in accordance with DA Form 12-51 DS/GS requirements for TD-1065/G.

TM 11-5805-637-34
TO 31S5-2G-272
C1

Change
No. 1

DEPARTMENTS OF THE ARMY
AND THE AIR FORCE
Washington, DC, 1 January 1986

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL BUFFER, DATA TD-1065/G (NSN 5805-01-028-8364) TD-1065A/G (NSN 5805-01-182-3937)

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Remove pages	***Insert pages***
i and ii	i and ii
l-1and l-2	l-l and l-2
2-1 through 24	2-l through 24
2-9 through 2-20	2-9 through 2-20
3-11 through 3-16	3-ll through 3-16
A-1	A-l/(A-2 blank)
Figure FO-5	Figure FO-5
Figure FO-8	Figure FO-8
Figure FO-10	Figure FO-10

4. File this change sheet in front of the manual for reference purposes.

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Technical Manual
No. 11-5805-637-34
Technical Manual
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Technical Order
No. 31S5-2G-272

DEPARTMENTS OF THE ARMY
THE NAVY, AND THE AIR FORCE

Washington, DC, 16 April 1981

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL BUFFER, DATA TD-1065/G (NSN 5805-01-028-8364) AND TD-106SA/G (NSN 5805-01-182-3937) AND TD-1065B/G (NSN 5805-01-185-4194)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-ME-PS Fort Monmouth. NJ 07703-5000.

For Air Force, submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 6-5, Section VI, T.O. 00-5-1. Forward directly to prime ALC/MST.

For Navy, mail comments to the Commander, Space and Naval Warfare Systems Command, ATTN: SPAWAR 8122, Washington, DC 20363-5100.

In either case, a reply will be furnished direct to you.

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1 Scope

This manual contains a functional description and direct support and general support maintenance instructions for Buffer, Data TD-1065/G, TD-1065A/G and TD-1065B/G. The Buffer, Data is referred to as data buffer in this manual. Appendix A lists the publications applicable to this equipment,

1-2. Consolidated Index Of Army Publications And Blank Forms

Refer to the latest issue of DA Pam 25-30 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

1-3. Maintenance Forms, Records, and Roports

a. *Reports of Maintenance and Unsatisfactory Equipment.* Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750 as contained in Maintenance Management Update. Air Force personnel will use AFR 66-1 for maintenance reporting and TO-O-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performed utilizing the Maintenance Data Collection Subsystem (MDCS) LAW OPNAVINST 4790.2, Vol 3 and unsatisfactory material/conditions (UR submissions) LAW OPNAVINST 4790.2, Vol 2, chanter 17.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy ROD)) as prescribed in AR 735-1l-2/DLAR 4140.55/ NAVMATINST 4355.73B/AFR400-54/MCO 4430.3H.

c. Discrepancy in Shipment Report (DISREP) (SF361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR-4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR)

If your equipment needs improvement let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-PA-MA-D, Fort Monmouth, New Jersey 07708-5000. We'll send you a reply.

1-5. Administrative Storage

Administrative Storage of Equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS charts as covered in TM 11-5805-637-12 before storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness. Disassembly and repacking of equipment for ship ment or limited storage is covered in TM 11-5805-637-12 and TM 750-244-20.

1-6. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

Section II. DESCRIPTION AND DATA

1-7. Description

Refer to TM 11-5805-637-12 for a description of the data buffer.

1-7.1 Differences Between Models

NOTE

Except where indicated Buffer, Data TD-1065/G information referenced in this manual relates to the Buffer, Data TD-1065A/G and the TD-1065B/G as well.

a. Only the TD-1065A/G containing circuit card assembly channel unit, CCA19A6A, or the TD-1065B/G with circuit card assembly channel unit CCA19A6B can be used in conjunction with central office telephone automatic AN/TCC-39.

NOTE

Except where indicated CCA19A6 information referenced in this manual relates to the CCA19A6A and CCA19A6B as well.

b. Functional characteristics are as follows.

(1) TD-1065/G with CCA19A6 provides full duplex operation for 16KB and 32KB data (4W) or half duplex operation for 16KB data and full duplex operation for 32KB data (2W).

(2) TD-1065A/G with CCA19A6A provides full duplex operation for 32KB data (4W) or half duplex operation for 16KB data (2W).

(3) TD-l065B/G with CCA19A6B provides TD-1065/G operation (Mode A) or TD-1065/G operation (Mode B).

1-8. Tabulated Data

Refer to TM 11-5805-637-12 for tabulated data pertaining to the data buffer.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. OVERALL BLOCK DIAGRAM DISCUSSION

2-1. Introduction

This chapter provides a functional description of the data buffer. It includes an overall block diagram discussion and a functional system discussion with detailed block diagram descriptions of each functional element in the data buffer.

2-2. General
(fig. FO-1)

a. The data buffer is used in conjunction with multiplexer TD-660( )/G. This permits the data buffer to operate with both voice and data signals. The TD-660( )/G may be used in a six-channel or a 12-channel mode of operation. The TD-660( )/G multiplexes and encodes up to six or 12 four-wire voice frequency channels into a single time-division-multiplex pulse-code-modulation (tdm/pcm) channel. This takes place in the TD-660( )/G transmit section. Conversely, the TD-660( )/G receive section demultiplexes and decodes a tdm/pcm channel to provide up to six or 12 four-wire voice frequency channel outputs. The data buffer automatically compensates for either six-channel or 12-channel operation. If the data buffer becomes inoperative, operating the data buffer power ON/OFF circuit breaker to OFF restores relays that route incoming signals around the data buffer. This permits the TD-660( )/G to operate normally with voice and tdm/pcm signals.

b. The data buffer is comprised of four functional sections: transmit, receive, fault locator, and power supply. Both the transmit and receive sections utilize signals provided by the TD-660( )/G. The fault locator and power supply provide maintenance service and power to functional blocks of the data buffer.

2-3. Transmit Section

a. The transmit section receives up to six or 12 channels of diphase data/voice signals. These signals are processed in conjunction with the TD-660( )/G to combine them into a single output channel containing six or 12 channels of the tdm data and pcm signals.

b. Up to six or 12 channels of diphase data/voice signals are applied to the data buffer audio filter. The audio filter routes voice input signals to the TD-660( )/G and routes diphase data to an associated data buffer channel circuit card assembly (CCA). The audio filter also serves to reduce electromagnetic interference radiating from the data buffer. It also reduces undesirable radiation of signals containing data or voice information.

NOTE

Each channel CCA has one transmit section and one receive section. For 12-channel operation, all 12 channel CCAs are used to process data. For six-channel operation, only the odd-numbered channel CCAs are used to process data.

c. Each channel CCA converts diphase data to binary data, adjusts the data rate, and structures the data so that it can be inserted into the multiplexed pcm signal. The channel CCA then applies the data (now in binary format) to the transmit common CCA. The TD-660( )/G converts the voice channels from the audio filter into a single tdm/pcm channel. The TD-660( )/G then applies the pcm channel, along with timing and address lines to the high speed filter. The high speed filter provides filtering for the pcm, timing, and address signals. The high speed filter then applies these signals to the transmit common CCA. The high speed filter also serves to reduce electromagnetic interference radiating from the data buffer. It also reduces undesirable radiation of signals containing voice or data information.

d. The transmit common CCA examines the data from the channel CCAs to determine mode of operation (six or 12 channel). It automatically adjusts to either mode, then inserts the active binary data channels into the empty pcm time slots from the high speed filter. This forms a single combined multiplexed data and pcm channel. The combined channel is applied to another section of the high speed filter. Here it is filtered and applied to the data buffer output along with the address and timing lines.

2-4 Receive Section

a. The TD-660( )/G accepts a multiplexed pcm/data channel and its corresponding timing line. The TD-660( )/G demultiplexes and decodes the pcm/data channel. It applies the voice channels directly to the audio filter. It also applies the multiplexed data, along with timing and address, to the high speed filter.

b. The high speed filter filters and routes the data to the receive common CCA. Here, the data is examined

for mode (six or 12 channel). After adjusting to either mode, the receive common CCA retimes the data and applies it to an associated channel CCA. The channel CCAs convert the data to the source frequency (16 kb/s or 32 kb/s) and from binary form to diphase. The diphase data channels are then applied to the audio filter.

c. The audio filter routes voice channels from the TD-660( )/G directly to associated data buffer outputs. The active data channels from the channel CCAs are impedance matched by the audio filter. The data channels are then routed to associated data buffer outputs,

2-5. Fault Locator Section

The fault locator CCA provides a means of determining the operational status of the data buffer. In the event of a failure, it aids in locating the cause of the fault. A front panel ALARM indicator lamp illuminates when built-in test equipment (BITE) detects a fault condition. A front panel TEST indicator lamp is used in conjunction with BITE features to localize a fault.

2-6. Power Supply Section

The power supply converts a 115 Vac power input to ±10 Vdc to supply power to all data buffer circuits.

2-7. System Timing

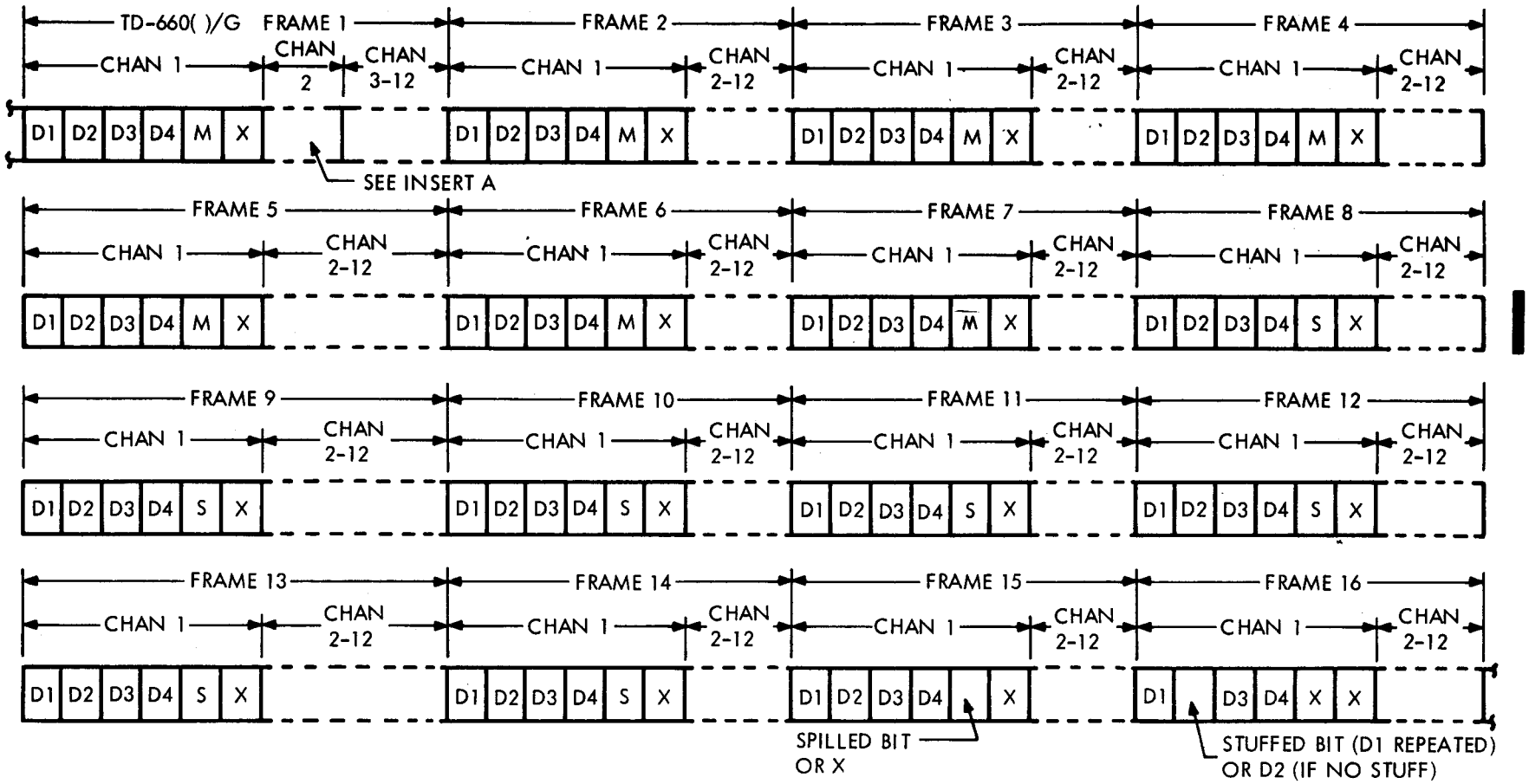
The following paragraphs describe overall system timing and formatting. Both timing generated by the TD-660( )/G and timing generated by the data buffer are discussed.

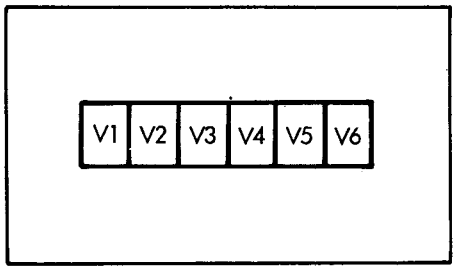
a. TD-660( )/G Frame Format. Figure FO-2 illustrates the pcm frame format of the TD-660( )/G for both six and 12-channel operation. For 12-channel operation, each frame consists of 12 channels. For six-channel operation, each frame consists of six channels. The frame length is the same for either six or 12-channel operation. So that six channels may occupy the same time span as 12 channels, the channels are expanded for six-channel operation. Each channel in the six-channel mode frame occupies the same time span as two channels in the 12-channel mode frame. The channel bit structure remains the same for either the six or 12-channel mode frame. Each channel contains six bits. The six bits comprise a pcm word representative of the voice information contained in that channel. The sixth bit of the last channel in each frame (channel 6 or channel 12) is used as a framing bit. The framing bit signifies the end of the frame.

b. Data Buffer Control Channel Format. Figure 2-1 illustrates the format of receive inputs to, and transmit outputs of, the data buffer during 12-channel operation. Figure 2-2 illustrates the format of receive inputs to, and transmit outputs of, the data buffer during six-channel operation. The data buffer format is exactly the same for either six or 12-channel operation, except for the number of channels per frame. As in the TD-660( )/G frame format, each six-channel mode frame contains six channels, while each 12-channel mode frame contains 12 channels. The format illustrated represents a data buffer control channel, which is comprised of the fifth bit from 16 consecutive TD-660( )/G frames. The control channel contains information that indicates mode (data or voice) and data rate (16 kb/s or 32 kb/s in the data mode) for each of the six or 12 channels. The control channel also contains information that controls data synchronization information in the data mode. Channel 1 is shown containing data in these examples; channel 2 is shown containing pcm. In actual operation, any channel can contain either data or pcm. The following discussion is limited to channels 1 and 2. However, this discussion also applies to channels 3 through 6 for six-channel operation, or 3 through 12 for 12-channel operation.

(1) *Data channel.* A typical data channel is shown in figures 2-1 and 2-2 as channel 1. The first four bits contain data; the fifth bit is used for control channel functions. Bit 5 in frames 1 through 7 is a marker bit that makes up a 7-bit word that indicates rate and mode. A 1110010 pattern indicates a 32 kb/s data rate. A 0001101 pattern indicates a 16 kb/s data rate. Any other pattern indicates the voice mode. Bit 5 in frames 8 through 14 is a signaling bit indicating that either a stuff or a spill operation has been performed. The stuff/spill operation is a method of synchronization that permits the data buffer to operate with asynchronous data rates. During a stuff operation, bit 1 in frame 16 is repeated in the bit 2 position. It is then ignored by the receiving equipment. During a spill operation, a data bit is inserted in the bit 5 position in frame 15. This bit is recovered by the receiving equipment and reinserted into its proper time slot. Either a stuff or spill operation is performed on each data channel. When the incoming data rate is slower than the rate required by the data buffer, more stuff operations are performed than spill operations. Conversely, when the incoming data rate is faster than the rate required by the data buffer, more spill operations are performed than stuff operations.

(2) *PCM channel.* A typical pcm data channel is shown in figures 2-1 and 2-2 as channel 2. All six bits of a pcm channel contain encoded voice information in each TD-660( )/G frame. The data buffer recognizes the voice mode by the absence of either a 1110010 or 0001101 pattern as explained in paragraph 2-b.(1).





INSERT A

NOTES:

1. ONE DATA BUFFER CONTROL CHANNEL CORRESPONDS TO SIXTEEN 12-CHANNEL TD-660( )/G FRAMES.
2. M = MARKER BITS (FRAMES 1-7).
   1110010 PATTERN INDICATES 32 KB/S DATA RATE.
   0001101 PATTERN INDICATES 16 KB/S DATA RATE.
   ANY OTHER PATTERN INDICATES VOICE MODE.
3. S = SPILL/STUFF SIGNALING BITS (FRAMES 8-14).
   S = 1 FOR STUFF; S = 0 FOR SPILL.
4. X = UNUSED BIT.
5. D1-D4 ARE DATA BITS.
6. V1-V6 ARE PCM BITS.
7. CHANNEL 1 IS SHOWN CONTAINING DATA.
   CHANNEL 2 IS SHOWN CONTAINING VOICE.

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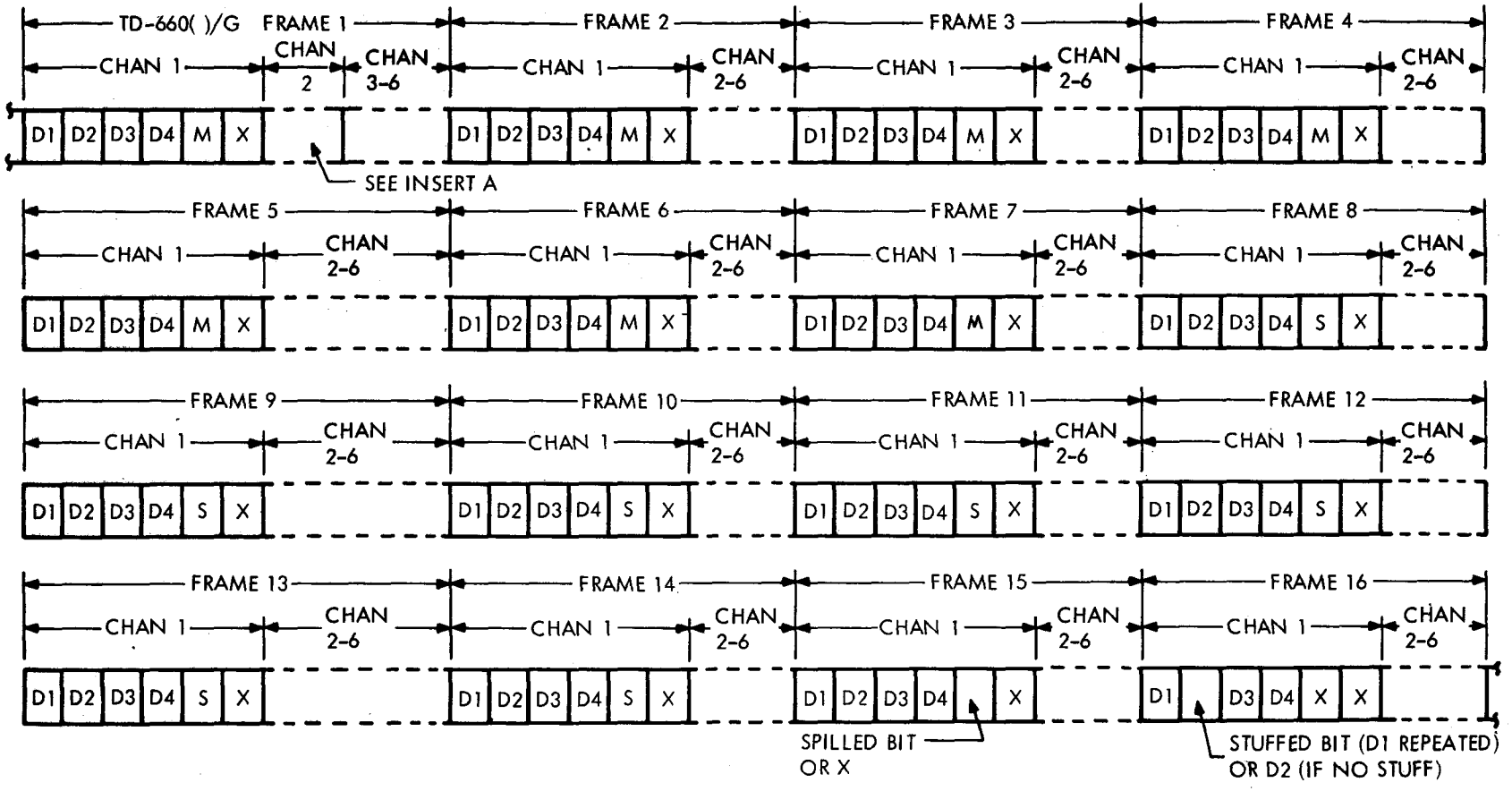
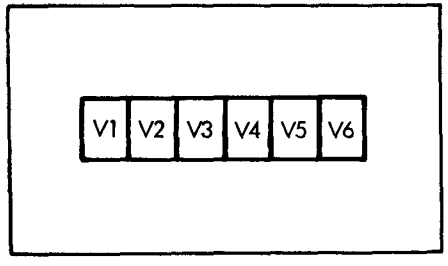
Figure 2-1. Data buffer control channel format, 12-channel operation.





INSERT A

NOTES:

1. ONE DATA BUFFER CONTROL CHANNEL CORRESPONDS TO SIXTEEN 6-CHANNEL TD-660( )G/ FRAMES.
2. M = MARKER BITS (FRAMES 1-7).
   1110010 PATTERN INDICATES 32 KB/S DATA RATE.
   0001101 PATTERN INDICATES 16 KB/S DATA RATE.
   ANY OTHER PATTERN INDICATES VOICE MODE.
3. S = SPILL/STUFF SIGNALING BITS (FRAMES 8-14).
   S = 1 FOR STUFF; S = 0 FOR SPILL.
4. X = UNUSED BIT.
5. D1-D4 ARE DATA BITS.
6. V1-V6 ARE PCM BITS.
7. CHANNEL 1 IS SHOWN CONTAINING DATA.
   CHANNEL 2 IS SHOWN CONTAINING VOICE.

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Figure 2-2. Data buffer control channel format, six-channel operation.

Section II. FUNCTIONAL SYSTEM DISCUSSION

2-8 General

The data buffer is comprised of four different CCAs and three replaceable assemblies as follows:

a. Power Supply 19A1
b. Fault locator CCA 19A3
c. Transmit common CCA 19A4
d. Receive common CCA 19A5
e. Channel CCA19A6, CCA19A6A, or 19A6B
f. High speed filter 19A7
g. Audio filter 19A10

Each CCA and replaceable assembly is described in the following paragraphs.

2-9. Power Supply 19A1 (fig. 2-3)

The power supply converts 115 Vac, 50-400 Hz power to ±10 Vdc. The ±10 Vdc is distributed throughout the data buffer. The power supply receives 115 Vac power from line filter 19FL1 and overvoltage absorbers 19RV1 and 19RV2. The line filter reduces electromagnetic interference entering or leaving the data buffer. The overvoltage absorbers protect the power supply from excessive input voltage transients. The 115 Vac input is applied through POWER ON/OFF circuit breaker CB1 to stepdown transformer T1. The output of transformer T1 is applied to diode bridge CCA 19A1A2. The diode bridge CCA contains two full wave bridge rectifiers. The outputs of the two rectifiers are applied through filter CCA 19A1A1 to reduce ripple.

2-10. Fault Locator CCA 19A3 (fig. FO-3)

a. The fault locator CCA monitors the statue of 22 signals within the data buffer. These signals indicate the operational status of data buffer CCAs and assemblies, and are listed in table 2-1. A fault in any of these signals, except +10V and -10V, enables both an audible alarm and an external remote alarm. A fault condition also causes a front panel ALARM indicator lamp to illuminate. A fault condition in any of these signals can be localized by positioning a front panel rotary switch to each of 10 positions. A front panel TEST indicator lamp illuminates to indicate that the signal associated with the selected switch position is present.

Table 2-1. Signals Monitored by Fault Locator CCA

Mnemonic name	Function	Origin
CUAL 1 through CUAL 12	Channel CCA alarm	Channel CCAs 19A6, 19A6A or 19A6B 1 through 12
TXCOMM	Transmit common	Transmit common CCA 19A4
RXCOMM	Receive common	Receive common CCA 19A5
BAUXAD	Buffered auxiliary address	High speed filter 19A7
BTXPCM	Buffered transmit pcm	High speed filter 19A7
BTXTIM	Buffered transmit timing	High speed filter 19A7
BRXAD	Buffered receive address	High speed filter 19A7
BRXPCM	Buffered receive pcm	High speed filter 19A7
BRXTIM	Buffered receive timing	High speed filter 19A7
+10V	+10Vdc	Power supply 19A1
−10V	−10 Vdc	Power supply 19A1

b. Six signals from high speed filter 19A7 are applied to the buffers and amplifiers. The buffers and amplifiers convert these pulse signals to logic levels that indicate the presence or absence of the signals. The buffers and amplifier outputs are related to their inputs as follows

Input Signal	Output Signal
BAUXAD	TXPRMM (transmit framing monitor)
BTXPCM	TXPCMM (transmit pcm monitor)
BTXTIM	TXTIMM (transmit timing monitor)
BRXAD	RXFRMM (receive framing monitor)
BRXPCM	RXPCMM (receive pcm monitor)
BRXTIM	RXTIMM (receive timing monitor)

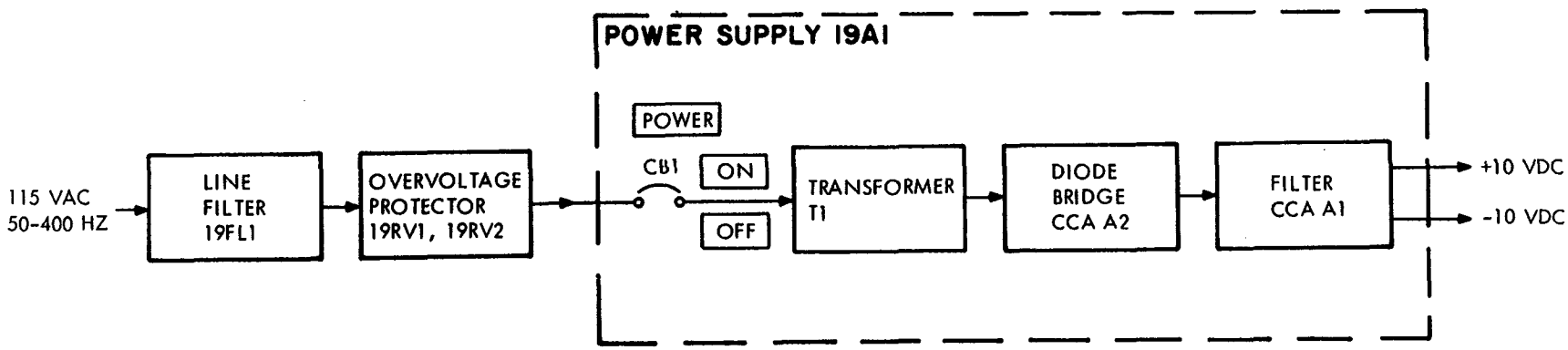


Figure 2-3. Power supply 19A1, functional block diagram.

The outputs of the buffers and amplifiers are combined in the NAND gates to produce a relay control enable signal. This signal is present only when all input signals, including CCMTR (common circuit monitor), are present. Absence of the relay control signal indicates an alarm condition. The relay control enable signal is applied to the l-second delay circuit. When all inputs are present, the l-second delay circuit produces a DLY (delay) signal. Loss of an input causes the DLY signal to be removed after a delay of 1 second.

c. When the DLY signal is present, the relay control enable circuit produces two outputs: RLYDRV (relay drive) and alarm disable. The RLYDRV signal causes alarm relay 19K1 to operate. This extinguishes ALARM indicator lamp 19DS1 and disables the remote alarm signal. The alarm disable signal disables the audible alarm circuit. Loss of DLY results in loss of the RLYDRV and alarm disable signals. Loss of RLYDRV restores the alarm relay, thereby illuminating the ALARM indicator and enabling the remote alarm. Loss of the alarm disable signal enables the audible alarm circuit. A SPKRDR (speaker drive) signal is then applied to loudspeaker 19LS1 to produce an alarm tone. The alarm tone can be silenced by depressing alternate-action BUZZER OFF pushbutton switch 19S2. At any time, the audible alarm can either be activated or silenced by alternately depressing and releasing the BUZZER OFF pushbutton switch. When the data buffer is initially turned on, the unit power-on alarm enable circuit momentarily generates an alarm condition. This occurs when +10V from power supply 19A1 momentarily generates a power-on alarm signal. This is applied to the relay control circuit, and generates an alarm for the duration of the power-on alarm signal.

d. Two signals are applied to the common circuit alarm detector. These are TXCOMM from transmit common CCA 19A4, and RXCOMM from receive common CCA 19A5. When both signals are present, a CCMTR signal enables the NAND gates. Loss of either TXCOMM or RXCOMM removes CCMTR, which also removes the relay control enable signal. This generates an alarm as previously described.

e. The channel alarm detector receives one CUAL (channel alarm) signal from each of 12 channel CCAs 19A6. When all CUAL signals are present, a CCHMTR (channel monitor) signal is applied to the relay control circuit. Loss of any CUAL signal removes CCHMTR and generates an alarm as previously described.

f. The 10-volt monitor circuit receives +10V and -10V from power supply 19A1. This circuit evaluates the amplitude of the ±10 volts, and produces two output signals if the ±10 volt input is above a set lower limit. These signals, +10VMTR (+10 volt monitor) and -10VMTR (-10 volt monitor), are applied to rotary switch 19S1.

g. Ten fault locator monitor signals are applied to the rotary switch. These signals are:

(1) CCHMTR
(2) +10VMTR
(3) -10VMTR
(4) CCMTR
(5) TXFRMM
(6) TXPCMM
(7) TXTIMM
(8) RXFRMM
(9) RXPCMM
(10) RXTIMM

Any one of these signals can be selected by the rotary switch. The selected signal is applied to the lamp driver as signal MTRINP (monitor input). If MTRINP is present, the lamp driver generates FLTLMP (fault lamp) to illuminate TEST indicator lamp 19D2. The absence of the selected signal removes MTRINP and FLTLMP and extinguishes the TEST indicator lamp.

2-11. Transmit Common CCA 19A4

a. General. The transmit common CCA, figure 2-4, is divided into two functional sections, These are (1) the input/select section, and (2) the output/timing section. The input/select section receives six or 12 channels of pcm. It also receives six or 12 channels of multiplexed data. These signals are combined into a single tdm output signal of data and pcm. The combined data/pcm signal is applied to the output/timing section where it is retimed for proper phasing. The output/timing section also generates clocks which control timing functions on each channel CCA 19A6.

(1) The input/select section operates in one of two modes, six channel or 12 channel. The operating mode is determined by the frequency of signal BTXTIM. In the six-channel mode, BTXTIM, along with the incoming data, rate, and occupancy signals, must be restructured. Restructuring serves two purposes. First, it allows the input/select section to deliver a selected timing signal at the 12-channel rate. This is then used to derive the channel CCA interface signals. Also, restructuring is necessary to expand six channels of data into a 12-channel frame length. After restructuring, data is combined with BTXPCM into a single tdm signal. Occupancy (stuff/spill signaling) bits or rate (16 kb/s or 32 kb/s) bits are also inserted into bit 5 of each data channel during the combining process. These bits constitute the data buffer's control channel. See paragraph 2-7b. for an explanation of the control channel format. In the 12-channel mode, data and pcm are similarly combined. However, the signals are not first restructured. The selected timing signal is applied to the output/timing section. The selected and combined pcm and data signal is also applied to the output/timing section. Address signal BAUXAD is retimed and

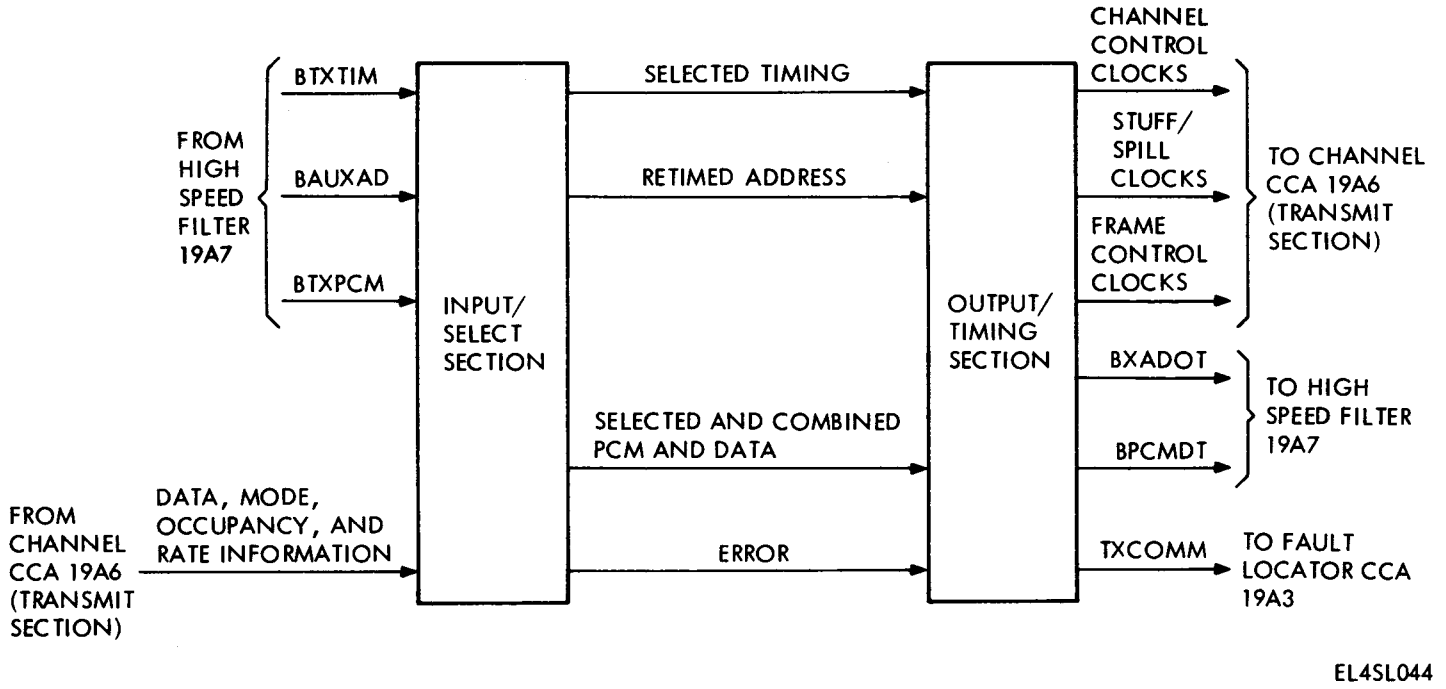


Figure 2-4. Transmit common CCA 19A4, overall functional block diagraJm.

applied to the output/timing section as a retimed address signal. The delay is necessary for proper phasing with both pcm and data signals. The input/select section also produces an error signal to indicate a problem in the six-channel mode timing circuits.

(2) The output/timing section uses the selected timing and retimed framing signals to produce three groups of channel CCA control clocks. These are: the channel control clocks, the stuff/spill clocks, and the frame control clocks. The channel control, clocks control channel timing and elastic store read-in timing in each channel CCA (transmit section). The stuff/spill clocks control stuff and spill operation timing in each channel CCA (transmit section). Finally, the frame control clocks control frame timing, and control channel timing in each channel CCA (transmit section). The output/timing section also retimes the selected and combined pcm and data signal, and the retimed address signal. Retiming is necessary so that the corresponding pcm and address output signals, BPCMOT and BXADOT, are properly phased. BITE circuits in the output/timing section monitor the error signal from the input/select section. If an error is indicated, output signal TXCOMM signals fault locator CCA 19A3 to produce an alarm. The BITE circuits also monitor several timing functions internal to the output/timing section. Errors in these monitored timing functions also produce TXCOMM and generate an alarm.

b. Input/Select Section. The input/select section, figure FO-4, operates in one of two modes: six channel or 12 channel. The data buffer must be able to recognize whether the incoming data is structured in a six-channel format or a 12-channel format. It accomplishes this by counting the number of transmit timing pulses contained in one frame. A 12-channel frame contains 72 pulses, while a six-channel frame contains only 36 pulses. When the format has been determined, the mode is selected by one of two enable signals and data is processed accordingly.

(1) ***Mode Selection.*** Transmit timing signal BTXTIM, from high speed filter 19A7, is applied to the pulse stretcher/shaper. The pukes are stretched and applied to the 6/12-chan mode select circuit as signal PRIDLY (primary delay). The 6/12-chan mode select circuit counts the number of PRIDLY pukes contained in one frame. Information on frame length is obtained from signal BAUXAD. If the 6/12-chan mode select circuit counts 72 PRIDLY pulses per millisecond a 12-chan enable signal is produced. If the 6/12-chan mode select circuit counts 36 PRIDLY pulses per millisecond, a 6-than enable signal is produced. The enable signals are applied to the 6/12-than signal selector to select the proper set of signals for the mode of operation. Both enable signals are also used by the output/timing section to enable one of two phase adjust circuits.

(2) *Transmit Timing.* Input signal BTXTIM is stretched to become signal PRIDLY as previously described. In the 12-channel mode, PRIDLY will be 576 KHz. In this case, PRIDLY is applied directly to the 6/12-chan signal selector. The 12-chan enable signal then causes the 6/12-chan signal selector to route PRIDLY to output TCLK (transmit clock). TCLK is distributed to various input/select and output/timing section circuits. In the six channel mode, PRIDLY will be only 288 KHz. In order to ensure proper timing, TCLK must always be 576 KHz. To achieve this, PRIDLY is applied to the frequency doubler. The frequency of PRIDLY is doubled to 576 KHz and applied to the 6/12-chan signal selector as signal PLL (phase-locked-loop). The 6-chan enable signal then causes the 6/12-chan signal selector to route PLL to output TCLK. The accuracy of the frequency doubler is monitored in the six-channel mode. As long as the frequency doubler is operating properly, a lock signal is applied to the lock-in detector. Signal PRIDLY ia also applied to the lock-in detector. If the frequency doubler is not operating properly, the lock-in detector produces an error signal. The error signal is applied to the BITE circuit in the output/timing section. During the 12-channel mode, the 12-chan enable signal is applied to the lock-in detector. This inhibits the lock-in detector from erroneously producing the error signal during the 12-channel mode. In either mode, signal PRIDLY is routed to the output/timing section. It is used by the phase adjust circuits to provide a pcm delay clock.

(3) *Transmit PCM.* Transmit pcm signal BTXPCM, from high speed filter 19A7, is applied to the pcm retiming circuit. The pcm retiming circuit uses TCLK to retime BTXPCM. This delays BTXPCM so that it may be properly combined with either six or 12-channel data. The output of the pcm retiming circuit, signal pcm, is then applied to the combining circuits and the 6-chan data/voice select circuit. These circuits are used to combine the pcm signal with either 12-channel or six-channel data, respectively.

(4) ***Transmit Data, 12-Channel Mode.*** In the 12-channel mode, the combining circuits are used to combine data bits with occupancy (stuff/spill signaling) and rate (16 kb/s or 32 kb/s) bits. The data channels are then combined with pcm channels into a single 12-channel data/pcm signal. Data bits from each channel CCA 19A6 are applied to the DBUS retiming circuit as signal DBUS (data bus). The DBUS retiming circuit uses signal TCLK to retime the DBUS signal. The retimed data bits are applied to the combining circuits. Signals OBUS (occupancy bus) and RBUS (rate bus) are also applied to the combining circuits. The combining circuits multiplex the data bits with the signaling bits contained in OBUS and RBUS. A bit 5 gate pulse and a marker signal from the output/timing section are applied to the combining circuits to control signal-

ing bit insertion. Of the six bits contained in each TD-660( )/G channel time slot, data bits are inserted into the first four. The fifth bit is a control bit. It receives either rate information from RBUS or stuff/spill signaling information from OBUS. During frame 15, the control bit may be a valid data bit. If so, signal frame 15 causes the valid data bit (spill bit) to be inserted into its proper control channel time slot. The sixth bit is unused and is ignored by the receiving equipment. It is inhibited by a pulse derived from the channel control clocks (signal clocks) from the output/timing section. This inhibit pulse allows the sixth bit of a pcm word to pass through the combining circuits. The combined data and control bit information from each active data channel is then multiplexed with the active pcm channels. The data/pcm combining process is controlled by a delayed mode signal derived from MBUS (mode bus). MBUS contains information on the mode (data or voice) of each channel. MBUS is applied to the data-to-analog switchover delay circuit. As long as the state of MBUS remains constant for a particular channel, the delayed mode signal will also remain constant. If the state of MBUS changes from voice to data for a particular channel, the delayed mode signal will also change immediately. However, if the state of MBUS changes from data to voice for a particular channel, a delay is introduced. This delay is generated using several clocks from the output/timing section. The delay is necessary to compensate for data-to-voice switchover delays introduced by each channel CCA 19A6. The delayed mode signal is then applied to the combining circuits. If the state of the delayed mode signal shows that a channel contains voice information (pcm), the pcm signal is gated into that channel's time slot. If the state of the delayed mode signal shows that a channel contains data, the combined data and control bits are gated into that channel's time slot. The combined 12-chan data/pcm signal is applied to the 6/12-chan signal selector. The 12-chan enable signal then causes the 6/12-chan signal selector to route the 12-chan data/pcm signal to output TDATA (transmit data). Figure FO-5A shows the structure of signal TDATA during a typical 12-channel frame. In the example, channels 4, 8, 9, and 12 are shown as voice channels while the remaining channels are shown as data channels. In actual operation, however, any channel could contain either data or voice. As previously described, the first four bits of each data channel are shown containing data bits. The fifth bit is shown containing control information from either OBUS or MBUS. The sixth bit is unused. All six bits of each voice channel are shown containing pcm. The sixth bit of voice channel 12, however, is used as a framing bit. Signal TDATA is routed to the output/timing section for phase adjustment.

(5) *Transmit Data, Six-Channel Mode.* In the six-channel mode, data must first be restructured before it can be combined with pcm. This is performed in a 6-chan store circuit. The restructured data channels are combined with pcm channels in 6-chan data/voice select circuit. This produces a single six-channel data/pcm signal. Data bits from DBUS are combined with OBUS and RBUS bits in the combining circuits as in 12-channel operation. The combined data and control bits are applied to the 6/12-chan signal selector as signal 12-chan data. Figure FO-5B shows the structure of the 12-chan data signal during a typical six-channel frame. At this point, data is still structured in a 12-channel format. However, in six-channel operation, only the odd-numbered 12-channel time slots are active. The even-numbered time slots are not used. Therefore, odd-numbered 12-channel time slots 1 through 11 become six-channel time slots 1 through 6. In the example, channels 1, 2, 4, and 5 are shown as data channels. Channels 3 and 6 are shown as voice channels. Since the 12-chan data signal has not yet been combined with the active pcm channels, channels 3 and 6 are shown with unused bits. The 6-chan enable signal causes the 6/12-chan signal selector to route the 12-chan data signal to output DO (data out). Signal DO is then applied to 6-chan store circuit. During the 12-channel mode, ground is applied to signal DO instead of the 12-chan data signal. This eliminates noise during the 12-channel mode. DO is read into the 6-chan store circuit using a read-in clock developed by the 6-chan read-in clock generator. The read-in clock is derived from TCLK and a clock from the output/timing section. Frame length information is obtained from signal XMTRST. Data is read out of the 6-chan store circuit by a read-out clock generated by the 6-chan store read-out clock generator. The read-out clock is derived from signal TCLK. A bit 6 inhibit signal from the output/timing section is applied to the 6-chan store circuit. The bit 6 inhibit signal is also applied to the 6-chan read-out clock generator. This signal causes the read-out clock to "pause at the bit 6 time slot. This inhibits the bit 6 time slot from erroneously passing an invalid data bit to the 6-chan data/voice select circuit but allows bit 6 of a pcm word to pass through. The output of the 6-chan store circuit is a 6-chan data signal. Figure FO-5C shows the structure of the 6-chan data signal derived from the typical 12-chan data signal shown in figure FO-5B. The 6-chan storage process has expanded the data bits. This allows each six-channel time slot to occupy the same space as two 12-channel time slots. It also causes the inactive even-numbered 12-channel time slots to be deleted, The 6-chan data signal is combined with the pcm signal in the 6-chan data/voice select circuit, The combining process is governed by the state of the delayed mode signal as previously described for the 12-channel combining process. Figure FO-5D shows the structure of

the six-channel pcm signal which is combined with the active data channels. Since only channels 3 and 6 contain voice, all other channels are shown containing unused bits. Bit 6 of channel 6 contains the framing bit. The combined output of the 6-chan data/voice select circuit is applied to the 6/12 chan signal selector as signal 6-chan data/pcm. The 6-chan enable signal then causes the 6-chan data/pcm signal to be routed to output TDATA. Figure FO-5E shows the structure of signal TDATA derived from the data and pcm signals shown in figures FO-5C and FO-5D. Data and pcm channels have been combined into a single six-channel tdm signal. As in 12-channel operation, TDATA is routed to the output/timing section for phase adjustment.

(6) ***Auxiliary Address.*** Signal BAUXAD is applied to the address retiming circuit. The BAUXAD pulses are delayed to produce two differently phased outputs. One of the phases is applied to the output/timing section as signal delayed address. The other phase is used by the frame synch pulse circuit to generate signal XMTRST (transmit reset). XMTRST is routed to various output/timing section circuits as a synchronization pulse for proper channel and bit timing alignment.

c. Output/Timing Section. The output/timing section, figure FO-6, operates using the timing, data, and address signals obtained from the input/select section. The phases of TDATA and delayed address are adjusted to provide pcm and address outputs to high speed filter 19A7. Also, TCLK and delayed address are used to provide various channel and frame control signals to each channel CCA 19A6. A BITE circuit monitors various signals from the input/select and output timing sections. If any of these signals indicate an error, or are not within tolerance, an alarm is generated.

(1) *PCM/Auxiliury Address Retiming.* Signal PRIDLY from the input/select section is applied to both the 6-chan phase adjust circuit and the 12-chan phase adjust circuit. The 6-chan phase adjust circuit uses PRIDLY to generate a DLYCLK (delay clock) signal which is used to retime six-channel data and address. The 12-chan phase adjust circuit uses PRIDLY to generate a DLYCLK signal which is used to retime 12-channel data and address. During the six-channel mode, the 6-chan enable signal from the input/select section is applied to the 6-chan phase adjust circuit. This causes signal DLYCLK to be gated from the 6-chan phase adjust output. During the 12-channel mode, the 12-chan enable signal is applied to the 12-chan phase adjust circuit. This causes signal DLYCLK to be gated from the 12-chan phase adjust output. The active DLYCLK signal is applied to the pcm and aux address retiming circuit. The pcm and aux address retiming circuit uses DLYCLK to retime signals TDATA and delayed address from the input/select section. The retimed signals BXADOT (buffered transmit address output) and BPCMOT (buffered pcm output) are applied to high speed filter 19A7. Retiming with the adjustable DLYCLK signal is necessary to maintain the required phase relationship between TIM OUT and both XMT PCM OUT and AUX ADRS OUT.

(2) *Channel Control Timing.* Signal TCLK from the input select section is applied to the channel control counter. The channel control counter divides down TCLK to produce several clocks which are applied to the channel control timing circuit. The channel control timing circuit uses the clocks to generate signals TSHCLK (transmit shift clock), TBTCLK (transmit burst clock), TR1 through TR3, and TC1 through TC4. These signals are used by the transmit section of each channel CCA 19A6 for timing and control. Signal TSHCLK is used to generate an elastic store read-out clock in the channel CCAs. TSHCLK is also used as the bit 5 gate pulse which is applied to the input/select section to control the combining process. Signal TBTCLK is used to generate a burst buffer clock in the channel CCAs. Signals TR1 through TR3, and TC1 through TC4 contain encoded information that defines the channel time slots. These are distributed among the channel CCAs in the proper combinations to enable each channel during its particular time slot. The channel control timing circuit also produces TR and TC clocks which are monitored by the BITE circuit.

(3) *Frame Control Timing.* Signal delayed address from the input/select section is applied to the frame control counter. The frame control counter uses de layed address to produce several clocks which are applied to the frame control timing circuit. The frame control timing circuit uses the clocks to generate several frame control timing signals. These are: OCSTRB (occupancy strobe), TRCD (transmit record), CLR (clear), frame 15, and a marker signal. Signal OCSTRB is used to inspect the occupancy of the elastic store in the transmit section of each channel CCA. Signals TRCD and CLR provide start and stop pulses which establish the measurement interval of the voice/data/rate discriminator in the transmit section of each channel CCA. The frame 15 pulse and the marker signal are used by the input/select section to control the combining process.

(4) *Occupancy Control and Bit 6 Inhibit.* The occupancy control timing circuit examines the state of signal OBUS to initiate stuff and spill operations. OBUS contains information on the occupancy level of the transmit elastic store circuit in each channel CCA. A stuff pulse (STF) is generated if the occupancy is below a preset threshold. A spill pulse (SPL) is generated if the occupancy is above a preset threshold. The occupancy control timing circuit generates STF and SPL pulses in their proper time slot utilizing clock signals

from two circuits. These are the channel control counter and the frame control timing circuit. See paragraph 2-7b. for an explanation of control channel format. Several clocks generated by the channel control timing circuit are used by the bit 6 inhibit circuit. This circuit generates a bit 6 inhibit pulse which is used by the input/select section. The input/select section uses the bit 6 inhibit pulse to inhibit the data bit 6 time slot. One of the channel control counter clocks is also routed to the input/select section. This clock is used to generate a 6-chan store read-in clock.

(5) ***BITE Operation.*** The BITE circuit monitors various signals from the transmit common circuits. A 1 kHs signal from the frame control counter is applied to the BITE circuit. A large deviation from a constant rate generates signal TXCOMM. TXCOMM is applied to fault locator 19A3 to generate an alarm. If rotary switch 19S1 is in the COM position, +10V is applied to FAULT LED DSl (via a resistor) as signal CCALEN (common alarm enable). This illuminates the FAULT LED as long as the BITE circuit remains in an alarm status. TR and TC pulses from the channel control timing circuit are also applied to the BITE circuit. A large deviation from a constant rate generates an alarm as previously described. Signals BXADOT and BPCMOT are applied to the BITE circuit. Absence of these pulse signals generates an alarm as previously described. An error signal from the lock-in detector of the input/se. lect section is also applied to the BITE circuit. If this signal is present, an error is indicated. This generates an alarm as previously described.

2-12. Receive Common CCA 19A5

(fig. FO-7)

a. The receive common CCA performs the following functions

(1) Retirees and reshapes incoming signals.

(2) Restructures the incoming signals to compensate for six-channel operation.

(3) Discriminates between a six or 12-channel format,

(4) Divides down the clock and address signals.

(5) Controls Channel CCA 19A6, 19A6A or 19A6B receive section timing functions.

(6) Generates a read-out clock for reading data out of an elastic store circuit in the Channel CCAs 19A6, 19A6, or 19A6B, receive section.

b. The receive common CCA operates in one of two modes 12 channel or six channel. In the 12-channel mode, incoming signals are reshaped and retimed, then routed directly through a 6/12-channel signal selector. In the six-channel mode, incoming signals are also reshaped and retimed. Then they are restructured to fit into a 12-channel frame format. The restructured signals are then routed through the 6/12-channel signal selector. The 6/12-channel signal selector is enabled to select either the 12-channel mode signals or the six-channel mode signals. Enabling is accomplished by a six-channel/12-channel discriminator. The discriminator counts the number of receive clock pulses contained in one frame. A six-channel frame will contain 36 pulses, while a 12-channel frame will ; contain 72. Any count less than 576 will cause the, discriminator to select the six-channel mode, while a" count of 72 selects the 12-channel mode.

c. Receive timing signal BRXTIM from high speed falter 19A7 is applied to the pulse stretcher ***shaper.*** The pulses are stretched and applied to the 6/12-channel signal selector as signal CLKR (receive clock). CLKR is also applied to the frequency doubler. The frequency doubler doubles the frequency of CLKR to produce a double CLKR (receive clock, frequency doubled) signal. The double CLKR signal is aIso ap plied to the 6/12-channel signal selector. If the frequency doubler is not operating correctly, it provides an error signal to the BITE circuit. The rcv pcm retiming circuit uses signal CLKR to retime the incoming BRXPCM signal. The retimed BRXPCM is applied to the 6/12-channel signal selector as signal PCM. The PCM signal is also applied to the rcv pcm delay circuit. The rcv pcm delay circuit compresses the pcm bits to half their original pulse width. The rcv pcm delay circuit also delays the start of each pcm channel in the six-channel mode. This delay allows the six channels to be inserted into the 12-channel frame format. The de lay is accomplished through the application of a burst clock from the six-channel burst clock circuit. The burst clock is developed from the 576 kHz clock timing signal from the 6/12-channel signal selector. The output of the rcv pcm delay circuit, a delayed pcm signal, is applied to the 6/12-channel signal selector. See paragraph 2-7 for an explanation of six and 12-channel timing and frame format. The address stretcher circuit also uses signal CLKR to retime signal BRXAD. The BRXAD pulses are then stretched and applied to the 6/12-channel signal selector as an address signal. The address signal is also applied to the address delay circuit. The address delay circuit uses signal CLKR to delay the address pulses to be synchronous with the delayed pcm signal. The output of the address delay circuit, a delayed address signal, is applied to the 6/12-channel signal selector.

d. The address and CLKR signals are applied to the six-channel/12-channel discriminator. The discriminator counts the number of CLKR pulses in each frame to produce either a 6-chan enable signal or a 12-chan enable signal. Application of the 6-chan enable signal causes the 6/12-channel signal selector to select signals which correspond to the six-channel mode. Application of the 12-chan enable signal causes the 6/12-channel signal selector to select signals which correspond to the 12-channel mode. The six and 12-

channel mode signals and their related 6/12-channel signal selector outputs are shown below.

6-Chan Mode	12-Chan Mode	output
delayed pcm	pcm	RPCM (receive pcm)
delayed address	address	RCVRST (receive reset)
double CLKR	CLKR	576 kHz clock

e. The RPCM output of the 6/12-channel signal selector ia applied to each channel CCA 19A6 (receive section). The 576 kHz clock output of the 6/12-channel signal selector is applied to the channel control counter. The channel control counter divides down the 576 kHz clock to produce several clocks which are used by the elastic store signal decoder. The channel control counter is synchronized to the TD-660( )/G frame format by signal RCVRST. The elastic store signal decoder decodes the channel control counter clocks to produce signals RBTCLK (receive burst clock). RSHCLK (receive shift clock), and STFSPL (stuff/spill). Signals RBTCLK and RSHCLK are used to generate and retime a burst buffer clock in each channel CCA (receive section). Signal STFSPL is used to generate an elastic store read-in clock in each channel CCA (receive section). The RCVRST output of the 6/12-channel signal selector is applied to the channel control timing circuit. The channel control timing circuit uses RCVRST and several clocks from the channel control counter to produce two groups of channel timing signals. These signals, RC1 through RC4 and RR1 through RR3, contain encoded information that defines the channel time slots. These are distributed to the channel CCAs in combinations to enable each channel~uring its particular time slot (see table 2-2).

Table 2-2. Signal Versus Channel Assignments

To Channel CCA No.	Signal						
	RCX	RCY	RCZ	RR	RST	RCD	FHI
1	RC3	RC1	RC1	RR1	RSTA	RCDA	FHIA
2	RC3	RC1	RC1	RR2	RSTA	RCDA	FHIA
3	RC3	RC1	RC1	RR3	RSTA	RCDA	FHIA
4	RC3	RC1	RC2	RR1	RSTA	RCDA	FHIA
5	RC3	RC1	RC2	RR2	RSTA	RCDA	FHIA
6	RC3	RC1	RC2	RR3	RSTA	RCDA	FHIA
7	RC1	RC3	RC3	RR1	RSTB	RCDB	FHIB
8	RC1	RC3	RC3	RR2	RSTB	RCDB	FHIB
9	RC1	RC3	RC3	RR3	RSTB	RCDB	FHIB
10	RC1	RC3	RC4	RR1	RSTB	RCDB	FHIB
11	RC1	RC3	RC4	RR2	RSTB	RCDB	FHIB
12	RC1	RC3	RC4	RR3	RSTB	RCDB	FHIB

f. The frame detection signal decoder produces several signals which are used by the channel CCAs to extract the control channel information from RPCM. The 576 kHz clock signal and several clock signals from the channel control counter are applied to the frame detection signal decoder. These are used to generate the control channel timing signals. Signals RC1 through RC4, and RR1 through RR3 are also applied to the frame detection signal decoder. These supply channel time alot information. The outputs of the frame detection signal decoder are DIG 5 (digit 5), MKR (marker), 576 kHz, RCDA and RCDB (record A and B), and RSTA and RSTB (reset A and B). Signal DIG 5 is used to load control channel information into the control channel register in each channel CCA receive section. MKR is a reference code which is compared to the loaded contents of the control channel register to determine data mode and rate. Signal 576 kHz is a clock used to circulate the bits in the control channel register. RCDA and RCDB are used to record the results of the MKR/control channel register comparison in the channel CCA marker counter. RSTA and RSTB reset the channel CCA control channel comparison counter before the next comparison is made.

g. The elastic store high/low clock generator contains a crystal oscillator which provides three clock outputs. These are FLO (frequency low), and FHIA and FHIB (frequency high A and B). All three are used by the channel CCAs (receive section) to generate a receive elastic store read-out clock.

h. The BITE circuit monitors various signals from the receive common CCA circuits. If any of these are missing or not within tolerance, an alarm is generated. RR and RC pulses from the channel control timing circuit are applied to the BITE circuit. A large deviation from a constant rate generates signal RXCOMM. RXCOMM is applied to fault locator CCA 19A3 to generate an alarm. If rotary switch 19S1 is in the COM position, +10V is applied to FAULT LED DS1 as signal CCALEN. This illuminates the FAULT LED as long as the BITE circuit remains in an alarm status. A 320 Hz signal from the elastic store high/low clock generator is also applied to the BITE circuit. A large deviation from a constant 320 Hz rate generates an alarm as previously described. Signals FHIA and RPCM are applied to the BITE circuit. Absence of

either of these pulse signals generates an alarm as previously described. During the six-channel mode, the BITE circuit also examines a phase-locked loop and error signal from the frequency doubler. If the error signal is present, an alarm is generated as previously described. During the 12-channel mode, the 12-chan enable signal from the six-channel/12-channel discriminator is applied to the BITE circuit. This inhibits the BITE circuit from examining CLKR and the error signal. This prevents an alarm from being erroneously generated while in the 12-channel mode.

2-13. Channel CCA19A6, 19A6A, 19A6B

a. General. The Channel CCA is divided into two functional sections, transmit and receive. The following paragraphs describe the Channel CCA. A switch on the Channel CCA selects either 4W (4 wire) or 2W (2 wire) operation. When the switch is in the 4W position, both transmit and receives process data simultaneously (full duplex operation). When the switch is in the 2W position only one section (transmit or receive) of the Channel CCA processes data at any given time (half duplex operation).

NOTES

On Channel CCA 19A6 (TD-1065/G), when the switch is in the 4W position, full duplex operation is enabled for 16KB and 32KB data. When the switch is in the 2W position, half duplex operation is enabled for 16KB data, full duplex operation is enabled for 32KB data.

On Channel CCA19A6A (TD-1065A/G), when the switch is in the 4W position, full duplex operation is enabled for 32KB data only. When the switch is in the 2W position, half duplex operation is enabled for 16KB data only.

On Channel CCA19A6B (TD-1065B/G),the mode switch selects either CCA19A6 operation (Mode A) or CCA19A6A operation (Mode B).

b. Transmit Section. The transmit section, fig. FO-8, performs data timing recovery, voice/data/rate discrimination, diphase-to-binary conversion data rate equalization, and format structuring for inserting data into a data/scm channel. In addition, the transmit section contains a built-in test equipment (BITE) circuit.

(1) The transmit section receives TXD (transmit data) from audio filter 19A10. This signal is either diphase data or voice. TXD is applied to the input amplifier. The data is at either a 16 kb/s or a 32 kb/s rate. The input amplifier restores and squares these pulses, and applies them to the clock recovery circuit. The clock recovery circuit uses a 2.048160 MHz clock (FHI) from receive common CCA 19A5 to generate a clock synchronous to the incoming data rate. FHI is also used to recover the positive and negative data transitions (number of zero crossings). The zero crossing information is applied to the voice/data/rate discriminator. Signal TRCD and the output of the mode select circuit provide start and stop pulses which establish the measurement interval of the voice/data/rate discriminator. The stop pulses generated by the mode select circuit are derived from signal CLR. The mode select circuit also controls 2 wire/4 wire operation for the channel CCA. Inputs from 2W/4W Switch S1 are applied to the mode select circuit. When the switch is in the 4W position, the stop pulses are generated continuously.

NOTE

Channel cards CCA 19A6 only, when the switch is in the 2W position, operation is dependent upon data rate. On modified channel cards (CCA 19A6A) the switch selects the data rate (16kb/s 2W mode).

A data rate signal from the voice/data/rate discriminator is applied to the mode select circuit. This signal contains information which indicates the data rate (32 kb/s or 16 kb/s). For the 32kb/s data rate, the mode select circuit generates the stop pulses continuously to allow 4 wire operation. For the 16kb/s data rate, only one channel CCA section (transmit or receive) is enabled at any given time. The transmit section can process data only if the rereceive section is not processing data. Under these conditions, Signal S16 (16kb/s data rate) is absent from the receive section, enabling the mode select circuit. Stop pulses are generated continuously. At the same time, signals D16(2W) (16kb/s data, 2 wire mode) and D (data) are generated. Signal D16(2W) inhibits the binary to-diphase converter in the receive section. Signal D causes the relay driver in the receive section to remain in the data mode state. When the receive section is processing data, signal S16 is generated, thereby forcing the mode select circuit to inhibit the voice/data/rate discriminator. This causes the transmit section to stop **processing data.** Signals D16(2W) and D are also removed to allow receive section operation. The voice/data/rate discriminator determines data rate by counting the rate of zero crossings. If the zero crossing rate is lower than that established for 16 or 32 kb/s data, the TXD signal is determined to be voice. If the TXD sigmal is voice, a data inhibit signal is routed to the bus control circuit. The bus control circuit then routes an MBUS signal to transmit common CCA 19A4.

(2) If the discriminator determines that TXD is data, no data inhibit signal is generated. The diphase output of the input amplifier is now converted to binary form in the diphase-to-binary converter. The binary data is then applied to the transmit elastic store circuit. Here, the input data rate is equalized to the average data buffer transmission rate. The signals which clock data into and out of the transmit elastic store circuit are generated by two clock circuits. These are the elastic store read-in clock and the elastic store read-out clock, respectively. The elastic store read-in clock circuit provides a clock signal at the incoming data rate. The elastic store read-out clock circuit derives its clock from three signals. These are TSHCLK, STF, and SPL. The elastic store read-out clock circuit provides a clock signal at the average data buffer transmission rate. The clock signal is modified to permit stuff or spill operation. See paragraph 2-7b. for an explanation of the control channel format. The data output of the transmit elastic store circuit is clocked into the burst buffer. Here, the data is formatted using a clock generated by the burst buffer clock circuit. The burst buffer clock circuit derives its clock from TBTCLK, and two clocks (TR and TC) representative of the channel time slot. The burst buffer clock circuit generates a clock which reads data from the transmit elastic store circuit into the burst buffer at a 32 kHz rate. This clock is derived from signals TR and TC. The data is read out of the burst buffer by a clock which is at the pcm rate. This 576 kHz clock is derived from signal TBTCLK. Of the six possible bite contained in each channel, the data which is read out is contained in the first four. If a spill operation is indicated, bit 5 of frame 15 will also be read out. The data bits are then routed from the burst buffer to the bus control circuit. The bus control circuit then routes a DBUS (data bus) signal to transmit common CCA 19A4.

(3) The occupancy detector compares the clock rate of the elastic store read-in clock to the rate of the elastic store read-out clock. The occupancy detector senses the relative phasing of the two clocks. This tells the occupancy detector whether the occupancy of the transmit elastic store circuit is above or below a preset threshold. The status of the occupancy detector is inspected by signak OCSTRB to produce an occupancy signal. This occupancy signal is routed to the transmit common CCA via the bus control circuit and signal OBUS (see paragraph 2-11b(4). The voice/data/rate discriminator routes data rate information to the bus control circuit. The bus control circuit then transmits this information to transmit common CCA 19A4 via an RBUS signal.

(4) The BITE circuit monitors two signals from the transmit and receive sections of the channel CCA. If one of these signals is missing, or not within tolerance, an alarm is generated. Stuff pulses from the elastic store read-out clock are applied to the stuff detector. The stuff detector measures rate of the stuff pulses. A large deviation from a constant rate produces an error signal. This signal is applied to the BITE circuit which generates signal CUALM (channel alarm monitor). CUALM is applied to fault locator CCA 19A3 to generate an alarm. If the rotary switch is in the CHAN position, +10V is applied to FAULT LED DS1 as signal CUALEN (channel alarm enable). This illuminates the FAULT LED as long as the BITE circuit remains in an alarm statue. An elastic store monitor signal and a valid data signal from the receive section of the channel CCA are also applied to the BITE circuit. The elastic store monitor signal indicates an alarm condition in the receive elastic store circuit. The valid data signal indicates that the data bits being stored in the receive elastic store circuit are valid (not voice). When both the valid data and elastic store monitor signals are present, an alarm is generated by the BITE circuit as previously described. A data inhibit signal from the voice/data/rate discriminator is applied to the BITE circuit during the voice mode. This inhibits the BITE circuit from erroneously generating an alarm.

c. Receive Section. The receive section, fig. FO-9, identifies the frames in the data buffer control channel so that the operating mode, data rate, and location of stuff and spill bits can be determined. In addition, the receive section provides rate equalization and timing smoothing, and converts the binary data into diphase form. Refer to paragraph 2-7b for an explanation of the data buffer control channel format.

NOTE

Several signals are routed to specific channel CCAs from receive common CCA 19A5. RCX, RCY, and RCZ are combinations of RC1 through RC4. RR corresponds to RR1 through RR3. RST and RCD correspond to RSTA and RSTB, and RCDA and RCDB, respectively. FHI corresponds to FHIA and FHIB. Refer to table 2-2 for channel number assignments for these signals.

(1) The channel slot gate receives RPCM from receive common CCA 19A5. This signal is either data or pcm, and consists of six-bit words. The channel slot gate passes the four data bits and the control channel bit to the control channel register. Bits 1 through 4 are the data bits; bit 5 is the control channel bit. The control channel bit for the particular channel is contained in every frame of RPCM. The control channel register performs two functions.

(a) First, it stores the control channel bit con-

tained in frames 1 through 7 of the data buffer control channel for comparison to a marker reference. These seven bits make up a marker word that represents received data rate and mode. A 1110010 word represents 32 kb/s; a 0001101 word represents 16 kb/s. The presence of any other word implies the voice mode.

(b) Second, the control channel register stores the control channel bit contained in frames 8 through 14. These seven bitsa make up a word indicating that a stuff or a spill operation has been performed. A 0000000 word indicates a spill operation; a 1111111 word indicates a stuff operation.

(2) The control channel bits are read into the control channel register by a timing pulse. This timing pulse is derived by gating DIG 5 with a channel gating signal from the burst buffer block. DIG 5 occurs at the fifth bit of each RPCM word. After a bit is read into the control channel register, it is recirculated by a burst of seven pulses of a gated 576 kHz signal. This signal is derived from 576 kHz gated with signal RCX and occurs once every frame. It takes a total of seven frames to fill the control channel register with seven control bits. By recirculating the bits, none is lost from the register until the following timing pulse enters another control bit into the register. At the same time that the bits are recirculated, they are applied to the control bit comparison counter. Here, they are compared with signal MKR.

(3) Signal RCY is applied to the frame counter which counts the number of TD-660( )/G frames. When the frame counter reaches the count of seven, a marker enable signal is produced. This is applied to the frame counter enable circuit. The frame counter enable circuit then produces signal RINHIB (receive inhibit) which causes the frame counter to stall at frame seven. The marker enable signal is also applied to the control bit comparison counter. This causes the control bit comparison counter to serially compare the output of the control channel register with signal MKR. Each bit compared causes the control bit comparison counter to count up one step. Conversely, each non-comparison inhibits the control bit comparison counter. Each bit of a 32 kb/s marker word will make a positive comparison with signal MKR. This increments the control bit comparison counter. Each bit of a 16 kb/s marker word will make a non-comparison with signal MKR. For the marker to be recognized as representing a 32 kb/s data rate, seven comparisons must be made. For the marker word to be recognized a 16 kb/s data rate, seven non-comparisons must be made. After all seven bits have been compared, the total counts are present as a count signal. The counter decode logic circuit examines the total counts present on the count signal. Seven counts cause the counter decode logic circuit to produce signal 32 kb/s decode. Zero counts cause the counter decode logic circuit to produce signal 16 kb/s decode. More than zero but less than seven counts will cause neither of the decode signals to be produced. Signal RCD (record) then clocks the two decode signals into the marker counter. The marker counter contains one counter section for each of the two decode signals. When signal 16 kb/s decode is present, a 16 kb/s marker counter is incremented. When signal 32 kb/s decode is present, a 32 kb/s marker counter is incremented. Neither marker counter isa incremented when both decode signals are absent. A count of one on either marker counter produces an enable signal which is applied to the frame counter enable circuit. This causes signal RINHIB to be removed and allows the frame counter to begin counting again This removes the marker enable signal from the con trol bit comparison counter and frame counter enable circuits. The control bit comparison counter is reset by signal RST (reset).

(4) As the frame counter counts frames 8 through 14, the control channel register is filled with control bits from those frames. The control bits are applied to the control bit comparison counter as they are recirculated. Here they are compared to see if they contain either seven ones or seven zeros. The results of these comparisons are applied to the stuff/spill code counter via the counter decode logic circuit. The counter decode logic circuit produces a 16 kb/s decode signal or a 32 kb/s decode signal as previously described. During frame 14, a stuff/spill enable signal is produced by the frame counter. This signal is applied to the stuff/pill code counter. The stuff/spill enable signal allows the RCD pulse to record the statue of the 16 or 32 kb/s decode signals in the stuff/spill code counter. The stuff/spill code counter is then incremented by the stuff/spill enable signal as long as either decode signal is present. The absence of the decode signals will cause the stuff/spill code counter to remain at the count of zero.

(5) When the frame counter reaches count 16, it resets itself and begins counting up from frame 1. The control bit comparison counter is reset by signal RST. However, the marker counter and stuff/spill code counter are not reset and remain at their previous count. As the frame counter counts up from frames 1 through 7 again, comparisons are made as previously described. If seven comparisons are again made, the appropriate marker counter section (16 kb/s or 32 kb/s) will be incremented one more count. Similarly, when frame 14 is reached, the stuff/spill code counter is incremented. When the marker counter reaches the count of three, a corresponding output signal is produced. This signal (16 kb/s rate or 32 kb/s rate) is applied to the data/rate detector. When the

stuff/spill code counter reaches the count of three, an enable signal is applied to the data/rate detector. The data/rate detector then produces either signal S16 (16 kb/s data rate) or S32 (32 kb/s data rate). If the marker counter and stuff/spill code counter never reach the count of three, neither S16 or S32 is prduced. This indicates the voice mode. After either data rate has been detected, the counter decode logic circuit's method of decoding is modified. Signals S16 and S32 are applied to the counter decode logic circuit. Presence of S16 or S32 causes the counter decode logic circuit to examine the 16 kb/s and 32 kb/s count signals for a count total of six instead of seven. From here on, only six out of seven control bits are required to match the MKR bits. This keeps the data buffer from erroneously slipping back into the voice mode if noise occurs in the lines. Signals S16 and S32 are also applied to the data detector. Presence of either signal causes the relay driver to be enabled. The relay driver produces signal RLY (relay) which operates a relay in audio filter 19A10. This causes signals RXDA, RXDB, and RXDS (receive data A, B and shield common) to be applied through a transformer to the data buffer output. The absence of S16 and S32 disables the relay driver and removes signal RLY. This restores the relay in audio filter which applies the audio signal from the TD-660( )/G to the data buffer output. The relay driver can also be enabled by signal D from the channel CCA (transmit section). This occurs while the transmit section is processing 16 kb/s data.

(6) The stuff/spill detector decodes the stuff/spill signal from the control bit comparison counter. This allows it to determine whether a stuff or a spill operation has been performed on the incoming data. A majority of the seven stuff/spill pulses (at least four) is all that the stuff/spill detector requires to determine the stuff or spill operation. The majority event (stuff or spill) is recorded in the stuff/spill detector during frame 14. The stuff/spill detector is enabled during frame 14 by the stuff/spill enable signal. The output of the stuff/spill detector is applied to the read-in clock circuit. The read-in clock circuit then adds or deletes the appropriate clock pulses from the read-in clock. This prevents the stuff bits from being read into the receive elastic store circuit. It also allows the spill bits to read into the receive elastic store circuit.

(7) Rate equalization and timing smoothing are performed by a burst buffer and receive elastic store circuit. Data (RPCM) from the associated channel is applied to the buffer retime circuit. The data is retimed and read into the burst buffer by a retime clock. The retime clock, a 576 kHz signal gated to the channel's time slot, is produced by the burst buffer clock circuit. The burst buffer clock circuit derives the retime clock from signal RBTCLK. Data is readout of the burst buffer by the burst clock from the burst buffer clock circuit. The burst clock, a 32 kHz clock gated to the channel's time slot, is derived from signals RR and RCZ. In addition, signal RSHCLK is gated with the spill signal during frame 15. This allows the spill bit to be read out of the burst buffer. The data from the burst buffer is applied to the receive elastic store circuit. Data is read into the receive elastic store circuit by the read-in clock from the read-in clock circuit. The read-in clock circuit derives the read-in clock from the 32 kHz RR signal. Spill bits are read into the receive elastic store circuit by means of an extra clock pulse inserted into the read-in clock signal. This occurs during frame 15(F 15) as instructed by the stuff/spill detector. The read-in clock circuit obtains the extra clock pulse from signal STFSPL gated with the channel gating signal. If the stuff/spill signal indicates a stuff operation, a read-in clock pulse is deleted during frame 16(F16). The read-in clock circuit derives the timing for deleting the clock pulse from signal STFSPL and the channel gating signal. The deletion of the particular clock pulse inhibits the stuff bit from being read into the receive elastic store circuit.

(8) The data bits are read out of the receive elastic store circuit by the read-out index signal. The read-out index signal is controlled by the occupancy monitor circuit. The occupancy monitor circuit compares the phase of the read-in clock to the read-out clock to control the read-out index signal. The read-out clock is produced by two circuits: the read-out clock select circuit and the frequency divider. The read-out clock select circuit derives its output signal from the FLO and FHI clocks from receive common CCA 19A5. Clocks FLO and FHI are marginally offset. FLO is lower than the data source rate's range of variation. FHI is higher than the data source rate's range of variation. If the occupancy level of the receive elastic store circuit goes below 50 percent, the FLO clock is selected. If the occupancy level goes above 50 percent, the FHI clock is selected. Clock selection is controlled by the clock select signal from the occupancy monitor. The selected clock signal is applied, to the frequency divider as signal RCLK (read-out clock). The frequency divider divides RCLK by 64 to produce the read-out clock. Since the receive elastic store occupancy changes as a result of stuff and spill bits, the occupancy monitor can sense the stuff and spill operations. The occupancy monitor causes the read-out index signal to index the receive elastic store's register either up or down to control the data output. If a spill bit is detected, the receive elastic stores register is indexed up once. If a stuff bit is detected, the receive elastic store's register is indexed down once. In this manner, the occupancy level of the receive elastic store circuits is maintained at 50 percent. The store control enable circuit enables the read-out index signal only during the data mode. During the voice mode, it inhibits the read-out index signal. This

keeps invalid data from being read out of the receive elastic store circuit. Signal RINHIB is applied to the store control enable circuit during the choice mode. This causes signal RMON (receive monitor) to be removed from the elastic store read-out control circuit. Removal of RMON disables the read-out index signal. During the data mode RINHIB is not present, and RMON is produced. This enables the read-out index signal. The occupancy of the elastic store circuit is also monitored for BITE puposes. Depletion or overflow of the receive elastic store is sensed by the occupancy monitor. The occupancy monitor then produces an elastic store monitor signal. The elastic store monitor signal is routed to the BITE circuit in the channel CCA (transmit section).

(9) The smooth data from the receive elastic store circuit is applied into the binary-to-diphase converter, It is clocked into the converter by the retime clock from the occupancy monitor circuit. The data is converted from binary to diphase format and clocked out. The signal used to clock data out of the binary-to-diphase converter is either at a 16 kb/s or 32 kb/s rate. Signals S16 and S32 are applied to the output clock select circuit. The active signal selects a clock developed by the read-out clock circuit which is correct for the data rate being used. The selected output clock is applied to the binary-to-diphase converter. The binary-to-diphase converter can be disabled by a signal from the data detector. During the voice mode, the disable signal is generated. This prevents the binary-to-diphase converter from transmitting invalid data. The binary-to-diphase converter is also disabled by signal D16(2W) from the channel CCA (transmit section). This occurs in the 2 wire mode while the transmit section is processing 16 kb/s data. As long as the binary-to-diphase converter is not disabled, the data is clocked out to the line driver. The line driver adjusts the logic level of the data and applies it to the audio filter as signals RXDA, RXDB, and RXDS.

(10) Two signals from the channel CCA (receive section) circuits are applied to the BITE circuit in the channel CCA (transmit section). These are: a valid data signal, and an elastic store monitor signal. The valid data signal is produced by the data detector during the data mode. It enables the BITE circuit. During the voice mode, the valid data signal is removed and the BITE circuit is disabled. The elastic store monitor signal is produced by the occupancy monitor as previously described. The presence of this signal generates an alarm in the BITE circuit.

2-14. High Speed Filter 19A7 (fig. 2-5)

a. General: This high speed filter filters and distributes all high speed, wide band digital signal inputs and outputs of the data buffer. It also serves to convert input pcm signal levels of 0 to -2V to logic levels of 0 to +10V. These logic levels are compatible with the complementary metallic oxide semiconductor (CMOS) circuits used in the data buffer. The high speed filter also converts outgoing CMOS logic levels to standard pcm levels. The high speed filter contains two filters

(1) PCM/auxiliary address filter 19A7A1

(2) Receive clock/timing filter 19A7A2

b. PCM/Auxiliary Address Filter 19A7A1. The pcm/auxiliary address filter controls, filters, and distributes transmit pcm and auxiliary address signals. These signals are received from the TD-660( )/G, and are routed as data buffer outputs.

(1) When power is removed from the data buffer, +10V is removed from relay CCAs 19A7A1A2 and 19A7A1A4. The relays in these CCAs are restored and route XMT PCM IN from the TD-660( )/G directly to the data buffer output as XMT PCM OUT. The relays also route AUX ADRS IN from the TD-660( )/G directly to the data buffer output as AUX ADRS OUT. Thus, when data buffer power is removed, these signals bypass the data buffer and permit normal operation of the TD-660( )/G. When power is applied, -10V operates the relays. XMT PCM IN is now connected to filter 19A7A1FL1, and XMT PCM OUT is connected to filter 19A7A1FL2. Similarly, AUX ADRS IN is connected to filter 19A7A1FL3, and AUX ADRS OUT is connected to filter 19A7A1FL4.

(2) XMT PCM IN and AUX ADRS IN signals are amplified in pcm/aux address CCAs 19A7A1A1 and 19A7A1A3, respectively. The output of these amplifiers are applied to transmit common CCA 19A4 as BTXPCM and BAUXAD, respectively.

(3) The remaining signals distributed and filtered by the pcm/aux address filter are processed in a similar manner. These signals are routed from transmit common CCA 19A4 to the data buffer outputs as follows:

Filter Input	Data Buffer Output
BPCMOT	XMT PCM OUT
BXADOT	AUX ADRS OUT

(4) BTXPCM and BAUXAD are also routed to fault locator CCA 19A3. The fault locator monitors these signals and generates an alarm if the flow of pulses is interrupted.

c. Receive Clock/Timing Filter 19A7A2. The receive clock/timing filter filters and distributes receive pcm, receive auxiliary address, 12 channel timing, and receive auxiliary clock signals.

(1) The TD-660( )/G routes RCV PCM FR AUX through an amplifier in auxiliary pcm filter CCA 19A7A2A1, and filter 19A7A2FL1. This signal is

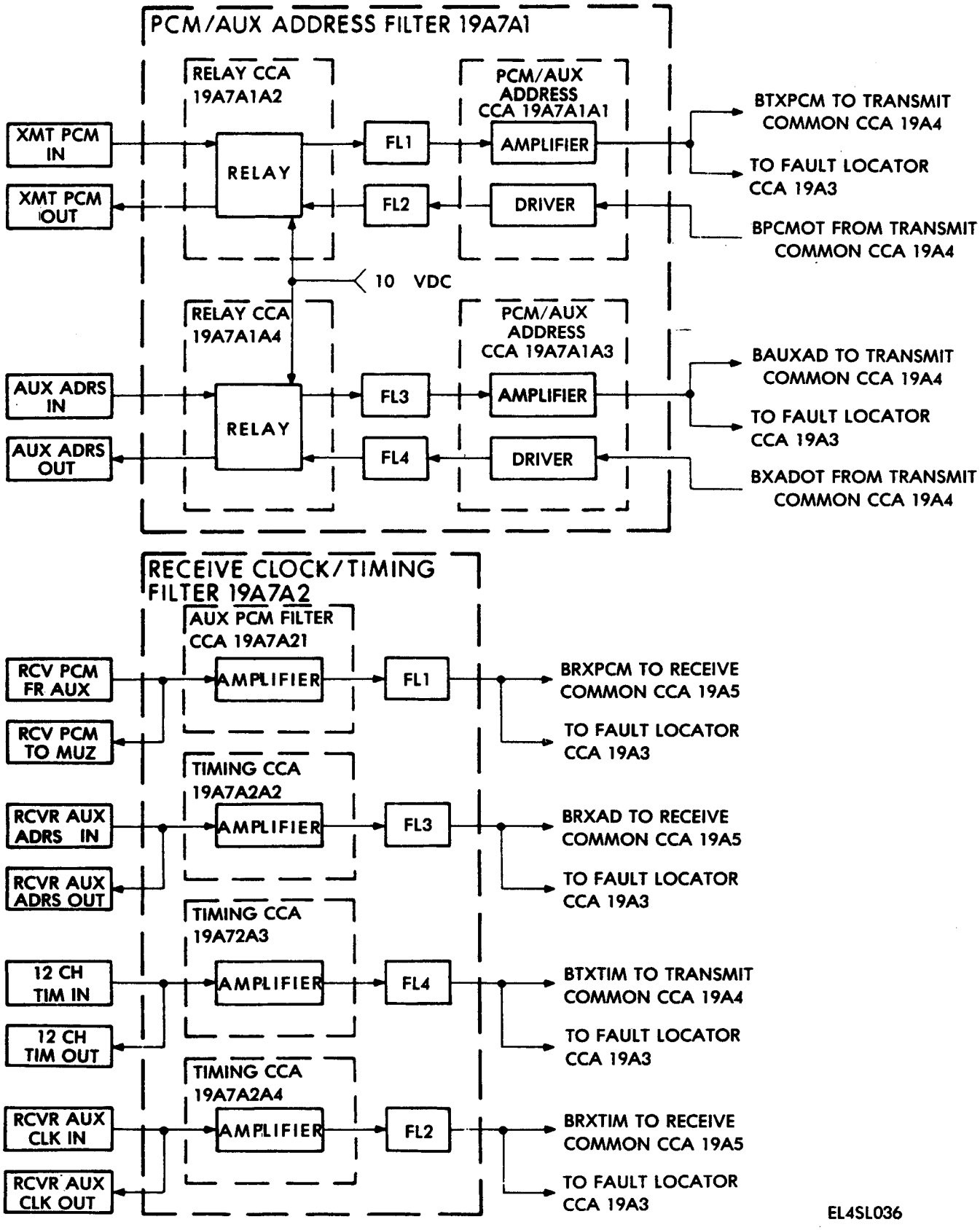


Figure 2-5. High speed filter 19A7. functional block diagram

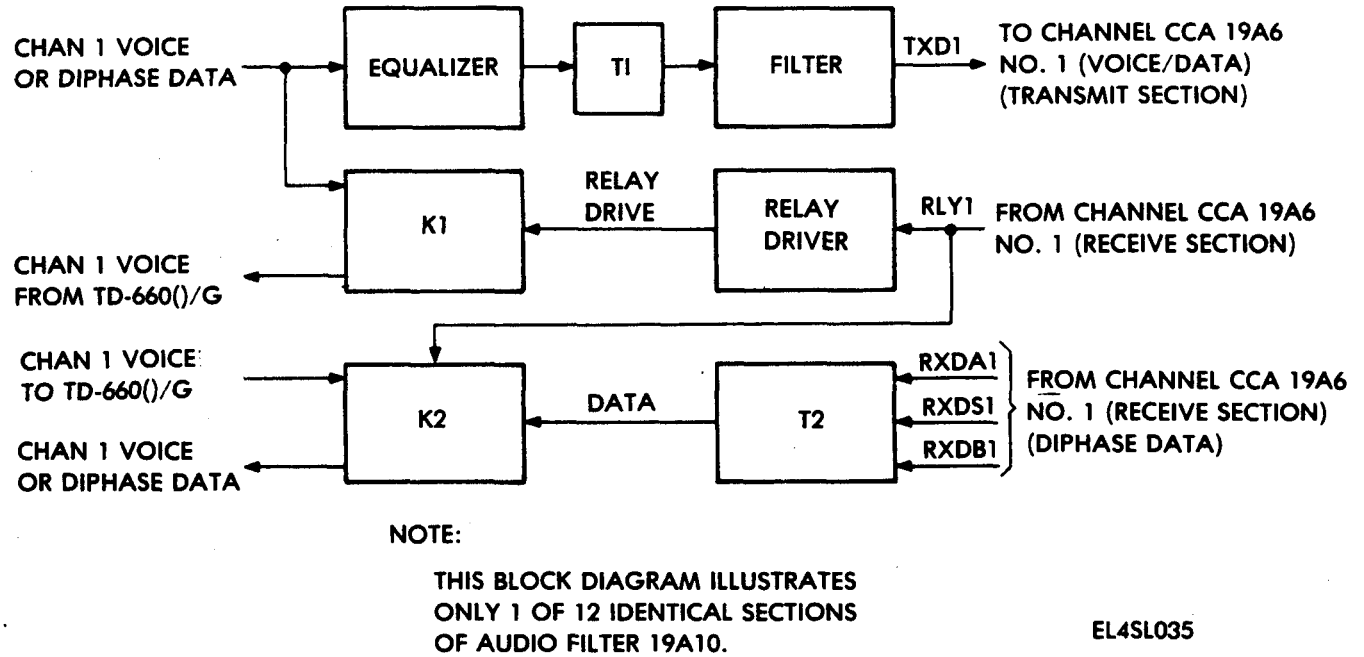


Figure 2-6. Audio filter 19A10, functional block diagram.

applied to receive common CCA 19A5 as BRXPCM. RCV PCM TO AUX is routed from the KG-27 when secure operation is used.

(2) The remaining signals distributed and filtered by the receive clock/timing filter are processed in the same manner as previously described. These signals are routed as follows:

TD-660( )/G Input	Filter Output signal	Routed To
RCV AUX ADRS IN	BRXAD	Receive common CCA 19A5
12 CH TlM lN	BTXTIM	Transmit common CCA 19A4
RCVR AUX CLK IN	BRXTIM	Receive common CCA 19A5

All filter output signals are also routed to fault locator CCA 19A3. The fault locator monitors these signals and generates an alarm if the flow of pulses is interrupted.

2-15. Audio Filter 19A1O (fig. 2-6)

a. The audio filter distributes all low speed, narrow band audio signal inputs and outputs of the data buffer. It also serves to filter data buffer inputs. The audio filter is comprised of 12 identical sections. One section is associated with the transmit and receive function of each of 12 data buffer channels. Each section contains two transformers, two relays, a relay driver, an equalizer, and a filter. The following paragraphs describe the section associated with channel 1.

b. Channel 1 voice or diphase data is applied through an equalizer. The equalizer provides frequency compensation for losses introduced by data buffer input cables. The equalizer output is routed through transformer T1 and a filter as TXDl (transmit data channel 1). TXD1 is routed to the transmit section of channel CCA 19A6 for channel 1.

c. If the receive section of the channel 1 detects incoming voice, it removes a RLY1 (relay channel 1) signal from the relay driver. The relay driver restores relay K1, and the absence of RLY1 restores relay K2. This also occurs if power is removed from the data buffer. Under these conditions, the channel 1 voice input is routed directly to the TD-660( )/G transmit channel by K1. At the same time, the channel 1 voice input from the TD-660( )/G receive channel is routed directly to the data buffer channel 1 voice or diphase data output. Thus, the data buffer is bypassed.

d. If the receive section of the channel CCA detects incoming data, RLY1 is generated and relays K1 and K2 operate. Relay K1 then terminates the channel 1 voice or diphase data input with approximately 650 ohms. Relay K2 connects the data buffer channel 1 voice or diphase data output to the receive section of the channel CCA. This routes RXDA1, RXDB1, and RXDS1 (receive data A, B, and shielded common, channel 1) through transformer T2 and relay K2 to the data buffer output.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL

3-1. Scope

This chapter includes instructions for troubleshooting, testing, and maintaining the data buffer and power supply assembly 19A1 at the direct support maintenance level. It also includes a power supply schematic diagram and power supply wiring diagram to aid in troubleshooting the power supply. The data buffer overall schematic diagram is also provided to aid in troubleshooting the front panel components and associated wiring. All cable harnesses and associated connectors outside of the power supply and front panel components are repaired at depot level.

3-2. Voltage and Resistance Measurements

Voltage and resistance measurements are limited to continuity and resistance measurements in the power supply assembly and front panel component associated wiring. Continuity and resistance measurements within the power supply assembly are performed utilizing the power supply schematic diagram (fig. FO-11), and the power supply wiring diagram (fig. FO-12). With the power supply assembly removed from the data buffer, continuity and resistance measurements may be safely preformed directly on the two power supply CCAs. Continuity measurements on the front panel components and associated wiring are performed utilizing the data buffer overall schematic diagram (fig. FO-13).

Section II. TOOLS AND EQUIPMENT

3-3. Tools and Equipment Required

All required tools and equipment are listed in the Maintenance Allocation Chart (MAC) contained in TM 11-5805-637-12.

3-4. Coaxial and Triaxial Cable Termination Fabrication

All unused coaxial and triaxial cable connectors on the data buffer must be terminated in 91 ohms. Fabricate these terminations as follows:

a. Coaxial Cable Termination. Solder a 91 ohm, ¼ watt, type RLR resistor across the terminals of a UG/U-88 BNC connector.

b. Triaxial Cable Termination. Solder a 91 ohm, ¼ watt, type RLR resistor between the inner pin and the outer shield of a Trompeter part No. PL-76 (or equivalent) triaxial cable connector.

Section III. TROUBLESHOOTING

Troubleshooting may be performed while the equipment is operating as part of a system or, if necessary, after the equipment has been removed from service. When trouble occurs, make as many observations and checks as possible to determine if the local equipment is at fault or if the trouble exists elsewhere in the system.

3-5. Use of Troubleshooting Charts

The direct support troubleshooting chart for the data buffer is given in table 3-1. It includes symptoms and probable causes that may persist after corrective actions such as obvious CCA replacement, assembly replacement, and lamp replacement have been tried at the organizational category. The direct support troubleshooting chart for power supply assembly 19A1 is given in table 3-2. The power supply, after being repaired, should then be tested in a test bed data buffer to check for proper operation. If the TEST indicator lamp is illuminated for the −10 and +10V positions on the test bed data buffer, and data buffer operation appears normal, the repaired power supply may be returned to stock.

NOTE

If the remedy column indicates that a panel-mounted component is faulty, check associated wiring and continuity through component prior to removing component.

3-6. Continuity Checks

If trouble is not corrected by the procedures given in table 3-1 or 3-2, the wiring continuity in the power supply should be checked. Refer to the power supply assembly schematic diagram, fig. FO-11, and the power supply wiring diagram, fig. FO-12. The chassis wiring or CCA connector assembly may also be at fault. Return to depot for maintenance.

NOTE

If table 3-1 calls for a check of relay 19K1, the relay may be checked in the following manner. With power removed from the data buffer, there should be continuity between pins B and C of REMOTE ALARM connector 19J4. Pin 2 of ALARM indicator socket 19XDS1 should also have continuity to ground. With power applied to the data buffer, there should be continuity between pins A and B of REMOTE ALARM connector 19J4. Pin 2 of ALARM indicator socket 19XDS1 should not be connected to ground. If the above conditions do not check out, the relay or associated wiring is at fault. Always check continuity of associated wiring before replacing relay.

Table 3-1. Data Buffer Troubleshooting Chart

Trouble Symptom	Possible Cause	Remedy
1. TEST indicator lamp is extinguished for all front panel rotary switch positions even though unit appears operational.	a. Defective TEST indicator lamp socket 19XDS2 (fig. 3-5). b. Defective rotary switch 19S1 (fig. 3-5).	a. Check socket and replace if defective (para 3-10*g*). b. Check rotary switch and replace if defective (para 3-10*h*).
2. TEST indicator lamp is extinguished for one or more, but not all front panel rotary switch positions, even though unit appears operational.	a. Defective rotary switch 19S1 (fig. 3-5).	a. Check rotary switch and replace if defective (para 3-10*h*).
3. ALARM indicator does not illuminate although one or more positions on the front panel rotary switch show an extinguished TEST indicator lamp.	a. Defective alarm relay 19K1 (fig. 3-2). b. Defective ALARM indicator socket 19XDS1 (fig. 3-5). c. Defective rotary switch (fig. 3-5).	a. Check relay and replace if defective (para 3-10*d*). b. Check socket and replace if defective (para 3-10*f*). c. Check rotary switch and replace if defective (para 3-10*h*).
4. ALARM indicator remains illuminated although unit appears operational. (TEST indicator lamp is illuminated for all front panel rotary switch positions.)	a. Defective alarm relay 19K1 (fig. 3-2). b. Defective ALARM indicator socket 19XDS1 (fig. 3-5).	a. Check relay and replace if defective (para 3-10*d*). b. Check socket and replace if defective (para 3-10*f*).
5. Audible alarm does not activate when ALARM indicator is illuminated and/or cannot be activated by pushing BUZZER OFF switch.	a. Defective loudspeaker 19LS1 (fig. 3-5).	a. Check loudspeaker and replace if defective (para 3-10*i*).
6. Audible alarm cannot be disabled by BUZZER OFF switch.	a. Defective BUZZER OFF switch 19S2 (fig. 3-5).	a. Check BUZZER OFF switch and replace if defective (para 3-10*e*).
7. +10V and −10V positions on the front panel rotary switch show an extinguished TEST indicator lamp, even though unit appears operational.	a. Defective TEST indicator lamp socket 19XDS2 (fig. 3-5). b. Defective rotary switch 19S1 (fig. 3-5).	a. Check socket and replace if defective (para 3-10*g*). b. Check rotary switch and replace if defective (para 3-10*h*).
8. During an alarm condition, all rotary switch positions show an illuminated TEST indicator lamp.	a. Defective rotary switch 19S1 (fig. 3-5).	a. Check rotary switch and replace if defective (para 3-10*h*).
9. POWER ON indicator does not illuminate when POWER ON/OFF switch is set to ON, even though power supply and CCAs have been changed.	a. Defective ac line filter 19FL1 (fig. 3-2). b. Chassis or CCA connector wiring problems.	a. Check ac line filter and replace if defective (para 3-10*b*). b. Return unit to depot.
10. Remote alarm does not operate when unit is in an alarm condition, even though audible alarm and ALARM indicator are operative.	a. Defective REMOTE ALARM connector (fig. 3-1). b. Defective alarm relay 19K1 (fig. 3-2).	a. Check connector and replace if defective (para 3-10*j*). b. Check relay and replace if defective (para 3-10*d*).

Table 3-2. Power Supply Troubleshooting Chart

Trouble Symptom	Possible Cause	Remedy
1. No +10 or −10V.	a. Defective transformer 19A1T1 (fig. 3-6).	a. Remove diode bridge CCA (para 3-10*l*) and check continuity through transformer (primary = 10-15Ω, secondary = 1-3Ω). Replace if defective (para 3-10*n*).
	b. Defective circuit breaker 19A1CB1 (fig. 3-6 and 3-7).	b. Check continuity through circuit breaker. Replace if defective (para 3-10*o*).
	c. Defective diode(s) on diode bridge CCA 19A1A2 (fig. 3-6).	c. Remove diode bridge CCA (para 3-10*l*) and check forward and reverse resistance through each diode (forward = 5-15Ω, reverse ≥ 1000Ω). Replace any defective diode found.
	d. Defective capacitor(s) or resistor(s) on filter CCA 19A1A1 (fig. 3-6).	d. Remove filter CCA (para 3-10*m*) and check resistance through components, one at a time, by lifting one of the leads (capacitors = neither shorted nor open, resistors = 390Ω ± 10%).
	e. Defective overvoltage absorber 19A1RV1 (fig. 3-6). **NOTE** Overvoltage absorber is soldered between terminals 1 and 2 of transformer 19A1T1.	e. Remove overvoltage absorber (para 3-10*g*). Replace if shorted.
	f. Defective connector 19A1P1 (fig. 3-6) or associated wiring.	f. Check wiring between connector pins and power supply points using figure FO-11 and FO-12. Repair faulty wiring or replace connector (para 3-10*r*) if necessary.
2. Either +10V or −10V is absent, but not both.	a. Defective diode(s) on diode bridge CCA 19A1A2 (fig. 3-6).	a. Remove diode bridge CCA (para 3-10*l*) and check forward and reverse resistance through each diode (forward = 5-15Ω, reverse ≥ 1000Ω). Replace any defective diode found.
	b. Defective capacitor(s) or resistor(s) on filter CCA 19A1A1 (fig. 3-6).	b. Remove filter CCA (para 3-10*m*) and check resistance through components, one at a time, by lifting one of the leads (capacitors = neither shorted nor open, resistors = 390Ω ± 10%).
	c. Defective connector 19A1P1 (fig. 3-6) or associated wiring.	c. Check wiring between connector pins and power supply points using figure FO-11 and FO-12. Repair faulty wiring or replace connector (para 3-10*r*) if necessary.
3. +10V and −10V are present, but POWER ON indicator does not illuminate.	a. Defective POWER ON indicator socket 19A1XDS1 (fig. 3-7).	a. Check continuity through indicator socket. Replace if defective (para 3-10*p*).
4. +10V and −10V are present, but power supply still causes data buffer to malfunction.	a. Defective connector 19A1P1 (fig. 3-6) or associated wiring.	a. Check continuity between all connector pins and power supply points using figure FO-11 and FO-12. Repair faulty wiring or replace connector (para 3-10*r*) if necessary.

Section IV. MAINTENANCE OF DATA BUFFER

3-7. Adjustments

Do not perform any adjustments on the data buffer at the direct support maintenance level.

CAUTION

Potentiometers and variable capacitors are contained on printed circuit boards. Do not attempt to adjust these components.

3-8. Alignment

Do not perform any alignment procedures on the data buffer at the direct support maintenance level.

3-9. Repair

Repair of the data buffer consists of replacing the assemblies or components found to be defective during troubleshooting. Refer to removal and replacement procedures.

3-10. Removal and Replacement

After removal and replacement of any component or assembly, except for covers, perform an operational test in accordance with paragraph 3-11 and 3-12.

CAUTION

Most chassis mounting and securing is accomplished by means of captive-type nuts. Do not attempt to turn nuts unless specifically instructed to do so.

NOTE

CCAs are marked to show polarization of applicable components such as capacitors and diodes. The positive terminal of these components is indicated by a square solder pad and the negative terminal by a round solder pad. Pin 1 of multi-pin components such as integrated circuits is also indicated by a square pad.

a. Rear Access Cover Assembly (Fig. 3-1).

(1) Loosen 10 captive screws securing rear access cover assembly to the data buffer.

(2) Pull the rear access cover assembly from the data buffer.

(3) Replace rear access cover assembly by reversing removal procedure.

NOTE

When tightening rear access cover captive screws, tighten each a few turns in sequence. Do not overtighten. In the event that the captive screws cannot be aligned with their respective holes, pull rear access cover assembly back slightly, realign, and tighten.

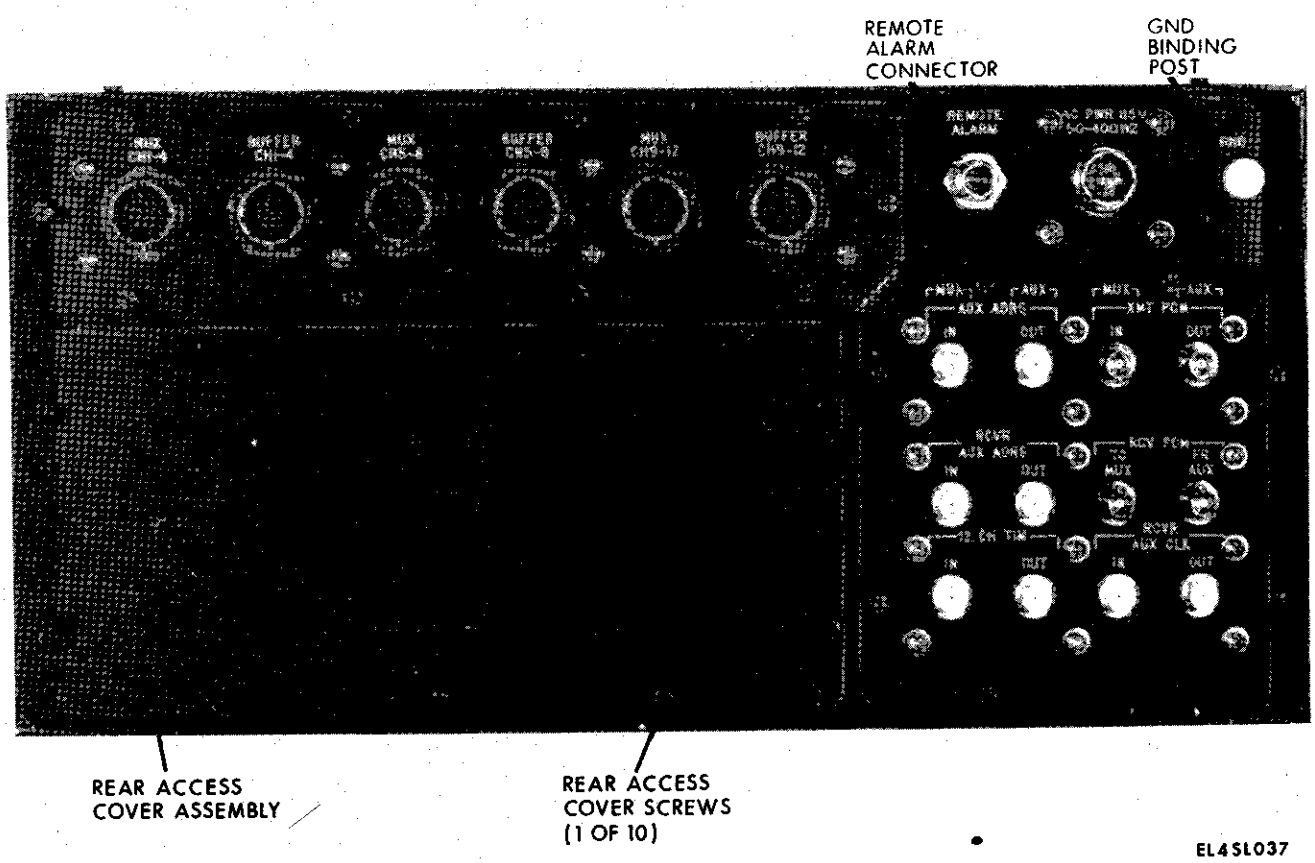


Figure 3-1. Data buffer, rear view.

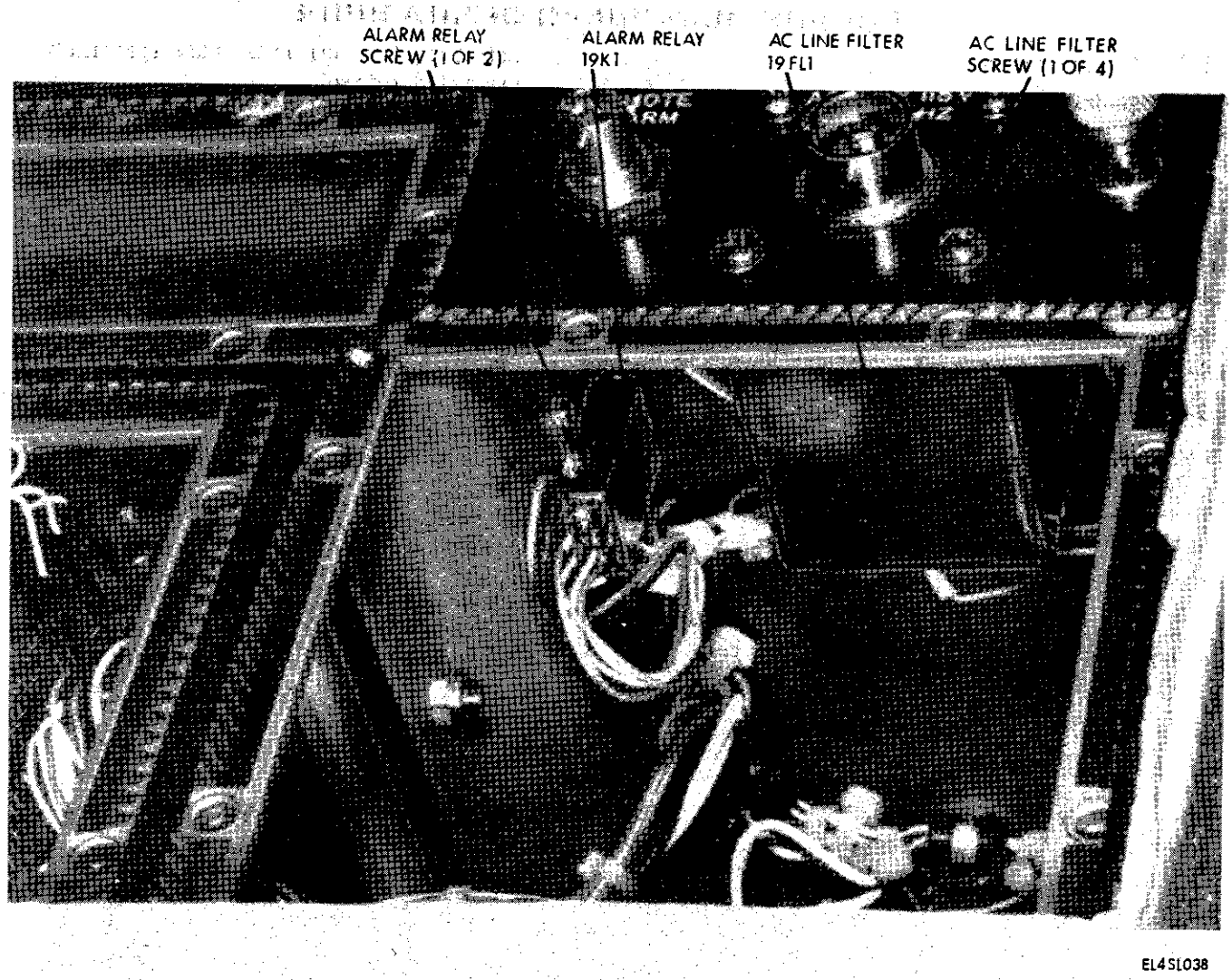


Figure 3-2. Removal and replacement of ac line filter and alarm relay.

b. AC Line Filter 19FL1 (Fig. 3-2).

(1) Remove power supply and high speed filter assemblies in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove four screws securing ac line filter to rear of data buffer.

(3) Remove ac line filter from data buffer with wires still attached.

(4) Tag, unsolder, and remove the three wires and the two overvoltage protectors from the ac line filter.

(5) Install replacement ac line filter in the reverse order of removal.

c. Upper and/or Lower Printed Circuit Card Guides (Fig. 3-3 and 3-4).

(1) Remove front cover assembly and 15 printed circuit card assemblies in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove six screws (fig. 3-3) securing shielding gasket to data buffer and remove shielding gasket.

(3) Remove three screws (fig. 3-3) securing lower printed circuit card guide and/or three screws securing upper printed circuit card guide to data buffer, as applicable.

(4) Remove rear access cover assembly in accordance with paragraph 3-10*a*.

(5) If upper printed circuit guide is being replaced, remove audio filter assembly in accordance with TM 11-5805-637-12.

(6) Remove four screws (fig. 3-4) securing lower printed circuit card guide and/or four screws securing upper printed circuit card guide to printed circuit card connector assembly, as applicable.

(7) If lower printed circuit card guide is being replaced, remove three screws, flat washers, and nuts (fig. 3-4) securing lower printed circuit card guide to data buffer.

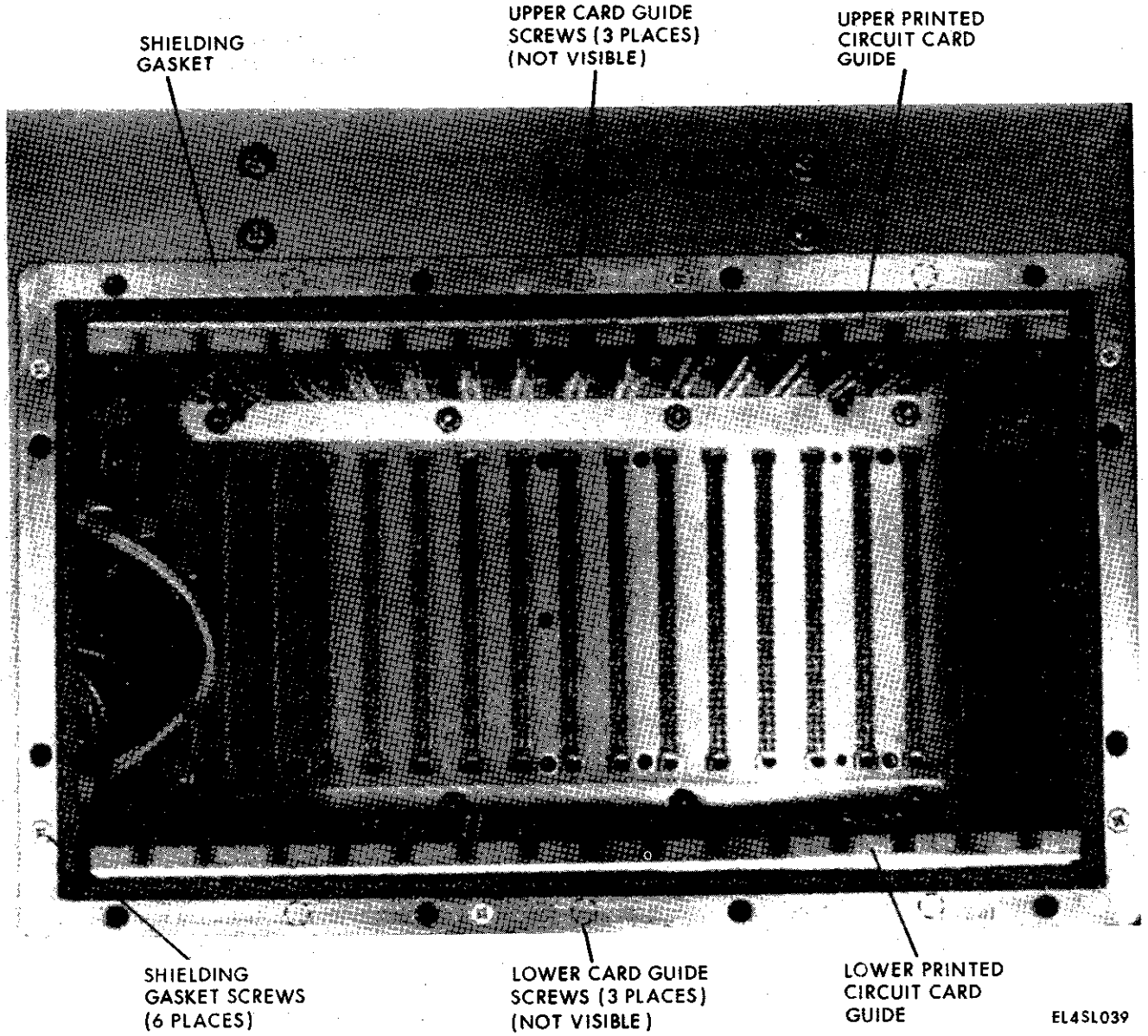


Figure 3-3. Printed circuit card guides, front view.

NOTE

The three screws removed in step (7) are not held down by captive-type nuts. Remove the nuts with the screws.

(8) Remove lower and/or upper printed circuit card guides from data buffer.

(9) Install replacement lower and/or upper printed circuit card guides in the reverse order of removal, but do not fully tighten screws. When all screws are in loosely, insert two printed circuit card assemblies, one at each end of the card guide assemblies. Use these as a guide to align the guide assemblies before tightening screws. Insert remaining printed circuit card assemblies.

d. Alarm Relay 19K1 (Fig. 3-2).

(1) Remove high speed filter and audio filter assemblies from data buffer in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove two screws and nuts securing alarm relay to inside wall of data buffer. Remove cable clamps as necessary by removing screw, washer, and nut securing clamp to inside wall of data buffer.

(3) Remove alarm relay, with wires attached, through rear of data buffer.

(4) Tag, unsolder, and remove wires from the relay.

(5) Install replacement relay in the reverse order of removal.

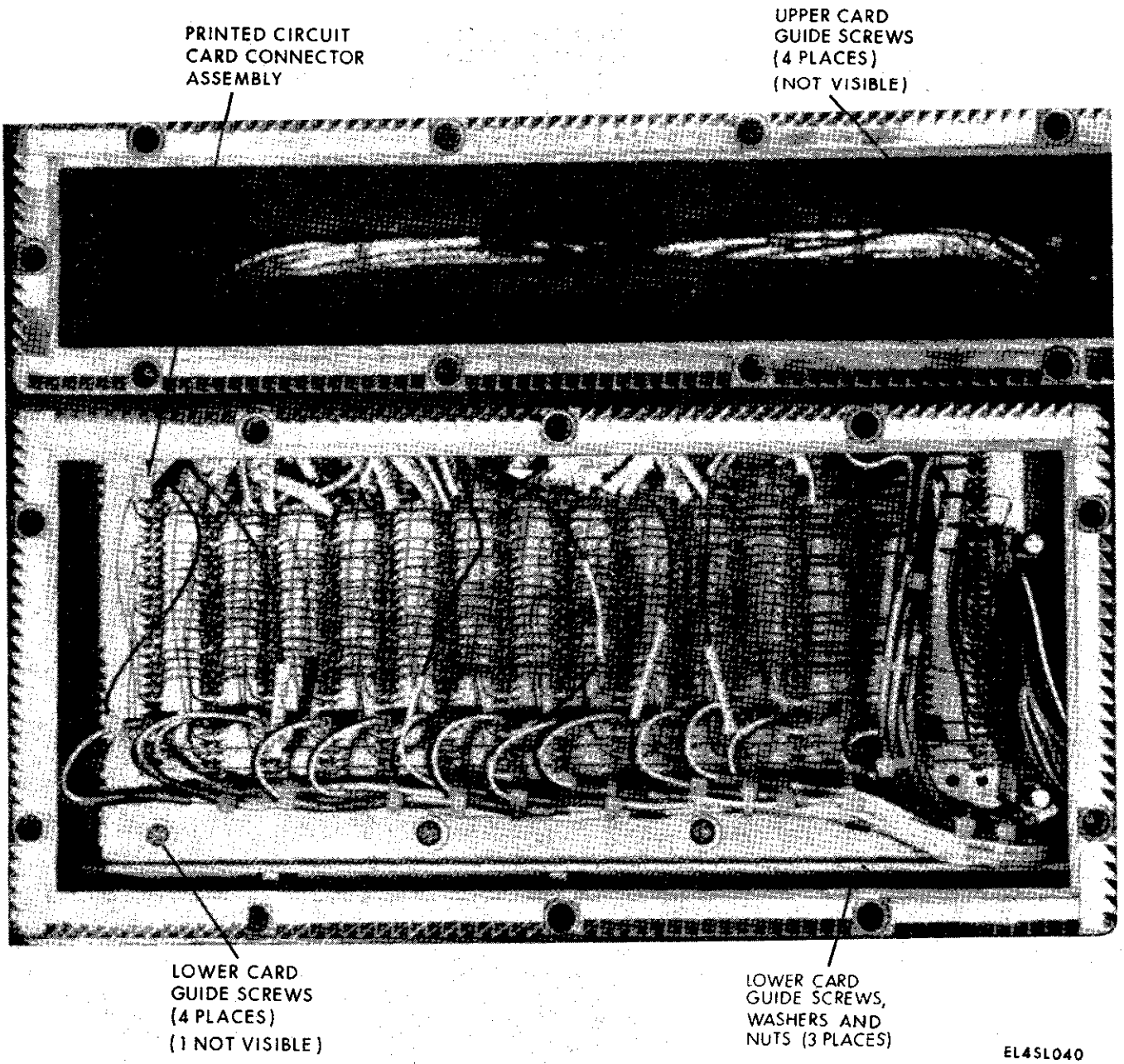


Figure 3-4. Printed circuit card guides, rear view.

e. BUZZER OFF Switch 19S2 (Fig. 3-5).

(1) Remove power supply and high speed filter assemblies in accordance with replacement procedures in TM 11-5805-637-12.

(2) Being careful not to scratch front panel, remove hardware securing switch to front panel and push out switch through rear of panel.

(3) Drop switch down through power supply opening in front panel.

(4) Tag, unsolder, and remove wires from switch.

(5) Install replacement switch in the reverse order of removal.

f. ALARM Indicator Socket 19XDS1 (Fig. 3-5).

(1) Remove power supply and high speed filter assemblies in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove BUZZER OFF switch (para 3-10*e*) and loudspeaker (para 3-10*i*).

(3) Remove hardware from rear of socket and push socket out front of panel.

(4) Tag, unsolder, and remove wires from socket.

(5) Install replacement socket in the reverse order of removal.

g. TEST Indicator Socket 19XDS2 (Fig. 3-5).

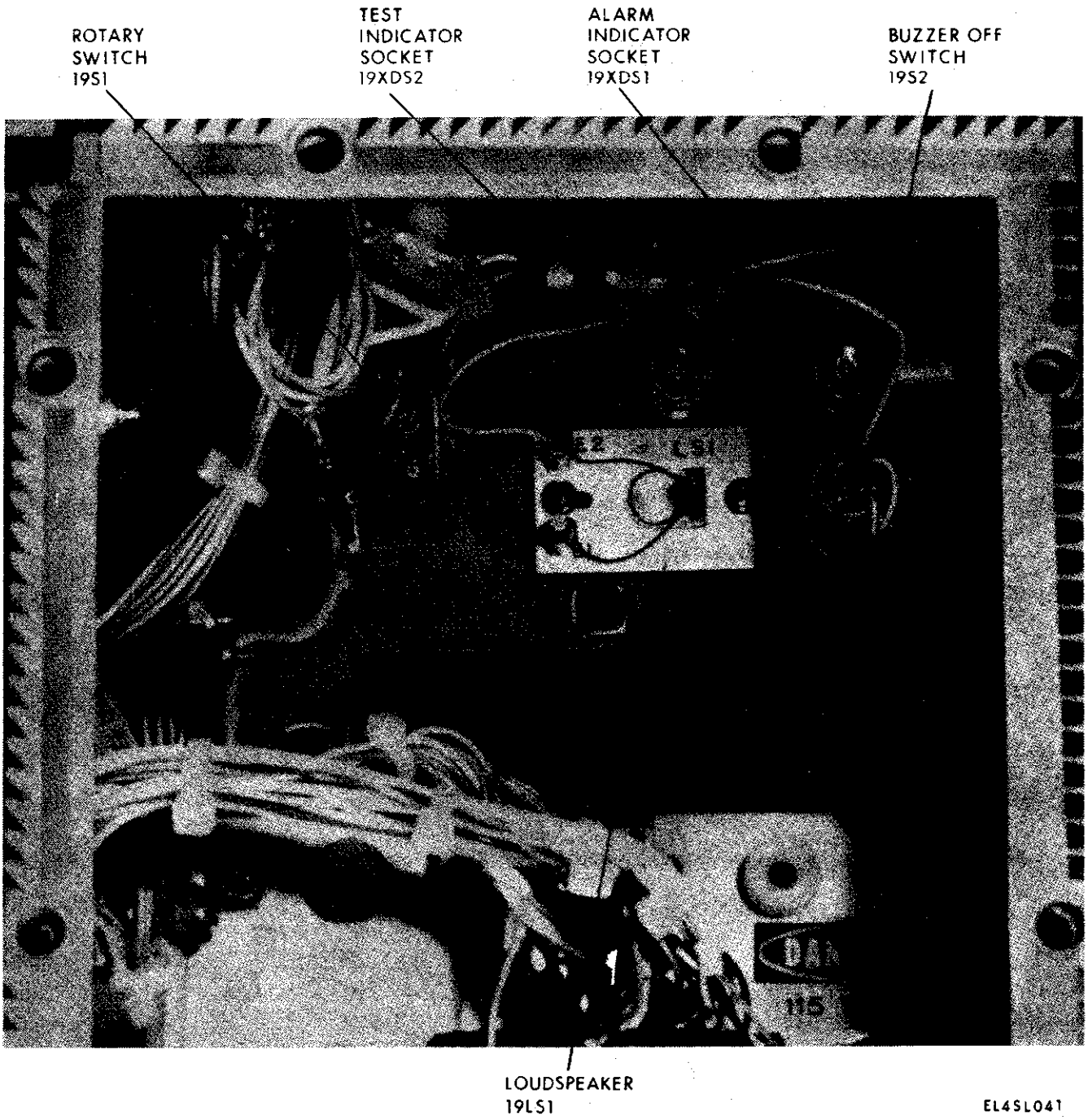


Figure 3-5. Removal and replacement of front panel components.

(1) Remove power supply and high speed filter assemblies in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove hardware from rear of socket and push socket out front of panel.

(3) Tag, unsolder, and remove wires from socket.

(4) Install replacement socket in the reverse order of removal.

h. Rotary Switch 19S1 (Fig. 3-5).

(1) Remove power supply and high speed filter assemblies in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove the knob from the switch.

(3) Remove hardware securing switch to front panel and push switch out carefully through rear of panel. Guide switch by wiring harness.

(4) Remove cable clamps as necessary by removing screw, washer, and nut securing clamp to inside

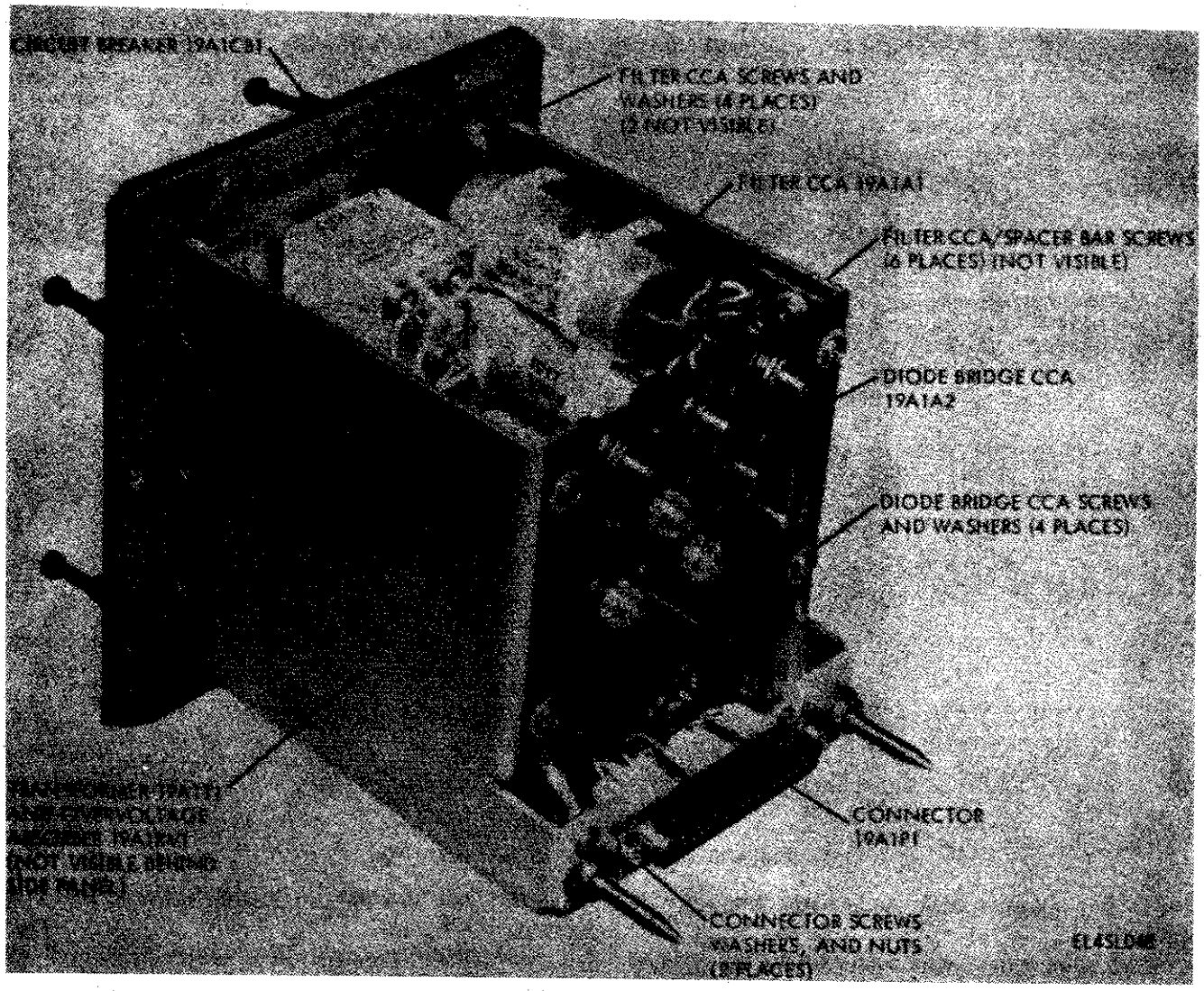


Figure 3-6. Power supply assembly, top rear view.

wall of data buffer. Drop switch down through power supply opening in front panel.

(5) Tag, unsolder, and remove the harness wires from the rotary switch.

(6) Add jumper wires to replacement switch per connections on old switch.

(7) Install replacement switch in the reverse order of removal. Align switch slot with panel markings and rotate switch knob several times to make sure switch is properly installed. Align knob so that it points away from flat side of switch shaft.

i. Loudspeaker 19LS1 (Fig. 3-5).

(1) Remove power supply and high speed filter assemblies in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove two screws securing loudspeaker to inside of front panel and remove loudspeaker, retaining plate, and gasket.

(3) Drop loudspeaker assembly down through power supply opening in front panel.

(4) Tag, unsolder, and remove the wires from the terminals on the loudspeaker.

(5) Install replacement loudspeaker in the reverse order of removal.

j. REMOTE ALARM Connector (Fig. 3-1).

(1) Remove power supply and high speed filter assemblies in accordance with replacement procedures in TM 11-5805-637-12.

(2) Being careful not to scratch rear panel, remove hardware securing REMOTE ALARM connector to rear panel of data buffer. Push out connector through rear of panel.

(3) Remove cable clamps as necessary by removing screw, washer, and nut to inside wall of data buffer. Drop connector down through opening in rear of data buffer.

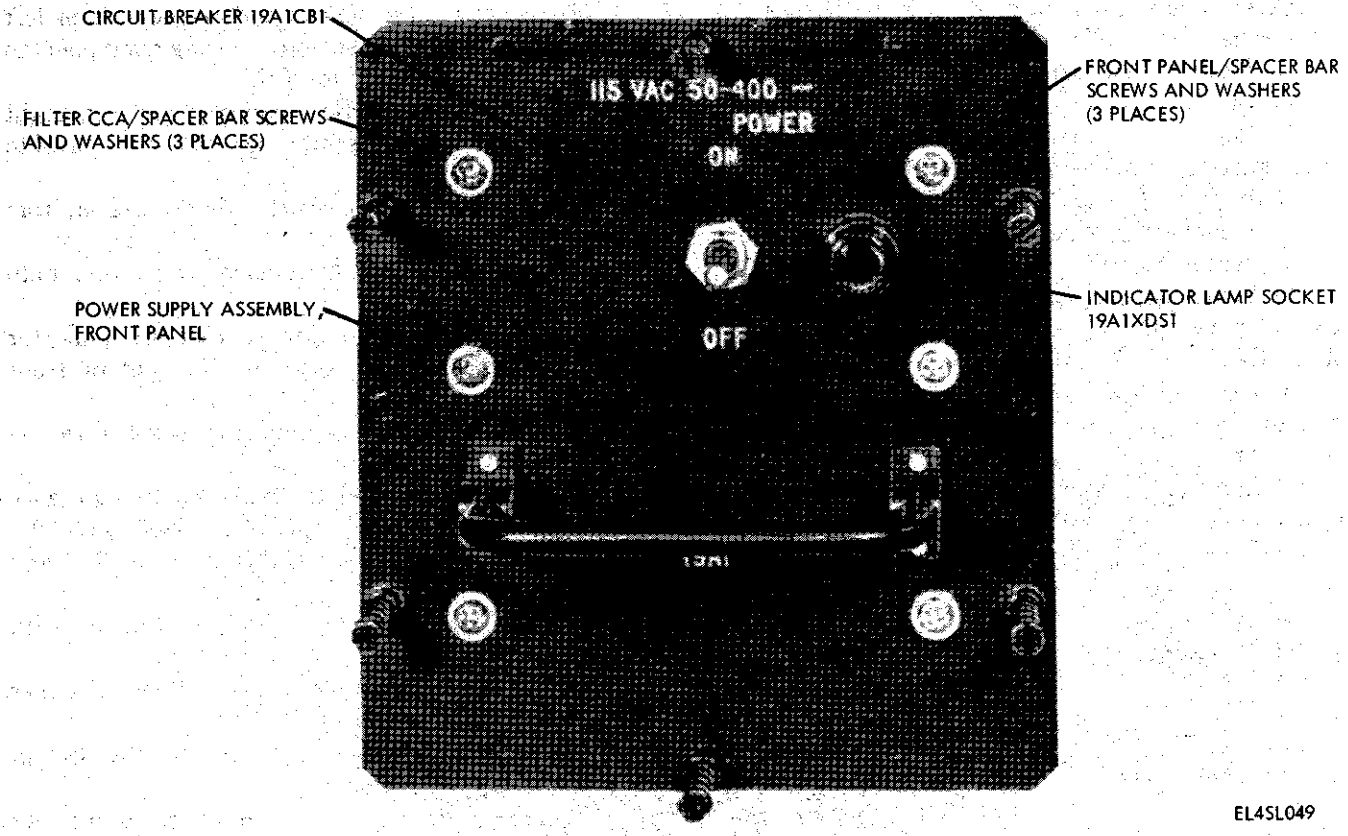


Figure 3-7. Power supply assembly, front view.

(4) Tag, unsolder, and remove wires from the connector.

(5) Install replacement connector in the reverse order of removal.

k. GND Binding Post (Fig. 3-1).

(1) Remove power supply and high speed filter assemblies in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove hardware and lug from rear of binding post and push binding post out through rear of data buffer.

(3) Install replacement binding post in the reverse order of removal.

l. Diode Bridge CCA 19A1A2 (Fig. 3-6).

CAUTION

When replacing diodes on diode bridge CCA, replace protector caps on diodes as shown in figure 3-6 to prevent damage to wiring.

(1) Remove power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove four screws and washers securing diode bridge CCA to rear of power supply assembly. Remove diode bridge CCA with wires attached.

(3) Tag, unsolder, and remove wires from diode bridge CCA.

(4) Install repaired diode bridge CCA in the reverse order of removal.

(5) Replace power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

m. Filter CCA 19A1A1 (Fig. 3-6 and 3-7).

(1) Remove power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove diode bridge CCA in accordance with paragraph 3-10*l*.

(3) Remove six screws from left side of power supply assembly securing filter CCA and attached spacer bars.

(4) Remove three screws and washers from front of power supply assembly securing filter CCA and attached spacer bars.

(5) Remove filter CCA, with wires attached, through rear of power supply assembly.

(6) Remove spacer bars from filter CCA by removing four screws and washers securing spacer bars to filter CCA.

(7) Tag, unsolder, and remove wires from filter CCA.

NOTE

When installing new capacitors on filter CCA, secure capacitors to CCA with new straps.

(8) Install repaired filter CCA in the reverse order of removal.

(9) Replace power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

n. Transformer 19A1T1 (Fig. 3-7and 3-8).

(1) Remove power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove three screws and washers from left front of power supply assembly securing front panel filter CCA.

(3) Remove three screws and washers from right front of power supply assembly securing front panel to spacer bar.

(4) Remove front panel, with wires attached, and lay to one side.

(5) Remove four screws from bottom of power supply.

(6) Remove transformer, with wires attached, through front of power supply assembly.

(7) Tag, unsolder, and remove wires from transformer. Transfer the overvoltage absorber from pins of removed transformer to the same pins on replacement transformer.

(8) Install replacement transformer in the reverse order of removal.

(9) Replace power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

o. Circuit Breaker 19A1CB1 (Fig. 3-6 and 3-7).

(1) Remove power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove hardware securing circuit breaker to front panel. Remove circuit breaker, with wires attached, through top of power supply assembly.

(3) Tag, unsolder, and remove wires from circuit breaker.

(4) Install replacement circuit breaker in the reverse order of removal.

(5) Replace power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

p. POWER ON Indicator Socket 19A1XDS1 (Fig. 3-7).

(1) Remove power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove three screws and washers from left front of power supply assembly securing front panel to spacer bar and attached filter CCA.

(3) Remove three screws and washers from right front of power supply assembly securing front panel to spacer bar.

(4) Remove front panel, with wires attached, from power supply assembly.

(5) Tag, unsolder, and remove wires from indicater socket.

(6) Remove hardware from rear of indicator socket and push socket out through front of front panel.

(7) Install replacement indicator socket in the reverse order of removal.

(8) Replace power supply assembly in accordance with replacement procedure in TM 11-5805-637-12.

q. Overvoltage Absorber 19A1RV1 (Fig. 3-7 and 3-8).

(1) Remove diode bridge CCA in accordance with paragraph 3-10l.

(2) Unsolder and remove overvoltage absorber from transformer terminals 1 and 2.

(3) Install replacement overvoltage absorber in the reverse order of removal.

(4) Replace power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

r. Connector 19A1P1 (Figure 3-6).

(1) Remove power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

(2) Remove two screws, washers, and nuts securing the connector to the power supply. Remove connector, with wires attached, from power supply.

(3) Slide sleeving back from connector pins so that wire/pin connections are exposed. Tag, unsolder, and remove wires from connector pins. Do not remove sleeving.

(4) Install replacement connector in the reverse order of removal, sliding sleeving back over pins after wires are soldered on.

(5) Replace power supply assembly in accordance with replacement procedures in TM 11-5805-637-12.

Section V. DiRECT SUPPORT TESTiNG PROCEDURES

3-11. Introduction

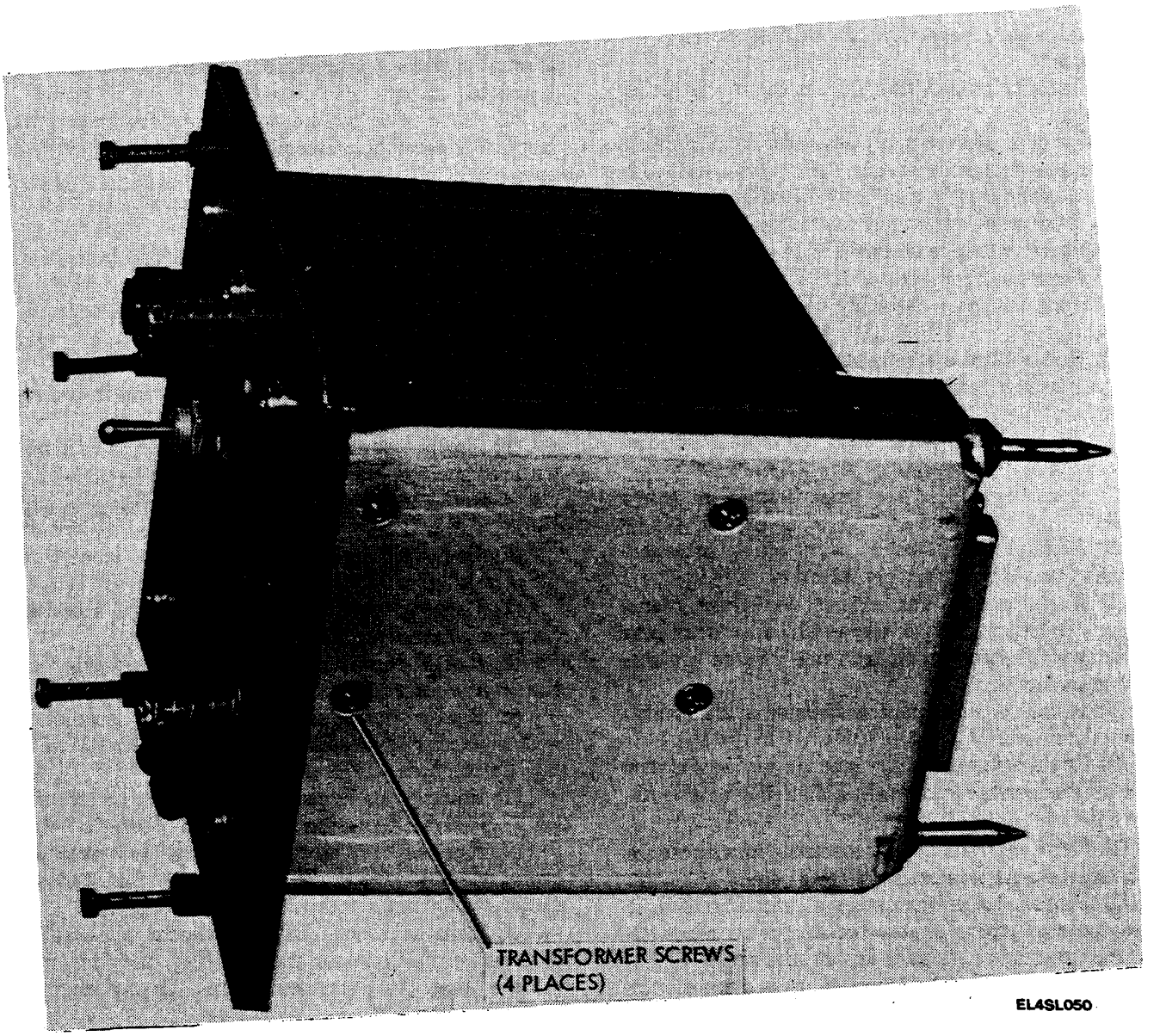
Testing the data buffer at the direct support maintenance level consists of performing the data buffer operational test. This test is used to verify proper data buffer operation after the data buffer has been repaired. Failure of any of the operational test steps indicates a fault in the data buffer. When a fault is indicated, it maybe isolated by using the troubleshooting procedures in Section III of this chapter.

3-12. Operational Test

NOTE

This tests only voice and relay functions of the data buffer. To insure proper data operation of data buffer, test unit in an operational system to see if traffic passes through without errors.

To perform the data buffer operational test, proceed as follows:



Figures 3-8. Power supply assemblys, bottom view.

a. Set POWER switches on all equipment to OFF. Connect equipment as shown in figure FO-10. Set the TD-660 ( )/G MODE switch to the 12 CH position.

b. Connect the oscilloscope and signal generator as indicated in table 3-3 for channel 1 testing. Set POWER switches on all equipment to ON.

c. Adjust signal generator to produce output frequency of 1 KHz at -4 dBm, using electronic voltmeter to observe signal level.

d. The waveform displayed on RIGHT oscilloscope channel (TD-1065/G output) should appear similar to waveform displayed on LEFT channel (TD - 1065/G input), but RIGHT channel peak-to-peak voltage should be about 10% less than that of LEFT channel.

e. Repeat steps *b* through ***d*** for channels 2 through 12.

f. Set POWER switch on data buffer to OFF.

g. Repeat steps *b* through *e.*

h. Set POWER switches on all equipment to OFF.

Table 3-3. Connections for Data Buffer Operational Test

CHANNEL TESTED	CONNECT FREQUENCY GENERATOR TO	CONNECT OSCILLOSCOPE TO
1	BUFFER CH1-4, pins A, B	BUFFER CH1-4, pins C, D
2	BUFFER CH1-4, pins J, K	BUFFER CH1-4, pins L, M
3	BUFFER CH1-4, pins E, F	BUFFER CH1-4, pins G, H
4	BUFFER CH1-4, pins N, P	BUFFER CH1-4, pins R, S
5	BUFFER CH5-8, pins A, B	BUFFER CH5-8, pins C, D
6	BUFFER CH5-8, pins J, K	BUFFER CH5-8, pins L, M
7	BUFFER CH5-8, pins E, F	BUFFER CH5-8, pins G, H
8	BUFFER CH5-8, pins N, P	BUFFER CH5-8, pins R, S
9	BUFFER CH9-12, pins A, B	BUFFER CH9-12, pins C, D
10	BUFFER CH9-12, pins J, K	BUFFER CH9-12, pins L, M
11	BUFFER CH9-12, pins E, F	BUFFER CH9-12, pins G, H
12	BUFFER CH9-12, pins N, P	BUFFER CH9-12, pins R, S

Section VI. OPERATIONAL TEST

3-13. Introduction

a. The TS-3981 can be used to test the Data Buffer TD-1065/G for errors, sync acquisition time, the alarm operation. The same setup is used for all tests. Loopback testing is used The TD-1065( )/G must be operated with a Multiplexer TD-660A/G or TD-660B/G. The TD-660/G cannot be used.

b. Audio test must be performed before power is supplied to the system.

NOTE

Except where indicated buffer data TD-660A/G Monnation referenced in this manual relates to the TD-660B/G as well.

3-14. Set-Up for Test Set Error Detector, and SG-1139/G Digital Data Generator

a. Interconnect the equipment shown in Figure 3-9 when data generator or error detector is available.

b. Set controls of TD-660A/G units as follows

(1) Master/Slave set to "Master"

(2) Mode set to "12 CH"

(3) 2 wire/4 wire set, to "4 wire"

(4) "Aux" (In/out) set to "OUT".

c. Turn on TD-660A/G unit and note the following

(1) "Out of frame" indicator is extinguished.

(2) All indicators are normal.

d. After opening the TD1065/G Circuit Card Assembly (CCA) access cover, set all 2 wire/4 wire switches on the Channel Unit CCAs (19A6) to the 4-wire position (UP). On Channel Unit CCA (19A6B) set A/B mode switch to the A mode position (UP).

e. Apply power to the TB-1065/G and note the following

(1) Initial alarm indicators (both audible and visual) clear automatically. The audible alarm is silenced using the "BUZZER OFF" pushbutton switch on TD-1065/G.

(2) Note the status of the green "TEST" lamp on the TD-1065/G for the TEST SWITCH positions listed below:

SWITCH POSITION	GREEN "TEST" LAMP INDICATION
OFF	OFF
-10V	ON
+10V	ON
XMT FRAME	ON
XMT TIME	ON
XMT PCM	ON
RCV PCM	ON
RCV TIME	ON
RCV FRAME	ON
COM	ON
CHAN	ON

(3) On the TD-660A/G units, note the following

(a) "Out of frame" indicators are extinguished

(b) All indicators are normal.

3-15. Operation When Using TS-3981/P or SG-1139/G

a. If TS-3981/P is used set the controls as follows for the 32 kb/sec (4-wire test):

(1) "PATTERN" Switch set to "LONG".

(2) "OPERATION" Switch set to "4W'

(3) "CORRELATOR LOOP" Switch set to "OPEN"

(4) "DATA" (ON/OFF) Switch set to "ON".

(5) "Rate Selection" Switch set to "7" (32 kb/s).

(6) "Display Select" Switch set to "ERRORS".

b. If using the SG-1139/G set the controls as follows:

(I) "TIMING" to "MASTER"

(2) "DATA RATE (kb/s)" to "32".

3-16 Test

a. Energize the TS-3981/P or SG-139/G and interconnect to Channel 1 of the TD-1065/G.

NOTE

"DATA" (Activity) lamp on DSED(S) is/are lit (illuminated).

b. Using the display "RESET" pushbutton switch on the TS-3981/P or SG-1139/G, reset the display to show no errors. Correlate data transmission for errors for not less than five (5) seconds. Acceptance criteria will be no errors shown on display. Rejection criteria will be when any error(s) is/are shown on the display.

c. Using the "SINGLE ERROR" insertion pushbutton switch, inject errors (not less than ten (l0))into the data stream. Acceptance criteria will be that the number of errors shown on the display equal the number of errors inserted. Rejection criteria shall be that the number shown does not equal the number of errors inserted.

d. Set A/B mode switch on Channel Unit CCA (19A6B) to B position (down). Repeat steps a thru c.

e. Repeat paragraph 3-15 steps a or b and paragraph 3-16 steps a-d for the remaining eleven (11) channels. This completes the 32kb/s 4-wire tests.

f. TD-1065/G and TD-1065B/G with CCA 19A6B in A mode only, for 16KB/s 4-wire tests use figure 3-9. Set the "DATA" (RATE SELECT) Switch on the TS 3981/P to the "6" position (16kb/s) or data rate (kb/s) "SWITCH" on the SG-1139/G to "16".

g. Interconnect the TS-3981/P or SG-1139/G to Channel 1 of the TD-1065/G or TD-1065B/G.

NOTE

"Data" (activity) indicator on the SED (UNIT B) is "on".

h. Using the display "RESET" pushbutton switch on the TS-3981/P or SG-1139/G, reset the display to show no errors. Correlate data transmissions for errors for not less than five (5) seconds. Acceptance criteria will be no errors shown on display(s). Rejection criteria will be when any error(s) is/are shown on the display(s).

i. Using the "SINGLE ERROR" insert pushbutton switch on the DSED(S), inject errors (not less than ten (10)) into the data stream. Acceptance criteria shall be that the number of errors displayed equal the number inserted.

j. Repeat paragraph 3-16 steps f, g, h, and i for the remaining eleven (11) channels.

3-17 161kb/s 2-wire Tests, TD-106S ( )/Q

a. Connect as shown in figure 3-10.

h Set 2W/4W Switches on CCA 19A6, CCA 19A6A or CCA 19A6B card to 2W position(down). On Channel Unit CCA 19A6B A/B mode SWITCH to A mode position (up).

c Interconnect TS-3981/P or SG-1139/G to channel 1 of the TD-1065 ( )/G controls on both drop boxes to channel 1.

d. Observe the "data" activity indicator. Acceptance criteria shall be that the activity indicator is lit or flashing. Rejection criteria shall be that the activity indicator is off.

e. Set A/B mode switch on Channel Unit CCA (19A6B) to B position (down). Repeat step d.

f. Repeat paragraph 3-17 steps a thru e for the remaining 11 channels. This completes the 16kb/sec-2 wire testing.

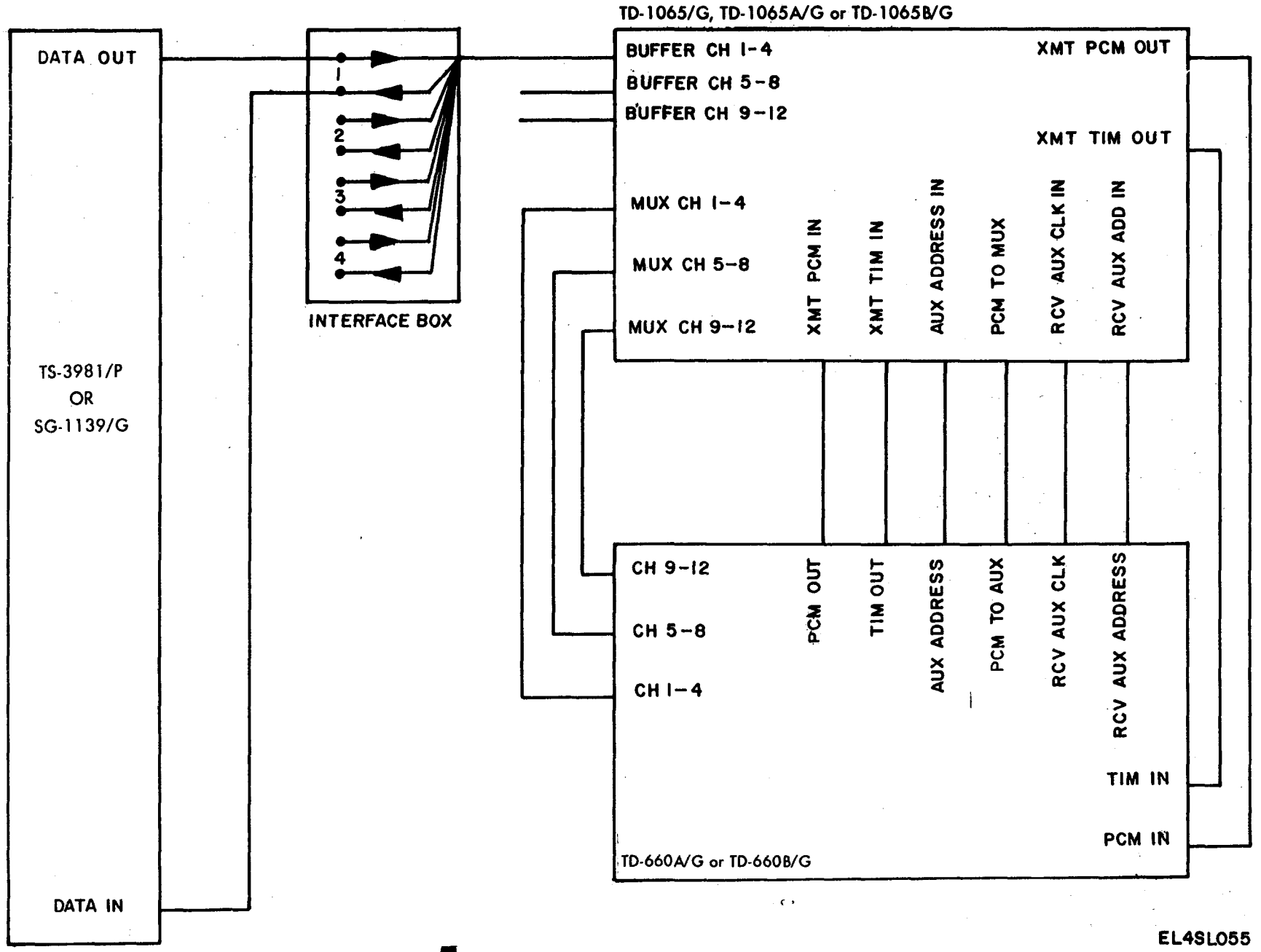


Figure 3-9. 16/32 KB/S 4W Tests TD-660A/G

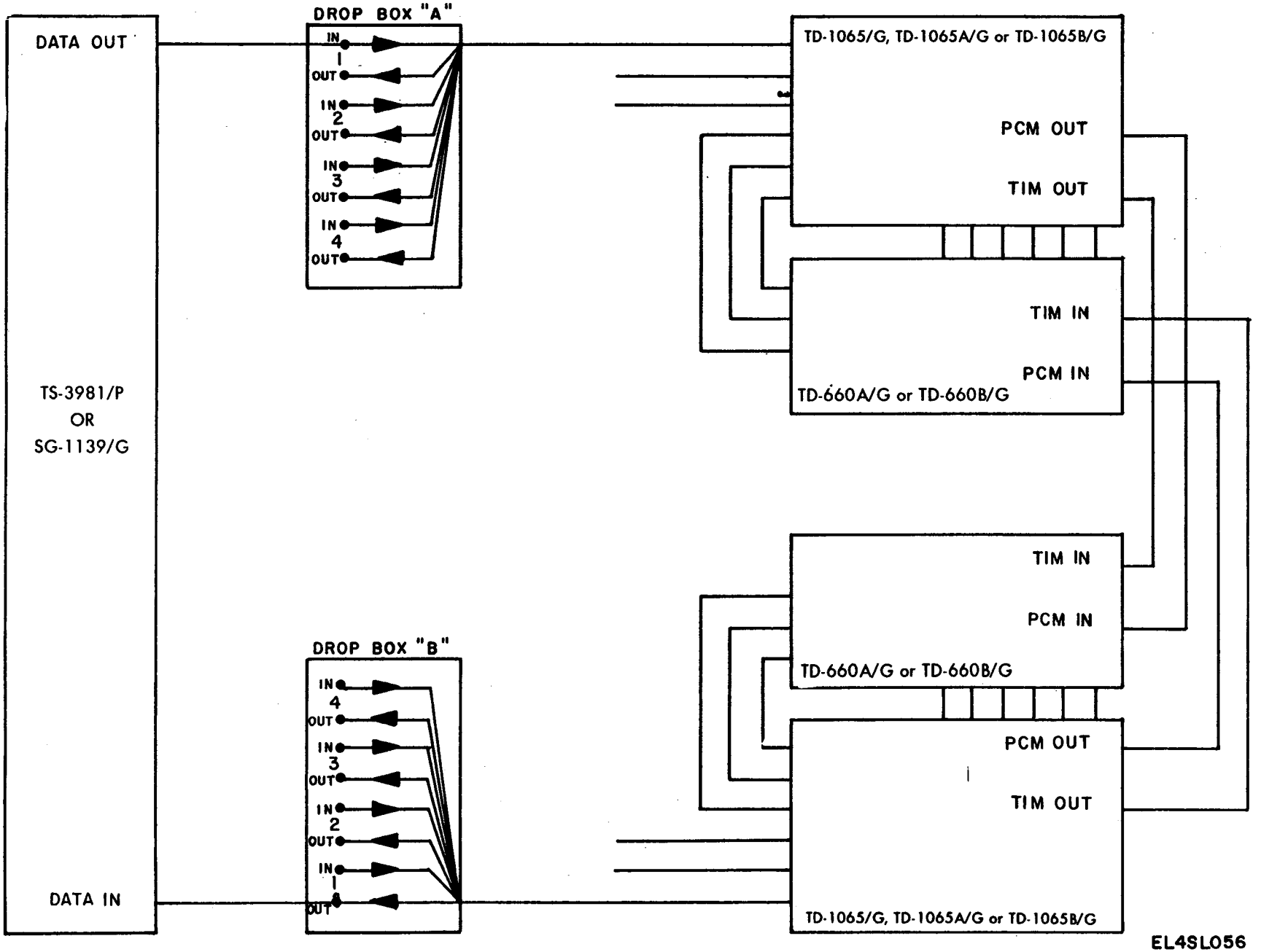


Figure 3-10. 16KB/S 2W Test

CHAPTER 4

GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

The direct support maintenance instructions contained in Chapter 3 of this manual are applicable to general support maintenance.

APPENDIX A

REFERENCES

DA Pam 25-30	Consolidated Index of Army Publications and Blank Forms.
DA Pam 738-750	The Army Maintenance Management System (TAMMS).
TM 11-5805-637-12	Operator and Organizational Maintenance Manual, Buffer, Data TD-1065/G (NSN 58054)14)28-8364).
TM 11-5805-637-2ZP	Organizational Maintenance Repair Parts and Special Tools Lists for Data Buffer TD-1065/G (NSN 5805-01-028-8364).
TM 11-5805-637-34P	Direct Support and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools) for Data Buffer TD-1065/G (NSN 5805-01-028-8364).
TM 11-6625-654-14	Operator's, Organizational, Direct Support and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools List) for Multimeter, AN/USM-223.
TM 11-6625-683-15	Operator's, Organizational, Direct Support, General Support, and Depot Maintenance Manual Signal Generator AN/URM-127 (NSN 6625-00-783-5965).
TM 11-6625-2658-14	Operator's, Organizational, Direct Support and General Support Maintenance Manual for Oscilloscope, AN/USM-281C (NSN 6625-00-106-9622).
TB 43-0118	Field Instructions for Painting and Preserving Electronics Command Equipment Including Camouflage Pattern Painting of Electrical Equipment Shelter.
TM 740-90-1	Administrative Storage of Equipment.
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

APPENDIX B

REPAIR PARTS AND SPECIAL TOOLS LISTS

Refer to TM 11-5805-637-34P for repair parts and special tools list.

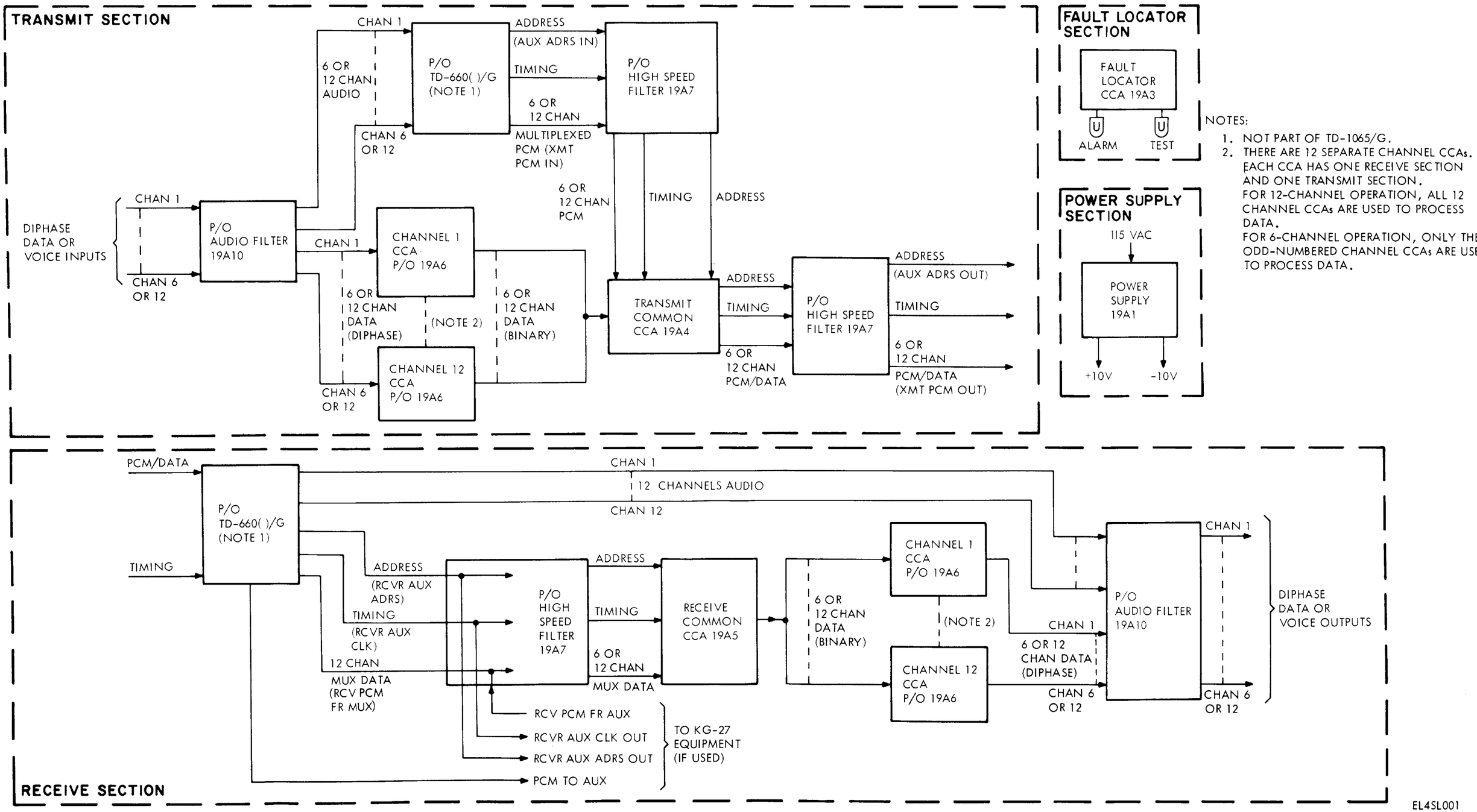
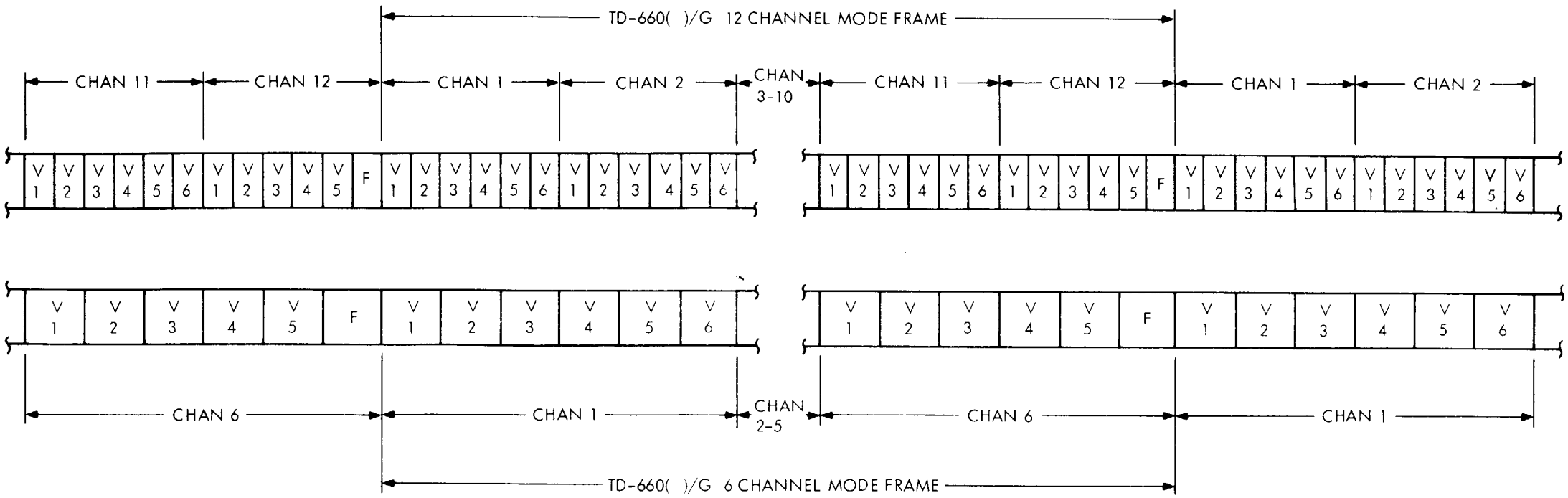


Figure FO-1. Data buffer, overall block diagram.



NOTES:

1. EACH 12 CHANNEL MODE FRAME CONTAINS 12 CHANNELS. EACH CHANNEL CONTAINS 6 BITS. BITS V1-V6 ARE VOICE (PCM) BITS. BIT 6 OF CHANNEL 12 IS THE FRAMING BIT (F).

2. EACH 6 CHANNEL MODE FRAME CONTAINS 6 CHANNELS. EACH CHANNEL CONTAINS 6 BITS. BITS V1-V6 ARE VOICE (PCM) BITS. BIT 6 OF CHANNEL 6 IS THE FRAMING BIT (F).

EL4SL042

Figure FO-2. TD-660( )/G frame format, six and 12-channel.

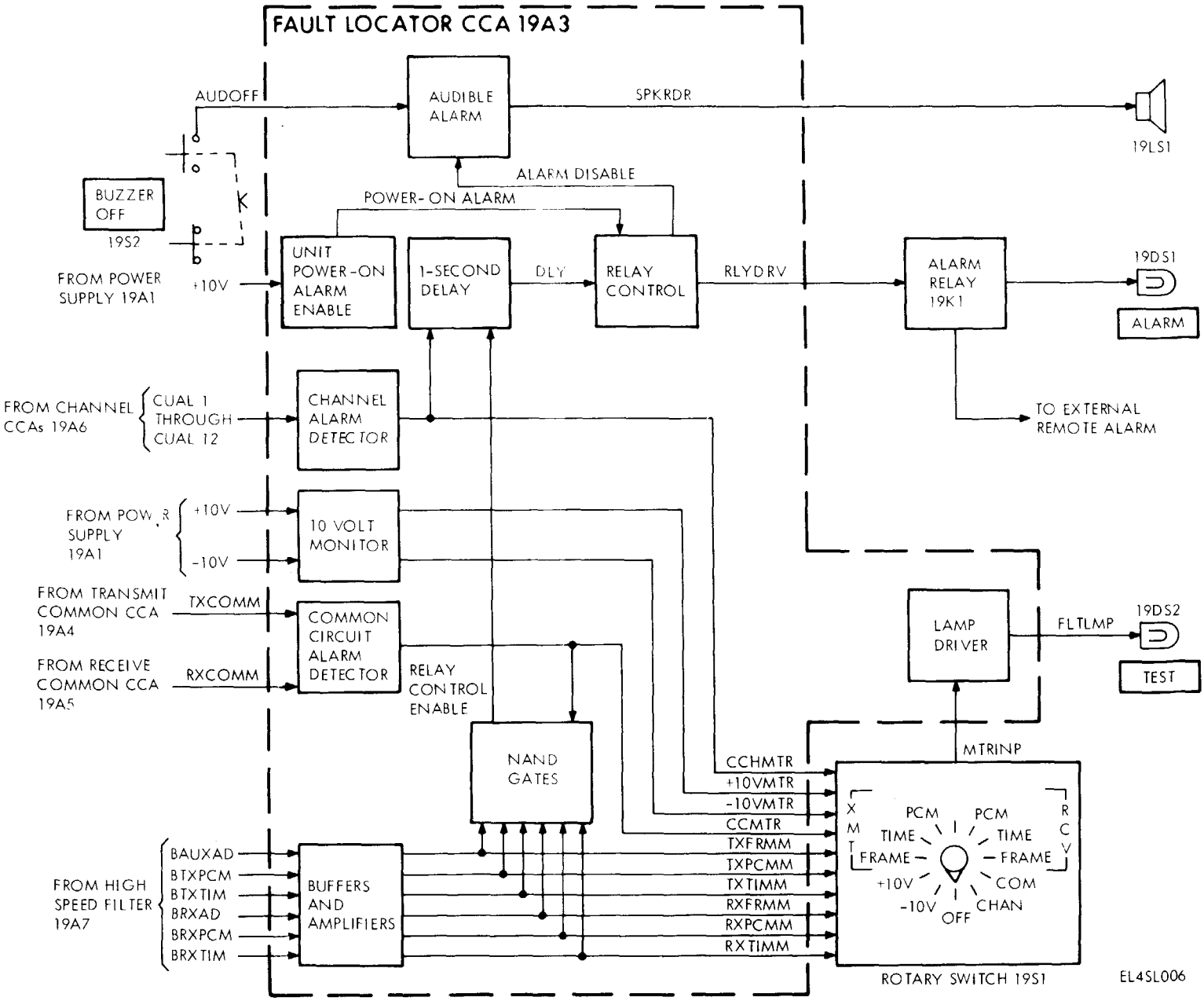


Figure FO-3. Fault locator CCA 19A3, functional block diagram

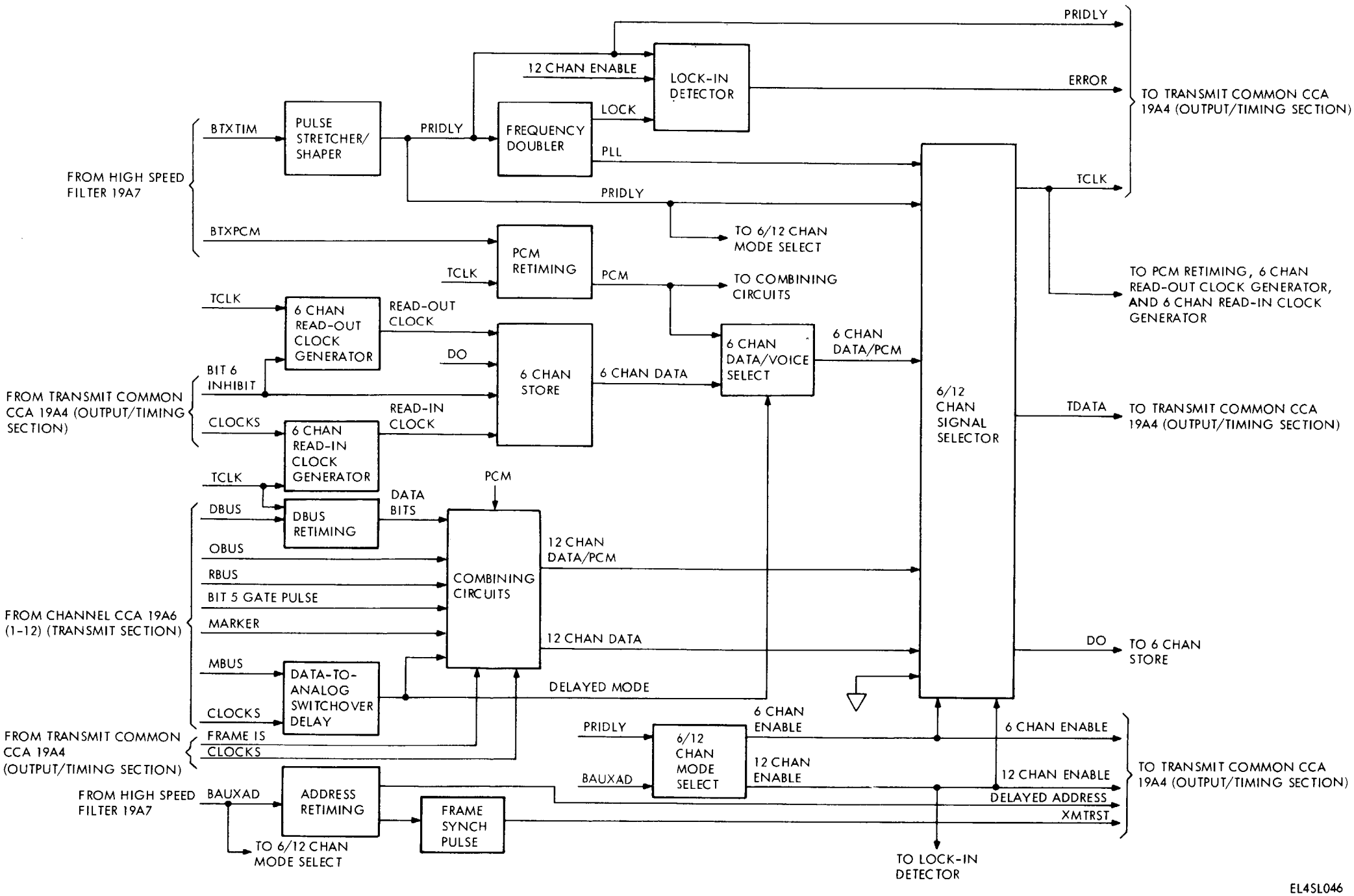
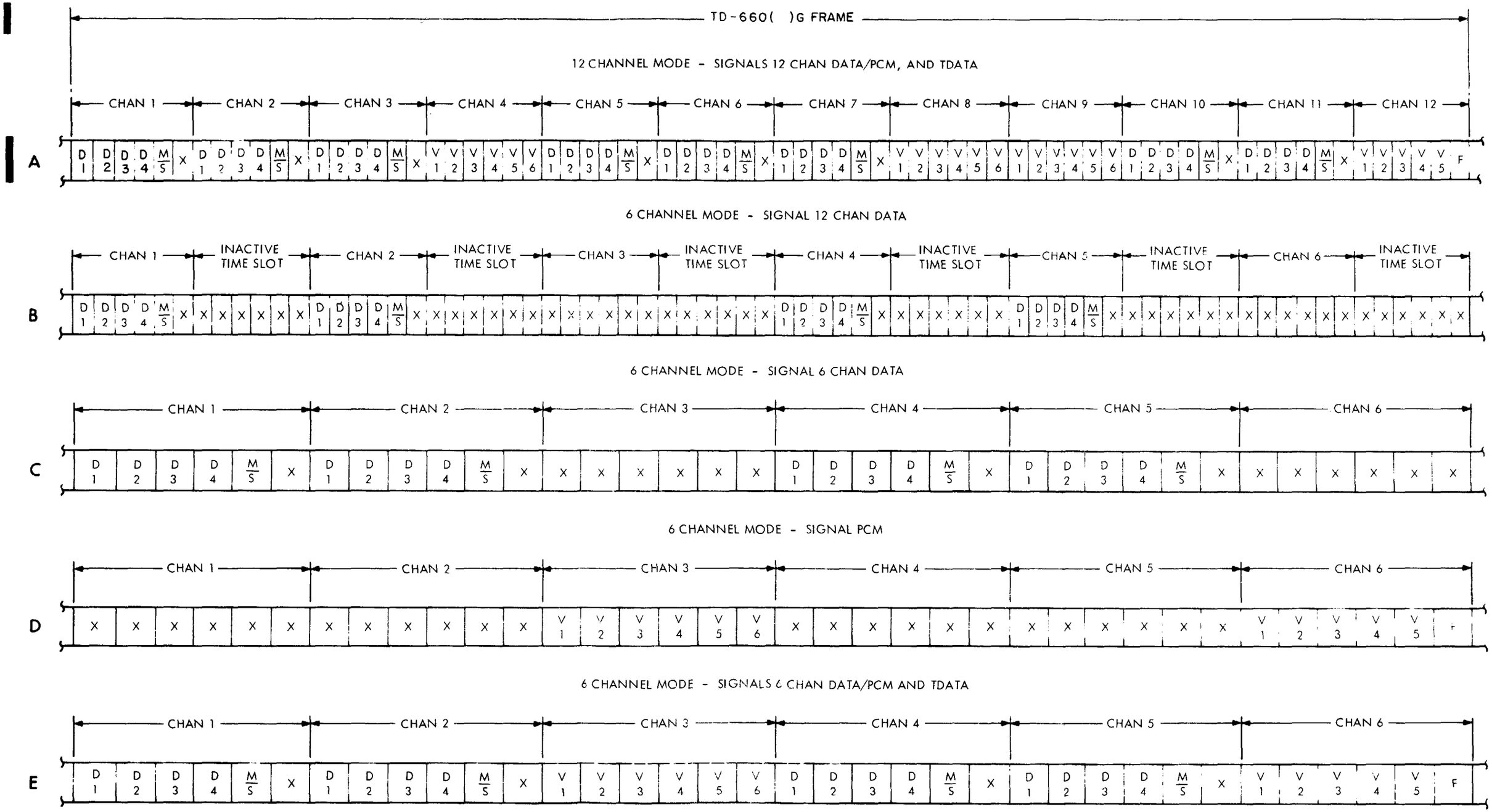


Figure FO-4. Transmit common CCA 19A4 (input/select section), functional block diagram.



NOTES:

1. FRAME SHOWN IS TYPICAL OF ANY FRAME EXCEPT CONTROL CHANNEL FRAMES 15 OR 16.
2. 12 CHANNEL MODE FRAME IS SHOWN CONTAINING DATA IN CHANNELS 1, 2, 3, 5, 6, 7, 10, AND 11. 12 CHANNEL MODE FRAME IS SHOWN CONTAINING VOICE IN CHANNELS 4, 8, 9, AND 12.
3. 6 CHANNEL MODE FRAME IS SHOWN CONTAINING DATA IN CHANNELS 1, 2, 4, AND 5. 6 CHANNEL MODE FRAME IS SHOWN CONTAINING VOICE IN CHANNELS 3 AND 6.
4. $\frac{M}{S}$ = EITHER M OR S; M = MARKER BITS (FROM RBUS), S = STUFF/SPILL SIGNALING BITS (FROM OBUS).
5. D1-D4 ARE DATA BITS (FROM DBUS).
6. V1-V6 ARE PCM (VOICE) BITS.
7. X = UNUSED BIT

EL4SL057

Figure FO-5. Combining channel process timing, six and 12-channel.

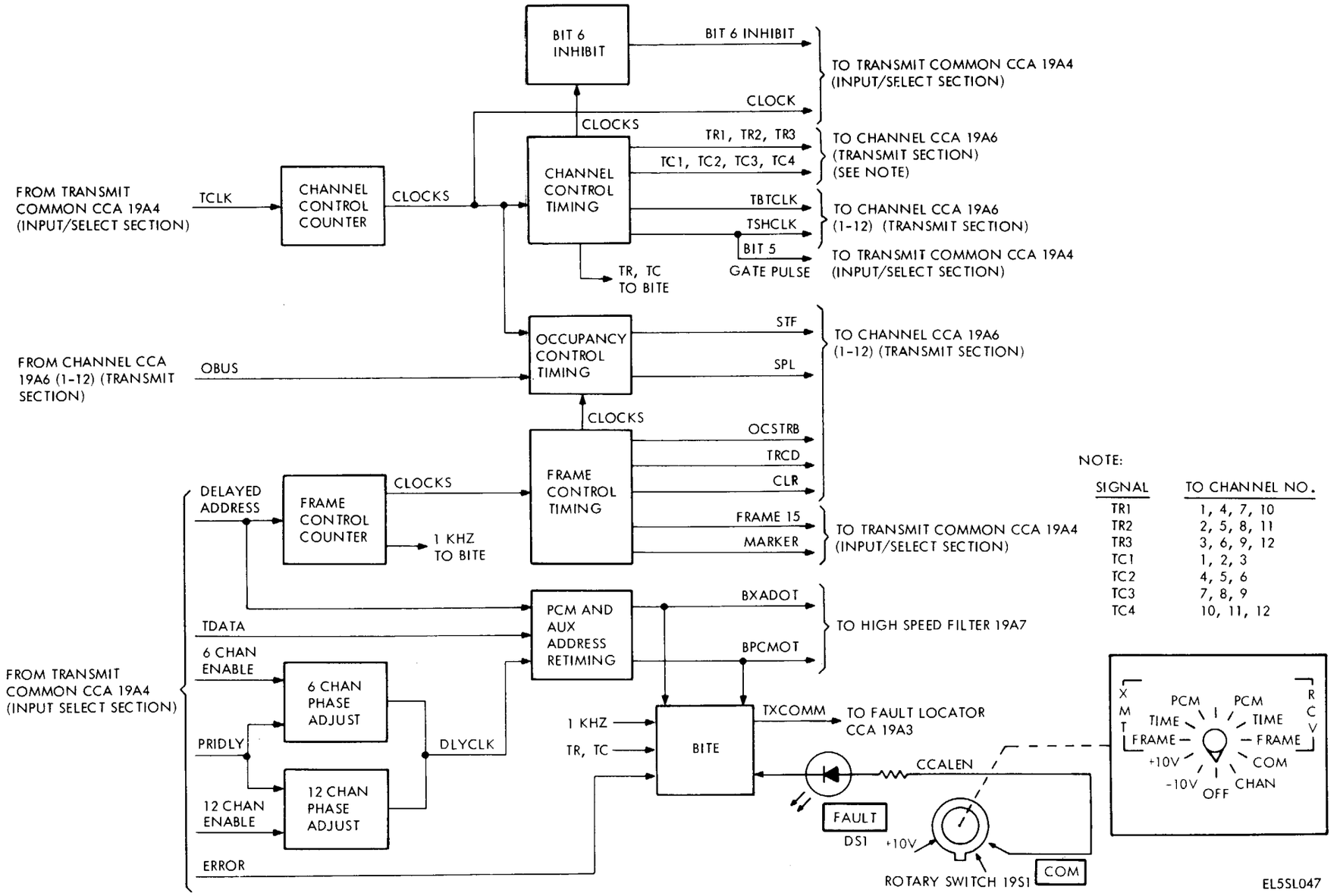
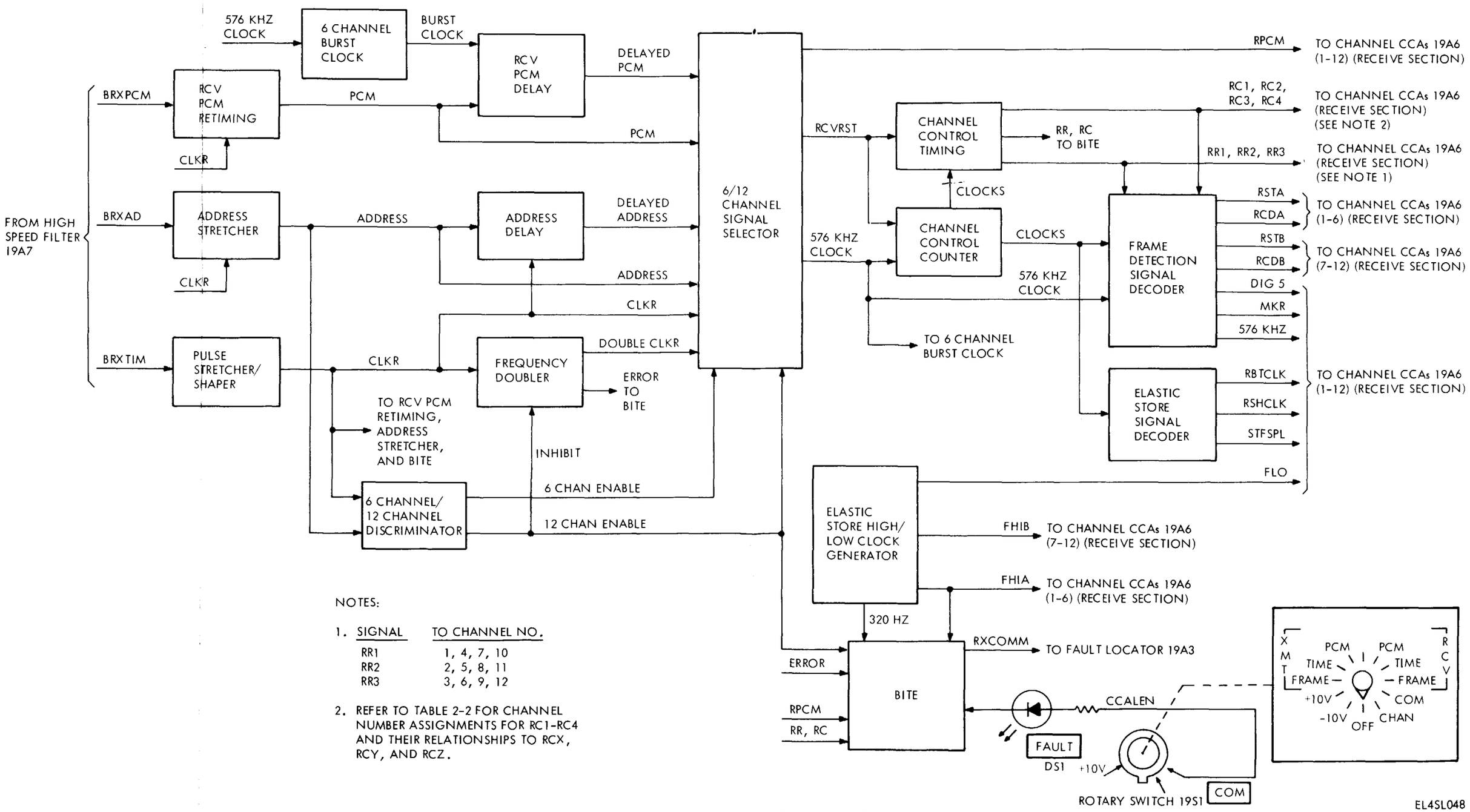


Figure FO-6. Transmit common CCA 19A4 (output/timing section), functional block diagram.



NOTES:

1. SIGNAL — TO CHANNEL NO.

SIGNAL	TO CHANNEL NO.
RR1	1, 4, 7, 10
RR2	2, 5, 8, 11
RR3	3, 6, 9, 12

2. REFER TO TABLE 2-2 FOR CHANNEL NUMBER ASSIGNMENTS FOR RC1-RC4 AND THEIR RELATIONSHIPS TO RCX, RCY, AND RCZ.

Figure FO-7. Receive common CCA 19A5, functional block diagram.

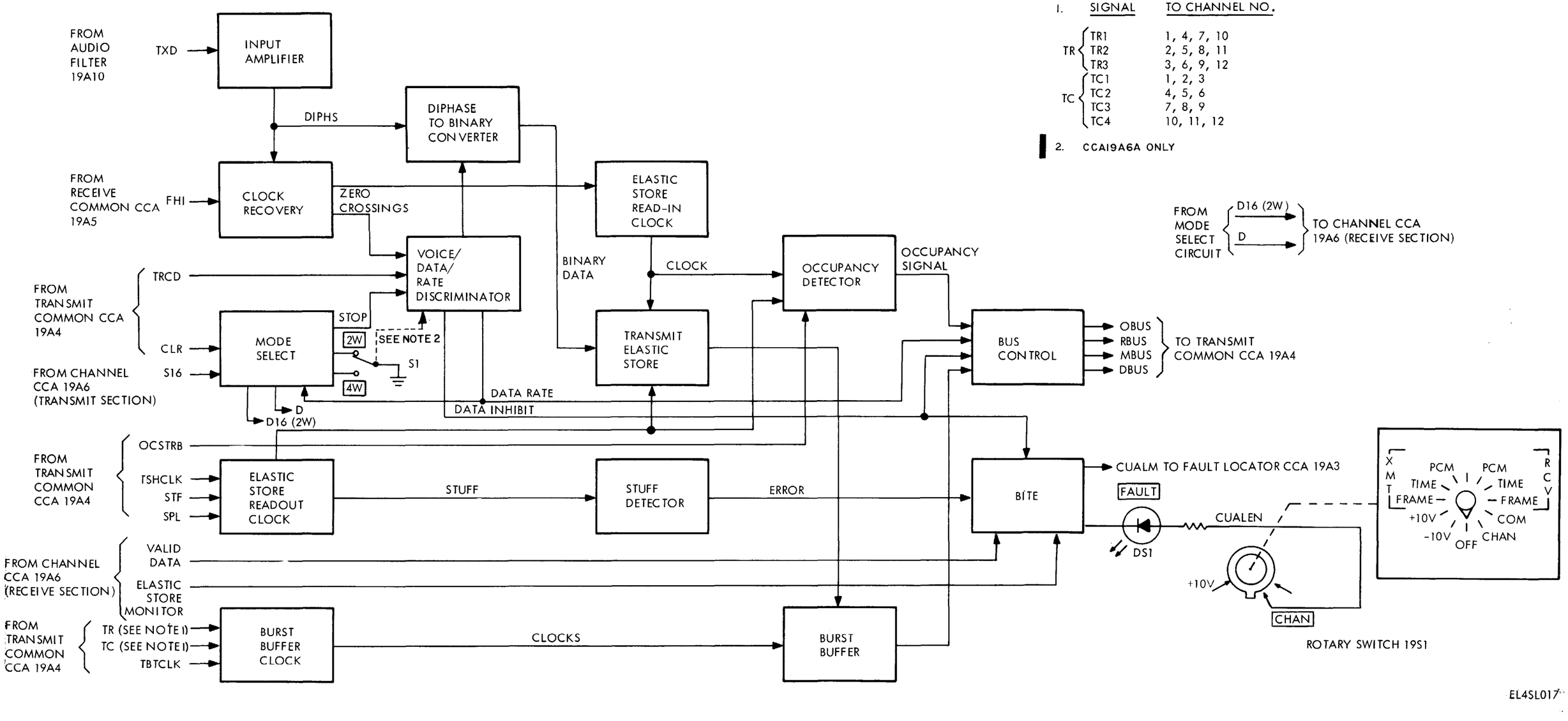
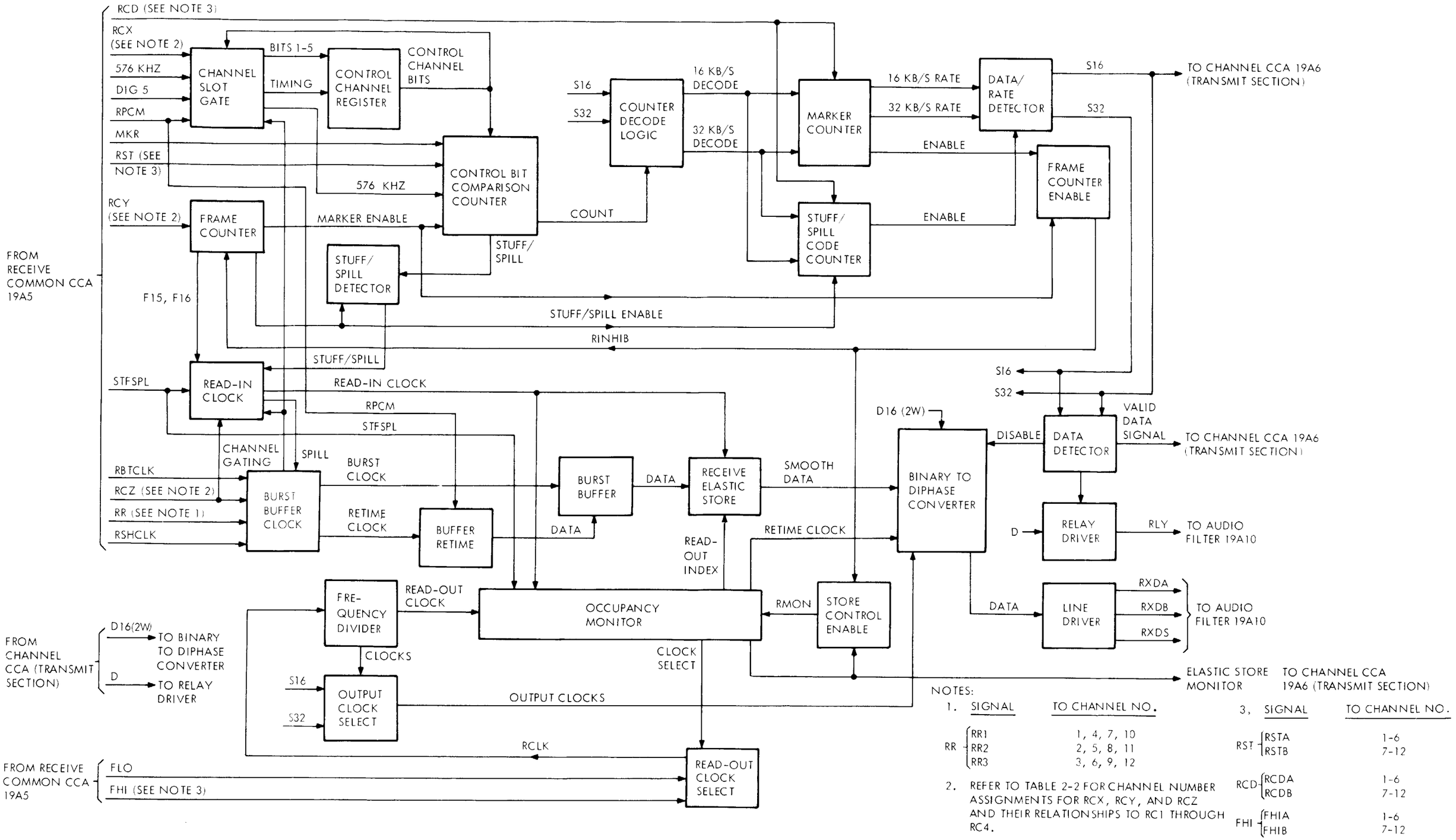


Figure FO-8. Channel CCA 1GA6 and CC19A6A (transmit section), functional block diagram.

CHANGE 1



NOTES:

1.

SIGNAL		TO CHANNEL NO.
RR	RR1	1, 4, 7, 10
	RR2	2, 5, 8, 11
	RR3	3, 6, 9, 12

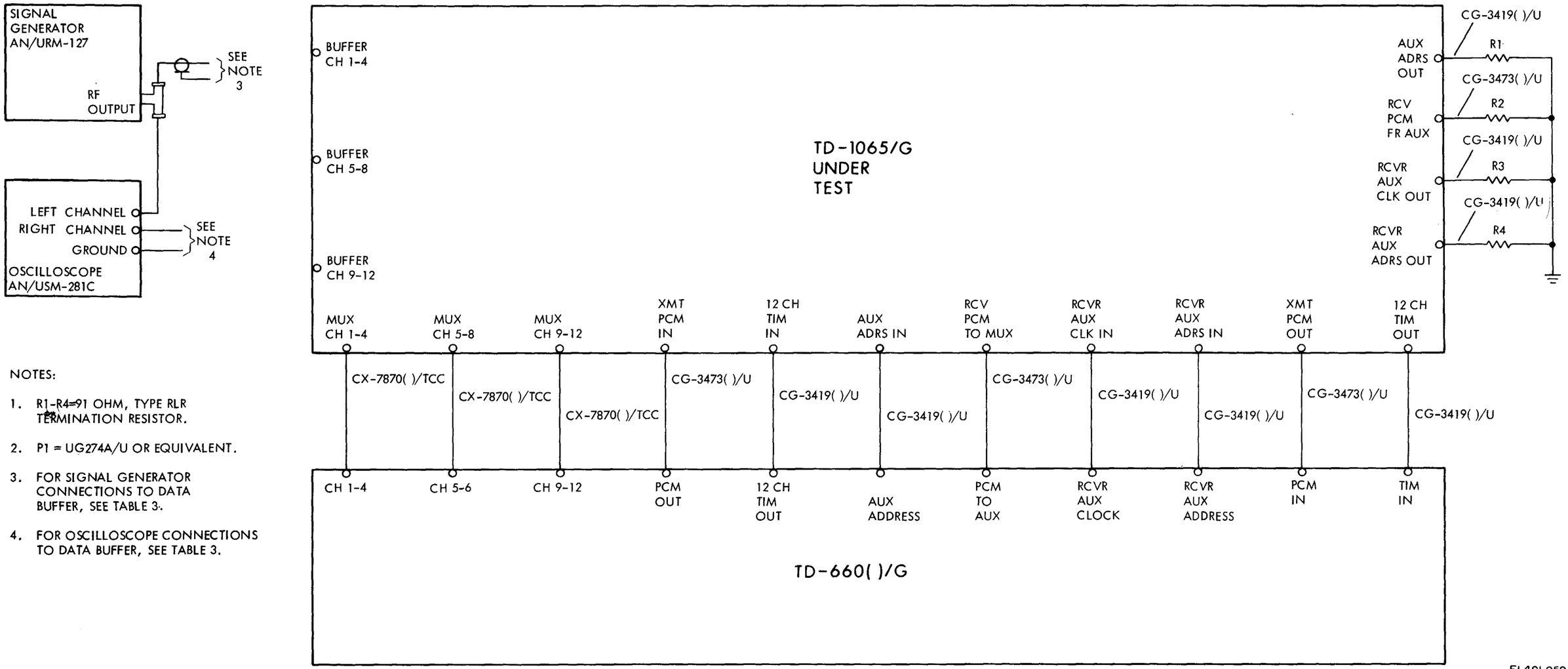
2. REFER TO TABLE 2-2 FOR CHANNEL NUMBER ASSIGNMENTS FOR RCX, RCY, AND RCZ AND THEIR RELATIONSHIPS TO RC1 THROUGH RC4.

3.

SIGNAL		TO CHANNEL NO.
RST	RSTA	1-6
	RSTB	7-12
RCD	RCDA	1-6
	RCDB	7-12
FHI	FHIA	1-6
	FHIB	7-12

EL4SL022

Figure FO-9. Channel CCA 19A6 (receive section), functional block diagram.

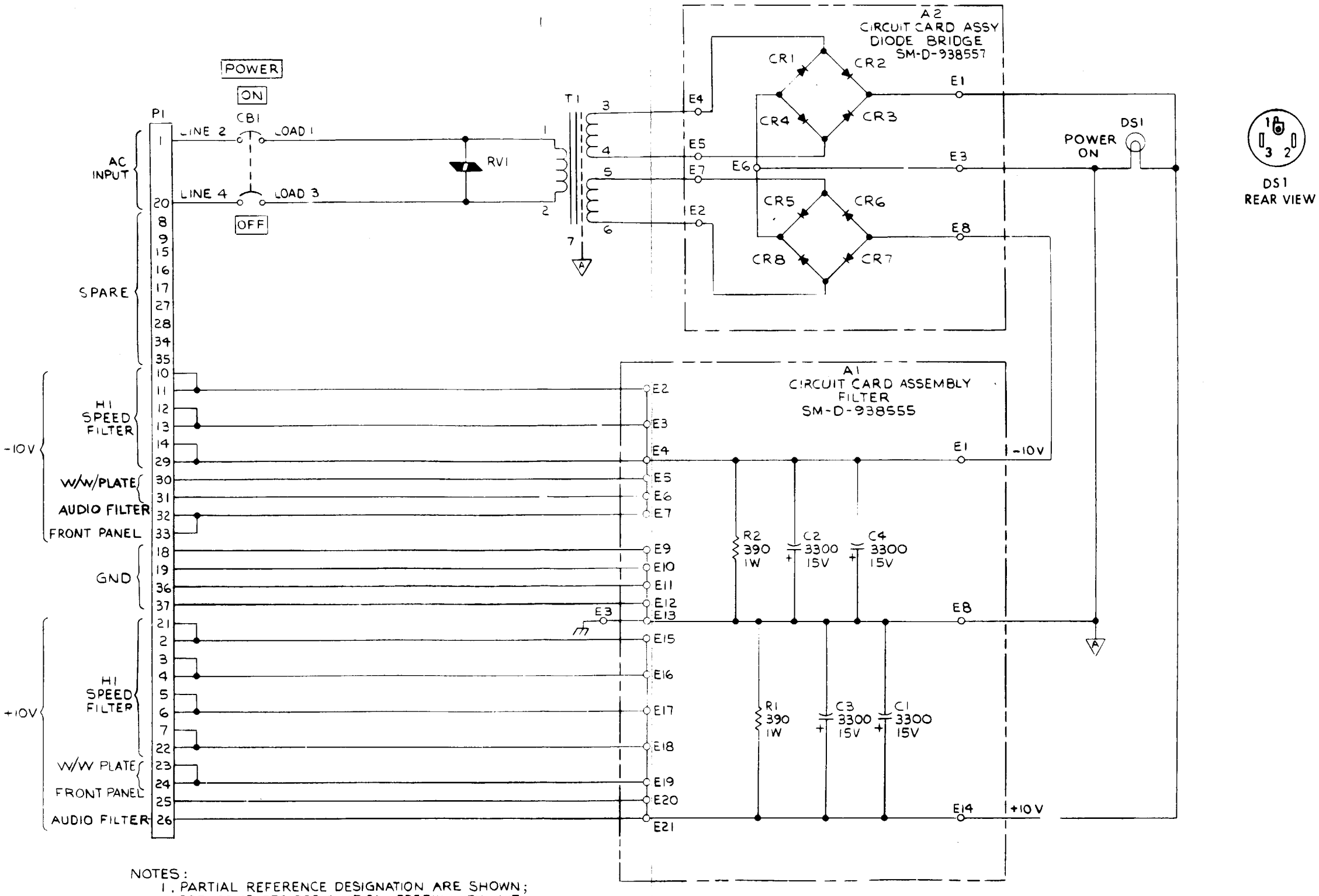


NOTES:

1. R1-R4=91 OHM, TYPE RLR TERMINATION RESISTOR.
2. P1 = UG274A/U OR EQUIVALENT.
3. FOR SIGNAL GENERATOR CONNECTIONS TO DATA BUFFER, SEE TABLE 3.
4. FOR OSCILLOSCOPE CONNECTIONS TO DATA BUFFER, SEE TABLE 3.

Figure FO-10. Data buffer, system test diagram.

EL4SL059

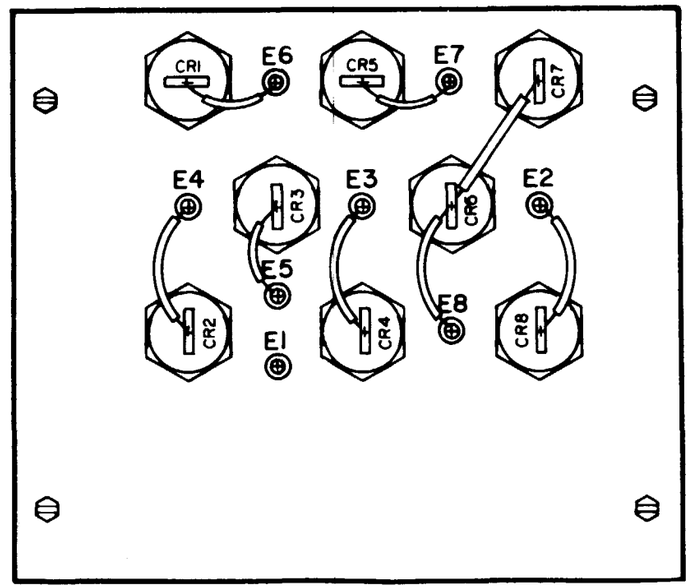


NOTES:
1. PARTIAL REFERENCE DESIGNATION ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED:
   A. RESISTANCE VALUES ARE IN OHMS
   B. CAPACITANCE VALUES ARE IN MICROFARADS
   C. ALL DIODES ARE IN1202A
   D. ALL VOLTAGES ARE DC
3. ▭ INDICATES FRONT PANEL MARKING

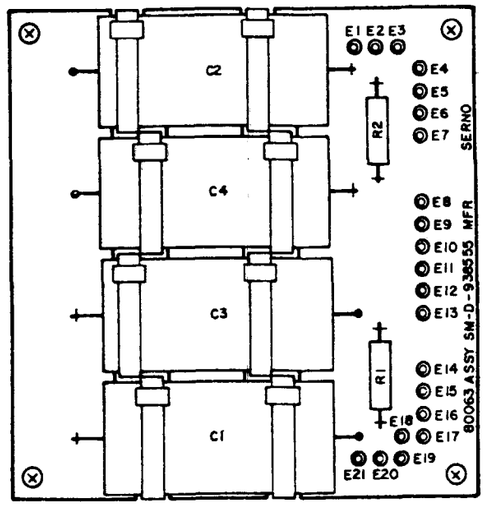
EL4SL003

Figure FO-11. Power supply 19A1, schematic diagram.

FROM	TO	COLOR	FROM	TO	COLOR
P1-1	CB1-2	BROWN	P1-27	NC	
P1-2	A1-E15	BROWN	P1-28	NC	
P1-3	A1-E16	RED	P1-29	A1-E4	GREEN
P1-4	A1-E16	ORANGE	P1-30	A1-E5	BLUE
P1-5	A1-E17	YELLOW	P1-31	A1-E6	VIOLET
P1-6	A1-E17	GREEN	P1-32	A1-E7	GREY
P1-7	A1-E18	BLUE	P1-33	A1-E8	WHITE
P1-8	NC		P1-34	NC	
P1-9	NC		P1-35	NC	
P1-10	A1-E2	BLACK	P1-36	A1-E11	GREEN
P1-11	A1-E2	BROWN	P1-37	A1-E12	BLACK
P1-12	A1-E3	RED	CB1-1	T1-1	GREY
P1-13	A1-E4	ORANGE	CB1-3	T1-2	WHITE
P1-14	A1-E4	YELLOW	T1-3	A2-E4	GREEN
P1-15	NC		T1-4	A2-E5	YELLOW
P1-16	NC		T1-5	A2-E7	ORANGE
P1-17	NC		T1-6	A2-E2	RED
P1-18	A1-E9	ORANGE	T1-7	A1-E3	BLACK
P1-19	A1-E10	YELLOW	A1-E3	A1-E13	BLACK
P1-20	CB1-4	RED	A2-E1	A1-E14	GREY
P1-21	A1-E15	BLACK	A2-E1	XDS1-2	VIOLET
P1-22	A1-E18	VIOLET	A2-E3	A1-E8	BROWN
P1-23	A1-E19	GREY	A2-E3	XDS1-1	BLUE
P1-24	A1-E19	WHITE	A2-E8	A1-E1	BLACK
P1-25	A1-E20	BLACK			
P1-26	A1-E21	WHITE			



Wiring connections on rear of diode bridge CCA, not listed in wiring table at left, are shown above. All wires are white.



EL4SL052

Figure FO-12. Power supply 19A1, wiring diagram.

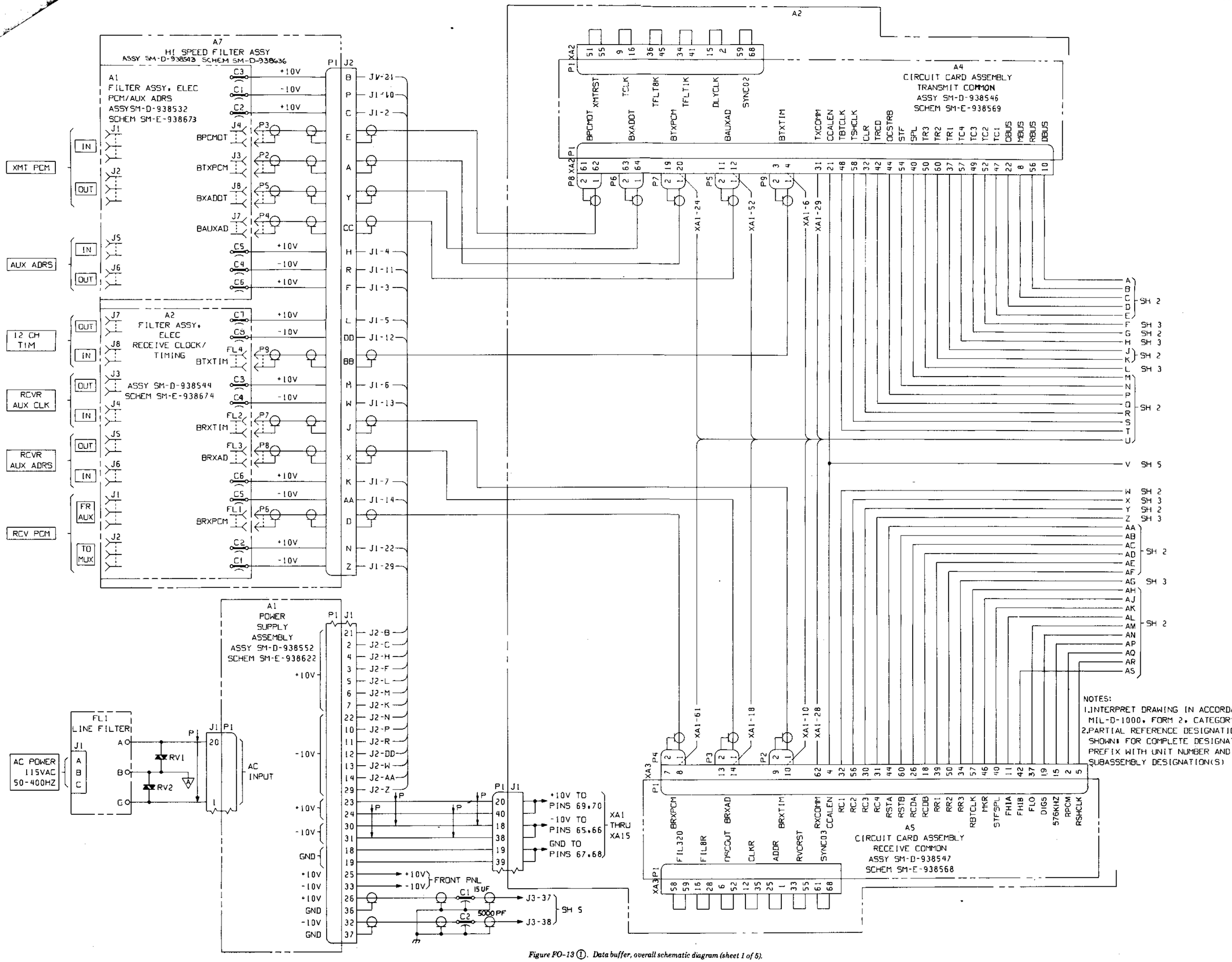


Figure FO-13 (1). Data buffer, overall schematic diagram (sheet 1 of 5).

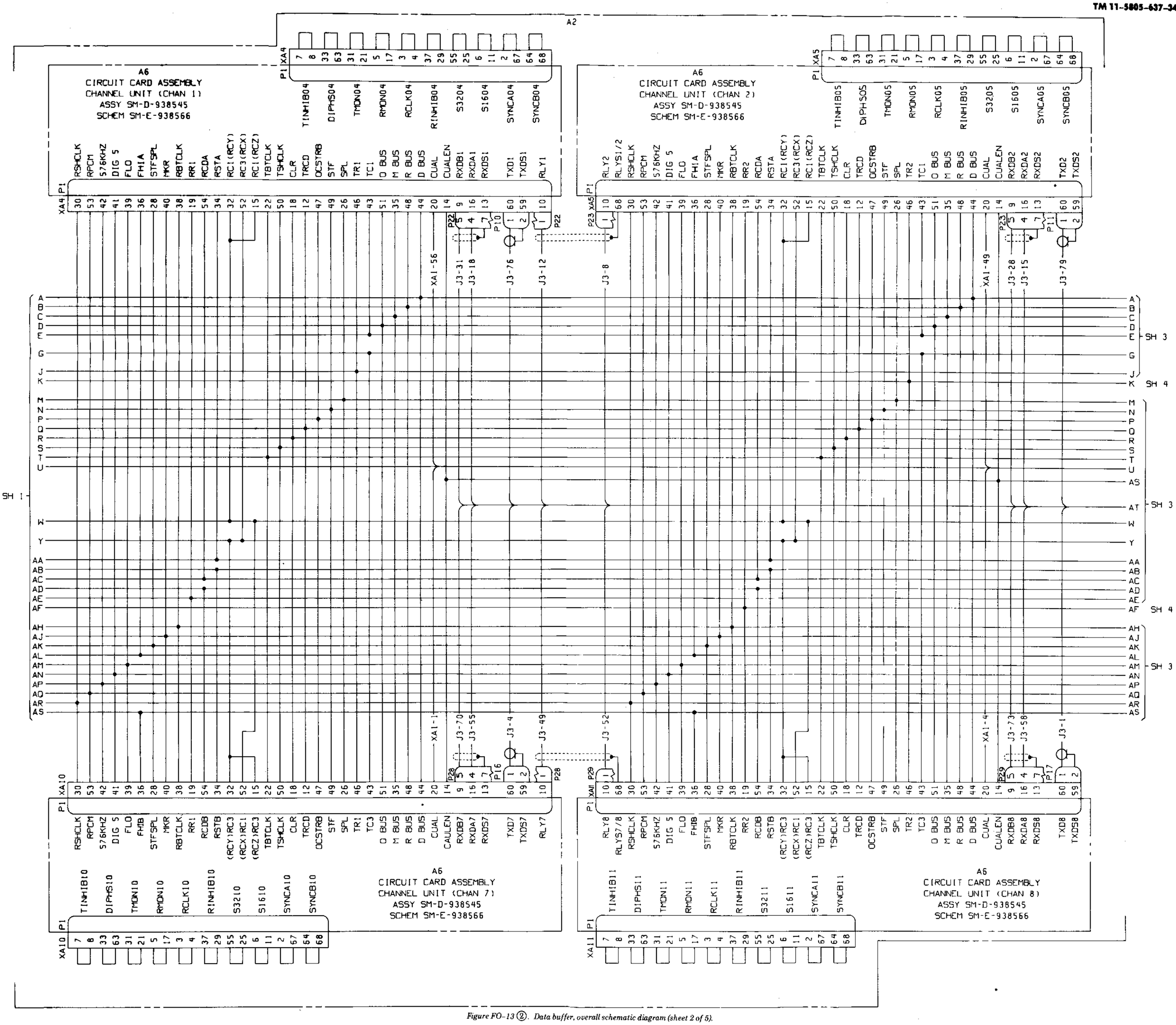


Figure FO-13 (2). Data buffer, overall schematic diagram (sheet 2 of 5).

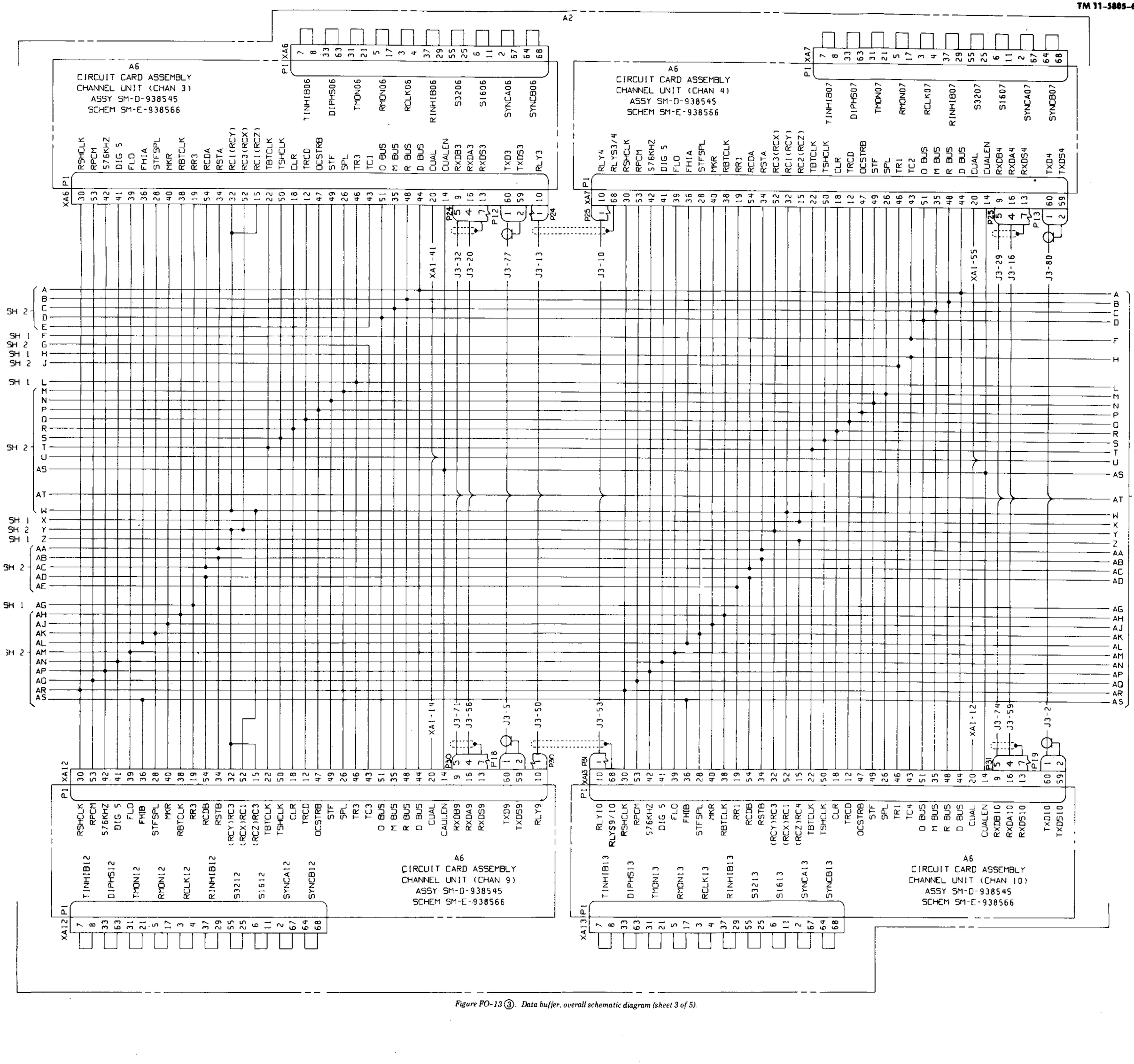


Figure FO-13 (3). Data buffer, overall schematic diagram (sheet 3 of 5).

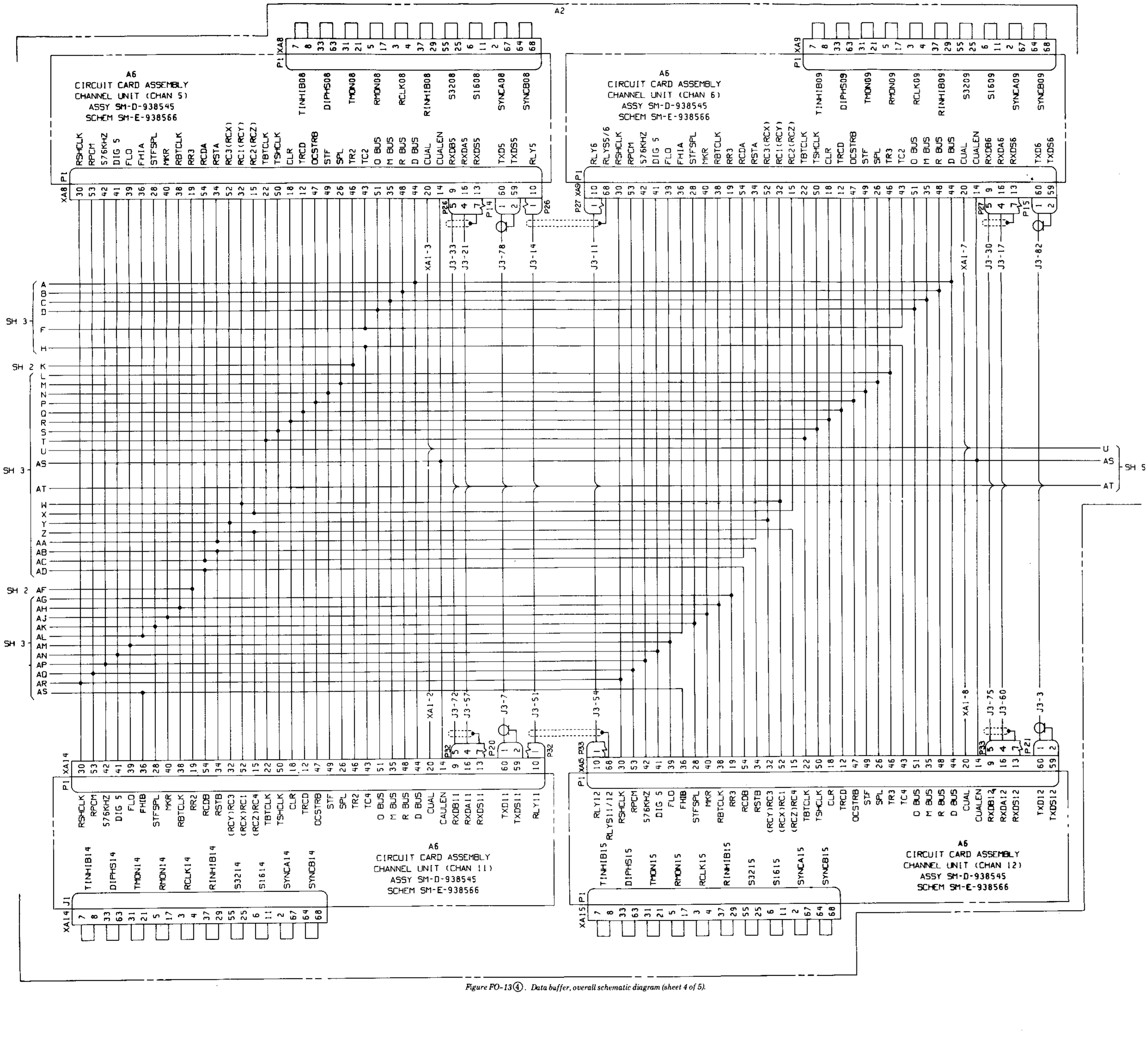


Figure FO-13④. Data buffer, overall schematic diagram (sheet 4 of 5).

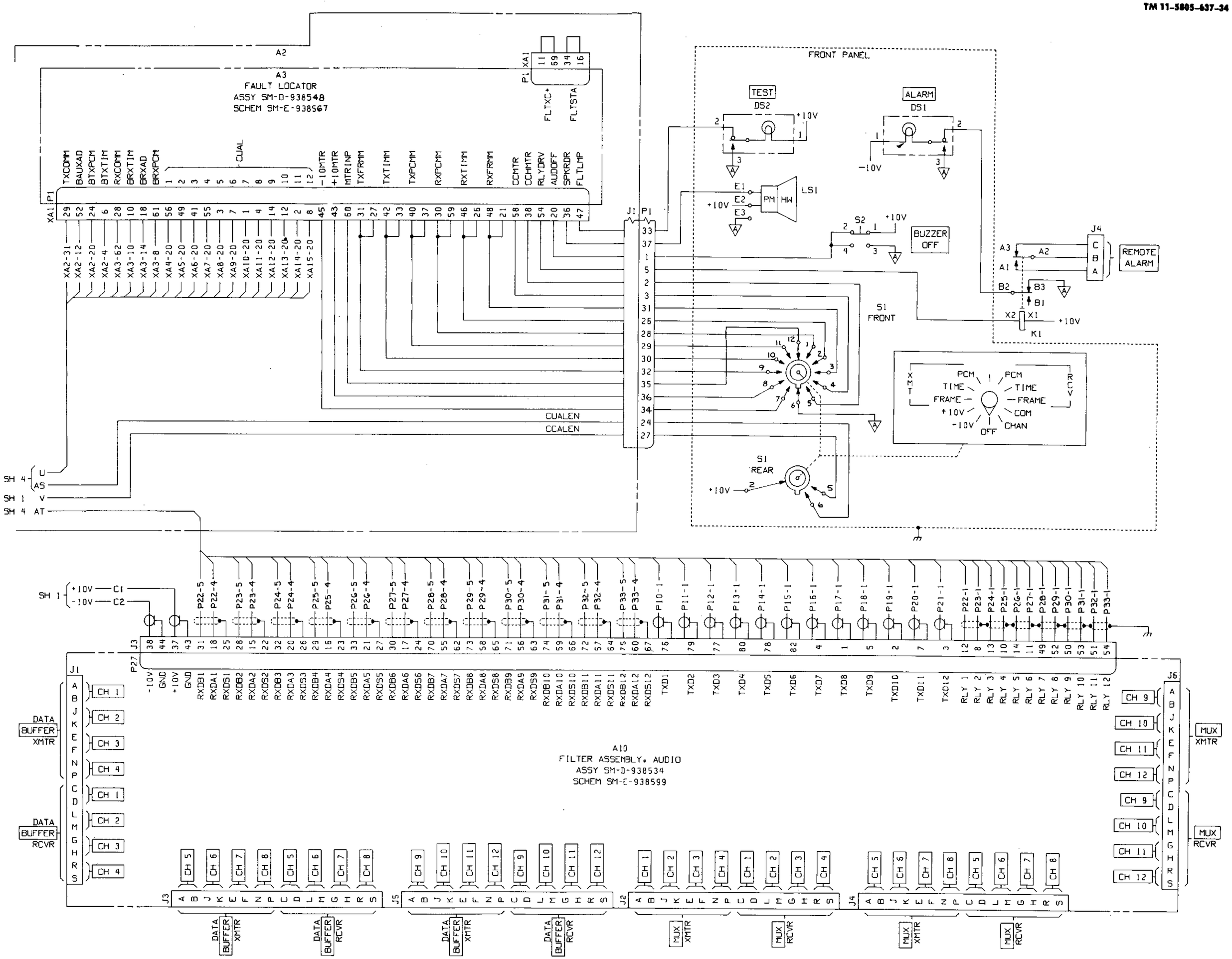
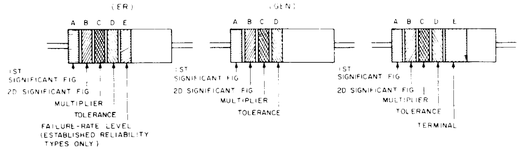


Figure FO-13⑤. Data buffer, overall schematic diagram (sheet 5 of 5).



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE. (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1½ TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

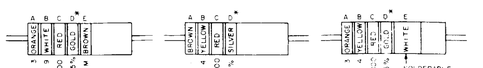
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS. (THESE ARE NOT COLOR CODED.)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA-NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND TYPE RESISTORS, COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

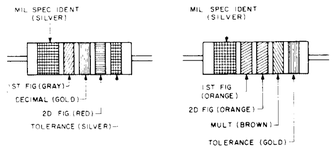
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



(A) 8.2UH ± 10% (B) 330UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED.

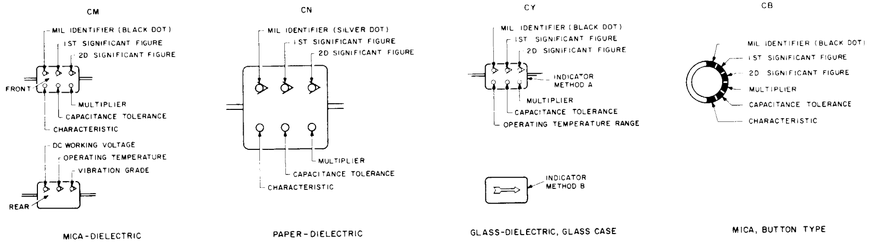
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES

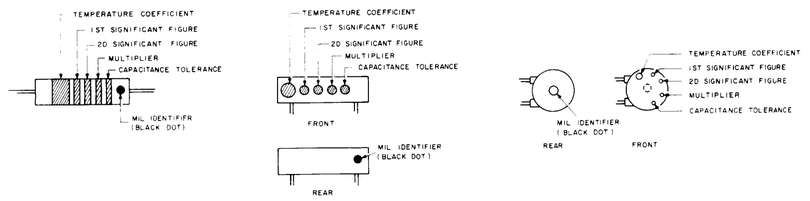
COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.





C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE				CHARACTERISTIC			DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY, CB	0	0	1			±20%	±20%		A			−55°TO+70°C	10-55HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				−55°TO+85°C	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				−55°TO+125°C	10-2,000HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										−55°TO+150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	−30	1	1	10	±1%		
RED	−80	2	2	100	±2%	±0.25 UUF	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		±5%	±0.5 UUF	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.

2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS. MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.

3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.

4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

Figure FO-14. Standard color coding chart.

By Order of the Secretary of the Army:

E. C. MEYER
General, United States Army
Chief of Staff

Official:

J. C. PENNINGTON
Major General, United States Army
The Adjutant General

DISTRIBUTION:
Active Army:
HISA (Ft Monmouth) (21)
USAINSCOM (2)
COE(l)
TSG(l)
USAARENBD (1)
DARCOM (1)
TRADOC (2)
OS Maj Comd (4)
TECOM (2)
USACC (4)
MDW(l)
Armies (2)
Corps (2)
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USASIGS (5)
USAADS (2)
USAFAS (2)
USAARMS (2)
USAIS (2)
USAES (2)
USAICS (3)
MAAG (1)
USARMIS (1)
USAERDAA (1)
USAERDAW (l)
Fort Gordon (10)
Fort Carson (5)
Army Dep (1) except
SAAD (30)
TOAD (14)
SHAD (2)
Fort Gillem (10)
USA Dep (1)
Sig Sec USA Dep (1)
Fort Richardson (CERCOM Ofc) (2)
Units org under fol TOE:
(2 copies each unit)
29-207
29-610
ARNG: None
USAR: None
For explanation of abbreviations used, see AR 310-50.

* U.S. GOVERNMENT PRINTING OFFICE: 1990 - 261-872 (20847)

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

SOMETHING WRONG WITH THIS PUBLICATION?

FROM (PRINT YOUR UNIT'S COMPLETE ADDRESS)
Commander
Stateside Army Depot
ATTN: AMSTA-US
Stateside, N.J. 07703

DATE SENT
10 July 1975

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/PRC-76

BE EXACT PIN-POINT WHERE IT IS

PAGE NO	PARAGRAPH	FIGURE NO	TABLE NO	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure the the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		FO3		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER
SSG I. M. DeSpiritof 999-1776

SIGN HERE
I. M. DeSpiritof

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DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5805-637-34	16 Apr 81	DS/GS Maintenance Manual for Data Buffer TD-1065/G

BE EXACT PIN-POINT WHERE IT IS

PAGE NO	PARAGRAPH	FIGURE NO	TABLE NO

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

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THE METRIC SYSTEM AND EQUIVALENTS

'NEAR MEASURE

. Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

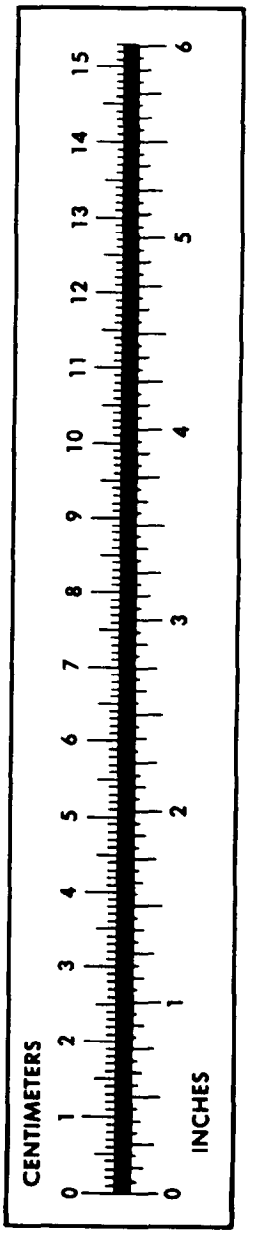
TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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