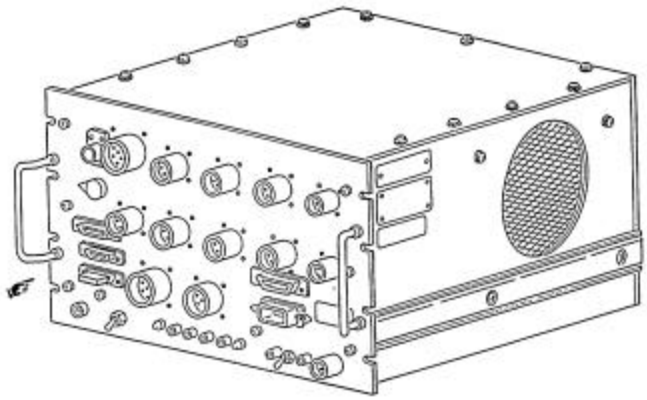
TECHNICAL MANUAL

OPERATOR' S, ORGANIZATIONAL,

AND DIRECT SUPPORT

MAINTENANCE MANUAL



INTERFACE UNIT TEST SET TS-4221/U
(NSN 6625-01-323-3125) (EIC: N/A)

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HEADQUARTERS, DEPARTMENT OF THE ARMY

15 MARCH 1992

Change
No. 1

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 1 March 1997

Operator's, Unit, And Direct Support Maintenance Manual

INTERFACE UNIT TEST SET TS-4221/U
(NSN 6625-01-323-3125) (EIC: N/A)

TM 11-6625-3150-13, 15 March 1992, is changed as follows:

1. Remove old pages and insert new pages as indicated below. New or changed material is indicated by a vertical bar in the margin of the page. Added or revised illustrations are indicated by miniature pointing hands

Remove Pages	*Insert Pages*
A and B	A and B
1-0	1-0
1-3 through 1-12	1-3 through 1-12
None	1-12.1 and 1-12.2
1-13 and 1-14	1-13 and 1-14
1-63 through 1-66	1-63 through 1-66
2-1 and 2-2	2-1 and 2-2
4-3 through 4-8	4-3 through 4-8
4-9/(4-10 blank)	4-9/(4-10 blank)
5-1 through 5-4	5-1 through 5-4
None	5-4.1 and 5-4.2
5-5 and 5-6	5-5 and 5-6
5-17 and 5-18	5-17 and 5-18
5-23 through 5-36	5-23 through 5-36
5-41 and 5-42	(5-41 blank)/5-42
5-43 through 5-52	5-43 through 5-52
B-1 through B-8	B-1 through B-7/(B-8 blank)
FO-1 (Sheet 1 of 2)	FO-1 (Sheet 1 of 2)
FO-1 (Sheet 2 of 2)	FO-1 (Sheet 2 of 2)
FO-2	FO-2
None	FO-17
Cover	Cover

2. File this change sheet in front of the publication for reference purposes.

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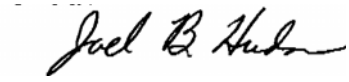


JOEL B. HUDSON
Administrative Assistant to the
Secretary of the Army
04314

DISTRIBUTION:

To be distributed in accordance with the initial distribution number (IDN) 369224 requirements for TM 11-6625-3150-13.

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER
3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL
4. SEND FOR HELP AS SOON AS POSSIBLE
5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

SAFETY SUMMARY

WARNING

- **Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required (para 5-13, 5-14, 5-15, 5-19, 5-20 and 5-21).**
- **Zinc chromate dust primer is highly toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate (para 5-22).**
- **Isopropyl alcohol is flammable and moderately toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate (para 5-22).**
- **Set POWER ON/OFF switch to OFF, unplug ac power cord, before removing fuse cover to prevent electrical shock (para 4-9).**
- **When lifting or handling heavy objects, use two people to prevent possible back injury (para 5-8, 5-16).**
- **Capacitors hold voltages after power is removed. Ground C1 before working inside IUTS to prevent injury to personnel (para 5- 8, 5-11, 5-16).**

HOW TO USE THIS MANUAL

1. **HOW DO I FIND INFORMATION?** To help you locate information, this manual has three types of indexes.

   a. Front Cover. Use front cover index and black tabs at the edge of pages to quickly find the chapters or this manual shown on the cover.

   b. Table of Contents. Entries within the main table of contents duplicate the entries on the front cover and are highlighted. This is in case the cover is torn off or soiled beyond legibility.

   c. Chapter Indexes. These indexes are located in the front of each chapter. The listings are in the order of appearance.

2. **HOW DO I BECOME FAMILIAR WITH THE EQUIPMENT?** See chapter 1 for physical and functional descriptions.

3. **DOES THE MANUAL CONTAIN OPERATOR INSTRUCTIONS?** See chapter 2 and 3.

4. **WHAT IS THE EXTENT OF ORGANIZATIONAL MAINTENANCE?** See chapter 4. Normally, organizational maintenance is limited to quarterly preventive maintenance checks and services and replacement of defective line replaceable units (LRUs).

5. **WHERE IS DIRECT SUPPORT MAINTENANCE COVERED?** See chapter 5.

6. **ARE OTHER MANUALS REQUIRED?** Refer to appendix A for a list. Obtain these manuals through supply channels.

7. **WHAT TOOLS AND EQUIPMENT ARE REQUIRED?** Turn to appendix B (Maintenance Allocation) for a listing.

8. **HOW DO I GET SPARE PARTS?** Refer to paragraph 4-3 and 5-3.

9. **WHAT ACTIONS ARE TAKEN IF MISTAKES ARE FOUND IN THE MANUAL?** See the block on the table of contents and paragraph 1-3 for procedures.

HOW TO USE THIS MANUAL - Continued

10. **DO I NEED TO KNOW ANY SPECIAL SAFETY INSTRUCTIONS?** Ensure you understand the information on page A and B before you operate or maintain the equipment.

11. **WHAT OTHER FEATURES SHOULD I KNOW ABOUT THIS MANUAL?** You should know the use of NOTES, CAUTIONS, AND WARNINGS. Definitions are:

NOTE

An essential operating or maintenance procedure, caution, or statement which must be highlighted.

CAUTION

An operating or maintenance procedure, practice, condition, statement, etc., which, if not strictly observed, could result in damage to, or destruction of, equipment or loss of mission effectiveness or long term health hazards to personnel.

WARNING

An operating or maintenance procedure, practice, condition, statement, etc., which, if not strictly observed, could result in INJURY to or DEATH of personnel.

Technical Manual

No. 11-6625-3150-13

HEADQUARTERS,
DEPARTMENT OF THE ARMY
Washington, DC 15 March 1992

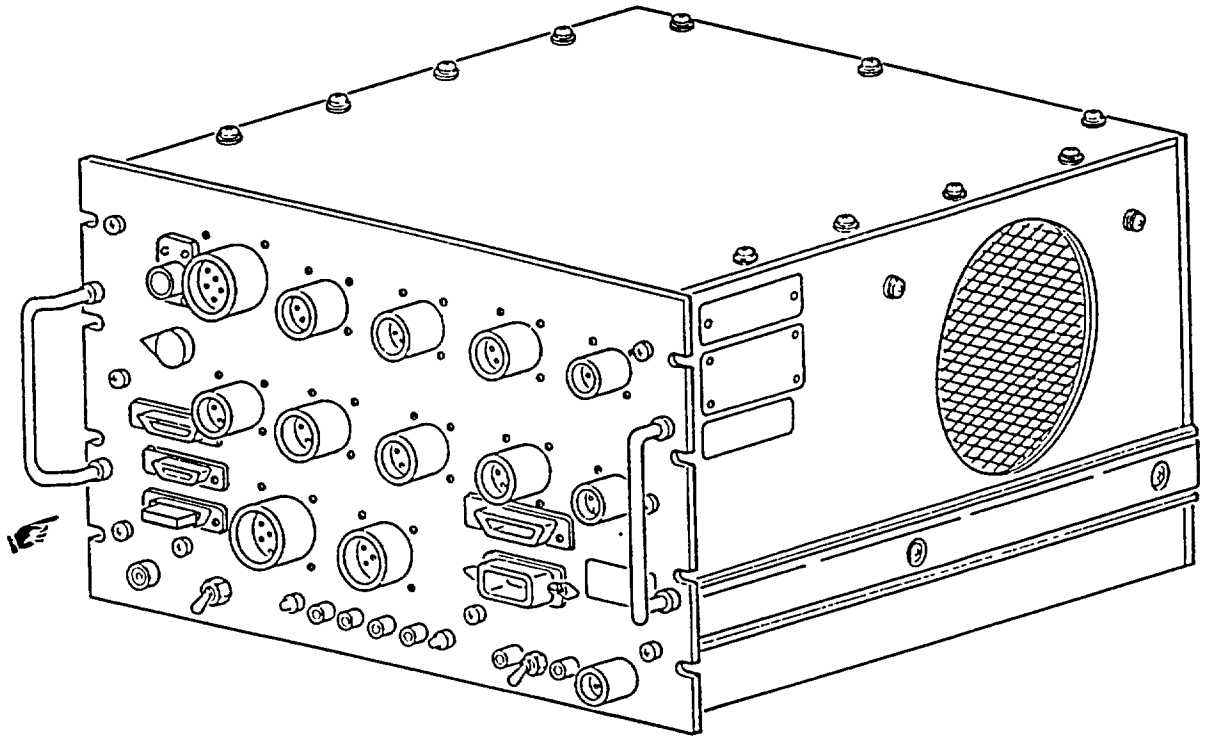
OPERATOR'S, ORGANIZATIONAL, AND DIRECT SUPPORT MAINTENANCE MANUAL
TEST SET, INTERFACE UNIT TS-4221/U
(NSN 6625-01-323-3125) (EIC: N/A)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms) or DA Form 20282 located in back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-LM-LT, Fort Monmouth, New Jersey 07703-5007.

In either case a reply will be furnished direct to you.

Page



INTERFACE UNIT TEST SET
TS-4221/U

CHAPTER 1

INTRODUCTION

CHAPTER CONTENTS **Page**

Section I. Introduction

1-1. SCOPE

Type of Manual: Operator's, Organizational, and Direct Support Maintenance

Model Number and Equipment Name: TS-4221/U - Interface Unit Test Set

Purpose of Equipment: Used to test the interface unit (IU), computer processor (CP), and receiver, digital control (RDC).

1-2. MAINTENANCE FORMS, RECORDS, AND REPORTS

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750, as contained in Maintenance Management Update.

b. Reporting of Item and Packaging Discrepancies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/ SECNAVINST 4355. 18/AFR 400-54/MCO 4430.3J.

1-2. MAINTENANCE FORMS, RECORDS, AND REPORTS - Continued

c. Transportation Discrepancy Report (TDR) (SF 361). Fill out and forward Transportation Discrepancy Report (TDR) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1-3. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR)

If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design or performance. Put it on an SF 368 (Product Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ED-PH, Fort Monmouth, New Jersey 07703-5007. We'll send you a reply.

1-4. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS

Refer to the latest issue of DA Pam 25-30 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

1-5. ADMINISTRATIVE STORAGE

Administrative storage of equipment issued to and used by Army activities will have Preventive Maintenance Checks and Services (PMCS) performed before storing. When removing the equipment from administrative storage, the PMCS checks should be performed to assure operational readiness.

1-6. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR)

If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design or performance. Put it on an SF 368 (Product Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ED-PH, Fort Monmouth, New Jersey 07703-5007. We'll send you a reply.

1-7. REFERENCE INFORMATION

This listing includes the nomenclature cross reference list and list of abbreviations used in this manual.

a. Nomenclature Cross Reference List

Common Name	Official Nomenclature
Computer processor (CP)	Computer Processor CP-1692/U
Frequency synthesizer (FS)	Frequency Synthesizer O-1833/U
IF processor (IFP)	Intermediate Frequency Processor CV-4008/U

1-7. REFERENCE INFORMATION - Continued

Common Name	Official Nomenclature
IF switch (IFS)	Intermediate Frequency Switch SA-2542/U
Interface unit (IU)	Interface Unit J-4522/U
Interface unit test set (IUTS)	Interface Unit Test Set TS-4221/U
NAV Set	Carousel IV-E High-Accuracy Inertial Navigation System
Operator terminal	Alphanumeric Display Station HP2645A
Radio frequency antenna (RFA)	Radio Frequency Antenna AS-3901/U
Receiver digital control (RDC)	Control, Receiver C- 11634/U
Receiver PS	Power Supply-Receiver PP- 8184/U
System PS	Power Supply PP-8158/U
Wide band data link	Interoperable Airborne Data Link
Oscillator (OSC) (G1)	Assy, Oscillator Rubidium (G1)
Tick generator (A2)	CCA, Tick Generator (A2) (C5090411)
Computer processor interface (CPIF) (A3)	CCA, Computer Processor Interface (A3) (C5116808)
Computer processor simulator (CP SIM) (A4)	CCA, Computer Processor Simulator (A4) (C5117002)
Test set digital/analog (TSD/A) (A5) (A6)	CCA, Test Set Digital/Analog (A5) (A6) (C5117012)
Test set, IF processor (TSIFP) (A7)	CCA, Test Set IF Processor (A7) (C5117017)
Test set local oscillator (TSLO) (A8)	CCA, Test Set, Local Oscillator (AS) (C5117022)
Test set radio frequency (TSRF) (A9)	CCA, Test Set Radio Frequency (A9) (C5117027)
1553B interface (1553B IF) (A10)	CCA, 1553B Interface (A10) (SM-D-873904)
IU data link (IUDL) (A11)	CCA, Interface Unit Data Link (A11) (SM-D-873900)
IU navigation (IUNAV) (A12)	CCA, Interface Unit Navigation (A12) (SM-D-873908)
Test set bus (TSBUS) (A13)	CCA, Test Set Bus (A13) (C5117007)
Dual bus processor (DBP) (A14)	CCA, Dual Bus Processor (A 14) (C5116888)

1-7. REFERENCE INFORMATION - Continued

Programmable static random-access memory (PSRAM) (A15)	CCA, Programmable Static Random-Access Memory (A15) (C5117032)
Power supply (A17)	Power Supply (A17) (C5118502)

b. List of Abbreviations.

CP	Computer processor
FIFO	first-in-first out memory
FS	Frequency synthesizer
GPIB	general purpose interface bus
GPS	global positioning satellite
IFP	IF processor
IFS	IF switch
IU	Interface unit
IUTS	Interface unit test set
LO	local oscillator
MHz z	Megahertz
PGC	Pulse generator control
RFA	Radio frequency antenna
RDC	Receiver digital control
ROM	Read-only memory
Osc	Oscillator (G1)
CPIF	computer processor interface (A3)
CP SIM	computer processor simulator (A4)
TSD/A	Test Set D/A (A5) (A6)
TSIFP	Test Set IF Processor (A7)
TSLO	Test set local oscillator (A8)
TSRF	Test set radio frequency (A9)
TTL	Transistor-transistor logic
UTIC	Universal time interval counter
1553B	1553B interface (A10)
IUDL	IU data link (A11)
IUNAV	IU navigation (A12)
TSBUS	Test set bus (A13)
DBP	Dual bus processor (A14)
PSRAM	Programmable static random-access memory (A15)

1-8. SAFETY, CARE, AND HANDLING

a. Safety. For artificial respiration, refer to FM -21-11. When lifting or handling heavy objects, use two persons to prevent possible back injury.

b. Care. Do not use the equipment as a step or a seat.

c. Handling. Do not drop the equipment or turn it over roughly. Avoid damage to connectors.

SECTION II. EQUIPMENT DESCRIPTION

1-9. CHARACTERISTICS, CAPABILITIES, FEATURES

CHARACTERISTICS

- MODULAR CONSTRUCTION
- OPERATES ON STANDARD AC LINE VOLTAGE
- DESIGNED FOR RACK OR BENCH MOUNTING

CAPABILITIES

- SIMULATES ANALOG IF PROCESSOR (IFP) OUTPUT SIGNALS TO TEST INTERFACE UNIT (IU)
- SIMULATES THE FOLLOWING DIGITAL OUTPUTS:
  - IU DATA TO TEST COMPUTER PROCESSOR (CP)
  - FREQUENCY SYNTHESIZER (FS) AND RADIO FREQUENCY ANTENNA (RFA) DATA TO TEST RECEIVER DIGITAL CONTROL (RDC)
  - CP, NAV SET, AND WIDE BAND DATA LINK DATA TO TEST IU

FEATURES

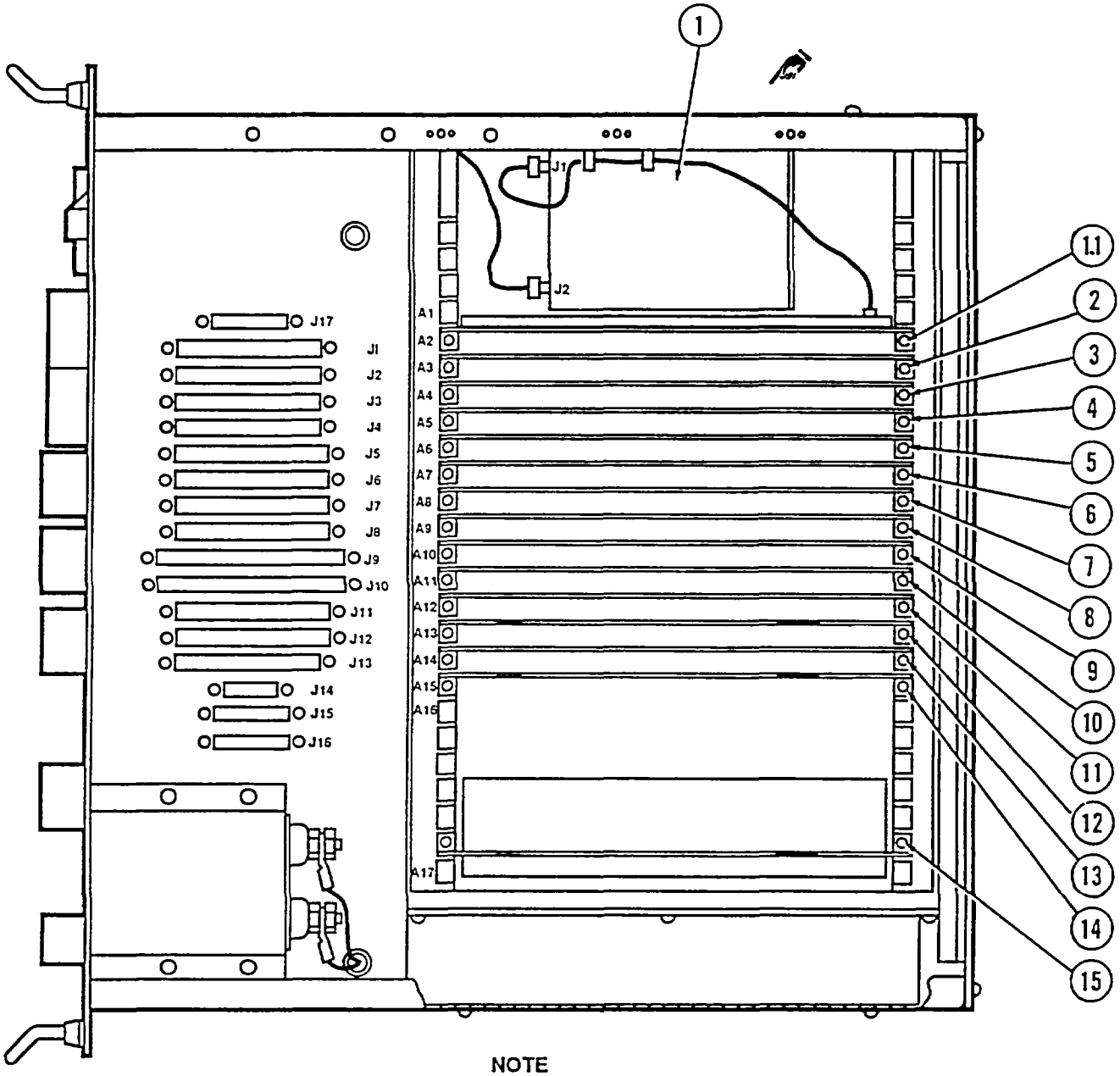
- REQUIRES OPERATOR INTERFACE DEVICE (OPERATOR TERMINAL)
- FRONT PANEL INTERFACE FOR OPERATOR TERMINAL OR OTHER PERIPHERAL DEVICES
- COMPLETE, SELECTABLE, INTERNALLY STORED TEST PROGRAMS FOR IU, CP, AND RDC
- DIAGNOSTIC PROGRAM LOAD SELECTION VIA SINGLE FRONT PANEL SWITCH
- BUILT-IN COOLING FAN
- COMPLETE TEST CABLE SET

1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS

a. Internal Components.

(1)	OSCILLATOR (61).	High accuracy clock
(1.1)	TICK GENERATOR (A2).	Simulates global positioning satellite (GPS) time tick
(2)	COMPUTER PROCESSOR INTERFACE (CPIF) (A3).	Simulates data from IU
(3)	COMPUTER PROCESSOR SIMULATOR (CP SIM) (A4).	Simulates CP outputs
(4)	TEST SET DIGITAL/ANALOG (TSD/A) (A5).	Simulates IFP outputs
(5)	TEST SET DIGITAL/ANALOG (TSD/A) (A6).	Simulates IFP outputs
(6)	TEST SET IF PROCESSOR (TSIFP) (A7).	Simulates IFP and trigger outputs
(7)	TEST SET LOCAL OSCILLATOR (TSLO) (A8).	Simulates FS outputs
(8)	TEST SET RADIO FREQUENCY (TSRF) (A9).	Simulates RFA outputs
(9)	1553B INTERFACE (1553B IF) (A10).	Supports 1553B bus operation
(10)	INTERFACE UNIT DATA LINK (IUDL) (All).	Provides high-speed serial channel and self test loop-back
(11)	INTERFACE UNIT NAVIGATION (IUNAV) (A12).	Simulates navigation data
(12)	TEST SET BUS (TSBUS) (A13).	Provides GPIB. Provides spare RS-232C channels, interrupts, and timers
(13)	DUAL BUS PROCESSOR (DBP) (A14).	8086 microprocessor which controls functions and testing of LRUs
(14)	PROGRAMMABLE STATIC RANDOM-ACCESS MEMORY (PSRAM) (A15).	Stores operating and diagnostic programs
(15)	POWER SUPPLY (A17).	Supplies and distributes power

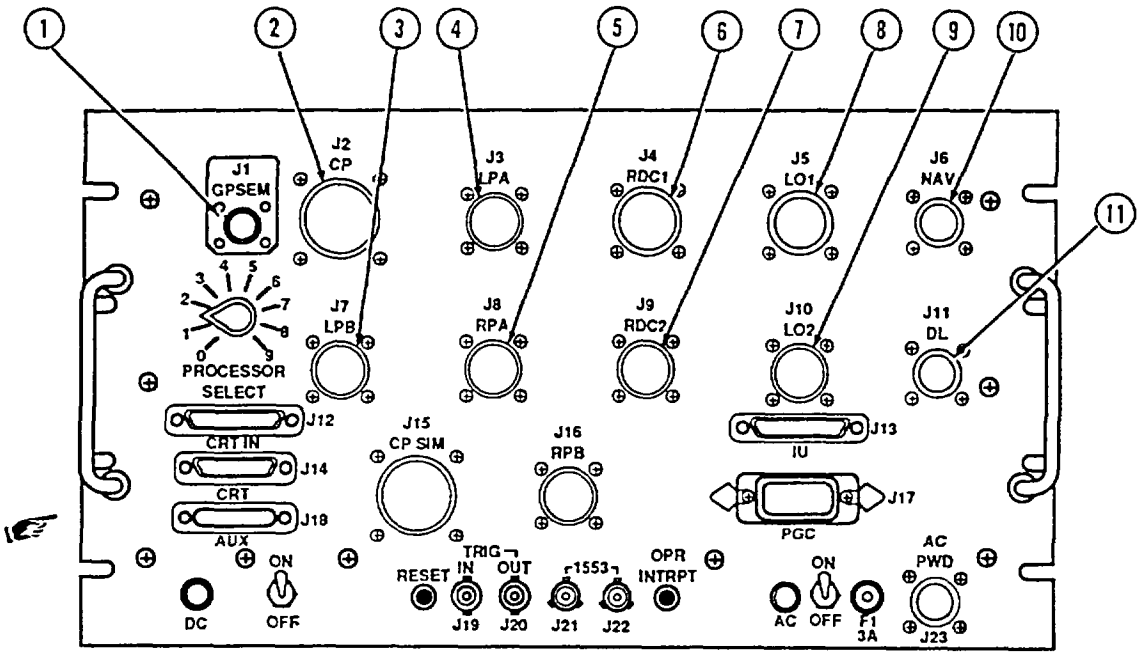
1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS - Continued



NOTE
(CCA SLOTS A1, A16 NOT USED)

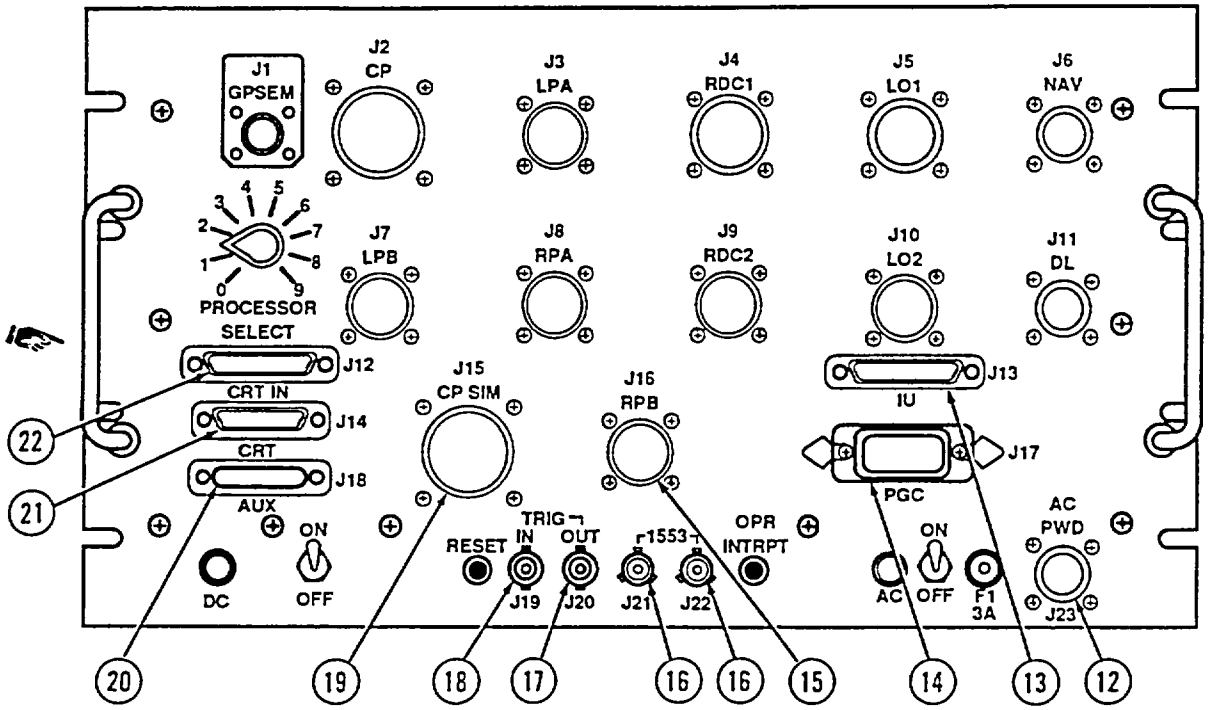
1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS - Continued

b. External Interfaces.



(1)	GPSEM (J1)	GPS output to test IU
(2)	CP (J2).	Data bus output to CP
(3)	LPB (J7).	Outputs simulated left pod quadrant B signals
(4)	LPA (J3).	Outputs simulated left pod quadrant A signals
(5)	RPA (J8).	Outputs simulated right pod quadrant A signals
(6)	RDC1 (J4).	Outputs simulated data signals to RDC1
(7)	RDC2 (J9).	Outputs simulated data signals to RDC2
(8)	L01 (J5).	Outputs simulated FS No. 1 signals
(9)	L02 (J10).	Outputs simulated FS No. 2 signals
(10)	NAY (06).	Outputs simulated navigation signals
(11)	DL (J11).	Outputs simulated data link outputs

1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS - Continued



(12) AC PWR (J23). AC power input

(13) IU (J13). I/O port to IU

(14) PGC (J17). Outputs control data to digital delay width generator

(15) RPB (J16). Outputs simulated right pod quadrant B signals

(16) 1553B (J21/J22). 1553B bus ports

(17) TRIG OUT (J20). Trigger output to digital delay width generator

(18) TRIG IN (J19). Trigger input from digital delay width generator

(19) CP SIM (J15). Outputs simulated CP data

(20) AUX (J18). I/O port to disk drive

(21) CRT (J14). Outputs data to CRT

(22) CRT IN (J12). I/O port to CP

1-11. EQUIPMENT DATA

a. **Physical**

Weight	45.00 lb (20.41 kg)
Height	10.50 in (26.67 cm)
Width	19.00 in (48.26 cm)
Length	17.00 in (43.18 cm)

b. **Functional**

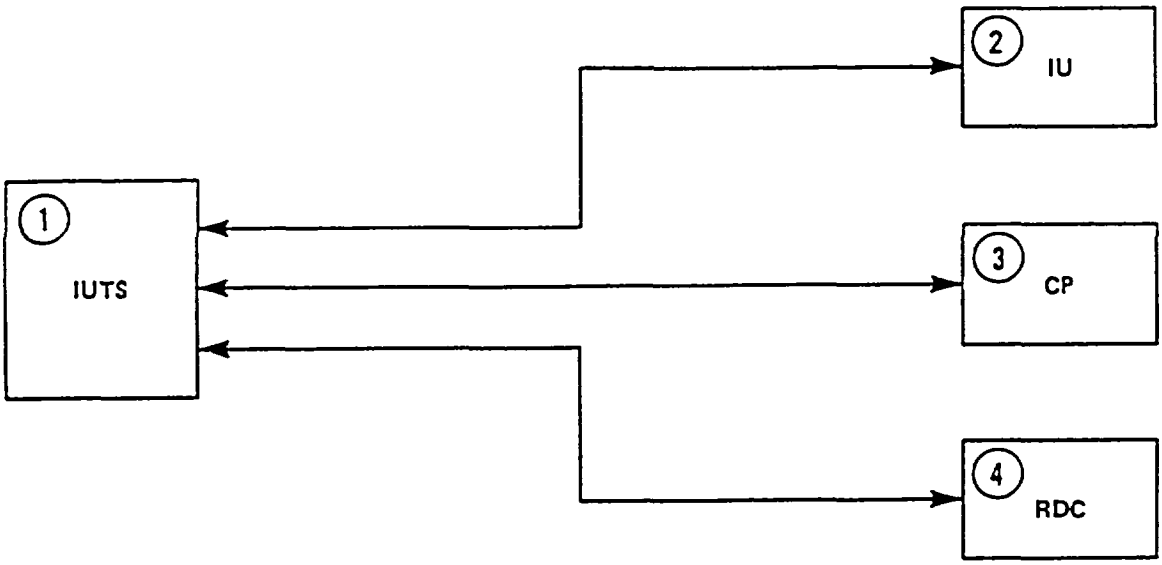
Input Power	115 Vac @ 2.0 amp + 28 Vdc @ 4.0 amp
Interface	
External	Interface unit Computer processor Receiver digital control
Internal	BUS1 and BUS2
Input	Control signals and data
Output	Simulation signals and data

c. **Environmental**

Temperature	
Operating	+ 32 degrees F (0 degrees C) to -109 degrees F (+43 degrees C)
Non-operating	- 61 degrees F (-51 degrees C) to +154 degrees F (+68 degrees C)
Altitude	
Operating	10,000 ft (3,048 m)
Non-operating	40,000 ft (12,192 m)
Humidity	0 to 98 percent
Fungus	Fungus resistant
Salt fog	Prolonged exposure without degradation
Sand and Dust	Exposure without damage or degradation
Vibration	Transportable by ground vehicle, watercraft, or aircraft
Rain	
Operating	No damage or degradation

Section III. TECHNICAL PRINCIPLES OF OPERATION

1-12. OVERVIEW



(1) **INTERFACE UNIT TEST SET (IUTS).** Provides digital/analog (D/A) interfaces, and IFP control functions for testing IFP interfaces in IU. Also provides test interfaces for FIFO memory in CP, LO status, and ROM data to RDC.

(2) **INTERFACE UNIT (IU).** Receives and converts analog signals to digital signals from IFP. Transfers pulse data to CP.

(3) **COMPUTER PROCESSOR (CP).** Receives pulse data from IU and processes data to be sent back to IU.

(4) **RECEIVER, DIGITAL, CONTROL (RDC).** Receives commands from IU. Distributes commands to IFS, IFP, and RFA. Transmits ROM data and lock status to IU.

1-13. DETAILED OPERATION

(1) COMPUTER PROCESSOR INTERFACE (CPIF) (A3). Tests FIFO memory in CP.

(2) COMPUTER PROCESSOR SIMULATOR (CP SIM) (A4). Simulates FIFO memory function for testing CP interface in IU.

(3) TEST SET LOCAL OSCILLATOR (TSLO) (AS). Receives FS BCD frequency-tuned data words, L01 and L02, from RDC 1 and RDC 2. Converts differential input data and sends it to DBP (A14). Sends simulated FS lock status signals (LK1 and LK2) to RDC 1 and RDC 2.

(4) TEST SET RADIO FREQUENCY (TSRF) (A9). Simulates outputs from RFA to RDC 1 and RDC 2.

(5) TEST SET IF PROCESSOR (TSIFP) (A7). Generates control signals for testing IFP interface in IU.

(6) TEST SET DIGITAL/ANALOG (TSD/A) (A5) (A6). Simulates analog signals for testing IFP interface in IU.

(7) DUAL-BUS PROCESSOR (DBP) (A14). Controls data handling on bus 1 and bus 2, memory control, and testing.

(8)_ TEST SET BUS (TSBUS) (A13). Generates interrupts, control, and timing signals. Provides an IEEE-STD-488 GPIB to communicate with an external digital delay waveform generator (DDWG). Provides two spare RS-232C channels.

(9) INTERFACE UNIT NAVIGATION (IUNAV) (A12). Generates simulated signals to test IUNAV board in IU.

(10) PROGRAMMABLE STATIC RANDOM ACCESS MEMORY (PSRAM) (A15). Stores operating and diagnostic programs in ROM and stores selected programs and data in RAM.

(11) INTERFACE UNIT DATA LINK (IUDL) (All). Provides a high-speed serial data communications channel to test IU data link interface. Performs self-test using loop-back.

(12) 1553B INTERFACE (A10). 1553B interface (A10) is a high-speed bi-directional transceiver with self-test capability. 1553B interface supports serial communications with IU via MIL-STD-1553 data bus.

(12.1) TICK GENERATOR (A2). Simulates GPS time tick and transmits GPS data to test IU.

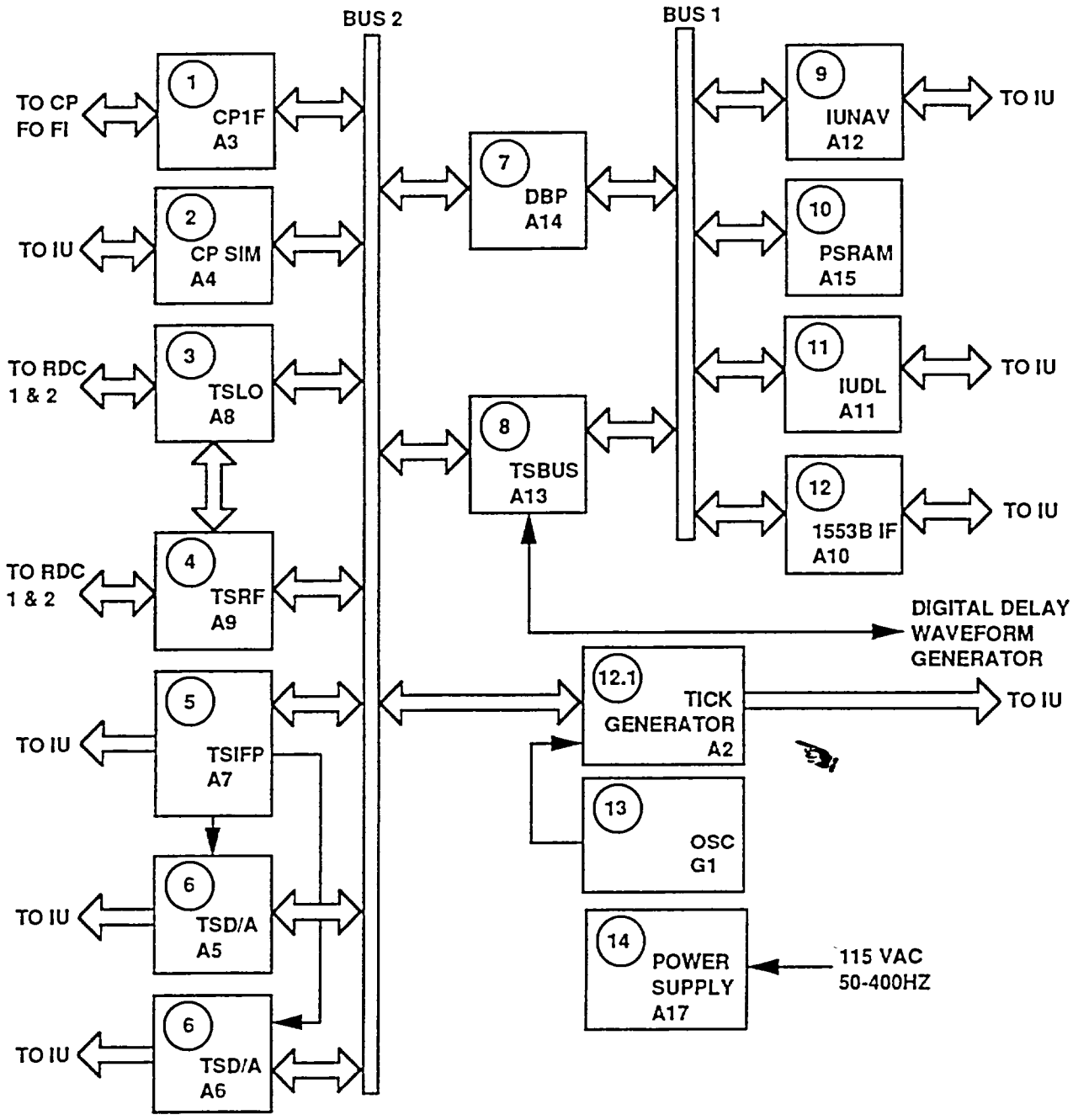
(13) OSCILLATOR (GI). Rubidium oscillator generates a high-accuracy 10 MHz signal.

(14) POWER SUPPLY (A17). Converts +115 Vac to four output voltages (+ 5 Vdc, - 5 Vdc, +12 Vdc, and -12 Vdc) for operation of IUTS.

a. Overview. Refer to the IUTS functional block diagram. IUTS is special test equipment and forms part of AQL maintenance subsystem. Purpose of IUTS is to test the IU interfaces and the CP FIFO memory in the AQL system. IUTS produces pre-programmed test patterns for each interface being tested. IU interfaces are:

- IFP
- CPIF
- RDC
- 1553B interface
- Data link communication system
- Navigation system

1-13. DETAILED OPERATION - Continued



IUTS FUNCTIONAL BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

a. 1. Tick Generator (A2). Refer to the tick generator (A2) block diagram. Tick generator (A2) provides simulated GPS data and time tick signals to the IU under test. These signals are under IUTS software control.

Tick generator (A2) receives:

- Address data (AO-A11) from bus 2
- VO read and write from DBP (A14)
- Data (D0-D7) from bus 2
- System RESET signal INIT-/ from TSBUS (A13)
- RUBCLK from oscillator (G1)
- Serial GPS data signal TXD5 from TSBUS (A13)

Tick generator (A2) outputs:

- Acknowledge to bus 2
- INTRCLK to DBP (A 14) interrupt input
- DRCLK to IU
- TXD5-$ and TXD5-* to IU

(1) Address lines AO-A11 are decoded to produce ADDEC. The read/write decoder uses ADDEC and the I/VO read and write signals from DBP (A14) to generate the acknowledge signal to bus 2, acknowledging the read or write. The read/write decoder also generates a read and a write strobe for the command register.

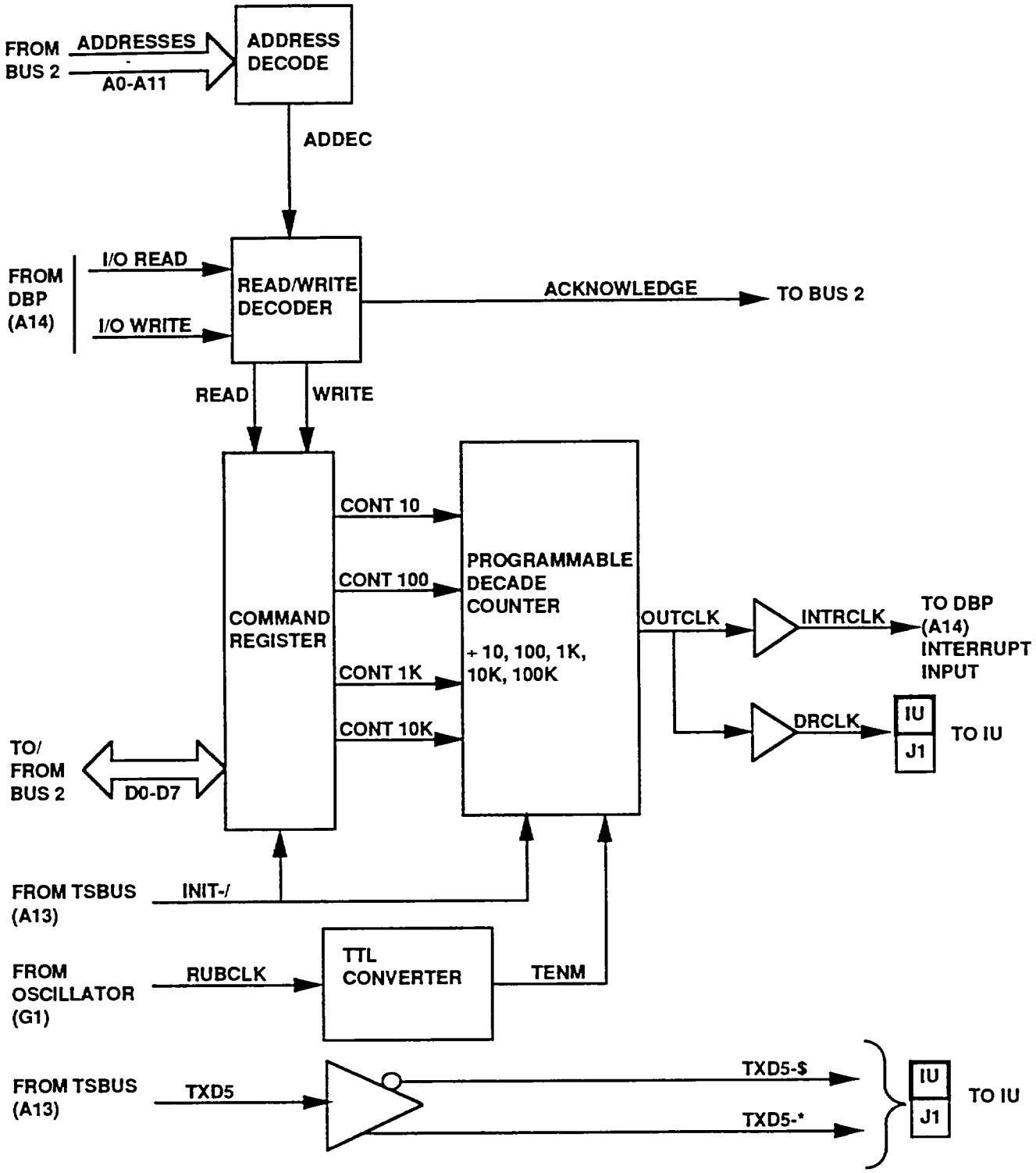
(2) An I/O write command writes data from data bits DO-D7 into the command register. The data becomes CONT 10, CONT 100, CONT 1K, and CONT 10K, which programs the programmable decade counter. An /0O read command allows the data in the command register to be read back onto the data bus. INIT-/ is the power on reset from TSBUS (A 13) and clears the command register.

(3) The 10 MHz sinewave output of oscillator (GI) (RUBCLK) is converted to transistor-transistor logic (TTL) signal TENM and input to the programmable decade counter where it is divided by 10, 100, 1K, 10K, or 100K to generate OUTCLK. The division is controlled by the status of CONT 10, CONT 100, CONT 1K, and CONT 10K inputs to the programmable decade counter. INIT-/ is the power on reset from TSBUS (A 13) and clears the programmable decade counter.

(4) The OUTCLK output of the programmable decade counter is split into two signals and buffered to produce INTRCLK and DRCLK. DRCLK is sent to the IU for test purposes. INTRCLK is the GPS interrupt input to DBP CCA A14.

(5) Simulated navigation data (TXD5) from a serial communications controller on TSBUS (A13) is converted into a differential signal (TXD5-S and TXD5-*) and output to the IU for test purposes.

1-13. DETAILED OPERATION - Continued



TICK GENERATOR (A2) BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

b. CPIF (A3). Refer to the CPIF (A3) block diagram. CPIF (A3) controls differential pulse data transfer between IU and CP.

CPIF (A11) receives:

- 32-BIT DATA from bus 2
- INTERRUPT SIGNALS from CP
- Address data (A1-7) from bus 2
- CPIF ENABLE from TSBUS (A13)

CPIF (A3) outputs:

- 32-BIT DATA to bus 2
- CONTROL SIGNALS to bus 2 and CPIF (A3)
- CP INTERRUPT to TSBUS (A13)
- 4 CP COMMAND SIGNALS, CP COMMAND STROBE SIGNAL, AND CP CLOCK to the CP
- 32-BIT DATA (D0-31) on DIFF BUS to the CP

(1) 32-BIT DATA (called beginning of look header) (BOL) from bus 2 is applied to internal bus D. All of the control signals and enables to route the data through CPIF (A3) are generated within CPIF (A3) itself. Output from the 16-bit latches is enabled on internal bus DI. Data on bus DI are enabled to the 32-bit transceiver. The transceiver puts 32-bit data on internal bus DO and into differential drivers. The differential drivers send the 32bit data (DIFF BUS) to the CP via internal bus DC which connects to the 32-bit differential bus.

(2) Additional 32-bit data called intercept word (IW) may follow the BOL but require holding to allow frequency retrigger (FRT) signals to be sent to the CP first. IW is then enabled from bus DI into FIFO. When CP is ready for 1W, 32-bit data (TW) is put onto DO bus by FIFO and sent by differential drivers to CP the same as BOL.

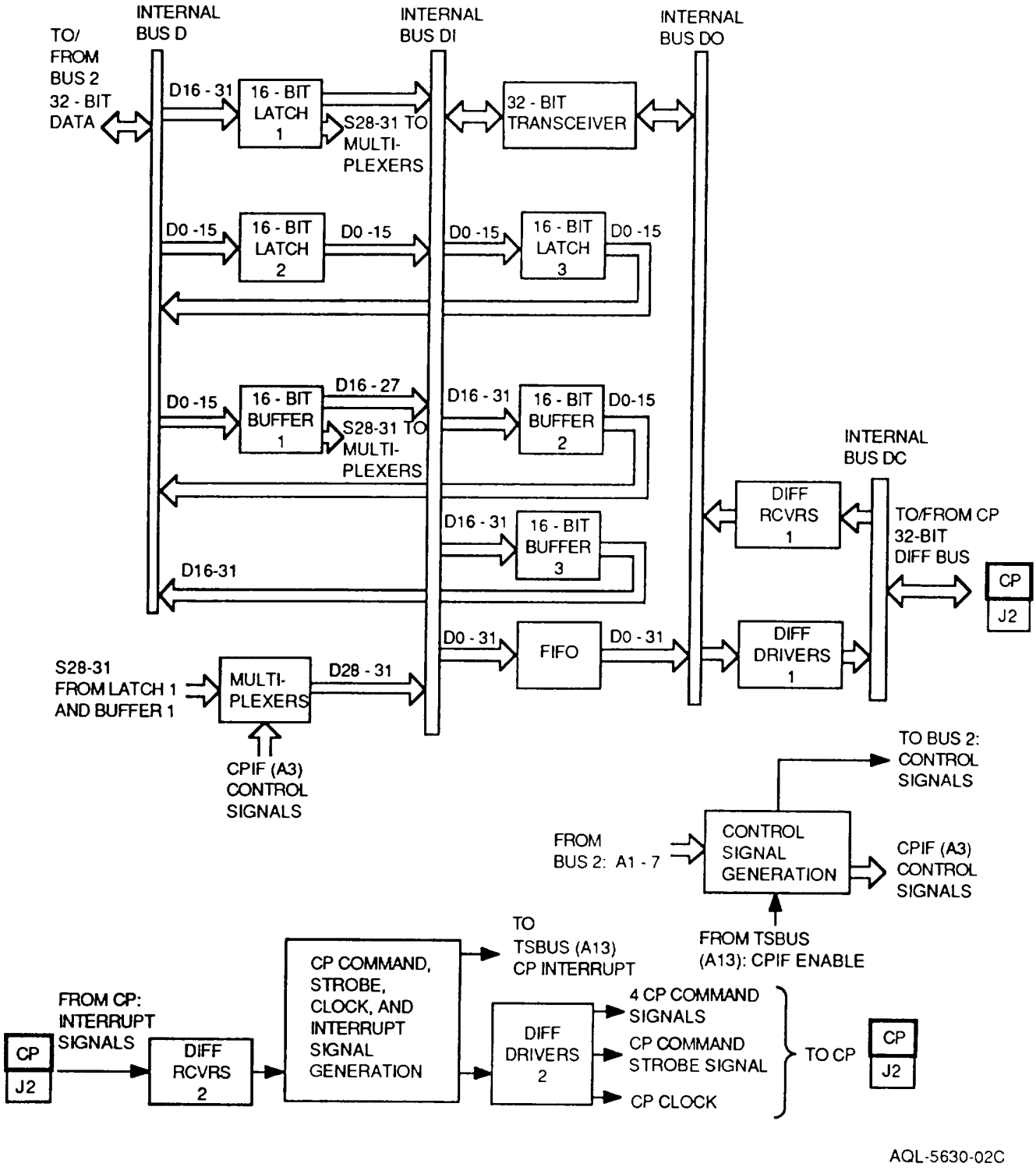
(3) When 32-bit data (FRT) is sent to the CP, it is transmitted the same as BOL. End of look header (EOL) follows to complete data transfer.

(4) Data bits 28-31 of 32-bit data word going to CP are address information and are enabled out of 16-bit latch number 1 and buffer number 1 directly to multiplexers. CPIF control signals and data bits 28-31 control flow of 32-bit data through CPIF (A3).

(5) CP status is sent to CPIF (A3) as 32-bit status word. Status word is sent via the 32-bit differential bus and CPIF internal bus DC to differential receivers number 1. At specific times, data bits DO-15 from bus D are also enabled into 16-bit buffer number 1. The data controls transfer of CP status word as in paragraph (4). The status word out of differential receivers number 1 is put on bus DO and enabled through the 32-bit transceiver to bus DI. From bus DI, data bits DO-15 are enabled through the 16-bit latch number 3 to bus D and the digitizer bus. Data bits DO-15 from the digitizer bus are sent to DBP (A14). From bus DI, data bits D 16-31 are enabled through buffer number 3 to bus D and the digitizer bus. The digitizer bus is connected directly to bus 2 through TSBUS (A13). Status word is destined for DBP (A14) which can only receive 16-bit words. Data bits D16-31 were enabled into the 16-bit buffer number 2 and held. Now data bits D16-31 are enabled out of the 16-bit buffer as DO-15 onto bus D and follow the same route as the first 16-bits to DBP (A14).

(6) CPIF (A3) receives address bits A1-7 via bus 2 and CPIF ENABLE from TSBUS (A13). These signals are applied to the control signal generation circuits. CONTROL SIGNALS are used in CPIF (A3) and bus 2.

1-13. DETAILED OPERATION- Continued



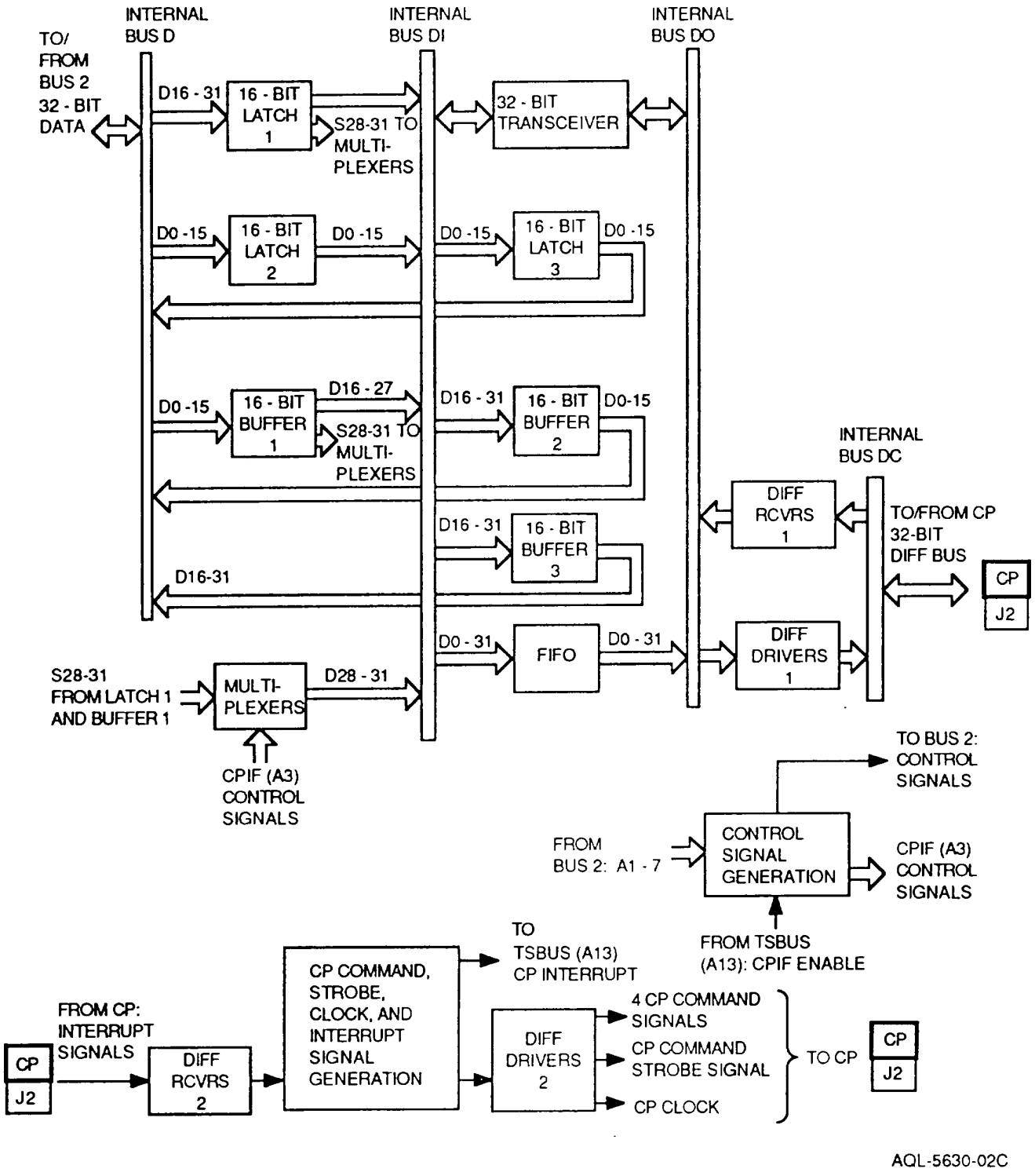
CPIF (A3) BLOCK DIAGRAM

1-13. DETAILEDOPERATION-Continued

(7) INTERRUPT SIGNALS from the CP are applied to differential receivers number 2. The differential receiver outputs are applied to CP command, strobe, and interrupt signal - generation circuit which generates the following outputs and transmits them to the computer processor through differential drivers number 2.

- CP INTERRUPT to TSBUS1 (A13)
- CP COMMAND SIGNALS to the CP
- CP COMMAND STROBE SIGNAL to the CP
- CP CLOCK to the CP

1-13. DETAILED OPERATION- Continued



CPIF (A3) BLOCK DIAGRAM

1-13. DETAILED[OPERATION-Continued

c. CP SIM (A4). Refer to the CP SIM (A4) block diagram. CP SIM (A4) simulates interface between IU and CP FIFO memory. Interface simulation is accomplished by transferring 32-bit data in and out of a 32-bit wide RAM.

The CP SIM (A4) accepts:

- 32-bit differential data from the IU
- 16-bit data from DBP (A14) via bus 2
- Address lines from DBP (A14) via bus 2
- Control signals and clock signals from the IU

The CP SIM (A4) outputs:

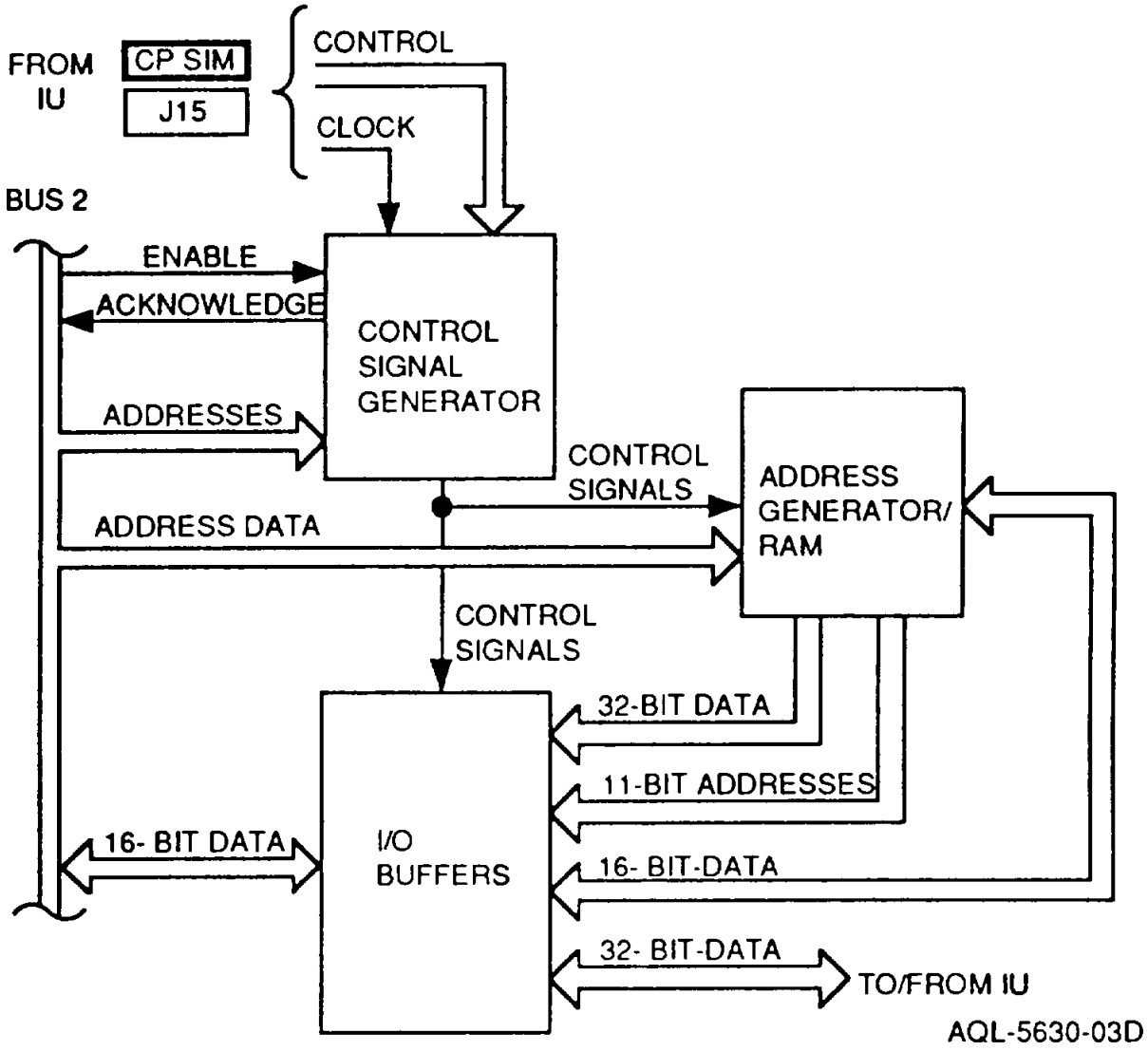
- 32-bit differential data to the IU
- 16-bit data to bus 2
- Control signal response to DBP (A14), TSBUS (A13) via bus 2, and IU

(1) Using control signals from the control signal generator and address lines from bus 2, the address generator produces addresses for the on-board RAM. Refer to the address generator/RAM section for further information.

(2) Using differential data and control signals from the IU, the control signal generator produces reply signals to the DBP (A14), and control signals to the address generator/RAM, and the UO buffers. Refer to the control signal generator section for further information.

(3) Using control signals from the control signal generator, data and addresses from the address generator/RAM and DBP (A14), the IO buffers input and output 16-bit parallel data to and from the DBP (A14) and inputs and outputs 32-bit differential data to and from the IU. Refer to the I/O buffers section for further information.

1-13. DETAILED OPERATION - Continued



CP SIM (A4) BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

d. Address Generator/RAM. Refer to the CP SIM (A4) address generator block diagram. The address generator section of this card produces addresses for storage in RAM.

The address generator/RAM accepts:

- 11-bit address lines A2-12 from bus 2
- ADDRESS SELECT, WRITE STROBE H, and WRITE STROBE L from the control signal generator
- INCREMENT and RESET from the control signal generator
- OUTPUT ENABLES and BOARD STATUS from the control signal generator
- 32-bit RAM data DI0-31 from the I/O buffers

The address generator/RAM outputs:

- 32-bit RAM data DI0-31 to the I/O buffers
- 1-bit counter full signal to the control signal generator
- 11-bit address lines AC2-12 to the I/O buffers

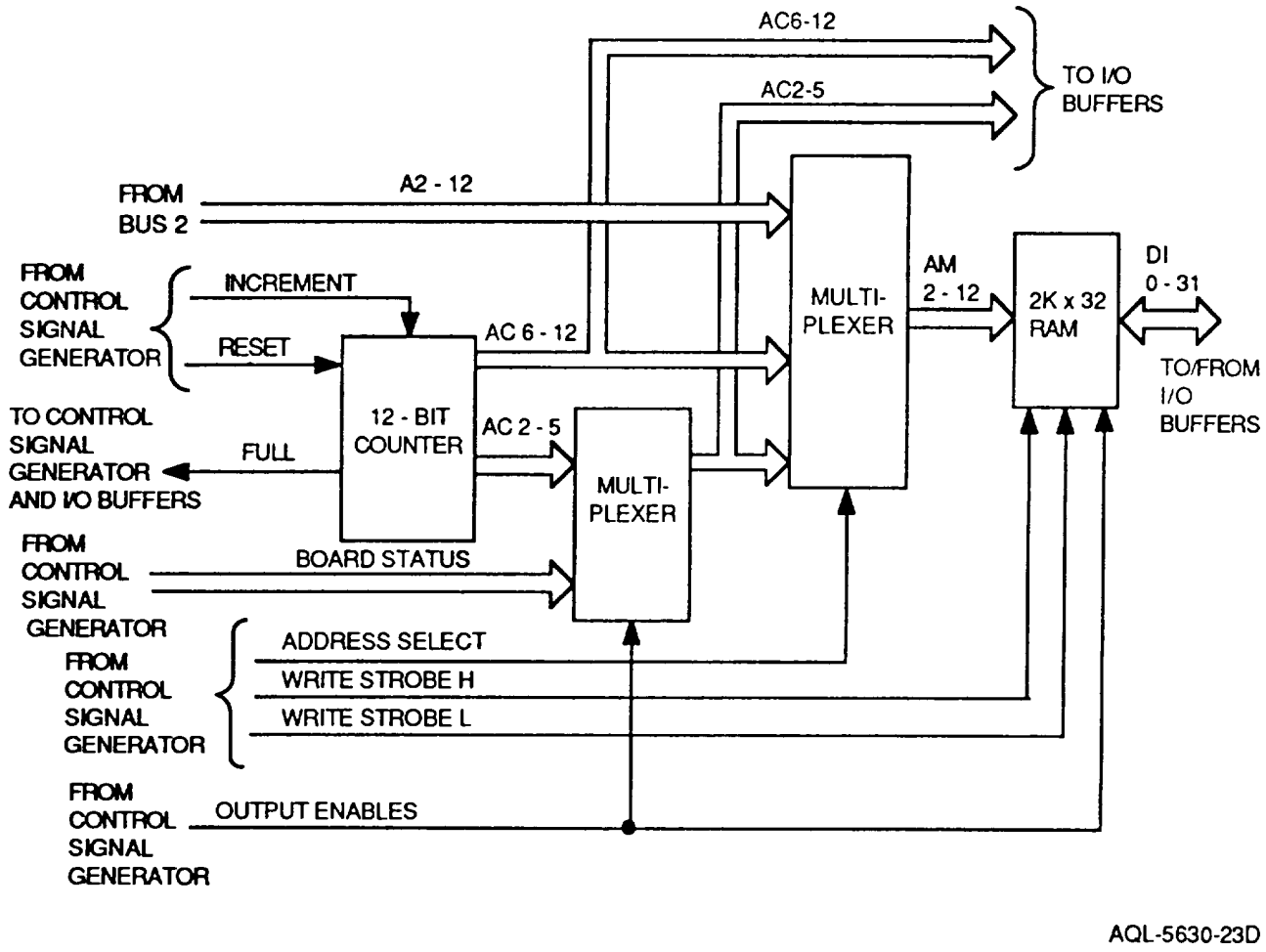
(1) Using the INCREMENT input, the 12-bit counter generates address signals AC2-5 and AC6-12, and a 1-bit counter full signal.

(2) Using the board status lines, 4 bits of address lines from the 12-bit counter (AC2-5), and OUTPUT ENABLES, address lines to the second multiplexer (AM2-5), are selected.

(3) Using the 11 address lines (A2-12) or the address lines AC6-12, AC2-5, and ADDRESS SELECT, the memory address lines AM2-12 are selected by the second multiplexer.

(4) The 2K x 32 RAM simulates CP FIFO memory. Address signals AM2-12 from the second multiplexer are written into RAM upon receipt of a write signal. RAM data DI0-31 is output from RAM upon receipt of WRITE STROBE H, WRITE STROBE L, and OUTPUT ENABLES.

1-13. DETAILED OPERATION- Continued



CP SIM (A4) ADDRESS GENERATOR/RAM BLOCK DIAGRAM

1-13. DETAILED OPERATION- Continued

e. Control Signal Generator. Refer to the CP SIM (A4) control signal generator block diagram. The control signal generator section produces reply signals to the DBP (A14), and control signals to the address generator/RAM and the I/O buffers.

The control signal generator accepts:

- 4-bit address (A16-19) from bus 2
- 3-bit address (A01-03) from bus 2
- CLOCK and CONTROL from the IU
- FULL from the address generator/RAM
- CPSIM ENABLE from TSBUS (A13)

The control signal generator outputs:

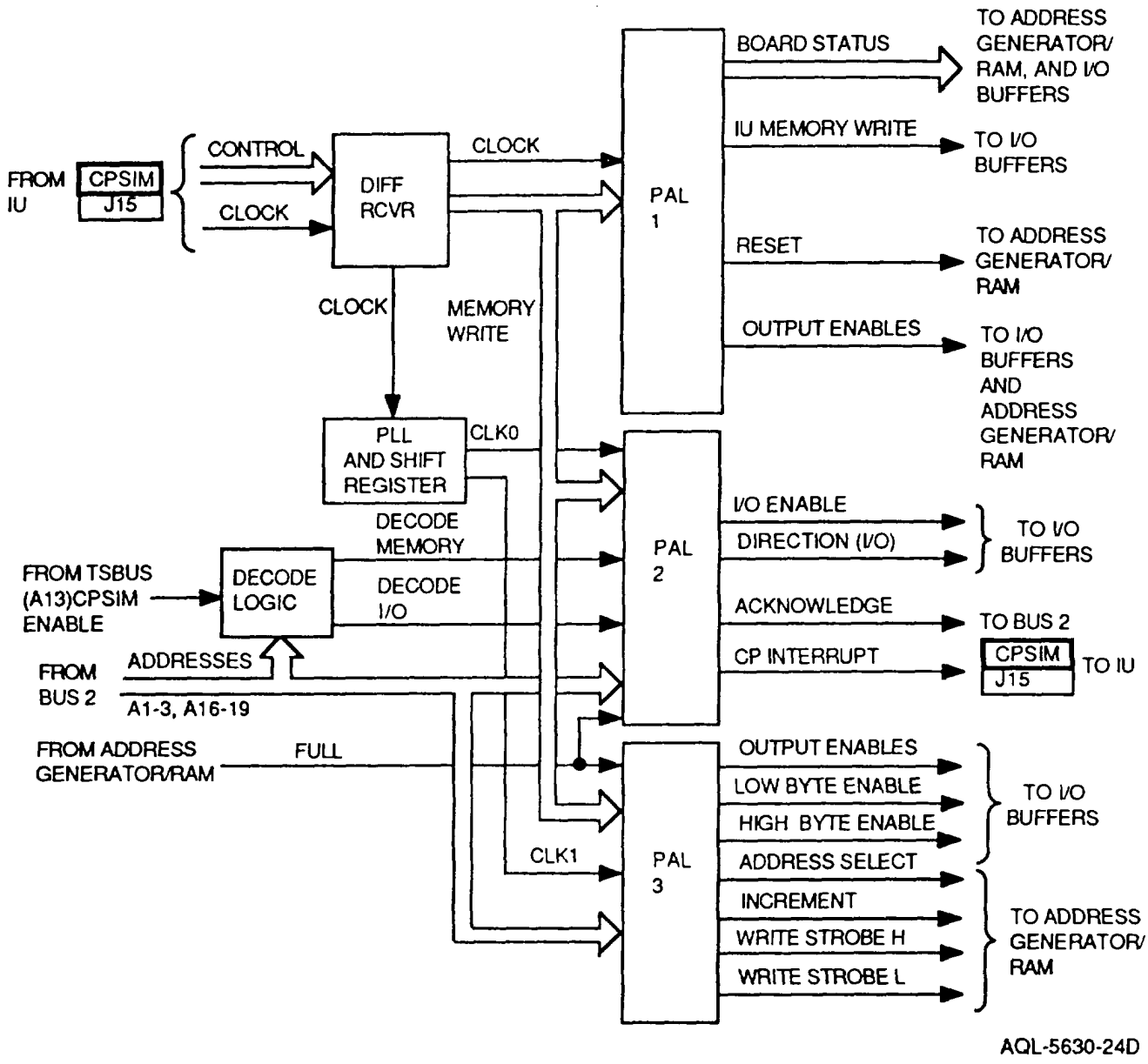
- IU MEMORY WRITE to I/O buffers
- I/O ENABLE to the 1/O buffers
- DIRECTION (I/O) to the I/O buffers
- ACKNOWLEDGE to bus 2
- CP INTERRUPT to the IU via the differential bus
- RESET to the address generator/RAM
- OUTPUT ENABLES to the I/O buffers and address generator/RAM
- LOW BYTE ENABLE to the IO buffers
- HIGH BYTE ENABLE to the IO buffers
- ADDRESS SELECT to the address generator/RAM
- INCREMENT to the address generator/RAM
- WRITE STROBE H (high) to the address generator/RAM
- WRITE STROBE L (low) to the address generator/RAM
- BOARD STATUS to the address generator/RAM and I/O buffers

(1) CLOCK is applied to the phase-lock loop (PLL) and shift register via the differential receiver. The PLL generates CLKO and CLK1 for PALS 2 and 3.

(2) When CPSIM ENABLE is applied, the decode logic decodes the upper four address lines (A16-19) and generates DECODE MEMORY to PAL 2. Using the lower three address lines (A01-03), the decode logic outputs DECODE IO to PAL 2. The differential receiver generates MEMORY WRITE from CONTROL. The combination of CLOCK, MEMORY WRITE, DECODE MEMORY, FULL, AND DECODE I/O causes PAL 2 and PAL 3 to output the various signals used throughout the CP SIM and the IUTS.

(3) Using MEMORY WRITE and CLOCK, PAL 1 produces the various signals used by other CP SIM sections.

1-13. DETAILED OPERATION - Continued



CP SIM (A4) CONTROL SIGNAL GENERATOR BLOCK DIAGRAM

1-13. DETAILED OPERATION- Continued

f. I/O Buffers. Refer to the CP SIM (A4) I/O buffers block diagram. The UO buffers section inputs and outputs 16-bit parallel data to and from the DBP (A14), and inputs and outputs 32-bit differential data to and from the IU.

The I/O buffers accept:

- 11-bit addresses (AC2-12) from the address generator/RAM
- 32-bit data (DDO-31) from the IU
- LOW BYTE ENABLE, HIGH BYTE ENABLE, and DIRECTION UO from the control signal generator
- 16-bit data (DO-15) from bus 2
- DI0-13 from address generator/RAM
- Counter full status (FULL) from the address generator/RAM
- I/O ENABLE from the control signal generator
- IU MEMORY WRITE from the control signal generator
- BOARD STATUS from the address generator/RAM
- OUTPUT ENABLES from the control signal generator

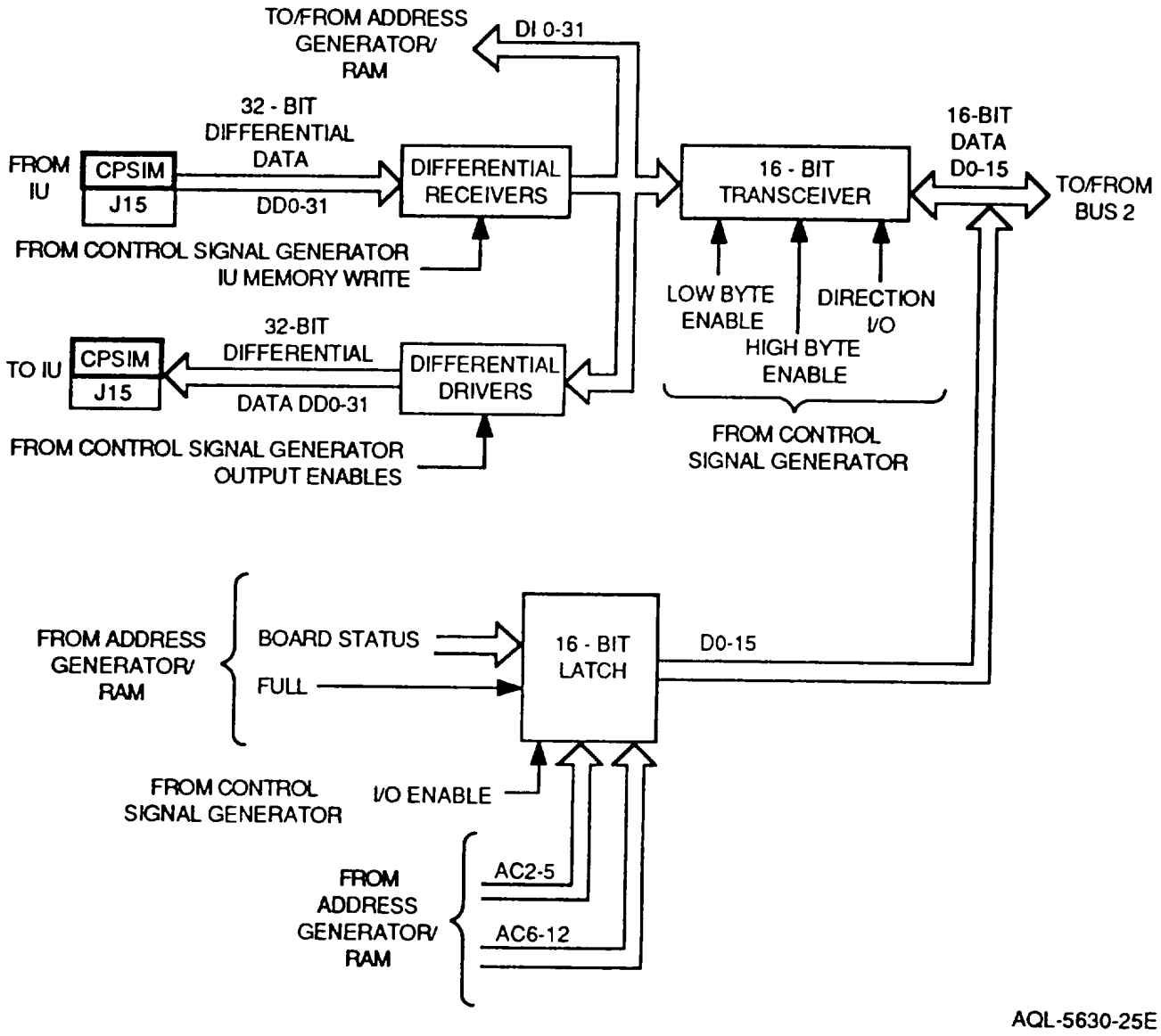
The I/O buffers output:

- DIO-13 to address generator/RAM
- 32-bit data (DDO-31) to the IU
- 16-bit data (DO-15) to bus 2

(1) The differential receivers and differential drivers are used to transfer data to and from the RAM to the IU using IU MEMORY WRITE and OUTPUT ENABLES.

(2) The 16-bit transceiver transfers 16-bit data to and from bus 2 using DIRECTION I/O, LOW BYTE ENABLE, and HIGH BYTE ENABLE. The 16-bit latch holds the counter address and full status and board status, which may be enabled onto bus 2 using I/O ENABLE.

1-13. DETAILED OPERATION -Continued



CP SIM (A4) I/O BUFFERS BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

g. TSLO (A8). Refer to the TSLO (AS) block diagram. The software-controlled TSLO (A8) tests the IU/FS/RFA/RDC interface by receiving FS BCD frequency-tuned data words, L01 and LO2, from the RDC and transmitting FS lock-status signals (LK1 and LK2) to the RDC via a differential bus. TSLO (AS) also sends control signals to TSRF (A9).

TSLO (As) accepts:

- BCD frequency-tuned FS data words, L01 and L02, as 48 differential signals (L0100-123 and L0200-223) from the RDC
- Frequency strobes (FSTB1, FSTB2) as two differential signals from RDC
- Three address lines (A01-03B2) from bus 2
- INIT4 from TSBUS (A13) via test set control bus
- ICLK from TSBUS (A13) via test set control bus
- LO ENABLE from TSBUS (A13)
- WRITE ENABLE and READ ENABLE from bus 2

TSLO (As) outputs:

- LOAD COMMAND to TSRF (A9)
- 16-bit data (D00-15B2) to bus 2
- Acknowledge signal (XACKB2-/) to bus 2
- FS lock-status signals (LK1, LK2) as two differential signals to RDC
- READ STROBES to TSRF (A9)

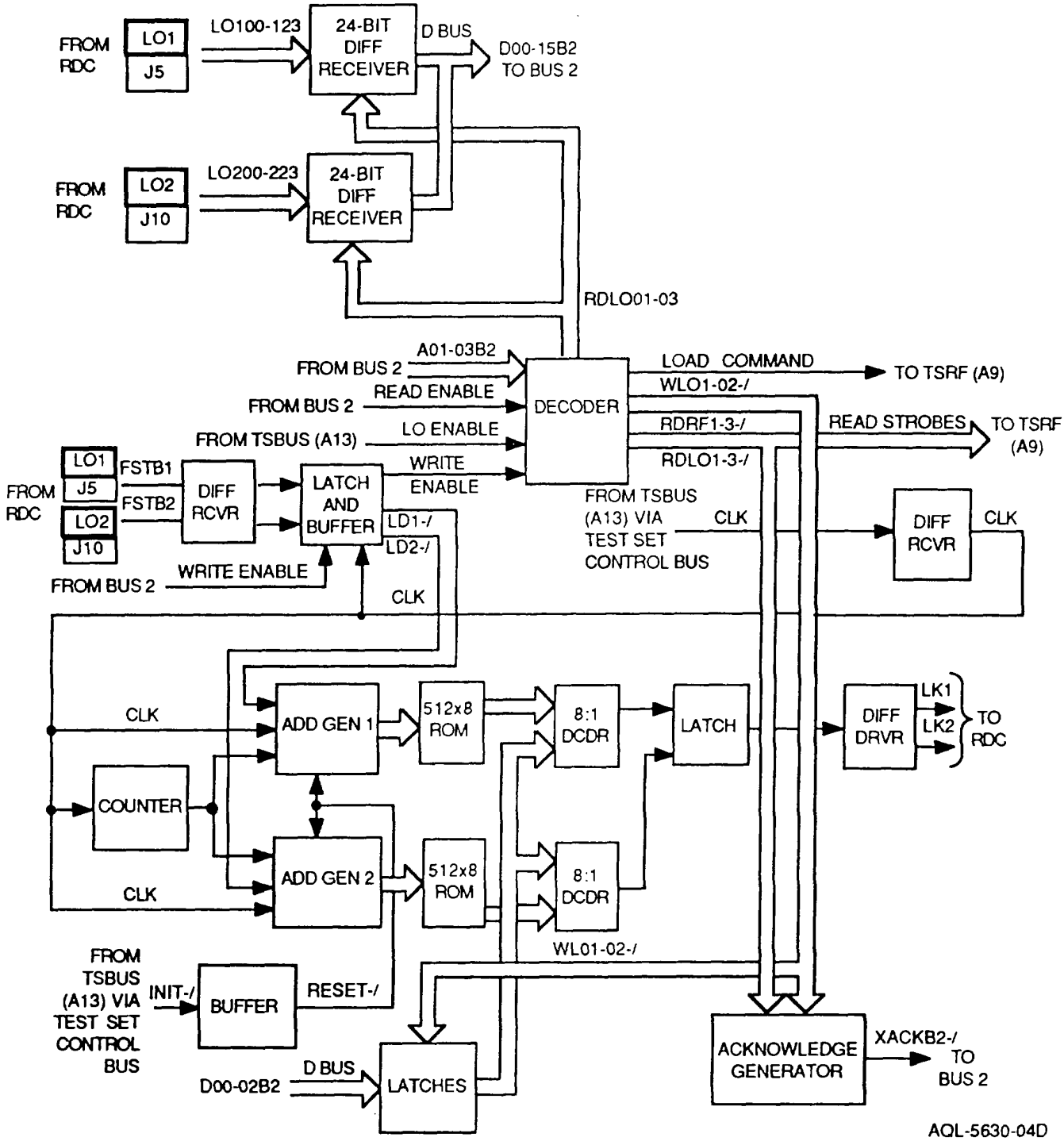
(1) TSLO input and output data and signals:

- An input clock signal (CLK) from TSBUS (A13) is received by a differential receiver and the output signal CLK is used as the board clock.
- INIT-/ is received and buffered to become the board reset signal RESET-/.
- Two 24-bit differential receiver and filter networks receive the 24-bit frequency tune words L0100-123 and LO200-223 from the RDC.
- Strobe RDLO1-/ enables the lower 16 bits of tune word L01 onto bus 2. Strobe RDLO2-/ enables the lower 16 bits of tune word L02 onto bus 2. Strobe RDLO3-/ enables the upper 8 bits of tune word L01 and the upper 8 bits of tune word L02 onto bus 2.

(2) TSLO read strobe, write strobe and acknowledge generation:

- Bus 2 address lines A01-03B2 and LO ENABLE are used to generate the read and write strobes. LO ENABLE and the address signals are fed into a decoder which generates read strobes RDLO01-03-/ and RDRF1-3-/ and write strobes WL01-02-/ and LOAD COMMAND. LOAD COMMAND and RDRF1-3-/ are outputs used by the TSRF (A9) module.
- The read and write strobes are fed into an acknowledge generator which outputs the acknowledge signal XACKB2-/.
- FSTB1 and FSTB2 are applied to the latch and buffer via the differential receiver. The signals are written into the latch by WRITE ENABLE. The latch outputs LD1-/ and LD2-/ are buffered and applied to the address generators. The WRITE ENABLE output from the latch and buffer is applied to the decoder. Write commands (WLO1-02-/) from the decoder are controlled by WRITE ENABLE. Read commands (RDRF1-3-/ and RDLO1-3-/) are controlled by READ ENABLE.

1-13. DETAILED OPERATION - Continued



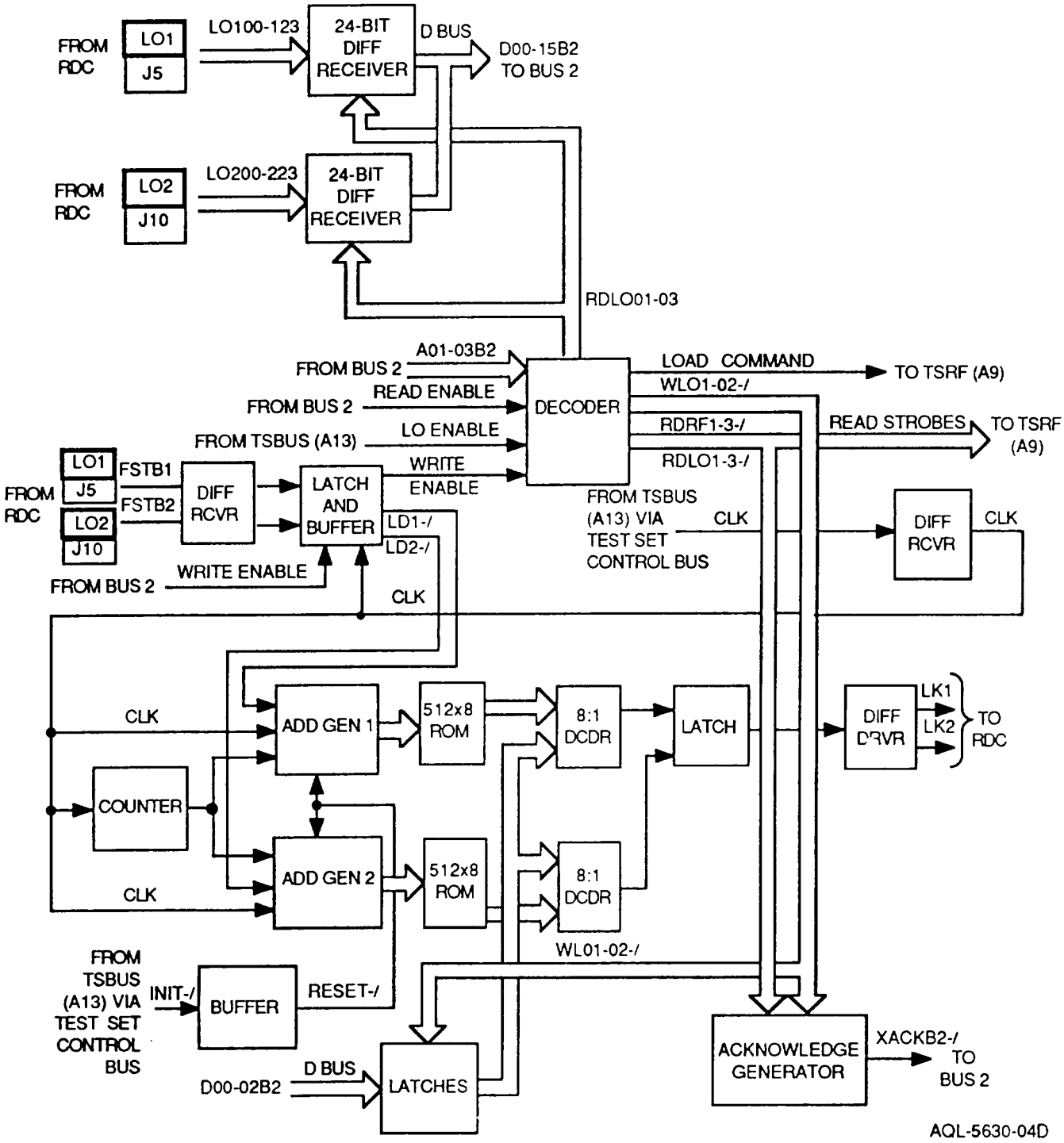
TSLO (AS) BLOCK DIAGRAM

1-13. DETAILED OPERATION-Continued

(3) TSLO lock status.

- Frequency strobe signals FSTB1 and FSTB2 from the RDC are applied to differential receivers, then buffered and latched to form load signals LD1-/ and LD2-. The load signals are used to pre-load the address generators (ADD GEN 1 and ADD GEN 2). The address generators are incremented by a 64 psec signal generated from an 8-bit free running counter clocked by CLKI. The outputs of the address generators are used as inputs to two 512 x 8 ROM containing lock status data. Data bits D00-02B2 are clocked into latches by write strobes WLO1-/ and WL02-/. The output of the latches is used as an input to two 8:1 decoders selecting 1 bit from each ROM. The status bits from the decoders are latched and sent to differential drivers. The outputs of the differential drivers are the lock status signals LK1 and LK2.

1-13. DETAILED OPERATION - Continued



TSLO (AS) BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

h. TSRF (A9). Refer to the TSRF (A9) block diagram. The TSRF simulates outputs from RFA to RDC1 and RDC2.

TSRF (A9) accepts:

- Data from RDC in the form of three 16-bit differential data words
- READ STROBES and LOAD COMMAND from TSLO (As)
- PHASE CALIBRATION DATA TXD3 from TSBUS (A13)

TSRF (A9) outputs:

- 16-bit data (D00-15B1) to bus 2
- Simulated RFA ROM PHASE CALIBRATION data to the RDC as six differential signals
- which represent low-band (LB), mid-band (MB), and high-band (HB) phase-correction data

(1) Control data:

- The TSRF (A9) circuit card consists of twelve differential receivers arranged to receive three 16-bit data words.

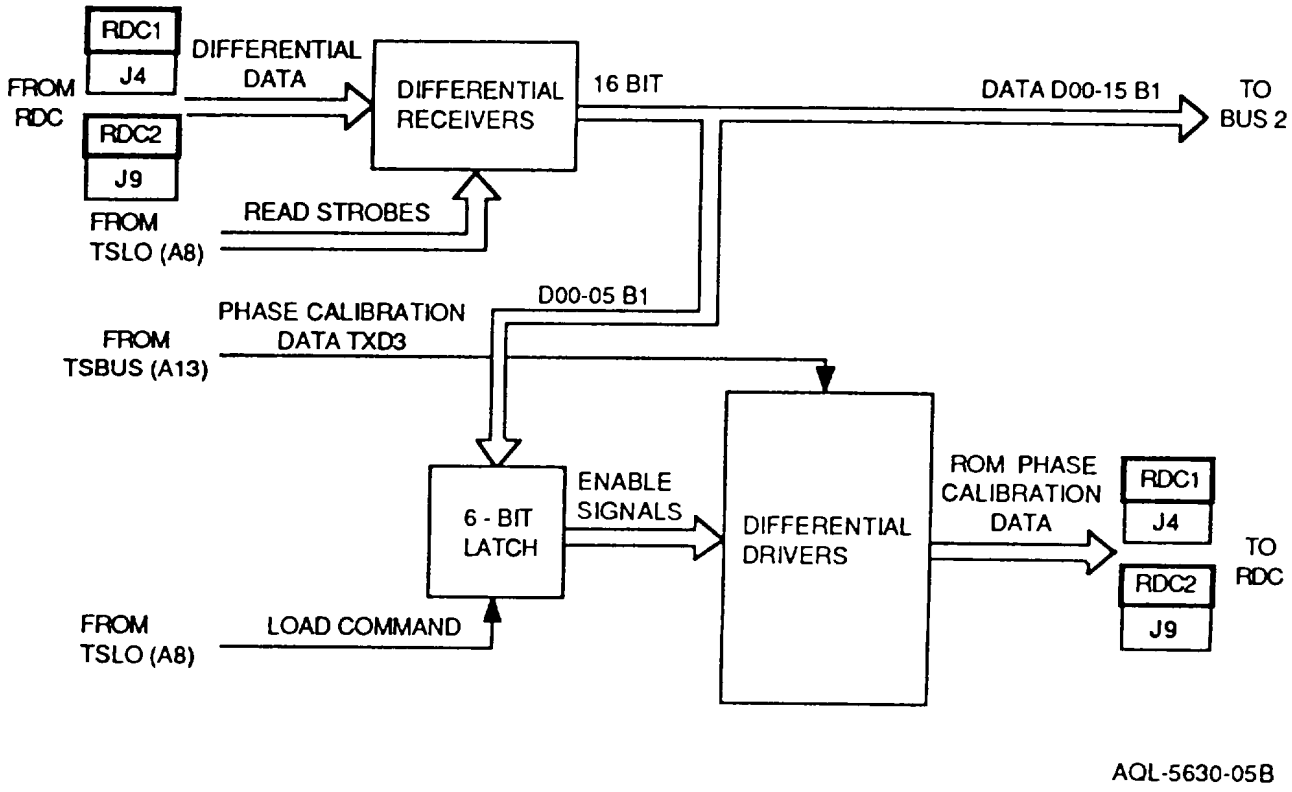
- The output of each 16-bit word may be enabled onto bus 2 by one of three READ STROBES.

- Data word 1 contains control signals for IFS A and IFP A Data word 2 contains control signals for IFS B and IFP B. Data word 3 contains control signals for RF antennas A and B.

(2) Phase calibration data:

- Data bits D00-05B1 are written into a 6-bit latch on load signal LOAD COMMAND. The latch output, ENABLE SIGNALS, is used to enable one of six differential drivers. When enabled, a driver passes input data as differential ROM PHASE CALIBRATION DATA for one of the selected RF antenna bands.

1-13. DETAILED OPERATION - Continued

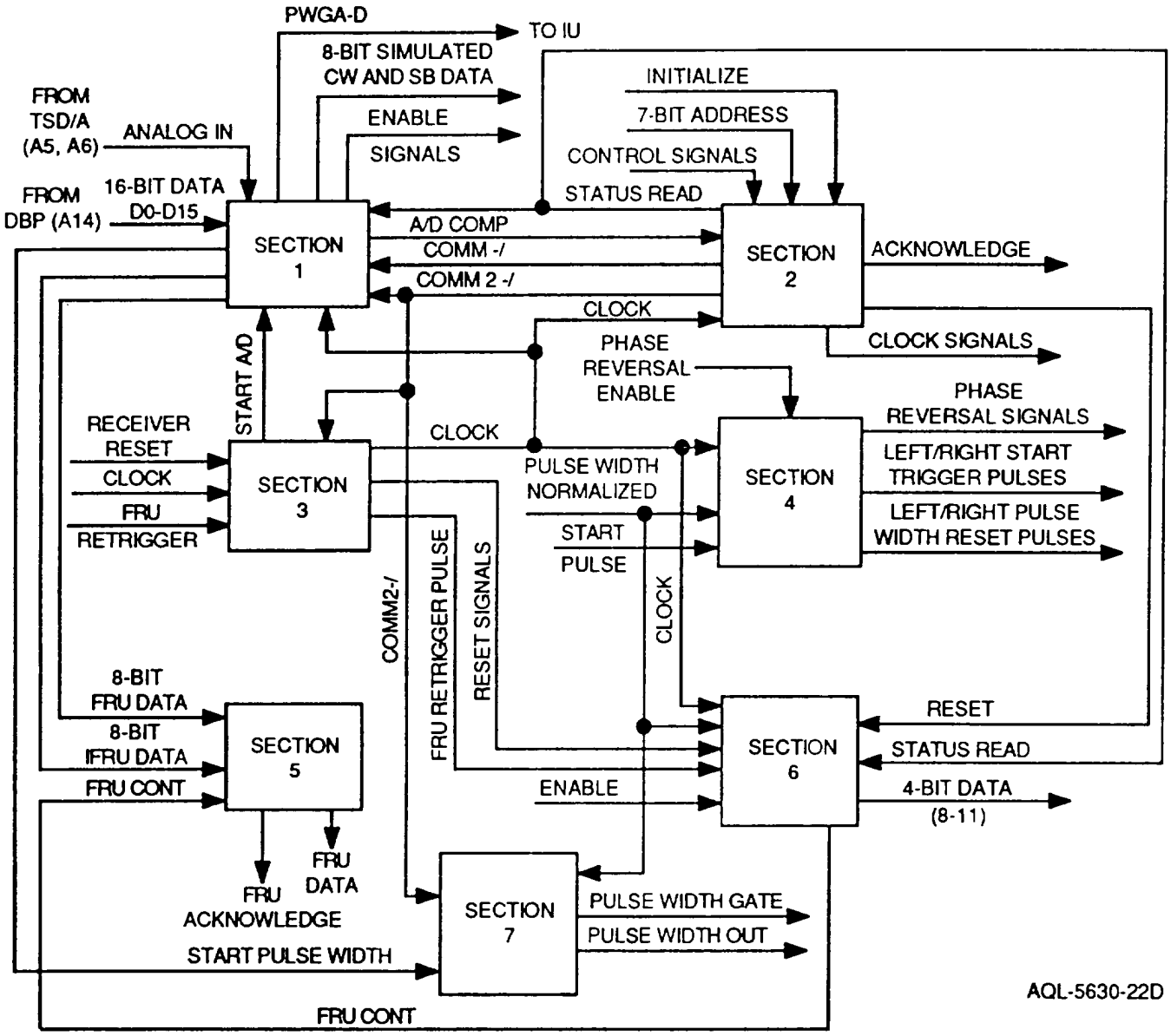


TSRF (A9) BLOCK DIAGRAM

1-13. DETAILEDOPERATION-Continued

j. TSIFP (A7). Refer to the overall TSIFP (A7) block diagram. The software-controlled TSIFP (A7) functions as directed by DBP (A14) running operating system and diagnostic programs. In conjunction with TSD/A (A5) and TSD/A (A6), TSIFP (A7) tests the IFP interface to the IU by generating simulated IFP 1,0 data and control signals. Data flow between the IU, TSIFP (A7), TSD/A (AS), and TSD/A (A6) is entirely dependent upon operating system programs and diagnostic/test programs as executed by DBP (A13) with interaction of operator terminal and associated peripheral devices. Refer to the following seven paragraphs for further information. The major elements of the TSIFP (A7) are divided into seven groups. Refer to TSIFP (A7) sections one through seven.

1-13. DETAILED OPERATION - Continued



TSIFP (A7) OVERALL BLOCK DIAGRAM

1-13. DETAILED OPERATION-Continued

j. TSIFP (A7) Section One. Refer to the TSIFP (A7) block diagram, section one. TSIFP (A7) section one inputs data to and outputs data from the board.

TSIFP (A7) section one accepts:
- 16-bit data (DO-15B2) from DBP (A14) via bus 2
- ANALOG IN from TSD/A (A5) or TSD/A (A6)
- Control signal (STATUS READ) from TSIFP (A7) section two
- Control signal (START AID) from TSIFP (A7) section three
- Clock command signals (COMM-/, COMM2-, and AD96CK-/) from TSIFP (A7) section two
- CLOCK from TSIFP (A7) section three

TSIFP (A7) section one outputs:
- PHASE REVERSAL ENABLE to TSIFP (A7) section seven
- PWGA-D to IU
- A/D COMP to TSIFP (A7) section three
- START PUILSE WIDTH to TSIFP (A7) section seven
- ADDRESS SELECT to TSD/A (A5, A6)
- 8-BIT SIMULATED CW DATA (differential) to IU
- 8-BIT SIMULATED SB DATA (differential) to IU
- 8-bit FRU data to TSIFP (A7) section five
- 8-bit IFRU data to TSIFP (A7) section five
- 16-bit data to DBP (A14) via bus 2
- ANALOG ENABLE and TEST to TSD/A (A5, A6)
- PWGA-D to IU
- A/D COMP to TSIFP (A7) section three

TSIFP (A7) section one signal processing:

(1) The 16-bit transceiver is used to handle 16-bit parallel data between TSIFP (A7) and DBP(A14).

(2) Data is written into 16-bit latch (1), which outputs START PULSE WIDTH, PHASE REVERSAL ENABLE, DPWA-D, TEST, and 8-BIT SIMULATED CW AND SB DATA.

(3) 8-BIT SIMULATED CW AND SB DATA is sent through the differential drivers to the IU.

(4) Data is written into the 8-bit latch, which outputs ADDRESS SELECT to TSD/A (A5, A6) and ADDRESS SELECT CONTROL and ENABLE to the open collector drivers which output ANALOG ENABLE signals to TSD/A (A5) and TSD/A (A6).

(5) Data is written into 16-bit latch (2), which outputs 8-BIT FRU DATA and 8-BIT IFRU DATA to TSIFP (A7) section five.

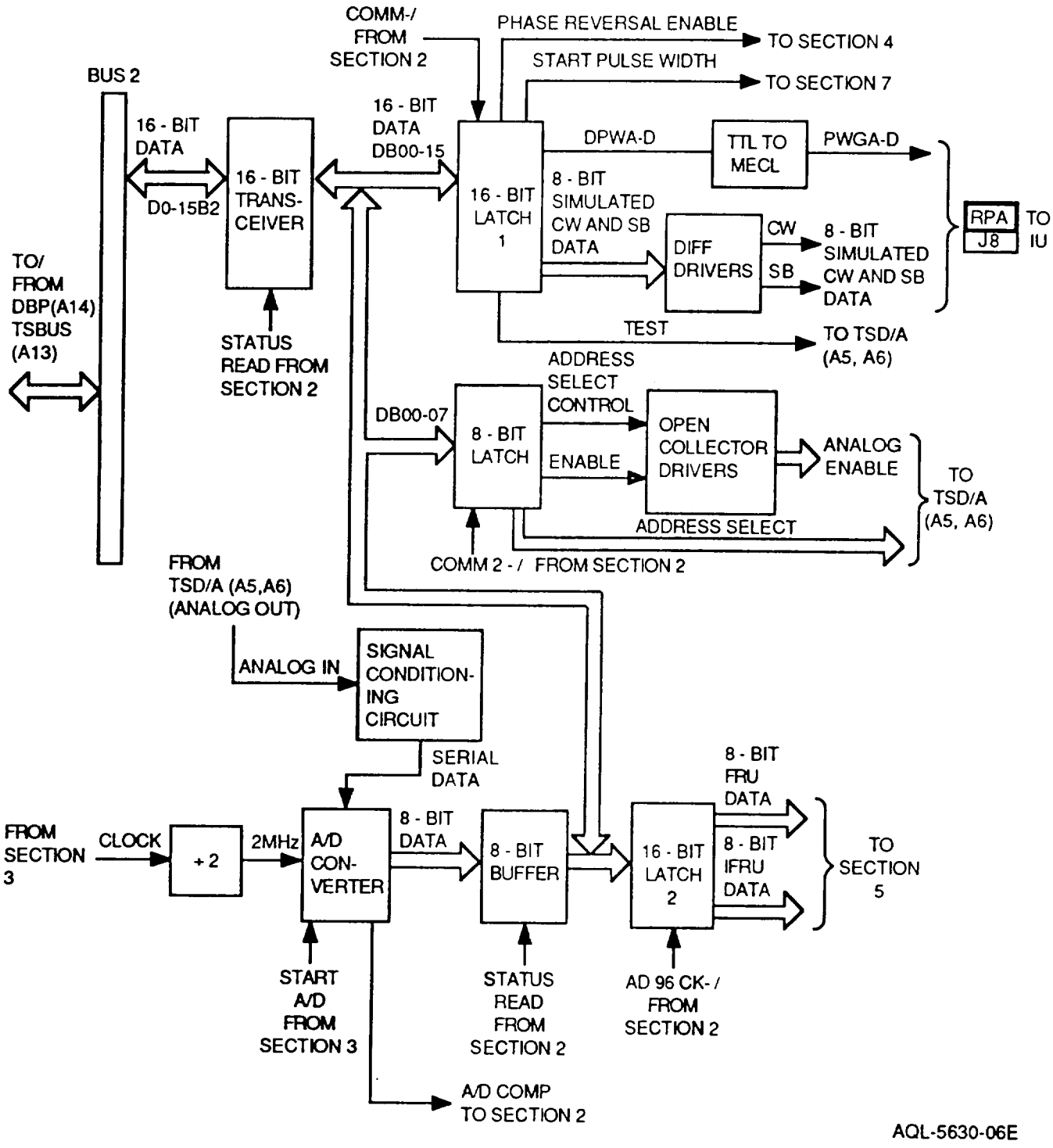
(6) ANALOG OUT from TSD/A (A5) or TSD/A (A6) is sent to the TSIFP (A7) as ANALOG IN. ANALOG IN is applied to the signal conditioning circuit and then to the A/D converter.

(7) The output of the A/D converter, 8-BIT DATA, is strobed through the 8-bit buffer to the 16-bit transceiver, where it is sent to DBP (A14) via bus 2.

(8) CLOCK is applied to the divide-by-two circuitry and output as 2 MHZ to the AID converter. A/D COMP is produced when the A/D converter is finished with its conversion and 8-BIT DATA is passed to the 8-bit buffer.

(9) Four bits from the 16-bit latch (DPWA-D) are sent to a TTL to MECL (Motorola emitter coupled logic) converter and output as PWGA-D to the IU.

1-13. DETAILED OPERATION - Continued



TSIFP (A7) BLOCK DIAGRAM, SECTION ONE

1-13. DETAILEDOPERATION-Continued

k. TSIFP (A7) Section Two. Refer to the TSIFP (A7) block diagram, section two. TSIFP (A7) section two generates signals for the D/A circuit cards (A5, A6) and control signals used elsewhere in the TSIFP.

TSIFP (A7) section two accepts:

- INITIALIZE from bus 2
- 7-BIT ADDRESS (A1-7) from bus 2
- CONTROL SIGNALS from bus 2
- CLOCK and A/D COMP from TSIFP (A7) section three
- A/D ENABLE from TSBUS (A13)
- A/D COMP from TSIFP (A7) section three

TSIFP (A7) section two outputs:

- RESET to TSIFP (A7) section six
- ACKNOWLEDGE to bus 2
- STATUS READ to TSIFP (A7) sections one and six
- Clock signals to TSD/A (A5), TSD/A (A6), and TSIFP (A7) sections one, three, and seven
- TSIFP (A7) section two signal processing:

(1) CONTROL SIGNALS are latched into the 8-bit latch and used as inputs into the PAL.

(2) The second input to the PAL, 6-BIT ADDRESS, is input via the 8-bit buffer.

(3) The PAL generates ACKNOWLEDGE, STATUS READ, and 4-BIT ADDRESS DECODE.

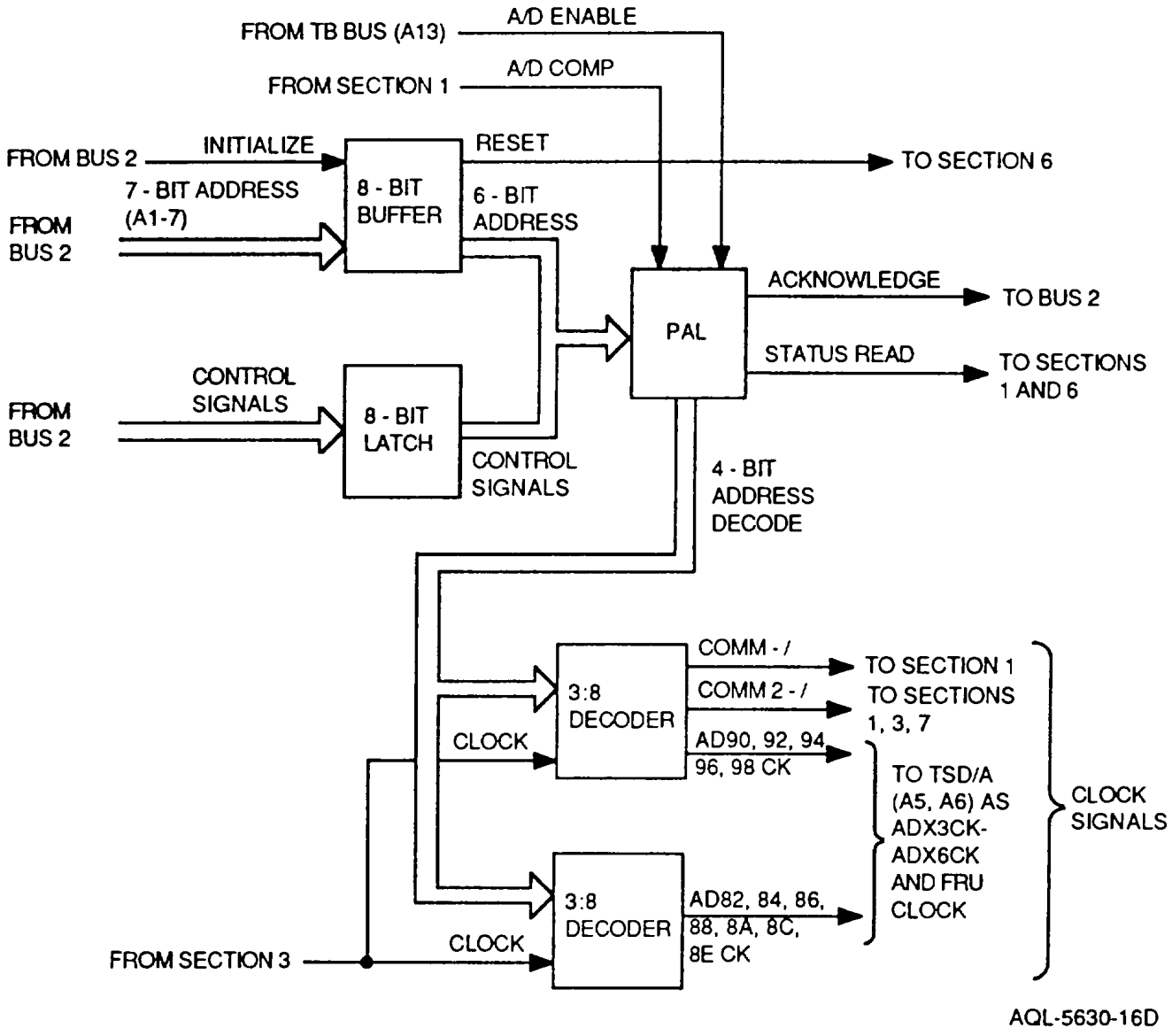
(4) ACKNOWLEDGE is sent to DBP (A14).

(5) A/D ENABLE asserts at the beginning of the A/D conversion and A/D COMP asserts at the end of the A/D conversion to provide intelligence for STATUS READ.

(6) STATUS READ is sent to a buffer and a receiver in TSIFP (A7) section one, and a PAL in TSIFP (A7) section six.

(7) 4-BIT ADDRESS DECODE is an input to the 3:8 decoders which generate clock signals COMM-/, COMM2-/, AD90, 92, 94, 96, 98 CK, and AD82, 84, 86, 88, 8A, 8C, 8E CK for TSD/A (A5) and TSD/A (A6). (These clock signals are named ADX3CK-ADX6CK and FRU CLOCK when they reach the TSD/A cards.)

1-13. DETAILED OPERATION- Continued



TSIFP (A7) BLOCK DIAGRAM, SECTION TWO

1-13. DETAILED OPERATION- Continued

l. TSIFP (A7) Section Three. Refer to the TSIFP (A7) block diagram, section three. TSIFP (A7) section three generates control signals for use in other TSIFP sections.

TSIFP (A7) section three accepts:

- RECEIVER RESET from IU
- FRU RETRIGGER from IU
- CLK from TSBUS (A13) via test set control bus
- COMM2-from TSIFP (A7) section two

TSIFP (A7) section three outputs:

- RESET SIGNAIS to TSIFP (A7) section six
- FRU RETRIGGER PULSE to TSIFP (A7) section six
- CLOCK to TSIFP (A7) sections one, two, four, and six
- START A/D to TSIFP (A7) section one

TSIFP (A7) section three signal processing:

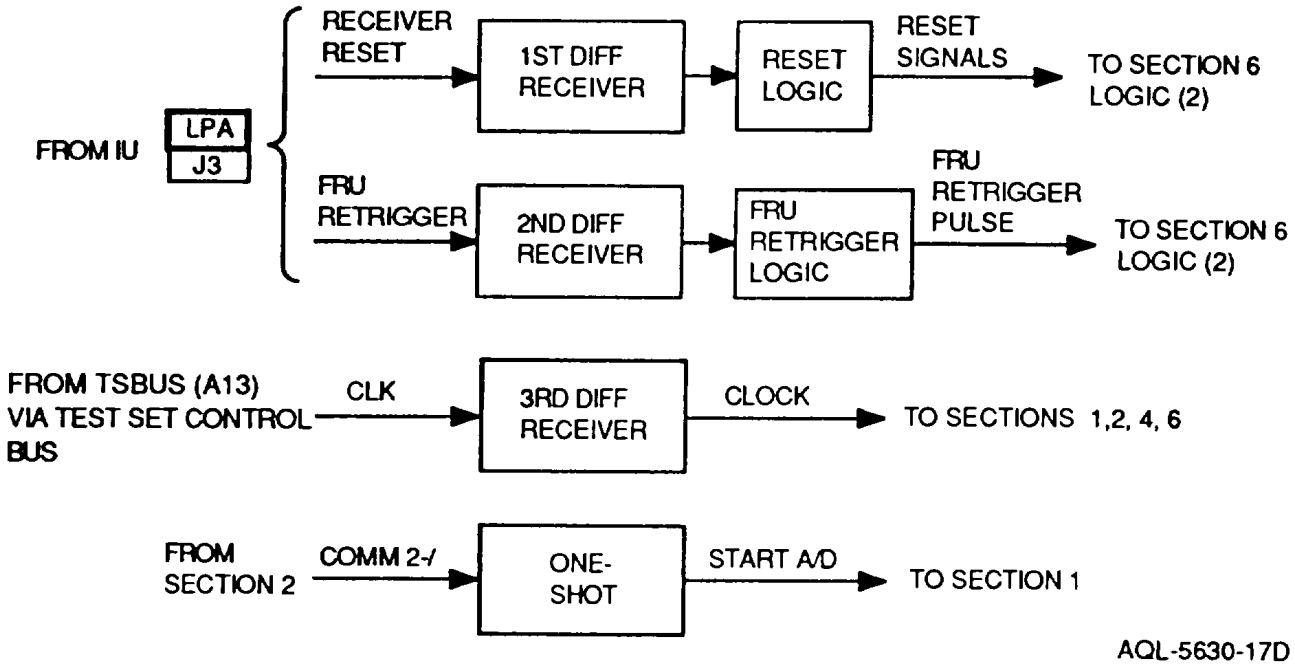
(1) RECEIVER RESET is applied to the reset logic circuit via the first differential receiver. The output of the reset logic circuit is RESET SIGNALS, used in TSIFP (A7) section 6.

(2) FRU RETRIGGER is applied to the FRU retrigger logic circuits via the second differential receiver. The signal is combined in the retrigger logic circuits to form FRU RETRIGGER PULSE, which is sent to TSIFP (A7) section six.

(3) CLK is applied to the third differential receiver, which generates CLOCK for use as TSIFP (A7) clocks in sections two, four, and six.

(4) When COMM2-/ is applied to the one-shot, it generates START A/D for the AD converter in TSIFP (A7) section one.

1-13. DETAILED OPERATION - Continued



TSIFP (A7) BLOCK DIAGRAM, SECTION THREE

1-13. DETAILED OPERATION-Continued

m. TSIFP (A7) Section Four. Refer to the TSIFP (A7) block diagram, section four. TSIFP (A7) section four generates trigger and reset pulses for use in the IU.

TSIFP (A7) section four accepts:

- PULSE WIDTH NORMALIZED from the digital delay/width generator
- CLOCK from TSIFP (A7) section three
- PHASE REVERSAL ENABLE from TSIFP (A7) section one
- START PULSE from TSIFP (A7) section seven

TSIFP (A7) section four outputs:

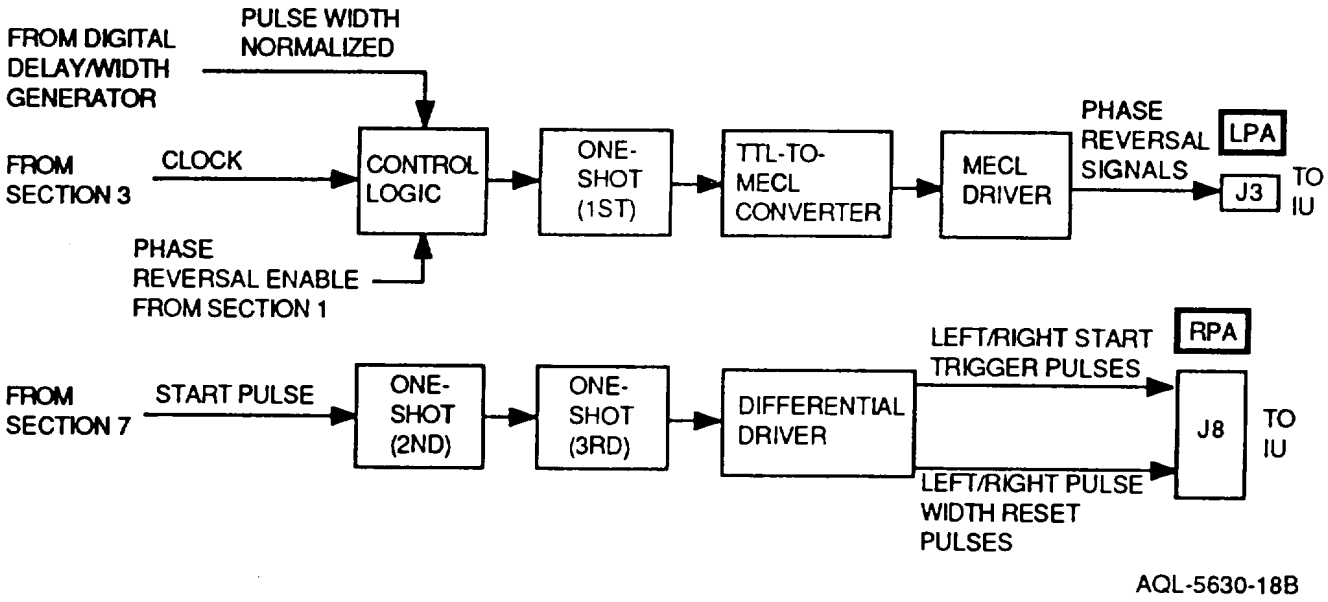
- PHASE REVERSAL SIGNALS to the IU
- LEFT/RIGHT START TRIGGER PULSES to the IU
- LEFT/RIGHT PULSE WIDTH RESET PULSES to the IU

TSIFP (A7) section four signal processing:

(1) Using PULSE WIDTH NORMALIZED, CLOCK, and PHASE REVERSAL ENABLE, the control logic, the first one-shot, the TTL to-MECL converter, and the MECL driver provide PHASE-REVERSAL SIGNALS to the IU.

(2) Using START PULSE, the second and third one-shots and the differential driver provide LEFT/RIGHT PULSE WIDTH RESET PULSES and LEFT/RIGHT START TRIGGER PULSES to the IU.

1-13. DETAILED OPERATION- Continued



TSIFP (A7) BLOCK DIAGRAM, SECTION FOUR

1-13. DETAILEDOPERATION-Continued

n. TSIFP (A7) Section Five. Refer to the TSIFP (A7) block diagram, section five. TSIFP (A7) section five generates various FRU signals for the TSD/A cards (A5, A6).

TSIFP (A7) section five accepts:

- 8-BIT FRU DATA from TSIFP (A7) section one
- 8-BIT IFRU DATA from TSIFP (A7) section one
- FRU CONT from TSIFP (A7) section six

TSIFP (A7) section five outputs:

- FRU ACKNOWLEDGE to TSD/A (A5) and TSD/A (A6)
- FRU DATA (FRUAO-7) to TSD/A (A6)

TSIFP (A7) section five signal processing:

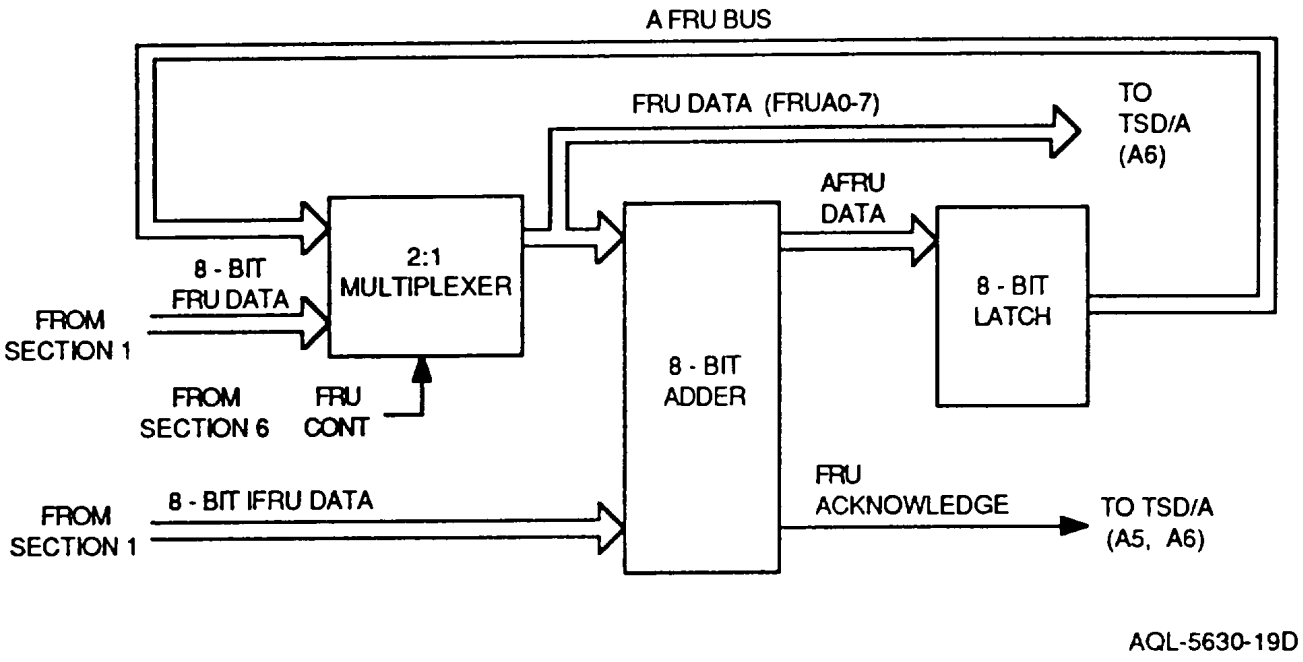
(1) FRU DATA and data from the AFRU bus are applied to the 2:1 multiplexer. Depending upon the state of FRU CONT, one or the other is passed to the 8-bit adder.

(2) This data is then added to 8-BIT IFRU data and latched into the 8-bit latch as AFRU data.

(3) The output of the multiplexer is also passed to TSD/A (A6) to be converted to an analog signal and sent to the IU.

(4) FRU ACKNOWLEDGE clocks data into latches on TSD/A (A5) and TSD/A (A6).

1-13. DETAILED OPERATION - Continued



TSIFP (A7) BLOCK DIAGRAM, SECTION FIVE

1-13. DETAILED OPERATION- Continued

o. TSIFP (A7) Section Six. Refer to the TSIFP (A7) block diagram, section six. TSIFP (A7) section six produces a 4-bit data word for bus 2 and a control signal for the DBP.

TSIFP (A7) section six accepts:

- STATUS READ from TSIFP (A7) section two
- RESET from TSIFP (A7) section two
- ENABLE from bus 2
- CLOCK from TSIFP (A7) section three
- PUI-E WIDTH NORMALIZED from the digital delay/width generator
- FRU RETRIGGER PULSE and RESET SIGNALS from TSIFP (A7) section three

TSIFP (A7) section six outputs:

- 4-BIT DATA (8-11) to bus 2
- FRU CONT to TSIFP (A7) section five

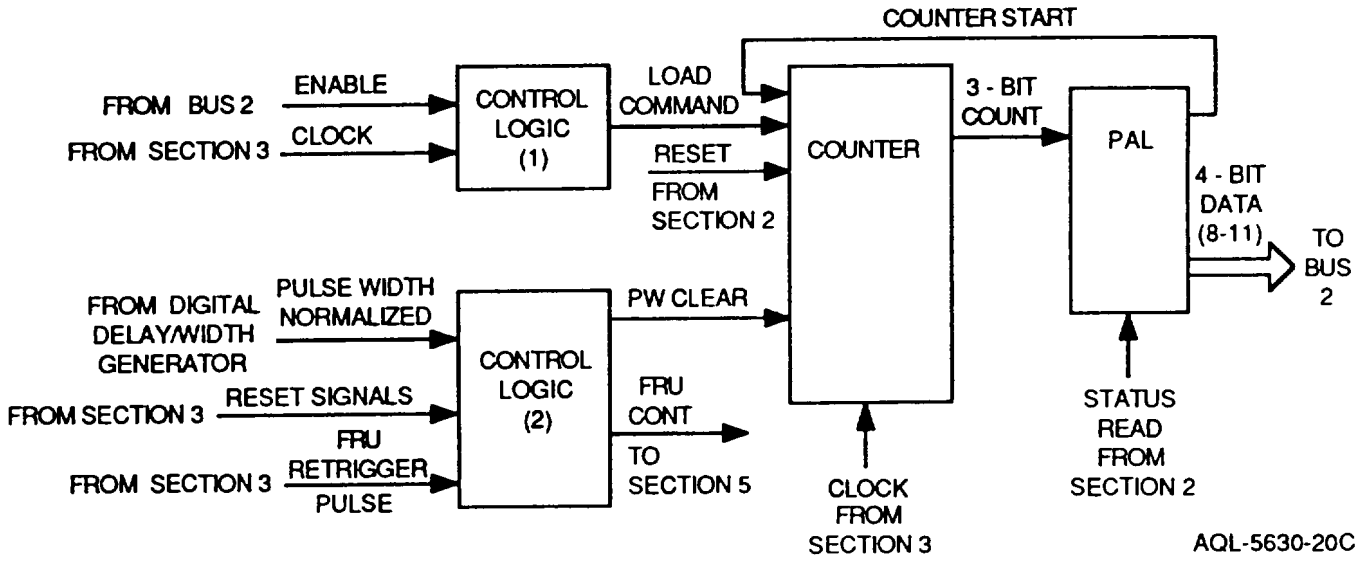
TSIFP (A7) section six signal processing:

(1) Using the inputs ENABLE and CLOCK, control logic circuit (1) provides LOAD COMMAND for the counter. The counter is pre-loaded and can be enabled to either count up or count down.

(2) Using the inputs PULSE WIDTH NORMALIZED, RESET SIGNALS, and FRU RETRIGGER PULSE, control logic circuit (2) generates the counter control signal PW CLEAR. Control logic circuit (2) also produces FRU CONT, used in TSIFP (A7) section five to control a 2:1 multiplexer.

(3) The PAL is used to generate COUNTER START and outputs the count onto data lines 8 to 11 of bus 2.

1-13. DETAILED OPERATION - Continued



TSIFP (A7) BLOCK DIAGRAM, SECTION SIX

1-13. DETAILED OPERATION - Continued

p. TSIFP (A7) Section Seven. Refer to the TSIFP (A7) block diagram, section seven. TSIFP (A7) section seven produces pulse width signals to the IU and the digital delay/width generator.

TSIFP (A7) section seven accepts:

- PULSE WIDTH NORMALIZED from the digital delay/width generator
- START PULSE WIDTH from TSIFP (A7) section one
- COMM2-/ from TSIFP (A7) section two

TSIFP (A7) section seven outputs:

- PULSE WIDTH GATE to IU
- PULSE WIDTH OUT to digital delay/width generator
- START PULSE to TSIFP (A7) section four

TSIFP (A7) section seven signal processing:

(1) PULSE WIDTH NORMALIZED from the test generator is converted to MECL levels (PULSE WIDTH GATE IN) and buffered into two identical pulse width signals.

(2) One of the pulse width signals goes directly to the control logic circuit, and the other goes through a delay line before going to the control logic circuit.

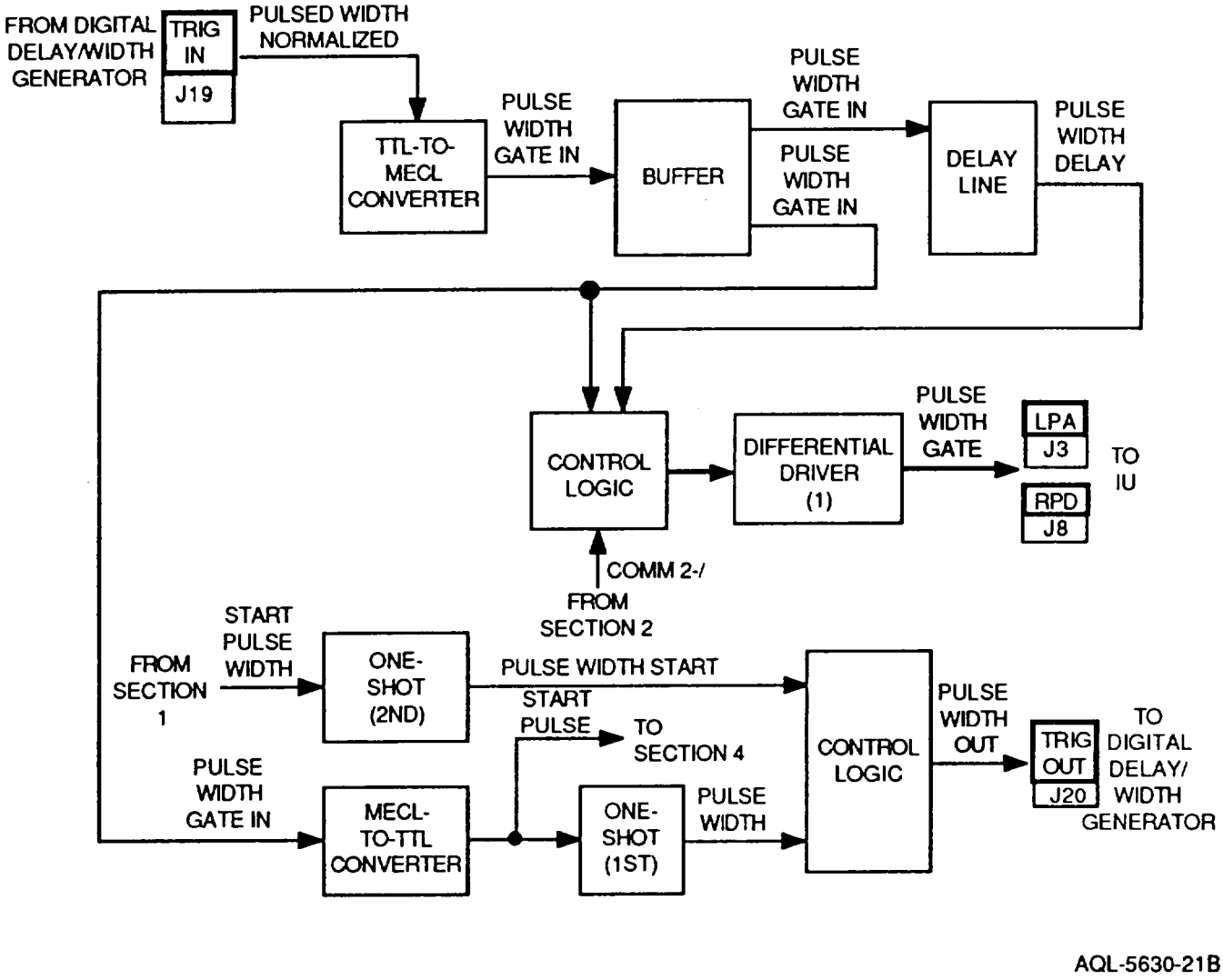
(3) The control logic circuit selects one of the two signals and outputs it through a differential driver as PULSE WIDTH GATE.

(4) The non-delayed pulse is converted back to a TTIL level used to trigger the first one-shot and is also sent to TSIFP (A7) section four as START PULSE.

(5) The output of the first one-shot, PULSE WIDTH, is applied to another control logic circuit.

(6) The second one-shot is used as an input to the control logic circuit to allow PULSE WIDTH from the first one-shot to pass through the control logic circuit and become PULSE WIDTH OUT.

1-13. DETAILED OPERATION - Continued



TSIFP (A7) BLOCK DIAGRAM, SECTION SEVEN

1-13. DETAILOPERATION-Continued

q. TSD/A (A5 and A6). TSD/A (AS and A6) function together to test IFP analog interface to IU by generating simulated pod quadrant A and B analog data.

NOTE

The following is representative of either TSD/A (A5) or TSD/A (A6).

TSD/A (A5 and A6) accept:

- 16-bit data from bus 2
- Latch clock signals ADX3 CK - ADX6 CK from TSIFP (A7)
- TEST from TSIFP (A7)
- ADDRESS SELECT from TSIFP (A7)
- ANALOG ENABLE from TSIFP (A7)
- FRUAO-7 from TSIFP (A7) (accepted by A6 only)
- FRU ACKNOWLEDGE and FRU CLOCK from TSIFP (A7)

TSD/A (A5 and A6) output:

- Left pod quadrant A simulated analog data to IU
- Left pod quadrant B simulated analog data to IU
- Right pod quadrant A simulated analog data to IU
- Right pod quadrant B simulated analog data to IU
- FRU DATA A and FRU DATA B to IU
- ANALOG OUT to TSIFP (A7)

(1) 16-bit data is buffered and strobed into 8-bit latches (1, 2) by latch clock signals (ADX3 CK- ADX6 CK) from TSIFP (A7).

(2) FRU data (FRUAO-7) is clocked into the 8-bit buffer by FRU ACKNOWLEDGE and FRU CLOCK This data and the test input line signal (TEST) address ROM whose digital output represents RFA pod data. ROM digital data outputs are converted by DIA converters (1, 3) to 16 analog signals representing:

- RFA df in-phase (I) data
- RFA df quadrature-phase (Q) data
- Fine-frequency FRU data

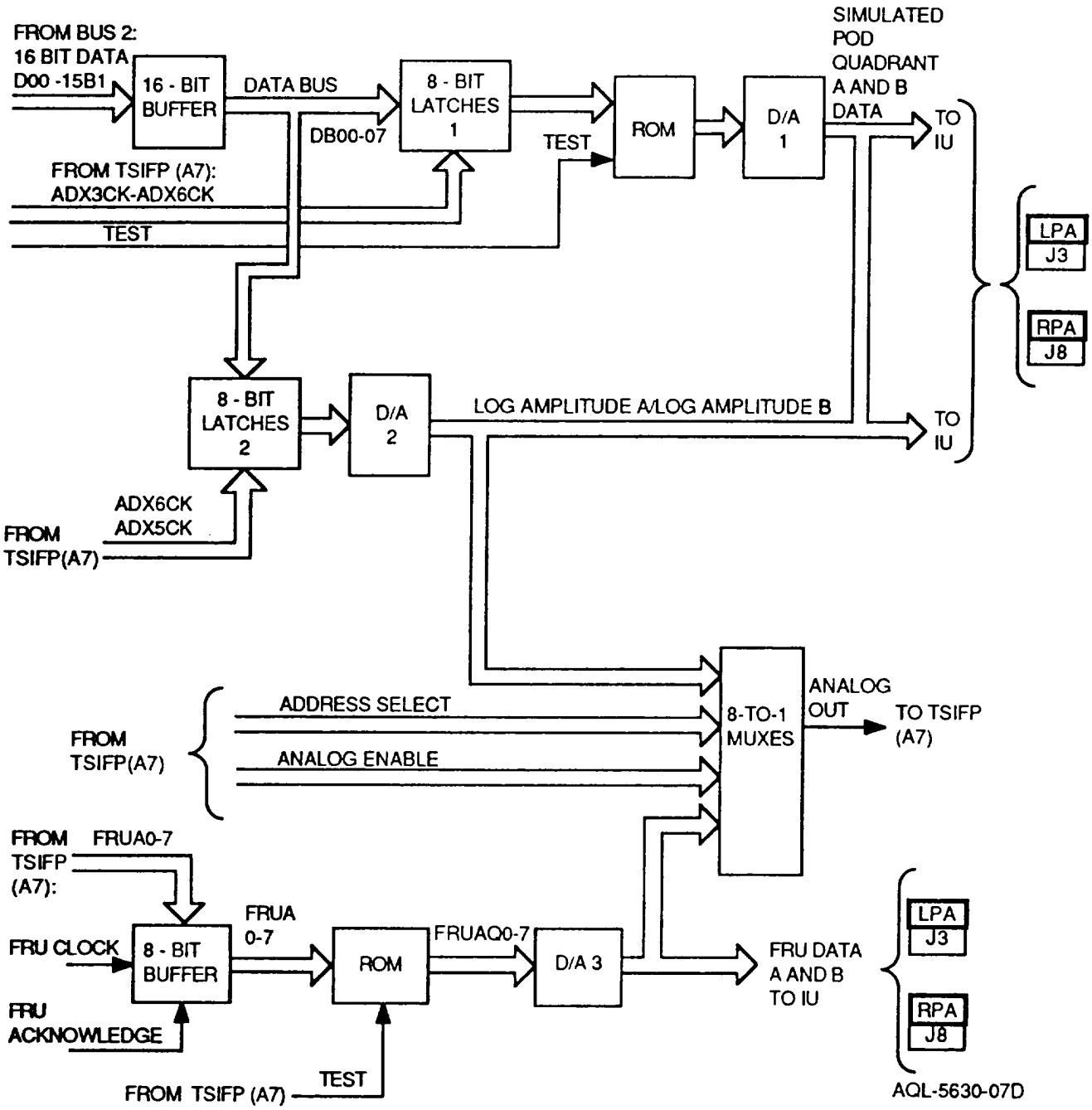
(3) These 16 ROM-derived analog signals are sent to the IU and to the 8-to-1 multiplexers.

(4) The upper data bits are latched into an 8-bit latch (2) and are directly converted by D/A converters (2) to analog signals, LOG AMPLITUDE A and LOG AMPLITUDE B. These analog signals are sent to the IU and to the 8-to-1 multiplexers.

(5) As a group, these signals represent simulated RFA pod quadrant A and B analog data.

(6) Any of these analog signals may be selected by ANALOG ENABLE and ADDRESS SELECT from TSIFP (A7). The selected signal is output through one of three 8-to-1 multiplexers as ANALOG OUT to TSIFP (A7).

1-13. DETAILED OPERATION- Continued



TSD/A (A5 AND A6) BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

r. DBP (A14). Refer to the DBP (A14) block diagram. DBP (A14) controls data flow between bus 1 and bus 2. A microprocessor controls data flow and memory manipulation, while a coprocessor computes numerics.

(1) The 12 MHz oscillator input to clock generator produces 4 MHZ CLOCK to the microprocessor, coprocessor, bus arbiter, and bus controller. RESET from the clock generator resets the microprocessor, coprocessor, and bus arbiter. 3-BIT BUS STATUS (SO-2) from the microprocessor is applied to the bus arbiter, bus controller, and 4bit latch (sheet 2). 3-BIT BUS STATUS causes the bus arbiter to generate BUS 1 AND BUS 2 CONTROL SIGNALS. 3-BIT BUS STATUS also causes the bus controller to generate I/O READ/WRITE signals and MEMORY READ/WRITE signals. MEMORY READ/WRITE accesses SRAM when no other bus activity is present. I/O READ/WRITE tells an input or output device to read from or write to data bus. In addition, the bus controller generates INTAA1-B1 containing decoded interrupt information, which is sent to the programmable interrupt controller on the TSBUS (A13) card. INTAB1 is also sent to the programmable interrupt controller as an interrupt acknowledge.

(2) When INTERRUTI'S (INTO-7) are asserted, the programmable interrupt controller sends INTERRUPT to the microprocessor, which executes software to handle the interrupt. The interrupt controller has an 8-bit bi-directional data bus to the microprocessor address/data bus for address and data flow.

(3) The microprocessor has a 4-bit address/status bus (AD16-19) and a 16-bit bi-directional address/data bus (ADO-15) for address, status, and data flow. The address/status bus is the four most significant address lines for memory operations. During memory operations, status information is available on these lines.

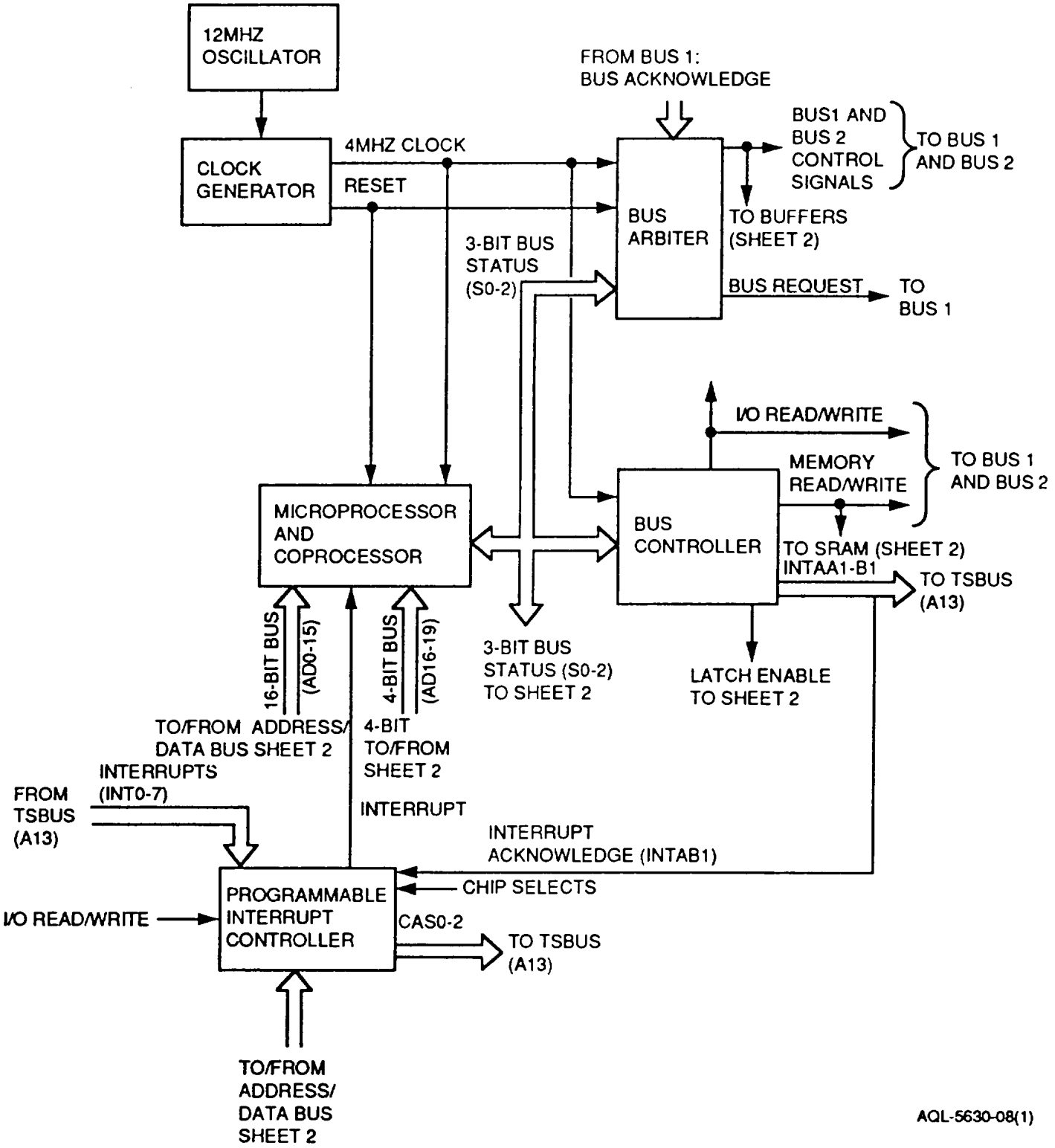
(4) When a DBP card is ready to use the bus, BUS REQUEST is sent to bus 1. When TSBUS (A13) grants access to the bus, it sends BUS ACKNOWLEDGE to DBP (A14).

(5) Decoded cascade information is sent to TSBUS (A13) on CASO-2.

(6) Address bits ADO-19 from the microprocessor are applied to the chip select generation circuitry via the 4 and 16-bit buses and latches. The chip select generation circuitry generates device-access chip selects for the programmable interrupt controller, serial communication interfaces, programmable interval counter (PIC), SRAM, EPROM, bus 1, and bus 2.

(7) Address data from the 4-bit and 16-bit latches are controlled by LATCH ENABLE from the bus controller. The 20-bit address bus also addresses a 48K x 8 SRAM and a 32K x 8 EPROM. The 16-bit address/data bus allows 16-bit data transfer between the microprocessor, bus 1, and bus 2. 16-bit data (DO0-15Bl1B2) is transmitted or received by the 16-bit transceivers (2 and 3). Address data from the address/status bus are buffered by the 20-bit buffers, which are enabled by control signals from the bus arbiter.

1-13. DETAILED OPERATION - Continued

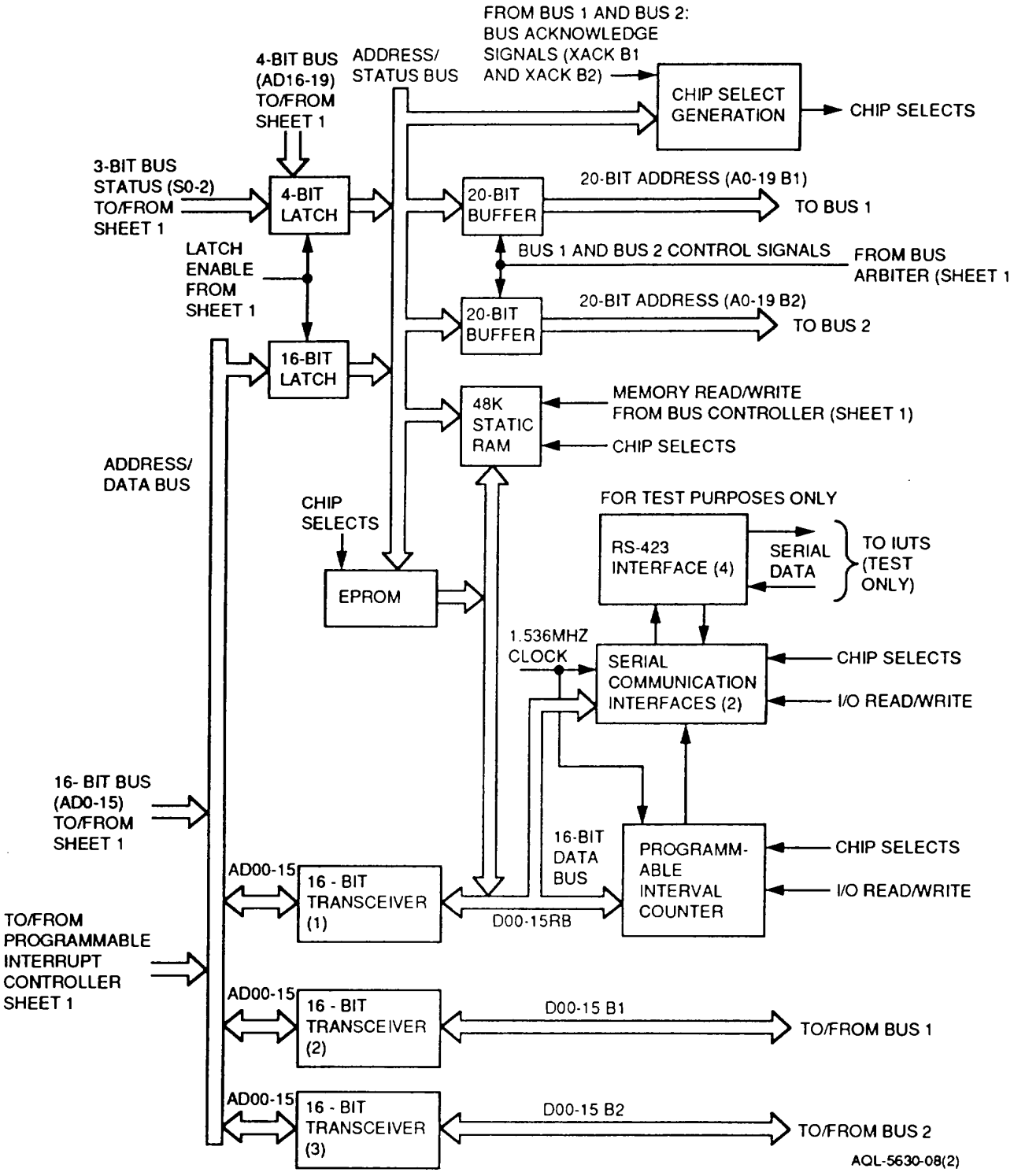


DBP (A14) BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

(8) The 16-bit transceiver (1) transfers data (D00-15RB) between the microprocessor and the RS-423 serial communication interfaces. The serial communication interfaces provide noise-free data transfer for diagnostic program load and cathode ray tube (CRT) test. The PIC (used as a baud rate generator) sets serial interface data transfer rates. The PIC and serial interfaces receive 1.536 MHZ CLOCK from the 1.536 MHz oscillator (part of the DBP). Serial interface data transfer is set at 153.6 KHz. Transmit and receive control signals are software-controlled interrupts from each serial interface. The 16-bit address/data bus allows address and data flow between each serial interface, the PIG, SRAM, EPROM, the microprocessor address/data bus, and the programmable interrupt controller (sheet 1). The EPROM contains software that controls DBP (A14).

1-13. DETAILED OPERATION - Continued



DBP (A14) BLOCK DIAGRAM

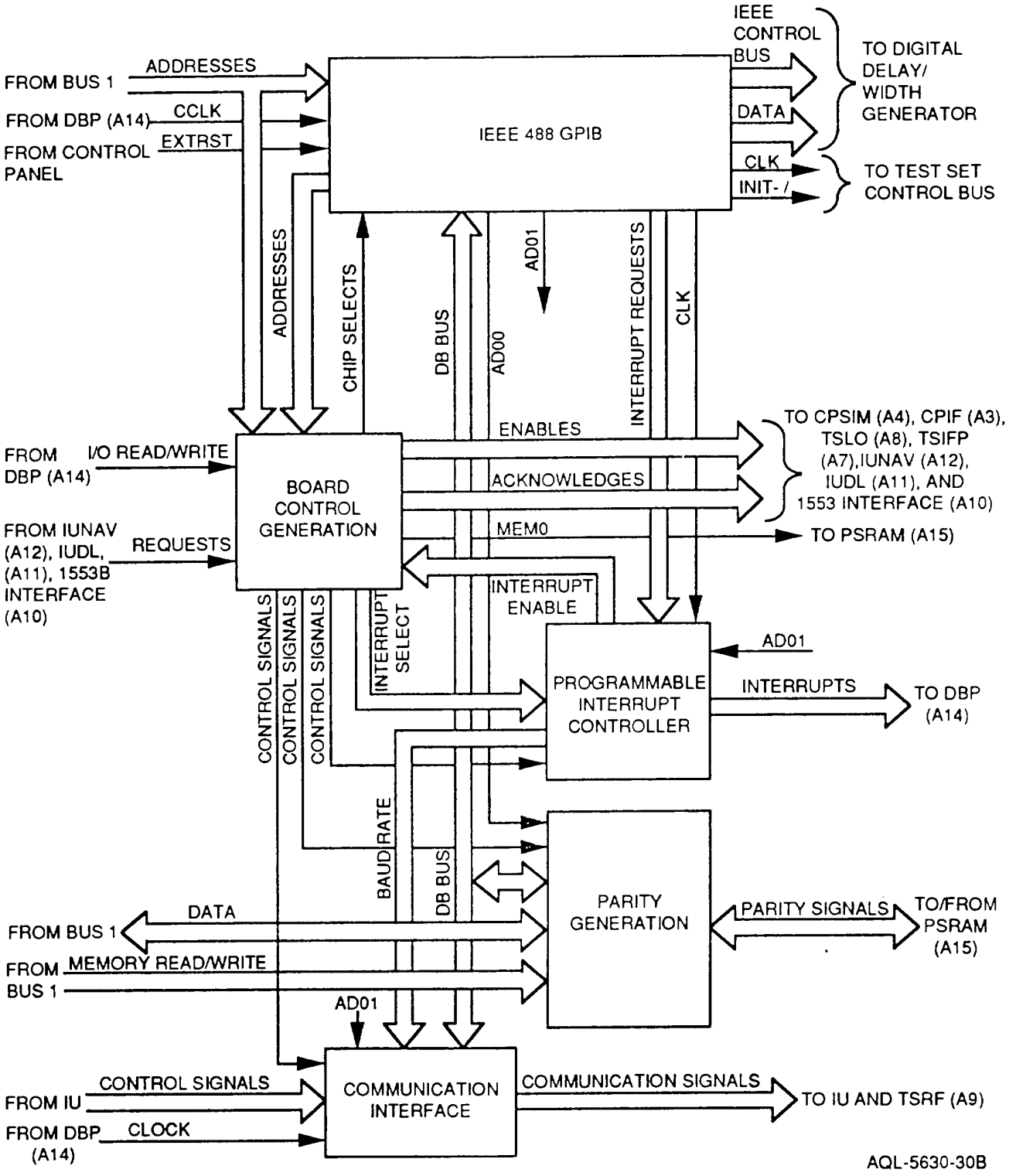
1-13. DETAILED OPERATION - Continued

a. TSBUS (A13). Refer to the TSBUS (A13) block diagram. The TSBUS provides a general purpose interface bus (GPIB) to communicate with digital delay/width generator and provides spare RS-232C channels, interrupts, and timers. The TSBUS (A13) is divided into five functional areas:

IEEE 488 GPIB
Board Control Generation
Programmable Interrupt Controller (PIC)
Parity Generation
Communication Interface

Refer to those areas for further information.

1-13. DETAILED OPERATION-Continued



TSBUS (A13) BLOCK DIAGRAM

1-13. DETAILED OPERATION-Continued

t. IEEE 488 GPIB. Refer to the IEEE 488 GPIB block diagram. The IEEE 488 consists of a 4 chip set that implements the IEEE-STD-488 digital interface GPIB.

The IEEE 488 GPIB section accepts:

- 8-bit data (DB00-07) from parity generation
- CHIP SELECTS from the board control generator
- 16-bit address lines (A00-15B1) from bus 1
- Clock signal CCLK from DBP (A14)
- External reset signal EXTRST from front panel

The IEEE 488 GPIB section outputs:

- IEEE CONTROL BUS to digital delay/ width generator
- 8-bit data (DI0-7) to digital delay/width generator
- Interrupt signals (IR10-7, IR20-7, IR30-7) to the PIC section
- Clock signal CLK to test set control bus and the PIC section
- RESET to the PIC section
- INIT-/ to test set control bus
- AD010 to the PIC and communication interface sections
- AD00 to the parity generation section

(1) When the operator presses SW2 (RESET) button on the test set front panel, the signal EXTRST is applied to a one-shot. The output of the one-shot, RESET, is used as a reset signal on and off the board. RESET is inverted to become INIT-/, and applied to the test set control bus.

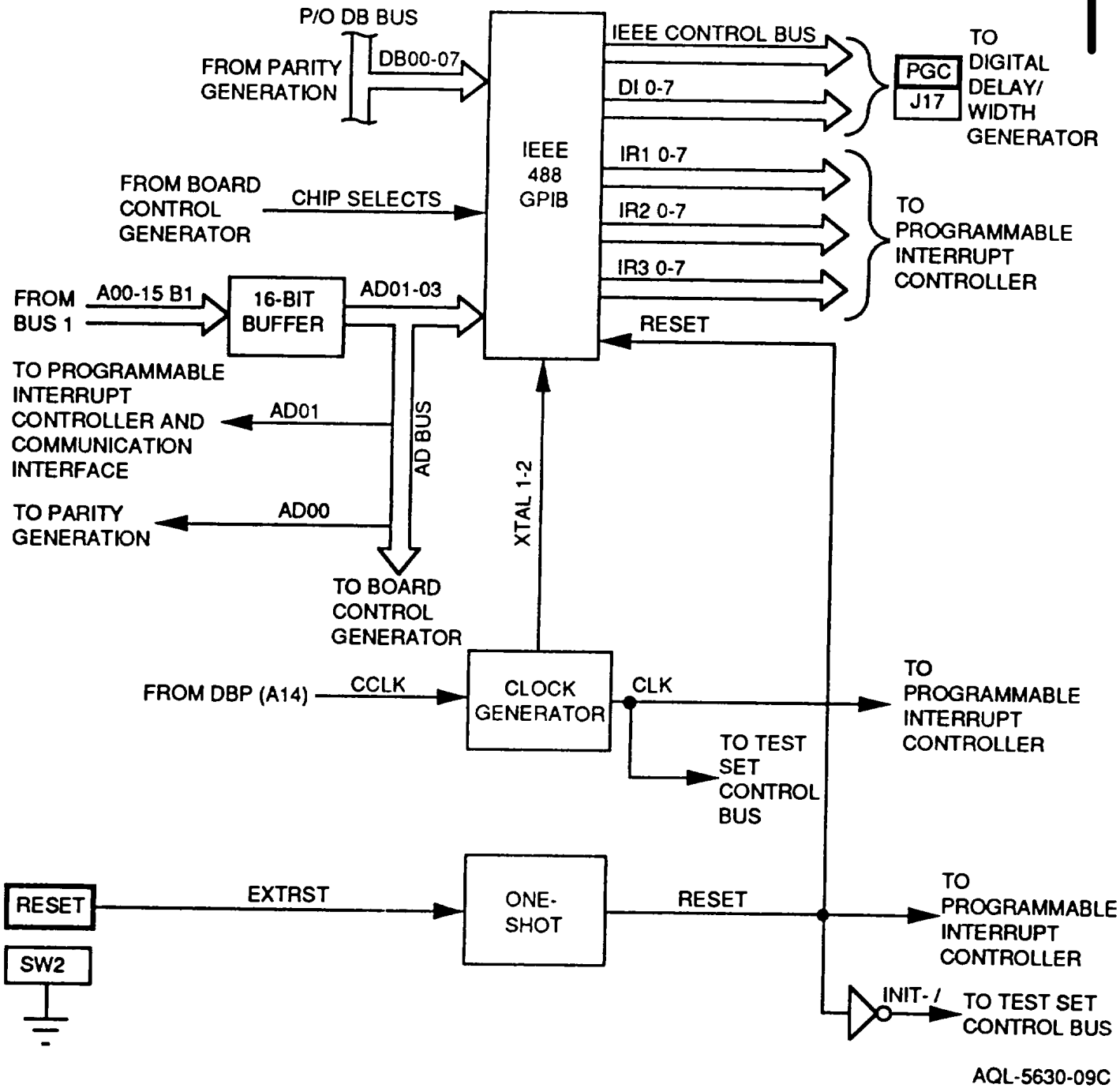
(2) Clock signal CCLK from DBP (A14) is applied to the clock generator and is output as CLK. CLK is used as a board clock, and is also sent to the test set bus. The clock generator also outputs XTAL 1 and 2 which are used by the IEEE 488 GPIB circuitry.

(3) Address lines A00-15B1 from bus 1 are applied to a 16-bit buffer and output on the AD bus. Address bits AD01-03 are applied to the IEEE 488 GPIB circuitry, AD01 is applied to the PIC and communication interface circuitry, and ADOO is applied to the parity generation circuitry.

(4) Data bits DB00-07 from the DB bus are applied to the IEEE 488 GPIB circuitry and output as DIO-7 for use by the digital delay/width generator.

(5) The remainder of the output signals, IEEE CONTROL BUS, IR10-7, IR20-7, and IR30-7, are generated by the interaction of data bits, address bits, and clock signals.

1-13. DETAILED OPERATION- Continued



IEEE 488 GPIB BLOCK DIAGRAM

1-13. DETAILED OPERATION-Continued

u. Board Control Generation. Refer to the board control generation block diagram. The board control generation section consists of a 16-bit buffer, a 6-bit latch, and five PALs. Its purpose is to create control and enable signals for use on the TSBUS (A13) as well as other cards.

The board control generation section accepts:

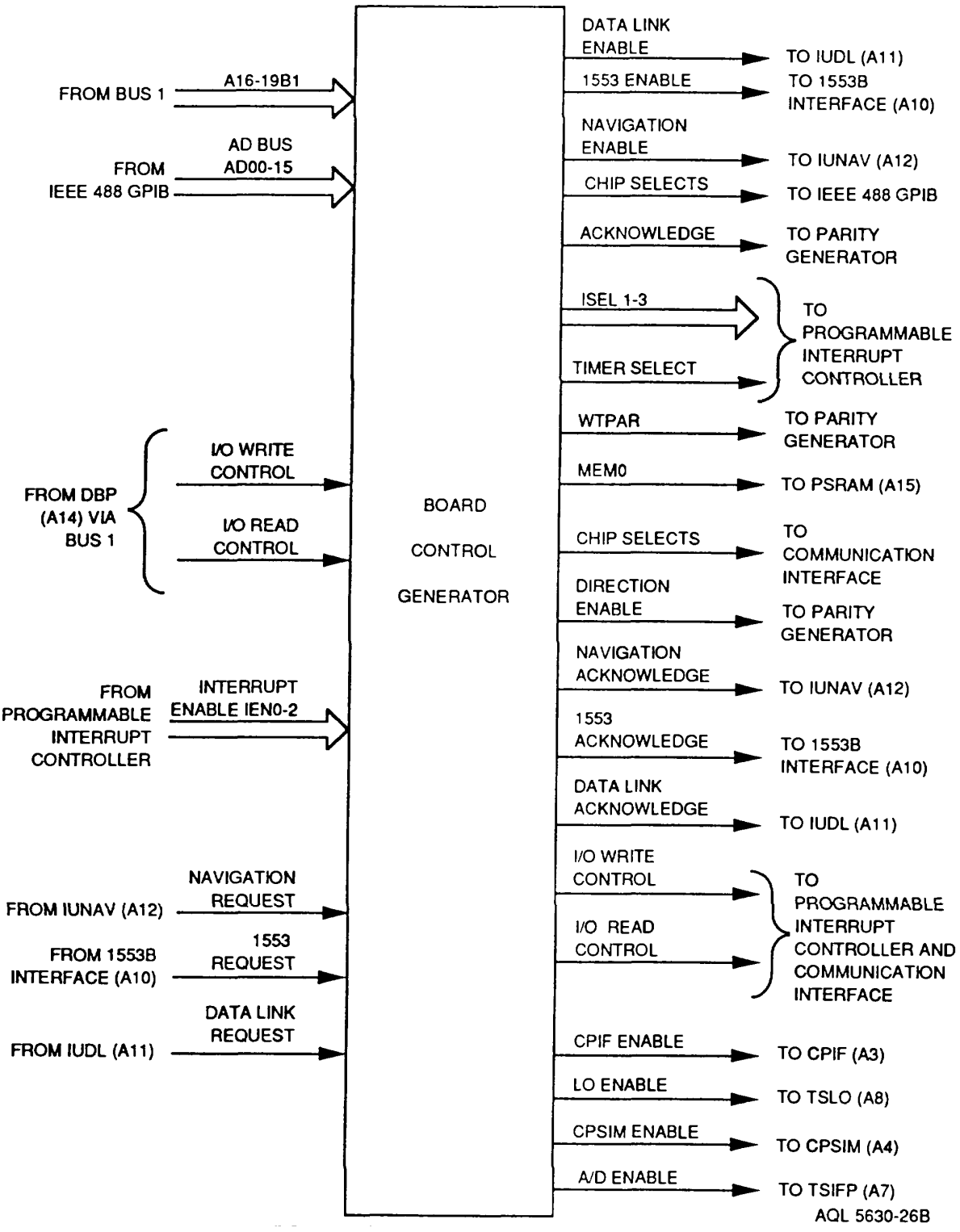
- 1553 REQUEST from 1553B interface (A10)
- Address bits A00-15 from the IEEE 488 GPIB section
- Address bits A16-19B1 from bus 1
- DATA LINK REQUEST from IUDL (All)
- /O WRITE CONTROL and I/O READ CONTROL from DBP (A14)
- INTERRUPT ENABLE IEN0-2 from the PIC section
- NAVIGATION REQUEST from IUNAV (A12)

The board control generation section outputs:

- 1553 ACKNOWLEDGE from 1553B interface (A10)
- 1553 ENABLE to 1553B interface (A10)
- A/D ENABLE to TSIFP (A7)
- ACKNOWLEDGE to the parity generation section
- CHIP SELECTS to the IEEE 488 GPIB and communication interface sections
- CPIF ENABLE to CPIF (A3)
- CPSIM ENABLE to CPSIM (A4)
- DATA LINK ACKNOWLEDGE from IUDL (All)
- DATA LINK ENABLE to IUDL (All)
- DIRECTION ENABLE to the parity generation section
- I/O WRITE CONTROL and 1O READ CONTROL to the PIC and communication interface sections
- LO ENABLE to TSLO (A8)
- MEMO to PSRAM (A15)
- NAVIGATION ENABLE and NAVIGATION ACKNOWLEDGE to IUNAV (A12)
- TIMER SELECT and interrupt signals ISEL1-3 to the PIC section
- Write parity signal (WTPAR) to the parity generation section

Based upon address inputs, read/write controls, interrupts, and external requests, the board control generator produces the outputs shown.

1-13. DETAILED OPERATION - Continued



BOARD CONTROL GENERATION BLOCK DIAGRAM

1-13. DETAILEDOPERATION-Continued

y. Parity Generation. Refer to the parity generation block diagram. The parity generation circuit consists of a 16-bit transceiver, a parity generator, a PAL, and a logic block. The parity generation circuitry outputs the parity of the upper and lower data bytes.

The parity generation section accepts:

- Data bits D00-15B1 from bus 1
- DIRECTION ENABLE from the board control generation section
- Address line ADOO from the IEEE 488 GPIB section
- ACKNOWLEDGE and WTPAR from the board control generation section
- Memory read/write commands MRDC and MWTC from bus 1
- Parity signals PARLO and PARHI from PSRAM (A15)

The parity generation section outputs:

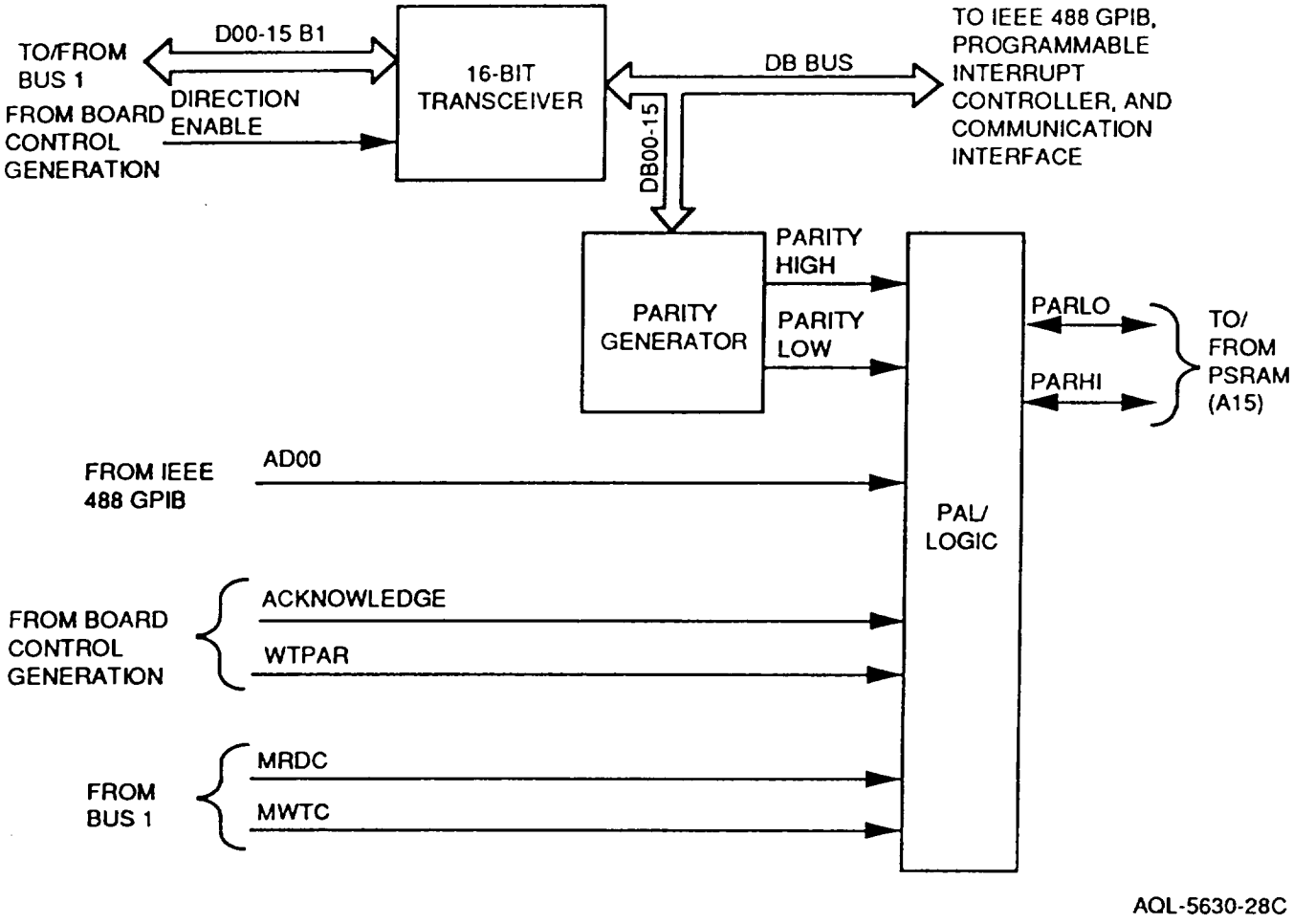
- Data bits D00-15B1 to bus 1
- Data on the DB bus to the IEEE 488 GPIB, PIC, and communication interface sections
- Parity signals PARLO and PARHI to PSRAM (A15)

(1) The 16-bit transceiver buffers data from bus 1 onto data bus DB.

(2) The parity generator applies PARITY HIGH and PARITY LOW to the PAL.

(3) The PAL and logic block are used to output parity information data based on the states of the address and read/write inputs.

1-13. DETAILED OPERATION - Continued



PARITY GENERATION BLOCK DIAGRAM

1-13. DETAILED OPERATION- Continued

w. PIC. Refer to the PIC block diagram. The PIC processes interrupt requests to produce interrupts. In addition, it furnishes different baud rate signals for the communication interface.

The PIC section accepts:

- 1553 INTERRUPT from 1553B interface (A10)
- Address bit AD01 from the IEEE 488 GPIB section
- Cascade control signals CASO-2 from DBP (A14)
- CLK, IR1 0-7, RESET, IR2 0-7, and IR3 0-7 from the IEEE 488 GPIB section
- CP INTERRUPT from CPIF (A3)
- Data bits DB00-07 from the parity generation section
- I/O WRITE CONTROL, 1O READ CONTROL, and TIMER SELECT from the board
- control generator section
- INTAA1-B1 from DBP (A14)
- Interrupt select signals ISELi-3 from the board control generator section
- SERIAL COMMUNICATIONS CONTROLLER INTERRUPT (RXRDY2-/) from IUDL (A11)

The PIC section outputs:

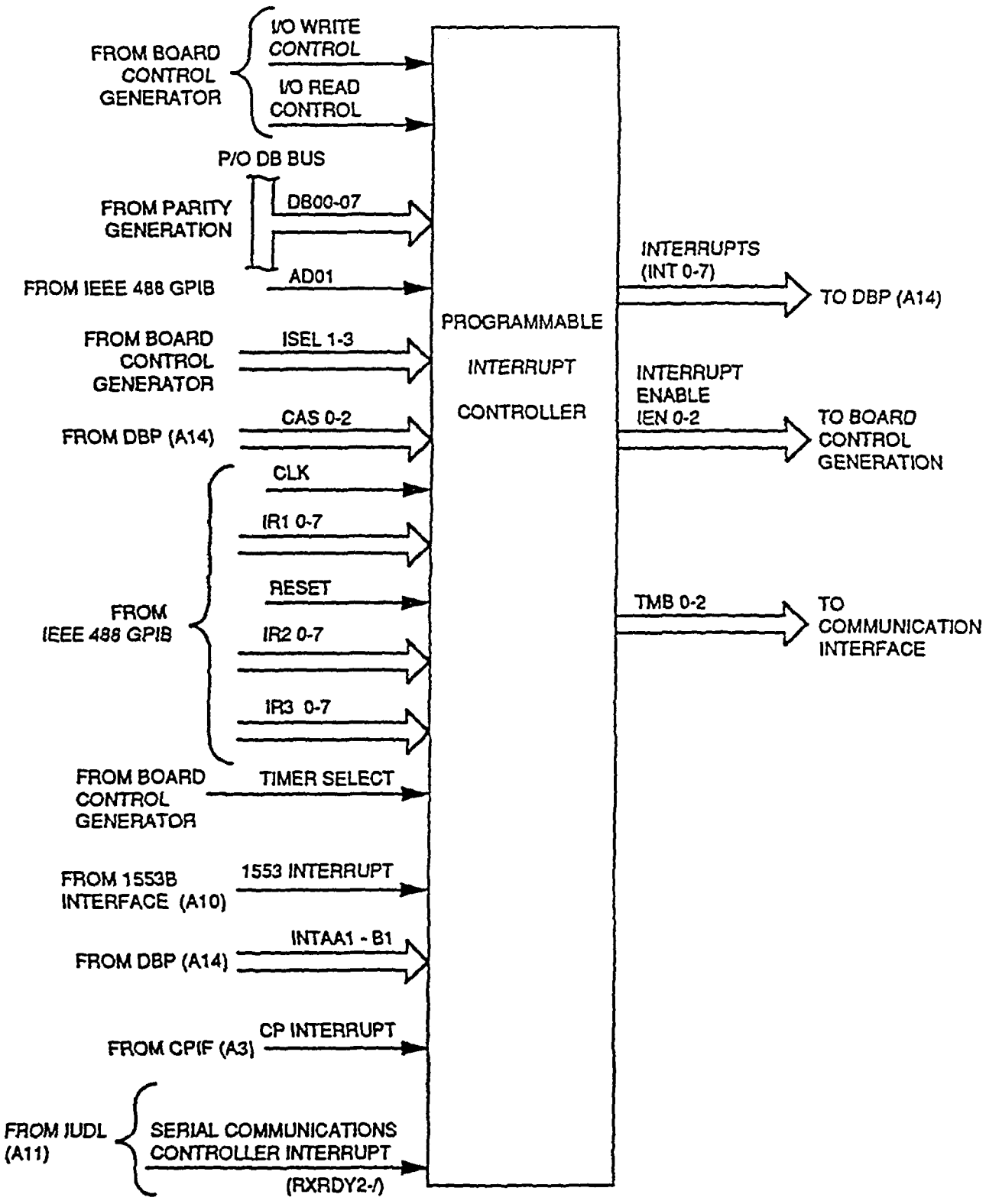
- Baud rate signals TMBO-2 to the communication interface section
- INTERRUPT ENABLE IENO-2 to the board control generation section
- Prioritized interrupt signals (INT0-7) to DBP (A14)

(1) The PIC section consists of three PIC, a PAL, and a programmable timer.

(2) The PIC accepts interrupt request inputs and outputs the prioritized interrupt signal INTERRUPTS.

(3) Based on TIMER SELECT, RESET, CLK, and address, and data inputs, the PIC section outputs baud rate signals TMBO-2.

1-13. DETAILED OPERATION - Continued



PIC BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

x. Communication Interface. Refer to the communication interface section block diagram. The communication interface section consists of three communication interface devices and a differential driver. The communication interface section provides serial communications between the IUTS and the IU.

The communication interface section accepts:

- Address bit AD01 from the IEEE 488 GPIB section
- Data bits DB00-07 from the parity generator section
- 1O READ CONTROL, I/O WRITE CONTROL, and CHIP SELECTS from the board control generator section
- 1.536 MHZ CLOCK from DBP (A14)
- Baud rate signals TMIB0-2 from the PIC
- CONTROL SIGNALS from the IU

The communication interface section outputs:

- Data terminal ready (DTR1-2) signals to the IU
- Serial communication signals (TXD1-2) to the IU
- Transmit data signal TXD3 to TSRF (A9) and tick generator (A2)

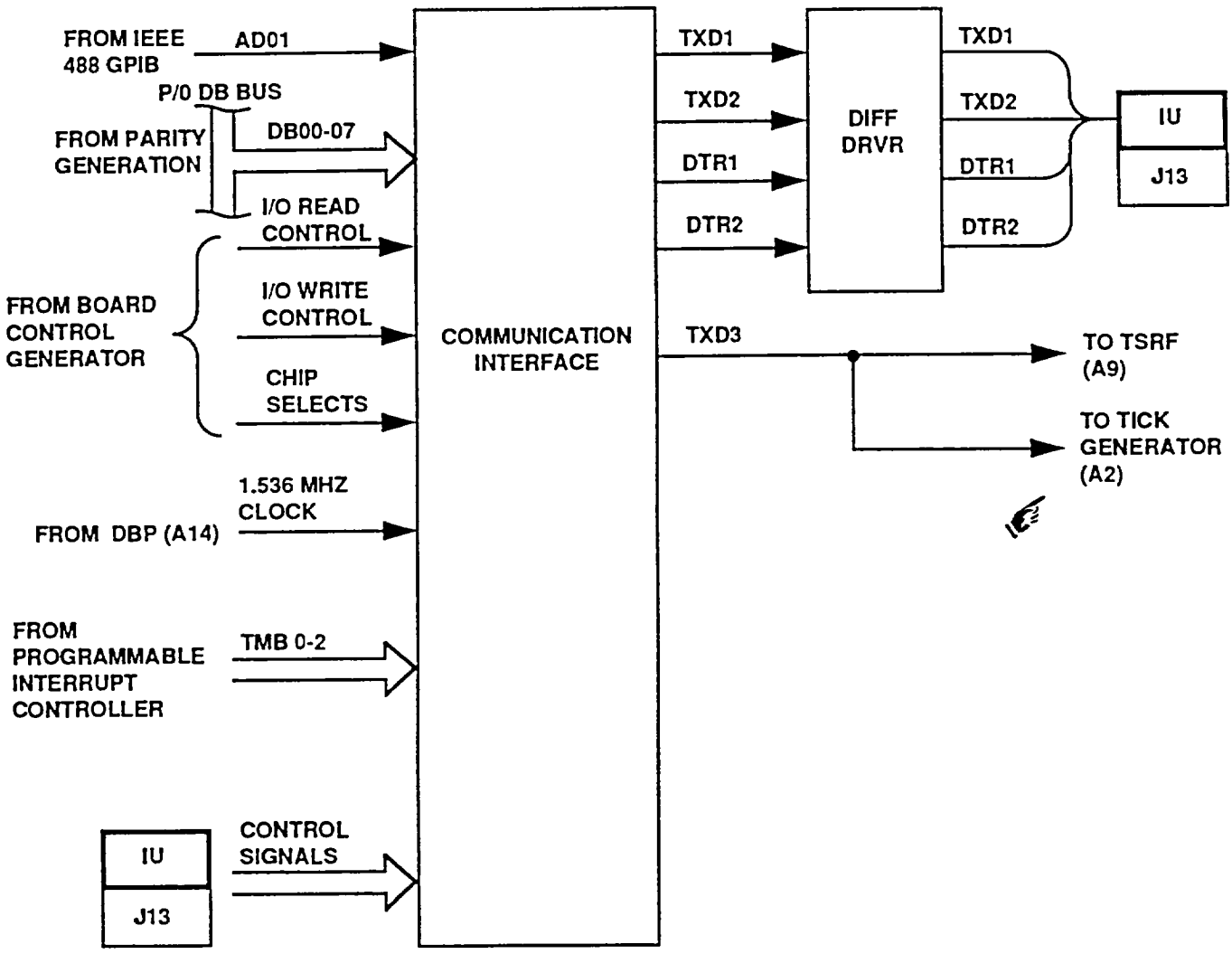
(1) Based upon the input signals, the communication interface circuitry outputs the signals shown.

(2) TXD 1-2 and DTR 1-2 are applied to the differential driver and output as differential signals.

(3) TXD3 is applied to TSRF (A9) as a phase calibration data signal.

(4) TXD3 is applied to tick generator (A2) as a GPS data signal.

1-13. DETAILED OPERATION - Continued



COMMUNICATION INTERFACE BLOCK DIAGRAM

1-13. DETAILED OPERATION- Continued

y. IUNAV (A12) Refer to the IUNAV (A12) block-diagram. IUNAV (A12) tests the IU navigation interface by generating simulated data patterns.

IUNAV (A12) accepts:

- NAVIGATION DATA, NAVIGATION CLOCK, and NAVIGATION SYNC from the IU
- 16-BIT DATA from bus 1
- NAVIGATION ACKNOWLEDGE and NAVIGATION ENABLE from TSBUS (A13)

IUNAV (A12) outputs:

- NAVIGATION INTERRUPT and CONTROL SIGNALS to the IU
- NAVIGATION REQUEST to TSBUS (A13)
- 20-BIT ADDRESS to bus 1
- 16-BIT DATA to DBP (14) via bus 1
- SERIAL DATA to IU

(1) IUNAV (A12) receives navigation data, clock, and sync (control) signals from the IU. Differential receivers convert incoming differential signals to serial TTL signals. Converted navigation data signals are sent to the 32-bit serial-to-parallel shift register. The most significant output bits (RND 16-30) are sent to the 16-bit MSB latch (1). MSB enable signal ENMSB is applied to the latch (1), enabling stored data onto the data bus. RND31-X is also applied to the latch (1), becoming the most significant bit of the data word enabled onto the data bus. Data on the data bus is latched to the 16-bit transceiver and onto bus 1. The least significant output data bits (RND00-15) from the 32-bit serial to parallel shift register are applied to the 16-bit LSB latch (2). LSB enable signal ENLSB enables this data onto the data bus.

(2) IUNAV (A12) is accessed by sending NAVIGATION REQUEST to TSBUS (A13), which responds with NAVIGATION ACKNOWLEDGE and NAVIGATION ENABLE. These signals together with navigation timing and control signals generate signals which control data flow and address generation.

(3) Address lines assert when NAVIGATION ACKNOWLEDGE asserts. Navigation data from the navigation system writes to IU memory. The IU reads navigation data from memory and sends it to the CP at BOL operation.

(4) Navigation signals also access a PROM segment through an 8-bit latch. PROM data is added to navigation data via the 15-bit adder to generate addresses for PSRAM (A15) on bus 1 via the 20-bit buffer. NVINT is generated after data transfer to IU memory, sent to the navigation request and control signal generation circuits, and output as NAVIGATION INTERRUPT.

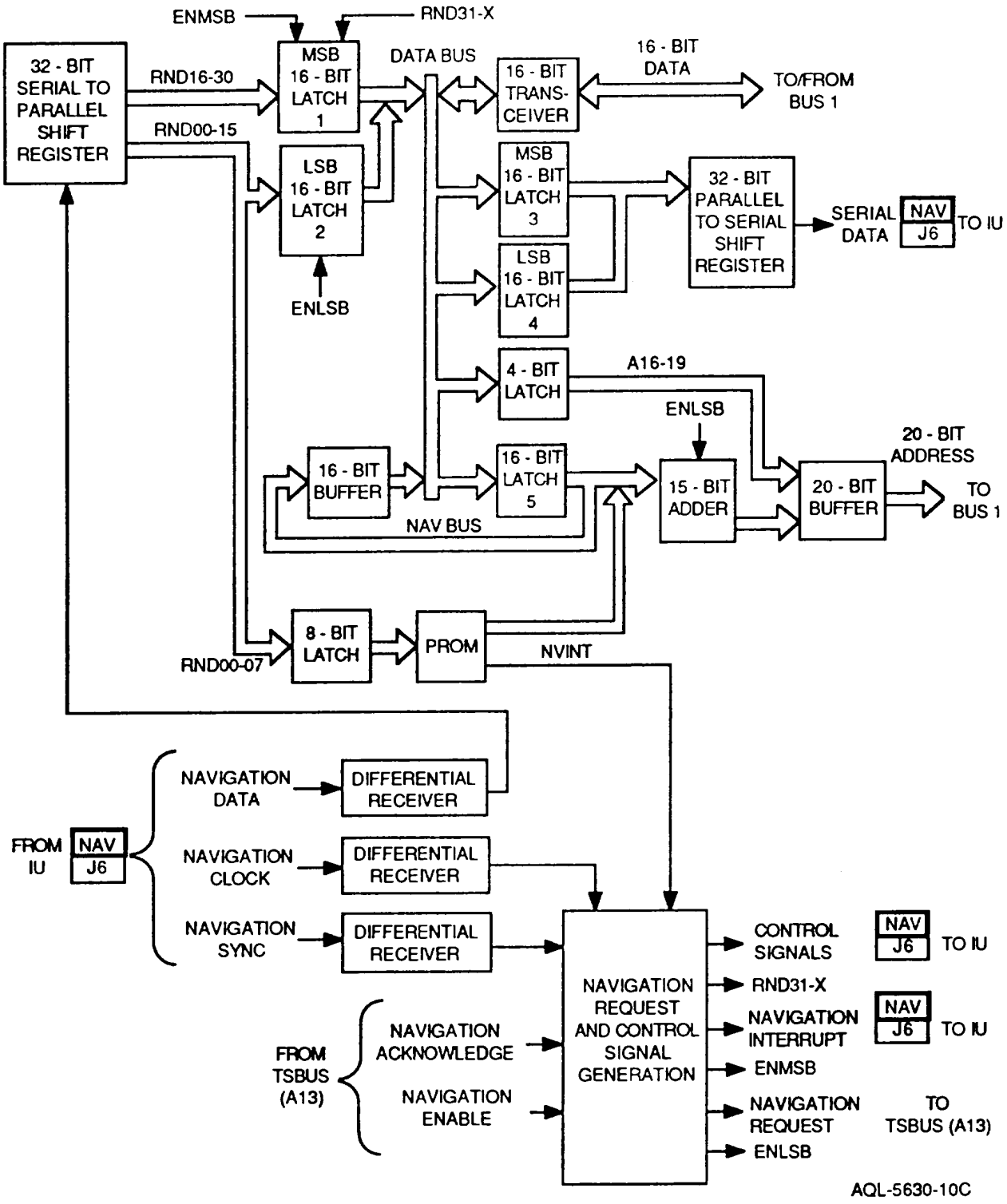
(5) Navigation signals are sent via two 16-bit latches (3) and (4) to a 32-bit parallel-to-serial shift register which converts navigation signals back to serial format and sends them to the IU.

(6) 16-bit data from the DBP enters IUNAV (A12) via bus 1. The data is applied to the internal bus via the 16-bit transceiver.

(7) Address data from bus 1 is applied to the 16-bit latch (5), then latched into the 15-bit adder. PROM data from the 8-bit latch is also applied to the adder, where it is added to the address data The output of the 15-bit adder, A1-15, is latched into the 20-bit buffer by ENLSB where it is combined with the output of the 4-bit latch, A16-19. Together, these inputs create the 20-bit address output.

(8) Address bits from the 16-bit latch (5) are sent to the internal bus via the 16-bit buffer. From there they are sent to the DBP via the 16-bit transceiver in order to verify that the address sent out of the DBP is the same one received by IUNAV (A12).

1-13. DETAILED OPERATION- Continued



IUNAV (A12) BLOCK DIAGRAM

1-13. DETAILED OPERATION- Continued

z. PSRAM (A15). Refer to the PSRAM (A15) block diagram. PSRAM (A15) stores operating and diagnostic programs in 48K of ROM and stores selected programs and data in 128K of RAM.

PSRAM (A15) accepts:

- MEMORY ENABLE (MEMO) from TSBUS (A13)
- Parity bits PARHI and PARLO from TSBUS (A13)
- 16-bit data (DO-15B1) from bus 1
- YO CONTROL, MEMORY READ, MEMORY WRITE BUS 1, AND BHEN 1 from bus 1
- Address lines A00-A19B1 from bus 1

PSRAM (A15) outputs:

- 16-bit data (DO-15B1) to bus 1
- Parity bits PARHI and PARLO to TSBUS (A13)
- ACKNOWLEDGE to bus 1

(1) PSRAM (A15) is configured as follows:

- 64K x 18 bits of SRAM (12-32K x 3-bit memory modules)
- 96K x 16 bits of ROM (12-16K x 8-bit memory chips)

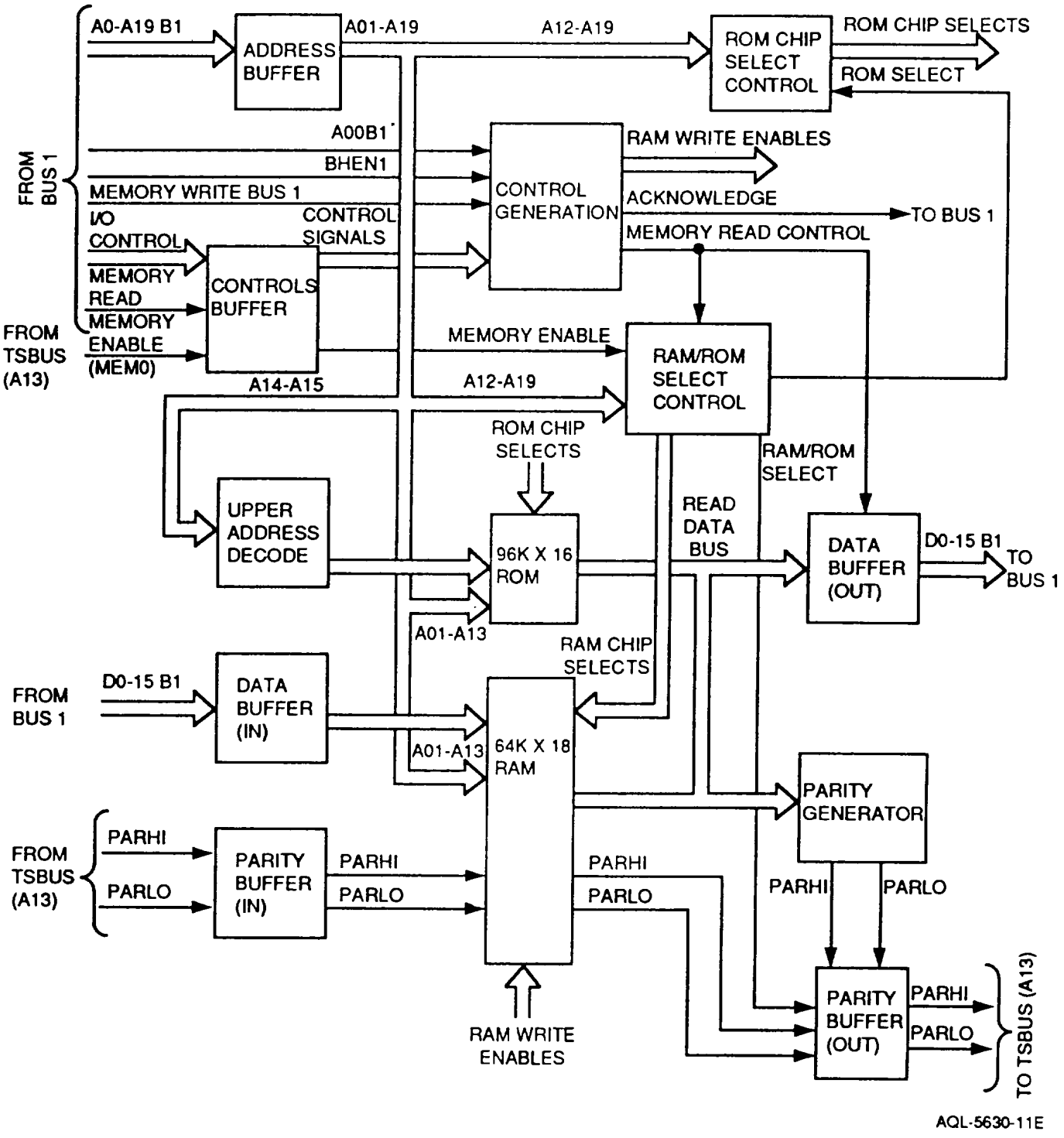
(2) Memory is accessed as follows:

- Address bits AOO0-19B1 are buffered and used throughout the card.
- I/O CONTROL, MEMORY ENABLE, and MEMORY READ are applied to the controls buffer, producing CONTROL SIGNALS and MEMORY ENABLE.
- MEMORY WRITE BUS 1, AOOB1, and BHEN1 are applied to the control generator along with CONTROL SIGNALS, producing several outputs.
- MEMORY READ CONTROL from the control generator is applied to the RAM/ROM select control. MEMORY ENABLE and address bits A12-A19 are also applied, producing RAM CHIP SELECTS and ROM SELECT. RAM CHIP SELECTS are applied to the RAM circuits.
- ROM SELECT is applied to the ROM chip select control circuitry along with address bits A12-A19 to produce ROM CHIP SELECT. This is applied to the ROM circuits.
- RAM WRITE ENABLES are applied to the RAM circuits.

(3) Data handling:

- Address bits A14 and A15 are applied to ROM via the upper address decoder. Address bits A01-A13 are applied to ROM directly. When ROM CHIP SELECT is active, data is read from ROM in accordance with the address received. The data is applied to the data buffer (out) and the parity generator via the read data bus.
- Data bits DO-15B1 are aplied to RAM via the data buffer (in). Parity bits PARHI and PARLO are applied to RAM via the parity buffer (in). Data and parity words are written into RAM when RAM CHIP SELECT and RAM WRITE ENABLE are active, in accordance with the address received.
- Data is read from RAM as selected by RAM CHIP SELECT, in accordance with the address received. This data is applied to the output data bus via the data buffer (out) and to the parity generator via the read data bus. Two parity bits are simultaneously output via the parity buffer (out).

1-13. DETAILED OPERATION- Continued



PSRAM (A15) BLOCK DIAGRAM

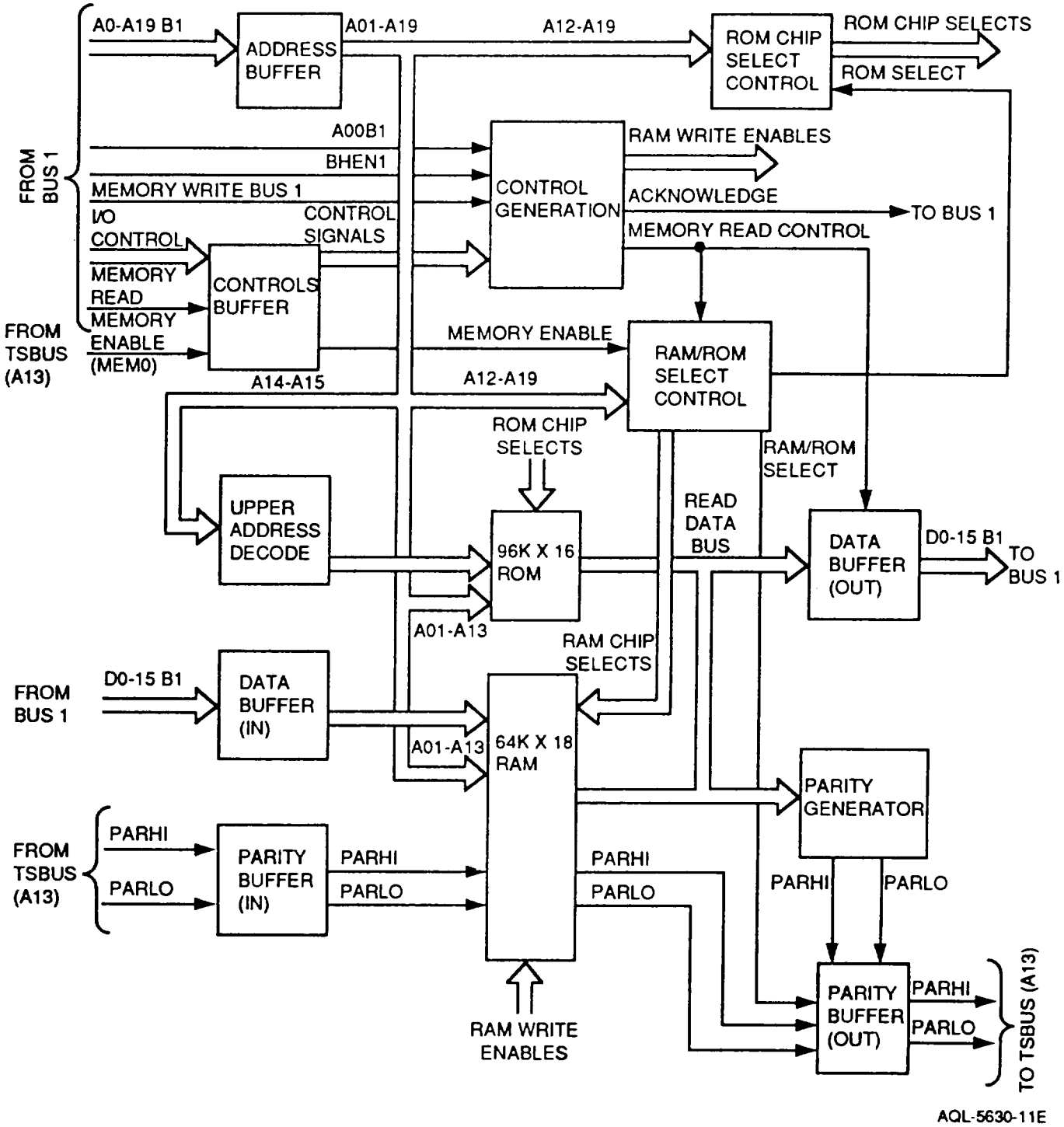
1-13. DETAILED OPERATION- Continued

- Data is read from ROM onto the output data bus via the data buffer (out). The data also goes to the parity generator which generates the parity and adds the upper and lower parity bits to ROM data via the parity buffer (out).

- RAM/ROM SELECT determines whether parity is read from the parity generator or RAM.

- ACKNOWLEDGE is sent to bus 1 to indicate completed memory transaction.

1-13. DETAILED OPERATION - Continued



PSRAM (A15) BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

aa. IUD, (A11). Refer to the IUDL (All) block diagram. IUDL (All) functions as a high-speed serial channel to test the IUDL interface in the IU, plus self-test using loop-back.

IUDL (A11) accepts:

- DATA LINK ACKNOWLEDGE and DATA LINK ENABLE from TSBUS (A13)
- 16-bit data (DO-15B1) from DBP (A14) via bus 1
- 20 KHZ CLOCK, 1.15 MHZ CLOCK, and SERIAL DATA RECEIVED from J11 (data link input)

IUDL (All) outputs:

- CONTROL SIGNALS to bus 1
- DATA LINK REQUEST to TSBUS (A13)
- SERIAL COMMUNICATIONS CONTROLLER INTERRUPT to TSBUS (A13)
- DATA INTERRUPT to TSBUS (A13)
- 16-bit data (DO-15B1) to DBP (A14) via bus 1
- 20-bit address (AO-15 and A16-19) to bus 1
- SERIAL DATA TRANSMITTED to J11 (data link output)

(1) IUDL (A11) sends DATA LINK REQUEST to TSBUS (A13) which responds with DATA LINK ACKNOWLEDGE and DATA LINK ENABLE. These signals address three PROM segments.

(2) SERIAL COMMUNICATIONS CONTROLLER INTERRUPT is generated at the completion of the serial communications operation.

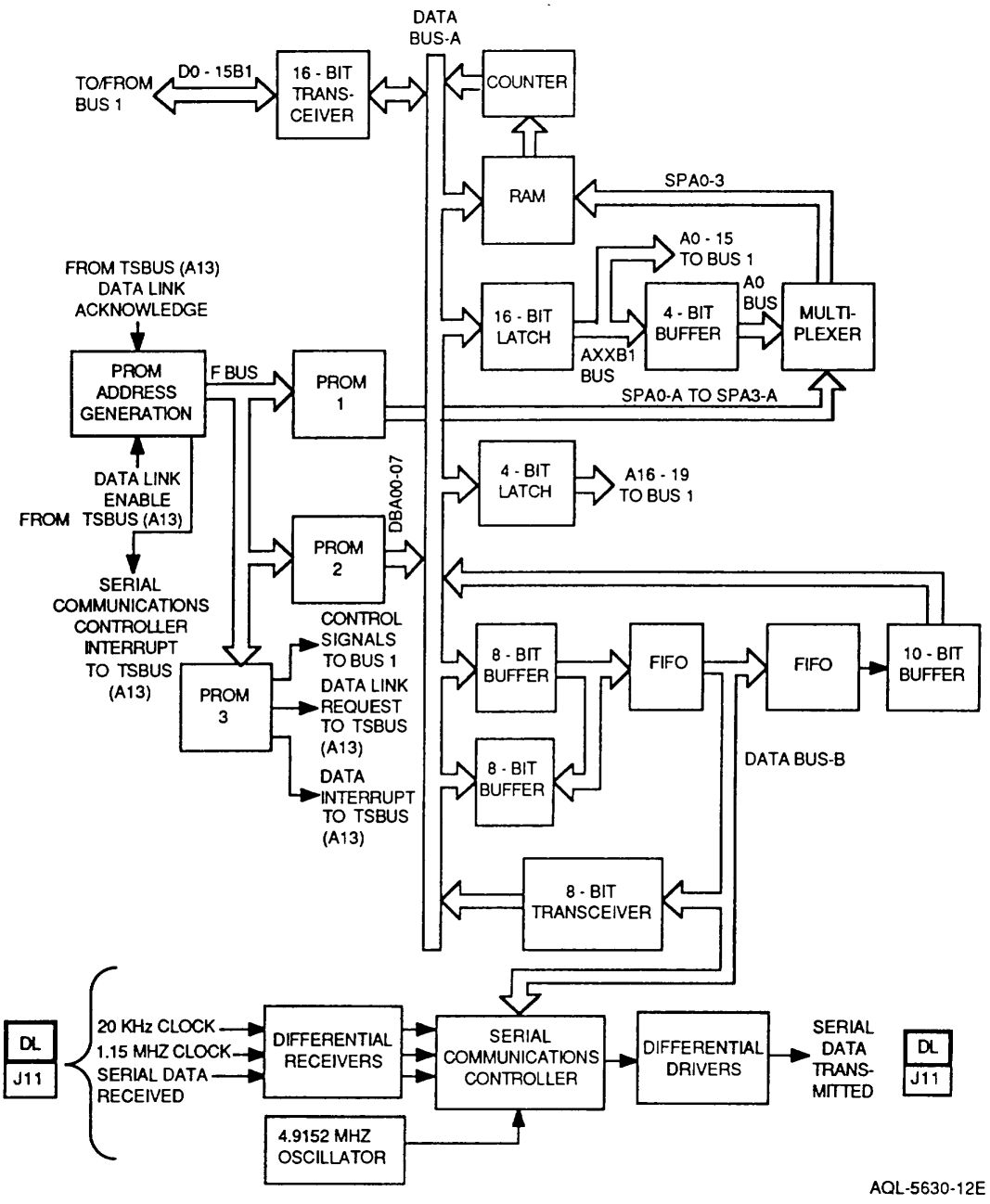
(3) Upper PROM segment (1) output addresses (SPAO-A to SPA3-A) are multiplexed through to a RAM segment. The middle PROM segment (2) puts 8-bits data (DBA00-07) on data bus-A. The lower PROM segment (3) outputs CONTROL SIGNALS, DATA LINK REQUEST, and RECEIVE DATA INTERRUPT.

(4) CONTROL SIGNALS control data flow through the interface. DATA INTERRUPT asserts when data from the data link is put onto bus 1 by the interface.

(5) The interface connects with bus 1 via a 16-bit transceiver. A RAM segment loads a 16-bit counter which generates the 20 address bits needed for static RAM access on bus 1. The counter output latches through as address bits AO-15, and as address bits A16-19. Four least significant address bits are buffered and multiplexed through to address RAM.

(6) A serial communications controller controls all IU and data link serial communications. The controller is clocked by 4.9152 MHz clock from 4.9152 MHz oscillator. The controller receives 20 KHz receive clock, 1.15 MHz transmit clock, and serial data from data link via differential receivers. The controller outputs serial data to data link via differential drivers. Data from the data link is converted to parallel data and sent to bus 1 via the bi-directional data bus. Data transferred to data link is sent to the controller via the bi-directional data bus where it is converted to serial data. The controller has a built-in-testmode for system verification.

1-13. DETAILED OPERATION - Continued

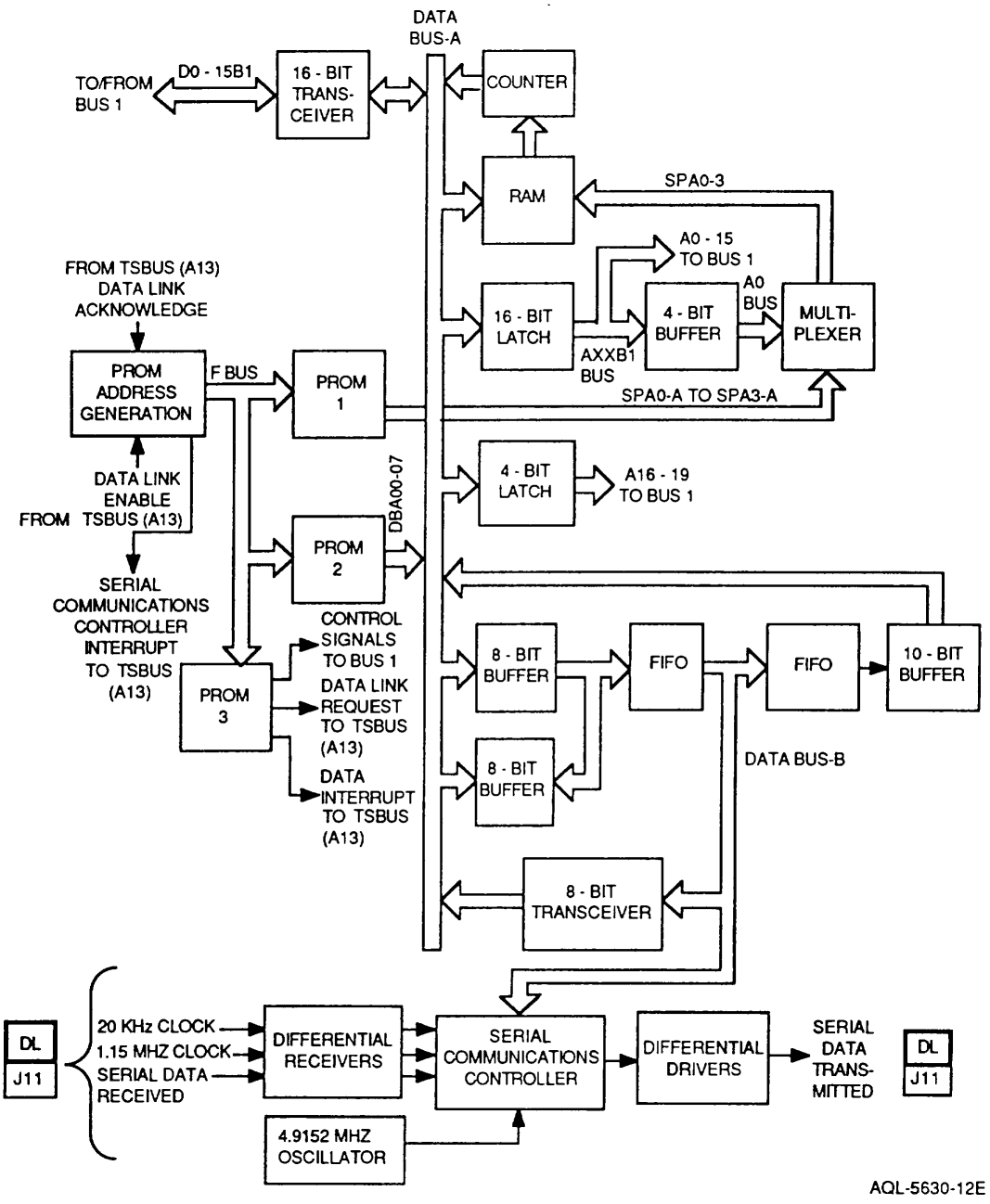


IUDL (A11) BLOCK DIAGRAM

1-13. DETAILED OPERATION-Continued

(7) Data from the controller is put into FIFO memory, buffered, and sent to bus 1 via the transceiver. Data written to the controller from bus 1 is buffered and written into FIFO memory before being sent to the controller. The 8-bit transceiver routes control words between the data link and the IU via the software-controlled controller.

1-13. DETAILEDOPERATION - Continued



IUDL (A11) BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

ab. 1553R Interface (A10). Refer to the 1553B interface (A10) block diagram. Per MILSTD1553B, command, status, and data words are 20 bits each: 16 data bits, 3 sync bits, and 1 parity bit. Command and status words are interchanged between IUTS and IU via 1553B interface (A10) interface. The 1553B, a standard military interface, communicates with the IU and converts parallel data to serial data for transmission, or receives serial data and converts to parallel data.

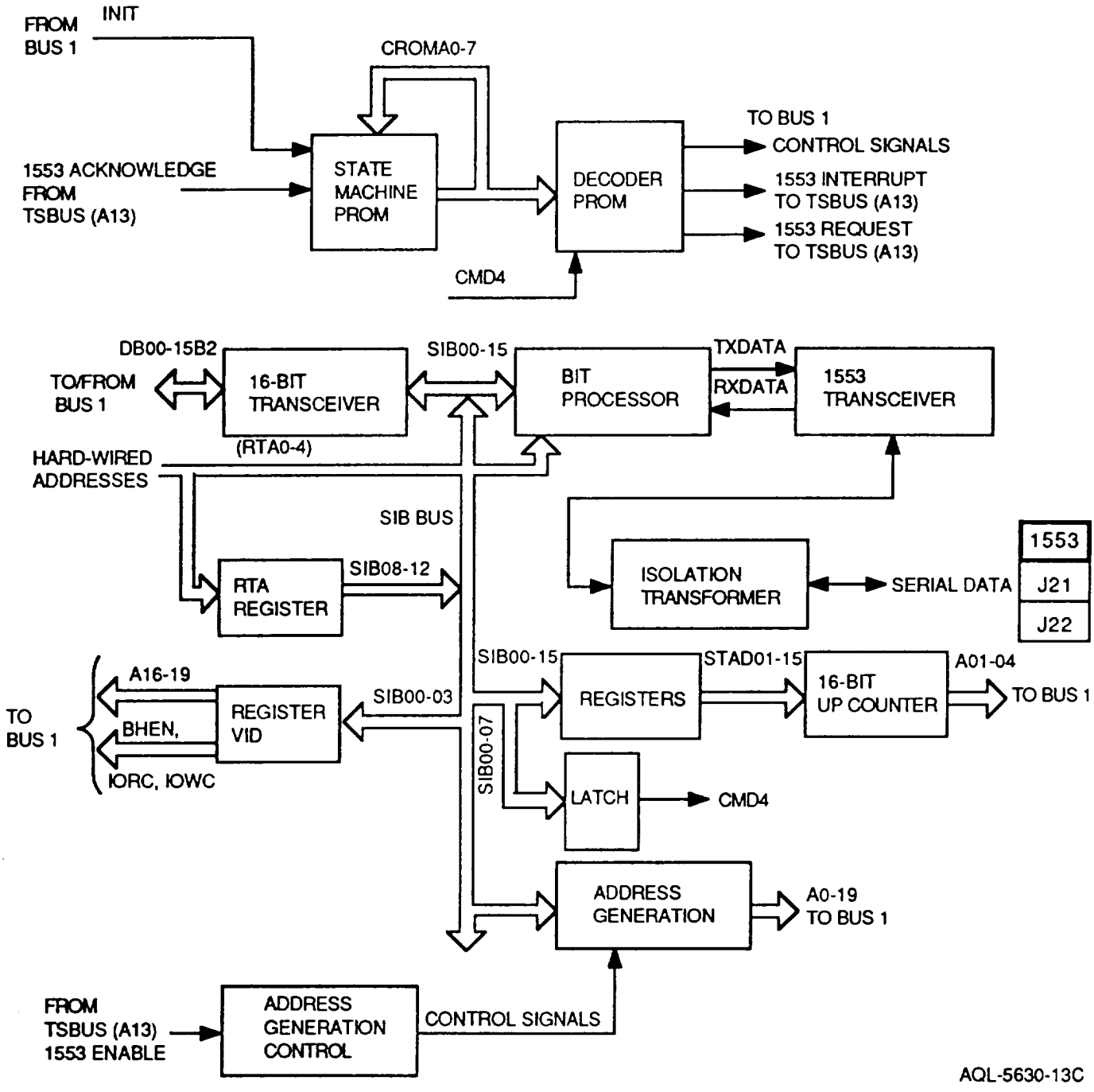
(1) A 16-bit transceiver connects 16-bit data (DB00-15B2) to the bit processor; data flows in either direction. The bit processor detects bit errors with parity detection and converts data from parallel to serial or serial to parallel. The 1553 transceiver controls serial data input and output of the bit processor. The isolation transformer connects to and isolates the transceiver from the serial data bus.

(2) When 1553B interface (A10) is required for data transmission or receiving, 1553 ENABLE from TSBUS (A13) is applied to address generation control circuits. The address generation control circuits produce CONTROL SIGNALS for the address generation circuits. The address generation decoder circuits provide address bits AO-19, which are applied to bus 1. 1553 REQUEST from the PROM is sent to TSBUS (A13), which then returns 1553 ACKNOWLEDGE to 1553B interface (A10). INIT resets PROM addressing, causing required control signal generation. INIT also resets the state machine, causing address word CROMAO-7 to be applied to the decoder PROM, which then generates output signals. These signals may consist of CONTROL SIGNALS, 1553 INTERRUPT, or 1553 REQUEST, depending upon the address word and latch output CMD4. CROMAO-7 is also applied as an input to the state machine, which causes it to output a different address word. This process continues until the next INIT is received.

(3) The hard-wired address input, RTAO-4, is applied to the bit processor and the RTA register. The output of the RTA register, SIB0812, is applied to the SIB bus. SIB00-03 is applied to a register, which outputs several signals. They are bus high enable signal BHEN, read/write control signals IORC and IOWC, and 4 bits of address data (A16-19). The output signals are sent to bus 1 which are used to access SRAM. SIB00-15 are registered and output to a 16-bit up counter as STAD01-15. This represents a start address that preloads the counter. The output of the counter is a 4-bit address (A01-04) to bus 1.

(4) A command word is applied to the 1553B interface (A10) as part of SERIAL DATA After it is routed to the bit processor via the isolation transformer and 1553 transceiver, it is placed on the SIB bus. SIB00-07 is applied to a latch. Latch output CMD4 is applied to the decoder PROM as part of the CROM address and is used as a bank select for the decoder PROM. When the bit processor detects a receive command word followed by a specified number of data words (DB00-15B2), a single status word on the SIB bus response is placed on the serial 1553B bus (after message validation). If more than one bit processor is placed on the 1553B bus, only the bit processor with a hard-wired address matching the 5-bit address field of the command status word is active at any given time. Similarly, if the bit processor detects a transmit command word, the status word response is again placed on the 1553B interface bus; however, in this case, the status word is followed by a specified number of data words. The data words are formed by latching the contents of PSRAM (A15) onto bus 2 for conversion to serial format within the bit processor. The process is concluded by transmitting the serial data to the IU.

1-13. DETAILED OPERATION-Continued



1553B INTERFACE (A10) BLOCK DIAGRAM

1-13. DETAILED OPERATION - Continued

ac. Oscillator (C1). Refer to the oscillator (G1) block diagram. Oscillator (G1), a rubidium oscillator, generates a high-accuracy 10 MHz sinewave for external use.

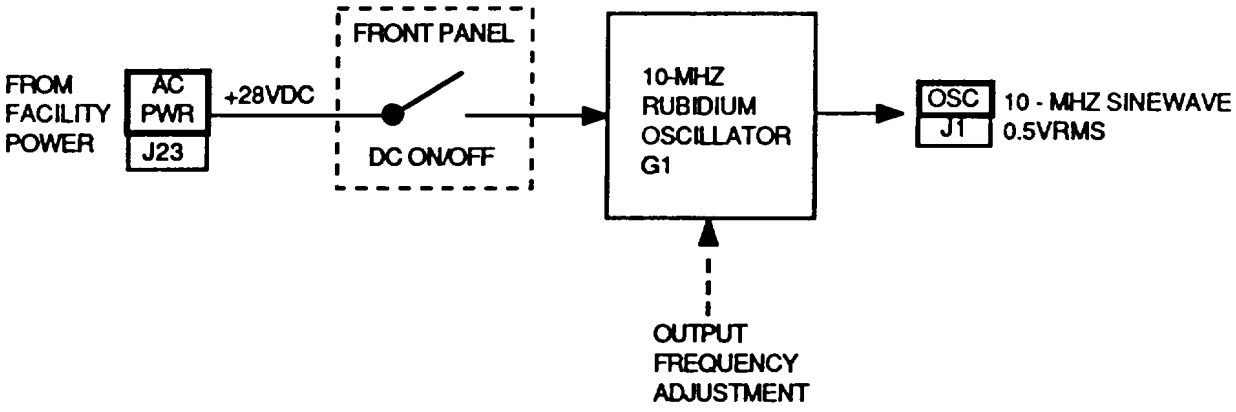
Oscillator (G1) accepts:

- +28 Vdc from facility power via the front panel DC ON/OFF switch
- Manual output frequency adjustment

Oscillator (G1) outputs:

- A 10 MHz sinewave of 0.5 volt root-means-square (RMS), OSCOUT, is fed directly to front panel connector J1

1-13. DETAILED OPERATION- Continued



OSCILLATOR (G1) BLOCK DIAGRAM

1-13. DETAILED OPERATION- Continued

ad. Power Supply (A17). Refer to the power supply (A17) block diagram. Power supply (A17) consists of four power supply modules mounted on a printed wiring board.

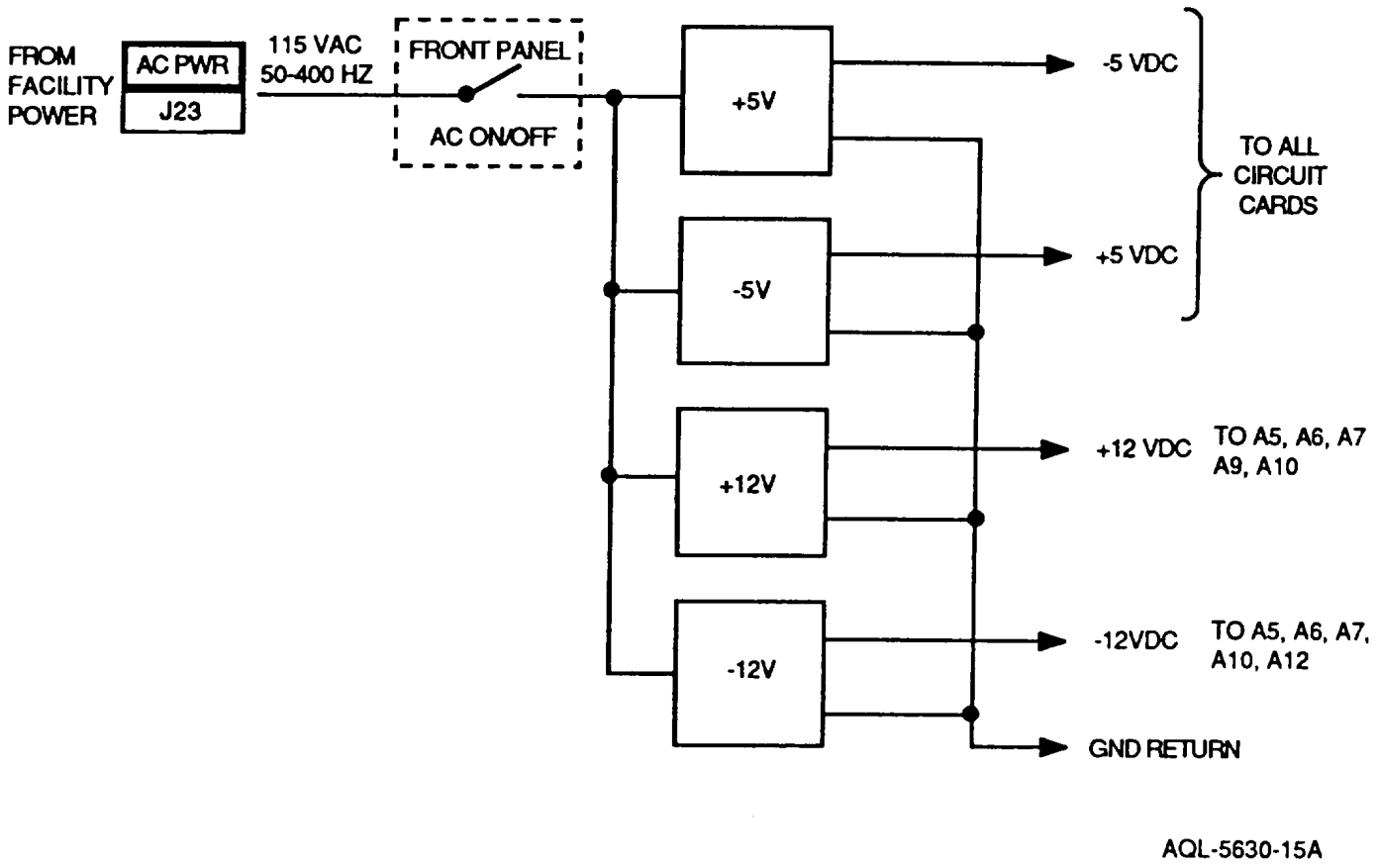
Power supply (A17) accepts:

- 115 Vac, 50 to 400 Hz, from facility power via front panel AC ON/OFF switch

Power supply (A17) outputs:

- +5 Vdc to all circuit cards
- - 5 Vdc to all circuit cards
- +12 Vdc to A5, A6, A7, A9, A10 circuit cards
- - 12 Vdc to A5, A6, A7, A10, A12 circuit cards

1-13. DETAILED OPERATION-Continued



POWER SUPPLY (A17) BLOCK DIAGRAM

CHAPTER 2

OPERATING INSTRUCTIONS

CHAPTER CONTENTS **Page**

Section I. DESCRIPTION AND USE OF OPERATOR'S CONTROLS AND INDICATORS

2-1. GENERAL

This section describes the function of the IUTS operator controls and indicators.

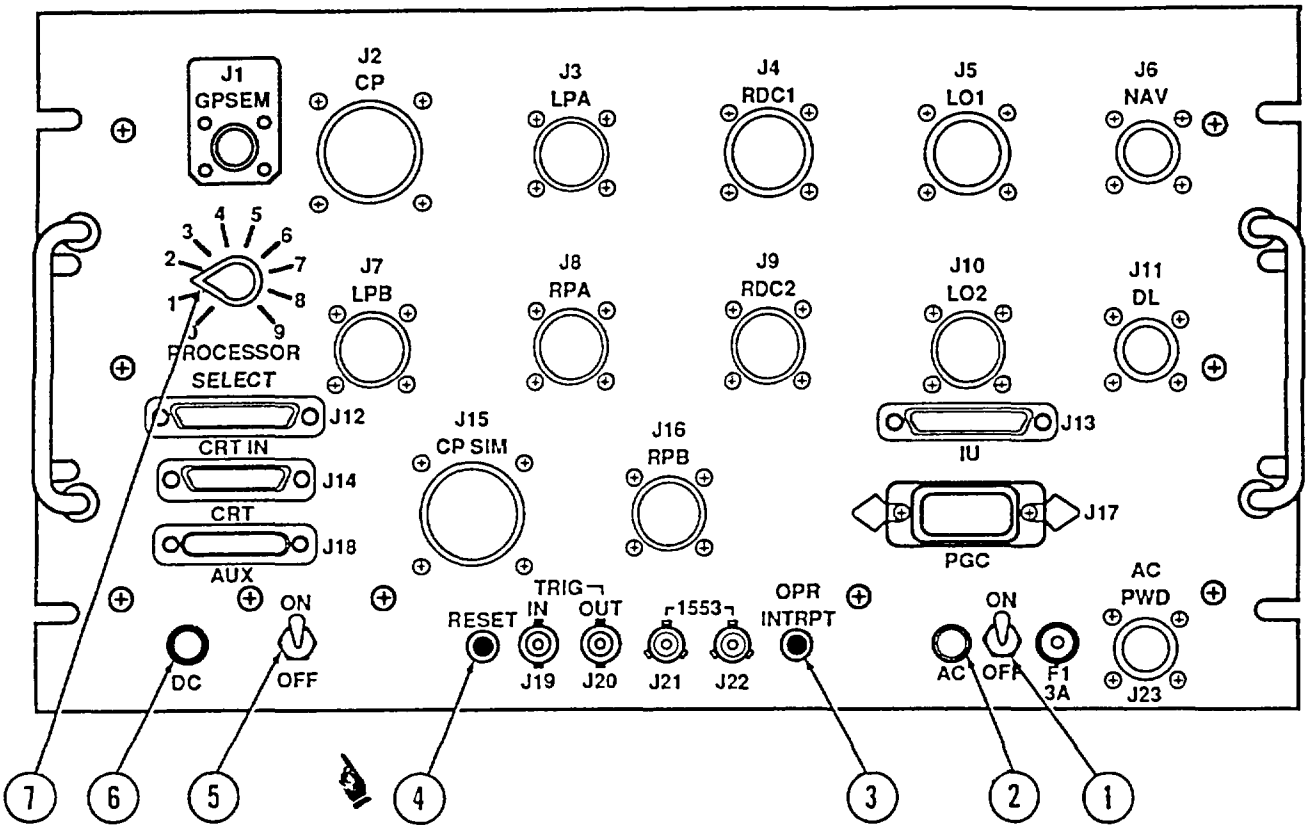
2-2. DAMAGE FROM IMPROPER SETTINGS

No combination of control settings will cause damage to equipment or create a hazard to personnel.

2-3. CONTROLS AND INDICATORS

The IUTS controls and indicators are illustrated on the next page.

2-3. CONTROLS AND INDICATORS - Continued



KEY	CONTROL OR INDICATOR	FUNCTION
1	AC ON/OFF (S1).	Applies power to IUTS
2	AC INDICATOR.	Lights when ac power is on
3	OPR INTRPT BUTTON (S2).	Interrupts and reinitializes diagnostic program currently loaded in RAM
4	RESET BUTTON (S3).	Aborts diagnostic program and clears RAM
5	DC ON/OFF (S4).	Turns dc power on and off
6	DC INDICATOR.	Lights when dc power is on
7	PROCESSOR SELECT (S5).	Selects processor to which diagnostic program is to be loaded

Section II. OPERATION UNDER USUAL CONDITIONS

2-4. GENERAL

The IUTS is used to test and troubleshoot the IU, CP, and RDC. Specific operating instructions for the IUTS are continued in chapter 5, direct support maintenance testing procedures. Consult the technical manual of the unit to be operated or repaired (appx A).

Section III. OPERATION UNDER UNUSUAL CONDITIONS I

2-5. OPERATION UNDER EMERGENCY CONDITIONS

There are no special procedures for unusual or emergency operation. Preventive and protective measures other than those that are a part of the PMCS are not required.

2-6. OPERATION AT TEMPERATURE EXTREMES

The chart below gives the temperature extremes for operation and exposure of the IUTS without degradation in performance.

	Operating temperature	Non-operating temperature
Minimum	+ 32-F (0° C)	- 60°F (-51° C)
Maximum	+109°F (+43° C)	+154oC (+68° C)

No special preconditions are required for operation within these limits.

CHAPTER 3

OPERATOR MAINTENANCE

For operator maintenance instructions, refer to TM 11-7740-331-13.

CHAPTER 4

ORGANIZATIONAL MAINTENANCE

CHAPTER CONTENTS **Page**

Section I. REPAIR PARTS, SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

4-1. COMMON TOOLS AND EQUIPMENT

For authorized common tools and equipment refer to the Modified Table of Organization and Equipment (MTOE) applicable to your unit.

4-2. SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

Refer to Maintenance Allocation (appx B), and TM 11-6625-3150-23P.

4-3. REPAIR PARTS

Repair parts are listed and illustrated in TM 11-6625-3150-23P.

Section II. SERVICE UPON RECEIPT

4-4. UNPACKING

Avoid damage to the container. Report the empty container through supply channels, or use to package a like unserviceable item.

4-5. CHECKING UNPACKED EQUIPMENT

a. Inspect the equipment for damage incurred during shipment. If the equipment has been damaged, report the damage on SF 364, Report of Discrepancy.

b. Check the equipment against the packing slip to see if the shipment is complete. Report all discrepancies in accordance with the instructions of DA Pam 738-750.

Section III. PREVENTIVE MAINTENANCE CHECKS AND SERVICES (PMCS)

4-6. PROCEDURES

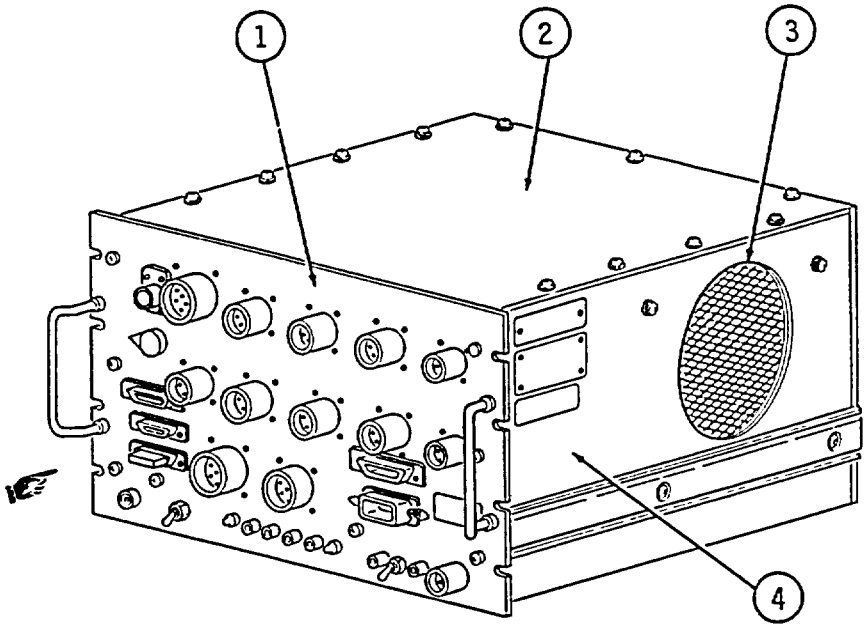
a. Follow the procedures in paragraph 4-7 to perform PMCS. Proceed by using the item number in the item column of the table in sequence.

Read from left to right at each item number. Perform the procedure in the procedure column at the time interval listed in the interval column.

b. Item numbers listed in paragraph 4-7 should be used when making out DA Form 2404, Equipment Inspection and Maintenance Worksheet. The item numbers in the PMCS table go into the TM Number column on DA Form 2404.

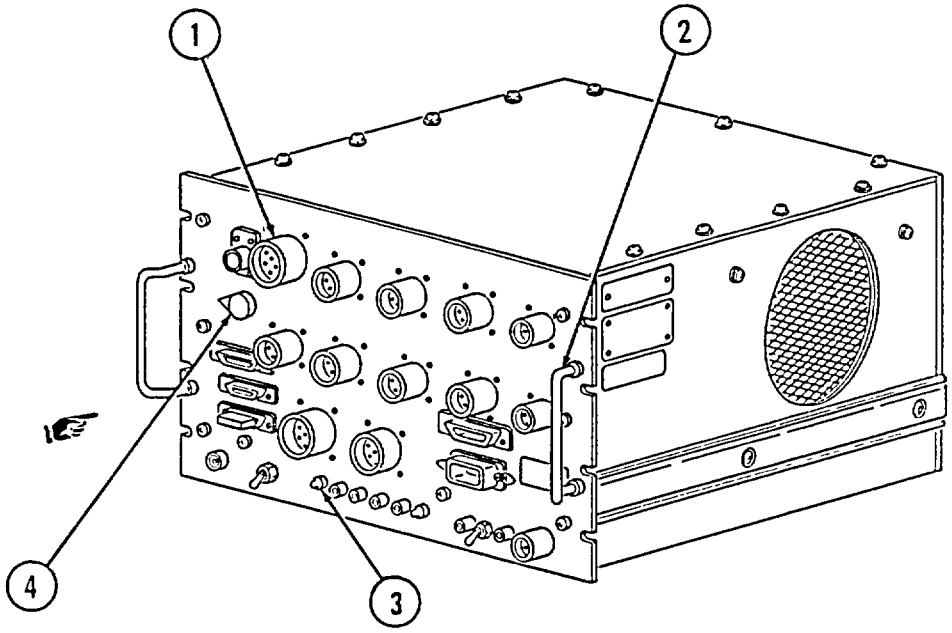
4-7. PREVENTIVE MAINTENANCE CHART

ORGANIZATIONAL PREVENTIVE MAINTENANCE CHECKS AND SERVICES

ITEM	INTERVAL Q	Q - QUARTERLY ITEM TO BE INSPECTED PROCEDURE
		EXTERIOR
		
(1)	•	**CHECK** front cover (1) is secure to chassis.
(2)	•	**CHECK** top cover (2) for secure fit. Tighten if loose.
(3)	•	**CHECK** filter screen (3) is clean and free of debris.
(4)	•	**CHECK** painted surfaces for missing, blistered, or chipped paint.

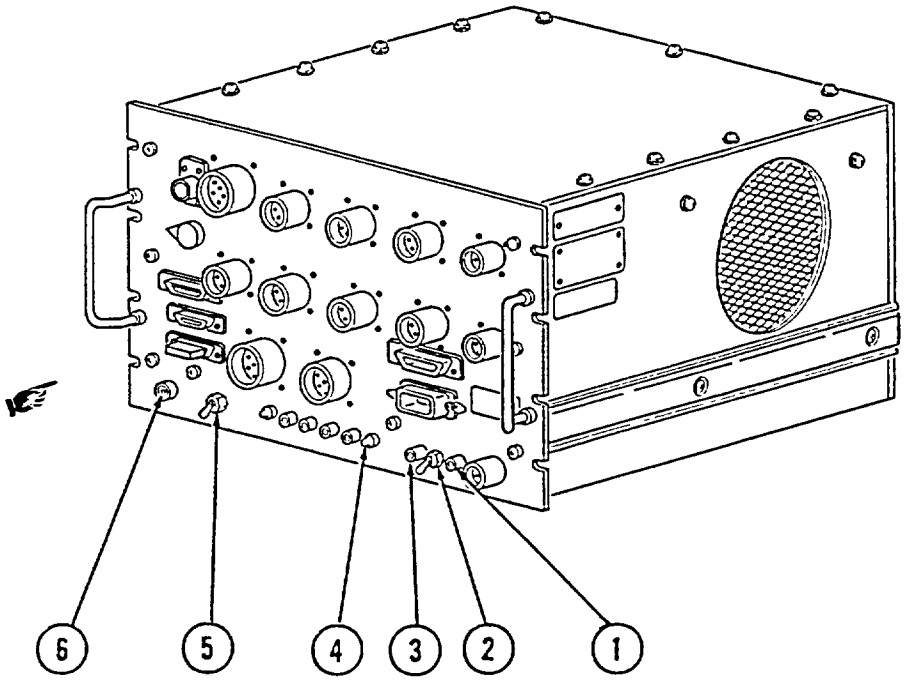
4-7. PREVENTIVE MAINTENANCE CHART - Continued

ORGANIZATIONAL PREVENTIVE MAINTENANCE CHECKS AND SERVICES - Continued

ITEM	INTERVAL Q	Q - QUARTERLY ITEM TO BE INSPECTED PROCEDURE
		FRONT PANEL 
(5)	•	**CHECK** front panel connectors (1) for secure attachment. Tighten if loose.
(6)	•	**CHECK** rack handles (2) for secure attachment. Tighten if loose.
(7)	•	**CHECK** PROCESSOR SELECT switch (4) rotates properly and knob is secure to shaft. Tighten if loose.
(8)	•	**CHECK** RESET button (3) operates without binding.

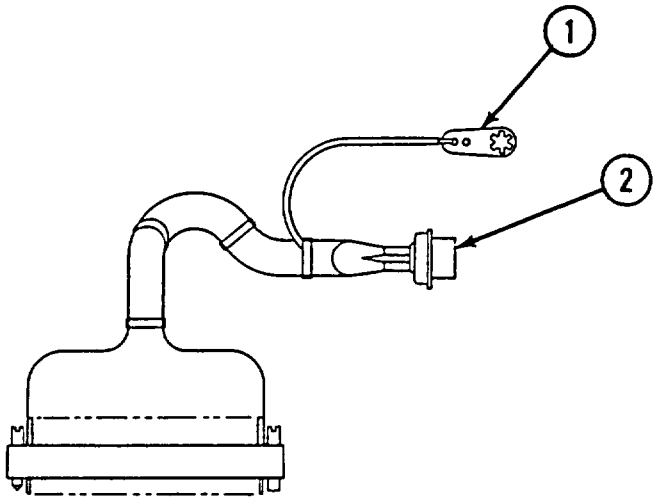
4-7. PREVENTIVE MAINTENANCE CHART - Continued

ORGANIZATIONAL PREVENTIVE MAINTENANCE CHECKS AND SERVICES - Continued

ITEM	INTERVAL Q	Q - QUARTERLY ITEM TO BE INSPECTED PROCEDURE
		FRONT PANEL 
(9)	•	**CHECK** dc ON/OFF switch (5) operates properly.
(10)	•	**CHECK** dc light (6) comes on when dc power is applied.
(11)	•	**CHECK** fuse cover (1) locks tight and is not chipped.
(12)	•	**CHECK** ac ON/OFF switch (2) operates properly.
(13)	•	**CHECK** AC indicator light (3) comes on when ac power is applied.
(14)	•	**CHECK** OPERATOR INTERRUPT button (4) operates without binding.

4-7. PREVENTIVE MAINTENANCE CHART - Continued

ORGANIZATIONAL PREVENTIVE MAINTENANCE CHECKS AND SERVICES - Continued

ITEM	INTERVAL Q	Q - QUARTERLY ITEM TO BE INSPECTED PROCEDURE
		TEST SET CABLES 
(15)	•	CHECK connectors (2) are clean and pins not bent.
(16)	•	CHECK ground straps (1) are secure and not frayed.

Section IV. MAINTENANCE

4-8. SCOPE

Organizational maintenance of the IUTS consists of PMCS, replacement of defective fuse (para 4-9), and indicator lamps DS1 and DS2 (para 4-10).

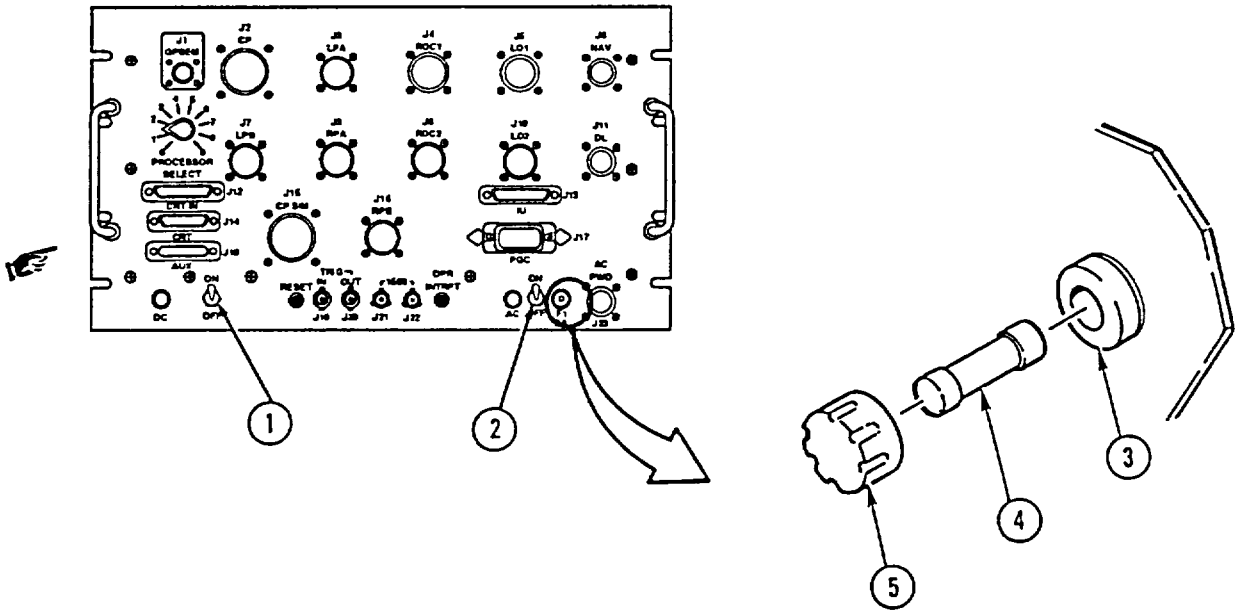
4-9. FUSE F1

a. Remove.

WARNING

Set POWER ON/OFF switch to OFF, unplug ac power cord, before removing fuse cover to prevent electrical shock.

(1) Set dc ON/OFF switch (1) to OFF.
(2) Set ac ON/OFF switch (2) to OFF.
(3) Remove fuse cover (5) from fuse holder (3).
(4) Remove fuse (4) from fuse cover (5).



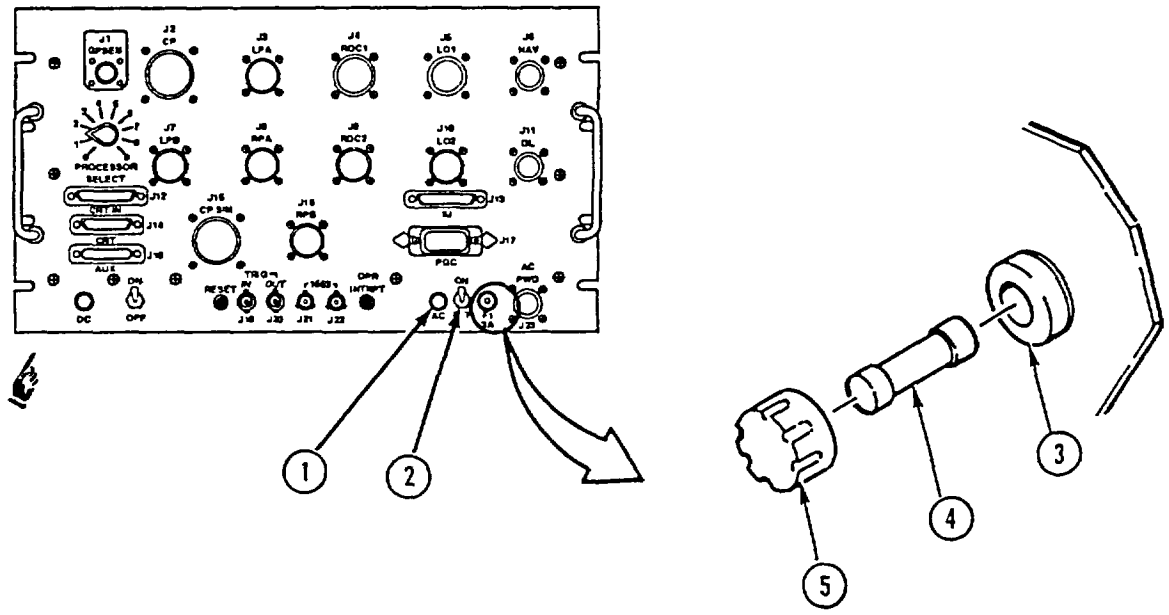
4-9. FUSE F1 - Continued

b. Installation.

WARNING

Set POWER ON/OFF switch to OFF, unplug ac power cord, before removing fuse cover to prevent electrical shock.

(1) Position fuse (4) in fuse cover (5).
(2) Install fuse cover (5) on fuse holder (3).
(3) Set ac ON/OFF switch (2) to ON.
(4) Check that AC indicator (1) is lit.
(5) Set ac ON/OFF switch (2) to OFF.



4-10. LAMP DS1 OR DS2

NOTE

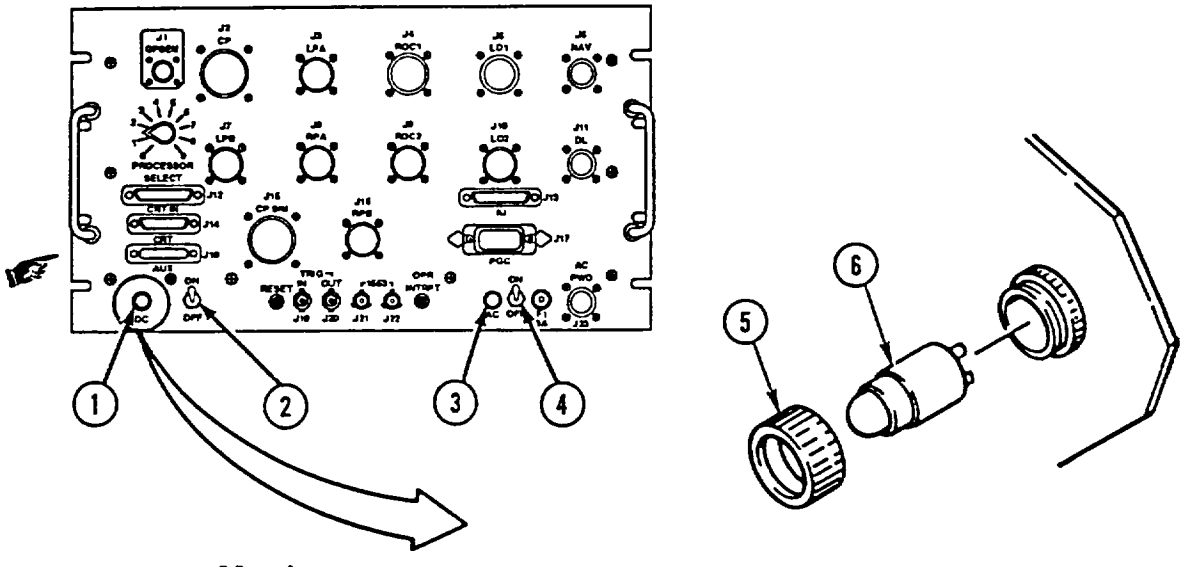
Procedure is the same for lamp DS1 or DS2.

a. Removal.

(1) Set dc ON/OFF switch (2) to OFF.

(2) Set ac ON/OFF switch (4) to OFF.

(3) Remove lamp retainer (5) and lamp (6).



b. Installation.

(1) Place lamp (6) in installed position.

(2) Install lamp retainer (5).

(3) Set ac ON/OFF switch (4) to ON.

(4) Set dc ON/OFF switch (2) to ON.

(5) Check that AC (3) and DC (1) indicators are on.

(6) Set dc ON/OFF switch (2) to OFF.

(7) Set ac ON/OFF switch (4) to OFF.

CHAPTER 5

DIRECT SUPPORT MAINTENANCE

CHAPTER CONTENTS **Page**

Section I. REPAIR PARTS, SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

5-1. COMMON TOOLS AND EQUIPMENT

For authorized common tools and equipment refer to the Modified Table of Organization and Equipment (MTOE) applicable to your unit.

5-2. SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

Refer to Maintenance Allocation (appx B), and TM 11-6625-3150-23P.

5-3. REPAIR PARTS

Repair parts are listed and illustrated in TM 11-6625-3150-23P

Section II. TROUBLESHOOTING

5-4. TEST EQUIPMENT REQUIRED

Refer to paragraph(s) 5-1 and 5-2, and test setup diagram.

5-5. TEST CONNECTIONS

a. Connect test setup (fig. 5-1)

(1) Set IUTS ac ON/OFF switch to OFF.

NOTE

There are two different operator terminals used in this test setup. One is for system 4 (HP Terminal 2645N given in steps (3) thru (5) below and the other for system 1 (HP Terminal 700/43 given in step (6) below):

(2) On operator terminal (HP MODEL 2645N) set the controls as follows:

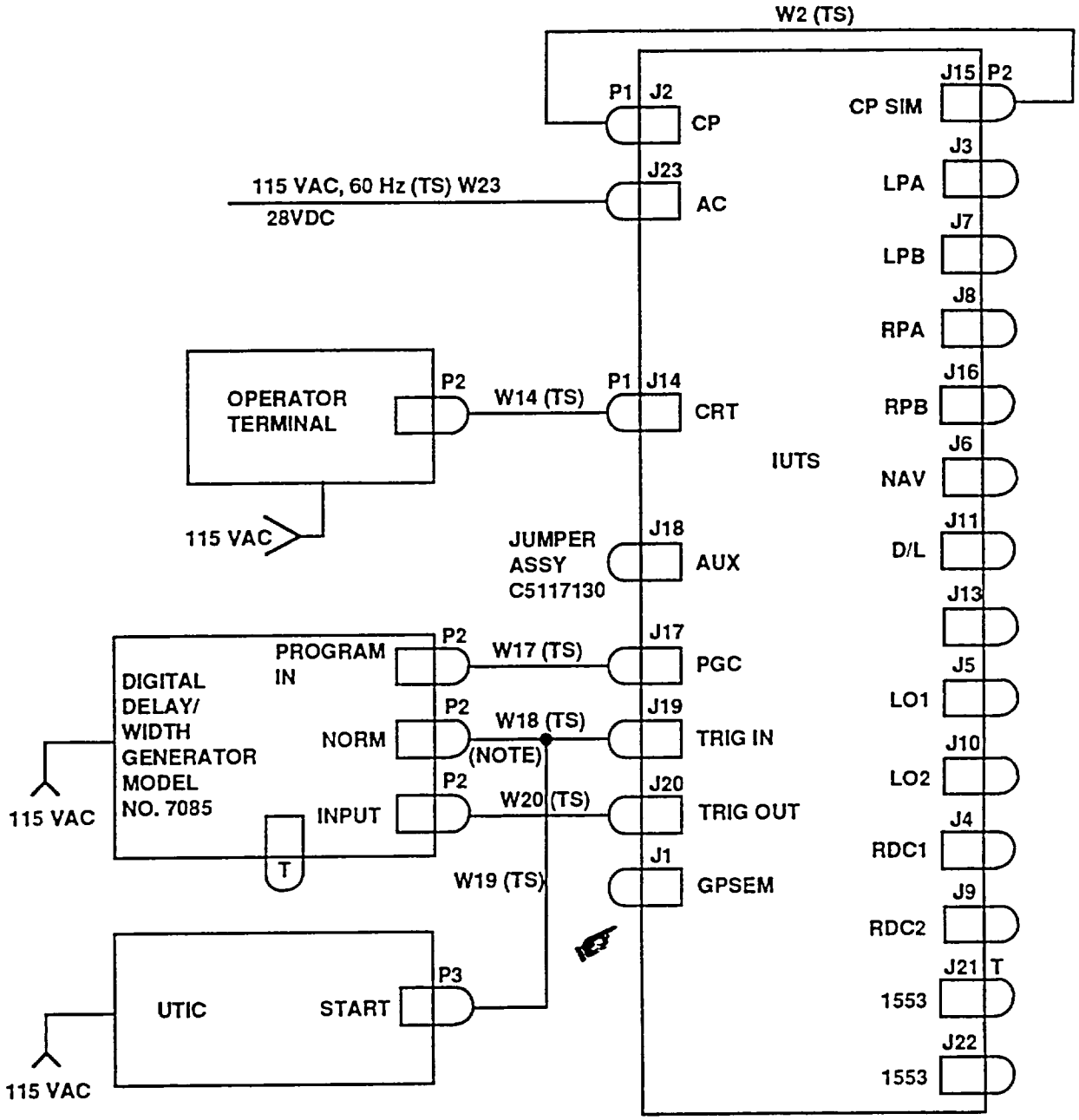
Switch	Set To
CRT monitor	ON
DUPLEX	FULL
PARITY	NONE
BAUD RATE	9600
Function	disengaged
REMOTE	engaged
CAPS LOCK	engaged

(3) Check that all operator terminal lamps, except TRANSMIT are off.

(4) On operator terminal, press RESET TERMINAL button

(5) Proceed to step (7) below.

(6) On operator terminal (HP MODEL 700/43) proceed as follows:



LEGEND: (TS)=TEST SET CABLES

NOTE: BNC-TEE UG-274 A/U

FIGURE 5-1. TEST SETUP DIAGRAM

5-5. TEST CONNECTIONS-Continued

a Turn operator terminal on.

b Enter setup mode by pressing SHIFT-SETUP.

c Select User Setup mode by pressing function key Fl.

NOTE

Data is changed by selecting the appropriate data column using the arrow keys. The space bar will cycle through the available choices for each column.

d Verify the following settings:

Time: Hour	Not Set
Minute	Not Set
Screen Saver	15 Minutes
Screen Attr	Normal
Refresh Rate	72 Hz
Cursor On	ON
Cursor Type	Blink Box
Smooth Scroll	Jump
Status Line	ON
On Line	ON LINE

e Select System Setup mode by pressing function key F8.

f Verify the following settings:

Screen Width	80
Miltipage	OFF
Auto Page	OFF
Attr Extent	Line
Bgnd Attr	Dim
Compatibility	Adds VP/A2
Enhanced Mode	OFF
Lead-in Char	ESC
EOM Char	NUL
Block Term	Us/Cr
Auto Scroll	ON
Auto Linefeed	OFF
Auto Wrap	ON
Monitor Mode	OFF
Graph Mode	OFF
Block Mode	Character
Protect Mode	OFF

g Select Data Communications mode by pressing function key F8.

5-5. TEST CONNECTIONS- Continued

h Verify the following settings for Main Port:

Baud Rate	9600
Data Length	8 Bits
Parity	None
Stop Bits	1
Communication	Full Duplex
Rec Pace	None
Xmit Pace	None
CTS	Ignore
DSR	Ignore
CD	Ignore
Monitor Line	OFF

i Select Keyboard mode by pressing function key F8

j Verify the following settings:

Key Click	ON
Edit Keys	Remote
Auto Repeat	ON
Nationality	US
Language	English
Margin Bell	OFF
Cursor Down	Ctri J
Lock or Gate	Lock
Lock Enable	ON

k Exit setup mode by pressing SETUP.

l Ensure CAPS LOCK is on.

(7) Proceed to test procedure (para 5-6).

5-6. TEST PROCEDURE AND FAULT ISOLATION

a. Use following procedure. This procedure is arranged in four columns.

Column (1). Contains step number. Do not skip steps unless ACTION column (4) directs otherwise.

Column (2). Contains test operation to be performed.

Column (3). Contains normal indication to be observed when procedure has been performed.

Column (4). Prescribes corrective action.

b. Whenever a corrective action has been taken, perform steps 1 through 18 to verify repair

c. If replacement of a part does not correct fault, reinstall original part before proceeding to next step.

d. Refer to applicable TM issued with the test equipment for operating instructions.

e. Refer to the following as required.

(1) FO-1. Component Locations.

(2) FO-2. Wiring Diagram, Axial Lead Connections.

(3) FO-3. Wiring Diagram, Cable Assembly W2 (J2-P1/P2).

(4) FO-4. Wiring Diagram, Cable Assembly W3 (J3-P1).

(5) FO-5. Wiring Diagram, Cable Assembly W4 (J4-P1).

(6) FO-6. Wiring Diagram, Cable Assembly W5 (J5-P1).

(7) FO-7. Wiring Diagram, Cable Assembly W6(J6-P1).

(8) FO-8. Wiring Diagram, Cable Assembly W7(J7-P1).

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

(9) FO-9. Wiring Diagram, Cable Assembly W8(J8-P1).

(10) FO-10. Wiring Diagram, Cable Assembly W9(J9-P1).

(11) FO-11. Wiring Diagram, Cable Assembly W10(J10-P1).

(12) FO-12. Wiring Diagram, Cable Assembly W11(J11-P1).

(13) FO-13. Wiring Diagram, Cable Assembly W13(J15-P1/P2).

(14) FO-14. Wiring Diagram, Cable Assembly W14(J16-P1).

(15) FO-15. Wiring Diagram, Cable Assembly W15(J17-P1).

(16) FO-16. Wiring Diagram, Cable Assembly P1-Jumper.

(17) FO-17. Wiring Diagram, Cable Assembly W25(J1-P1).

STEP	PROCEDURE	INDICATIONS	ACTION
	PART I. TEST PROCEDURE		
1.	On IUTS, set PROCESSOR SELECT switch to 9.		
2.	On IUTS, set ac ON/OFF switch to ON.	a. IUTS AC indicator on	If not, go to step 19.
		b. IUTS fan runs	If not, go to step 24.
3.	On IUTS, push and release RESET button.	MAIN MENU (fig. 5-2) appears	If not, go to step 27.

```
PWR UP   PASSED     HARDWARE TEST PACKAGE     CURRENT STAT
PROC =   TST        FUNCTION: MAIN MENU       ERROR COUNT
                            TEST
                  1. TEST IU (C5116265)
                  2. TEST CP (C5116266)
                  3. TEST RDC (C5116262)
                  4. RUN SELF TEST
                  5. TEST PROCESSOR BOARD
                  6. D/A ALIGNMENT PROCEDURE
                  7. PRI ALIGNMENT PROCEDURE
                  8. RUN CUSTOM TEST
                  9. ALLOW LOADING FROM PC
                 10. LOAD SPECIAL TEST SET PROGRAM FROM PC
                           SELECT OPTION:
Enter: M=Main menu, N=Next, P=Previous, K=Debug, ^B=Bell toggle
```

FIGURE 5-2. MAIN MENU

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
4.	On operator terminal, enter 7 <RETURN>.	TEST EXECUTION menu (fig. 5-3) appears	

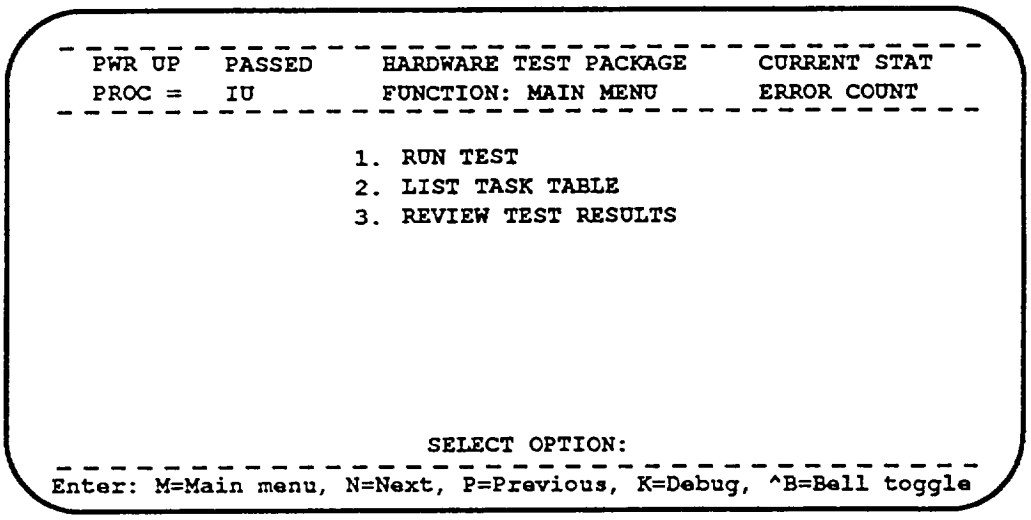


FIGURE 5-3. TEST EXECUTION MENU

5.	On operator terminal, enter 1 <RETURN>.	PRI alinement message (fig. 5-4) appears	

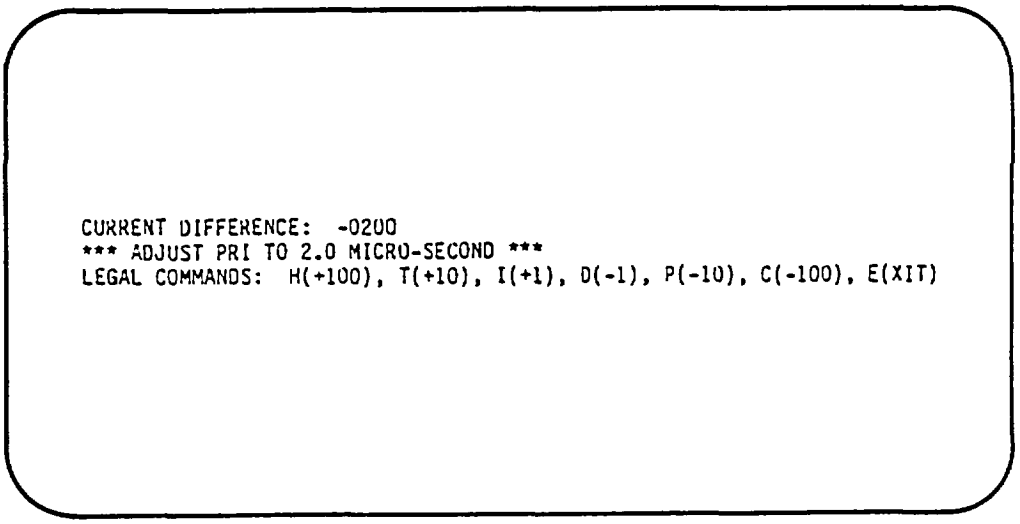


FIGURE 5-4. PRI ALIGNMENT MESSAGE

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
6.	On universal time interval counter (UTIC), adjust FREQ/ PERIOD input trigger level until stop trigger lamp starts blinking.	Stop trigger lamp blinks	
7.	On operator terminal, adjust UTIC to read 2.000 microseconds as follows:	UTIC	
	a. Increase Enter +100 H +10 T +1 I	a. increases	a. If adjustment is unsuccessful, replace A7 (para 5-10).
	b. Decrease Enter -100 C -10 P -1 D	b. decreases	b. If fault persists, send IUTS to higher level maintenance.
8.	On operator terminal enter E.	NO HARDWARE ERRORS WERE DETECTED STRIKE RETURN WHEN READY TO RETURN TO MENU	
9.	On operator terminal, enter <RETURN>.	TEST EXECUTION menu (fig. 5-3) reappears	
10.	On operator terminal enter M <RETURN>.	MAIN MENU (fig. 5-2) reappears	
11.	On operator terminal, enter 4 <RETURN>.	TEST EXECUTION menu (fig. 5-3) appears	

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
12.	Check messages in upper left-hand corner of display (fig. 5-3).	Following messages step 32. appear: PWR UP PASSED PROC = TST	If not, go to
		NOTE	
	The test takes about 90 seconds to run During this time, diagnostic task numbers will scroll on the next screen indicating the task being executed. **If the test halts on a diagnostic task for longer than 30 seconds, record any failure messages, and go to step 34.** **Push and release IUTS reset button to abort the test.**		
13.	On operator terminal, enter 1 <RETURN>.	Display scrolls	
14.	When test stops, check messages at end of display.	One of two messages appear:	
		a. NO HARDWARE ERRORS WERE DETECTED	a. Go to step 15.
		b. XX TEST MODULES ENCOUNTERED HARDWARE FAULT	b. Go to step 34.
15.	Perform CP test procedure using known good unit (TM 11-5895-1286-13).	One of two messages appear:	
		a. NO HARDWARE ERRORS WERE DETECTED	a. Go to step 16.

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
15.	Cont	b. XX TEST MODULES ENCOUNTERED/HARDWARE FAULT	b. Go to step 39.
16.	Perform IU test procedure using known good unit (TM 11-5895-1279-13).	One of two messages will appear:	
		a. NO HARDWARE ERRORS WERE DETECTED	a. Go to step 17.
		b. XX TEST MODULES ENCOUNTERED HARDWARE FAULT	b. Go to step 43.
17.	Perform RDC test procedure using known good unit, (TM 11-5895-1283-13).	One of two messages will appear:	
		a. NO HARDWARE ERRORS WERE DETECTED	a. Go to step 18.
		b. XX TEST MODULES ENCOUNTERED HARDWARE FAULT	b. Go to step 48.
18.	End test:		
	a. Remove test setup power.		
	b. Remove IUTS from test setup.		

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
	PART II. FAULT ISOLATION		
	A. AC INDICATOR DOES NOT LIGHT		
19.	Replace indicator lamp (para 4-10).Repeat steps 1 and 2.	AC indicator on	If not, go to step 20.
20.	Replace fuse (para 4-9). Repeat steps 1 and 2.	AC indicator on	If not, go to step 21.
21.	Check IUTS voltages: a. Remove bottom cover (para 5-8). b. Using DVM check voltage at (FO-1): Test Points E9 (gnd) to E10 E15 (gnd) to E16 E14 (gnd) to E13 E11 (gnd) to E12	 Vdc + 5.0 + 0.15 +12.0 + 0.15 -12.0 + 0.15 - 5.0 + 0.15	a. If not, go to step 22. b. If present and AC indicator is not on, send IUTS to higher level maintenance.
22.	Replace A17 (para 5-10). Repeat steps 1 and 2.	AC indicator on	If not, go to step 23.
23.	Replace ac ON/OFF power switch (para 5-12). Repeat steps 1 and 2.	AC indicator on	If not, send IUTS to higher level maintenance.
	B. IUTS FAN DOES NOT OPERATE		
24.	Replace C1 (para 5-11). Repeat steps 1 and 2.	IUTS fan runs	If not, go to step 25.
25.	Replace B1 (para 5-16). Repeat steps 1 and 2.	IUTS fan runs	If not, go to step 26.

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
26.	Replace S4 (para 5-12). Repeat steps 1 and 2.	IUTS fan runs	If not, send IUTS to higher level maintenance.
	C. MAIN MENU DOES NOT APPEAR		
27.	Replace A14 (para 5-10). Repeat steps 1 through 3.	MAIN MENU appears(fig. 5-2)	If not, go to step 28.
28.	Replace A13 (para 5-10). Repeat steps 1 through 3.	MAIN MENU appears (fig. 5-2)	If not, go to step 29.
29.	Check IUTS voltages: a. Remove bottom cover (para 5-8). b. Using DVM check voltage at (FO-1): Test Points E9 (gnd) to E10 E15 (gnd) to E16 E14 (gnd) to E13 E11 (gnd) to E12	 Vdc + 5.0 + 0.15 +12.0 +0.15 -12.0 + 0.15 - 5.0 t 0.15	a. If not, go to step 30. b. If present, go to step 31.
30.	Replace A17 (para 5-10). Repeat steps 1 through 3.	MAIN MENU (fig. 5-2) appears	If not, send IUTS to higher level maintenance.
31.	Replace A15 (para 5-10). Repeat steps 1 through 3.	MAIN MENU (fig. 5-2) appears	If not, send IUTS to higher level maintenance.
	D. FAULTY PWR UP/PROC MESSAGES		
32.	Replace A14 (para 5-10). Repeat steps 1 through 18.	Following messages appear: PWR UP PASSED PROC = TST	If not, go to step 33.

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
33.	Replace A13 (para 5-10). Repeat steps 1 through 18.	Following messages appear: PWR UP PASSED PROC = TST	If not, send IUTS to higher level maintenance.
	E. IUTS HARDWARE FAULT		
34.	On operator terminal, press <RETURN>.	TEST EXECUTION menu (fig. 5-3) appears	
35.	On operator terminal, enter 3 <RETURN>.	TEST RESULTS display (fig. 5-5) appears	
36.	Note and record task numbers of test modules that failed as shown on display (fig. 5-5). (para 5-7).		a. If task numbers 34 or 35 failed, go to alinement procedure b. If task numbers, are not 34 or 35, go to step 37.

```
------------------------------------------------------------------------------
      PWR UP   PASSED          HARDWARE TEST PACKAGE          CURRENT STAT  FAILED
      PROC =   TST             FUNCTION :  TEST RESULTS       ERROR COUNT     XX
------------------------------------------------------------------------------

      TASK NUMBERS OF TEST MODULES THAT FAILED

    * XXXXX



                    ENTER MODULE TASK NUMBER TO REVIEW RESULTS OR
                    P TO RETURN TO TEST EXECUTION SCREEN


------------------------------------------------------------------------------
ENTER M TO GO TO MAIN MENU,     N FOR NEXT MENU,   P FOR PREV., OR K FOR DEBUGGER
```

FIGURE 5-5. TEST RESULTS DISPLAY - TYPICAL ERROR MESSAGE

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
37.	Using matrix (fig. 5-6): a. Locate task number(s) in TASK NO. column. b. Opposite task number(s) identify suspect defective CCAs.		a. Replace suspect CCAs one at a time (para 5-10). b. Repeat steps 1 through 18 for each replaced CCA. c. If fault persists, go to step 38.
38.	Using chart below: a. Locate task number(s) in TASK NO. column. b. Opposite task number(s) identify suspect defective wire harness(es) and connector(s).		a. Replace defective wire harness(es) and/or connector(s). b. Repeat steps 1 through 18 for each replaced item. c. If fault persists, send IUTS to higher level maintenance.

NOTE
Check connectors and cable in order listed.

Task No.	Connectors	Cables	FO No.
94, 95, 96	J2 J15	W2 W13	FO-3 FO-13
03, 36	J15 J2	W13 W2	FO-13 FO-3

F. CP HARDWARE FAULT

39.	On operator terminal, press <RETURN>.	TEST EXECUTION menu (fig. 5-3) appears	

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

TASK NO.	CPIF A3	CP SIM A4	TSD/A A5	TSD/A A6	TSIFP A7	1553B A10	IUDL A11	IUNAV A12	TSBUS A13	DBP A14	PSRAM A15
9, 10, 11, 12, 13,									3	2	1
68, 69, 70,									1	2	
34			1		2				3		
35				1	2				3		
16, 17						3		1			2
19, 20, 21, 22, 23, 24						3	1				2
28, 29, 48						1					2
3, 36	2	1									3
94, 95, 96	1	2									3

FIGURE 5-6. IUTS TEST MODULE/CCA MATRIX

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
40.	On operator terminal, enter 3 <RETURN>.	TEST RESULTS display (fig. 5-5) appears	
41.	Note and record task numbers of test modules that failed as shown on display (fig. 5-5).	Task numbers appear	a. If task number 26 failed, replace A10 (para 5-10) and repeat step 15. If fault persists, send IUTS to higher level maintenance. b. If task number(s) are not 26, replace A3 (para 5-10) and repeat step 15. If fault still persists, go to step 42.
42.	Check W2 continuity. a. Remove top cover (para 5-8). b. Check for damaged connector. c. Using DVM check W2 continuity (FO-3).	Continuity	a. Replace damaged connector (para 5-18). b. Replace damaged wire(s) (para 5-21). c. If fault still persists, send IUTS to higher level maintenance.
	G. IU HARDWARE FAULT		
43.	On operator terminal, press <RETURN>.	TEST EXECUTION menu (fig. 5-3) appears	
44.	On operator terminal, enter 3 <RETURN>.	TEST RESULTS display (fig. 5-5) appears	
45.	Note and record task numbers of test modules that failed as shown on display (fig. 5-5).		Go to step 46.

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
46.	a. Locate task number(s) in TASK NO. column (fig. 5-7). b. Opposite task number(s), identify suspect defective CCA(s).		a. Replace suspect CCA(s) one at a time (para 5-10). b. Repeat step 16 for each replaced CCA. c. If fault persists, go to step 47.
47.	Using matrix (fig. 5-8): a. Locate task number(s) in TASK MODULES column. b. Opposite task number(s), identify suspect defective wire harness(es) and connector(s).		a. Replace defective wire harness(es) and/or connector(s). b. Repeat step 16 for each replaced item. c. If fault persists, send IUTS to higher level maintenance.
	H. RDC HARDWARE FAULT		
48.	On operator terminal, enter 3 <RETURN>.	TEST EXECUTION menu (fig. 5-3) appears	
49.	On operator terminal, enter 3 <RETURN>.	TEST RESULTS display (fig. 5-5) appears	
50.	Note and record task numbers of test modules that failed as shown on display (fig. 5-5).	Task numbers appear	Go to step 51.

5-6. TEST PROCEDURE AND ISOLATION - Continued

TASK NO.	CP SIM A4	TSD/A A5	TSD/A A6	TSIFP A7	1553B A10	IUDL A11	IUNAV A12	DBP A14	PSRAM A15	TICK A2	TS BUS A13	OSCG 1
21-27					3	1			2			
28-34					1				2			
68,69,72.73. 76,77,80,81		1		2								
70,71,74,75. 78,79,82.83			1	2								
16-18					3		1		2			
8-15								2	1			
2-5	1											
35										1	2	3

FIGURE 5-7. IU TEST MODULE/IUTS CCA MATRIX

TASK MODULES	FRONT PANEL CONNECTOR	CABLE	FOLDOUTS
16 - 18	J6	W6	FO-7
12 - 27	J11	W11	FO-12
68, 72, 76, 80	J3	W3	FO-4
69, 73, 77, 81	J7	W7	FO-8
70, 74, 78, 82	J8	W8	FO-9
71, 75, 79, 83	J16	W14	FO-14
35	J1	W25	FO-17

FIGURE 5-8. CONNECTOR/CABLE MATRIX

5-6. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
51.	Using chart below: a. Locate task number(s) in TASK NO. column. b. Opposite task number(s), identify suspect defective CCA(s).		a. Replace suspect CCA(s) one at a time (para 5-10). b. Repeat step 17 for each replaced CCA. c. If fault persists, go to step 52.
	Task No. / Suspect CCA 51 — 1553B A10 52 — TSLO A8 55 — TSLO A8 56 — TSRF A9 57 — TSRF A9		
52.	Using chart below: a. Locate task number(s) in TASK NO. column. b. Opposite task number(s) identify suspect defective wire harness(es) and connector(s).	c	a. Replace defective wire harness(es) and/or connector(s). b. Repeat step 17 for each replaced item. c. If fault persists, send IUTS to higher level maintenance.

NOTE

Check connectors and cables in order listed

Task No.	Connectors	Cables	FO No.
52, 55	J5	W5	FO-6
J1O	W10	FO-11	
56, 57	J4	W4	FO-5
J9	W9	FO-10	

5-71. D/A ALINEMENT PROCEDURE

STEP	PROCEDURE	INDICATIONS	ACTION
1.	Remove top cover (para 5-8).		
2.	On operator terminal, enter M <RETURN>.	MAIN MENU (fig. 5-2) reappears	
3.	On operator terminal, enter 6 <RETURN>.	TEST EXECUTION (fig. 5-3) reappears	
4.	On operator terminal, enter 1 <RETURN>.	NO ERROR or ERROR display appears	a. If NO ERROR display (fig. 5-9) appears, go to step 8. b. If ERROR display (fig. 5-10) appears, go to step 5.
5.	Locate and identify following columns on display (fig. 5-10): LEFT LA = RIGHT LA =	Each column contains series of hexadecimal values, e.g., 80, 81, etc.	
6.	Check values under column (fig. 5-10): LEFT LA =	 80 80	a. If not adjust A5R2 for value of If adjustment is unsuccessful, replace A5 (para 5-10) and repeat steps 2 through 4. b. If present, go to step 7.

5-7. D/A ALINEMENT PROCEDURE - Continued

```
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
00033: TSCAL :  LEFT LA = 80      RIGHT LA = 80
```

FIGURE 5-9. ALINEMENT DATA DISPLAY NO ERROR DISPLAY

```
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
00033: TSCAL :  LEFT LA = 81      RIGHT LA = 80      ADJUST TO LA = 80
```

FIGURE 5-10. ALINEMENT DATA DISPLAY ERROR DISPLAY

5-7. D/A ALINEMENT PROCEDURE - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
7.	Check values under column (fig. 5-10). RIGHT LA =	 80	a. If not, adjust A6R2 for value of 80. If adjustment is unsuccessful, replace A6 (para 5-10) and repeat paragraph 5-7. b. If present, go to step 8.
8.	a. Install top cover (para 5-8). b. Return to test procedure (para 5-6).		

Section III. MAINTENANCE

5-8. TOP OR BOTTOM COVERS

NOTE

Procedure is the same for top or bottom covers, except where noted.

a. Preliminary Procedures.

WARNING

Capacitors hold voltages after power is removed. Ground C1 before working inside IUTS to prevent injury to personnel.

(1) Remove power from test setup.

WARNING

When lifting or handling heavy objects, use two people to prevent possible back injury.

(2) Remove IUTS from test setup.

b. Removal.

(1) If removing bottom cover, position IUTS to access cover (3).

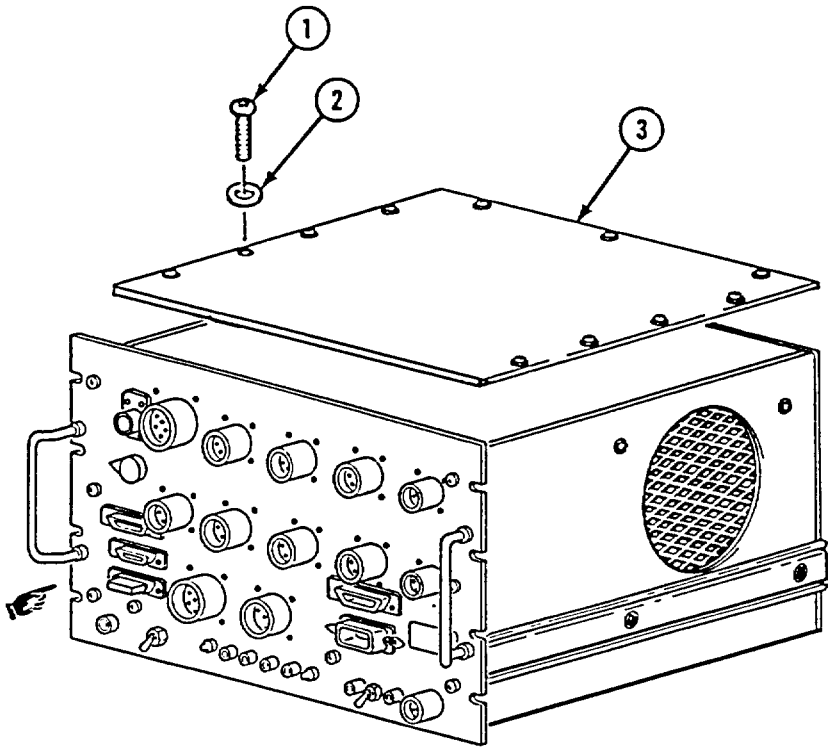
(2) Remove 11 screws (1) and washers (2).

(3) Remove cover (3).

5-8. TOP OR BOTTOM COVERS - Continued

c. Installation.

(1) Place cover (3) in installed position.
(2) Install 11 screws (1) and washers (2). Torque to 6-8 inch/pounds.



d. Follow-on Procedure. Perform test procedure (para 5-6).

5-9. OSCILLATOR G1

a. Preliminary Procedure. Remove top cover (para 5-8).

b. Removal.

(1) Disconnect cable W47 (6) from CCA A2 (3).

(2) Remove CCA A2 (3), A3 (4), and A4 (5) (para 5-10).

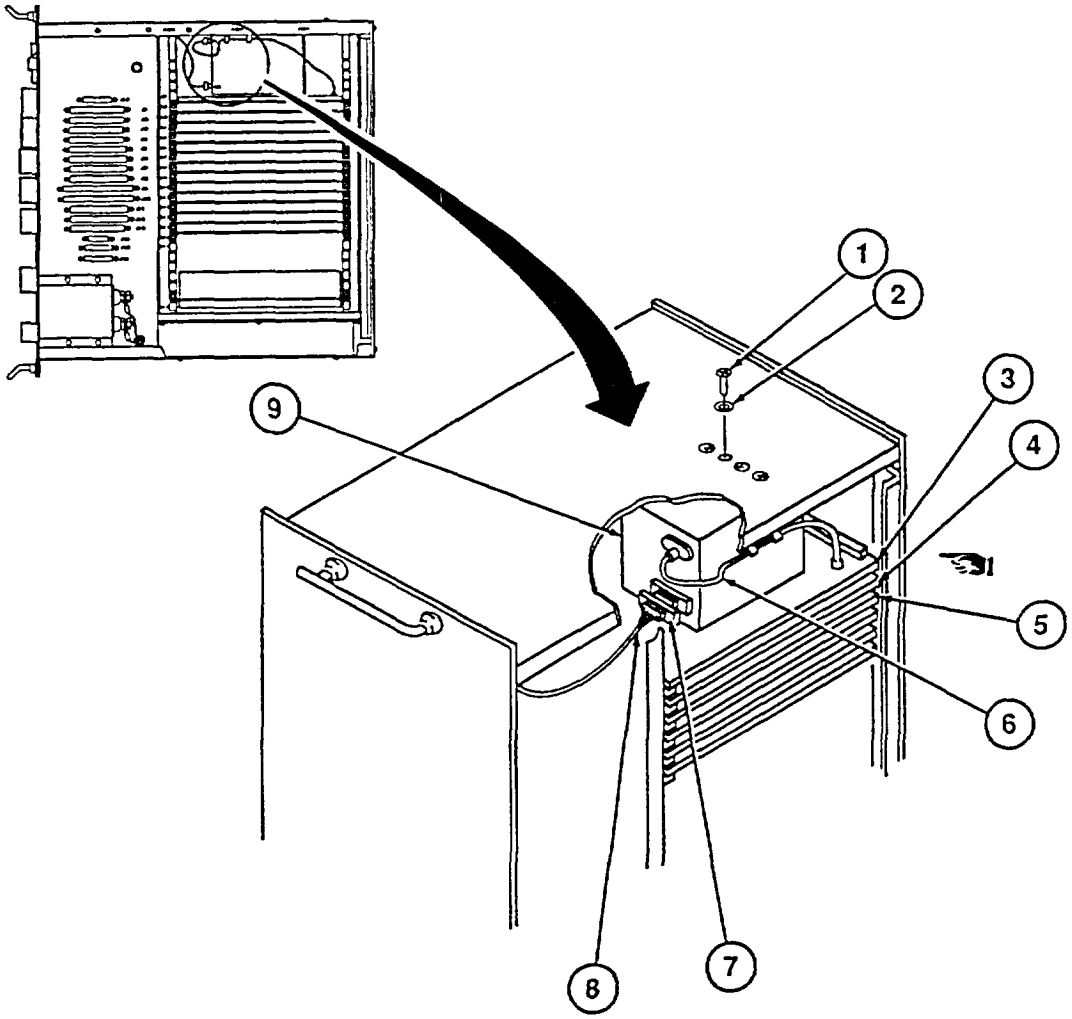
(3) Firmly grasp oscillator (9) and remove four screws (1) and washers (2).

(4) Raise oscillator (9) to provide access to attached cables.

(5) Loosen two jack screws (7) and disconnect connector (8).

(6) Disconnect cable W47 (6) from oscillator (9).

(7) Remove oscillator (9).



5-9. OSCILLATOR G1 - Continued

c. Installation.

(1) Position oscillator (9) above IUTS.

(2) Reconnect cable W47 (6) to oscillator (9).

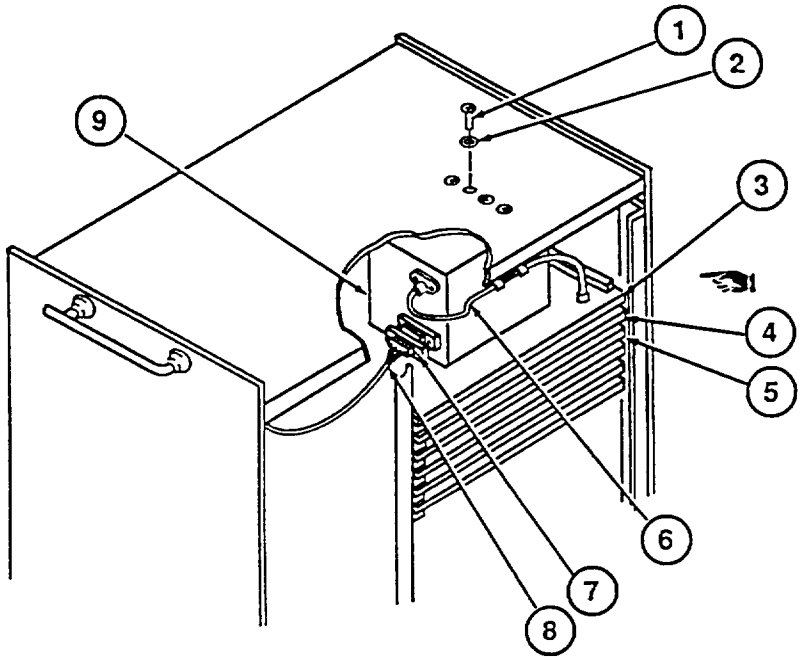
(3) Reconnect connector (8).

(4) Tighten two jack screws (7).

(5) Install oscillator and secure using four screws (1) and washers (2).

(6) Install CCA A2 (3), A3 (4), and A4 (5) (para 5-10).

(7) Reconnect cable W47 (6) to CCA A2 (3).



d. Follow-on Procedure. Install top cover (para 5-8).

5-10. CIRCUIT CARDS A2 THROUGH A15 AND A17

NOTE

Procedure is the same for all circuit cards, except where noted.

a. Preliminary Procedure. Remove top cover (para 5-8).

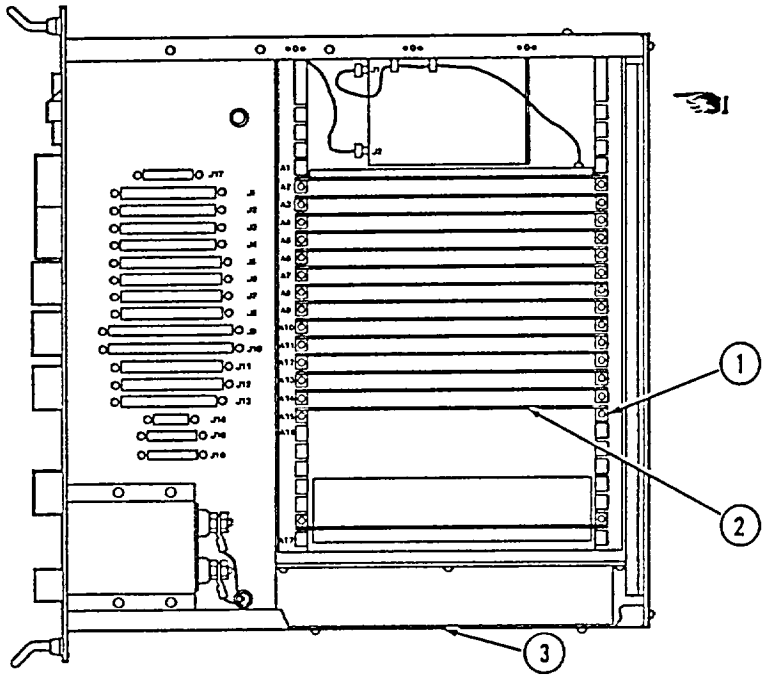
b. Removal.

(1) Loosen two cam locks (1).

NOTE

If removing power supply, A17, use handle.

(2) Using card extractor, remove circuit card (2) from IUTS (3).



c. Installation.

(1) Place circuit card (2) in IUTS (3).
(2) Tighten two cam locks (1).

d. Follow-on Procedure. Install top cover (para 5-8).

5-11. CAPACITOR C1

a. Preliminary Procedure. Remove top and bottom covers (para 5-8).

WARNING

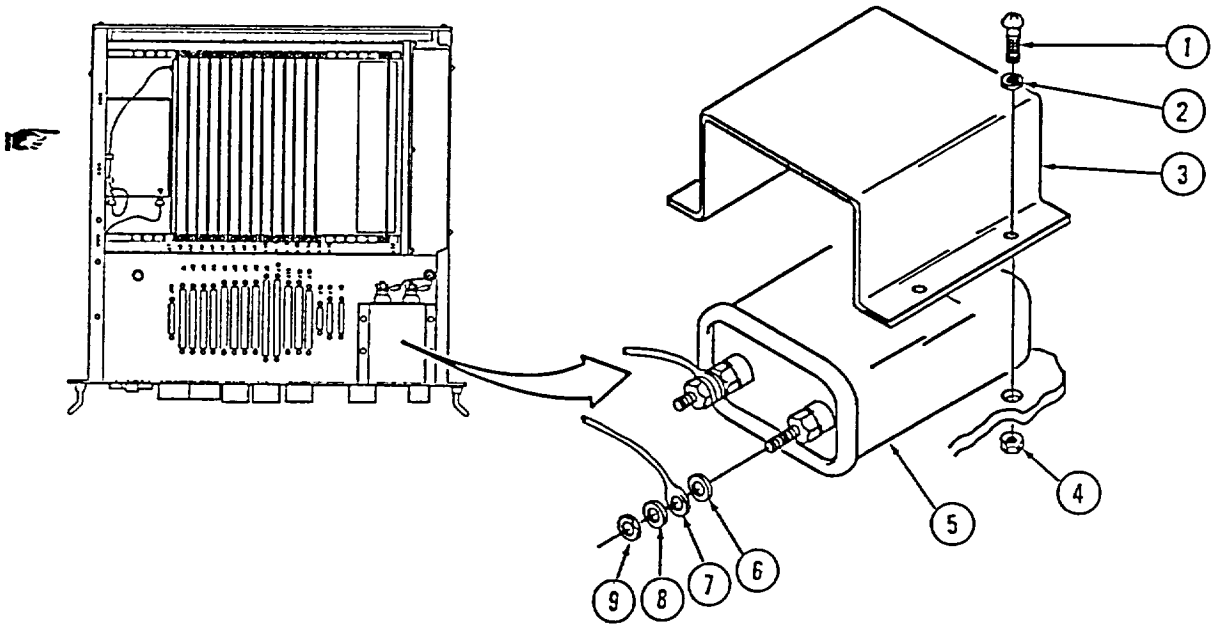
Capacitors hold voltages after power is removed. Ground C1 before working inside IUTS to prevent injury to personnel.

b. Removal.

(1) Remove two nuts (9), lockwashers (8), terminal lugs (7), and washers (6).

(2) Remove four screws (1), washers (2), and locknuts (4).

(3) Remove bracket (3) and capacitor C1 (5).



c. Installation.

(1) Place capacitor C1 (5) and bracket (3) in installed position.

(2) Install four screws (1), washers (2), and locknuts (4).

(3) Install two nuts (9), lockwashers (8), terminal lugs (7), and washers (6).

d. Follow-on Procedure. Install top and bottom cover (para 5-8).

5-12. SWITCH S1 OR S4

NOTE

Procedure is the same for switch S1 or S4, except where noted.

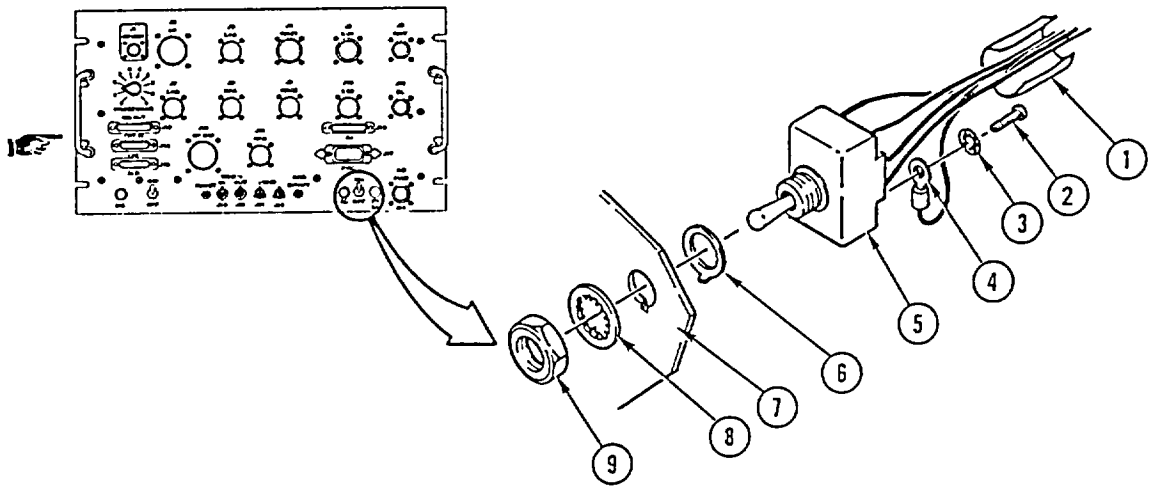
a. Preliminary Procedure. Remove bottom cover (para 5-8).

b. Removal.

(1) If working on switch S1, remove insulation sleeving (1).

(2) Tag wires (4). Remove screws (2), lockwashers (3), and wires (4).

(3) Remove nut (9), lockwasher (8), locking ring (6), and switch (5) from front panel (7).



c. Installation.

(1) Place switch (5) and locking ring (6) in installed position.

(2) Position locking ring (6) and switch (5) to engage front panel (7) keyway, then install nut (9) and lockwasher (8).

(3) If working on switch S1, route wires (4) through new length of insulation sleeving (1).

(4) Install screws (2) and lockwashers (3) to secure wires (4) as tagged. Rem ove tags.

(5) If working on switch S1, using heat gun, position and shrink insulation sleeving (1) over switch Sl (5).

d. Follow-on Procedure. Install bottom cover (para 5-8).

5-13. PUSHBUTTON SWITCH S2 OR S3

NOTE

Procedure is the same for switch S2 or S3.

a. Preliminary Procedure. Remove bottom cover (para 5-8).

b. Removal.

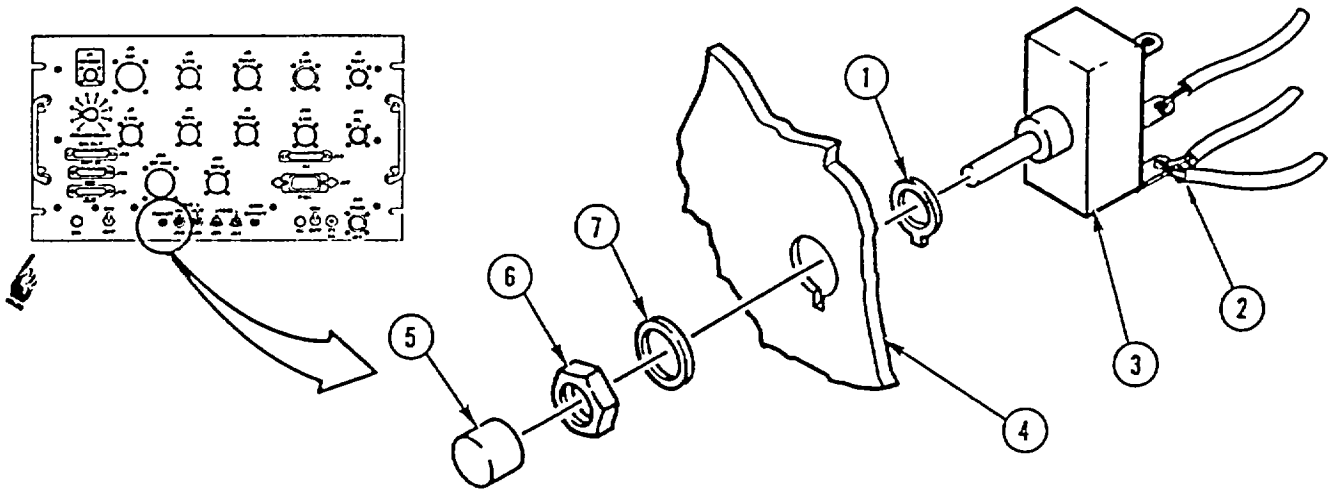
WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(1) Tag, unsolder, and remove wires (2).

(2) Pull off switch knob (5).

(3) Remove nut (6), lockwasher (7), locking ring (1) and switch (3) from front panel (4).



5-13. PUSHBUTTON SWITCH S2 OR S3 - Continued

c. Installation.

WARNING

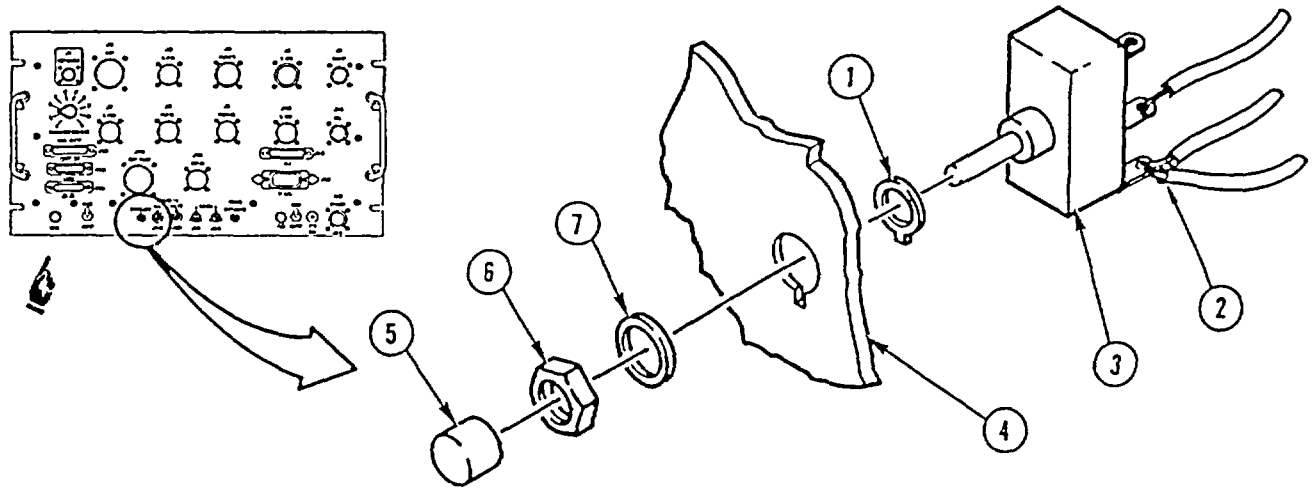
Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(1) Position locking ring (1) on switch (3).

(2) Position switch (3) so that locking ring (1) engages keyway in front panel (4).

(3) Install nut (6), lockwasher (7), and knob (5).

(4) Resolder wires (2) to switch (3) as tagged. Remove tags.



d. Follow-on Procedure. Install bottom cover (para 5-3).

5-14. FUSEHOLDER ASSEMBLY XF1

a. Preliminary Procedure. Remove bottom cover (para 5-8).

b. Removal.

(1) Remove insulation sleeving (1).

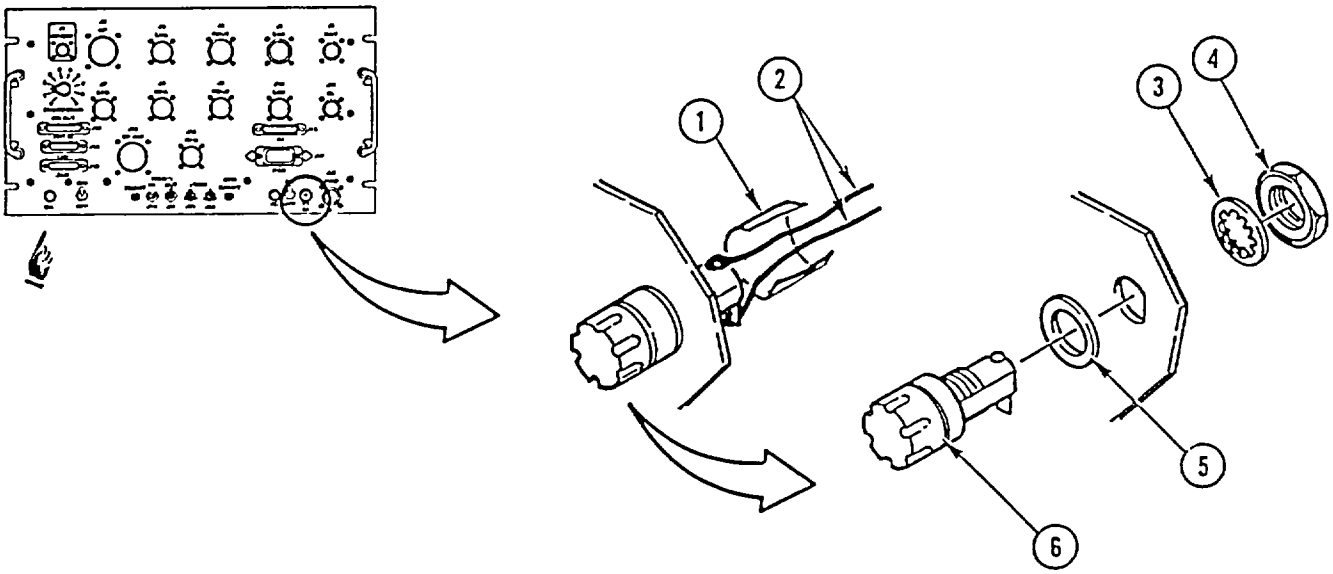
WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(2) Tag, unsolder, and remove wires (2).

(3) Remove nut (4) and washer (3) from rear of fuseholder (6).

(4) Remove fuseholder (6) with gasket (5).



5-14. FUSEHOLDER ASSEMBLY XF1 - Continued

c. Installation.

(1) Place fuseholder (6) with gasket (5) in installed position.

(2) Install nut (4) and lockwasher (3) on rear of fuseholder (6).

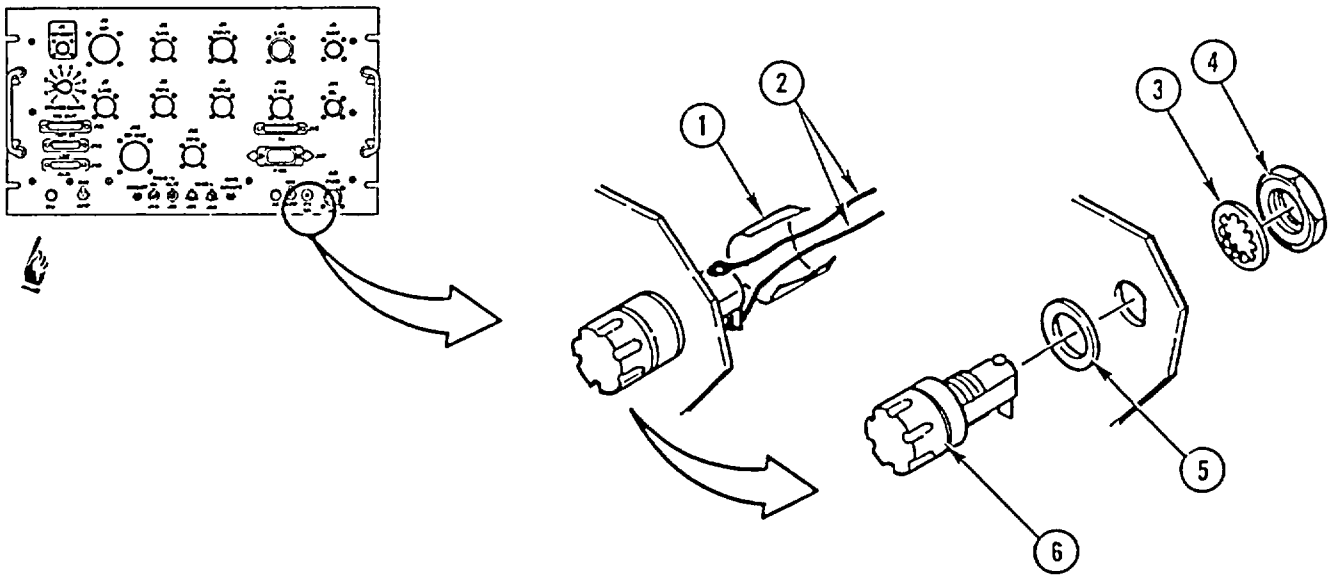
(3) Position wires (2) through new length of insulation sleevi ng (1).

WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(4) Resolder wires (2) as tagged. Remove tags.

(5) Using heatgun, shrink insulation sleeving (1) over fuseholder (6).



d. Follow-on Procedure. Install bottom cover (para 5-8).

5-15. LAMP ASSEMBLY DS1 OR DS2

NOTE

Procedure is the same for lamp assembly DS1 or DS2.

a. Preliminary Procedure. Remove bottom cover (para 5-8).

b. Removal.

(1) Remove insulation sleeving (2).

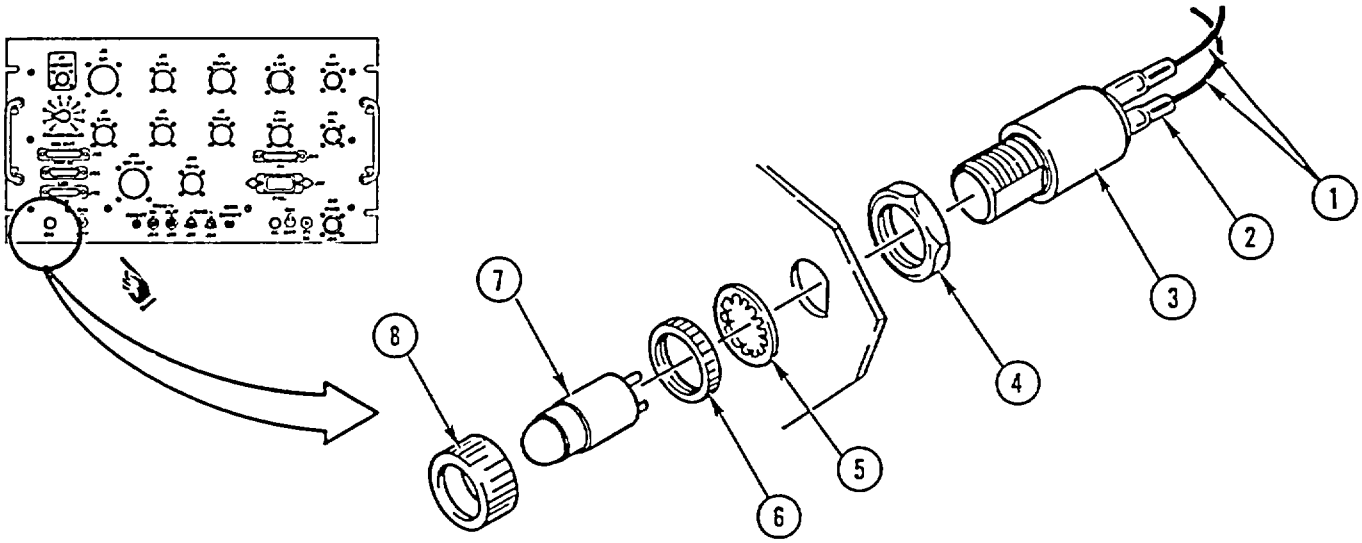
WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(2) Tag, unsolder, and remove wires (1).

(3) Remove collar (8), lamp (7), flange nut (6), and lockwasher (5).

(4) Remove lamp assembly (3) and hex nut (4) from rear of front panel.



5-15. LAMP ASSEMBLY DS1 OR DS2 - Continued

c. Installation.

(1) Place lamp assembly (3) and hex nut (4) in installed position.

(2) Install lockwasher (5), flange nut (6), lamp (7), and collar (8).

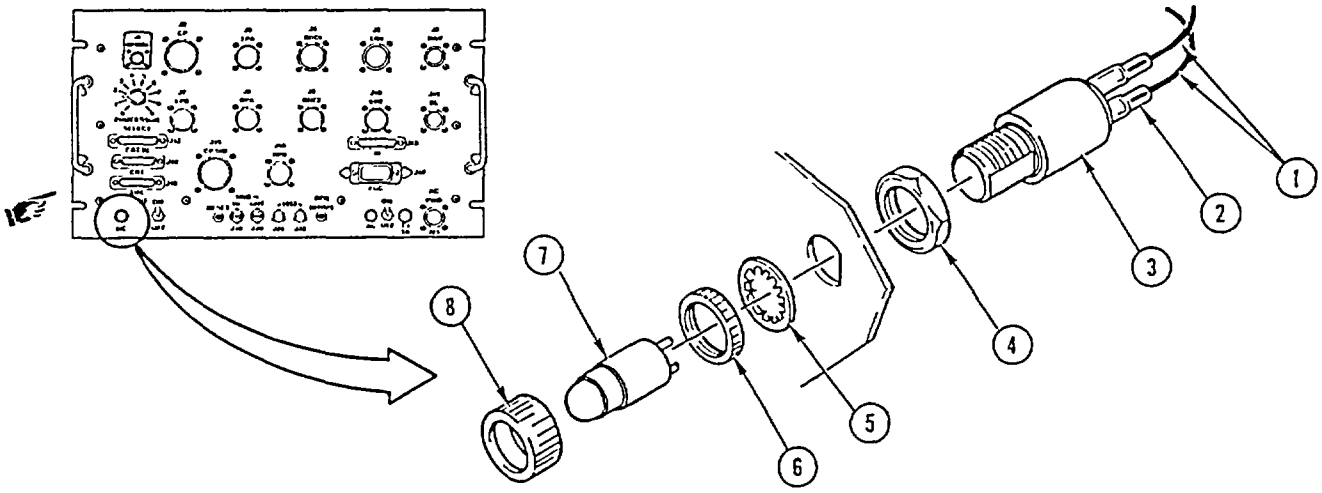
(3) Position insulation sleeving (2) on wires (1).

WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(4) Resolder wires (1) as tagged. Remove tags.

(5) Using heat gun, position and shrink insulation sleeving (2).



d. Follow-on Procedure. Install bottom cover (para 5-8).

5-16. FAN B1

a. Preliminary Procedure. Remove top and bottom covers (para 5-8).

WARNING

Capacitors hold voltages after power is removed. Ground C1 before working inside IUTS to prevent injury to personnel.

b. Removal.

WARNING

When lifting or handling heavy objects, use two people to prevent possible back injury.

(1) Position IUTS (1) so that side with fan B1 (2) faces upward.

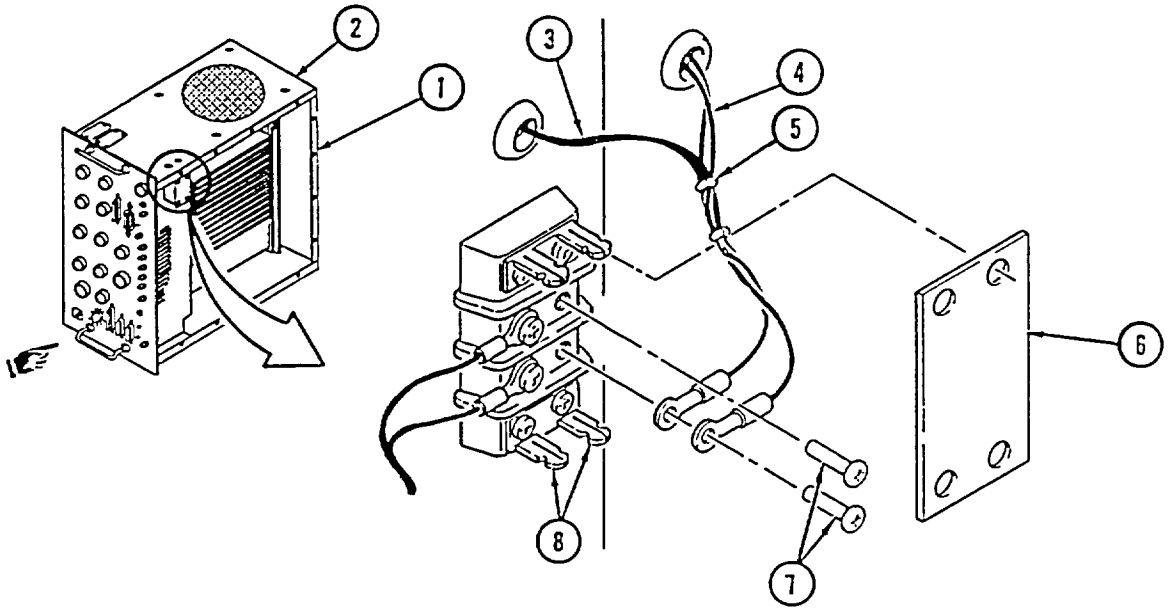
(2) Squeeze four retainer tangs (8) and remove TB1 cover (6).

(3) Tag wires (4).

(4) Remove wire screws (7) and wires (4).

(5) Remove fan wire (3) from capacitor C1.

(6) Remove cable ties (5), as required, to isolate fan wires (3) and (4).



5-16. FAN B1 - Continued

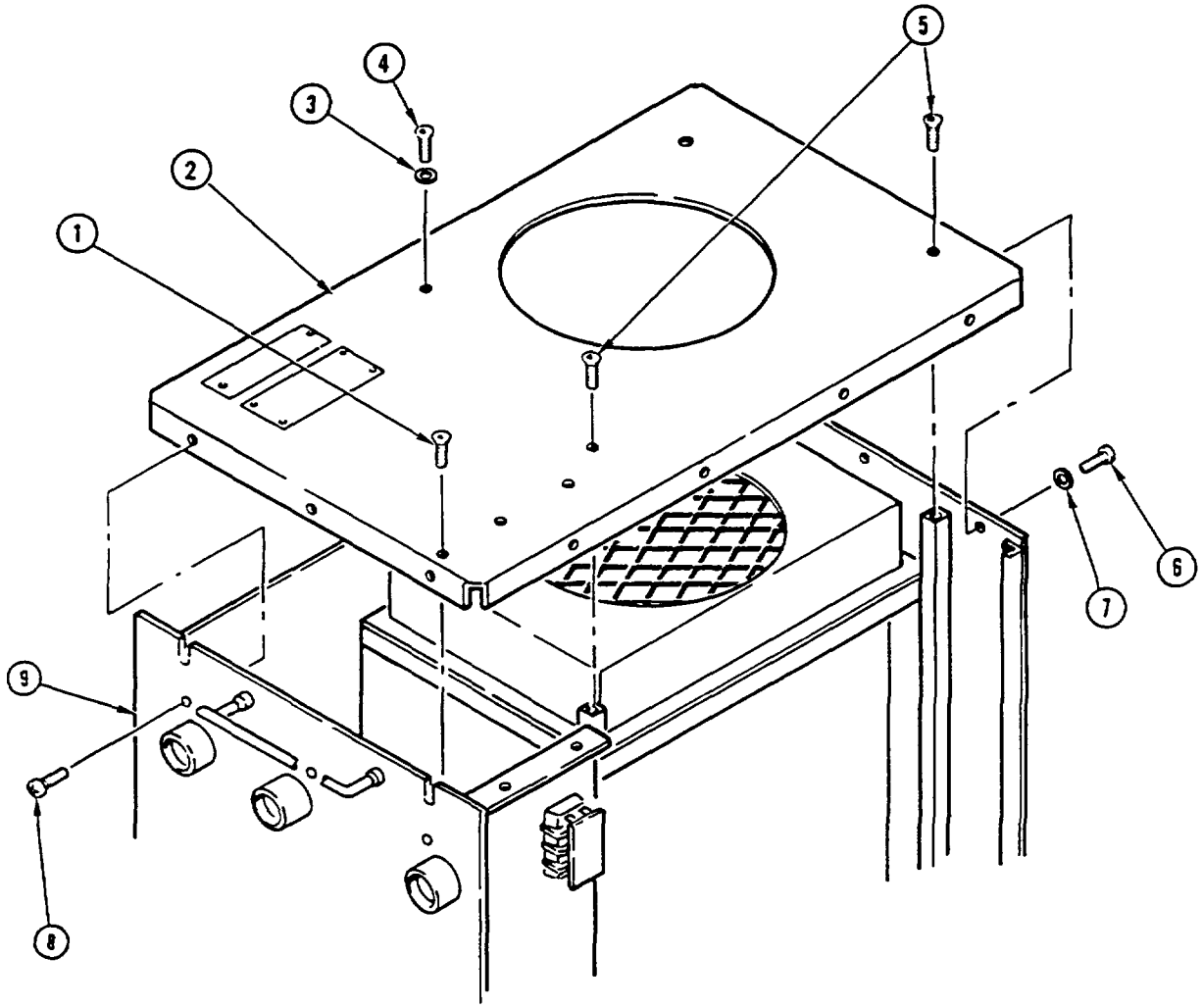
(7) Remove five screws (1) and (5) from side panel.

(8) Remove two screws (4) and washers (3) from side panel.

(9) Remove three screws (6) and washers (7) from rear panel.

(10) Remove three screws (8) from front panel (9).

(11) Remove side panel (2).



5-16. FAN B1 - Continued

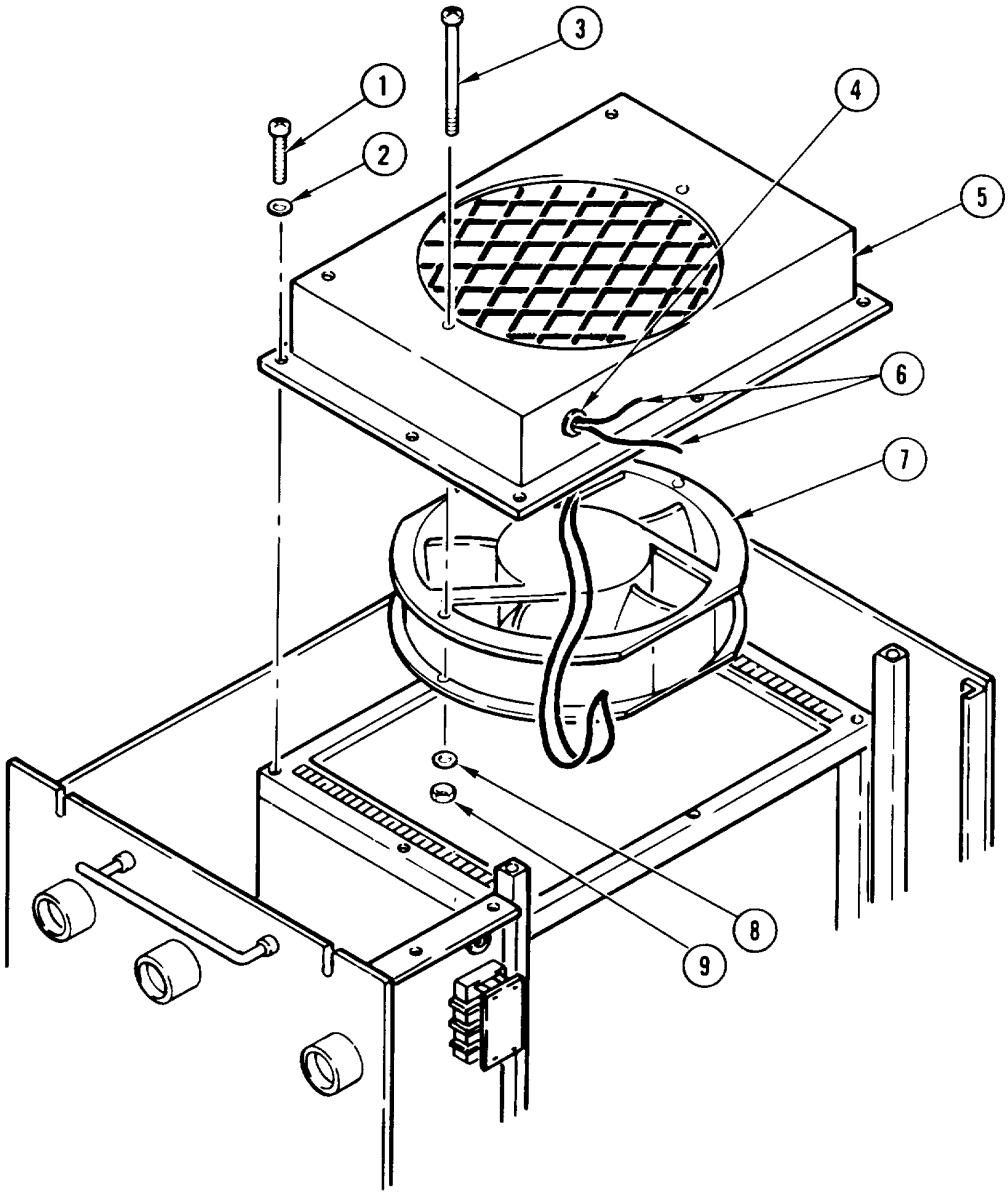
(12) Remove eight screws (1) and washers (2).

(13) Remove fan panel assembly (5) routing wires (6) through grommet (4).

(14) Remove two screws (3), washers (8), and locknuts (9).

(15) Remove fan B1 (7) from fan panel assembly (5).

(16) Transfer wire tags to replacement fan B1 (7).



5-16. FAN B1 - Continued

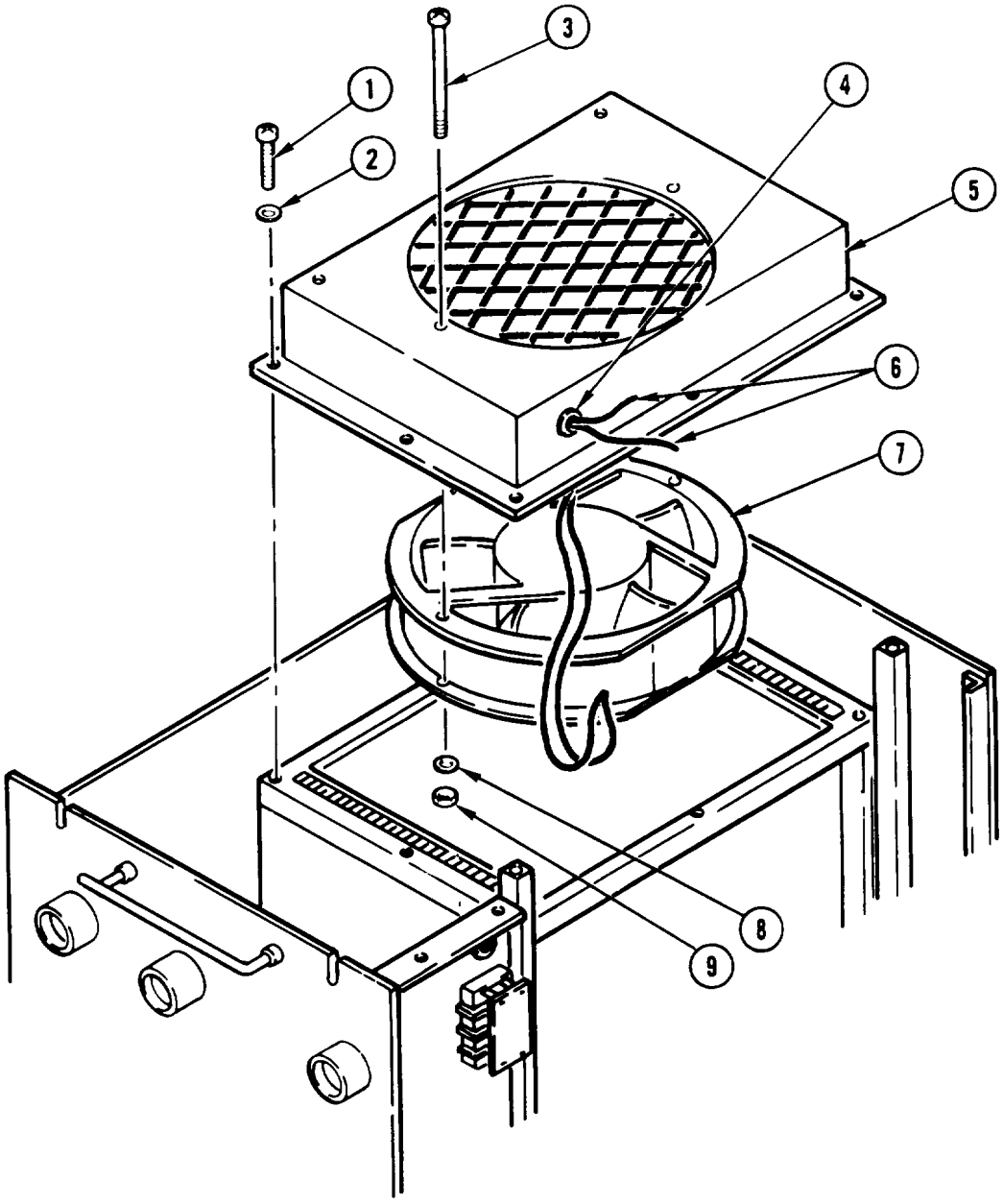
c. Installation.

(1) Position fan B1 (7) in fan panel assembly (5) routing wires (6) through grommet (4).

(2) Install two screws (3), washers (8), and locknuts (9).

(3) Place fan panel assembly (5) in installed position.

(4) Install eight screws (1) and washers (2).



5-16. FAN B1 - Continued

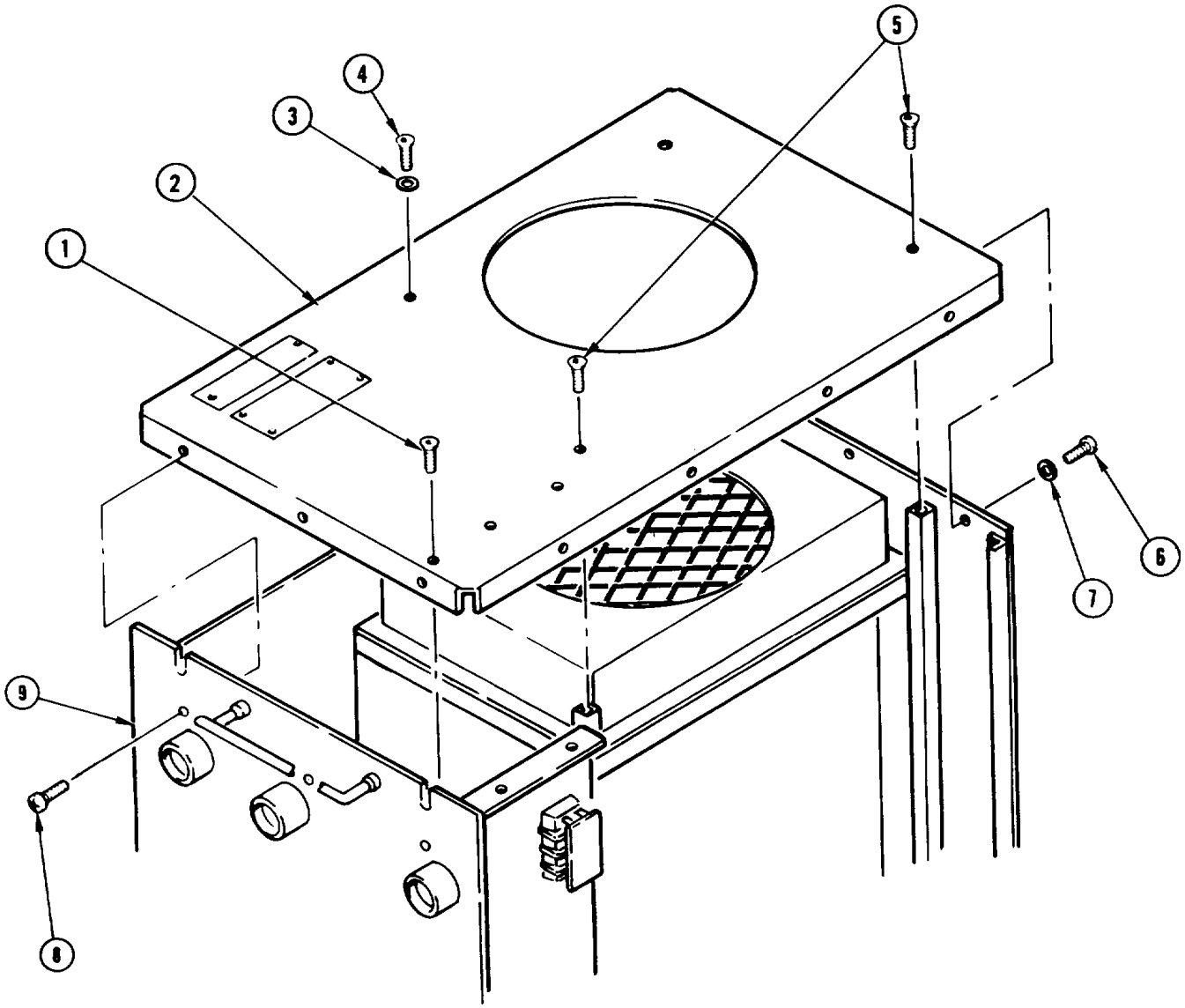
(5) Position side panel (2) in installed position.

(6) Install five screws (1) and (5) in side panel.

(7) Install two screws (4) and washers (3) in side panel (2).

(8) Install three screws (6) and washers (7) in rear panel.

(9) Install three screws (8) in front panel (9).



5-16. FAN B1 - Continued

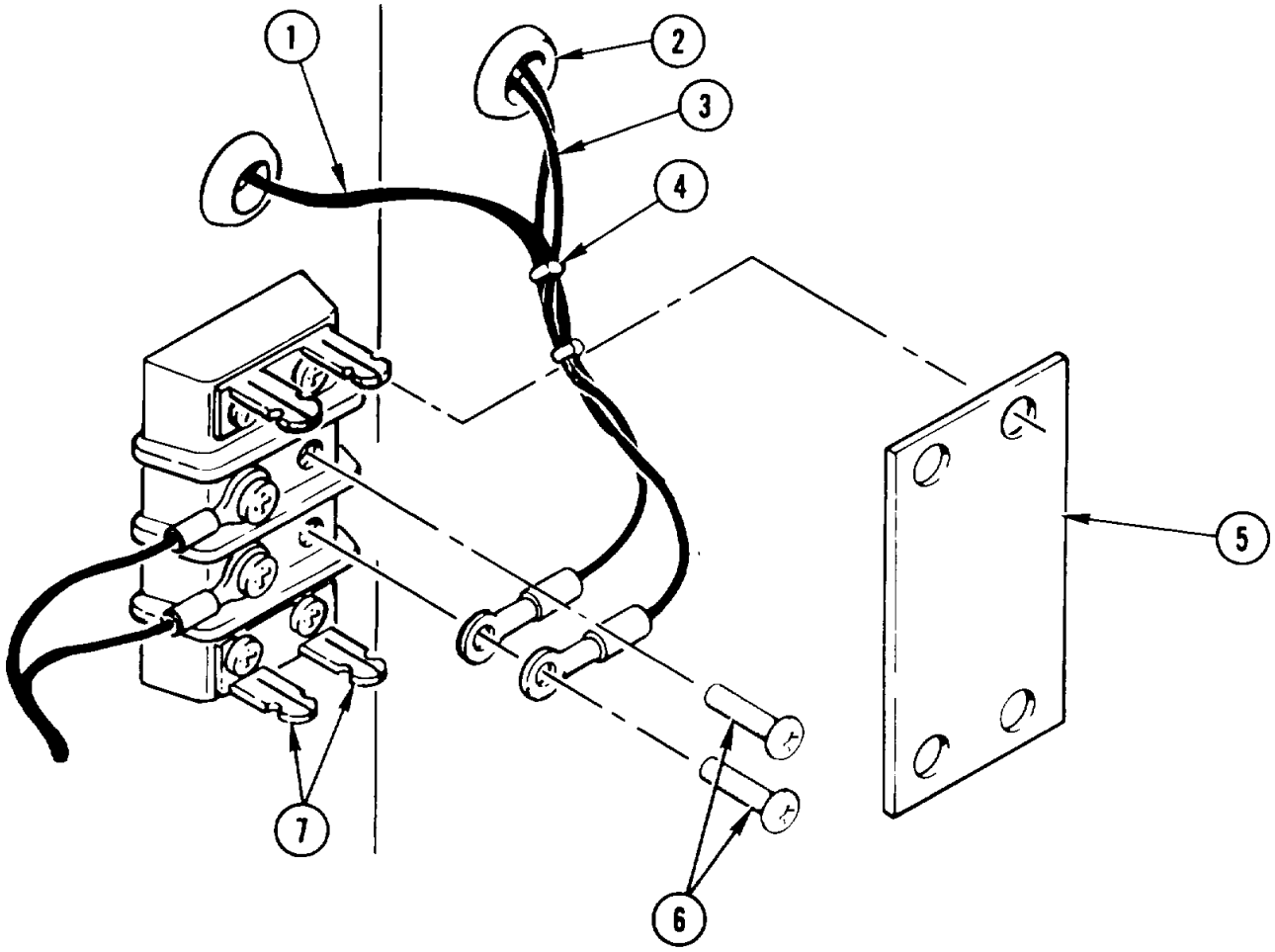
(10) Route fan wires (1) and (3) through grommet (2).

(11) Install two screws (6) to secure wires (3) as tagged. Remove tags.

(12) Connect fan wire (1) to capacitor C1.

(13) Press TB1 cover (5) on four retainer tangs (7) until cover is secure.

(14) Install cable ties (4), as required.



d. Follow-on Procedure. Install top and bottom covers (para 5-8).

5-17. DELETED

5-18. CONNECTORS J1 THROUGH J11, J15, J16, OR J23

NOTES

- **Procedure is the same for connectors J1 through J11, J15, J16, or J23, except where noted.**
- **On serial number 10001A through 1004A, there is a marking plate attached to the front panel by the mounting screws of J1. Remove and install this marking plate as required.**

a. Preliminary Procedures.

(1) If working on J23, remove bottom cover (para 5-8).

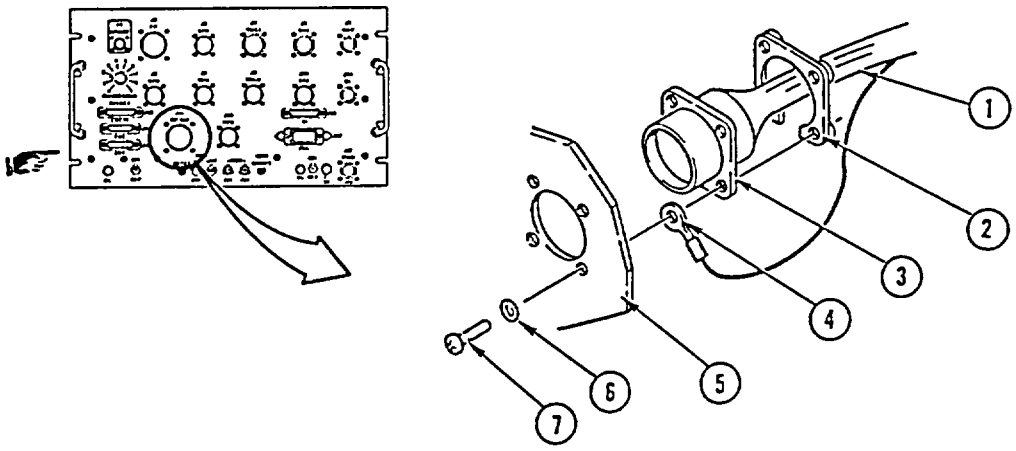
(2) If working on J1 through J11, J15, or J16, remove top cover (para 5-8).

5-18. CONNECTORS J1 THROUGH J11, J15, J16, OR J23 - Continued

b. Removal.

(1) Remove four screws (7), and washers (6), nutplate (2), connector (3), and ground lug (4) from front panel (5).

(2) Tag and remove wires (1).



c. Installation.

(1) Install wires (1) in connector (3) as tagged. Remove tags.

(2) Position connector (3) in rear of front panel (5).

(3) Position and hold ground lug (4) and nutplate (2) on rear of connector (3).

(4) Install four screws (7) and washers (6). Torque to 6-8 inch/pounds.

d. Follow-on Procedures.

(1) If working on connector J23, install bottom cover (para 5-8).

(2) If working on J1 through J11, J15, or J16, install top cover (para 5-8).

5-19. CONNECTORS J19 THROUGH J22

NOTE

Procedure is the same for J19 through J22.

a. Preliminary Procedure. Remove bottom cover (para 5-8).

b. Removal.

(1) Remove insulation sleeving (2) from wires (1).

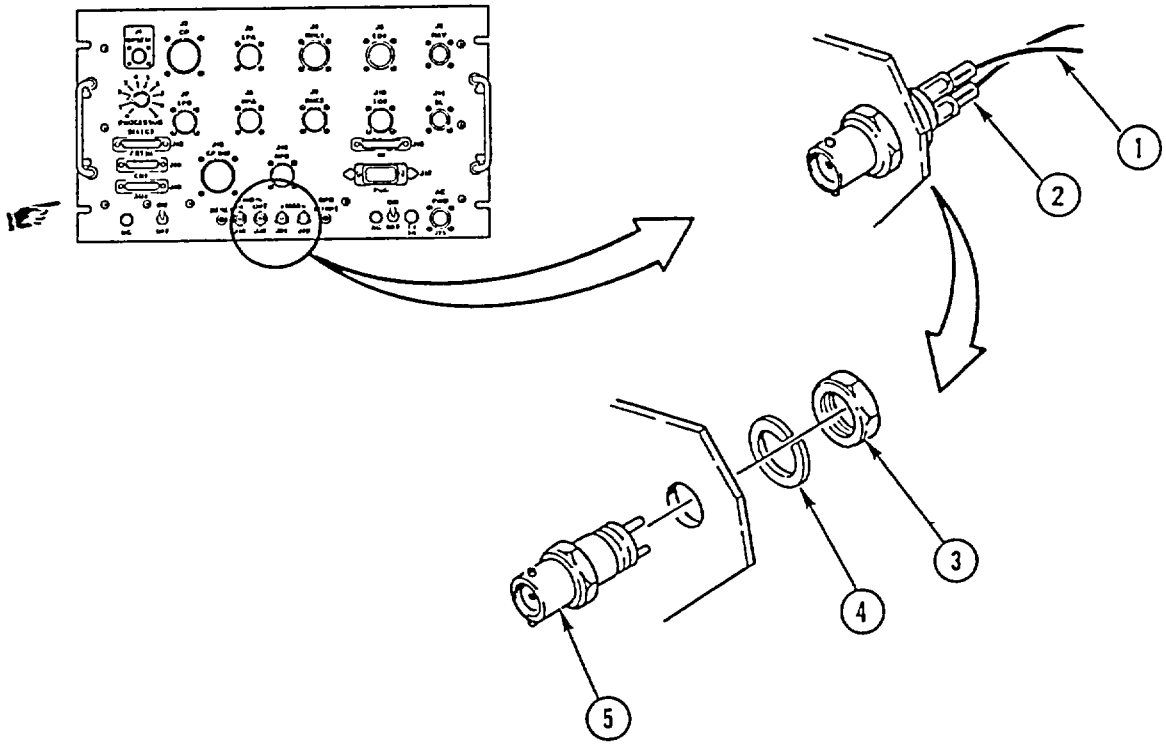
WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(2) Tag, unsolder, and remove wires (1).

(3) Remove nut (3) and washer (4).

(4) Remove connector (5).



5-19. CONNECTORS J19 THROUGH J22 - Continued

c. Installation.

(1) Place connector (5) in installed position.

(2) Install nut (3) and washer (4).

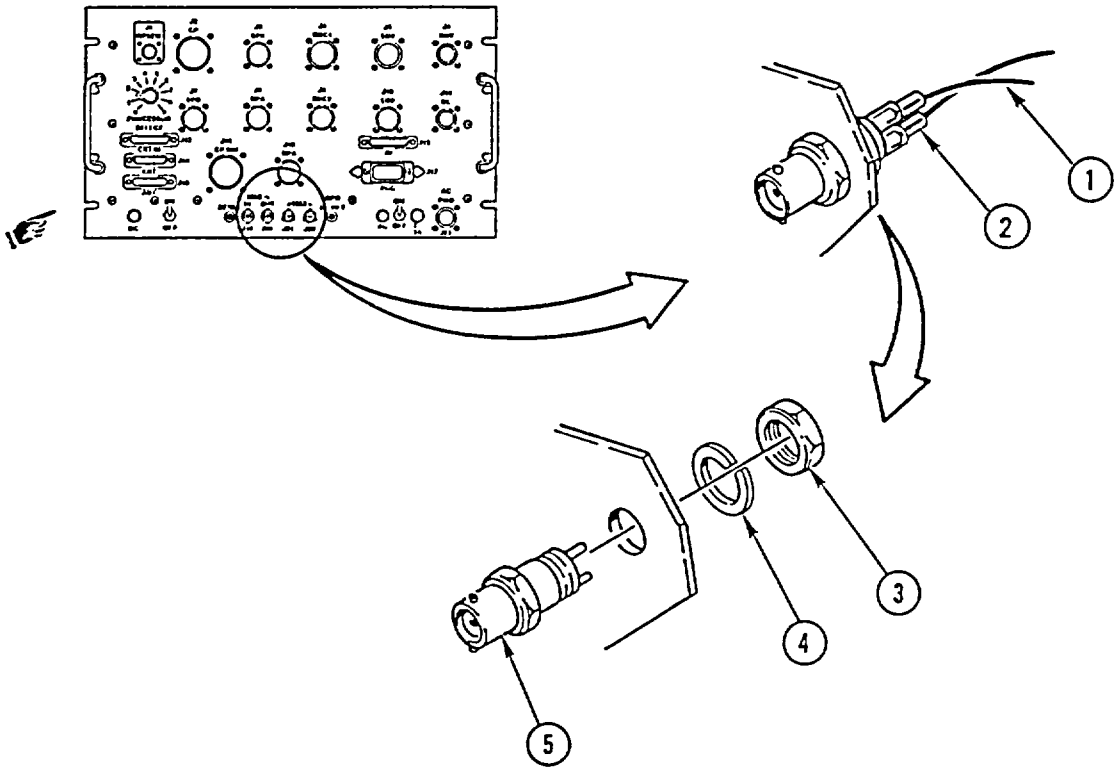
(3) Place new lengths of insulation sleeving (2) on wires (1).

WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(4) Resolder wires (1) as tagged. Remove tags.

(5) Using heat gun, position and shrink insulation sleeving (2).



d. Follow-on Procedure. Install bottom cover (para 5-8).

5-20. P1 CONNECTORS AT MOTHERBOARD

NOTE

Procedure is the same for all P1 connectors terminated at motherboard.

a. Preliminary Procedure. Remove top cover (para 5-8).

b. Removal.

(1) Loosen two captive screws (2).

(2) Disconnect connector (4).

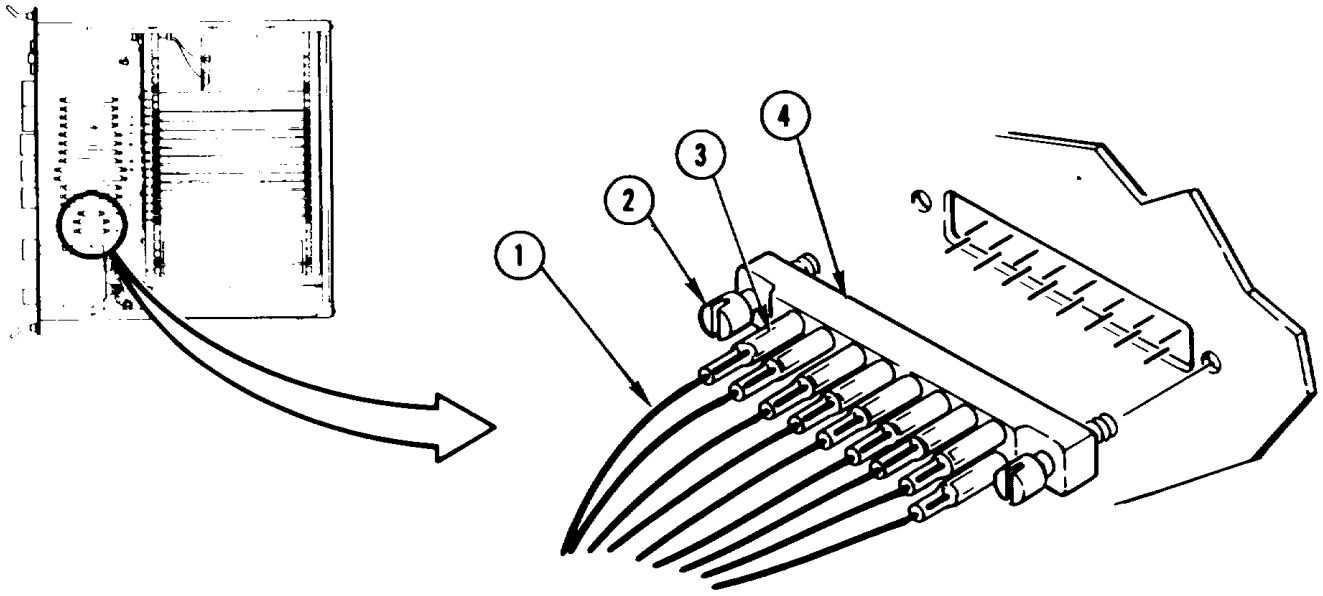
(3) Remove insulation sleeving (3).

WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(4) Tag, unsolder, and remove wires (1).

(5) Remove connector (4).



5-20. P1 CONNECTORS AT MOTHERBOARD - Continued

c. Installation.

(1) Position new length of insulation sleeving (3) on wires (1).

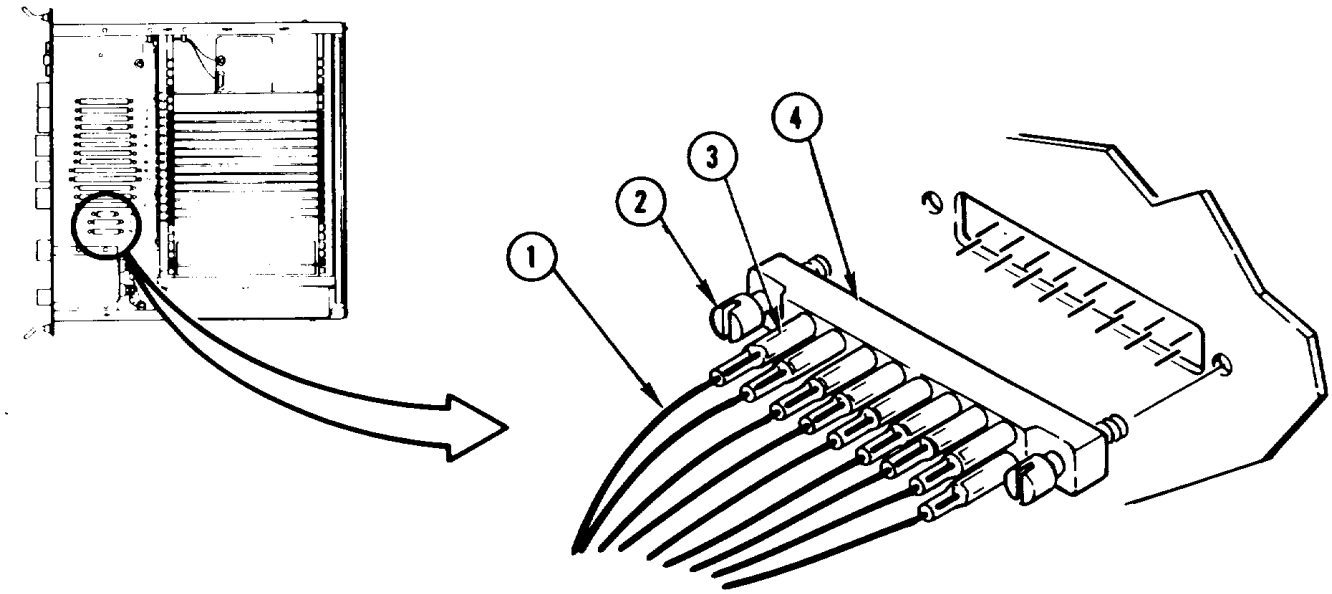
WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(2) Resolder wires (1) on connector (4) as tagged. Remove tags.

(3) Connect connector (4).

(4) Tighten two captive screws (2).



d. Follow-on Procedure. Install top cover (para 5-8).

5-21. REPAIR WIRE HARNESS

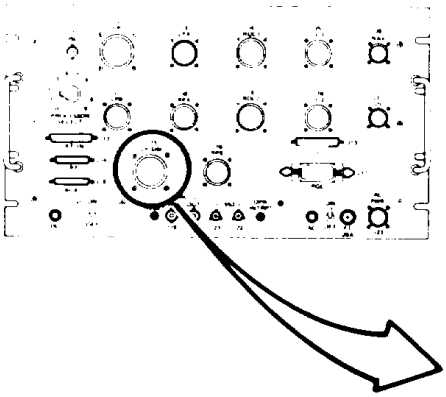
NOTES

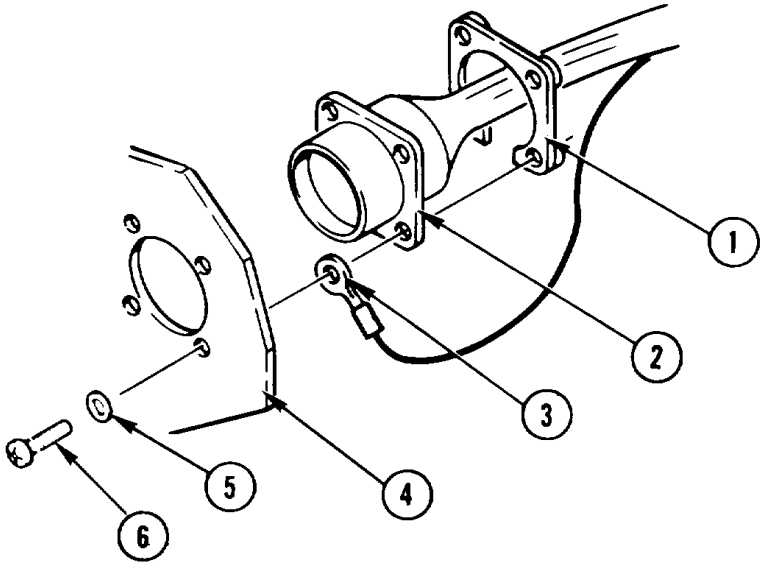
- **This procedure covers wire harness assemblies W2 through W11, W13, and W14. To repair wire harness W12, send IUTS to higher level maintenance.**
- **Refer to wiring diagram foldouts to find where the damaged wire(s) or cable(s) are terminated at the front panel (J connectors) and connector plate assembly (P connectors).**
- **This procedure covers wire harness removal, replacement of damaged wire(s), and wire harness reinstallation.**

a. Preliminary Procedure. Remove top cover (para 5-8).

b. Removal (Wire Harness).

(1) Remove four screws (6) and washers (5), nutplate (1), ground lug (3), and connector (2) from front panel (4).



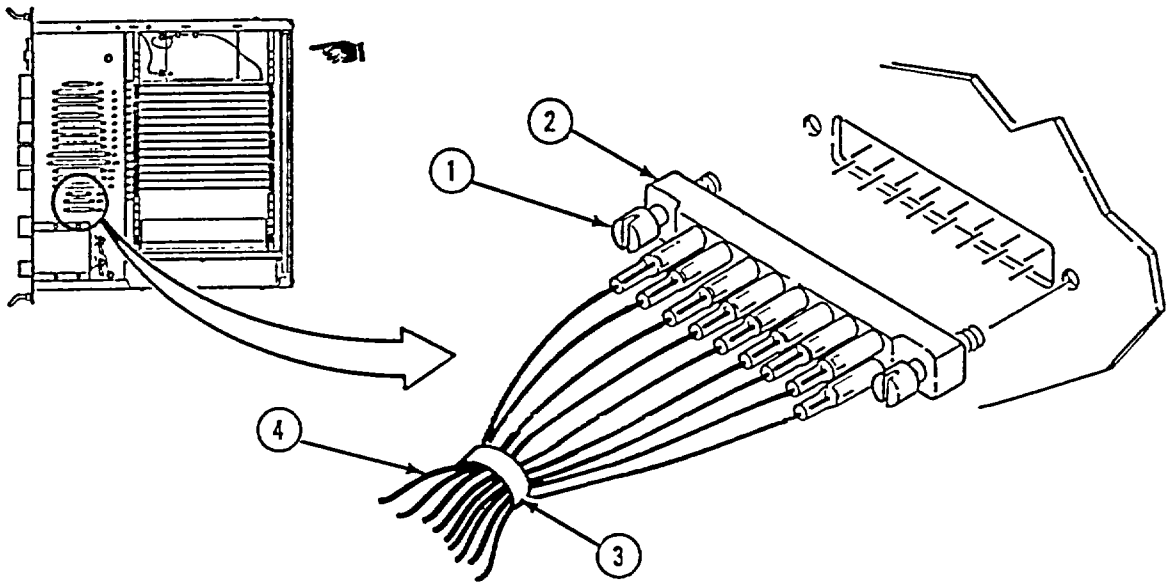


5-21. REPAIR WIRE HARNESS - Continued

(2) Loosen captive screws (1) and disconnect connector (2).

(3) Remove cable ties (3), as required, to isolate wire harness (4).

(4) Remove wire harness (4).



5-21. REPAIR WIRE HARNESS - Continued

c. Replacement (Wire).

(1) Check wire harness continuity to isolate damaged wire(s) (3). Tag wire(s).

(2) Cut and remove cable ties (2), as required.

(3) Remove insulation sleeving (4) at P connector (5).

WARNING

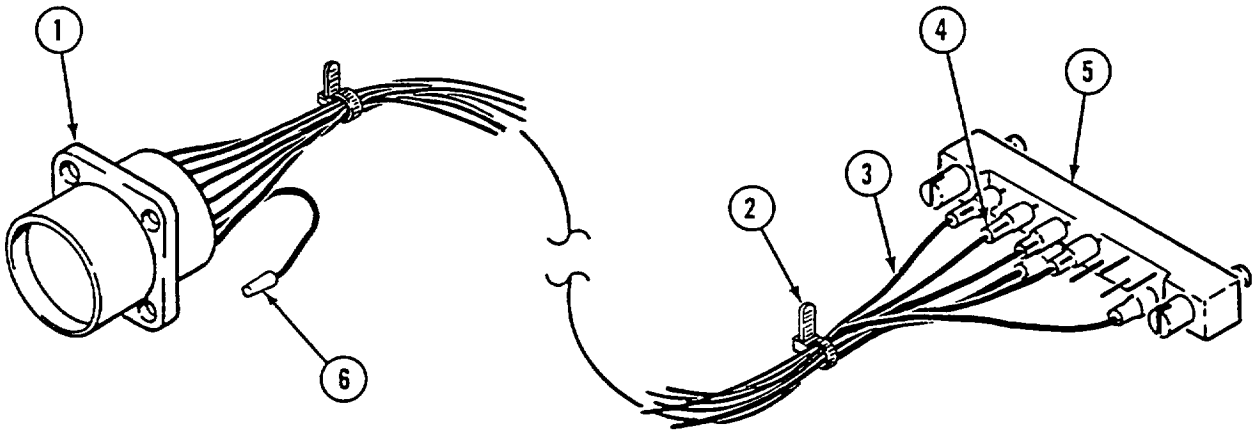
Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(4) Tag, unsolder, and remove damaged wires (3) from P connector (5).

(5) Remove wire(s) (3) and crimped contact (6) from J connector (1).

(6) Position replacement wire(s) (3) in installed position.

(7) Dress both ends of replacement wire(s) (3).



5-21. REPAIR WIRE HARNESS - Continued

(8) Position new length of insulation sleeving (4) on wire(s) (3) for P connector (5).

WARNING

Soldering operations can cause serious burns and eye injuries. Gloves, safety glasses, and protective apron are required.

(9) Resolder wire(s) (3) to P connector (5) as tagged.

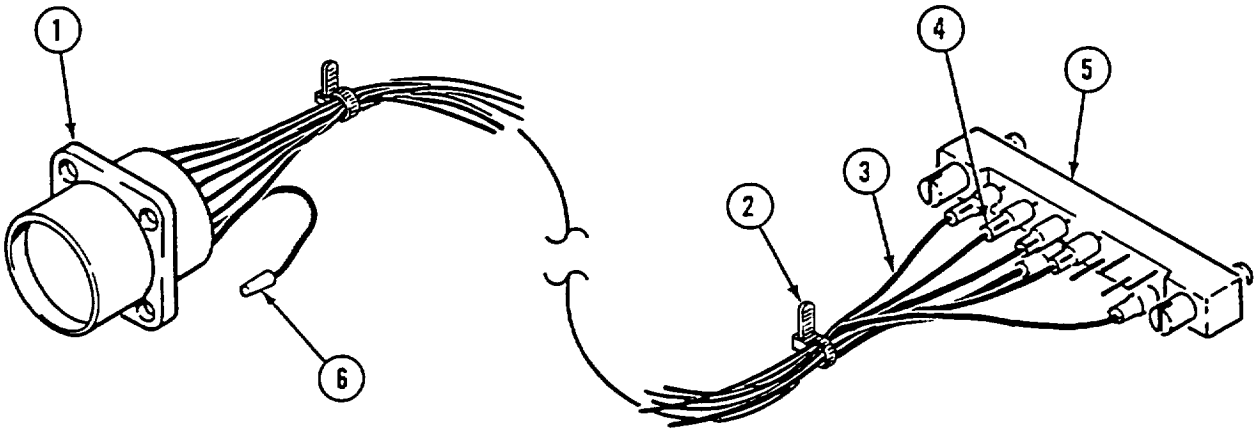
(10) Using heat gun, position and shrink insulation sleeving (4).

(11) Crimp replacement contact (6) to wire(s) (3).

(12) Install wire(s) (3) in J connector (1) as tagged. Remove tags.

(13) Install cable ties (2) as required.

(14) Check wire harness continuity. Repeat steps (1) through (12) until wire harness is good, or send wire harness to higher level maintenance.

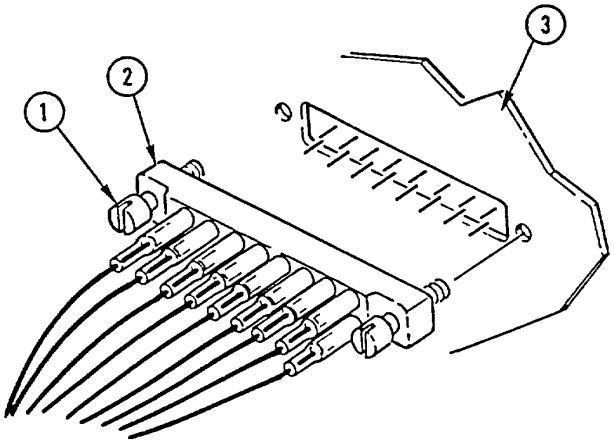


5-21. REPAIR WIRE HARNESS - Continued

d. Installation (Wire Harness).

(1) Connect P connector (2) to motherboard (3).

(2) Tighten two captive screws (1).

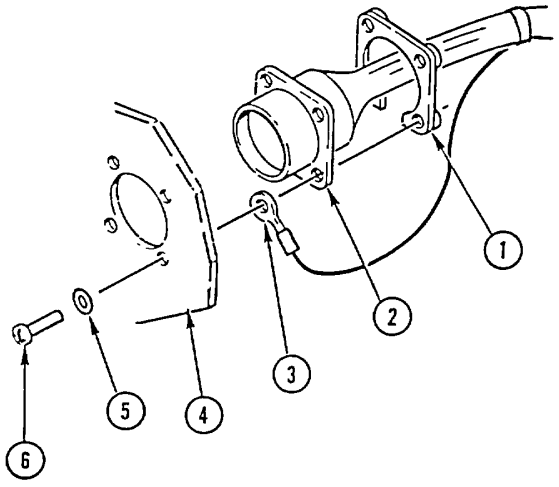


(3) Position J connector (2), ground lug (3) and nutplate (1) on rear of front panel (4).

NOTE

On serial number 1001A through 1004A, there is a marking plate attached to the front panel by the mounting screws of W25. Remove and install this marking plate as required.

(4) Install four screws (6) and washers (5). Torque to 6-8 inch/pounds.



e. Follow-on Procedures. Install top cover (para 5-8).

5-22. HELICOIL INSERTS

a. Removal.

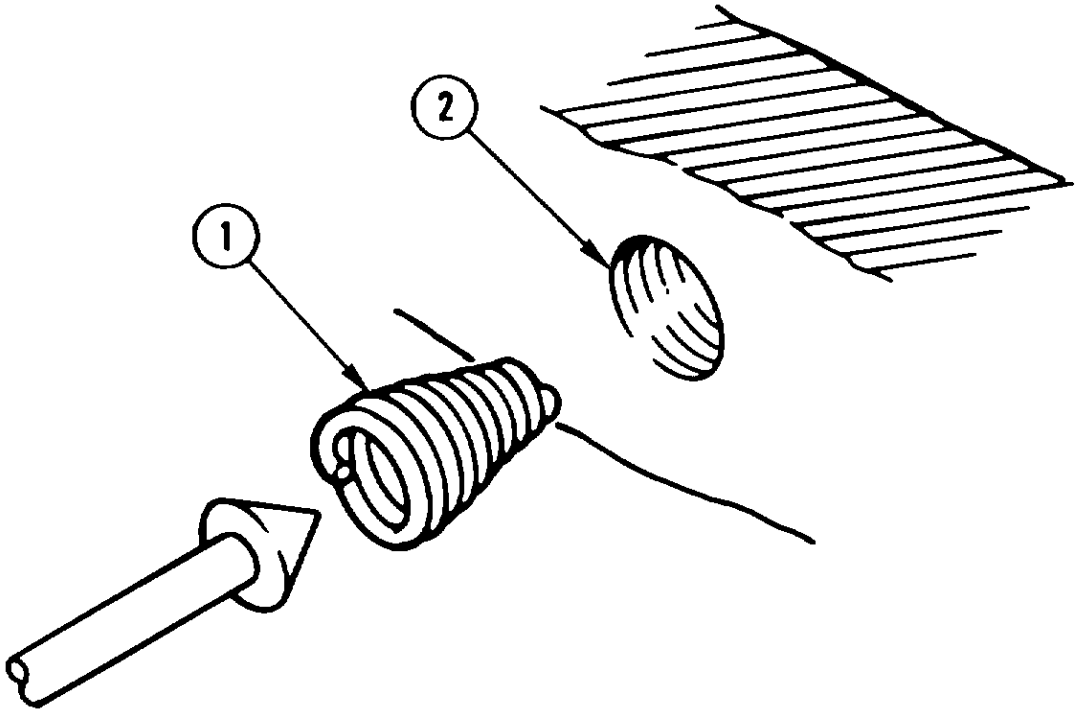
(1) Using removal tool, press and turn insert (1) counterclockwise.

(2) Remove insert (1). If insert cannot be removed, go to step (3).

(3) Using scribe, pry top thread of insert (1) away from housing hole (2).

(4) Using needle-nose pliers, turn insert (1) counterclockwise.

(5) Remove insert (1).



5-22. HELICOIL INSERTS - Continued

b. Installation.

WARNING

Isopropyl alcohol is flammable and moderately toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate.

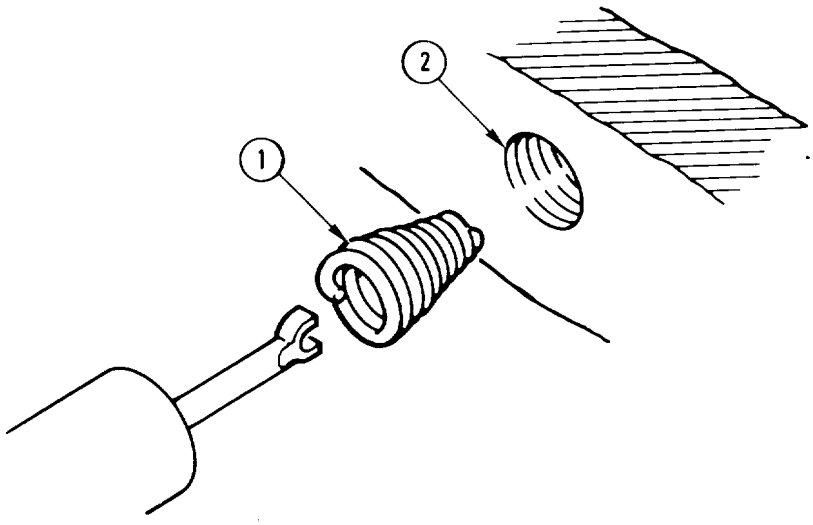
(1) Using pipe cleaner or swab, and isopropyl alcohol, clean housing hole (2).

(2) Place new insert (1) on insertion tool.

WARNING

Zinc chromate dust primer is highly toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate.

(3) Coat insert (1) with zinc chromate dust primer.



5-22. HELICOIL INSERTS - Continued

NOTE

Top thread of insert should be below housing surface between 1/4 and 1-1/2 turns.

(4) Using insertion tool, install insert (1) in housing hole (2) as follows:

(a) Aline insert threads with hole threads.

(b) Press insertion tool outer housing against hole housing (3).

(c) Turn insertion tool clockwise to thread insert into hole within limits given.

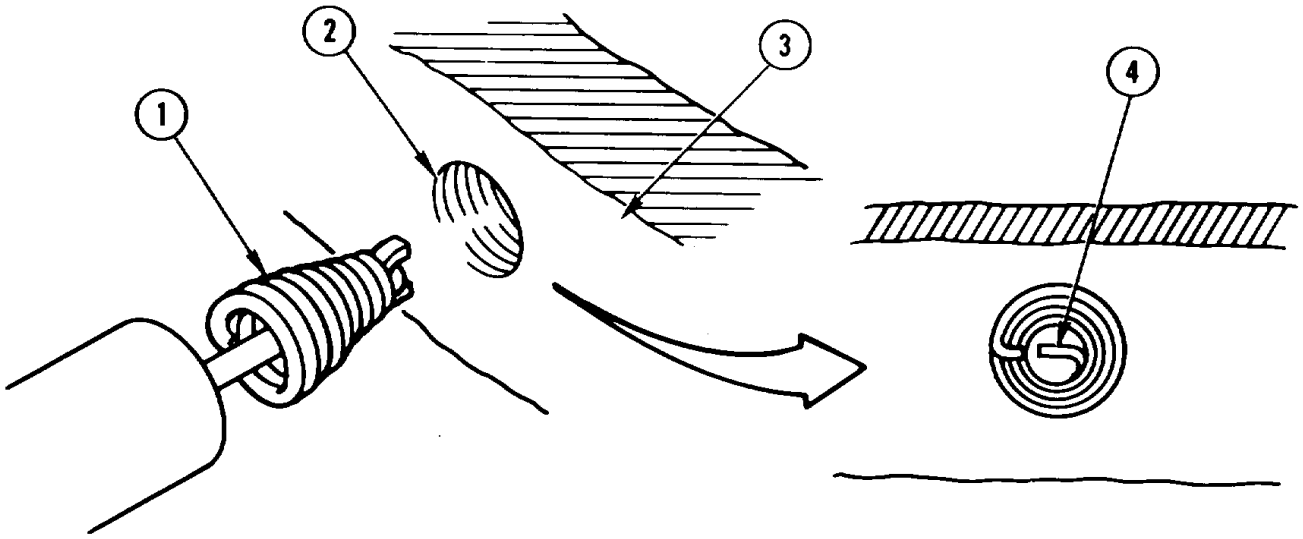
(5) Ensure insert (1) is between 1/4 and 1-1/2 turns below housing surface.

(a) If insert is installed within limits given, go to step (6).

(b) If insert is not installed within limits given, replace insert.

(6) Using tang removal tool, press and remove insert tang (4) from bottom of insert.

(7) Allow zinc chromate dust primer one hour to cure.



c. Follow-on Procedure. Install cover (para 5-8).

Section IV. PREPARATION FOR STORAGE OR SHIPMENT

5-23. STORAGE FACILITIES

a. Security of the stored equipment is required. The area used for storage must protect the equipment from being stolen.

b. The equipment in storage must be protected from the weather. Covered storage is required.

5-24. PROCEDURES

a. The equipment to be stored must be in good working order. Perform an operational check on the equipment prior to storage (para 5-5 and 5-6).

b. When putting the equipment into administrative storage (1-45 days) use a storage area that is accessible. Equipment in administrative storage must be able to be removed from storage and put into operation on 24 hour notice.

APPENDIX A

REFERENCES

A-1. SCOPE

This appendix lists all forms, field manuals, technical manuals, and miscellaneous publications referenced in this manual. Only those publications available to, and required by the user are listed.

A-2. FORMS

Recommended Changes to Publications and Blank Forms ..... DA Form 2028, DA Form 2028-2

Equipment Inspection and Maintenance Worksheet ..... DA Form 2404

Report of Discrepancy (ROD) ..... SF 364

Product Quality Deficiency Report ..... SF 368

A-3. FIELD MANUALS

First Aid and Safety ..... FM 21-11

A-4. TECHNICAL MANUALS

Operator's, Organizational, and Direct Support Maintenance Manual for Airborne Relay Facility AN/ARW-83(V)6 ..... TM 11-5895-332-13

Operator's, Organizational, and Direct Support Maintenance Manual for Interface Unit J-4522/U ..... TM 11-5895-1279-13

Operator's, Organizational, and Direct Support Maintenance Manual for Receiver, Digital Control C-11634/U ..... TM 11-5895-1283-13

Operator's, Organizational, and Direct Support Maintenance Manual for Computer Processor CP-1692/U ..... TM 11-5895-1286-13

Organizational, and Direct Support Repair Parts and Special Tools List for Interface Unit Test Set TS-4221/U ..... TM 11-6625-3150-23P

A-4. TECHNICAL MANUALS - Continued

Operator's. Organizational and Direct Support Maintenance Manual for Electronic Shop, Semi-trailer Mounted, AN/USM-624 ..... TM 11-7440-331-13

A-5. MISCELLANEOUS PUBLICATIONS

The Army Maintenance Management System ..... DA Pam 738-750

Consolidated Index of Army Publication and Blank Forms ..... DA Pam 25-30

Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command) ..... TM 750-244-2

APPENDIX B
MAINTENANCE ALLOCATION CHART
FOR
INTERFACE UNIT TEST SET TS-4221/U

B-1. GENERAL

This appendix provides a summary of the maintenance operations for Interface Unit Test Set TS-4221/U. It authorizes levels of maintenance for specific maintenance functions of repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

B-2. MAINTENANCE FUNCTION

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean(decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.

j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/ operational condition as prescribed by maintenance standards (I.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

B-3. COLUMN ENTRIES

a. Column-1, Group Number. Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column 2, Component/Assembly. Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance functions. Column 3 lists the functions to be performed on the item listed in column 2. When Items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4, Maintenance Level. Column 4 specifies, by the listing of a "work time" figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated level of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance levels, appropriate "work time" figures will be shown for each level. The number of task-hours specified by the "work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

C - Operator/Crew, O - Unit Maintenance/Aviation Unit Maintenance, F - Direct Support /Aviation Intermediate Maintenance, H - General Support Maintenance, D - Depot Maintenance

e. Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in section IV, Remarks, which is pertinent to the item opposite the particular code.

B-4. TOOL AND TEST EQUIPMENT REQUIREMENTS (Section III)

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Level. The codes in this column indicate the maintenance level allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (5-digit) in parentheses.

B-5. REMARKS

a. Reference Code. This code refers to the appropriate item in section II, column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in section II.

Section II. MAINTENANCE ALLOCATION CHART FOR INTERFACE UNIT TEST SET TS-4221/U

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQUIPMENT	(6) REMARKS
			C	O	F	H	D		
00	INTERFACE UNIT TEST SET TS-4221/U	INSPECT		0.5				11	
		TEST		1.5				1, 2, 4, 5, 6, 7, 9,10,11	A
		REPAIR			2.6			5,11,12,13	B, C, D
		REPLACE		0.1					
		OVERHAUL					5.0		
01	CCA TS D/A	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	
02	CCA INTERFACE	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	
03	CCA SIMULATOR	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	
04	CCATSIFP	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	
05	CCA TSLO	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	

SECTION II
MAINTENANCE ALLOCATION CHART
FOR
INTERFACE UNIT TEST SET TS-4221/U
(CONTINUED)

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQUIPMENT	(6) REMARKS
			C	O	F	H	D		
06	CCA TSRF	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	
07	CCA 1553 IF	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	
08	CCA IUDL	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	
09	CCA IU NAV	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	
10	CCA TS BUS	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	
11	CCA DBP	INSPECT			0.4			11	
		TEST					0.2		
		REPAIR					0.5		
		REPLACE			0.4				
		FAULT LOC					0.5	11	

SECTION II
MAINTENANCE ALLOCATION CHART
FOR
INTERFACE UNIT TEST SET TS-4221/U
(CONTINUED)

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQUIPMENT	(6) REMARKS
			C	O	F	H	D		
12	CCA PSRAM	INSPECT TEST REPAIR REPLACE FAULT LOC			0.4 0.4 		 0.2 0 5 0.5	11 11	
13	OSCILLATOR ASSY	INSPECT TEST REPAIR REPLACE FAULT LOC			0.4 0.4 		 0.2 0.5 0.5	11 11	
14	FAN PANEL ASSY	INSPECT TEST REPAIR REPLACE			0.3 0.8 1.6 0.3			11 5 11,13 11,13	

Section III. TOOL AND TEST EQUIPMENT REQUIREMENTS FOR INTERFACE UNIT TEST SET TS-4221/U

TOOL OR TEST EQUIPMENT REF CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL/NATO STOCK NUMBER	TOOL NUMBER
01	O, F	CONTROL PANEL C-11804/ALQ		
02	O, F	DIGITAL DELAY/WIDTH GENERATOR		
03	F	EXTENDER CARD		
04	O, F	INTERFACE UNIT		
05	O, F	MULTIMETER	6625-01-1329-2512	
06	O, F	OPERATOR TERMINAL		
07	O, F	OSCILLOSCOPE		
08	O, F	RECEIVER, DIGITAL CONTROL		
09	O, F	RECEIVER, POWER SUPPLY		
10	O, F	SYSTEM POWER SUPPLY		
11	O	TOOL KIT, ELECTRONIC EQUIPMENT TK-105/G	5180-00-010-0177	
12	F	TORQUE LIMITING SET		
13	F	HELICOIL KIT	5895-01-873-6874	
14	F	STOPWATCH		

Section IV. REMARKS

REFERENCE CODE	REMARKS
A	Organizational maintenance level accomplishes system tests using bit, mission test equipment and continuity tests of cables
B	Direct support maintenance level accomplishes those tests required to locate faulty modules, components, wiring and cable problems
C	Direct support maintenance level provides organizational maintenance assistance as required and repair of chassis frame by replacement of meters, switches, connectors, and other chassis and front panel mounted piece parts and selected modules/circuit cards and cable assembly repair/replacement.
D	Direct support maintenance level repairs minor damage to LRU chassis and covers by straightening, sanding and spot painting

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Section IV. REMARKS

REFERENCE CODE	REMARKS
A	Organizational maintenance level accomplishes system tests using bit, mission test equipment, and continuity tests of cables.
B	Direct support maintenance level accomplishes those tests required to locate faulty modules, components, wiring and cable problems.
C	Direct support maintenance level provides organizational maintenance assistance as required and repair of chassis/frame by replacement of meters, switches, connectors, and other chassis and front panel mounted piece parts and selected modules/circuit cards and cable assembly repair/replacement.
D	Direct support maintenance level repairs minor damage to LRU chassis and covers by straightening, sanding, and spot painting.
E	Direct support will check the dual bus processor CCA to determine that the following applicable microcircuits are installed: For the Marine Corps microcircuit USG shall carry the part number 845035C0925 and USH shall carry the part number 845035C0926. For the Army microcircuit USG shall carry the number C5118219 and USH shall carry the numberC5118220. The depot shall change the microcircuits.

By Order of the Secretary of the Army:

GORDON R. SULLIVAN
General, United States Army
Chief of Staff

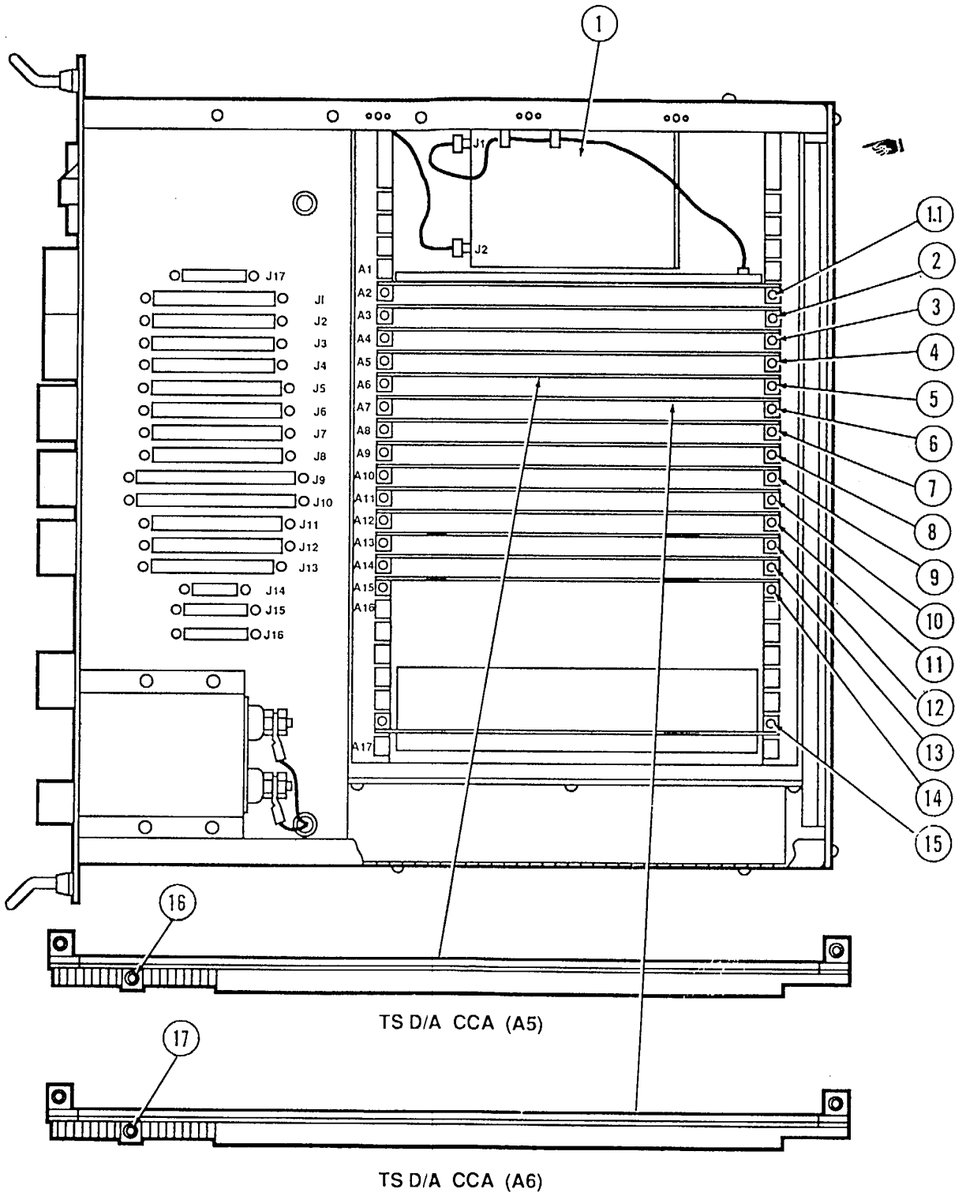
Official:

MILTON H. HAMILTON
Administrative Assistant to the
Secretary of the Army
01381

DISTRIBUTION:

To be distributed in accordance with DA Form 12-36-E, block 9224, Operator and Unit, Direct and General Support maintenance requirements for TM 11-6625-3150-13.

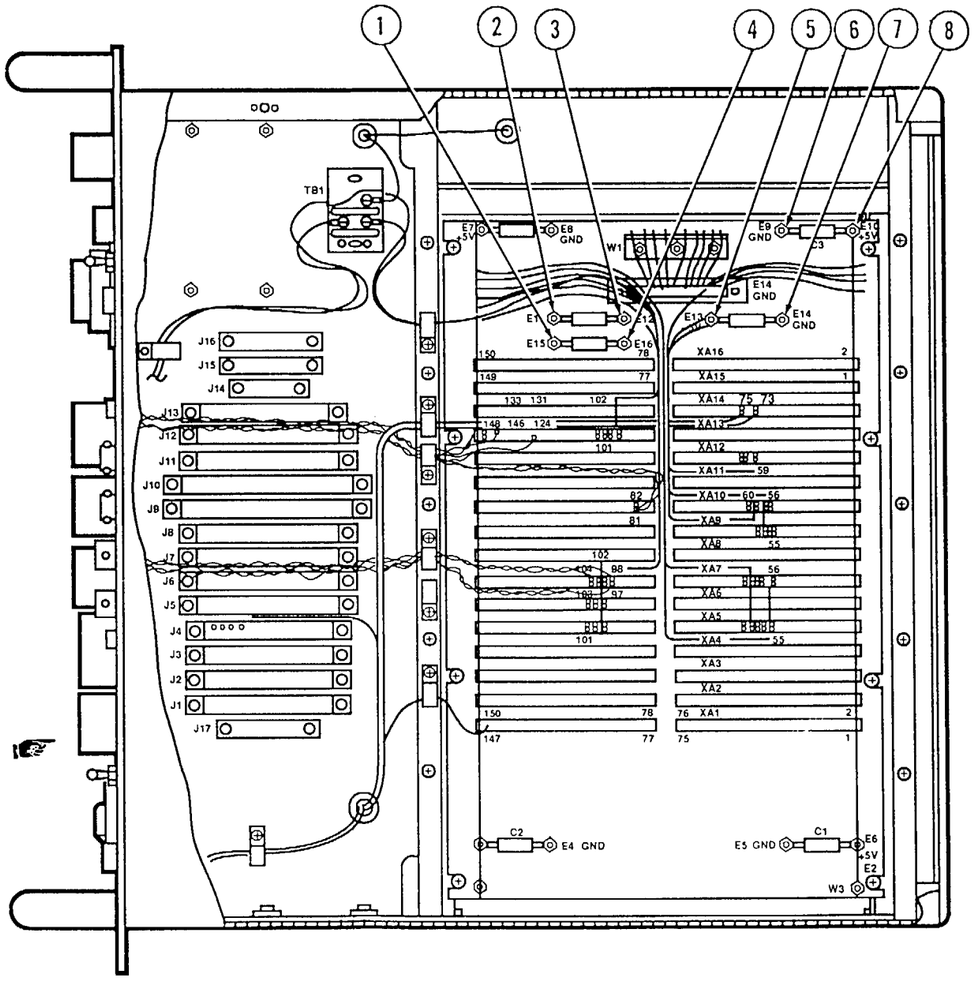
***U.S GOVERNMENT PRINTING OFFICE: 1992 - 682-084/60210**



REFERENCE DESIGNATION	COMPONENTS	
G1	OSCILLATOR	1
A2	TICK GENERATOR CCA	1.1
A3	COMPUTER PROCESSOR INTERFACE (CPIF)	2
A4	COMPUTOR PROCESSOR SIMULATOR CCA	3
A5	TEST SET DIGITAL/ANALOG CCA (TSD/A)	4
A6	TEST SET DIGITAL/ANALOG CCA (TSD/A)	5
A7	TEST SET IF PROCESSOR CCA (TSIFP)	6
A8	TEST SET LOCAL OSCILLATOR CCA (TSLO)	7
A9	TEST SET RADIO FREQUENCY CCA (TSRF)	8
A10	1553B INTERFACE CCA (1553B)	9
A11	INTERFACE UNIT DATA LINK CCA (IUDL)	10
A12	INTERFACE UNIT NAVIGATION CCA (IUNAV)	11
A13	TEST SET BUS CCA (TSBUS)	12
A14	DUAL BUS PROCESSOR CCA (DBP)	13
A15	PROGRAMMABLE STATIC RANDOM ACCESS MEMORY CCA (PSRAM)	14
A17	POWER SUPPLY CCA	15
	ADJUSTMENT POINT (A5)	16
	ADJUSTMENT POINT (A6)	17

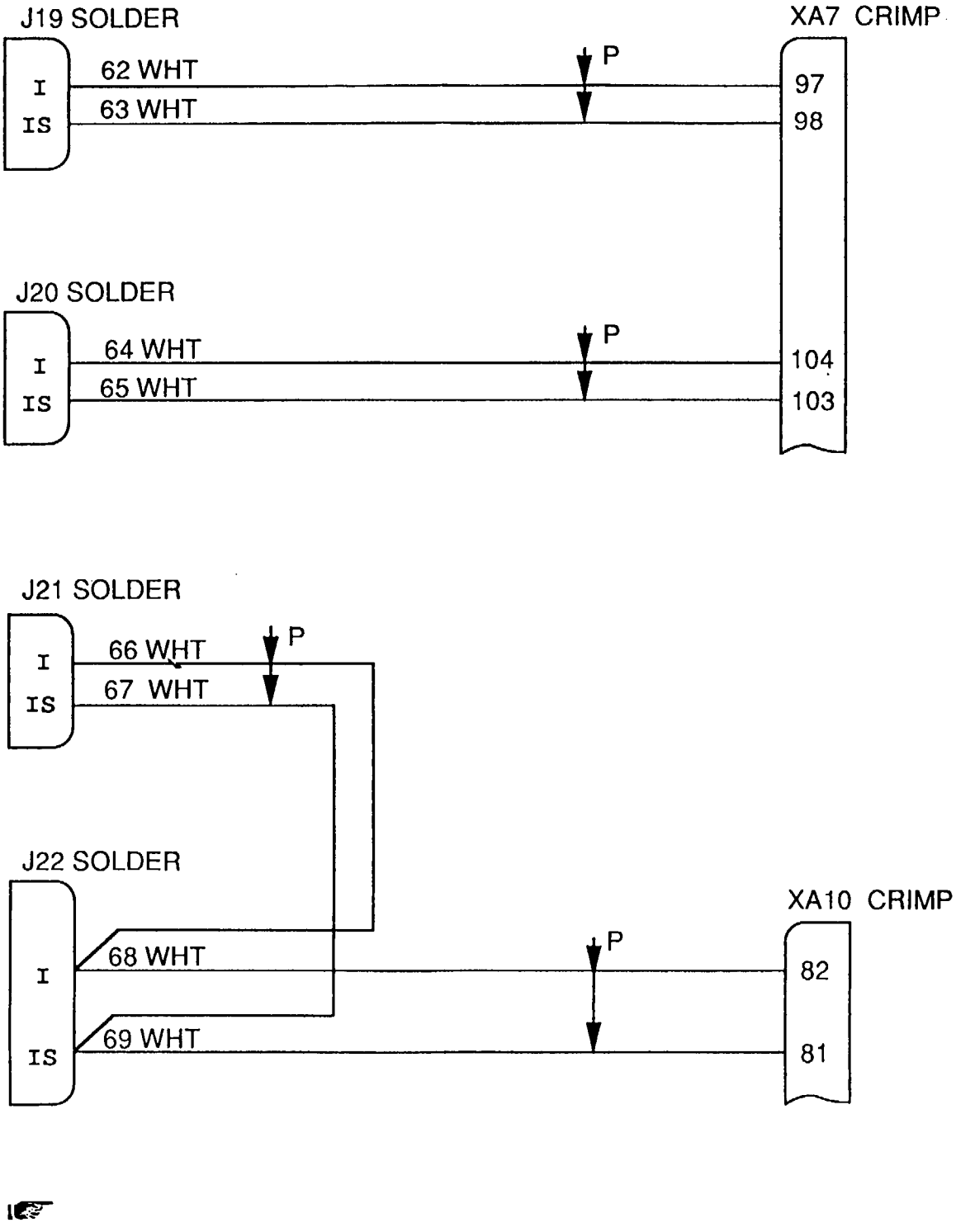
NOTE:
(CCA SLOTS A1, A16 NOT USED)

FO-1. Component Locations (Sheet 1 of 2)

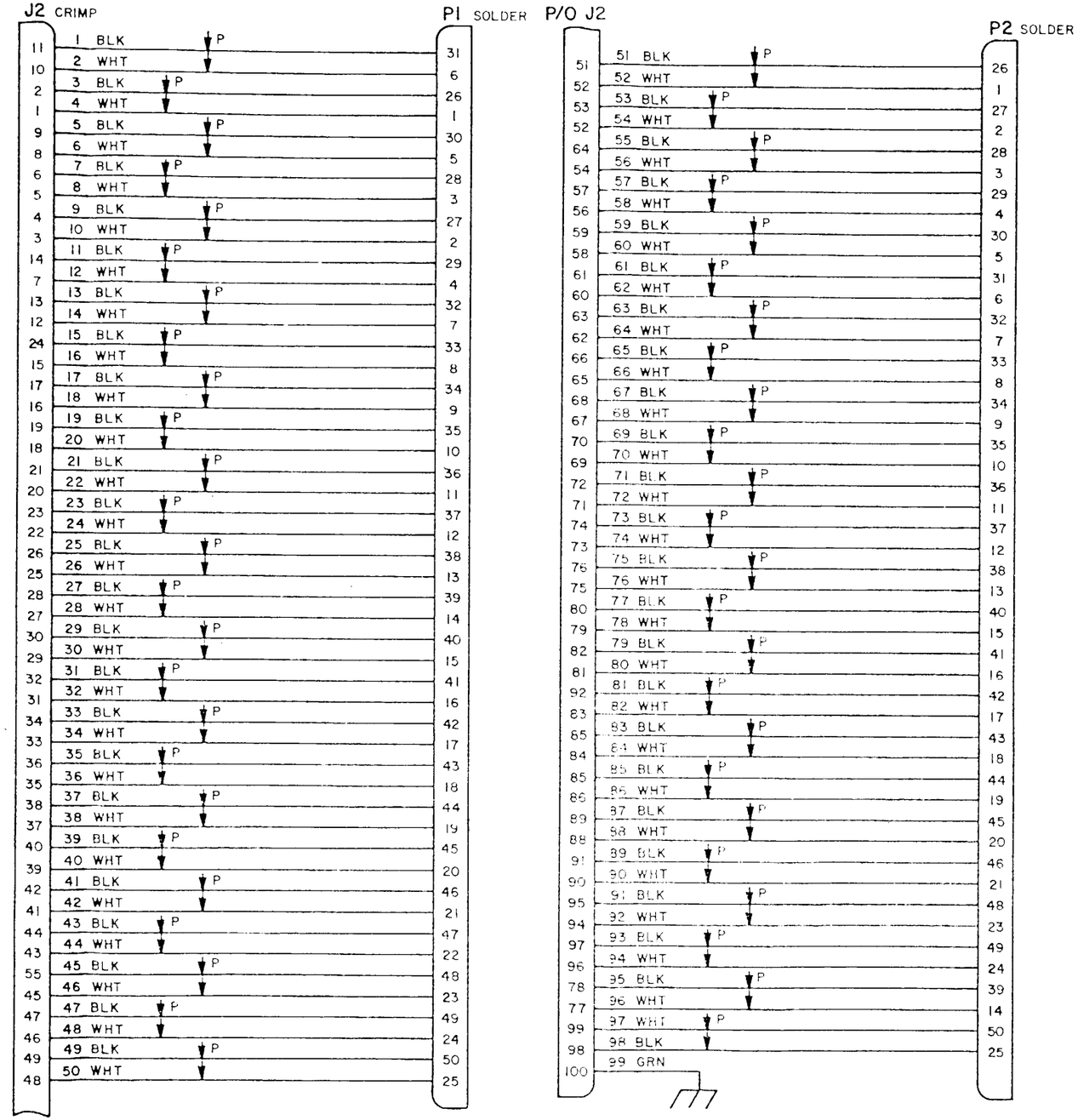


REFERENCE DESIGNATION	COMPONENTS	KEY
E15	GND	1
E11	GND	2
E12	+12.0 VDC	3
E16	GND	4
E13	-5.0 VDC	5
E9	GND	6
E14	GND	7
E10	+5.0 VDC	8

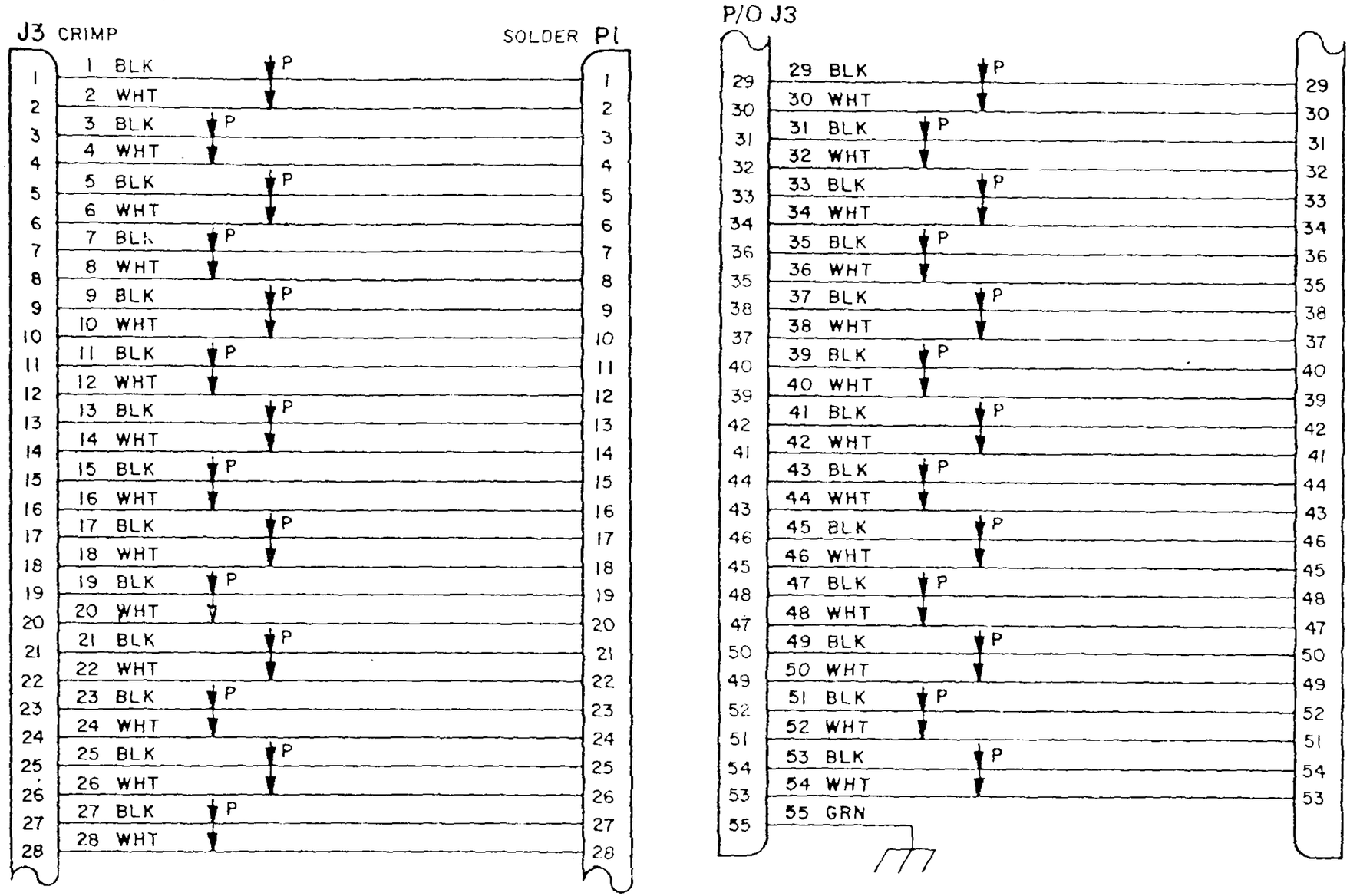
FO-1. Component Locations (Sheet 2 of 2)



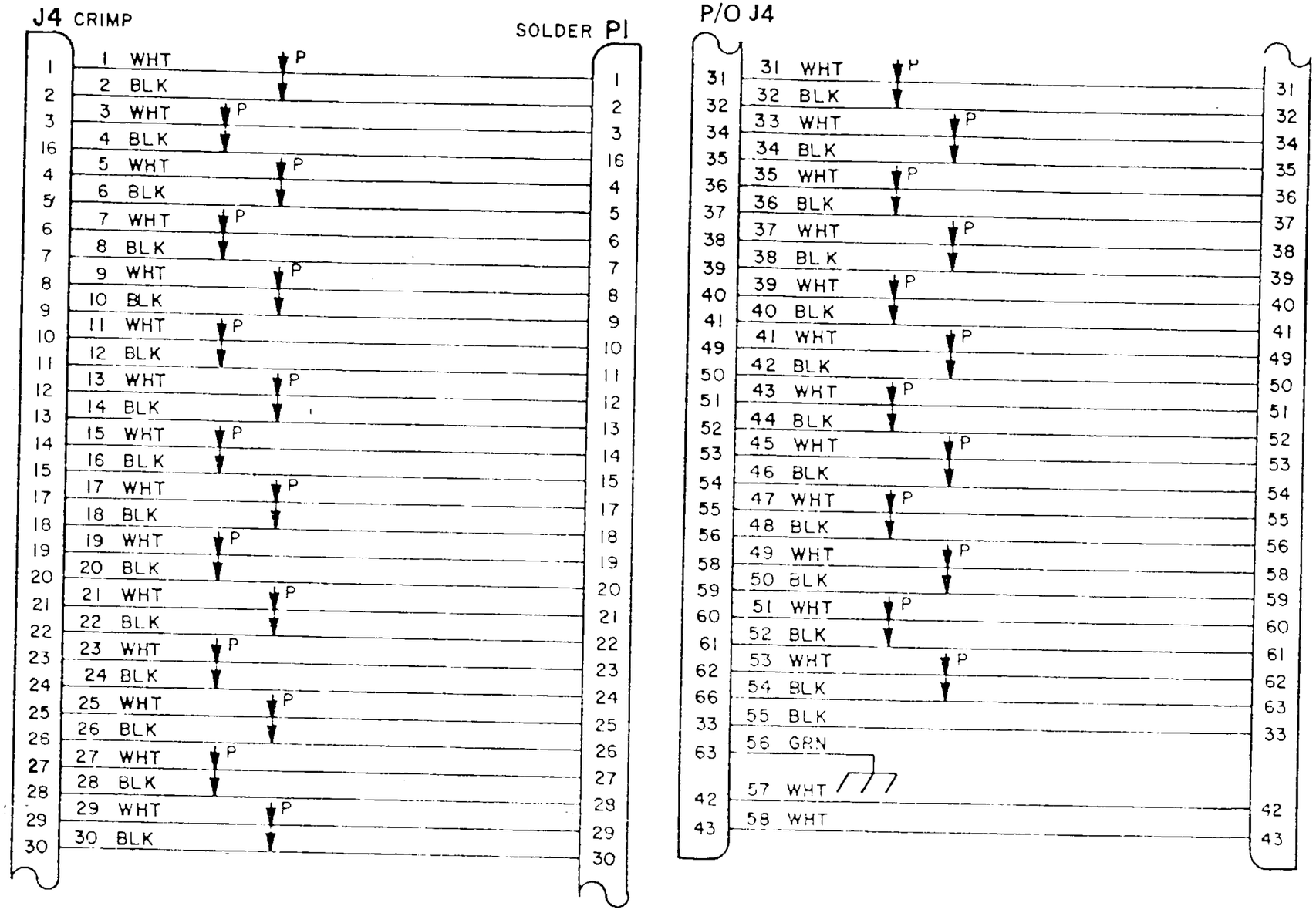
FO-2. Wiring Diagram, Axial Lead Connections



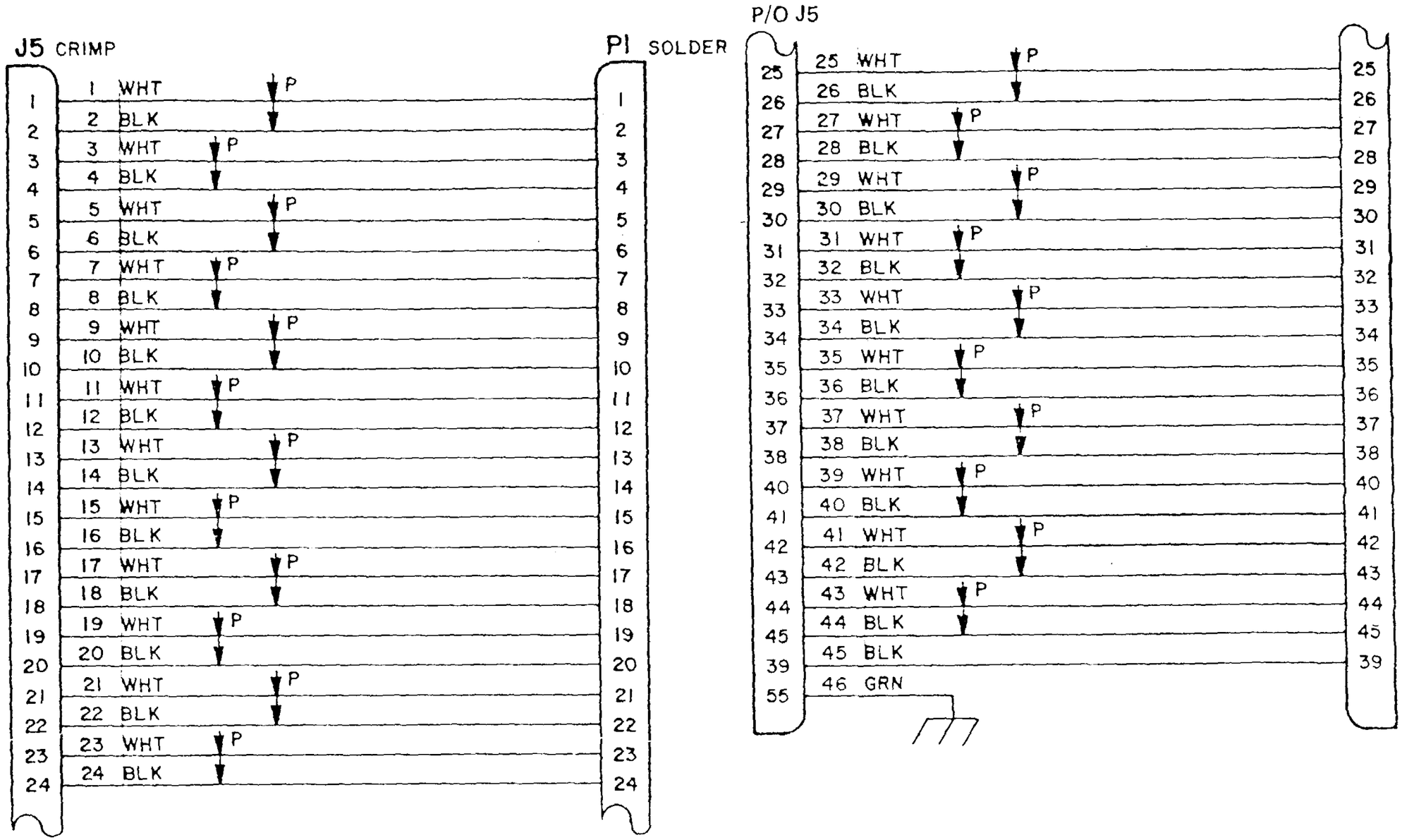
FO-3. Wiring Diagram, Cable Assembly W2 (J2-P1/P2)



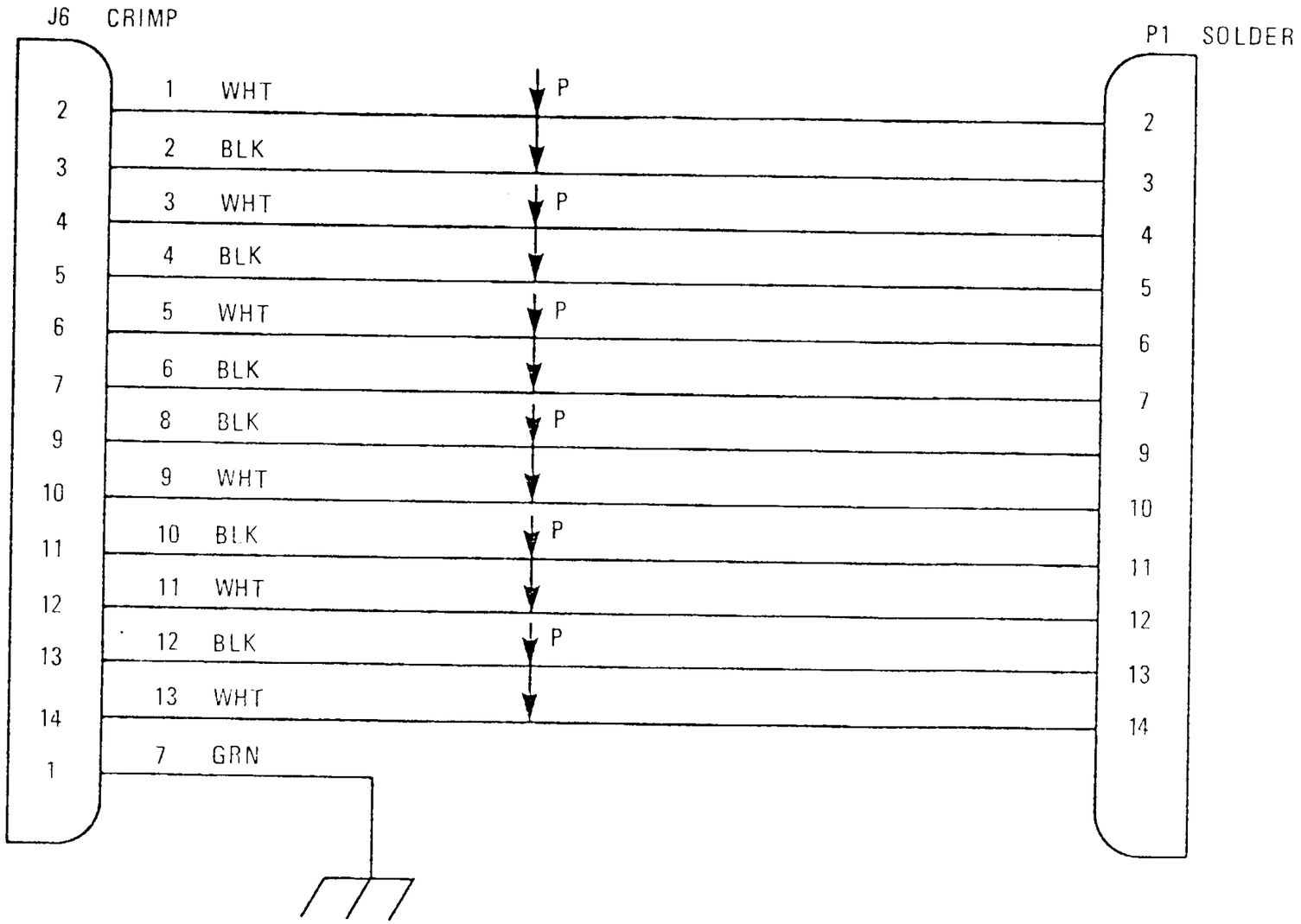
FO-4. Wiring Diagram, Cable Assembly W3 (J3-P1)



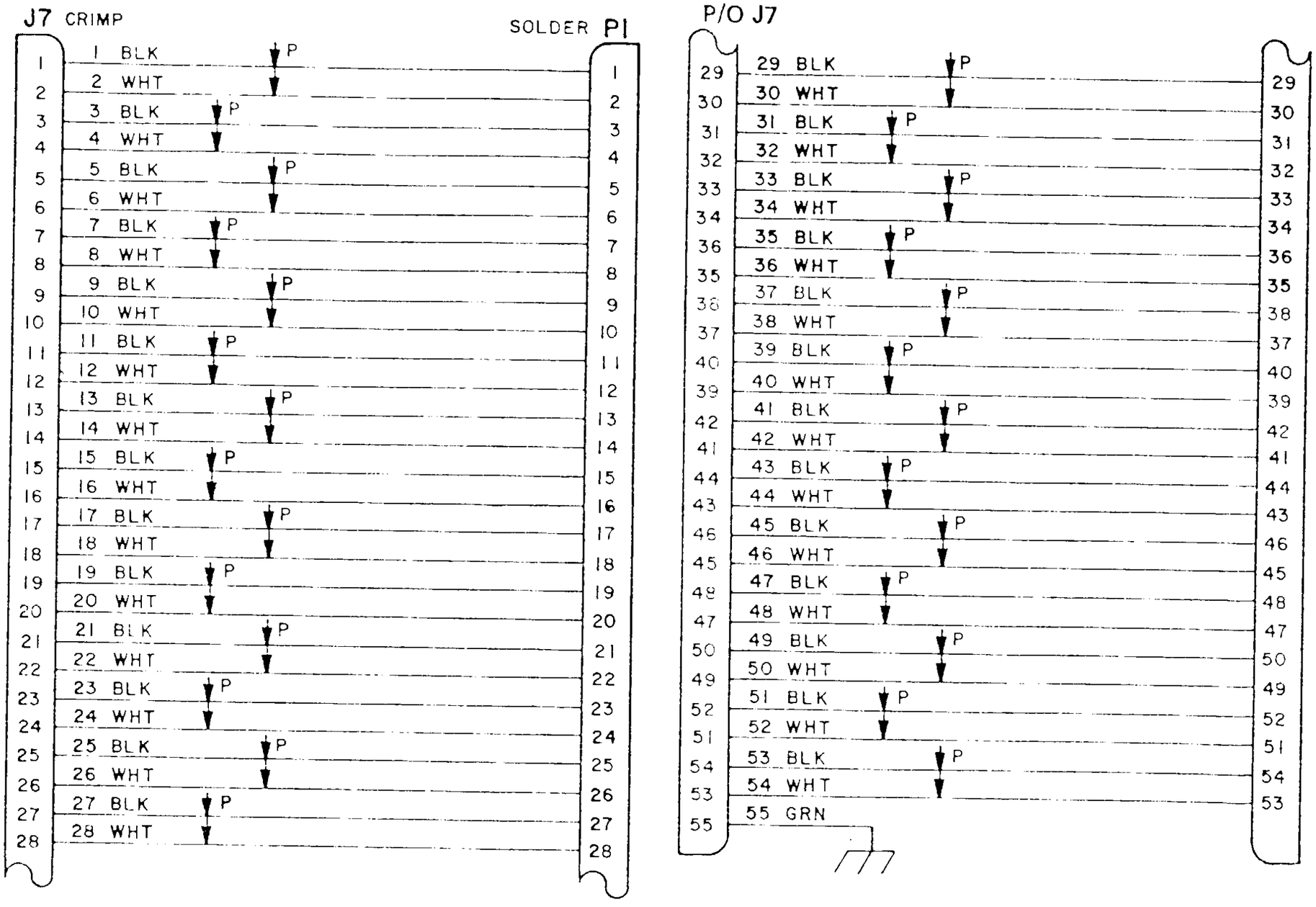
FO-5. Wiring Diagram, Cable Assembly W4 (J4-P1)



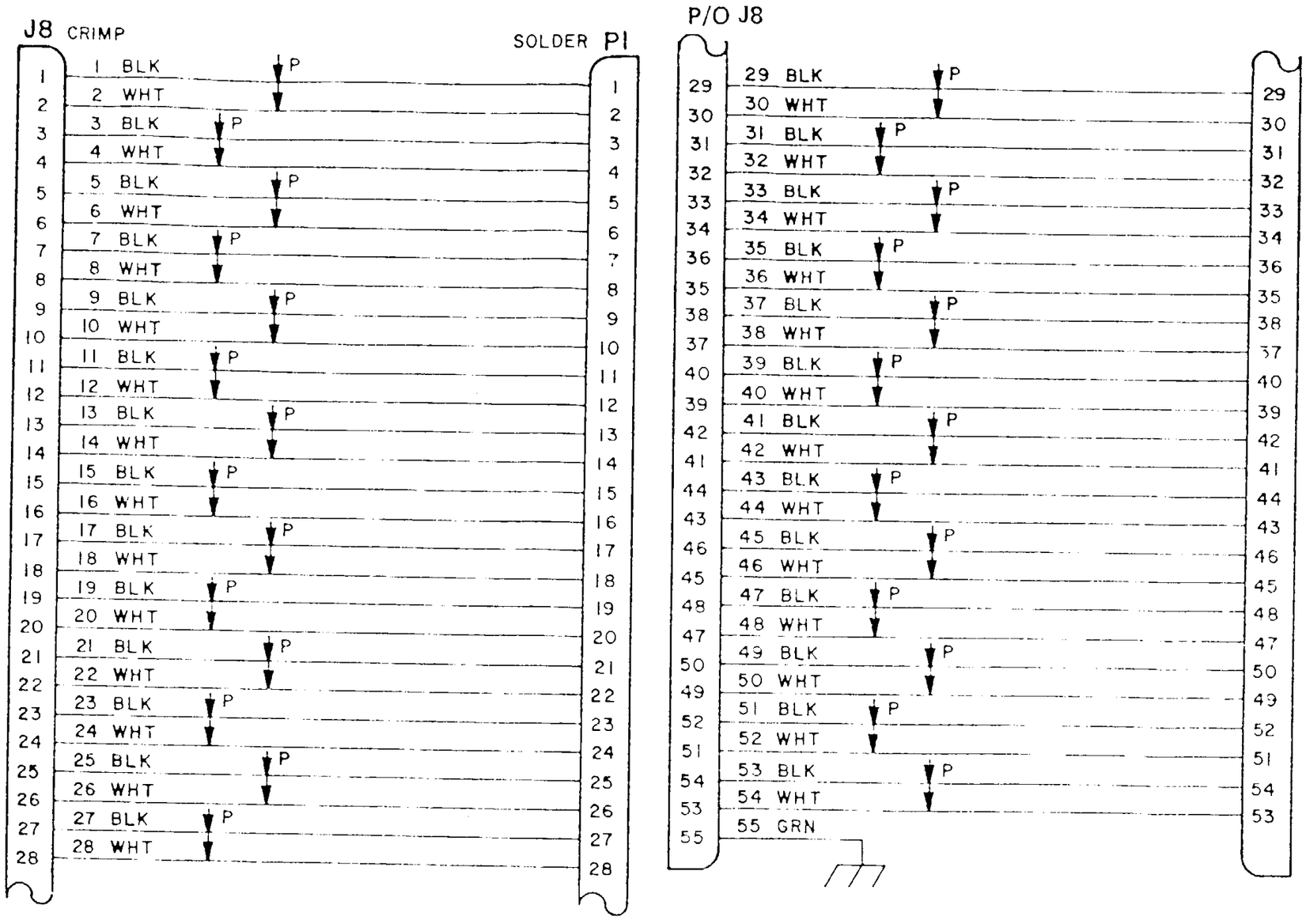
FO-6. Wiring Diagram Cable Assembly W5 (J5-P1)



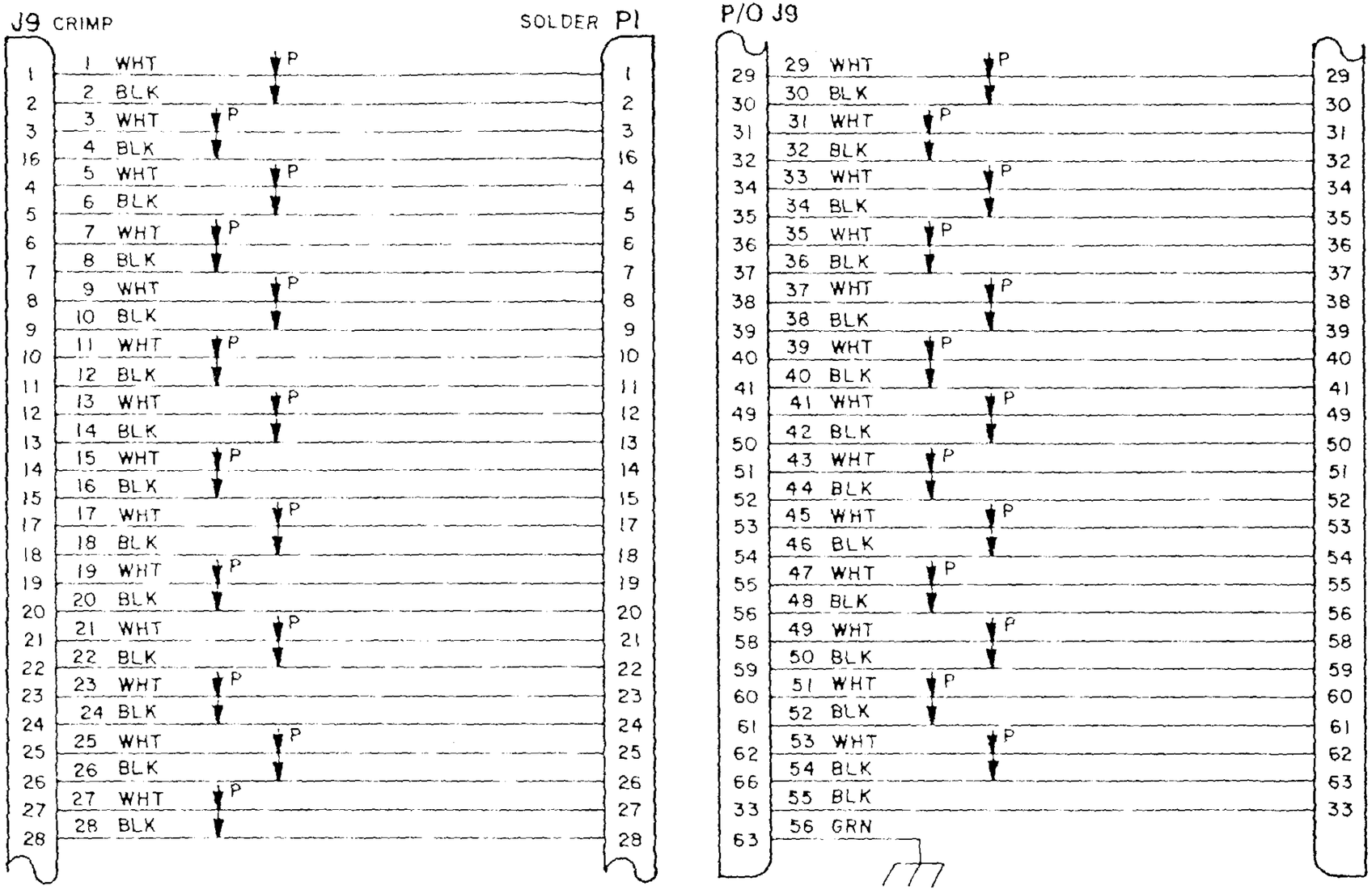
FO-7. Wiring Diagram, Cable Assembly W5 (J6-P1)



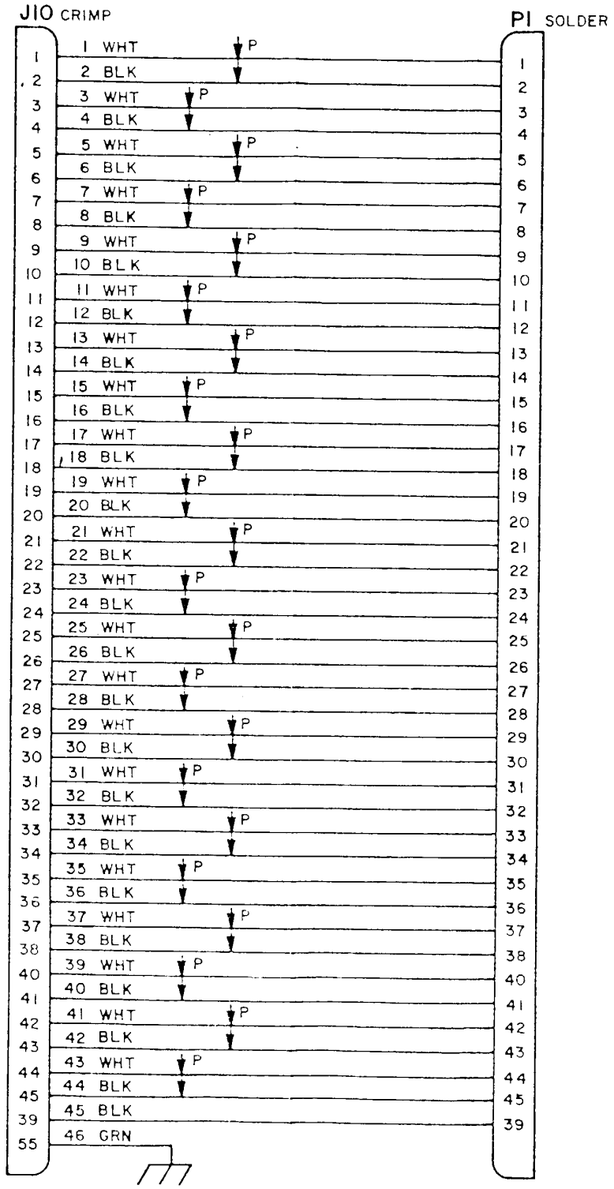
FO-8. Wiring Diagram, Cable Assembly W7 (J7-P1)



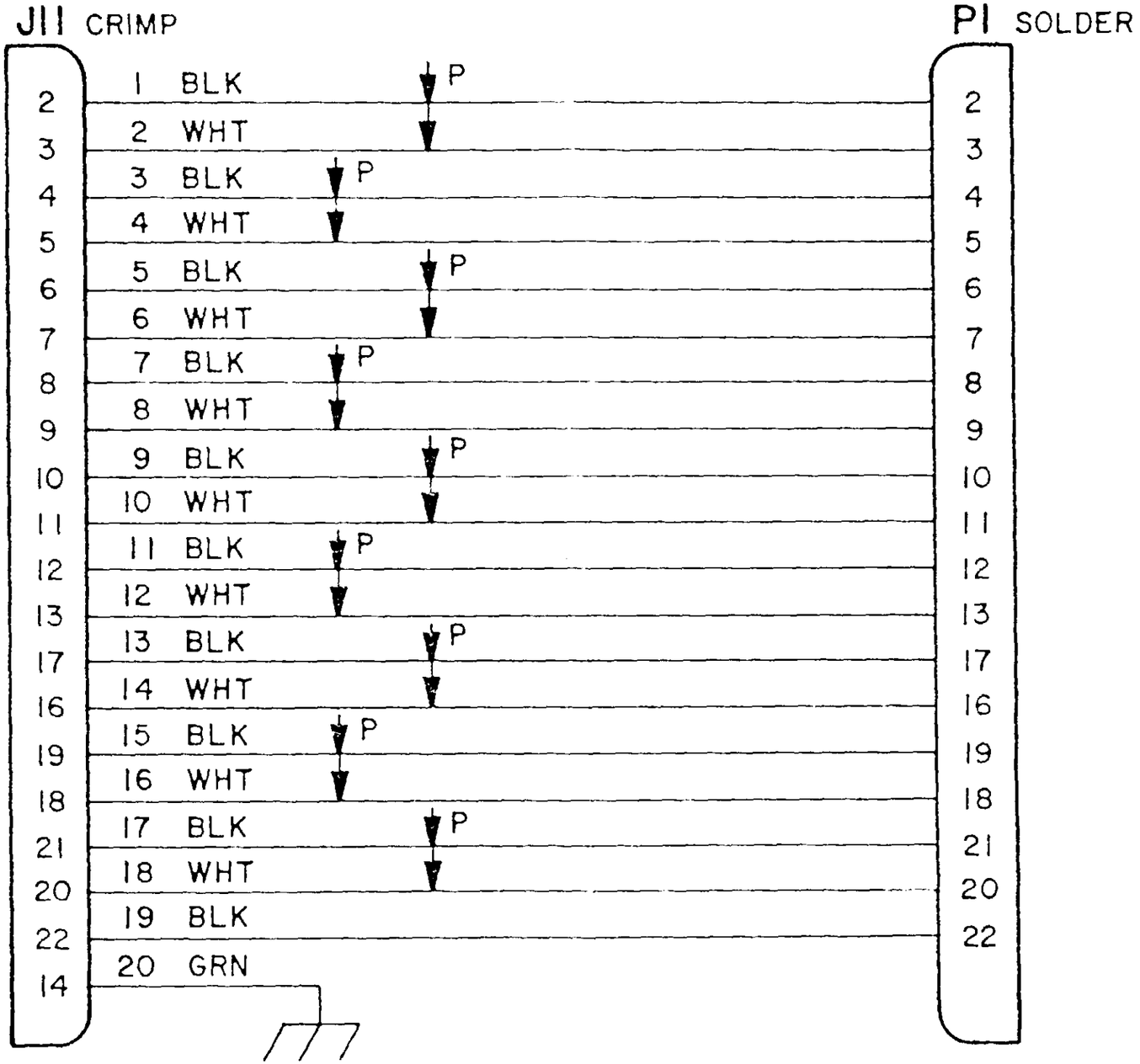
FO-9. Wiring Diagram, Cable Assembly W8 (J8-P1)



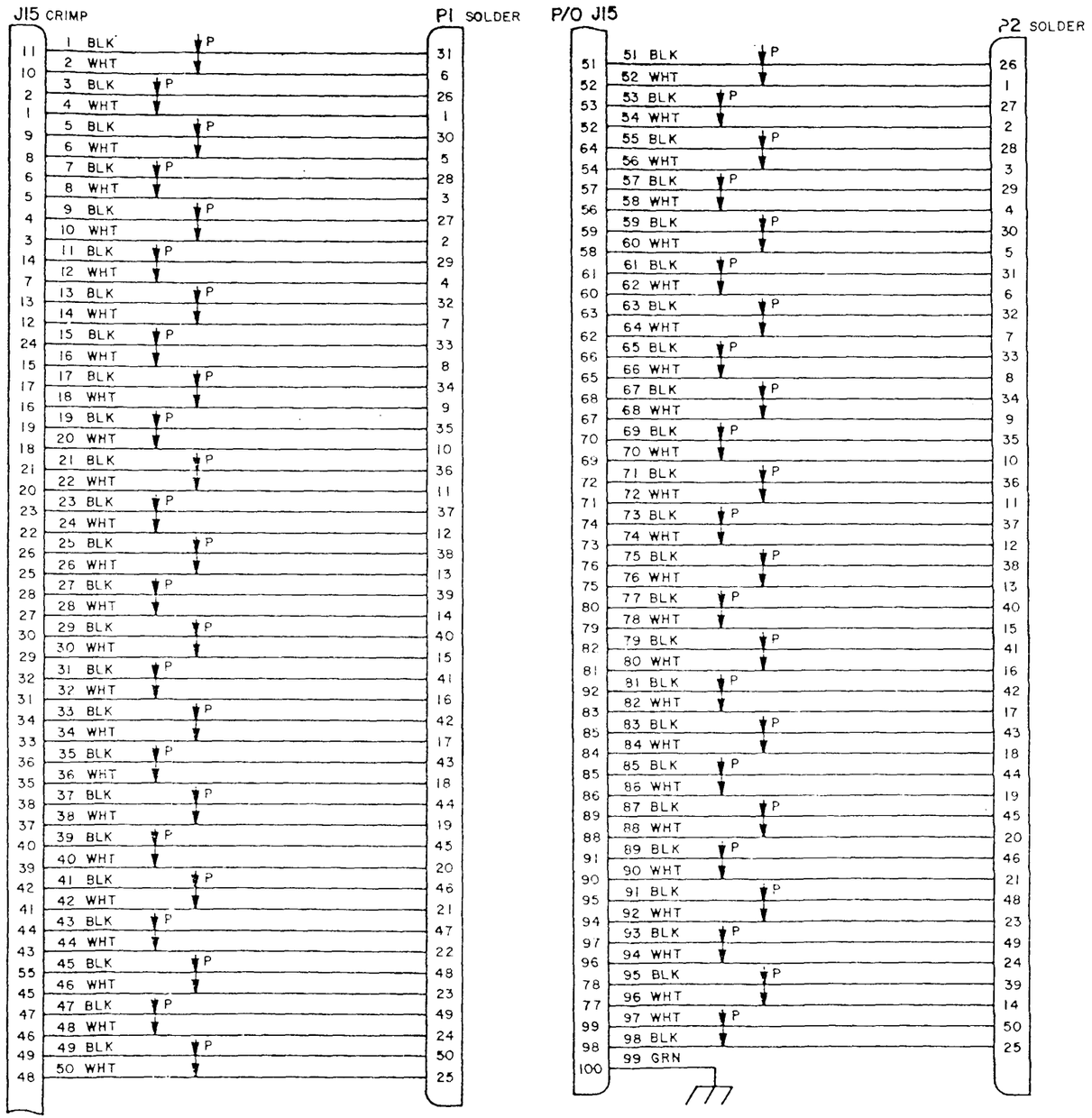
FO-10. Wiring Diagram, Cable Assembly W9 (J9-P1)



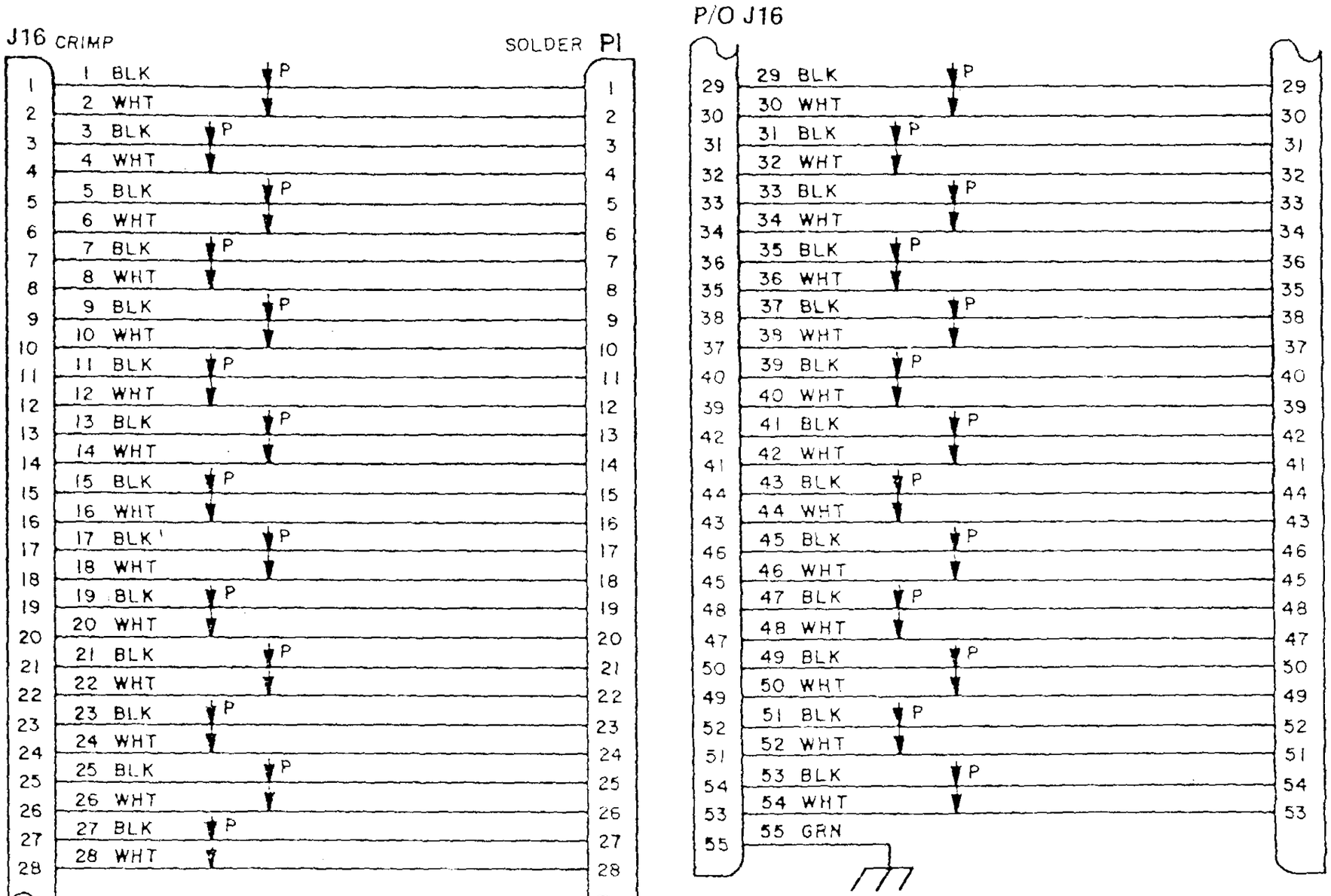
FO-11. Wiring Diagram, Cable Assembly W10 (J10-P1)



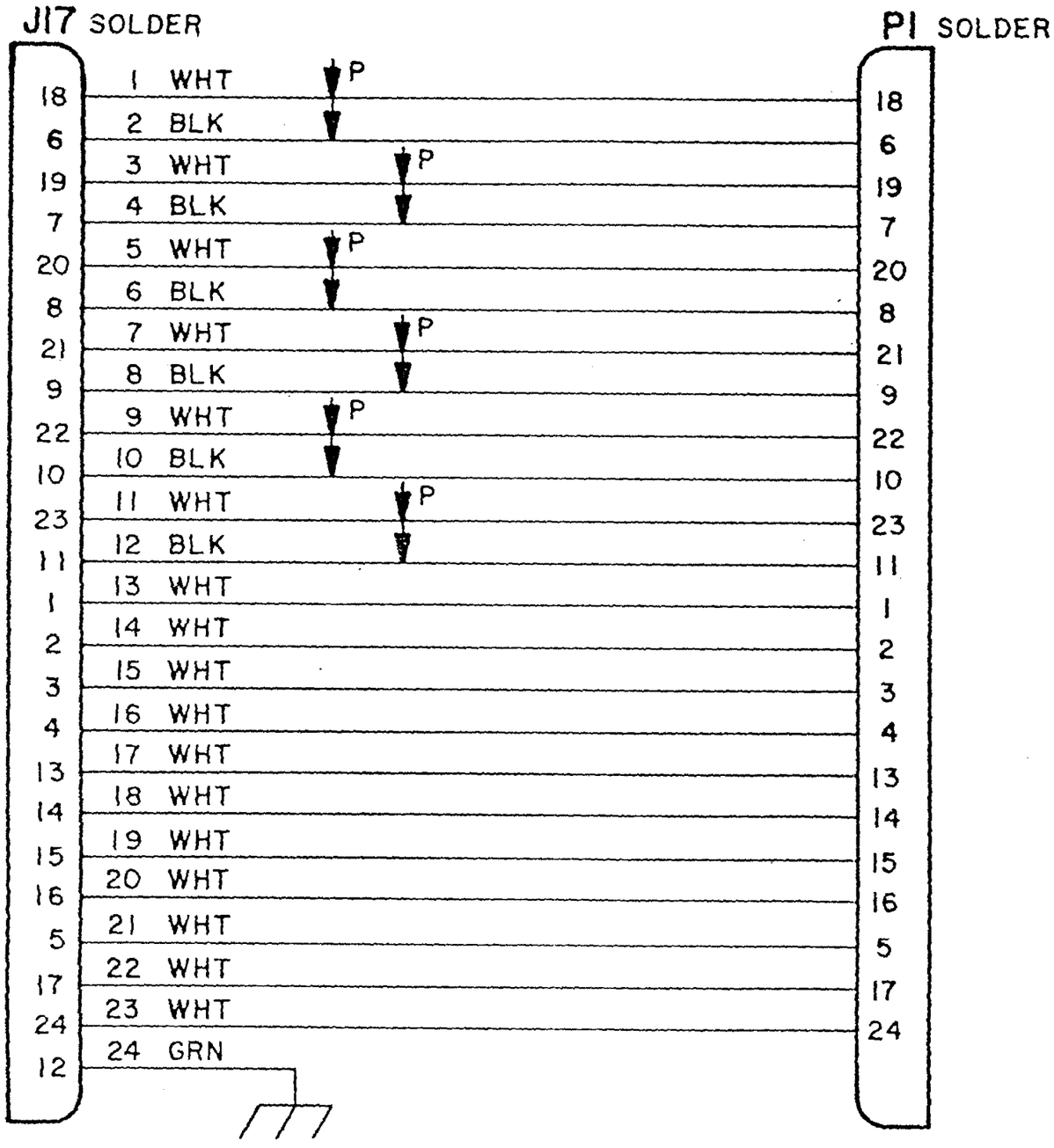
FO-12. Wiring Diagram, Cable Assembly W11 (J11-P1)



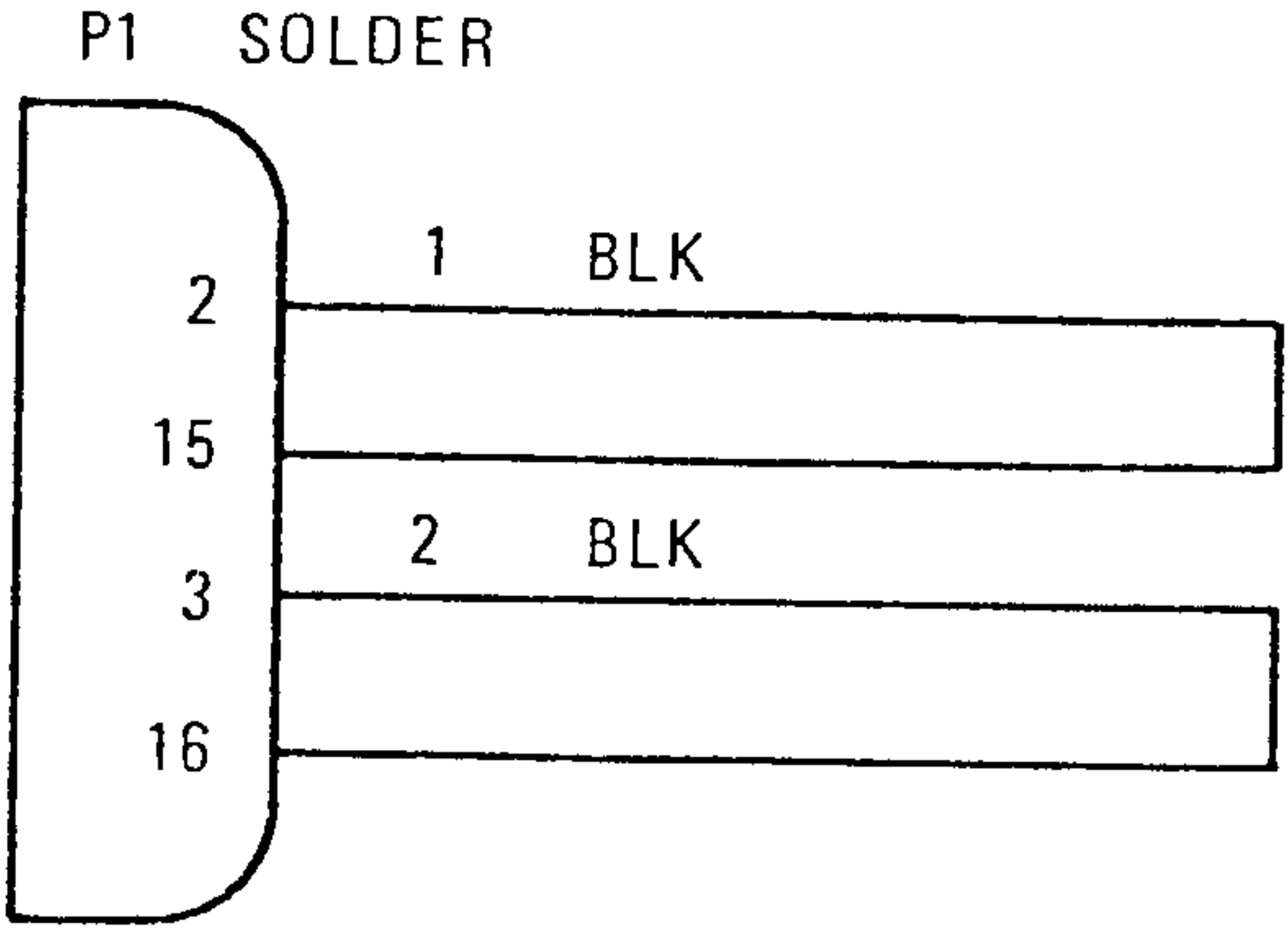
FO-13. Wiring Diagram W13 (J15-P1/P2)



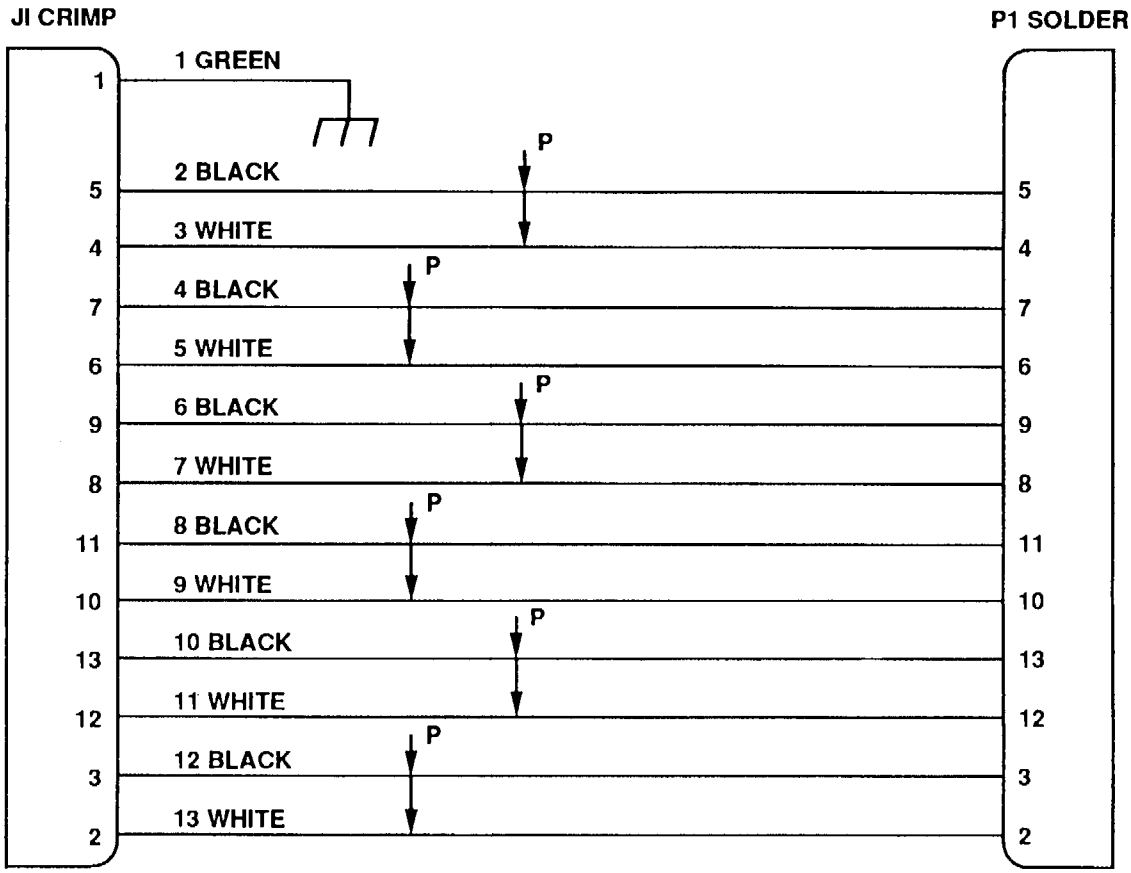
FO-14. Wiring Diagram, Cable Assembly W14 (J16-P1)



FO-15. Wiring Diagram, Cable Assembly W15 (J17-P1)



FO-16. Wiring Diagram (P1-Jumper)



FO-17. Wiring Diagram, Cable Assembly W25 (J1-P1)

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