TECHNICAL MANUAL

GENERAL SUPPORT MAINTENANCE MANUAL

FOR

COUNTER, ELECTRONIC DIGITAL READOUT

AN/USM-459A

(NSN 6625-01-271-3012) (EIC: QVH)

HEADQUARTERS, DEPARTMENT OF THE ARMY
15 FEBRUARY 1990

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1 DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

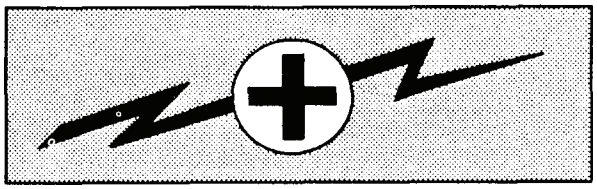
2 IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

3 IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL

4 SEND FOR HELP AS SOON AS POSSIBLE

5 AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

WARNING



HIGH VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technicians are aided by operators, they must be warned about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

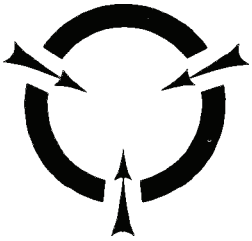
Be careful not to contact high-voltage connections or 115-Volt or 220-Volt ac input connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through the body.

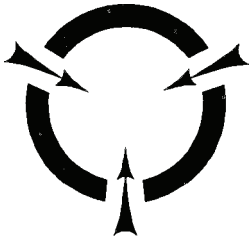
WARNING

Do not be misled by the terms "LOW VOLTAGE." Potentials as low as 50 Volts can cause death under certain conditions.

For first aid, refer to FM 4-25.11.



CAUTION



THIS EQUIPMENT CONTAINS PARTS AND ASSEMBLIES SENSITIVE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD). USE ESD PRECAUTIONARY PROCEDURES WHEN TOUCHING, REMOVING OR INSERTING PRINTED CIRCUIT BOARDS.

ESD
CLASS 1

NOTE

The symbol for static sensitive devices in military inventory is as depicted in the caution block above.

GENERAL HANDLING PROCEDURES FOR ESDS ITEMS

- USE WRIST GROUND STRAPS OR MANUAL GROUNDING PROCEDURES
- KEEP ESDS ITEMS IN PROTECTIVE COVERING WHEN NOT IN USE
- Ž GROUND ALL ELECTRICAL TOOLS AND IN TEST EQUIPMENT
- PERIODICALLY CHECK CONTINUITY AND RESISTANCE OF GROUNDING SYSTEM
- USE ONLY METALIZED SOLDER SUCKERS
- HANDLE ESDS ITEMS ONLY PROTECTED AREAS

MANUAL GROUNDING PROCEDURES

- MAKE CERTAIN EQUIPMENT IS POWERED DOWN
- TOUCH GROUND PRIOR TO REMOVING ESDS ITEMS
- Ž TOUCH PACKAGE OF REPLACEMENT ESDS ITEM TO GROUND BEFORE OPENING
- Ž TOUCH GROUND PRIOR TO INSERTING REPLACEMENT ESDS ITEMS

ESD PROTECTIVE PACKAGING AND LABELING

- INTIMATE COVERING OF ANTISTATIC MATERIAL WITH AN OUTER WRAP OF EITHER TYPE 1 ALUMINIZED MATERIAL OR CONDUCTIVE PLASTIC FILM OR HYBRID LAMINATED BAGS HAVING AN INTERIOR OF ANTISTATIC MATERIAL WITH AN OUTER METALIZED LAYER
- LABEL WITH SENSITIVE ELECTRONIC SYMBOL AND CAUTION NOTE

CAUTION

Devices such as CMOS, NMOS, MNOS, VMOS, HMOS, thin-film resistors PMOS, and MOSFET, used in many equipments, can be damaged by static voltages present in most repair facilities. Most of the components contain internal gate protection circuits that are partially effective, but sound maintenance practice and the cost of equipment failure in time and money dictate careful handling of all electrostatic sensitive components.

The following precautions should be observed when handling all electrostatic sensitive components and units containing such components:

CAUTION

Failure to observe all of these precautions can cause permanent damage to the electrostatic sensitive device. This damage can cause the device to fail immediately or at a later date when exposed to an adverse environment.

STEP 1 Turn off and/or disconnect all power and signal source and loads used with the unit.

STEP 2 Place the unit on grounded conductive work surfaces.

STEP 3 Ground the repair operator using a conductive wrist strap or other device using a 1-M series resistor to protect the operator.

STEP 4 Ground any tools (including soldering equipment) that will contact the unit. Contact with the operator's hand provides a sufficient ground for tools that are otherwise electrically isolated.

STEP 5 All electrostatic sensitive replacement components are shipped in conductive foam or tubes and must be stored in the original shipping container until installed.

STEP 6 When these devices and assemblies are removed from the unit, they should be placed on the conductive work surface or in conductive containers.

STEP 7 When not being worked on, wrap disconnected circuit boards in aluminum foil or in plastic bags that have been coated or impregnated with a conductive material.

STEP 8 Do not handle these devices unnecessarily or remove from their packages until actually used or tested.

CHANGE
NO. 1

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, D.C., 21 July 2006

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FOR

COUNTER, ELECTRONIC DIGITAL READOUT AN/USM-459A (NSN 6625-01-271-3012) (EIC: QVH)

HAZARDOUS MATERIAL INFORMATION – This document has been reviewed for the presence of solvents containing hazardous materials as defined by the EPCRA 302 and 313 lists by the AMCOM G-4 (Logistics) Environmental Division. As of the base document, dated 15 February 1990, all references to solvents containing hazardous materials have been removed from this document by substitution with non-hazardous or less hazardous materials where possible.

OZONE DEPLETING CHEMICAL INFORMATION – This document has been reviewed for the presence of Class I ozone depleting chemicals by the AMCOM G-4 (Logistics) Environmental Division. As of the base document, dated 15 February 1990, all references to Class I ozone depleting chemicals have been removed from this document by substitution with chemicals that do not cause atmospheric ozone depletion.

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3. Added illustrations are indicated by a vertical bar adjacent to the illustration identification number. Changed illustrations are indicated by a miniature pointing hand adjacent to the updated area and a vertical bar adjacent to the illustration identification number.

Remove Pages	Insert Pages
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None	A/(B Blank)
i and ii	i and ii

TM 11-6625-3232-40
C1

Remove Pages	**Insert Pages**
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DA Forms 2028-2	DA Form 2028
Cover	Cover

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Chief of Staff

Official:

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Date of issue for original and changed pages are:

Original	0	15 February 1990
Change	1	21 July 2006

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Page No.	* Change No.
Cover	1
a through d	1
A	1
B Blank	1
i and ii	1
iii and 1-0	1
1-1 and 1-2	1
1-3 through 1-31	0
1-32 Blank	0
2-1 through 2-3	1
2-4 through 2-48	0
A-1	1
A-2 Blank	1
B-1	1
B-2 Blank	1
Index-1 through Index-6	0
Glossary-1	0
Glossary-2 Blank	0
FO-1	0
FO-2 (SH. 1 of 3)	0
FO-2 (SH. 2 of 3)	0
FO-2 (SH. 3 of 3)	0
FO-3	0
FO-4	0
FO-5	0
FO-6	0

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TECHNICAL MANUAL
No. 11-6625-3232-40

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, D.C., 15 February 1990

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REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter or DA Form 2028 (Recommended Changes to Publications and Blank Forms) directly to: Commander, U. S. Army Aviation and Missile Command, AMSAM-MMC-MA-NP, Redstone Arsenal, AL 35898-5000. A reply will be furnished to you. You may also provide DA Form 2028 information to AMCOM via email, fax or the World Wide Web. Our fax number is: DSN 788-6546 or Commercial 256-842-6546. Our email address is: 2028@redstone.army.mil. Instructions for sending an electronic 2028 may be found at the back of this manual immediately preceding the hardcopy 2028. For the World Wide Web use: https://amcom2028.redstone.army.mil.

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TABLE OF CONTENTS

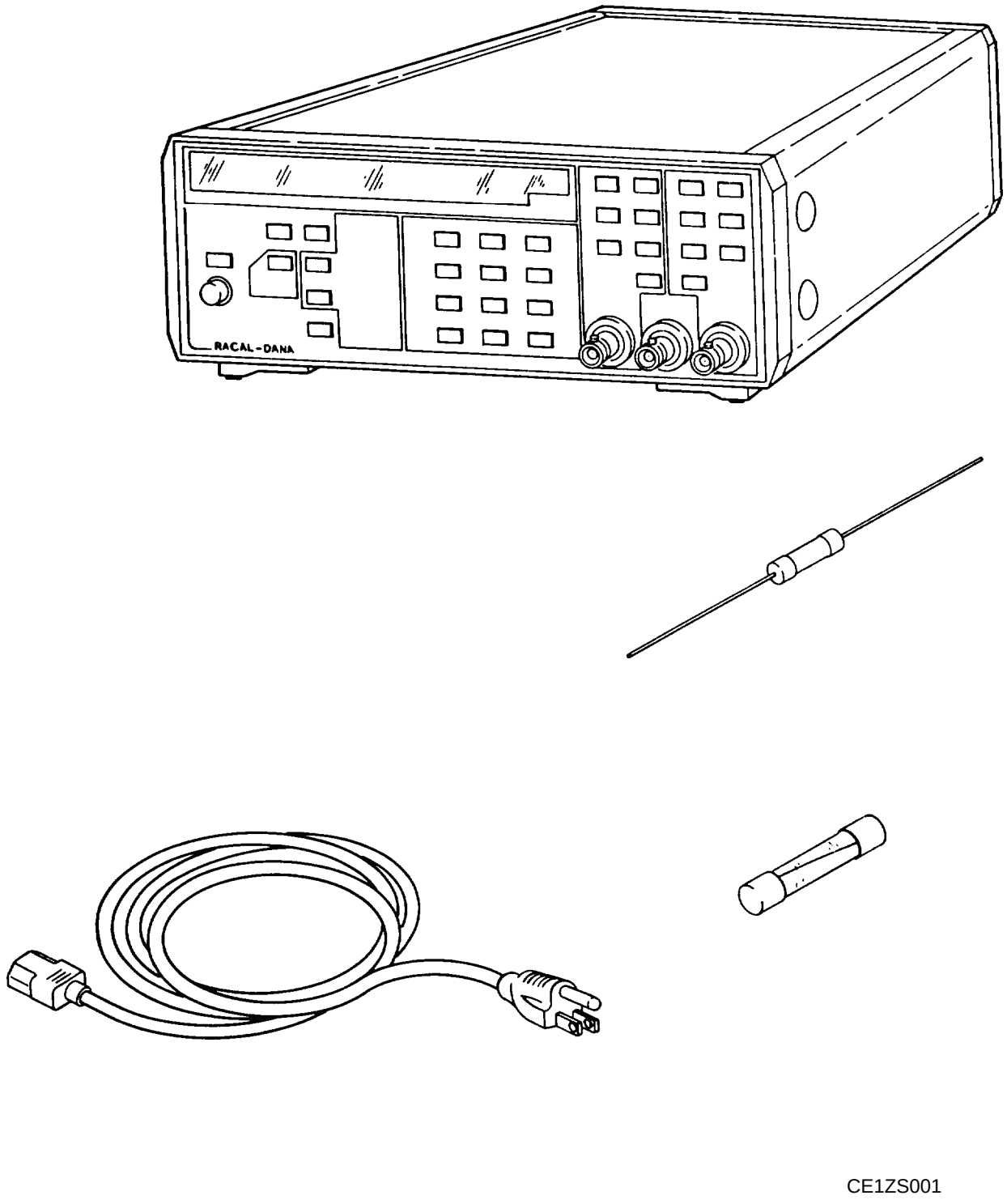
HOW TO USE THIS MANUAL

This manual tells about the Digital Electronic Counter AN/USM-459A and contains instructions about how to use it during maintenance on other electronic equipment.

The technical manual for the electronic equipment being maintained will tell where to make certain connections and when to use various accessories which are part of the AN/USM-459A.

When first receiving the AN/USM-459A, start at the front of the manual and go all the way through to the back. Become familiar with every part of the manual and the AN/USM-459A.

This manual has an edge index which will help find specific information in a hurry. Simply spread the pages on the right edge of the manual until the printed blocks can be seen. Open the manual where the block on the edge of the page lines up with the selected topic printed on the front cover block.



CE1ZS001

Figure 1-1. Digital Electronic Counter AN/USM-459A.

CHAPTER 1
INTRODUCTION

Section 1. GENERAL INFORMATION

1-1. SCOPE.

a. Type of Manual: Intermediate General Support Maintenance Manual.

b. Equipment Name and Model Number: Digital Electronic Counter AN/USM-459A.

c. Purpose of Equipment: The Counter is designed to provide measurement functions including frequency, period, time interval, totalize, phase, and ratio.

1-2. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS.

Refer to the latest issue of DA Pam 25-30 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

1-3. MAINTENANCE FORMS, RECORDS, AND REPORTS.

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 750-8 as contained in The Army Maintenance Management System (TAMMS) Users Manual.

b. Report of Item and Packaging Deficiencies. Fill out and forward SF 364 (Report of Discrepancy) (ROD) as prescribed in AR735-11-2/DLAI 4140.55/SECNAVIST4355.18A/ AFJMAN 23-215.

c. Transportation Discrepancy Report (TDR)(SF 361). Fill out and forward Transportation Discrepancy Report (TDR)(SF 361) as prescribed in DA Pam 25-30.

1-4. DESTRUCTION OF ARMY ELECTRONICS MATERIEL TO PREVENT ENEMY USE.

Destruction of Army materiel to prevent enemy use is described in TM 750-244-2.

1-5. NOMENCLATURE CROSS-REFERENCE LIST.

Common names will be used when the Digital Electronic Counter AN/USM-459A is mentioned in this manual.

NOTE

Official nomenclature must be used when filling out report forms or looking up technical manuals.

Common Name	Official Nomenclature
Counter	Counter, Electronic Digital Readout AN/USM-459A
Digital Electronic Counter	Counter, Electronic Digital Readout AN/USM-459A
AN/USM-459A	Counter, Electronic Digital Readout AN/USM-459A

1-6. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR).

If your Digital Electronic Counter AN/USM-459A needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design or performance. Put it on an SF 368 (Product Quality Deficiency Report). Mail it to us at: Commander, US Army Aviation and Missile Command, AMSAM-MMC-MA-NM, Redstone Arsenal, AL. 35898-5000. We'll send you a reply.

1-7. WARRANTY INFORMATION.

The Counter is warranted by Racal-Dana for one year. Warranty starts on the date of shipment to the original buyer. Report all defects in material or workmanship to your supervisor who will take appropriate action.

Section II. EQUIPMENT DESCRIPTION

1-8. EQUIPMENT CHARACTERISTICS, CAPABILITIES, AND FEATURES.

a. CHARACTERISTICS.

- Allows for:

  Frequency measurements.
  Period measurements.
  Time interval measurements.
  Totalized measurements.
  Phase measurements.
  Ratio measurements.
  Amplitude measurements.

- Designed for bench top use.

b. CAPABILITIES AND FEATURES.

- Fused input for instrument protection (C only).
- Pushbutton control allows for easy operation of equipment.
- LED indicators on front panel for constant equipment status.
- Nine digit LED for information display.
- One digit LED for exponent display.
- Self check confirms operational status.
- Error codes define incorrect operating procedures and circuit failures.
- Programmed interface for remote operation.

1-9. EQUIPMENT DATA.

WEIGHTS AND DIMENSIONS

Counter:

Weight	8lbs (3.63 kg)
Length	13.03 in. (331 mm)
Width	8.35 in. (212 mm)
Height	3.46 in. (88 mm)

POWER REQUIREMENTS

Voltage:

100Vac operation	90 to 110Vac
120Vac operation	103 to 127Vac
220Vac operation	193 to 237Vac
240Vac operation	207 to 253Vac

Frequency	45 to 450Hz
Power	35 VA maximum

Fuse Rating:

100/120Vac operation	0.50 amp, 250 volt
220/240Vac operation	0.25 amp, 250 volt

ENVIRONMENTAL

Operating temperature range	0 to +50° c
Storage temperature range	– 40 to +70° C

Relative humidity:

30°c	95% maximum
40°c	75% maximum
50°c	45% maximum

Operating altitude	0 to 3,050 meters
Storage altitude	0 to 12,000 meters
Vibration	2 g
Shock	30 g

PERFORMANCE

Frequency:

Input A:

DC-coupled:	DC to 160 MHz
AC-coupled:	10 Hz to 160 MHz

Input B:

DC-coupled: . . . . . DC to 100 MHz
AC-coupled: . . . . . 10 Hz to 100 MHz

Input C: . . . . . 40 MHz to 1.3 GHz

Sensitivity:

Sine Wave:

Input A:

DC to 100 MHz . . . . . 25 mVrms
100 to 160 MHz . . . . . 50 mvrms

Input B: . . . . . 25 mvrms

Input C:

40 MHz to 1 GHz . . . . . <15 mvrms
1 to 1.3 GHz . . . . . <75 mVrms

Pulse (inputs A and B, 5 ns min width): . . . . . 75 mVp-p

Dynamic Range:

input A (x1 attenuation):

DC to 50 MHz . . . . . 75 mV to 5 Vp-p
50 to 100 MHz . . . . . 75 mV to 2.5 Vp-p
100 to 160 MHz . . . . . 150 mV to 2.5 Vp-p

Input B (xl attenuation):

DC to 50 MHz . . . . . 75 mV to 5 Vp-p
50 to 100 MHz . . . . . 75 mV to 2.5 VP-P

Input C:

40 MHz to 1 GHz. . . . . .
1 to 1. 3GHz. . . . . 75 mV rms to5Vrms

Signal Operating Range (inputs A and B):

xl attenuation: . . . . . ± 5.1V
x10 attenuation: . . . . . ±51V

Input Impedance:

inputs A and B (nominal, x1 and x10 attenuation):

Separate Mode: . . . . . 50 Ω or 1 M Ω//< 45pF
Common Mode: . . . . . 50 Ω or 1 M Ω//< 55pF

input C (nominal, AC-coupled): . . . . . 50 Ω

Maximum Input:

Inputs A and B (without damage):

50 Ω: . . . . . 5V (DC+ AC rms)

1 M Ω (x1 attenuation):

DC to 2 kHz: . . . . . 260V (DC + AC rms)
>2 kHz . . . . . Decreasing to 5 Vrms, 100 kHz and above

1 M Ω (x10 attenuation):

DC to 20 kHz: . . . . . 260V (DC+ AC rms)
>20 kHz . . . . . Decreasing to 50 Vrms, at 100 kHz and above

Input C (fuse protected):

Without damage: . . . . . 7 Vrms
Damage level . . . . . 2.5 W

Coupling (inputs A and B): ..... AC or DC

Low Pass Filter ((inputs A and B, A selectable): ..... 50 kHz nominal

Trigger Slope (inputs A and B): ..... ⌐ or ¬

Attenuator (inputs A and B): ..... x1 or x10

Trigger Level Range (inputs A and B):

Manual:

X1 attenuation: ..... ±5.1V in 20 mv steps
X10 attenuation: ..... ±51V in 200 mv steps

Automatic: ..... ± 51V

Trigger Level Accuracy (inputs A and B):

x1 attenuation: ..... ±30 mV± 1% of trigger level reading
X10 attenuation ..... ±300 mV± 1% of trigger level reading

Auto Trigger (inputs A and B):

Frequency Range: ..... DC and 50 Hz to 100 MHz
Min. Amplitude (AC): ..... Typical 150 mV p-p (5ns width)
x10 attenuator: ..... Auto select if input signal exceeds ±5.1V or 5.1V p-p (5 ns width)

VSWR (input Cat 1 GHz): ..... <2.1:1

Internal Time base:

Frequency: ..... 10 MHz
Aging: ..... <1 x 10^{-9} per day (after 48 hours of operation)

Stability:

Temperature (0 to +50° C): ..... <7 x 10^{-9}
Line Voltage (2 minutes after 10% line voltage change): ..... <5 X 10^{-10}

Gate Time:

Range: ..... 1 ms to 10 sec

Time (frequency, period, and ratio modes):

9 + overflow resolution: ..... 10 sec
9resolution: ..... 1 sec
8 resolution: ..... 0,1 sec
7 resolution: ..... 0,01 sec
6,5,4,3 resolution: ..... 0.001 sec

Trigger Level Outputs (rear panel):

Range ..... ±5.1V

Accuracy (relative to true trigger level):

x1 attenuation: ..... ±1% V output ± 10 mV
X10 attenuation: ..... ± 1% V output ±100 mV

Impedance: ..... l0k Ω nominal

Frequency Standard Output (rear panel):

Frequency: ..... 10 MHz
Amplitude: ..... >600 mV p-p into 50 Ω
Impedance: ..... 250 Ω nominal

External Standard Input (rear panel):

Frequency: ..... 10 MHz
Signal Amplitude (sine wave): ..... 100 mV rms to 10V rms

Impedance:

1V$_{P-P}$ ..... 1 k Ω nominal
10V$_{P-P}$ ..... 500 Ω nominal

Digital Interface (rear panel):

Control Capability: ..... All functions and controls except power on/off and standby charge output : ..... Engineering format (11 digits and exponent)
IEEE-STD-488-1978 subsets: SH1, AH1, T5, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, C0, E2
Handshake Time: ..... 250µs to 1 ms/character dependent on message content
Read Rate: ..... Typically 20/s dependent upon measurement function

MEASUREMENT MODES

Frequency A:

Range: ..... DC to 160 MHz
Digits Displayed: ..... 3 t0 9 digits plus overflow
LSD* Displayed (Hz): ..... Fx 10^{-D} (D= No. of digits, F= Frequency rounded up to next decade)
Resolution (Hz-rms value): ..... ± LSD ± (Trigger Error* x Frequency) + Gate Time
Accuracy (Hz-rms value): ..... ± Resolution ± (Timebase Error x Frequency)

Frequency C:

Range: ..... 40 MHz to 1.3 GHz
Digits Displayed: ..... 3 to 9 digits plus overflow
LSD Displayed (Hz): ..... Fx 10^{-D} (D= No. of digits, F= Frequency rounded up to next decade)
Resolution (Hz-rms value): ..... ± LSD ± (Trigger Error x Frequency) + Gate Time
Accuracy (Hz-rms value): ..... ± Resolution ± (Timebase Error x Frequency)

Period A:

Range: ..... 6.25 ns to 1.7x 10^{3} sec
Digits Displayed: ..... 3 to 9 digits plus overflow
LSD Displayed (see): ..... P x 10^{-D} (D = No. of digits, P= Period rounded up to next decade)

Resolution (see-rms value):

3-5 digits ..... ± LSD ± (Trigger Error x Period) + Gate Time
6-9 digits ..... ± 2LSD ± (Trigger Error x Period)+ Gate Time

Accuracy (see-rms value): ..... ± Resolution ± (Timebase Error x Period)

Time Interval (TI A->B):

Range:

Separate Mode: ..... 0 to 8 x 10^{5} sec
Common Mode: ..... 5 ns to 8x 10^{5} sec

Input:

Separate Mode: ..... Input A START and B STOP
Common Mode: ..... Input A START and STOP

Trigger Slopes: ..... ⎍ or ⎍ selectable START and STOP
LSD Displayed: ..... 1 ns min
Resolution (see-rms value): ..... ±LSD ± 1 ns ± Trigger Error
Accuracy (see-rms value): ..... ± Resolution ± (Time base Error x T1)
± Trigger Level Timing Error* ± 2 ns

● See glossary for additional information.

Total A by B:

Input: ..... Input A
Range: ..... 1.0^{12}-1 (9 most significant digits displayed)
Maximum Rate: ..... 1.0^{8} events/s
Minimum Pulse Width: ..... 5 ns at trigger points
Accuracy: ..... ± 1 count
Start/Stop: ..... Electrical (Input B) or Manual

Phase A rel B:

Range: ..... 0.1° t0 360°

LSD Displayed:

1 MHz ..... 0.1°
10 MHz ..... 1.0°
100 MHz ..... 10°

Resolution (degrees-rms value): ..... ±LSD± (Tl Resolution/Period A)x 360°
Accuracy (degrees-rms value): ..... ±LSD± (Tl Accuracy/Period A)x 360°

Ratio A/B

Range:

Input A: ..... DC to 100 MHz
Input B: ..... DC to100 MHz

LSD Displayed (for 6-9 digits selected): ..... 10+ (FREQ B x Gate Time) (rounded to nearest decade)
Resolution (rms value): ..... +LSD*(TriggererrorB/GateTime)x Ratio
Accuracy (rms value): ..... * Resolution

Ratio C/B:

Range:

Input C: ..... 40 MHz to 1.3GHz
Input B: ..... DC to 100 MHz

LSD Displayed (for 6-9 digits selected): ..... 640+(FREQBx Gate Time) (rounded to nearest decade)
Resolution (rms value): ..... ±LSD± (Trigger error B/ Gate Time)x Ratio
Accuracy (rms value): ..... ± Resolution

SPECIAL FUNCTIONS

Time Delay (Tl A–>Band Total A by B measurements only):

Range: ..... 200 µs to 800 ms nominal
Step Size: ..... 25µs nominal
Accuracy: ..... ±0.l% of reading ±50µs

Math (all measurements except Phase A rel B):

Function: ..... (Result -X)/Z
Entry Range: ..... * 1 x 10^{-10} to± 1 x 10^{10} to 9 significant figures

External Arming (all measurements except Phase A rel B):

Input Signal (rear panel): ..... TTL compatible (min. pulse width 200 ns)
Slope: ..... ⎍ or ⎏ independently selectable on START or STOP arm
Impedance: ..... 1 k Ω nominal

Amplitude Measurement

Peak (5 ns signal width):

Frequency Range: ..... 50 Hz to 20 MHz
Amplitude Range: ..... 160 mVp-p to 51 Vp-p

Resolution:

xl attenuation: . . . . . 20 mV
x10 attenuation: ..... 200 mV

Accuracy:

x1 attenuatio n: . . . . . ±50 mV + 6% V p-p
x10 attenuation: . . . . . *500 mV ± 10% Vp-p

DC(<15 mV p-p AC):

Amplitude Range: ..... ±51V

Resolution:

x1 attenuation: . . . . . 20 mV
x10 attenuation: . . . . . 200 mV

Accuracy:

x1 attenuation: . . . . . ±40 mV± 1% reading
x10 attenuation: .. . . . . ±400 mV± 1% reading

1-10. SAFETY, CARE, AND HANDLING.

Observe all WARNINGS, CAUTIONS, and NOTES in this manual. This equipment can be extremely dangerous if these instructions are not followed,

Section III. PRINCIPLES OF OPERATION

1-11. GENERAL FUNCTIONAL DESCRIPTION.

The Counter measures frequency from DC to 1.3 GHz using one of three input connectors. In addition to frequency, the period of a waveform, time interval between two events, total events occurring on one input, phase difference between two signals, frequency ratio of two signals, and peak amplitude of a signal can be measured and displayed.

Input signal information, entry information, and error messages are shown in the display. Various LED indicators provide additional instrument status.

AN/ USM-459A simplified block diagram is shown on figure 2-1. AN/USM-459A detailed block diagram is shown on figure FO-1.

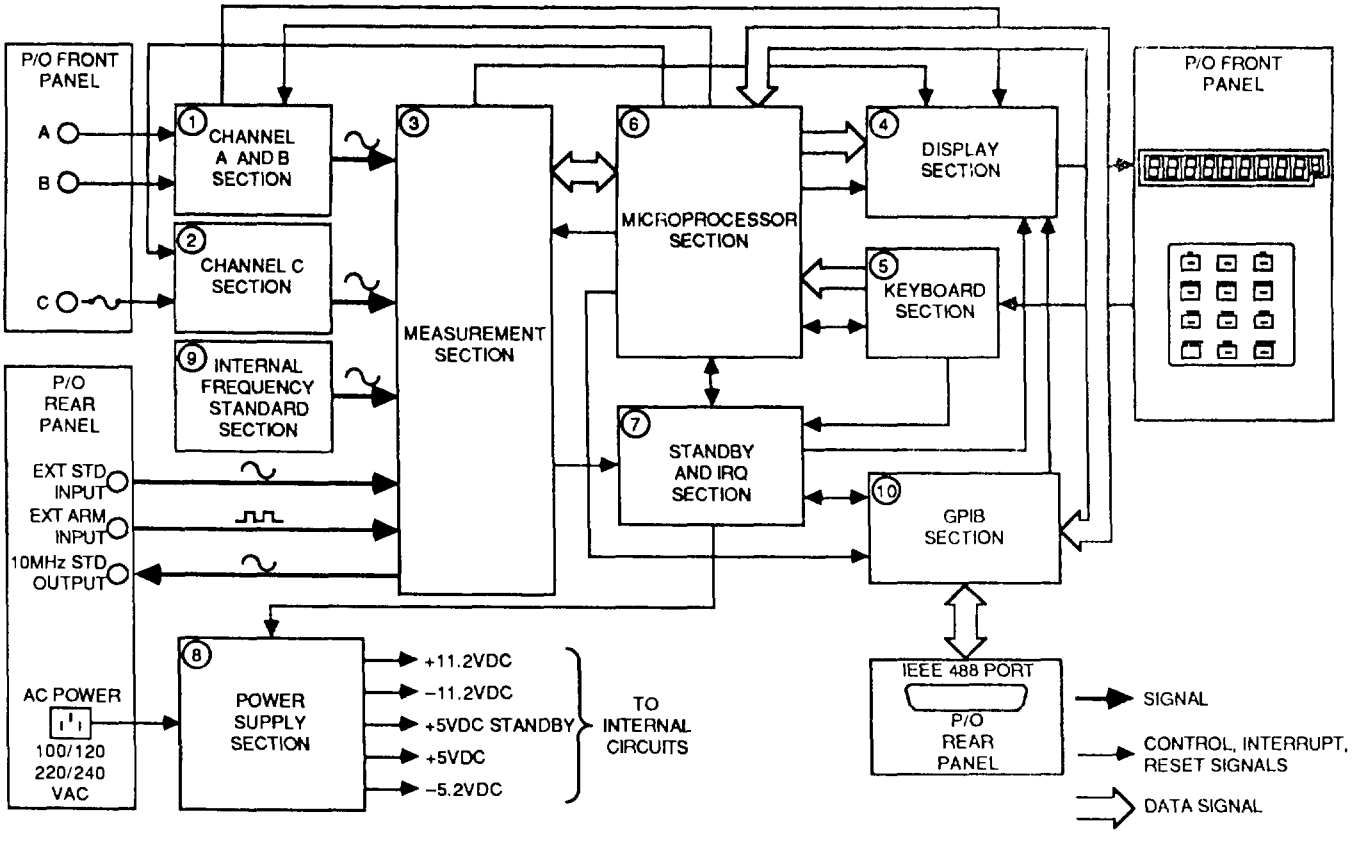


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Figure 1-2. Digital Electronic Counter AN/ USM-459A Simplified Block Diagram.

(1) The Channel A/B section processes input signals connected to front panel INPUT A and INPUT B connectors. Selection of 50 Ω or 1M Ω input impedance, AC or DC coupling, and x1 or x10 attenuation is provided. In addition, channel A input signal can be routed to both channel A and B outputs. If selected, filtering for channel A can be provided. Control signals from Microprocessor section control trigger levels for each channel along with selection of impedance, coupling, attenuation, routing, and filtering. Conditioned input signals are then sent to the Measurement section.

(2) The Channel C section processes the input signal connected to front panel INPUT C connector. Input protection is provided both by a front panel fuse, and signal limiting circuitry, The input signal amplitude is adjusted and then sampled to verify the level is adequate for measurement. Control signals from the Microprocessor section allow the conditioned input signal to be applied to the Measurement section.

(3) The Measurement section performs actual measurements of input signals provided by the Channel A/B or Channel C sections under control of the Microprocessor section according to the instructions from the Keyboard section or GPIB section. At the end of each measurement, an interrupt signal is sent to the Standby and IRQ section, and measured value data is sent to the Microprocessor section. A 10 MHz reference signal is required, and is provided by either the Internal Frequency Standard section or an external Frequency Standard connected to the rear panel EXT STD INPUT connector. A 10 MHz output, provided from the frequency standard in use, is made available at the rear panel 10 MHz STD OUTPUT connector. The rear panel EXT ARM INPUT connector provides the ability to externally start/stop the measurement cycle.

(4) The Display section provides measurement information and instrument status to the operator. The REM, ADDR, and SRQ LEDs are controlled by the GPIB section. The GATE LED is controlled by the Measurement section. The channel A and B TRIGGER LEDs are controlled by the Channel A/B section. The STANDBY LED is controlled by the Standby and IRQ section, All other front panel LEDs and digit display information are controlled by the Microprocessor section.

(5) The Keyboard section allows the operator to communicate with the Counter. When one of the 33 front panel keys is pressed (excluding STBY/CHRG), an interrupt signal is sent to the Standby and IRQ section and, the data is sent to the Microprocessor section. When the STBY/CHRG key is pressed, a control signal is sent to the Power Supply section via the Standby and IRQ section.

(6) Microprocessor section provides overall control of the internal circuitry in the Counter, including math functions. Data and control signals are sent to/received from the Channel A/B, Channel C, Measurement, Display, Keyboard, Standby and IRQ, and GPIB sections as required to perform all Counter operations.

(7) The Standby and IRQ section generates reset signals for the Microprocessor and GPIB sections, and also combines the interrupt signals from the GPIB, Measurement, and Keyboard section to the Microprocessor section. In addition, a control signal is sent to the Power Supply section to turn off all internal voltages except the +5 Vdc STANDBY.

(8) The Power Supply section provides the internal operating voltages for the Counter. Fuse protection is provided on the rear panel. During normal operation, regulated +11.2 Vdc, –11.2 Vdc, +5.0 Vdc, -5.2 Vdc are provided to all the sections for operation. When the Counter is in STBY/CHRG mode, regulated +5.0 Vdc is provided to the Internal Frequency Standard section to keep the oscillator operating, and to the Microprocessor section to keep the memory from erasing.

(9) The Internal Frequency Standard section provides a very stable 10 MHz signal used by the Counter. This signal is provided to the Measurement section for use as a frequency reference. The Oscillator used to generate the reference signal is operating when the Counter is in the ON or STBY/CHRG mode.

(10) The GPIB section allows the Counter to be operated remotely using an external controller connected to the rear panel IEEE 488 PORT connector. All functions except POWER ON/OFF and STBY/CHRG are programmable using the interface.

1-12. DETAILED FUNCTIONAL DESCRIPTION (fig. FO-2 thru FO-6).

(1) CHANNEL A/B (fig. 1-3). This section is responsible for processing input signals connected to front panel INPUT A and INPUT B connectors. This section is contained on the following circuit card assembly:

- A1 Motherboard Circuit Card Assembly (fig. FO-2, sheets 1 and 3).

The Channel A/B Section can be divided into the following major circuits:

- Impedance Selection Circuits (A and B).
- AC/DC Coupling Circuits (A and B).
- Attenuator Select Circuits (A and B).
- Common A Select Circuit.
- High Frequency Channel Buffer Circuits (A and B).
- Low Frequency Channel Buffer Circuits (A and B).
- Filter Select Circuit (A only).
- Output Circuits (A and B).

NOTE

Operation for channel A and channel B are similar, except for low-pass filter function (channel A only). Channel A is discussed below.

Impedance Selection Circuit. Selects 50 Ω or 1M Ω input impedance. Relay Al KC, operating under control of the Microprocessor Section, selects impedance for channel A input signal. When energized, input signal impedance at A1 J5 (Input A) is 50 Ω, controlled by resistors A1R78 and R79 in parallel.

AC/DC Coupling Circuit. Selects AC or DC Coupling. Relay A1KA, operating under control of the Microprocessor Section, selects coupling for channel A input signal. When de-energized, AC coupling of the input signal is provided through A1C65, When energized, DC coupling of the input signal is provided. A1R165 limits the current surge which occurs if DC coupling is selected while A1C65 is in the charged state.

Attenuator Select Circuit. Selects xl or x10 attenuation. Relay A1KF, operating under control of the Microprocessor Section, selects attenuation for channel A input signal, Attenuator is formed by A1R82, R83, R87. With KF de-energized, the attenuator has a series element (R82), and a shunt element (A1R83 and R87 in parallel) providing attenuation of 20 dB (nominal). With A1KF energized A1R82 is short-circuited, providing O dB attenuation. Signal is provided to both the High and Low Frequency Channel Buffer Circuits.

Common A Select Circuit. Provides the input to channel A to be routed to both channel A and channel B amplifier circuits. Relay A1KH, operating under control of the Microprocessor Section, selects the input to channel B amplifier. When energized, the signal connected to input A is routed to both channel A and B.

High Frequency Channel Buffer Circuit. Provides high frequency path for input signal. The Attenuator Circuit output signal is fed to through A1R160 and A1C73 to A1Q15 and A1Q17. A1CR5 protects the gate of A1Q15 against excessive negative voltage swings. The gain from the attenuator output to the emitter of A1Q17 is approximately + 0.94.

Low Frequency Channel Buffer Circuit. Provides low frequency path for input signal. The Attenuator Circuit output signal (from potential divider A1R87) is fed to A1U34 and Q25, The gain from A1R87 pin 1 to the emitter of A1Q25 is approximately + 0.94, Any offset in the system is nulled by adjusting A1R192. Tigger level is provided to A1U34 pin 2 through A1R202 and one section of Al R89.

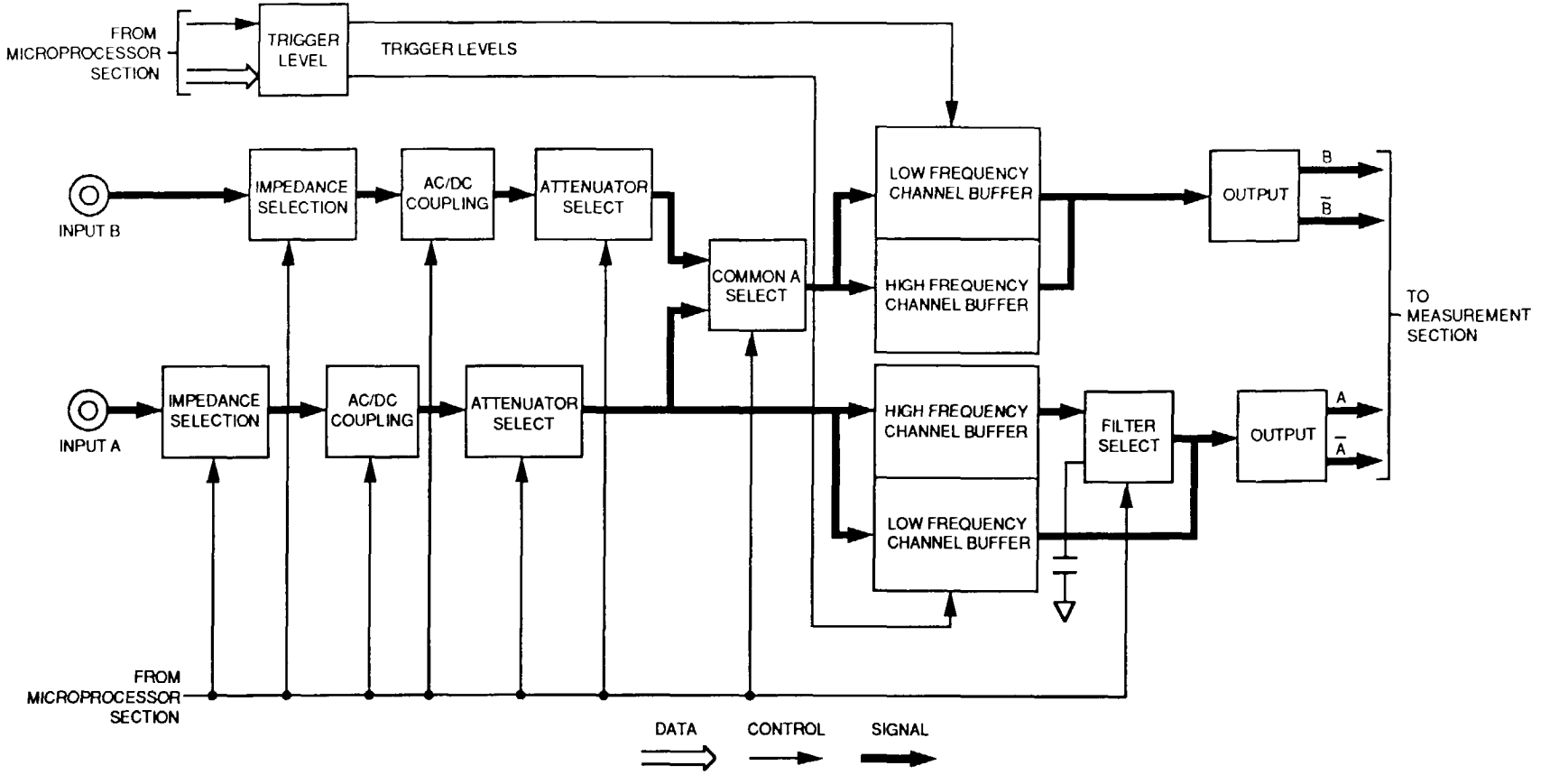

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Figure 1-3. Channel A/B Section Simplified Block Diagram.

Filter Select Circuit. Provides selectable low pass filter. Relay A1KE, operating under control of the Microprocessor Section, controls filter selection for channel A input signal only.

- When A1KE is de-energized (filter not selected), the signals from the High and Low Frequency Channel Buffer circuits are combined at the base of A1Q21 by the network A1C79 and A1R107. This acts as a low-pass filter to the output of the Low Frequency Buffer Circuit, and as a high-pass filter to the output of the High Frequency Buffer Circuit. The crossover frequency is 5 kHz.
- When A1KE is energized (filter selected), the High Frequency Channel Buffer output is opened, and A1C87 is connected across the Low Frequency Channel Buffer output, providing 50 kHz nominal bandwidth,

Output Circuit. Provides input signal measurement information to the Measurement Section. The signal at A1Q21 emitter is fed to diode bridge (A1CR18 - CR21) to limit signal swing to approximately ± 1V. This signal is then provided to Schmitt trigger U36a. The differential output of A1U36a forms the input to the Measurement Section. A1R149 adjusts channel A sensitivity by setting the hysteresis of A1U36a.

Trigger Level Circuit. Provides selectable trigger levels to the A and B channels. Tigger levels are set for the two channels independently in the Digital-to-Analog Converter (DAC - A1H2) under control of the Microprocessor Section. Trigger level for channel A is provided to the Low Frequency Channel Buffer Circuit at A1U34 pin 2. Feedback from the emitter of A1Q21 to A1U34 pin 2 is provided by A1R89 pins 5 and 3. This makes R89 pin 3 a virtual ground point, and the gain from the A1R136/R202 junction to the emitter of A1Q21 is - 0.94. This brings the selected trigger point on the input signal to OV at A1Q21 emitter.

For example, a 1 Vdc level at the Channel A input and a 1V trigger level from A1H2, combine to give 0V at A1Q21 emitter.

2 CHANNEL C (fig. 1-4). This section is responsible for processing input signals connected to front panel lNPUTC connector. This section is contained on the following circuit card assemblies:

- A1 Motherboard Circuit Card Assembly (fig. FO-2, sheet 3).
- A4 Channel C Prescaler Circuit Card Assembly (fig. FO-5).

The Channel C Section can be divided into the following major circuits:

- Signal Limiter Circuit.
- Automatic Gain Control Circuit.
- Amplifier Circuit.
- Prescaler Circuit,
- Low Signal Detector and Comparator Circuit.
- Continuous Signal Latch Circuit.
- Signal Gate Circuit.

Signal Limiter Circuit. Provides additional circuit protection for signal connected to J13 (INPUTC) connector. Initial protection provided by fuse mounted in J13. Input signal amplitude is limited by diode clamp A4CR8 - CR11.

Automatic Gain Control Circuit. Reduces the range of the input signal level routed to the Amplifier Circuit, An attenuator (A4L1/R6/CR2/CR7) controls gain by changing impedance of A4CR2 and CR7. Peak-to-peak detector (A4C48/CR1/CR3/R7) produces a negative voltage proportional to the signal amplitude. A direct current proportional to this voltage causes input signal amplitude to be offset by changes in attenuation.

Amplifier Circuit. Amplifies and shapes the conditioned input signal. The signal passes through four amplifier stages A4Q1 - Q4. Shaping circuit is formed by A4C46/R36/R37). Amplified input signal is routed to the Prescaler Circuit, and Low Signal Detector and Comparator Circuit.

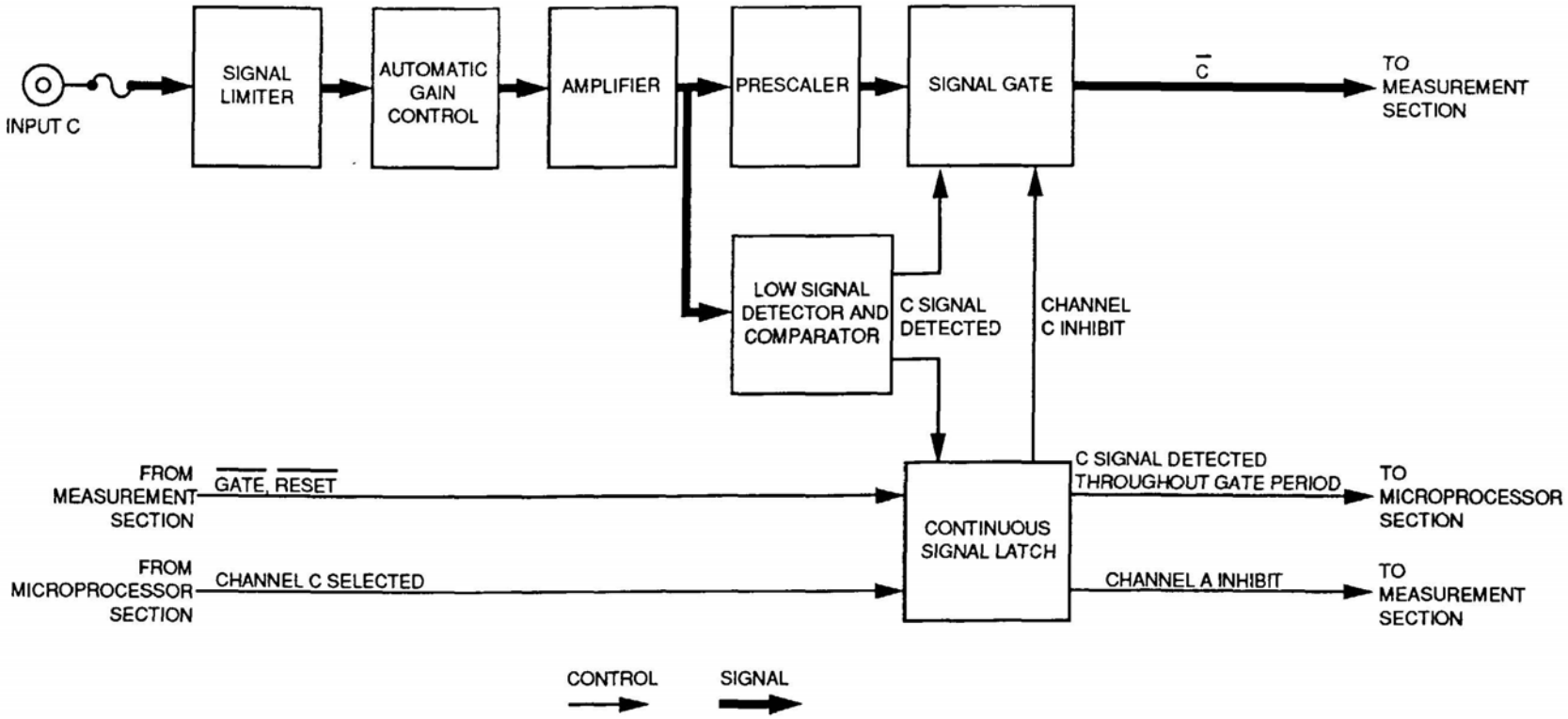

Figure 1-4. Channel C Section Simplified Block Diagram.

Prescaler Circuit. Prescales the conditioned and amplified input signal by 64. Prescaled signal (A4U3) is routed to the Signal Gate Circuit.

Low Signal Detector and Comparator Circuit. Samples the conditioned and amplified input signal to determine if signal amplitude is sufficient for measurement, The signal at the output of the Amplifier Circuit is fed to the low-signal detector (A4C23/CR5). The detector output is compared with the threshold voltage set by adjusting A4R27. The comparator (A4U1b) output is at logic 1 if the detector output is below the threshold (Channel C's signal amplitude too low for accurate counting). The comparator output is at logic O if the detector output is above the threshold (Channel C's signal amplitude sufficient for accurate counting), The output level is routed to the Continuous Signal Latch Circuit. Inverter (A4U1a) inverts the level, and routes it to the Signal Gate Circuit.

Continuous Signal Latch Circuit, Samples the Detector and Comparator Circuit output to determine that, during the entire gate period, the input signal amplitude was sufficient for measurement, The latch (A4U4) is RESET at the beginning of each gate period. The GATE signal is inverted (A4U1C) and compared with the Detector and Comparator Circuit output. If both inputs are at a logic 1, indicating that the Channel C signal level is too low while the gate is open, the Continuous Signal Latch is set. The latch output is supplied to the Microprocessor Section to prevent the result of any measurement made during that gate period from being displayed. To keep the two channels from being enabled at the same time,

When Channel C is selected, a Logic 1 is applied to the latch. This signal is buffered (A4U2C) and routed to the Measurement Section to inhibit Channel A/B.

When Channel C is not selected, a Logic O is applied to the latch. This signal is inverted (A4U4b) and buffered (A4U1d) and routed to the Signal Gate Circuit. This level is used to inhibit the Channel C output.

Signal Gate Circuit. Switches the A4 Channel C Prescaler output signal to on or off. Prescaler Circuit output signal is routed through the Signal Gate Circuit for output to the Measurement Block provided that;

- Amplitude of the input signal is sufficient for measurement.
- Channel C is selected.

NOTE

Part of the Signal Gate Circuit (Low Signal Latch A1U41b) is physically located on the Al Motherboard Circuit Card Assembly (fig. FO-2, sheet 3).

The output gate switches the A4 Channel C Prescaler output signal. Signal can be routed to the Measurement Section or inhibited. The low-signal latch controls the output gate. Inputs to the low-signal latch are as follows:

- Buffered Prescaler Circuit - Clock signal (used for clocking only).
- Low Signal Detector and Comparator Circuit - C Signal Detected level (used for input signal amplitude verification).
- Continuous Signal Latch Circuit - Channel C Inhibit signal (indicates if channel C selected)

A4 Channel C Prescaler output signal is routed to the Measurement Section when the Detector and Comparator Circuit output goes above the threshold and the Continuous Signal Latch Circuit output is logic 0. The low-signal latch (A1U41b) is armed and opens the output gate (A4U2b) on the next signal edge (clock) from the Prescaler Circuit. This enables the Channel C Prescaler to make C input measurements.

A4 Channel C Prescaler output signal is not routed to the Measurement Section when the Detector and Comparator Circuit output goes below the threshold or the Continuous Signal Latch Circuit output is logic 1. The low-signal latch (A1U41b) is set and inhibits the output gate.

(3) MEASUREMENT (fig. 1-5). This section performs the actual measurement of all input signals. This section is contained on the following circuit card assembly:

- A1 Motherboard Circuit Card Assembly (fig. FO-2, sheets 2 and 3).

The Measurement Section can be divided into the following major circuits:

- Multiple Counter and Control 2 (MCC2) Circuit.
- Multiple Counter and Control 1 (MCC1) Circuit.
- Timing Error Correction (TEC) Circuit.
- External Standard Detect Circuit.
- Divide by Two (+2) Circuit.
- internal Frequency Standard Buffer Circuit.
- External Frequency Standard Buffer Circuit.
- External Standard Detect Circuit.
- External Arming Circuit.

Multiple Counter and Control 2 (MCC2) Circuit. Performs actual measurement of Channel A/B and Channel C Section output signals under Microprocessor Section control. Selects internal or external standard, and provides 10 MHz standard output. Circuit described in detail below.

Multiple Counter and Control 1 (MCC1) Circuit. Provides overall control of the section. Generates necessary timing and control signals. Provides Measurement Section output information to the Microprocessor Section, Circuit described in detail below.

Timing Error Correction (TEC) Circuit. Provides increased accuracy by compensating for timing errors. Provides the necessary correction signals to MCC1 and MCC2 Circuits for measurement. Circuit described in detail below,

Divide by Two (+2) Circuit. Scales (by 2) or inhibits the Channel A/B Section output signal from the Measurement Section,

- During FREQ A and PERIOD A functions, the Channel A/B Section input A signal is + 2 and routed to the MCC2 Circuit (A1U39 pin 19).
- During FREQ C and RATIO C/B functions, the + 2 Circuit is disabled (A1U41a pin 5 is logic 1) by CHANNEL A INHIBIT control line (PST1) from the Channel C Section. This sets and holds the +2 Circuit (A1U41a) and the Channel A/B Section output signal is inhibited from reaching the MCC2 Circuit.

Internal Frequency Standard Buffer Circuit Provides input of the Internal Frequency Standard Section signal to the Measurement Section. The 10 MHz Internal Standard signal is shaped and buffered (A1U2) then routed to the MCC2 Circuit (A1U39 pin 2). The inverting inputs of A1U2 are connected to the bias voltage at A1U2 pin 11.

External Frequency Standard Buffer Circuit. Provides input of the External Standard signal to the Measurement Section. Input signal connected to the rear panel EXT. STD INPUT connector. Excessive signal amplitude is corrected (A1CR6/CR7/R32) and routed through buffer (A1U14a,b,c). The inverting inputs are connected to the bias voltage at A1U14 pin 11. The final stage has feedback connected through A1R11 for Schmitt Trigger action. Link LK1 is fitted between pins 8 and 9 of A1P16 to connect the differential output of the final stage to the MCC2 Circuit (A1U39 pin 3),

External Standard Detect Circuit. Informs the Microprocessor Section if a signal, with sufficient amplitude, is connected to the rear panel EXT STD INPUT connector. The signal is detected (A1CR26/C96/R129) and routed to the Microprocessor Section through A1U23 pin 6. If the level is above the TTL logic 1 threshold, the Microprocessor sets the MCC2 Circuit (A1U39 pin 38) to logic 0 and the Measurement Section switches to use the External Standard signal.

External Arming Circuit. The signal connected to the rear panel EXT ARM INPUT connector is amplified (A1Q5) and routed to the MCC1 Circuit (A1U18 pin 27).

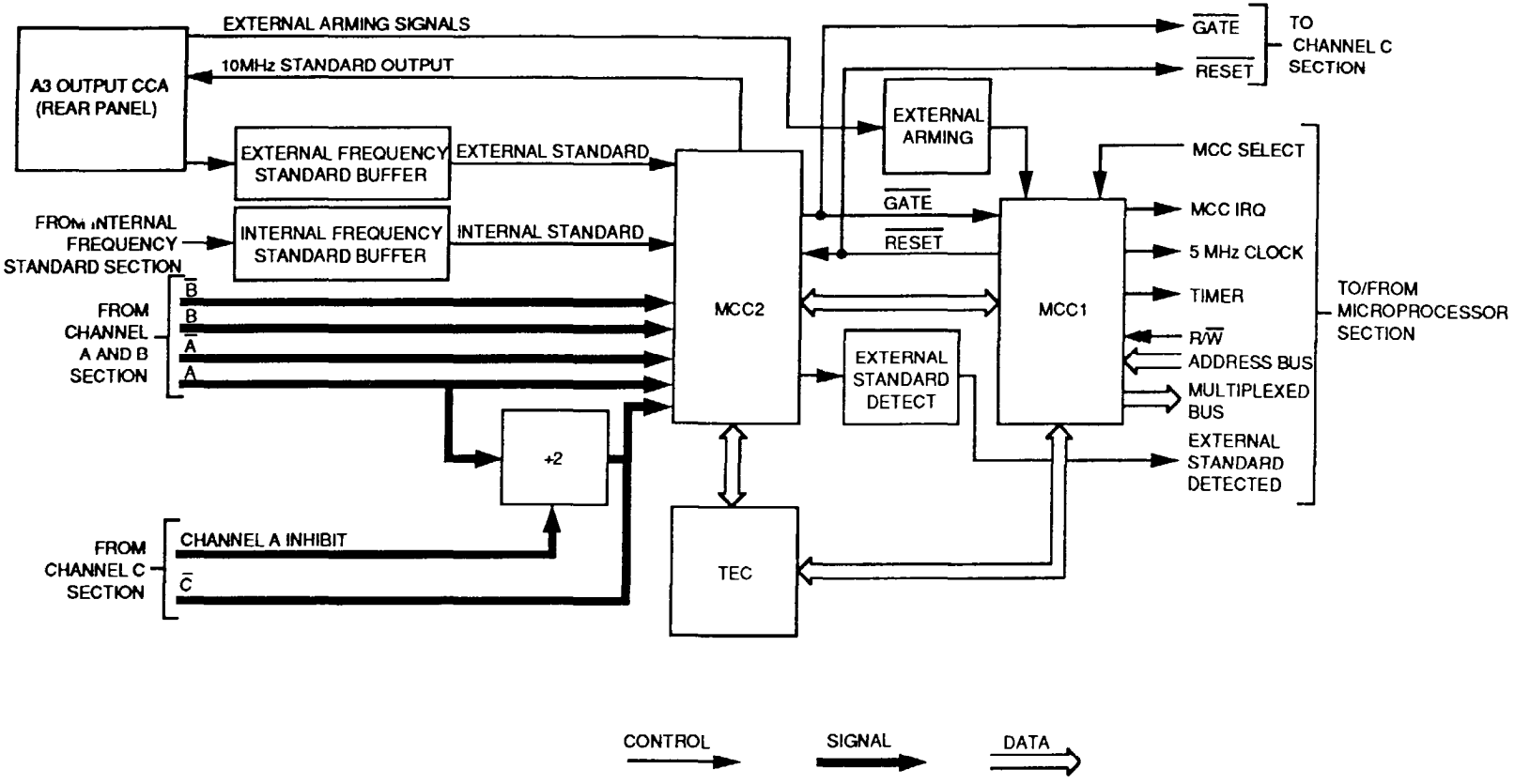

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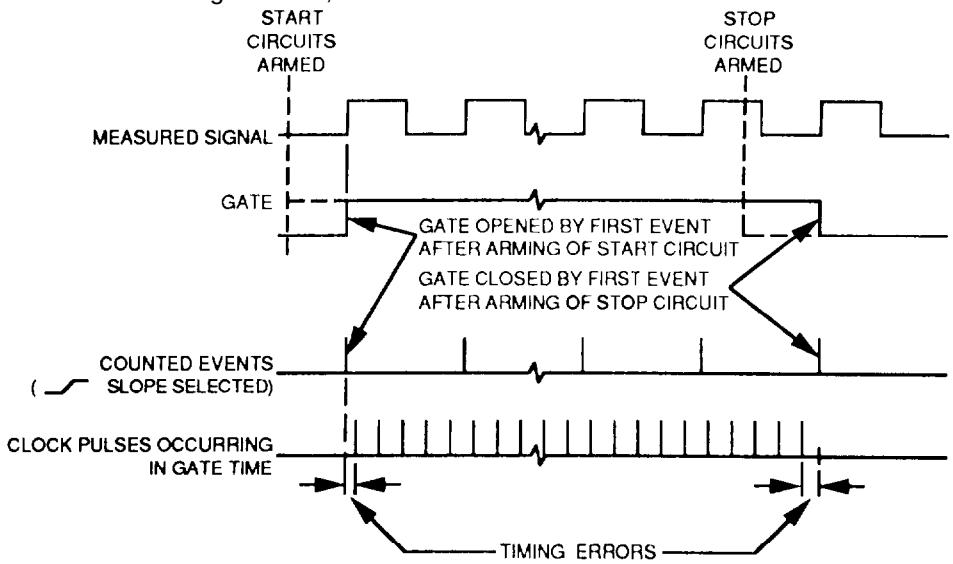
Figure 1-5. Measurement Section Simplified Block Diagram.

Measurement Method:

The recipromatic counting technique is used to measure signals. With this technique the measured signal, not the counter clock pulses, controls the start and stop of the measurement period (gate time) as shown below. The gate time, therefore, extends over an integral number of cycles of the measured waveform. The gate time is measured by counting the clock pulses which occur while the gate is open. This leads to timing errors at both ends of the gate time, as shown.



Signal measurement within the Measurement Section is performed as follows:

- MCC1 (A1U18) and MCC2 (A1U39) Circuits are configured by the Microprocessor Section according to the measurement function selected.

  For all measurement functions except FREQ A and PERIOD A, the differential outputs from Channel A/B Section are routed to MCC2 Circuit at (A1U39 pins 15, 16,17 and 18).

  For the FREQ A and PERIOD A functions, the Channel A/B Section input A signal is + 2 (A1U41a) and routed to the MCC2 Circuit (A1U39 pin 19).

  For the FREQ C and RATIO C/B functions, the C signal is routed to the MCC2 Circuit (A1U39 pin 19). During these functions, the+ 2 Circuit inhibits the Channel A/B Section signal.

- At the end of each measurement period, MCC1 Circuit generates an interrupt request (MCC IRQ) for the Microprocessor Section. The registers within MCC1 are addressed using the address bus and the MCC SELECT line from the Microprocessor Section. The measured value is transferred to the Microprocessor Section using the multiplexed bus.

- The available reference signals used by the MCC2 Circuit for measurement are selected as follows:

  The Internal Standard signal from the Internal Frequency Standard Buffer Circuit is connected to MCC2 Circuit (A1U39 pin 2) Used if an external signal does not have sufficient amplitude, or is not connected, to the rear panel EXT STD INPUT connector.

  The External Standard signal from the External Frequency Standard Buffer Circuit is connected to MCC2 Circuit (A1U39 pin 3) A buffered sample of the External Standard signal (A1U39 pin 24) IS applied to the External Standard Detect Circuit. This notifies the Microprocessor Section that an external standard input of sufficient amplitude is connected.

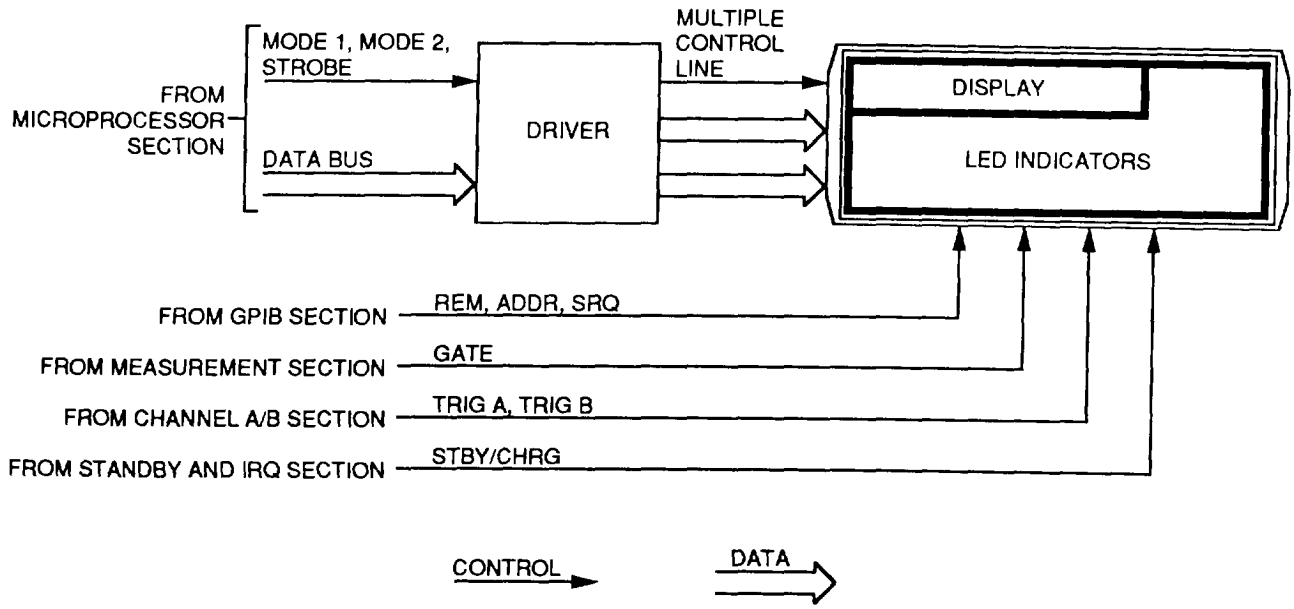
- A 10 MHz signal, derived from the standard selected, is routed from the MCC2 Circuit (A1U39 pin 37) to the rear panel 10 MHz STD OUTPUT connector.

Additional signals from the MCC1 Circuit (A1U18) include:

- A 5 MHz CLOCK signal (A1U18 pin 2) for the Microprocessor and GPIB Sections.
- A 39.0625 kHz TIMER clock signal (A1U18 pin 4) for the Microprocessor Section.
- A RESET (negative-going pulse at the end of each measurement period) signal (A1U18 pin 40) for the MCC2 Circuit and Channel C Section.

Additional signals from the MCC2 Circuit (A1U39) include:

- A 10 MHz INT REF OUT signal (A1U39 pin 36), derived from the frequency standard, for the TEC Circuit (HI pin 6). Signal is inverted (A1U29e) and routed to MCC1 Circuit (A1U18 pin 24).
- A GATE (logic 0 during the measurement period) signal (A1U39 pin 27) for the MCC1 Circuit and Channel C Section.



CE1ZS006

Figure 1-6. Display Section Simplified Block Diagram.

4 DISPLAY (fig. 1-6). This section is responsible for providing measurement information and instrument status to the operator. This section is contained on the following circuit card assembly:

- A1 Motherboard Circuit Card Assembly (fig. FO-2 sheet 2).
- A2 Display Circuit Card Assembly (fig. FO-3),

The Display Section can be divided into the following major circuits:

- Driver Circuits.
- Display Circuits.
- LED Indicator Circuits.

Driver Circuits. Interfaces the Microprocessor Section control and measurement information to specific lighted front panel display segments and LEDs. Driver Circuits control all front panel indications except the REM, ADDR, SRQ, TRIG A, TRIG B, GATE, and STBY/CHRG LEDs.

DisplayCircuits. Provides 10 digit alphanumeric display of measurement information to operator. Display consists of four two-digit displays (A2DI1-4) controlled by driver A2U4, and two one-digit displays (A2DI5/DI6) controlled by driver A2U3. Both drivers operate under control of the Microprocessor Section

LED Indicator Circuits. Provides 41 LED indicators for instrument status and measurement information. All LED indicators except A2DS1, 3-5, 7, 39, and 40 are controlled by display driver A2U3 under control of the Microprocessor Section. The remaining LED indicators are controlled as follows:

- REM (A2DS3), ADDR (A2DS4), SRQ (A2DS5) are driven by the GPIB Section.
- TRIG A (A2DS40) and TRIG B (A2DS39) are driven using A1U1 a/c by the Channel A/B Section.
- GATE (A2DS7) is driven using A1U1b by the Measurement Section.
- STBY/CHGR (A2DS1) is driven using A1Q13 by the Standby and Interrupt Section.

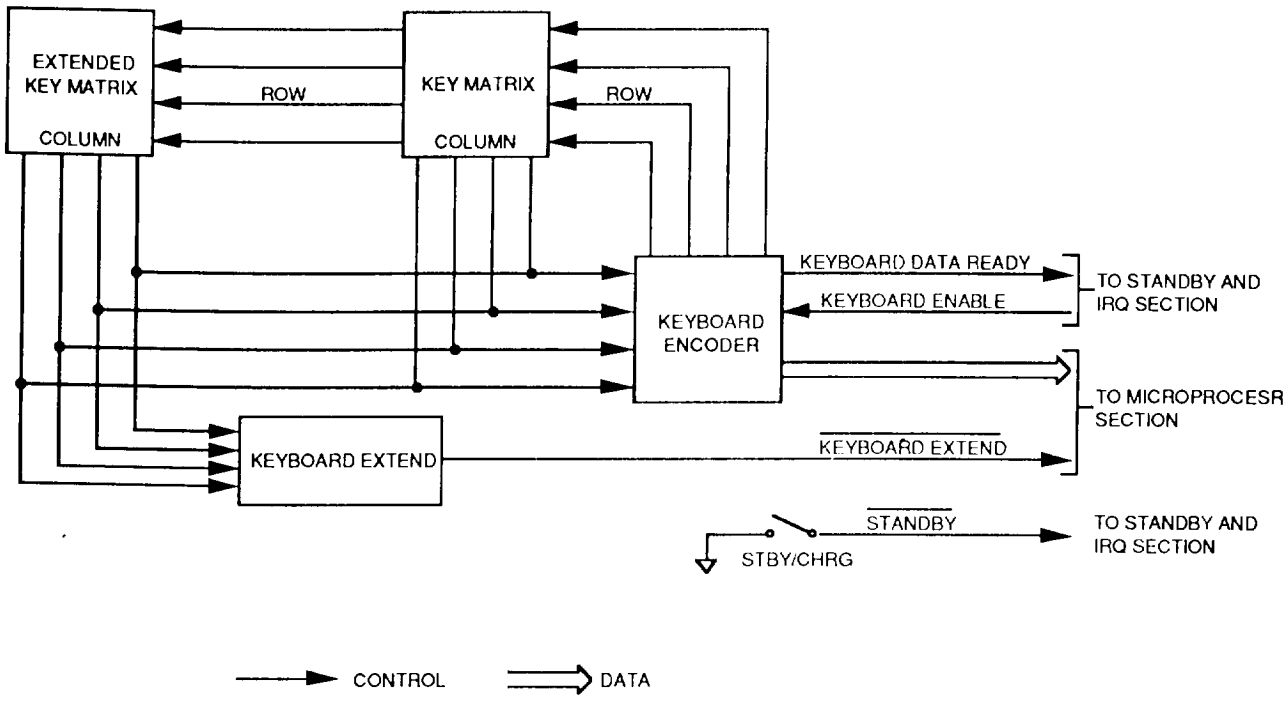


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Figure 1-7. Keyboard Section Simplified Block Diagram.

5 KEYBOARD (fig. 1-7). This section provides the operator a means to communicate commands to the internal circuits of the Counter. This section is contained on the following circuit card assembly:

- A2 Display Circuit Card Assembly (fig. FO-3).

The Keyboard Section can be divided into the following major circuits:

- Key Matrix Circuit.
- Extended Key Matrix Circuit.
- Keyboard Encoder Circuit.
- Keyboard Extend Circuit.

Key Matrix Circuit. Provides individual key select information to the Keyboard Encoder Circuit. Consists of 16 front panel keys in one matrix. Circuit described in detail below.

Extended Key Matrix Circuit. Provides individual key select information to the Keyboard Encoder Circuit. Consists of the remaining 16 front panel keys in one matrix. Circuit described in detail below.

Keyboard Extend Circuit. Informs the Microprocessor Section in what matrix a key was activated. Circuit described in detail below.

Keyboard Encoder Circuit. Informs the Microprocessor Section what key, by row and column, was activated. Circuit described in detail below.

The keys are divided into two 16-key matrices having common row lines connected to the Encoder Circuit. The Encoder Circuit normally holds the row lines at logic O. When a key is pressed, the corresponding column line is pulled to logic O. The encoder then scans the keyboard and stores a 4-bit code, corresponding to the row and column of the key, in an internal register. The KEYBOARD EXTEND line indicates which matrix contains the key that is pressed.

The inputs to Keyboard Encoder Circuit and KEYBOARD EXTEND line are normally held at logic 1. If a key in the Extended Key Matrix Circuit is pressed (column to logic O), the KEYBOARD EXTEND line will go to logic O. If a key in the Key Matrix Circuit is pressed, the KEYBOARD EXTEND line will remain at logic 1 because the column lines are isolated by A2CR6-CR10.

When the key-position code has been stored, the Encoder Circuit sets the KEYBOARD DATA READY line to logic 1. This generates a microprocessor interrupt. The Microprocessor Section sets the KEYBOARD ENABLE line to logic O. The Encoder Circuit then puts the 4-bit code (matrix row and column) onto the data bus, The Microprocessor Section then reads the KEYBOARD EXTEND line to determine which matrix contained the key that has been pressed.

When the STBY/CHRG key is pressed, the STANDBY control signal is sent to the Power Supply Section through the Standby and IRQ section.

6 MICROPROCESSOR (fig. 1-8). This section provides overall control of the internal circuitry in the Counter. This section is contained on the following circuit card assembly:

- Al Motherboard Circuit Card Assembly (fig. FO-2, sheet 3).

The Microprocessor Section can be divided into the following major circuits:

- Microprocessor Circuit.
- ROM Circuit.
- Address Latch Circuit.
- Chip Select Latch Circuit.
- Relay Control Line Latch Circuit.
- Control Line Latch Circuit.
- Auxiliary Read Latch Circuit.

Microprocessor Circuit. Provides overall control of the Microprocessor Section. Contains the following buses/ports:

A8 to A12 - 5-bit bus used for the high-order address bits.

B0 to B7 - 8-bit multiplexed bus which is used for the low-order address bits and for data.

PA0 to PA7 - port A input/output port.

PB0 to PB7 - port B input/output port.

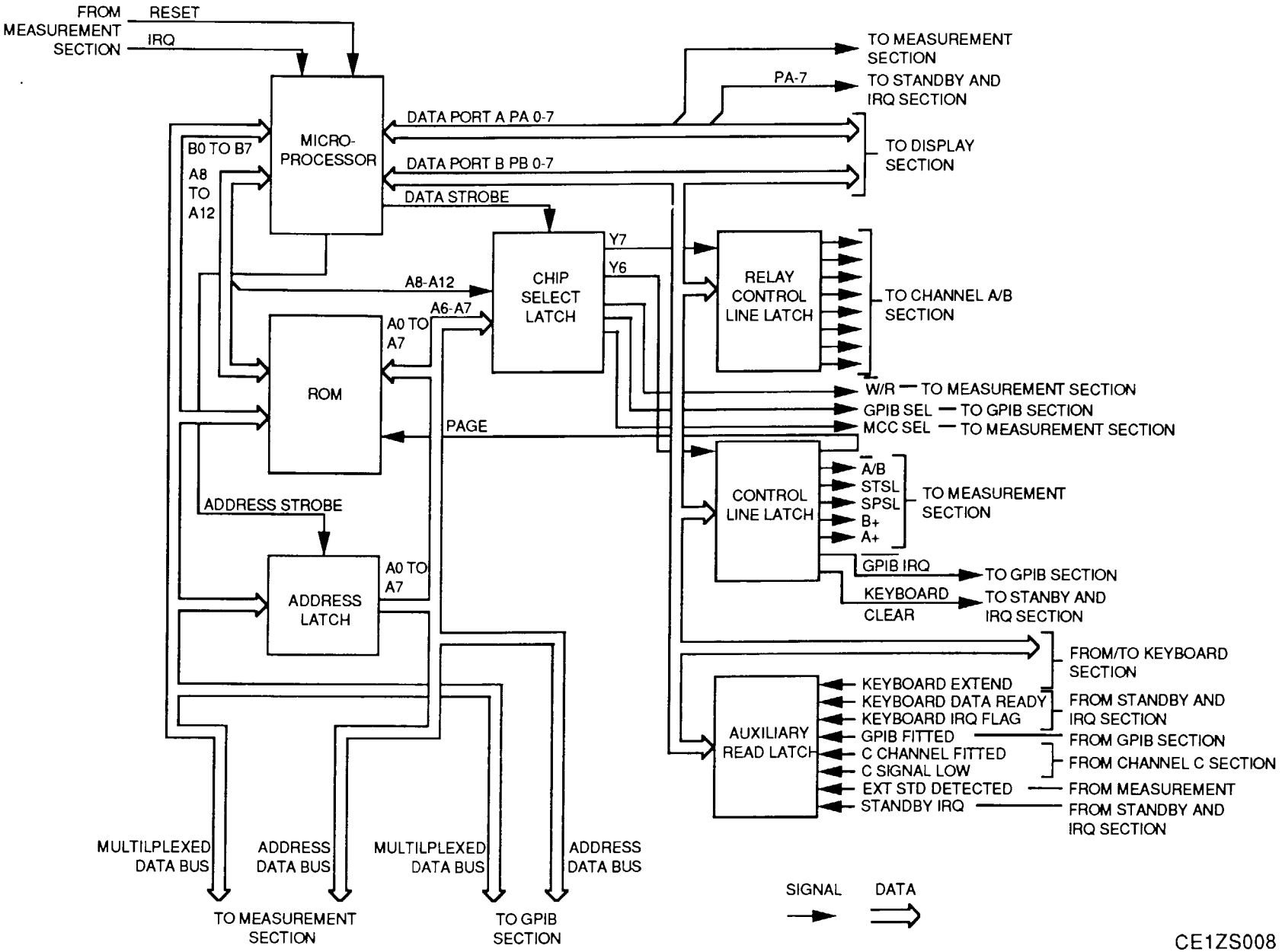


Figure 1-8. Microprocessor Section Simplified Block Diagram.

Multiplexed Bus Operation is as follows:

- The Microprocessor puts ADDRESS STROBE (A1U19 pin 6) at logic 1 and DATA STROBE (A1U19 pin 4) at logic 0. This enables the Address latch (A1U20 pin 11 at logic 1), disables ROM (A1U22 pin 20 at logic 1), and disables the Chip Select Latch (A1U21 pin 6 at logic 0).
- The address is put onto lines B0 to B7 and A8 to A12. When the lines have settled, the ADDRESS STROBE line is taken to logic 0. The low-order bits of the address are latched into the Address Latch (A1U20) and are held on address lines A0 to A7. Lines B0 to B7 are now free for use as a data bus.

The CLOCK (A1U19 pin 39) and TIMER (A1U19 pin 37) signals are generated in the Measurement Section, A RESET (A1U19 pin 1) signal is generated in the Standby and IRQ Section when the Counter is switched on or off,

ROM Circuit. Stores the system software used by the Microprocessor. See Microprocessor Circuit above for more information.

Address Latch Circuit. Under control of the Microprocessor, latches information from the multiplexer bus (B0-B7) to the address bus (A0-A7). See Microprocessor Circuit above for more information.

Chip Select Latch Circuit. The levels on address lines A6 to A12 are decoded in the Chip Select Latch (A1U21) to provide the following outputs:

- MCCSEL (chip-select signal for MCC1 A1U18 in the Measurement Section).
- GPIB SEL (chip-select signal for GPIB Address Decoder A6U3 in the GPIB Section).
- WR (write control signal for DACA1H2 in the Channel A/B Section).
- Y6 (chip select signal for Control Line Latch A1U25).
- Y7 (chip select signal for Relay Control Line Latch A1U24).

These outputs are only available when Chip Select Latch is enabled (logic 1 at A1U21 pin 6 and logic 0 at A1U21 pins 4 and 5). The level at A1U21 pin 6 is set by the DATA STROBE output at A1U19 pin 4 (at logic 1 when the multiplexed bus is available for data transfer). All outputs from Chip Select Latch are decoded from addresses with lines A9 to A12 at logic 0, when A1U21 pins 4 and 5 are held at logic 0 by the output from A1U27a, b,d.

Relay Control Line Latch Circuit. Under control of the Microprocessor data port B, maintains voltage levels on the control lines to the Channel A/B See? ion. Detailed circuit information is provided below.

Control Line Latch Circuit. Under control of the Microprocessor data port B, maintains voltage levels on the control lines to the Measurement, GPIB, and Keyboard Sections. Detailed circuit information is provided below.

Auxillary Read Latch Circuit. Read the status of the other sections in the Counter and provides the information to the Microprocessor using data port B. Detailed circuit information is provided below.

The logic levels required on the control lines and on the PAGE line (most significant bit of RAM address) are set into Relay Control Line Latch (A1U24) and Control Line Latch (A1U25) from data port B of the Microprocessor (A1U19), The latch strobe signals are decoded in the Chip Select Latch (A1U21), Data may be read by the Microprocessor from the Auxiliary Read Latch (A1U23). The latch strobe signal is provided from data port A of the Microprocessor,

The latches and registers connected to the multiplexed bus in the Measurement Section are controlled by the MCC SELECT signal. The display data latches in the Display Section are controlled by strobe and chip select signals obtained from port A.

(7) STANDBY AND IRQ (fig. 1-9). Generates reset signals for the Microprocessor and GPIB Sections. Provides standby switching signal for the Power Supply Section. Combines the interrupt signals from the GPIB, Measurement, and Keyboard Sections and routes the information to the Microprocessor Section. This section is contained on the following circuit card assembly:

- Al Motherboard Circuit Card Assembly (fig. FO-2, sheet 3).

The Standby and IRQ Section can be divided into the following major circuits:

- Reset Circuit.
- Standby Select Circuit.
- Standby IRQ Latch Circuit.
- Standby ON/OFF Latch Circuit.
- Keyboard IRQ Latch Circuit.
- IRQ Select Circuit.
- IRQ Inhibit Circuit.

Reset Circuit. Generates reset signals for the Microprocessor and GPIB Sections whenever power is applied to or removed from the Power Supply Section. When the Power Supply Section is switched on, the input to A1U32f if held low until A1C125 charges through A1R215, Q29a, and R216. The output at A1U32f pin 12 goes to logic 1 when power is applied, but drops to logic O after approximately 500 ms. This output is inverted (A1U32e) to provide the Microprocessor Section RESET, and buffered (A1Q29c) to provide the GPIB Section RESET.

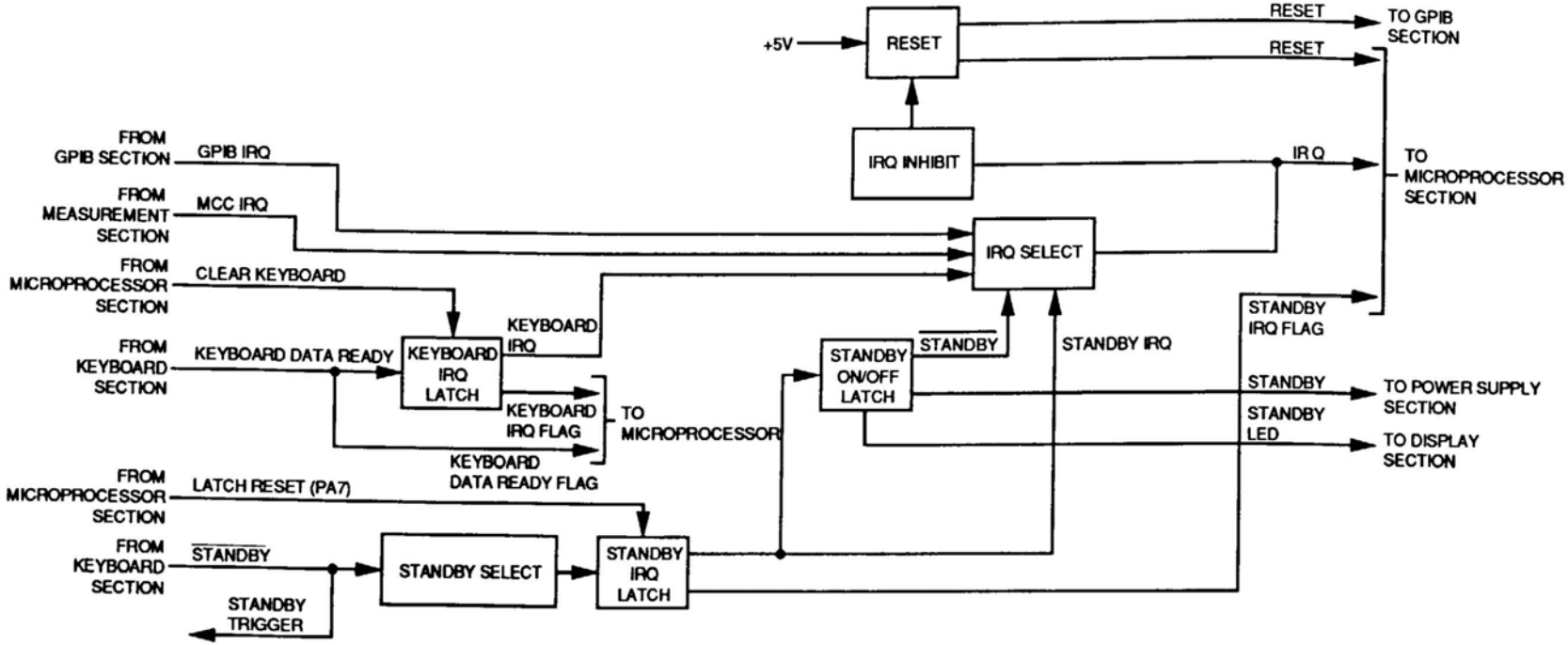
If there is a reduction in the +5V STANDBY supply (power off or failure) the potential across A1R217 falls. The potential at A1Q27 emitter is maintained by the charge in Al C125, so A1Q27 conducts, The current in A1R218 makes the base of Al Q29d positive. The transistor conducts and holds the base of A1Q27 low until A1C125 is completely discharged. This ensures that a good reset action is obtained, even if power is quickly restored.

Standby Select Circuit. When STBY/CHRG key in the Keyboard Section is selected, the STANDBY signal (A1P1 pin 14) is taken to 0V. Denouncing is provided by A1R158 and C126. The leading edge of the signal is sharpened in A1U32C, C118, R151, and U32d. The output sets Standby IRQ latch (A1U30c/d).

Standby IRQ Latch Circuit. The negative-going output from A1U30C pin 10 is passed through A1U30a, U32a, and R152 10 Microprocessor Section (A1U19 pin 2) This signal (STANDBY IRQ) provides a Microprocessor interrupt. The positive-going output from A1U30d pin 11 forms the STANDBY IRQ FLAG (read by the Microprocessor using A1U23 during the Interrupt routine) and clocks the Standby ON/OFF Latch (A1U26b) to the set state. The LATCH RESET signal (A1U19 pin 7) from the Microprocessor Section is used to reset the Standby IRQ Latch (logic 1 to A1U30C pin 8) at the end of the interrupt routine.

Standby ON/OFF Latch Circuit. A logic 0 level at A1U26b pin 8 switches on A1Q13 and provides power for the STANDBY LED in the Display Section. The STANDBY output is applied to A1U30b pin 5 and disables the other interrupts which are connected to A1U30b pin 6. The logic 1 level at A1U26b pin 9 shuts down the Power Supply Section (except the +5V STANDBY SUPPIY).

On return from standby, the Standby IRQ Latch is again set. This provides a Microprocessor interrupt and sets the standby IRQ flag as before. The positive-going output from A1U30d pin 11 clocks the Standby ON/OFF Latch back to the reset state, so that the STANDBY LED is turned off and the Power Supply Section is restored. The Microprocessor Resets the Standby IRQ Latch at the end of the interrupt routine.



CE1ZS009

Figure 1-9. Standby and IRQ Section Simplified Block Diagram.

Keyboard IRQ Latch Circuit. The KEYBOARD DATA READY signal from the Keyboard Section goes to logic 1 to indicate data is available. This clocks A1U26a to the set state and provides a KEYBOARD IRQ FLAG at A1U23 pin 11, and a KEYBOARD IRQ signal to the IRQ Select Circuit .(A1U28b pin 9).

IRQ Select Circuit. Interrupts from the Measurement Section (MCC IRQ) and the GPIB Section (GPIB IRQ) are connected to A1U28b pins 10, 12, and 13.

If any of these interrupts occur, A1U28b pin 8 and A1U30b pin 6 will go to logic 1. If the Standby ON/OFF Latch (A1U26b) is not set, A1U30b pin 5 will be at logic 1 and the IRQ signal passes through A1U30a and U32a to the Microprocessor Section (A1U19 pin 2).

When the Counter is switched into or out of the standby state, the Standby IRQ Latch (A1U30c,d) is set. The STANDBY IRQ signal from A1U30C pin 10 is routed to the Microprocessor Section (A1U19 pin 2) through A1U30a and U32a.

IRQ Inhibit Circuit. The circuit comprising A1R220, C121, U32b, and CR28 disables the Microprocessor IRQ input and holds the GPIB reset line low (using A1Q29c), while the +5V power supply to A1R220 is switched off. On return from standby, A1C121 charges and A1U32b pin 4 goes to logic 0. The Microprocessor IRQ input is enabled and the GPIB RESET line is reset. The delay in enabling the interrupts prevents the Standby IRQ Latch, which occurs on return from standby, from being acted upon before the Power Supply Section is fully restored.

(8) POWER SUPPLY (fig, 1-10). This section is responsible for providing all internal DC operating voltages. This section is contained on the following circuit card assembly:

- A1 Motherboard Circuit Card Assembly (fig. FO-2, sheet 2).

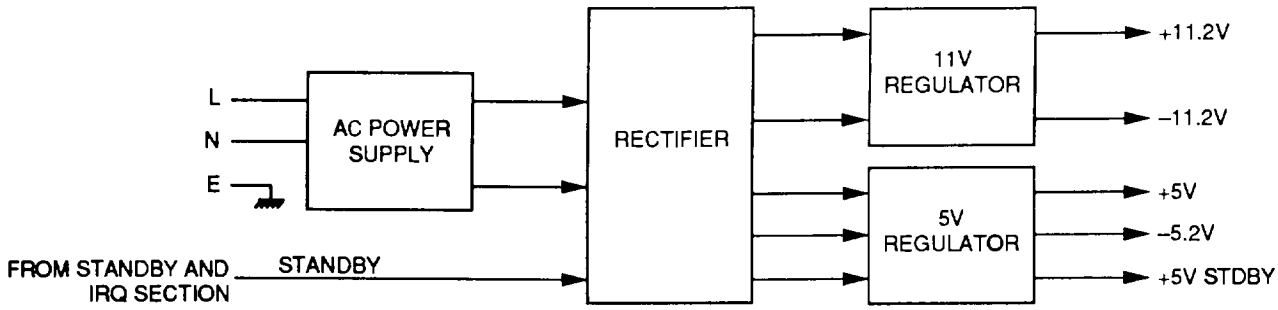
The Power Supply Section can be divided into the following major circuits:

- AC Power Supply Circuit.
- Rectifier Circuits.
- 11V Regulator Circuits.
- 5V Regulator Circuits.

AC Power Supply Circuit. Converts the line voltage available to usable AC voltage for internal power supplies. Provides AC line connection and contains the fuse protection, on/off switching, line filtering, and voltage selection facilities. AC power connected at the power input plug (A1J10) passes through fuse A1F1, and then RF filter (A1L1/L2/C46/C47/C48) to the POWER switch (A1S1b). The switched AC supply is connected to primary windings of T1 through the voltage selection card. Secondary AC voltages are provided to the Rectifier Circuits.

Rectifier Circuits. Converts the AC Power Supply Circuit AC secondary voltages into DC voltages. Consists of two separate rectifiers. The ±5V rectifier is made up of A1CR11, C49 and C50. The ±11V rectifier is made up of A1CR12, C52, and C59. Rectified outputs are routed to both Regulator Circuits.

11V Regulator Circuits. Regulates the Rectifier Circuit ±11V output to DC voltage levels for use in the Counter internal circuits. Provides two DC output voltages. A1U3 provides regulated +11.2V. A1U4 provides regulated –11.2V. The common terminals of both regulators are held at approximately -0.7V and +0.7V by diodes A1CR13 and CR14.



CE1ZS010

Figure 1-10. Power Supply Section Simplified Block Diagram,

5V Regulator Circuits. Regulates the Rectifier Circuit ±5V output to DC voltage levels for use in the Counter internal circuits. Provides three DC output voltages.

+5Vdc. Provided by two discrete component regulators having series elements A1Q8 and Q12. The non-inverting inputs to comparators (A1U31a and U31C) are connected to a +2.5V reference voltage, derived in hybrid circuit A1H2. Potential dividers formed by elements of A1R49 hold each inverting input at half the output voltage of the associated regulator.

-5.2Vdc. Provided by a discrete component regulator having A1Q6 as its series element. Comparator (A1U31b) inputs are held at approximately 0V. The potential divider controlling the inverting input is connected across the +5V and –5.2V supplies.

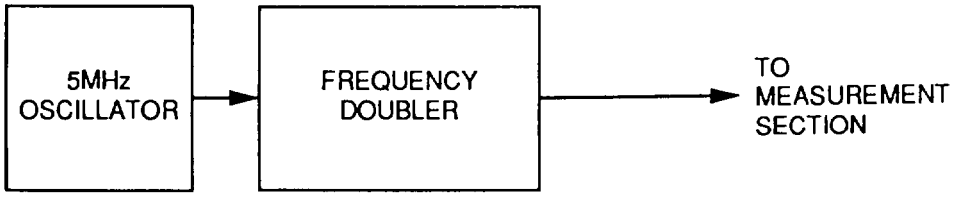
+5V Standby. Deactivates the +5 and -5V regulators during STBY/CHRG. When STBY/CHRG selected, standby latch A1U26b is clocked to the set state. The base of A1Q11 is pulled high and A1U31a pin 3 is pulled low, The base of A1Q9 is pulled low by A1U31a, the base current of A1Q8 is cut off, and the +5V regulator is shut down. When the voltage of the +5V regulator falls, A1U31b pin 6 goes more negative. The base of A1Q7 is taken towards 0V by A1U31bso that the base current of A1Q6 is cut off and the -5.2V regulator is shut down.

(9) INTERNAL FREQUENCY STANDARD (fig. 1-11). This section provides the stable internal reference signal used by the Measurement Section when making frequency measurements. This section is contained on the following assembly:

- A1 Motherboard Circuit Card Assembly (fig. FO-2, sheet 2).
- A4 Oscillator Assembly (fig. FO-5).

The Internal Frequency Standard Section can be divided into the following major circuits:

- 5 MHz Oscillator Circuit.
- Frequency Doubler Circuit.



CE1ZS011

Figure 1-11. Internal Frequency Standard Section Simplified Block Diagram.

5 MHz Oscillator Circuit. Generates a high stability temperature controlled 5 MHz signal.

Frequency Doubler Circuit. Provides the stable 10 MHz signal used in the Measurement Section. The 5 MHz input is applied to the balanced amplifier (A4A1Q1 and Q2). The base of A4A1Q3 is driven by the differential outputs from the amplifier through A4A1CR1 and CR2. This produces a 10 MHz signal. This 10 MHz signal is amplified and filtered in two stages (A4A1Q3 and Q5), and routed through buffer (A4A1Q6) to A1P14 pin 4. The 10 MHz internal reference signal is routed to the Measurement Section through buffer A1U2.

The 10 MHz output signal is fed back during the positive peaks of the signal. This adjusts the gain of A4A1Q5 to provide automatic level control.

(10) GPIB (fig. 1-12). This section allows all Counter functions, except POWER ON/OFF and STBY/CHRG, to be operated remotely using an external controller. This section is contained on the following assembly:

- A6 GPIB Circuit Card Assembly (fig. FO-6).

The GPIB Section can be divided into the following major circuits:

- General Purpose Interface Adapter (GPIA) Circuit.
- Microprocessor Circuit,
- ROM Circuit.
- RAM Circuit.
- Latch Circuits.
- Transceivers Circuits.
- Demultiplexer Circuit.
- Address Decoder Circuit.
- Bilateral Switch Circuit,

General Purpose Interface Adapter (GPIA) Circuit. Provides data transfer and IEEE-488 handshake protocol. Detailed circuit information is provided below.

Microprocessor Circuit. Provides overall control of the GPIB Section without involving the Microprocessor Section, Detailed circuit information is provided below.

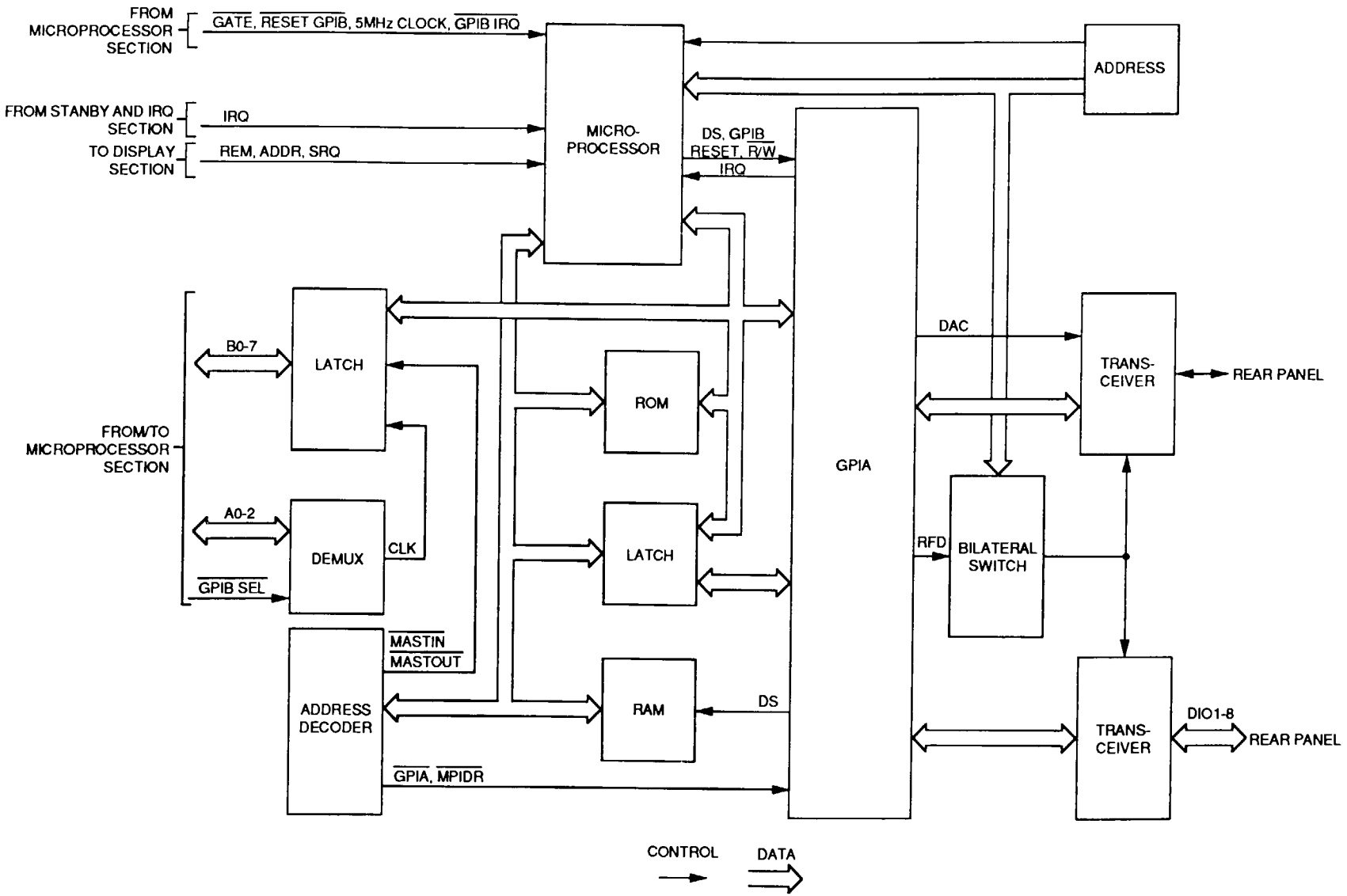


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Figure 1-12. GPIB Section Simplified Block Diagram.

ROM Circuit. Stores the software used by the Microprocessor circuit. Detailed circuit information is provided below.

RAM Circuit. Provides storage of data for Microprocessor and GPIA circuits. Detailed circuit information is provided below.

Latch Circuits. Transfers information from one type bus to another type bus. Made up of three separate latches.

- A6U1 latches Microprocessor Section information to GPIB Section.
- A6U2 latches GPIB Section information to Microprocessor Section.
- A6U11 latches eight low-order bits from multiplexed bus to address bus within GPIB Section.

Detailed circuit information is provided below.

Transceivers Circuits. Transmits/receives data and commands to/from interface bus (external controller). Detailed circuit information is provided below.

Demultiplexer Circuit. Controls flow of information to and from GPIB Section under control of the Microprocessor Section. Detailed circuit information is provided below.

Address Decoder Circuit. Controls flow of information within GPIB Section under control of the Microprocessor Circuit. Detailed circuit information is provided below,

Bilateral Switch Circuit. Controls flow of information within the Transceiver and GPIA Circuits under control of the Microprocessor Circuit. Detailed circuit information is provided below,

The GPIB Section is a self-contained, microprocessor-controlled assembly that handles the transferor data without involving the Microprocessor Section. Data transfer is made one byte at a time, each transfer being controlled by the IEEE-488 handshake protocol.

The GPIB Section performs the following functions:

- Address Setting.
- Address Recognition.
- Reading from the Bus.
- Writing to the Bus.
- Serial Poll.
- Data Transfer Between Microprocessors.

Address Setting, The microprocessor (A6U9) reads the settings of the address switches (A6S1), using port B inputs, approximately every 1 msec. The address settings are written into the internal address register in General Purpose Interface Adapter (GPIA) A6U12.

Address Recognition. When the interface address is set on the bus by the external controller, it is recognized by comparison with the contents of the internal address register in GPIA (A6U12).

Reading from the Bus. When the interface is addressed to listen, GPIA (A6U12) conducts the handshake procedure up to the point where the ready for data (RFD) indication is given. At this point GPIA (A6U12) sets the bilateral switch (A6U13) to complete the RFD line, and sets the Transceivers (A6U14 and U15) into the receive condition. Data from the Transceivers enters GPIA (A6U12) data-in register and an interrupt request is sent to microprocessor (A6U9).

The microprocessor (A6U19) interrupt routine establishes the reason for the interrupt. Address decoder (A6U8) is enabled/addressed using lines A4 to A7 and sends GPIA (A6U12) enable signal GPIA. The data-in register of GPIA (A6U12) is addressed using R/W, and A0 to A2. Microprocessor (A6U9) then reads the contents of GPIA (A6U12) data-in register and transfers the data to RAM (A6U28).

When GPIA (A6U12) data-in register has been read, the interrupt request is canceled and the DAC line is set high. The handshake routine then continues, and a further byte, if available is loaded into the data-in register. The interrupt and data transfer sequence is then repeated.

Writing to the Bus. When the interface is addressed to talk, GPIA (A6U12) sends an interrupt request to microprocessor (A6U9). GPIA (A6U12) data-out register is normally empty under these conditions.

At this point microprocessor (A6U9) sets bilateral switch (A6U13) to break and hold the RFD line at 0V. An interrupt request is then sent to microprocessor (A6U9). Even if the listening device indicates that it is ready for data, GPIA (A6U12) will not attempt to load the contents of the data-out register onto the bus.

The microprocessor (A6U19) interrupt routine establishes the reason for the interrupt. Address decoder (A6U8) is enabled/addressed using lines A4 to A7 and sends GPIA (A6U12) enable signal GPIA. The data-out register of GPIA (A6U12) is addressed using R/W, and A0 to A2. A data byte is then written into the register and the interrupt request is canceled.

Following the data transfer, microprocessor (A6U9) reconnects the RFD line by using bilateral switch (A6U13). When the listening device (external controller) indicates that it is ready for data, GPIA (A6U12) loads the contents of the data-out register onto the bus through Transceivers (A6U14 and U15), and continues with the handshake routine.

When GPIA (A6U12) data-out register has been read, an interrupt request is generated. Microprocessor (A6U9) again sets the RFD line to 0V using bilateral switch (A6U13) and the data transfer and data transmission sequence is then repeated.

Serial Poll. GPIA (A6U12) status byte register is normally updated approximately every 1 msec by microprocessor (A6U9). When the interface is addressed to talk, following the receipt of the serial poll enable (SPE) message, GPIA (A6U12) puts the status byte onto the bus without further action by microprocessor (A6U9).

Data Transfer Between Microprocessors. Data transfer between microprocessors in the Microprocessor Section and GPIB Section is made using the multiplexed data bus on both devices. Connections between the buses is made by using a D-type latch (A6U1 or U2). Latch used is dependent on the direction of data transfer. All data transfers are initiated by the sending device. The first byte indicates number of bytes to be transferred.

Data transfer from Microprocessor Section microprocessor (A1U19) to GPIB Section microprocessor (A6U9) is as follows:

- Microprocessor Section microprocessor (A1U19) sets GPIBIRQ line low to provide an interrupt request to GPIB Section microprocessor (A6U9). As part of the interrupt routine, address decoder (A6U8) is enabled and addressed to establish that the interrupt is from Microprocessor Section microprocessor (A1U19) and not GPIA (A6U12) using MPIDR line.
- GPIB Section microprocessor (A6U9) prepares to receive data, then enables and addresses address decoder (A6U8) to give a ready for data (RFD) signal (via data bus) to Microprocessor Section microprocessor (A1U19).
- Microprocessor Section microprocessor (A1U19) enables and addresses demultiplexer (A6U3) to read the RFD signal, put the first data byte on the bus, and clock latch (A6U1). Data from bus is latched into A6U1. A data valid (DAV) signal (via data bus) is then sent to GPIB Section microprocessor (A6U9).
- GPIB Section microprocessor (A6U9) reads the DAV signal, then cancels its RFD signal. Address decoder (A6U8) sets MASTIN line to enable latch (A6U1) and reads the data. A data accepted (DAC) signal is sent through latch (A6U2) and the ready for data (RFD) signal is reset. Microprocessor Section microprocessor (A1U19) cancels its data valid (DAV) signal and enters the next data byte into latch (A6U1). Data transfer continues until the required number of bytes have been received.

For data transfer from GPIB Section microprocessor (A6U9) to Microprocessor Section microprocessor (A1U19) is similar.

- The GPIBIRQ signal from GPIB Section microprocessor (A6U9) is read by the Microprocessor Section microprocessor (A1U19) during its interrupt routine. The IRQ signal is cancel led by the Microprocessor Section microprocessor (A1U19).
- During data transfer, the RFD, DAV, DAC signals are reversed. Data transfer is made through latch (A6U2) using MASTOUT line.

CHAPTER 2
MAINTNENANCE INSTRUCTIONS

Section I. REPAIR PARTS, SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

2-1. COMMON TOOLS AND EQUIPMENT.

Common tools and equipment required for general support maintenance of Digital Electronic Counter AN/USM-459A are listed in the Maintenance Allocation Chart (MAC), TM 11-6625-3232-12, Appendix B.

2-2. SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT.

There are no Special tools, TMDE, or support equipment required.

2-3. REPAIR PARTS.

Repair parts are listed and illustrated in the Repair Parts and Special Tools List, TM 11-6625-3232-24P.

Section II. SERVICE UPON RECEIPT

2-4. SERVICE UPON RECEIPT OF MATERIAL.

a. Unpacking. Special design reusable packing material inside this shipping carton provides maximum protection for Counter. Avoid damaging carton and packing material during equipment unpacking. Use the following steps for unpacking Counter:

- Cut and remove paper sealing tape on carton top and open carton.
- Grasp Counter firmly while restraining shipping carton and lift equipment and packing material vertically.
- Place Counter and end cap packing material on a suitable flat clean and dry surface.
- Remove end cap packing material while firmly supporting Counter.
- Remove protective plastic bag from Counter. Place desiccant bags back inside protective plastic bag.
- Place protective plastic bag and end cap packing material inside shipping carton.
- Return shipping carton to supply system.

b. Checking Unpacked Equipment.

- Inspect the equipment for damage incurred during shipment. If the equipment has been damaged, report the damage on SF 364, Report of Discrepancy (ROD).
- Check the equipment against the packing slip to see if the shipment is complete. Report all discrepancies in accordance with the instructions of DA Pam 750-8.
- Check to see whether the equipment has been modified.

2-5. PRELIMINARY SERVICING AND ADJUSTMENT OF EQUIPMENT.

a. Perform turn-on procedures given in TM 11-6625-3232-12.
b. Complete performance tests (para 2-17).

Section III. TROUBLESHOOTING SYMPTON INDEX

Counter

2-6. GENERAL.

Troubleshooting at the intermediate general support maintenance level requires you to locate any malfunction as quickly as possible. The amount of troubleshooting you can do is based on what the Maintenance Allocation Chart says you can fix. Because of this, the only trouble symptoms you will find here are those that could be caused by faulty items you can fix.

NOTE

- Before using the troubleshooting table, check your work order and talk to unit maintenance, if possible, for a description of the symptoms and the steps that have been taken to correct them.

- Check all forms and tags attached to, or accompanying, the equipment to determine the reason for removal from service.

2-7. TROUBLESHOOTING GUIDELINES.

The following is a list of aids that you can use when troubleshooting the Counter:

a. The Counter has built-in self tests that are used in troubleshooting. Procedures for self tests are specified in troubleshooting procedures.

b. Refer to the principles of operation, Chapter 1, Section Ill as required. This provides circuit theory of the section you are troubleshooting with references to the detailed functional and schematic diagrams. Counter Detailed Functional Block diagram and assembly/cable locator is located on figure FO-1. Detailed Functional Block and Schematic diagrams and assembly component locators for all major assemblies are located on figures FO-2 thru FO-6.

c. Circuit cooler, freezing compound (Appendix B, item 4) can be used in isolating problems. The most generally used method is to spray suspected circuits/components to see if the malfunction can be temporarily fixed. This method will not work all the time, but it can be a great timesaver. It is especially helpful on intermittent problems that get worse with a rise in temperature.

d. Many problems on Counters that have been in service for awhile are caused by corrosion. Sometimes removing and reseating the affected cable will correct a malfunction. Cleaning connector pins and/or switch contacts with isopropyl alcohol (Appendix B, item 1) will repair many types of digital and analog circuit malfunctions.

e. For microcircuit and connector orientation, pin one is identified by a “1” on printed circuit board.

2-8. EQUIPMENT INSPECTION.

The following inspection procedures shall be used to locate obvious malfunctions with the Counter.

a. Inspect all external surfaces of Counter for physical damage, breakage, loose or dirty contacts, and missing components.

b. Remove top and bottom covers (para 2-24) and A6 GPIB Circuit Card Assembly (para 2-33) as required to access components.

W A R N I N G

Counter contains high voltages. After power is removed, discharge capacitors to ground through 100 Ω resistor before working inside Counter to prevent electrical shock.

C A U T I O N

Do not disconnect or remove any board assemblies in the Counter unless the instrument is unplugged. Some board assemblies contain devices that can be damaged if the board is removed when the power is on. Several components, including MOS devices, can be damaged by electrostatic discharge. Use conductive foam and grounding straps when servicing is required around sensitive components. Use care when unplugging IC'S from high-grip sockets.

c. Inspect printed circuit board surfaces for discoloration, cracks, breaks, and warping.

d. Inspect printed circuit board conductors for breaks, cracks, cuts, erosion, or looseness.

e. Inspect all assemblies for burnt or loose components.

f. Inspect all chassis-mounted components for looseness, breakage, loose contacts or conductors.

g. Inspect Counter for disconnected, broken, cut, loose, or frayed cables or wires.

2-9. TROUBLESHOOTING TABLE.

The Troubleshooting table (table 2-1) lists common malfunctions which may be found during normal operation or maintenance of the Counter or its components, you should perform the tests or inspections and corrective actions in the order listed.

NOTE

- After repair of Counter verify malfunction is cleared. If not, perform the proper adjustment (table 2-2).
- All voltage readings referenced to chassis ground unless otherwise specified.
- See figure FO-1 for assembly and cable location diagram.

Table 2-1. Troubleshooting.

MALFUNCTION	TEST OR INSPECTION	CORRECTIVE ACTION
1. Counter Displays ER XX Errors.		
	ER 50 Displayed.	
	Perform Check Mode Test (para 2-11).	
		● Replace faulty component/assembly.
	ER51 Displayed.	
	Perform Channel A Test (para 2-13).	
		● Replace faulty component/assembly.
	ER 52 Displayed.	
	Perform Channel A Test (para 2-13).	
		● Replace faulty component/assembly.
	ER 53 Displayed.	
	Perform Channel A Test (para 2-13).	
		● Replace faulty component/assembly.
	ER54 Displayed.	
	Perform Channel A Test (para 2-13).	
		● Replace faulty component/ assembly.
	ER 55 Displayed.	
	Perform Channel A Test (para 2-13).	
		● Replace faulty component / assembly.
	ER 56 Displayed.	
	Perform Channel B Test (para 2-14).	
		● Replace faulty component/assembly.
	ER57 Displayed.	
	Perform Channel B Test (para 2-14).	
		● Replace faulty component/assembly.
	ER58 Displayed.	
	Perform Channel B Test (para 2-14).	
		● Replace faulty component/assembly.

Table 2-1. Troubleshooting — Continued.

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION
1. Counter Displays ER XX Errors —Continued.
ER60 Displayed.
Troubleshoot A1 Motherboard Circuit Card Assembly - Microprocessor Section - Control Line Latch circuit (around A1U25, page line) using figure FO-2 sheet 3.
● Replace faulty component/assembly.
ER61 Displayed,
Troubleshoot A1 Motherboard Circuit Card Assembly - Microprocessor Section RAM circuit (around A1U19) using figure FO-2 sheet 3.
● Replace faulty component/assembly.
2. All AN/USM-459A Failures,
Step 1, Set POWER switch to OFF.
● Disconnect all external cables except power cable.
Step 2. Set POWER switch to ON, Verify display lights.
● If indication is correct, proceed with step 4.
Step 3. Verify AC Line voltage and rear panel fuse.
● Replace faulty component.
Step 4. Using Digital Multi meter, verify the following voltages (fig. FO-2, sheet 1): A1Q8 collector . . . . . +4.7 to +5.5 Vdc A1Q12 collector . . . . . +4.7 to +5.5 Vdc A1Q6 collector . . . . . – 5.0 to -5.4 Vdc A1U3 output ..... +10.3 to +12.3 Vdc A1U4 output ..... -10,3 to -12.3 Vdc
● If indications are correct, proceed with step 5.
● If indications are incorrect, troubleshoot Al Motherboard Circuit Card Assembly - Power Supply Section using figure FO-2 sheet 2. Replace faulty component.

Table 2-1. Troubleshooting — Continued.

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION

2, All AN/USM-459A Failures — Continued.

Step5. Set POWER switch to OFF, then ON. Verify Counter displays "1992'' for approximately two seconds, then an eight digit number for approximately two seconds, then "00000000". Verify the following front panel LED conditions:

Hz LED ..... ON
RESOLUTION LED ..... ON
FREQ A LED ..... ON
INPUT A ⎍ LED ..... ON
INPUT B ⎍ LED ..... ON
INPUT A TRIG LED ..... ON or OFF
INPUT B TRIG LED ..... ON or OFF
All other displays and indicators OFF

- If ER XX is displayed, troubleshoot using table 2-1, malfunction number 1,
- If only LEDs are incorrect, troubleshoot A2 Display Circuit Card Assembly - Display Section using figure FO-3. Replace faulty component/assembly.
- If only display is incorrect, perform System Reset Test (para 2-10),
- If both display and LEDs are incorrect, troubleshoot A2 Display Circuit Card Assembly - Display Section using figure FO-3. Replace faulty component/assembly.

Step 6. Select CHECK mode using FUNCTION keys. Verify display indicates 10.0000000 E6.

- If front panel does not respond to key commands, troubleshoot A2 Display Circuit Card Assembly - Keyboard Section using figure FO-3. Replace faulty component/assembly.
- If front panel display indications are incorrect, perform Check Mode Test (para 2-11),

Step 7. Press STBY/CHRG key. Verify STBY/CHRG LED goes ON and all other indicators are OFF.

- If incorrect, and A1Q13 (C) is +5 Vdc (fig. FO-2, sheet 1), troubleshoot A2 Display Circuit Card Assembly - Display Section using figure FO-3, Replace faulty component/assembly.
- If incorrect, and A1Q13 (C) is not +5 Vdc (fig. FO-2, sheet 1), troubleshoot A1 Motherboard Circuit Card Assembly - Standby and IRQ Section Block around A1U26 using figure FO-2 sheet 3, Replace faulty component.

Step 8. Press STBY/CHRG key. Verify STBY/CHRG LED goes OFF, Verify display indicates 10.0000000 E6 ± 2 (LSD),

- If incorrect, troubleshoot Al Motherboard Circuit Card Assembly - Standby and IRQ Section Block around A1U26 using figure FO-2 sheet 3. Replace faulty component.

Table 2-1. Troubleshooting — Continued.

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION
2. All AN/USM-459A Failures — Continued.
Step 9. Complete performance tests (para 2-17).
NOTE Complete as many performance tests as possible to assist in isolating malfunction.
● If all performance tests pass, unit is operational, ● If performance tests fail, troubleshoot malfunction using table 2-1, malfunctions 3 through 11. ● If all performance tests pass, and malfunction only occurs during remote operation, perform GPIB Test (para 2-16).
3. Channel A Sensitivity Test Failure.
Step 1. Adjust Channel A Input (para 2-20).
Step 2. Perform Channel A Test (para 2-13).
● Replace faulty component/assembly.
4. Channel B Sensitivity Test Failure.
Step 1. Adjust Channel B Input (para 2-21).
Step 2. Perform Channel B Test (para 2-14).
● Replace faulty component/assembly.
5. Channel C Sensitivity Test Failure.
Step 1. Adjust Channel C Input (para 2-22).
Step 2. Perform Channel C Test (para 2-15).
● Replace faulty component/assembly.
6. External Input Sensitivity Test Failure.
Troubleshoot around A1U14 and U39 using figure FO-2, sheet 2.
● Replace faulty component/assembly.
7. Internal Output Level Test Failure.
Step 1. Troubleshoot Al Motherboard Circuit Card Assembly - Internal Frequency Standard Section around A1U2 and U39 using figure FO-2, sheet 2.
● Replace faulty component.
Step 2. Troubleshoot A5 Oscillator Assembly - Internal Frequency Standard Section using figure FO-4.
● Replace faulty assembly,

Table 2-1. Troubleshooting — Continued.

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION
8. Minimum Time Interval Test Failure.
Step 1. Troubleshoot Al Motherboard Circuit Card Assembly - Channel A and B Section around A1KH using figure FO-2, sheet 1.
● Replace faulty component.
Step 2. Troubleshoot A1 Motherboard Circuit Card Assembly - Measurement Section around A1H1, U18 and U39 using figure FO-2, sheet 3.
● Replace faulty component.
9. External Arming Test Failure.
Troubleshoot A1 Motherboard Circuit Card Assembly - Measurement Section around A1U18 and Q5 using figure FO-2, sheet 3.
● Replace faulty component/assembly.
10. Trigger Levels Test Failure.
Perform Trigger Test (para 2-12).
● Replace faulty component/assembly.
11. Internal Frequency Standard Accuracy Test Failure.
Step 1. Adjust Internal Frequency Standard (para 2-23).
Step 2. Troubleshoot Al Motherboard Circuit Card Assembly - Internal Frequency Standard Section around A1U2 and U39 using figure FO-2, sheet 2.
● Replace faulty component.
Step 3. Troubleshoot A5 Oscillator Assembly - Internal Frequency Standard Section using figure FO-4.
● Replace faulty assembly.

2-10. SYSTEM RESET TEST.

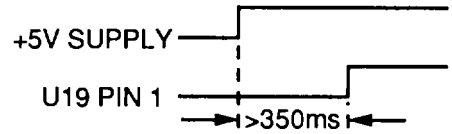
DESCRIPTION

This test is used to isolate a reset problem in the A1 Motherboard Circuit Card Assembly (fig. FO-2) to the malfunctioning component.

NOTE

Perform this procedure only when instructed from table 2-1 or another troubleshooting test. Do not perform this or any other troubleshooting test as a separate procedure unless otherwise instructed as certain conditions have been established and/or tested prior to performing this test.

1. Connect Oscilloscope channel A to +5 Vdc supply (A1Q8) collector (fig. FO-2 sheet 1) and channel B to A1U19 pin 1 (reset).
2. On AN/USM-459A, cycle POWER ON/OFF switch from OFF to ON.
3. Verify Oscilloscope display is as shown.



   - If signal is incorrect, troubleshoot Standby and IRQ Section - Reset Circuit (around Q27/Q29/U32) using figure FO-2, sheet 3. Replace faulty component.
4. Using an Oscilloscope, verify A1U19 pin 39 is 5 MHz at = 4 Vp-p (clock).
   - If signal is incorrect, troubleshoot Measurement Section - MCC1 Circuit (around U18) using figure FO-2, sheet 3. Replace faulty component.
   - If signal is correct, troubleshoot Microprocessor Section (around U19) using figure FO-2, sheet 3. Replace faulty component.
5. Remove power and disconnect test equipment.

2-11. CHECK MODE TEST.

DESCRIPTION

This test is used to isolate a Check Mode failure in the A1 Motherboard Circuit Card Assembly (fig. FO-2) to the malfunctioning component.

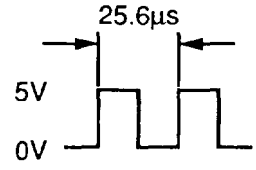
NOTE

Perform this procedure only when instructed from table 2-1 or another troubleshooting test. Do not perform this or any other troubleshooting test as a separate procedure unless otherwise instructed as certain conditions have been established and/or tested prior to performing this test.

1. On AN/USM-459A, verify unit is in CHECK mode and observe display.
   - If display shows ER 50, proceed with step 3,

2-11. CHECK MODE TEST — Continued.

2. Using an Oscilloscope, verify A1U19 pin 37 (timer) is as shown.



- If signal is correct, troubleshoot Measurement Section - MCC2 Circuit (around U39) using figure FO-2, sheet 3. Replace faulty component.
- If signal is incorrect, malfunction is A1U18 or U19. Troubleshoot using figure FO-2, sheet 3 and replace faulty component.

3. On AN/USM-459A, select and activate the following special functions and observe display.

Special Function 73 — display reads from 580 to 1020. Record value.

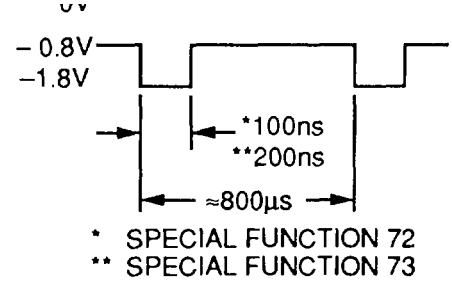
Special Function 72 —display reads value recorded for Special Function 73 + 2 (+20, – 40).

Special Function 75 — display reads from 580 to 1020. Record value.

Special Function 74 —display reads value recorded for Special Function 75 + 2 (+20, - 40).

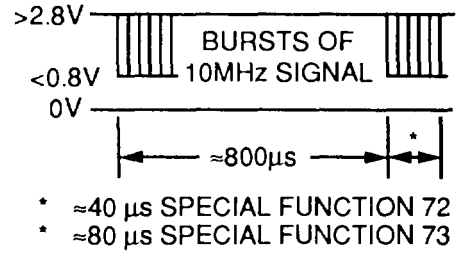
- If only Special Function 72 or 73 incorrect, proceed with step 4.
- If only Special Function 74 or 75 incorrect, proceed with step 6.
- If all values are correct, troubleshoot Measurement Section - MCC2 Circuit (around U39) using figure FO-2, sheet 3. Replace faulty component.

4. On AN/USM-459A, select and activate the following special functions and, using an Oscilloscope, verify A1U39 pin 8 (ST TEC out) is as shown.



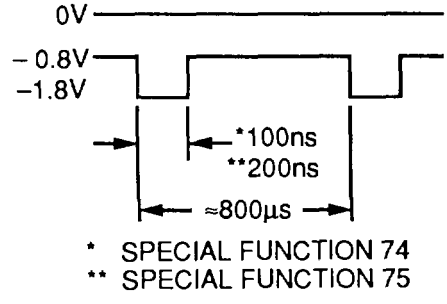
- If signal is incorrect, malfunction is A1U39 or H1. Troubleshoot using figure FO-2, sheet 3 and replace faulty component.

5. On AN/USM-459A, select and activate the following special functions and, using an Oscilloscope, verify A1U18 pin 26 (ST TEC) is as shown.



- If signal is correct, malfunction is A1U18. Replace faulty component.
- If signal is incorrect, malfunction is A1U18 or H1. Troubleshoot using figure FO-2, sheet 3 and replace faulty component.

6. On AN/USM-459A, select and activate the following special functions and, using an Oscilloscope, verify A1U39 pin 7 (SP TEC out) is as shown.

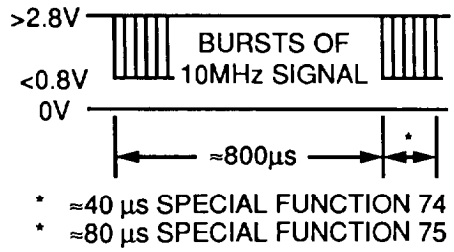


- If signal is incorrect, malfunction is A1U39 or H1, Troubleshoot using figure FO-2, sheet 3 and replace faulty component.

2-11. CHECK MODE TEST — Continued.

7. On AN/USM-459A, select and activate the following special functions and, using an Oscilloscope, verify A1U18 pin 25 (SP TEC) is as shown.

   - If signal is correct, malfunction is A1U18. Replace faulty component.
   - If signal is incorrect, malfunction is A1U18 or HI. Troubleshoot using figure FO-2, sheet 3 and replace faulty component.



8. Remove power and disconnect test equipment.

2-12. TRIGGER TEST.

DESCRIPTION

This test is used to isolate a failed Trigger Level Performance Test in the Counter (fig. FO-1) to the malfunctioning assembly or component.

NOTE

Perform this procedure only when instructed from table 2-1 or another troubleshooting test. Do not perform this or any other troubleshooting test as a separate procedure unless otherwise instructed as certain conditions have been established and/or tested prior to performing this test.

1. On AN/USM-459A,

   - Verify A6 GPIB Circuit Card Assembly is installed (para 2-33).
   - Apply power and select CHECK function.
   - Select and activate special function 71.

   Verify all LEDs except GATE and STBY/CHRG flash on-off. Verify the REM, ADDR, and SRQ LEDs stay on. Trig A and/or Trig B LEDs may be on or off.

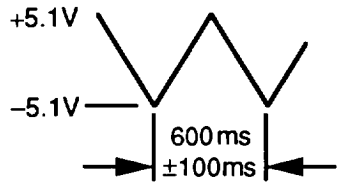
   - If incorrect, troubleshoot A2 Display Circuit Card Assembly - Display Section using figure FO-3. Replace faulty assembly or component.

2. On AN/USM-459A,

   - Remove A6 GPIB Circuit Card Assembly (para 2-33).
   - Apply power and select CHECK function.
   - Select and activate the special function 76

3. Using an Oscilloscope, verify rear panel Trigger Outputs A and B are as shown.

   - If signals are incorrect, troubleshoot Al Motherboard Circuit Card Assembly -Channel A and B Section (around A1H2) using figure FO-2, sheet 3. Replace faulty component.



2-12. TRIGGER TEST — Continued.

4. On AN/USM-459A,
   - Deactivate special function 71.
   - Ground Input A center conductor.
   - Ground Input B center conductor.
   - Using the front panel keys, enter a trigger level of +5. 1V on Input A.
   - Using the front panel keys, enter a trigger level of +5.1V on Input B.
5. On AN/USM-459A, verify Trig A LED is off.
   - If correct, proceed with step 7.
6. Using an Oscilloscope, verify A1U36 pin 1 is =– 0.75V.
   - If level is correct, troubleshoot A1 Motherboard Circuit Card Assembly - Channel A and B Section (around A1U1a/Q1) using figure FO-2, sheet 1. Replace faulty component.
   - If level is incorrect, troubleshoot A1 Motherboard Circuit Card Assembly - Channel A and B Section (around A1U36a/Q21) using figure FO-2, sheet 1. Replace faulty component.
7. On AN/USM-459A, select and activate special function 21. Verify Trig B LED is off.
   - If correct, proceed with step 9.
8. Using an Oscilloscope, verify A1U36 pin 16 is =- 0.75V.
   - If level is correct, troubleshoot A1 Motherboard Circuit Card Assembly - Channel A and B Section (around A1U1c/Q3) using figure FO-2, sheet 1. Replace faulty component.
   - If level is incorrect, troubleshoot A1 Motherboard Circuit Card Assembly - Channel A and B Section (around A1U36b/Q23) using figure FO-2, sheet 1. Replace faulty component.
9. On AN/USM-459A,
   - Using the front panel keys, enter a trigger Ievel of – 5.1V on Input A.
   - Using the front panel keys, enter a trigger level of -5.1 V on Input B.
   - Deactivate special function 21.
10. On AN/USM-459A, verify Trig A LED is on.
   - If correct, proceed with step 12.
11. Using an Oscilloscope, verify A1U36 pin 1 is =– 1.55V.
   - If level is correct, troubleshoot A1 Motherboard Circuit Card Assembly - Channel A and B Section (around A1U1a/Q1) using figure FO-2, sheet 1. Replace faulty component.
   - If level is incorrect, troubleshoot A1 Motherboard Circuit Card Assembly - Channel A and B Section (around A1U36a/Q21) using figure FO-2, sheet 1. Replace faulty component.
12. On AN/USM-459A, select and activate special function 21. Verify Trig B LED is on.
   - If correct, proceed with step 14.
13. Using an Oscilloscope, verify A1U36 pin 16 is =- 1.55V.
   - If level is correct, troubleshoot A1 Motherboard Circuit Card Assembly - Channel A and B Section (around A1U1c/Q3) using figure FO-2, sheet 1. Replace faulty component.
   - If level is incorrect, troubleshoot A1 Motherboard Circuit Card Assembly - Channel A and B Section (around A1U36b/Q23) using figure FO-2, sheet 1. Replace faulty component.
14. Troubleshoot all other trigger malfunctions using figure FO-2. Replace faulty component.
15. Remove power and disconnect test equipment.

2-13. CHANNEL A TEST.

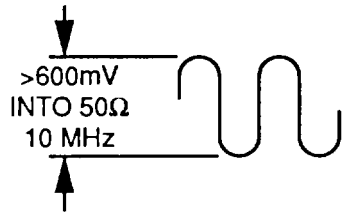
DESCRIPTION

This test is used to isolate a failure in the Input A circuits in the A1 Motherboard Circuit Card Assembly (fig. FO-2) to the malfunctioning assembly or component.

NOTE

Perform this procedure only when instructed from table 2-1 or another troubleshooting test. Do not perform this or any other troubleshooting test as a separate procedure unless otherwise instructed as certain conditions have been established and/or tested prior to performing this test.

1. Using an Oscilloscope, verify rear panel 10 MHz STD OUTPUT is as shown.



   - If signal is incorrect, troubleshoot Internal Frequency Standard Section using figure FO-2 sheet 3, and FO-4. Replace faulty assembly or component.

2. On AN/USM-459A,
   - Connect 10 MHz STD OUTPUT connector to Input A connector using a 50 Ω BNC-BNC cable.
   - Select CHECK function.
   - Select and activate special function 77.
   - Wait 10 seconds.

3. On AN/USM-459A, verify display indicates "0. 0"
   - If "Er 51" displayed, troubleshoot around A1KE and KF using figure FO-2, sheet 1. Replace faulty component.
   - If "Er 52" displayed, troubleshoot around A1KC using figure FO-2, sheet 1. Replace faulty component.
   - If "Er 53" displayed, troubleshoot around A1KA using figure FO-2, sheet 1. Replace faulty component.
   - If "Er 54" displayed, troubleshoot around A1KE using figure FO-2, sheet 1. Replace faulty component.
   - If "Er 55" displayed, troubleshoot around A1KH using figure FO-2, sheet 1. Replace faulty component.

4. On AN/USM-459A,
   - Select and activate special function 70.
   - Select FREQ A function.
   - Set RESOLUTION to 9 digits.
   - Press and hold RESOLUTION key until exponent digit is on and gate time is =10 seconds.
   - Select Input A to 50 Ω.
   - Select Input A AUTO TRIG.

5. On AN/USM-459A, verify display indicates "000.000000^{3}" ± 2(LSD) and O/F indicator is ON.
   - If incorrect, troubleshoot Measurement Section around A1U39 using figure FO-2, sheet 3. Replace faulty component.

6. Troubleshoot all other channel A malfunctions using figure FO-2. Replace faulty component or assembly.

7. Remove power and disconnect test equipment.

2-14. CHANNEL B TEST.

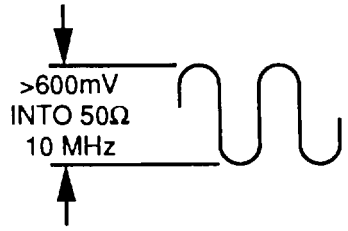
DESCRIPTION

This test is used to isolate a failure in the Input B circuits in the A1 Motherboard Circuit Card Assembly (fig. FO-2) to the malfunctioning assembly or component.

NOTE

Perform this procedure only when instructed from table 2-1 or another troubleshooting test. Do not perform this or any other troubleshooting test as a separate procedure unless otherwise instructed as certain conditions have been established and/or tested prior to performing this test.

1. Using an Oscilloscope, verify rear panel 10 MHz STD OUTPUT is as shown.



   - If signal is incorrect, troubleshoot Internal Frequency Standard Section using figure FO-2 sheet 3, and FO-4. Replace faulty assembly or component.

2. On AN/USM-459A,
   - Connect 10 MHz STD OUTPUT connector to Input B connector using a 50 Ω BNC-BNC cable.
   - Select CHECK function.
   - Select and activate special function 78.
   - Wait 10 seconds.

3, On AN/USM-459A, verify display indicates "0. 0"
   - If 'Er 56" displayed, troubleshoot around A1KG using figure FO-2, sheet 1. Replace faulty component.
   - If "Er 57" displayed, troubleshoot around A1KD using figure FO-2, sheet 1, Replace faulty component.
   - If "Er 58" displayed, troubleshoot around A1KB using figure FO-2, sheet 1. Replace faulty component.

4. On AN/USM-459A,
   - Select and activate special function 70.
   - Select FREQ A function.
   - Set RESOLUTION to 9 digits.
   - Press and hold RESOLUTION key until exponent digit is on and gate time is =10 seconds.
   - Select Input B to 50 Ω.
   - Select Input B AUTO TRIG.
   - Select and activate special function 21.

5. On AN/USM-459A, verify display indicates "000.000000[3]" ± 2(LSD) and O/F indicator is ON.
   - If incorrect, troubleshoot Measurement Section around A1U39 using figure FO-2, sheet 3. Replace faulty component.

6. Troubleshoot all other channel B malfunctions using figure FO-2. Replace faulty component or assembly.

7. Remove power and disconnect test equipment,

2-15. CHANNEL C TEST.

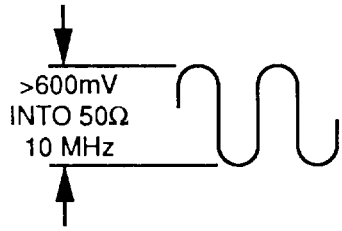
DESCRIPTION

This test is used to isolate a failure in the Input C circuits in the Counter (fig. FO-1) to the malfunctioning assembly or component.

NOTE

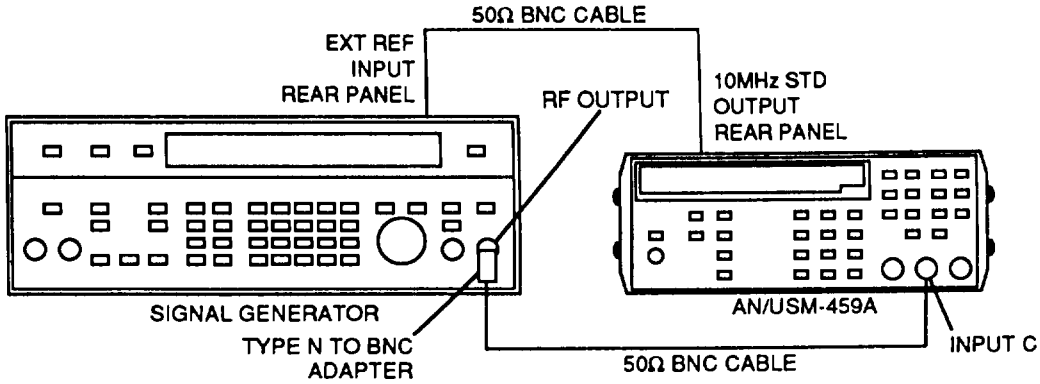
Perform this procedure only when instructed from table 2-1 or another troubleshooting test. Do not perform this or any other troubleshooting test as a separate procedure unless otherwise instructed as certain conditions have been established and/or tested prior to performing this test.

1. Using an Oscilloscope, verify rear panel 10 MHz STD OUTPUT is as shown.



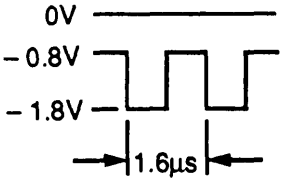
   - If signal is incorrect, troubleshoot Internal Frequency Standard Section using figure FO-2 sheet 3, and FO-4. Replace faulty assembly or component.

2. On AN/USM-459A,
   - Connect 10 MHz STD OUTPUT connector to Input A connector using a 50 Ω BNC-BNC cable.
   - Select FREQ C function.
   - Set RESOLUTION to 8 digits (set without signal input).
3. On AN/USM-459A verify GATE LED is not flashing.
   - If correct, proceed with step 5.
4. On AN/USM-459A, disconnect 50 Ω BNC-BNC cable at Input A connector, and verify GATE LED is not flashing.
   - If correct, troubleshoot around Al Motherboard Circuit Card Assembly - Channel C Section around A1U41a and U39 using figure FO-2, sheet 3. Replace faulty component.
   - If signal is incorrect, replace faulty A4 Channel C Prescaler Circuit Card Assembly (para 2-31).
5. On AN/USM-459A, disconnect 50 Ω BNC-BNC cable at Input A connector.
6. Connect test equipment as shown.



2-15. CHANNEL C TEST — Continued.

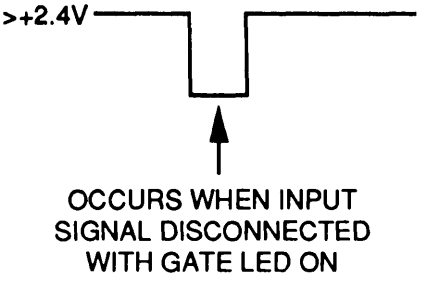
7. On AN/USM-459A,
   - Cycle POWER ON/OFF switch from OFF to ON.
   - Select FREQ C function.
8. Set Signal Generator controls as follows:
   - Frequency to 40 MHz.
   - Output level to 500 mV.
9. On AN/USM-459A verify GATE LED flashes, Verify display indicates 40.000000^{6} ± 2(LSD).
   - If correct, proceed with step 11.
10. Using an Oscilloscope, verify A1U39 pin 19 (C) is as shown.
    - If signal is correct, troubleshoot Al Motherboard Circuit Card Assembly - Measurement Section around A1U39 using figure FO-2, sheet 3. Replace faulty component,
    - If signal is incorrect, replace faulty A4 Channel C Prescaler Circuit Card Assembly (para 2-31).



11. On AN/USM-459A,
    - Set RESOLUTION to 9 digits.
    - Press and hold RESOLUTION key until exponent digit is on and gate time is ≈10 seconds.
    - Disconnect cable from Input Connector while GATE LED is ON,
12. On AN/USM-459A, verify display indicates "0.
    - If correct, proceed with step 14.
13. Using an Oscilloscope, verify A1U23 pin 13 (C LOW) is as shown.

NOTE

Trace displayed only when the signal is disconnected from the front panel with GATE LED on. It may be necessary to repeatedly reconnect and disconnect the input signal to verify indication on Oscilloscope. If Oscilloscope is set to 0.1ms/DIV, signal will be ≈2 divisions wide. Use internal negative trigger.



- If signal is correct, troubleshoot A1 Motherboard Circuit Card Assembly - Microprocessor Section around A1U19 and U23 using figure FO-2, sheet 3. Replace faulty component.
- If signal is incorrect, replace faulty A4 Channel C Prescaler Circuit Card Assembly (para 2-31).

14. Troubleshoot all other channel C malfunctions using figure FO-2 and figure FO-5. Replace faulty component or assembly.
15. Remove power and disconnect test equipment.

2-16. GPIB TEST.

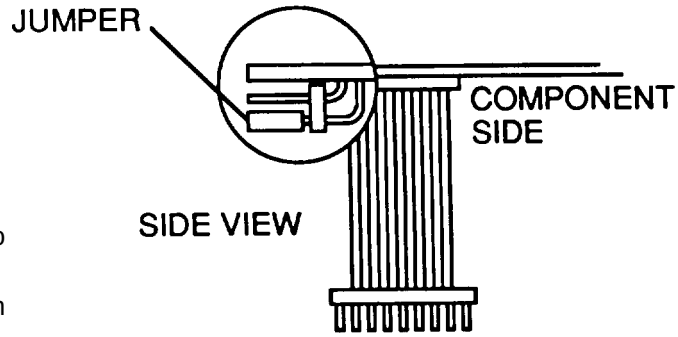
DESCRIPTION

This test is used to isolate a failure in the GPIB circuits in the Counter (fig. FO-1) to the malfunctioning assembly or component.

NOTE

Perform this procedure only when instructed from table 2-1 or another troubleshooting test. Do not perform this or any other troubleshooting test as a separate procedure unless otherwise instructed as certain conditions have been established and/or tested prior to performing this test.

1.

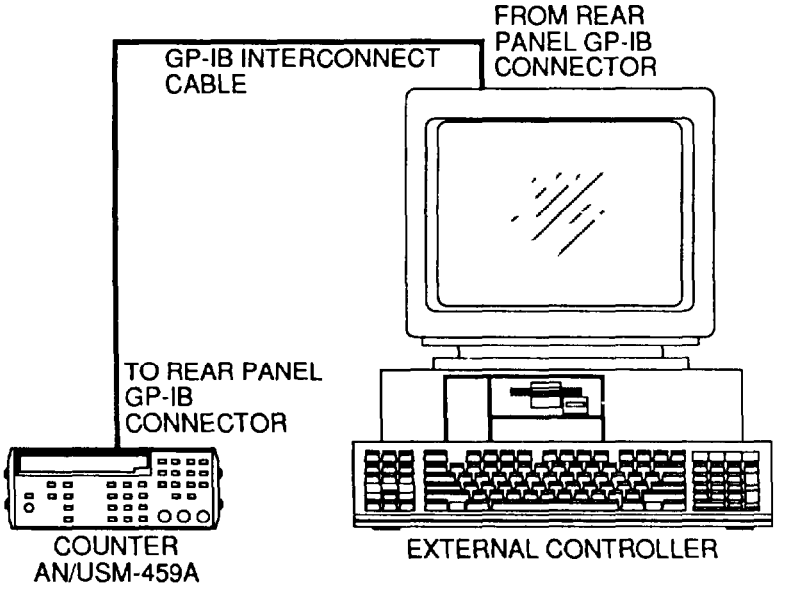


- Record rear panel address switch settings. Set position 1 to OFF (0).
- Cycle POWER ON/OFF switch from OFF to ON.
- Verify REM, SRQ, and ADDR LEDs flash on then off.

2. On AN/USM-459A,verify display flashes 1992, then 8572 XXXX, then indicates “00000000”.
   - If LEDs do not flash, replace defective A6 GPIB Circuit Card Assembly (para 2-33).
   - If Display frozen at 8572 XXXX, malfunction is between A1U19 and A6U9 microprocessors. Troubleshoot using figure FO-2, sheet 3 and FO-6. Replace faulty component/assembly.
3. On AN/USM-459A, change rear panel address switch position 1 and verify when ON, ADDR LED goes ON, and when OFF, ADDR LED goes OFF. Leave in OFF position.
   - If incorrect, replace defective A6 GPIB Circuit Card Assembly (para 2-33).

2-16. GPIB TEST — Continued.

4. Connect test equipment as shown.



5. On AN/USM-459A,
   - Verify all cables, except GPIB interconnect and power cable, are disconnected from AN/USM-459A.
   - Set the rear address switch to 15.
   - Cycle POWER ON/OFF switch from OFF to ON.
   - Press SHIFT (LED to ON), RECALL, then LOCAL keys and verify 15 is displayed.
   - Press CONTINUE key.
6. On the Controller, enter and run a program to perform the following functions:

   Reset the Counter

   Place Counter in CHECK mode.

   Read current display to the controller.

   Terminate Program.

   The following example is for an HP 85 controller.

```
10  REMOTE 715
20  OUTPUT 715; "CK"
30  DIM Z$ 21
40  ENTER 715; Z$
50  DISP Z$
60  END
```

7. On the Controller, verify REM and ADDR LEDs are on, and the display indicates CK+0010.0000000 E+06 ± 2(LSD).

   I If incorrect, replace defective A6 GPIB Circuit Card Assembly (para 2-33).
8. Reset rear panel address to position recorded in step 1.
9. Disconnect test equipment.

Section IV. MAINTENANCE PROCEDURES

2-17. PERFORMANCE TEST.

DESCRIPTION

This procedure covers:

- Channel A Sensitivity Test
- Channel B Sensitivity Test
- Channel C Sensitivity Test
- External Input Sensitivity Test
- Internal Output Level Test
- Minimum Time Interval Test
- External Arming Test
- Trigger Levels Test
- Internal Frequency Standard Accuracy Test

NOTE

- Performance test procedure steps should be done in the order given.
- Keep test equipment interconnecting cables as short as possible.
- A performance test checklist is provided at the end of the performance test procedures. Use the checklist while doing the test procedures.
- To guarantee specifications listed in Chapter 1, performance tests must be completed within the temperature range of +21°C to +25°C.
- Allow an initial 60 minute warm-up period when performing the first performance test to allow the Counter to stabilize.
- Allow Counter 5 minutes to stabilize if turned off less than five minutes during performance tests. Use STBY whenever possible.
- The initialized setup of Counter controls and indicators is to be performed prior to each performance test.

INITIALIZED SETUP.

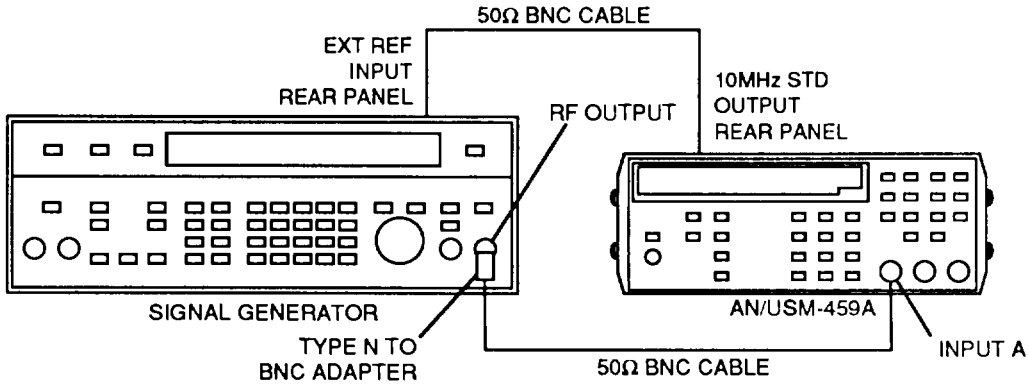
1. Initialization of Counter controls and indicators is accomplished by cycling the POWER ON/OFF switch from OFF to ON.

2. Initialized state of Counter should be as follows:

DISPLAY	00000000
Hz LED	ON
RESOLUTION LED	ON
FREQ A LED	ON
INPUT A ⎍ LED	ON
INPUT B ⎍ LED	ON
INPUT A TRIG LED	ON or OFF
INPUT B TRIG LED	ON or OFF
All other displays and indicators	OFF

CHANNEL A SENSITIVITY TEST.

1. Connect test equipment as shown.



2. On AN/USM-459A,

   .Cycle POWER ON/OFF switch from OFF to ON.

   .Select Input A to 50 Ω.

   .Set RESOLUTION to 8 digits (set without signal input).

3. Set Signal Generator controls as follows:

   .Frequency to 160 MHz.

   .Output level to 50 mVrms.

4. On AN/USM-459A verify GATE LED and Input A TRIG LED flash. Verify display reading is 160 MHz ±1 count.

5. Set Signal Generator and AN/USM-459A controls as shown. Verify AN/USM-459A conditions and readings are within specified limits.

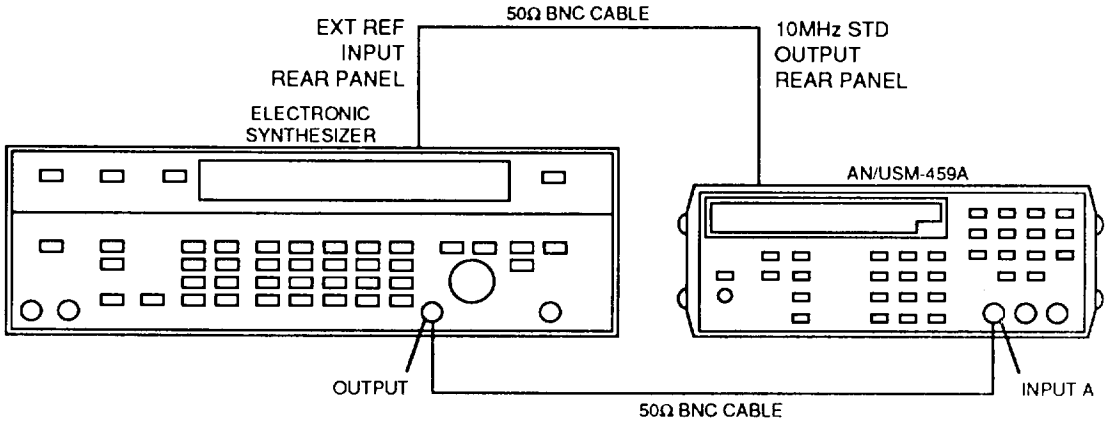
NOTE

Disconnect signal input when setting resolution.

Signal Generator		AN/USM-459A			
Frequency	Level	Resolution	GATE LED	A TRIG LED	Display
100 MHz	25 mVrms	8 Digits	Flashing	Flashing	100 MHz ± 1 count
10 MHz	25 mVrms	7 Digits	Flashing	Flashing	10 MHz ± 1 count

CHANNEL A SENSITIVITY TEST — Continued.

6. Connect test equipment as shown.



7. Set Electronic Synthesizer controls as follows:
   - Frequency to 100 kHz.
   - Output level to 25 mVrms.
8. On AN/USM-459A, set RESOLUTION to 5 digits (set without signal input). Verify GATE LED and Input A TRIG LED flash. Verify display reading is 100 kHz ± 1 count.
9. Set Electronic Synthesizer and AN/USM-459A controls as shown. Verify AN/USM-459A conditions and readings are within specified limits.

NOTE

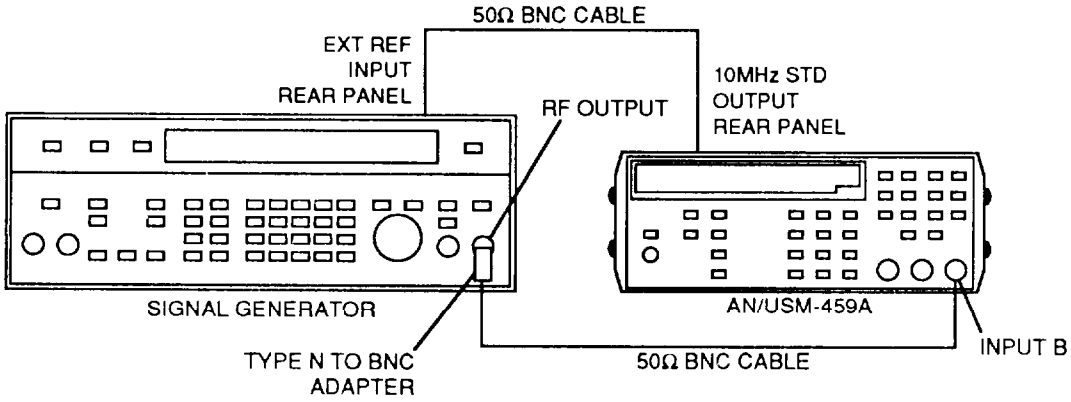
Disconnect signal input when setting resolution.

Electronic Synthesizer		AN/USM-459A			
Frequency	Level	Resolution	GATE LED	A TRIG LED	Display
5 kHz	25 mVrms	3 Digits	Flashing	Flashing	5 kHz ± 1 count
10 HZ	25 mVrms	3 Digits	Flashing	Flashing	10Hz ± 1 count

10. Disconnect test equipment.

CHANNEL B SENSITIVITY TEST.

1. Connect test equipment as shown.



CHANNEL B SENSITIVITY TEST — Continued

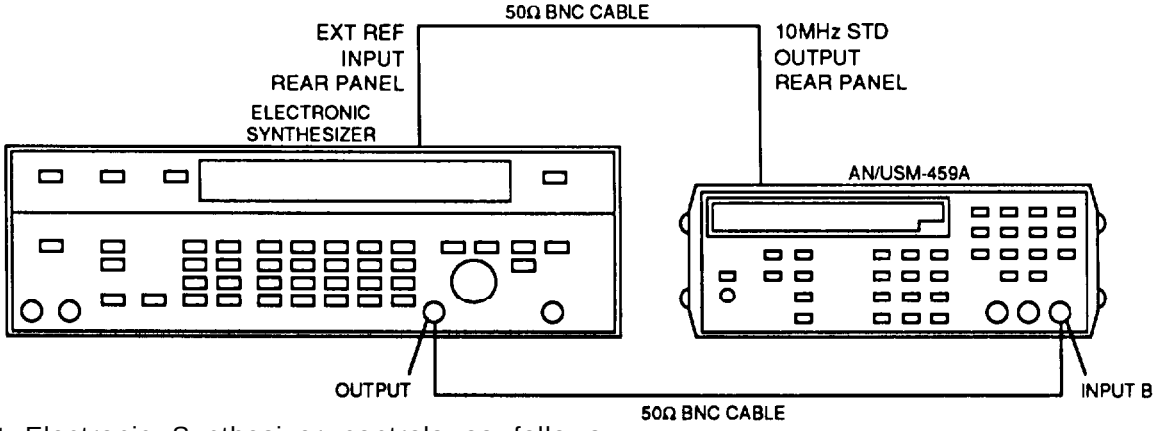
2. On AN/USM-459A,
   - Cycle POWER ON/OFF switch from OFF to ON,
   - Enter 21 using numeric keys.
   - Select SHIFT key (LED to ON).
   - Press STORE, then SF keys.
   - Select SHIFT, then SF keys (SF LED to ON),
   - Select Input B to 50 Ω.
   - Set RESOLUTION to 8 digits (set without signal input),
3. Set Signal Generator controls as follows:
   - Frequency to 100 MHz.
   - Output level to 25 mVrms.
4. On AN/USM-459A verify GATE LED and Input B TRIG LED flash. Verify display reading is 100MHz ± 1 count.
5. Set Signal Generator and AN/USM-459A controls as shown. Verify AN/USM-459A conditions and readings are within specified limits.

NOTE

Disconnect signal input when setting resolution.

Signal Generator		AN/USM-459A			
Frequency	Level	Resolution	GATE LED	B TRIG LED	Display
10 MHz	25 mVrms	7 Digits	Flashing	Flashing	10 MHz ± 1 count

6. Connect test equipment as shown



7. Set Electronic Synthesizer controls as follows:
   - Frequency to 100 kHz,
   - Output level to 25 mVrms.
8. On AN/USM-459A, set RESOLUTION to 5 digits (set without signal input). Verify GATE LED and Input B TRIG LED flash. Verify display reading is 100 kHz ± 1 count.

CHANNEL B SENSITIVITY TEST — Continued

9, Set Electronic Synthesizer and AN/USM-459A controls as shown. Verify AN/USM-459A conditions and readings are within specified limits.

NOTE

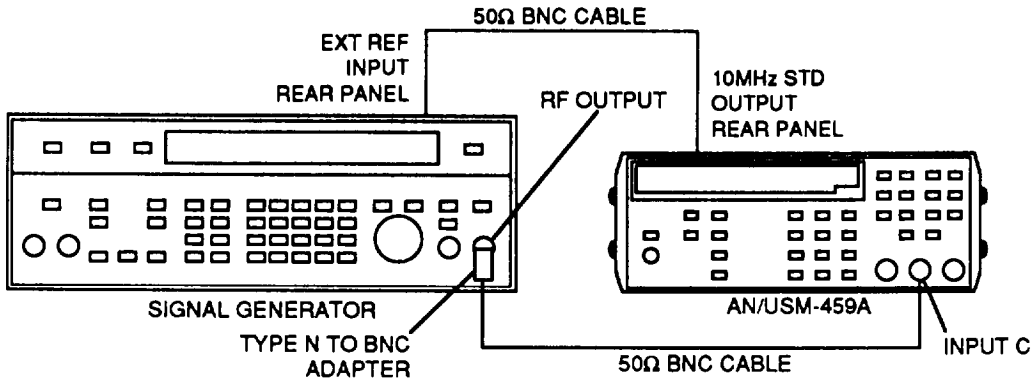
Disconnect signal input when setting resolution.

Electronic Synthesizer Frequency	Level	AN/USM-459A Resolution	GATE LED	B TRIG LED	Display
5 kHz	25 mVrms	3 Digits	Flashing	Flashing	5 kHz ± 1 count
10 Hz	25 mVrms	3 Digits	Flashing	Flashing	10 Hz ± 1 count

10. Disconnect test equipment,

CHANNEL C SENSITIVITY TEST.

1. Connect test equipment as shown,



2. On AN/USM-459A,
   - Cycle POWER ON/OFF switch from OFF to ON.
   - Select FREQ C using FUNCTION keys.
   - Set RESOLUTION to 9 digits (set without signal input).
3. Set Signal Generator controls as follows:
   - Frequency to 1.3 GHz.
   - Output level to 75 mVrms.
4. On AN/USM-459A verify GATE LED is flashing and display reading is 1.3 GHz ± 3 counts.

CHANNEL C SENSITIVITY TEST — Continued.

5. Set Signal Generator and AN/USM-459A controls as shown. Verify AN/USM-459A conditions and readings are within specified limits.

NOTE

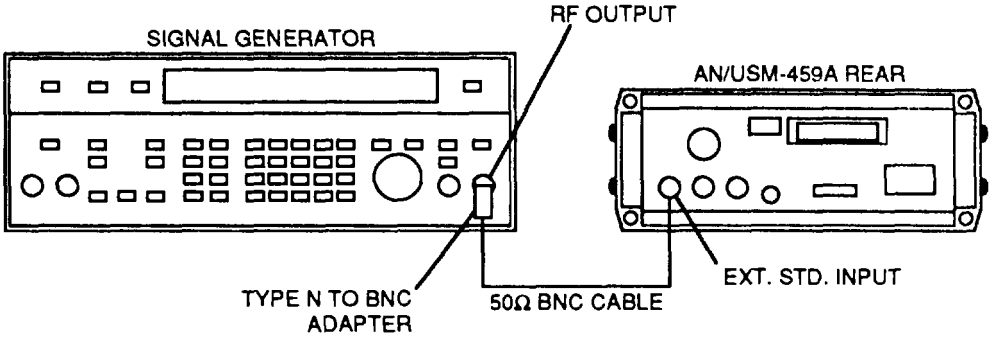
Disconnect signal input when setting resolution.

Signal Generator		AN/USM-459A		
Frequency	Level	Resolution	GATE LED	Display
1 GHz	15 mVrms	9 Digits	Flashing	1GHz ± 2 counts
500 MHz	15 mVrms	8 Digits	Flashing	500 MHz ± 1 count
100 MHz	15 mVrms	8 Digits	Flashing	100 MHz ± 1 count
40 MHz	15 mVrms	8 Digits	Flashing	40 MHz ± 1 count

6. Disconnect test equipment.

EXTERNAL INPUT SENSITIVITY TEST.

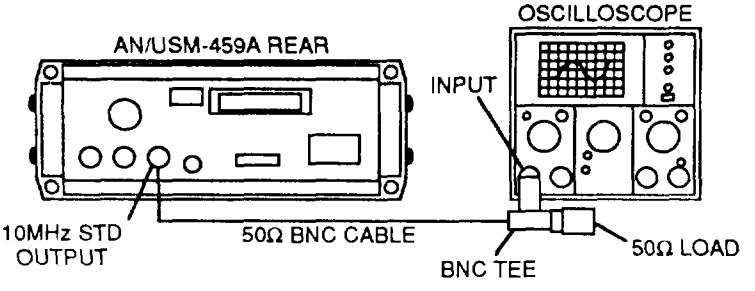
1. Connect test equipment as shown.



2. On AN/USM-459A, cycle POWER ON/OFF switch from OFF to ON.
3. Set Signal Generator controls as follows:
   - Frequency to 10 MHz.
   - Output level to 100 mVrms.
4. On AN/USM-459A verify EXT STD LED is ON (not flickering).
5. Disconnect test equipment.

INTERNAL OUTPUT LEVEL TEST.

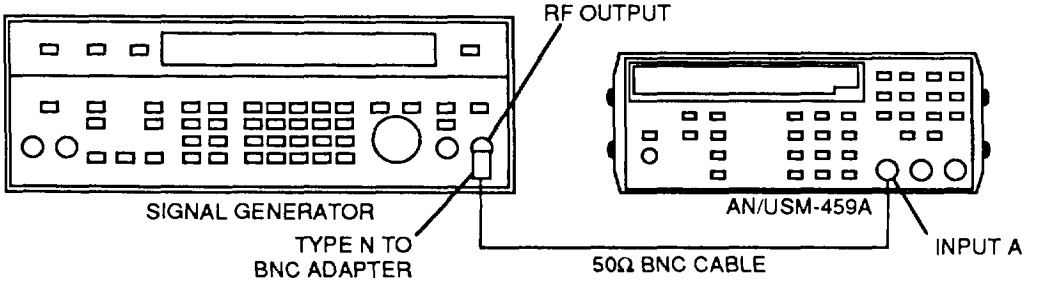
1. Connect test equipment as shown.



2. On AN/USM-459A, cycle POWER ON/OFF switch from OFF to ON.
3. Set Oscilloscope controls to display signal.
   - Verify display signal amplitude is ³ 600 mVp-p.
   - Verify display signal duty cycle is between 30%. and 70%.
4. Disconnect test equipment.

MINIMUM TIME INTERVAL TEST.

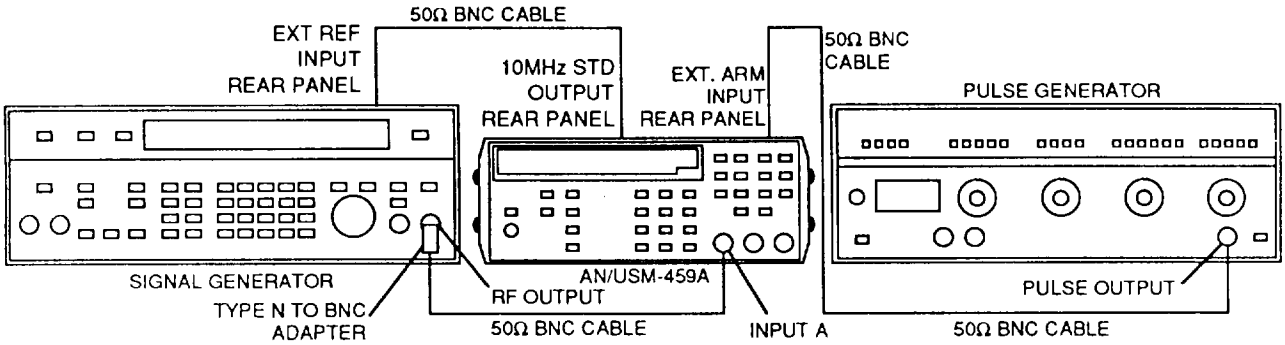
1. Connect test equipment as shown.



2. On AN/USM-459A,
   - Cycle POWER ON/OFF switch from OFF to ON.
   - Select Input A to 50 Ω.
   - Select TI A —> B using FUNCTION keys.
   - Select COM A (LED to ON).
3. Set Signal Generator controls as follows:
   - Frequency to 100 MHz,
   - Output level to 1 Vrms.
4. On AN/USM-459A, verify display reads 0 ± 2 nsec.
5. Disconnect test equipment.

EXTERNAL ARMING TEST.

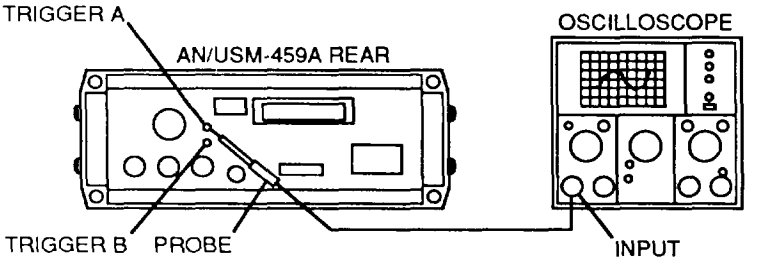
1. Connect test equipment as shown.



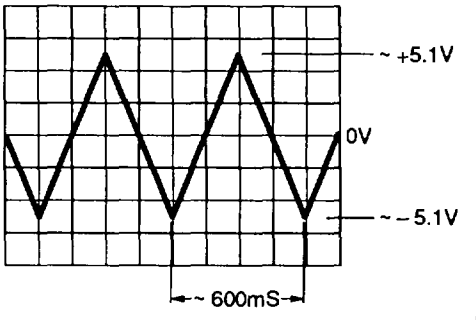
2. On AN/USM-459A,
   - Cycle POWER ON/OFF switch from OFF to ON.
   - Select Input A to 50Q.
   - Set RESOLUTION to 5 digits (set without signal input).
3. Set Signal Generator controls as follows:
   - Frequency to 10 MHz.
   - Output level to 200 mVrms.
4. Set Pulse Generator controls as follows:
   - Mode to single pulse.
   - Pulse width to 300 µsec.
   - Polarity to positive.
   - Pulse level to TTL (Low= 0V to +0.4V, High = +2.4 V to +5.OV)
5. On AN/USM-459A,
   - Enter 1 6 using numeric keys.
   - Select SHIFT key (LED to ON).
   - Press STORE, then SF keys.
   - Select SHIFT, then SF keys (SF LED to ON).
6. Set Pulse Generator to output one pulse.
7. On AN/USM-459A, verify display indicates 10.0000 E6 Hz ± one count and GATE LED is OFF.
8. On AN/USM-459A,
   - Enter 1 0 using numeric keys.
   - Select SHIFT key (LED to ON).
   - Press STORE, then SF keys.
   - Select SHIFT, then SF keys (S FLED to OFF).
9. Disconnect test equipment.

TRIGGER LEVELS TEST.

1. Connect test equipment as shown,



2. On AN/USM-459A,
   - Cycle PO WE RON/OFF switch from OFF to ON.
   - Select CHECK using FUNCTION keys.
   - Enter 7 6 using numeric keys.
   - Select SHIFT key (LED to ON).
   - Press STORE, then SF keys.
   - Select SHIFT, then SF keys (SF LED to ON).
   - Verify TRIG A and TRIG B LEDs are flashing.
3. Set Oscilloscope coupling to DC and other controls to display signal. Verify signal on Oscilloscope display is as shown.
4. Connect Oscilloscope probe to AN/USM-459A rear panel TRIGGER B output connector. Verify signal on Oscilloscope display is as shown.



5. On AN/USM-459A,
   - Enter 7 0 using numeric keys.
   - Select SHIFT key (L ED to ON).
   - Press STORE, then SF keys.
   - Select SHIFT, then SF keys (SF LED to OFF).
6. Disconnect Oscilloscope.
7. On AN/USM-459A,
   - On Input A, press TRIG LEVEL key, enter 5 using numeric key, then press TRIG LEVEL key.
   - On Input B, press TRIG LEVEL key, enter 5 using numeric key, then press TRIG LEVEL key.
8. Using a Digital Multi meter, verify AN/USM-459A rear panel TRIGGER A and B output connectors are +5 Vdc ±60 mVdc.
9. Repeat steps 7 and 8 using the AN/USM-459A values as shown, Verify Digital Multi meter readings are within specified limits.

AN/USM-459A Level		Digital Multi meter reading	
Input A	Input B	Trigger A	Trigger B
o	0	0V ± 10 mVdc	0V ± 10 mVdc
- 5	- 5	–5V ± 60 mVdc	–5V ± 60 mVdc

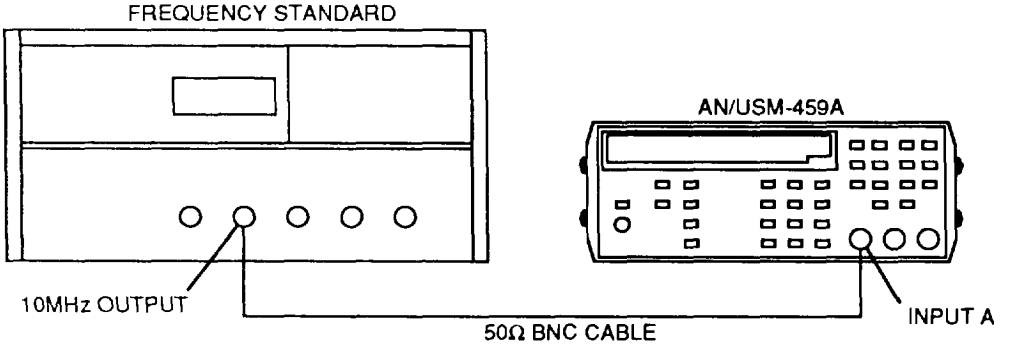
10. Disconnect test equipment.

INTERNAL FREQUENCY STANDARD ACCURACY TEST.

NOTE

Allow 72 hours of uninterrupted warm-up.

1. Connect test equipment as shown.



2. On AN/USM-459A,
   - Cycle POWER ON/OFF switch from OFF to ON.
   - Allow 72 hours uninterrupted warm-up.
   - Enter 1 0 using numeric keys.
   - Select SHIFT key (LED to ON).
   - . Press EXP key.
   - Enter 6 using numeric key.
   - Select SHIFT key (LED to ON).
   - Press STORE, then X keys.
   - Select SHIFT key (LED to ON).
   - Press RECALL, then X keys.
   - Verify display indicates 10.0000000 E6.
   - Press CONTINUE key.
   - Select SHIFT key (LED to ON).
   - Press R-X/Z key.
3. Set Frequency Standard output to 10 MHz.
4. On AN/USM-459A, verify display reads Ooo ± 300 E-3.
5. Disconnect test equipment.

PERFORMANCE TEST CHECKLIST.

Test and step		Measured value		Desired value
CHANNEL A SENSITIVITY TEST.				
160 MHz at 25 mV	Step 4	_____	MHz	160 MHz ± 1 count
100 MHz at 25 mV	Step 5	_____	MHz	100 MHz ± 1 count
10 MHz at 25 mV	Step 5	_____	MHz	10 MHz ± 1 count
100 kHz at 25 mV	Step 8	_____	kHz	100 kHz ± 1 count
5 kHz at 25 mV	Step 9	_____	kHz	5 kHz ± 1 count
10 Hz at 25 mV	Step 9	_____	Hz	10 Hz ± 1 count
CHANNEL B SENSITIVITY TEST.				
100 MHz at 25 mV	Step 4	_____	MHz	100 MHz ± 1 count
10 MHz at 25 mV	Step 5	_____	MHz	10 MHz ± 1 count
100 kHz at 25 mV	Step 8	_____	kHz	100 kHz ± 1 count
5 kHz at 25 mV	Step 9	_____	kHz	5 kHz ± 1 count
10 Hz at 25 mV	Step 9	_____	Hz	10 Hz ± 1 count
CHANNEL C SENSITIVITY TEST.				
1.3 GHz at 75 mV	Step 4	_____	GHz	1.3 GHz ± 3 count
1.0 GHz at 15 mV	Step 5	_____	GHz	1.0 GHz ± 2 counts
500 MHz at 15 mV	Step 5	_____	MHz	500 MHz ± 1 count
100 MHz at 15 mV	Step 5	_____	MHz	100 MHz ± 1 count
40 MHz at 15 mV	Step 5	_____	MHz	40 MHz ± 1 count
EXTERNAL INPUT SENSITIVITY TEST.				
10 MHz at 100 mV	Step 4	(√) _correct display		EXT STD LED ON
INTERNAL OUTPUT LEVEL TEST.				
	Step 3	_____	mVp-p	≥ 600 mVp-p
		_____	%	30% to 70%
MINIMUM TIME INTERVAL TEST.				
100 MHz at 1 V	Step 4	_____	nsec	–2 nsec to +2 nsec
EXTERNAL ARMING TEST.				
300µsec TTL	Step 7	_____	Hz	9.9999E6 Hz to 10.0001E6 Hz

PERFORMANCE TEST CHECKLIST,

Test and step		Measured value	Desired value
TRIGGER LEVELS TEST.			
Trigger A	Step 3	(√) _correct waveform	≈ 10.2 Vp-p at ≈2 Hz
Trigger B	Step 4	(√) _correct waveform	≈ 10.2 Vp-p at ≈2 Hz
Trigger A, + 5 V	Step 8	_____ Vdc	+4.94 to +5.06 Vdc
Trigger B, + 5 V	Step 8	_____ Vdc	+4.94 to +5.06 Vdc
Trigger A, O V	Step 9	_____ mVdc	–10 to +10 mVdc
Trigger B, O V	Step 9	_____ mVdc	–10 to +10 mVdc
Trigger A, – 5 V	Step 9	_____ Vdc	+4.94 to +5.06 Vdc
Trigger B, + 5 V	Step 9	_____ Vdc	+4.94 to +5.06 Vdc
INTERNAL FREQUENCY STANDARD ACCURACY TEST.			
10 MHz	Step 4	_____ count	$-300E^{-3}$ to +300 E^{-3}

2-18. ADJUSTMENTS.

DESCRIPTION

The adjustment procedures cover:

Adjust Channel A Input (para 2-20

Adjust Channel B Input (para 2-21

Adjust Channel C Input (para 2-22

Adjust Internal Frequency Standard (para 2-23).

NOTE

- Specific adjustments may be necessary after repair/replacement of specific assemblies in the Counter or failure of a performance test, Adjustment is not required if malfunction has been cleared after repair.
- Never perform all adjustments from para 2-20 thru 2-23 at one time.
- The adjustment needed after repair/replacement of specific assemblies are as shown in table 2-2.
- To guarantee specifications listed in Chapter 1, adjustments must be completed within the temperature range of +21°C to +25°C.
- Use rear panel for all ground connections unless otherwise specified.
- All indications and waveforms are referenced to chassis ground unless otherwise specified.
- All voltages specified as RMS unless otherwise specified,
- Assembly and cable location diagram is figure FO-1. Individual circuit card component locator diagrams are on figures FO-2 thru FO-6.
- After adjust procedure is completed remove power and install top and bottom covers (para 2-24).

Table 2-2. Post Repair/Replace Adjustments.

Repaired/Replaced Assembly	Adjust
Al Motherboard Circuit Card Assembly	Adjust Channel A Input (para 2-20). Adjust Channel B Input (para 2-21).
A2 Display Circuit Card Assembly	None.
A3 Output Circuit Card Assembly	None.
A4 Channel C Prescaler CCA	Adjust Channel C Input (para 2-22).
A5 Oscillator Assembly	Adjust Internal Frequency Standard (para 2-23).
A6 GPIB Circuit Card Assembly	None.

2-19. INITIAL SETUP

1. Remove two screws and rear bezel (para 2-24).

NOTE

Keep the top cover in place during the procedures except when necessary to make an internal connection or adjustment.

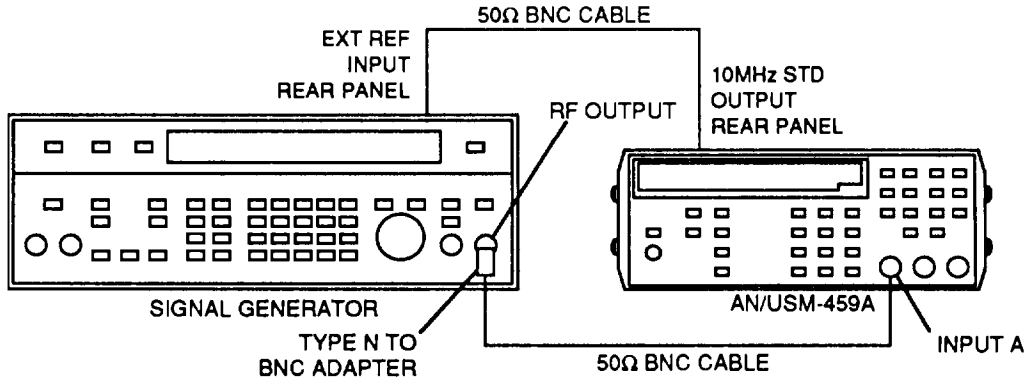
2. Perform turn-on procedures TM 11-6625-3232-12, paragraph 2-6.

W A R N I N G

Dangerous voltages are present with the covers removed. Where maintenance can be performed without power applied, the power should be removed.

2-20. ADJUST CHANNEL A INPUT.

1. On AN/USM-459A,
   - Set A1R149 (fig. FO-2, sheet 1) fully CCW.
   - Set A1R192 to its mid-point.
   - Select FREQ A using FUNCTION keys.
   - Select Input A to 50 Ω.
   - Set RESOLUTION to 3 digits (set without signal input).
2. Connect test equipment as shown.



3. Set Signal Generator controls as follows:
   - Frequency to 100 MHz.
   - Output level to 3.0 mVrms.

2-20. ADJUST CHANNEL A INPUT — Continued.

4. On AN/USM-459A,
   - Adjust A1R192 to obtain a stable reading of 100.0 ± 0.1 E6 with GATE and Input A TRIG LEDs flashing,

NOTE

Adjustment of A1R192 will cause random displays to occur on both sides of the correct position.

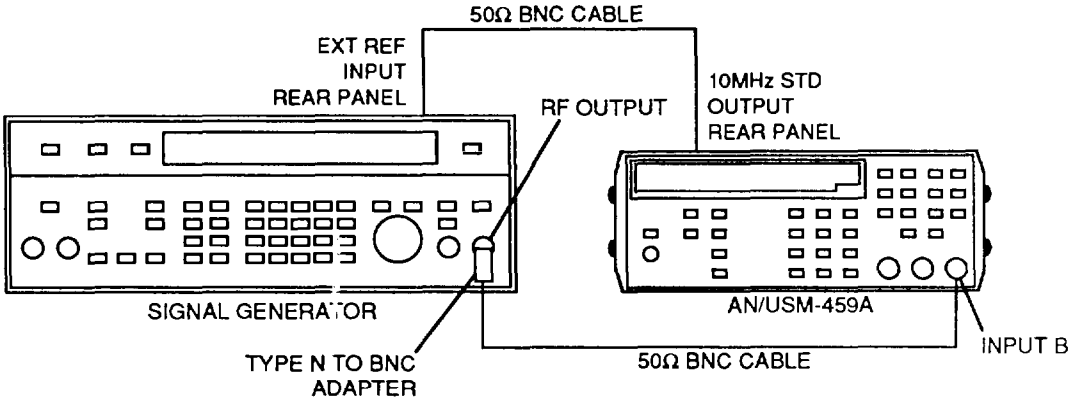
5. Disconnect input and verify that the display indicates 100.0 ±0.1E6 without GATE LED flashing,
   - If incorrect, repeat steps 1 through 4.
   - If correct, proceed with step 6.
6. On AN/USM-459A,
   - Disconnect signal to Input A connector.
   - Press CONTINUE key.
   - Set RESOLUTION to 8 digits (set without signal input).
   - Reconnect signal to Input A connector.
7. Set Signal Generator output level to 13.0 mVrms.
8. On AN/USM-459A,
   - SLOWLY adjust A1R149 CW until display just becomes unstable.
   - Readjust A1R149 CCW SLOWLY until display stabilizes and indicates 100.000000±.000001 E6.
9. Set Signal Generator output level to 7.0 mVrms.
10. On AN/USM-459A, verify GATE LED is not flashing.
    - If incorrect, repeat steps 7 through 10.
11. Remove power and disconnect test equipment. Install top cover (para 2-24).

2-21. ADJUST CHANNEL B INPUT.

1. On AN/USM-459A,
   - Set A1R150 (fig. FO-2, sheet 1) fully CCW.
   - Set A1R193 to its mid-point.
   - Select FREQ A using FUNCTION keys.
   - Select Input B to 50 Ω.
   - Set RESOLUTION to 3 digits (set without signal input).
   - Enter 2 1 using numeric keys.
   - Select SHIFT key (LED to ON).
   - Press STORE, then SF keys.
   - Select SHIFT, then SF keys (SF LED to ON),

2-21. ADJUST CHANNEL B INPUT — Continued.

2. Connect test equipment as shown.



3. Set Signal Generator controls as follows:
   - Frequency to 100 MHz.
   - Output level to 3.0 mVrms.
4. On AN/USM-459A,
   - Adjust A1R193 to obtain a stable reading of 100.0 ± 0.1 E6 with GATE and input B TRIG LEDs flashing.

NOTE

Adjustment of A1R193 will cause random displays to occur on both sides of the correct position.

5. Disconnect input and verify that the display indicates 100.0 ±0.1E6 without GATE LED flashing.
   - If incorrect, repeat steps 1 through 4.
   - If correct, proceed with step 6.
6. On AN/USM-459A,
   - Disconnect signal to Input B connector.
   - Press CONTINUE key.
   - Set RESOLUTION to 8 digits (set without signal input).
   - Reconnect signal to Input B connector.
7. Set Signal Generator output level to 13.0 mVrms.
8. On AN/USM-459A,
   - SLOWLY adjust A1R150 CW until display just becomes unstable.
   - Readjust A1R150 CCW SLOWLY until display stabilizes and indicates 100.000000*.000001 E6.
9. Set Signal Generator output level to 7.0 mVrms.
10. On AN/USM-459A, verify GATE LED is not flashing.
    - If incorrect, repeat steps 7 through 10.

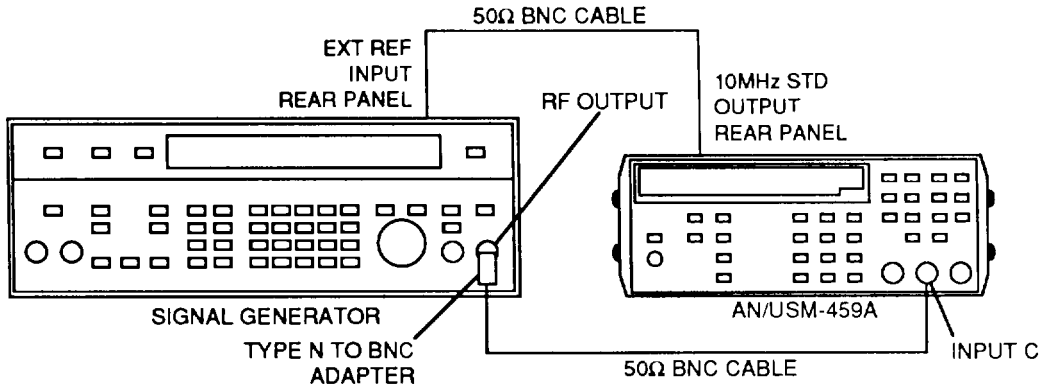
2-21. ADJUST CHANNEL B INPUT — Continued.

11. On AN/USM-459A,
    - Enter 20 using numeric keys.
    - Select SHIFT key (LED to ON).
    - Press STORE, then SF keys.
    - Select SHIFT, then SF keys (SF LED to OFF).
12. Remove power and disconnect test equipment. Install top cover (para 2-24).

2-22. ADJUST CHANNEL C INPUT.

---

1. On AN/USM-459A,
    - Set A4R27 (fig. FO-5) fully CW.
    - Select FREQ C using FUNCTION keys.
2. Connect test equipment as shown.



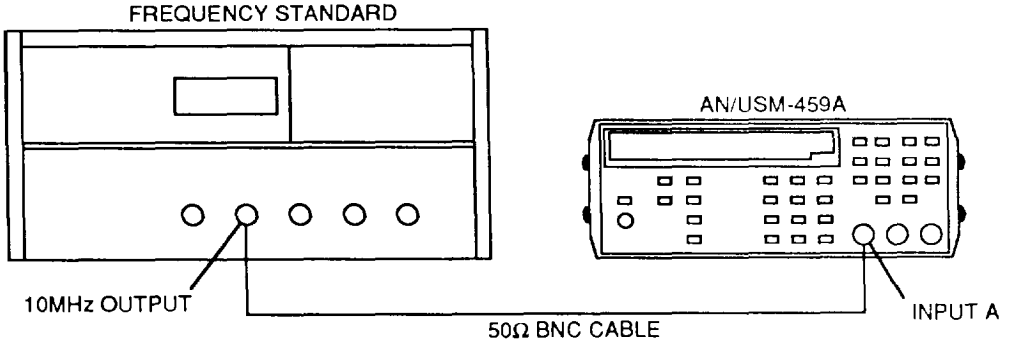
3. Set Signal Generator controls as follows:
    - Frequency to 1.0 GHz.
    - Output level to 8.0 mVrms.
4. On AN/USM-459A,
    - Adjust A4R27 CCW to obtain a stable reading of 1000.00000 ±.00001 E6 with GATE LED flashing.
5. Set Signal Generator output level to 7.0 mVrms.
6. On AN/USM-459A, verify GATE LED is not flashing.
    - If incorrect, repeat steps 3 through 6.
7. Remove power and disconnect test equipment. Install top cover (para 2-24).

2-23. ADJUST INTERNAL FREQUENCY STANDARD.

NOTE

Allow 72 hours of uninterrupted warm-up before making adjustment.

1. Connect test equipment as shown.



2. On AN/USM-459A,
   - Select FREQ A using FUNCTION keys.
   - Enter 1 0 using numeric keys.
   - Select SHIFT key (LED to ON).
   - Press EXP key.
   - Enter 6 using numeric key.
   - Select SHIFT key (LED to ON).
   - Press STORE, then X keys.
   - Select SHIFT key (LED to ON).
   - Press RECALL, then X keys.
   - Verify display indicates 10.0000000 E6.
   - Press CONTINUE key.
   - Select SHIFT key (LED to ON).
   - Press R-X/Z key.
3. On AN/USM-459A, verify display reads 0 ± 10 E-3.
   - If incorrect, adjust rear panel FREQUENCY STD ADJUST FINE control until reading is within specified limits.

NOTE

If COARSE adjustment is necessary, repeat adjustment procedure from beginning.

4. Remove power and disconnect test equipment. Install top cover (para 2-24).

2-24. REPLACE TOP AND BOTTOM COVERS.

DESCRIPTION

This procedure covers: Remove. Install.

INITIAL SETUP

W A R N I N G

Dangerous voltages are present with covers removed.

NOTE

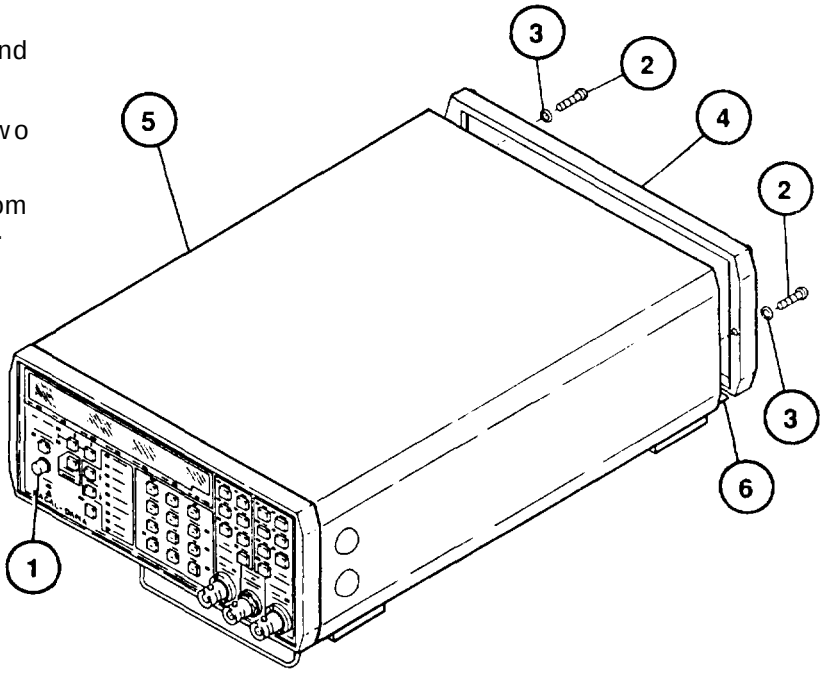
Task the same for both covers.

REMOVE

1. Set POWER switch (1) to off and remove AC power cable.
2. Remove two screws (2), two washers (3) and rear bezel (4).
3. Slide top cover (5) and/or bottom cover (6) toward rear and remove.

INSTALL

1. Install top cover (5) and/or bottom cover (6) and slide forward.
2. Install rear bezel (4).
3. Install two washers (3) and two screws (2).
4. Reconnect AC power cable and set POWER switch (1) to ON.



END OF TASK

2-25. REPLACE BOTTOM FEET.

DESCRIPTION

This procedure covers: Remove, Install.

INITIAL SETUP

NOTE

PRELIMINARY PROCEDURES:

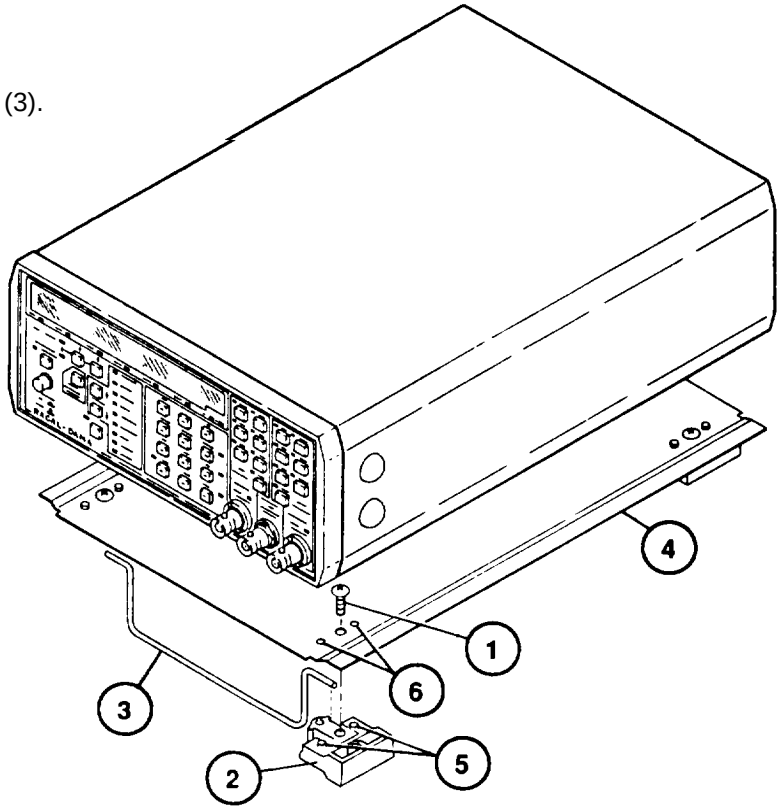
- Remove bottom cover (para 2-24).
- Task the same for all feet and only one is shown.

REMOVE

1. Remove screw (1).
2. Remove bottom foot (2) and stand (3).

NOTE

Stand only used on front feet,



INSTALL

1. If installing front foot, place stand (3) into foot (2).
2. Install foot (2) on bottom cover (4) so keys (5) are aligned with key holes (6).
3. Install screw (1).

NOTE

FOLLOW-ON MAINTENANCE:

- Install bottom cover (para 2-24).

END OF TASK

2-26. REPLACE FRONT PANEL ASSEMBLY.

DESCRIPTION

This procedure covers: Remove. Install.

INITIAL SETUP

NOTE

PRELIMINARY PROCEDURES:

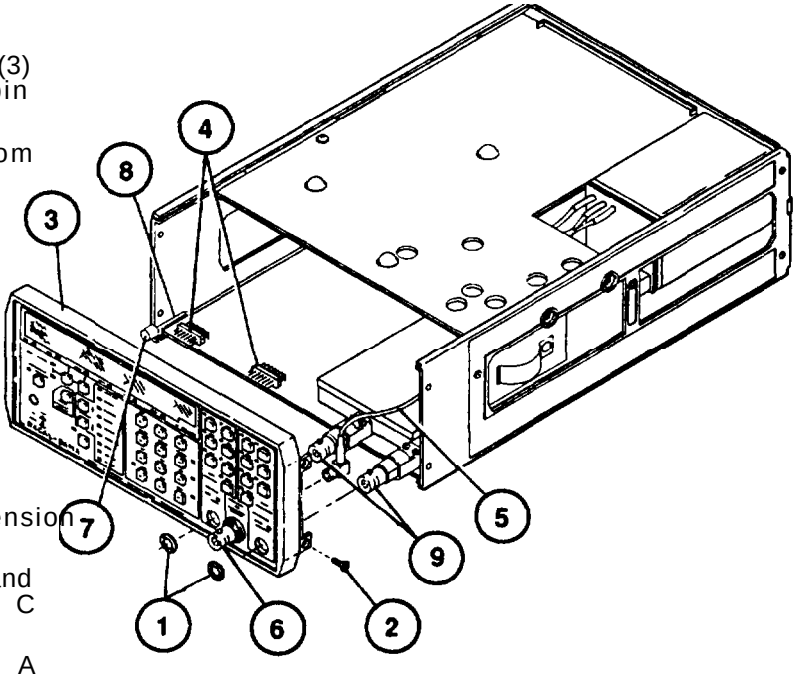
- Remove top and bottom covers (para 2-24).

REMOVE

1. Remove two nuts (1).
2. Remove four screws (2).
3. Carefully pull front panel assembly (3) forward to disconnect two 14 pin connectors (4).
4. Disconnect coaxial cable (5) from Input C connector (6).
5. Remove front panel assembly (3).

NOTE

ON/OFF knob (7) may stay in front panel or remain on extension shaft (8).



INSTALL

1. Install ON/OFF knob (7) on extension shaft (8).
2. Position front panel assembly (3) and reconnect coaxial cable (5) to Input C connector (6).
3. Install front panel assembly (3) so A and B input connectors (9) and ON/OFF knob (7) are through holes.
4. Align 14 pin connectors (4) and press front panel assembly (3) into place,
5. Install four screws (2).
6. Install two nuts (1).

NOTE

FOLLOW-ON MAINTENANCE:

- Install top and bottom covers (para 2-24).

END OF TASK

2-27. REPLACE REAR PANEL ASSEMBLY.

DESCRIPTION

This procedure covers: Remove. Install.

INITIAL SETUP

NOTE

PRELIMINARY PROCEDURES:

- Remove voltage selection card (para 3-9 in TM 11-6625-3232-12).
- Remove top and bottom covers (para 2-24).
- Remove A5 Oscillator Assembly (para 2-32).

REMOVE

1. Remove two screws (1) and lockwashers (2).
2. Remove four screws (3) and washers (4).
3. Carefully pull rear panel assembly (5) toward rear to disconnect two four pin connectors (6).
4. Remove nut (8), lockwasher (7), and bridge diode (9),
5. Remove nut (10) and green/yellow wire (11).
6. Remove rear panel assembly (5).

INSTALL

1. Position rear panel assembly (5) behind Counter and install green/yellow wire (11) and nut (10).
2. Install bridge diode (9) on stud (12). Install lockwasher (7) and nut (8),
3. Position rear panel assembly (5) so four pin connectors (6), and GPIB connector (13) are aligned and press into place,
4. Install four washers (4) and screws (3).
5. Install two lockwashers (2) and screws (1).

NOTE

FOLLOW-ON MAINTENANCE:

- Install voltage selection card (para 3-9 in TM 11-6625-3232-12).
- Install A5 Oscillator Assembly (para 2-32).
- Install top and bottom covers (para 2-24).

END OF TASK

2-28. REPLACE A1 MOTHERBOARD CIRCUIT CARD ASSEMBLY.

DESCRIPTION

This procedure covers: Remove. Install.

INITIAL SETUP

NOTE

PRELIMINARY PROCEDURES:

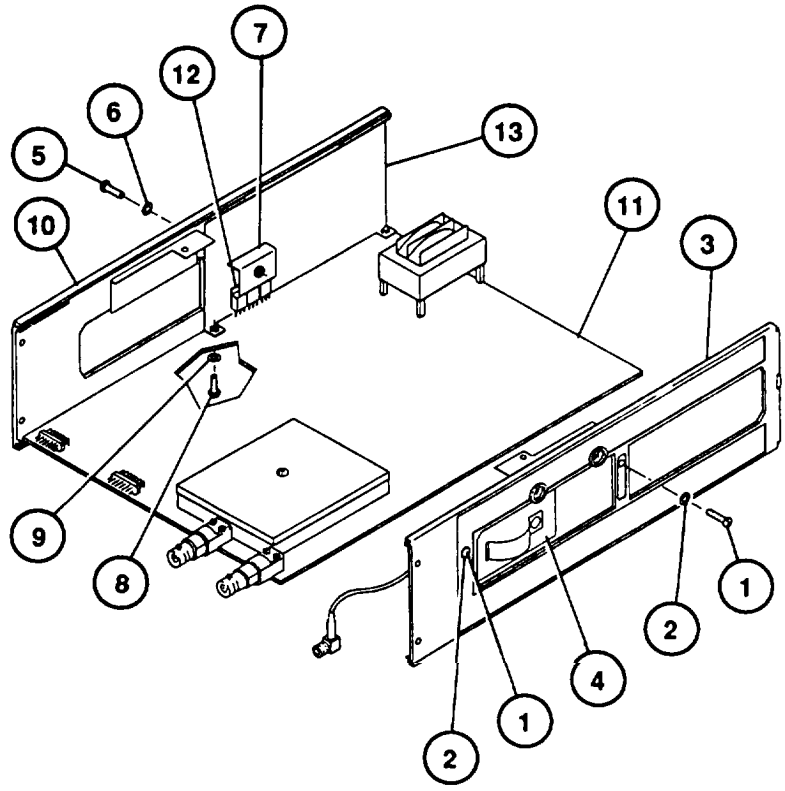
- Remove top and bottom covers (para 2-24).
- Remove Front Panel Assembly (para 2-26).
- Remove A5 Oscillator Assembly (para 2-32).
- Remove A6 GP-IB Circuit Card Assembly (para 2-33).
- Remove Rear Panel Assembly (para 2-27).

REMOVE

1. Remove two screws (1) and lockwashers (2).
2. Remove right-side frame (3) and A4 Channel C Prescaler Circuit Card Assembly (4).
3. Remove screw (5), washer (6), and transistor retainer (7).
4. Remove two screws (8), washers (9), and left side frame (10).

INSTALL

1. Position A1 Motherboard Circuit Card Assembly (11) on left side frame (10).
2. Install two washers (9) and screws (8).
3. Verify three insulators (12) are in place on heats ink (13) and install transistor retainer (7), washer (6), and screw (5).
4. Install A4 Channel C Prescaler Circuit Card Assembly (4) and right side frame (3).
5. Install two lockwashers (2) and scre



FOLLOW-ON MAINTENANCE:

- Install Front Panel Assembly (para 2-26).
- Install Rear Panel Assembly (para 2-27).
- Install A5 Oscillator Assembly (para 2-32).
- Install A6 GP-IB Circuit Card Assembly (para 2-33).
- Install top and bottom covers (para 2-24).

END OF TASK

2-29. REPLACE A2 DISPLAY CIRCUIT CARD ASSEMBLY.

DESCRIPTION

This procedure covers: Remove. Install.

INITIAL SETUP

NOTE

PRELIMINARY PROCEDURES:

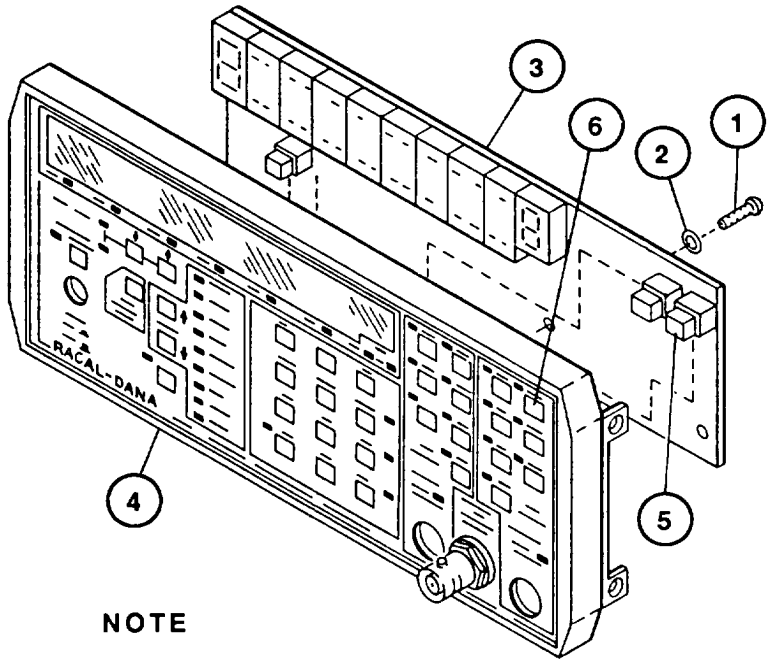
- Remove top and bottom covers (para 2-24).
- Remove Front Panel Assembly (para 2-26).

REMOVE

1. Remove three screws (1) and lockwashers (2).
2. Remove A2 Display Circuit Card Assembly (3).

INSTALL

1. Position A2 Display Circuit Card Assembly (3) into front panel (4) so all keys (5) are through proper hole (6).
2. Install three lockwashers (2) and screws (l).
3. Make sure all keys (5) move freely.



NOTE

FOLLOW-ON MAINTENANCE:

- Install Front Panel Assembly (para 2-26).
- Install top and bottom covers (para 2-24).

END OF TASK

2-30. REPLACE A3 OUTPUT CONNECTOR CIRCUIT CARD ASSEMBLY.

DESCRIPTION

This procedure covers: Remove. Install.

INITIAL SETUP

NOTE

PRELIMINARY PROCEDURES:

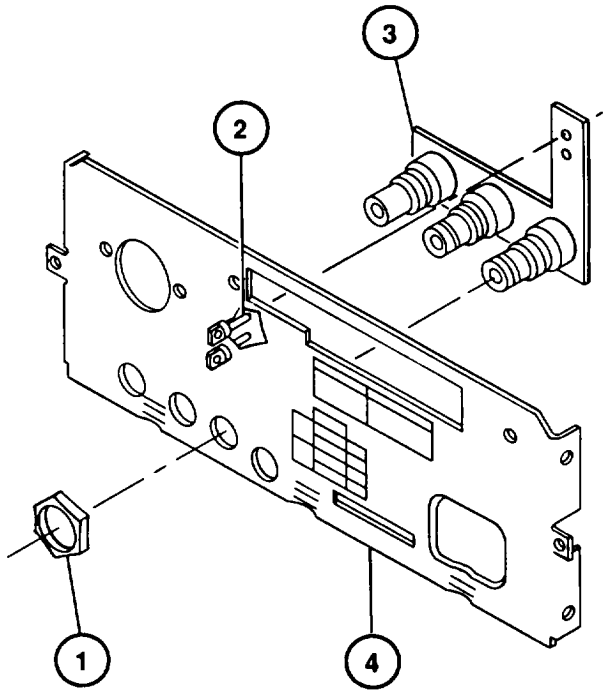
- Remove top and bottom covers (para 2-24).
- Remove A5 Oscillator Assembly (para 2-32).
- Remove Rear Panel Assembly (para 2-27).

REMOVE

1. Remove three nuts (1).
2. Unsolder two terminals (2).
3. Remove A3 Output Connector Circuit Card Assembly (3).

INSTALL

1. Position A3 Output Connector Circuit Card Assembly (3) through holes on rear panel assembly (4).
2. Install three nuts (1).
3. Resolder two terminals (2).



NOTE

FOLLOW-ON MAINTENANCE:

- Install Rear Panel Assembly (para 2-27).
- Install A5 Oscillator Assembly (para 2-32).
- Install top and bottom covers (para 2-24).

END OF TASK

2-31. REPLACE A4 CHANNEL C PRESCALER CIRCUIT CARD ASSEMBLY.

DESCRIPTION

This procedure covers: Remove. Install.

INITIAL SETUP

NOTE

PRELIMINARY PROCEDURES:

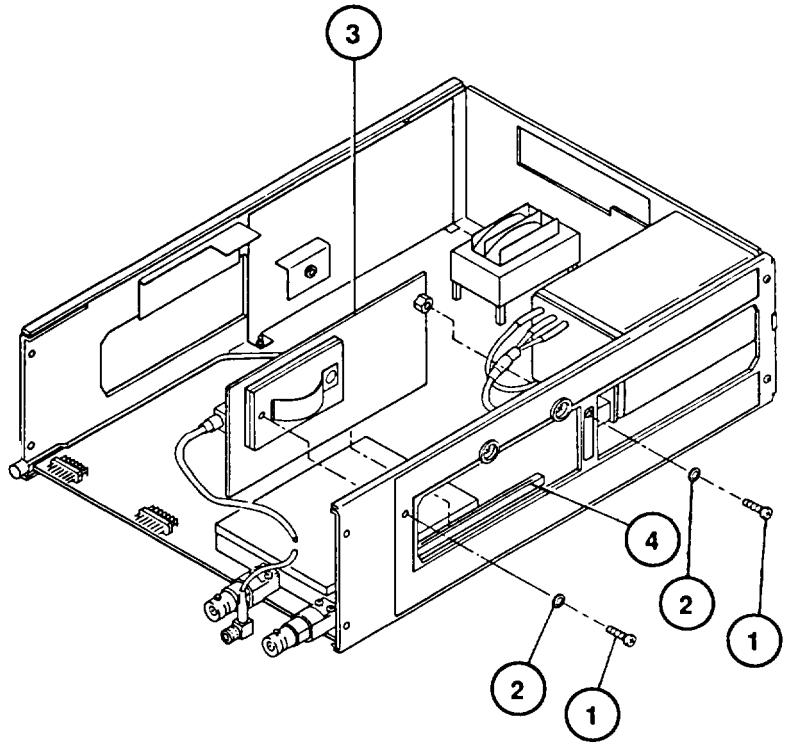
- Remove top and bottom covers (para 2-24).
- Remove A6 GP-IB Circuit Card Assembly (para 2-33).
- Remove Front Panel Assembly (para 2-26).

REMOVE

1. Remove two screws (1) and lockwashers (2).
2. Remove A4 Channel C Prescaler Circuit Card Assembly (3).

INSTALL

1. Position A4 Channel C Prescaler Circuit Card Assembly (3) in Counter and align 30 pin connector (4). Press into place.
2. Install two lockwashers (2) and screws (1).



NOTE

FOLLOW-ON MAINTENANCE:

- Install Front Panel Assembly (para 2-26).
- Install A6 GP-IB Circuit Card Assembly (para 2-33),
- Install top and bottom covers (para 2-24).

END OF TASK

2-32. REPLACE A5 OSCILLATOR ASSEMBLY.

DESCRIPTION

This procedure covers: Remove. Install.

INITIAL SETUP

NOTE

PRELIMINARY PROCEDURES:

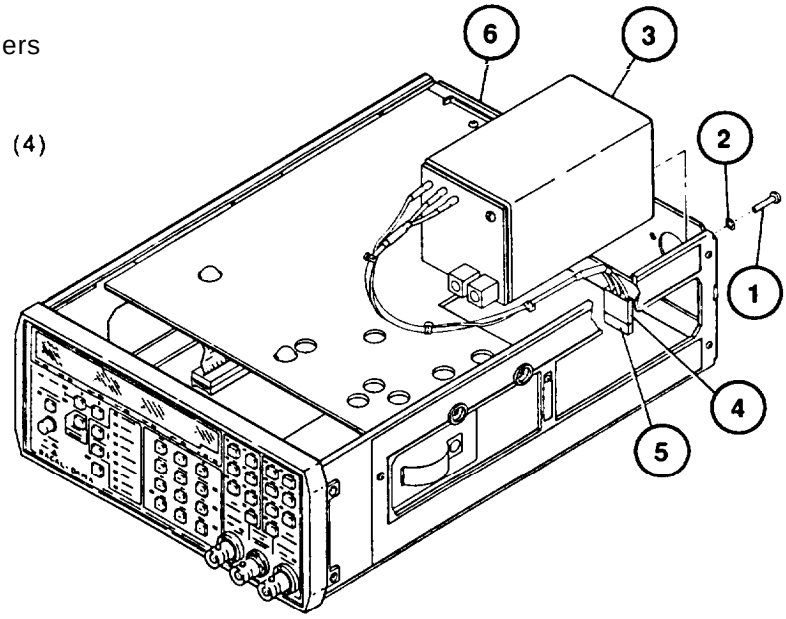
- Remove top cover (para 2-24).

REMOVE

1. Remove two screws (1) and washers (2).
2. Remove A5 Oscillator Assembly (3).
3. Disconnect three conductor cable (4) from PL14 (5).

INSTALL

1. Position A5 Oscillator Assembly (3) inside Counter and reconnect three conductor cable (4) to PL14 (5).
2. Position A5 Oscillator Assembly (3) in place on rear panel assembly (6) and install two washers (2) and screws (1).



NOTE

FOLLOW-ON MAINTENANCE:

- Install top cover (para 2-24).

END OF TASK

2-33. REPLACE A6 GPIB CIRCUIT CARD ASSEMBLY.

DESCRIPTION

This procedure covers: Remove. Install.

INITIAL SETUP

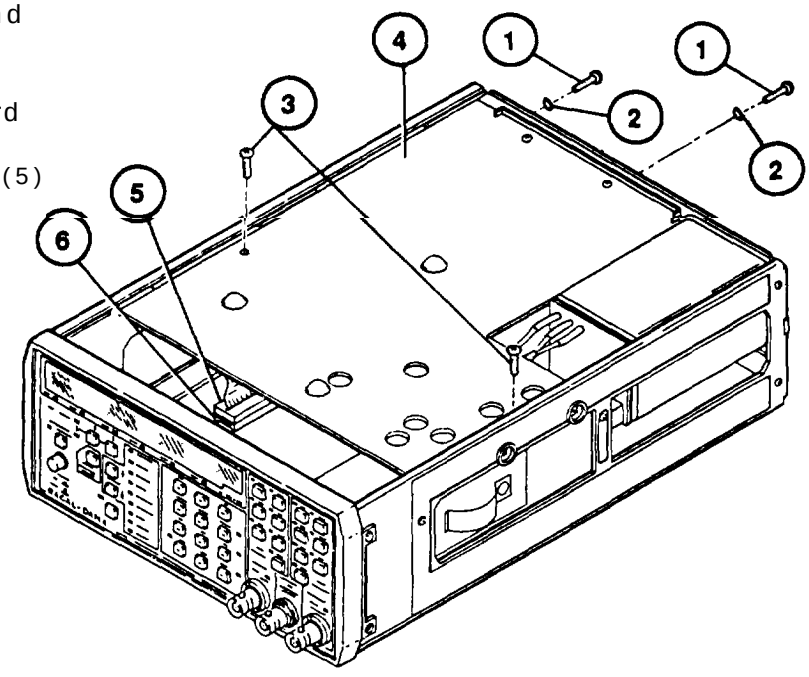
NOTE

PRELIMINARY PROCEDURES:

- Remove top cover (para 2-24).

REMOVE

1. Remove two screws (1) and lockwashers (2).
2. Remove two screws (3).
3. Remove A6 GPIB Circuit Card Assembly (4).
4. Disconnect 28 pin ribbon cab (5) from SK4 (6).



INSTALL

1. Position A6 GPIB Circuit Card Assembly (4) inside Counter and reconnect 28 pin ribbon cable (5) to SK4 (6).
2. Position A6 GPIB Circuit Card Assembly (4) in place and install two screws (3).
3. Install two lockwashers (2) and screws (1).

NOTE

FOLLOW-ON MAINTENANCE:

- Install top cover (para 2-24).

END OF TASK

Section V. PREPARATION FOR STORAGE OR SHIPMENT

2-34. PACKAGING.

Package Counter in original shipping container. When using packing materials other than the original, use the following guidelines:

- Wrap Counter in non-static generating plastic packing material.
- Use double-wall cardboard shipping container.
- Protect all sides with shock-absorbing material to prevent Counter movement within the container.
- Seal the shipping container with approved sealing tape
- Mark “FRAGILE” on all sides, top, and bottom of shipping container.

2-35. TYPES OF STORAGE.

- Short-Term (administrative) = 1 to 45 days.
- Intermediate = 46 to 180 days
- Long term = over 180 days. After long term storage, perform turn-on procedure (TM 11-6625-3232-12, para 2-6). If this procedure fails, perform troubleshooting procedures (table 2-l).

2-36. ENVIRONMENT.

The Counter should be stored in a clean, dry environment. In high humidity environments, protect the Counter from temperature variations that could cause internal condensation. The following environmental conditions apply to both shipping and storage:

Temperature	-40° C to + 70°C (-40° F to +158° F)
Relative Humidity (sea level)	less than 95% at +30°C
Altitude	less than 12,000 meters (39,370 feet)
Vibration	less than 2g
Shock	less than 30 g

APPENDIX A
REFERENCES

A-1. SCOPE.

This appendix lists all forms, field manuals, technical manuals, and miscellaneous publication references in this manual.

A-2. FORMS.

Equipment Inspection and Maintenance Worksheet.....DA Form 2404

Product Quality Deficiency Report.....SF 368

Recommended Changes to Equipment Technical Publications..... DA Form 2028-2

Recommended Changes to Publications and Blank Forms .....DA Form 2028

Report of Discrepancy (ROD).....SF 364

Transportation Discrepancy Report (TDR).....SF 361

A-3. TECHNICAL MANUALS.

Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command) ..... TM 750-244-2

Operator's, and Unit Maintenance Manual for Digital Electronic Counter AN/USM-459A (NSN 6625-01-271-3012) (EIC: QVH).....TM 11-6625-3232-12

Unit, Intermediate, Direct Support Maintenance Repair Parts and Special Tools List, for Digital Electronic Counter AN/USM-459A (NSN 6625-01-271-3012).....TM 11-6625-3232-24P

A-4. MISCELLANEOUS PUBLICATIONS.

Abbreviations for Use of Drawings, Specifications, Standards and in Technical Documents..... MIL-STD-12

Consolidated Index of Army Publications and Blank Forms.....DA Pam 25-30

Common Table of Allowances, Expendable/Durable Items (Except Medical, Class V, Repair Parts, and Heraldic Items)..... CTA 50-970

First Aid ..... FM 4-25.11

Interactive Electronic Technical Manual (IETM) for Calibration and Repair Requirements for the Maintenance of Army Materiel .....TB 43-180

Reporting of Item and Packaging Discrepancies..... AR 735-11-2

The Army Maintenance Management System (TAMMS) Users Manual.... DA Pam 750-8

Safety Requirements for Maintenance of Electrical and Electronic Equipment..... TB 385-4

APPENDIX B
EXPENDABLE SUPPLIES AND MATERIALS LIST

Section I. INTRODUCTION

B-1. SCOPE.

This appendix lists expendable supplies you will need for maintenance on the Test Set. These items are authorized to you by CTA 50-970, Expendable items (Except Medical, Class V, Repair Parts and Heraldic Items).

B-2. EXPLANATION OF COLUMNS.

a. Column (1) – Item Number. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material (e.g., "Use cleaning compound, item 5, App. B").

b. Column (2) - Level. This column identifies the lowest level of maintenance that requires the listed item.

C - Operator/Crew

O - Unit Maintenance

H - General Support Maintenance

c. Column (3) - National Stock Number. This column indicates the National Stock Number assigned to the item and is used for requisitioning purposes.

d. Column (4) - Description. This column indicates the Federal item name and, if required, a minimum description to identify the item. The last line for each item gives the FSCM (in parentheses) followed by the part number.

e. Column (5) – Unit of Measure (U/M). This column indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., EA, IN, PR). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that satisfies your requirements.

Section II. EXPENDABLE SUPPLIES AND MATERIALS LIST

(1) ITEM NUMBER	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION	(5) U/M
1	O	6810-01-382-2904	Isopropyl Alcohol, Technical 8 oz Can, ASTM D 770	CN
2	C	8305-00-267-3015	Cloth, Cheesecloth, Cotton, Lintless, CCC-C-440, Type II, Class 2 (81349)	YD
3	C		Detergent, Mild, Liquid	OZ
4	H	6850-01-409-2602	Circuit Cooler, Freezing Compound, 10 oz Can, P/N MCC-FR2	CN

GLOSSARY

Section I. ABBREVIATIONS

GPIA . . . . . General Purpose Interface Adaptor
GPIB . . . . . General Purpose Interface Bus
I/P . . . . . Input
LSD . . . . . Least Significant Digit
O/P . . . . . output
SF . . . . . Special Function

Section II. DEFINITION OF UNUSUAL TERMS

Least Significant Digit (LSD)

In frequency and period modes, display automatically upranges at 1.1 x decade and downranges at 1.05 x decade, except on Input C for input frequency >1 GHz.

Trigger Error

Calculated as follows (seconds):

$$\sqrt{\frac{(e_{i1}^2 + e_{n1}^2)}{S1^2} + \frac{(e_{i2}^2 + e_{n2}^2)}{S2^2}}$$

where ei = input amplifier RMS noise
en = input signal RMS noise in 160 MHz bandwidth
S = Slew rate at trigger point V/s
Suffix 1 denotes START edge
Suffix 2 denotes STOP edge

Trigger Level Timing Error

Calculated as follows (seconds):

$$0.035 \left(\frac{1}{S1} - \frac{1}{S2} \right)$$

where S1 = Slew rate on START edge V/s
S2 = Slew rate on STOP edge V/s

INDEX

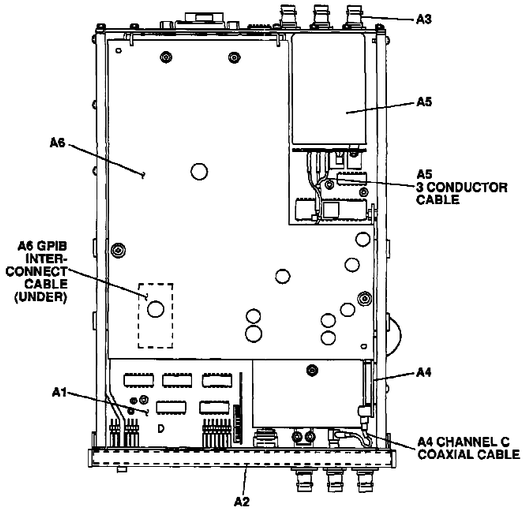
INDEX — Continued

INDEX — Continued

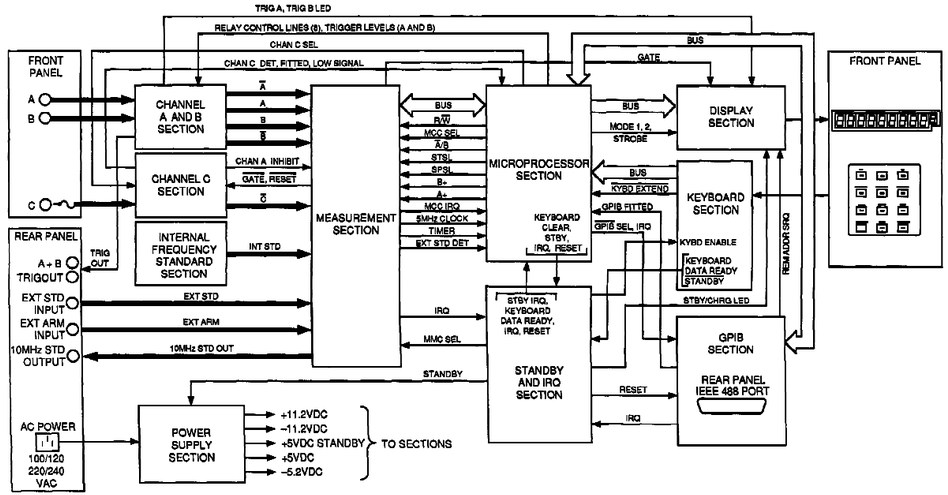
INDEX — Continued

INDEX — Continued

INDEX — Continued



ASSEMBLY AND CABLE LOCATOR, TOP VIEW



FUNCTIONAL BLOCK DIAGRAM

CE1ZS013

Figure FO-1. AN/USM-459A Assembly and Cable Locator, and Functional Block Diagram.

NOTES:

1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A1 TO ABBREVIATION FOR COMPLETE REFERENCE DESIGNATOR.

2. COMPONENT REFERENCE DESIGNATORS PRINTED ON CIRCUIT CARD DO NOT MATCH PRINCIPLES OF OPERATION, COMPONENT LOCATOR, OR SCHEMATIC DIAGRAM IN MANUAL. THE FOLLOWING IS A LIST OF AFFECTED PARTS:

ON CCA	IN MANUAL	COMPONENT
D-	CR-	DIODE
E-	U-	MICROCIRCUIT
I-	DS-	LED
P-	P-	CONNECTOR
RK-	K-	RELAY
SK-	J-	CONNECTOR

3. UNLESS OTHERWISE SPECIFIED:
RESISTANCE IS IN OHMS
CAPACITANCE IS IN MICROFARADS
INDUCTANCE IS IN MICROHENRIES

4. UNLESS OTHERWISE SPECIFIED ALL VOLTAGE READINGS AND WAVEFORMS REFERENCED TO CHASSIS GROUND.

5. NORMAL POSITION OF LK-1 IS A1P16 PINS 8 AND 9.

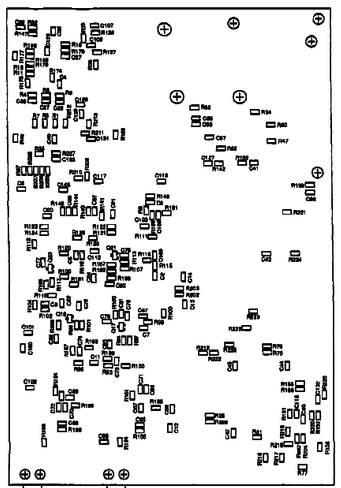
6. NORMAL POSITION OF LK-4 IS A1P16 PINS 2 AND 3.

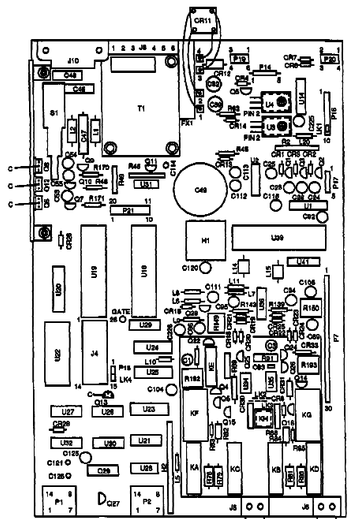
7. POSITION OF VOLTAGE SELECTION CARD IS AS FOLLOWS:

VOLTAGE	SHORTED
100 VAC	PINS 1 - 2, 3 - 4, 5 - 6.
120 VAC	PINS 1 - 2, 3 - 4 - 5.
220 VAC	PINS 2 - 3, 5 - 6.
240 VAC	PINS 2 - 3, 4 - 5.

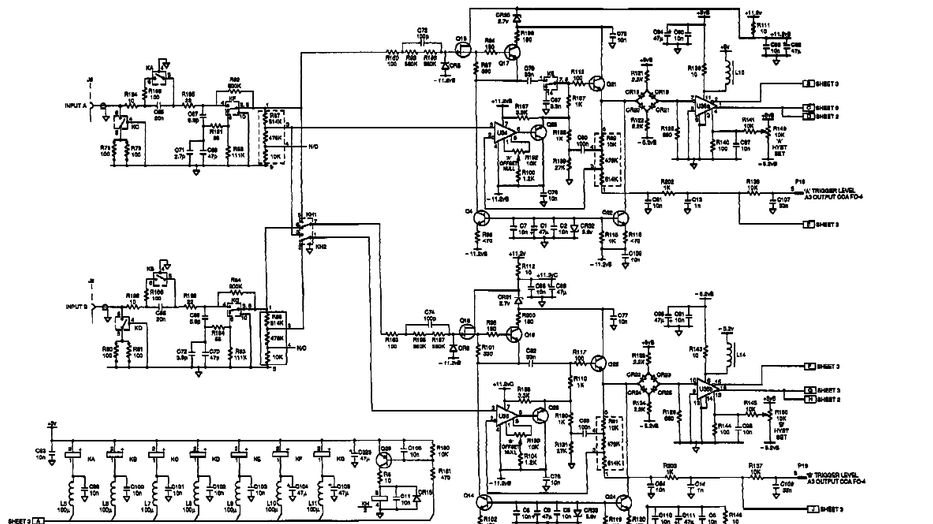
8. ALL RELAYS DRAWN DE-ENERGIZED.

A1 COMPONENT LOCATOR, BOTTOM VIEW



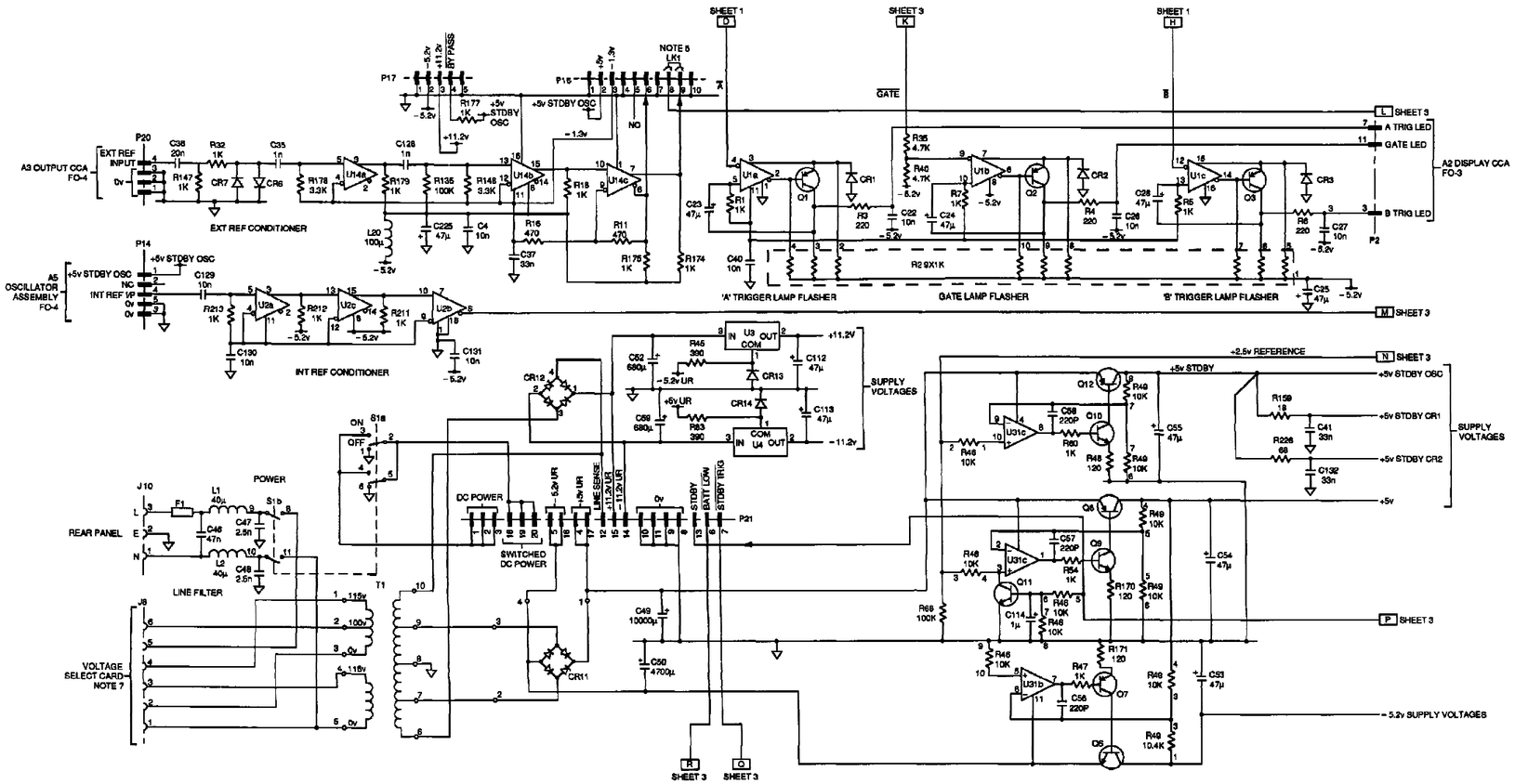


A1 COMPONENT LOCATOR, TOP VIEW



CE1Z8014

Figure FO-2. A1 Motherboard Circuit Card Assembly Component Locator, and Schematic Diagram (Sheet 1 of 3).



CE1ZS015

Figure FO-2. A1 Motherboard Circuit Card Assembly Component Locator, and Schematic Diagram (Sheet 2 of 3).

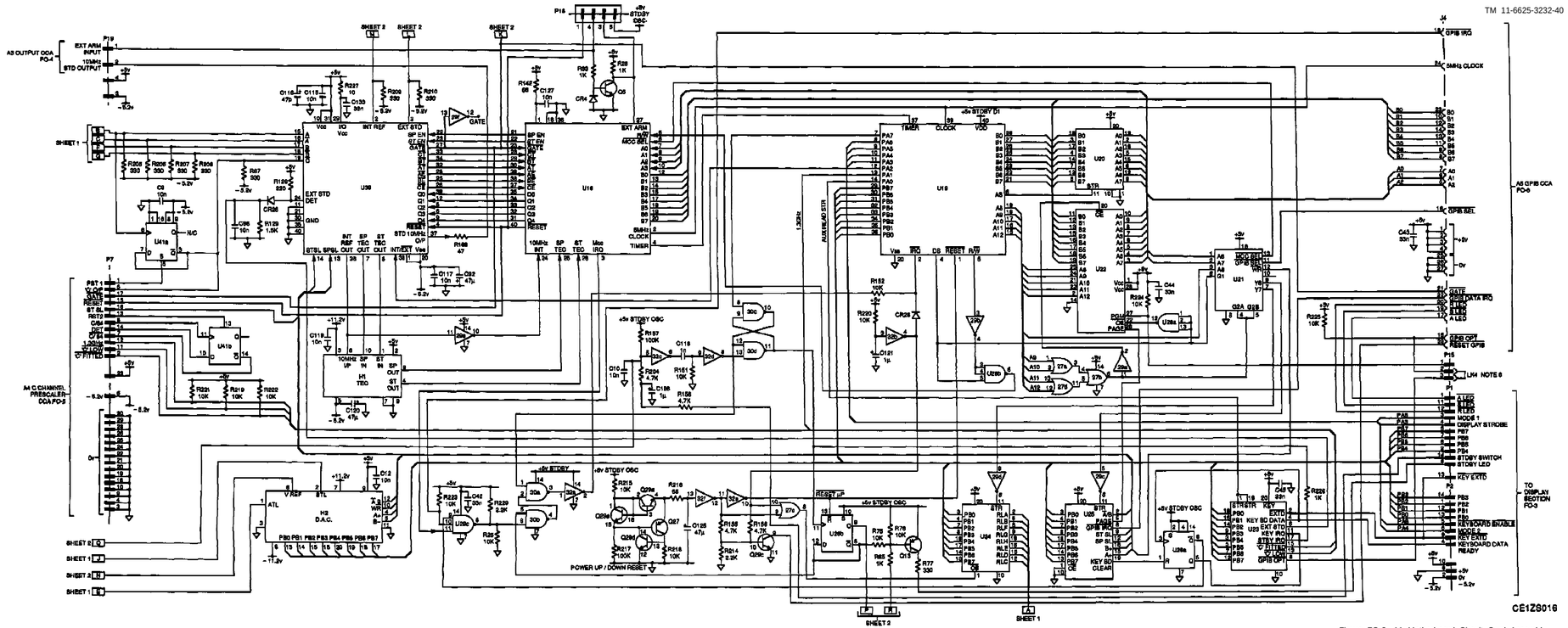


Figure FO-2. A1 Motherboard Circuit Card Assembly Component Locator, and Schematic Diagram (Sheet 3 of 3).

NOTES:

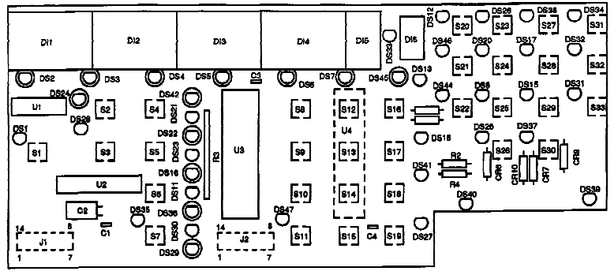
1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A2 TO ABBREVIATION FOR COMPLETE REFERENCE DESIGNATOR.

2. SOME OF THE COMPONENT REFERENCE DESIGNATORS PRINTED ON CIRCUIT CARD DO NOT MATCH PRINCIPLES OF OPERATION, COMPONENT LOCATOR, OR FUNCTIONAL BLOCK DIAGRAM IN MANUAL. THE FOLLOWING IS A LIST OF AFFECTED PARTS:

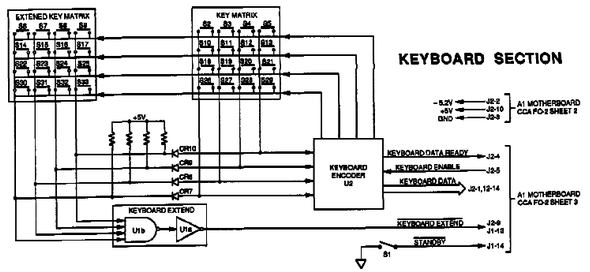
ON CCA	IN MANUAL	COMPONENT
D-	CR-	DIODE
IC-	U-	MICROCIRCUIT
LP-	DS-	LED
PL-	P-	CONNECTOR
RL-	K-	RELAY
SK-	J-	CONNECTOR

3. UNLESS OTHERWISE SPECIFIED:
RESISTANCE IS IN OHMS
CAPACITANCE IS IN MICROFARADS
INDUCTANCE IS IN MICROHENRIES

4. UNLESS OTHERWISE SPECIFIED ALL VOLTAGE READINGS AND WAVEFORMS REFERENCED TO CHASSIS GROUND.



A2 COMPONENT LOCATOR, FRONT VIEW



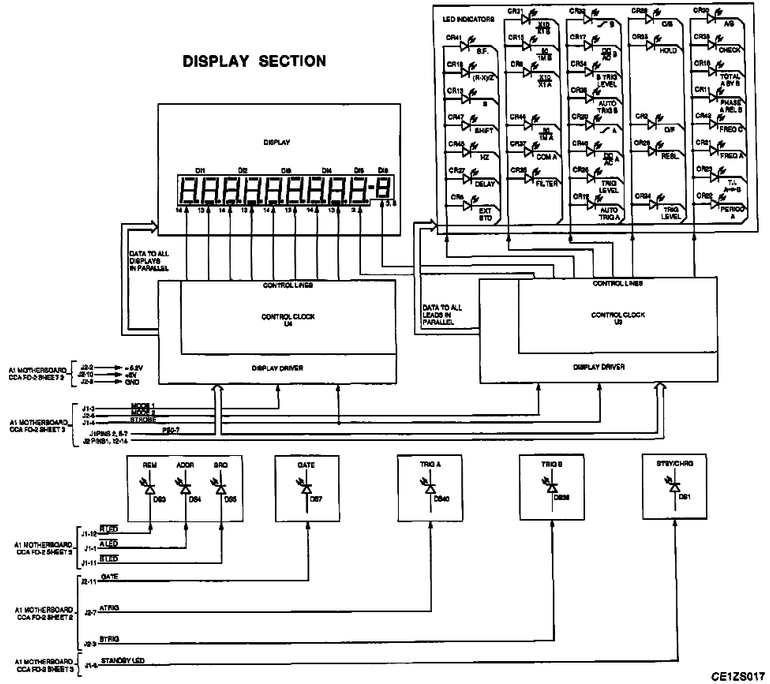


Figure FO-3. A2 Display Circuit Card Assembly Component Locator, and Functional Block Diagram.

NOTES:

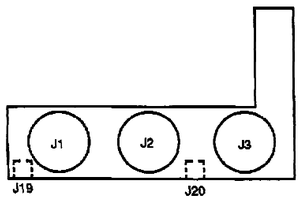
1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A3, A5, or A5A1 TO ABBREVIATION FOR COMPLETE REFERENCE DESIGNATOR.

2. SOME OF THE COMPONENT REFERENCE DESIGNATORS PRINTED ON CIRCUIT CARD DO NOT MATCH PRINCIPLES OF OPERATION, COMPONENT LOCATOR, OR FUNCTIONAL BLOCK DIAGRAM IN MANUAL. THE FOLLOWING IS A LIST OF AFFECTED PARTS:

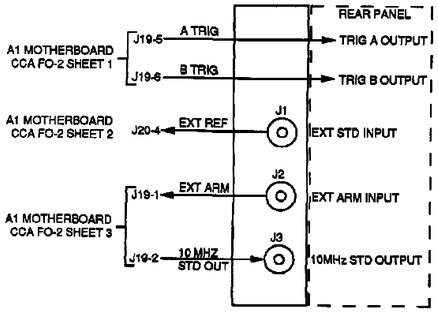
ON CCA	IN MANUAL	COMPONENT
D-	CR-	DIODE
IC-	U-	MICROCIRCUIT
LP-	DS-	LED
PL-	P-	CONNECTOR
RL-	K-	RELAY
SK-	J-	CONNECTOR

3. UNLESS OTHERWISE SPECIFIED:
RESISTANCE IS IN OHMS
CAPACITANCE IS IN MICROFARADS
INDUCTANCE IS IN MICROHENRIES

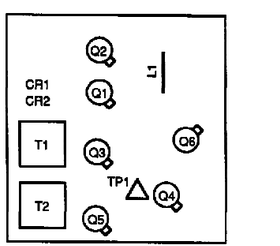
4. UNLESS OTHERWISE SPECIFIED ALL VOLTAGE READINGS AND WAVEFORMS REFERENCED TO CHASSIS GROUND.



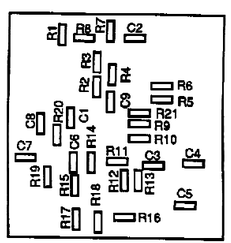
A3 COMPONENT LOCATOR



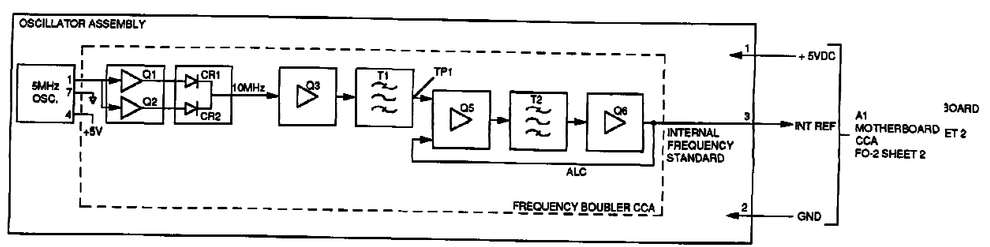
A3 FUNCTIONAL BLOCK DIAGRAM



A5 COMPONENT LOCATOR, FRONT VIEW



A5 COMPONENT LOCATOR, REAR VIEW



A5 FUNCTIONAL BLOCK DIAGRAM

CE1ZS018

Figure FO-4. A3 Output Circuit Card Assembly and A5 Oscillator Component Locator, and Functional Block Diagram.

NOTES:

1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A4 TO ABBREVIATION FOR COMPLETE REFERENCE DESIGNATOR.

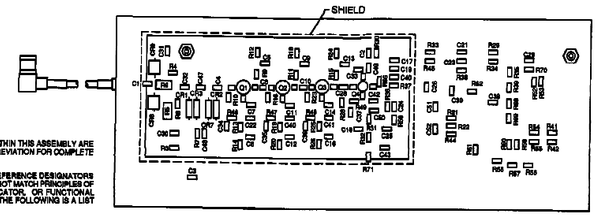
2. SOME OF THE COMPONENT REFERENCE DESIGNATORS PRINTED ON CIRCUIT CARD DO NOT MATCH PRINCIPLES OF OPERATION, COMPONENT LOCATOR, OR FUNCTIONAL BLOCK DIAGRAM IN MANUAL. THE FOLLOWING IS A LIST OF AFFECTED PARTS:

ON CCA	IN MANUAL	COMPONENT
CR-	CR-	DIODE
U-	U-	MICROCIRCUIT
LI-	DS-	LED
P1-	P-	CONNECTOR
K1-	K-	RELAY
J1-	J-	CONNECTOR

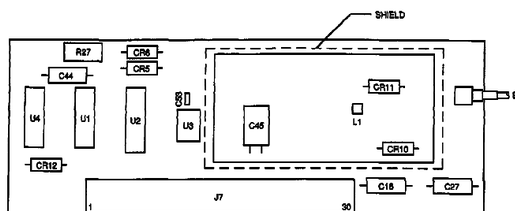
3. UNLESS OTHERWISE SPECIFIED:
RESISTANCE IS IN OHMS
CAPACITANCE IS IN MICROFARADS
INDUCTANCE IS IN MICROHENRIES

4. UNLESS OTHERWISE SPECIFIED ALL VOLTAGE READINGS AND WAVEFORMS REFERENCED TO CHASSIS GROUND.

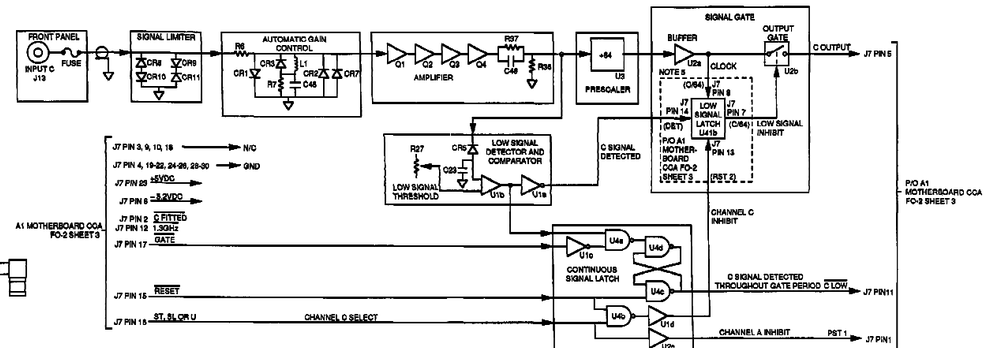
5. PHYSICALLY LOCATED ON A1 MOTHERBOARD CCA. ADD A1 TO ABBREVIATION FOR COMPLETE REFERENCE DESIGNATOR.



A4 COMPONENT LOCATOR, REAR VIEW



A4 COMPONENT LOCATOR, FRONT VIEW



CE1Z6019

Figure FO-5. A4 Channel C Prescaler Circuit Card Assembly Component Locator, and Functional Block Diagram.

NOTES:

1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A6 TO ABBREVIATION FOR COMPLETE REFERENCE DESIGNATOR.

2. SOME OF THE COMPONENT REFERENCE DESIGNATORS PRINTED ON CIRCUIT CARD DO NOT MATCH PRINCIPLES OF OPERATION, COMPONENT LOCATOR, OR FUNCTIONAL BLOCK DIAGRAM IN MANUAL. THE FOLLOWING IS A LIST OF AFFECTED PARTS:

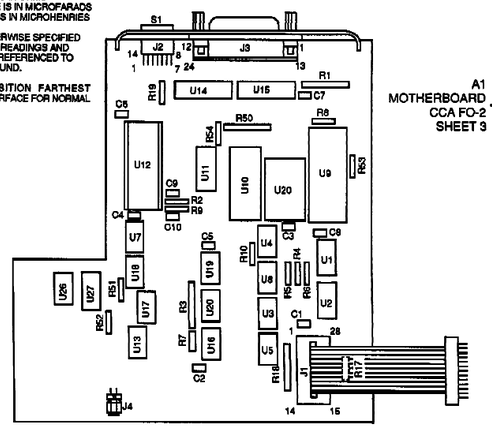
ON CCA	IN MANUAL	COMPONENT
D-	CR-	DIODE
IC-	U-	MICROCIRCUIT
LP-	DS-	LED
PL-	P-	CONNECTOR
RL-	K-	RELAY
SK-	J-	CONNECTOR

3. UNLESS OTHERWISE SPECIFIED:
RESISTANCE IS IN OHMS
CAPACITANCE IS IN MICROFARADS
INDUCTANCE IS IN MICROHENRIES

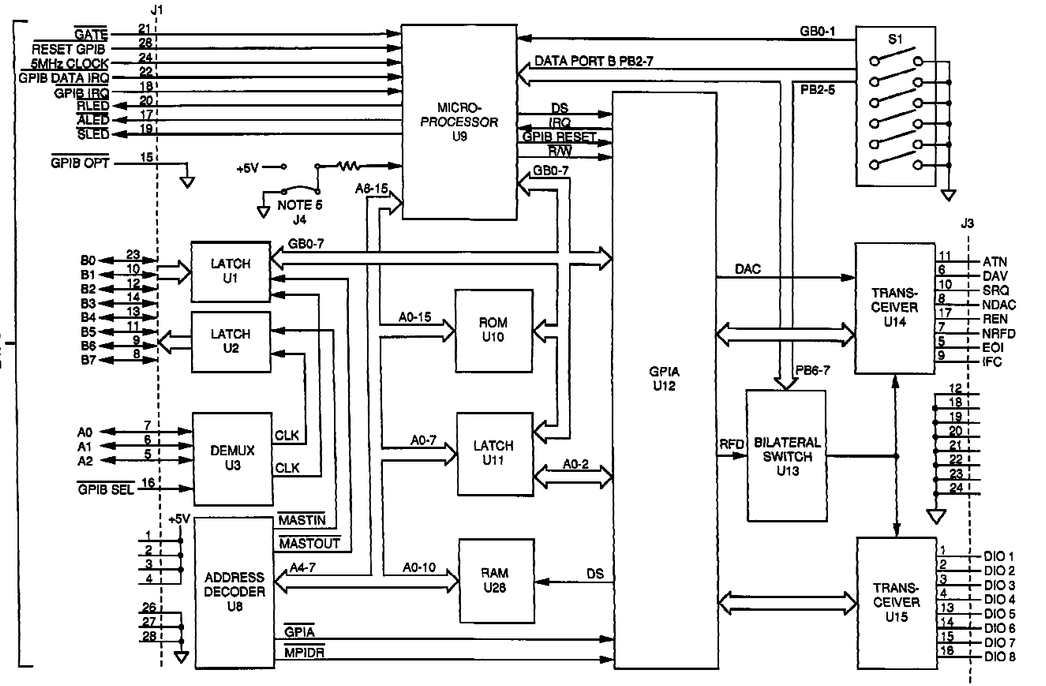
4. UNLESS OTHERWISE SPECIFIED ALL VOLTAGE READINGS AND WAVEFORMS REFERENCED TO CHASSIS GROUND.

5. JUMPER POSITION FARTHEST FROM CCA SURFACE FOR NORMAL OPERATION.

A6 COMPONENT LOCATOR



A1
MOTHERBOARD
CCA FO-2
SHEET 3



CE1ZS020

Figure FO-6. A6 GPIB Circuit Card Assembly Component Locator, and Functional Block Diagram.

By Order of the Secretaries of the Army and the Marine Corps:

CARL E. VUONO
General, United States Army
Chief of Staff

Official:

WILLIAM J. MEEHAN II
Brigadier General, United States Army
The Adjutant General

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To: 2028@redstone.army.mil

Subject: DA Form 2028

1. ***From:*** Joe Smith
2. *Unit:* home
3. ***Address:*** 4300 Park
4. ***City:*** Hometown
5. ***St:*** MO
6. ***Zip:*** 77777
7. ***Date Sent:*** 19−OCT−93
8. ***Pub no:*** 55−2840−229−23
9. ***Pub Title:*** TM
10. ***Publication Date:*** 04−JUL−85
11. *Change Number:* 7
12. *Submitter Rank:* MSG
13. ***Submitter FName:*** Joe
14. *Submitter MName:* T
15. ***Submitter LName:*** Smith
16. ***Submitter Phone:*** 123−123−1234
17. ***Problem:*** **1**
18. *Page:* 2
19. *Paragraph:* 3
20. *Line:* 4
21. *NSN:* 5
22. *Reference:* 6
23. *Figure:* 7
24. *Table:* 8
25. *Item:* 9
26. *Total:* 123
27. ***Text:***

This is the text for the problem below line 27.

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TO: (*Forward to proponent of publication or form)(Include ZIP Code)* Commander, U.S. Army Aviation and Missile Command ATTN: AMSAM–MMC–MA–NP Redstone Arsenal, 35898	FROM: (*Activity and location)(Include ZIP Code)* MSG, Jane Q. Doe 1234 Any Street Nowhere Town, AL 34565	

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PUBLICATION/FORM NUMBER	DATE	TITLE
TM 9–1005–433–24	16 Sep 2002	Organizational, Direct Support, And General Support Maintenance Manual for Machine Gun, .50 Caliber M3P and M3P Machine Gun Electrical Test Set Used On Avenger Air Defense Weapon System

ITEM NO.	PAGE NO.	PARA–GRAPH	LINE NO. *	FIGURE NO.	TABLE NO.	RECOMMENDED CHANGES AND REASON
1	WP0005 PG 3		2			Test or Corrective Action column should identify a different WP number.

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PAGE NO.	COLM NO.	LINE NO.	NATIONAL STOCK NUMBER	REFERENCE NO.	FIGURE NO.	ITEM NO.	TOTAL NO. OF MAJOR ITEMS SUPPORTED	RECOMMENDED ACTION

PART III – REMARKS (*Any general remarks or recommendations, or suggestions for improvement of publications and blank forms. Additional blank sheets may be used if more space is needed.)*

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PUBLICATION/FORM NUMBER	DATE	TITLE

ITEM NO.	PAGE NO.	PARA–GRAPH	LINE NO. *	FIGURE NO.	TABLE NO.	RECOMMENDED CHANGES AND REASON

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