TECHNICAL MANUAL

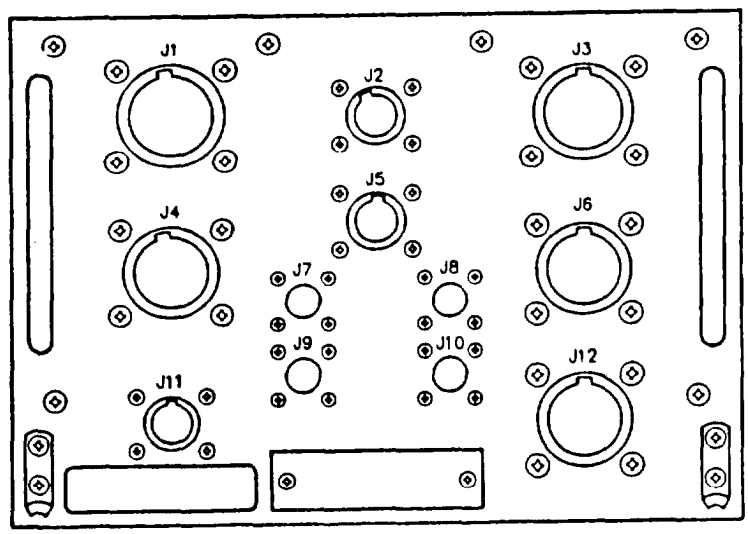
MAINTENANCE INSTRUCTIONS

DIRECT SUPPORT AND

GENERAL SUPPORT

DIRECTION FINDER CONTROL
C-11002/USQ
NSN 5895-01-115-9154

This publication together with TM 32-5811-012-34P supersedes TM 32-5811-012-34&P dated 15 May 1989.



AUGUST 1993

HEADQUARTERS, DEPARTMENT OF THE ARMY

WARNING

High voltage is used in the operation of this equipment. Avoid contacting high-voltage connections when installing or operating this equipment. Injury or death may result if personnel fail to follow safety precautions.

AC neutral and ground are not the same. It is possible for voltage potentials to exist between ac neutral and ground. These potentials may cause shock and personal injury.

Before performing any inspection procedure ensure that power is disconnected from the DF control.

Adequate ventilation should be provided while using trichlorotrifluoroethane. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since trichlorotrifluoroethane dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use heavy duty rubber gloves that the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

Before performing any removal procedure, ensure that power is disconnected from the DF control.

Before performing any replacement procedures, ensure that power is disconnected from the DF control.

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, DC, 31 August 1993

MAINTENANCE INSTRUCTIONS
DIRECT SUPPORT AND GENERAL SUPPORT
FOR
DIRECTION FINDER CONTROL C-11002/USQ
5895-01-115-9154

REPORT ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms) or DA Form 2028-2 located at the back of this manual, direct to: Director, U.S. Army CECOM Intelligence Materiel Management Center, ATTN: SELIM-TE, Vint Hill Farms Station, Warrenton, Virginia 22186-5279. A reply will be furnished to you.

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HOW TO USE THIS MANUAL

This manual is designed to help you perform direct support and general support maintenance on the Direction Finder Control, C-11002/USQ. The written procedures, tables and illustrations should be used together to help you do your job more effectively. Don't skip steps and don't take short cuts.

Before you begin any task, you should read through the complete procedure. Make sure you know what needs to be done; then go back and follow the steps as written.

This manual is divided into the following chapters:

Chapter 1 - INTRODUCTION
Chapter 2 - DIRECT SUPPORT MAINTENANCE PROCEDURES
Chapter 3 - GENERAL SUPPORT MAINTENANCE PROCEDURES

At the back of the manual, you will find the following appendices:

Appendix A - REFERENCES
Appendix B - MAINTENANCE ALLOCATION CHART (MAC)
Appendix C - EXPENDABLE AND DURABLE ITEMS LIST
Appendix D - FRONT PANEL CONNECTOR PIN FUNCTIONS
Appendix E - WIRE LISTS

1. Turn to the section or chapter you want to use. If it is necessary to troubleshoot the system, use the logic diagram provided.

2. If it is necessary to repair or replace an item, turn to the index at the back of the manual to locate the task. Before beginning the task, look through the procedure. You must familiarize yourself with the entire maintenance procedure.

3. Warnings and cautions are provided to provide instructions regarding potentially hazardous conditions which may harm the maintenance personnel or the equipment. These instructions must be observed to avoid personnel injury or death or equipment damage or destruction.

4. Once you have thoroughly familiarized yourself with the maintenance procedure, you are ready to perform it. Additional information which will help you perform the task is located in the appendices at the back of the manual.

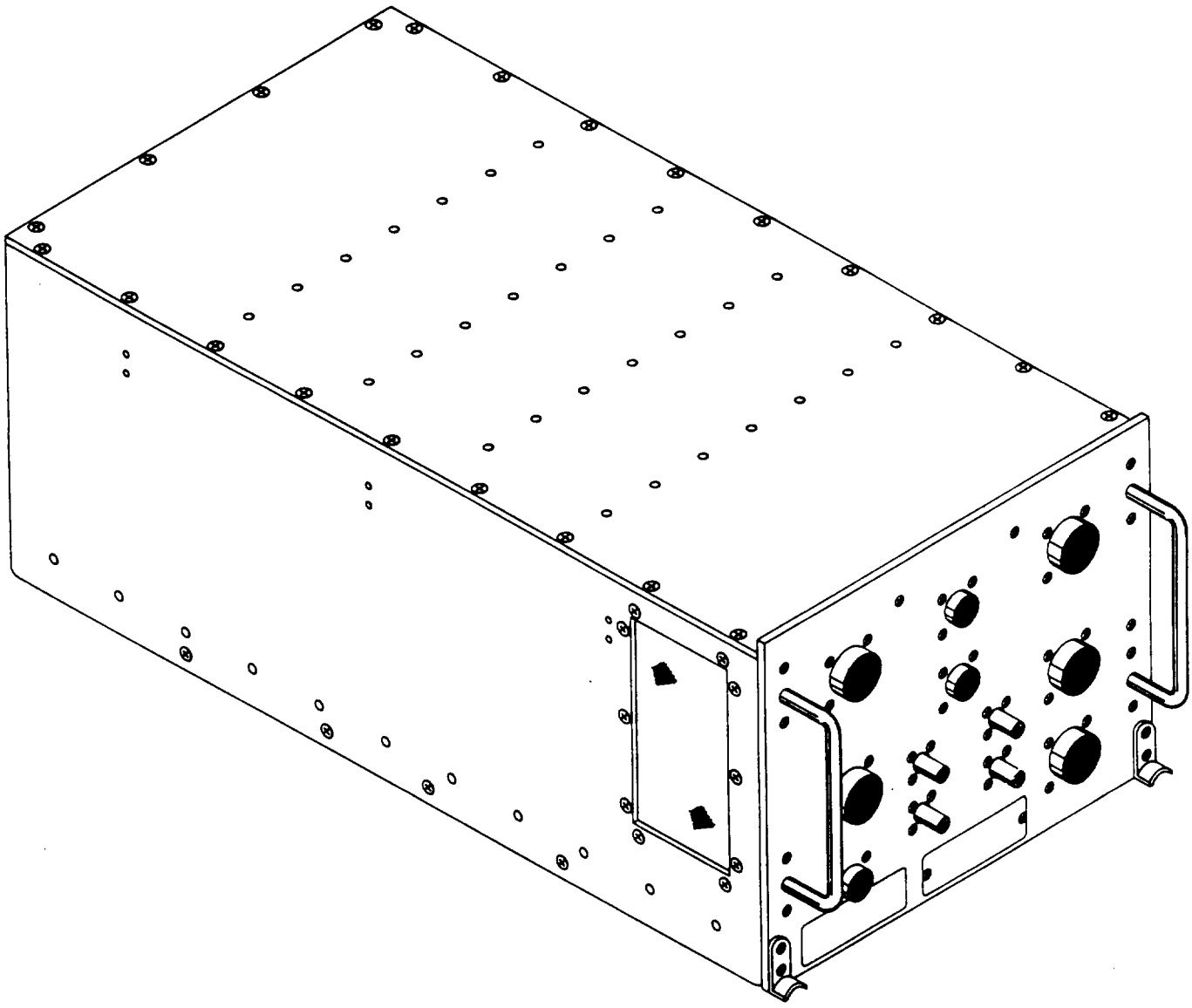

Figure 1-1. Direction Finder Control

CHAPTER 1

INTRODUCTION

Section I. GENERAL INFORMATION

1.1.1 SCOPE.

a. Type of Manual: Direct support (DS) and general support (GS)maintenance.

b. Model Number and Equipment Name: C-11002/USQ - Direction Finder Control.

c. Purpose of Equipment To provide main controlling and computing functions in a direction finding subsystem.

1.1.2 MAINTENANCE FORMS, RECORDS, AND REPORTS.

Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA PAM 738-750, Army Maintenance Management System (TAMMS).

1.1.3 DESTRUCTION OF ARMY MATERIEL TO PREVENT ENEMY USE.

Procedures for the destruction of Army materiel are contained in TM 750-244-2, Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

1.1.4 PREPARATION FOR STORAGE OR SHIPMENT.

Instructions for preparing the equipment for storage or shipment are included in Section VII of Chapter 3.

1.1.5 OFFICIAL NOMENCLATURE, NAMES, AND DESIGNATIONS.

Shortened nomenclature for the Direction Finder Control, C-11002/USQ has been used in this manual to make procedures easier for you to read. The Direction Finder Control, C-11002/USQ, hereinafter will be referred to as the DF control.

1.1.6 REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATION (EIR).

If your DF control needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design or performance. Put it on an SF 368 (Quality Deficiency Report). Mail it to the Director, U.S. Army CECOM Intelligence Materiel Management Center, ATTN: SELIM-TE, Vint Hill Farms Station, Warrenton, VA 22186-5279. A reply will be furnished directly to you.

1.1.7 SAFETY, CARE, AND HANDLING.

To assure personnel safety and prevent equipment damage, observe all WARNINGS and CAUTIONS in this manual during equipment maintenance. WARNINGS contain information which, if not carefully observed, could result in personal injury or death; CAUTIONS contain information which, if not observed, could result in damage to the equipment.

1.1.8 CORROSION PREVENTION AND CONTROL.

Corrosion Prevention and Control (CPC) of Army material is a continuing concern. It is important that any corrosion problems with this item be reported so that the problem can be corrected and improvements can be made to prevent the problem in future items.

While corrosion is typically associated with rusting of metals, it can also include deterioration of other materials, such as rubber and plastic. Unusual cracking, softening, swelling, or breaking of these materials may also be a corrosion problem.

If a corrosion problem is identified, it can be reported using Standard Form 368, Product Quality Deficiency Report. Use of keywords such as "corrosion," "rust," "deterioration," or "cracking" will ensure that the information is identified as a CPC problem.

The form should be submitted to the address specified in DA PAM 738-750.

1.1.9 NUCLEAR HARDNESS.

This equipment does not have nuclear survivability requirements.

1.1.10 SECURITY MEASURES FOR ELECTRONIC DATA.

This equipment does not contain classified electronic data.

Section II. EQUIPMENT DESCRIPTION AND DATA

1.2.1 EQUIPMENT CHARACTERISTICS, CAPABILITIES, AND FEATURES.

The DF control is used as the main controlling and computing element in a direction finding subsystem. It is a solid state, air cooled unit which contains 18 circuit card assemblies and two axial blowers. When the DF control receives a command message, it responds as follows:

a. Switches DF antennas.

b. Evaluates the resulting DF audio levels and adjusts the DF antenna delays accordingly.

c. Converts the final antenna delay to target LOB data.

d. Transfers the target LOB data to the computer.

The DF control interfaces with a DF receiver, a RF processor and a computer via an internal interface within the DF control. A typical implementation of the DF control is shown in Figure 1-2.

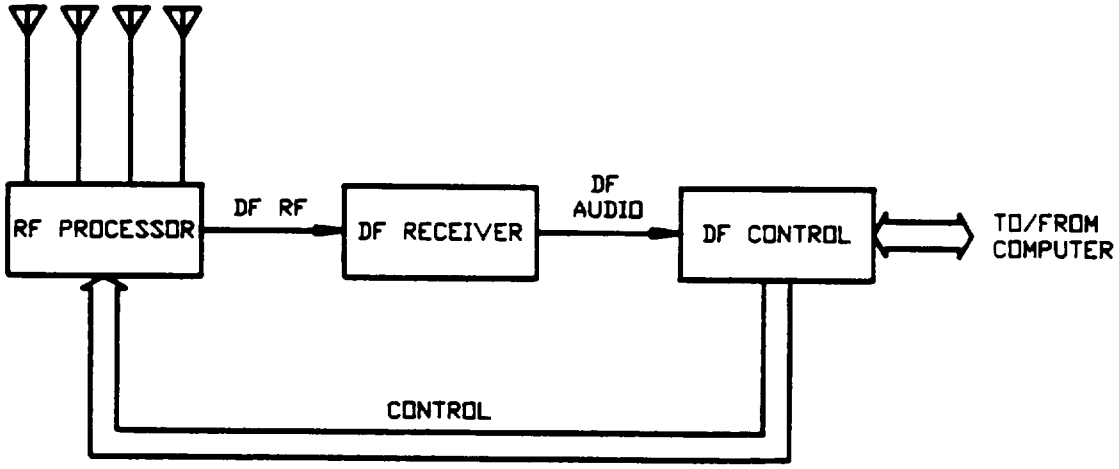

Figure 1-2. Typical DF Control Application

1.2.2 LOCATION AND DESCRIPTION OF MAJOR COMPONENTS.

An external view of the DF control is shown in Figure 1-1. Input/output connectors and identification plates are located on the front panel. Cooling air inlets are located near the front of each side of the unit and the air is exhausted at the rear of the unit. Circuit card identification and location is located on a label affixed to the inside of the top cover.

In addition, the DF control is capable of performing calibration and self-tests in response to computer command messages.

1.2.3 DIFFERENCES BETWEEN MODELS.

There is only one model of the C-11002/USQ DF control.

1.2.4 EQUIPMENT DATA.

Input power requirements	+5.0 ±0.25 V dc, 20 A -10.0 ±0.5 V dc, 5 A +15 ±0.5 V dc, 0.2 A -15 ±0.5 V dc, 0.2 A 115 ±11.5 V ac, 400 Hz ±57 Hz, 3 Φ (cooling fans)
Data storage capacity:	
Permanent instructions (ROM)	8192 x 24-bit words (196,608 bits)
Calibration tables (ROM)	8192 x 16-bit words (131,072 bits)
Scratch pad (RAM)	2048 x 16-bit words (32,768 bits)
Instruction execution time	2.4 microseconds (nominal)
External serial data transfer rate:	
Between computer and DF control	1 MHz (nominal)
Between DF control and RF processor	500 kHz (nominal)
Environmental characteristics:	
Temperature	-40° to +55 °C (-40° to +131 °F)
Humidity	0 to 98%
Altitude	0 to 40,000 feet
Physical characteristics:	
Height	7.8 inches (19.81 cm)
Width	10.2 inches (25.92 cm)
Length	22.2 inches (56.39 cm)
Weight	24.8 pounds (11.27 kg)

1.2.5 EQUIPMENT CONFIGURATION.

There is only one configuration of the C-11002/USQ DF control.

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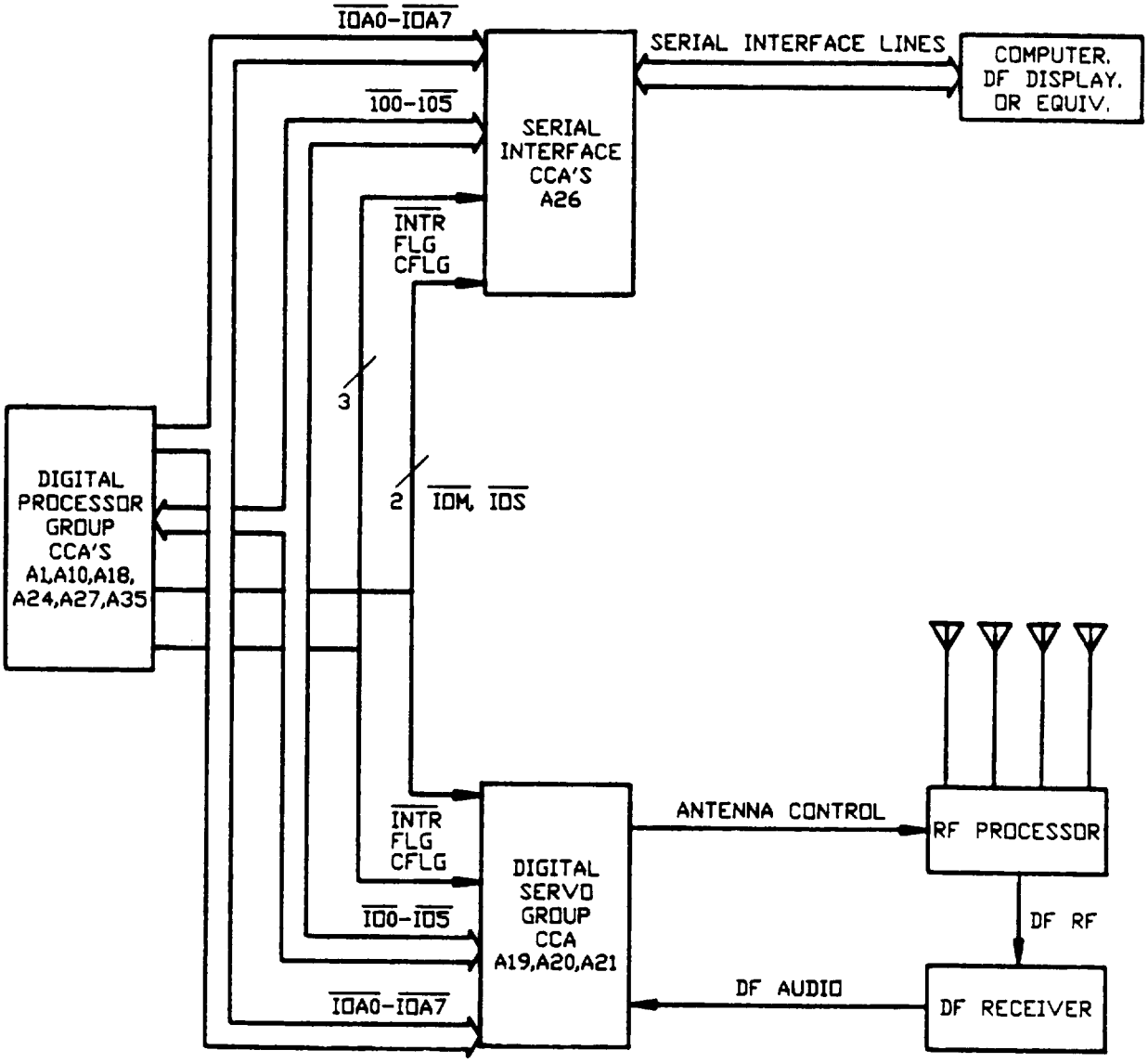


Figure 1-3. DF Control Block Diagram

Section III. PRINCIPLES OF OPERATION

1.3.1 FUNCTIONAL DESCRIPTION.

The DF control is comprised of three functional groups:

a. The digital servo group

b. The digital processor group

c. The serial interface group

The digital processor group executes the DF function according to preprogrammed instructions (firmware) and by exchanging data, commands, and status information with other system units. The digital servo and serial interface are peripheral groups providing the means for asynchronous exchange of information. See Figure 1-3 for the DF control block diagram. The digital processor communicates with the peripheral groups via the signal listed in Table 1.1.

The Circuit Card Assemblies (CCAs) which constitute a functional group are listed at the beginning of that group's detail description. Due to the fact that a single CCA may contain many different functions or, conversely, a single function may involve more than one CCA, component circuit theory is organized according to the task performed by the circuit rather than by the circuit (or CCA) location. See Figures FO-1 thru FO-26 for functional block or schematic diagrams for the DF control.

NOTE

Most digital circuits in this equipment use positive logic. Signal names reflect the signal function when the signal is true. A signal is considered true when it is in the more positive of the two permissible states (normally +5 V), and false when it is low (normally zero volts). Overscored signal names are read with a NOT preceding the function. Example: RESET is read as NOT RESET. When RESET is low (false) the implied opposite (RESET) condition is considered true. However, I/O bus and data transmission lines are driven with inverter drivers. Therefore, signal transfer on these lines is accomplished using overscored (complemented) signal levels. Thus, on these lines, the data bit is considered true when the overscored signal line is low.

Table 1-1. Digital Processor Group Signals

Signal	Function
$\overline{IO0}$ thru $\overline{IO15}$ (input/output or I/O bus). A 16-bit parallel bus. All data are negative true.	This bidirectional bus transfers information between the digital processor group and a peripheral group.
$\overline{IOA0}$ thru $\overline{IOA7}$ (input/output address or IOA bus). An eight-bit parallel bus. All bits are negative true.	The digital processor group generates an eight-bit code onto this bus to: Select the peripheral group, Command the peripheral group, Define the I/0 bus information. The DF control $\overline{IOA}$ assignments are as follows: $\overline{IOA}$ (negative true) — addressed group 011_8, 031_8 — Serial interface group 012_8, 013_8, 014_8 — Digital servo group
FLG0 thru FLG15 (flag) Flag set = high Flag clear = low	When set, the flag indicates that the digital processor group is ready for internal data exchange or external data exchange with a peripheral group. The element or group then clears the flag and transfers the information via the I/0 or internal bus. When processing or transferring of the data requires excessive time or a unique sequence of instructions, the cleared flag activates an interrupt signal. This interrupt causes the digital processor group to depart from its normal sequence of programmed instructions and jump to an instruction set (or subroutine), which is determined by the interrupt signal. The flag and interrupt signal allocations are as follows:
$\overline{INT0}$ thru $\overline{INT7}$ (interrupts) $\overline{INT}$ active = low $\overline{INT}$ inactive = high	

Table 1-1. Digital Processor Group Signals (Continued)

Signal	Function
FLG0 thru FLG15 (flag) (Continued)	Flag INT Group 0.1 6 Serial interface 2 5 Digital servo 13 4 Digital processor timer 14 7 Digital processor power-up sequence 15 None A DF control fault annunciator (for special test equipment)

NOTE: The number denotes the priority of the interrupt. For example, if interrupts 6 and 7 were active at the same time, the digital processor would respond to interrupt 7 first, then service interrupt 6.

1.3.2 DIGITAL SERVO GROUP.

The digital servo group interfaces the digital processor group with the RF processor and the DF receiver. In addition, this group generates timing signals for alternate selection of RF processor hybrid output ports, DF analog-to-digital conversion, transfer of converted binary data to the digital processor, and transfer of antenna switch command and delay line preset (DLP) data from the digital processor to the RF processor. The digital servo group consists of the following CCAs:

Servo conversion CCA A19
Servo timing CCA A20
Servo serial interface CCA A21

The digital servo group accomplishes two basic DF control functions: servo data acquisition and servo control transfer.

1.3.2.1 Servo Data Acquisition. (See Figure FO-1.) The servo data acquisition circuits generate the data transfer mode (DT MOD) signal, which alternately selects RF source A and RF source B inputs from antennae A and B, respectively, for input to the DF receiver via the RF processor. The servo data acquisition circuits convert the resulting audio outputs of the DF receiver into binary baseline data, which are proportional to their amplitude. The appropriate handshake functions are then performed to transfer the binary data to the digital processor, which calculates the error and the next RF processor delay line insertion command. The data transfer function is repeated until a suitable amount of inserted RF processor delay time is found. When the amplitudes of both baseline components are within predetermined parameters, the digital processor recognizes that the proper amount of inserted time delay has been found. When this occurs, the line of bearing (LOB) measurement is complete.

The digital processor group responds to operating parameters such as DF receiver frequency, baseline antenna pair selection, and stored calibration constants by selecting appropriate signal sampling times. This dates supplied to the servo acquisition circuits via the IO0 through IO3 I/O bus lines. The IOA0 through IOA7 lines, as well as the IOM signal, are configured to address the digital servo and define the I/O data as servo control inputs.

The command decoding ciruits on CCA A21 respond to the IOA 014_8 code, the low IOM, and the IOS(I/O strobe) by transferring the sample time commands (IO0 through IO3) to servo timing CCA A20 and servo conversion CCA A19.

The 16-kHz clock from the servo clock generator on servo timing CCA A20 is routed to a pair of divide-by-N circuits. One of the divide-by-N circuits is controlled by two bits from the integration dump control. The remaining divide-by-N circuit is controlled by three bits from the integration time control. The combined outputs from the two divide-by-N circuits create the track/hold clock. Each positive edge of the track/hold clock sets the track/hold flip-flop. As a result, the track/hold clock period (s) determines the total audio signal sampling and conversion time. The divide-by-N output to the integrator dump timer determines the duration, (d), of the INT DUMP signal. The resulting output integration time and integration dump time bits select the respective input sample times(s) and integrator dump times (d) according to Table 1-2.

Table 1-2. Servo Timing

INPUT (negative true)				Sample (s) time (milliseconds)	Integration dump (d) time (microseconds)
$\overline{IO3}$ (ID1)	IO2 (ID0)	IO1 (IT1)	$\overline{IO0}$ (IT0)		
1	1	1	1	0.50	40
1	0	1	0	1.02	240
0	1	0	1	2.04	560
0	0	0	0	4.09	1200

In addition to determining sample time, the IT0 and IT1 bits control the charging rate of the integrator on servo conversion CCA A19. A Shorter sample time results in a faster integrator charge rate.

The servo data acquisition circuits of the digital servo group process DF audio inputs as follows (see Figure 1-4).

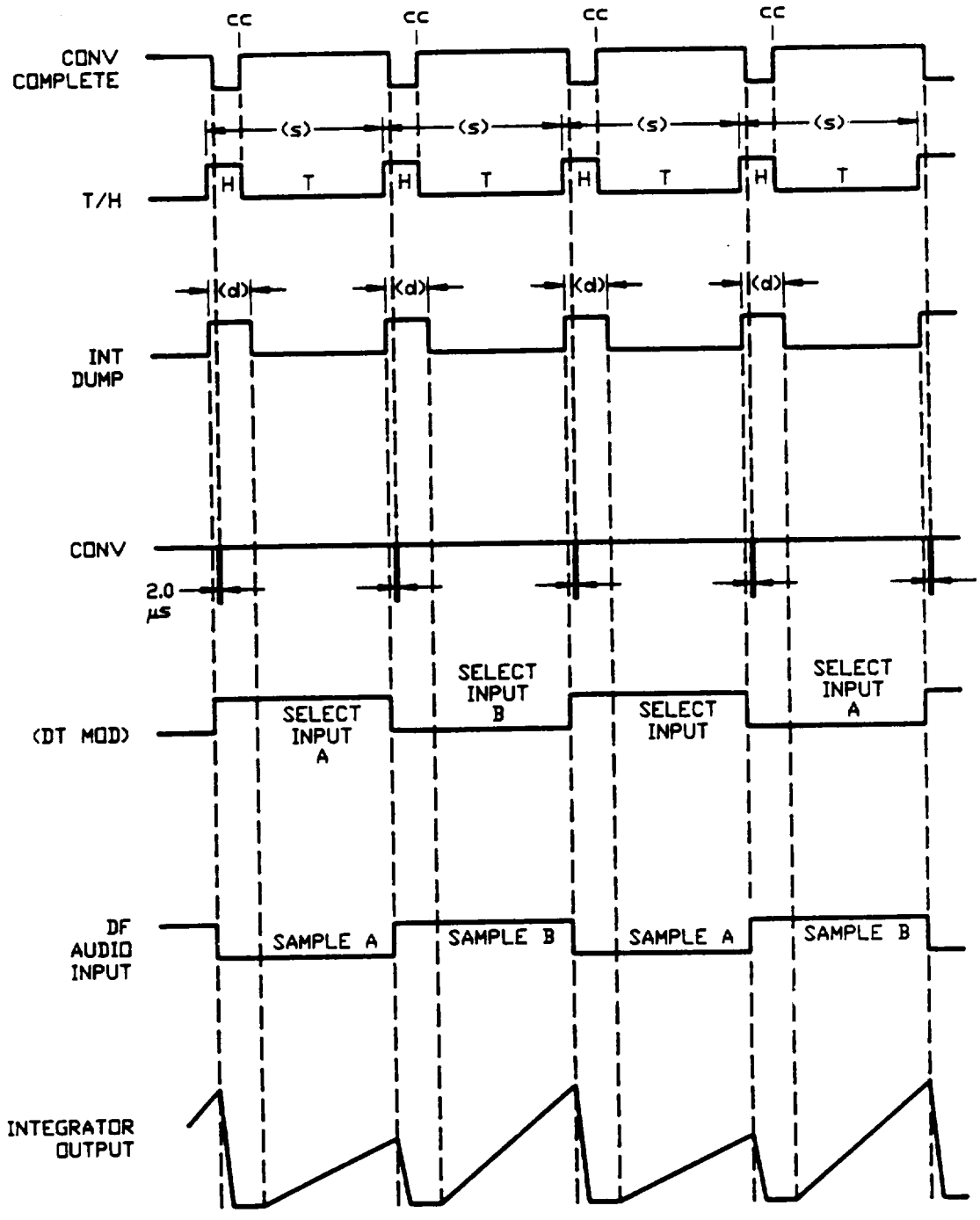


Figure 1-4. Servo Data Acquisition Timing Diagram

When a conversion operation has ended, the A/D converter generates a high COW COMPLETE (CC) signal. This signal resets the track/hold flip-flop. The resulting low track/hold signal brings the track/hold circuits on CCA A19 to the track (T) mode of operation. In this mode, the integrator output feeds the track/hold storage capacitor.

The integrator provides an output level proportional to the average of the DF audio A signal over the integration time. During the track (integrate) mode of operation, the INT DUMP signal is low (false). As a result, the solid state dump switch is opened, permitting the integrator capacitor to charge as a function of the input audio level. This charge is also stored by the track/hold storage capacitor when the TRACK/HOLD (T/H) signal is low (in track mode).

After a time interval determined by the track/hold clock, the track/hold flip-flop is set. The resulting high T/H signal disconnects the track/hold storage capacitor from the integrator. six tenths of a microsecond later, the integrator dump time is activated, providing a high (true) INT DUMP signal. This high (d) input activates the dump switch, discharging the integrator in less than 10 microseconds and preventing it from charging. In addition, the high INT DUMP signal is applied to CCA A21 for strobing the RF processor command data. Concurrent with the rising edge of the INT DUMP signal, the timer INT DUMP (low) signal edge clocks the input select flip-flop on CCA A21. This toggles the flip-flop, changing DT MOD input selection from A to B. The resulting B audio signal is applied to the integrator of servo conversion CCA A19 for the next integration cycle. The (d) time interval during which the integrator is discharged is determined by the INT DUMP time clock. This clock is derived from the timer divide-by-N circuit. The track/hold storage capacitor retains the former integrator charge voltage level because it is isolated from the integrator by the track/hold switch. The stored voltage level is applied to the A/D converter via the track/hold switch.

A CONV pulse initializes and activates the A/D converter 2.0 microseconds after the integrator Dump timer is activated. The A/D converter then uses the A/D CLOCK input (from the servo clock generator) to convert the voltage input (from the track/hold storage capacitor) into an equivalent 10-bit binary number. When the conversion is accomplished, the COW COMPLETE line is driven high. The high edge of CONV COMPLETE clocks the handshake logic of servo timing CCA A20. The logic circuits respond by generating a true (high) CFLG2 and a false (low) INT5. CFLG2 clears digital processor flag 2. INT5 initiates a servo data input operation. The digital processor generates the servo data acquisition control code DA (data acquisition) or SC (servo control) on the IOA bus (014_8), together with a high ION (input/output mode) signal. The command decoding circuits of CCA A21 respond to these inputs by generating a high A/D ENABLE signal. An inverter on CCA A20 inverts this high to a low (false) A/D DISABLE signal that enables the I/O bus drivers in CCA A19. Enabled, the I/O bus drivers transfer the 10-bit binary servo data, representing the DF antenna signal received via DF antenna A, to the digital processor via the I/O bus.

The high CONV COMPLETE signal also resets the track/hold flip-flop. The resulting low track/hold signal switches the track/hold switch back to the track mode of operation.

The track/hold signal is also used with the A/D ENABLE signal to generate servo data status bit IO10 (see Figure FO-1). When both of these signals are high (HOLD mode and IO0 - IO9 data bus drivers enabled) , the signals generate a low IO10 status bit. When low, this bit alerts the digital processor that valid servo data is active on the I/O bus. The processor ignores the servo output while status bit IO10 is high. Also, a signal DA ENABLE is used with the CONT MOD signal to generate status bit IO11. This status bit indicates to the processor whether the DT MOD output of the antenna select flip-flop is high or low. When DT MOD is high, bit IO11 is low to indicate A antenna pair selection. When DT MOD is low, bit IO11 is high to indicate B antenna pair selection. Table 1-3 provides a summary of the IO10 and IO11 bits when the digital processor is receiving digital servo data.

Table 1-3. Servo Data Status Bits

Servo Data Status Bit	State	T/H Signal State	Interpretation/Digital Servo Condition
$\overline{\text{IO10}}$ (negative true)	1	High (hold)	Servo conversion still in process; servo data (IO0 thru IO9 unacceptable)
	c	Low (track)	Servo conversion completed; accept servo data
$\overline{\text{IO11}}$ (negative true)	1	x	DT MOD high (1)
	0	x	DT MOD low (0)

x = May be high or low.

1.3.2.2 Servo Control Transfer. (See Figure 1-5.) The servo control transfer function is accomplished by serial servo interface CCA A21. Transfer registers on CCA A21 are loaded with a 24-bit word received from the digital processor in two 12-bit bytes (see Figure 1-6). The first byte, consisting of 12 DLP bits, is parallel-loaded from the IO0 through IO11 bus lines into registers U17 and U23. This loading operation results from the IOA bus code of 012_8 and a low IOM input to the command decoder of CCA A21. The DLP output of the command decoder places registers U17 and U23 in the LOAD mode while bus code 012_8 is active. The registers are placed back in the SHIFT mode when the bus code changes. Then the second byte, consisting of antenna switch command data, is placed on the 100 through IO11 by the digital processor. An IOA code of 013_8 and a low IOM signal produce an antenna switch command decoder output signal (ASC).

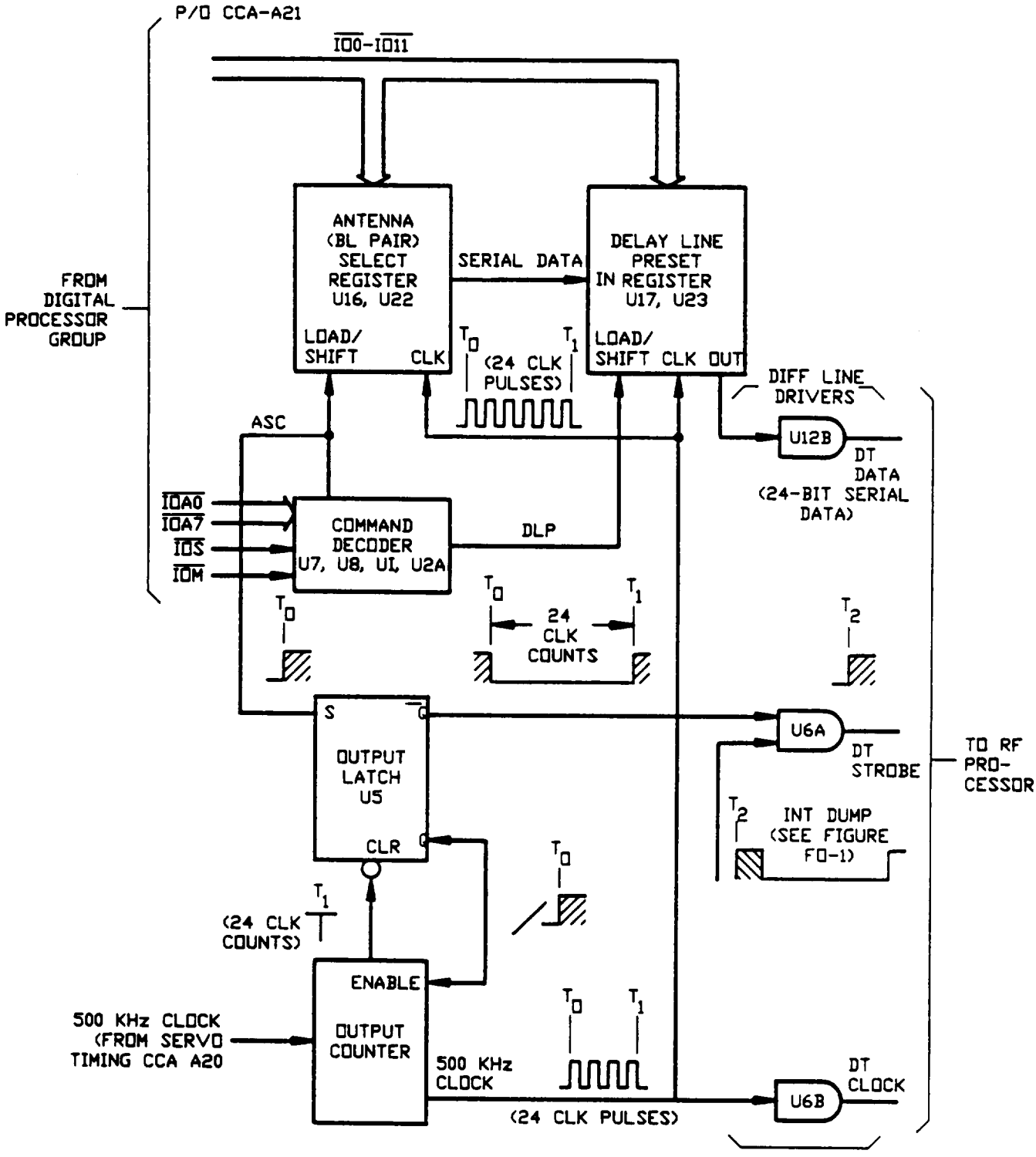


Figure 1-5. Servo Control Transfer Block Diagram

DELAY LINE
PRESET COMMAND (DLP)
I/O BUS BIT

11	10	9	8	7	6	5	4	3	2	1	0
DL11	DL10	DL9	DL8	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0
SPARE	SPARE	SPARE	D8	D7	D6	D5	D4	D3	D2	D1	ENABLE 1

ANTENNA SWITCH
COMMAND (ASC)
I/O BUS BIT

11	10	9	8	7	6	5	4	3	2	1	0
AS11	AS10	AS9	AS8	AS7	AS6	AS5	AS4	AS3	AS2	AS1	AS0
SPARE	INTERCEPT AMPLIFIER BYPASS	SPARE	SPARE	DF AMP BYPASS	SPARE	BITE ENABLE	REVERSE SW	BL SW3	BL SW2	BL SW1	SPARE
S11	S10	S9	S8	S7	S6		S4	S3	S2	S1	

Figure 1-6. Antenna Command Data Formats

This ASC signal causes the following sequence of events to occur:

a. The antenna switch command data is loaded into registers U16 and U22 since initially the ASC signal places U16 and U22 in LOAD .

b. Output latch U5 is set by ASC signal ASC switching from low to high.

c. The output counter is enabled by U5 output.

d. The 333-kHz shift clock (500-kHz for all boards except -3) is applied to registers U16, U22, U17, and U23, and to line driver U6B.

The clock serially shifts the 24-bit DLP and antenna switch command word residing in the registers, via differential line driver U12B, out to the RF processor for serial loading of the command word.

When the output counter has counted 24 clock pulses, it clears output latch U5 with a low input_and terminates the clock. Cleared, output latch U5 provides a high Q output, which enables line driver U6A. Enabled, the line driver responds to the next rising edge of the INT DUMP signal by generating a high DT (data transfer) STROBE. This strobe is used to load the DLP and antenna switch command word into buffer registers within the RF processor. As a result, new data is transferred to the RF processor's RF switch drivers during the same time interval in which DT MOD (derived from INT DUMP) selects an alternate sampling antenna.

1.3.2.3 Servo Conversion CCA A19. (See Figure FO-21.) Servo conversion CCA A19 integrates and digitizes the analog (audio) input signals from the DF receiver. The resulting digital output is gated via the I/O bus to the digital processor for the DF calculation.

CCA A19 can amplify up to four analog input signals with preamplifiers U15, U16, U17, and U18. The amplified signals are applied to multiplexer U11. The multiplexer, under control of the analog input (A1) control signals (i.e., AI0 and AI1) from servo serial interface CCA A21, applies the selected analog signal to amplifier U3 pin 5. For this application, the AI0 and AI1 signals are low, selecting the amplified output of U18 as the input to amplifier U3. The output of U3 pin 4, is applied to the ±5 V level shifter, comprised of U3 pin 12, U3 pin 3, and U3 pin 10. A regulated ±12 V is provided by regulators U21 and U22 which isolate the reference voltages from the power supply.

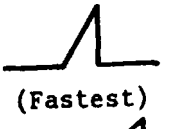
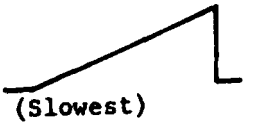
The level shifter is capable of shifting the dc level of the input voltage by as much as ±5 V. The amount of shift is controlled by level shift control potentiometer R20. Since the input audio voltage varies between -4.0 V and +1.0 V, a level shift of +4.0 V is required. The output of level shifter U3 pin 3 is applied to amplifier U7, which inverts the signal.

The output of U7 is -4.0 V for a +1.0 V input signal, and O V for a 4.0 V input signal. This signal is then applied to an integrator circuit composed of eight resistors, multiplexer U6, amplifier U1, and a 5600 pF capacitor. Under control of the integration time control signals (IT0, IT1) from servo serial interface CCA A21, multiplexer U6 selects one of four resistors to work in conjunction with the capacitor. (See Table 1-4.)

NOTE

The integrator capacitor charges faster when a smaller value resistor is selected by the multiplexer, producing an output ramp with a steeper slope.

Table 1-4. Integrator Ramp Control

Integrator Time Control Bit (I/0 bus bit)			Selected Resistor (value)	Ramp Slope (charge rate)
IT2	IT1 (IO1)	IT0 (IO0)		
High	Low	Low	R35 (40.2K)	 (Fastest)
High	Low	High	R36 (80.6K)	
High	High	Low	R37 (162K)	
High	High	High	R38 (330K)	 (Slowest)

NOTE: IT2 is always high due to pullup resistor R13 on servo timing CCA A20.

The integration time bits control sample time (s), providing more time when a slower charge rate (i.e., more shallow ramp slope) is selected. This ramp can rise from 0 V up to a maximum of 10 V, depending upon the analog signal input level.

The ramp is applied to the track/hold circuit consisting of U8 and C35. A low track/hold signal places U8 in the track mode. This allows storage capacitor C35 to charge to the maximum ramp voltage present at the output of U1. The track/hold pulse goes high to place U8 in the hold mode by isolating C35 from the output of the integrator. This permits C35 to retain its charge during the integrator dump operation.

A high INT DUMP signal is then applied to the solid state dump switch. The switch responds by shorting the integrator capacitor, discharging it, and bringing the ramp voltage down to zero. The integrator output ramp remains at 0 V for the duration of the INT DUMP signal. This length of time (d) depends upon the IO3 and IO2 bits received and decoded on servo serial interface CCA A21 to provide IT0 and IT1 (integrator timing signals). Two microseconds after INT DUMP starts, a CONV pulse is applied to the A/D converter, activating it. Storage capacitor C35, isolated from the integrator during the DUMP operation, feeds the activated A/D converter.

The A/D converter consists of ground threshold detector U4, variable voltage divider network U5, and 10-bit counter U9. The input CONV pulse initializes counter U9. The resulting counter output configures variable voltage divider network U5 for maximum resistance between its -15 V input and output pin 3. This allows the positive analog input (at U5 pin 16) to offset the -15 V by an amount proportional to the analog voltage. As a result, the output of U5 pin 3 is positive. This positive input (the inverting input) to ground threshold detector U4 forces U4 pin 9 low to control counter U9.

The 10-bit counter output is now the binary equivalent of the analog voltage input. This output is applied to I/O bus drivers U12 through U14. As a result of its frozen count, counter U9 drives pin 3 low. This low is inverted by U12A to provide an active (high) CONV COMPLETE signal to latches U12 and U11 of servo timing CCA A20 (see Figure FO 22). The digital processor provides a high FLG2 (flag 2) input to latch U12 to notify the digital servo input (interrupt 5) subroutine. This subroutine provides a high IOM signal and an A/D ENABLE CODE via the IOA bus. Servo serial interface CCA A21 translates these inputs into a high A\D ENABLE signal. This high is inverted by U6D on servo binary CCA A20 to provide a low A/D DISABLE signal. This low is applied to U12B on servo conversion CCA A19. U12B responds to the low by going high to enable I/O bus drivers U12 through U14. The enabled I/O bus drivers then transfer the 10-bit binary A/D data to the digital processor via the I/O bus.

The high CONV COMPLETE input to U11 on servo timing CCA A20 causes a low track, T/H signal to be generated by CCA A20. This again permits the track/hold circuits of CCA A19 to track the integrator ramp voltage (at this time the INT DUMP signal has expired).

1.3.2.4 Servo Timing CCA A20. (See Figure FO-22.) Servo timing CCA A20 provides the A/D clock used by CCA A21 for transferring antenna control data to the RF processor. The frequency of the A/D clock is 333 kHz. In addition, CCA A20 responds to the CONV COMPLETE signal from CCA A19 by generating digital servo T/H, CONV, and INT DUMP signals as well as digital processor CFLG2 and INT5 handshake signals.

1.3.2.4.1 Servo Timing. Oscillator U18 generates the basic 1.0-MHz clock. Counter U8 divides this clock by 3 to provide the 333-kHz A/D clock outputs via inverters U16E and U16D.

Presettable counter U14 and U20 divide the basic (1.0 MHz) clock by 32 to produce a 31.25-kHz (approximate) clock. This clock is divided by U21 to provide a 10.4-kHz clock to the integrator dump timer and track/hold clock divide-by-N circuit. The integrator dump timer divide-by-N circuits consist of U9E, U9F, U3A, U17D, and U2. When activated, these circuits determine the time interval (d) for the INT DUMP and INT DUMP signals according to the ID1 and ID0 inputs from servo serial interface CCA A21. These inputs preset counter U2, thereby determining the number of 16-kHz clock pulses required for U2 to reach a terminal (15) count. Table 1-5 shows the ID0 and ID1 inputs, the corresponding counter preset value and the resulting INT DUMP signal duration.

Table 1-5. INT DUMP Signal Duration

ID1	ID0	Preset Count	INT DUMP Approx. Signal Length (d)
Low	Low	14	50 microseconds
Low	High	12	240 microseconds
High	Low	8	620 microseconds
High	High	0	1400 microseconds

The track/hold clock divide-by-N circuits consist of counters U21, U15, and multiplexer U22. These circuits determine the T/H signal period (s) by responding to IT0 and IT1 signals from CCA A21. IT2 is always high. Counters U21 and U15 divide the 10.4-kHz clock input into 1.3-kHz, 650-Hz, 325-Hz, and 162-Hz outputs. These clocks are applied to multiplexer U22. U22 selects one of these clocks according to the integrator time signals as shown in Table 1-6.

Table 1-6. Track/Hold Clock Divide-By-N

Integrator Time		Selected Multiplexer (U22) Output Clock	Track/Hold Clock Period (s)
IT1	IT0		
Low	Low	1.3 kHz	0.750 milliseconds
Low	High	650 Hz	1.5 milliseconds
High	Low	325 Hz	3.0 milliseconds
High	High	162 Hz	6.0 milliseconds

Servo timing CCA A20 (see Figure 1-7) responds to the track/hold clock and the CONV COMPLETE input from servo conversion CCA A19 in the following manner:

1.3.2.4.1.1 Timing Sequence T1. The positive edge of the track/hold clock (U22 pin 5) clocks and sets track/hold latch U11A. This provides a rising output from U11A pin 5, which clocks and sets dump delay latch U4B. The set output track/hold latch also provides a low output at U11A, which is inverted by U6C to provide a high (hold mode) T/H signal.

1.3.2.4.1.2 Timing Sequence T2 The high Q output of U4B pin 9 causes U4A to be set less than a microsecond later by the 1.0-MHz basic clock input. The resulting high Q output (U4A pin 5) and the 1.0-MHz clock drive the output of U3C low, clearing U4B. The rising Q output (U4B pin 8) clocks and sets dump control latch U5B. U5B provides a high transition output (U5B pin 9), which clocks and sets U10B and activates integrator dump timer U2. The low Q output of U5B is inverted once by U6B to provide an active (high) INT DUMP signal, then again by U6E to provide the low INT DUMP signal. Activated, the counter counts the 10.4-kHz clock input from a preset value to a terminal 15 count. The preset value, controlled by the ID0 and ID1 inputs, determines the time in which the INT DUMP signal remains active. The high counter TC output (U2 pin 15), resulting from a terminal count, is inverted by U3D to clear latch U5B and terminate the INT DUMP signal.

1.3.2.4.1.3 Timing Sequence T3. The high Q output of set latch U10B drives the D input of U5A high at T2. The next 500-kHz clock (T3) transfers this high input to the U5A Q output. This Q output is high, however, the low Q output of U5A immediately clears U10B. In turn, the low Q output of U10B causes U5A to be reset by the very next 500-kHz clock (T4). The resulting pulse output of U5A pin 5 is inverted by U6A to provide the negative-going CONV pulse, which activates the A/D converter on servo conversion CCA A19. The CONV pulse is 2-micro-seconds wide because that is the time between two sequential 500-kHz pulse.

1.3.2.4.1.4 Timing Sequence T4. When activated by the positive edge of the CONV pulse, the A/D converter pulls CONV COMPLETE low.

1.3.2.4.1.5 Timing Sequence T5. When the A/D conversion process is completed, CCA A19 pulls CONV COMPLETE high. This high edge clocks latch U11B. Since U11A is set at this time, its Q output (U11A pin 6) is low. With this low input to pin 12, latch U11B responds to CONV COMPLETE by resetting. The resulting low Q output (U11B pin 9) immediately clears U11A via AND gate U17A. Cleared, track/hold latch U11A provides a low track mode output signal and provides a low Q output (U11A pin 5) , which presets latch U11B.

1.3.2.4.1.6 Timing Sequence T6. The track mode of operation remains until the track/hold clock again sets track hold latch U11A, repeating the servo timing cycle. INT DUMP clocks J-K flip-flop U11B on CCA A21 with its negative edge. The flip-flop toggles when clocked to select an alternate baseline pair antenna at the RF processor. As a result, the cycle time for the INT DUMP signal determines each antenna input sample time(s).

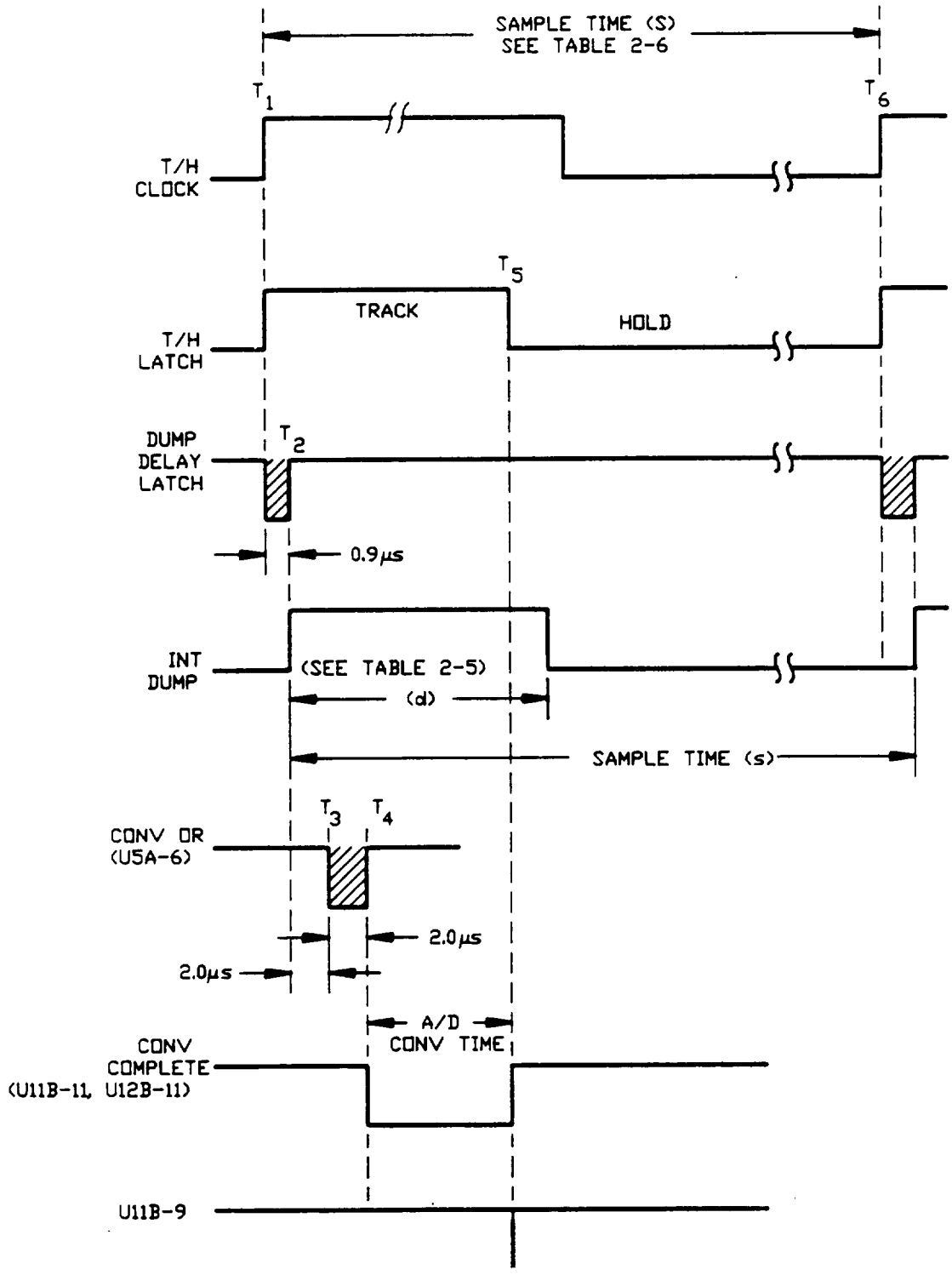


Figure 1-7. Servo Timing Diagram

1.3.2.5 Handshake Logic. (See Figure 1-8.) When ready to receive binary servo data from the digital servo group, the digital processor sets FLG2. Reset flip-flop U12A is cleared at this time. U17C, enabled by a high SERVO ENABLE input, responds to the high FLG2 input by providing a high (d) input to U12B pin 12. The positive edge of FLG2 also clocks and resets flip-flop U12A. The resulting low Q output of U12A pin 6 clears latch U12B. When U12B is cleared, the INT5 output goes high (false), and CFLG2 goes low. Also, the low Q output of U12B pin 9 clears U12A again.

Servo conversion CCA A19 provides a high CONV COMPLETE input when data have been converted into equivalent binary values. The high transition of CONV COMPLETE U12B pin 11 clocks and sets latch U12B on CCA A20. Set, U12B drives U24A pin 3 low, providing a true INT5 signal. At the same time, the low Q output of U12B pin 8 drives the CFLG2 output high via NAND gate U24D. This low clears FLG2. The true (low) INT5 signal initializes the digital processor interrupt 5 subroutine, which processes the received servo data and sets FLG2.

1.3.2.6 Servo Serial Interface CCA A21. (See Figure FO-23.) Servo serial interface CCA A21 contains the logic that stores coded delay line and antenna baseline pair switching commands from the digital processor and transfers these commands to the RF processor. In addition, CCA A21 decodes digital processor IOA inputs into digital servo commands.

1.3.2.6.1 Command Decoding. Comparator U7, in conjunction with inverter U1, NOR gate U2A, and decoder U8, translates the 8-bit IOA bus input (IOA0 through IOA7) and the IOM signal into servo command signals (see Table 1-7).

1.3.2.6.2 Antenna Command Transfer. The digital processor places the delay line preset data on the IO0 through IO11 bus lines when a delay line preset byte is being transferred. A delay line preset code is then applied to the IOA bus and a low IOM signal is applied to servo serial interface CCA A21. Inverter U1C inverts the low IOM to produce a high input to NOR gate U2A. This forces the output of U2A pin 1 low. This low equals the low output of inverter U1E. comparator U7 responds to this, and the equality between its B inputs and the IOA3 through IOA7 input bits, by going high at pin 9 (Z). The high is inverted by U1D to provide a low, enabling an input to decoder U8. This low, combined with the IOA0 through IOA2 inputs, produces a low output at U8 pin 6. This low forces the output of NAND gate U9B pin 6 high, enabling delay line preset gate U9C.

At this time, output latches U5A and U5B are reset. The low Q output (U5 pin 5) switches the A inputs to the output ports of multiplexer U3. As a result, the IOS strobe, inverted by U1B, is applied to the DLP gate (U9C pin 10) via multiplexer output port 2Y (U3 pin 7). The enabled gate responds to this input by producing a negative loading pulse. This pulse is applied to multiplexer U3 pin 11, which routes the pulse to output port 3Y (U3 pin 9). The negative pulse output of multiplexer U3 pin 9 is applied to U23 pin 1 to load the IO0 through 107 bits in DLP register U23.

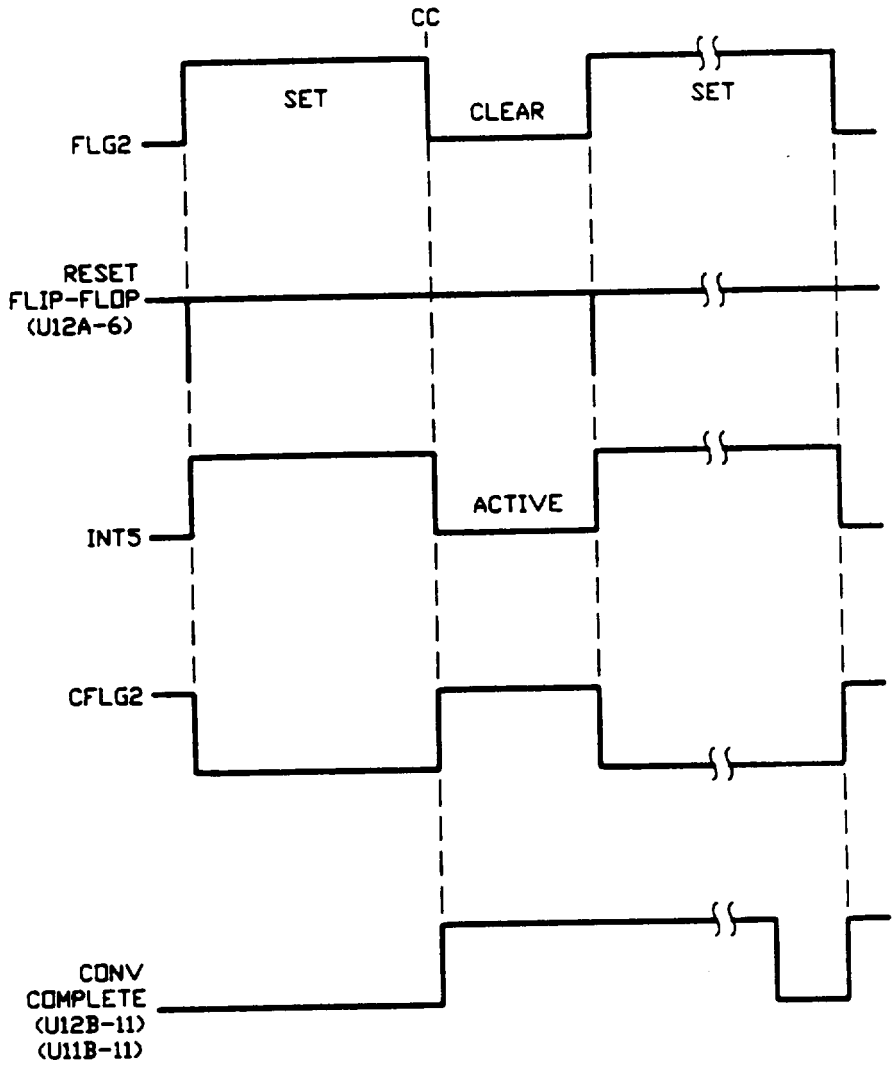


Figure 1-8. Servo Handshake Logic Timing Diagram

Table 1-7. Command Decoding

IOA bus code (negative but true)										
$\overline{\text{IOA 7}}$	$\overline{\text{IOA 6}}$	$\overline{\text{IOA 5}}$	IOA 4	IOA 3	$\overline{\text{IOA 2}}$	$\overline{\text{IOA 1}}$	IOA 0	Octal	IOA State	Command/function
										NOTE All commands require IOS (input/output strobe) signal except A/D ENABLE.
0	0	0	0	1	0	1	0	012	low	DLP (delay line preset)- Loads data bits IO0 thru IO11 into delay line preset registers U17 and U23.
0	0	0	0	1	0	1	1	013	low	ASC (antenna switch command) - Loads data bits IO0 thru IO11 into antenna baseline pair select registers U16 and U22. This command also initiates serial transfer of the DLP and ASC command to the RF processor.
0	0	0	0	1	1	0	0	014	low	SC (servo command output) - Transfers data bits IO0 thru IO5 to the digital servo group. Bit allocations are as follows: a. $\overline{\text{IO0}}$, $\overline{\text{IO1}}$ - These inputs become the respective IT0, IT1 signals, which determine audio sampling and conversion time, as

Table 1-7. Command Decoding (Continued)

IOA bus code (negative but true)										
$\overline{IOA\ 7}$	$\overline{IOA\ 6}$	IOA 5	$\overline{IOA\ 4}$	IOA 3	$\overline{IOA\ 2}$	IOA 1	IOA 0	Octal	$\overline{IOA}$ State	Command/function
0	0	0	0	1	1	0	0	014	low	SC (Continued) well as the integrator change rate on CCA A19. b. $\overline{IO4}$, $\overline{IO5}$ - These inputs become the respective AIO, AI1 signals, which control the A analog input multiplexer on CCA A19. c. $\overline{IO2}$, IO3 - These inputs become the respective ID0, ID1 signals, which determine integrator dump time on CCA A19.
0	0	0	0	1	1	0	0	014	high	A/D ENABLE - Enables I/O bus drives on CCA A19. This transfers IO data bits, representing the DF RCVR audio level, to the digital processor via the IO0 thru IO9 bus lines.

The high Q output of reset latch U5 pin 6 places DLP register U17 into the load mode of operation. This allows the DLP pulse from U9C pin 8 to transfer the IO8 through IO11 data bits into DLP register U17.

The antenna switch command (ASC) data are then placed on the 100 through IO11 bus when an antenna switch command IOA bus code is being sent. Decoder U8 provides a low output at pin 5 in response to the low IOM and antenna switch command IOA bus code. This low forces U9A high at pin 3, enabling antenna switch command gate U9D.

Enabled, U9D responds to the inverted IOS pulse from output port 2Y of the multiplexer (U3 pin 7) by producing a negative pulse at U9D pin 11. This negative pulse is transferred to the antenna switch command register (U22 pin 1) via multiplexer U3 (using input port 4A, U3 pin 14, and output port 4 Y , U 3 pin 12) and to output latch U5 pin 11. The pulse parallel loads IO0 and IO7 data bits into antenna switch command register U22. At the same time, the high Q output of latch U5A (pin 6) allows the antenna switch command pulse (from U9D pin 11) to load the IO8 through IO11 antenna switch command data bits into register U16.

The rising (trailing edge) of the negative pulse that loads data into U22 clocks and sets output latch U5B. The resulting high Q output of U5B pin 9 sets latch U5A on the positive edge of the 500-kHz clock (output of U1A).

The high Q output of reset latch U5 pin 6 places DLP register U17 into the load mode of operation. This allows the DLP pulse from U9C pin 8 to transfer the IO8 through IO11 data bits into DLP register U17.

The ASC data are then placed on the IO0 through IO11 bus when an antenna switch command IOA bus code is being sent. Decoder U8 provides a low output at pin 5 in response to the low IOM and antenna switch command IOA bus code. This low forces U9A high at pin 3, enabling antenna switch command gate U9D.

Enabled, U9D responds to the inverted IOS pulse from output port 2Y of the multiplexer (U3 pin 7) by producing a negative pulse at U9D pin 11. This negative pulse is transferred to the antenna switch command register (U22 pin 1) via multiplexer U3 (using input port 4A, U3 pin 14, and output port 4Y U3 pin 12) and to output latch U5 pin 11. The pulse parallel loads IO0 and IO7 data bits into antenna switch command register U22. At the same time, the high Q output of latch U5A (pin 6) allows the antenna switch command pulse (from U9D pin 11) to load the IO8 through IO11 antenna switch command data bits into register U16.

The rising (trailing edge) of the negative pulse that loads data into U22 clocks and sets output latch U5B. The resulting high Q output of U5B pin 9 sets latch U5A on the positive edge of the 500-kHz clock (output of U1A).

Set, output latch U5A provides a high Q output and a low a output. The high Q output switches multiplexer U3 to provide the following outputs:

Output	Signal	Function
1Y pin 4	500-kHz clock	Drives line driver U6B, providing output DT (data transfer) clock. Drives a 24-bit counter circuit (U23 and U24) via U1F.
2Y pin 7 4Y pin 12 3Y pin 9	500-kHz clock	The 2Y output drive gates U9C, U9D, and U10A. The output of U9D provides a serial shift clock to antenna switch command U16, and to analog digital connector register U22 via multiplexer output 4Y. The output of U9C providesz the serial shift clock directly to delay line preset register U23 via multiplexer output 3Y. Clocked, the delay line preset and ASC registers shift command data to the data transfer lines via NOR-gate U2C and line driver U12B.

The low Q output of output latch U5A enables the 24-bit counter circuits (U4 and U11A) through NAND gate U10B and drives NAND gates U9A and U9B high to enable antenna switch command gate U9D and delay line preset gate U9C. These gates are now used as serial shift clock drivers. The U5A low Q output also places delay line preset register U17 and antenna switch command register U16 into the serial output mode of operation.

Enabled, binary counter U4 is driven by the clock output of the multiplexer. This counter, in conjunction with J-K flip-flop U11A and NAND gate U10D, terminates the transfer operation after 24 clocks have been generated, and the complete 24-bit command has been serially clocked out to the RF processor (see Figure 1-9) . U4 pin 11 (the QD output of the binary counter) goes high on the 8th clock, then low during the 16th clock. The low transition causes flip-flop U11A to set, providing one high input to NAND gate U10D. Eight clock counts later (during the 24th clock), U4 pin 11 goes high again. This drives pin 11 of NAND gate U10D low, thereby clearing latches U5A and U5B.

Cleared, output latch U5A terminates the data transfer operation by stopping the clock. The line driver is enabled by being tied high through R4. Enabled, U6A responds to the next true (high) INT DUMP_ (from servo timing CCA A20) by providing true DT STROBE (high) and DT STROBE (low) outputs. These outputs are applied to the RF processor, which responds by loading the antenna switch command and delay line preset data into the respective decoding circuits.

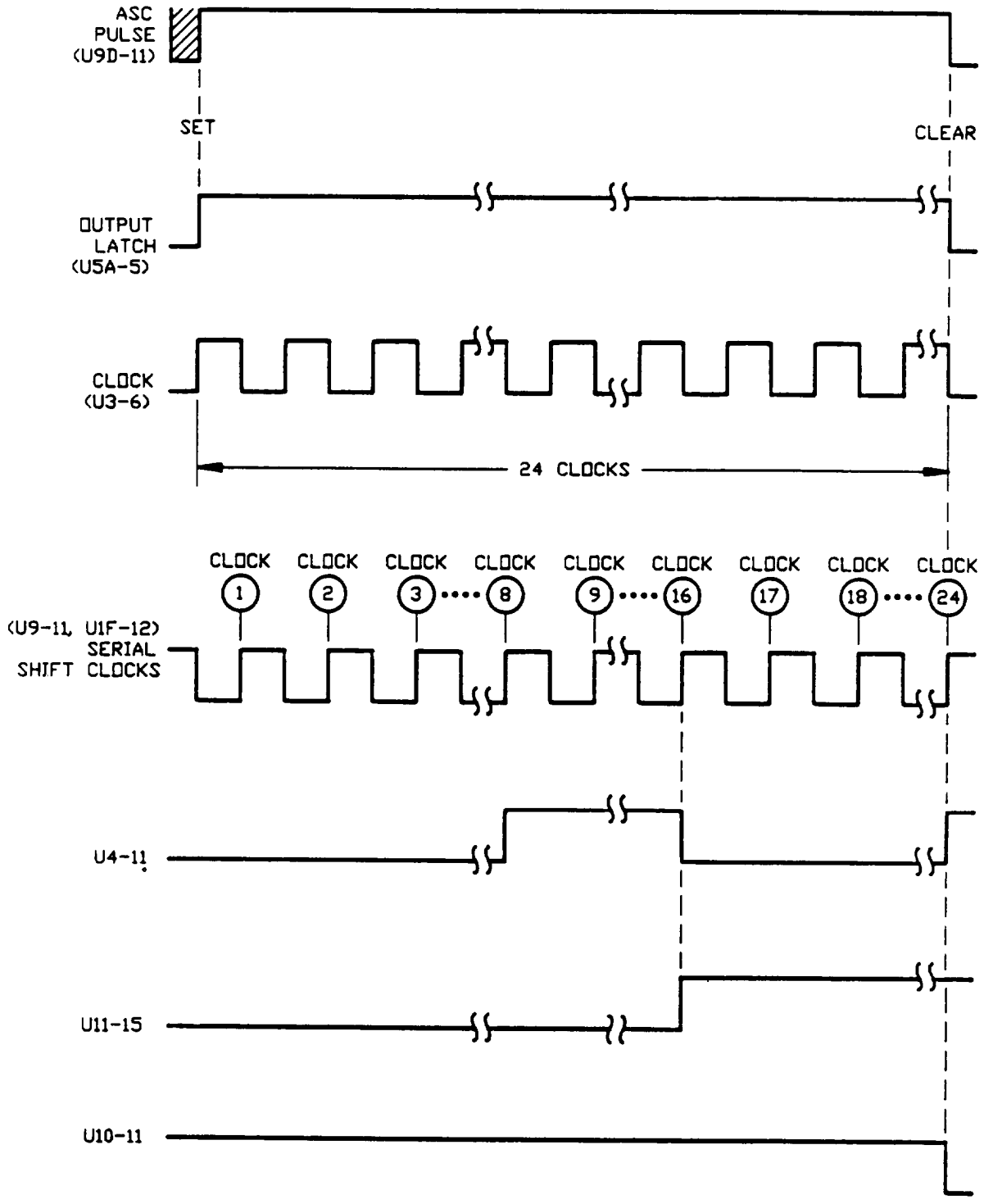


Figure 1-9. Antenna Switch Command/Delay Line Preset

1.3.3 DIGITAL PROCESSOR GROUP.

The digital processor group contains the firmware, calibration data, temporary storage capacity, and interface control to perform the following:

a. Generate a DF antenna (baseline pair) select command word, which is transferred to the RF processor via the digital servo group.

b. Generate DLP data to the RF processor (via the digital servo group) in response to the difference in DF audio inputs.

c. Accept from the digital servo group binary data derived from DF audio inputs.

d. Calculate an LOB based on the values of the binary inputs from the digital servo group.

e. Execute the DF calculation sequence of DF control self-test sequence in response to computer input commands. The resulting data are transferred to the computer via serial interface CCA A26.

The digital processor group consists of the following CCAs:

Display multiplexer CCA A1
Arithmetic logic unit (ALU) CCAs A2, A3
Program counter I/O CCAs A4, A5
Flag-jump logic CCA A6
Instruction decoder CCA A7
Processor timing CCA A8
Read only memory (ROM) extender CCA A9
8K memory buffer CCAs A10, A27
8K memory CCAs A18, A35
Random access memory (RAM) CCA A24

The digital processor group consists of a preprogrammed data processor, storage device, DF subsystem controller, and timing unit. Processing of data is performed using 16-bit data words. This processing is controlled by 24-bit instruction words that are permanently stored in the program ROMs. Processed dta are temporarily stored in RAM scratchpads. While the program instruction ROMs and calibration ROMs are permanent storage devices, the scratchpad RAM is volatile, and processed data within the RAMs are lost when the DF control loses power.

The digital processor group communicates with the digital servo and serial interface groups via a 16-bit bidirectional I/O data bus. Each interface is identified and selected by a unique 8-bit address IOA0 through IOA7) which is output by the digital processor device address register. Flag registers and interrupt logic circuits allow asynchronous data transfer between the digital processor and the addressed interface via the bidirectional input/output register (IOR).

The ALU provides mathematical and logical processing of digital processor data. All other elements feed data to the ALU for processing, retrieving processed data from the ALU for storage, or transferring data to other system units.

Data are fed into the ALU via the source bus and the operand bus. A source is any digital processor storage element (i.e., register or RAM) selected to provide data to the 16-bit source bus (SO through S15). The operand bus is an exclusive ALU register data path to the ALU. One of eight ALU registers combined with the source bus data input may be selected to input data via the operand bus for arithmetic or logical processing. The ALU registers may provide data inputs to the ALU via the operand bus and source bus at the same time. A clock pulse loads ALU processed data on the destination bus into a selected register or memory element (RAM).

A source driver, destination bus recipient, or any of the following registers may be the scratchpad (RAM):

IRAR (interrupt return address register)
STKP (stack pointer register)
DEVR (device address register)
IOR (input/output register)
MAR (scratchpad/memory address register)
PC (program counter)
ALU register 0 through 7 (eight registers)

Only the timer register receives data from the destination bus.

When performing I/O operations, data are transferred from the designated source to the source bus, through the ALU, into the designated storage element via the destination bus. This transfer occurs because the ALU is configured to do nothing during this operation.

The ALU is completely bypassed during the load-immediate operation and transfers 16 instruction word bits (IR6 through IR21) directly to the destination bus via the load-immediate bus drivers.

The 16-bit data on the source bus, the destination bus, the operand bus, the I/O bus, and the load-immediate bus use negative true logic. That is, a logic 1 bit equals approximately 0 V, while a logic 0 bit equals approximately +4V. The ALU performs negative true arithmetic and logical processing of data.

1.3.3.1 Simplified Digital Processor Operation. During a typical digital processor operation cycle, the program counter addresses the instruction ROMs with RAD0 through RAD15 (positive true ROM address

bits) . The ROM OUTPUT, a 24-bit instruction word (INB0 through INB23 positive-true bit), is decoded in instruction decoder CCA A7 and processor timing CCA A8. As a result of this decoded instruction, the following occurs:

(1) A storage element is selected to drive the source bus.

(2) An ALU register is selected to drive the operand bus.

(3) The ALU is configured to process data received from the source bus and the operand bus.

(4) The program counter is advanced to the address (RAD0 through RAD15) of the next ROM instruction to be executed.

(5) A storage element is selected to receive the processed data (i.e., ALU output) via the destination bus.

1.3.3.2 Key Digital Processor Elements. Table 1-8 lists the key digital processor elements and the hardware components which comprise these elements.

Table 1-8. Digital Processor Elements

Element	Hardware Implementation/Function
Interrupt Return Address Register (IRAR)	CCA A4 U29 (S0-S3, D0-D3 data) Registers U26 (S4-S7, D4-D7 data) CCA A5 U29 (S8-S11, D8-D11 data) Registers U26 (S12-S15, D12-D15 data)
Stack Pointer Register (STKP)	CCA A4 U17 (S0-S3, DO-D3) * Registers U18 (S4-S7, D4-D7) * CCA A5 U17 (S8-S11, D8-D11) * Registers U18 (S12-S15, D12-D15) * * Source bus drivers: CCA A4: U16, U19, U20, U21 (S0-S7) CCA A5: U16, U19, U21 (S8-S15)
Device Address Register (DEVR)	CCA A4 U7 (S0-S3, D0-D3) & (IOA0-IOA3) ** Registers U8 (S4-S7, D4-D7) * (IOA7-IOA7) ** * Source bus drivers: CCA A4: U14 and U15 ** I/O device address bus drivers: CCA A4: U16 and U21

Table 1-8. Digital Processor Elements (Continued)

Element	Hardware Implementation/Function
Input/Output (data) Register (IOR)	CCA A4 U6 (S0-S3, D0-D3) * (IO0-IO3) ** Registers U1 (S4-S7, D4-D7) * (IO4-IO7) ** CCA A5 U6 (S8-S11, D8-D11) * (IO8-IO11) ** Registers U1 (S12-S15, D12-D15) * (IO12-IO15) ** * Source bus drivers: CCA A4: U13, U28(S0-S3); U2, U24 (S4-S7) CCA A5: U13, U28 (S8-S15, U2, U24 (S12-S15) ** I/O bus drivers: CCA A4: U13 (IO0-IO5); U2 (IO4-IO7) CCA A5: U13 (IO8-IO11); U2 (IO12-IO15)
Program Counter (PC)	CCA A4 U4 (bits 0-3) (D0-D11) ALUs U3 (bits 12-15) (D12-D15) PC Registers CCA A5 U11 (bits 8-11) U10 (bits 12-15) Source bus drivers: CCA A4: U19 and U20 (S0-S7) CCA A5: U19 and U20 (S8-S15) Program ROM address buffers: CCA A4: U30 (RAD0-RAD3), U22 (RAD4-RAD7) CCA A5: U30 (RAD8-RAD11), U22 (RAD12-RAD15)
Scratchpad Memory Address Register (MAR)	CCA A2 U16 (S0-S3, D0-D3) * (SPAD0-SPAD3) ** Registers U20 (S4-S7, D4-D7) * (SPAD4-SPAD7) ** CCA A3 U16 (S8-S11, D8-D11) * (SPAD8-SPAD11) ** Registers U20 (S12-S15) * (SPAD12-SPAD15) ** * Source bus drivers: CCA A2: U23, U26 (S0-S7) CCA A3: U23, U26 (S8-S15) ** Scratchpad memory address bus buffers: CCA A2: U15 (SPAD0-SPAD3), U28 (SPAD4-SPAD7) CCA A3: U15 (SPAD9-SPAD11), U28 (SPAD12-SPAD15)

Table 2-8. Digital Processor Elements (Continued)

Element	Hardware Implementation/Function

ALU REGISTER	WRITE ADDRESS (DESTINATION FIELD)				OPERAND FIELD READ ADDRESS*			SOURCE FIELD ADDRESS*			
	INB3	INB2	INB1	INB0	INB17	INB16	INB15	INB21	INB20	INB19	INB18
0	1	0	0	0	0	0	0	1	0	0	0
1	1	0	0	1	0	0	1	1	0	0	1
2	1	0	1	0	0	1	0	1	0	1	0
3	1	0	1	1	0	1	1	1	0	1	1
4	1	1	0	0	1	0	0	1	1	0	0
5	1	1	0	1	1	0	1	1	1	0	1
6	1	1	1	0	1	1	0	1	1	1	0
7	1	1	1	1	1	1	1	1	1	1	1

ALU REGISTER DATA WORD

CCA A2								CCA A3							
BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	BIT 9	BIT 10	BIT 11	BIT 12	BIT 13	BIT 14	BIT 15
U4	U1	U3	U2	U5	U7	U14	U12	U4	U1	U3	U2	U5	U7	U14	U12

* PART OF INSTRUCTION WORD

Program ROMS

See Figure FO-3, which is a mechanical simulation showing ROM storage location selection in response to the RAD0-RAD15 address input. The address bits are reformatted in the following manner:

Address Bits	Function
RAD10 - RAD15	Selects ROM CCA
RAD8 - RAD9	Selects ROM CCA device
RAD0 - RAD7	Selects ROM CCA device storage location

Table 1-8. Digital Processor Elements (Continued)

Element	Hardware Implementation/Function
16-bit (calibration) ROMS	Permanent storage for DF calibration data is provided by 8K memory CCA A35. The SPAD0-SPAD15 address inputs select one of 8,192 calibration data words. The addressed 16-bit calibration word is output to the MS0-MS15 lines via 8K memory buffer A27. See Figure FO-4, which is a mechanical simulation showing calibration ROM storage location selection in response to the SPAD0-SPAD15 address input. The address bits are reformatted in the following manner: Address Bits — Function SPAD10 - SPAD15 — Selects calibration ROM CCA SPAD8, SPAD9 — Selects calibration ROM CCA devices SPAD0 - SPAD7 — Selects calibration ROM ROM CCA device storage location

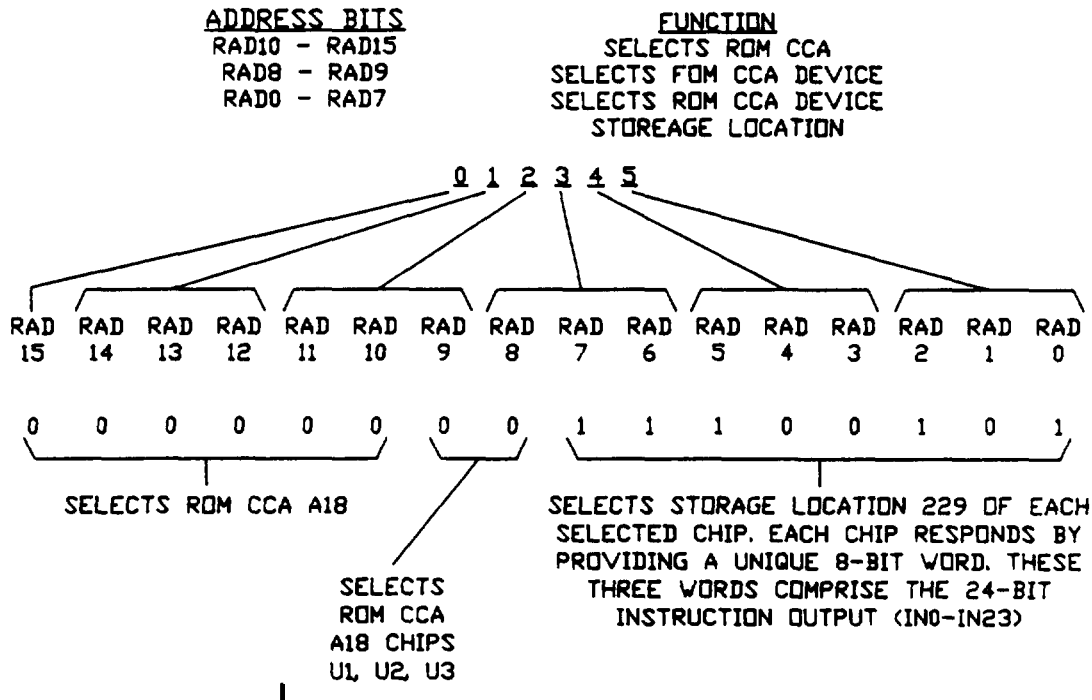
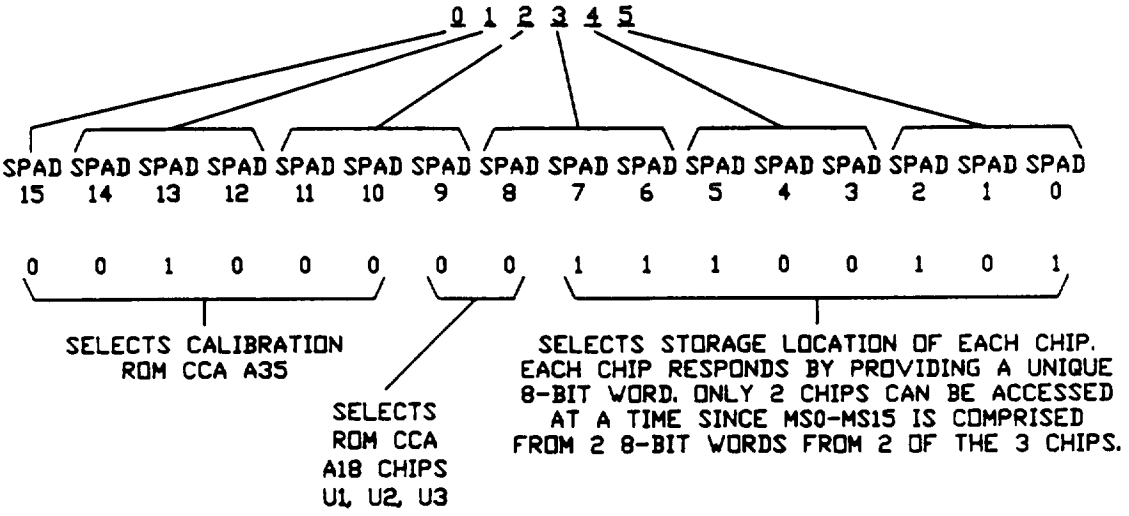


Table 1-8. Digital Processor Elements (Continued)

Element	Hardware Implementation/Function
	
RAM (Scratchpad) Memory	See Figure FO-4. RAM CCA A24 is addressed when SPAD11-SPAD15 are all 0s. SPAD0-SPAD10 selects one of 2,048 16-bit storage locations.
Carry Register	Instruction decoder CCA A7, register U2, and inverter U15.
Overflow Register	Instruction decoder CCA A7, register U7, NAND gate U13, and inverter U15.
Timer	Timer register: CCA A8; U15B, U25A, and U25B Time clock generator: CCA A7; U5 Timer counter: CCA A11; U11, U12, U15, and U16
Spin Register (scratchpad input)	CCA A2 Registers U21 (SPIN0-SPIN3) U27 (SPIN4-SPIN7) CCA A3 Registers U21 (SPIN8-SPIN11) U27 (SPIN12-SPIN15)

1.3.3.2.1 Interrupt Return Address Resister (IRAR). The IRAR is a special-purpose 16-bit register. It can be loaded from the destination bus (D0-D15) or selected to place data onto the source bus (S0-S15). This register retains the contents of the program counter when an interrupt sequence is executed.

1.3.3.2.2 Stack Pointer Resister (STKP). The STKP is a 16-bit register that can be loaded from the destination bus or selected to place data on the source bus. In addition, it can be incremented or decremented by one count during an I/O-control type of instruction. This register serves as an index pointer to a reserved group fo words in the scratchpad RAM memory, which is referred to as the stack. The stack is used to store subroutine return addresses with associated data. In response to an interrupt by certain programs, the contents of all the processor registers are loaded into the stack.

1.3.3.2.3 Device Address Register (DEVR). The DEVR can be loaded from the eight least significant bits of the destination bus and can be selected to place data on the eight least significant bits of the source bus. The output of the register drives the 8-bit I/O device address bus (IOA0 - IOA7) that selects the digital servo or serial interface for communication with the digital processor.

1.3.3.2.4 Input/Output (Data) Register (IOR). The IOR is a 16-bit register that provides a means for data exchange between the digital processor and an addressed interface. When an I/O input operation is executed, data from an addressed interface are loaded into the IOR via the I/O bus. The data are then transferred into a designated digital processor storage element via the source bus and the destination bus. An output I/O operation loads data from a digital processor storage element into the IOR via the source bus and destination bus. The data are then transferred to an addressed interface via the I/O bus.

1.3.3.2.5 Program Counter (PC). The PC is a 16-bit register that contains the address of the next instruction in the ROM program to be executed. It is incremented by one count during each instruction cycle so that the next instruction to be executed is the one at the next higher program address.

The contents of the PC may be changed during the execution of an instruction in order to cause a conditional or unconditional branch in the program. A jump instruction can cause the eight least significant bits of the PC to be incremented or decremented by an amount corresponding to the value contained in the relative address field of that instruction. The eight most significant bits can also be modified during a jump instruction if the add or subtract from the lower order bits results in the generation of a carry or borrow. Thus, a jump instruction can cause the PC to move ahead by up to 256 program steps or back by as many as 254 steps. The difference is due to the fact that the PC has already been incremented by 1 prior to the addition or subtraction of the relative address. The PC can also be loaded directly from the destination bus or selected to place data on the source bus. An unconditional jump can therefore be caused by any instruction that designates the PC as the destination. When the processor has been halted, the PC can also be loaded from the address of the digital processor test set. This permits testing of basic PC

functions as well as providing ameans to manually force the program to a particular entry point.

The output of the PC drives the 16-bit ROM address bus (RAD0 - RAD15). It is the address on this bus that selects the next program instruction to be loaded from the ROM program into the instruction register.

1.3.3.2.6 Scratchpad Memory Address Register (MAR). The MAR is a 16-bit register that can be loaded from the destination bus or selected to put data on the source bus. In addition, it can be incremented or decremented by one count in a load-immediate or I/O-control type of instruction. The MAR also drives the memory address bus (SPAD0 - SPAD15). This 16-bit bus selects the scratchpad memory storage location to be accessed by the read or write instruction. In addition, the MAR selects the 16-bit ROM that outputs only to the source bus.

1.3.3.2.7 ALU Registers. The eight ALU registers (R0 - R7) in the processor are data storage elements, each of which stores one 16-bit data word. Only these registers can place data on the operand bus. Therefore, when an ALU operation, such as add, subtract, AND, OR, XOR, is to be performed on the two data words, one of the data words must be from an ALU register. There is no restriction on the use of the registers, as far as selection of the same or different registers to drive the source and operand buses or to be loaded from the destination bus.

1.3.3.2.8 Program ROMs. One 8K memory ROM CCA provides permanent storage for up to 8,192 24-bit instruction words that control digital processor operation. Instruction words are selected by the 16-bit RAD0 - RAD15 input from the program counter CCA. The INB0 - INB23 bits are output via one 8K memory buffer CCA A10 during T1 of every instruction cycle.

1.3.3.2.9 16-Bit Calibration ROMs. One 8K memory buffer provides permanently stored DF calibration data. One of 8,192 data words are selected by the SPAD0 - SPAD15 address input. The addressed 16-bit calibration word is output to the MS0 - MS15 lines via ROM buffer CCA A27.

1.3.3.2.10 RAM (Scratchpad) Memory. RAM CCA A24 decodes the SPAD0 - SPAD15 address word and selects one of 2,048 available locations for temporary storage (writing) or retrieval of a 16-bit data word. SPIN0 - SPIN15 data, obtained from the destination bus via SPIN drivers on CCA A2 and A3, are written into the selected RAM storage location. Data read out of the RAM CCA are applied to the source bus drivers on CCAs A4 and A5 via the MS0 - MS15 lines.

1.3.3.2.11 Carry Register The carry register is a 1-bit storage register that indicates a carry or borrow occurred from the most significant position (ALU15) of the 16-bit output of the ALU (ALU0 - ALU15). The carry register is also used in conjunction with shift operations to implement multiple word shifts. The state of the carry register after the execution of an arithmetic instruction is independent of the state of the register prior to the instruction. It

need not be cleared prior to the execution of an arithmetic or shift operation. The state of the carry register is inhibited from changing during the jump and load-immediate classes of instruction.

1.3.3.2.12 Overflow Register. The overflow register is a 1-bit storage register used to indicate that a carry or borrow has occurred in the most significant position (ALU14) of the 16-bit output of the ALU (ALU0 - ALU15). This causes the sign bit (ALU15) to change because the range of numbers that can be accommodated in 16-bits had been exceeded. For example, 16384 + 16384 = 32768. However, in binary notation this is:

0100000000000000 + 0100000000000000 = 1000000000000000

The addition of these two numbers has caused the sign bit (ALU15) to change, indicating that the result is negative. This operation causes the overflow bit to set, indicating that the result is not truly negative but that the range of possible numbers has been exceeded. The OVFL signal bit can also be set (equals 1) as the result of an arithmetic left shift in which the bit being shifted out of the next to the most significant bit (ALU14) is different from the sign bit. Once set, the overflow register can only be cleared by an I/O-control instruction.

1.3.3.2.13 Timer. The timer is used to provide variable length time delays for digital processor operations. The timer clock generator consists of a binary counter which clocks the timer counter once every 16 instruction cycles. Clocked, the counter counts down from a preset number until a terminal (zero count) is reached. Then a TDGB pulse is generated, which sets the timer register. The resulting active (low) TIMER output is applied to the decision logic of flag jump logic CCA A6. The timer counter is preset to a starting count with data from the destination bus.

1.3.3.2.14 Scratchpad Input Register (SPIN). The SPIN registers are 16-bit, negative-true data latches that receive data from the destination bus in response to MEMCL (memory clock). Data is these registers are written into RAM memory by the SPW0 and SPW1 signals.

1.3.3.3 Digital Processor Timing. The digital processor retrieves a set of programmed instructions from the ROMs and executes the functions prescribed by these instructions. Each instruction execution cycle is divided into a discrete time interval. (See Figures FO-5 and FO-17.) At time T1 of the instruction cycle, the 24-bit instruction word from the ROM CCA is clocked to the instruction register. The resulting decoded instruction bits perform the following:

a. Gate data to the source and operand buses during time T1.

b. Load the address of the next sequential instruction during time T2.

c. Execute the operations dictated by the decoded instructions during execution times T2, T3, and T4.

d. Load the results of performed operations into a designated register via the destination bus during time T4.

Several other digital processor operations occur during time T4. These include incrementing or decrementing the scratchpad (RAM) address or stack pointer register; setting, clearing, or complementing the carry register; and clearing the overflow register. Should the contents of the program counter register be changed (by a conditional jump or load-immediate instruction), the change is performed during time T4.

The remaining T5 and T6 instruction cycle times are allocated for access time to the ROM, write cycles of the RAM scratchpads (SPW0, SPW1), generation of I/O signals, execution of a conditional jump operation, or execution of an interrupt sequence.

The processor timing functions are performed in part by processor timing CCA A8. All timing functions are derived from 5-MHz crystal clock Y1 and the timing logic consisting of U5, U4, U6, U11, and U3. J-K flip-flops U3 and U11 form a two-stage ring counter, the four states of which determine times T1, T2, T3, and T4. This two-stage ring counter sequences through four possible states two times to generate a full-length instruction. J-K flip-flops U4 and U5 to form a modified ring counter that has three possible states. The three states of this counter determine which subcycle of an instruction is to be executed, T1 to T4, T4 to T6, or T6 to T1. U5 and U4 are clocked by the complement of the clock signal used to drive U3 and U11.

Signals ICLK and $\overline{\text{EXEC}}$ are decoded from the states of U3 and U11 by gates U10 pin 6 and U2 pin 6, respectively. The leading edge of ICLK occurs at time T1 and is used to clock the next instruction to be executed into the instruction register. The trailing edge of ICLK occurs at time T2 and is used to increment the program counter.

The trailing edge of $\overline{\text{EXEC}}$ occurs at time T4 and clocks the data on the destination bus into the assigned location. When a conditional jump instruction modifies the contents of the program counter, the modified program address is clocked into the program counter at time T4.

The conditions that require full length instructions (ROM access time, memory as the destination, I/O strobe pulse, load-immediate to program counter or a conditional jump, modification of the contents of MAR, or incrementing or decrementing the STKP) are ORed by U12 to control the length of the instruction cycle. When these conditions are not active, a high-speed ROM instruction cycle may be initiated by a low HSROM signal. This input is inverted by U8 and the resulting high drives the output of enabled NAND gate U12 low. This low prevents the setting of J-K flip-flop U4. Since U4 remains cleared, J-Ks U5 and U6 cannot be toggled to provide T5 and T6 cycles. NAND gates U2 and U10, however, remain enabled by the high Q output of U4 pin 6, permitting generation of a high speed T1 through T4 instruction cycle.

1.3.3.4 Manual Digital Processor Control. (See Figure FO-17.) Additional logic is used in conjunction with the processor timing logic to provide the following manual processor control functions:

RUN, HALT, SINGLE STEP, PRESET, and BREAK POINT. These functions are not accessible during normal operating conditions because these switches are mounted on the digital processor test set.

The RUN and HALT control functions manually start and stop the execution of the program. The run/halt condition is determined by the state of the latch consisting of U21 pin 6 and U17 pin 8. In the run mode, U17 pin 8 is high. Pressing the HALT switch causes the HALT signal to go low, clering the latch. Similarly, a programmed halt clears the latch when U17 pin 12 goes low as a result of an I/O control instruction in which bit 12 of the instruction is high.

Pressing the RUN switch causes the output of the switch debounce circuit, composed of U22 pin 3 and U22 pin 6, to change state. U15 toggles to the set condition on the falling edge of the output of the switch debounce circuit, causing the run/halt to change state to the run condition. At time T3 of the first instruction to be executed, U15 is cleared. This circuit ensures proper operation of the processor in the event that a halt instruction of a break point occurs before the operator can release the RUN switch.

The SINGLE STEP switch causes the processor to execute one instruction if the processor is in the halt mode. The logic associated with the SINGLE STEP switch (U9 pin 3, U9 pin 6, and U14 pin 2) operates in the same manner as the RUN switch logic. The exception is that the single step function causes a full-length instruction cycle, and U14 pin 2 is cleared between time T4 and T5 of the instruction cycle.

The PRESET switch causes the contents of the program counter to be replaced with the address indicated by the ADDRESS switches. The switch debounce circuit formed by U22 pin 8 and U22 pin 11 in conjunction with J-K flip-flop U14 pin 6 operates in the same manner as the SINGLE STEP switch. However, the EXEC signal is inhibited by the preset function so that no instruction is executed, and the program counter is parallel loaded from the ADDRESS switches.

The BREAK POINT switch causes the processor halt when the program address, indicated by the ADDRESS switches occurs. When the processor is in the halt mode, pressing the BREAK POINT switch causes the latch formed by U17 pin 8 to go high and U10 pin 12 to be set. The ADEQ0 signal goes high when the selected address occurs in the execution of the program causing J-K flip-flop U11 pin 5 to toggle to the set state. This, in turn, causes the processor to halt, and simultaneously clears the break point latch. Once the processor has halted at the selected address, the BREAK POINT switch must be pressed again if the processor is to be halted at another break point.

1.3.3.5 Instruction Words and Decoded Functions. See Figure 1-10 for instruction word format. During time T1, ICLK (instruction clock) loads the 24-bit output of the ROM buffers, instruction bits INB0 through INB23, into the appropriate instruction registers. Instruction bits INB4 through INB23 are loaded into instruction registers U28, U19, U25, U24, and U26 of instruction decoder CCA A7. Bits INB0 through INB3 are loaded into destination register U26 of processor timing CCA A8. The two most significant bits (INB23 and INB22) in the instruction registers determine the class of instruction.

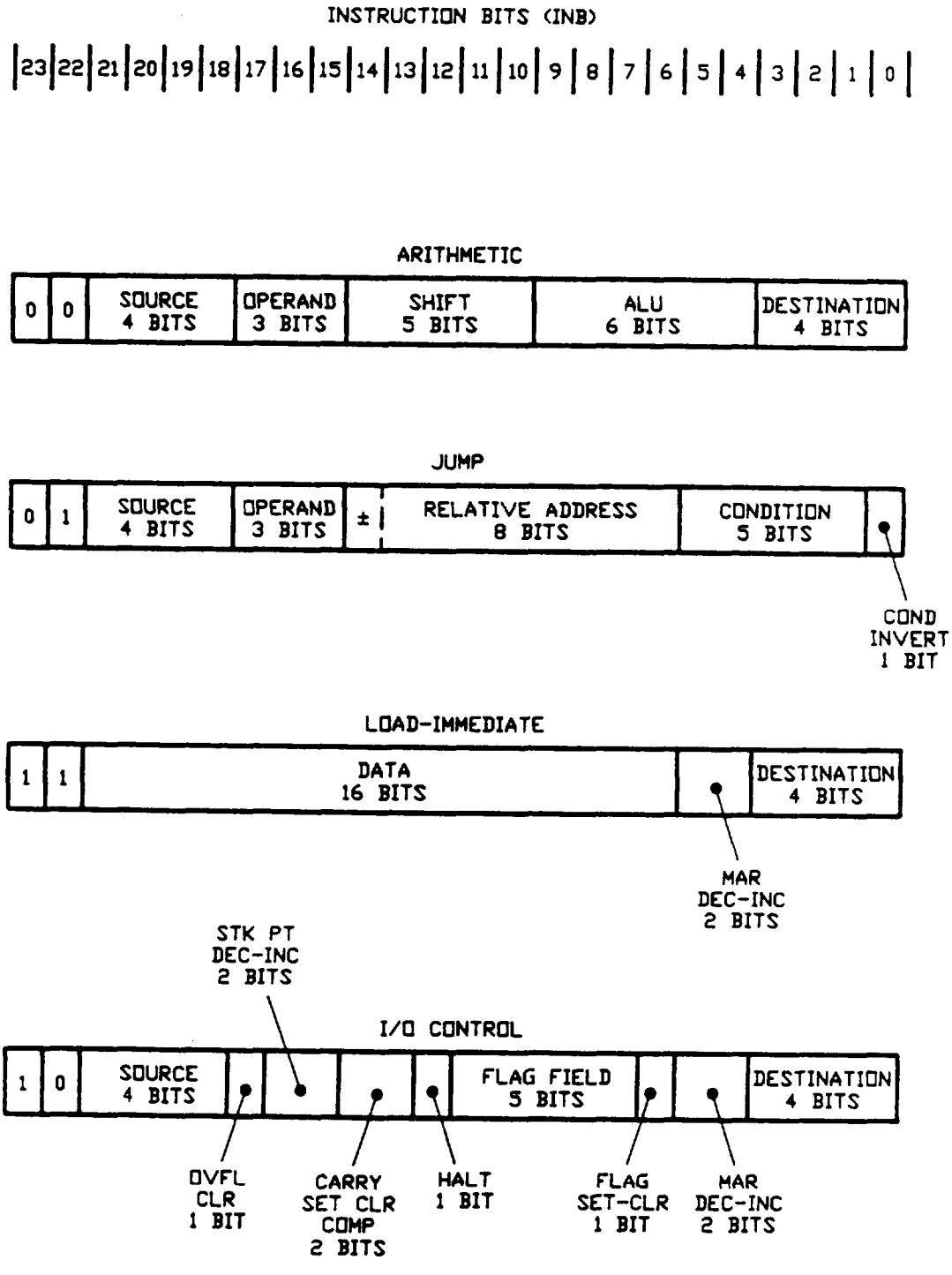


Figure 1-10. Instruction Word Formats

The four classes of digital processor instructions are arithmetic, jump, load-immediate, and I/O control. Table 1-9 lists the instruction class, the code, the primary decoding circuits and instruction decoder output that results from input bits 23 and 22 of the instruction word.

Table 1-9. Instruction Class Decoding

	Instruction Bits (positive true)			CCA A7 Output (negative true)			
Instruction Class	INB 23	INB 22	CCA A7 Decoder Circuit	$\overline{\text{ALUG}}$ (Pin 86) 0 = True	$\overline{\text{JMP}}$ (Pin 59) 0 = True	$\overline{\text{LIG}}$ (Pin 87) 0 = True	$\overline{\text{I/O}}$ (Pin 41) 1 = True
Arithmetic	0	0	U10	0	1	1	o
Jump	0	1	U11	1	0	0	0
Load-Immediate	1	1	U10	1	1	0	0
I/O Control	1	0	U27	0	1	1	1

1.3.3.5.1 Arithmetic Instruction. The arithmetic instruction selects two inputs to arithmetic logic unit CCA A2 and A3, indicating the arithmetic or logical operation to be performed, then shifting the ALU output and interpreting the results into carry and overflow register status signals. The arithmetic instruction word then designates the digital processor register, which will receive the data resulting from the ALU operations.

1.3.3.5.1.1 Class Field (INB22 and INB23). This portion of the instruction word identifies the arithmetic function. When INB22 and INB23 are false (low), a true (low) ALUG (arithmetic/logic unit gate) signal is generated by the class decoding circuits on instruction decoder CCA A7, while all other function signals (i.e., JMP, LIG, and I/O) are false. ALUG gates the output of the arithmetic logic unit CCAs to the destination bus.

1.3.3.5.1.2 Source field (INB18 through INB21). (See Figure 1-11.) The source field code designates a digital processor register as one of the data inputs to the arithmetic logic unit CCAs. During time T1, ICLK loads the instruction bits into the instruction registers on CCA A7. The resulting IR18 through IR21 output bits are translated by source bus decoder U23 into a gate, which enables the output of the selected register to the source bus. When INB21 (and the resulting IR21) bit is a 1, IR20, IR19, and IR18 select one of the eight ALU registers to drive the source bus. When the source field code is 0111_2, no register is selected, and the source bus data equals 0.

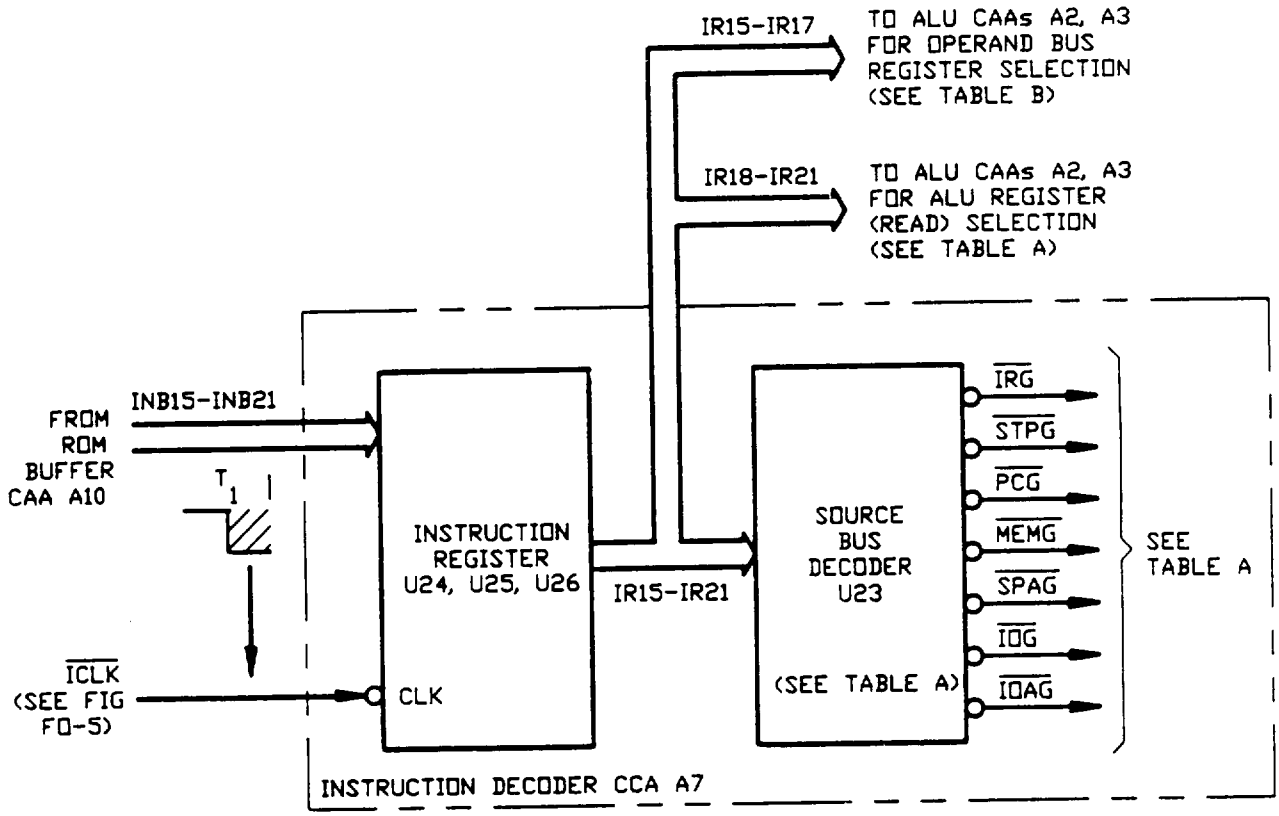


TABLE A
SOURCE DECODING

INB/IR				MNEMONIC	SELECTED SOURCE
21	20	19	18		
0	0	0	0	INTERRUPT RET GATE (IRG)	INTERRUPT RET REG
0	0	0	1	STACK POINTER GATE (STPG)	STACK POINTER REG
0	0	1	0	PROGRAM COUNTER GATE (PCG)	PROGRAM COUNTER
0	0	1	1	MEMORY GATE (MEMG)	RAM OR CAL ROM
0	1	0	0	MEMORY ADDRESS GATE (SPADG)	MEMORY ADDRESS REG
0	1	0	1	I/O DATA GATE (IOG)	I/O DATA REGISTER
0	1	1	0	I/O ADDRESS GATE (IOAG)	I/O ADDRESS REGISTER
0	1	1	1		NONE
1	0	0	0		ALU REGISTER 0
1	0	0	1		ALU REGISTER 1
1	0	1	0		ALU REGISTER 2
1	0	1	1		ALU REGISTER 3
1	1	0	0		ALU REGISTER 4
1	1	0	1		ALU REGISTER 5
1	1	1	0		ALU REGISTER 6
1	1	1	1		ALU REGISTER 7

TABLE B
OPERAND DECODING

INB/IR			OPERAND BUS SELECTION
17	16	15	
0	0	0	ALU REGISTER 0
0	0	1	ALU REGISTER 1
0	1	0	ALU REGISTER 2
0	1	1	ALU REGISTER 3
1	0	0	ALU REGISTER 4
1	0	1	ALU REGISTER 5
1	1	0	ALU REGISTER 6
1	1	1	ALU REGISTER 7

Figure 1-11. Source/Operand Bus Select

1.3.3.5.1.3 Operand Field (INB15 through INB17). (See Figure 1-11.) The operand field selects one of the eight ALU registers as the second input to the ALU circuits. Output bits IR15 through IR17 result from the INB15 through INB17 inputs to instruction registers U24 and U25. These instruction register bits select the ALU register to drive the operand bus (as shown in Figure 1-11, Table B).

1.3.3.5.1.4 ALU Function Control Field (INB4 through INB9). (See Figure FO-6.) The ALU function control field determines which operation arithmetic or logic is performed on the source bus (SOR) and operand bus (OP) data input to the ALU circuits. The 5-bit control field code is translated by the decoding circuits of CCA A7 in the following manner:

a. INB4 is converted into the $\overline{CN}$ or carry input signal to the ALU. When an arithmetic or logic operation is to be executed, an additional operation interprets a high **CN** as a carry input. A low **CN** means no carry input. A subtraction operation interprets a high **CN** as a no-borrow condition while a low $\overline{CN}$ is a true-borrow condition.

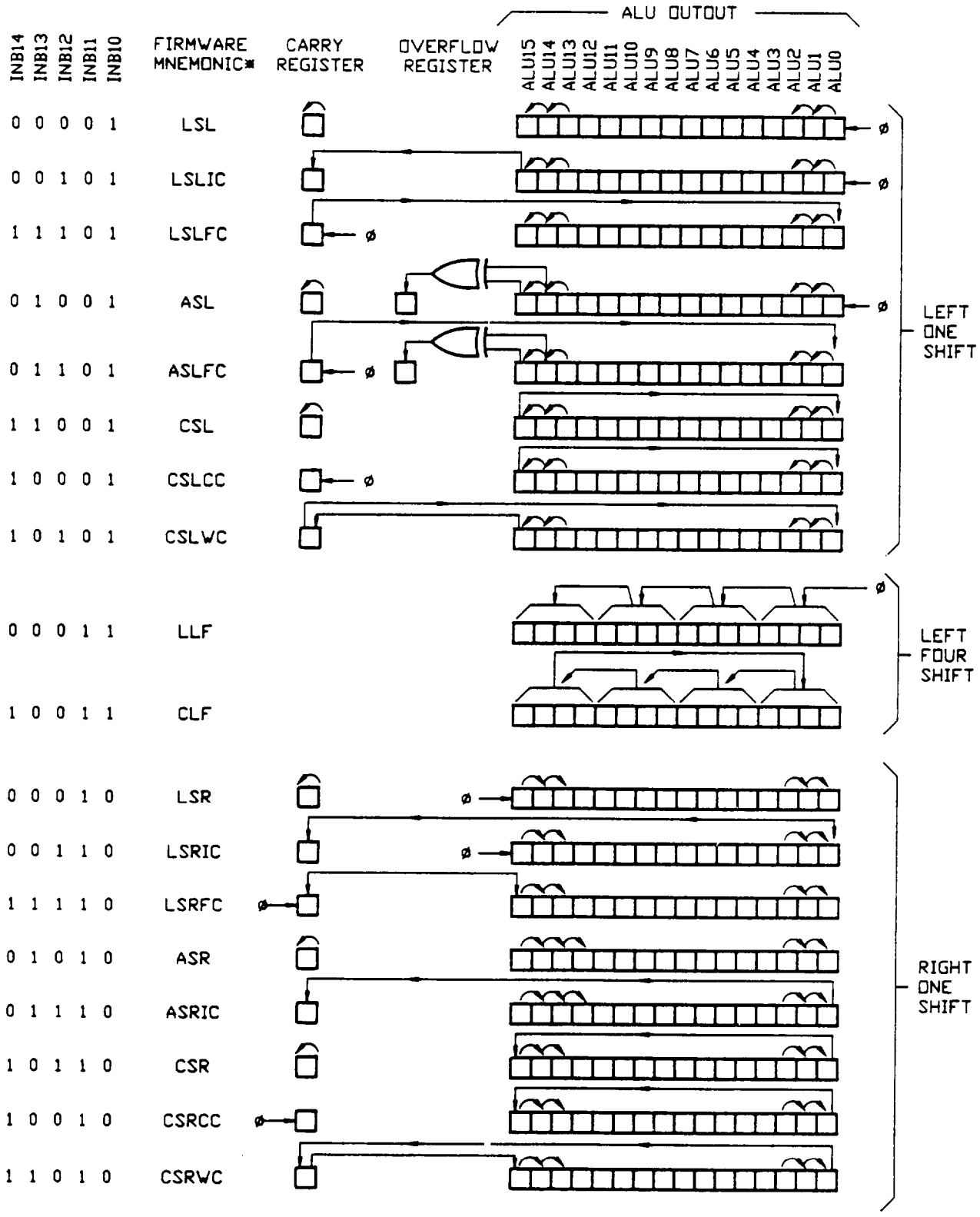
b. INB5 converts into the M (mode control) signal and causes the ALU to perform logical combining of the input data when high. When M is low the ALU performs arithmetic functions.

c. INB6 through INB9 are converted into AS0, AS1, AS2, and AS3 (ALU select) bits. These inputs to the ALU define the specific arithmetic or logic operation performed. The resulting ALU output data, i.e., ALU0 through ALU15, together with a resulting carry (or borrow) CN15 are applied to the shift multiplexer circuits for further processing.

1.3.3.5.1.5 Shift Field (INV10 through INB14). (See Figure 1-10.) The shift field determines which shift operation is to be performed on the 16-bit data (i.e., ALU0 through ALU15) resulting from the ALU operation. The INB12 through INB14 shift field bits determine whether a carry or overflow (resulting from the ALU calculation) is stored or discarded. In addition, these three bits cause the shifted data to wrap around, or be displaced by 0. The actual shift is controlled by the state of INB10 and INB11.

When a no shift operation is to be performed, the 16-bit output of the ALU calculating circuits, ALU0 through ALU15, is transferred to the respective destination bus lines DO through D15. A 1-bit shift right. operation causes the ALU1 bit to be transferred to the DO line, the ALU2 bit to the D1 line, and so forth. Each ALU bit is offset to the right of its respective destination busline. The most significant ALU bit (ALU15) is transferred to the **D14** line. The state of the **D15** line is determined by the INB12, INB13, and INB14 instruction bits.

Figure 1-12 shows the shift field bit codes and the shift functions performed as a result of this operation, and Table 1-10 defines the associated firmware mnemonics. Figure FO-7 shows the digital processor hardware that performs these functions. The response of the ALU shift circuits to the arithmetic shift field code can be seen on Figure FO-7, Tables A through F. When the shift field contains the



*SEE TABLE 2-10 FOR FIRMWARE MNEMONIC DEFINITIONS

Figure 1-12. Shift Functions

Table 1-10. Firmware Shift Mnemonic Definitions

Firmware mnemonic[1]	Function
LSL	Logic shift left. All ALU bits are shifted to the left by one. The OL1 (least significant shift left variable) equals 0 and is placed in the ALU10 position. The displaced ALU15 bit is not used and the carry register remains unchanged.
LSLIC	Logic shift left, including carry. Same as LSL except. the displaced ALU15 bit is loaded into the carry register.
LSFLC	Logic shift left from carry. The carry register output bit is displaced into the ALU0 bit position while all ALU bits are shifted to the left by one position. The displaced ALU15 bit is lost. After the shift operation, the carry register is cleared (loaded with a 0 bit).
ASL	Arithmetic shift left. All ALU bits, except $\overline{\text{ALU15}}$, are shifted to the left by one position. ALU15 and the carry register remain unchanged. Variable bit OL1 equals 0 and is loaded into the ALU0 position. If, as a result of the shift operation, **ALU15** and **ALU14** bits are different, the overflow register is set (loaded with a 1).
ASLFC	Arithmetic shift left from carry. All ALU bits are shifted to the left by 1, except ALU15. ALU15 remains unchanged. the carry register bit is shifted into the bit position vacated by ALU0. The carry register is then cleared (loaded with a 0 bit). If the bit shifted into the ALU14 position is different from ALU15, the carry register is set (loaded with a 1 bit).
CSL	Circulate shift left. All ALU bits are shifted left by one position. The ALU15 bit is shifted into the ALU0 position. The carry register remains unchanged.
CSLCC	Circulate shift left, clear carry. Same as CSL, except carry register is cleared (loaded with a 0 bit).
CSLWC	Circulate shift left with carry. All ALU bits, including the carry register bit, are shifted to the left by one bit position. The carry register bit is displaced by the ALU15 bit, while the carry register bit displaces ALU0.

[1] These mnemonics represent the INB10 thru INB14 codes during an arithmetic instruction, not signal lines.

Table 1-10. Firmware Shift Mnemonic Definitions (Continued)

Firmware mnemonic[1]	Function
LLF	Logic shift left four. All ALU bits are shifted to the left by four positions. ALU15, ALU14, ALU13, and ALU12 are lost. ALU0, ALU1, ALU2, and ALU3 bit positions are displaced by respective variable bits 4L0, 4L1, 4L2, and 4L3. All variable bits equal 0.
CLF	Circulate left four. Same as LLF except ALU15, ALU14, and ALU13 become variable bits 4L3, 4L2, 4L1, and 4L0, which are shifted into respective ALU3, ALU2, ALU1, and ALU0 positions.
LSR	Logic shift right. All ALU bits are shifted to the right by one position. A 0 bit is loaded into the ALU15 position and the carry register remains unchanged.
LSRIC	Logic shift right, including carry. Same as LSR except the ALU0 bit is loaded into the carry register.
LSRFC	Logic shift right from carry. All ALU bits are shifted to the right. The carry register bit is shifted into the ALU15 bit position, then the carry register is cleared (loaded with a 0 bit).
ASR	Arithmetic shift right. Same as LSR, except the ALU15 bit remains unchanged.
ASRIC	Arithmetic shift right, including carry. All ALU bits are shifted to the right by one position. ALU0 displaces the carry register bit. The ALU15 bit remains unchanged.
CSR	Circulate shift right. All ALU bits are shifted to the right by one position. ALU0 displaces ALU15. Carry register remains unchanged.
CSRCC	Circulate shift right, clear carry. Same as CSR except carry register is cleared (loaded with a 0 bit).
CSRWC	Circulate shift right with carry. All ALU bits, and the carry register bit, are shifted to the right by one position. The ALU0 bit displaces the carry register bit, while the carry register bit displaces ALU15.

[1] These mnemonics represent the INB10 thru INB14 codes during an arithmetic instruction, not signal lines.

code 01101 (INB14-INB10), an ASLFC operation is performed.

Figure 1-10 shows that a shift-left operation is performed on the $\overline{\text{ALU0}}$ through ALU15 output bits; the OVFL (overflow) status is set if the ALU14 and ALU15 bits are different, and the carry bit resulting from the preceding arithmetic operation) is loaded to the DO line before the CARRY status is cleared.

Figure FO-7 shows the digital processor components that perform the shift functions. Table A of this figure represents the combined functions of instruction register U19 and decoding gate U18. The output of this circuit, SC0 and SC1, control the shift multiplexer on the ALUs of arithmetic logic unit CCAs A2 and A3. The multiplexer control lines (SC0, SC1) are in the following states in response to the INB11 (0 bit) and INB0 (1 bit) inputs:

SC1 = 1 (shift left by one)

SC2 = 0

This causes the shift multiplexer on CCAs A2 and A3 to select the switch [2] inputs.

NOTE

All multiplexer are functionally represented as tables or mechanical switches to facilitate this explanation.

This is a shift-left-by-1 operation. Each ALU output data bit ($\overline{\text{ALU0}}$ through ALU15) is transferred to a destination bus line (DO through D15) of an incremented bit value, for example, ALU13, is transferred to the D14 line. The most significant destination bus line, D15, and the least significant, DO, become a function of the respective 15L1 and OL1 variables.

Table C of Figure FO-7 represents the combined functions of instruction register U19 and multiplexer U6 and U14. U6 and U14 respond to the INB14, INB13, and INB12 (011_2) code by providing the following shift left variables:

$\overline{\text{15L0}} = \overline{\text{ALU15}}$

$\overline{\text{OL1}} = \overline{\text{ALU CARRY}}$

ALU bit 15 remains on the D15 line and the DO line is loaded with the carry that resulted from the ALU arithmetic operation.

Table D of Figure FO-7 represents the combined functions of instruction register U9, inverter U20, and multiplexer U4. When driven by INB13, INB10, and INB11, the circuits select the inputs that determine the CARRY and OVFL signal status. INB11 (0 bit) and INB10 (1 bit) force multiplexer U4 to select input ports [2]. As a result, INB13 determines if overflow register U7 can change state, and the output of multiplexer U3 determines the state of the carry register.

The INB13 1 bit provides one high input to overflow register gate U13. An inverted 0 INB14 bit further enables U13. The state of the overflow register is now determined by an exclusive-OR combination of the ALU14 and ALU15 data bits. If these bits are of the same value, overflow register U7 remains in its current state. Otherwise (i.e., the bits are different), the register is reset, providing a true (low) OVFL status signal via inverter U15.

Table E of Figure FO-7 represents the combined functions of register U25 and multiplexer U3. The output of this circuit has been selected to control carry register U2 via multiplexer U20. The INB14, INB13, and INB12 code is 011. Therefore, a (negative logic) 0 bit is applied to port [2] (the upper section) of multiplexer U4. Since negative logic 0 is high, this input causes the ZA output to go high and the ZA output to go low. As a result, the EXEC clock signal sets U2 and the CARRY status signal is cleared.

1.3.3.5.1.6 Destination Field (INB0 through INB3). (See Figure 1-13.) This field determines which digital processor register will receive the data processed and shifted by the ALU circuits, then output to the destination bus.

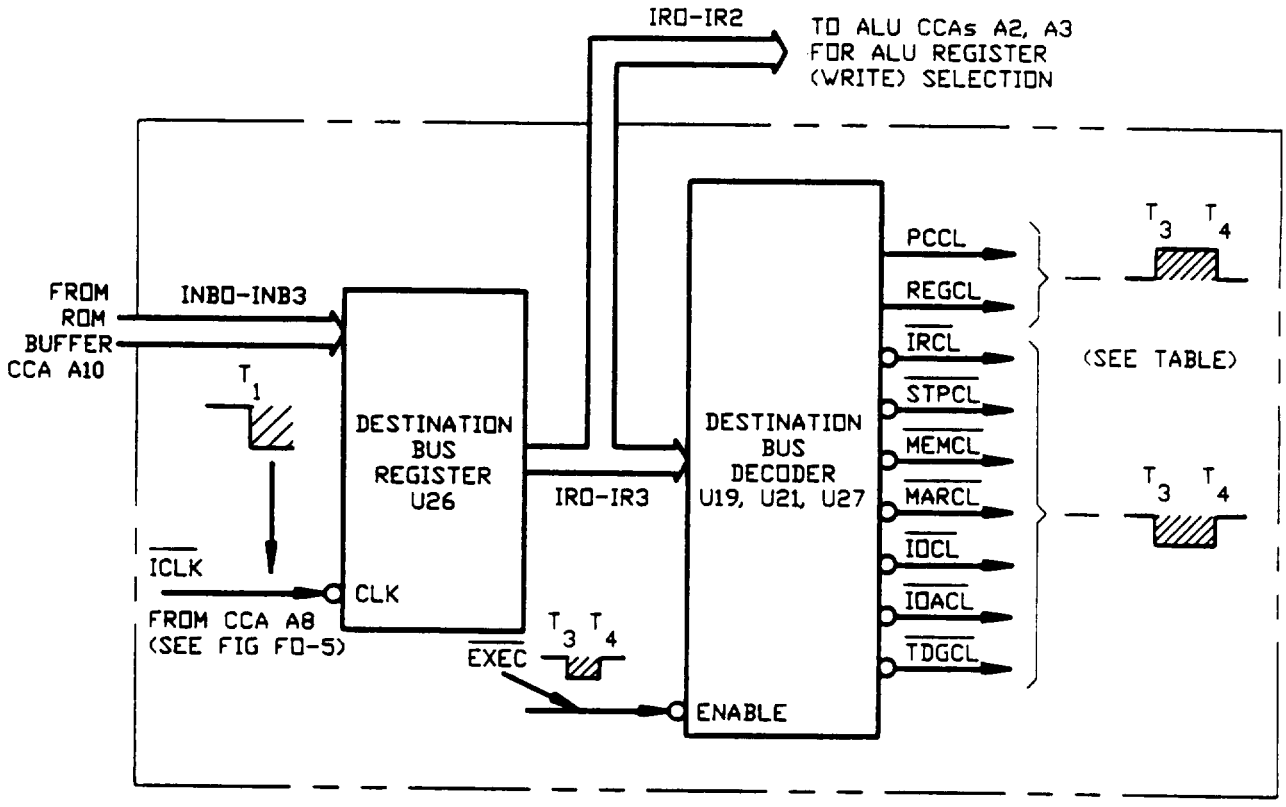
Instruction bits INB0 through INB3 are loaded into the destination bus registers U26 by ICLK during time T1. The resulting IR0 through IR3 output bits are directly applied to the ALU registers and to the destination bus decoding circuits of U19, U21, and U27. When IR3 bit is a 1, an ALU register is selected to receive destination bus data by a direct IR0 through IR2 input. An IR3 0 bit causes the destination bus decoding circuits to generate a clock during time T3 or T4 (based on the register selected), which loads destination bus data into the selected register (see Table B, Figure 1-11).

1.3.3.5.2 Jump Instruction. (See Figure 1-10.) The jump instruction provides the capability to perform conditional branching. First the instruction designates a condition to be tested. If the test condition is satisfied, the program counter jumps to a specified instruction address. A failed test condition defeats the jump operation, and the program advances to the next sequential instruction address.

1.3.3.5.2.1 Class Field (INB22, INB23). (See Table 1-9.) This part of the instruction word identifies the jump function. The decoding circuit on CCA A7 respond to the INB23 and INB22 1 code by providing true JMP and LIG (load-immediate gate) signals and false ALUG and I/O signals.

NOTE

Although the data output of CCAs A2 and A3 is not used, these ALUs perform equality-inequality tests, the results of which may be used during the jump instruction cycle.



DESTINATION BUS SELECTION

INB/IR				MNEMONIC	SELECTED DESTINATION
3	2	1	0		
0	0	0	0	INTERRUPT RET CLK (IRCL)	INTERRUPT RETURN REGISTER
0	0	0	1	STACK POINTER CLK (STPCL)	STACK POINTER REGISTER
0	0	1	0	PROGRAM COUNTERCLK (PCCL)	PROGRAM COUNTER
0	0	1	1	DATA MEMORY CLK (MEMCL)	DATA MEMORY
0	1	0	0	MEMORY ADDRESS CLK (MARCL)	MEMORY ADDRESS REGISTER
0	1	0	1	I/O DATA CLK (IOCL)	I/O DATA REGISTER
0	1	1	0	I/O ADDRESS CLK (IDACL)	I/O DEVISE REGISTER
0	1	1	1	TIME DELAY CLK (TDGCL)	TIMER REGISTER
1	0	0	0		ALU REGISTER 0
1	0	0	1		ALU REGISTER 1
1	0	1	0		ALU REGISTER 2
1	0	1	1		ALU REGISTER 3
1	1	0	0		ALU REGISTER 4
1	1	0	1		ALU REGISTER 5
1	1	1	0		ALU REGISTER 6
1	1	1	1		ALU REGISTER 7
1	X	X	X	REGCL-ALU REG WRITE CLK	ALL ALU REGISTERS*

*REGCL GENERATED WHENEVER IR3='1'

Figure 1-13. Destination Bus Select Functional Block Diagram

The $\overline{JMP}$ signal gates various decoding circuits that configure the condition test, while LIG loads the relative jump address to the destination bus. If the jump condition is satisfied, the destination bus data are added to, or subtracted from, the address of the next instruction to be executed.

1.3.3.5.2.2 Source Field (INB18 through INB21). (See Figure 1-13.) These bits select a register that provides data to the destination bus. During instruction time T1, these data are gated to the ALUs (of CCA A2 and A3) and compared with operand bus data.

1.3.3.5.2.3 Operand Field (INB15 through INB17). These bits select an ALU register that inputs data to the ALU via the operand bus. These data are compared with the source bus input and provide various test results for the jump decision.

1.3.3.5.2.4 Bit (INB14). (See Table 1-11.) Bit INB14 determines whether the relative jump address will be added to, or subtracted from, the current instruction address when a jump condition is satisfied. The program counter circuits interpret an INB14 bit into a subtract function. An INB0 bit adds the relative jump address to the current address.

Table 1-11. Program Counter ALU Control

Program counter (positive true)

Instruction cycle time	INB14	CCA A5 program counter I/O (positive logic)				CCA A4 program counter I/O (positive logic)					Results
		PCS3	PCS2M	PCS1M	PSC0	PCS3	PSC2L	PCS1L	PCS0	PCN	
T_1 thru T_3	Does not matter	1	1	1	1	1	1	1	1	0	ALUs configured for a plus carry operation (Carry: PCCNL is true, low, during this time interval)
T_3 thru T_4	0 (add jump address)	1	1	1	1	1	0	0	1	0	CCA A5 ALUs configured to accept A input only in arithmetic mode CCA A4 ALUs configured for arithmetic A plus B operation
	1 (subtract jump address)	0	0	0	0	0	1	1	0	0	CCA A5 ALUs configured for arithmetic A minus 1 operation CCA A4 ALUs configured for arithmetic A minus B minus 1 operation

1.3.3.5.2.5 Relative Jump Address field (INB6 through INB13). (See Figure FO-8.) These eight bits determine the magnitude of the jump and the maximum value is 255_{10}. Since the program-counter is always incremented by 1 during the early execution of all program instructions, the range of the address change is $+256_{10}$ or -254_{10}, relative to the jump instruction address. Instruction decoder CCA A7

converts the positive logic INB6 through INB13 bits into negative logic IR6 through IR13 data, which are compatible to the destination bus. The active LIG (load-immediate gate) signal loads IR6 through IR13 on the destination via bus drivers U11 and U22 on CCA A2.

1.3.3.5.2.6 Program Counter. (See Figure FO-8.) The program counter (PC) basically consists of four ALUs (U3 and U4 residing on CCAs A4 and A5), and four program counter registers (U10 and U11 on CCAs A4 and A5). Program counter I/O CCA A4 produces the eight lower instruction ROM address bits (RAD0 through RAD7), and CCA A5 provides the eight higher order instruction ROM address bits (RAD8 through RAD15). These ALUs are controlled by the PCS3, PCS2L, PCS1L, PCS0, and PCM signals derived from the PC decoding circuits on CCA A7. during the course of the jump instruction cycle, these control lines configure the PC ALUs to perform the following functions (refer to Table 1-11):

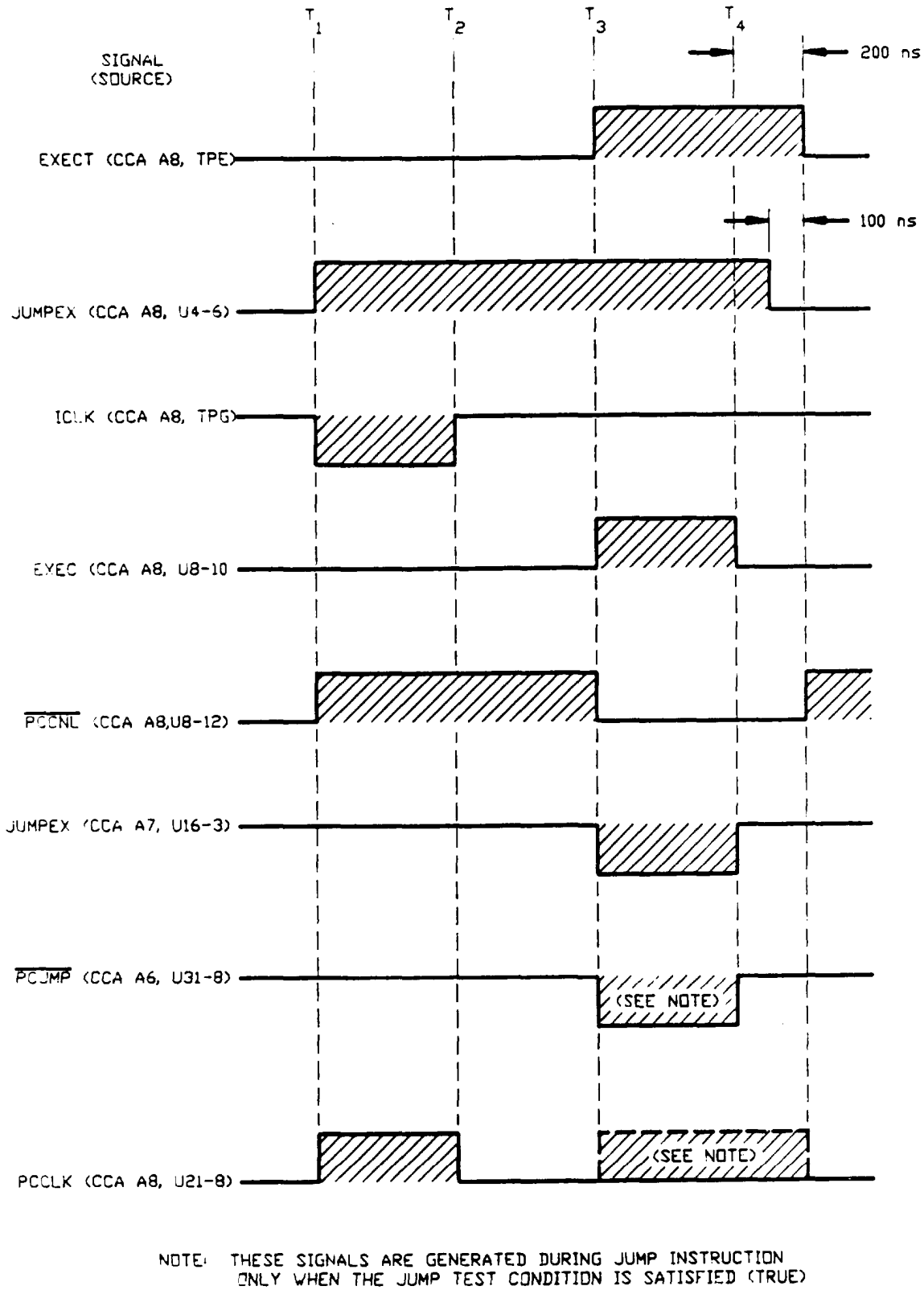
a. During times T1 through T3, a carry (PCCNL) is added to the A input (i.e., the current instruction address) to the ALUs on CCA A4.

b. During times T3 through T4, data from the destination bus (i.e., the B input) are either added to, or subtracted from, the A input (the incremental instruction address) of the CCA A4 ALUS.

Figure 1-14 is a program counter timing diagram that shows how the PC ALU control signals are generated as a function of the instruction cycle time. (See Figure FO-16, sheet 2.) During times T1 through T3 the low EXEC signal (derived from processor timing CCA A8) forces the output of NAND gates U29 pins 6 and 12, U16 pin 8, U17 pin 12, and U18 pin 3 high. This provides the high (1) PCS1M, PCS1L, PCS3, PCS2L, and PCS2M ALU control signals. The low input causes AND gate U27 pin 6 to go low, producing an arithmetic mode control signal (PCM). The EXEC line, in conjunction with the true (low) JMP input, forces the PCS0 output U9 pin 6 high (1 state). During this time period, CCA A8 provides an active carry (PCCNL) input to the PC ALU.

(See Figure FO-8.) During time T2, the positive edge of ICLK provides the PCCLK (program counter clock) output (from U21 pin 8 on CCA A8). This negative transition loads the incremented address (in the PC ALUs) into the instruction ROMs via the PC register. If the jump condition test fails, this addressed instruction is executed during the next instruction cycle.

(See Figures 1-14 and FO-16, sheet 2.) During times T3 through T4, EXEC goes high to enable the NAND/AND gate decoders. As a result, the PC ALU control signals (PCS3, PCS2L, PCS1L, PCS0, PCM) become a function of IR14 and IR14 (derived from the INB14 bit). This configures the PC ALUs for addition or subtraction of the relative jump address depending upon the state of INB14.



NOTE: THESE SIGNALS ARE GENERATED DURING JUMP INSTRUCTION ONLY WHEN THE JUMP TEST CONDITION IS SATISFIED (TRUE)

Figure 1-14. Program Counter Timing Diagram

Table 1-12. Jump Test Conditions

Jump Condition Field							Selected Test Bit	Remarks
INB15	INB5	INB4	INB3	INB2	INB1	INB0		
1	0	0	0	0	0	:	Timer register (TIME)	1. Selected by CCA A6 data multiplexer A (U29, U30 combination).
1	0	0	0	0	1	:	ALU borrow bit (CN15)	
1	0	0	0	1	0	:	Carry register (CARRY)	*2. (a) INBO=1 (high). Test condition is satisfied when test bit is low.
1	0	0	0	1	1	:	Overflow register (OVFL)	(b) INBO=0 (low). Test condition is satisfied when test bit is high.
1	0	0	1	0	0	:	Source bus bit 0 (S0)	
1	0	0	1	0	1	:	Source bus bit 1 (S1)	3. (a) When CN15 is low (borrow generated) the data on the OPR bus data is more than the source bus data.
1	0	0	1	1	0	:	I/O mode (IOM)	
1	0	0	1	1	1	:	Interrupt status (IRUPC)	(b) When CN15 is high (borrow not generated) the data on the OPR bus is less than, or equal to, the source bus data.
0	0	0	0	0	0	:	Timer register (TIME)	
0	0	0	0	0	1		ALU borrow bit (CN15)	
0	0	0	0	1	0		Carry register (CARRY)	
0	0	0	0	1	1		Overflow register (OVFL)	
0	0	0	1	0	0		Source bus bit 8 (S8)	
0	0	0	1	0	1		Source bus bit 9 (S9)	
0	0	0	1	1	0		I/O mode (IOM)	
0	0	0	1	1	1		Interrupt status (IRUPC)	
1	0	1	0	0	0	:	(SOR) = OPR) (A=B)	1. Selected by CCA A6 data multiplexer B (U26, U27, U30 combination).
1	0	1	0	0	1	:	ALU borrow bit (CN15)	
1	0	1	0	1	0	:	Source bus bit 2 (S2)	*2. (a) INBO=1 (high). Test condition is satisfied when test bit is low.
1	0	1	0	1	1	:	Source bus bit 3 (S3)	(b) INBO=0 (low). Test condition is satisfied when test bit is high.
1	0	1	1	0	0	:	Source bus bit 4 (S4)	
1	0	1	1	0	1	:	Source bus bit 5 (S5)	3. (a) When A=B is high, source bus data = OPR bus data.
1	0	1	1	1	0	:	Source bus bit 6 (S6)	
1	0	1	1	1	1	:	Source bus bit 7 (S7)	(b) When A=B is low, source bus data does not equal OPR bus data.
0	0	1	0	0	0	:	(SOR) = (OPR) (A=B)	
0	0	1	0	0	1		ALU borrow bit (CN15)	(c) When CN15 is low (borrow generated), OPR bus data is more than source bus data.
0	0	1	0	1	0		Source bus bit 10 (S10)	
0	0	1	0	1	1		Source bus bit 11 (S11)	(d) When CN15 is high (no borrow generated), OPR bus data is less than, or equal to source bus data.
0	0	1	1	0	0		Source bus bit 12 (S12)	
0	0	1	1	0	1		Source bus bit 13 (S13)	
0	0	1	1	1	0		Source bus bit 14 (S14)	
0	0	1	1	1	1		Source bus bit 15 (S15)	
X	1	0	0	0	0	:	Flag 0 Flag 0 (FLG0)	1. Selected by CCA A6 flag multiplexer A (U10).
X	1	0	0	0	1	:	Flag 1 Flag 1 (FLG1)	*2. (a) INBO=1 (high). Test condition is satisfied when flag bit is low (flag register is cleared).
X	1	0	0	1	0	:	Flag 2 Flag 2 (FLG2)	
X	1	0	0	1	1	:	Flag 3 Flag 3 (FLG3)	(b) INBO=0 (low). Test condition is satisfied when flag bit is high (flag register is set).
X	1	0	1	0	0	:	Flag 4 Flag 4 (FLG4)	
X	1	0	1	0	1	:	Flag 5 Flag 5 (FLG5)	3. X = may be high or low.
X	1	0	1	1	0	:	Flag 6 Flag 6 (FLG6)	
X	1	0	1	1	1	:	Flag 7 Flag 7 (FLG7)	
X	1	1	0	0	0	:	Flag 8 Flag 8 (FLG8)	1. Selected by CCA A6 flag multiplexer B (U13).
X	1	1	0	0	1	:	Flag 9 Flag 9 (FLG9)	*2. (a) INBO=1 (high). Test condition is satisfied when flag bit is low (flag register is cleared).
X	1	1	0	1	0	:	Flag 10 Flag 10 (FLG10)	
X	1	1	0	1	1	:	Flag 11 Flag 11 (FLG11)	(b) INBO=0 (low). Test condition is satisfied when flag bit is high (flag register is set).
X	1	1	0	1	1	:	Flag 12 Flag 12 (FLG12)	
X	1	1	1	0	1	:	Flag 13 Flag 13 (FLG13)	3. X = not used.
X	1	1	1	1	0	:	Flag 14 Flag 14 (FLG14)	
X	1	1	1	1	1	:	Flag 15 Flag 15 (FLG15)	

Also during times T3 through T4, the EXEC signal is inverted to provide an active low JUMPEX signal. This is applied to flag-jump logic CCA A6 to enable the jump condition test circuits. These circuits generate a true PC JUMP only when the tested condition is satisfied. PC JUMP toggles PCCLK gate low for a second time 200 nanoseconds after T4, causing the PC registers to load the jump address from the ALUs into the program instruction ROMs. If the jump condition test fails, a second PCCLK is not generated, and the previously loaded address remains to be executed during the next instruction cycle.

1.3.3.5.2.7 Condition Test Select Field (INB0 through INB5). INB0 through INB5, the 6-bit condition test select field, is converted into IR and IR bits, which control the multiplexer on flag-jump logic CCA A6. Table 1-12 shows the instruction bit codes, and the resulting conditions tested.

NOTE

An additional instruction bit, INB15, is used to select a test bit when the result of an ALU comparison is not a test consideration. (INB15 is normally used to select the operand bus input for the ALU comparison test.)

(See Figure FO-16, sheet 1.) When the JMP instruction (bits 22 and 23) is decoded, the output of exclusive-OR gate U21, and NAND gate U11 is forced to provide the following output (positive true):

AS 3	AS 2	AS 1	AS 0
1	0	0	1

This output controls the ALUs on ALU CCAs A2 and A3 (not the program counter ALUs). When the results of the ALU calculations are considered for the jump condition test, INB5 equals 0. This 0 bit forces the M (ALU mode) signal low. As a result of the AS0 through AS1 and M signals, ALUs of CCAs A2 and A3 are configured to perform the following arithmetic operation:

(SOR) (OPR), where

(SOR) = the 16-bit source bus data input to the ALUs.

(OPR) = the 16-bit operand bus data input to the ALUs.

The ALU $\overline{CN15}$ (borrow) and A=B (comparison) output resulting from this operation is used by-the flag jump logic circuits (of CCA A6) for source bus/operand bus equality or inequality tests.

Figure FO-9 shows the multiplexer circuits on CCA A6, which select a test condition in response to INB0 through INB5, INB15, and the state of the ALU CN (input borrow) and M (mode) control lines. The following four functional multiplexer feed status signals into jump latch multiplexer U28:

Multiplexer	Function
Flag mux A (U10)	Selects the flag status bit from one of eight flag registers (flag registers 0 through 7)
Flag mux B (U13)	Selects the flag status bit from one of eight flag registers (flag registers 8 through 15)
Data mux A (U29, U30)	Selects a status bit from source bus S0 and S1, S8, and S9 data, or any of the following: CARRY, OVFL (carry overflow), TIME, IOM, IRUPC (timer, input/output mode registers, interrupt), CN15
Data mux B (U26, U27 and U30)	Selects a status bit from source bus S2 through S7, S10 through S15 data, or A=B/CN15 (ALU CCA outputs), or the timer, carry overflow, interrupt or input\output mode registers.

Status bit selection in these multiplexer is a function of IR3, IR2, IR1 and, in some cases, IR15. These control signals are determined by the state of the INB3, INB2, INB1, and the INB15 bits, respectively. A direct or inverted output may be selected for each status bit when a true or false bit condition is the test requirement.

Jump latch multiplexer U28 may select up to 40 different true or false test conditions. The input flag or data multiplexer selection is determined by the M (mode) and CN (borrow input) lines. The state of instruction bit INB0 chooses a true or false test. The tested condition is satisfied when the selected input to U28 is high, causing the output of the jump latch multiplexer to go low, setting jump latch U31 during T3-T4 time period. Two hundred nanoseconds after time T4, the WAIT signal derived from CCA A8 resets jump latch U31, completing the PC JMP signal. The positive edge of PC JMP provides the second PCCKL signal, which loads the jump address from the program address ALUs into the program ROMs.

1.3.3.5.3 Load-Immediate Instruction. (See Figure 1-10.) The load-immediate instruction causes instruction bits to be loaded directly into the register designated by the destination field. For example, an unconditional jump operation is a load-immediate instruction with the program counter being the selected destination. A 2-bit field in this instruction can increment or decrement the memory address register (MAR), which selects a RAM or calibration ROM storage location.

1.3.3.5.3.1 Class Field (INB22, INB23). (See Table 1-9.) This part of the instruction word identifies the load-immediate operation by providing a true (low) LIG (load-immediate gate) signal, while the JMP, ALUG, and I/O are false. The low LIG signal enables load-immediate bus U11 and U22 on CCAs A2 and A3. As a result, bits IR6

through $\overline{IR21}$ (negative true versions of instruction bits INB6 through INB21) are loaded on the destination bus during time T1.

1.3.3.5.3.2 Data Field (INB6 through INB21). These instruction bits are inverted by instruction decoder CCA A7 and placed on the load-immediate bus as negative logic IR6 through IR21 bits. A true (low) LIG signal loads these data on the destination bus. The data are then loaded into the register designated by the destination field of the load-immediate instruction.

1.3.3.5.3.3 Destination Field (INB0 through INB3). (See Figure 1-13.) This 4-bit field designates the register that receives the destination bus data loaded by the LIG signal.

1.3.3.5.3.4 MAR Increment/Decrement Field (INB4, INB5). (See Figure 1-15.) The MARUP, MARDN gates (on instruction decoder CCA A7) are enabled when a load-immediate or I/O instruction is being executed. The EXEC signal causes the MAR increment or decrement operation to be executed during time T4. Becuse of the MAR register working in a negative true logic state, MAR increment operation (INB4 true) results in a MARDN signal and MAR decrement operation (INB5 true) results in a MARUP signal. A high INB4 input results in a MARDN signal (positive edge during T4), which is applied to the countdown input of the MAR register residing in CCA A2. The MAR register consists of four cascaded up/down binary counters (U16, U20 on CCA A2, and U16, U20 on CCA A3), which provide the SPAD0 through SPAD15 RAM and calibration ROM address bits. The output of these registers may be changed by one count when a MARDN signal (resulting from an INB4 1 bit) or a MARUP signal (an INB5 1 bit) drives the respective count down (CNTDN) or count up (CNTUP) inputs.

1.3.3.5.3.5 Load MAR Immediate. (See Figure 1-13.) The MAR may be loaded from the destination bus during the load-immediate instruction cycle when this register is selected by the instruction destination field. The resulting MARCL (derived from the destination bus decoder on CCA A8) parallel loads D0 through D15 data on the SPAD0 through SPAD15 lines via the MAR and SPAD buffers.

This parallel loading operation first occurs during time T3. Should the MAR increment/decrement field provide an INB4 or INB5 1 bit, the new MAR address is changed by 1 during time T4.

1.3.3.5.4 I/O Control Instruction. (See Figure 1-10.) The I/O instruction is the only class of instruction that permits direct transfer of source bus data to the destination bus. It also permits the program ROMs to be addressed by internal elements, as well as elements external to the digital processor. Overflow clear bit INB17 causes the OVFL to be cleared (set to 0) if it is a 1. A 0 INB17 bit leaves the overflow register unchanged. The stack pointer field (bits 16 and 15) provides the option to increment or decrement the contents of the STKP. When the stack pointer field is 00, the STKP remains unchanged. The carry field (bits 14 and 13) provides the option to set (10), clear (01), complement (11), or leave the carry register unchanged (00). The halt field (bit 12) causes the processor to halt after completing the execution of the instruction containing the halt

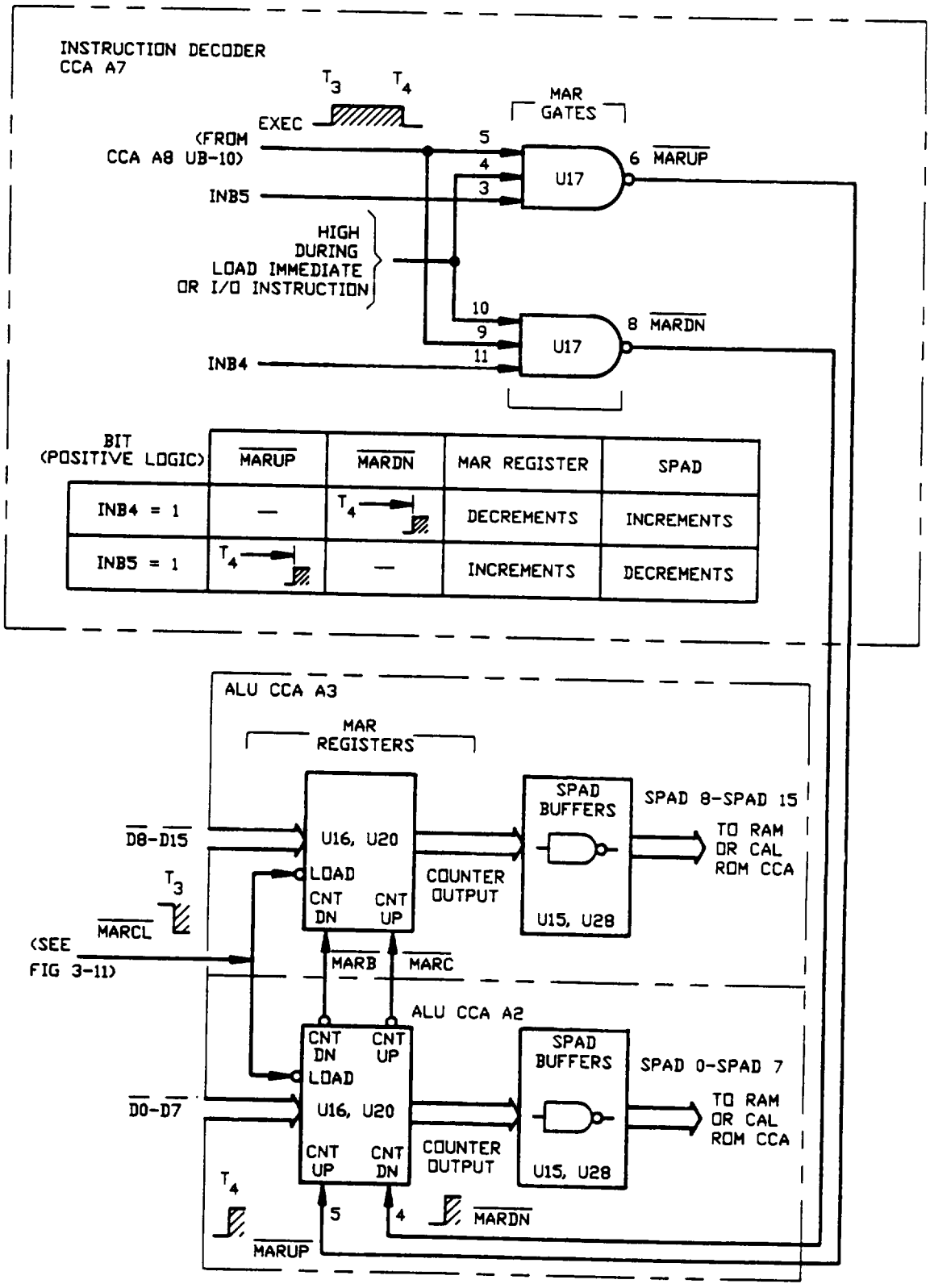


Figure 1-15. MAR Control Functional Block Diagram

command. The processor halts in a state ready to execute the next instruction, but will not resume operation until manually commanded to do S0. The flag field (INB11, INB10, INB9, INB8, and INB7), in conjunction with the flag set/clear field (INB6), can select and set or clear any of the 16 1-bit flag registers. These bits also provide interrupt mode control, as well as I/O mode bit and I/O strobe pulse control.

MAR field functions are identical to those of the MAR field in the load-immediate class instruction. All of the various control fields within the I/O control class of instructions are completely independent, and may be used in any combination to construct the desired operation.

1.3.3.5.4.1 Class Field (INB22, INB23). (See Table 1-9.) The direct transfer of source bus data to the destination bus occurs via ALU CCAs A2 and A3, which are forced to the do-nothing mode" of operation by the decoded I/O class field. The decoded class field also provides a true (low) ALUG signal, which gates the ALU output data to the destination bus .

(See Figures FO-6 and FO-7.) The decoding circuits on CCA A7 respond to the INB23 1 bit and the INB22 0 bit by generating the following ALU CCA control signals (positive true logic):

CN	$\overline{\text{ALUG}}$	AS3	AS2	AS1	AS0	M	SC0	SC1
0	0	1	1	1	1	0	1	1

The low M (mode) signal causes the ALU microcircuits (on CCAs A2 and A3) to go into the arithmetic mode of operation. The AS0 through AS3 bits configure the ALU microcircuits to transfer the source bus input data into the shift multiplexer (CN = 0 provides no carry input to the ALUs). The shift control bits (SC0, SC1) configure the ALU CCA shift multiplexers into the no-shift mode. This transfers the ALU output (ALU0 through ALU15) through the shift multiplexer to the destination bus drivers (U9 and U10 on CCAs A2 and A3). These drivers, enabled by the active (low) ALUG (ALU gate) signal, passes the data to the destination bus.

As a result of the decoded I/O instruction, the PC ALU control decoding circuits of instruction decoder CCA A7 provide the following (positive true) outputs:

Mode control	CCA A5 ALU function control				CCA A4 ALU function control			
PCM	PCS3	PCS2M	PCS1M	PCS0	PCS3	PCS2L	PCS1L	PCS0
0	1	0	1	0	1	0	1	0

This configures the PC ALUs (on CCAs A4 and A5) to pass the B inputs through the destination bus to the program counter registers. When the destination field of the I/O instruction provides a PCCLK signal (see Figure 1-13), data from the PC ALUs address the program ROMs via

the program counter registers and the RAD0 through RAD15 drivers (U22 and U30) of CCAs A4 and A5.

1.3.3.5.4.2 Source Field (INB18 through INB21). (See Figure 1-11.) The source field determines which register inputs data to the source bus, and ultimately to the destination bus. The I/O instruction allows data from the I/O bus to be loaded into the digital processor by selecting the IOR (input/output register) to drive the source bus.

1.3.3.5.4.3 Destination Field (0 through INB3). (See Figure 1-13.) The destination field selects a register to receive data from the destination bus. An I/O instruction allows an external element to address the program ROMs by designating the program counter as the recipient of destination bus data.

1.3.3.5.4.4 MAR Increment\Decrement Field (INB4, INB5). The contents of the MAR may be changed by one count during the I/O instruction cycle as a result of these inputs.

1.3.3.5.4.5 Flag Field (INB6 through INB11). These bits allow a synchronous exchange of data between the digital processor and an external device interface (e.g., serial interface CCA A26 for the computer, or servo serial interface CCA A21 for the digital servo). Data are transferred to the interface selected by IOAO through IOA7 via the I/O bus lines in response to the following DF control external device handshake signals:

a. The IOM (input/output mode) signal, which goes low for digital processor output operation, and high for input operation.

b. The IOS (input/output strobe) signal which, in certain data exchanges, loads data into or out of the digital processor.

c. The flag status signal, which sets the flag register when I/O operation starts, and clears the flag register when I/O operation terminates.

Figure FO-10 shows the flag and 1/0 control logic that reside on CCA A6. INB6 through INB11 are inverted by CCA A7 and the resulting IR6 through IR11 bits are applied to CCA A6. The CCA A6 primary control functions are selected by multiplexer U22.

U22 responds to the input IR9 through IR11 bits by transferring a negative gate to ports [0] through [7]:

Output Ports	Functions
[0] through [3]	Provide a clock to one of four flag register select multiplexer. The selected multiplexer responds to IR7 and IR8 bits by transferring the clock to one of four flag registers. The clocked flag register resets if INB6= 0 or sets when INB6 = 1.

Output Ports	Functions (Continued)
[4]	Provides a clock (IRC) to interrupt latch U16 on CCA A8.
[5]	Provides a direct clear input to all flag registers.
[6]	Clocks the I/O register. When IR6 is high (INB6 = 0), it clears the I/O register. This provides a low output mode) IOM signal. A low IRB6 (INB = 1) sets the I/O register, producing a high (input mode) IOM signal.
[7]	Clocks the IOS flip-flop. This produces an IOS (I/O strobe) when IR6 is low (INB = 1).

1.3.3.5.4.6 Flag Register. (See Figure FO-15.) Sixteen flag registers reside on CCA A6. Each register consists of two flip-flops (see Figure 1-16). Table 1-13 lists these flag registers and the components that constitute the registers.

Table 1-13. Flag Registers

Flag	Flip-flops	Inverter
0	U2A, B	U25
1	U19A, B	U20
2	U17A, B	U25
3	U18A, B	U25
4	U9A, B	U25
5	U1A, B	U25
6	U12A, B	U20
7	U3A, B	U20
8	U14A, U6B	U20
9	U23A, B	U32
10	U14A, U6A	U32
11	U24A, B	U32
12	U7A, B	U32
13	U16A, B	U32
14	U5A, B	U20
15	U8A, B	U32

Flip-flop A is set by INB6 1 bit (IR6 input is low), or cleared by INB6 0 bit (IR6 input is high), when clocked by an input from the I/O-flag control logic. When set, the low Q output of flip-flop A drives the inverted output high, providing a set FLAG status signal to the interface represented by this flag register. When the subsequent data transfer operation is completed, the interface device applies a clock to flip-flop B, clearing the flip-flop. The resulting low Q output

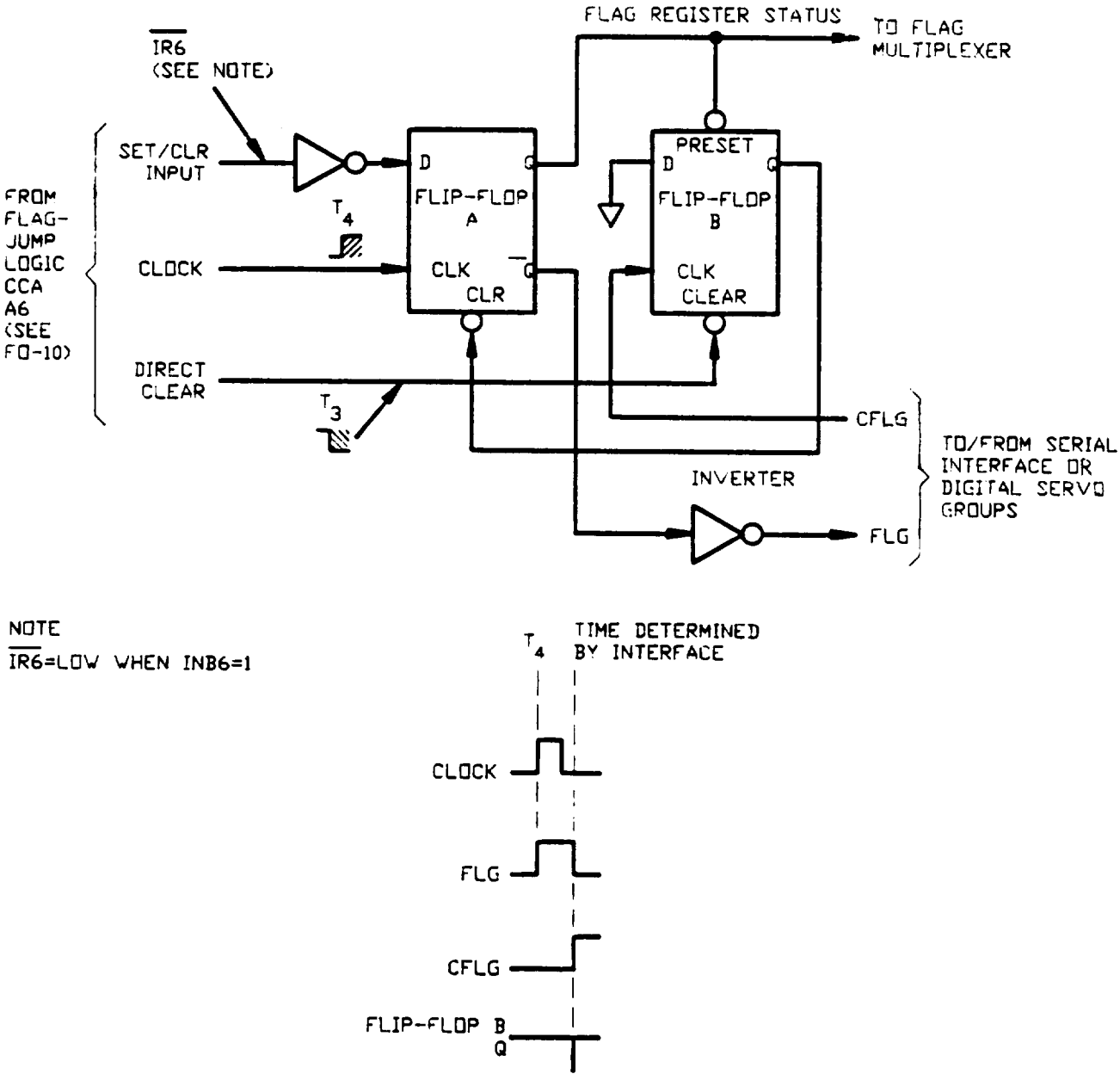


Figure 1-16. Typical Flag Register Function Block Diagram

clears flip-flop A, clearing the flag status. The digital processor may also clear the flag status by applying a high IR6 (INB6 = 0) input while clocking flip-flop A. The Q output of flip-flop A provides a flag status bit to the jump condition logic circuits.

1.3.3.5.4.7 Halt Bit (INB12). (See Figure 1-17.) When I/O instruction bit 12 is equal to 1, the digital processor is stopped. The 1 bit in instruction decoder CCA A7 is inverted, and the resulting low IR12 signal is applied to CCA A8. U8 on CCA A8 inverts IR12 to provide a high input to 1/0 halt gate U17. A decoded I/O instruction causes U17 pin 13 to be high. Ring counter U11 pin 3 (Q output) goes high during time T3, driving the output of enabled halt gate U17 low. This low sets the halt latch, providing a high input to stop gate U2. Since no digital processor manual inputs are applied to U2, stop gate U2 is enabled. As a result, the high halt input drives U2 pin 8 low. This low inhibits the J gate input of first ring counter U3. This prevents U3 from setting again; causing the count operation" to stop after the next time T6. Manual single-step or preset control can temporarily defeat this halt to allow the digital processor to step through a desired number of program steps.

1.3.3.5.4.8 Carry Register Control Field (INB13, INB14). (See Figure 1-18.) INB13 and INB14 control the state of the carry register during an I/O instruction. The state of these instruction bits may set, clear, or toggle the carry register during time T4.

1.3.3.5.4.9 Stack Pointer Register Control Field (INB15, INB16). (See Figure 1-19.) INB16 (1 state) increments the stack register by one count, while an INB15 1 bit increments the register count. When both bits are in the 0 state, the stack pointer register remains unchanged.

The stack pointer register consists of four cascaded up/down binary counters, U17 and U18, on program counter CCAs A4 and A5. Collectively, these counters provide 16 bits of stack pointer register data. The counters count up by 1 when clocked by STKUP or count down by 1 in response to a STKDN input. These STKUP and STKDN signals are derived from INB16 and INB15, on instruction decoder CCA A7. These bits drive NAND gate U16 or U18, which are enabled by the decoded I/O class instruction bits. The resulting SUP or SDN drives OR gate U20 on processor timing CCA A8. OR gate U20 is enabled by SUP or SDN and a gating input from pin 6. A SUP or SDN input causes a STKUP or STKDN positive-edge signal to be generated 100 nanoseconds before time T1. This output drives the count up or down based upon the inputs from the up/down binary counters.

A $\overline{\text{STPG}}$ loads the stack point data to the source bus. The destination bus data becomes stack pointer register data when loaded into the register by a STPCL.

1.3.3.5.4.10 Overflow Resister Control Bit (INB17). (See Figure 1-20.) During an I/O instruction, when the INB17 bit is in the 1 state, the overflow register (U24, U15) is cleared during time T4. A 0 INB17 bit leaves the overflow register unchanged.

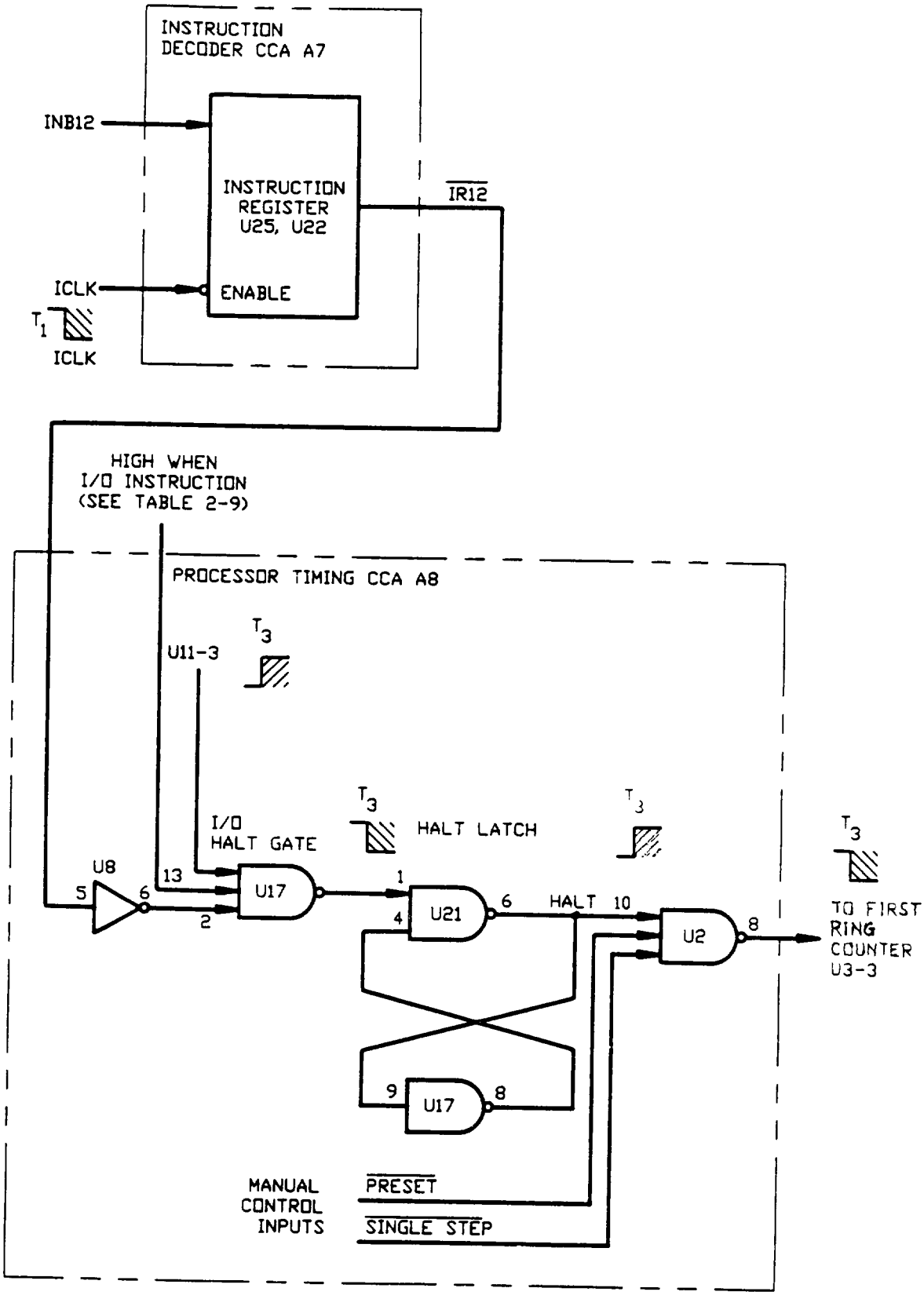
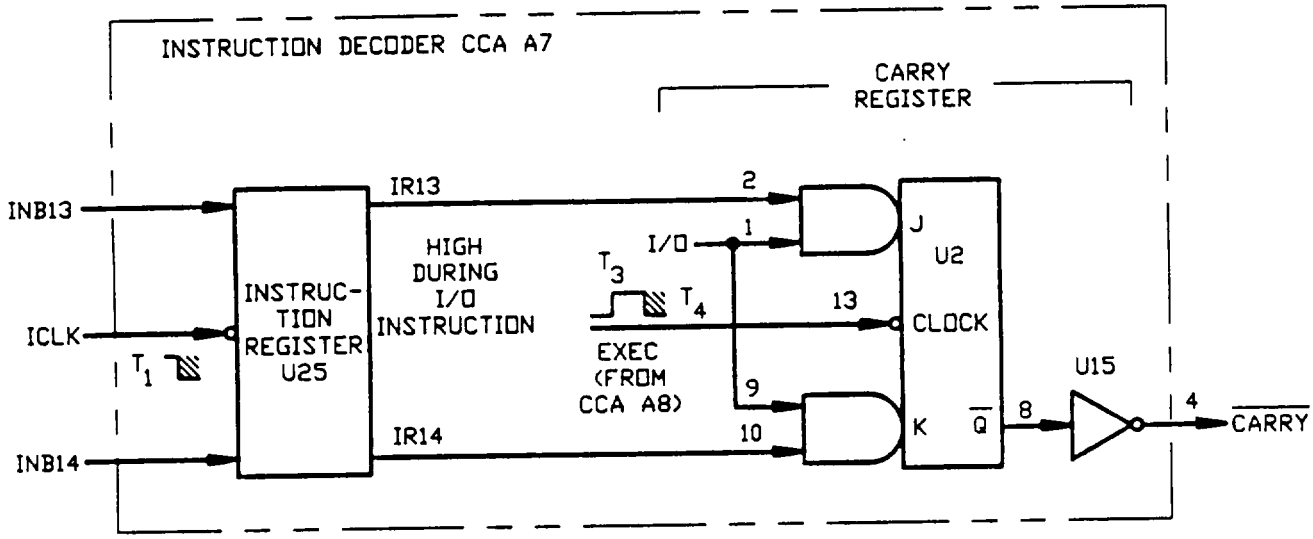


Figure 1-17. I/O Halt Functional Block Diagrm



INPUT (POSITIVE TRUE)		
INB14	INB13	$\overline{\text{CARRY}}$ (NEGATIVE TRUE)
0	0	N.C.
0	1	HIGH (CLEARED)
1	0	LOW (SET)
1	1	REVERSES STATE (TOGGLES)

Figure 1-18. Carry Register Control Functional Block Diagram

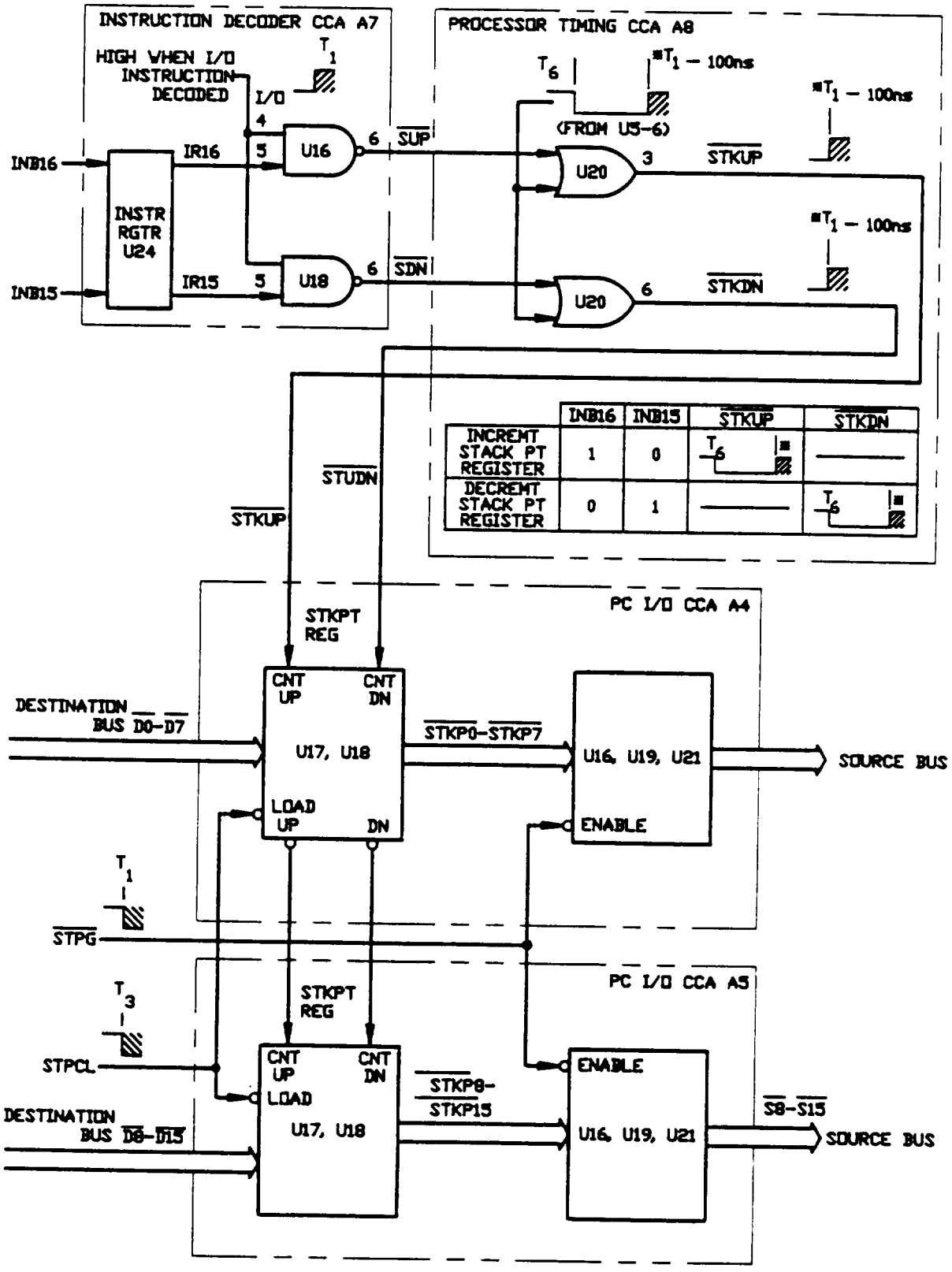
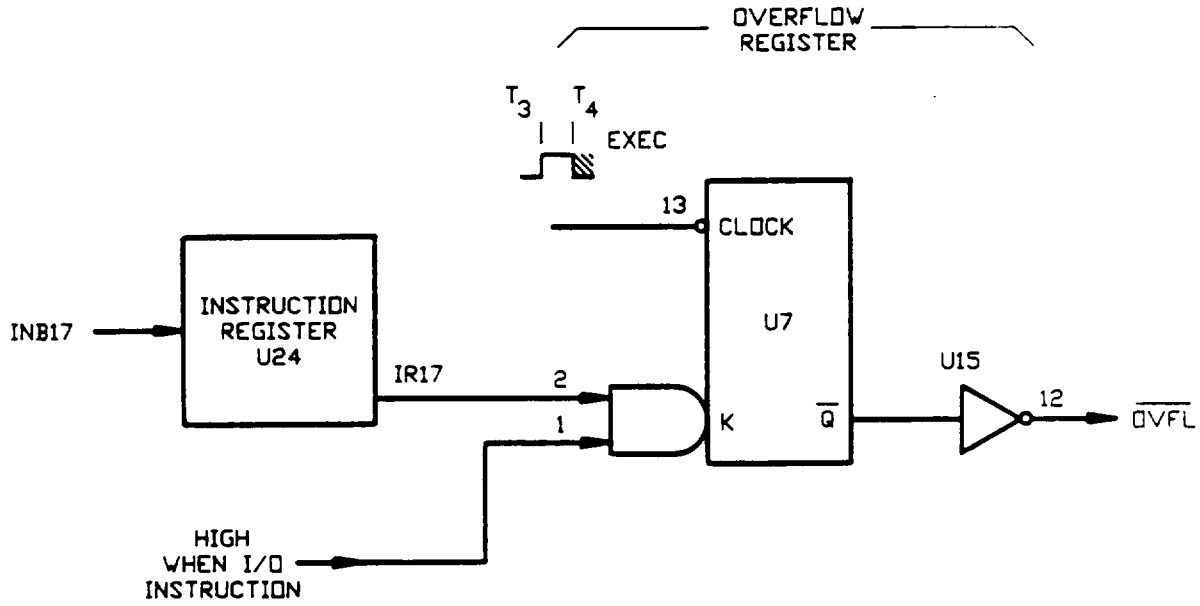


Figure 1-19. Stack Pointer Register Control Functional Block Diagram



INB17 (POS TRUE)	OVERFLOW REGISTER STATE	$\overline{\text{OVFL}}$
1	RESET	LOW
0	N.C.	N.C.

N.C. = NO CHANGE

Figure 1-20. CCA A7 Overflow Register Control Functional Block Diagram

1.3.3.5.4.11 Interrupt Sequence. (See Figures 1-21 and FO-17.) The interrupt system permits an external group to access the digital processor for service. Each of these groups has a dedicated instruction subroutine stored in the digital processor instruction ROMs. This subroutine is addressed when the group activates its unique interrupt line (i.e., drives INT low), and the digital processor program cycles to an interrupt sequence. The interrupt sequence is initiated when instruction bits INB6, INB9, INB10, and INB11 are configured as follows:

(Positively true)

INB11	INB10	INB9	INB6
0	1	1	1

During event 1, the I/O flag control logic (see Figure 1-21) interprets the INB9 and INB10 bits into IRC (interrupt clock), which clocks interrupt latch U16 pin 3 during time T4. The D input to latch IR6 is low as a result of an INB6 1 bit. The clocked latch resets, providing a low enable input to priority decoder U24 pin 5. (See Table 1-14.) The eight interrupt lines of the decoder control the 3-bit binary output lines according to the priority to the interrupt input lines. For example, FLG14, if active (low), has control precedence over interrupt lines 0 through 6 (INT0 through INT6). Therefore, a low I7 input line causes a binary 7 to be generated on lines A2, A1, and A0 regardless of any other active (low) input. If FLG14 is inactive (high), an active low 16 (interrupt 6) has priority control, resulting in a binary 6 output.

Table 1-14. Interrupt Priority Decoder

Priority	Interrupt lines	Binary output line (negative true)		
		A2	A1	A0
First	$\overline{\text{FLG14}}$ (power on initialize)	1	1	1
Second	$\overline{\text{INT6}}$ (computer service)	1	1	0
Third	$\overline{\text{INT5}}$ (digital servo service)	1	0	1
Fourth	$\overline{\text{INT4}}$	1	0	0
Fifth	$\overline{\text{INT3}}$	0	1	1
Sixth	$\overline{\text{INT2}}$	0	1	0
Seventh	$\overline{\text{INT1}}$	0	0	1
Eighth	$\overline{\text{INT0}}$	0	0	0

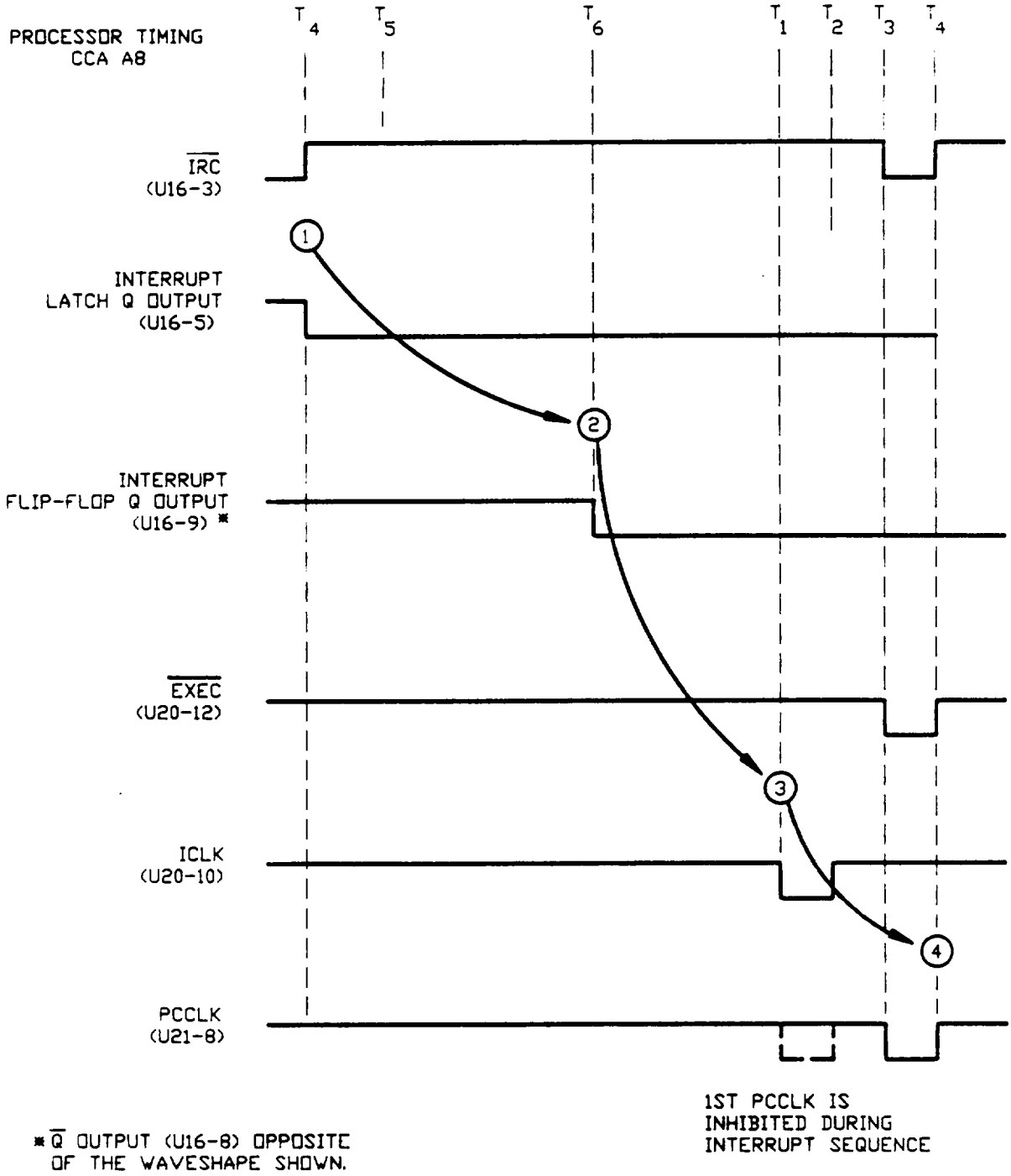


Figure 1-21. Interrupt Timing Diagram

$\overline{\text{INT0}}$ has the lowest priority and controls the output lines (producing a binary 0) only when no other interrupt line is active. When any interrupt input line is active, the GS output line goes low. When no interrupt line is active, this line remains high.

The binary coded output of the priority decoder is applied to interrupt multiplexer U23, while the low GS output is applied to the D input (pin 12) of interrupt flip-flop U16.

In event 2, the Q output of ring counter U5 goes high during the next time T6 to clock U16 pin 11. Since its D input is low, U16 resets. The resulting low Q output of U16 pin 9 drives the COM1 and COM2 lines high via NAND gate U28. In addition, the high Q output forces ASW0 through ASW2 bits into the 0 state (high). The low Q output allows the EXEC signal to produce PCCLK via gate U21 by enabling OR gate U20 with a low input to pin 13. The Q output is now inverted by U25 to provide a high IRWS (instruction register write strobe). This high forces the instruction registers on CCA A7, and destination bus register on CCA A8, to switch to a hardwired instruction word. Table 1-15 lists the output IR instruction bits and describes the resulting digital processor configuration.

NOTE

As a result of the hardwired digital processor configuration, the address of the next programmed instruction to be executed in transferred from the program counters to the interrupt return address register (IRAR) via the coupled source destination bus. This operation is executed during times T1 thru T4.

The low Q output (U16 pin 9) drives the PCWS (program counter write strobe signal) low via input U9 pin 10 and output U25 pin 8. This switches the ASW0 through ASW15 to the input of the program counter registers (U10 and U11) on CCAs A4 and A5. The ASW0 through ASW15 bits address the program ROMs during the next PCCLK clock pulse ASW0 through ASW2 is a function of the priority decoder A0 through A2 lines. ASW3 through ASW15 are high (negative logic 0 bits).

The high Q output of U16 pin 8 of processor timing CCA A8 inhibits OR gate U20 at pin 9, preventing the generation of a PCCLK pulse during times T1 and T2, and causes interrupt multiplexer U23 to switch the interrupt priority decoder (U24) A0 through A2 bits to the respective ASW0 through ASW2 lines. (See Table 1-14.)

During the third event, time T1, the program counter (next instruction) address is loaded onto the direct coupled source-destination bus.

During the fourth event, time T4, the next instruction address is loaded into IRAR by IRCL (interrupt return register clock), and PCCLK (resulting from EXEC during PCCLK gate U21) loads the ASW0 through ASW15 data to the program counter register. The ASW0 through ASW15 data bits now address the program ROMs of CCA A18 to provide the special interrupt subroutine selected by ASW0 through ASW15.

During the next instruction cycle, the hardwired INB9 and INB10 1 bits (See Table 1-15 and Figure FO-10) provide a second IRC (interrupt clock). The IRC input to interrupt latch U16A on CCA A8 is high as a result of the hardwired INB6 0 bit. The latch responds to these inputs by setting. Interrupt latch U16B is then set by the low Q output of U16A. The outputs of the set interrupt latches switch and remove the hardwired inputs to instruction registers on CCA A7 (i.e., U19, U24, U25, U26, and U28) and register U26 on CCA A8. The program counter registers are then switched to accept PC ALU address inputs instead of the ASW0 through ASW15 address.

Table 1-15. Interrupt Configuration

Instruction register	Hardwired output (positive true)	Results
CCA A7 U19, U24, U25, U26, U28	IR4 thru IR7 = 0 IR8, IR11 = 0 IR9, IR10 = 1	(a) Program counter drives source bus.
	IR12 thru IR15 = 0 IR16 thru IR18 = 0 IR19 = 1	(b) ALU CCAs configured to transfer source bus data directly onto the destination bus.
	IR20 thru IR22 = 0	(c) A logic high (IR6) is applied to the interrupt latch D input (U16 pin 12).
CCA A8 U26	IR0 thru IR3 = 0	The IRAR (interrupt return address resistors) receive data from the destination bus.

Switched, the instruction registers accept instruction bus inputs for the program ROMs. These instructions comprise the special subroutine which was accessed initially by the interrupt sequence address input (i.e., ASW0 through ASW15). When servicing of the interrupting group is concluded, the subroutine generates an I/O instruction. This instruction retrieves the program address that was stored in the IRAR (interrupt return address register) during the interrupt sequence. The address is applied to the program ROMs, allowing the digital processor to resume execution of its normal (noninterrupt) instruction set.

1.3.3.6 ROM Extender CCA A9. (See Figure FO-18.) ROM extender CCA A9 provides the means by which the external diagnostic ROMs (i.e., ROMs residing in the digital processor test set) control the digital processor instruction bus. The RAD0 through RAD15 digital processor program counter address outputs are applied to external diagnostic ROMs via ROM extender buffers U3 through U6 and external equipment wiring. The 24-bit external instruction word is then transferred to the digital processor instruction bus via external wiring and instruction bus buffers U9, U10, U13, and U14.

The DF ENABLE signal (controlled by the digital processor test set) determines whether the external (diagnostic) ROMs or the internal program ROMs drive the instruction bus. When the DF ENABLE signal is high (as a result of the digital processor test set not being connected or the connected test set providing a high input) , U15A goes low. This provides an RS15 input that enables internal program ROM buffer A10. This low also forces the output of U15B high, disabling instruction bus buffers U9, U10, U13, and U14. When the digital processor test set drives DF ENABLE low, U15A provides a high RS15 output that disables internal program ROM buffer A10. This high forces the output of U15B low, enabling the instruction ROM buffers, and transferring external diagnostic ROM instructions into the digital processor.

1.3.3.7 Display Multiplexer CCA A1. (Refer to Figure FO-12.) Display multiplexer CCA A1 multiplexes the display data for transmission to the digital processor test set. the display multiplexer accepts 60 bits of display data from the digital processor buses and applies them to 8-bit multiplexer U5, U9, U13, U17, U6, U1, U10, and U14, which multiplex the data under control of MUX0 - MUX2 binary commands from the test set. The outputs of the multiplexer are buffered by gates U7 and U8, then routed to the digital processor test set as signals DM0 through DM7. Display multiplexer CCA A1 also contains the timer counter circuits described in Table 1-8.

1.3.4 SERIAL INTERFACE GROUP.

The serial interface group provides data formatting and handshake signals for information and command interchange between the computer and the digitalprocessor group. (See Figures 1-22 and FO-25.) The serial interface group consists of the serial interface CCA A26 which provides the means for exchanging data and commands between the digital processor and the computer. The handshake logic of CCA A26 coordinates the transfer of information between the 16-bit parallel I/O bus of the digital processor, and the serial data path between the DF control and the computer. Table 1-16 lists these signals and briefly describes their functions.

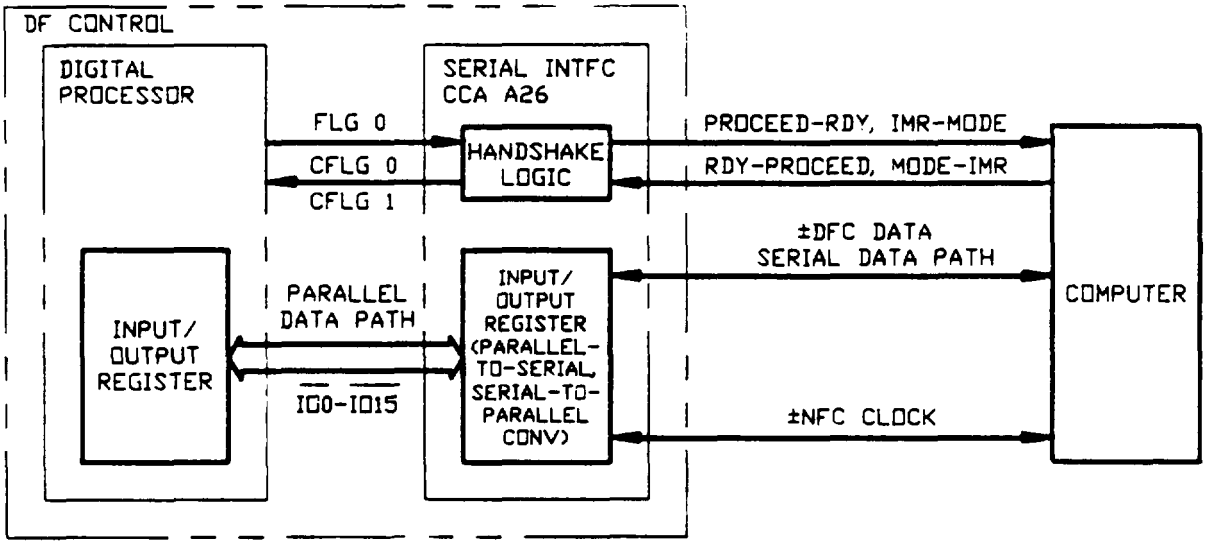


Figure 1-22. Computer Interface Block Diagram

Table 1-16. Computer/DF Control Interface Signals

Signal	Function
DFC DATA	A message consisting of one or more DFC DATA words is serially transferred between the DF control and the computer in response to handshake signals. Each DFC DATA word consists of 16 serial bits.
NFC CLOCK (df data clock)	This clock serially shifts the DFC DATA words for the computer /DF control data exchange.
+MODE IMR (input mode request)	This handshake signal is controlled by the computer: High = Computer output; DF control input. Low = Computer input; DF control output. +MODE IMR is normally low.
+IMR Mode (input mode request)	This handshake signal is controlled by the DF control: High = DF control request to interrupt the computer for DF control message. Low = No DF control message.
+READY PROCEED	This handshake signal, controlled by the computer, is driven high to notify the DF control that the computer is ready to accept the next DF control word.
+PROCEED READY	This handshake signal, controlled by the DF control, is driven high to notify the computer that the DF control is ready to accept the next computer word.

1.3.4.1 Computer Message Input. (See Figures 1-23 and FO-11.) The computer message input consists of three timing sequences as follows:

1.3.4.1.1 Timing Sequence 1. The computer drives +MODE-IMR true (high) when it has a message for the DF control. this high is inverted by U23B to provide a low enabling input to the data receiver consisting of U4D and U24B. The serial 16-bit computer data word is then transmitted to the DF control input register via the enabled data receiver. The computer also applies a +NFC data clock to the register and to 16-bit counter U11 via clock receiver U24A. The clock synchronously loads the computer data into the input register while advancing the count of U11 from a zero count.

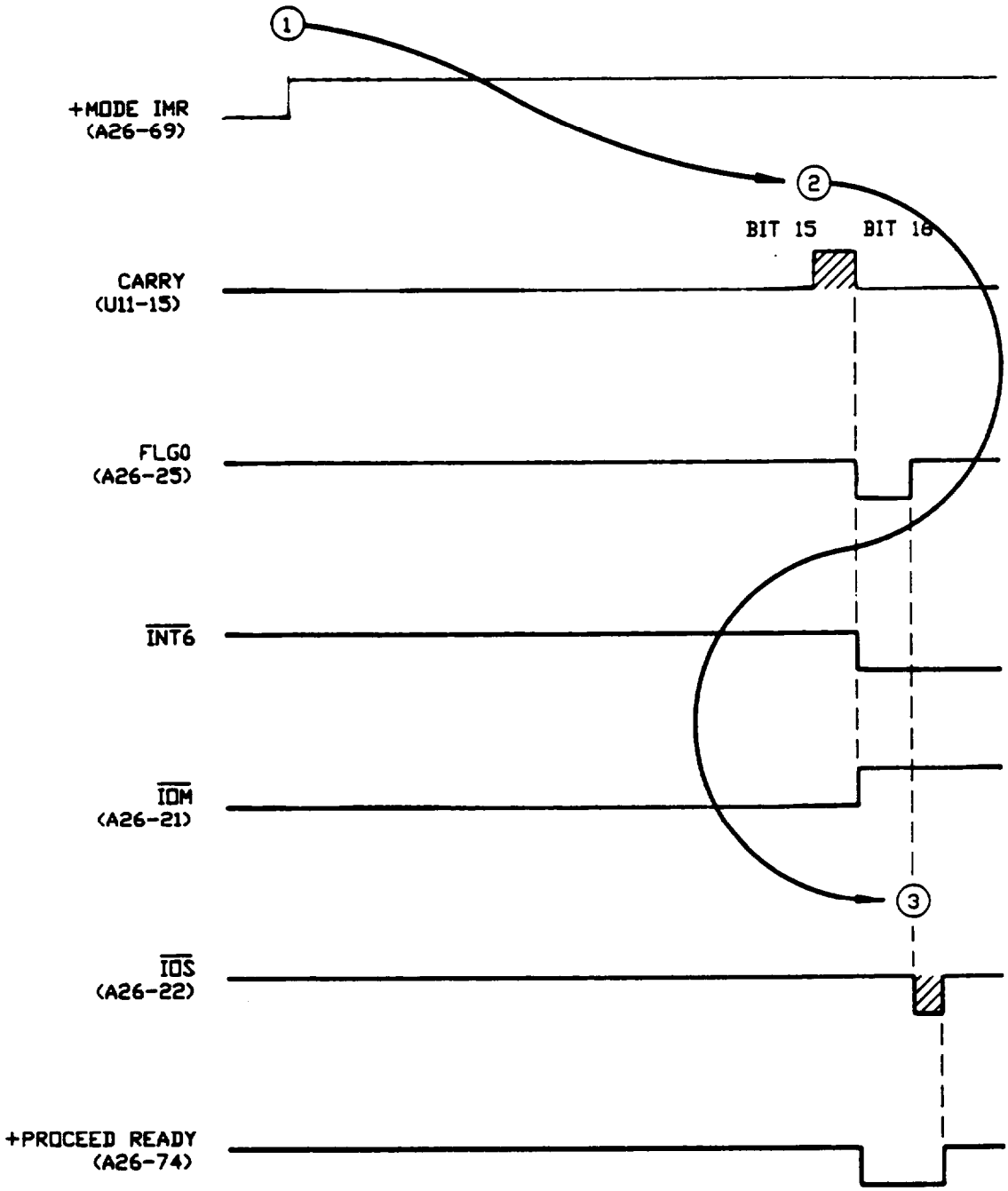


Figure 1-23. Computer Message Input Timing Diagram

1.3.4.1.2 Timing Sequence 2. U11 responds to the clock pulses by providing a high carry signal during the 15th pulse, then a low carry signal during the 16th pulse input. (The 16th clock pulse also loads the 16th serial data bit into the input register.) The low transition of the carry signal produces a positive edge CFLG0 (clear flag 0) signal. The resulting low FLG0 signal activates the INT6 signal. The digital processor responds to true (low) INT6 by going to the interrupt 6 subroutine. This subroutine includes addressing CCA A26 with a 011_8 IOA bus code (negative logic; 1 = low, O = high) :

$\overline{IOA7}$	$\overline{IOA6}$	$\overline{IOA5}$	$\overline{IOA4}$	$\overline{IOA3}$	$\overline{IOA2}$	$\overline{IOA1}$	$\overline{IOA0}$
o	0	0	0	1	0	0	1

The command decoder responds to this and a high IOM input by providing a low enabling signal to the 1/0 bus drivers. Enabled, the I/O drivers transfer the computer data, which are formatted into a parallel word, from the input register to the digital processor via the I/O bus.

1.3.4.1.3 Timing Sequence 3. The digital processor sends an IOS strobe and sets FLG0 when these data are stored. The leading edge (negative-going) of the strobe resets the 16-bit counter to zero count. The positive IOS signal edge clocks I/O mode latch U2A and I/O word logic latch U1B.

Simultaneously, U2A resets and U1B sets. The resulting low Q output of the 1/0 mode latch sends a low +IMR MODE signal to the computer, while disabling the clock generator on CCA A26. The high Q output of start latch U1B combines with the true FLG0 to produce a true (high) +PROCEED READY signal at the output of line driver U18A. This signal notifies the computer that the digital processor is ready to accept the next 16-bit input message word.

The input word sequence repeats with FL0 again being cleared at its conclusion by the CARRY signal. The CARRY signal clocks stop latch U2B,_U8D with its negative edge. The stop latch then responds to the low Q output of the start latch by resetting. The low Q output of the reset stop latch clears the start latch. Cleared, the start latch provides a false (low) +PROCEED READY output, and directly resets the stop latch. Again the start latch is set with the IOS strobe when the digital processor is ready to accept another computer input word.

1.3.4.2 DF Control Ouput Message. (See Figures 1-29 and FO-11.) the DF control output message consists of five timing sequences:

1.3.4.2.1 Timing Sequence 1. When the DF control has an output message for the computer, the digital processor addresses CCA A26 with an IOA bus code of 11_8, sets FLG0, and places the first word to the I/O bus pulling IOM low. This combination produces a high command decoder output at U7D pin 11. This high allows the IOS strobe to set I/O mode latch U2A. The resulting high Q output is transferred via U18B to the computer as an +IMR MODE interrupt request. The IOS strobe then sets I/O word logic start latch U1B. The combined high outputs of the I/O mode latch and the start latch remove the disable input from the clock generator (U3, U5, and U6). The high Q output of

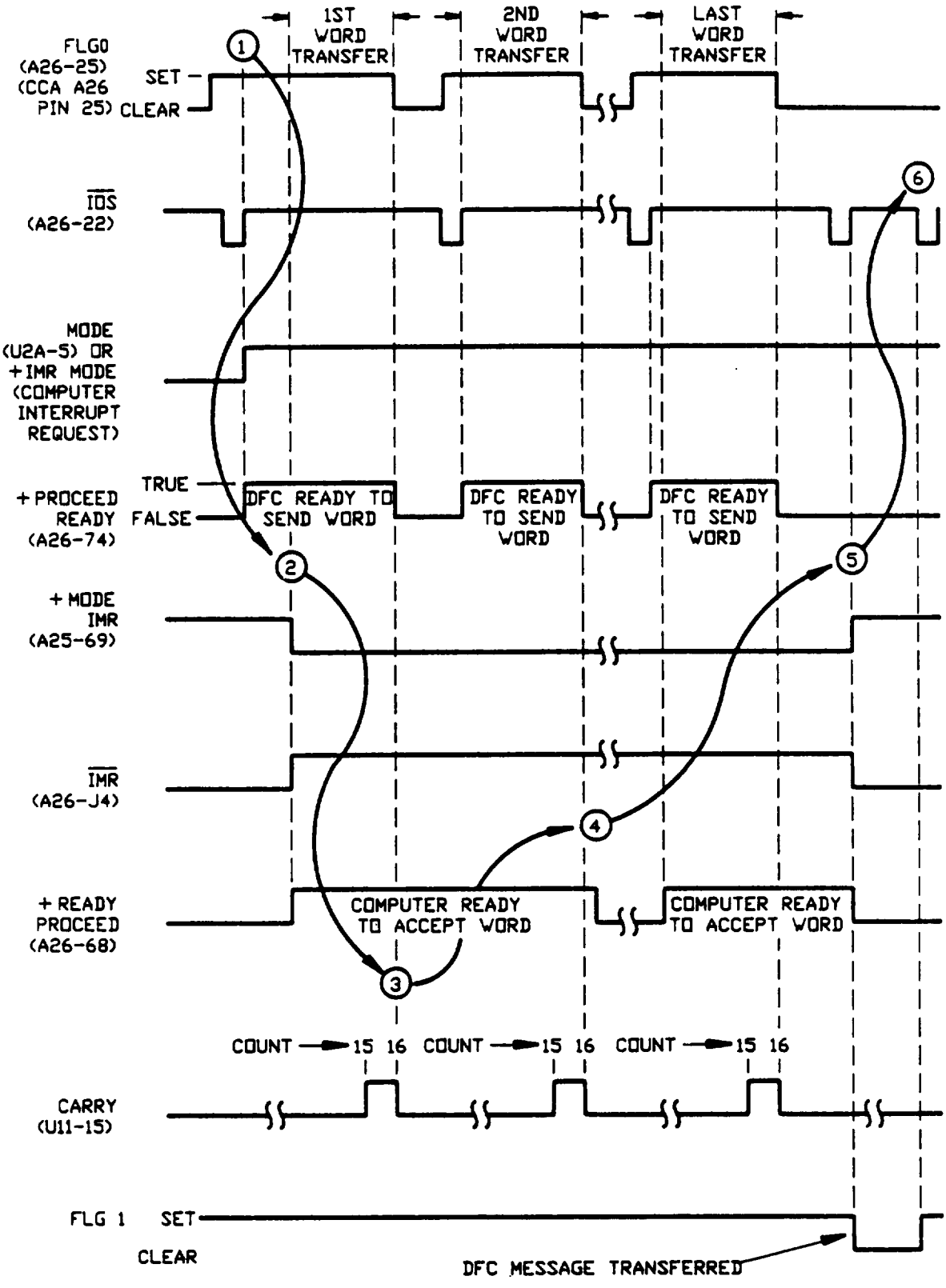


Figure 1-24. DF Control Message Output Timing Diagram

the start latch also provides a true (high) +PROCEED READY signal when combined with the true (high) FLG0 signal at line driver U18B.

1.3.4.2.2 Timing Sequence 2. When the program is ready for an interrupt, the computer responds to the true (high) +IMR MODE signal by driving +MODE IMR false low. This low is inverted by line receiver U23B to produce a high IMR signal. The rising edged IMR signal clocks and sets FLG1 latch U1A, enabling the FLG1 logic. The high IMR signal also enables DF control data line driver U12B, and inhibits line receiver U24B and U4D.

When ready to accept DF control data, the computer drives the +READY PROCEED line true (high). This high enables the clock generator and NFC clock line driver U12A via line receiver U23A and U8A. As a result, the clock generator provides a 1-MHz clock to the DF control output register via U24A, the computer input register via NFC line driver U12A, and to the 16-bit counter via U24A.

The DF control output register responds to the 1-MHz DATA CLK by converting the I/O bus word into serial data and shifting data out to the +DFC DATA line via U12B. The NFC clock output of U12A loads the serial DF control bit into the computer register half a clock period later. The 16-bit counter U11 is incremented each time DF control bit is transferred.

1.3.4.2.3 Timing Sequence 3. When the 15th bit is transferred, U11 reaches a count of 15, and the counter responds by producing a hiqh carry signal. The 16th count (concurrent with the transfer of the last, 16th, DF control bit) pulls the carry signal low. This low clears FLG0; driving the +PROCEED READY signal false (low), and resets the stop latch (U2B and U8D). The resulting low output of the stop latch clears start latch U1B. Cleared, the start latch drops its Q output low to disable the clock generator via the disable gate and provide a false low +PROCEED READY signal via line driver U18A.

The cleared (low) FLG0 informs the digital processor to place the next DF control message word on the 1/0 bus. Then an IOA 11_8 bus code is generated, FLG0 is set, and the IOS strobe again sets the I/O word logic to repeat the word transfer sequence.

1.3.4.2.4 Timing Sequence 4. The computer interprets data in the first received word as DF control message length. This tells the computer how many 16-bit words are in the DF control message. The computer responds to the second DF control word by driving +READY PROCEED false (low). When these words are processed, the computer drives +READY PROCEED true. Then +READY PROCEED is driven false after the next DF control word is transferred. The +READY PROCEED line is toggled true (high) when the computer is ready to accept the word, then false (low) after the word is transferred, for each subsequent DF control word.

1.3.4.2.5 Timing Sequence 5. When the last DF control word is transferred, the computer drives +MODE IMR high, while +READY PROCEED goes false. In response to the high +MODE IMR, U23B provides a low IMR input to the FLG1 logic. The logic then sends a CFLG1 signal to

the digital processor. The digital processor interprets the cleared FLG1 as a computer request to send a message.

1.3.4.2.6 Timing Sequence 6. The resulting interrupt 6 subroutine produces an IOA bus code of 31_8, a low IOM signal, and an IOS. The command decoder on CCA A26 responds to these inputs by clearing U1A, thereby initializing the FLG1 logic. IOM is driven high for the computer input message.

1.3.5 POWER DISTRIBUTION.

1.3.5.1 AC Power Distribution. Refer to Figure FO-27. AC power distribution consists of three phase, 115 Vat, 400 Hz applied to front panel connector J11. From J11, the 115 Vac is applied to vaneaxial blowers B1 and B2, which supply air circulation and cooling for the DF control. Phase one of the AC input also operates an AC timer. Pins E and F of J11 function as an interlock to indicate the AC voltage is applied to the DF control when it is operating in the system configuration.

1.3.5.2 DC Power Distribution. DC power distribution consists of +15 Vdc and -15 Vdc, -10 Vdc and +5 Vdc applied to front panel connector J12, along with appropriate return and sense lines. The +15 Vdc and -15 Vdc feed servo conversion CCA A19 via terminals E14 and E15 on the contact assembly. The -10 Vdc is applied through E16 to CCAs A18 and A35 via two busbars wired to pins 11 and 12 of each CCA. The +5 Vdc is applied through terminals E3 through E5, E8 and E9.

1.3.5.3 Thermistic Switch. The thermistic switch functions as an overtemperature sensor to provide a closed circuit indication if the temperature in the DF control becomes too high when the unit is operating in the system configuration.

CHAPTER 2

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

Direct support maintenance for the DF control is not required. Units removed during organizational maintenance are forwarded to the general support level for maintenance as described in Chapter 3.

CHAPTER 3

GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

Section I. REPAIR PARTS

3.1.1 COMMON TOOLS AND EOUIPMENT.

For authorized common tools and equipment, refer to the Modified Table of Organization and Equipment (MTOE), CTA 50-970, or CTA 8-100, as applicable to your unit.

3.1.2 SPECIAL TOOLS AND SUPPORT EQUIPMENT.

A list of special tools and Test, Measurement and Diagnostic Equipment (TMDE) is provided as part of the Maintenance Allocation Chart (MAC) located in Appendix B to this manual.

3.1.3 REPAIR PARTS.

Repair parts are listed and illustrated in the repair parts and special tools list, TM 32-5800-002-34P covering unit maintenance for this equipment.

Section II. SERVICE UPON RECEIPT

3.2.1 SERVICE UPON RECEIPT OF MATERIEL.

a. Inspect the equipment for damage incurred during shipment. If the equipment has been damaged, report the damage on SF 364, Report of Discrepancy (ROD), in accordance with AR 55-38, Reporting of Transportation Discrepancies in Shipments.

b. Check the equipment against the packing slip to see if the shipment is complete. Report all discrepancies on DA Form 2404, Equipment Inspection and Maintenance Work Sheets, in accordance with the instructions of DA PAM 738-750, The Army Maintenance Management System (TAMMS).

c. Check to see whether the equipment has been modified. Modified equipment has the Modification Work Order (MWO) number on the front panel, near the nomenclature plate. Also, check to see whether all currently applicable MWOs have been applied. Current MWOs applicable to the equipment are listed in DA PAM 25-30, Consolidated Index of Army Publications and Blank Forms.

3.2.2 INSTALLATION INSTRUCTIONS.

At the proper rack location, slide the DF control into the rack until the unit fully engages the mating dagger pins. Secure the DF control in place by tightening the two rack mounted anti-rotation knobs over the DF control hold-down hooks.

Attach all interconnecting cables to the connectors located on the front panel. Pin functions for each connector are contained in Appendix D.

Section III. EQUIPMENT CHECK PROCEDURES

3.3.1 EQUIPMENT CHECK.

This equipment does not require an individual equipment check after installation. Calibration and self-test of the DF control is in response to computer commands when the unit is part of a functional system.

Section IV. PREVENTIVE MAINTENANCE CHECKS AND SERVICES

3.4.1 PREVENTIVE MAINTENANCE.

Preventive Maintenance Checks and Services (PMCS) are essential for the efficient operation of the DF control. PMCS will aid in discovering and correcting defects before they result in serious malfunctions. The checks and services are listed in Table 3-1. Report any defects using the forms referenced in TM 38-750 (TAMMS).

Section V. TROUBLESHOOTING

3.5.1 TROUBLESHOOTING.

Troubleshooting consists of performing the system test for the DF control. If the test identifies the DF control as faulty, the DF control must be removed from the system and replaced. Troubleshooting allocated to General Support shall be in accordance with paragraph 3.6.10.

Table 3-1. Organizational Preventive Maintenance Checks and Services Monthly Schedule

NOTE

If the equipment must be kept in continuous operation, check and service only those items that can be checked and serviced without disturbing operation. Make the complete checks and services when the equipment can be shut down.

Item no.	Item to be checked	Procedure	Equipment will be reported not ready (Red) if:
		WARNING Ensure power source is disconnected before withdrawing the unit from the rack. Refer to system Technical Manual for system shutdown procedure. HIGH VOLTAGE may be present at the power connector connected to J11. This HIGH VOLTAGE could cause death.	
1	Front panel hardware	Check all hardware for tightness. All hardware should be securely mounted.	Hardware cannot be secured.
2	Front panel connectors	Check connectors for proper connection.	Connections cannot be secured.
3	Fans, B1& B2	Check fan for proper operation.	No air flow or excessively noisy operation.

Section VI. MAINTENANCE PROCEDURES

3.6.1 GENERAL.

This section provides maintenance instructions for those assemblies/ subassemblies of the DF control that are the responsibility of general support maintenance personnel, and are not tested with the AN/USM-410. Refer to TM 32-5811-012-40 for maintenance instructions for all CCAs tested with the AN/USM-410(V)2.

3.6.2 INSPECTION OF INSTALLED ITEMS.

WARNING

Before performing any inspection procedure, ensure that power is disconnected from the DF control.

AC neutral and ground are not the same. It is possible for voltage potentials to exist between ac neutral and ground. These potentials may cause shock and personal injury.

3.6.2.1 Chassis Inspection. To inspect the DF control chassis and chassis mounted components, remove top and bottom access covers in accordance with paragraph 3.6.4.1 and 3.6.4.2, then proceed as follows:

a. Check for discolored, burned or cracked wire insulation, or broken wires or terminals. Also check for cracked heatshrink tubing.

b. Check cables for correct pin depths.

c. Check for loose or broken tie wrap mounts, mounting clamps, or tiedown straps.

d. Check for discolored (cold), cracked, or loose solder connections.

e. Check for leaking, bulging, or burned transformers, capacitors, or filters.

f. Check for discolored, burned, powdered, or cracked diodes, resistors or other semiconductor devices.

g. Check for damaged brackets, covers, housings, and plates. Check for loose or missing attaching hardware.

h. Replace top and bottom access covers in accordance with paragraph 3.6.9.20 and 3.6.9.21.

i. Inspect exterior surfaces of the unit for dust, chipped paint, and corrosion. If necessary, spot paint surfaces as follows:

(1) Remove rust and corrosion from metal surfaces by lightly sanding them with No. 000 sandpaper (item 8, App. C).

(2) Brush two coats of light green semi-gloss enamel (item 6, App. C).

(3) Refer to the applicable cleaning and refinishing practices specified in TM 43-0118.

3.6.2.2 CCA Inspection. To inspect CCAs within the DF control, remove the top and bottom access covers in accordance with paragraph 3.6.4.1 and 3.6.4.2, then proceed as follows:

CAUTION

Certain CCAs contain electrostatic discharge sensitive (ESDS) devices that can be damaged by static electricity. Special handling methods and materials must be used to prevent damage. DO not touch or remove any ESDS device or circuit without properly grounding your body, tools, and test equipment. Handle such CCAs on the edges only, and store such CCAs in conductive (antistatic) bags.

a. Check for cracked or broken ejectors.

b. Check for cracked circuit card.

c. Check for loose or damaged shields or heatsinks.

d. Check for printed wiring traces that are loose, broken, or otherwise damaged.

e. Check for loose, burned, or broken switches or connectors.

f. Check for discolored, burned, or broken wiring straps.

g. Check for cracked, discolored, or burned component insulator pads.

h. Check for burned, powdered, or broken resistors, diodes, transistors, and ICs.

i. Check for leaking, bulging, cracked, burned, or powdered capacitors or inductors.

j. Replace top and bottom access covers in accordance with paragraph 3.6.9.20 and 3.6.9.21.

3.6.3 CLEANING.

Make sure exterior surfaces of the equipment are clean. To clean the DF control, proceed as follows:

a. Remove dust and loose dirt with a clean, soft cloth (item 4, App. C).

b. Remove dust and dirt from plugs and jacks with a soft bristle brush (item 3, App. C).

WARNING

Adequate ventilation must be provided while using trichlorotrifluoroethane. Prolonged breathing of vapor should be avoided. The solvent must not be used near heat or open flame; the products of decomposition are toxic and irritating. Since trichlorotrifluoro-ethane dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use heavy duty rubber gloves (item 7, App. C) that the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

c. Remove grease, fungus, and ground-in dirt using a cloth dampened (not wet) with trichlorotrifluoroethane (item 13, App. C).

3.6.4 REMOVAL PROCEDURES.

These procedures describe how to remove those assemblies and subassemblies of the DF control that are not tested with the AN/USM-410(V)2 and are authorized to be replaced at the general support level. Removal procedures are presented in a logical sequence to completely disassemble the DF control. Disassemble the equipment only to the extent necessary to perform a particular repair function. Refer to Figure 3-2 for component location.

WARNING

Before performing any removal procedure, ensure that power is disconnected from the DF control.

3.6.4.1 Top Access Cover Removal. To remove the top access cover (1) from the DF control, loosen the 26 screw fasteners (2) that are part of the cover, then lift the cover off of the chassis (3).

3.6.4.2 Bottom Access Cover Removal. To remove the bottom access cover (4) from the DF control, loosen the 26 screws (2) that are part of the cover, then lift the cover off the chassis (3).

CAUTION

Certain CCAs in the DF control contain electrostatic discharge sensitive (ESDS) devices that can be damaged by static electricity. Special handling methods and materials must be used to prevent damage. Do not touch or remove any ESDS device or circuit without properly grounding your body, tools, and test equipment. Handle such CCAs on the edges only, and store such CCAs in conductive (antistatic) bags.

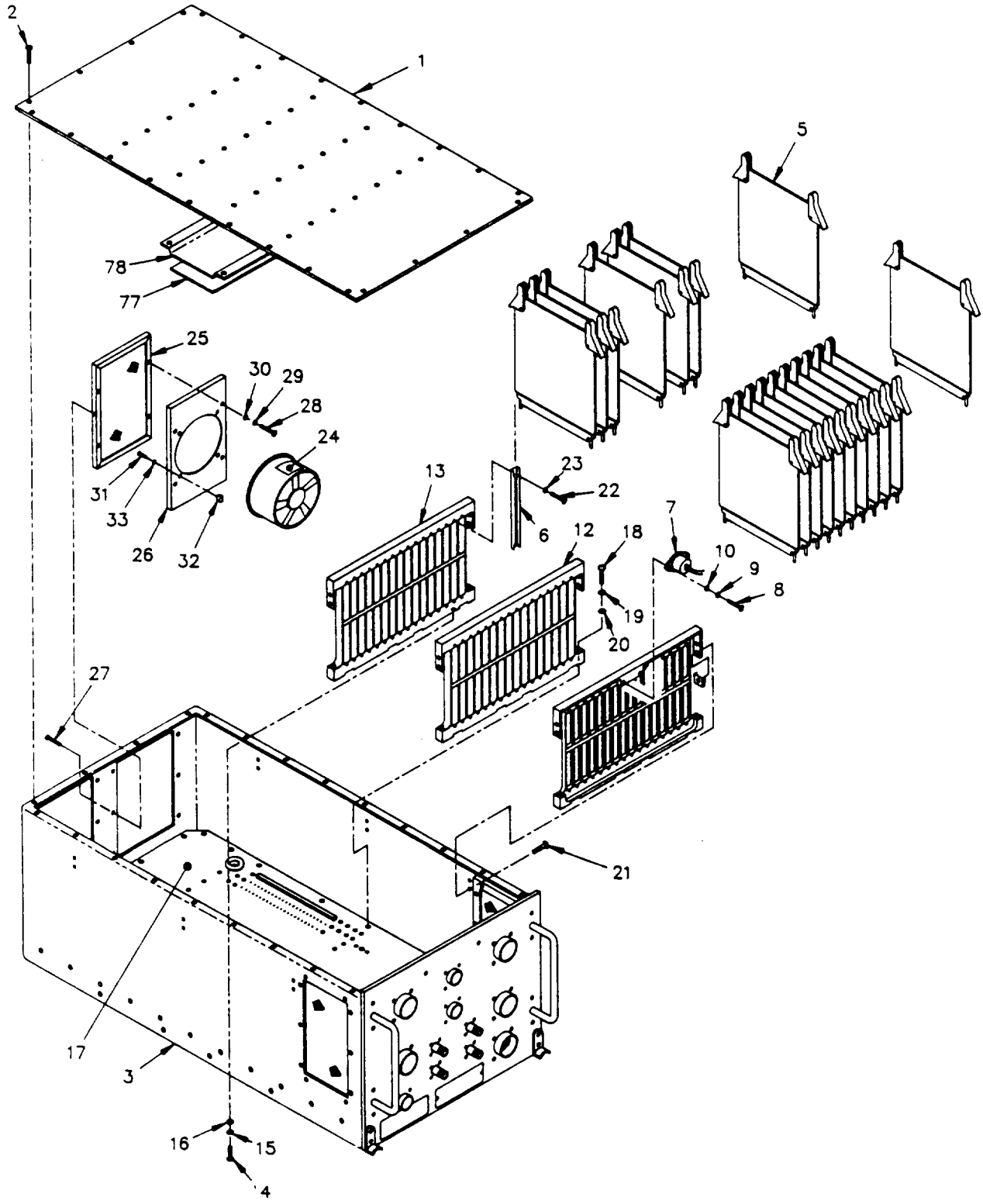


Figure 3-1. Direction Finder Control (1 of 3)

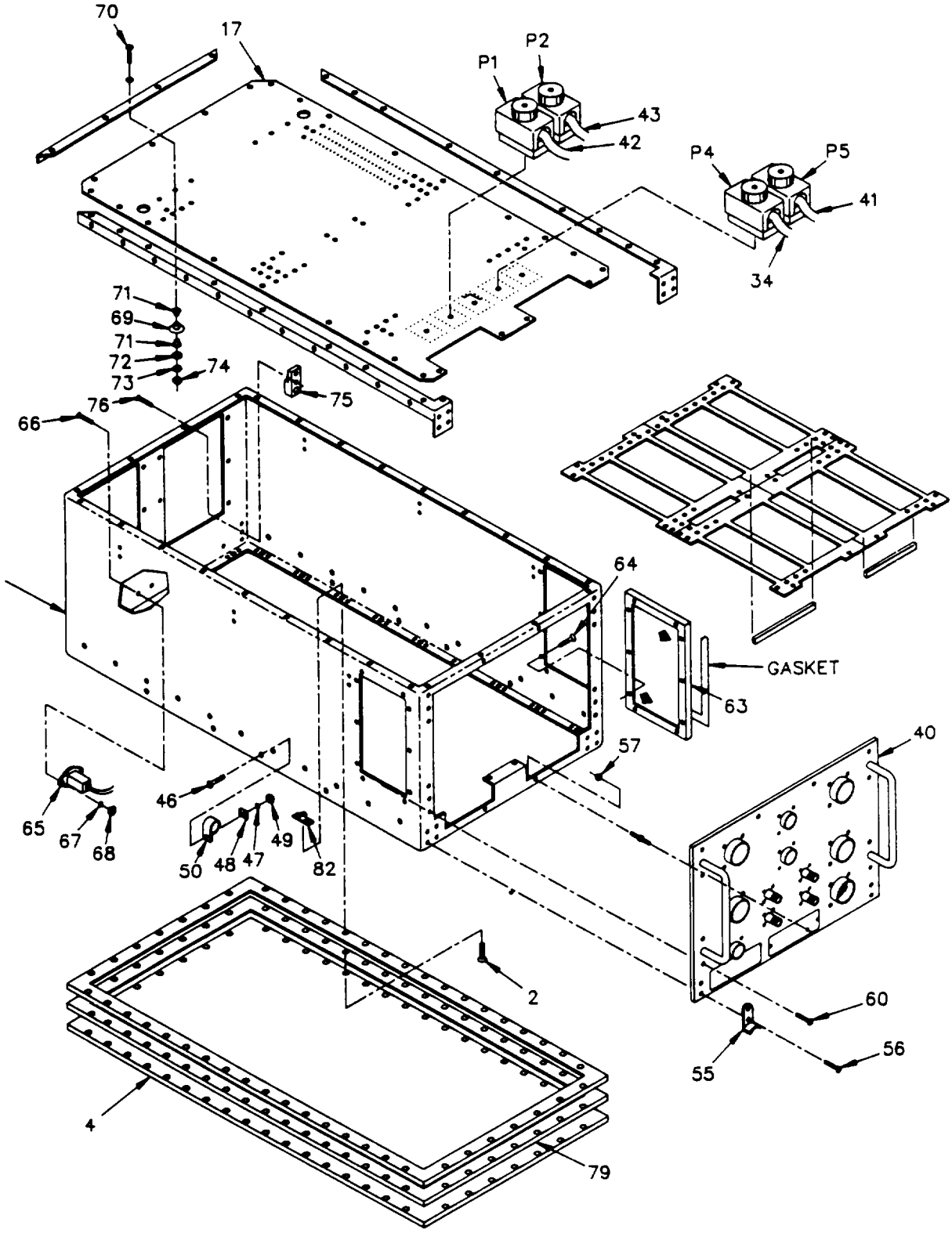


Figure 3-1. Direction Finder Control (2 of 3)

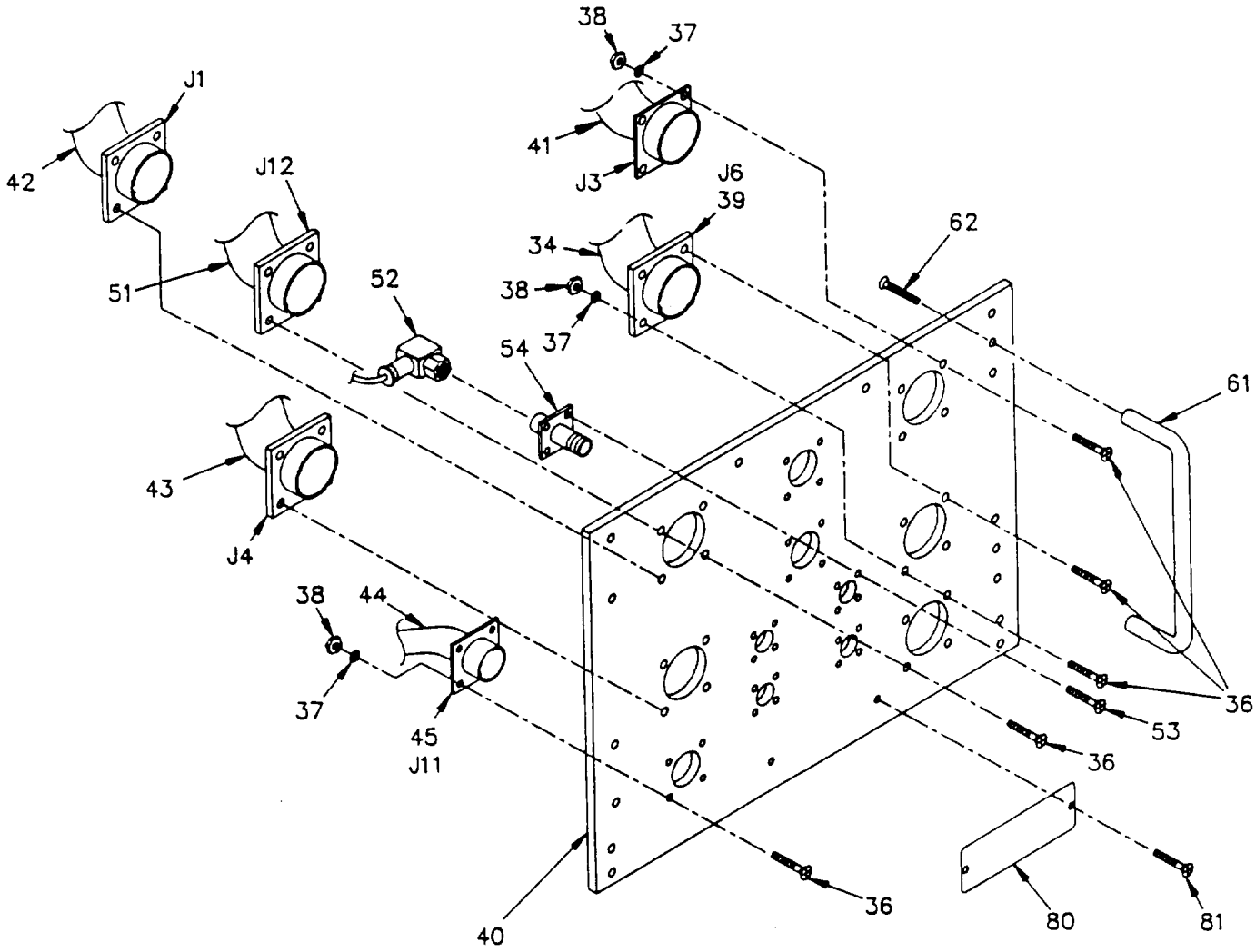


Figure 3-1. Direction Finder Control (3 of 3)

3.6.4.3 CCA Removal. To remove CCA (5) from the DF control, remove top access cover (1) in accordance with paragraph 3.6.4.1, then lift up on the CCA ejectors to free the card from the connector, and pull the CCA out of the card guides (6).

3.6.4.4 Thermister Switch S1 Removal. To remove thermister switch S1 (7) from the DF control, proceed as follows:

a. Remove top access cover (1) in accordance with paragraph 3.6.4.1.

b. Tag wires that connect to S1 for proper reconnection, then remove heatshrink tubing covering solder connections, desolder and remove wires from thermister switch S1.

c. Remove two screws (8), lockwashers (9), and flat washers (10) that secure S1 to front CCA mounting guide plate (11) ; then remove S1.

3.6.4.5 CCA Mounting Guide Plate Removal. To remove the front, center, or rear CCA mounting guide plate (11, 12, or 13), proceed as follows:

a. Remove top and bottom access covers (1 and 4) in accordance with paragraphs 3.6.4.1 and 3.6.4.2.

b. Remove CCAs as needed in accordance with paragraph 3.6.4.3.

c. If front guide plate (11) is being removed, remove thermistic switch S1 in accordance with paragraph 3.6.4.4.

d. Place DF control chassis (3) bottom-side up.

CAUTION

When performing step d, be extremely careful not to damage contact assembly wiring when removing screws.

e. Remove four screws (14), lockwashers (15) , and flat washers (16) that secure guide plate (11, 12, or 13) to contact assembly (17).

f. Place DF control chassis right-side up and remove two screws (18), lockwashers (19), and flat washers (20) that secure guide plate to chassis (inside).

g. Remove four screws (21, two on each side) that secure guide plate to upper part of chassis.

3.6.4.6 CCA Card Guide Removal. The CCA mounting guide plates (front, center, and rear) contain 72 card guides for the CCAs in the DF control. To remove a card guide (6) , proceed as follows:

a. Remove top and bottom access covers (1 and 4) in accordance with paragraphs 3.6.4.1 and 3.6.4.2.

b. Remove CCAs as needed in accordance with paragraph 3.6.4.3.

c. Remove two screws (22) and lockwashers (23) that secure CCA card guide to guide plate and remove card guide.

d. Remove applicable CCA mounting guide plate in accordance with paragraph 3.6.4.5.

3.6.4.7 Vaneaxial Fan Assembly Removal. A vaneaxial fan assembly consists of the fan (24), air interlock panel (25), and fan spacer (26). To remove a vaneaxial fan assembly from the DF control, proceed as follows:

a. Remove top and bottom access cover (1 and 4) in accordance with paragraphs 3.6.4.1 and 3.6.4.2.

b. Remove Ty-wrap on underside of cabinet to allow fan to be lifted out.

c. Grasp fan (24) with your hand, then remove 10 screws (27) that secure fan assembly to rear portion of chassis.

d. Carefully lift fan assembly out of chassis to obtain access to fan wiring.

e. Tag wiring for proper reconnection, then remove wires from fan terminal strip. Be sure to replace screws back into terminal strip for later use.

3.6.4.8 Special Purpose Cable Assembly W1 Removal. Special purpose cable assembly WI (34) consists of front panel connector J6, connector P4, and related wiring. To remove W1 from the DF control, proceed as follows:

a. Remove top access cover (1) in accordance with paragraph 3.6.4.1.

b. Loosen and remove connector P4 from J4 on contact assembly (17).

c. Remove fOUr screws (36), flat washers (37), and nuts (38) that secure connector J6 (39) to front panel (40). Remove any wires secured to a connector mounting screw, then remove special purpose cable assembly W1 from chassis. As required, remove any lacing necessary to remove W1.

3.6.4.9 Special Purpose Cable Assembly W2 Removal. Special purpose cable assembly W2 (41) consists of front panel connector J3, connector P5, and related wiring. Removal procedures for W2 are the same as for W1. To remove W2, refer to paragraph 3.6.4.8.

3.6.4.10 Special Purpose Cable Assembly W3 Removal. Special purpose cable assembly W3 (42) consists of front panel connector J1, connector P1, and related wiring. Removal procedures for W3 are the same as for W1. To remove W3, refer to paragraph 3.6.4.8.

3.6.4.11 Special Purpose Cable Assembly W4 Removal. Special purpose cable assembly W4 (43) consists of front panel connectors J2, J4, and J5, connector P2, and related wiring. Removal procedures for W4 are the same as for W1. To remove W4. refer to paragraph 3.6.4.8.

NOTE

Unsolder wires leading to thermistic relay.

3.6.4.12 Special Purpose Cable Assembly W5 Removal. Special purpose cable assembly W5 (44) consists of front panel connector J11 and related wiring. To remove W5 from the DF control, proceed as follows:

a. Remove bottom access cover (4) in accordance with paragraph 3.6.4.2.

b. Remove four screws (36), flat washers (37), and nuts (38) that secure connector J11 (45) to front panel.

c. Tag wiring for proper reconnection, then disconnect or unsolder wires of cable assembly at terminating locations. Refer to F0-26.

d. Cut lacing cord as required to divorce W5 from W6, then remove screw (46), lockwasher (47), saddle washer (48), and nut (49).

3.6.4.13 Special Purpose Cable Assembly W6 Removal. Special purpose cable assembly W6 (51) consists of front panel connector J12 and related wiring. Removal procedures for W6 are the same as for W5. To remove W6, refer to paragraph 3.6.4.12.

3.6.4.14 RF Cable Assemblies W7 Through W10 Removal. To remove an RF cable assembly (52) from the DF control, proceed as follows:

a. Remove top and bottom access covers (1 and 4) in accordance with paragraph 3.6.4.1 and 3.6.4.2.

b. Tag cable to be removed for proper reconnection, then unsolder cable at terminating locations.

c. Cut lacing cord as required and remove cable.

d. Remove cable connector from adapter connector (54) and remove cable from chassis.

3.6.4.15 Holddown Hook Removal. To remove either of the two holddown hooks (55) from the lower corners of the front panel (40), remove two screws (56) that secure holddown hook to front panel.

3.6.4.16 Front Panel Removal. To remove the front panel (40) from the DF control, proceed as follows:

a. Remove top and bottom access covers (1 and 4) in accordance with paragraphs 3.6.4.1 and 3.6.4.2.

b. Remove front panel connectors in accordance with paragraphs 3.6.4.8 through 3.6.4.14.

c. Remove two holddown hooks (55) in accordance with paragraph 3.6.4.15.

d. Remove two nuts (57) that secure bottom of front panel to front chassis frame. Nuts are accessible from inside chassis.

e. Remove 10 screws (60) that secure front panel to chassis, then remove front panel.

3.6.4.17 Bow Handles Removal. To remove a bow handle (61) from the DF control, proceed as follows:

a. Remove front panel (40) from chassis in accordance with paragraph 3.6.4.16.

b. Remove two screws (62) that secure handle to front panel.

3.6.4.18 Air Exhaust Panel Removal. To remove an air exhaust panel (63) from the DF control, remove top access cover (1) in accordance with paragraph 3.6.4.1, then remove the 10 screws (64) that secure the panel to the side of the chassis and remove the panel.

3.6.4.19 Total Time Meter Removal. To remove the total time meter (65) from the rear of the DF control, proceed as follows:

a. Remove bottom access cover (4) in accordance with paragraph 3.6.4.2.

b. Slide heatshrink tubing away from terminals, tag wires for proper reconnection, then unsolder wires.

c. Remove two screws (66), flat washers (67), and nuts (68) that secure meter to chassis (3) , then remove meter.

3.6.4.20 Terminal Stud Removal. To remove terminal stud E14, E15, or E16 (69) from the DF control, proceed as follows:

a. Remove top and bottom access covers (1 and 4) in accordance with paragraph 3.6.4.1 and 3.6.4.2.

NOTE

If long screwdriver is not available, blower must be removed (right side).

b. Tag all wires for proper reconnection, then unsolder wires from terminal stud.

c. Remove screw (70), two nylon sleeves (71), flat washer (72), lockwasher (73), and nut (74) that secure terminal stud to chassis (3), and remove terminal stud.

3.6.4.21 Support Plate Removal. To remove a support plate (75) from the rear bottom corner of the DF control, remove the bottom access cover (4) in accordance with paragraph 3.6.4.2, then remove two screws (76) that secure plate to chassis (3) and remove plate.

3.6.4.22 Identification Plate Removal. To remove the identification plate (80) from the front panel (40), remove the two screws (81) that secure the identification plate to the panel and remove the plate.

3.6.5 DISASSEMBLY PROCEDURES.

The following paragraphs describe how to disassemble the vaneaxial fan assembly and special purpose cable assemblies W1 through W4 and W6. Refer to Figures 3-1 and 3-2 as applicable.

3.6.5.1 Vaneaxial Fan Assembly Disassemble. To disassemble the vaneaxial fan assembly, proceed as follows:

a. Remove four screws (28), lockwashers (29), and flat washers (30) that secure air interlock panel (25) to fan spacer (26), then remove air interlock panel.

b. Rotate four screws (31) that secure fan (24) to fan spacer until rim clamps (32) release fan and permit it to be removed.

c. To remove a rim clamp from the fan spacer, grasp clamp with pliers and remove screw (31) and flat washer (33).

3.6.5.2 Special purpose Cable Assembly Disassemble. Special purpose cable disassembly consists of removing the front panel connector and when applicable, disassembling and removing the backplane connector. To disassemble a special purpose cable, refer to Figure 3-2 and proceed as follows:

3.6.5.2.1 Backplane Connector P1 thru P4.

a. Grasp knob (1) and remove retaining screw (2), then carefully pry knob off of machine bolt (3).

b. Turn connector over to expose bottom, then remove two screws (4) that secure cover (5) to insulator plate (6) and remove cover.

c. Remove two screws (7) that secure cable clamp (8) to insulator plate and remove cable clamp.

d. Tag all wires for proper reconnection, then use extractor tool to remove wires from insulator plate.

3.6.5.2.2 Front Panel Connectors. To remove a broken or defective front panel connector, proceed as follows:

a. Remove wire harness assembly and defective connector in accordance with paragraph 3.6.4.8 through 3.6.4.14 as applicable.

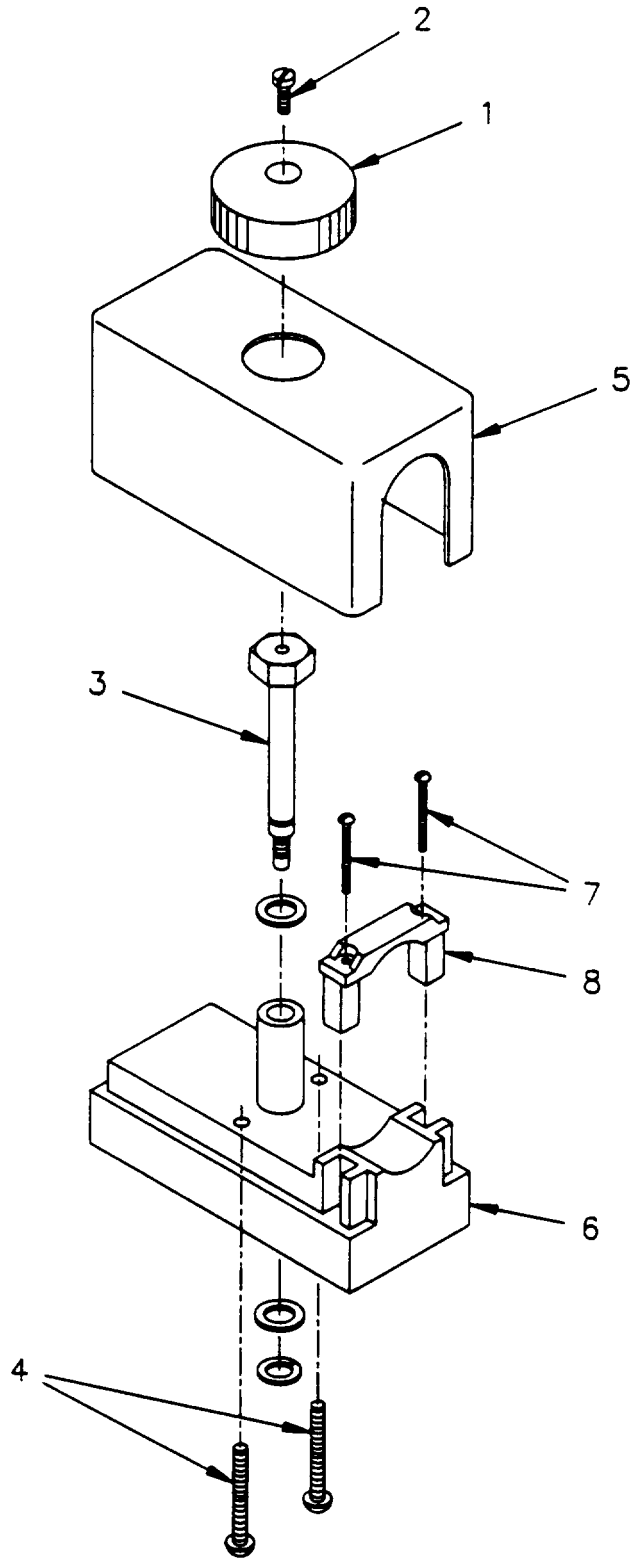


Figure 3-2. Connectors W1P4, W2P5, W3P1, and W4P2

b. Using masking tape or some other means of identification, tag all wires for reconnection purposes.

c. Using extractor tool, remove wires from connector.

3.6.6 REPAIR PROCEDURES.

This paragraph describes how to repair those assemblies/components that are authorized to be repaired at the general support level, and which are not tested with ATE.

3.6.6.1 Top Access Cover Repair. The following procedures describe how to repair the top access cover by removing and replacing a bracket, electrical shield gasket, silicone sponge pad, externally relieved body screw or label. Refer to Figure 3-1 for parts location.

3.6.6.1.1 Bracket Replacement. To replace a defective bracket, proceed as follows:

a. Remove rivets securing damaged bracket (78) to top access cover in accordance with paragraph 3.6.6.3.1, steps a. through e.

b. Mount replacement bracket to underside of access cover and secure with new rivets in accordance with paragraph 3.6.6.3.1, step f.

3.6.6.1.2 Electrical Shield Gasket Relacement. To replace a damaged shield gasket (79) , proceed as follows:

a. Remove rivets securing damaged shield gasket (79) to top access cover in accordance with paragraph 3.6.6.3.1, steps a. through e.

b. Mount replacement shield gasket to underside of access cover and secure with new rivets in accordance with paragraph 3.6.6.3.1, step f.

3.6.6.1.3 Captive Screw Replacement. To replace a damaged captive screw (2) , proceed as follows:

a. Remove a sufficient number of rivets surrounding the area where defective captive screw (2) is located. (Refer to paragraph 3.6.6.3.1, steps a. through e.)

b. pull shield gasket (79) away from plate a sufficient amount to gain access to defective screw, then use pair of dikes to cut off screw threads. Remove washer and defective screw.

c. Obtain replacement, and use center punch and hammer to make washer conical in shape.

d. Place conically shaped washer over hole in access plate where defective screw was removed. Use pliers to secure washer.

e. Thread replacement captive screw into hole and through washer. Use pliers to flatten washer as much as possible. Replace rivets to secure shield gasket (79) to plate in accordance with paragraph 3.6.6.3.1, step f.

3.6.6.1.4 Silicone Sponge Replacement. To replace the silicone sponge (77) , proceed as follows:

a. Use knife or other sharp tool to cut away and remove damaged silicone sponge pad.

WARNING

Adequate ventilation must be provided while using trichlorotrifluoroethane. Prolonged breathing of vapor should be avoided. The solvent must not be used near heat or open flame; the products of decomposition are toxic and irritating. Since trichlorotrifluoro-ethane dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use heavy duty rubber gloves (item 7, App. C) that the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

b. Remove old adhesive using a cloth dampened (not wet) with trichlorotrifluoroethane (item 13, App. C).

c. Cut two lengths of silicone sponge (item 9, App. C) approximately 2 3/8 x 8 7/8 inches.

d. Apply type 1 adhesive (item 1, App. C) sparingly to top surface of bracket, then press sponge down onto bracket.

3.6.6.1.5 Label Replacement. To replace either of the two labels on the underside of the top access cover, proceed as follows:

a. Use knife or other sharp instrument to lift corner of damaged label and peel it off cover.

WARNING

Adequate ventilation must be provided while using trichlorotrifluoroethane. Prolonged breathing of vapor should be avoided. The solvent must not be used near heat or open flame; the products of decomposition are toxic and irritating. Since trichlorotrifluoro-ethane dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use heavy duty rubber gloves (item 7, App. C) that the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

b. Clean area with a cloth dampened (not wet) with trichloro-trifluoroethane (item 13, App. C). Allow one-minute drying time.

c. Remove backing from replacement label. Verify that label is oriented correctly and apply it to access cover.

3.6.6.2 Bottom Access Cover Repair. The bottom access cover is repaired by removing and replacing the electrical shielding gasket or a captive screw. To replace these items, refer to paragraph 3.6.6.1.2 and 3.6.6.1.3.

3.6.6.3 Chassis Repair. The following procedures describe how to repair the chassis by removing and replacing a damaged rivet, nut plate, electrical shield gasket, or cable mount or grommet.

3.6.6.3.1 Rivet Replacement. To replace a rivet(s) on the chassis, proceed as follows:

a. Remove covers and components as required to gain access to rivet(s) to be replaced. (Refer to paragraph 3.6.4.)

b. Center punch the rivet head of rivet to be replaced.

c. Using a drill smaller than the diameter of the rivet, drill out the center of rivet head to be replaced.

d. Increase the size of the drill to rivet size or a size slightly smaller than rivet size, and again drill out rivet head. Rivet head should fall off at this point. If not, position a punch or similar tool against the rivet head and strike it with a hammer.

e. Using a punch and a hammer, punch out the remainder of the rivet to be replaced.

f. Obtain and install appropriate size rivet. Using the riveter and appropriate size head, install the replacement rivet.

g. Replace covers and components in accordance with procedures in paragraph 3.6.9.

3.6.6.3.2 Nut Plate Replacement. To replace a damaged nut plate (82) on the chassis, proceed as follows:

a. Remove covers and components as required to gain access to nut plate. (Refer to paragraph 3.6.4.)

b. Remove two rivets that secure nut plate (82) to chassis in accordance with paragraph 3.6.6.3.1, steps a. through e.

c. Remove damaged nut plate. Secure replacement nut plate to chassis with two rivets in accordance with paragraph 3.6.6.3.1, step f.

3.6.6.3.3 Electrical Shield Gasket Replacement. To replace a damaged electrical shield gasket strip around the air interlock panel (25) or the exhaust air panel (63), proceed as follows:

a. Remove covers and/or components as required to gain access to damaged gasket strip. (Refer to paragraph 3.6.4.)

b. Use knife or other sharp instrument to lift corner of gasket strip and pressure sensitive tape, then peel damaged portion off component.

WARNING

Adequate ventilation must be provided while using trichlorotrifluoroethane. Prolonged breathing of vapor should be avoided. The solvent must not be used near heat or open flame; the products of decomposition are toxic and irritating. Since trichlorotrifluoroethane dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use heavy duty rubber gloves (item 7, App. C) that the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

c. Clean area with a cloth dampened (not wet) with trichlorotrifluoroethane (item 13, App. C). Allow one-minute drying time.

d. Cut gasket strip to size, remove adhesive backing, and press into place.

3.6.6.3.4 Grommet Repair. Should a plastic grommet come loose from the chassis, proceed as follows:

a. Remove cover and/or components in accordance with procedures in paragraph 3.6.4 to obtain access to area where repair is to occur.

WARNING

Adequate ventilation must be provided while using trichlorotrifluoroethane. Prolonged breathing of vapor should be avoided. The solvent must not be used near heat or open flame; the products of decomposition are toxic and irritating. Since trichlorotrifluoroethane dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use heavy duty rubber gloves (item 7, App. C) that the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

b. Remove old adhesive using a cloth dampened (not wet) with trichlorotrifluoroethane (item 13, App. C).

c. After one minute drying time, apply coating of clear adhesive, type 910 (item 2, App. C) to surface where part is to be mounted, then press part into adhesive and allow to dry.

d. Replace covers and components in accordance with procedures in paragraph 3.6.9.

3.6.6.4 Cable Assembly Repair. Cable assembly repair consists of replacing a backplane connector, panel-mounted connector or a damaged wire. To repair a cable assembly, proceed as follows:

a. If a backplane connector is defective, remove and replace it in accordance with paragraphs 3.6.5.2.1 and 3.6.7.2.1.

b. If a panel-mounted connector is defective, remove and replace it in accordance with paragraph 3.6.5.2.2 and 3.6.7.2.2.

c. If a continuity check of the cable harness reveals a defective wire, two methods of repair are possible:

(1) Use extractor tool to remove contact and defective wire from both connectors. Cut off both ends of defective wires and leave wire in harness.

(2) Cut new wires to length, then attach correct contact to each wire end and crimp.

(3) Use insertion tool to insert contacts into connectors.

(4) Use lacing tape (item 12, App. C) to secure the wire to the cable harness.

d. If a continuity check reveals several defective wires in the harness, use the second method of repair as follows:

(1) Cut away all lacing to expose defective wires, then use extractor tool to remove contacts and defective wires from harness.

(2) Cut new wires to length, attach new contacts and crimp. Use insertion tool to insert new wires into connectors, then use lacing tape (item 12, App. C) to relate cable harness.

3.6.6.5 RF Cable Assembly Repair An RF cable assembly can be repaired by removing and replacing a defective RF connector. To repair an RF cable assembly, proceed as follows:

a. Loosen and remove nut at back of connector, then remove cable from connector body.

b. Cut outer insulation, shielding and dielectric back a sufficient amount to expose enough center conductor to attach center pin. Attach center pin.

c. Slip outer sleeve braid protector onto cable, then insert cable into connector body and tighten nut onto back of connector.

3.6.6.6 CCA Mounting Guide Plate Repair. The front, center and rear CCA mounting guide plates (11, 12, and 13) are repairable by removing and replacing a damaged self-locking clinch nut. To replace a clinch nut (rivetless nut plate), proceed as follow:

a. Use a 100°, 90° or 82° countersink bit with hand drill or drill. press to mill the corner of the clinch nut swage or flare. Refer to Figure 4-5. Be careful not to damage opening.

b. Use a center punch and mallet to carefully tap out clinch nut.

c. Insert replacement clinch nut into opening. Attach hand tool (Figure 3-4) to nut and swage nut sleeve into place.

3.6.7 REASSEMBLY PROCEDURES.

Reassembly procedures contained in this manual are limited to those procedures that are performed on a SRU/assembly that is not tested with the AN/USM-410(V)2 ATE. These procedures include reassembly of the vaneaxial fan assembly and special purpose cable assemblies. Refer to Figures 3-1 and 3-2 as applicable.

3.6.7.1 Vaneaxial Fan Assembly Reassembly. To reassemble the vaneaxial fan assembly, proceed as follows:

a. Mount fan (24) to fan spacer (26) and secure with rim clamps (32) by rotating four screws (31) until rim clamps have secured fan to spacer.

b. Secure air interlock panel (25) to fan spacer using four screws (28), lockwashers (29), and flat washers (30).

3.6.7.2 Special Purpose Cable Assembly Reassemble. Special purpose cable reassembly consists of replacing front panel connectors, and when applicable, replacing a backplane connector. To reassemble a special purpose cable, refer to Figure 3-2 and proceed as follows:

3.6.7.2.1 Backplane Connector P1 thru P4.

a. Use insertion tool to insert wires into insulator plate (6) as marked during disassembly.

b. Secure cable harness to insulator plate using cable clamps (8) . Secure clamp to plate with two screws (7).

c. Place cover (5) on insulator plate (6) and secure with two screws (7).

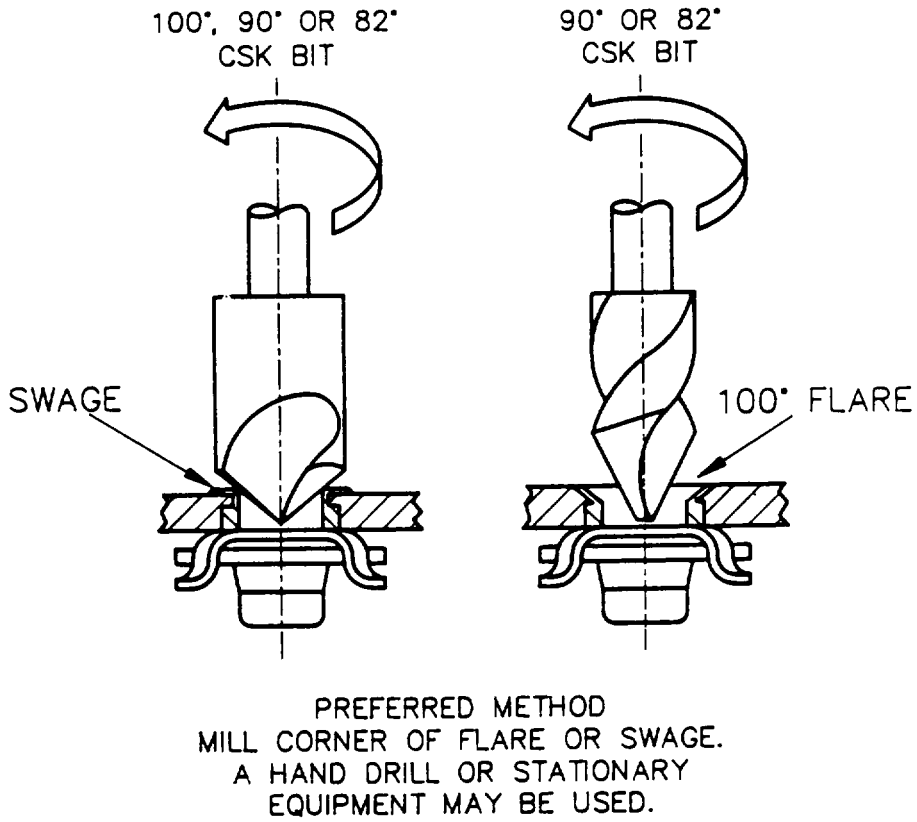


Figure 3-3. Preferred Method for Removing Clinch Nut

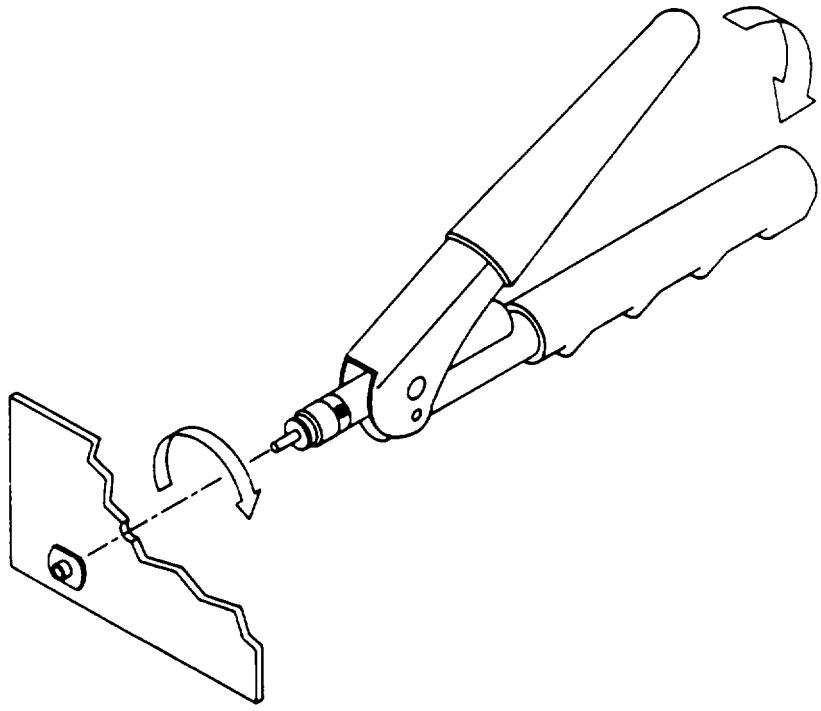


Figure 3-4. Clinch Nut Installation Tool

d. Mount knob (1) onto machine bolt head and secure with retaining screw (2).

3.6.7.2.2 Front Panel Connectors. To reassemble a front panel connector, use insertion tool to insert wires into connector as tagged during disassembly.

3.6.8 ALINEMENT PROCEDURES.

Alinement procedures contained in this manual are limited to those procedures that are performed on a SRU/assembly that is not tested with the AN/USM-410 ATE. All SRUs/assemblies within the DF control are tested with the AN/USM-410; therefore, no alinement procedures are presented in this section.

3.6.9 REPLACEMENT PROCEDURES.

Replacement procedures in this manual describe how to replace those SRUs/assemblies of the DF control that are not tested with the AN/USM-410 and are authorized to be replaced at the general support level. Replacement procedures are presented in a logical sequence to completely reassemble the DF control. Refer to Figure 3-1 for component locations.

WARNING

Before performing any replacement procedure, ensure that power is disconnected from the DF control.

3.6.9.1 Support Plate Replacement. To replace a support plate (75) at the rear bottom corners of the DF control, apply type 242 locking compound (item 5, App. C) to two screws (76) , then use screws to secure the plate to the chassis (3). Replace bottom access cover (4) in accordance with paragraph 3.6.9.20.

3.6.9.2 Terminal Stud Replacement. To replace terminal stud E14, E15, or E16 (69) in the DF control, proceed as follows:

a. Secure terminal stud to chassis (3) with screw (70), two nylon sleeves (71), flat washer (72), lockwasher (73), and nut (74). Be sure to mount nylon sleeves to insulate terminal stud from chassis.

b. Solder wires to terminal stud as tagged during removal.

c. Replace top and bottom access covers (1 and 4) in accordance with paragraphs 3.6.9.21 and 3.6.9.20.

3.6.9.3 Total Time Meter Replacement. To replace the total time meter (65) at the rear of the DF control, proceed as follows:

a. Mount total time meter to inside of chassis (3) and secure with two screws (66), flat washers (67), and nuts (68).

b. Slide length of heatshrink sleeving (item 10, App. C) over wires that connect to time meter. Solder wires to time meter as tagged during removal, then slide heatshrink sleeving over connection and shrink.

c. Replace bottom access cover (4) in accordance with paragraph 3.6.9.20.

3.6.9.4 Air Exhaust Panel Replacement. Refer to paragraph 3.6.6.3.3 for electrical shield replacement. To replace an air exhaust panel (63) in the DF control, mount the panel to the inside of the chassis (3) and secure it with 10 screws (64). Replace the top access cover (1) in accordance with paragraph 3.6.9.21.

3.6.9.5 Bow Handle Replacement. To replace a bow handle (61) on the DF control front panel, proceed as follows:

a. Mount handle to outside of front panel and secure with two screws (62).

b. Reassemble front panel to chassis in accordance with paragraph 3.6.9.6.

3.6.9.6 Front Panel Replacement. To replace the front panel (40) on the DF control, proceed as follows:

a. Mount front panel to chassis (3) and secure with 10 screws (60) .

b. Secure bottom of front panel to chassis frame using two flat washers (59), lockwashers (58), and nuts (57).

c. Install two holddown hooks (55) in accordance with paragraph 3.6.9.7.

d. Replace front panel connectors in accordance with paragraphs 3.6.9.8, 3.6.9.9, and 3.6.9.13.

e. Replace top and bottom access covers (1 and 4) in accordance with paragraphs 3.6.9.21 and 3.6.9.20.

3.6.9.7 Holddown Hook Replacement. To install either of the two holddown hooks (55) at the lower corners of the front panel (40), secure the holddown hooks to the panel with two screws (56).

3.6.9.8 RF Cable Assemblies W7 thru W10 Replacement. To replace an RF cable in the DF control, proceed as follows:

a. Install adapter connector (54) to RF cable connector.

b. Place chassis bottom-side up, then route RF cable being replaced so that it follows route of other RF cables. Use lacing tape (item 12, App. C) to lace cable in with other RF cables.

c. Solder RF cable to terminating location as tagged during removal.

d. Replace bottom access cover (4) in accordance with paragraph 3.6.9.20.

3.6.9.9 Special Purpose Cable Assembly W1 Replacement. To replace special purpose cable assembly W1 (34) in the DF control, proceed as follows:

a. Mount front panel connector J6 (39) to front panel with four screws (36), flat washers (37), and nuts (38). Be sure to secure ground wires to one of attaching screws.

b. Connect backplane connector P4 (35) to J4 on contact assembly (17) and secure by tightening connector knob.

c. Replace top access cover (1) in accordance with paragraph 3.6.9.21.

3.6.9.10 Special purpose Cable Assembly W2 Replacement. Replacement procedures for special purpose cable assembly W2 (41) are the same as for W1. To replace W2, refer to paragraph 3.6.9.9.

3.6.9.11 Special Purpose Cable Assembly W3 Replacement. Replacement procedures for special purpose cable assembly W3 (42) are the same as for W1. To replace W3, refer to paragraph 3.6.9.9.

3.6.9.12 Special Purpose Cable Assembly W4 Replacement. Replacement procedures for special purpose cable assembly W4 (43) are the same as. for W1. To replace W4, refer to paragraph 3.6.9.9.

3.6.9.13 Special Purpose Cable Assembly W5 Replacement. To replace special purpose cable assembly W5 (44) in the DF control, proceed as follows:

a. Place chassis bottom-side up, the route W5 along right side of chassis to wire termination locations. Use lacing tape (item 12, App. C) to relate harness as required.

b. Secure harness to chassis (3) using four cable loops (50), screws (46), lockwashers (47), flat washers (48), and nuts (49) mounted to side of chassis.

c. Solder wires to terminating locations as marked during removal.

d. Secure connector J11 (45) to front panel (40) with four screws (36), flat washers (37), and nuts (38).

e. Replace bottom access cover (4) in accordance with paragraph 3.6.9.20.

3.6.9.14 Special Purpose Cable Assembly W6 Replacement. Replacement procedures for special purpose cable assembly W6 (51) are the same as for W5. To replace W6, refer to paragraph 3.6.9.13.

3.6.9.15 Vaneaxial Fan Assembly Replacement. Refer to paragraph 3.6.6.3.3 to replace RF shielding strip. To replace the vaneaxial fan assembly in the DF control, proceed as follows:

a. Connect wires to fan terminal strip as tagged during removal.

b. Mount fan assembly inside chassis and secure with 10 screws (17).

c. Replace top access cover (1) in accordance with paragraph 3.6.9.21.

3.6.9.16 CCA Card Guide Replacement. To replace a CCA card guide on the CCA mounting guide plates, proceed as follows:

a. Mount CCA card guide (6) to CCA mounting guide plate and secure with two screws (22) and lockwashers (23).

b. Replace any CCAs that were removed in accordance with paragraph 3.6.9.19.

c. Replace top access cover in accordance with paragraph 3.6.9.21.

3.6.9.17 CCA Mounting Guide Plate Replacement. To replace the front, center, or rear CCA guide mounting plate (11, 12, or 13) in the DF control, proceed as follows:

a. If front guide plate was replaced, install thermistic switch S1 in accordance with paragraph 3.6.9.18.

b. Install CCA mounting guide plate in correct position inside chassis and secure to sides of chassis with four screws (21, two on each side).

c. Apply type 242 locking compound (item 6, App. C) to two screws (18), then use screws, lockwashers (19), and flat washers (20) to secure guide plate to contact assembly (17).

CAUTION

When performing step d, be extremely careful not to damage contact assembly wiring when inserting screws.

d. Place DF control chassis (3) bottom-side up and secure bottom of guide plate to contact assembly with four screws (14), lockwashers (15), and flat washers (16).

e. Replace top and bottom access covers in accordance with paragraphs 3.6.9.21 and 3.6.9.20.

3.6.9.18 Thermister Switch S1 Replacement. To replace thermister switch S1 (7) in the DF control, proceed as follows:

a. Mount S1 at proper location on front CCA guide mounting plate (11) and secure with two screws (8), lockwashers (9), and flat washers (10).

b. Slip length of 0.125 ID black heatshrink sleeving (item 10, App. C) over each wire that connects to S1. Solder wires to S1 as tagged during removal, then slide heatshrink sleeving over connection and shrink.

co Replace top access cover (1) in accordance with paragraph 3.6.9.21.

CAUTION

Certain CCAs in the DF control contain electrostatic discharge sensitive (ESDS) devices that can be damaged by static electricity. Special handling methods and materials must be used to prevent damage. Do not touch or remove any ESDS device or circuit without properly grounding your body, tools, and test equipment. Handle such CCAs on the edges only, and store such CCAs in conductive (antistatic) bags.

3.6.9.19 CCA Replacement. To replace a CCA in the DF control, determine the appropriate location for installing the CCA (See Table 3-2 for location and orientation.), then insert the CCA into the card guides (6) and push it firmly into the CCA connector on the contact assembly (17). Replace top access cover in accordance with paragraph 3.6.9.21.

3.6.9.20 Bottom Access Cover Replacement. To replace the bottom access cover (4) on the DF control, place the DF control bottom-side up and position the bottom access cover over the opening and secure it to the chassis by tightening the 26 screw fasteners (2).

3.6.9.21 Top Access Cover Replacement. To replace the top access cover (1) on the DF control, place the DF control right-side up and position the top access cover over the opening. Be sure to orient the cover properly, then secure it to the chassis by tightening the 26 screw fasteners (2).

3.6.9.22 Identification Plate Replacement. To replace an identification plate (80) on the front panel (40), apply type 242 locking compound (item 5, App. C) to the attaching screws (81), then mount identification plate to front panel with two screws.

3.6.10 TESTING PROCEDURES.

Testing procedures contained in this manual are limited to those procedures that are performed on a SRU/assembly that is not tested with the AN/USM-410 ATE. To test vaneaxial blowers B1 and B2, thermistic switch S1, or the total time meter, follow the procedures presented in Figures 3-5 and 3-6.

Table 3-2. CCA Locations

REF DES	C-11002/USQ		REF DES	C-11002/USQ	
	PART NO.	NAME		PART NO.	NAME
A1	10-001134-4	Display Multiplexer	A18	C5135413-1	8K Memory
A2	10-001044-3	Arithmetic Logic Unit	A19	10-001094-33	Servo Conversion
A3	10-001044-3	Arithmetic Logic Unit	A20	10-001104-3	Servo Timing
A4	10-001054-3	Program Counter I/O	A21	10-001124-13	Servo Serial Ifc
A5	10-001054-3	Program Counter I/O	A22	Not Used	
A6	10-001064-3	Jump Flag Logic	A23	Not Used	
A7	10-001074-3	Instruction Decoder	A24	C5135423-1	Random Access Memory
A8	10-001084-3	Processor Timing	A25	Not Used	
A9	10-001144-3	ROM Extender	A26	10-123804-3	Serial Interface
A10	C5135419-1	8K Memory Buffer	A27	C5135419-1	8K Memory Buffer
A11	Not Used		A28	Not Used	
A12	Not Used		A29	Not Used	
A13	Not Used		A30	Not Used	
A14	Not Used		A31	Not Used	
A15	Not Used		A32	Not Used	
A16	Not Used		A33	Not Used	
A17	Not Used		A34	Not Used	
			A35	C5135413-1	8K Memory
			A36	Not Used	

NOTE: Reference designators begin with Al at left front through A18 at right front, then A19 at left rear through A36 at right rear. All circuit card components are on the right side when the cards are installed.

3.6.11 ADJUSTMENT PROCEDURES.

Adjustment procedures contained in this manual are limited to those procedures that are performed on a SRU/assembly that is not tested with the AN/USM-410 ATE. All SRUs/assemblies within the DF control- are tested with the AN/USM-410; therefore, no adjustment procedures are presented in this section.

Section VII. PREPARATION FOR STORAGE OR SHIPMENT

3.7.1 PREPARATION FOR STORAGE OR SHIPMENT.

The DF control is shipped in a reusable container. When the received unit is a replacement for a defective DF control, the defective unit may be shipped in the same container. Pack the DF control in accordance with SB-38-100.

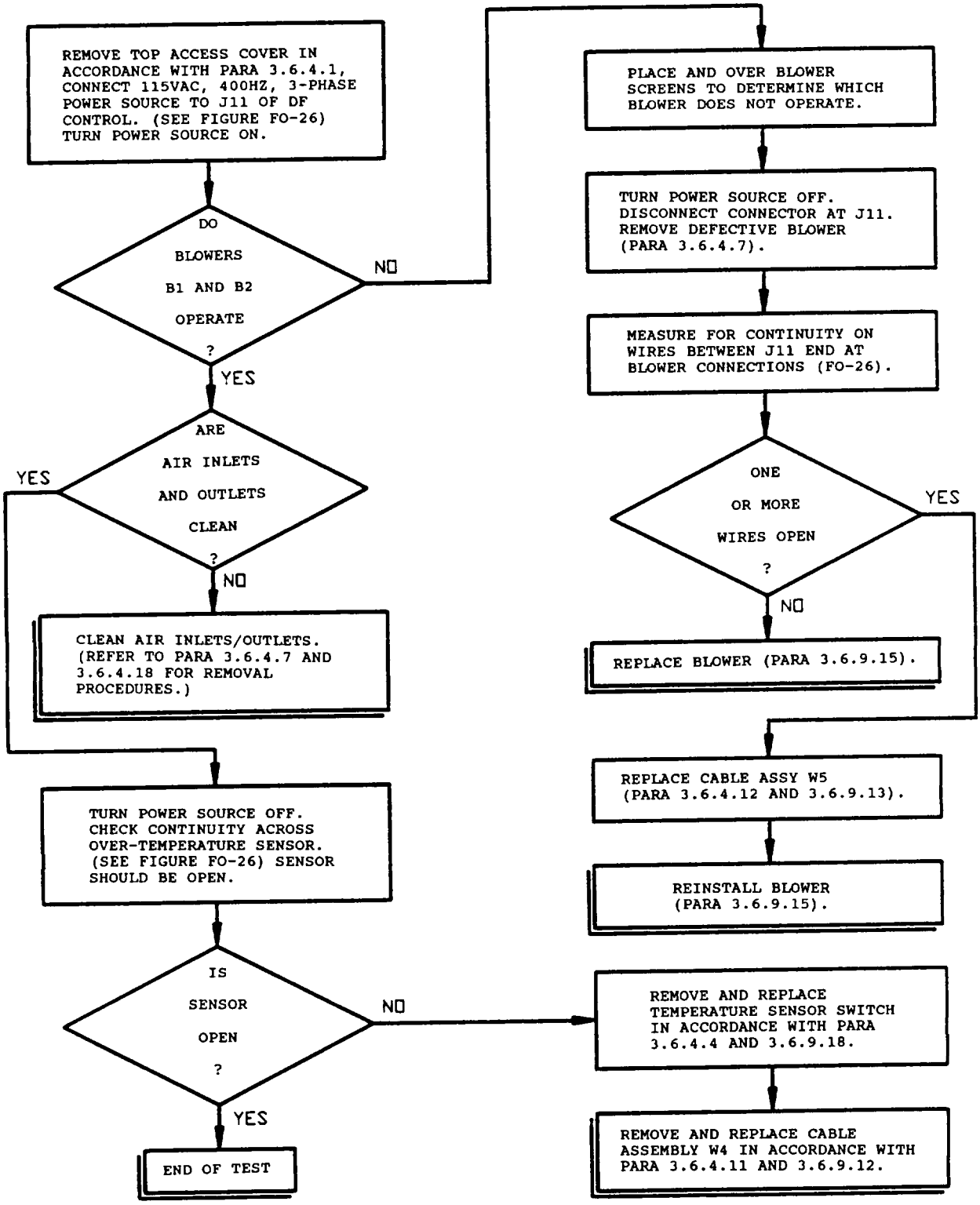


Figure 3-5. Overtemperature Condition Test Logic Diagram

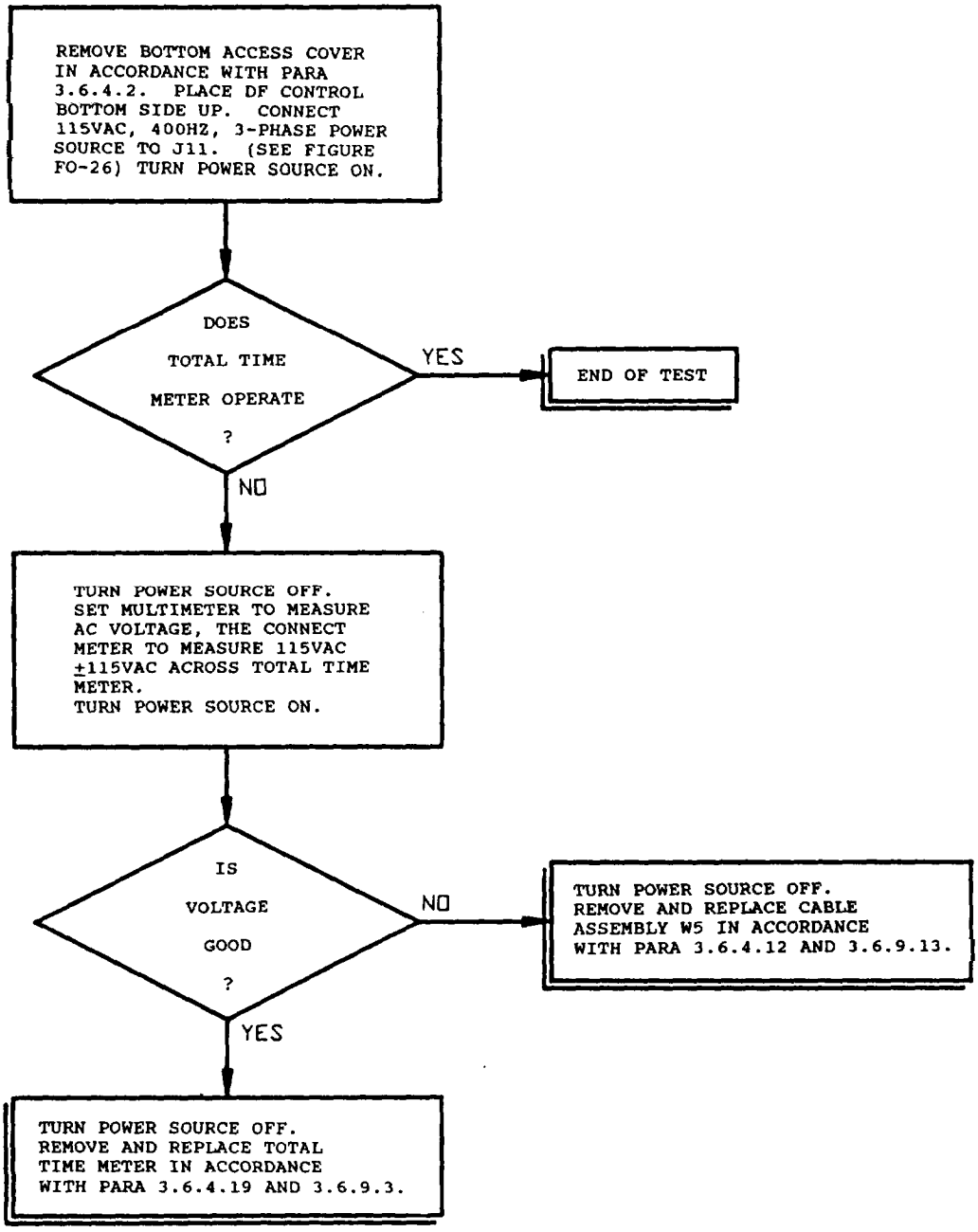


Figure 3-6. Total Time Meter Test Logic Diagram

APPENDIX A

REFERENCES

A-1. Technical Manuals

TM 32-5800-002-34P	Repair Parts and Special Tools List, Direct Support and General Support, Direction Finder Control, C-11002/USQ
TM 750-244-2	Procedures for Destruction of Electronics Material to Prevent Enemy Use (Electronics Command)
TM 750-245-4	Direct Support and General Support Quality Control: Inspector's Inspection Criteria
TM 43-0139	Painting Instructions for Field Use
TM 38-230-2	Preservation Packaging, and Packing of Military Supplies and Equipments
TM 38-260	Preparation and Inspection of Industrial Production Equipment for Storage and Shipment

A-2. Technical Bulletins

TB SIG 222	Solder and Soldering
TB 43-0118	Field Instructions for Painting and Preserving Electronics Command Equipment

A-3. Supply Bulletins

SB 38-100	Preservation, Packaging and Packing Materials, Supplies and Equipment Used By the Army
SB 11-30	Transportation, Storage, Testing, Shelf Life, and Quantity Unit Pack
SB 11-573	Painting and Preservation Supplies Available for Field Use for Electronics Command Equipment
CTA 50-970	Expendable Items
SB 708-41/42	Federal Supply Code for Manufacturers, United States and Canada, Code to Name, Cataloging Handbook H4-2

REFERENCES (CONTINUED)

A-4. Pamphlets

DA Pam 25-30	Consolidated Index of Army Publications and Blank Forms
DA Pam 310-1 (Microfiche only)	Index of Administrative Publications
DA Pam 310-2 (Microfiche only)	Index of Blank Forms
DA Pam 310-3 (Microfiche only)	Index of Doctrinal, Training, and Organizational Publications
DA Pam 310-4 (Microfiche only)	Index of Technical Publications (Includes: Equipment Identification Lists, Lubrication Order, Modification Work Orders, Supply Bulletins, Supply Catalogs, Supply Manuals, Technical Bulletins, Technical Manuals and Technical Publications Rescinded for Active Army Use But Valid For USAR, ARNG, or FMS/IL Programs
DA Pam 738-750	The Army Maintenance Management System (TAMMS)

A-5. Army Regulations

AR 310-25	Dictionary of United States Army Terms
AR 310-50	Authorized Abbreviations and Brevity Codes
AR 700-42	Classification, Reclassification, Maintenance, Insurance, and Reporting of Maintenance Training Aircraft
AR 55-38	Discrepancy in Shipment Report

A-6. Forms

DA Form 3803	Decontamination Tag
DA Form 2028	Recommended Changes to DA Technical Manuals, Parts Lists or Supply Manual 8 or 9
DA Form 2404	Equipment Inspection and Maintenance Work Sheet
DA Form 2408	Equipment Log Book Assembly Instruction for General Equipment

REFERENCES (CONTINUED)

A - 6 Forms (Continued)

DA Form 2408-1	Equipment Daily or Monthly Log
DA Form 2408-5	Equipment Modification Record
DA Form 2408-9	Equipment Control Record
DD Form 5504	Maintenance Request
Standard Form 364	Report of Discrepancy (ROD)
Standard Form 368	Quality Deficiency Report

APPENDIX B

MAINTENANCE ALLOCATION CHART (MAC)

Section I. INTRODUCTION

B-1. GENERAL.

a. This introduction (Section I) provides a general explanation of all maintenance and repair functions authorized at various maintenance levels under the standard Army Maintenance System concept.

b. The Maintenance Allocation Chart (MAC) in Section II designates overall authority and responsibility for the performance of maintenance functions on the Direction Finder Control C-11002-USQ. The application of the maintenance functions to the end item or component will be consistent with the capacities and capabilities of the designated maintenance levels, which are shown in the MAC in Column (4) as:

Unit - includes two subcolumns, C (operator/crew) and 0 (unit) maintenance
Direct Support - includes an F subcolumn.
General Support - includes an H subcolumn.
Depot - includes a D subcolumn.

c. Section III lists the tools and test equipment (both special tools and common tool sets) required for each maintenance function as referenced from Section II.

d. Section IV contains supplemental instructions and explanatory notes for a particular maintenance function.

B-2. MAINTENANCE FUNCTIONS. Maintenance functions are limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical and/or electrical characteristics with established standards through examination (e.g., by sight, sound, or feel).

b. Test. To verify serviceability by measuring the mechanical, pneumatic, hydraulic, or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition; e.g., to clean (includes decontaminate, when required) , to preserve, to drain, to paint or to replenish fuel, lubricants, chemical fluids, or gases.

d. Adjust. To maintain or regulate, within prescribed limits, by bringing into proper position, or by setting the operating characteristics to specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or be adjusted on instruments or test, measuring, and diagnostic equipment used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Remove/Install. To remove and install the same item when required to perform service or other maintenance functions. Install may be the act of emplacing, seating, or fixing into position a spare, repair part, or module (component or assembly) in a manner to allow the proper functioning of an equipment or system.

h. Replace. To remove an unserviceable item and install a serviceable counterpart in its place. "Replace" is authorized by the MAC and assigned maintenance level is shown as the 3rd position code of the SMR code.

i. Repair. The application of maintenance services[1] including fault location/troubleshooting[2], removal/installation, and disassembly/assembly[3] procedures, and maintenance actions[4] to identify troubles and restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item or system.

j. Overhaul. That maintenance effort (service/action) prescribed to restore an item to a completely serviceable/operational condition as required by maintenance standards in appropriate technical publications (i.e., DMWR). Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The

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[1]Services - Inspect, test, service, adjust, align, calibrate, and/or replace.

[2]Fault location/troubleshooting - The process of investigating and detecting the cause of equipment malfunctioning; the act of isolating a fault within a system or unit under test (UUT).

[3]Disassembly/assembly - The step-by-step breakdown (taking apart) of a spare/functional group coded item to the level of its least component, that is, assigned an SMR code for the level of maintenance under consideration (i.e. , identified as maintenance significant) .

[4]Actions - Welding, grinding, riveting, straightening, facing, machining, and/or resurfacing.

rebuild operation includes the act of returning to zero those age measurements (e.g., hours/miles) considered in classifying Army equipments/components.

B-3. EXPLANATION OF COLUMNS IN THE MAC, SECTION II.

a. Column (1), Group Number. Column (1) lists functional group code numbers, the purpose of which is to identify maintenance significant components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column (2), Component/Assembly. Column (2) contains the item names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

Column (3), Maintenance Function. Column (3) lists the functions to be performed on the item listed in Column (2). (For detailed explanation of these functions, see paragraph B-2).

d. Column (4), Maintenance Category. Column (4) specifies each level of maintenance authorized to perform each function listed in Column (3), by indicating work time required (expressed as manhours in whole hours or decimals) in the appropriate subcolumn. This work-time figure represents the active time required to preform that maintenance function at the indicated level of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance levels, appropriate work-time figures will be shown for each level. The work-time figure represents the average time required to restore an item (assembly, subassembly, component, module, end item, or system) to a serviceable condition under typical field operating conditions. This time includes preparation time (including any necessary disassembly/assembly time), troubleshooting/ fault location time, and quality assurance time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the Maintenance Allocation Chart. The symbol designations for the various maintenance levels are as follows:

c.	Operator or crew maintenance.
o.	Unit maintenance.
F.	Direct support maintenance.
L	Specialized Repair Activity (SRA)[5].
H.	General support maintenance.
D....	Depot maintenance.

e. Column (5), Tools and Test Equipment Reference Code. Column (5) specifies, by code, those common tool sets (not individual tools),

[5]This maintenance level is not included in Section II, Column (4) of the Maintenance Allocation Chart. Functions to this level of maintenance are identified by a work-time figure in the "H" column of Section II, Column (4), and an associated reference code is used in the Remarks Column (6). This code is keyed to Section IV, Remarks, and the SRA complete repair application is explained there.

common TMDE, special tools, special TMDE, and special support equipment required to perform the designated function. Codes are keyed to tools and test equipment in Section III.

f. Column (6), Remarks. When applicable, this column contains a letter code, in alphabetical order, which is keyed to the remarks contained in Section IV.

B-4. EXPLANATION OF COLUMNS IN TOOL AND TEST EQUIPMENT REQUIREMENTS, SECTION III.

a. Column (1), Reference Code. The tool and test equipment reference code correlates with a code used in the MAC, Section II, Column (5).

b. Column (2), Maintenance Category. The lowest level of maintenance authorized to use the tool or test equipment.

c. Column (3), Nomenclature. Name or identification of the tool or test equipment.

d. Column (4), National Stock Number. The National Stock Number of the tool or test equipment.

e. Column (5), Tool Number. The manufacturer's part number, model number, or type number.

B-5. EXPLANATION OF COLUMNS IN REMARKS, SECTION IV.

a. Column (1), Remarks Code. The code recorded in Column (6), Section II.

b. Column (2), Remarks. This column lists information pertinent to the maintenance function being performed in the MAC, Section II.

Section II. MAINTENANCE ALLOCATION CHART FOR DIRECTION CONTROL FINDER, C-11002/USQ

(1) Group Number	(2) Component/ Assembly	(3) Maintenance Function	(4) Maintenance Level					(5) Tools and Equipment Ref Code	(6) Remarks Code
			Unit		Direct Support	General Support	Depot		
			C	O	F	H	D		
00	DF CONTROL UNIT	INSPECT				0.1		8	
		TEST				0.5		1,2,5,6,8	A,C
		SERVICE				1.0		8	
		REPAIR				0.5		1,2,4,5,8	
01	CCA,DISPLAY MUX	INSPECT				0.1			
	A1	TEST				0.5		2,5	A
		REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A
02	CCA,ALU	INSPECT				0.1			
	A2	TEST				0.5		2,5	A
03	A3	REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A
04	CCA,PROGRAM	INSPECT				0.1			
	COUNTER A4	TEST				0.5		2,5	A
05	A5	REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A
06	CCA,FLAG JUMP	INSPECT				0.1			
	LOGIC	TEST				0.5		2,5	A
	A6	REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A
07	CCA,INSTR DECODER	INSPECT				0.1			
	A7	TEST				0.5		2,5	A
		REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A
08	CCA,PROCESS	INSPECT				0.1			
	TIMING	TEST				0.5		2,5	A
	A8	REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A
09	CCA,ROM EXTENDER	INSPECT				0.1			
	A9	TEST				0.5		2,5	A
		REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A
10	CCA,8K MEMORY	INSPECT				0.1			
	BUFFER	TEST				0.5		2,5	A
	A10	REPLACE				0.1		5,8	
11	A27	REPAIR				0.5		2,5,8	A
12	CCA,SERVO	INSPECT				0.1			
	CONVERSN	TEST				0.5		2,5	A
	A19	REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A
13	CCA,SERVO TIMING	INSPECT				0.1			A
	A20	TEST				0.5		2,5	
		REPLACE				0.1		5,8	A
		REPAIR				0.5		2,5,8	
14	CCA,SERVO SRL	INSPECT				0.1			
	INTFC	TEST				0.5		2,5	A
	A21	REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A

Section II. MAINTENANCE ALLOCATION CHART FOR DIRECTION CONTROL FINDER, C-11002/USQ (CONTINUED)

(1) Group Number	(2) Component/ Assembly	(3) Maintenance Function	(4) Maintenance Level					(5) Tools and Equipment Ref Code	(6) Remarks Code
			Unit		Direct Support	General Support	Depot		
			C	O	F	H	D		
15	CCA,RANDOM ACS MEM A24	INSPECT				0.1			
		TEST				0.5		2,5	A
		REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A
16	CCA,SERIAL INTFC A26	INSPECT				0.1			
		TEST				0.5		2,5	A
		REPLACE				0.1		5,8	
		REPAIR				0.5		2,5,8	A
17	CONTACT ASSEMBLY, DF A37	REPLACE					X		B
		REPAIR					X		B
18	CABLE ASSEMBLY, I/O W1	INSPECT				0.1			
		TEST				0.7		1	
		REPLACE				0.3		4,8	
		REPAIR				0.8		4,8	
19	CABLE ASSEMBLY, FLAG W2	INSPECT				0.1			
		TEST				0.7		1	
		REPLACE				0.3		4,8	
		REPAIR				0.8		4,8	
20	CABLE ASSEMBLY, ROM W3	INSPECT				0.1			
		TEST				0.7		1	
		REPLACE				0.3		4,8	
		REPAIR				0.8		4,8	
21	CABLE ASSEMBLY, DSPL W4	INSPECT				0.1			
		TEST				0.7		1	
		REPLACE				0.3		4,8	
		REPAIR				0.8		4,8	
22	CABLE ASSEMBLY, AC W5	INSPECT				0.1			
		TEST				0.7		1	
		REPLACE				0.3		4,8	
		REPAIR				0.8		4,8	
23	CABLE ASSEMBLY,DC W6	INSPECT				0.1			
		TEST				0.7		1	
		REPLACE				0.3		4,8	
		REPAIR				0.8		4,8	
24	CABLE ASSEMBLY,RF W7	INSPECT				0.1			
		TEST				0.2		1	
		REPLACE				0.2		4,8	
		REPAIR				0.2		4,8	
25	CABLE ASSEMBLY,RF W8	INSPECT				0.1			
		TEST				0.2		1	
		REPLACE				0.2		4,8	
		REPAIR				0.2		4,8	
26	CABLE ASSEMBLY,RF W9	INSPECT				0.1			
		TEST				0.2		1	
		REPLACE				0.2		4,8	
		REPAIR				0.2		4,8	

Section II. MAINTENANCE ALLOCATION CHART FOR DIRECTION CONTROL FINDER, C-11002/USQ (CONTINUED)

(1)	(2)	(3)	(4) Maintenance Level					(5)	(6)
			Unit		Direct Support	General Support	Depot	Tools and Equipment Ref Code	Remarks Code
Group Number	Component/ Assembly	Maintenance Function	C	O	F	H	D		
27	CABLE,ASSEMBLY RF W10	INSPECT				0.1			
		TEST				0.2		1	
		REPLACE				0.2		4,8	
		REPAIR				0.2		4,8	
28	COVER,ACCESS,TOP	INSPECT				0.1		8	
		REPLACE				0.1		8	
		REPAIR				0.4		3,7,8	
29	COVER,ACCESS, BOTTOM	INSPECT				0.1		8	
		REPLACE				0.1		8	
		REPAIR				0.3		3,7,8	
30	PLATE,MOUNTING CARD	INSPECT				0.1		8	
		REPLACE				0.2		8	
		REPAIR				0.2		8,9	
31	PLATE,MOUNTING, CARD	INSPECT						8	
		REPLACE						8	
		REPAIR						8,9	
32	CHASSIS, ELECTRICAL	REPLACE					X		B
		REPAIR					X		B
33	CCA,8K MEMORY A18	INSPECT				0.1		5	C
		TEST				0.5		5,8	
34	A35	REPLACE				0.1		5,8	
		REPAIR				0.5			

Section III. TOOL AND TEST EQUIPMENT REQUIREMENTS FOR DIRECTION FINDER CONTROL, C-11002/USQ

TOOL OR TEST EQUIPMENT REF CODE	MAINTENANCE LEVEL	NOMENCLATURE	NATIONAL STOCK NUMBER	TOOL NUMBER
1	H	MULTIMETER, DIGITAL	6625-01-139-2512	AN/PSM-45
2	H	TEST KIT	6625-01-069-4223	AN/USM-410(V)2
3	H	RIVETER KIT	6665-01-022-4165	HP-200
4	H	MAINTENANCE KIT, ELECTRONIC	6625-01-068-1665	MK-1961/G
5	H	MAINTENANCE KIT, ELECTRONIC	6625-01-068-1666	MK-1962/G
6	H	PROGRAMMER SIMULATOR	- - -	MX-9854/U
7	H	TOOL KIT, ELECTRONIC EQUIPMENT	5180-00-605-0079	TK-100/G
8	H	TOOL KIT, ELECTRONIC EQUIPMENT	5180-00-610-8177	TK-105/G
9	H	TOOL, INSTALLATION, CLINCH NUT	- - -	DBVB6503-4-D

Section IV. REMARKS FOR DIRECTION FINDER CONTROL, C-11002/USQ

REFERENCE CODES	REMARKS
A	These SRUs are tested and repaired using the AN/USM-410(V)2 Automatic Test Equipment.
B	Refer to DMWR 32-5811-TBD for depot-level removal, replacement, and repair instructions.
C	**CAUTION** Programmable read-only memory CCA, C-5135413-1, requires an adapter assembly, C-5144684-1, to reprogram PROM. Programming the CCA with simulator adapter MX-9854/U will result in damage to the CCA and the programmer.

APPENDIX C

EXPENDABLE AND DURABLE ITEMS LIST

Section I. INTRODUCTION

C-1. SCOPE.

This appendix lists expendable and durable items you will need to maintain the Direction Finder Control C-11002/USQ. These items are authorized by CTA 50-970, Expendable Items (except Medical, Class V, Repair Parts, and Heraldic Items).

C-2. EXPLANATION OF COLUMNS.

a. Column 1 - Item Number. This number is assigned to the entry in the listing for referencing when required.

b. Column 2 - Level. This column identifies the lowest level of maintenance that requires the listed item.

C. . . . . Operator/Crew
O . . . . . Unit Maintenance
F . . . . . Direct Support Maintenance
H. . . . . General Support Maintenance
D . . . . . Depot Maintenance

c. Column 3 - National Stock Number (NSN). This is the national stock number assigned to the item; use it to request or requisition the item.

d. Column 4 - Description. Indicates the Federal item and, if required, a description to identify the item. The last line for each item indicates the part number followed by the Commercial and Government Entity Code (CAGEC) in parentheses, if applicable.

e. Column 5 - Unit of Measure (U/M)/Unit of Issue (U/I). This measure is expressed by a two-character alphabetical abbreviation (e.g., EA, IN, PR). If the unit of measure differs from the unit of issue as shown in the Army Master Data File (AMDF), requisition the lowest unit that will satisfy your requirements.

Section II. EXPENDABLE AND DURABLE ITEMS LIST

(1) Item Number	(2) Level	(3) National Stock Number	(4) Description	(5) (U/M)/ (U/I)
1	H	8040-01-063-7509	Adhesive	GL
2	H	8040-00-826-3535	Adhesive, type 910 (19139)	PT
3	H	8020-00-257-0382	Brush, soft	EA
4	H	8305-00-222-2423	Cloth	RO
5	H	8040-01-250-3969	Compound, locking, type 242 (05972)	EA
6	H	8010-00-087-0103	Enamel, color 24410	QT
7	H	8415-00-266-8673	Gloves, rubber, heavy duty	PR
8	H	5350-00-186-8854	Sandpaper, no. 000	SHT
9	H	9320-01-084-3660	Silicone sponge, 1/8-inch thk	SHT
10	H	5970-00-812-2969	Sleeving, heat shrink	IN
11	H	3439-01-008-7580	Solder	RO
12	H	8135-00-798-9706	Tape, lacing	RO
13	H	6850-00-105-3084	Trichlorotrifluoroethane	GL

APPENDIX D

FRONT PANEL CONNECTOR PIN FUNCTIONS

Connector J1: **Connector J1 (cont'd):**

Pin	Function/Remarks	Pin	Function/Remarks
1	$\overline{\text{RIN0}}$	25	$\overline{\text{RIN12}}$
2	$\overline{\text{RIN0}}$ RTN	26	$\overline{\text{RIN12}}$ RTN
3	$\overline{\text{RIN1}}$	27	$\overline{\text{RIN13}}$
4	$\overline{\text{RIN1}}$ RTN	28	$\overline{\text{RIN13}}$ RTN
5	$\overline{\text{RIN2}}$	29	$\overline{\text{RIN14}}$
6	$\overline{\text{RIN2}}$ RTN	30	$\overline{\text{RIN14}}$ RTN
7	$\overline{\text{RIN3}}$	31	$\overline{\text{RIN15}}$
14	$\overline{\text{RIN3}}$ RTN	32	$\overline{\text{RIN15}}$ RTN
8	$\overline{\text{RIN4}}$	33	$\overline{\text{RIN16}}$
9	$\overline{\text{RIN4}}$ RTN	34	$\overline{\text{RIN16}}$ RTN
10	$\overline{\text{RIN5}}$	35	$\overline{\text{RIN17}}$
11	$\overline{\text{RIN5}}$ RTN	36	$\overline{\text{RIN17}}$ RTN
12	$\overline{\text{RIN6}}$	37	$\overline{\text{RIN18}}$
13	$\overline{\text{RIN6}}$ RTN	38	$\overline{\text{RIN18}}$ RTN
16	$\overline{\text{RIN7}}$	39	$\overline{\text{RIN19}}$
17	$\overline{\text{RIN7}}$ RTN	40	$\overline{\text{RIN19}}$ RTN
18	$\overline{\text{RIN8}}$	41	$\overline{\text{RIN20}}$
19	$\overline{\text{RIN8}}$ RTN	42	$\overline{\text{RIN20}}$ RTN
20	$\overline{\text{RIN9}}$	43	$\overline{\text{RIN21}}$
21	$\overline{\text{RIN9}}$ RTN	44	$\overline{\text{RIN21}}$ RTN
22	$\overline{\text{RIN10}}$	46	$\overline{\text{RIN22}}$
23	$\overline{\text{RIN10}}$ RTN	47	$\overline{\text{RIN22}}$ RTN
24	$\overline{\text{RIN11}}$	48	$\overline{\text{RIN23}}$
15	$\overline{\text{RIN11}}$ RTN	49	$\overline{\text{RIN23}}$ RTN

FRONT PANEL CONNECTOR PIN FUNCTIONS (CONTINUED)

Connector J1:

Pin	Function/Remarks
56	$\overline{\text{XAD0}}$
57	$\overline{\text{XAD0}}$ RTN
58	$\overline{\text{XAD1}}$
59	$\overline{\text{XAD1}}$ RTN
60	$\overline{\text{XAD2}}$
61	$\overline{\text{XAD2}}$ RTN
62	$\overline{\text{XAD3}}$
63	$\overline{\text{XAD3}}$ RTN
64	$\overline{\text{XAD4}}$
65	$\overline{\text{XAD4}}$ RTN
67	$\overline{\text{XAD5}}$
68	$\overline{\text{XAD5}}$ RTN
69	$\overline{\text{XAD6}}$
70	$\overline{\text{XAD6}}$ RTN
71	$\overline{\text{XAD7}}$
72	$\overline{\text{XAD7}}$ RTN
73	$\overline{\text{XAD8}}$
74	$\overline{\text{XAD8}}$ RTN
75	$\overline{\text{XAD9}}$
76	$\overline{\text{XAD9}}$ RTN
77	$\overline{\text{XAD10}}$
78	$\overline{\text{XAD10}}$ RTN
79	$\overline{\text{XAD11}}$
80	$\overline{\text{XAD11}}$ RTN

Connector J1 (cont'd):

Pin	Function/Remarks
81	$\overline{\text{XAD12}}$
82	$\overline{\text{XAD12}}$ RTN
83	$\overline{\text{XAD13}}$
84	$\overline{\text{XAD13}}$ RTN
86	$\overline{\text{XAD14}}$
87	$\overline{\text{XAD14}}$ RTN
88	$\overline{\text{XAD15}}$
89	$\overline{\text{XAD15}}$ RTN
90	DF ENABLE
91	DF ENABLE RTN
100	SHIELD, GND FLYING LEAD

Connector J2:

1	GND
2	GND
3	DT MOD OUT
4	DT MOD OUT RTN
5	DT CLK OUT
6	DT CLK OUT RTN
7	DT DATA
8	DT DATA OUT RTN
9	DT STROBE OUT
10	DT STROBE OUT RTN
11	SPARE
12	SPARE

FRONT PANEL CONNECTOR PIN FUNCTIONS (CONTINUED)

Connector J2 (cont'd):

Pin	Function/Remarks
13	SPARE
14	SPARE
15	SPARE
16	SPARE
17	SPARE
18	SPARE
19	SPARE
20	SPARE
21	SPARE
22	SHLD GND

Connector J3:

Pin	Function/Remarks
1	FLG0
2	FLG0 RTN
3	FLG1
4	FLG1 RTN
5	FLG2
6	FLG2 RTN
7	FLG3
8	FLG3 RTN
9	FLG4
10	FLG4 RTN
11	FLG5
19	FLG5 RTN
13	FLG6
14	FLG6 RTN

Connector J3 (cont'd):

Pin	Function/Remarks
15	FLG7
16	FLG7 RTN
17	FLG8
18	FLG8 RTN
12	FLG9
20	FLG9 RTN
21	FLG10
22	FLG10 RTN
23	FLG11
24	FLG11 RTN
25	FLG12
26	FLG12 RTN
27	FLG13
28	FLG13 RTN
29	FLG14
30	FLG14 RTN
31	FLG15
32	FLG15 RTN
33	CFLG0
34	CFLG0 RTN
35	CFLG1
36	CFLG1 RTN
37	CFLG2
38	CFLG2 RTN
39	CFLG3

FRONT PANEL CONNECTOR PIN FUNCTIONS (CONTINUED)

Connector J3 (cont'd):		Connector J3 (cont'd):	
Pin	**Function/Remarks**	**Pin**	**Function/Remarks**
40	CFLG3 RTN	64	CFLG15 RTN
41	CFLG4	65	$\overline{\text{INT1}}$
42	CFLG4 RTN	66	$\overline{\text{INT1}}$ RTN
43	CFLG5	67	$\overline{\text{INT2}}$
44	CFLG5 RTN	68	$\overline{\text{INT2}}$ RTN
45	CFLG6	69	$\overline{\text{INT3}}$
46	CFLG6 RTN	70	$\overline{\text{INT3}}$ RTN
47	CFLG7	71	$\overline{\text{INT4}}$
57	CFLG7 RTN	72	$\overline{\text{INT4}}$ RTN
49	CFLG8	73	$\overline{\text{INT5}}$
50	CFLG8 RTN	74	$\overline{\text{INT5}}$ RTN
51	CFLG9	75	$\overline{\text{INT6}}$
52	CFLG9 RTN	76	$\overline{\text{INT6}}$ RTN
53	CFLG10	77	$\overline{\text{INT0}}$
54	CFLG10 RTN	78	$\overline{\text{INT0}}$ RTN
55	CFLG11	79	+5VDC
56	CFLG11 RTN	80	+5VDC
48	CFLG12	81	+5VDC
58	CFLG12 RTN	82	+5VDC
59	CFLG13	83	INHIBIT
60	CFLG13 RTN	84	INHIBIT
61	CFLG14	85	SHIELD
62	CFLG14 RTN	86	SPARE
63	CFLG15	87	SPARE

FRONT PANEL CONNECTOR PIN FUNCTIONS (CONTINUED)

Connector J3 (cont'd):

Pin	Function/Remarks
88	SPARE
89	SPARE
90	SPARE
91	SPARE
92	SPARE
93	SPARE
94	SPARE
95	SPARE
96	SPARE
97	SPARE
98	SPARE
99	SPARE
100	SPARE

Connector J4:

Pin	Function/Remarks
1	$\overline{\text{DM0}}$
2	$\overline{\text{DM0}}$ RTN
3	$\overline{\text{DM1}}$
4	$\overline{\text{DM1}}$ RTN
5	$\overline{\text{DM2}}$
6	$\overline{\text{DM2}}$ RTN
7	$\overline{\text{DM3}}$
8	$\overline{\text{DM3}}$ RTN
9	$\overline{\text{DM4}}$
10	$\overline{\text{DM4}}$ RTN
11	$\overline{\text{DM5}}$

Connector J4 (cont'd):

Pin	Function/Remarks
12	$\overline{\text{DM5}}$ RTN
13	$\overline{\text{DM6}}$
14	$\overline{\text{DM6}}$ RTN
15	$\overline{\text{DM7}}$
16	$\overline{\text{DM7}}$ RTN
17	$\overline{\text{MUX0}}$
18	$\overline{\text{MUX0}}$ RTN
19	$\overline{\text{MUX1}}$
20	$\overline{\text{MUX1}}$ RTN
21	$\overline{\text{MUX2}}$
22	$\overline{\text{MUX2}}$ RTN
23	RUNS
24	RUNS RTN
25	$\overline{\text{RUNS}}$
54	$\overline{\text{RUNS}}$ RTN
26	SGLST
27	SGLST RTN
28	$\overline{\text{SGLST}}$
55	$\overline{\text{SGLST}}$
29	HALT
30	HALT RTN
31	$\overline{\text{BRKPT}}$
32	$\overline{\text{BRKPT}}$ RTN
33	PRES

FRONT PANEL CONNECTOR PIN FUNCTIONS (CONTINUED)

Connector J4 (cont'd):

Pin	Function/Remarks
34	PRES RTN
35	$\overline{\text{PRES}}$
56	$\overline{\text{PRES}}$ RTN
36	$\overline{\text{COM1}}$
37	$\overline{\text{LASW0}}$
38	$\overline{\text{LASW1}}$
39	$\overline{\text{LASW2}}$
40	$\overline{\text{ASW3}}$
41	$\overline{\text{ASW4}}$
42	$\overline{\text{ASW5}}$
43	$\overline{\text{ASW6}}$
44	$\overline{\text{ASW7}}$
45	$\overline{\text{ASW8}}$
46	$\overline{\text{COM2}}$
47	$\overline{\text{ASW9}}$
48	$\overline{\text{ASW10}}$
49	$\overline{\text{ASW11}}$
50	$\overline{\text{ASW12}}$
51	$\overline{\text{ASW13}}$
52	$\overline{\text{ASW14}}$
53	$\overline{\text{ASW15}}$
65	SHIELD FLYING LEAD

Connector J5:

Pin	Function/Remarks
1	OVERTEMP
2	OVERTEMP RTN

Connector J5 (cont'd):

Pin	Function/Remarks
3	SPARE
4	SPARE
5	SPARE
6	SPARE
7	SPARE
8	SI CLK IN
9	SI CLK OUT
10	DATA
11	DATA RTN
12	CLK
13	CLK RTN
14	READY PROCEED
15	READY PROCEED RTN
16	PROCEED READY
17	PROCEED READY RTN
18	IMR MODE
19	IMR MODE RTN
20	MODE IMR
21	MODE IMR RTN
22	SHLD GND

Connector J6:

Pin	Function/Remarks
1	$\overline{\text{IO0}}$
2	$\overline{\text{IO0}}$ RTN
3	$\overline{\text{IO1}}$
4	IO1 RTN

FRONT PANEL CONNECTOR PIN FUNCTIONS (CONTINUED)

Connector J6 (cont'd):		Connector J6 (cont'd):	
Pin	**Function/Remarks**	**Pin**	**Function/Remarks**
5	$\overline{IO2}$	29	$\overline{IO14}$
6	$\overline{IO2}$ RTN	30	$\overline{IO14}$ RTN
7	$\overline{IO3}$	31	$\overline{IO15}$
8	$\overline{IO3}$ RTN	32	$\overline{IO15}$ RTN
9	$\overline{IO4}$	33	$\overline{IOA0}$
10	$\overline{IO4}$ RTN	34	$\overline{IOA0}$
11	$\overline{IO5}$	35	$\overline{IOA1}$
12	$\overline{IO5}$ RTN	36	$\overline{IOA1}$ RTN
13	$\overline{IO6}$	37	$\overline{IOA2}$
14	$\overline{IO6}$ RTN	38	$\overline{IOA2}$ RTN
15	$\overline{IO7}$	39	$\overline{IOA3}$
16	$\overline{IO7}$ RTN	40	$\overline{IOA3}$ RTN
17	$\overline{IO8}$	41	$\overline{IOA4}$
18	$\overline{IO8}$ RTN	42	$\overline{IOA4}$ RTN
19	$\overline{IO9}$	43	$\overline{IOA5}$
20	$\overline{IO9}$ RTN	44	$\overline{IOA5}$ RTN
21	$\overline{IO10}$	45	$\overline{IOA6}$
22	$\overline{IO10}$ RTN	46	$\overline{IOA6}$ RTN
23	$\overline{IO11}$	47	$\overline{IOA7}$
24	$\overline{IO11}$ RTN	48	$\overline{IOA7}$ RTN
25	$\overline{IO12}$	49	$\overline{IOS}$
26	$\overline{IO12}$ RTN	50	$\overline{IOS}$ RTN
27	$\overline{IO13}$	51	$\overline{IOM}$
28	$\overline{IO13}$ RTN	52	$\overline{IOM}$ RTN

FRONT PANEL CONNECTOR PIN FUNCTIONS (CONTINUED)

Connector J6 (cont'd):

Pin	Function/Remarks
53	$\overline{PR}$
54	$\overline{PR}$ RTN
55	+5VDC
56	+5VDC
57	+5VDC
58	+5VDC
59	AGC OUT
60	ABC OUT RTN
61	SHIELD
63	$\overline{PCCNL}$
64	$\overline{PCCNL}$ RTN
65	SHIELD

Connector J7:

	ANALOG 0

Connector J8:

	INT MON

Connector J9:

	BLANKING

Connector J10:

	ANALOG 1

Connector J11:

Pin	Function/Remarks
A	115VAC 01
B	115VAC 02
C	115VAC 03
D	NEUT
E	INTERLOCK

Connector J11 (cont'd):

Pin	Function/Remarks
F	INTERLOCK
G	SPACE
H	CHASSIS GND

Connector J12:

Pin	Function/Remarks
A	+15VDC
B	-15VDC
C	±15VDC RTN
D	SPARE
E	SPARE
F	+5VDC
H	+5VDC RTN
J	-5VDC RTN
K	+5VDC SENSE
L	+5VDC
M	+5VDC
N	+5VDC RTN
P	+5VDC RTN
R	+5VDC SENSE
S	-10VDC
T	-10VDC RTN
U	SPARE
V	+5VDC
W	+5VDC RTN
X	SHLD GND

APPENDIX E

WIRING LISTS

5-1. SCOPE.

This chapter contains the wire lists for the DF control. The lists are used to determine point-to-point wiring. Each point's origin (from) and destination (to) are listed. When a point listed in the FROM column is routed to more than one point, the FROM point is listed only once and the rest are left blank with only the TO point listed. Points that are not connected are not listed. Pin-for-pin cables are not listed. (Pin-for-pin cables are cables that have identical plugs at both ends and each pin connected has the same pin number at both ends.) All other connections are listed. Wiring interconnections shown in Figure F0-27 have not been repeated in this chapter. Wire lists and wiring diagrams take precedence over schematics due to unused circuit cards connector pins.

The following lists are provided:

Contact Assembly A37 Wire List

FROM CONNECTOR		TO CONNECTOR		WIRE			
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	FUNCTION/REMARKS
XA19	82	XA20	56				A/D CLOCK
XA19	63	XA20	83				A/D DISABLE
XA2	76	XA3	76				A=B
XA3	76	XA6	17				A=B
XA4	40	XA5	28				AD EQM
XA5	40	XA8	62				AD EQO
J4	P9	XA19	13				AGC GAIN
XA21	61	XA19	43				AI 0
XA21	62	XA19	45				AI 1
XA3	58	XA2	58				ALUG*
XA2	58	XA7	86				ALUG*
XA7	10	XA2	62				ALU 0
XA3	38	XA8	88				ALU 12*
XA8	87	XA3	37				ALU 13*
XA3	40	XA8	85				ALU 14*
XA8	85	XA7	46				ALU 14*
XA7	45	XA8	86				ALU 15*
XA6	86	XA3	52				ALU 15*
XA2	38	XA3	45				ALU 4*
XA2	37	XA3	44				ALU 5*
XA3	43	XA2	41				ALU 6*
XA2	41	XA2	40				ALU 6*
XA2	52	XA3	46				ALU 7*
XA3	46	XA3	47				ALU 7*
XA2	70	XA3	62				ALU 8*
XA8	20	XA4	32				ASW 0*
XA4	34	XA8	22				ASW 1*
XA5	33	J2	K3				ASW 10*
J2	K4	XA5	26				ASW 11*
XA5	46	J2	K5				ASW 12*
J2	K6	XA5	43				ASW 13*
XA5	48	J5	K7				ASW 14*
J2	K8	XA5	39				ASW 15*
XA4	33	XA8	16				ASW 2*
XA4	26	J2	E5				ASW 3*
J2	E6	XA4	46				ASW 4*
XA4	43	J2	E7				ASW 5*
J2	E8	XA4	48				ASW 6*
XA4	39	J2	E9				ASW 7*
J2	E0	XA5	32				ASW 8*
XA5	34	J2	K2				ASW 9*
XA7	88	XA2	64				AS 0
X2	64	XA3	64				AS 0
XA3	63	XA2	63				AS 1
XA2	63	XA7	68				AS 1
XA7	67	XA3	65				AS 2

*Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA3	65	XA2	65				AS 2
XA2	66	XA3	66				AS 3
XA3	66	XA7	85				AS 3
XA10	27	XA9	86				DF INHIBIT
XA8	84	J2	C7				BRK PT*
XA1	63	XA6	28				CARRY*
XA6	28	XA7	20				CARRY*
XA6	30	J5	C7				CF LG 0
J5	C8	XA6	40				CF LG 1
XA6	76	J5	K1				CF LG 10
J5	K2	XA6	88				CF LG 11
XA6	78	J5	K3				CF LG 12
J5	K4	XA6	86				CF LG 13
XA6	53	J5	K5				CF LG 14
J5	K6	XA6	87				CF LG 15
XA6	6	J5	C9				CF LG 2
J5	C9	XA20	74				CF LG 2
J5	C0	XA6	16				CF LG 3
XA6	8	J5	E1				CF LG 4
J5	E2	XA6	18				CF LG 5
XA6	52	J5	E3				CF LG 6
J5	E8	XA6	42				CF LG 7
XA6	65	J5	E9				CF LG 8
J5	E0	XA6	74				CF LG 9
XA27	69	XA34	77				CIN 0A
XA34	77	XA33	77				CIN 0A
XA33	77	XA35	77				CIN 0A
XA35	77	XA36	77				CIN 0A
XA29	77	XA28	77				CIN 0B
XA28	77	XA32	77				CIN 0B
XA32	77	XA30	77				CIN 0B
XA30	77	XA27	56				CIN 0B
XA27	71	XA34	73				CIN 1A
XA34	73	XA33	73				CIN 1A
XA33	73	XA35	73				CIN 1A
XA35	73	XA36	73				CIN 1A
XA28	73	XA29	73				CIN 1B
XA29	73	XA32	73				CIN 1B
XA32	73	XA30	73				CIN 1B
XA30	73	XA27	55				CIN 1B
XA27	81	XA34	42				CIN 10A
XA34	42	XA33	42				CIN 10A
XA33	42	XA35	42				CIN 10A
XA35	42	XA36	42				CIN 10A
XA29	42	XA30	42				CIN 10B
XA30	42	XA28	42				CIN 10B

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA28	42	XA32	42				CIN 10B
XA32	42	XA27	82				CIN 10B
XA27	80	XA33	41				CIN 11A
XA33	41	XA34	41				CIN 11A
XA34	41	XA35	41				CIN 11A
XA35	41	XA36	41				CIN 11A
XA32	41	XA30	41				CIN 11B
XA30	41	XA28	41				CIN 11B
XA28	41	XA29	41				CIN 11B
XA29	41	XA27	79				CIN 11B
XA27	45	XA33	40				CIN 12A
XA33	40	XA34	40				CIN 12A
XA34	40	XA36	40				CIN 12A
XA27	69	XA34	77				CIN 0A
XA34	77	XA33	77				CIN 0A
XA33	77	XA35	77				CIN 0A
XA35	77	XA36	77				CIN 0A
XA29	77	XA28	77				CIN 0B
XA28	77	XA32	77				CIN 0B
XA32	77	XA30	77				CIN 0B
XA30	77	XA27	56				CIN 0B
XA27	71	XA34	73				CIN 1A
XA34	73	XA33	73				CIN 1A
XA33	73	XA35	73				CIN 1A
XA35	73	XA36	73				CIN 1A
XA28	73	XA29	73				CIN 1B
XA29	73	XA32	73				CIN 1B
XA32	73	XA30	73				CIN 1B
XA30	73	XA27	55				CIN 1B
XA27	81	XA34	42				CIN 10A
XA34	42	XA33	42				CIN 10A
XA33	42	XA35	42				CIN 10A
XA35	42	XA36	42				CIN 10A
XA29	42	XA30	42				CIN 10B
XA30	42	XA28	42				CIN 10B
XA28	42	XA32	42				CIN 10B
XA32	42	XA27	82				CIN 10B
XA27	80	XA33	41				CIN 11A
XA33	41	XA34	41				CIN 11A
XA34	41	XA35	41				CIN 11A
XA35	41	XA36	41				CIN 11A
XA32	41	XA30	41				CIN 11B
XA30	41	XA28	41				CIN 11B
XA28	41	XA29	41				CIN 11B
XA29	41	XA27	41				CIN 11B
XA27	45	XA33	40				CIN 12A

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA33	40	XA34	40				CIN 12A
XA34	40	XA36	40				CIN 12A
XA36	40	XA35	40				CIN 12A
XA29	40	XA30	40				CIN 12B
XA30	40	XA28	40				CIN 12B
XA28	40	XA32	40				CIN 12B
XA32	40	XA27	31				CIN 12B
XA27	47	XA33	39				CIN 13A
XA33	39	XA34	39				CIN 13A
XA34	39	XA36	39				CIN 13A
XA36	39	XA35	39				CIN 13A
XA30	39	XA29	39				CIN 13B
XA29	39	XA28	39				CIN 13B
XA28	39	XA32	39				CIN 13B
XA32	39	XA27	33				CIN 13B
XA27	46	XA33	38				CIN 14A
XA33	38	XA38	38				CIN 14A
XA34	38	XA35	38				CIN 14A
XA35	38	XA36	38				CIN 14A
XA29	38	XA32	38				CIN 14B
XA32	38	XA28	38				CIN 14B
XA28	38	XA30	38				CIN 14B
XA30	38	XA27	34				CIN 14B
XA27	37	XA34	34				CIN 15A
XA34	34	XA33	34				CIN 15A
XA33	34	XA36	34				CIN 15A
XA36	34	XA35	34				CIN 15A
XA29	34	XA32	34				CIN 15B
XA32	34	XA28	34				CIN 15B
XA28	34	XA30	34				CIN 15B
XA30	34	XA27	25				CIN 15B
XA27	72	XA33	75				CIN 2A
XA33	75	XA35	75				CIN 2A
XA35	75	XA34	75				CIN 2A
XA34	75	XA36	75				CIN 2A
XA28	75	XA32	75				CIN 2B
XA32	75	XA30	75				CIN 2B
XA30	75	XA29	75				CIN 2B
XA29	75	XA27	58				CIN 2B
XA27	63	XA34	76				CIN 3A
XA34	76	XA35	76				CIN 3A
XA35	76	XA33	76				CIN 3A
XA33	76	XA36	76				CIN 3A
XA28	76	XA30	76				CIN 3B
XA30	76	XA29	76				CIN 3B
XA29	76	XA32	76				CIN 3B

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA32	76	XA27	52				CIN 3B
XA27	61	XA33	15				CIN 4A
XA33	15	XA34	15				CIN 4A
XA34	15	XA35	15				CIN 4A
XA35	15	XA36	15				CIN 4A
XA30	15	XA29	15				CIN 4B
XA29	15	XA32	15				CIN 4B
XA32	15	XA28	15				CIN 4B
XA28	15	XA27	54				CIN 4B
XA27	62	XA34	74				CIN 5A
XA34	74	XA33	74				CIN 5A
XA33	74	XA35	74				CIN 5A
XA35	74	XA36	74				CIN 5A
XA27	53	XA28	74				CIN 5B
XA28	74	XA30	74				CIN 5B
XA30	74	XA29	74				CIN 5B
XA29	74	XA32	74				CIN 5B
XA27	76	XA36	72				CIN 5A
XA36	72	XA33	72				CIN 6A
XA33	72	XA35	72				CIN 6A
XA35	72	XA34	72				CIN 6A
XA27	72	XA29	72				CIN 6B
XA29	72	XA32	72				CIN 6B
XA32	72	XA30	72				CIN 6B
XA30	72	XA28	72				CIN 6B
XA27	73	XA34	57				CIN 7A
XA34	57	XA33	57				CIN 7A
XA33	57	XA36	57				CIN 7A
XA36	57	XA35	57				CIN 7A
XA27	78	XA28	57				CIN 7B
XA28	57	XA29	57				CIN 7B
XA29	57	XA32	57				CIN 7B
XA32	57	XA30	57				CIN 7B
XA27	74	XA33	44				CIN 8A
XA33	44	XA34	44				CIN 8A
XA34	44	XA36	44				CIN 8A
XA36	44	XA35	44				CIN 8A
XA27	75	XA32	44				CIN 8B
XA32	44	XA28	44				CIN 8B
XA28	44	XA29	44				CIN 8B
XA29	44	XA30	44				CIN 8B
XA27	59	XA36	43				CIN 9A
XA36	43	XA35	43				CIN 9A
XA35	43	XA34	43				CIN 9A
XA34	43	XA33	43				CIN 9A
XA27	60	XA29	43				CIN 9B

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA29	43	XA28	43				CIN 9B
XA28	43	XA30	43				CIN 9B
XA30	43	XA32	43				CIN 9B
XA6	34	XA7	83				CIN *
XA7	83	XA2	61				CIN *
XA3	50	XA7	28				CIN 15*
XA7	28	XA6	26				CIN 15*
XA6	26	XA6	25				CIN 15*
XA3	61	XA2	50				CIN 7*
J2	E1	XA8	83				COM 1
XA8	82	J2	K1				COM 2
XA19	83	XA20	87				CONV
XA19	65	XA20	64				CONV COMP
XA11	5	XA11	30				CS-0A11
XA12	5	XA12	30				CS-0A12
XA13	30	XA13	5				CS-0A13
XA14	30	XA14	5				CS-0A14
XA15	30	XA15	5				CS-0A15
XA16	5	XA16	30				CS-0A16
XA17	30	XA17	5				CS-0A17
XA18	30	XA18	5				CS-0A18
XA28	30	XA28	5				CS-0A28
XA29	5	XA29	30				CS-0A29
XA30	30	XA30	5				CS-0A30
XA31	5	XA31	30				CS-0A31
XA32	30	XA32	5				CS-0A32
XA33	5	XA33	30				CS-0A33
XA34	5	XA34	30				CS-0A34
XA35	5	XA35	30				CS-0A35
XA36	30	XA36	5				CS-0A36
XA11	49	XA11	7				CS-1A11
XA13	7	XA13	49				CS-1A13
XA12	7	XA12	49				CS-1A12
XA14	7	XA14	49				CS-1A14
XA15	49	XA15	7				CS-1A15
XA16	7	XA16	49				CS-1A16
XA17	49	XA17	7				CS-1A17
XA18	49	XA18	7				CS-1A18
XA28	7	XA28	49				CS-1A28
XA29	7	XA29	49				CS-1A29
XA30	7	XA30	49				CS-1A30
XA31	7	XA31	49				CS-1A31
XA32	49	XA32	7				CS-1A32
XA33	7	XA33	49				CS-1A33
XA34	7	XA34	49				CS-1A34
XA35	7	XA35	49				CS-1A35

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA36	7	XA36	49				CS-1A36
XA11	67	XA11	6				CS-2A11
XA12	67	XA12	6				CS-2A12
XA13	6	XA13	67				CS-2A13
XA14	67	XA14	6				CS-2A14
XA15	67	XA15	6				CS-2A15
XA16	6	XA16	67				CS-2A16
XA17	67	XA17	6				CS-2A17
XA18	67	XA18	6				CS-2A18
XA28	67	XA28	6				CS-2A28
XA29	6	XA29	67				CS-2A29
XA30	67	XA30	6				CS-2A30
XA31	6	XA31	67				CS-2A31
XA32	6	XA32	67				CS-2A32
XA33	67	XA33	6				CS-2A33
XA34	6	XA34	67				CS-2A34
XA35	6	XA35	67				CS-2A35
XA36	67	XA36	6				CS-2A36
XA11	85	XA11	8				CS-3A11
XA12	85	XA12	8				CS-3A12
XA13	85	XA13	8				CS-3A13
XA14	8	XA14	85				CS-3A14
XA15	8	XA15	85				CS-3A15
XA16	85	XA16	8				CS-3A16
XA17	8	XA17	85				CS-3A17
XA18	85	XA18	8				CS-3A18
XA28	8	XA28	85				CS-3A28
XA29	8	XA29	85				CS-3A29
XA30	8	XA30	85				CS-3A30
XA31	85	XA31	8				CS-3A31
XA32	8	XA32	85				CS-3A32
XA33	85	XA33	8				CS-3A33
XA34	8	XA34	85				CS-3A34
XA35	8	XA35	85				CS-3A35
XA36	8	XA36	85				CS-3A36
XA20	79	XA21	27				DA ENABLE
XA9	85	J1	M7				DF ENABLE
J2	A1	XA1	52				DM0*
XA1	50	J2	A2				DM1*
J2	A3	XA1	49				DM2*
XA1	51	J2	A4				DM3*
J2	A5	XA1	4B				DM4*
XA1	47	J2	A6				DM5*
J2	A7	XA1	45				DM6*
XA1	46	J2	A8				DM7*
XA2	34	XA1	84				D0*

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA1	84	XA4	70				D0*
XA2	32	XA1	76				D1*
XA1	76	XA4	69				D1*
XA5	12	XA1	70				D10*
XA1	70	XA3	29				D10*
XA3	31	XA1	62				D11*
XA1	62	XA5	10				D11*
XA5	6	XA1	7				D12*
XA1	7	XA3	22				D12*
XA3	87	XA1	15				D13*
XA1	15	XA5	5				D13*
XA5	8	XA1	23				D14*
XA1	23	XA3	88				D14*
XA3	86	XA1	31				D15*
XA1	31	XA5	9				D15*
XA1	68	XA2	29				D2*
XA2	29	XA4	12				D2*
XA4	10	XA2	31				D3*
XA2	31	XA1	60				D3*
XA1	9	XA2	22				D4*
XA2	22	XA4	6				D4*
XA4	5	XA2	87				D5*
XA2	87	XA1	17				D5*
XA1	25	XA2	88				D6*
XA2	88	XA4	8				D6*
XA2	86	XA4	9				D7*
XA4	9	XA1	33				D7*
XA1	86	XA5	70				D8*
XA5	70	XA3	34				D8*
XA3	32	XA5	69				D9*
XA5	69	XA1	78				D9*
XA8	64	XA7	70				EXEC
XA7	70	XA6	62				EXEC
XA7	84	XA8	14				EXECT
XA6	5	J5	A1				FLG 0
J5	A2	XA6	38				FLG 1
XA6	85	J5	C1				FLG 10
J5	C2	XA6	84				FLG 11
XA6	83	J5	C3				FLG 12
XA6	44	XA8	30				FLG 14
XA8	30	J5	C5				FLG 14
J5	C6	XA1	79				FLG 15
XA1	79	XA6	81				FLG 15
J5	A3	XA6	7				FLG 2
XA6	7	XA20	68				FLG 2
J5	A4	XA6	10				FLG 3

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
J5	A5	XA6	9				FLG 4
J5	A6	XA6	12				FLG 5
J5	A7	XA6	41				FLG 6
J5	A8	XA6	43				FLG 7
J5	P9	XA6	35				FLG 8
J5	P0	XA6	80				FLG 9
XA8	74	J2	C6				HALT
XA18	26	XA17	26				HSROM*
XA17	26	XA16	26				HSROM*
XA16	26	XA15	26				HSROM*
XA15	26	XA31	26				HSROM*
XA31	26	XA14	26				HSROM*
XA14	26	XA12	26				HSROM*
XA12	26	XA11	26				HSROM*
XA11	26	XA8	5				HSROM*
XA7	80	XA6	50				ICLK
XA6	50	XA8	44				ICLK
XA20	39	XA21	60				ID 0
XA21	63	XA20	40				ID 1
XA9	64	XA31	77				INB 0
XA31	77	XA8	40				INB 0
XA8	40	XA10	68				INB 0
XA10	68	XA1	85				INB 0
XA1	77	XA10	70				INB 1
XA10	70	XA8	42				INB 1
XA8	42	XA31	73				INB 1
XA31	73	XA9	72				INB 1
XA9	66	XA31	42				INB 10
XA31	42	XA10	83				INB 10
XA10	83	XA7	74				INB 10
XA7	74	XA1	67				INB 10
XA1	59	XA7	71				INB 11
XA7	71	XA10	84				INB 11
XA10	84	XA31	41				INB 11
XA31	41	XA9	63				INB 11
XA9	79	XA31	40				INB 12
XA31	40	XA10	44				INB 12
XA10	44	XA7	40				INB 12
XA7	40	XA1	10				INB 12
XA1	18	XA7	44				INB 13
XA7	44	XA10	43				INB 13
XA10	43	XA31	39				INB 13
XA31	39	XA9	75				INB 13
XA9	76	XA31	38				INB 14
XA31	38	XA10	42				INB 14
XA10	42	XA7	37				INB 14

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA7	37	XA1	26				INB 14
XA1	34	XA7	35				INB 15
XA7	35	XA10	41				INB 15
XA10	41	XA31	34				INB 15
XA31	34	XA9	82				INB 15
XA9	74	XA31	66				INB 16
XA31	66	XA10	40				INB 16
XA10	40	XA7	16				INB 16
XA7	16	XA1	81				INB 16
XA1	73	XA7	19				INB 17
XA7	19	XA10	39				INB 17
XA10	39	XA31	65				INB 17
XA31	65	XA9	80				INB 17
XA9	78	XA31	64				INB 18
XA31	64	XA10	6				INB 18
XA10	6	XA7	14				INB 18
XA7	14	XA1	65				INB 18
XA1	57	XA7	13				INB 19
XA7	13	XA10	5				INB 19
XA10	5	XA31	63				INB 19
XA31	63	XA9	73				INB 19
XA9	68	XA31	75				INB 2
XA31	75	XA8	38				INB 2
XA8	38	XA10	67				INB 2
XA10	67	XA1	69				INB 2
XA1	12	XA10	8				INB 20
XA10	8	XA7	52				INB 20
XA7	52	XA31	61				INB 20
XA31	61	XA9	83				INB 20
XA9	77	XA31	59				INB 21
XA31	59	XA7	56				INB 21
XA7	56	XA10	7				INB 21
XA10	7	XA1	20				INB 21
XA1	28	XA10	10				INB 22
XA10	10	XA7	51				INB 22
XA7	51	XA31	55				INB 22
XA31	55	XA9	81				INB 22
XA9	84	XA31	56				INB 23
XA31	56	XA7	50				INB 23
XA7	50	XA10	9				INB 23
XA10	9	XA1	36				INB 23
XA1	61	XA8	36				INB 3
XA8	36	XA10	64				INB 3
XA10	64	XA31	76				INB 3
XA31	76	XA9	61				INB 3
XA9	71	XA31	15				INB 4

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA31	15	XA10	66				INB 4
XA10	66	XA7	73				INB 4
XA7	73	XA1	8				INB 4
XA1	16	XA7	79				INB 5
XA7	79	XA10	65				INB 5
XA10	65	XA31	74				INB 5
XA31	74	XA9	65				INB 5
XA9	69	XA31	72				INB 6
XA31	72	XA10	83				INB 6
XA10	83	XA7	76				INB 6
XA7	76	XA1	24				INB 6
XA1	32	XA7	72				INB 7
XA7	72	XA10	87				INB 7
XA10	87	XA31	57				INB 7
XA31	57	XA9	70				INB 7
XA9	62	XA31	44				INB 8
XA31	44	XA10	85				INB 8
XA10	85	XA7	69				INB 8
XA7	69	XA1	83				INB 8
XA1	75	XA7	78				INB 9
XA7	78	XA10	86				INB 9
XA10	86	XA31	43				INB 9
XA31	43	XA9	67				INB 9
XA20	88	XA19	59				INTDMP
J5	M3	XA8	7				INT 0*
J5	K7	XA8	34				INT 1*
J5	K8	XA8	32				INT 2*
J5	K9	XA8	31				INT 3*
J5	M1	XA8	28				INT 5*
XA8	28	XA20	76				INT 5*
J5	M2	XA8	25				INT 6*
XA7	41	XA8	24				I/O
XA8	24	XA6	60				I/O
XA8	50	XA5	82				I/O ACL*
XA5	82	XA4	82				I/O ACL*
XA4	76	XA5	76				I/O AG*
XA5	76	XA7	26				I/O AG*
XA21	35	XA4	80				I/O A0*
J4	C7	XA21	35				I/O A0*
XA4	74	XA26	16				I/O A1*
J4	C8	XA4	74				I/O A1*
XA5	73	J4	K3				I/O A10*
J4	K4	XA5	78				I/O A11*
XA5	7	J4	K5				I/O A12*
J4	K6	XA5	11				I/O A13*
XA5	14	J4	K7				I/O A14*

Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
J4	K8	XA5	16				I/O A15*
XA21	33	XA26	14				I/O A2*
J4	C9	XA21	33				I/O A2*
XA4	78	XA26	10				I/O A3*
J4	C0	XA4	78				I/O A3*
J4	E1	XA4	7				I/O A4*
XA4	7	XA21	8				I/O A4*
J4	E2	XA4	11				I/O A5*
XA4	11	XA21	7				I/O A5*
J4	E3	XA4	14				I/O A6*
XA4	14	XA21	9				I/O A6*
XA21	10	XA4	16				I/O A7*
XA4	16	J4	E7				I/O A7*
J4	K1	XA5	80				I/O A8*
XA5	74	J4	K2				I/O A9*
XA5	72	XA4	72				I/O CL*
XA4	72	XA8	52				I/O CL*
XA4	68	XA5	68				I/O G*
XA5	68	XA7	27				I/O G*
XA6	13	XA5	30				I/O M
XA5	30	XA8	81				I/O M
XA8	81	XA4	30				I/O M
J4	E9	XA8	79				I/O M*
XA8	79	XA21	12				I/O M*
XA8	76	XA21	11				I/O S*
XA6	37	XA8	76				I/O S*
J4	E8	XA6	37				I/O S*
J4	P1	XA4	66				I/O 0*
XA4	66	XA19	67				I/O 0*
XA19	67	XA21	17				I/O 0*
XA4	63	XA21	20				I/O 1*
J4	P2	XA19	69				I/O 1*
XA19	69	XA4	63				I/O 1*
XA20	81	XA5	64				I/O 10*
XA21	13	XA20	81				I/O 10*
J4	C1	XA21	13				I/O 10*
XA20	72	XA21	24				I/O 11*
XA5	45	XA20	72				I/O 11*
J4	C2	XA5	45				I/O 11*
XA20	71	XA5	29				I/O 12*
J4	C3	XA20	71				I/O 12*
J4	C4	XA5	24				I/O 13*
J4	C5	XA5	31				I/O 14*
J4	C6	XA5	36				I/O 15*
XA21	23	XA26	64				I/O 2*

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
J4	A3	XA19	75				I/O 2*
XA19	75	XA21	23				I/O 2*
XA21	16	XA19	77				I/O 3*
XA4	45	XA21	16				I/O 3*
J4	A4	XA4	45				I/O 3*
XA4	29	XA21	15				I/O 4*
J4	A5	XA4	29				I/O 4*
XA21	15	XA26	62				I/O 4*
J4	A6	XA21	18				I/O 5*
XA21	18	XA19	79				I/O 5*
XA19	79	XA4	24				I/O 5*
XA19	84	XA26	60				I/O 6*
XA21	19	XA19	84				I/O 6*
J4	A7	XA21	19				I/O 6*
J4	A8	XA21	25				I/O 7*
XA21	25	XA19	85				I/O 7*
XA19	85	XA4	36				I/O 7*
XA21	21	XA26	56				I/O 8*
XA5	66	XA21	21				I/O 8*
J4	A9	XA5	66				I/O 8*
J4	A0	XA5	63				I/O 9*
XA5	63	XA19	87				I/O 9*
XA19	87	XA26	53				I/O 9*
XA6	48	XA8	27				IR C*
XA5	50	XA8	58				IR CL*
XA6	58	XA4	50				IR CL*
XA4	47	XA5	47				IR G*
XA5	47	XA7	32				IR G*
XA7	58	XA8	66				IR WS
XA8	15	XA6	29				IR 0*
XA6	29	XA3	9				IR 0*
XA3	9	XA2	9				IR 0*
XA2	10	XA3	10				IR 1
XA3	10	XA6	31				IR 1
XA6	31	XA8	33				IR 1
XA7	49	XA6	51				IR 10*
XA6	51	XA2	21				IR 10*
XA2	20	XA6	46				IR 11*
XA6	46	XA7	75				IR 11*
XA8	12	XA7	8				IR 12*
XA7	8	XA2	24				IR 12*
XA2	23	XA7	9				IR 13*
XA7	62	XA8	80				IR 14*
XA8	80	XA3	16				IR 14*
XA3	5	XA3	13				IR 15*

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA3	13	XA2	5				IR 15*
XA2	5	XA7	22				IR 15*
XA7	22	XA6	14				IR 15*
XA7	15	XA2	6				IR 16*
XA2	6	XA3	15				IR 16*
XA3	15	XA3	6				IR 16*
XA3	30	XA3	19				IR 17*
XA3	19	XA7	6				IR 17*
XA7	6	XA2	30				IR 17*
XA7	25	XA3	21				IR 18*
XA3	21	XA3	27				IR 18*
XA3	27	XA2	27				IR 18*
XA2	28	XA3	28				IR 19*
XA3	28	XA3	20				IR 19*
XA3	20	XA7	12				IR 19*
XA8	29	XA6	33				IR 2
XA6	33	XA3	8				IR 2
XA3	8	XA2	8				IR 2
XA2	26	XA3	26				IR 20*
XA3	26	XA3	24				IR 20*
XA3	24	XA7	5				IR 20*
XA7	7	XA3	14				IR 21*
XA3	14	XA3	23				IR 21*
XA3	23	XA2	14				IR 21*
XA8	51	XA6	27				IR 3*
XA6	68	XA7	82				IR 6*
XA7	82	XA8	23				IR 6*
XA8	23	XA2	16				IR 6*
XA2	13	XA7	77				IR 7*
XA7	77	XA6	79				IR 7*
XA6	73	XA7	66				IR 8*
XA7	66	XA2	15				IR 8*
XA2	19	XA7	81				IR 9*
XA7	81	XA6	55				IR 9*
XA19	53	XA20	42				IT 0
XA20	42	XA21	65				IT 0
XA21	64	XA20	41				IT 1
XA20	41	XA19	55				IT 1
XA19	57	XA20	43				IT 2
XA6	23	XA8	61				JMP*
XA8	61	XA7	59				JMP*
XA7	42	XA6	32				JMPEX
J2	E2	XA8	19				LAS W0*
XA8	6	J2	E3				LAS W1*
J2	E4	XA8	8				LAS W2*

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA7	87	XA2	18				LI G*
XA2	18	XA3	18				LI G*
XA3	68	XA2	68				M
XA2	68	XA7	64				M
XA7	64	XA6	36				M
XA2	85	XA3	51				MARB*
XA3	49	XA2	84				MARC*
XA2	83	XA3	83				MARCL*
XA3	83	XA8	54				MARCL*
XA8	78	XA7	23				MARDN*
XA7	23	XA2	51				MARDN*
XA2	49	XA7	61				MARUP*
XA7	61	XA8	77				MARUP*
XA8	56	XA2	81				MEMCL*
XA2	81	XA3	81				MEMCL*
XA23	89	XA20	79				MEME*
XA23	79	XA22	89				MEME*
XA22	89	XA22	79				MEME*
XA22	79	XA24	79				MEME*
XA24	79	XA24	89				MEME*
XA4	42	XA7	38				MEMG*
XA7	38	XA5	42				MEMG*
XA21	79	XA20	84				MOD CONT
XA22	49	XA27	68				MS 0*
XA27	68	XA4	53				MS 0*
XA4	53	XA23	49				MS 0*
XA23	49	XA24	49				MS 0*
XA23	47	XA24	47				MS 1*
XA24	47	XA4	54				MS 1*
XA4	54	XA27	70				MS 1*
XA27	70	XA22	47				MS 1*
XA22	83	XA27	83				MS 10*
XA27	83	XA5	55				MS 10*
XA5	55	XA24	83				MS 10*
XA24	83	XA23	83				MS 10*
XA24	7	XA23	7				MS 11*
XA23	7	XA5	57				MS 11*
XA5	57	XA27	84				MS 11*
XA27	84	XA22	7				MS 11*
XA27	44	XA22	10				MS 12*
XA22	10	XA5	41				MS 12*
XA5	41	XA24	10				MS 12*
XA24	10	XA23	10				MS 12*
XA24	23	XA23	23				MS 13*
XA23	23	XA5	21				MS 13*

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA5	21	XA27	43				MS 13*
XA27	43	XA22	23				MS 13*
XA27	42	XA22	15				MS 14*
XA22	15	XA5	20				MS 14*
XA5	20	XA24	15				MS 14*
XA24	15	XA23	15				MS 14*
XA24	26	XA5	18				MS 15*
XA5	18	XA22	26				MS 15*
XA22	81	XA27	67				MS 2*
XA27	67	XA4	55				MS 2*
XA4	55	XA23	81				MS 2*
XA23	81	XA24	81				MS 2*
XA23	5	XA24	5				MS 3*
XA24	5	XA4	57				MS 3*
XA4	57	XA22	5				MS 3*
XA22	5	XA27	64				MS 3*
XA22	9	XA27	66				MS 4*
XA27	66	XA4	41				MS 4*
XA4	41	XA24	9				MS 4*
XA24	9	XA23	9				MS 4*
XA23	8	XA24	8				MS 5*
XA24	8	XA4	21				MS 5*
XA4	21	XA22	8				MS 5*
XA22	8	XA27	65				MS 5*
XA27	88	XA22	22				MS 6*
XA22	22	XA4	20				MS 6*
XA4	20	XA23	22				MS 6*
XA23	22	XA24	22				MS 6*
XA23	21	XA24	21				MS 7*
XA24	21	XA4	18				MS 7*
XA4	18	XA22	21				MS 7*
XA22	21	XA27	87				MS 7*
XA22	57	XA27	85				MS 8*
XA27	85	XA5	53				MS 8*
XA5	53	XA23	57				MS 8*
XA23	57	XA24	57				MS 8*
XA23	82	XA24	82				MS 9*
XA24	82	XA5	54				MS 9*
XA5	54	XA27	86				MS 9*
XA27	86	XA22	82				MS 9*
XA1	42	J2	49				MUX 0*
J2	A0	XA1	43				MUX 1*
XA1	44	J2	C1				MUX 2*
XA1	55	XA6	22				OVFL*

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA6	22	XA7	18				OVFL*
XA7	29	XA3	54				0 15*
XA4	44	XA8	68				PC CLK
XA8	68	XA5	44				PC CLK
XA8	17	XA4	62				PC CNL*
XA4	62	J4	E6				PC CNL*
XA4	49	XA5	62				PC CNN*
XA5	61	XA7	34				PC G*
XA7	34	XA4	61				PC G*
XA8	75	XA6	39				PC JMP*
XA5	65	XA7	65				PC M
XA7	65	XA4	65				PC M
XA4	60	XA7	39				PC S0
XA7	39	XA5	60				PC S0
XA7	60	XA4	59				PC S1L
XA7	63	XA5	59				PC S1M
XA7	57	XA4	67				PC S2L
XA7	54	XA5	67				PC S2M
XA5	58	XA4	58				PC S3
XA4	58	XA7	55				PC S3
XA4	52	XA5	52				PC WS
XA5	52	XA8	70				PC WS
XA10	69	XA16	77				PIN 0A
XA16	77	XA17	77				PIN 0A
XA17	77	XA18	77				PIN 0A
XA18	77	XA15	77				PIN 0A
XA10	56	XA11	77				PIN 0B
XA11	77	XA14	77				PIN 0B
XA14	77	XA12	77				PIN 0B
XA12	77	XA13	77				PIN 0B
XA10	71	XA15	73				PIN 1A
XA15	73	XA18	73				PIN 1A
XA18	73	XA17	73				PIN 1A
XA17	73	XA16	73				PIN 1A
XA10	55	XA14	73				PIN 1B
XA14	73	XA12	73				PIN 1B
XA12	73	XA11	73				PIN 1B
XA11	73	XA13	73				PIN 1B
XA10	81	XA16	42				PIN 10A
XA16	42	XA18	42				PIN 10A
XA18	42	XA17	42				PIN 10A
XA17	42	XA15	42				PIN 10A
XA10	82	XA13	42				PIN 10B
XA13	42	XA12	42				PIN 10B
XA12	42	XA14	42				PIN 10B

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA14	42	XA11	42				PIN 10B
XA10	80	XA17	41				PIN 11A
XA17	41	XA15	41				PIN 11A
XA15	41	XA16	41				PIN 11A
XA16	41	XA18	41				PIN 11A
XA10	79	XA12	41				PIN 11B
XA12	41	XA11	41				PIN 11B
XA11	41	XA14	41				PIN 11B
XA14	41	XA13	41				PIN 11B
XA10	45	XA18	40				PIN 12A
XA18	40	XA15	40				PIN 12A
XA15	40	XA16	40				PIN 12A
XA16	40	XA17	40				PIN 12A
XA10	31	XA13	40				PIN 12B
XA13	40	XA12	40				PIN 12B
XA12	40	XA11	40				PIN 12B
XA11	40	XA14	40				PIN 12B
XA10	47	XA16	39				PIN 13A
XA16	39	XA15	39				PIN 13A
XA15	39	XA18	39				PIN 13A
XA18	39	XA17	39				PIN 13A
XA10	33	XA12	39				PIN 13B
XA12	39	XA14	39				PIN 13B
XA14	39	XA13	39				PIN 13B
XA13	39	XA11	39				PIN 13B
XA10	46	XA16	38				PIN 14A
XA16	38	XA15	38				PIN 14A
XA15	38	XA18	38				PIN 14A
XA18	38	XA17	38				PIN 14A
XA10	34	XA13	38				PIN 14B
XA13	38	XA14	38				PIN 14B
XA14	38	XA12	38				PIN 14B
XA12	38	XA11	38				PIN 14B
XA10	37	XA18	34				PIN 15A
XA18	34	XA15	34				PIN 15A
XA15	34	XA17	34				PIN 15A
XA17	34	XA16	34				PIN 15A
XA11	34	XA10	25				PIN 15B
XA10	25	XA12	34				PIN 15B
XA12	34	XA14	34				PIN 15B
XA14	34	XA13	34				PIN 15B
XA10	38	XA16	66				PIN 16A
XA16	66	XA15	66				PIN 16A
XA15	66	XA18	66				PIN 16A
XA18	66	XA17	66				PIN 16A
XA11	66	XA10	28				PIN 16B

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Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA10	28	XA12	66				PIN 16B
XA12	66	XA14	66				PIN 16B
XA14	66	XA13	66				PIN 16B
XA10	36	XA15	65				PIN 17A
XA15	65	XA18	65				PIN 17A
XA18	65	XA16	65				PIN 17A
XA16	65	XA17	65				PIN 17A
XA11	65	XA10	30				PIN 17B
XA10	30	XA13	65				PIN 17B
XA13	65	XA12	65				PIN 17B
XA12	65	XA14	65				PIN 17B
XA10	12	XA18	64				PIN 18A
XA18	64	XA17	64				PIN 18A
XA17	64	XA15	64				PIN 18A
XA15	64	XA16	64				PIN 18A
XA11	64	XA10	11				PIN 18B
XA10	11	XA12	64				PIN 18B
XA12	64	XA13	64				PIN 18B
XA13	64	XA14	64				PIN 18B
XA10	14	XA15	63				PIN 19A
XA15	63	XA17	63				PIN 19A
XA17	63	XA16	63				PIN 19A
XA16	63	XA18	63				PIN 19A
XA11	63	XA10	13				PIN 19B
XA10	13	XA14	63				PIN 19B
XA14	63	XA12	63				PIN 19B
XA12	63	XA13	63				PIN 19B
XA10	72	XA15	75				PIN 2A
XA15	75	XA16	75				PIN 2A
XA16	75	XA18	75				PIN 2A
XA18	75	XA17	75				PIN 2A
XA12	75	XA11	75				PIN 2B
XA11	75	XA10	58				PIN 2B
XA10	58	XA14	75				PIN 2B
XA14	75	XA13	75				PIN 2B
XA10	16	XA18	61				PIN 20A
XA18	61	XA16	61				PIN 20A
XA16	61	XA15	61				PIN 20A
XA15	61	XA17	61				PIN 20A
XA11	61	XA12	61				PIN 20B
XA12	61	XA10	15				PIN 20B
XA10	15	XA13	61				PIN 20B
XA13	61	XA14	61				PIN 20B
XA10	20	XA17	59				PIN 21A
XA17	59	XA15	59				PIN 21A
XA15	59	XA18	59				PIN 21A

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA18	59	XA16	59				PIN 21A
XA11	59	XA12	59				PIN 21B
XA12	59	XA10	17				PIN 21B
XA10	17	XA13	59				PIN 21B
XA13	59	XA14	59				PIN 21B
XA10	22	XA18	55				PIN 22A
XA18	55	XA16	55				PIN 22A
XA16	55	XA17	55				PIN 22A
XA17	55	XA15	55				PIN 22A
XA12	55	XA11	55				PIN 22B
XA11	55	XA13	55				PIN 22B
XA13	55	XA14	55				PIN 22B
XA14	55	XA10	18				PIN 22B
XA15	56	XA17	56				PIN 23A
XA17	56	XA16	56				PIN 23A
XA16	56	XA18	56				PIN 23A
XA18	56	XA10	24				PIN 23A
XA10	19	XA12	56				PIN 23B
XA12	56	XA11	56				PIN 23B
XA11	56	XA14	56				PIN 23B
XA14	56	XA13	56				PIN 23B
XA16	76	XA18	76				PIN 3A
XA18	76	XA17	76				PIN 3A
XA17	76	XA15	76				PIN 3A
XA15	76	XA10	63				PIN 3A
XA10	52	XA12	76				PIN 3B
XA12	76	XA13	76				PIN 3B
XA13	76	XA11	76				PIN 3B
XA11	76	XA14	76				PIN 3B
XA15	15	XA17	15				PIN 4A
XA17	15	XA18	15				PIN 4A
XA18	15	XA16	15				PIN 4A
XA16	15	XA10	61				PIN 4A
XA10	54	XA13	15				PIN 4B
XA13	15	XA14	15				PIN 4B
XA14	15	XA11	15				PIN 4B
XA11	15	XA12	15				PIN 4B
XA17	74	XA15	74				PIN 5A
XA15	74	XA18	74				PIN 5A
XA18	74	XA16	74				PIN 5A
XA16	74	XA10	62				PIN 5A
XA10	53	XA12	74				PIN 5B
XA12	74	XA14	74				PIN 5B
XA14	74	XA13	74				PIN 5B
XA13	74	XA11	74				PIN 5B

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Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA15	72	XA16	72				PIN 6A
XA16	72	XA18	72				PIN 6A
XA18	72	XA17	72				PIN 6A
XA17	72	XA10	76				PIN 6A
XA10	77	XA11	72				PIN 6B
XA11	72	XA13	72				PIN 6B
XA13	72	XA14	72				PIN 6B
XA14	72	XA12	72				PIN 6B
XA16	57	XA17	57				PIN 7A
XA17	57	XA18	57				PIN 7A
XA18	57	XA15	57				PIN 7A
XA15	57	XA10	73				PIN 7A
XA10	78	XA11	57				PIN 7B
XA11	57	XA14	57				PIN 7B
XA14	57	XA12	57				PIN 7B
XA12	57	XA13	57				PIN 7B
XA15	44	XA16	44				PIN 8A
XA16	44	XA17	44				PIN 8A
XA17	44	XA18	44				PIN 8A
XA18	44	XA10	74				PIN 8A
XA10	75	XA12	44				PIN 8B
XA12	44	XA13	44				PIN 8B
XA13	44	XA14	44				PIN 8B
XA14	44	XA11	44				PIN 8B
XA17	44	XA16	43				PIN 9A
XA16	43	XA18	43				PIN 9A
XA18	43	XA10	59				PIN 9A
XA10	59	XA15	43				PIN 9A
XA10	60	XA14	43				PIN 9B
XA14	43	XA11	43				PIN 9B
XA11	43	XA13	43				PIN 9B
XA13	43	XA12	43				PIN 9B
XA8	37	XA5	35				PR
XA5	35	XA4	35				PR
XA8	46	XA4	38				PR*
J4	E0	XA5	38				PR*
XA5	38	XA6	66				PR*
XA6	66	XA7	24				PR*
XA7	24	XA8	46				PR*
XA8	72	J2	C8				PRES
J2	C9	XA8	73				PRES*
XA13	78	XA4	88				RAD 0
XA4	88	XA17	78				RAD 0
XA17	78	XA18	78				RAD 0
XA18	78	XA9	5				RAD 0

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA9	5	XA15	78				RAD 0
XA15	78	XA16	78				RAD 0
XA16	78	XA31	78				RAD 0
XA31	78	XA12	78				RAD 0
XA12	78	XA11	78				RAD 0
XA11	78	XA14	78				RAD 0
XA14	37	XA11	37				RAD 1
XA11	37	XA31	37				RAD 1
XA31	37	XA12	37				RAD 1
XA12	37	XA15	37				RAD 1
XA15	37	XA16	37				RAD 1
XA16	37	XA18	37				RAD 1
XA18	37	XA9	11				RAD 1
XA9	11	XA17	37				RAD 1
XA17	37	XA4	87				RAD 1
XA4	87	XA13	37				RAD 1
XA13	46	XA5	86				RAD 10
XA5	86	XA18	46				RAD 10
XA18	46	XA17	46				RAD 10
XA17	46	XA9	17				RAD 10
XA9	17	XA16	46				RAD 10
XA16	46	XA12	46				RAD 10
XA12	46	XA11	46				RAD 10
XA11	46	XA31	46				RAD 10
XA31	46	XA15	46				RAD 10
XA15	46	XA14	46				RAD 10
XA14	46	XA11	27				RAD 11
XA11	27	XA31	27				RAD 11
XA31	27	XA15	27				RAD 11
XA15	27	XA12	27				RAD 11
XA12	27	XA16	27				RAD 11
XA16	27	XA9	15				RAD 11
XA9	15	XA17	27				RAD 11
XA17	27	XA18	27				RAD 11
XA18	27	XA5	84				RAD 11
XA5	84	XA13	27				RAD 11
XA13	20	XA5	85				RAD 12
XA5	85	XA18	20				RAD 12
XA18	20	XA9	20				RAD 12
XA9	20	XA16	20				RAD 12
XA16	20	XA31	20				RAD 12
XA31	20	XA12	20				RAD 12
XA12	20	XA15	20				RAD 12
XA15	20	XA14	20				RAD 12
XA14	20	XA11	20				RAD 12

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	FUNCTION/REMARKS
XA11	20	XA17	20				RAD 12
XA17	20	XA10	23				RAD 12
XA10	26	XA17	18				RAD 13
XA17	18	XA11	18				RAD 13
XA11	18	XA12	18				RAD 13
XA12	18	XA31	18				RAD 13
XA31	18	XA15	18				RAD 13
XA15	18	XA14	18				RAD 13
XA14	18	XA16	18				RAD 13
XA16	18	XA18	18				RAD 13
XA18	18	XA9	14				RAD 13
XA9	14	XA5	83				RAD 13
XA5	83	XA13	18				RAD 13
XA13	22	XA5	81				RAD 14
XA5	22	XA18	22				RAD 14
XA18	22	XA9	18				RAD 14
XA9	22	XA14	22				RAD 14
XA14	22	XA15	22				RAD 14
XA15	22	XA31	22				RAD 14
XA31	22	XA16	22				RAD 14
XA16	22	XA12	22				RAD 14
XA12	22	XA11	22				RAD 14
XA11	22	XA17	22				RAD 14
XA17	22	XA10	32				RAD 14
XA10	35	XA16	24				RAD 14
XA16	24	XA14	24				RAD 15
XA14	24	XA17	24				RAD 15
XA17	24	XA11	24				RAD 15
XA11	24	XA18	24				RAD 15
XA18	24	XA12	24				RAD 15
XA12	24	XA31	24				RAD 15
XA31	24	XA15	24				RAD 15
XA15	24	XA9	16				RAD 15
XA9	16	XA5	79				RAD 15
XA5	79	XA13	24				RAD 15
XA13	60	XA4	86				RAD 2
XA4	86	XA9	7				RAD 2
XA9	7	XA12	60				RAD 2
XA12	60	XA18	60				RAD 2
XA18	60	XA16	60				RAD 2
XA16	60	XA15	60				RAD 2
XA15	60	XA14	60				RAD 2
XA14	60	XA31	60				RAD 2
XA31	60	XA17	60				RAD 2
XA17	60	XA11	60				RAD 2

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA15	80	XA17	80				RAD 3
XA17	80	XA14	80				RAD 3
XA14	80	XA31	80				RAD 3
XA31	80	XA16	80				RAD 3
XA16	80	XA11	80				RAD 3
XA11	80	XA12	80				RAD 3
XA12	80	XA18	80				RAD 3
XA18	80	XA9	9				RAD 3
XA9	9	XA4	84				RAD 3
XA4	84	XA13	80				RAD 3
XA13	81	XA4	85				RAD 4
XA4	85	XA9	6				RAD 4
XA9	6	XA18	81				RAD 4
XA18	81	XA12	81				RAD 4
XA12	81	XA17	81				RAD 4
XA17	81	XA11	81				RAD 4
XA11	81	XA15	81				RAD 4
XA15	81	XA16	81				RAD 4
XA16	81	XA31	81				RAD 4
XA31	81	XA14	81				RAD 4
XA11	82	XA16	82				RAD 5
XA16	82	XA14	82				RAD 5
XA14	82	XA31	82				RAD 5
XA31	82	XA12	82				RAD 5
XA12	82	XA17	82				RAD 5
XA17	82	XA18	82				RAD 5
XA18	82	XA9	12				RAD 5
XA9	12	XA15	82				RAD 5
XA15	82	XA4	83				RAD 5
XA4	83	XA13	82				RAD 5
XA13	84	XA4	81				RAD 6
XA4	81	XA9	8				RAD 6
XA9	8	XA14	84				RAD 6
XA14	84	XA17	84				RAD 6
XA17	84	XA15	84				RAD 6
XA15	84	XA18	84				RAD 6
XA18	84	XA12	84				RAD 6
XA12	84	XA16	84				RAD 6
XA16	84	XA11	84				RAD 6
XA11	84	XA31	84				RAD 6
XA14	71	XA16	71				RAD 7
XA16	71	XA12	71				RAD 7
XA12	71	XA18	71				RAD 7
XA18	71	XA15	71				RAD 7
XA15	71	XA17	71				RAD 7

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA17	71	XA31	71				RAD 7
XA31	71	XA11	71				RAD 7
XA11	71	XA9	10				RAD 7
XA9	10	XA4	79				RAD 7
XA4	79	XA13	71				RAD 7
XA13	10	XA5	88				RAD 8
XA5	88	XA9	19				RAD 8
XA9	19	XA31	10				RAD 8
XA31	10	XA17	10				RAD 8
XA17	10	XA15	10				RAD 8
XA15	10	XA14	10				RAD 8
XA14	10	XA12	10				RAD 8
XA12	10	XA11	10				RAD 8
XA11	10	XA16	10				RAD 8
XA16	10	XA18	10				RAD 8
XA18	9	XA17	9				RAD 9
XA17	9	XA16	9				RAD 9
XA16	9	XA12	9				RAD 9
XA12	9	XA11	9				RAD 9
XA11	9	XA14	9				RAD 9
XA14	9	XA15	9				RAD 9
XA15	9	XA31	9				RAD 9
XA31	9	XA9	13				RAD 9
XA9	13	XA5	87				RAD 9
XA5	87	XA13	9				RAD 9
XA8	35	XA3	12				REGCL
XA3	12	XA2	12				REGCL
XA9	37	J1	A3				RIN 0*
J1	A4	XA9	38				RIN 1*
XA9	47	J1	C3				RIN 10*
J1	C4	XA9	48				RIN 11*
XA9	49	J1	C5				RIN 12*
J1	C6	XA9	50				RIN 13*
XA9	51	J1	C7				RIN 14*
J1	C8	XA9	52				RIN 15*
XA9	53	J1	C9				RIN 16*
J1	C0	XA9	54				RIN 17*
XA9	55	J1	E1				RIN 18*
J1	E2	XA9	56				RIN 19*
XA9	39	J1	A5				RIN 2*
J1	E3	XA9	57				RIN 20*
XA9	58	J1	E8				RIN 21*
J1	E9	XA9	59				RIN 22*
XA9	60	J1	E0				RIN 23*
J1	A6	XA9	40				RIN 3*

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Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA9	41	J1	A7				RIN 4*
J1	A8	XA9	42				RIN 5*
XA9	43	J1	A9				RIN 6*
J1	A0	XA9	44				RIN 7*
XA9	45	J1	C1				RIN 8*
J1	C2	XA9	46				RIN 9*
XA1	71	XA8	69				RUN*
XA8	10	J2	C2				RUNS
J2	C3	XA8	9				RUNS*
XA7	53	XA2	82				SC 0
XA2	82	XA3	82				SC 0
XA3	67	XA2	67				SC 1
XA2	67	XA7	47				SC 1
XA8	48	XA7	48				SDN*
XA8	11	J2	C4				SGLST
J2	C5	XA8	13				SGLST*
XA7	30	XA2	72				SPADG*
XA2	72	XA3	72				SPADG*
XA2	42	XA22	59				SPAD 0
XA22	59	XA30	78				SPAD 0
XA30	78	XA35	78				SPAD 0
XA35	78	XA23	59				SPAD 0
XA23	59	XA24	59				SPAD 0
XA24	59	XA36	78				SPAD 0
XA36	78	XA28	78				SPAD 0
XA28	78	XA33	78				SPAD 0
XA33	78	XA34	78				SPAD 0
XA34	78	XA29	78				SPAD 0
XA29	78	XA32	78				SPAD 0
XA28	37	XA33	37				SPAD 1
XA33	37	XA29	37				SPAD 1
XA29	37	XA34	37				SPAD 1
XA34	37	XA32	37				SPAD 1
XA32	37	XA36	37				SPAD 1
XA36	37	XA35	37				SPAD 1
XA35	37	XA23	67				SPAD 1
XA23	67	XA24	67				SPAD 1
XA24	67	XA30	37				SPAD 1
XA30	37	XA22	67				SPAD 1
XA22	67	XA2	33				SPAD 1
XA3	69	XA22	41				SPAD 10
XA22	41	XA30	46				SPAD 10
XA30	46	XA36	46				SPAD 10
XA36	46	XA24	41				SPAD 10
XA24	41	XA35	46				SPAD 10

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Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA35	46	XA23	41				SPAD 10
XA23	41	XA34	46				SPAD 10
XA34	46	XA33	46				SPAD 10
XA33	46	XA28	46				SPAD 10
XA28	46	XA29	46				SPAD 10
XA29	46	XA32	46				SPAD 10
XA32	27	XA29	27				SPAD 11
XA29	27	XA28	27				SPAD 11
XA28	27	XA33	27				SPAD 11
XA33	27	XA34	27				SPAD 11
XA34	27	XA24	77				SPAD 11
XA24	77	XA23	77				SPAD 11
XA30	27	XA35	27				SPAD 11
XA35	27	XA36	27				SPAD 11
XA36	27	XA22	77				SPAD 11
XA21	43	XA20	27				FLG 12
XA3	71	XA30	27				SPAD 11
XA3	79	XA22	73				SPAD 12
XA22	73	XA30	20				SPAD 12
XA30	20	XA24	73				SPAD 12
XA24	73	XA23	73				SPAD 12
XA23	73	XA36	20				SPAD 12
XA36	20	XA34	20				SPAD 12
XA34	20	XA33	20				SPAD 12
XA33	20	XA29	20				SPAD 12
XA29	20	XA32	20				SPAD 12
XA32	20	XA28	20				SPAD 12
XA23	20	XA35	20				SPAD 12
XA35	20	XA27	23				SPAD 12
XA27	26	XA35	18				SPAD 13
XA35	18	XA28	18				SPAD 13
XA23	18	XA29	18				SPAD 13
XA29	18	XA32	18				SPAD 13
XA32	18	XA33	18				SPAD 13
XA33	18	XA34	18				SPAD 13
XA34	18	XA24	85				SPAD 13
XA24	85	XA36	18				SPAD 13
XA36	18	XA23	85				SPAD 13
XA23	85	XA30	18				SPAD 13
XA30	18	XA22	85				SPAD 13
XA22	85	XA3	74				SPAD 13
XA3	73	XA22	86				SPAD 14
XA22	86	XA30	22				SPAD 14
XA30	22	XA24	86				SPAD 14
XA24	86	XA23	86				SPAD 14

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Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA23	86	XA36	22				SPAD 14
XA36	22	XA32	22				SPAD 14
XA32	22	XA34	22				SPAD 14
XA34	22	XA33	22				SPAD 14
XA33	22	XA28	22				SPAD 14
XA28	22	XA29	22				SPAD 14
XA29	22	XA35	22				SPAD 14
XA35	22	XA27	32				SPAD 14
XA27	35	XA3	24				SPAD 15
XA35	24	XA29	24				SPAD 15
XA29	24	XA24	87				SPAD 15
XA24	87	XA34	24				SPAD 15
XA34	24	XA28	24				SPAD 15
XA26	24	XA33	24				SPAD 15
XA33	24	XA36	24				SPAD 15
XA36	24	XA32	24				SPAD 15
XA32	24	XA23	87				SPAD 15
XA23	87	XA30	24				SPAD 15
XA30	24	XA22	87				SPAD 15
XA22	87	XA3	80				SPAD 15
XA2	69	XA22	69				SPAD 2
XA22	69	XA30	60				SPAD 2
XA30	60	XA23	69				SPAD 2
XA23	69	XA24	69				SPAD 2
XA24	69	XA29	60				SPAD 2
XA29	60	XA34	60				SPAD 2
XA34	60	XA32	60				SPAD 2
XA32	60	XA28	60				SPAD 2
XA28	60	XA36	60				SPAD 2
XA36	60	XA35	60				SPAD 2
XA35	60	XA33	60				SPAD 3
XA34	80	XA33	80				SPAD 3
XA33	80	XA35	80				SPAD 3
XA35	80	XA29	80				SPAD 3
XA29	80	XA28	80				SPAD 3
XA28	80	XA36	80				SPAD 3
XA36	80	XA32	80				SPAD 3
XA32	80	XA23	58				SPAD 3
XA23	58	XA24	58				SPAD 3
XA24	58	XA30	80				SPAD 3
XA30	80	XA22	58				SPAD 3
XA22	58	XA2	71				SPAD 4
XA2	79	XA22	11				SPAD 4
XA22	11	XA30	81				SPAD 4
XA30	81	XA24	11				SPAD 4

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Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	FUNCTION/REMARKS
XA24	11	XA23	11				SPAD 4
XA23	11	XA32	81				SPAD 4
XA32	81	XA29	81				SPAD 4
XA29	81	XA36	81				SPAD 4
XA36	81	XA28	81				SPAD 4
XA28	81	XA35	81				SPAD 4
XA35	81	XA33	81				SPAD 4
XA33	81	XA34	81				SPAD 4
XA35	82	XA34	82				SPAD 5
XA34	82	XA29	82				SPAD 5
XA29	82	XA33	82				SPAD 5
XA33	82	XA36	82				SPAD 5
XA36	82	XA28	82				SPAD 5
XA28	82	XA32	82				SPAD 5
XA32	82	XA24	18				SPAD 5
XA24	18	XA23	18				SPAD 5
XA23	18	XA30	82				SPAD 5
XA30	82	XA22	18				SPAD 5
XA22	18	XA2	74				SPAD 5
XA2	73	XA22	12				SPAD 6
XA22	12	XA30	84				SPAD 6
XA30	84	XA24	12				SPAD 6
XA24	12	XA23	12				SPAD 6
XA23	12	XA34	84				SPAD 6
XA34	84	XA33	84				SPAD 6
XA33	84	XA36	84				SPAD 6
XA36	84	XA28	84				SPAD 6
XA28	84	XA32	84				SPAD 6
XA32	84	XA29	84				SPAD 6
XA29	84	XA35	84				SPAD 6
XA34	71	XA36	71				SPAD 7
XA36	71	XA32	71				SPAD 7
XA32	71	XA28	71				SPAD 7
XA28	71	XA35	71				SPAD 7
XA35	71	XA33	71				SPAD 7
XA33	71	XA29	71				SPAD 7
XA29	71	XA23	20				SPAD 7
XA23	20	XA24	71				SPAD 7
XA24	20	XA30	71				SPAD 7
XA30	71	XA22	20				SPAD 7
XA22	20	XA2	80				SPAD 7
XA3	42	XA22	14				SPAD 8
XA22	14	XA30	10				SPAD 8
XA30	10	XA24	14				SPAD 8
XA24	14	XA23	10				SPAD 8

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Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA23	14	XA29	10				SPAD 8
XA29	10	XA33	10				SPAD 8
XA33	10	XA35	10				SPAD 8
XA35	10	XA28	10				SPAD 8
XA28	10	XA32	10				SPAD 8
XA32	10	XA34	10				SPAD 8
XA34	10	XA36	10				SPAD 8
XA32	9	XA29	9				SPAD 9
XA29	9	XA34	9				SPAD 9
XA34	9	XA35	9				SPAD 9
XA35	9	XA33	9				SPAD 9
XA33	9	XA36	9				SPAD 9
XA36	9	XA28	9				SPAD 9
XA28	9	XA23	13				SPAD 9
XA23	13	XA24	13				SPAD 9
XA24	13	XA30	9				SPAD 9
XA30	9	XA22	13				SPAD 9
XA22	13	XA3	33				SPAD 9
XA23	78	XA24	78				SPIN 0
XA24	78	XA2	25				SPIN 0
XA2	25	XA22	78				SPIN 0
XA22	74	XA2	17				SPIN 1
XA2	17	XA24	74				SPIN 1
XA24	74	XA23	74				SPIN 1
XA23	66	XA24	66				SPIN 10
XA24	66	XA3	11				SPIN 10
XA3	11	XA22	66				SPIN 10
XA22	60	XA3	7				SPIN 11
XA3	7	XA23	60				SPIN 11
XA23	60	XA24	60				SPIN 11
XA23	51	XA24	51				SPIN 12
XA24	51	XA3	36				SPIN 12
XA3	36	XA22	51				SPIN 12
XA22	38	XA3	77				SPIN 13
XA3	77	XA24	38				SPIN 13
XA24	38	XA23	38				SPIN 13
XA23	29	XA24	29				SPIN 14
XA24	29	XA3	78				SPIN 14
XA3	78	XA22	29				SPIN 14
XA22	25	XA3	75				SPIN 15
XA3	75	XA24	25				SPIN 15
XA24	25	XA23	25				SPIN 15
XA23	62	XA24	62				SPIN 2
XA24	62	XA2	11				SPIN 2
XA2	11	XA22	62				SPIN 2

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Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA22	S6	XA22	53				SPIN 3
XA22	53	XA2	7				SPIN 3
XA2	7	XA24	53				SPIN 3
XA24	53	XA23	53				SPIN 3
XA23	45	XA24	45				SPIN 4
XA24	45	XA2	36				SPIN 4
XA2	36	XA22	45				SPIN 4
XA22	37	XA2	77				SPIN 5
XA2	77	XA24	37				SPIN 5
XA24	37	XA23	37				SPIN 5
XA24	27	XA23	27				SPIN 6
XA23	27	XA2	78				SPIN 6
XA2	78	XA22	27				SPIN 6
XA22	19	XA2	75				SPIN 7
XA2	75	XA24	19				SPIN 7
XA24	19	XA23	19				SPIN 7
XA23	71	XA24	71				SPIN 8
XA24	71	XA3	25				SPIN 8
XA3	25	XA22	71				SPIN 8
XA22	72	XA3	17				SPIN 9
XA3	17	XA24	72				SPIN 9
XA24	72	XA23	72				SPIN 9
XA24	28	XA23	28				SPW 0*
XA23	28	XA22	28				SPW 0*
XA22	28	XA8	39				SPW 0*
XA8	41	XA22	31				SPW 1*
XA22	31	XA23	31				SPW 1*
XA23	31	XA24	31				SPW 1*
XA4	27	XA5	25				STPB*
XA4	22	XA5	23				STPC*
XA4	37	XA5	37				STPCL*
XA5	37	XA8	60				STPCL*
XA8	43	XA4	25				STPDN*
XA4	77	XA7	31				STPG*
XA7	31	XA5	77				STPG*
XA8	45	XA4	23				STPUP*
XA8	47	XA7	43				SUP*
XA4	75	XA2	60				S 0*
XA2	60	XA1	80				S 0*
XA1	80	XA6	15				S 0*
XA1	72	XA2	59				S 1*
XA2	59	XA4	71				S 1*
XA4	71	XA6	11				S 1*
XA6	19	XA5	19				S 10*
XA5	19	XA1	66				S 10*
XA1	66	XA3	57				S 10*

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA3	55	XA1	58				S 11*
XA1	58	XA5	56				S 11*
XA5	56	XA6	21				S 11*
XA6	20	XA5	51				S 12*
XA5	51	XA1	11				S 12*
XA1	11	XA3	35				S 12*
XA3	56	XA1	19				S 13*
XA1	19	XA5	15				S 13*
XA5	15	XA6	45				S 13*
XA6	47	XA5	17				S 14*
XA5	17	XA1	27				S 14*
XA1	27	XA3	48				S 14*
XA3	53	XA1	35				S 15*
XA1	35	XA5	13				S 15*
XA5	13	XA7	36				S 15*
XA7	36	XA6	49				S 15*
XA6	54	XA4	19				S 2*
XA4	19	XA2	57				S 2*
XA2	57	XA1	64				S 2*
XA2	55	XA1	56				S 3*
XA1	56	XA4	56				S 3*
XA4	56	XA6	56				S 3*
XA6	58	XA4	51				S 4*
XA4	51	XA2	35				S 4*
XA2	35	XA1	13				S 4*
XA1	21	XA2	56				S 5*
XA2	56	XA4	15				S 5*
XA4	15	XA6	64				S 5*
XA6	57	XA4	17				S 6*
XA4	17	XA2	48				S 6*
XA2	48	XA1	29				S 6*
XA1	37	XA2	53				S 7*
XA2	53	XA4	13				S 7*
XA4	13	XA6	59				S 7*
XA6	61	XA5	75				S 8*
XA5	75	XA1	82				S 8*
XA1	82	XA3	60				S 8*
XA3	59	XA1	74				S 9*
XA1	74	XA5	71				S 9*
XA5	71	XA6	63				S 9*
XA20	85	XA19	61				T/H
XA8	67	XA1	41				TDGB*
XA1	39	XA8	49				TDGCL*
XA7	33	XA1	53				TDGDN*
XA11	16	XA11	32				VGG - 0A11

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	FUNCTION/REMARKS
XA12	16	XA12	32				VGG - 0A12
XA13	32	XA13	16				VGG - 0A13
XA14	16	XA14	32				VGG - 0A14
XA15	32	XA15	16				VGG - 0A15
XA16	32	XA16	16				VGG - 0A16
XA17	16	XA17	32				VGG - 0A17
XA18	32	XA18	16				VGG - 0A18
XA28	32	XA28	16				VGG - 0A28
XA29	32	XA29	16				VGG - 0A29
XA30	16	XA30	32				VGG - 0A30
XA31	16	XA31	32				VGG - 0A31
XA32	16	XA32	32				VGG - 0A32
XA33	16	XA33	32				VGG - 0A33
XA34	32	XA34	16				VGG - 0A34
XA35	16	XA35	32				VGG - 0A35
XA36	16	XA36	32				VGG - 0A36
XA11	51	XA11	17				VGG - 1A11
XA12	17	XA12	51				VGG - 1A12
XA13	51	XA13	17				VGG - 1A13
XA14	17	XA14	51				VGG - 1A14
XA15	17	XA15	51				VGG - 1A15
XA16	51	XA16	17				VGG - 1A16
XA17	17	XA17	51				VGG - 1A17
XA18	51	XA18	17				VGG - 1A18
XA28	51	XA28	17				VGG - 1A28
XA29	17	XA29	51				VGG - 1A29
XA30	51	XA30	17				VGG - 1A30
XA31	51	XA31	17				VGG - 1A31
XA32	17	XA32	51				VGG - 1A32
XA33	17	XA33	51				VGG - 1A33
XA34	51	XA34	17				VGG - 1A34
XA35	51	XA35	17				VGG - 1A35
XA36	17	XA36	51				VGG - 1A36
XA11	14	XA11	62				VGG - 2A11
XA12	62	XA12	14				VGG - 2A12
XA13	62	XA13	14				VGG - 2A13
XA14	62	XA14	14				VGG - 2A14
XA15	62	XA15	14				VGG - 2A15
XA16	14	XA16	62				VGG - 2A16
XA17	14	XA17	62				VGG - 2A17
XA18	62	XA18	14				VGG - 2A18
XA28	62	XA28	14				VGG - 2A28
XA29	62	XA29	14				VGG - 2A29
XA30	62	XA30	14				VGG - 2A30
XA31	62	XA31	14				VGG - 2A31

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA32	14	XA32	62				VGG - 2A32
XA33	14	XA33	62				VGG - 2A33
XA34	62	XA34	14				VGG - 2A34
XA35	62	XA35	14				VGG - 2A35
XA36	14	XA36	62				VGG - 2A36
XA11	13	XA11	83				VGG - 3A11
XA12	13	XA12	83				VGG - 3A12
XA13	83	XA13	13				VGG - 3A13
XA14	13	XA14	83				VGG - 3A14
XA15	13	XA15	83				VGG - 3A15
XA16	13	XA16	83				VGG - 3A16
XA17	13	XA17	83				VGG - 3A17
XA18	83	XA18	13				VGG - 3A18
XA28	13	XA28	83				VGG - 3A28
XA29	13	XA29	83				VGG - 3A29
XA30	83	XA30	13				VGG - 3A30
XA31	83	XA31	13				VGG - 3A31
XA32	83	XA32	13				VGG - 3A32
XA33	83	XA33	13				VGG - 3A33
XA34	13	XA34	83				VGG - 3A34
XA35	13	XA35	83				VGG - 3A35
XA36	83	XA36	13				VGG - 3A36
XA8	53	XA6	70				WAIT*
J1	K1	XA9	21				XAD 0*
XA9	22	J1	K2				XAD 1*
J1	M1	XA9	31				XAD 10*
XA9	32	J1	M2				XAD 11*
J1	M3	XA9	33				XAD 12*
XA9	34	J1	M4				XAD 13*
J1	M5	XA9	35				XAD 14*
XA9	36	J1	M6				XAD 15*
J1	K3	XA9	23				XAD 2*
XA9	24	J1	K4				XAD 3*
J1	K5	XA9	25				XAD 4*
XA9	26	J1	K6				XAD 5*
J1	K7	XA9	27				XAD 6*
XA9	28	J1	K8				XAD 7*
J1	K9	XA9	29				XAD 8*
XA9	30	J1	K0				XAD 9*
XA10	1	J3	K3				XA10+5-1
XA10	2	J3	K6				XA10+5-2
XA10	3	XA10	21				XA10 GND
XA10	21	XA10	29				XA10 GND
XA10	29	XA10	48				XA10 GND
J3	K7	XA11	1				XA11+5-1

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
J3	K0	XA11	91				XA11+5-91
XA11	87	XA11	88				XA11+5V
XA11	88	XA11	29				XA11+5V
XA11	29	XA11	86				XA11+5V
XA11	86	XA11	69				XA11+5V
XA11	69	XA11	2				XA11+5V
XA11	2	XA11	50				XA11+5V
XA11	79	XA11	33				XA11-9V
XA11	33	XA11	31				XA11-9V
XA11	31	XA11	11				XA11-9V
XA11	11	XA11	52				XA11-9V
XA11	3	XA11	25				XA11 GND
XA11	25	XA11	23				XA11 GND
XA11	23	XA12	19				XA11 GND
XA12	1	J3	K8				XA12+5-1
XA12	88	XA12	2				XA12+5V
XA12	2	XA12	87				XA12+5V
XA12	87	XA12	86				XA12+5V
XA12	86	XA12	50				XA12+5V
XA12	50	XA12	29				XA12+5V
XA12	29	XA12	69				XA12+5V
XA12	33	XA12	31				XA12-9V
XA12	31	XA12	52				XA12-9V
XA12	52	XA12	79				XA12-9V
XA12	79	XA12	11				XA12-9V
XA12	3	XA12	25				XA12 GND
XA12	25	XA12	23				XA12 GND
XA12	23	XA12	19				XA12 GND
XA12	19	XA12	45				XA12 GND
XA13	1	J3	K9				XA13+5-1
XA13	69	XA13	29				XA13+5V
XA13	29	XA13	88				XA13+5V
XA13	88	XA13	87				XA13+5V
XA13	87	XA13	86				XA13+5V
XA13	86	XA13	2				XA13+5V
XA13	2	XA13	50				XA13+5V
XA13	52	XA13	31				XA13-9V
XA13	31	XA13	11				XA13-9V
XA13	11	XA13	79				XA13-9V
XA13	79	XA13	33				XA13-9V
XA13	3	XA13	28				XA13 GND
XA13	28	XA13	25				XA13 GND
XA13	25	XA13	23				XA13 GND
XA13	23	XA13	19				XA13 GND
XA14	91	J4	P4				XA14+5-91

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
J4	P5	XA14	92				XA14+5-92
XA14	50	XA14	2				XA14+5V
XA14	2	XA14	87				XA14+5V
XA14	87	XA14	69				XA14+5V
XA14	69	XA14	86				XA14+5V
XA14	86	XA14	29				XA14+5V
XA14	29	XA14	88				XA14+5V
XA14	11	XA14	33				XA14-9V
XA14	33	XA14	31				XA14-9V
XA14	31	XA14	52				XA14-9V
XA14	52	XA14	79				XA14-9V
XA14	3	XA14	19				XA14 GND
XA14	19	XA14	23				XA14 GND
XA14	23	XA14	28				XA14 GND
XA14	28	XA14	25				XA14 GND
XA14	25	XA14	45				XA14 GND
J4	P6	XA15	91				XA15+5-91
J4	P7	XA15	92				XA15+5-92
XA15	29	XA15	88				XA15+5V
XA15	88	XA15	69				XA15+5V
XA15	69	XA15	50				XA15+5V
XA15	50	XA15	86				XA15+5V
XA15	86	XA15	87				XA15+5V
XA15	87	XA15	2				XA15+5V
XA5	52	XA15	79				XA15-9V
XA5	79	XA15	31				XA15-9V
XA5	31	XA15	33				XA15-9V
XA15	33	XA15	11				XA15-9V
XA15	3	XA15	25				XA15 GND
XA15	25	XA15	23				XA15 GND
XA15	23	XA15	19				XA15 GND
XA15	19	XA15	21				XA15 GND
XA16	91	J4	P8				XA15+5-91
XA16	92	J5	P4				XA16+5-92
XA16	69	XA16	2				XA16+5V
XA16	2	XA16	87				XA16+5V
XA16	87	XA16	86				XA16+5V
XA16	86	XA16	29				XA16+5V
XA16	29	XA16	88				XA16+5V
XA16	88	XA16	50				XA16+5V
XA16	33	XA16	52				XA16-9V
XA16	52	XA16	11				XA16-9V
XA16	11	XA16	79				XA16-9V
XA16	79	XA16	31				XA16-9V
XA16	3	XA16	45				XA16 GND

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA16	45	XA16	25				XA16 GND
XA16	25	XA16	23				XA16 GND
XA16	23	XA16	19				XA16 GND
XA16	19	XA16	21				XA16 GND
J5	P5	XA17	91				XA17+5-91
J5	P6	XA17	92				XA17+5-92
XA17	29	XA17	88				XA17+5V
XA17	88	XA17	50				XA17+5V
XA17	50	XA17	87				XA17+5V
XA17	87	XA17	86				XA17+5V
XA17	86	XA17	2				XA17+5V
XA17	2	XA17	69				XA17+5V
XA17	79	XA17	33				XA17-9V
XA17	33	XA17	11				XA17-9V
XA17	11	XA17	31				XA17-9V
XA17	31	XA17	52				XA17-9V
XA17	3	XA17	21				XA17 GND
XA17	21	XA17	19				XA17 GND
XA17	19	XA17	23				XA17 GND
XA17	23	XA17	25				XA17 GND
XA17	25	XA17	28				XA17 GND
XA18	91	J5	P7				XA18+5-91
J5	P8	XA18	92				XA18+5-92
XA18	88	XA18	2				XA18+5V
XA18	2	XA18	29				XA18+5V
XA18	29	XA18	87				XA18+5V
XA18	87	XA18	86				XA18+5V
XA18	86	XA18	50				XA18+5V
XA18	50	XA18	69				XA18+5V
XA18	11	XA18	52				XA18-9V
XA18	52	XA18	31				XA18-9V
XA18	31	XA18	33				XA18-9V
XA18	33	XA18	79				XA18-9V
XA18	23	XA18	21				XA18 GND
XA18	21	XA18	19				XA18 GND
XA18	19	XA18	28				XA18 GND
XA18	28	XA18	25				XA18 GND
XA18	25	XA18	45				XA18 GND
XA18	45	XA18	3				XA18 GND
XA19	19	J3	K4				XA19-15V-1(-)
XA19	19	XA19	20				XA19-15V-1(-)
XA19	20	J3	K5				XA19-15V-2
XA19	71	XA19	72				XA19-15V(+)
XA22	3	XA22	75				XA22 GND
XA22	75	XA22	80				XA22 GND
XA22	80	XA22	84				XA22 GND

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA22	84	XA22	88				XA22 GND
XA23	3	XA23	76				XA23 GND
XA23	76	XA23	80				XA23 GND
XA23	80	XA23	84				XA23 GND
XA23	84	XA23	88				XA23 GND
XA24	3	XA24	75				XA24 GND
XA24	75	XA24	76				XA24 GND
XA24	76	XA24	80				XA24 GND
XA24	80	XA24	84				XA24 GND
XA24	84	XA24	88				XA24 GND
XA27	27	XA27	48				XA27 GND
XA27	48	XA27	21				XA27 GND
XA27	21	XA27	3				XA27 GND
XA28	2	XA28	29				XA28+5V
XA28	29	XA28	88				XA28+5V
XA28	88	XA28	69				XA28+5V
XA28	69	XA28	87				XA28+5V
XA28	87	XA28	50				XA28+5V
XA28	50	XA28	86				XA28+5V
XA28	31	XA28	79				XA28-9V
XA28	79	XA28	33				XA28-9V
XA28	33	XA28	11				XA28-9V
XA28	11	XA28	52				XA28-9V
XA28	3	XA28	25				XA28 GND
XA28	25	XA28	23				XA28 GND
XA29	86	XA29	88				XA29+5V
XA29	88	XA29	69				XA29+5V
XA29	69	XA29	50				XA29+5V
XA29	50	XA29	87				XA29+5V
XA29	87	XA29	29				XA29+5V
XA29	29	XA29	2				XA29+5V
XA29	11	XA29	33				XA29-9V
XA29	33	XA29	79				XA29-9V
XA29	79	XA29	52				XA29-9V
XA29	52	XA29	31				XA29-9V
XA29	3	XA29	23				XA29 GND
XA29	23	XA29	25				XA29 GND
XA29	25	XA29	45				XA29 GND
XA30	69	XA30	2				XA30+5V
XA30	2	XA30	87				XA20+5V
XA30	87	XA30	88				XA30+5V
XA30	88	XA30	50				XA30+5V
XA30	50	XA30	29				XA30+5V
XA30	29	XA30	86				XA30+5V
XA30	31	XA30	79				XA30-9V
XA30	79	XA30	11				XA30-9V

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA30	11	XA30	33				XA30-9V
XA30	33	XA30	52				XA30-9V
XA30	3	XA30	28				XA30 GND
XA30	28	XA30	25				XA30 GND
XA30	25	XA30	23				X30 GND
XA31	87	XA31	88				XA31+5V
XA31	88	XA31	91				XA31+5V
XA31	33	XA31	11				XA31-9V
XA31	11	XA31	79				XA31-9V
XA31	79	XA31	52				XA31-9V
XA31	52	XA31	31				XA31-9V
XA31	3	XA31	69				XA31 GND
XA31	69	XA31	50				XA31 GND
XA31	50	XA31	29				XA31 GND
XA31	29	XA31	86				XA31 GND
XA31	86	XA31	28				XA31 GND
XA31	28	XA31	21				XA31 GND
XA31	21	XA31	23				XA31 GND
XA31	23	XA31	25				XA31 GND
XA31	25	XA31	45				XA31 GND
XA32	69	XA32	50				XA32+5V
XA32	50	XA32	2				XA32+5V
XA32	2	XA32	29				XA32+5V
XA32	29	XA32	86				XA32+5V
XA32	86	XA32	87				XA32+5V
XA32	87	XA32	88				XA32+5V
XA32	79	XA32	52				XA32-9V
XA32	52	XA32	31				XA32-9V
XA32	31	XA32	11				XA32-9V
XA32	11	XA32	33				XA32-9V
XA32	3	XA32	28				XA32 GND
XA32	28	XA32	23				XA32 GND
XA32	23	XA32	25				XA32 GND
XA32	25	XA32	45				XA32 GND
XA33	2	XA33	29				XA33+5V
XA33	29	XA33	86				XA33+5V
XA33	86	XA33	50				XA33+5V
XA33	50	XA33	88				XA33+5V
XA33	88	XA33	87				XA33+5V
XA33	87	XA33	69				XA33+5V
XA33	31	XA33	79				XA33-9V
XA33	79	XA33	52				XA33-9V
XA33	52	XA33	33				XA33-9V
XA33	33	XA33	11				XA33-9V
XA33	3	XA33	21				XA33 GND

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA33	21	XA33	25				XA33 GND
XA33	25	XA33	23				XA33 GND
XA34	29	XA34	88				XA34+5V
XA34	88	XA34	2				XA34+5V
XA34	2	XA34	86				XA34+5V
XA34	86	XA34	87				XA34+5V
XA34	87	XA34	69				XA34+5V
XA34	69	XA34	50				XA34+5V
XA34	11	XA34	31				XA34-9V
XA34	31	XA34	79				XA34-9V
XA34	79	XA34	52				XA34-9V
XA34	52	XA34	33				XA34-9V
XA34	3	XA34	45				XA34 GND
XA34	45	XA34	23				XA34 GND
XA34	23	XA34	25				XA34 GND
XA34	25	XA34	21				XA34 GND
XA35	86	XA35	29				XA35+5V
XA35	29	XA35	2				XA35+5V
XA35	2	XA35	69				XA35+5V
XA35	69	XA35	50				XA35+5V
XA35	50	XA35	87				XA35+5V
XA35	87	XA35	88				XA35+5V
XA35	11	XA35	52				XA35-9V
XA35	52	XA35	33				XA35-9V
XA35	33	XA35	31				XA35-9V
XA35	31	XA35	79				XA35-9V
XA35	3	XA35	25				XA35 GND
XA35	25	XA35	23				XA35 GND
XA35	23	XA35	21				XA35 GND
XA35	21	XA35	28				XA35 GND
XA36	81	XA36	88				XA36+5V
XA36	88	XA36	29				XA36+5V
XA36	29	XA36	86				XA36+5V
XA36	86	XA36	2				XA36+5V
XA36	2	XA36	69				XA36+5V
XA36	69	XA36	50				XA36+5V
XA36	31	XA36	52				XA36-9V
XA36	52	XA36	79				XA36-9V
XA36	79	XA36	33				XA36-9V
XA36	33	XA36	11				XA36-9V
XA36	3	XA36	45				XA36 GND
XA36	45	XA36	28				XA36 GND
XA36	28	XA36	25				XA36 GND
XA36	25	XA36	23				XA36 GND
XA36	23	XA36	21				XA36 GND

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA7	11	XA2	46				OL 1*
XA2	45	XA8	65				OL 4*
XA8	59	XA2	44				IL 4*
XA3	41	XA7	17				15l 1*
XA7	21	XA3	70				15R 1*
XA2	43	XA8	57				2L 4*
XA8	55	XA2	47				3L 4*
XA21	5	XA20	54				500 KHZ
XA21	59	XA20	83				INT DMP*
XA2	14	XA8	7				INT 0*
XA21	39	XA8	34				INT 1*
XA21	40	XA8	32				INT 2*
XA2	37	XA8	31				INT 3*
XA21	35	XA6	67				INT 4*
XA21	26	XA8	25				INT 6*
XA21	31	XA26	27				PR*
XA19	9	XA19	3				ANAL 2 SIG
XA19	5	XA19	1				ANAL 3 SIG
XA5	29	XA26	52				I/O 12*
XA20	73	XA26	49				I/O 13*
XA20	50	XA6	87				CFLG 15
XA20	49	XA6	53				CFLG 14
XA20	48	XA6	86				CFLG 13
XA20	47	XA6	78				CFLG 12
XA20	46	XA6	88				CFLG 11
XA20	45	XA6	6				CFLG 10
XA20	44	XA6	74				CFLG 9
XA20	38	XA6	65				CFLG 8
XA20	37	XA6	42				CFLG 7
XA20	36	XA6	52				CFLG 6
XA20	35	XA6	8				CFLG 4
XA20	34	XA6	16				CFLG 3
XA20	32	XA26	24				CFLG 1
XA20	31	XA26	26				CFLG 0
XA20	30	XA6	81				FLG 15
XA20	29	XA6	44				FLG 14
XA20	27	XA6	83				FLG 12
XA20	26	XA6	84				FLG 11
XA20	25	XA6	85				FLG 10
XA20	24	XA6	80				FLG 9
XA20	23	XA6	35				FLG 8
XA20	22	XA6	43				FLG 7
XA20	21	XA6	41				FLG 6
XA20	20	XA6	9				FLG 4
XA20	19	XA6	10				FLG 3

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
XA20	18	XA6	68				FLG 2
XA20	17	XA6	38				FLG 1
XA20	16	XA6	5				FLG 0
XA26	3	XA26	9				XA26 GND
XA21	7	XA26	8				IO A5*
XA26	9	XA26	17				XA26 GND
XA21	34	XA26	10				IO A3*
XA26	11	XA21	8				IO A4*
XA21	9	XA26	12				IO A6*
XA26	14	XA4	73				IO A2*
XA26	16	XA21	36				IO A1*
XA21	12	XA26	21				IO M*
XA21	11	XA26	22				IO S*
XA26	24	XA6	40				CFLG 1
XA26	25	XA20	16				FLG 0
XA20	26	XA6	30				CFLG 0
XA21	26	XA26	28				INT 6*
XA5	36	XA26	47				IO 15*
XA5	24	XA26	49				IO 13*
XA26	50	XA20	75				IO 14*
XA21	24	XA26	51				IO 11*
							IO 12*
XA26	53	XA21	22				IO 9*
XA5	64	XA26	54				IO 10*
XA26	56	XA19	86				IO 8*
XA4	36	XA26	57				IO 7*
XA4	24	XA26	59				IO 5*
XA26	60	XA44	31				IO 6*
XA19	77	XA26	61				IO 3*
XA26	62	XA19	81				IO 4*
XA21	20	XA26	63				IO 1*
XA26	64	XA4	64				IO 2*
XA21	17	XA26	66				IO 0*
XA26	67	J2	P4				-RDY PRCD
XA26	68	J2	P3				+RDY PRCD
XA26	69	J2	P9				+MODE IMR
XA26	70	J2	P0				-MODE IMR
XA26	73	J2	P6				-PRCD RDY
XA26	74	J2	P5				+PRCD RDY
XA26	75	J2	P1				+NFC CLOK
XA26	76	J2	P2				-NFC CLOK
XA26	83	J2	M9				+DFC DATA
XA26	84	J2	M0				-DFC DATA
XA26	85	J2	P8				-IMR MODE
XA26	86	J2	P7				+IMR MODE

* Part of Instruction Word

Contact Assembly A37 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
J5	K0	XA8	26				INT 4*
J5	C4	XA6	82				FLG 13
XA6	G7	XA8	63				INT 4*
XA21	41	XA20	88				INT DMP
							AI 0
XA26	55	J2	C0				SI CLK OUT
XA26	72	J2	D0				SI CLK IN
XA4	80	XA26	18				IO A0*
XA20	28	XA6	82				FLG 13
J2	M3	XA21	88				DT CLOCK
J2	M4	XA21	87				DT CLOCK*
J2	M5	XA21	83				DT DATA
J2	M6	XA21	84				DT DATA*
J2	K9	XA21	81				DT MOD
J2	K0	XA21	82				DT MOD*
J2	M8	XA21	86				DT STROBE*
J2	M7	XA21	85				DT STROBE
XA8	26	XA8	63				INT 4*
XA5	31	XA26	50				IO 14*
XA26	47	XA20	77				IO 15*
XA4	38	XA21	31				PR*
XA22	77	XA32	27				SPAD 11
XA19	19	XA19	20				-15 VDC
XA19	71	XA19	72				+15 VDC
XA20	33	XA6	18				CFLG 5
XA22	53	XA22	56				SPIN 3

* Part of Instruction Word

Special Purpose Cable Assembly W1 Wire List

FROM CONNECTOR		TO CONNECTOR		WIRE			
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	FUNCTION/REMARKS
P4	P1	J6	1	24 AWG	WHT	8"	IO0
P4	N1	J6	2	24 AWG	BLK	8"	IO0 RTN
P4	P2	J6	3	24 AWG	WHT	8"	IO1
P4	N2	J6	4	24 AWG	BLK	8"	IO1 RTN
P4	A3	J6	5	24 AWG	WHT	8"	IO2
P4	B3	J6	6	24 AWG	BLK	8"	IO2 RTN
P4	A4	J6	7	24 AWG	WHT	8"	IO3
P4	B4	J6	8	24 AWG	BLK	8"	IO3 RTN
P4	A5	J6	9	24 AWG	WHT	8"	IO4
P4	B5	J6	10	24 AWG	BLK	8"	IO4 RTN
P4	A6	J6	11	24 AWG	WHT	8"	IO5
P4	B6	J6	12	24 AWG	BLK	8"	IO5 RTN
P4	A7	J6	13	24 AWG	WHT	8"	IO6
P4	B7	J6	14	24 AWG	BLK	8"	IO6 RTN
P4	A8	J6	15	24 AWG	WHT	8"	IO7
P4	B8	J6	16	24 AWG	BLK	8"	IO7 RTN
P4	A9	J6	17	24 AWG	WHT	8"	IO8
P4	B9	J6	18	24 AWG	BLK	8"	IO8 RTN
P4	A0	J6	19	24 AWG	WHT	8"	IO9
P4	B0	J6	20	24 AWG	BLK	8"	IO9 RTN
P4	C1	J6	21	24 AWG	WHT	8"	IO10
P4	D1	J6	22	24 AWG	BLK	8"	IO10 RTN
P4	C2	J6	23	24 AWG	WHT	8"	IO11
P4	D2	J6	24	24 AWG	BLK	8"	IO14 RTN
P4	C3	J6	25	24 AWG	WHT	8"	IO12
P4	D3	J6	26	24 AWG	BLK	8"	IO12 RTN
P4	C4	J6	27	24 AWG	WHT	8"	IO13
P4	D4	J6	28	24 AWG	BLK	8"	IO13 RTN
P4	C5	J6	29	24 AWG	WHT	8"	IO14
P4	D5	J6	30	24 AWG	BLK	8"	IO14 RTN
P4	C6	J6	31	24 AWG	WHT	8"	IO15
P4	D6	J6	32	24 AWG	BLK	8"	IO15 RTN
P4	C7	J6	33	24 AWG	WHT	8"	IOA0
P4	D7	J6	34	24 AWG	BLK	8"	IOA0
P4	C8	J6	35	24 AWG	WHT	8"	IOA1
P4	D8	J6	36	24 AWG	BLK	8"	IOA1 RTN
P4	C9	J6	37	24 AWG	WHT	8"	IOA2
P4	D9	J6	38	24 AWG	BLK	8"	IOA2 RTN
P4	C0	J6	39	24 AWG	WHT	8"	IOA3
P4	D0	J6	40	24 AWG	BLK	8"	IOA3 RTN
P4	E1	J6	41	24 AWG	WHT	8"	IOA4
P4	F1	J6	42	24 AWG	BLK	8"	IOA4 RTN
P4	E2	J6	43	24 AWG	WHT	8"	IOA5
P4	F2	J6	44	24 AWG	BLK	8"	IOA5 RTN

* Part of Instruction Word

Special Purpose Cable Assembly W1 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
P4	E3	J6	45	24 AWG	WHT	8"	IOA6
P4	F3	J6	46	24 AWG	BLK	8"	IOA6 RTN
P4	E7	J6	47	24 AWG	WHT	8"	IOA7
P4	G8	J6	48	24 AWG	BLK	8"	IOA7 RTN
P4	E8	J6	49	24 AWG	WHT	8"	IOS
P4	F8	J6	50	24 AWG	BLK	8"	IOS RTN
P4	E9	J6	51	24 AWG	WHT	8"	IOM
P4	F9	J6	52	24 AWG	BLK	8"	IOM RTN
P4	E0	J6	53	24 AWG	WHT	8"	PR
P4	F0	J6	54	24 AWG	BLK	8"	PR RTN
P4	P4	J6	55	24 AWG	RED	8"	+5VDC
P4	P5	J6	56	24 AWG	RED	8"	+5VDC
P4	P6	J6	57	24 AWG	RED	8"	+5VDC
P4	P7	J6	58	24 AWG	RED	8"	+5VDC
P4	P9	J6	59	24 AWG	WHT	8"	AGC OUT
P4	N9	J6	60	24 AWG	BLK	8"	AGC OUT RTN
		J6	61	24 AWG	BLK	4"	SHIELD
P4	E6	J6	63	24 AWG	WHT	8"	PCCNL
P4	G9	J6	64	24 AWG	BLK	8"	PCCNL RTN
		J6	65	24 AWG	BLK	4"	SHIELD
P4	A1						KEY
P4	A2						KEY
P4	B1						KEY
P4	B2						KEY

* Part of Instruction Word

Special Purpose Cable Assembly W2 Wire List

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
P5	A1	J3	1	24 AWG	WHT	10"	FLG0
P5	B1	J3	2	24 AWG	BLK	10"	FLG0 RTN
P5	A2	J3	3	24 AWG	WHT	10"	FLG1
P5	B2	J3	4	24 AWG	BLK	10"	FLG1 RTN
P5	A3	J3	5	24 AWG	WHT	10"	FLG2
P5	B3	J3	6	24 AWG	BLK	10"	FLG2 RTN
P5	A4	J3	7	24 AWG	WHT	10"	FLG3
P5	B4	J3	8	24 AWG	BLK	10"	FLG3 RTN
P5	A5	J3	9	24 AWG	WHT	10"	FLG4
P5	B5	J3	10	24 AWG	BLK	10"	FLG4 RTN
P5	A6	J3	11	24 AWG	WHT	10"	FLG5
P5	B6	J3	19	24 AWG	BLK	10"	FLG5 RTN
P5	A7	J3	13	24 AWG	WHT	10"	FLG6
P5	B7	J3	14	24 AWG	BLK	10"	FLG6 RTN
P5	A8	J3	15	24 AWG	WHT	10"	FLG7
P5	B8	J3	16	24 AWG	BLK	10"	FLG7 RTN
P5	P9	J3	17	24 AWG	WHT	10"	FLG8
P5	N9	J3	18	24 AWG	BLK	10"	FLG8 RTN
P5	P0	J3	12	24 AWG	WHT	10"	FLG9
P5	N0	J3	20	24 AWG	BLK	10"	FLG9 RTN
P5	C1	J3	21	24 AWG	WHT	10"	FLG10
P5	D1	J3	22	24 AWG	BLK	10"	FLG10 RTN
P5	C2	J3	23	24 AWG	WHT	10"	FLG11
P5	D2	J3	24	24 AWG	BLK	10"	FLG11 RTN
P5	C3	J3	25	24 AWG	WHT	10"	FLG12
P5	D3	J3	26	24 AWG	BLK	10"	FLG12 RTN
P5	C4	J3	27	24 AWG	WHT	10"	FLG13
P5	D4	J3	28	24 AWG	BLK	10"	FLG13 RTN
P5	C5	J3	29	24 AWG	WHT	10"	FLG14
P5	D5	J3	30	24 AWG	BLK	10"	FLG14 RTN
P5	C6	J3	31	24 AWG	WHT	10"	FLG15
P5	D6	J3	32	24 AWG	BLK	10"	FLG15 RTN
P5	C7	J3	33	24 AWG	WHT	10"	CFLG0
P5	D7	J3	34	24 AWG	BLK	10"	CFLG0
P5	C8	J3	35	24 AWG	WHT	10"	CFLG1
P5	D8	J3	36	24 AWG	BLK	10"	CFLG1 RTN
P5	C9	J3	37	24 AWG	WHT	10"	CFLG2
P5	D9	J3	38	24 AWG	BLK	10"	CFLG2 RTN
P5	C0	J3	39	24 AWG	WHT	10"	CFLG3
P5	D0	J3	40	24 AWG	BLK	10"	CFLG3 RTN
P5	E1	J3	41	24 AWG	WHT	10"	CFLG4
P5	F1	J3	42	24 AWG	BLK	10"	CFLG4 RTN
P5	E2	J3	43	24 AWG	WHT	10"	CFLG5
P5	F2	J3	44	24 AWG	BLK	10"	CFLG5 RTN
P5	E3	J3	45	24 AWG	WHT	10"	CFLG6
P5	F3	J3	46	24 AWG	BLK	10"	CFLG6 RTN

* Part of Instruction Word

Special Purpose Cable Assembly W2 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
P5	E8	J3	47	24 AWG	WHT	10"	CFLG7
P5	F8	J3	57	24 AWG	BLK	10"	CFLG7 RTN
P5	E9	J3	49	24 AWG	WHT	10"	CFLG8
P5	F9	J3	50	24 AWG	BLK	10"	CFLG8 RTN
P5	E0	J3	51	24 AWG	WHT	10"	CFLG9
P5	F0	J3	52	24 AWG	BLK	10"	CFLG9 RTN
P5	K1	J3	53	24 AWG	WHT	10"	CFLG10
P5	L1	J3	54	24 AWG	BLK	10"	CFLG10 RTN
P5	K2	J3	55	24 AWG	WHT	10"	CFLG11
P5	L2	J3	56	24 AWG	BLK	10"	CFLG11 RTN
P5	K3	J3	48	24 AWG	WHT	10"	CFLG12
P5	L3	J3	58	24 AWG	BLK	10"	CFLG12 RTN
P5	K4	J3	59	24 AWG	WHT	10"	CFLG13
P5	L4	J3	60	24 AWG	BLK	10"	CFLG13 RTN
P5	K5	J3	61	24 AWG	WHT	10"	CFLG14
P5	L5	J3	62	24 AWG	BLK	10"	CFLG14 RTN
P5	K6	J3	63	24 AWG	WHT	10"	CFLG15
P5	L6	J3	64	24 AWG	BLK	10"	CFLG15 RTN
P5	K7	J3	65	24 AWG	WHT	10"	INT1
P5	L7	J3	66	24 AWG	BLK	10"	INT1 RTN
P5	K8	J3	67	24 AWG	WHT	10"	INT2
P5	L8	J3	68	24 AWG	BLK	10"	INT2 RTN
P5	K9	J3	69	24 AWG	WHT	10"	INT3
P5	L9	J3	70	24 AWG	BLK	10"	INT3 RTN
P5	K0	J3	71	24 AWG	WHT	10"	INT4
P5	L0	J3	72	24 AWG	BLK	10"	INT4 RTN
P5	M1	J3	73	24 AWG	WHT	10"	INT5
P5	N1	J3	74	24 AWG	BLK	10"	INT5 RTN
P5	M2	J3	75	24 AWG	WHT	10"	INT6
P5	N2	J3	76	24 AWG	BLK	10"	INT6 RTN
P5	M3	J3	77	24 AWG	WHT	10"	INT0
P5	N3	J3	78	24 AWG	BLK	10"	INT0 RTN
P5	P4	J3	79	26 AWG	RED	10"	+5VDC
P5	P5	J3	80	26 AWG	RED	10"	+5VDC
P5	P6	J3	81	26 AWG	RED	10"	+5VDC
P5	P7	J3	82	26 AWG	RED	10"	+5VDC
P5	M4	J3	83	24 AWG	WHT	10"	INHIBIT
P5	N4	J3	84	24 AWG	BLK	10"	INHIBIT RTN
P5		J3	85	24 AWG	BLK	4"	SHIELD
P5		J3	86				N/C
P5		J3	87				N/C
P5		J3	88				N/C
P5		J3	89				N/C
P5		J3	90				N/C
P5		J3	91				N/C
P5		J3	92				N/C

* Part of Instruction Word

Special Purpose Cable Assembly W2 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
P5		J3	93				N/C
P5		J3	94				N/C
P5		J3	95				N/C
P5		J3	96				N/C
P5		J3	97				N/C
P5		J3	98				N/C
P5		J3	99				N/C
P5		J3	100				N/C
P5		A9					KEY
P5		A0					KEY
P5		B9					KEY
P5		B0					KEY

* Part of Instruction Word

Special Purpose Cable Assembly W3 Wire List

FROM CONNECTOR		TO CONNECTOR		WIRE			
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	FUNCTION/REMARKS
P1	A3	J1	1	24 AWG	WHT	10"	RIN0
P1	B3	J1	2	24 AWG	BLK	10"	RIN0 RTN
P1	A4	J1	3	24 AWG	WHT	10"	RIN1
P1	B4	J1	4	24 AWG	BLK	10"	RIN1 RTN
P1	A5	J1	5	24 AWG	WHT	10"	RIN2
P1	B5	J1	6	24 AWG	BLK	10"	RIN2 RTN
P1	A6	J1	7	24 AWG	WHT	10"	RIN3
P1	B6	J1	14	24 AWG	BLK	10"	RIN3 RTN
P1	A7	J1	8	24 AWG	WHT	10"	RIN4
P1	B7	J1	9	24 AWG	BLK	10"	RIN4 RTN
P1	A8	J1	10	24 AWG	WHT	10"	RIN5
P1	B8	J1	11	24 AWG	BLK	10"	RIN5 RTN
P1	A9	J1	12	24 AWG	WHT	10"	RIN6
P1	B9	J1	13	24 AWG	BLK	10"	RIN6 RTN
P1	A0	J1	16	24 AWG	WHT	10"	RIN7
P1	B0	J1	17	24 AWG	BLK	10"	RIN7 RTN
P1	C1	J1	18	24 AWG	WHT	10"	RIN8
P1	D1	J1	19	24 AWG	BLK	10"	RIN8 RTN
P1	C2	J1	20	24 AWG	WHT	10"	RIN9
P1	D2	J1	21	24 AWG	BLK	10"	RIN9 RTN
P1	C3	J1	22	24 AWG	WHT	10"	RIN10
P1	D3	J1	23	24 AWG	BLK	10"	RIN10 RTN
P1	C4	J1	24	24 AWG	WHT	10"	RIN11
P1	D4	J1	15	24 AWG	BLK	10"	RIN11 RTN
P1	C5	J1	25	24 AWG	WHT	10"	RIN12
P1	D5	J1	26	24 AWG	BLK	10"	RIN12 RTN
P1	C6	J1	27	24 AWG	WHT	10"	RIN13
P1	D6	J1	28	24 AWG	BLK	10"	RIN13 RTN
P1	C7	J1	29	24 AWG	WHT	10"	RIN14
P1	D7	J1	30	24 AWG	BLK	10"	RIN14 RTN
P1	C8	J1	31	24 AWG	WHT	10"	RIN15
P1	D8	J1	32	24 AWG	BLK	10"	RIN15 RTN
P1	C9	J1	33	24 AWG	WHT	10"	RIN16
P1	D9	J1	34	24 AWG	BLK	10"	RIN16 RTN
P1	C0	J1	35	24 AWG	WHT	10"	RIN17
P1	D0	J1	36	24 AWG	BLK	10"	RIN17 RTN
P1	E1	J1	37	24 AWG	WHT	10"	RIN18
P1	F1	J1	38	24 AWG	BLK	10"	RIN18 RTN
P1	E2	J1	39	24 AWG	WHT	10"	RIN19
P1	F2	J1	40	24 AWG	BLK	10"	RIN19 RTN
P1	E3	J1	41	24 AWG	WHT	10"	RIN20
P1	F3	J1	42	24 AWG	BLK	10"	RIN20 RTN
P1	E8	J1	43	24 AWG	WHT	10"	RIN21
P1	F8	J1	44	24 AWG	BLK	10"	RIN21 RTN
P1	E9	J1	46	24 AWG	WHT	10"	RIN22
P1	F9	J1	47	24 AWG	BLK	10"	RIN22 RTN

* Part of Instruction Word

Special Purpose Cable Assembly W3 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
P1	E0	J1	48	24 AWG	WHT	10"	RIN23
P1	F0	J1	49	24 AWG	BLK	10"	RIN23 RTN
P1	K1	J1	56	24 AWG	WHT	10"	XAD0
P1	L1	J1	57	24 AWG	BLK	10"	XAD0 RTN
P1	K2	J1	58	24 AWG	WHT	10"	XAD1
P1	L2	J1	59	24 AWG	BLK	10"	XAD1 RTN
P1	K3	J1	60	24 AWG	WHT	10"	XAD2
P1	L3	J1	61	24 AWG	BLK	10"	XAD2 RTN
P1	K4	J1	62	24 AWG	WHT	10"	XAD3
P1	L4	J1	63	24 AWG	BLK	10"	XAD3 RTN
P1	K5	J1	64	24 AWG	WHT	10"	XAD4
P1	L5	J1	65	24 AWG	BLK	10"	XAD4 RTN
P1	K6	J1	67	24 AWG	WHT	10"	XAD5
P1	L6	J1	68	24 AWG	BLK	10"	XAD5 RTN
P1	K7	J1	69	24 AWG	WHT	10"	XAD6
P1	L7	J1	70	24 AWG	BLK	10"	XAD6 RTN
P1	K8	J1	71	24 AWG	WHT	10"	XAD7
P1	L8	J1	72	24 AWG	BLK	10"	XAD7 RTN
P1	K9	J1	73	24 AWG	WHT	10"	XAD8
P1	L9	J1	74	24 AWG	BLK	10"	XAD8 RTN
P1	K0	J1	75	24 AWG	WHT	10"	XAD9
P1	L0	J1	76	24 AWG	BLK	10"	XAD9 RTN
P1	M1	J1	77	24 AWG	WHT	10"	XAD10
P1	N1	J1	78	24 AWG	BLK	10"	XAD10 RTN
P1	M2	J1	79	24 AWG	WHT	10"	XAD11
P1	N2	J1	80	24 AWG	BLK	10"	XAD11 RTN
P1	M3	J1	81	24 AWG	WHT	10"	XAD12
P1	N3	J1	82	24 AWG	BLK	10"	XAD12 RTN
P1	M4	J1	83	24 AWG	WHT	10"	XAD13
P1	N4	J1	84	24 AWG	BLK	10"	XAD13 RTN
P1	M5	J1	86	24 AWG	WHT	10"	XAD14
P1	N5	J1	87	24 AWG	BLK	10"	XAD14 RTN
P1	M6	J1	88	24 AWG	WHT	10"	XAD15
P1	N6	J1	89	24 AWG	BLK	10"	XAD15 RTN
P1	M7	J1	90	24 AWG	WHT	10"	DF ENABLE
P1	N7	J1	91	24 AWG	BLK	10"	DF ENABLE RTN
		J1	100	24 AWG	BLK	4"	SHIELD, GND FLYING LEAD
P1	N9	J1					KEY
P1	N0	J1					KEY
P1	P9	J1					KEY
P1	P0	J1					KEY

* Part of Instruction Word

Special Purpose Cable Assembly W4 Wire List

FROM CONNECTOR		TO CONNECTOR		WIRE			
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	FUNCTION/REMARKS
P2	A1	J4	1	24 AWG	WHT	10"	DM0
P2	B1	J4	2	24 AWG	BLK	10"	DM0 RTN
P2	A2	J4	3	24 AWG	WHT	10"	DM1
P2	B2	J4	4	24 AWG	BLK	10"	DM1 RTN
P2	A3	J4	5	24 AWG	WHT	10"	DM2
P2	B3	J4	6	24 AWG	BLK	10"	DM2 RTN
P2	A4	J4	7	24 AWG	WHT	10"	DM3
P2	B4	J4	8	24 AWG	BLK	10"	DM3 RTN
P2	A5	J4	9	24 AWG	WHT	10"	DM4
P2	B5	J4	10	24 AWG	BLK	10"	DM4 RTN
P2	A6	J4	11	24 AWG	WHT	10"	DM5
P2	B6	J4	12	24 AWG	BLK	10"	DM5 RTN
P2	A7	J4	13	24 AWG	WHT	10"	DM6
P2	B7	J4	14	24 AWG	BLK	10"	DM6 RTN
P2	A8	J4	15	24 AWG	WHT	10"	DM7
P2	B8	J4	16	24 AWG	BLK	10"	DM7 RTN
P2	A9	J4	17	24 AWG	WHT	10"	MUX0
P2	B9	J4	18	24 AWG	BLK	10"	MUX0 RTN
P2	A0	J4	19	24 AWG	WHT	10"	MUX1
P2	B0	J4	20	24 AWG	BLK	10"	MUX1 RTN
P2	C1	J4	21	24 AWG	WHT	10"	MUX2
P2	D1	J4	22	24 AWG	BLK	10"	MUX2 RTN
P2	C2	J4	23	24 AWG	WHT	10"	RUNS
P2	D2	J4	24	24 AWG	BLK	10"	RUNS RTN
P2	C3	J4	25	24 AWG	WHT	10"	RUNS
P2	D3	J4	54	24 AWG	BLK	10"	RUNS RTN
P2	C4	J4	26	24 AWG	WHT	10"	SGLST
P2	D4	J4	27	24 AWG	BLK	10"	SGLST RTN
P2	C5	J4	28	24 AWG	WHT	10"	SGLST
P2	D5	J4	55	24 AWG	BLK	10"	SGLST RTN
P2	C6	J4	29	24 AWG	WHT	10"	HALT
P2	D6	J4	30	24 AWG	BLK	10"	HALT RTN
P2	C7	J4	31	24 AWG	WHT	10"	BRKPT
P2	D7	J4	32	24 AWG	BLK	10"	BRKPT RTN
P2	C8	J4	33	24 AWG	WHT	10"	PRES
P2	D8	J4	34	24 AWG	BLK	10"	PRES RTN
P2	C9	J4	35	24 AWG	WHT	10"	PRES
P2	D9	J4	56	24 AWG	BLK	10"	PRES RTN
P2	E1	J4	36	24 AWG	WHT	10"	COM1
P2	E2	J4	37	24 AWG	WHT	10"	LASW0
P2	E3	J4	38	24 AWG	WHT	10"	LASW1
P2	E4	J4	39	24 AWG	WHT	10"	LASW2
P2	E5	J4	40	24 AWG	WHT	10"	ASW3
P2	E6	J4	41	24 AWG	WHT	10"	ASW4
P2	E7	J4	42	24 AWG	WHT	10"	ASW5
P2	E8	J4	43	24 AWG	WHT	10"	ASW6

* Part of Instruction Word

Special Purpose Cable Assembly W4 Wire List (Continued)

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
P2	E9	J4	44	24 AWG	WHT	10"	ASW7
P2	E0	J4	45	24 AWG	WHT	10"	ASW8
P2	K1	J4	46	24 AWG	WHT	10"	COM2
P2	K2	J4	47	24 AWG	WHT	10"	ASW9
P2	K3	J4	48	24 AWG	WHT	10"	ASW10
P2	K4	J4	49	24 AWG	WHT	10"	ASW11
P2	K5	J4	50	24 AWG	WHT	10"	ASW12
P2	K6	J4	51	24 AWG	WHT	10"	ASW13
P2	K7	J4	52	24 AWG	WHT	10"	ASW14
P2	K8	J4	53	24 AWG	WHT	10"	ASW15
		J4	65	24 AWG	BLK	4"	SHIELD FLNG LOAD
P2	L1	J2	1	24 AWG	BLK	10"	GND
P2	L2	J2	2	24 AWG	BLK	10"	GND
P2	K9	J2	3	24 AWG	WHT	10"	DT MOD
P2	K0	J2	4	24 AWG	BLK	10"	DT MOD
P2	M3	J2	5	24 AWG	WHT	10"	DT CLOCK
P2	M4	J2	6	24 AWG	BLK	10"	DT CLOCK
P2	M5	J2	7	24 AWG	WHT	10"	DT DATA
P2	M6	J2	8	24 AWG	BLK	10"	DT DATA
P2	M7	J2	9	24 AWG	WHT	10"	DT STROBE
P2	M8	J2	10	24 AWG	BLK	10"	DT STROBE
P2		J2	22	24 AWG	BLK	4"	SHIELD GN
P2	M9	J5	10	24 AWG	WHT	7"	+DFC DATA
P2	M0	J5	11	24 AWG	BLK	7"	-DFC DATA
P2	P1	J5	12	24 AWG	WHT	7"	+NFC CLOK
P2	P2	J5	13	24 AWG	BLK	7"	-NFC CLOK
P2	P3	J5	14	24 AWG	WHT	7"	+RDY PRCD
P2	P4	J5	15	24 AWG	BLK	7"	-RDY PRCD
P2	P5	J5	16	24 AWG	WHT	7"	+PRCD RDY
P2	P6	J5	17	24 AWG	BLK	7"	-PRCD RDY
P2	P7	J5	18	24 AWG	WHT	7"	+IMR MODE
P2	P8	J5	19	24 AWG	BLK	7"	-IMR MODE
P2	P9	J5	20	24 AWG	WHT	7"	+MODE IMR
P2	P0	J5	21	24 AWG	BLK	7"	-MODE IMR
		J5	22	24 AWG	BLK	7"	SHIELD GN
		J5	1	24 AWG	WHT	12"	OVER-TEMP
		J5	2	24 AWG	BLK	12"	OVER-TEMPTN
P2	C0	J5	8	24 AWG	WHT	7"	SI CLK IN
P2	D0	J5	9	24 AWG	WHT	7"	SI CLK OU
P2	M1						KEY
P2	M2						KEY
P2	N1						KEY
P2	N2						KEY

* Part of Instruction Word

Special Purpose Cable Assembly W5 Wire List

FROM CONNECTOR		TO CONNECTOR		WIRE			FUNCTION/REMARKS
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	
J11	A	B1	01	24 AWG	GRY	48"	115V, 400 HZ 01 FAN
J11	D	M1	NEUT	24 AWG	GRY	48"	115V, 400 HZ NEUTRAL M1
J11	E	J11	F	24 AWG	WHT	2"	INTERLOCK
J11	H	A37	E1	24 AWG	BLK	5"	SHIELD
J11	B	B1	02	24 AWG	GRY	48"	400 HZ 02 FAN
J11	C	B1	03	24 AWG	GRY	48"	400 HZ 03 FAN

* Part of Instruction Word

Special Purpose Cable Assembly W6 Wire List

FROM CONNECTOR		TO CONNECTOR		WIRE			
REF DES	PIN	REF DES	PIN	SIZE	COLOR	LENGTH	FUNCTION/REMARKS
J12	A	E14		16 AWG	RED	31.0	+15VDC
J12	B	E15		16 AWG	VIO	31.0	-15VDC
J12	C	E2	LUG	16 AWG	BLK	12.0	±15VDC RTN
J12	D						SPARE
J12	E						SPARE
J12	F	E8	LUG	16 AWG	RED	18.0	+5VDC
J12	G	E5	LUG	16 AWG	RED	23.0	+5VDC
J12	H	E2	LUG	16 AWG	BLK	12.0	+5VDC RTN
J12	K	E6	LUG	16 AWG	RED	23.0	+5VDC SENSE
J12	L	E3	LUG	16 AWG	RED	23.0	+5VDC
J12	M	E4	LUG	16 AWG	RED	23.0	+5VDC
J12	N	E2	LUG	16 AWG	BLK	12.0	+5VDC RTN
J12	P	E2	LUG	16 AWG	BLK	12.0	+5VDC RTN
J12	R	E4	LUG	16 AWG	RED	23.0	+5VDC SENSE
J12	S	E16			VIO	31.0	-10VDC
J12	T	E2	LUG	16 AWG	BLK	12.0	+10VDC RTN
J12	U		LUG	16 AWG			SPARE
J12	X	GND	LUG	16 AWG	BLK	6.0	SHIELD GROUND
J12	W	E2	LUG	16 AWG	BLK	12.0	+5VDC RTN
J12	J	E2	LUG	16 AWG	BLK	12.0	+5VDC RTN
J12	V	E9	LUG	16 AWG	RED	16.0	+5VDC
J12	E6	E7	LUG	16 AWG	RED	15.0	
XA18	11-12	E16		20	VIO	22.0	-10VDC
XA36	11-12	E16		20	VIO	22.0	-10VDC
XA19	71	E14		20	RED	29.0	+15VDC
XA19	19	E15		20	VIO	24.0	-15VDC

* Part of Instruction Word

GLOSSARY

Mnemonic	Definition	Comments
A=B	Input Word A Equals Input Word B	ALU CCA output which is high when the ALUs are configured for subtraction, and the two 16-bit input data words are equal.
A/D CLOCK	Analog-to-Digital Clock	500-Hz clock, derived from servo timing CCA A20, used by servo conversion CCA A19 for converting to integrator output into an equivalent digital value.
A/D DISABLE	Analog-to-Digital Disable	This input, the result of a decode IOA bus input, (a) goes high to disable the A/D converter output servo conversion CCA A19 onto the I/O bus and, (b) goes low to transfer CCA A19 A/D converted data on the I/O bus.
A/D ENABLE	Analog-to-Digital Converter Enable (positive true)	Signal is the direct result of IOA bus decoding. This servo signal interface CCA A21 output is inverted by servo timing CCA A20 to provide a false (low) A/D DISABLE signal. The low A/D DISABLE transfers the A/D converted data (of servo conversion CCA A19) onto the I/O bus.
ADEQ0	Address Equals Zero (positive true)	Signal derived from program count CCAs which halts the digital processor when breakpoint program address is reached.
AI1, AI0	Analog Input Control (positive true)	This 2-bit code, derived from respect 1/0 bus IO5 and IO4 bits, selects one of four DF receiver analog signal inputs.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
ALU	Arithmetic Logic Unit	Circuits on the ALU CCAs which respond to a MODE signal and either 16 different mathematical or 16 different logic operations on two groups of 16-bit data words, according to the command code and MODE signal level.
$\overline{\text{ALUG}}$	ALU Gate (negative true)	Loads 16-bit (ALUO-ALU15) ALU output data onto destination bus (DO-D15).
ALUO-ALU15	Arithmetic Logic Unit Bits 0 - 15 (negative true)	These bits are generated by the ALU circuits as a result of a mathematical or logic operation.
ANALOG 0 SIG, 0 RTN ANALOG 1 SIG, 1 RTN ANALOG 2 SIG, 2 RTN ANALOG 3 SIG, 3 RTN		Four different input signal paths to servo conversion CCA A19. These inputs may be derived from as many as four different DF receivers.
ASC	Antenna Switch Command	Eight-bit data which configures the antenna baseline pair selection of the RF processor.
$\overline{\text{ASWO}}$-$\overline{\text{ASW15}}$	Switched Addressed Input (negative true)	Input to a program counter I/O CCA which controls the digital processor program ROM address under the following conditions: (a) interrupt sequence is activated, and (b) digital processor test set is connected with PRESET switch pressed.
ASO-AS3	ALU Function Select Bits 0 - 3 (positive true)	These four bits determine what arithmetic of logic operation are preformed by the digital processor ALU CCAs.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
BRKPT	Breakpoint (negative true)	Command derived from the digital processor test set which activates those circuits that automatically halt the digital processor when the breakpoint address is received.
CARRY	Carry (negative true)	Active output of carry register in response to an ALU CCA mathematical operation which results in a carry bit (CN15) being generated.
CC	Conversion Complete	See CONV COMPLETE.
CFLGO-CFLG15	Clear Flag	Positive signal generated by an external element which clears the digital processor FLG and initiates a data transfer operation.
CN	Carry Input (negative true)	Carry input to ALU circuits. High = carry input, low = no carry input.
CN15	Carry Bit (negative true)	This bit is generated as a result of an ALU mathematical operation overflowing.
CNV	Conversion Pulse (negative true)	This pulse is generated by servo timing CCA A20 to initialize and activate the A/D converter on servo conversion CCA A19.
CONV COMPLETE (CC)	Conversion Complete	The rising leading edge of this signal notifies the digital servo group that the A/D conversion process is concluded, and initiates the integrator track mode of operation.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
CS0-CS3	Chip Select (negative true)	Decoded RAD9 and RAD8 (ROM address) output which selects a group of three ROM chips on a program memory data.
DFC DATA	DFC Data	Serial differential data which are exchanged between the DF control, or communication processor, and the computer.
DLP	Delay Line Preset	Twelve-bit data applied to the RF processor which determines the amount of variable delay to be inserted into an RF signal path to the DF receiver.
DM0-DM7	Multiplexed Data Out	Eight lines onto which digital processor signals are multiplexed and transferred to the digital processor test set.
DT CLOCK	Data Transfer Clock	Clock generated by digital servo group to serial shift DT DATA into the RF processor.
DT DATA	Data Transfer Data	Serial data which is transferred from the digital servo group to the RF processor. This data contains the 12 DLP bits and the 12 ASC bits.
DT MOD	Data Transfer Modulation	Variable rate signal which alternates selection of two baseline DF antennas for use by the DF receiver. This signal rate is determined by IT0 and IT1.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
DT STROBE	Data Transfer Strobe	Signal generated by the digital servo group to load serially transferred DT data into decoders on the RF processor.
DO-D15	Destination Bus (negative true)	Sixteen-bit bus used for internal transfer of digital processor information from the ALU CCAs to a storage element.
EXEC	Positive Gate	Activates the execution phase of the digital processor instruction cycle.
Firmware		Any program permanently inscribed into PROMs. For example, the DF control, communication processor, and receiver control process data according to preprogrammed PROM instructions, or "firmware."
FLGO-FLG15	Flags	Line which notifies the digital processor of an external element's readiness to exchange data via the 1/0 bus. The external element acknowledges by clearing the flag prior to the data exchange.
F15	Fault or Flag 15 Cleared	Flag 15 is a cleared (low) as a result if a detected digital processor failure. This signal provides a digital processor test set or system diagnostic fault indication.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
$\overline{\text{HALT}}$	Halt (negative true)	This input from the digital processor test set causes the digital processor to stop executing its instructions.
$\overline{\text{HSROM}}$	High-Speed ROM Command (negative true)	This command from the high-speed ROM causes processor timing CCA A8 to provide a short, high speed instruction cycle.
I/O BUS	Input/ OutPut Bus (Bits IO0-I05) (negative true)	Transfers data to and from the digital processor.
ID0, ID1	Integrator Dump Bits (negative true)	This code derived from respective I/O bus IO2 and IO3 bits, controls time frame (d). This time frame (INT DUMP) allows the integrator of servo conversion CCA A19 to discharge.
IMR MODE	Input Mode Request Mode	This differential signal is controlled by the DF control or the communication processor. High + line = request to the computer to interrupt for message transfer. Low + line = no message.
INB0-INB23	Buffer Instruction output	Twenty-four-bit output of ROM buffers resulting from IN0-IN23 input from internal program ROMs or external signal processor test set diagnostic ROMs.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
INT DUMP, INT DUMP	Integrator Dump	INT DUMP is a positive gate which discharges the integrator on servo conversion CCA A19. The positive edge of this signal generates DT STROBE. The negative (leading) edge of the INT DUMP signal clocks a flip-flop to generate DT MOD.
INT MON SIG	Integral Signal Monitoring	Provides a test sample of the integrator output (ramp) waveform on servo conversion CCA A19.
INT0-INT7	Interrupt	Active low signal which usually works in conjunction with FLG signals. This signal causes the digital processor to branch to a program instruction set which is unique to the external element generating the interrupt signal.
IN0-IN23	Instruction Bits 0-23	Positive true 24-bit output of digital processor program ROMs in response to the RAD0-RAD15 input. This input is applied to the ROM buffers.
I/O	Input/Output Instruction (positive true)	This output, decoded by instruction decoder CCA A7, defines an I/O class of distinction.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
IOA	Input/Output Address (negative true)	Eight-bit digital processor that determines which interface element exchanges data on the I/O bus, or defines the data on the I/O bus as information or commands. In addition, the IOA bus may be used by the digital processor to directly command an interface element.
IOACL	I/O Address Clock (negative true)	Loads the digital processor destination bus data D0-D7) onto the IOA0-IOA7 input/output address bus as well as into the IOA register.
$\overline{\text{IOAG}}$	Input/Output Address Gate (negative true)	Loads data in the IOA registers onto the digital processor source bus (S0-S7).
IOCL	Input/Output Clock (negative)	Loads data from the digital processor destination bus into the I/O registers.
IOG	Input/Output Gate (negative)	Loads data in I/O registers onto the digital processor source bus (S0-S15).
IOM, $\overline{\text{IOM}}$	Input/Output Mode	IOM high or IOM low defines digital processor output I/O operation. IOM low or IOM high defines digital processor input I/O operation.
IOS	Input/Output Strobe	Negative strobe sometimes used by the digital processor to transfer data or execute a command as defined by the IOA bus .

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
IRC	Interrupt Clock	Clock pulse from flagjump logic CCA A6 which sets or clears the interrupt latch, depending on the state of the IR6 bit.
$\overline{\text{IRCL}}$	Interrupt Return Register Clock (negative)	Loads the return address into the interrupt return register prior to execution of an address jump operation, during the interrupt sequence.
$\overline{\text{IRUPC}}$	Interrupt Latch Cleared Signal (negative true)	This signal is true when the interrupt latch on processor timing CCA A8 is cleared, indicating the interrupt sequence is in process.
IRWS	Instruction Register (see pg. 2-69) Write Strobe (positive true) (Note: In both places "STROBE" should be "select")	When driven true by an interrupt sequence, this signal switches hardwired inputs to the destination bus registers on processor timing CCA A8, as well as to the resisters of decoder CCA A7.
IR0-IR23	Instruction Register (negative true)	Twenty-four-bit instruction register output to digital processor decoding circuits. These decoder circuits interpret the instructions into operations to be performed in the diqital processor. IR6-IR23 may also be used as data to be placed on the $\overline{\text{destination}}$ bus (D0-D15 lines) during a digital processor load-immediate instruction cycle.
IR0-IR23	Instruction Register (positive true)	

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
IT0, IT1	Integration Time Bits	These negative true bits, derived from the I/O bus IO0 and IO1 bits, determine (a) analog DF receiver signal sampling time(s) and DF antenna toggle rate, and (b) servo conversion CCA A19 integrator change rate.
JMP	Jump (negative true)	This true signal defines a digital processor address jump operation and enables the jump decision logic on flagjump CCA A6
JUMP	Jump Execute (negative true)	This true signal activates the digital processor operation when the jump conditions are satisfied.
LIG	Load-Immediate Gate	Loads bits IR6-IR21 directly on the destination bus (D0-D15)
M	Mode	This signal determines whether the ALU circuit performs an arithmetic operation or logic operation. High = logic operation and low = arithmetic operation.
MAR	Memory Address Register	This register stores the RAM (or scratchpad) address obtained from the destination bus (D0-D15). The negative true MAR output is inverted by SPAD drivers to provide the positive true SPAD0-SPAD15 output of the MAR SPAD drivers is also used to address the calibration ROMs.
MARCL	Memory Address Register Clock (negative true)	Loads data from the destination bus (D0-D15) into MAR.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
MARUP, MARDN	Memory Address Register Up-Clock or Down-Clock (negative true)	MARUP increases the MAR data by 1. MARDN decreases MAR data by 1.
MEMCL	Memory Clock Pulse (negative)	Loads data on the destination bus (D0-D15) onto SPINO-SPIN15 lines for the purpose of writing this data into RAM scratchpad memory.
MEMG	RAM or Scratchpad Output Gate (negative)	Enables RAM address input (SPAD0-SPAD15) and enables transfer of resulting MS0-MS15 (RAM output data) onto the source bus (S0-S15).
MOD CONT	Modulation Control	Signal derived from DT MOD which is converted into a IO11 bit. When A/D converter data is transferred onto the I/O bus, this bit antenna indicates which DF antenna is selected.
MOD IMR	MODE Input Mode Request	This differential signal, controlled by the computer, controls the direction of DFC data flow. High + line = computer generates data. Low + line = computer receives data.
MS0-MS15	Scratchpad Memory Output (Bits 0 - 15) (negative true)	Data output of RAM (scratchpad memory) or calibration ROMs which is applied to the bus (S0-S15) via source bus drivers.
MUX0-MUX2	Multiplexer Address	Three-bit digital processor test set input to display multiplexer CCA A1. This input selects one of eight (8-bit) data words for transfer to the test set via the DM0-DM7 lines.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
NFC CLOCK	Data Clock	This clock serially shifts data between the computer and the DF control or communication processor.
$\overline{\text{OVFL}}$	Oveflow (negative true)	Indicates oveflow register has been set (loaded with a 1 bit) as result of an ALU CCA data overflow.
PCCLK	Program Counter Clock	Clock which transfers the program counter address onto the RAD0-RAD15 lines.
$\overline{\text{PCCNL}}$, $\overline{\text{PCCNM}}$	Program Counter ALU Carry Control	When high, inserts a carry input to the ALUs on the program counter CCAs. PCCNL is used for the lower order program counter CCA (CCA that generates RAD0-RAD7). PCCNM is used for the higher order program counter CCA (CCA that generates RAD8-RAD15).
PCG	Program Counter Gate (negative)	Loads the digital processor program counter address (RAD0-RAD15) onto the source bus (S0-S15). (Note: Actually an inverted (negative true version) of RAD0-RAD15 is loaded.)
$\overline{\text{PCJMP}}$	Program Counter Jump Gate (negative)	This signal is generated by the flag-jump logic CCA when jump logic conditions are satisfied. The processor timing CCA responds to PCJMP by generating a second instruction cycle PCCLK pulse which loads the jump address into the program ROMs.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
PCM	Program Counter ALU Mode Control	Controls the mode of operation for the ALU chips on the program counter CCAs. High = logic mode. Low = arithmetic mode.
PCS0, PCSIL, PCS2L, PCS3	Lower Order Program Counter ALU Operation Select Bits	Controls operation of ALUs on lower order program counter CCA. The ALUs on this CCA ultimately determine the RAD8-RAD15 portion of the 16-bit program ROM address word.
PCWS	Program Counter Write Strobe (Note: "Strobe" here and in the text should be "select") (positive true)	This signal is true when the digital processor test set operator presses the PRESET switch, or when the digital processor is interrupted. When generated by the processor timing CCA, PCWS selects ASW0-ASW15 inputs to the program counter CCAs to address the program instruction ROM CCAs.
PR	Power Up Reset (negative true)	Active when the digital processor is executing the power-up routine.
PRES, $\overline{\text{PRES}}$	Preset	Differential signal, derived from the digital processor test set, which presets a DPTS-selected program address (ASW0-ASW15) into the digital processor program ROMs.
PROCEED READY		This differential signal is driven high (on the + line) by the DF control or communication processor to notify the computer of the unit's readiness to receive the next serial data word.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
RAD0-RAD15	ROM Address	Sixteen-bit word which addresses the digital processor program ROMs to access the instruction word.
RAM	Random Access (Scratchpad) Memory	Internal storage device used by the digital processor for temporary storage of 16-bit bus commands, data, or addresses. SPAD0-SPAD15 (positive-true scratchpad) address 0 - 15 selects a RAM storage location where SPIN0-SPIN15 (negative-true scratchpad) 0 - 15 input data is written (entered), or where MS0-MS15 (negative-true scratchpad memory output) is read (retrieved).
READY PROCEED		This differential signal is driven high (on the + line) by the computer to notify the DF control or communication processor that the computer is ready to accept the next serial data word.
REGCL	Register Clock	Loads destination bus (D0-D15) data into ALU registers.
RIN0-RIN3	Diagnostic ROM Input 0-23 (negative true)	Digital processor test set diagnostic ROM instruction input to digital processor (via ROM extender CCA). This input, generated in response to the digital processor XAD0-XAD15 output to the digital processor test set, is generated by the ROM extender CCA to provide INB0-INB23 bits.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
RUNS, RUNS	Run Start	Differential input from digital processor test set which causes the digital processor to start execution of its instructions again after a halt question has been executed.
Scratchpad	(Also called RAM memory)	See RAM
SC0, SC1	Shift Control 1 and 2 Bits (positive true)	Configures the ALU CCA shift multiplexer for one of four data shift operations: SC1 SCO 0 0 Shift left by 4 bits. 0 1 Shift right by 1 bit. 1 0 Shift left by 1 bit. 1 1 No shift.
SDN	Stack Pointer Register Decrement Pulse (negative true)	This signal is decoded by the instruction decoder CCA to decrease the data in the stack pointer register by 1. This input to the processor timing CCA prevents a short, high-speed instruction cycle from being executed.
SGLST, SGLST	Single Step	These active differential inputs (from the digital processor test set) cause the digital processor to step through one instruction cycle at a time after a digital processor halt command has been executed.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
S0-S15	Source Bus	Sixteen-bit, negative true bus used for transfer of digital processor information from a storage element to the ALUs.
SPADG	Scratchpad of RAM Address Gate	Negative-true signal which loads true scratchpad or RAM address (positive true SPAD-SPAD15) onto the source bus (S0-S15).
SPIN0-SPIN15	Scratchpad Input 0 - 15 (negative true)	Sixteen-bit data input to digital processor RAM (scratchpad) memory. This input is derived from the destination bus (D0-D15).
SPQ0, SPW1	Scratchpad Write Gate (negative true)	Processor timing CCA gate which causes SPIN0-SPIN15 data to be written into the digital processor RAM (scratchpad).
STPCL	Stack Pointer Register Clock (negative)	Loads data from the destination bus (D0-D15) into the stack pointer register.
STPDN	Negative Pulse	A clock which decreases the stack pointer register data by 1.
STPG	Stack Pointer Gate (negative)	Loads stack pointer register data onto the digital processor source bus .
STPUP	Negative Pulse	A clock which increases the stack pointer register data by 1.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
SUP	Stack Pointer Register Increment Pulse (negative true)	This signal is decoded by the instruction decoder CCA to increase the data in the stack pointer register by 1. This input to the processor timing CCA also prevents a short, high-speed instruction cycle from being executed.
T/H Signal	Track/Hold Signal	When high (hold mode), permits digital servo group to convert stored (held) integrator data into equivalent binary information. When low (track mode), permits the integrator to generate a ramp, while the A/D converter is isolated.
TDGB	Timer Countdown Gate	Positive edge trigger provided by digital processor timer to set the time delay register when the timer reaches a terminal (0) count.
TDGCL	Timer Clock	Negative clock pulse which loads destination bus data (D0-D7) into timer (on the display multiplexer CCA).
XAD0-XAD15	External ROM address 0-15 (negative true)	Inverted RAD0-RAD15 output (via ROM extender CCA) which addresses diagnostic ROMs of the digital processor test set.
WAIT		Negative processor timing CCA output gate which executes a digital processor address jump operation when jump test conditions are set.

GLOSSARY (CONTINUED)

Mnemonic	Definition	Comments
OL1	Shift-Left-By-1 Variable Bit (negative true)	This bit displaces the least significant ALU bit (ALU0) during certain ALU data shift-left-by-1 operations.
15L1	Shift-Left-By-1 Variable Bit (negative true)	This bit displaces the most significant ALU bit (ALU15) during certain ALU data shift-left-by-1 operations.
1SR1	Shift-Right-by-1 Variable Bit (negative true)	This bit displaces the most significant ALU bit (ALU15) during certain ALU data shift-left-by-1 operations.
4L0, 4L3	Shift-Left-By-4 Variable Bits 0 - 3 (negative true)	These four bits displace the four least significant ALU bits (ALU0-ALU3) during an ALU data shift-left-by-4 operation.
500-Hz		Clock generated by servo-timing CCA for use by the digital servo group.

ALPHABETICAL INDEX

ALPHABETICAL INDEX (CONTINUED)

ALPHABETICAL INDEX (CONTINUED)

ALPHABETICAL INDEX (CONTINUED)

ALPHABETICAL INDEX (CONTINUED)

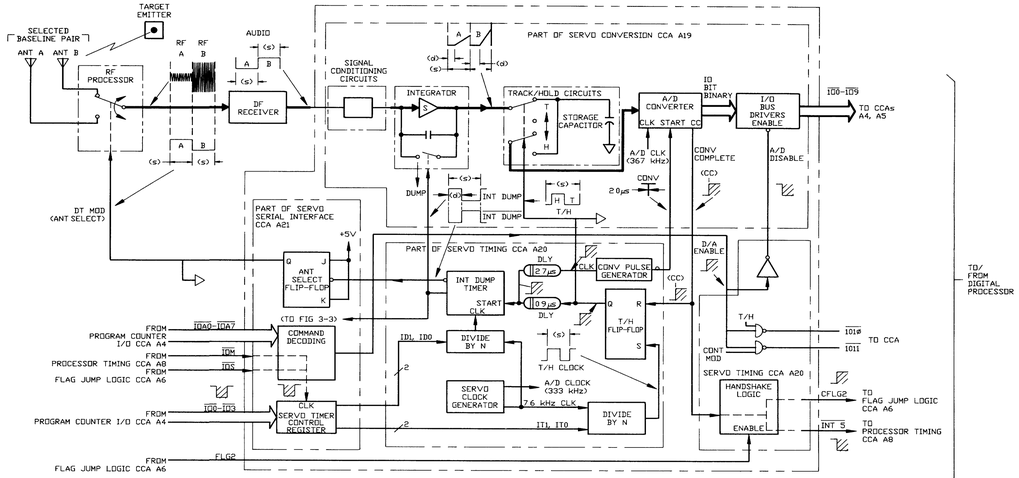


Figure FO-1. **Servo Data Acquisition Functional Block Diagram**

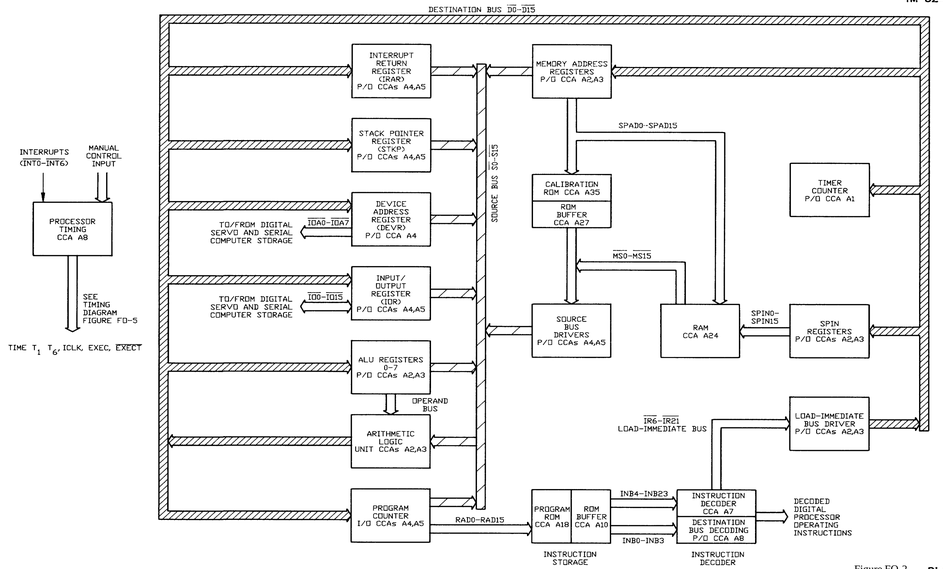
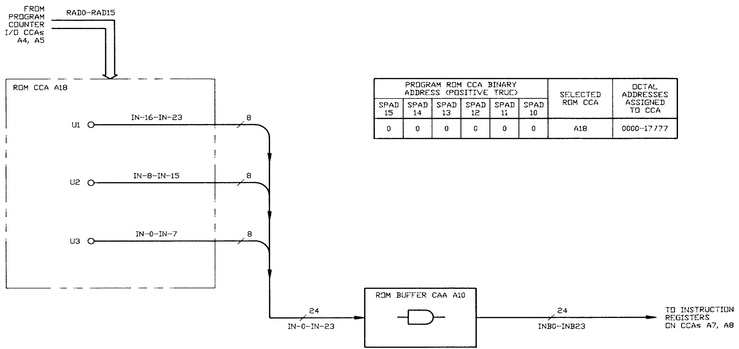


Figure FO-2. **Digital Processor Architecture**



PROGRAM ROM CCA BINARY ADDRESS (POSITIVE TRUE)						SELECTED ROM CCA	OCTAL ADDRESSES ASSIGNED TO CCA
SPAD 15	SPAD 14	SPAD 13	SPAD 12	SPAD 11	SPAD 10		
0	0	0	0	0	0	A18	0000-17777

Figure FO-3. **ROM Organization**
FP-5/(FP-6 blank)

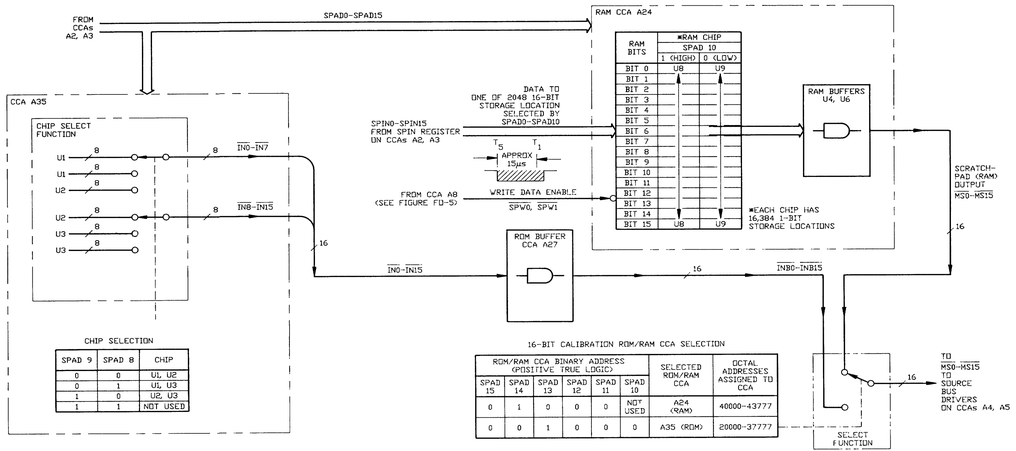


Figure FO-4. RAM/Calibration ROM Organization

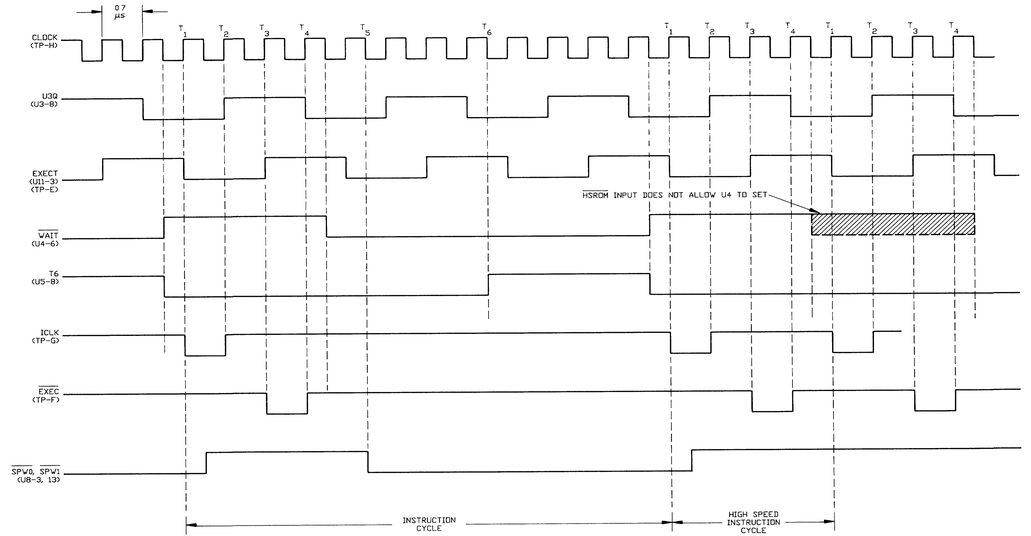


Figure FO-5. **Digital Processor Timing Diagram**

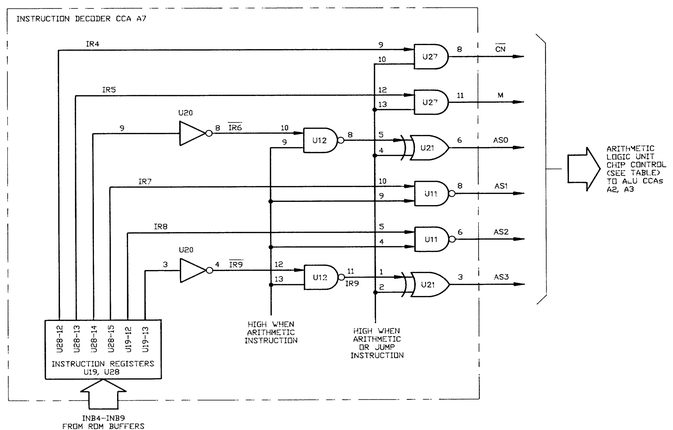


Figure FO-6. **ALU Decode Functional Block Diagram (Sheet 1 of 2)**

INSTRUCTION (POSITIVE TRUE LOGIC)							RESULTING ALU CCA INPUTS (POSITIVE TRUE)						ALU (U6, U13) CONFIGURATION (ALL DATA NEGATIVE TRUE)	
IN89	IN88	IN87	IN86	IN85	IN84	OCTAL	AS3	AS2	AS1	AS0	M	CN	LOGIC*	ARITHMETIC
0	0	0	0	0	0	00	1	1	1	1	0	0	———	(SDR)
0	0	0	0	0	1	01	1	1	1	1	0	1	———	(SDR) PLUS 1
0	0	0	0	1	0	02	1	1	1	1	1	0	(SDR)	———
0	0	0	0	1	1	03	1	1	1	1	1	1	(SDR)	———
0	0	0	1	0	0	04	1	1	1	0	0	0	———	(SDR) (OP) PLUS (SDR)
0	0	0	1	0	1	05	1	1	1	0	0	1	———	(SDR) (OP) PLUS (SDR) PLUS 1
0	0	0	1	1	0	06	1	1	1	0	1	0	(SDR) (OP)	———
0	0	0	1	1	1	07	1	1	1	0	1	1	(SDR) (OP)	———
0	0	1	0	0	0	10	1	1	0	1	0	0	———	(SDR) (OP) PLUS (SDR)
0	0	1	0	0	1	11	1	1	0	1	0	1	———	(SDR) (OP) PLUS (SDR) PLUS 1
0	0	1	0	1	0	12	1	1	0	1	1	0	(SDR) $\overline{(OP)}$	———
0	0	1	0	1	1	13	1	1	0	1	1	1	(SDR) $\overline{(OP)}$	———
0	0	1	1	0	0	14	1	1	0	0	0	0		3 TIMES (SDR)
0	0	1	1	0	1	15	1	1	0	0	0	1		3 TIMES (SDR) PLUS 1
0	0	1	1	1	0	16	1	1	0	0	1	0	OUTPUT ALL 0's	———
0	0	1	1	1	1	17	1	1	0	0	1	1	OUTPUT ALL 0's	———
0	1	0	0	0	0	20	1	0	1	1	0	0	———	(SDR)+(OP)
0	1	0	0	0	1	21	1	0	1	1	0	1	———	(SDR)+(OP) PLUS 1
0	1	0	0	1	0	22	1	0	1	1	1	0	(SDR)+(OP)	———
0	1	0	0	1	1	23	1	0	1	1	1	0	(SDR)+(OP)	———
0	1	0	1	0	0	24	1	0	1	0	0	0	———	(SDR) $\overline{(OP)}$ PLUS [(SDR)+(OP)]
0	1	0	1	0	1	25	1	0	1	0	0	1	———	(SDR) $\overline{(OP)}$ PLUS [(SDR)+(OP)] PLUS 1
0	1	0	1	1	0	26	1	0	1	0	1	0	(OP)	———
0	1	0	1	1	1	27	1	0	1	0	1	1	(OP)	———
0	1	1	0	0	0	30	1	0	0	1	0	0	———	(SDR) PLUS (OP)
0	1	1	0	0	1	31	1	0	0	1	0	1	———	(SDR) PLUS (OP) PLUS 1
0	1	1	0	1	0	32	1	0	0	1	1	0	(SDR)$\oplus$(OP)	———
0	1	1	0	1	1	33	1	0	0	1	1	1	(SDR)$\oplus$(OP)	———
0	1	1	1	0	0	34	1	0	0	0	0	0	———	(SDR) PLUS [(SDR)+(OP)]
0	1	1	1	0	1	35	1	0	0	0	0	1	———	(SDR) PLUS [(SDR)+(OP)] PLUS 1
0	1	1	1	1	0	36	1	0	0	0	1	0	$\overline{(SDR)}$ (OP)	———
0	1	1	1	1	1	37	1	0	0	0	1	1	$\overline{(SDR)}$ (OP)	———

INSTRUCTION (POSITIVE TRUE LOGIC)							RESULTING ALU CCA INPUTS (POSITIVE TRUE)						ALU (U6, U13) CONFIGURATION (ALL DATA NEGATIVE TRUE)	
IN89	IN88	IN87	IN86	IN85	IN84	OCTAL	AS3	AS2	AS1	AS0	M	CN	LOGIC*	ARITHMETIC
1	0	0	0	0	0	40	0	1	1	1	0	0	———	(SDR)+$\overline{(OP)}$
1	0	0	0	0	1	41	0	1	1	1	0	1	———	(SDR)+$\overline{(OP)}$ PLUS 1
1	0	0	0	1	0	42	0	1	1	1	1	0	(SDR)+$\overline{(OP)}$	———
1	0	0	0	1	1	43	0	1	1	1	1	1	(SDR)+$\overline{(OP)}$	———
1	0	0	1	0	0	44	0	1	1	0	0	0	———	(SDR) MINUS (OP) MINUS 1
1	0	0	1	0	1	45	0	1	1	0	0	1	———	(SDR) MINUS (OP)
1	0	0	1	1	0	46	0	1	1	0	1	0	(SDR)$\oplus$(OP)	———
1	0	0	1	1	1	47	0	1	1	0	1	1	(SDR)$\oplus$(OP)	———
1	0	1	0	0	0	50	0	1	0	1	0	0	———	(SDR) (OP) PLUS [(SDR)+(OP)]
1	0	1	0	0	1	51	0	1	0	1	0	1	———	(SDR) (OP) PLUS [(SDR)+(OP)] PLUS 1
1	0	1	0	1	0	52	0	1	0	1	1	0	(OP)	———
1	0	1	0	1	1	53	0	1	0	1	1	1	(OP)	———
1	0	1	1	0	0	54	0	1	0	0	0	0	———	(SDR) PLUS [(SDR)+(OP)]
1	0	1	1	0	1	55	0	1	0	0	0	1	———	(SDR) PLUS [(SDR)+(OP)] PLUS 1
1	0	1	1	1	0	56	0	1	0	0	1	0	$\overline{(SDR)}$+(OP)	———
1	0	1	1	1	1	57	0	1	0	0	1	1	$\overline{(SDR)}$+(OP)	———
1	1	0	0	0	0	60	0	0	1	1	0	0	———	OUTPUT MINUS 1
1	1	0	0	0	1	61	0	0	1	1	0	1	———	OUTPUT REMAINS THE SAME
1	1	0	0	1	0	62	0	0	1	1	1	0	OUTPUT ALL 1's	———
1	1	0	0	1	1	63	0	0	1	1	1	1	OUTPUT ALL 1's	———
1	1	0	1	0	0	64	0	0	1	0	0	0	———	(SDR) $\overline{(OP)}$ MINUS 1
1	1	0	1	0	1	65	0	0	1	0	0	1	———	(SDR) $\overline{(OP)}$
1	1	0	1	1	0	66	0	0	1	0	1	0	$\overline{(SDR)}$+$\overline{(OP)}$	———
1	1	0	1	1	1	67	0	0	1	0	1	1	$\overline{(SDR)}$+$\overline{(OP)}$	———
1	1	1	0	0	0	70	0	0	0	1	0	0	———	(SDR)+(OP) MINUS 1
1	1	1	0	0	1	71	0	0	0	1	0	1	———	(SDR) (OP)
1	1	1	0	1	0	72	0	0	0	1	1	0	$\overline{(SDR)}$ $\overline{(OP)}$	———
1	1	1	0	1	1	73	0	0	0	1	1	1	$\overline{(SDR)}$ $\overline{(OP)}$	———
1	1	1	1	0	0	74	0	0	0	0	0	0	———	(SDR) MINUS 1
1	1	1	1	0	1	75	0	0	0	0	0	1	———	(SDR)
1	1	1	1	1	0	76	0	0	0	0	1	0	$\overline{(SDR)}$	———
1	1	1	1	1	1	77	0	0	0	0	1	1	$\overline{(SDR)}$	———

(SDR)=SOURCE BUS DATA
(OP)=OPERAND BUS DATA

Figure FO-6. **ALU Decode Functional Block Diagram (Sheet 2 of 2)**

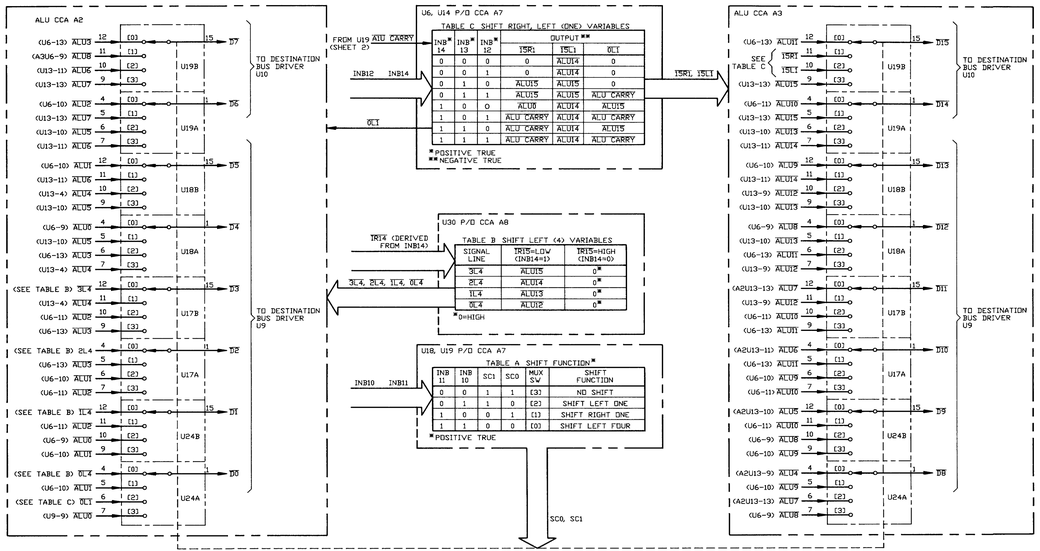


Figure FO-7. **ALU Shift Functional Block Diagram (Sheet 1 of 2)**

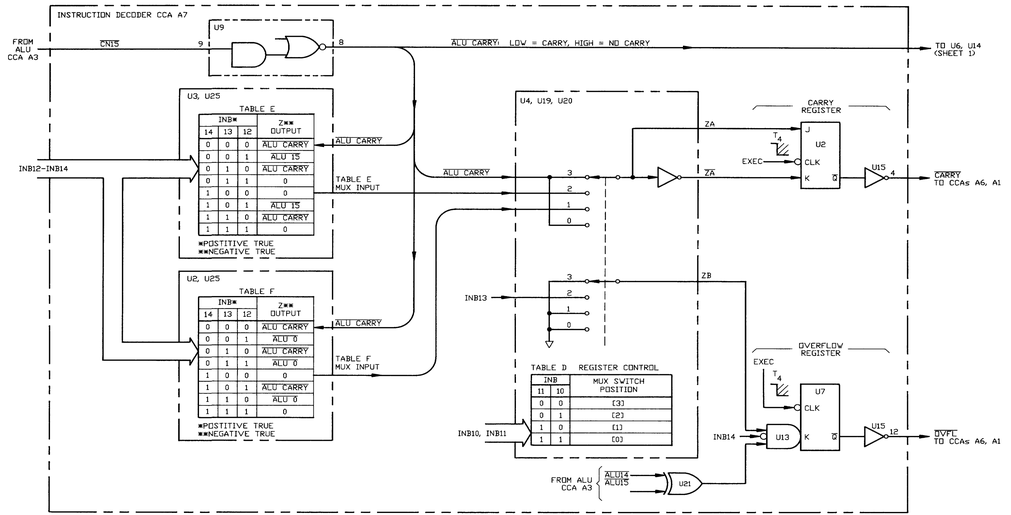


Figure FO-7 **ALU Shift Functional Block Diagram (Sheet 2 of 2)**

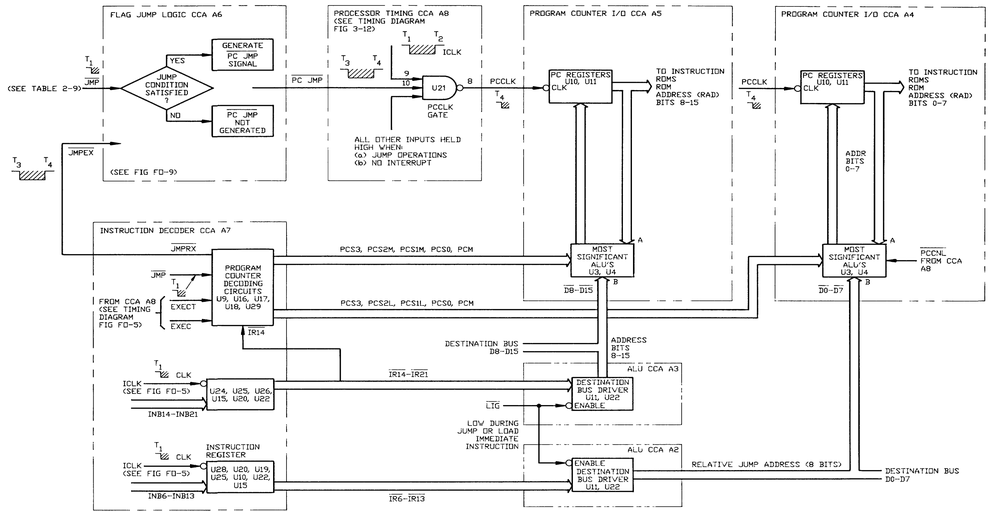


Figure FO-8 **Program Counter Functional Block Diagram**

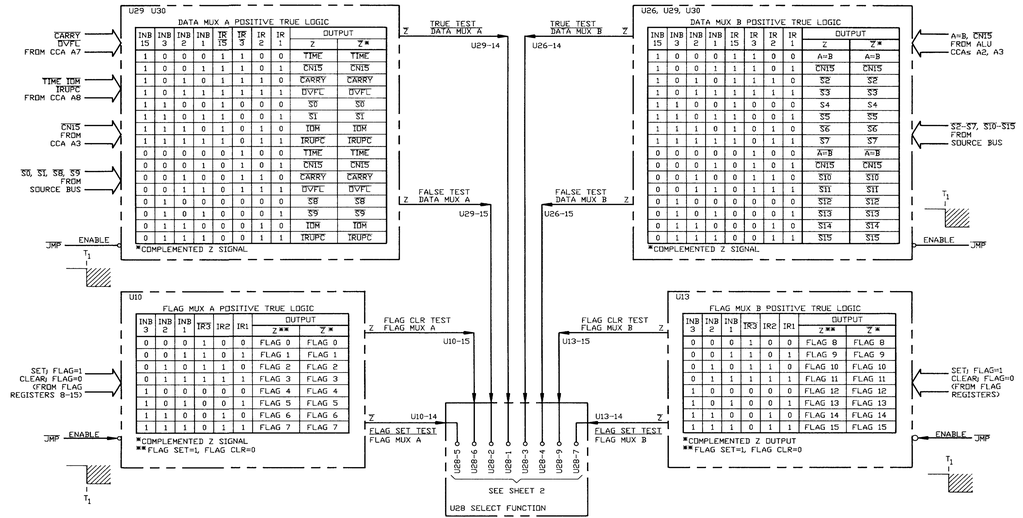
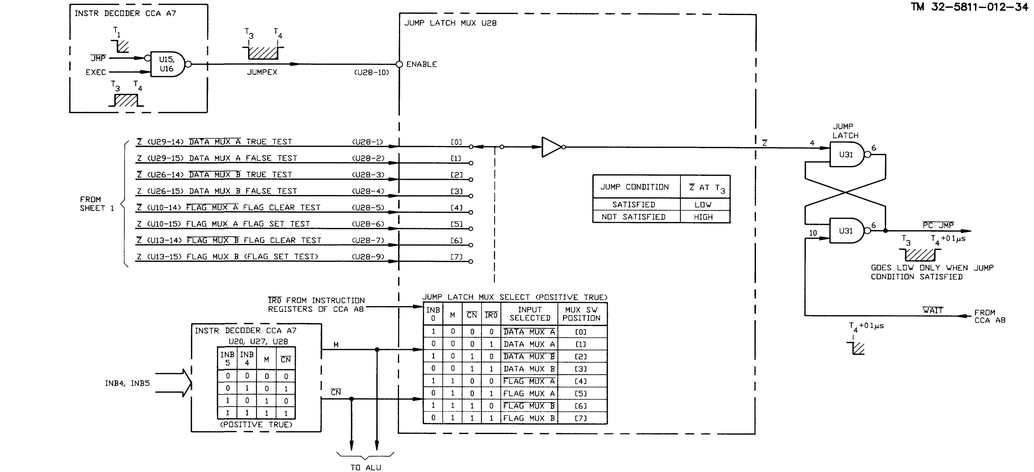


Figure FO-9. **CCA A6 Jump Test Condition Select Functional Block (Sheet 1 of 2)**



NOTE: CALCULATING ALUs ON CCAs A2, A3 ARE FORCED INTO THE FOLLOWING CONFIGURATION DURING A JUMP INSTRUCTION:

M	CN	ALU FUNCTION (CCAs A2, A3)
0	0	(SOR) MINUS (OPR) MINUS 1
0	1	(SOR) MINUS (OPR)

Figure FO-9. **CCA A6 Jump Test Condition Select Functional Block Diagram (Sheet 2 of 2)**

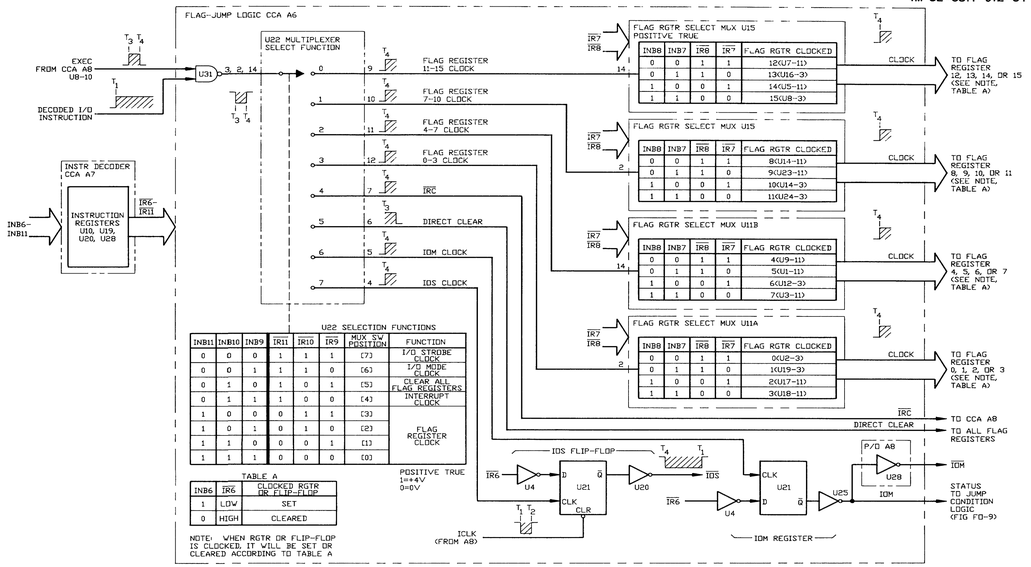


Figure FO-10 **I/O Functional Select Functional Block Diagram**

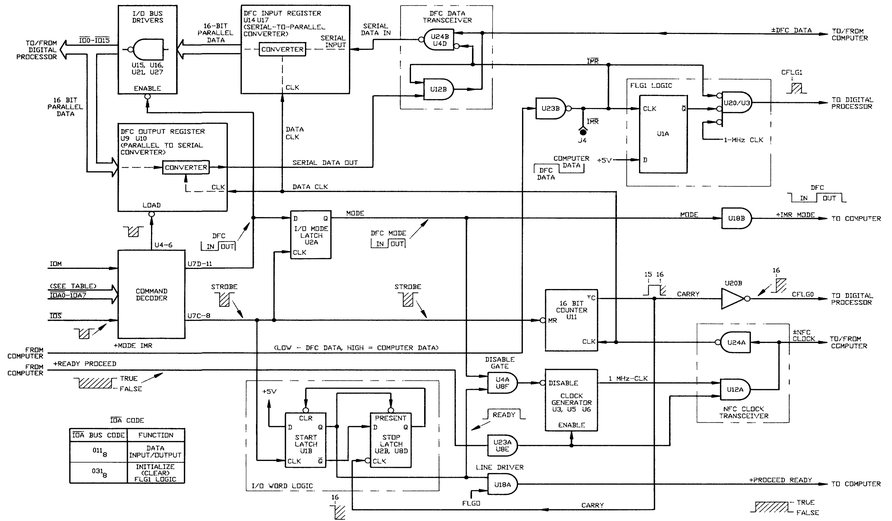


Figure FO-11 **Computer Interface Logic Functional Block Diagram**

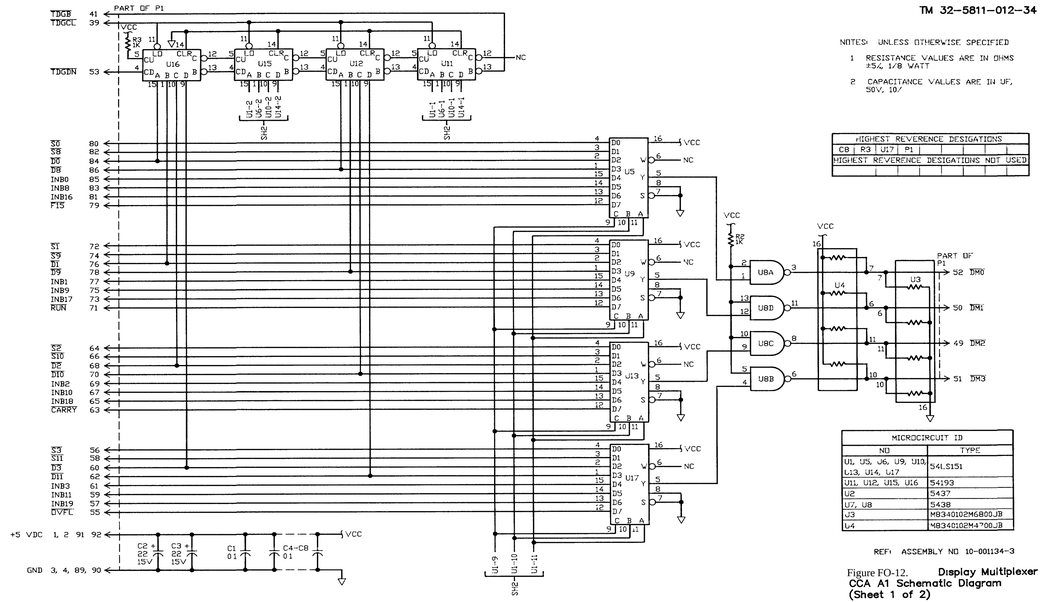


Figure FO-12. **Display Multiplexer CCA A1 Schematic Diagram (Sheet 1 of 2)**

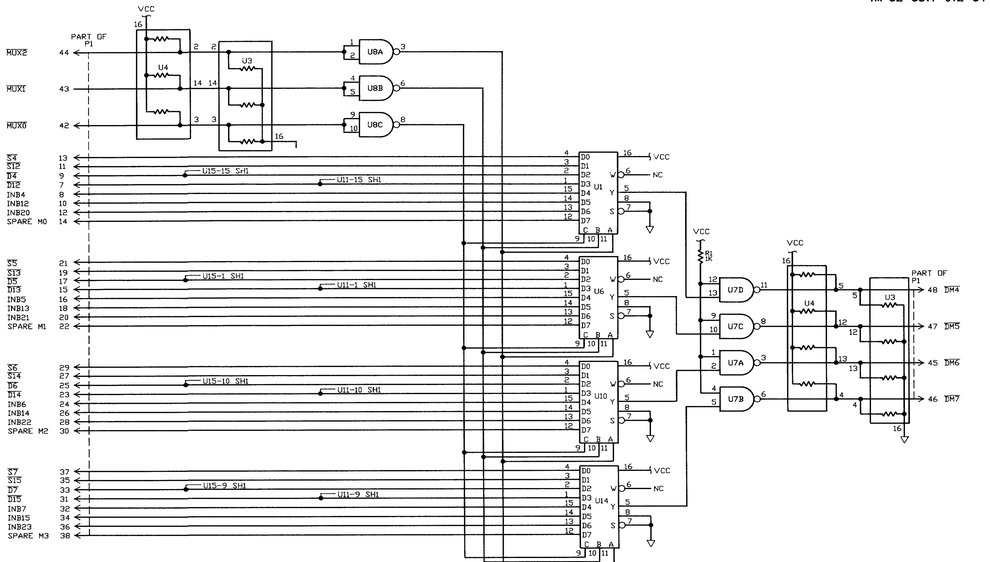
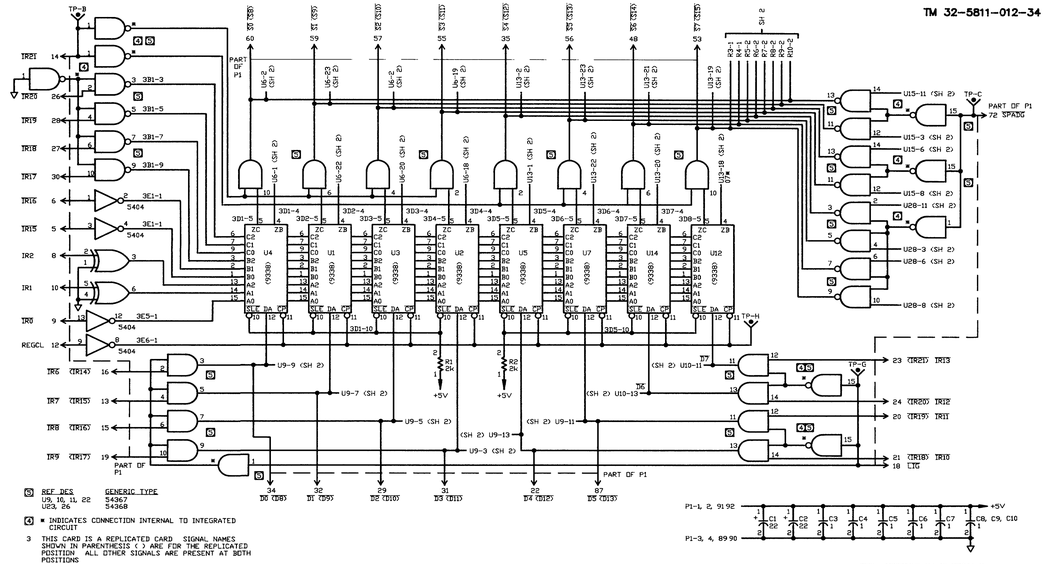


Figure FO-12. Display Multiplexer CCA A1 Schematic Diagram (Sheet 2 of 2)



	REF DES	GENERIC TYPE
	U9, 10, 11, 22	54367
	U23, 24	54368

4 ■ INDICATES CONNECTION INTERNAL TO INTEGRATED CIRCUIT

3 THIS CARD IS A REPLICATED CARD. SIGNAL NAMES SHOWN IN PARENTHESIS ( ) ARE FOR THE REPLICATED POSITION. ALL OTHER SIGNALS ARE PRESENT AT BOTH POSITIONS

2 ALL CAPACITANCE VALUES ARE IN MICROFARADS

1 ALL RESISTANCE VALUES ARE IN OHMS, 1/8W, ±5%

NOTES: UNLESS OTHERWISE SPECIFIED

Figure FO-13. **Arithmetic Logic Unit CCA A2, A3 Schematic Diagram (Sheet 1 of 2)**

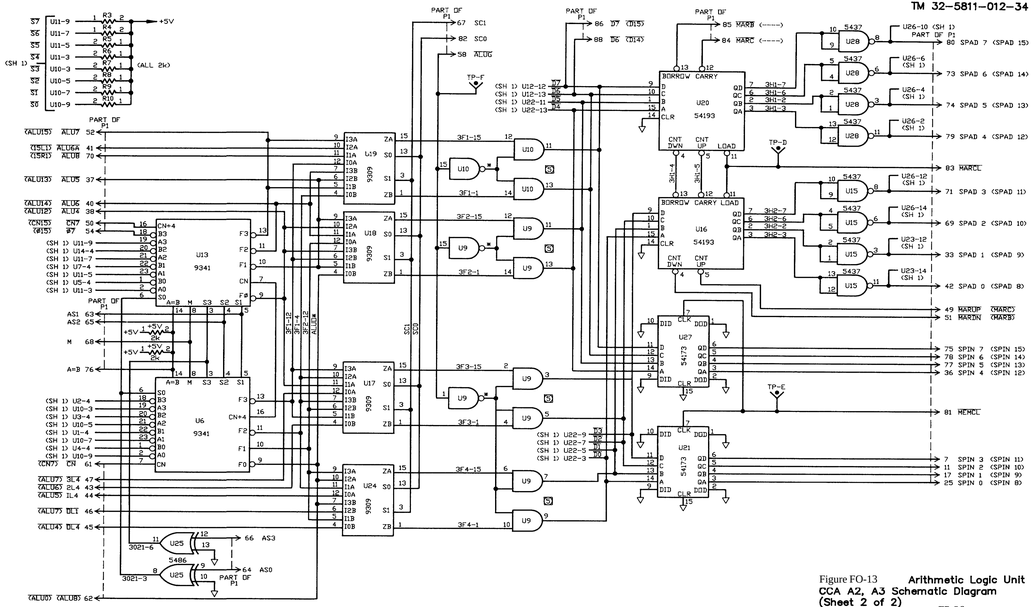


Figure FO-13 **Arithmetic Logic Unit CCA A2, A3 Schematic Diagram (Sheet 2 of 2)**

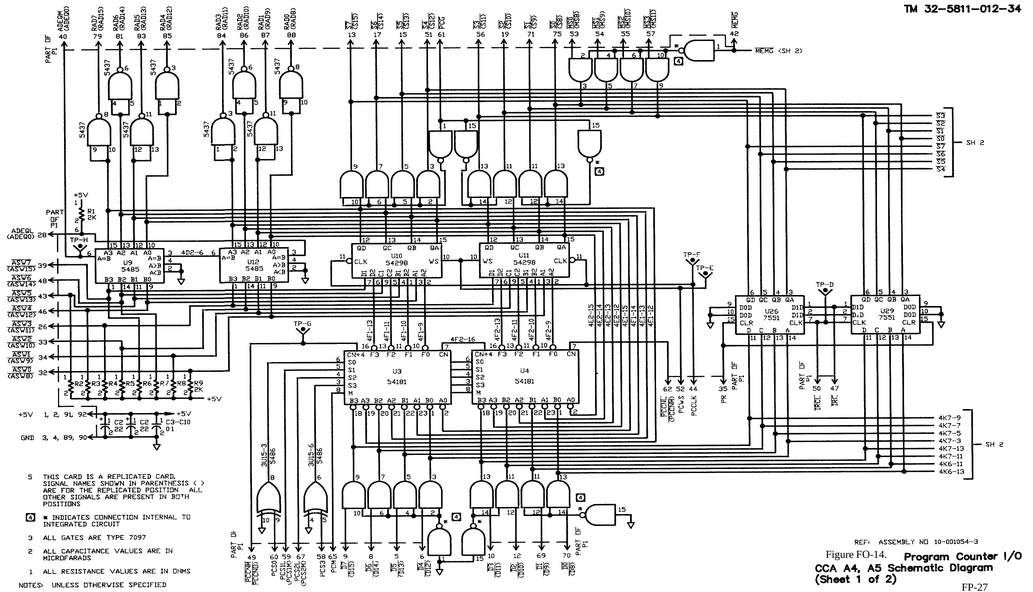


Figure FO-14. **Program Counter I/O CCA A4, A5 Schematic Diagram (Sheet 1 of 2)**

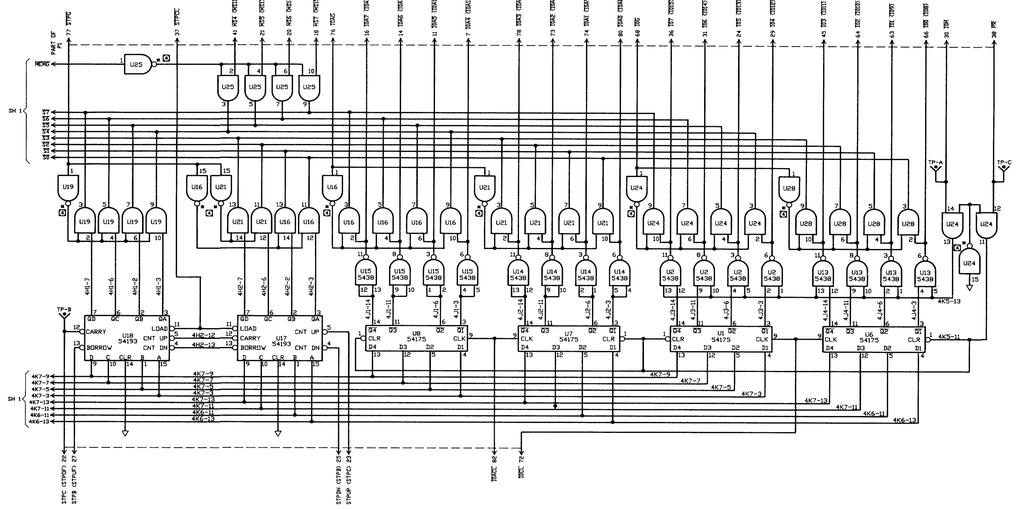


Figure FO-14. Program Counter I/O CCA A4, A5 Schematic Diagram (Sheet 2 of 2)

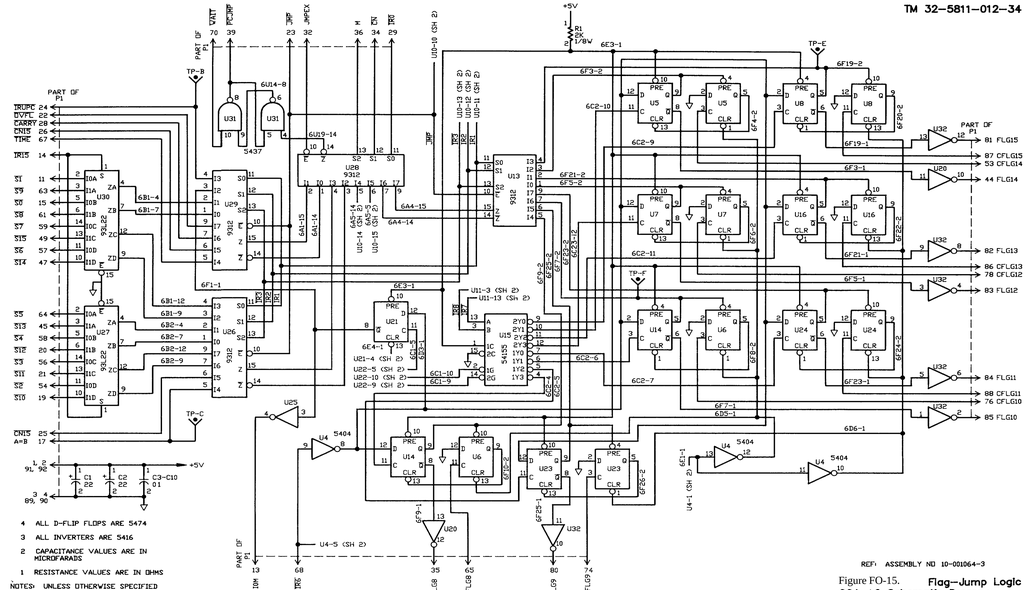


Figure FO-15. Flag–Jump Logic CCA A6 Schematic Diagram (Sheet 1 of 2)

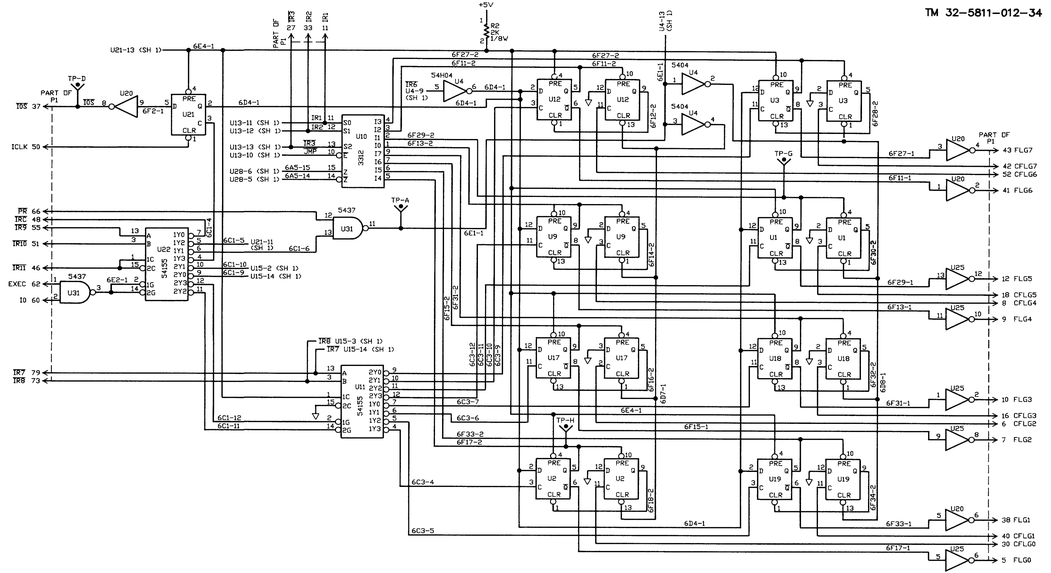


Figure FO-15. **Flag–Jump Logic CCA A6 Schematic Diagram (Sheet 2 of 2)**

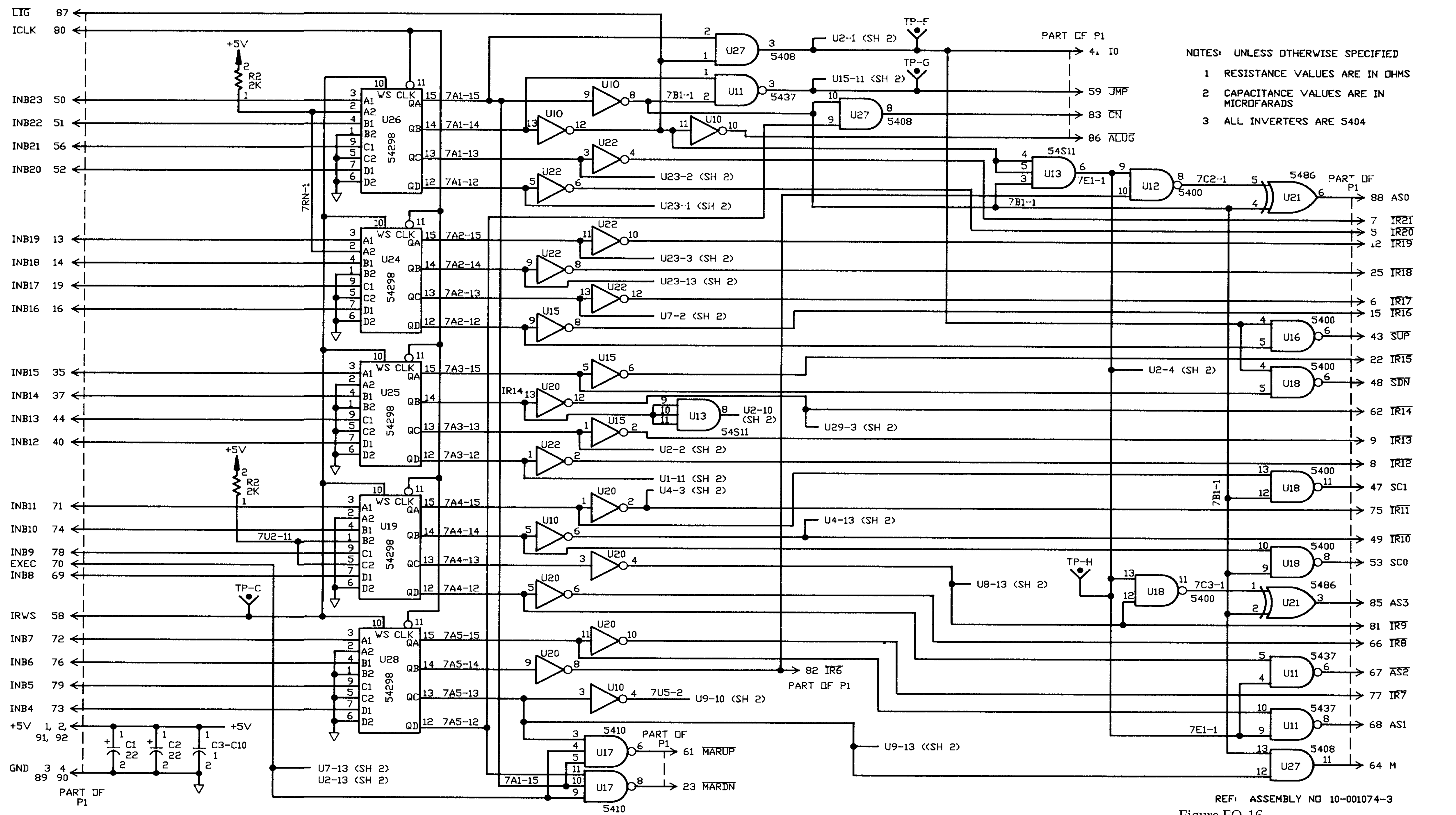


Figure FO-16. Instruction Decoder CCA A7 Schematic Diagram (Sheet 1 of 2)

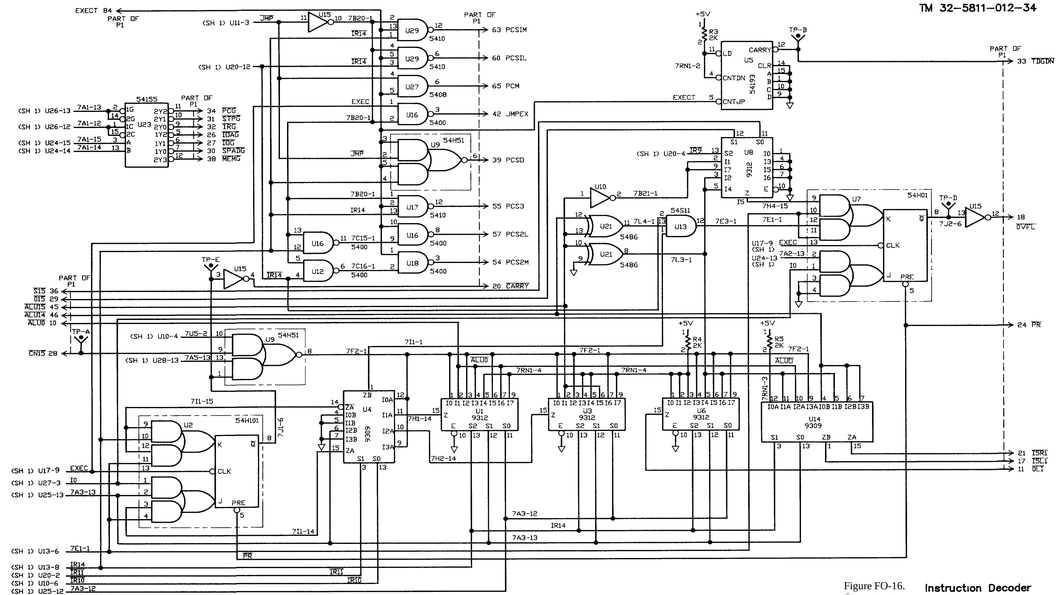
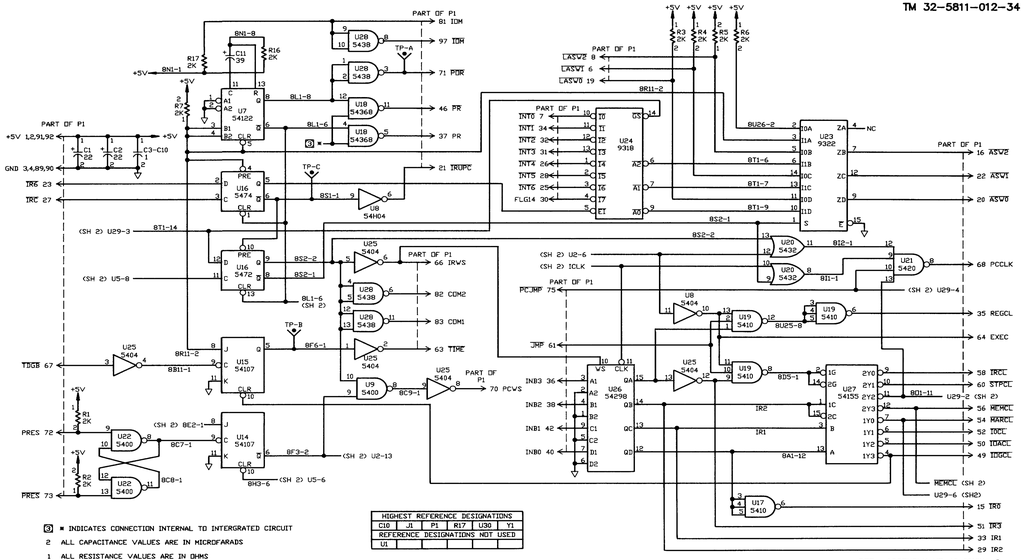


Figure FO-16. Instruction Decoder CCA A7 Schematic Diagram (Sheet 2 of 2)



HIGHEST REFERENCE DESIGNATIONS					
C10	J1	P1	R17	U30	Y1
REFERENCE DESIGNATIONS NOT USED					
U1					

[3] = INDICATES CONNECTION INTERNAL TO INTERGRATED CIRCUIT

2 ALL CAPACITANCE VALUES ARE IN MICROFARADS

1 ALL RESISTANCE VALUES ARE IN OHMS

NOTES: UNLESS OTHERWISE SPECIFIED

Figure FO-17. **Processor Timing CCA A8 Schematic Diagram (Sheet 1 of 2)**

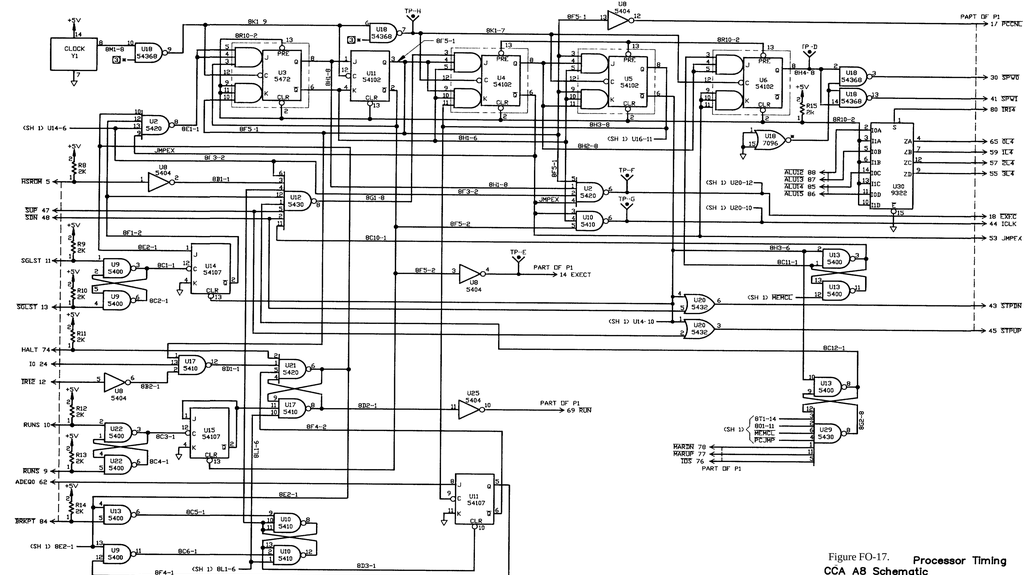


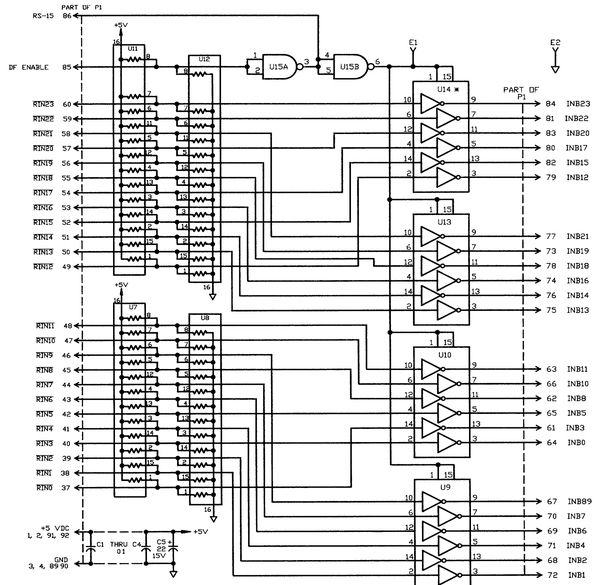
Figure FO-17. Processor Timing
CCA A8 Schematic
(Sheet 2 of 2)

NOTES: UNLESS OTHERWISE SPECIFIED

1 RESISTANCE VALUES ARE IN OHMS ±5%, 1/8W

2 CAPACITANCE VALUES ARE IN UF 50V, ±10%

MICROCIRCUIT ID	
NO	TYPE
U1, U7, U11	MB34012CM4700JB
U2, U8, U12	MB34012M6800JB
U3, U4, U5, U6	5438
U9, U10, U13, U14	54368
U15	5437



REF: ASSEMBLY NO 10-001144-3

Figure FO-18. **ROM Extender CCA A9 Schematic Diagram (Sheet 1 of 2)**

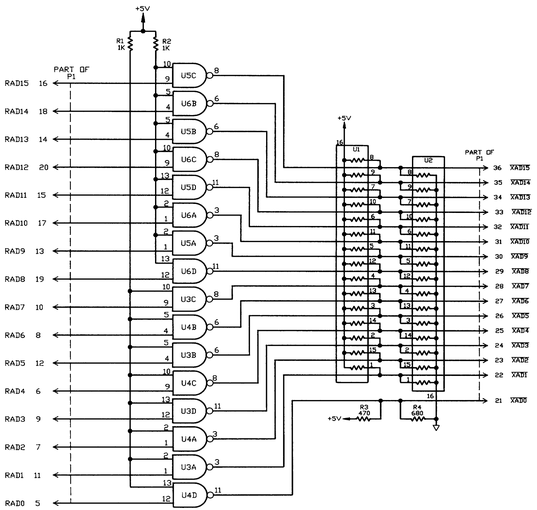


Figure FO-18. **ROM Extender CCA A9 Schematic Diagram (Sheet 2 of 2)**

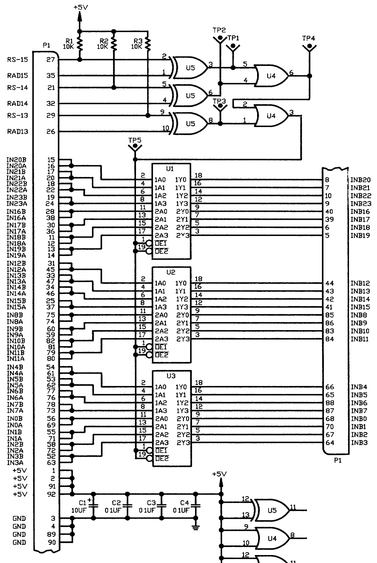
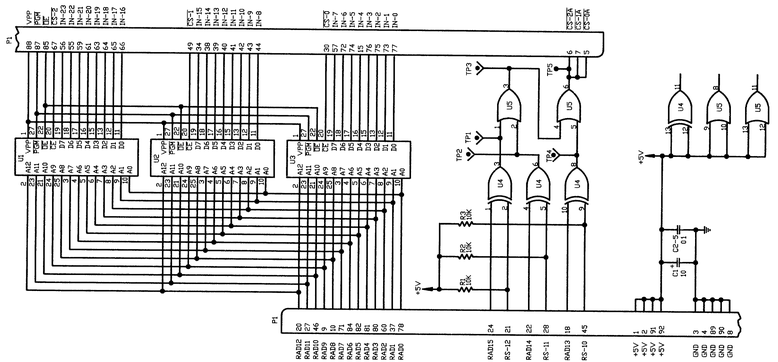


Figure FO-19. **ROM Buffer CCA A10, A27 Schematic Diagram**



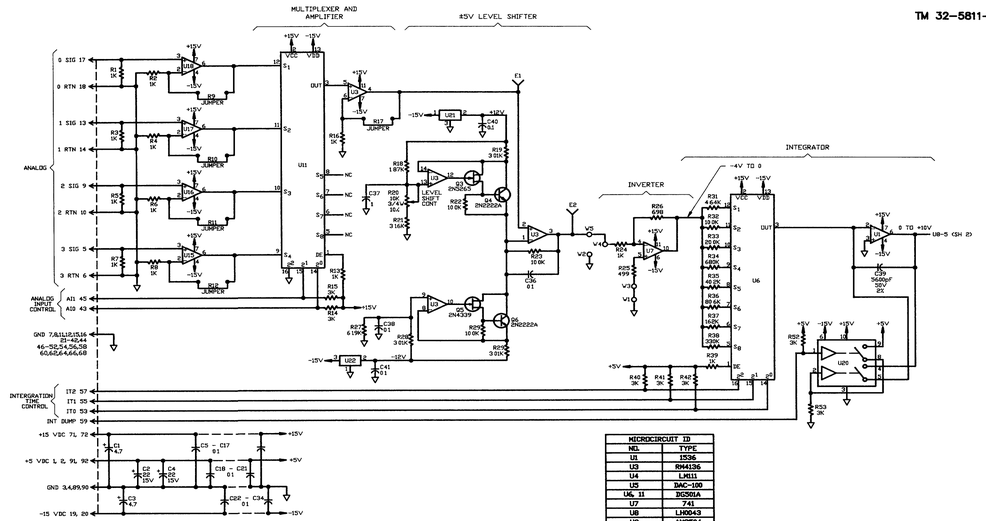
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES ARE ±5% 1/4W
2. CAPACITANCE VALUES ARE 10% 50V

REF DES	TYPE	+5V	GND
U1-3	2764	28	14
U4	LS86	14	7
U5	LS32	14	7

REF: ASSEMBLY NO C5135413-1

Figure FO-20. **Read Only Memory CCA, A18, A35 Schematic Diagram**



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES ARE IN Ω, RATINGS ARE AS FOLLOWS:
   1/4W, ±5% R13 - 15, 34, 38 - 42, 45, 47, 49 - 51
   1/10W, ±1% R1 - 8, 16, 18, 19, 21 - 33, 35 - 37, 44
   1/8W, ±5% R46, 52, 53
2. CAPACITANCE VALUES ARE IN UF, ±10%, 50V

HIGHEST REFERENCE DESIGNATIONS					
R53	C65	C41	Q6	U22	F1
REFERENCE DESIGNATIONS NOT USED					
Q1, 2	U2,19	CR1	R9-12,17,43,44		

MICROCIRCUIT ID	
NO.	TYPE
U1	1536
U3	RM4136
U4	LM111
U5	DAC-100
U6, 11	DG501A
U7	741
U8	LM0043
U9	AM2504
U10	LM0008H
U12, 13, 14	5438
U15, 16, 17, 18	GP05
U19	HI2-200-8
U21	LM148,AM-12
U22	LM1894-12

REF: ASSEMBLY NO. 10-001094-33

Figure FO-21. **Servo Conversion CCA A19 Schematic Diagram (Sheet 1 of 2)**

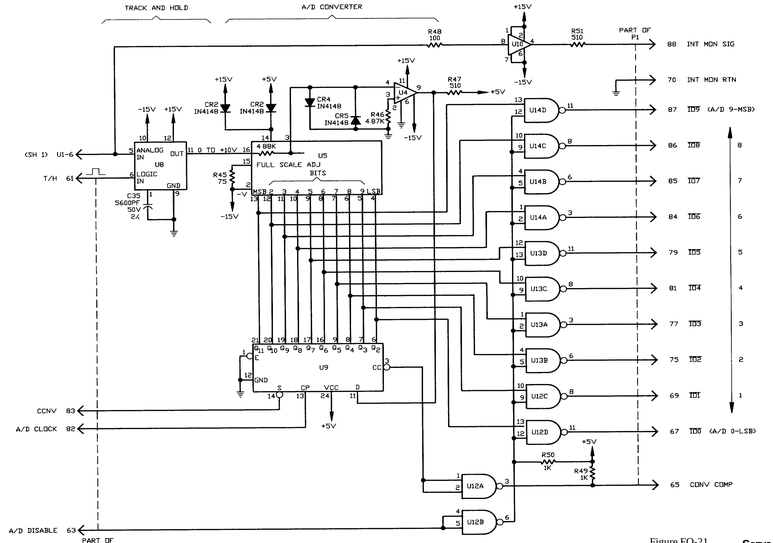
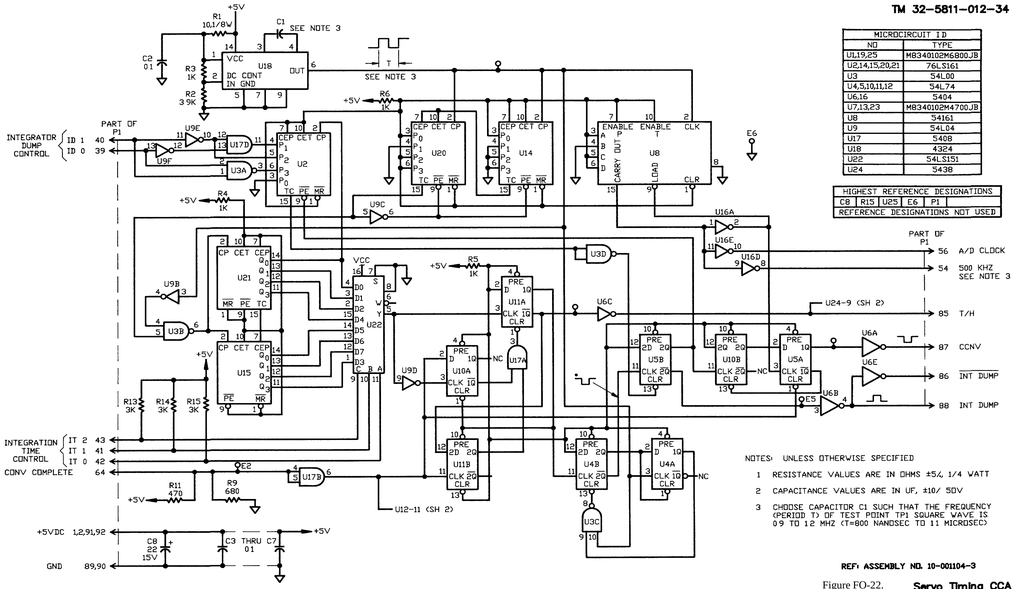


Figure FO-21. **Servo Conversion CCA A19 Schematic Diagram (Sheet 2 of 2)**



MICROCIRCUIT ID	
NO	TYPE
U1,19,25	MB3401D2M6800JB
U2,14,15,20,21	74LS161
U3	54L00
U4,5,10,11,12	54L74
U6,16	5404
U7,13,23	MB3401D2M4700JB
U8	54161
U9	54L04
U17	5408
U18	4324
U22	54LS151
U24	5438

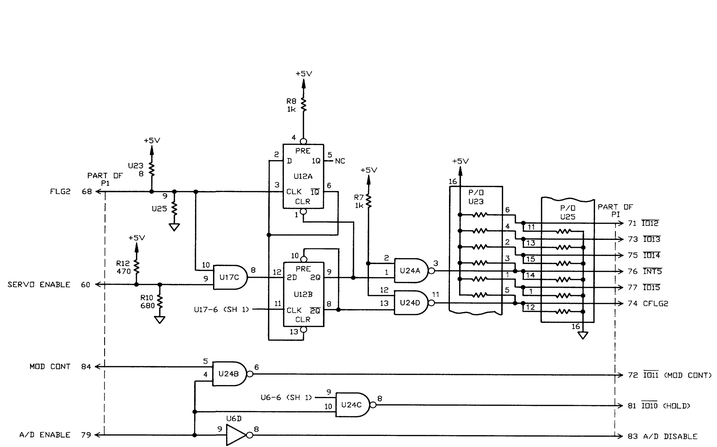
HIGHEST REFERENCE DESIGNATIONS				
C8	R15	U25	E6	P1
REFERENCE DESIGNATIONS NOT USED				

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES ARE IN OHMS ±5% 1/4 WATT
2. CAPACITANCE VALUES ARE IN UF, ±10% 50V
3. CHOOSE CAPACITOR C1 SUCH THAT THE FREQUENCY (PERIOD T) OF TEST POINT TP1 SQUARE WAVE IS 09 TO 12 MHZ (T=800 NANOSEC TO 11 MICROSEC)

REF: ASSEMBLY NO. 10-001104-3

Figure FO-22. **Servo Timing CCA A20 Schematic Diagram (Sheet 1 of 2)**



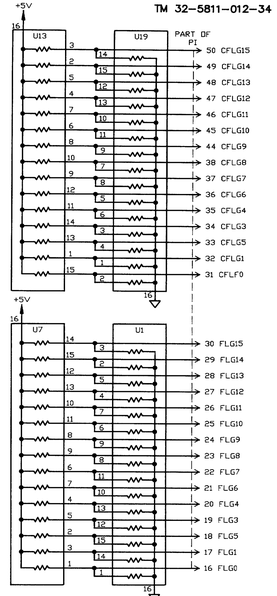
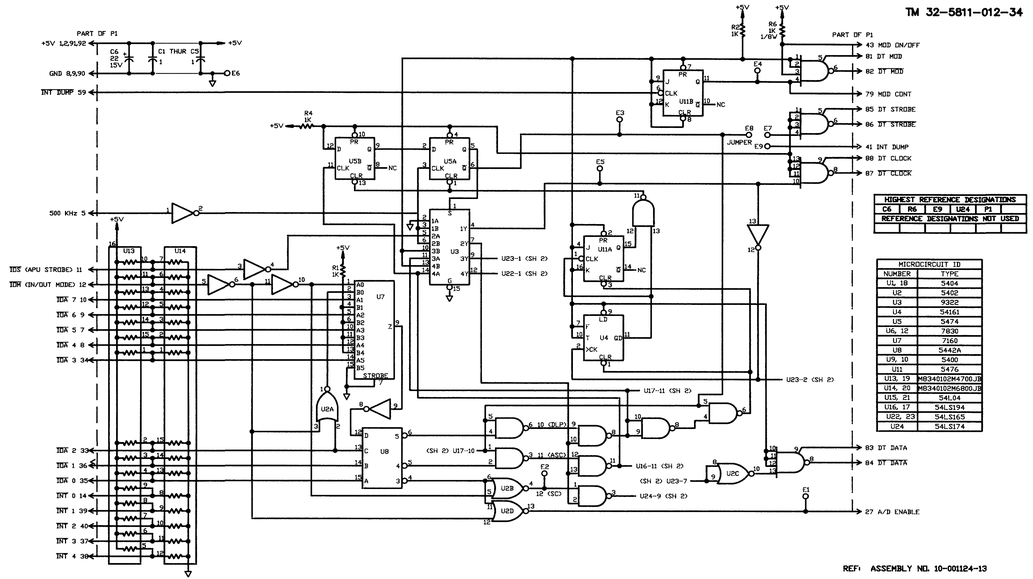


Figure FO-22. **Servo Timing CCA A20 Schematic Diagram (Sheet 2 of 2)**



HIGHEST REFERENCE DESIGNATIONS					
C6	R6	E9	U24	P1	
REFERENCE DESIGNATIONS NOT USED					

MICROCIRCUIT ID	
NUMBER	TYPE
U1, 18	5404
U2	5402
U3	9322
U4	54161
U5	5474
U6, 12	7830
U7	7160
U8	5442A
U9, 10	5400
U11	5476
U13, 19	MB340102M4700JB
U14, 20	MB340102M6800JB
U15, 21	54L04
U16, 17	54LS194
U22, 23	54LS165
U24	54LS174

Figure FO-23. **Servo Serial Interface CCA A21 Schematic Diagram (Sheet 1 of 2)**

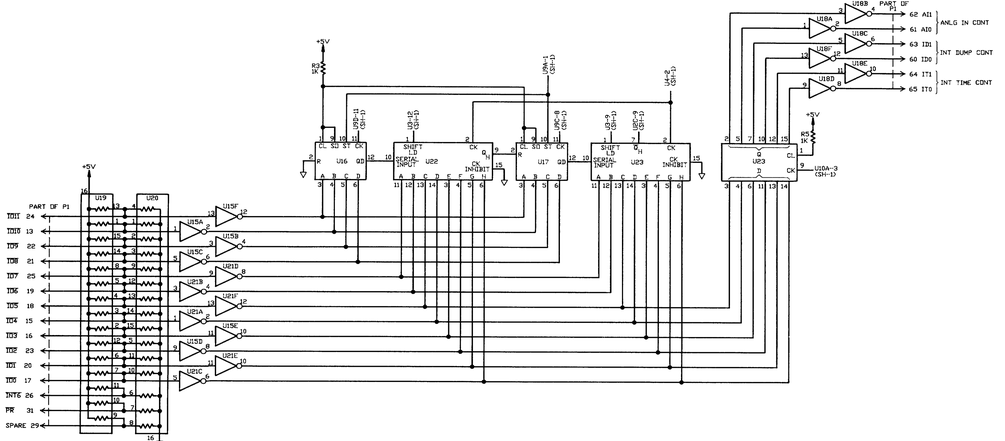


Figure FO-23. Servo Serial Interface CCA A21 Schematic Diagram (Sheet 2 of 2)

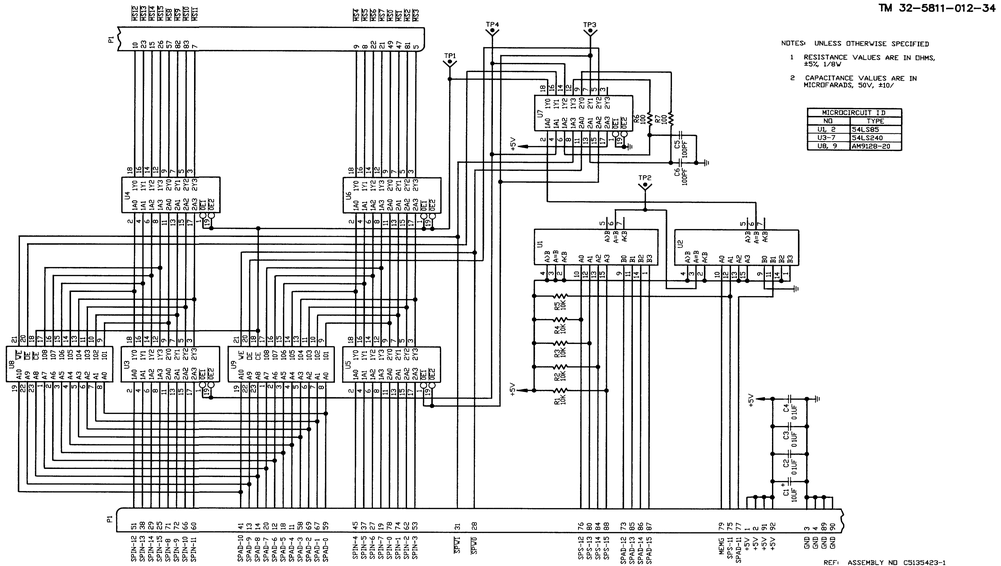
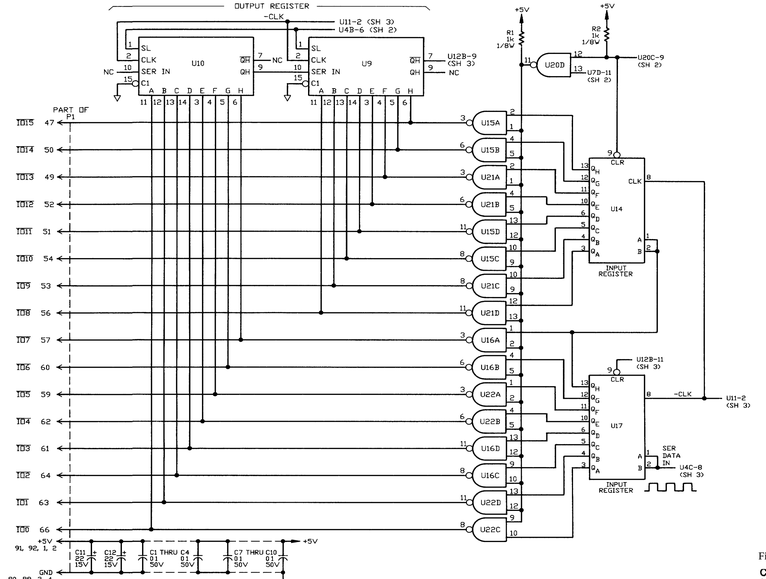


Figure FO-24. **Random Access Memory CCA A24 Schematic Diagram**



NOTES: UNLESS OTHERWISE SPECIFIED

1 RESISTANCE VALUES ARE IN OHMS ±5%, 1/4 WATT

2 CAPACITANCE VALUES ARE IN UF

MICROCIRCUIT IDENT			
REF DES	TYPE	VCC	GND
U1, 2, 5	54L74	14	7
U3	54L02	14	7
U4, 7, 13	54L00	14	7
U6	4324	14	7
U8	54L04	14	7
U9, 10	54L165A	16	8
U11	7416,76	16	8
U12, 18	9614	16	8
U14, 17	54L164	14	7
U15, 16, 20-22	5438	14	7
U19	7160	16	8
U23, 24	9615	16	8

HIGHEST REFERENCE DESIGNATIONS					
C12	E2	J8	P1	R36	U24
REFERENCE DESIGNATIONS NOT USED					

REF: ASSEMBLY NO 10-123804-1

Figure FO-25. **Serial Interface CCA A26 Schematic Diagram (Sheet 1 of 3)**

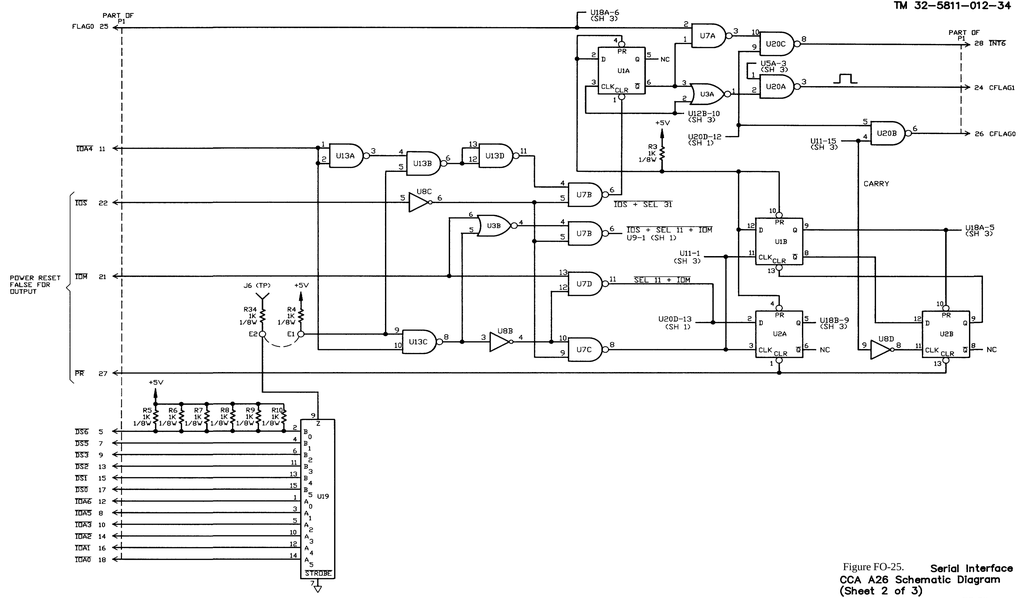


Figure FO-25. **Serial Interface CCA A26 Schematic Diagram (Sheet 2 of 3)**

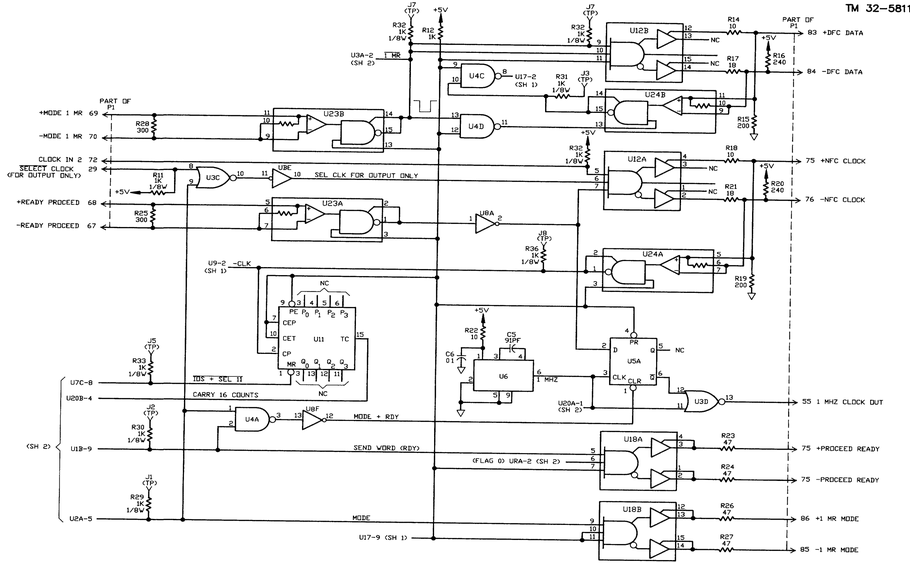
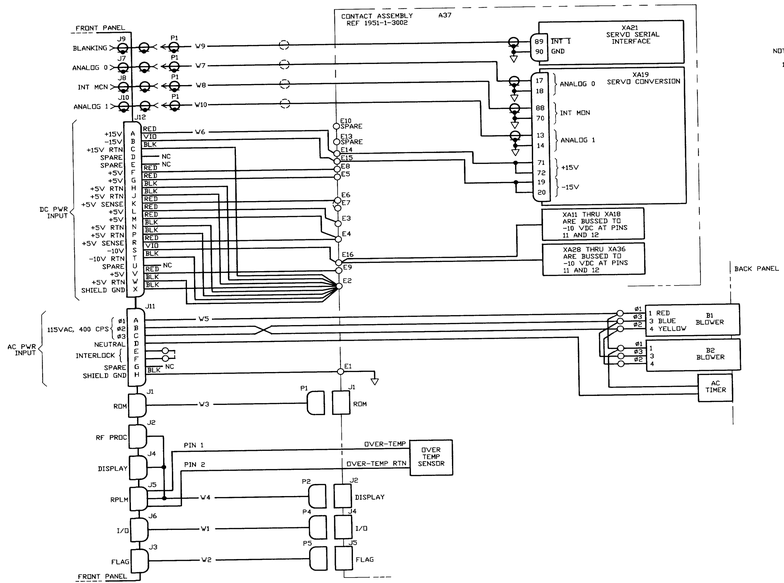


Figure FO-25. **Serial Interface CCA A26 Schematic Diagram (Sheet 3 of 3)**



NOTES:

1 FRONT PANEL CONNECTORS CHASSIS GROUND (SHIELDED) PINS ARE AS NOTED:

CHASSIS GROUND	
CONNECTOR	PIN NO
J1	100
J2	22
J3	100
J4	79
J5	22
J6	79
J11	H
J12	X

Figure FO-26. **DF Control Wiring Diagram**

By Order of the Secretary of the Army:

GORDON R. SULLIVAN
General, United States Army
Chief of Staff

Official:

MILTON H. HAMILTON
Administrative Assistant to the
Secretary of the Army

*** U.S. G. P. O. :1993-400-723:80077**

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3		2		Item 10. Change illustration. Reason: Tube end shown assembled on wrong side of lever cam.
109		51		Item 3. The NSN and P/N are not listed on the AMDF nor the MCRL. Request correct NSN and P/N be furnished.
2-8			2-1	Preventive Maintenance Checks and Services. Item 7 under "Items to be inspected" should be changed to read as follows: Firing linkage and firing mechanism pawl.
12	1-6a			Since there are both 20- and 30- round magazines for this rifle, data on both should be listed.

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