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NAVY NAVELEX 0967-LP-593-4070
AIR FORCE TO 31W2-2FCC98-2

GENERAL SUPPORT MAINTENANCE MANUAL

MULTIPLEXER SETS
AN/FCC-98(V)1 (NSN 5820-01-072-0560)
AND
AN/FCC-98(V)1X (NSN 5820-01-086-6217)

This copy is a reprint which includes current pages from Changes 1 through 3.

DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE

8 JULY 1981

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C3

Change
No. 3

DEPARTMENTS OF THE ARMY,
THE NAVY, AND THE AIR FORCE
Washington, DC, 15 May 1992

General Support Maintenance Manual
MULTIPLEXER SETS
AN/FCC-98(V)1
(NSN 5805-01-072-0560) (EIC: LFZ)
and
AN/FCC-98(V)1 X
(NSN 5805-01-086-6217) (EIC: LFO)

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2-35 and 2-36	2-35 through 2-36.1/(2-36.2 blank)
None	3-70.1 through 3-70.7/(3-70.8 blank)
3-249 and 3-250	3-249 and 3-250
None	FO-3A (Sheet 3.1 of 3)
None	FO-4A (Sheet 5.1 of 6)
FO-15	FO-15

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MULTIPLEXER SETS
AN /FCC-98(V)1 (NSN 5820-01-072-0560)
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WASHINGTON, DC, *17 May 1985*

General Support Maintenance Manual

MULTIPLEXER SETS

AN/FCC-98(V)1 (NSN 5820-01-072-0560)

AND

AN/FCC-98(V)1X (NSN 5820-01-086-6217)

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3-215 and 3-216	3-215 and 3-216
3-221 through 3-242	3-221 through 3-242
3-247 and 3-248	3-247 and 3-248
Figure FO-10 (Sheet 1 of 2)	Figure FO-10 (Sheet 1 of 2)
Figure FO-15	Figure FO-15

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5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. **DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL**
2. **IF POSSIBLE, TURN OFF THE ELECTRICAL POWER**
3. **IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL**
4. **SEND FOR HELP AS SOON AS POSSIBLE**
5. **AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION**

WARNING

· **Adequate ventilation should be provided while using trichlorotrifluoroethane. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since trichlorotrifluoroethane dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.**

· **Hazardous voltage is present inside multiplexer set even though POWER switch may be OFF. The most dangerous areas are in the vicinity of display panel assembly and rear assembly.**

· **This equipment weighs approximately 100 pounds. To avoid serious personal injury when lifting, a two-man lift is required. Check handles for damage before lifting.**

· **Compressed air shall not be used for cleaning purposes except where reduced to less than 29 pounds per square inch (psi) and then only with effective chip guarding and personnel protection equipment. Do not use compressed air to dry parts when TRICHLOROTRIFLUOROETHANE has been used. Compressed air is dangerous and can cause serious bodily harm if protective means or methods are not observed to prevent chip or particle (of whatever size) from being blown into the eyes or unbroken skin of the operator or other personnel.**

TECHNICAL MANUAL
No. 11-5805-711-40
TECHNICAL MANUAL
NAVELEX 0967-LP-593-4070
TECHNICAL ORDER
No. 31W2-2FCC98-2

DEPARTMENTS OF THE ARMY,
THE NAVY, AND THE AIR FORCE

WASHINGTON, DC, *8 July 1981*

GENERAL SUPPORT MAINTENANCE MANUAL
MULTIPLEXER SETS AN/FCC-98(V)1 (NSN 5820-01-072-0560) (EIC: LFZ) AND AN/FCC-98(V)1X (NSN 5820-01-086-6217) (EIC:LFO)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to Commander, U.S. Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-LM-LT, Fort Monmouth, NJ 07703-5000.

For Air Force, submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 6-5, Section VI, T.O. 00-5-1. Forward direct to prime ALC/MST.

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In either case, a reply will be furnished direct to you.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS-Continued

LIST OF ILLUSTRATIONS-Continued

LIST OF ILLUSTRATIONS-Continued

LIST OF ILLUSTRATIONS-Continued

LIST OF TABLES

LIST OF TABLES-Continued

CHAPTER 1
INTRODUCTION

1-1. Scope

This manual contains information for repairing components of Multiplexer Sets AN/FCC-98(V)1 and AN/FCC-98(V)IX (hereinafter called the multiplexer set) at general support. It includes troubleshooting, testing, disassembly, repair, and adjustment instructions. Functional descriptions, diagrams, and supporting data are also provided. Throughout this manual, Multiplexer Set AN/FCC-98(V) refers to both models unless otherwise indicated. The components covered I are identified in table 1-1.

1-2. Consolidated Index of Army Publications and Blank Forms

Refer to the latest issue of DA Pam 25-30 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

1-3. Maintenance Forms, Records, and Reports

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750, as contained in Maintenance Management Update. Air Force personnel will use AR 66-1 for maintenance reporting and TO-00-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performed utilizing the Maintenance Data Collection Subsystem (MDCS) IAW OPNAVINST 4790.2, Vol. 3, and unsatisfactory material/conditions (UR submissions) IAW OPNAVINST 4790.2, Vol 2, chapter 17.

b. Reporting of Item and Packaging Discrepancies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/SECNAVINST 4355.18/AFR 400-54/MCO 4430.3J.

c. Transportation Discrepancy Report (TDR)(SF361). Fill out and forward Transportation Discrepancy Report (TDR) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.3jC/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR)

a. Army. If your multiplexer set needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment: Put in I on an SF 368 (Product Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMS EL-ED-pH . Fort Monmouth, NJ 07703-5 0 07. We'll send you a reply.

b. Air Force. Air Force personnel are encouraged to submit EIRs in accordance with AFR 900-4.

c. Navy. Navy personnel are encouraged to submit EIRs through their local Beneficial Suggestion Program.

1-5. Administrative Storage

Administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS charts before storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness. Disassembly and repacking of equipment for shipment or limited storage are covered in TM 11-5805-711-13.

1-6. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

1-7. Description of Multiplexer Set AN/FCC- 98(V)

For a description of Multiplexer Set AN/FCC-98(V), refer to TM 11-5805-711-13.

1-8. Tabulated Data for Multiplexer Set AN/FCC-98(V)

Tabulated data for Multiplexer Set AN/FCC-98(V) is contained in TM 11-5805-711-13.

Table 1-1. Repairable Components, Multiplexer Set AN/FCC-98(V)

Official nomenclature	Common name	Equipment placard part number
Transmit-Receive Data Timing Group OB-91/FCC-98(V)	DTG	PCM, 17440-010 MUX, 17450-010 DRIVER, 17460-010 RCVR, 17470-010 DEMUX, 17480-010 PCD, 17500-010
Multiplexer Set Test Module TS-3693/FCC-98(V)	BITE(built-in test equipment)	BITE 17160-010
Power Supply Group OP-124/FCC-98(V)	AC PWR SPLY group	None
	Power and alarm unit	PWR SPLY, 17140-010
	AC power control panel	AC PWR CONT, 17063-010
	AC EMI filter	NONE (17020-010)
	Transformer rectifier-filter	NONE (17050-010)
Power Supply Group OP-125/FCC-98(V)	DC PWR SPLY group	None
	Power and alarm unit	PWR SPLY, 17140-010
DC control panel	DC power control panel	DC PWR CONT, 17067-010
	DC EMI filter	NONE (17020-020)
Voice Frequency Channel Module PL-1411/FCC-98(V)	VF module	EM4 VF, 17210-010
Data Interleaving Channel Module PL-1412/FCC-98(V)	0-20 kb/s data module	0-20 kb/s, 17220-010
Data Interleaving Channel Module PL-1413/FCC-98(V)	50 kb/s data module	50 kb/s, 17230-010
Multirate Synchronous Data Module PL-1414/FCC-98(V)	Multirate data module	MRSDM, 17250-010
Electrical Equipment Cabinet CY-7786/FCC-98(V)	Cabinet	17025-030

CHAPTER 2
FUNCTIONING OF EQUIPMENT

Section I. GENERAL

2-1. Introduction

This chapter provides a functional description of the multiplexer set and each of its major components. The description is arranged in eight sections. Section I describes the overall multiplexer set. It covers interfaces between individual units of the set and provides a system-level block diagram. Sections II through VIII provide block diagrams and circuit descriptions for each unit of the multiplexer set.

2-2. Multiplexer Set Description

The multiplexer set (fig. 2-1) is a first level communications terminal with full duplex transmit and receive capabilities. It functions as a time division multiplexer and employs pulse code modulation to send and receive voice, data, and signaling information via a single mission bit stream (MBS). Up to 24 separate channels are available and can be configured to various voice/data combinations by selection of four different types of channel modules (VF, multirate data, 0-20 kb/s data, and 50 kb/s data modules). All 24 channels can be used for voice frequency (VF), but only 18 can be used for digital data (channels 1 through 12 and all other odd-numbered channels). The data timing components may be configured to operate in 3-, 6-, 12 or 24-channel mode and to handle either NRZ or bipolar data formats.

a. VF Module. The voice frequency channel module provides voice and signaling interface between the data timing group (DTG) and the external VF connections of the multiplexer set. The interface function of the VF module includes level adjustment of transmitted and received VF signals and processing of idle/busy status signals. The VF module adjusts the input gain to accept either -16 dBm or 0 dBm voice signals to maintain a uniform -10 dBm output to the DTG. Also included in-the VF module is a low pass filter which suppresses all frequencies in excess of 4 kHz. If a carrier group alarm (CGA) is received by the VF module, the module terminates all calls.

b. 0-20 Kb/s Data Module. Asynchronous data at any rate from 0 to 20 kb/s can be accepted by multiplexer set channels with 0-20 kb/s data modules installed in place of VF modules. Any channel from 1 through 12, or any odd channel from 13 through 23, can be utilized by a 0-20 kb/s module. The module encodes the incoming 0-20 kb/s asynchronous data in a 2-bit transitional code which is then transmitted at a synchronous 64 kb/s rate. This 64 kb/s synchronous data stream is transferred via an output buffer to the MUX unit of the DTG at the MBS data rate.

c. 50 Kb/s Data Module. Those channels that can accept a 0-20 kb/s data module can also accept a 50 kb/s data module. This module receives incoming 50 kb/s asynchronous data and applies it to a stuff circuit. This circuit adds no information bits (stuff bits containing no user data) to the incoming data as necessary to achieve a synchronous data rate of 64 kb/s. These no information stuff bits are added in the two least significant bit positions such that they are recognizable by a destuff circuit. This 64 kb/s synchronous data stream is then transferred via an output buffer to the MUX unit in the DTG at the MBS data rate.

d. Multirate Data Module. Synchronous data at 56, 64, 128, 256, and 512 kb/s can be transmitted and received when a multirate data module, strapped for operation at the desired rate, is utilized. The multirate data module can be installed in the same channel positions described for the asynchronous data modules. Since 64 kb/s is the highest rate that can be accommodated by a single channel, multirate data modules strapped for higher rates utilize multiple channels in 64 kb/s increments as required. The multirate data module receives incoming synchronous data at the selected (by strapping) rate, buffers the data, and

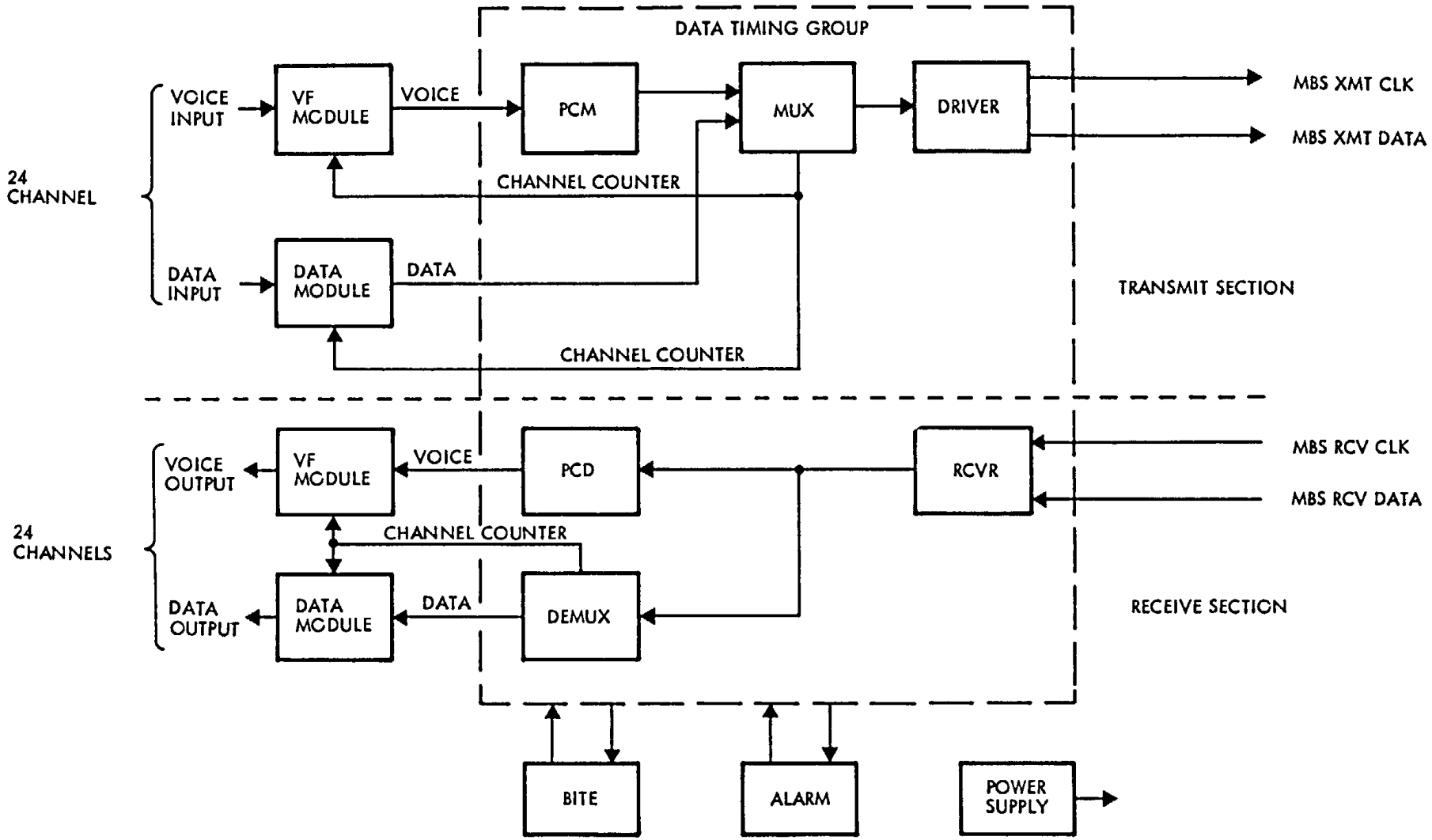


Figure 2-1. Multiplezer Set AN/FCC-98V block diagram.

applies it to the MUX unit in the DTGC at the MBS rate.

e. DTG. The DTG consists of a transmit section and a receive section. The transmit section includes the pulse .code modulator (PCM), multiplexer (MUX), and driver (DRIVER) modules. The receive section includes the receiver (RCVR), demultiplexer (DEMUX), and pulse code demodulator (PCD) modules.

(1) *Transmit section.* Transmission begins with multiplexing of the outputs from all in-use channels by the PCM module. The output of the multiplexer is sampled by a sample-and-hold circuit to produce a pulse-amplitude-modulated (PAM) signal. The PAM signal is converted to a pulse-code modulation (PCM) signal by an analog-to-digital converter. PCM is mixed with encoded data and framing bits to produce XMT MBS DATA. Timing and control signals for the PCM unit are generated by the MUX unit. The MUX unit also generates the 24 RCV CHAN CTR signals used to select channel units. In addition, the MUX unit inserts a 00001111 alarm pattern into the MBS in place of data when an alarm condition is present. The DRIVER unit buffers the XMT MBS DATA and transfers the data to the MBS XMT DATA connector at the rear of the multiplexer set. The DRIVER unit also generates XMT MBS CLK and other clock signals used by the transmit section of the multiplexer set. The clock generator may be synchronized by an external timing signal if desired. If no external timing signal is provided, the clock is produced by an internal crystal oscillator. The XMT MBS CLOCK is provided to a connector of the same name at the rear of the multiplexer set to provide clock for the communications interface. If the multiplexer set is configured for bipolar operation, no clock is provided.

(2) *Receive section.* RCV MBS CLOCK and RCV MBS DATA are converted to TTL levels by line receivers in the RCVR unit. The RCV MBS CLOCK is resynchronized by an analog phase-locked loop. RCV MBS DATA is resynchronized by a first-in-first-out buffer (FIFO) which is clocked from the recovered clock. The data and clock from the RCVR unit are then applied to the DEMUX unit. The DEMUX unit is the controller for the receive section. It detects the framing pattern and synchronizes the RCVR to the incoming data. It also contains a bit/channel counter and frame monitor. The DEMUX unit supplies serial data to the data module and channel counter signals to the VF and data modules. A PCD unit converts incoming PCM data to PAM data. This data is clocked into a serial-to-parallel register and changed to an analog signal by a digital-to-analog converter. The analog signal is demultiplexed by a 24-channel analog demultiplexer. Each of the 24 outputs is stored by a sample-and-hold circuit and filtered by a low pass filter. The outputs of the low pass filters drive the VF channel modules.

f. Alarms Module. The multiplexer set monitors both internal and external (incoming) functions and provides alarms to inform maintenance personnel of faulty operation. The alarm conditions detected include loss of power, loss of input signal, remote carrier group alarm (CGA), loss of frame synchronization, and loss of output signal. The major functions of the multiplexer set are monitored and the far-end terminal automatically notified of an alarm condition. At both terminals, voice channels are automatically busied out and data channels are forced to send all is. The same action is automatically initiated if test conditions (local loop test or remote loop test) that interrupt service are manually selected. Repair or removal of the abnormal condition automatically eliminates the alarm and restores service.

g. Built-In Test Equipment (BITE) Module. The BITE module contains a 1,020 Hz oscillator and associated attenuators that provide calibrated VF signals of various levels for patching into voice channels during alignment and testing. An ac metering circuit is also provided to measure the level of VF signals patched to BITE during testing. Signaling information (M-lead) can be produced by the BITE module and patched into a voice channel, and far-end signaling (E-lead) can be monitored with an off-hook/on-hook indicator. A dc metering circuit permits the operator to monitor each voltage output of the multiplexer set power supply. The BITE module also produces digital data streams at selectable clock rates that can be patched into data channels for testing. A test data stream can be patched back to the BITE module for error assessment after it has been looped through the data channel being tested. The BITE module compares the transmitted test pattern with the received test pattern to determine if any errors have been introduced by the data channel.

h. Power. The multiplexer set contains either an ac or a dc power supply group. The ac power supply group has a transformer rectifier-filter (TRF) circuit to convert from 117 or 230 Vac, at 47 to 420 Hz, primary power to the -44 to -56 Vdc input required by the dc-to-dc converter.

Both groups contain identical dc-to-dc converters. Each dc-to-dc converter utilizes the -44 to -56 volt input to produce multiplexer set operating voltages. In the dc power supply group, the input to the dc-to-dc converter is supplied directly by the dc primary power.

2-3. Frame Structure

The multiplexer set transmits multiplexed MBS data (MBS XMT DATA), and demultiplexes received MBS data (MBS RCV DATA) using one of four configured framing structures. The four frame structures (24-channel, 12-channel, 6 channel, or 3-channel frame format), as determined by operator configuration, are described in the following paragraphs.

a. 24-Channel Frame Format. The 24-channel framing and signaling format is shown in figure 2-2. A group of 12 frames constitutes a superframe. Each frame contains one synchronizing bit so that the receiving terminal can decode, demultiplex, and distribute the incoming bit stream properly. Each superframe contains synchronizing bits that form a 12-bit sequence (identified as framing bits in fig. 2-2). This sequence is used for frame synchronization and for marking frame numbers 6 and 12, which contain E and M signaling bits. This 12-bit sequence can be subdivided into two sequences: BF(t) (framing) and BF(s) (signaling framing). Framing bits BF(t) are odd-numbered and BF(s) are even-numbered. The BF(t) bit alternates (1-0-1-0) every other frame. The receiver locates this unique sequence in the incoming bit stream to maintain or regain frame synchronization. Frame 6 occurs when the BF(s) bit is a 1 preceded by three BF(s) Os, and frame 12 occurs when the BF(s) bit is a 0 preceded by three BF(s) l's. The receiver detects this sequence to identify these two frames.

(1) Each frame consists of 24-channel words (one for each channel) plus the BF(t) or BF(s) framing bit. Each channel is sampled 8000 times per second (8000 frames per second). The channels are sampled in numerically increasing sequence, and each framing bit occurs after channel 24 and before channel 1.

(2) Each channel word consists of eight bits (B1 through B8), which are presented serially to the MBS. Since there are 24 channels, a frame consists of 24 X 8 = 192 bits plus 1 framing bit

= 193 bits X 8000 terminal frames per second
= 1.544 Mb/s per second. The eight bits of each channel word may represent PCM voice if associated with a VF module, or digital data if associated with a data module. If voice, E and M signaling must be transmitted as well as the channel voice samples. This is done by time-sharing the least significant bit (B8) between voice and signaling. The B8 bits of each voice channel carry voice sample information for five frames, followed by one frame of signaling information. This is followed by five more frames of B8 voice and another frame of B8 signaling. This sequence is repeated every 12 frames.

(3) With some types of channel units, two separate signaling channels are required. Signaling bits carried by frame 6 are A signaling bits and those carried by frame 12 are B signaling bits. Channels with E and M signaling can operate properly using both A and B signaling bits only. When data channels are used, the signaling bit time sharing of B8 bit is inhibited. Thus, the full 8-bit sample is available, yielding 8 bits X 8000 samples per second = 64 kb/s of data transmission per channel.

b. 3-Channel Frame Format. The format for the 3-channel mode of operation is shown in figure 2-3. The superframe consists of 24 frames, each of which consists of three channel words. The channel words consist of eight bits each, and the frame rate is 8000 frames per second. (Each channel is still sampled 8000 times per second.) In this mode, no extra bandwidth is allocated to farming, and the frame is 3 X 8 = 24 bits. The MBS rate is 24 X 8000 = 192 kb/s. Framing bits are transmitted in B8 of channels 1, 2, and 3 during frames 12 and 24. The signaling bits are transmitted in B8 for voice only channels during frames 6 and 18. Signaling is suppressed for data channel modules so that the full 64 kb/s data stream is available except for B8 framing bits in frames 12 and 24. The A signaling and BF(t) framing bits are time-shared in the following manner. Each channel is transmitted as an 8-bit word for frames 1 through 5, 7 through 11, 13 through 17, and 19 through 23. During frames 6 and 18, each voice channel is transmitted as a 7-bit word plus signaling, and each data channel is transmitted as an 8-bit word. During frames 12 and 24, channels 1, 2, and 3 are transmitted as a 7-bit word plus a framing bit in position B8. The framing bits occur at the same rate as the signaling bits. Once frame synchronization is achieved, the position of the signaling bits is uniquely determined without a BF(s) pattern as for the 24-channel code. Framing bits follow a unique pattern to ensure optimal frame synchronization. Every 12th frame, the polarity of the framing bits of channels 1, 2, and 3 is reversed so that the

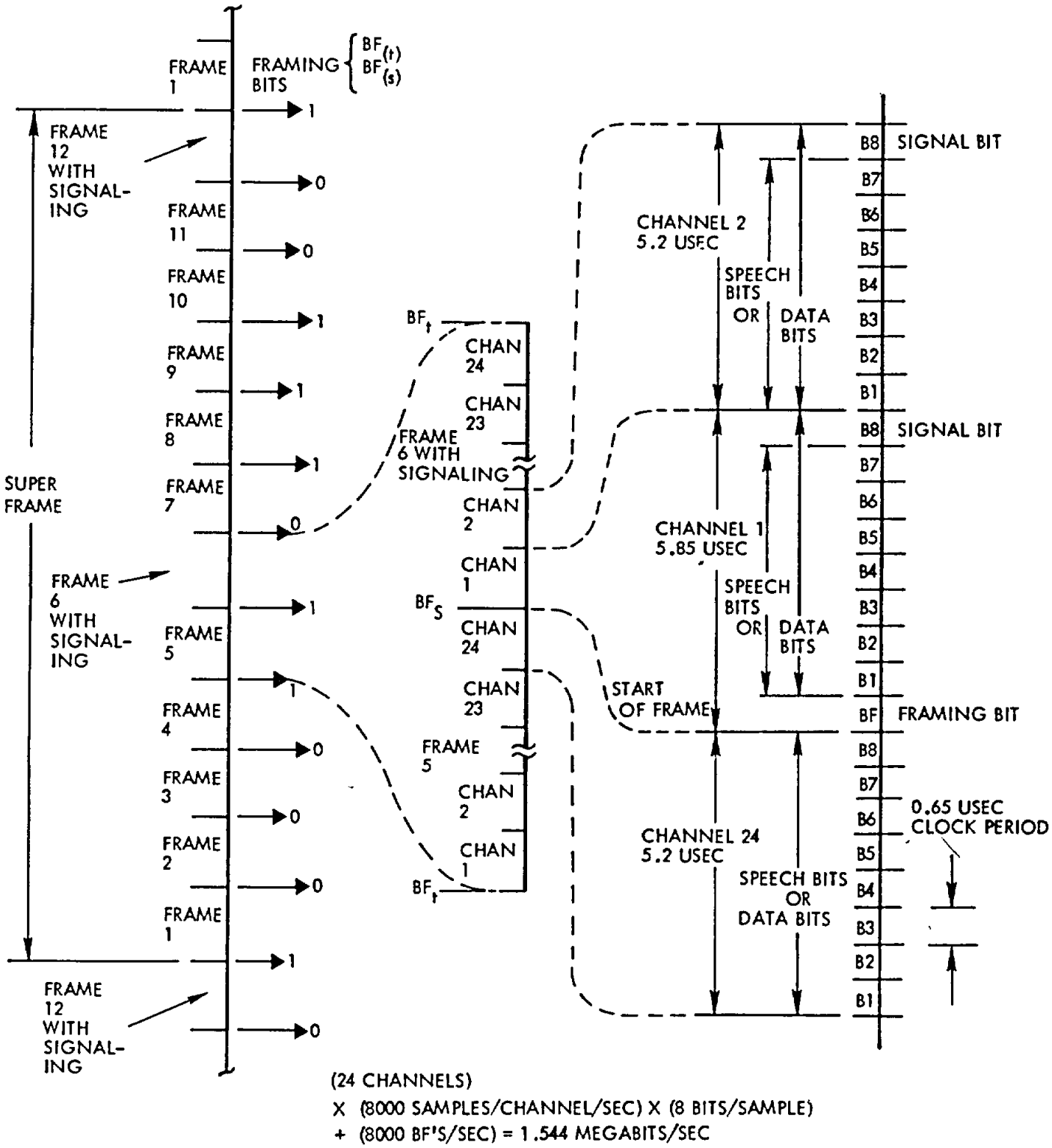


Figure 2-2. 24-channel frame structure.

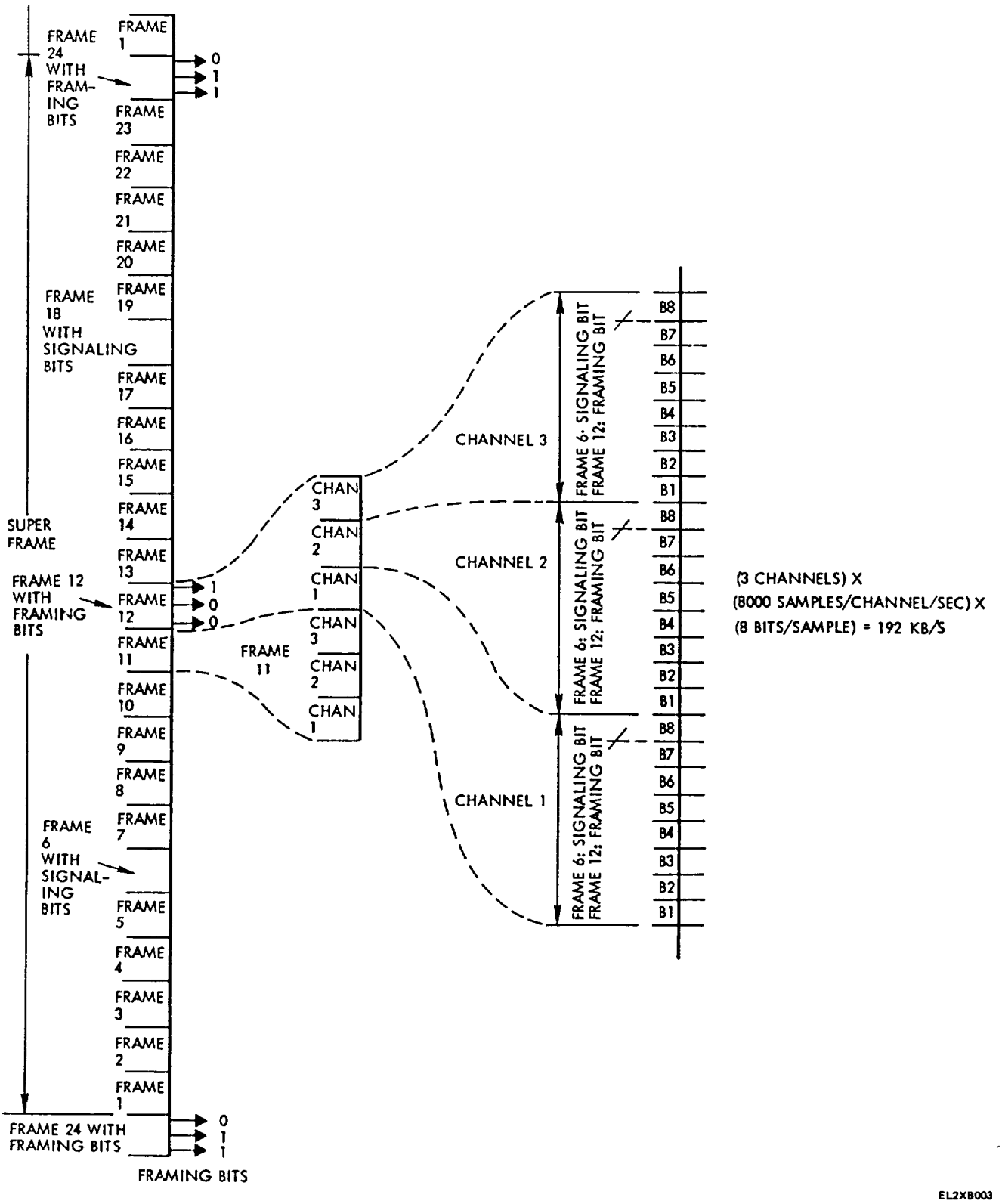


Figure 2-3. 3-channel frame structure.

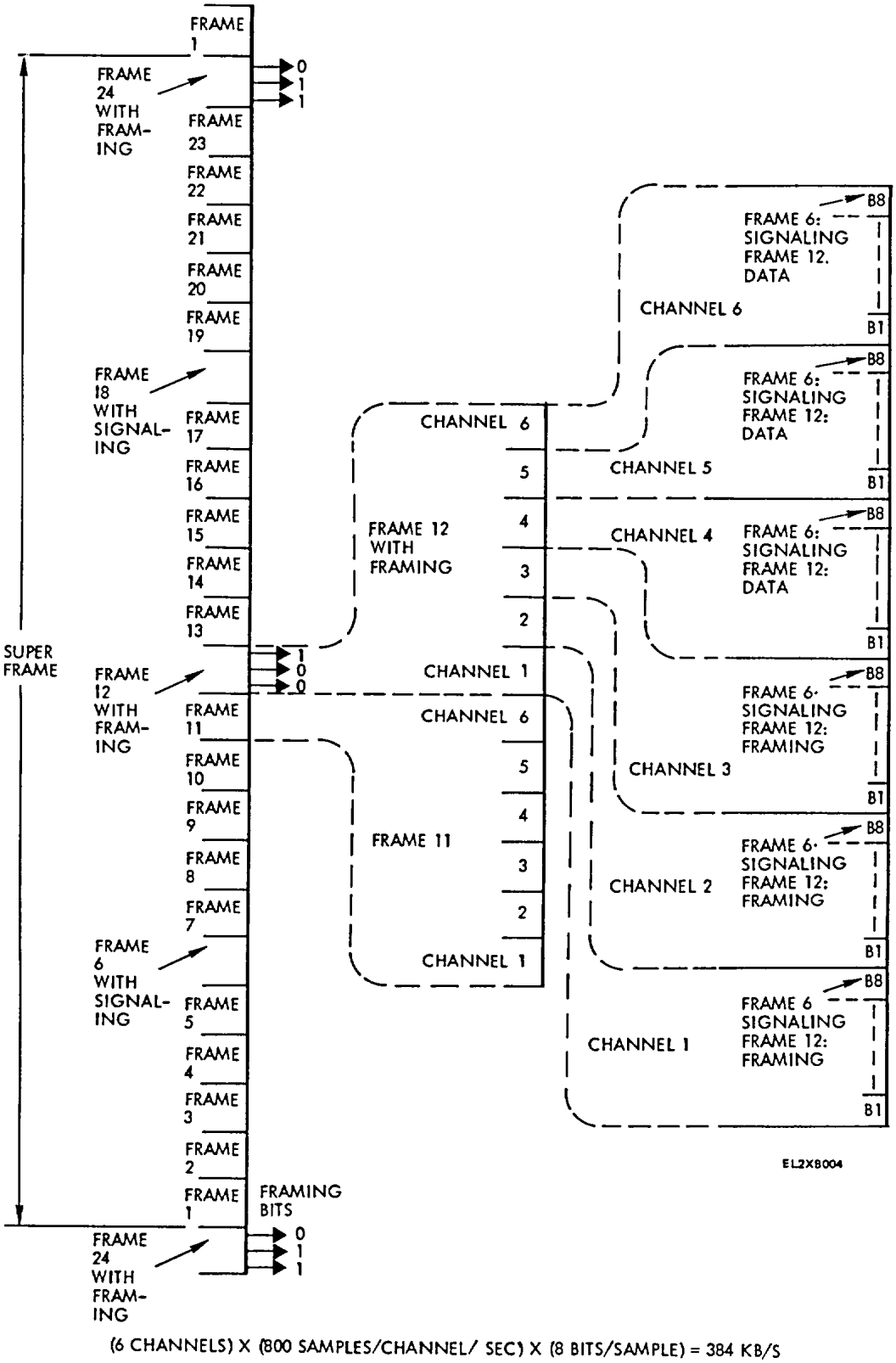


Figure 2-4. 6-channel frame structure.

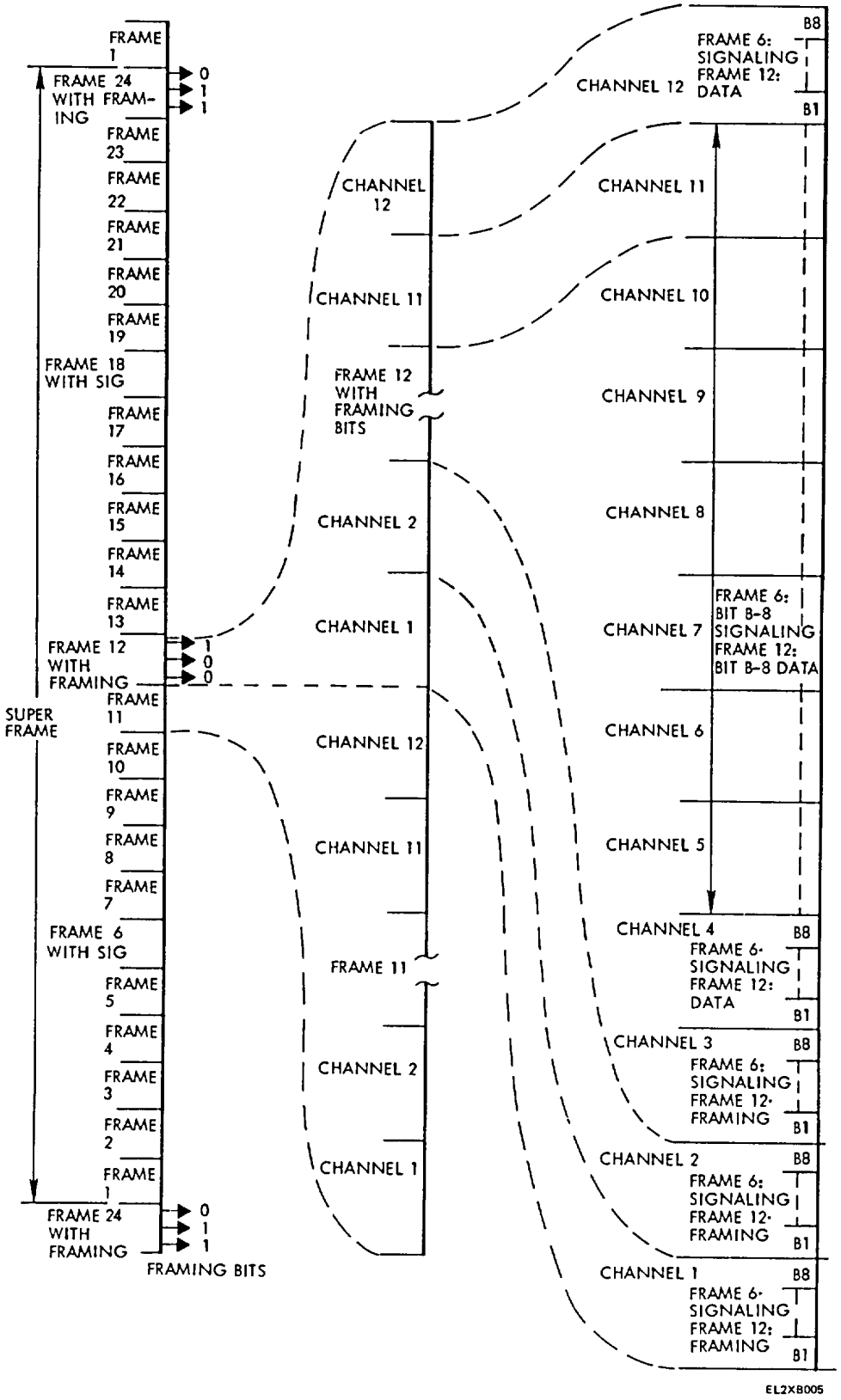


Figure 2-5. 12-channel frame structure.

001 pattern appears followed by the 110 pattern 12 frames later. This pattern repeats continually. The data is split into two paths. One is delayed 12 frames; the other is undelayed. The two data streams are continuously compared in an exclusive OR circuit for a sequence of three 1 bits spaced 8 bits apart, and repeating every 12 frames. This comparison is used to achieve frame acquisition. Once achieved, the signaling data can be located during the 6th and 18th frames, midway between frame data.

c. 6-Channel Frame Format. The format for the 6-channel mode of operation is shown in figure 2-4. The superframe contains 24 frames, each of which contains six channels. There are, therefore, 48 bits per frame and 1152 bits per superframe. Signaling occurs in B8 of each voice channel in frames 6 and 18. Framing occurs in B8 of channels 1, 2 and 3 of frames 12 and 24. Framing bits follow a unique pattern. Every 12th frame, the polarity of the framing bits is reversed so that 001 appears and is followed by 110 12 frames later. The framing pattern occupies B8 of channels 1, 2, and 3 every 12th terminal frame, just as for the 3-channel modes.

d. 12-Channel Frame Format. The 12-channel frame format (fig. 2-5) follows directly from the 3-channel and 6-channel formats already described. The superframe contains 24 frames and each frame contains 12 channels, yielding 96 bits per frame and 2304 bits per superframe. The MBS is transmitted at 768 kb/s. Signaling occurs in B8 of each voice channel in frames 6 and 18; framing occurs in B8 of channels 1, 2 and 3 of frames 12 and 24.

Section II. DATA TIMING GROUP

2-4. General Information

The DTG is the element of the multiplexer set that performs all functions required to multiplex and demultiplex information provided by the voice and data modules. To accomplish this, the data timing group develops timing and framing information, encodes and decodes analog voice signals, interfaces with its associated data channel units, and interfaces with the far-end terminal via the multiplexer output data, demultiplexer input data, and clock signals. Additional signals provide alarm and control functions as required for specified operation. The functional description of the DTG is divided into two sections: the transmit section and the receive section.

a. Transmit Section. Voice frequency data from the VF modules (fig. 2-6) is sampled by a 24 channel analog multiplexer in the PCM unit and then converted to PCM by the A-to-D encoder. After signaling information is added by the output control in B8 of frame 6, the transmit PCM data (delayed 16 bits to correct for the 16-bit VF conversion time) is multiplexed with the encoded data from the digital channel units by the digital MUX. Framing bits and the OGA pattern are also multiplexed with the data as controlled by the frame/OGA/voice/data control circuit. The transmit data is then applied to the bipolar driver or NRZ driver of the DRIVER unit as applicable. The DRIVER unit generates the MBS clock by dividing the output from a 24.704 MHz crystal oscillator (internal clock operation) or by selecting the output from a phase lock loop synchronized to an external timing source. Whenever an external timing source is available, an activity detector enables the clock source selector to select the external signal. If the external signal fails, switchover to the internally generated MBS clock is automatic. During internal clock operation, a clock select circuit selects the required MBS clock as determined by the multiplexer set configuration mode switches (configuration information is also supplied to the data bus control logic). The MBS clock rate selected by the clock select circuit is applied to two identical clock driver circuits, one for MBS clock and one for MBS REF CLOCK. In the bipolar mode, the clock and data are applied to the bipolar driver. A fault decoder monitors the NRZ clock and data outputs and the output from the 16 kHz phase lock loop. If loss of output occurs, the fault decoder sends an alarm enable to the multiplexer set alarm circuits. When the 16 kHz phase lock loop receives a reset channel one signal (RC1) from the data bus control logic, a 16 kb/s signal is supplied to the multiplexer set power supply to synchronize the power converter to the beginning of frame (channel 1). The data bus control logic also supplies channel counters to the VF and digital channel units and timing to the PCM for control of data bus operation.

b. Receive Section. The MBS NRZ clock and data received by the RCVR unit of the DTG (fig. 2-7), are applied to clock and data receivers. Bipolar MBS is applied to a bipolar clock/data recovery circuit via a bipolar receiver. The bipolar clock recovery circuit separates the clock and data and applies them to the bipolar/NRZ select circuit which selects the applicable format. The selected clock and data is then supplied to an elastic store

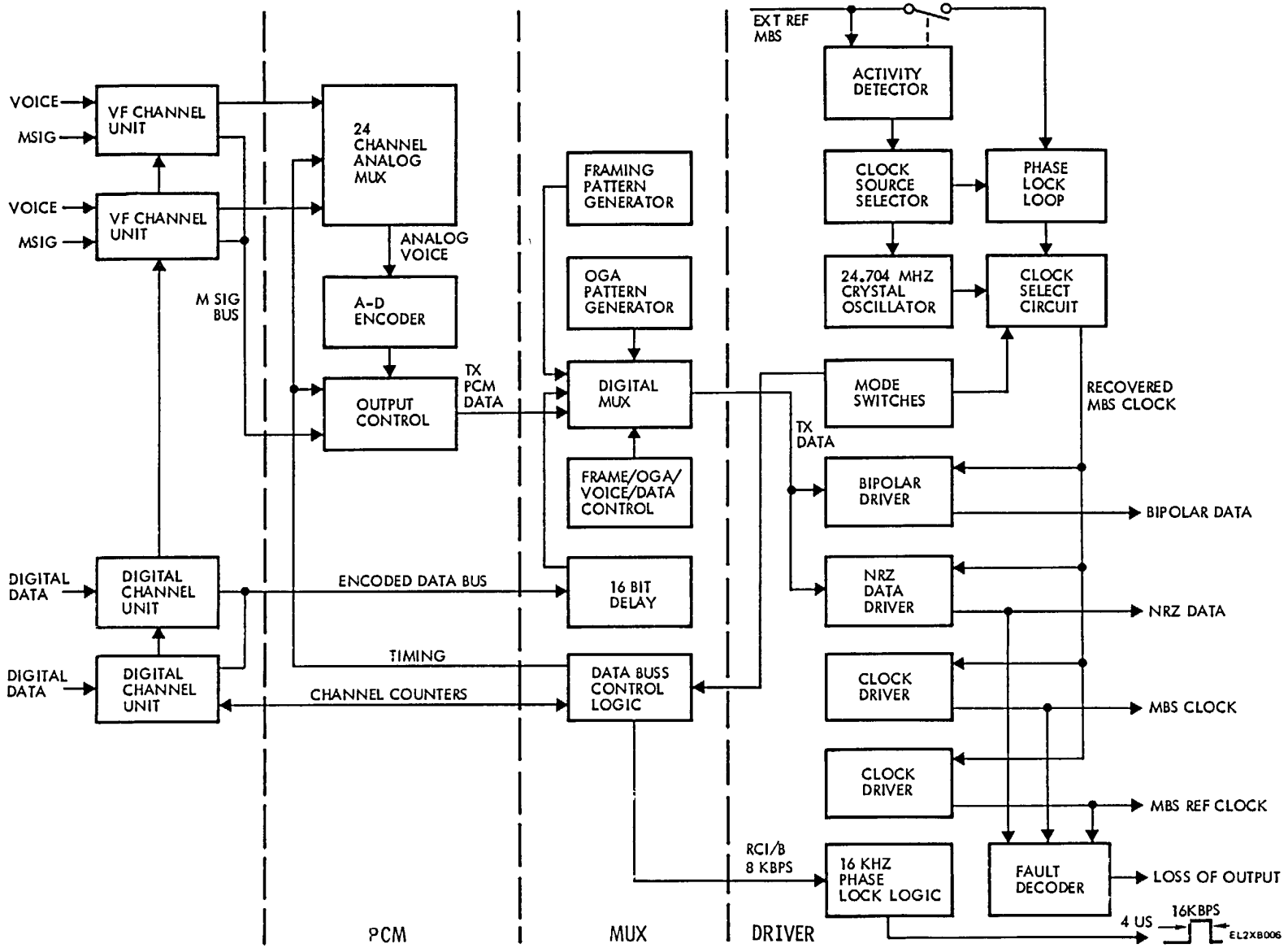


Figure 2-6. Multiplexer set transmit section block diagram.

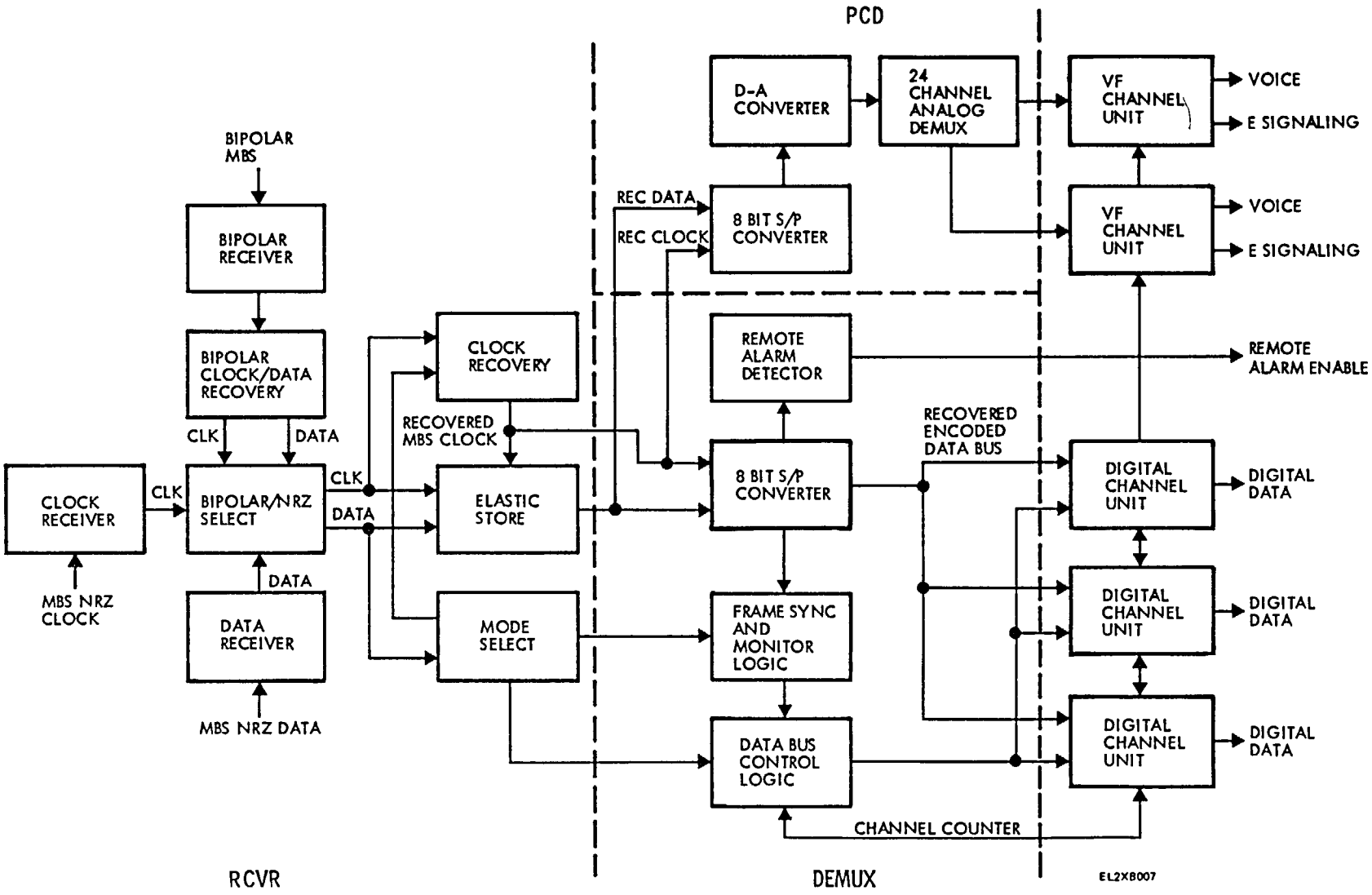


Figure 2-7. Multiplexer set receive section block diagram.

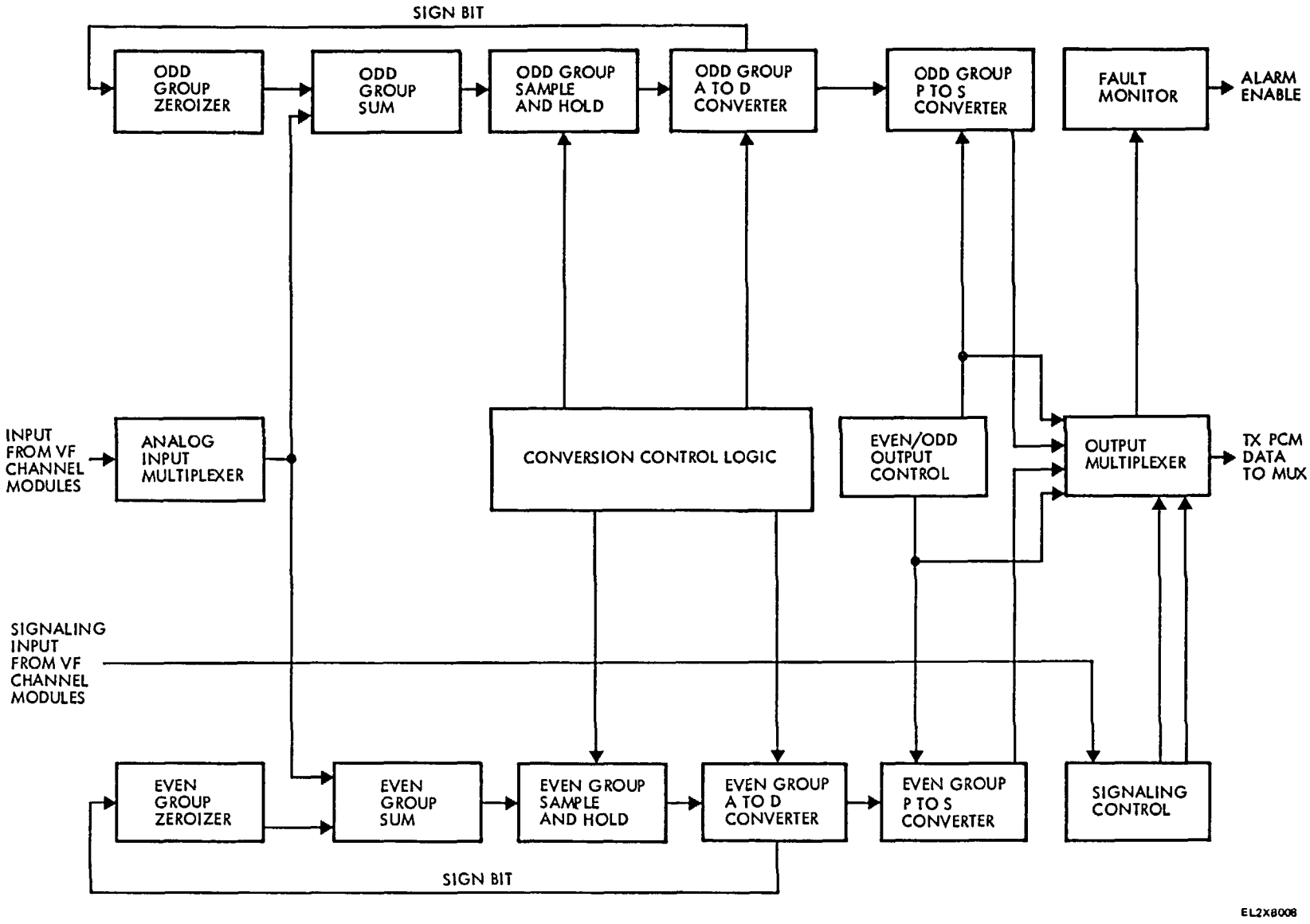


Figure 2-8. PCM unit block diagram.

which resynchronizes the data with the recovered MBS clock from the clock recovery circuit. The clock recovery circuit selects the applicable MBS clock rate as controlled by the multiplexer set configuration switches of the mode control circuit. The mode select circuit is user-programmed to select the mode of operation and the number of channels the multiplexer set will receive. Mode control signals are also supplied to the frame sync and monitor and data bus control logic of the DEMUX unit to provide frame sync and control of the data bus. The frame sync and monitor circuit detects the frame pattern and synchronizes the channel counter to the far-end set. The recovered data from the elastic store is applied to two 8-bit serial-to-parallel converters along with the recovered clock from the clock recovery circuit. The 8-bit serial-to-parallel converter in the DEMUX unit delays the data eight bits before applying it to the data channel modules. This corrects for the 8-bit delay caused by the PCM-to-VF conversion. The parallel output of this converter is also decoded by the remote alarm detector which detects a remote alarm and supplies a remote alarm-enable signal to the multiplexer set power supply. The second 8-bit serial-to-parallel converter supplies an 8-bit parallel word to a digital-to-analog converter. The output of the D-to-A converter is demultiplexed by a 24 channel analog demultiplexer which distributes the VF data to the channel modules at the correct channel times as determined by the receive channel counter from the data bus control logic. The channel counter provides 24 outputs, one for each of the 24-channel modules.

2-5. DTG Major Functions

Subparagraphs *a* through *f* below describe the overall operation of each module within the DTG.

a. PCM Unit. VF and signaling information (fig. 2-8) is received from the VF channel modules by the PCM unit and supplied to an analog input multiplexer. The analog multiplexer multiplexes the incoming signals to provide a signal analog signal containing the VF information. The multiplexed VF data is sampled by the odd group sample-and-hold and the even group sample-and hold at a time determined by the conversion control logic. The outputs of the sample-and-hold circuits remain constant over the entire conversion period of the odd group A-to-D converter and the even group A-to-D converter. The outputs of the A-to-D converters are loaded into the odd P-to-S converter and the even P-to-S converter, respectively, and shifted out serially. The even/odd output control provides timing and control signals for the two parallel-to-serial converters and the output multiplexer. The signaling information is multiplexed onto the PCM data or bit 8 (LSB) of each channel during frames 6 and 18 by the signaling control which overrides the PCM data when a signaling bit is to be inserted. The zeroizer circuits correct for offsets caused by the ratio of + and - sign bits and produce a dc output which is summed with the analog data from the input multiplexer. The fault monitor circuit monitors the data from the A-to-D converters and the conversion complete signals and provides a visual indication when these signals are not present. The fault alarm bus is also pulled low whenever there is a fault.

b. MUX Unit. The MUX unit consists of two functional sections, the data formating section and the channel counter section.

(1) *Data formating*. Digital data from the digital channel modules (fig. 2-9) is received by the MUX unit and applied to a 16-bit data delay circuit and zero suppress circuit. Encoded PCM data from the PCM unit is applied to the zero suppress circuit and the voice/zero suppress/1 kHz tone multiplexer. The 16-bit data delay circuit delays the received real time data by 16 bits to enable it to be interleaved with VF data at the proper channel time. An OGA pattern is also supplied from the OGA control circuit to the 16-bit data delay when an outgoing alarm is received from the power supply and a transmit full alarm select signal is received from the DRIVER unit. The delayed data or OGA pattern, if received from the OGA control circuit, is supplied to the data/voice/frame MUX. The zero suppress circuit is used only when the multiplexer set is configured for 24-channel bipolar operation and a data module is strapped for alternate channel operation (a zero suppress signal is supplied to the MUX unit from the DRIVER unit). If all eight bits in the data channel are 0, and B1 through B6 of the VF channel following the data channel are 0, or if the data channel following the VF module is 0; then a 1 is injected in the B7 location of the VF channel. This prevents loss of bit synchronization in the far-end terminal during periods when the mission bit stream is zero for long periods of time. When a data/voice-enable signal is received by the zero suppress circuit, a zero suppress signal is supplied to the voice/zero suppress/1 kHz tone MUX. The voice/zero suppress/1 kHz tone MUX also receives a digital word from the 1 kHz digital tone generator. This

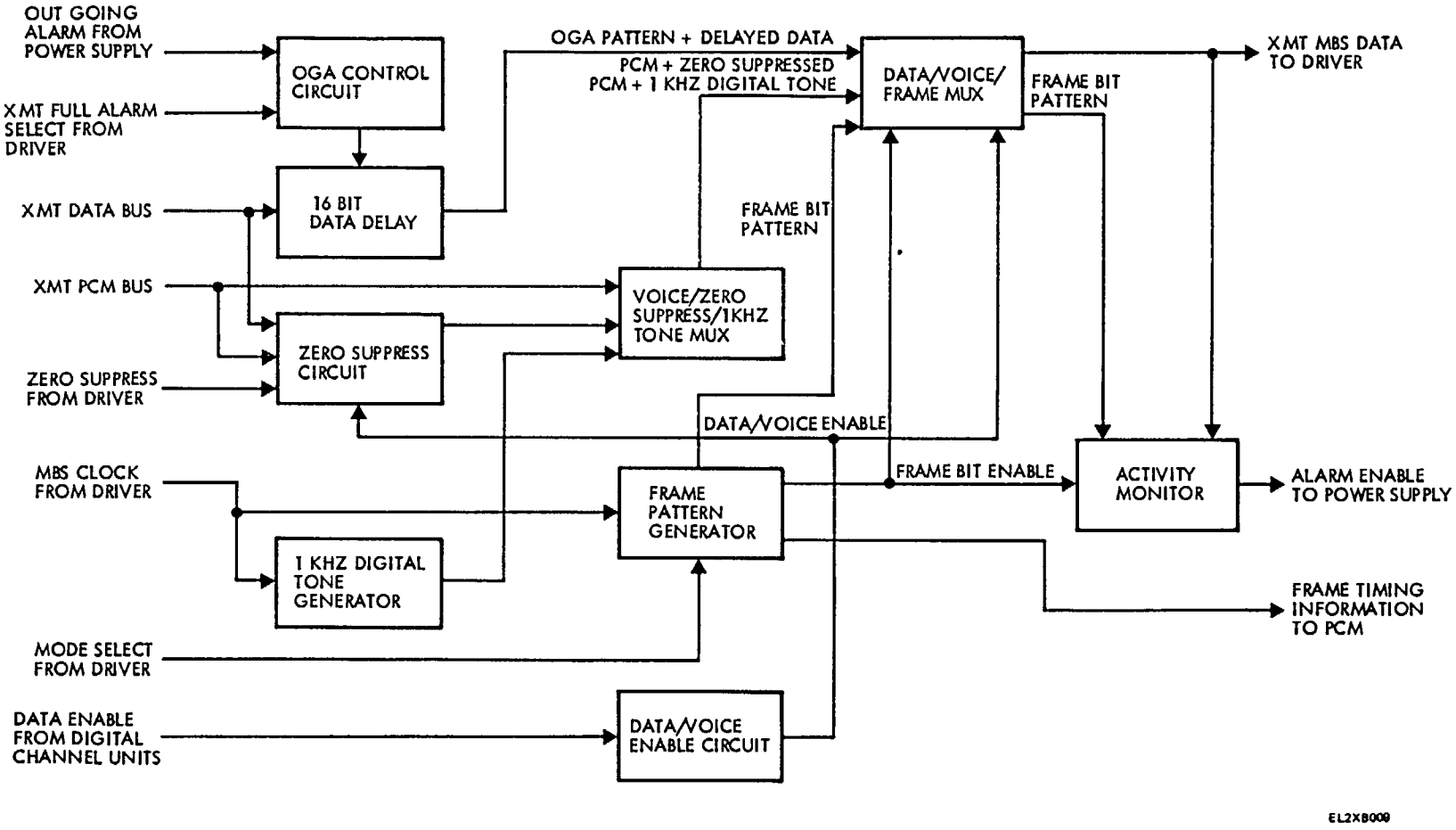


Figure 2-9. MUX unit data formatting section block diagram.

digital word is derived from the MBS clock and decoded by the VF modules at the far-end of the system to provide a 1 kHz sine wave. The voice/ zero suppress/1 kHz tone MUX then selects either PCM, zero suppressed PCM, or the 1 kHz digital tone and supplies it to the data/voice/frame MUX. The data/voice/frame MUX, as enabled by the data/voice enable and frame bit enable, interleaves the received digital data, PCM data, and framing bits to form the MBS data. The data/voice enable is supplied from the data/voice enable circuit as controlled by a data enable signal from the digital channel units. The frame bit pattern is supplied from the frame pattern generator (frame timing information is supplied to the PCM unit) as clocked by the MBS clock and enabled by the mode select signals from the DRIVER unit. The MBS data is then transferred to the DRIVER unit and activity monitor. The activity monitor also receives the frame bit enable and frame bit pattern. If the activity monitor detects a loss of frame bit pattern, frame bit enable, or MBS data, an alarm enable is - generated and supplied to the multiplexer set power module to illuminate a fault lamp. For 17450-020 versions, the zero suppress circuit injects a 1 in bit 7 whenever bits 1 through 7 are all zeroes on any given VF channel.

(2) *Channel counter.* The bit/channel counter (fig. 2-10) as clocked by the MBS clock, generates timing (sequencing) signals which are supplied to the bit counter decode and channel counter decode (encoded bit count and encoded channel count, respectively). The encoded channel count output from the bit/channel counter is also supplied to the PCM unit. The bit counter decode, as clocked by the MBS clock and controlled by the channel counter decode, determines the sequencing of bits in each channel and supplies a bit count to the channel counter control and reset circuit. Timing signals derived from the bit count decode are also supplied to other circuits within the MUX unit. The channel counter decode keeps track of the channel count and supplies the count to the channel counter control and reset. Channel counters (24-channel control signals) are also supplied to the channel modules to specify transmit times. The channel counter control and reset ensures proper sequencing of the bit/channel counter by providing a reset signal. The reset signal loads the bit/channel counter to its starting value and restarts the MUX unit at its. channel 1 position. An MBS clock is used to clock the channel counter control and reset and a transmit mode enable signal indicates the MUX unit's mode of operation (3-, 6-, 12-, or 24-channel).

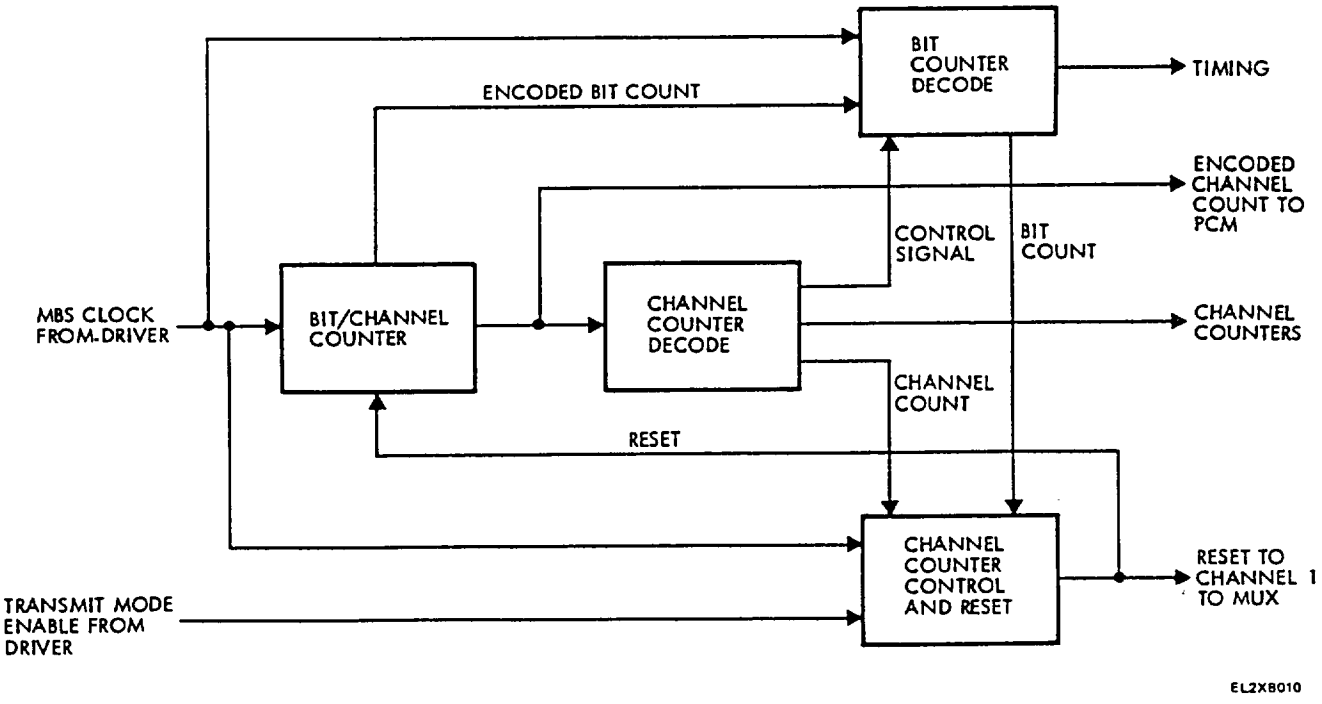


Figure 2-10. MUX unit channel counter section block diagram.

c. DRIVER Unit. The DRIVER unit is functionally divided into two sections, the timing section and the output drivers section.

(1) *Timing.* The external timing source input (fig. 2-11) is applied to a level translator via the 78-ohm balanced external timing source receiver. The level translator converts the 0 to +5 volt output of the receiver to a -5V to 0 logic level and applies it to a phase-locked loop and external clock activity monitor. The phase-locked loop provides an output to the clock source select synchronized to the external timing input. An internal oscillator also supplies an input (24.704 MHz) to the clock source select for use during the internal clock operational mode. If the external clock activity monitor detects a loss of the external clock, the clock source select automatically selects the internal clock mode. The output from the clock source select circuit is then applied to a clock divide chain which divides the frequency of the input down to various levels. All output clocks from the clock divide chain are then supplied to the clock MUX and fault monitor. Channel mode signals from the mode select are used to select one of the clocks applied to the clock MUX corresponding to the mode selected by the mode select circuit. The MBS clock output from the clock MUX is then supplied to the MUX unit and fault monitor. The mode select also supplies channel mode signals to the MUX and PCM units to select the number of channels the multiplexer set will transmit. Zero suppress and transmit full alarm select signals are supplied to the MUX unit to select zero suppressor operation and the full remote alarm select function. If the fault monitor detects a loss of output from the clock divide chain, clock MUX, or the 16 kHz phase lock loop, it transmits a loss of output signal via the alarm bus to the fault alarm light. The 16 kHz phase lock loop provides a 16KPPS signal to the power module to synchronize switching during channel 1 reset and also reduces switching noise.

(2) *Output drivers.* MBS clock and data from the MUX unit (fig. 2-12) are first applied to the data input enable logic. Unless a local loop enable signal is received, the MBS data is then supplied to the 78-ohm balanced MBS data output driver, the 100-ohm bipolar MBS data output driver, and the loss of output detector. If a local loop enable signal is received by the data input enable logic, the MBS data is replaced by loopback data. Data received by the 78-ohm balanced data output driver is clocked out of the driver by the MBC clock and supplied to the 100-ohm bipolar MBS data output driver. An operator select switch within the bipolar driver selects either the NRZ MBS data or the bipolar MBS data and supplies it to the output of the driver. The data is clocked out by the MBS clock. The loss of output detector monitors both the MBS clock and data and generates an alarm-enable if loss of output occurs. The MBS clock is also supplied to a 78-ohm balanced NRZ MBS clock output driver and a 78-ohm balanced master clock output driver. The drivers provide the NRZ MBS clock and master clock outputs from the multiplexer set, respectively.

d. RCVR Unit. The RCVR unit is functionally divided into two sections: the receivers section and the timing section.

(1) *Receivers.* MBS data received by the multiplexer set (fig. 2-13) is supplied to the input data select circuit of the RCVR unit. The input data select circuit selects between the NRZ or bipolar format and applies the input data to the applicable data receiver. The NRZ data is then transferred via a level translator to the NRZ/bipolar MUX. The level translator converts the 0 to +5 volt output of the receiver to a -5V to 0 logic level. Bipolar data is transferred to the bipolar data/clock recovery circuit, which separates the data and clock and applies them to the NRZ/bipolar MUX. The fourth input to the NRZ/bipolar MUX is the NRZ clock received from the 78-ohm clock receiver via a level translator. The MUX then selects between NRZ or bipolar data and clock and supplies the applicable data and clock to the loop MUX. Data is also supplied to the all ones/remote loop detector which detects any loss of data for a period longer than the period of the data pulse. If such a loss is detected, a remote loop alarm enable is generated to cause the remote loop alarm indicator to illuminate. The loop MUX, which also receives loopback clock and data, selects between the loopback mode and the true data and clock received. To choose the loopback mode, the loop MUX must receive a loopback enable from either the external or internal loopback circuits. If an external loopback signal is received by the external loopback receiver, a level shifter converts the TIL-level signal to a -5 volt level and applies it to the loop MUX as loopback enable. The loopback select provides an operator-controlled internal loopback mode. Whenever the RCVR unit front panel loopback switch is set to LOOP, the loopback select supplies a loopback enable to the loop MUX. The output of the loop mux (MBS data and MBS clock) is supplied to the loss of input detector and to the timing circuits of the RCVR unit. If

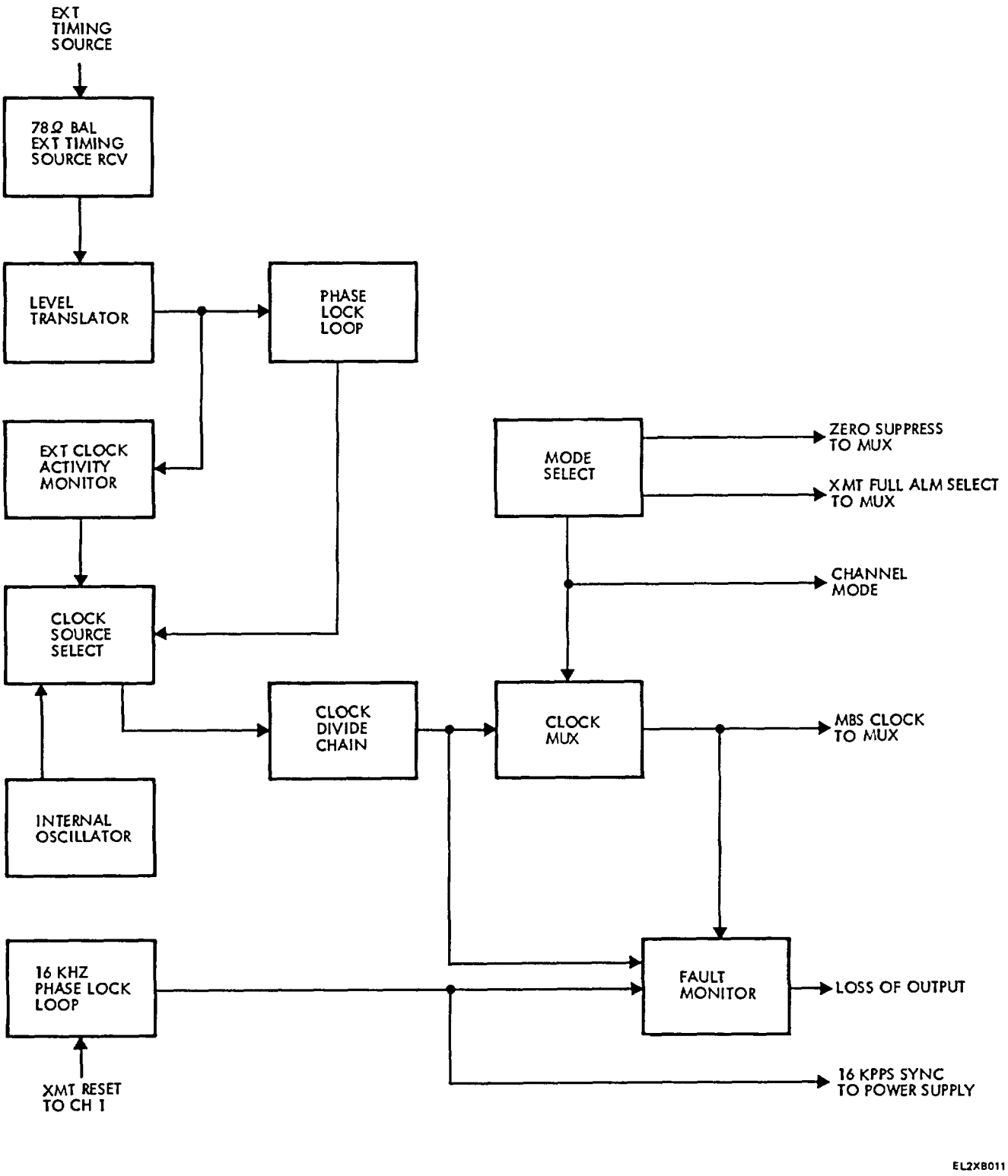


Figure 2-11. DRIVER unit timing section block diagram.

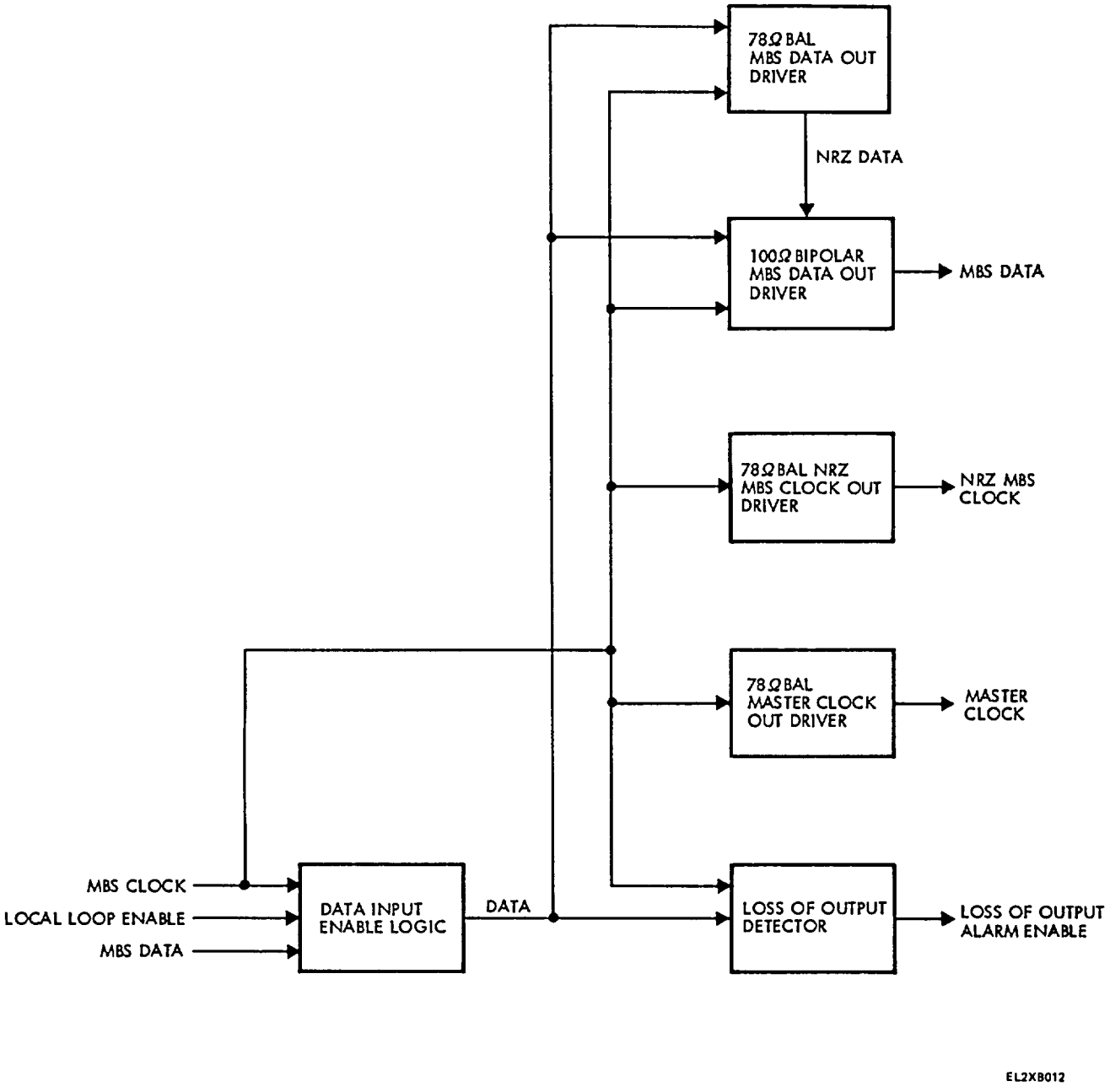


Figure 2-12. DRIVER unit output drivers section block diagram.

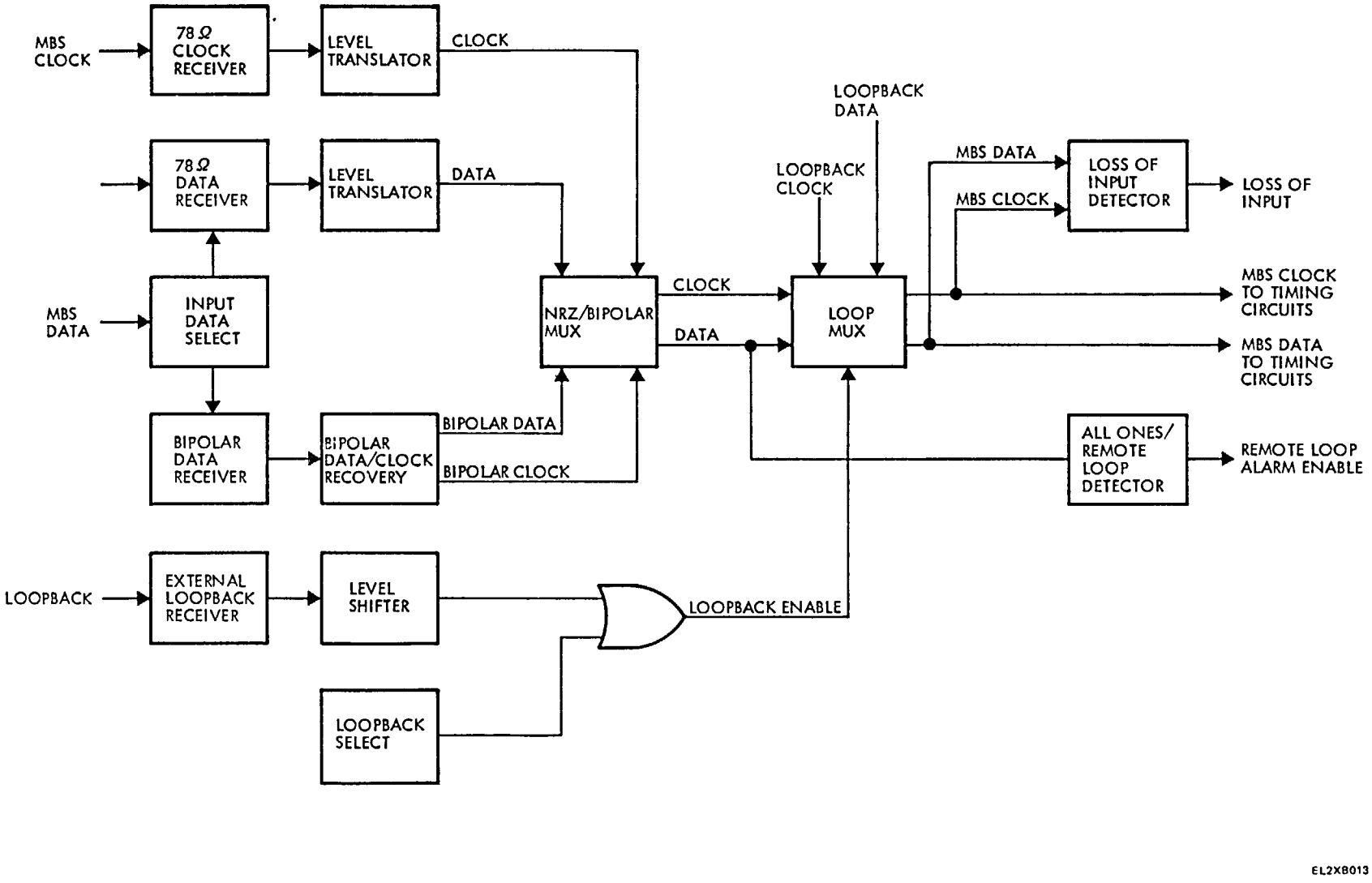


Figure 2-13. RCVR unit receivers section block diagram.

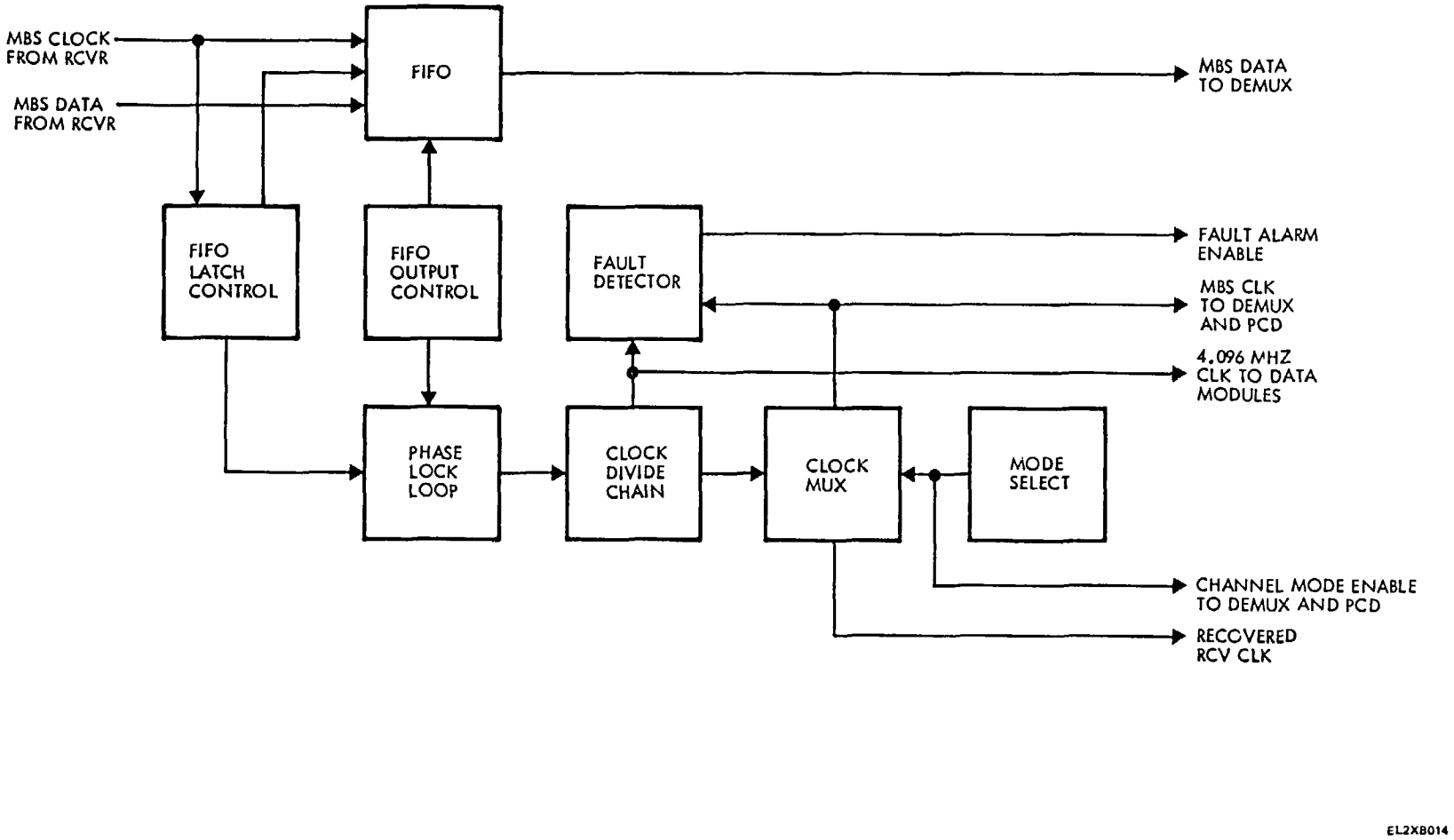


Figure 2-14. RCVR unit timing section block diagram.

the loss of input detector detects a loss of either the MBS data or clock, a loss of input alarm signal is supplied to the ALARM module.

(2) *Timing.* MBS clock and data received from the receivers section of the RCVR unit (fig. 2-14) are supplied to a FIFO. The FIFO is used to synchronize the received data with the recovered clock. The FIFO latch control, as clocked by the received MBS clock, loads the serial data received by the FIFO into a latch. The latch then stores the data until the FIFO output control supplies a load signal to the FIFO which causes the FIFO to transfer the data to the output of the RCVR unit. The FIFO latch control also divides the MBS clock by eight and supplies it as the V input to the phase lock loop. A similar signal is supplied by the FIFO output control as the R input to the phase lock loop. The phase lock loop synchronizes the phase of the two input signals and generates a 27.704 MHz clock which is supplied to the clock divide chain. The clock divide chain then divides the input clock to provide various output frequencies selectable by the clock MUX and also supplies a 4.096 MHz clock to the clock divide chain of the data modules. The clock MUX selects the applicable input clock as controlled by the channel mode enable signals from the mode select. Operator controlled switches of the mode select logic are set to select the required receive channel format. The channel mode enable from the mode select logic and the MBS clock from the clock MUX are both supplied to the DEMUX and PCD units. The recovered receiver clock from the clock MUX is supplied as an output from the multiplexer set for system timing applications. A fault detector monitors both the MBS clock from the clock MUX and 4.096 MHz clock from the clock divide chain. If the fault detector detects a loss of either input, a fault alarm enable is generated to illuminate an alarm indicator.

e. DEMUX Unit. The DEMUX unit (fig. 2-15) is functionally divided into three sections, the 24 channel acquisition section, the low rate (3, 6, or 12 channel) acquisition section, and the channel counter. The 24 channel and low rate acquisition sections use circuitry common to both. Portions of the DEMUX unit which are used for the 24-channel and low rate acquisition sections are described for the 24-channel mode only.

(1) *24-channel acquisition.* RCV MBS DATA from the RCVR unit is clocked through the data input shift register by RCV MBS clock. The data input shift register is a 36-bit register tapped every eight bits to provide a 3-bit output. This output is supplied to the pattern detector to locate frame bit and superframe candidates during the low rate mode. The data input shift register also supplies an 8-bit parallel word to the remote alarm detector. If B2 is 0 at the end of a channel time, the remote alarm line will go high indicating that a remote alarm has been received. If the multiplexer set is strapped for B2 = 0 + 00001111, the 00001111 condition will be detected during channel times which contain digital information. Initially, the cycle counter and the state counter of the control unit are the 0 state. The acquisition counter (÷N counter) is preset to a number equal to 256 minus the number of bits in one frame as determined by the mode select logic. When the acquisition counter reaches a count of 240, an operational gate signal (OGAT) is produced. The operational gate is 16 clocks wide. During the OGAT time 16 data bits are written into the first 16-bit register in the 24-channel pattern storage. When OGAT is terminated, the cycle counter advances to state 1 and the acquisition counter is again loaded with the preset data from the mode control logic. At the next OGAT the data in the first 16 locations in the 24-channel pattern storage is shifted into the second 16 locations while new data is shifted into the first 16 locations of the 24-channel pattern storage. At the end of the second OGAT, the cycle counter is advanced to state 2. After four OGATS, the 24-channel pattern storage contains a history of the 16-bit window of the previous four frames and the cycle counter is in state 4. During the first four states of the cycle counter, the sieve memory circuit was filled with 1's. When the cycle counter enters state 4, the control unit is preset to state 4. The control unit is the sequence controller and frame bit error monitor for the DEMUX unit. When the control unit enters state 4, the DEMUX unit enters the search mode. Data from the 24-channel pattern storage is then applied to the data prediction and check logic at the next OGAT. The data prediction and check logic predicts what the next bit in the frame pattern should be from the previous four frame bits. Thus the sixteen 4-bit histories stored in the 24-channel pattern storage may be examined during the acquisition cycle. If the bit predicted from these candidates compares favorably with the incoming data bit of the next frame, the candidate is said to be valid and the sieve bit which corresponds to that location in the 24-channel pattern storage is left a 1. If the predicted bit and the data bit do not compare favorably, the bit in

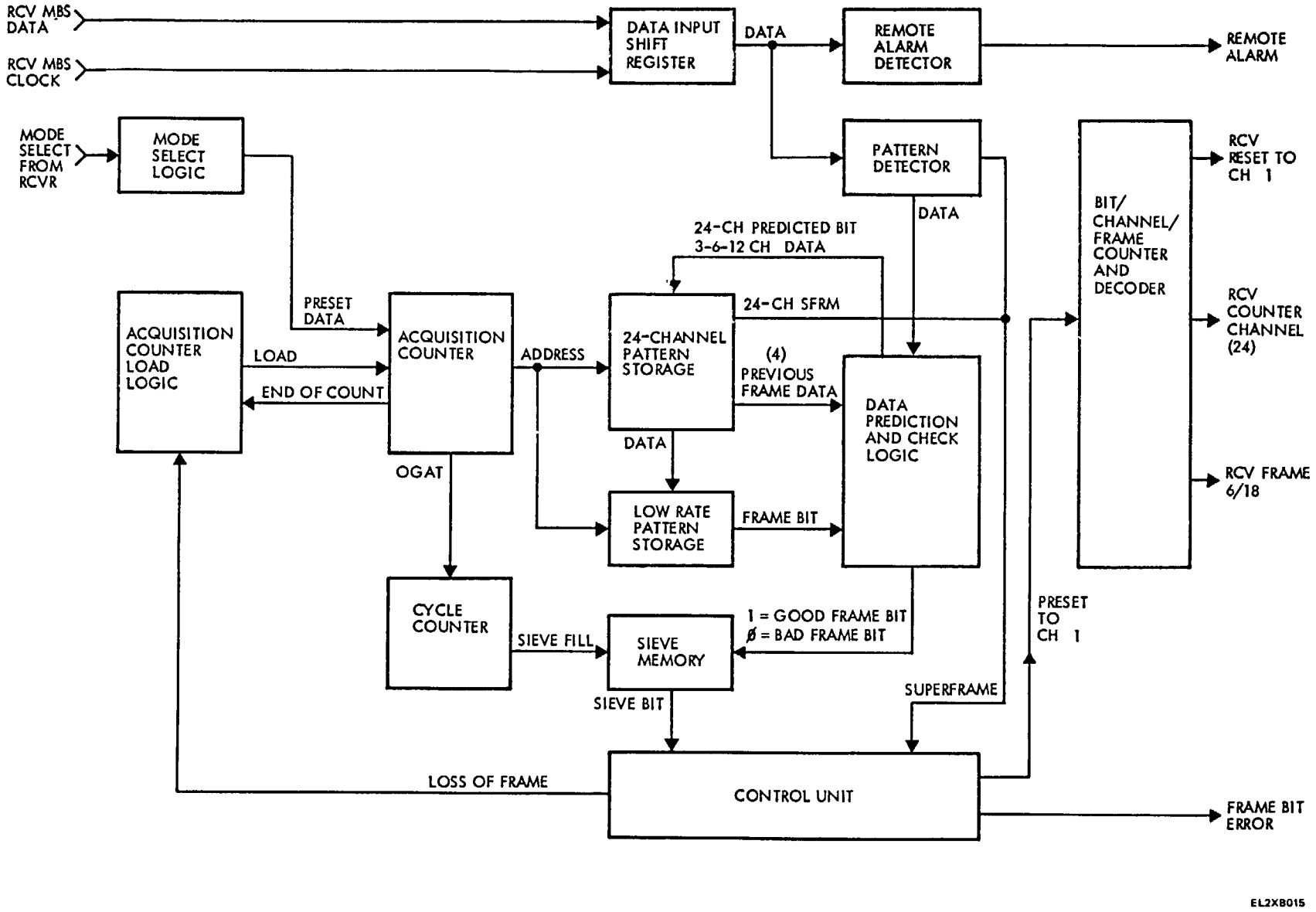


Figure 2-15. DEMUX unit block diagram.

the sieve memory will be set to 0. As the data is compared the incoming data bit is compared, and stored for one-half clock time during the read cycle of the 24-channel pattern storage. If the predicted bit and the received bit compare favorably, the received bit is written into the first location of the 24-channel pattern storage register. The data from the first register is shifted to the second, the second register is shifted to the third register and data in the third register is lost. This updates the register so that the next frame bit may be predicted from the previous four. After all sixteen 4-bit locations have been examined, the sieve memory is clocked by the control unit and if a 1 is left, frame is said to have been achieved. At this time, the control unit advances to state 13, the prime flip-flop is set and the cycle counter is set to state 11. When in state 13, the control unit monitors the output of the data prediction and check logic each time the first one is encountered in the sieve memory. If the predicted bit and the frame bit candidate compare favorably, the control unit will remain in state 13 and the prime flip-flop will remain set. If the bits do not compare favorably, the control unit will advance to state 14 and the prime flip-flop will be reset. If the next frame bit candidate compares favorably, the control unit will remain in state 14 and the prime flip-flop will be set. If the bits do not compare, the control unit will advance to state 15 and the prime flip-flop will be reset. This cycle continues until there have been either two good bits in a row which will return the control unit to state 13 or there have been three errors in a row which will cause the DEMUX unit to loose frame and begin a new frame search sequence. Refer to figure 2-16 for the control unit state diagram. When frame is achieved, the control unit generates the preset to one (PR1) signal which presets the channel counter to channel 1.

(2) *Low rate acquisition.* In the 3-, 6- or 12 channel modes, the acquisition counter divides by 288 for 3-channel operation, 576 for 6-channel operation and 1152 for 12-channel operation. A window, OGAT, is generated during the last 256 states of the acquisition counter. During this time the output of the 100,011 pattern detector is written into the pattern storage register. A 1 is written for a 100 and a 0 is written for 011. If a 100 or 011 pattern is detected, the sieve memory bit which corresponds to the location in the pattern storage register is left in the 1 state. If the data does not match, a 0 is written into the sieve RAM. At the end of four cycles, if a 1 is left in the sieve, frame is assumed and the DEMUX enters the monitor mode.

(3) *Channel counter.* The bit/channel/ frame counter produces either 3, 6, 12 or 24 discrete channel counter pulses at the RCV CH CTR outputs. The number of channels produced is determined by multiplexer set strapping. The RCV RESET TO CH 1 signal is generated and supplied to the PCD unit. RCV frame 6/18 is generated to provide synchronization of VF signaling.

f. PCD Unit. The PCD unit (fig. 2-17) converts PCM data to VF, extracts signaling, and distributes recovered VF data to the channel modules. PCM data from the DEMUX unit is supplied to a serial-to-parallel converter which converts the data to an 8-bit word as clocked by the MBS clock and enabled by the advanced channel counter. The output from the serial-to-parallel converter is then supplied to the signaling circuit and a D-to-A converter. The signaling circuit, as clocked by the MBS clock and enabled by the advanced channel counter, extracts the 8th bit of each channel during the signaling frame to supply signaling information to the VF modules. Parallel data received by the D-to-A converter is converted to a differential current signal with a magnitude and polarity determined by the relative value of the PCM word. The converted data is then supplied to a current driver which converts the current to a voltage proportional to the input current and applies it as PAM data to the channel decode. The channel decode is driven by the channel count decoder select and the channel count decoder output select. When the sample enable provides a strobe, as clocked by the MBS clock and enabled by the advanced channel counter, the channel count decoder select circuit selects one of three 8-channel decoders in the channel decode. The channel count decoder output select then selects one of the outputs of the selected decoder through which the PAM data is applied to the VF modules. A reset signal from the DEMUX unit synchronizes the channel output decoder select and channel count decoder output select to beginning of frame. The channel decoder select and decoder output select signals are both applied to a fault monitor. If the fault monitor detects a loss of either input, a fault alarm enable is generated to illuminate a fault indicator.

2-6. DTG Circuit Descriptions

The following subparagraphs provide the de-

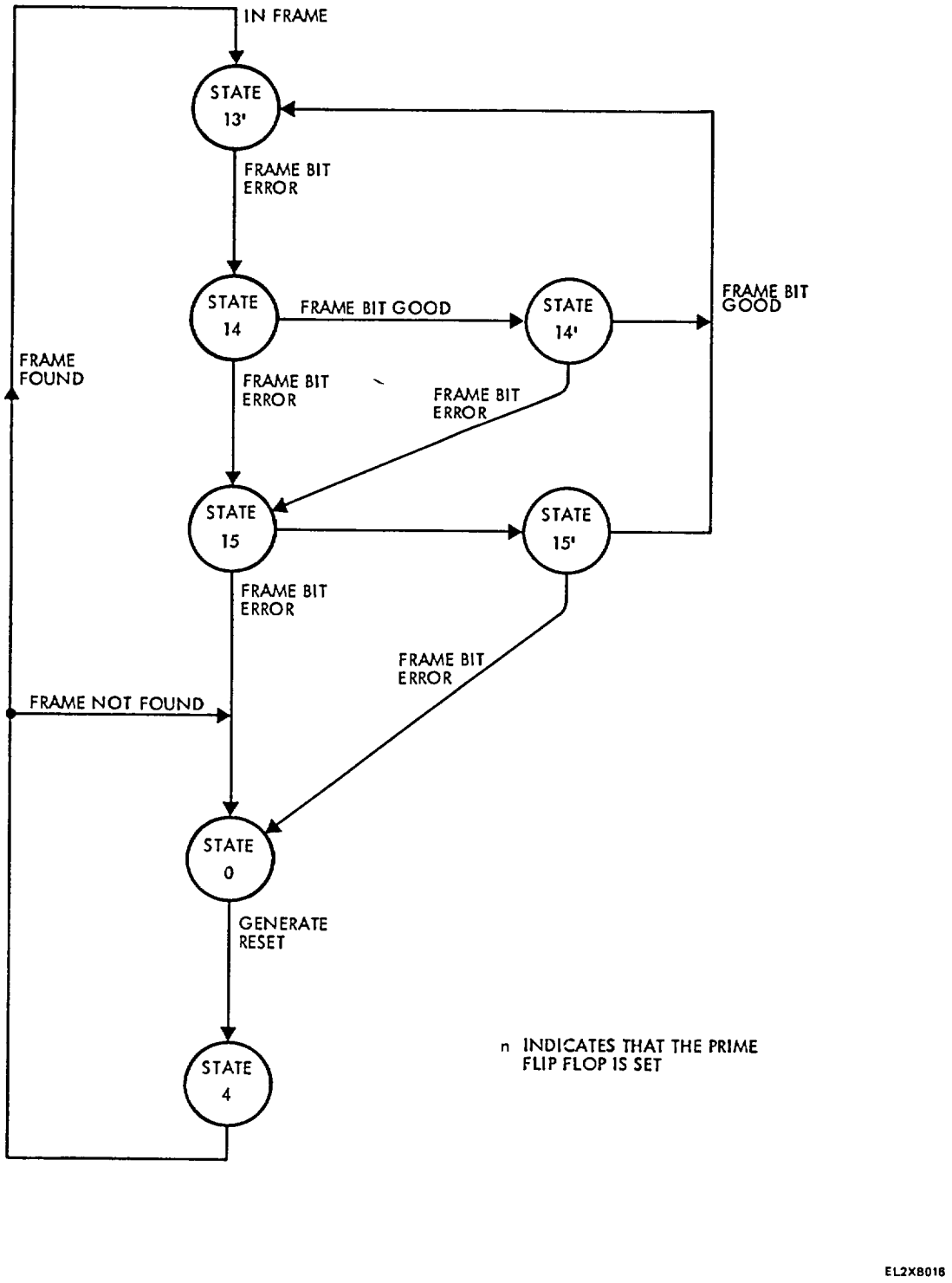


Figure 2-16. Control unit state diagram.

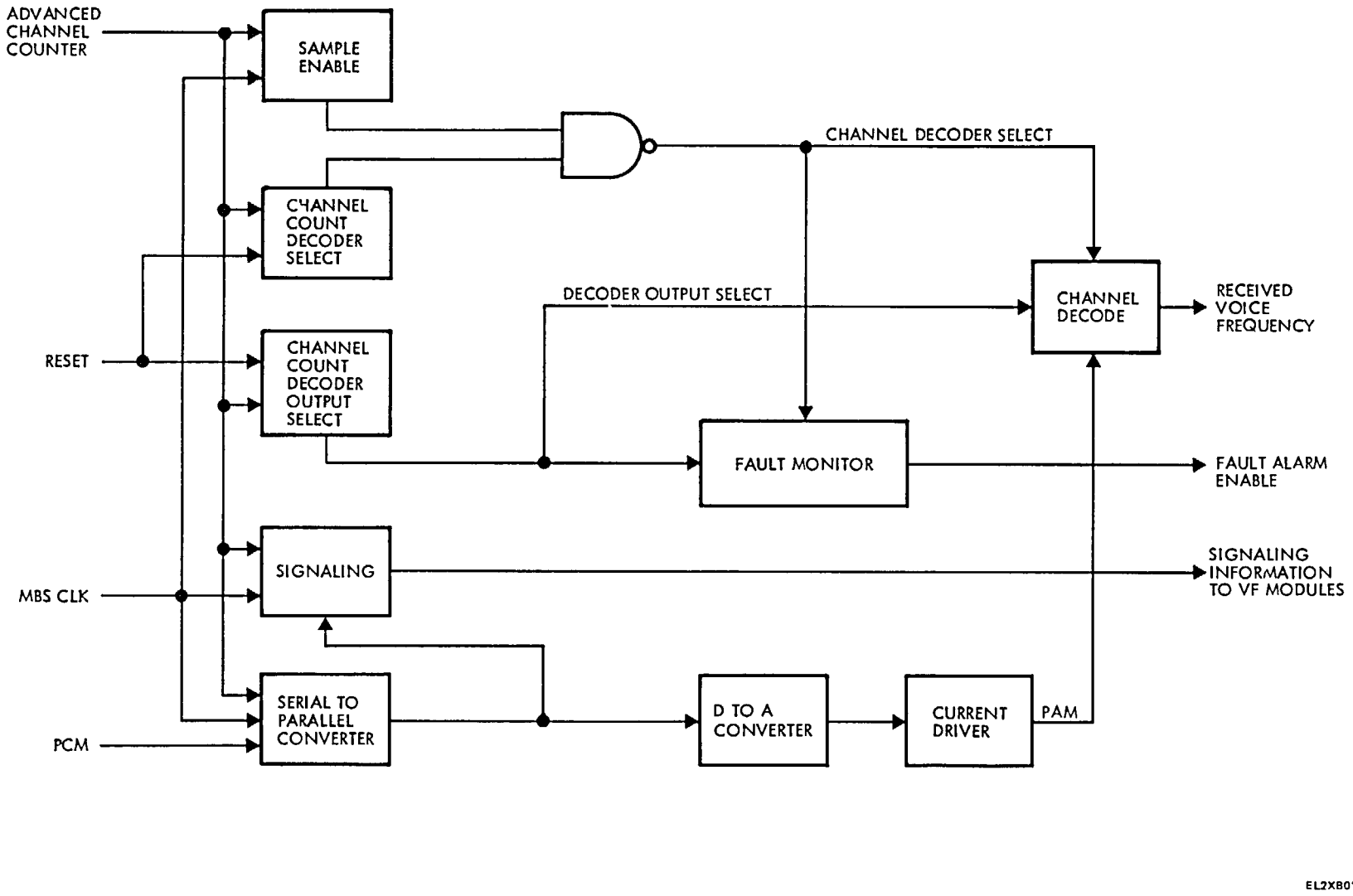


Figure 2-17. PCD unit block diagram.

tailed descriptions for the major circuits in each unit of the DTG.

a. PCM. Subparagraphs (1) through (10) below describe the individual circuits of the PCM unit.

(1) *Analog input multiplexer* (fig. FO-2, sheet 2). The analog input multiplexer consists of IC5, IC7, IC9, IC25, IC27, IC29, IC35, IC37, IC39, IC34, IC33, and IC3. The low pass filters IC5, IC7, IC9, IC25, IC27, and IC29 limit the bandwidth of the incoming signals. The outputs of each of the input filters are applied to a separate input of IC35, IC37 or IC39. Integrated circuits IC35, 37 and 39 are addressed by EC2°, $EC2^1$, and $EC2^2$ which are buffered and level-shifted by IC34A, B and F. Decoding of $EC2^3$ and $EC2^4$ is done by IC33A, IC3A, B and C, and IC33B and C to provide three chip select signals for IC35, IC37 and IC39. The filter outputs are sequentially sampled by IC35, IC37 and IC39 to provide a multiplexed analog signal containing the information from each of the VF channels at the correct time.

(2) *Sample and hold circuits* (fig. FO-2, sheet 2). Sample and hold circuits consist of odd and even groups. Both circuits are identical except for reference designators. This description applies to the odd group sample and hold circuit. The odd group sample and hold circuit consists of IC47D and IC67. The output of the analog input multiplexer is summed with the output of the zeroizer circuit by IC47D. The signal from IC47D is applied to the input of monolythic sample-and-hold amplifier IC67. Where a sample is taken, the S/H input of IC67 is made high by the conversion control logic. The signal at the input is applied to holding capacitor C135. When the S/H signal goes low, the voltage at C135 is held until the next sample pulse. The outputs of the sample and holds are provided for test purposes at the PAM ODD and PAM EVEN test points. If the output of IC65 does not exceed the level of the signal from the sample and hold, the output of IC66 will remain low and the bit will be reset to 0. The most significant bit is the sign bit which provides polarity information to the far-end terminal. If the signal is positive, the sign bit will be a 1 and if negative the sign bit will be a 0. At the next clock, the second bit is set and the capacitor again compares the voltage from the digital to analog converter (DAC) IC65 with the voltage from the sample and hold. If the voltage from the sample and hold was higher than the voltage from the DAC, the hit will be set to 1 unles the sign bit is a 1, in which case the bit will be set to 0. This is done to shift the curve of the DAC from a +8 bit p255 low device to a +128 bit p255 device. This bit setting procedure continues until all bits have been compared. At the end of the check cycle the conversion complete signal (CC) from successive approximation register IC64 (SAR) is sent to the conversion complete logic to acknowledge completion of the conversion. The CC signal is also used to set IC53B (IC53A), which disables the DAC. The eight outputs of the SAR are applied as an 8-bit word to the odd (even) P-to-S converter.

(3) *A-to-D converters* (fig. FO-2, sheet 2). A-to-D converters consist of odd and even circuits. Both circuits are identical except for reference designators. This description applies to the odd group A-to-D converter. The odd group A-to-D converter consists of IC66, IC51A, IC51D, IC64, IC65, IC53B, and IC77D. The output of the sample and hold is applied to the noninverting input of comparator IC66. The comparator output is applied to 2-line-to-l-line multiplexer IC77D used for test. The control input of the multiplexer is pulled to ground which connects the output of IC66 (IC56) to IC51D (IC51C). The output of IC51D (IC51C) connects to the D input of IC64 (IC54). The eight outputs from the register provide inputs to IC65 (IC55). When the S pin of IC65 (IC55) goes low the most significant bit of the register is set high. If the analog output at 10^E+ and 10^E-is greater than the input signal level, the output of IC66 (IC56) will go high and the most significant bit will remain set.

(4) *P-to-S converters* (fig. FO-2, sheet 2). P-to-S converter circuits consist of odd and even groups. Both circuits are identical except for reference designators. This description applies to the odd group P-to-S converter. The odd P-to-S converter consists of IC74. The eight parallel bits from the SAR are applied to inputs A through H of IC74. While the even group A-to-D converter is performing the conversion of the next channel, data is being shifted out of the odd P-to-S converter. The CLK INH signal at IC74 is held low by the even/odd output control while the odd group DAC is converting the PAM data to PCM data. After the conversion cycle is complete, a load pulse is produced by the even/odd output control. which loads the data into the shift register. At the next clock, the CLK INH input is made high and the data is shifted out by the next eight clocks.

(5) *Conversion control logic* (fig. FO-2, sheet 2). The major components of the conversion control logic include IC21C, IC42B, IC42A, IC23A,

IC22A, IC22B, IC2A, IC12, IC23B, IC21B, IC32B and IC22C. When the XMT ADV CHAN CTR goes high, one clock is passed through IC21C. Since the D input is tied to a pulldown and is always a 1, the Q output will go high. This makes the CLR and serial inputs A and B high. Each time a clock occurs, a 1 is loaded into IC12. When IC12 receives six clocks, the 1 shifted in by the first clock will appear at the Q_H output. A delay is provided by IC2A, IC22A and IC22B prior to the time IC12 is reset. When IC23A is reset, IC12 is cleared and the cycle repeats. When the 1 shifted into IC12 by the first clock of the cycle reaches the QB output, IC42A or IC42B will go low depending upon the condition of the EC2° signal. When the QH output of IC12 goes low IC23B and IC32B are clocked. The D inputs of both flip-flops are connected to EC2°. When EC2° is low, the Q output of IC23B is set to 0 and the Q output of IC32B is set to 1. The Q output of IC32B is used to enable the odd group A-to-D converter and the Q output of IC23B enables the even group A-to-D converter. At the end of the conversion cycle IC32B is reset by IC22C when a conversion complete signal is received from IC64. When the odd group conversion complete signal is received from IC54, IC23B is reset by IC21B.

(6) *Even/odd output control* (fig. FO-2, sheet 2). The even/odd output control consists of IC32A, IC31A, IC31B, IC41A, IC41B, IC71C, IC52F, IC22D, IC42C and IC42D. Each time the XMT ADV CHAN CTR occurs, IC32A is set. When the Q output goes high, one input of IC22D and IC71 goes high. This causes C136 to discharge through R122 and IC71C. When the capacitor has discharged, IC52F goes high causing the output of IC22D to go low. This resets IC32A. The result of this is a pulse at the Q output of IC32A. The Q output is gated with EC2° to produce a pulse when EC2° is high. This pulse is used to load the odd P-to-S converter. The Q output of IC32A clocks IC31A. The D input of IC31A is tied to the EC2° signal from the MUX unit. The EC2° signal contains the odd/even information. The Q output of IC31A is reclocked with SD7 or SD8 by IC31B and applied to the D input of IC41B which reclocks the output of IC31B and provides enable signals for the output multiplexer. The Q and Q outputs of IC41B are also used to enable the clock inhibit of the odd and even P-to-S converters while the Q output is gated with the Q output from IC41A to load the even P-to-S converter.

(7) *Output multiplexer* (fig. FO-2, sheet 2). The output multiplexer consists of IC43A, IC43B, IC43C and IC52C. Data from the odd P-to-S converter is applied to IC43A and data from the even P-to-S converter is applied to IC43C. The odd and even outputs from the even/odd output control are applied to a second input of IC43A and IC43C. The third input of IC43A and IC43C is used to disable the data output during signaling. The outputs of IC43A and IC43C and the signaling bit from the signaling control circuit are combined by IC43B which drives the XMT PCM BUS. The data is buffered at the output of IC43B by IC52C, which drives the MUX DATA test point.

(8) *Signaling control* (fig. FO-2, sheet 2). The signaling control circuit consists of IC1A, IC1B, IC11, IC21A, IC21D and Q1. The level of the XMT SIG A BUS is shifted by Q1 to a TTL level. Signaling information is reclocked by IC1B with SD8 and applied via the Q output to the D3 input of IC11. To provide the D1 input of IC11 and to disable IC1B, XMT FRAME 6+12 is clocked with XMT RESET TO CH 1 by IC1A. Next, IC11 is clocked by XMT ADV CH CTR to provide a two channel delay for correction of the conversion delay. The Q2 output of IC11 is one of two signals applied to gate IC21A. When IC21A receives SD7+SD8, a low is supplied to the output multiplexer to disable IC43A and IC43C. This permits signaling data from the Q4 output of IC11 via IC21D to be substituted for the least significant bit of the PCM data.

(9) *Zeroizers* (fig. FO-2, sheet 2). Zeroizer circuits consist of odd and even groups, identical except for reference designators. Only the odd group zeroizer is discussed. The odd group zeroizer consists of IC45, IC47A, IC78, IC79, IC69, IC70, and IC68. The conversion complete signal from the odd group A-to-D converter is applied to the D input of IC45A. Clock for IC45A is supplied at the D8 time by the conversion control logic. When the odd group A-to-D converter completes a conversion cycle the Q output of IC45A clocks IC45B, IC69, IC70, IC78, and IC79; and ODD S/B is applied to the up/down control of IC69, IC70, IC79, and IC80. A ±128 bit counter comprised of IC45B, IC78, and IC79, is used to detect the difference between the number of positive (0) and negative (1) polarity bits. If the number of polarity bits in either direction exceeds 128 the counter will overflow, causing the count of IC69 and IC70 to increase or decrease depending upon the polarity of the sign bit which caused IC78 and IC79 to overflow. When IC78 and IC79 overflow, IC45B produces a load pulse which resets the counter to 128. An 8-bit up/down counter is comprised of IC69 and 1C70. Integrated circuit

IC68 is an 8-bit digital-to-analog converter which, with IC47A, produces a voltage proportional to the binary weights of the outputs of IC69 and IC70. The output of IC47A is summed with the PAM signal at the sample and hold input.

(10) *Fault monitor* (fig. FO-2, sheet 2). The fault monitor consists of one-shot multivibrators IC61 and IC63, which are triggered by the outputs of the odd (even) group zeroizers and the output multiplexer. The time constants of the one-shots are longer than the time between trigger pulses, causing them to remain triggered. If any of the signals being monitored are missing, the associated one-shot will time-out and the output will go low. The outputs of the one-shots are ORed together by IC62. If any one-shot times out, the FAULT lamp on the PCM unit will light and the FAULT ALM BUS will go low. When the FAULT TEST pushbutton is pressed, all of the one-shots are reset. This will light the FAULT lamp, the ALL FAULT TEST lamp and will pull the FAULT ALM BUS low.

b. MUX. Subparagraphs (1) through (12) below describe the individual circuits of the MUX units.

(1) *Channel counter control and reset* (fig. FO-3, sheet 2). The major functional components of the channel counter control and reset include IC12A, IC12B, IC15, IC16D, IC25A, and IC25B. IC15 is an eight input multiplexer which monitors the outputs of the channel counter decode circuit. Select inputs A, B and C are connected to XMT 4/8/24 CHAN MODE, XMT 6/8 CHAN MODE and XMT 12/24 CHAN MODE, respectively. When the channel counter reaches the count selected by IC15, the output will go high. The method by which the reset is generated for 24-channel operation differs from the 3-, 6-and 12-channel modes due to the frame bit being inserted between channels 24 and 1. The reset must be held back for one bit time to allow for the frame bit. For 24-channel operation, XMT 24 CH MODE disables IC25B, which prevents D8 from the bit counter decode from initiating a reset. The output of IC25B will always be high. IC25A will allow the signal from IC15 to pass through the gate and be inserted. The output of IC25A is reclocked by IC16D. At the rising edge of the pulse at pin 3 of IC12A, the Q output will go high, which generates XMT RESET TO CHANNEL 1. Integrated circuit IC12B is clocked from BMBS CLK. At the rising edge of the clock, the Q output will go low, causing IC12B to reset. Since IC12B is reset, the D input to IC12A is low. At the rise of the next clock, the Q output of IC12A will be set to one which removes the reset signal from IC12B. This causes the XMT RESET TO CH 1 signal to be delayed by one clock period so that the frame bit may be sent. Figure 2-18 is a timing diagram for 3-, 6-, and 12-channel operation. Figure 2-19 is for the 24-channel mode.

(2) *Bit/channel counter* (fig. FO-3, sheet 2). The bit/channel counter consists of 4-bit binary counters IC27 and IC17. The three low-order bits of IC27 are used as the bit counter. The remaining bit of IC27 and the four bits of IC17 are used as the channel counter. The channel counter control and reset circuit resets the bit/channel counter to the all-zero state (zeros loaded into the parallel inputs) by applying a reset pulse (CCLK) to the parallel load input (pin 9 of IC27 and IC17). The binary coded outputs from the last five stages of the bit/channel counter are buffered by IC10A through F and made available to the PCM module for channel selection.

(3) *Bit counter decode* (fig. FO-3, sheet 2). The bit counter decode circuit consists of IC16, IC26, IC28D, IC46B, IC55C, IC56 and IC57. The three low order bits from IC27 of the bit/channel counter are decoded by IC26. The bit 2, bit 7 and bit 8 outputs of IC26 are then reclocked with BMBS CLK-1 by IC16 and applied to data selector IC57. If the multiplexer set is operating in the 24-channel mode, the select input (pin 1) of IC57 is low. This causes the signals at the A inputs of each multiplexer to appear at the outputs. For 24-channel operation SD6 is selected for SD6+SD7 and SD1 is selected for SD1+SD2. SD6+SD7 is reclocked by IC28D which delays the output by one clock period to produce SD7+SD8. If PC1 and PC2 are low and the system is configured for 24-channel operation (24 CH MODE received by IC55C), the output of IC55C will be high. This causes data selector IC57 to select the B data inputs to the selector for the period of PC1 or PC2.

(4) *Channel counter decode* (fig. FO-3, sheet 2). The channel counter decode circuit consists of IC6, IC7, IC8, IC9, IC18, and IC19. IC18 and IC19 decode the five high order bits of the bit/ channel counter and provide 24 negative-going outputs, which are latched by IC6, IC7, IC8 and IC9 to produce XMT CHAN CTR 1 through XMT CHAN CTR 24. The most significant bit of the bit/channel counter output enables IC18 and is inverted by IC10F to enable IC19. The twenty-fifth output of channel decoder IC19 (pin 9) is used in the 24-channel mode to provide a space for the frame bit. At the end of channel 24, the

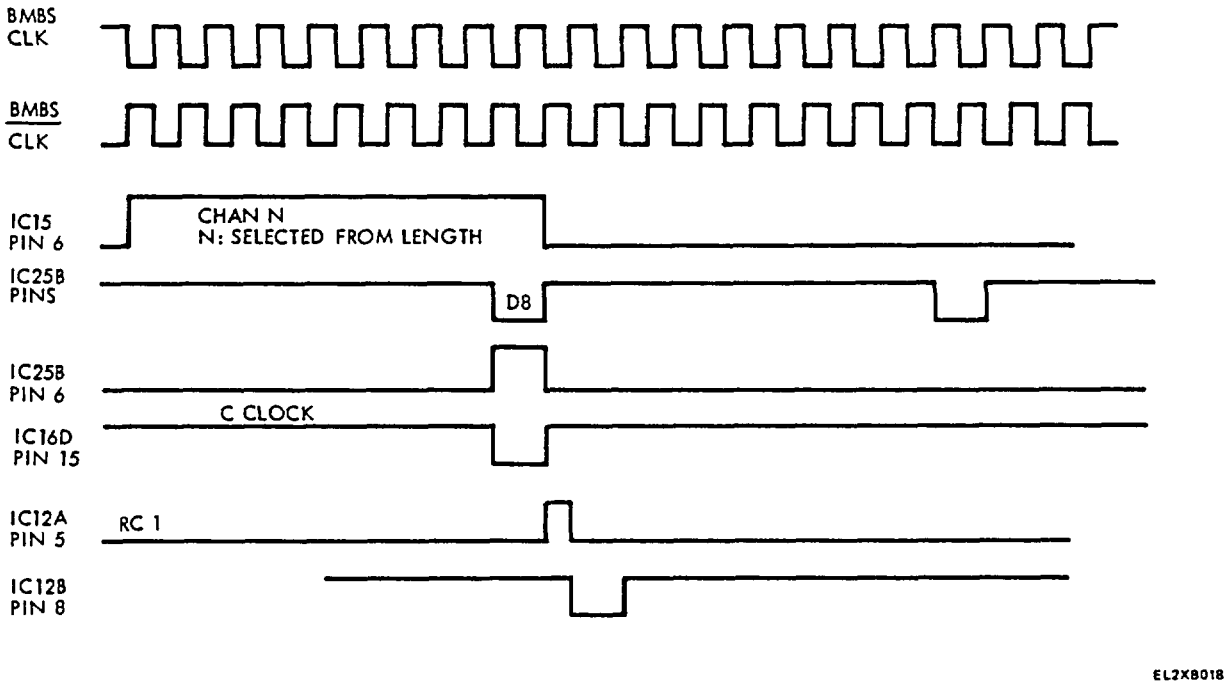


Figure 2-18. 3-, 6-, and 12-channel operation timing diagram.

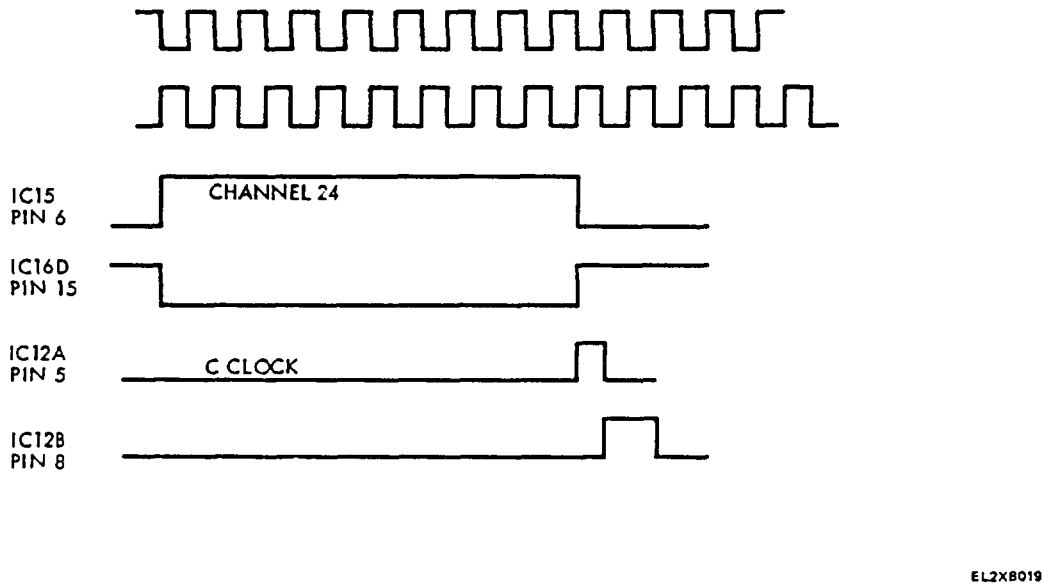


Figure 2-19. 24-channel operation timing diagram.

channel counter decode is allowed to advance one channel higher than channel 24 until the bit, channel counter has advanced through the bit one count before the bit channel counter is reset. This provides a 1-bit space for insertion of the frame bit.

(5) *Data/voice enable* (fig. FO-3, sheet 3). The data/voice enable consists of IC4E, IC46D, IC49, and IC50. The XMIT CONT BUS signal determines whether the data from the channel module is voice or data. If the channel being sampled contains a data module XMIT CONT BUS will be high. If the channel is a voice frequency channel, the XMT CONT BUS will be low. When XM3T CONT BUS is received it is inverted by IC4E and applied to the D inputs of IC50 and to one input of IC46D. The data at the D input of IC50 is clocked by D2 and held in IC50 until D8 time when it is shifted into the first stage of three-stage shift register IC49. At SD7+SD8, the data stored in IC50A is loaded into the first stage of the shift register. Each time SD7+SD8 occurs, the data in IC50A is loaded into the register and data already in the' register is shifted to the next stage. The 1Q output of IC49 is connected to IC46D. Timing diagram figure 2-20 shows the timing relationships of the clocks and XMIT CONT BUS to the output of IC49, IC50A and IC50B. IC50B reclocks the XMT CONT BUS with D2. This delays the data on the control bus by one bit time. The outputs of IC49 contain a history of the previous three channels, which are used by the zero suppressor.

(6) *Zero suppressor* (fig. FO-3, sheet 3). The XMT PCM BUS is buffered and inverted by IC4A, reinverted by IC5A and applied to one input of NAND gate IC45A. The other input of IC45A is driven by SD8. SD8 is high except during the D8 time. This enables IC45A to pass the first 7 bits of the PCM word. The output of IC45B passes the output of the 16 bit data delay if DLY 2 is a 1 (indicates that the previous channel was a voice channel). The output of IC45C is used to enable flip-flop IC35B, which is clocked by BMBS CLK when Q is high due to the action of IC55A. If the D input goes low during B0 through B7, the flip-flop will be set and the clock disabled by IC55B. If the channel being sampled is data and the previous channel was voice, IC36C will pass and invert the data. Monitoring of PCM DATA bits one through seven is (tone by IC35A. If any of the bits are low, the Q output of IC35A will go high and disable the clock to the flip-flop for the remainder of the channel time. If no zeros are detected, a 1 will be present at the output of IC35B at the end of the first seven bits. IC36C monitors XMT CONT BUS delayed by one channel time, XMIT CONT BUS delayed three channel times, and XMT DATA from the data channel modules. If the data channel remains high for the first seven bits and the previous 2 channels were data channels, then output of IC36 will remain low. If any bit is low the Q output of IC36-will go low and disable the lock until the next SD8. At the end of channel time if the Q output of IC35A or IC35B is low, the output IC46A will be high. IC24B enables IC36B by ANDing ZERO SUPPRESS and SD6+SD7. If the zero suppress line is low and the output of IC46A is high, a 0 will be inserted in B7 of the VF channel module. For 17450-020 versions (fig. FO-3A, sheet 3) zero suppression, the XMT PCM BUS is buffered and inverted by IC4A, reinverted by IC5A and applied to the D input of flip-flop IC35B, which is clocked by BMBS CLK when Q is high due to the action of IC55D. If the D input goes high during BO through B7, the flip-flop will be set and the clock disabled by IC55D. If any bit is high the Q output of IC35B will go low and disable the clock until the next SD8. At the end of channel time if the Q output of IC35B is low, the output IC464 will be high. IC24B enables IC36B by ANDing ZERO SUPPRESS and SD6+SD7. If the zero suppress line is low and the output of IC46A is high, a 1 will be inserted in B7 of the VF channel module

(7) 1*kHz digital tone generator* (fig. FO-3, sheet 3). The 1 kHz digital tone generator consists of IC13A, IC13B, IC22A, IC23, IC34A, and IC34B. Integrated circuits IC13A and IC13B comprise a ÷3 counter which is clocked once each frame by R1. The Q and Q outputs of IC13B are used as inputs to IC23, and 8-bit parallel-in serial-out shift register. Integrated circuit IC22A is a ÷2 counter which is clocked from IC13A. This flip-flop generates the sign bit, which is loaded into IC23 at the same time the data bits are loaded. The count sequence of IC13A. IC13B and IC22A is such that IC23 is loaded with a +97, +116, -97, -116 sequence to produce a 1 kHz tone at the output of each VF channel in the far-end set. As controlled by BMBS CLK and CH2, IC34A and IC34B strobe the parallel inputs into the shift register.

(8) *Voice/zero-suppress/1 KHZ MUX* (fig. FO-3, sheet 3). The voice/zero-suppress/1 KHZ MUX consists of IC24C, IC31A and IC46C. With the 1 KHZ TONE switch in the OFF position, IC31A passes PCM data or data from the 16 bit delay. With the 1 KHZ TONE switch in the ON position, IC46C passes the output of the 1 KHZ digital tone generator. The outputs of IC31A and IC46C are combined by IC24C.

(9) *Data/voice/frame MUX* (fig. FO-3, sheet 3. The data/voice/frame MUX consists of IC32, IC25C, IC14A, IC3B, IC3C, and IC3D. The dual 4-input multiplexer IC32 is controlled by the data, voice enable and frame pattern generator. The data/voice enable output applies a control signal to the A input of IC32. When the A input is low, the output of the voice/zero suppress 1 KHZ MUX is selected. When the A input is high, the output of the 16 bit data delay is selected. When a frame bit is to be sent, the B input of IC32 is brought high and the frame bit is selected regardless of the state of the A input. The 1Y out

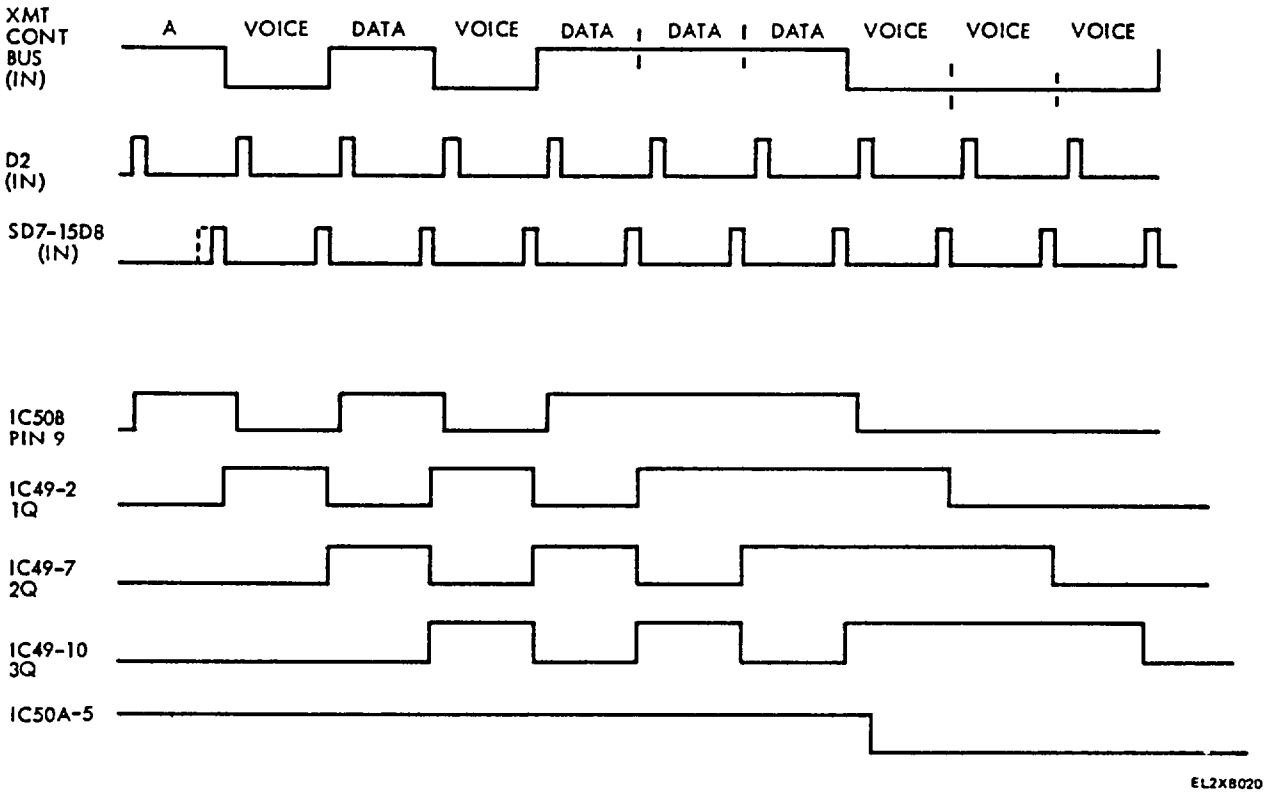


Figure 2-20. Data/voice enable timing diagram.

put of IC32 is then supplied to the driver unit as XMT MBS DATA via gate IC25C. If an on-going alarm is received from the OGA control circuit, IC25C is disabled and XMT MBS DATA is not supplied to the driver unit. The output of IC25C is buffered by IC3B and IC3C before it is applied to the test point and the output connector. The second section of IC32 maintains a logic zero at the FRAMING BIT PATTERN test point except when a valid frame bit is present. The output of section 2 of IC32 is buffered by IC14A and IC3D before being applied to the test point.

(10) *OGA control circuit* (fig. FO-3, sheet 3). If an OGA is present, the output of IC45D goes low for the D2 time. This causes the output of IC25C in the data/voice/frame MUX to go high regardless of the condition of the data/ voice/frame MUX. If the multiplexer set is strapped for digital alarm (B2=0+11110000) IC55B is enabled by XMT FULL ALARM SEL. When the OGA line is high, the first 8 bits of the 16 bit data delay circuit are loaded with the 11110000 pattern at the beginning of each channel.

(11) *Frame pattern generator* (fig. FO-3, sheet 3). The frame pattern generator comprises three main sections: 24-channel frame pattern encoder, 3/6/12-channel frame pattern encoder, and multiplexer select logic. These circuits are described below.

(a) 24-channel frame pattern encoder. The 24-channel frame pattern encoder consists of IC28C, IC39, IC38C, IC48D, IC48C, IC48B, IC58A, IC58B, IC40A, and IC40B. Flip-flop IC28C is clocked by BMBS CLK-1, and quad flip-flop IC39 is clocked by RC1 (reset to channel 1). The timing diagram for the 24-channel frame pattern encoder is shown in figure 2-21. The clear circuit (IC38C, IC48D, and IC28C) prevents illegal states of flip-flop IC39. The logic gates IC48C, IC58B, IC58A and IC48B) generate a signal that is typically low for 1.4 milliseconds and high for 0.1 millisecond at IC48B. The first three flip-flops within quad flip-flop IC39 (1Q, 2Q and 3Q) form a modified ring counter which circulates ones and zeros as shown in the diagram. The FR-12 output of IC48B is coupled to the 3-, 6-, and 12-channel frame pattern encoder. The logic signal from IC40B controls the multiplexer select logic.

(b) 3-, 6-, and 12-channel frame pattern encoder. The 3-, 6-, and 12-channel frame pattern encoder consists of IC28B, IC22B, IC28A, and IC47, IC25D, IC38A, IC48A, and IC58F. The timing diagram of this circuit is shown in (figure 2-22). Signal D2 indicates the presence of the bit of the word. Signal PC3 indicates the presence of the third channel of a frame. Upon receipt of the frame 12 signal (FR12) and third channel signal (PC3), IC38A goes low assuming 3-, 6-, 12-channel operation). This signal is then clocked through flip-flop IC47 and fed back to clear IC47 via IC48A and IC28A. The output of this circuit is sent directly to the multiplexer select logic through IC40C. The illustration shows how a logical 110 frame bit pattern is generated in the XMT MBS DATA. At the leading edge of the next frame 12 gate, flip-flop IC22B toggles to the 0 state and causes IC40C to produce a logical 001 frame bit pattern.

(c) Multiplexer select logic. The multiplexer select logic comprises gates IC37A, IC37B, IC37C, IC37D, and IC38B. If 3-, 6- or 12-channel mode is selected, the 24 CH MODE signal enables NAND gates IC37D and IC38B. Logic lines from the 24-channel frame pattern encoder via IC37D-13, and 3-, 6-, 12-channel frame pattern encoder via IC37A determine the logic level of frame bits to be supplied to the data/voice/frame multiplexer (IC32). The logic level of the frame bit selection (B input IC32) is determined by IC38B, IC37C and IC37B.

(12) *Activity monitor* (fig. FO-3, sheet 3). The activity monitor consists of IC41A, IC41B, IC51A, IC51B, IC53, IC54B and IC54C. Integrated circuits IC41A, IC41B, IC51A, and IC51B are retriggerable monostable multivibrators. The period of the data and clock signals is much shorter than the time-constant of the monostable, so that the Q outputs of each monostable will be high as long as the input signals are present. The Q outputs of IC41A, IC41B, IC51A, and IC51B are NORed by IC53A. The output of IC53A is inverted by IC54B and the FLTALMBUS is pulled low when an alarm is present. The reset lines of IC41A, IC41B, IC51A, and IC51B are connected to FAULT TEST switch S1. When S1 is pressed, the resets are brought low causing the Q outputs of IC41 and IC51 to go high. The ALL FAULT TEST lamp is illuminated by IC53B when all Q outputs are high.

c. DRIVER. Subparagraphs (1) through (15) below describe the individual circuits of the DRIVER unit. The first three pages of schematic FO-4 (1, 2, and 3) show the earliest configuration (DVR02)The next three pages (4, 5, and 6) show latest configuration (DVR04). Although the two circuits are almost identical, the reference designations have been changed. The reference

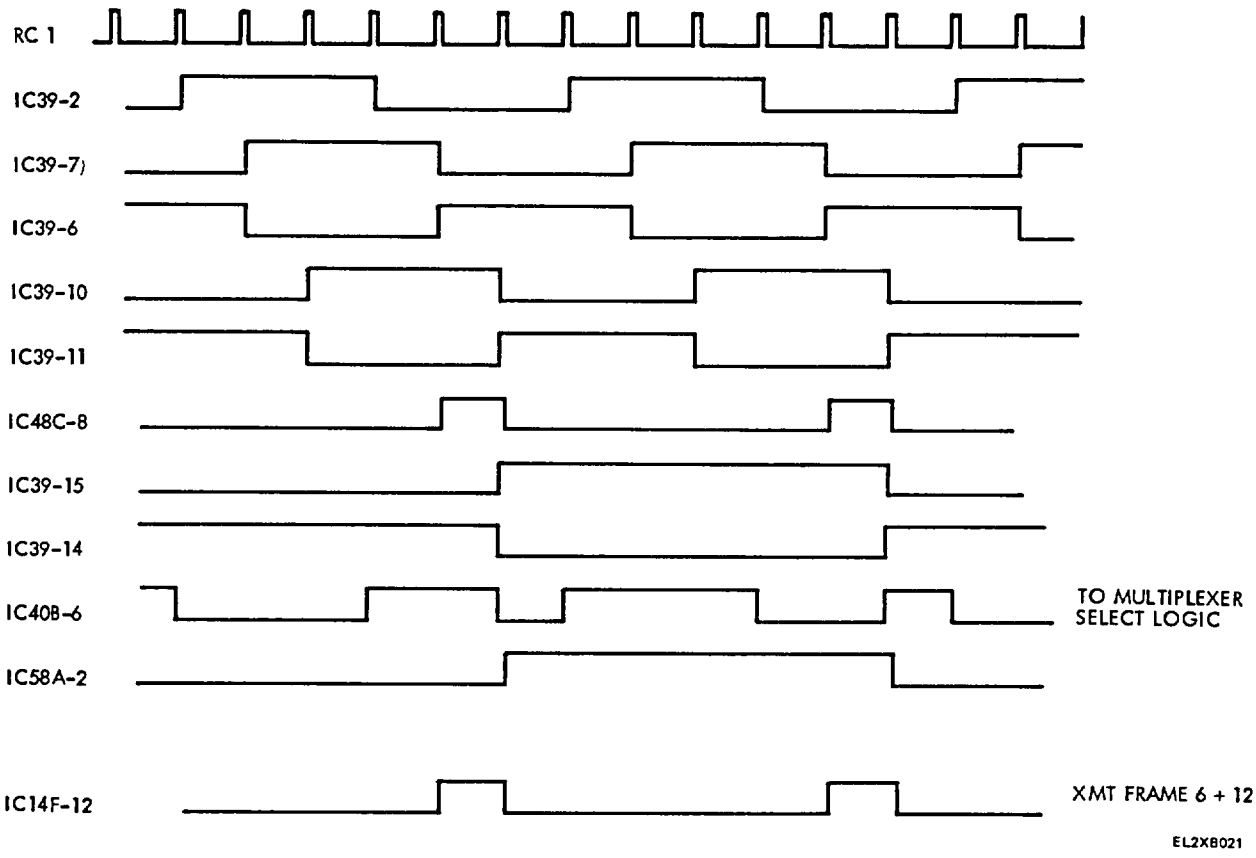


Figure 2-21. Timing diagram of 24-channel frame pattern encoder.

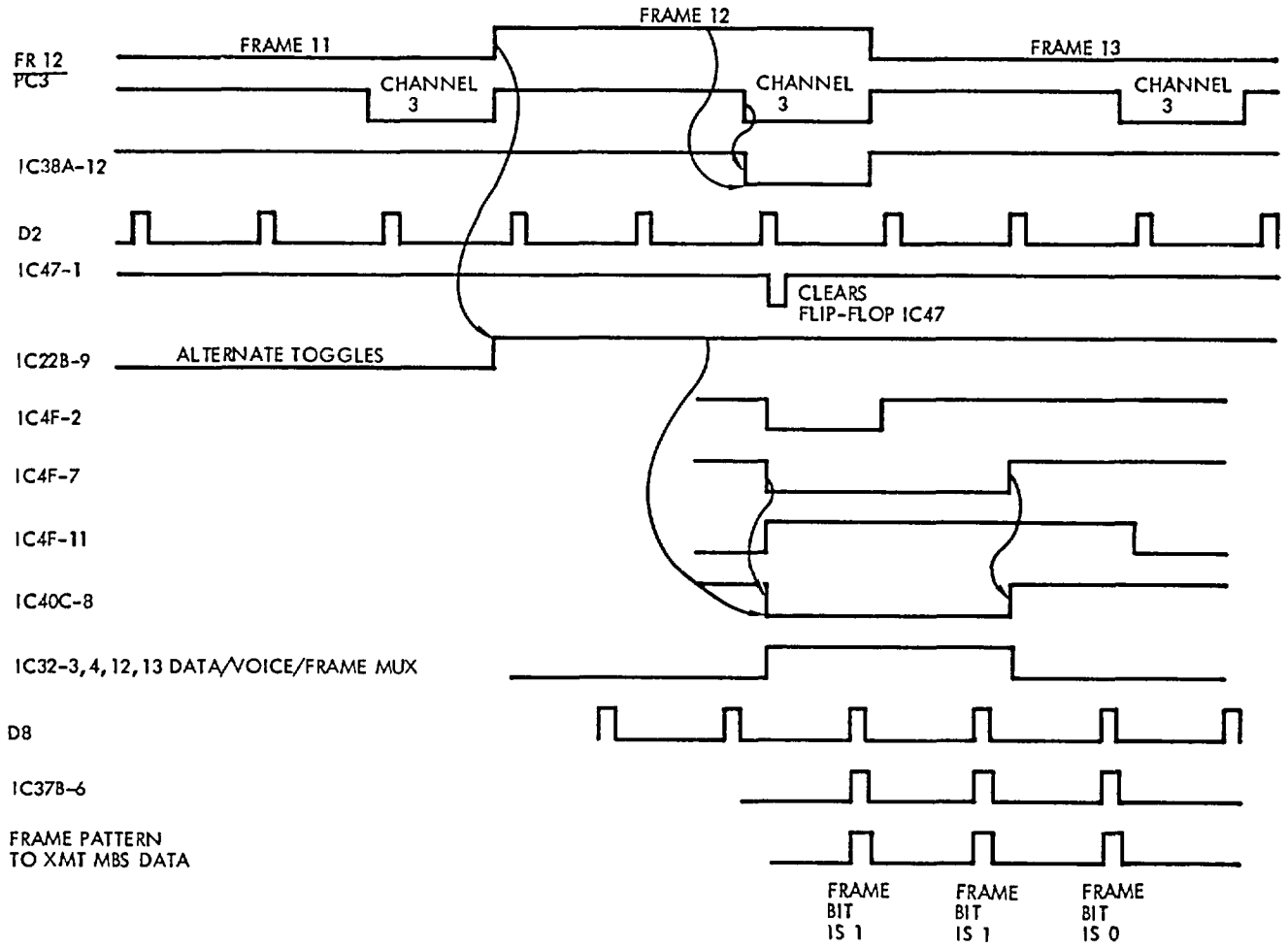


Figure 2-22. Typical waveforms for 3-, 6-, 12-channel frame pattern encoder (shown in 3-channel mode).

designators contained in parenthesis apply to DVR04 and the reference designators not contained in parenthesis apply to DVR02. Table 3-1 in chapter 3 specifies what serial numbers were built to each configuration.

(1) *78-ohm balanced external timing source receiver* (fig. FO-4, sheet 2 or 5). The 78-ohm balanced external timing source receiver consists of IC5B (IC12B) and differential line receiver. The inputs of the line receiver are clamped to 3.3 volts to prevent damage to the receiver by transients on the inputs.

(2) *Level translator* (fig. FO-4, sheet 2 or 5). The level translator consists of differential comparator IC15A (IC62A) which converts the 0 to +5 volt output of the 78-ohm balanced external timing source receiver to a -5V to 0 logic level required by the -5 volt referenced logic on the remainder of the DRIVER unit.

(3) *External clock activity monitor* (fig. FO-4, sheet 2 or 5). The external clock activity monitor consists of IC23B (IC24B) and IC33C (IC53C). Integrated circuit IC23B (IC24B) is a retriggerable monostable multivibrator triggered by the output of the level translator. The time constant of C31 (C26) and R59 (R31) is much greater than the period of the EXT TIMING SOURCE. As long as an external timing source is present, IC23B (IC24B) will remain in the triggered state. If there is no external timing source present, IC23B (IC24B) will time out causing the Q output to go low. The front panel EXT TIMING SOURCE lamp is driven by IC33C (IC53C).

(4) *Clock source select circuit* (fig. FO-4, sheet 2 or 5). The clock source select circuit consists of IC44C (IC5D), IC12 (IC22), and IC22C (IC32E). When no external timing source is present, IC12A (IC22A) connects the internal oscillator to the clock divide chains. When an external timing source is present, the output of the 24.704 MHz VCO is connected to the clock divide chains. IC22C (IC32E) and IC44C (IC5D) are used to supply an external clock to the DRIVER unit for test purposes.

(5) *Phase detector* (fig. FO-4, sheet 2 or 5). The phase detector consists of IC4 (IC51), IC14 (IC52), IC21 (IC61), Q1 (Q11), Q2 (Q12) and Q3 (Q13). Integrated circuits IC14 (IC52) and IC21 (IC61 are ÷8 counters, which divide the XMT MBS CLOCK and the external timing source from the level translator by eight and apply them to phase comparator IC4 (IC51) which compares .he edges of the signals from IC14 (IC52) and IC21 (IC61). If the phase of the external timing source leads the phase of the XMT MBS CLK, the phase comparator produces an output at the U1 output of IC4 (IC51). This causes Q3 (Q13) to turn off and Q1 (Q11) to turn on. When Q3 (Q13) is conducting, a ground is placed on the input of the loop filter. When the phase relationship of the phase comparator inputs is reversed, the D1 output of IC4 (IC51) produces an output which turns Q1 (Q11) on. This provides a negative voltage at the input of the loop filter.

(6) *Loop filter* (fig. FO-4, sheet 2 or 5). The loop filter consists of IC3 (IC31) and its associated components which comprise an active low pass filter. This filter averages the phase pulses to provide an error voltage proportional to the difference in the number of negative and ground pulses from the phase comparator. On late-model DRIVER units updated to provide bipolar loopback capability (fig. FO-4A) the loop filter circuitry is configured to provide a second-order low-pass response with a corner frequency near 350 Hz.

(7) *24.704 MHz VCO* (fig. FO-4, sheet 2 or 5). The 24.704 MHz VCO consists of IC31B (IC21B) and its associated components. The VCO output frequency from voltage-controlled multivibrator IC31 (IC21), is controlled by the error voltage from the loop filter. Late-model DRIVER units updated to provide bipolar loopback capability (fig. FO-4A) rely on the use of a voltage controlled crystal oscillator (VCXO). The VCXO has enough allowable deviation to provide the required ± 200 Hz frequency range from the nominal 1.544 MHz. The use of a crystal in the voltage controlled oscillator helps to stabilize the output frequency in response to high frequency noise voltages and also provides assistance in attenuation of phase noise frequencies above 350 Hz.

(8) *Clock divide chains* (fig. FO-4, sheet 2 or 5). The clock divide chains consist of IC53 (IC34), IC36D (IC65F), IC54A (IC44B), IC55 (IC35), IC6D (IC55C), IC54B (IC44A), IC46A (IC45A) IC43 (IC14), IC52 (IC33), IC56 (IC36), IC42 (IC46), IC31B (IC25B), and IC41 (IC26). A counter formed of IC53 (IC34), IC36D (IC65F), IC54A (IC44B), IC55 (IC35), IC6D (IC55G), IC54B (IC44A) and IC46A (IC45A) divides by the ratio of 192/193 ÷ 8 to produce a 3.072 MHz clock. Integrated circuit IC53 (IC34) is a ÷16 counter. Integrated circuit IC55 (IC35) is a ÷16 counter which is loaded with 00102 to create a ÷12 counter each time IC53(IC34) generates a carry output. After 192 counts, a carry will occur from both IC53 (IC34) and IC55 (IC35). When this occurs IC53 (IC34) is loaded with 1111^2 and IC55 (IC35) is loaded with 0010^2 and the cycle is repeated. A four bit binary counter is formed by IC43 (IC14), which divides the 3.072 MHz clock by 2^4, 2^8, and 2^{16} to produce

768 kHz, 384 kHz and 192 kHz clocks respectively. In conjunction with IC53 (IC34) and IC55 (IC35), IC56 (IC36) divides the 24.704 MHz clock by a ratio of 192/193 ÷3 to produce 8.192 MHz. Each time the 192/193 ÷8 counter generates a load pulse and IC56 (IC36) is in its maximum count state, a pulse is produced at the output of IC42 (IC46), which loads a 1101^2 into the counter. The QA output of IC56 (IC36) is divided by two by IC31B (IC25B) and buffered by IC32C (IC13C) to produce XMT 4.096 MHz CLK BUS. The 4.096 MHz is divided by 2^8 and 2^{16} by IC41 (IC26) to produce 512 kHz and 256 kHz clocks. The 24.704 MHz clock is divided by 16 by IC52 (IC33) to produce a 1.544 MHz clock.

(9) *Mode select* (fig. FO-4, sheet 2 or 5). The mode select circuit consists of S3, IC35C (IC16C), IC44A (IC5A) and IC44B (IC5B). Switch S3-A through S3-E selects the number of channels the multiplexer set will transmit. XMT 4 selects CH MODE, XMT 6 CH MODE, XMT 8 CH MODE, XMT 12 CH MODE and XMT 24 CH MODE signals are produced. Settings of S3 are encoded by IC35C (IC16C), IC44A (IC5A) and IC44B (IC5B) to produce a three-bit binary code (XMT 4/8/24 CH MODE, XMT 6/8 CH MODE and XMT 12/24 CH MODE). When all three lines are low, the multiplexer set is in the three-channel mode. Zero suppressor operation is done by S3-F, which produces the ZERO SUPPRESS signal. FULL REMOTE ALARM SELECT function is performed by S3-H, which produces the XMT FULL ALM SEL signal.

(10) *Clock MUX* (fig. FO-4, sheet 2 or 5). The clock MUX consists of IC34 (IC4). The 192 kHz, 256 kHz, 384 kHz, 512 kHz, 768 kHz and 1.544 MHz clocks are applied to the DO through D5 inputs of IC34 (IC4). Signals XMT 4/8/24 CH MODE, XMT 6/8 CH MODE and XMT 12/24 CH MODE are used to select one of the clocks which corresponds to the mode selected by the mode select circuit. The Y output of IC34 (IC4) is buffered by IC32A (IC13A) to produce XMT MBS CLK. Then W output is buffered by IC36F (IC65B) to produce XMT MBS CLK.

(11) *16kHz phase lock loop* (fig. FO-4, sheet 2 or 5). The 16 kHz phase lock loop consists of IC22E (IC32D), IC51 (IC42), IC22D (IC32F), IC22F (IC32C), IC23A .(IC24A), and IC31A (IC25A). The 16 kHz phase lock loop receives a XMT RESET TO CH 1 signal which is applied via inverter IC22E (IC32D) to phase lock loop IC51 (IC42). IC31A (IC25A), as clocked by the VCO output (pin 4) of IC51 (IC42), provides the second input to the phase-locked loop. The output of IC51 (IC42) is also supplied to one-shot IC23A (IC24A) which divides the signal down to 16 kHz. The output of the 16 kHz phase lock loop is then supplied as 16KPPS SYNC via buffer IC32D (IC13D) to the power module, TP5, and the fault monitor.

(12) *Fault monitor* (fig. FO-4, sheet 2 or 5). The fault monitor consists of IC25 (IC43), IC24 (IC54), IC33A (IC53A), IC33B (IC53B), DS1, and S1. Integrated circuits IC24A (IC54A) and IC24B (IC54B) are retriggerable monostable multivibrators with inputs supplied via flip-flops IC25B (IC43B) and IC25A (IC43A), respectively. The 16 KPPS SYNC signal included by IC25B (IC43B) from the 16 kHz phase lock loop with XMT 1.544 MHz from the clock divide chains. The XMT MBS CLK signal is clocked by IC25A (IC43A) from the clock MUX with XMT 4.096 MHz CLK BUS from the clock divide chains. Because the data period is much shorter than the time constant of the monostable multivibrators, the Q output of each mono-stable will be low as long as the input signals are present. The outputs of the multivibrators are NORed by IC33A (IC53A) and IC33B (IC53B). A detected fault (loss of input of IC25A (IC54A) or IC25B (IC54B)) will cause DS1 to illuminate and FAULT ALARM BUS to be supplied as an output from the DRIVER unit. When S1 is pressed, flip-flops IC25A (IC43A) and IC25B (IC43B) are reset causing the input to the multivibrators to go low and FAULT lamp DS1 to illuminate.

(13) *100-ohm bipolar MBS DATA OUT driver* (fig. FO-4, sheet 3 or 6). The 100-ohm bipolar MBS DATA OUT driver consists of IC36B (IC65D), IC36C (IC65E), IC26A (IC45B), IC6A (IC55D), IC36A (IC65C), IC16A (IC56B), IC6B (IC55A), IC6C (IC55B), Q4 (Q1), Q5 (Q2), T1, and S2. The reset input of IC26A (IC45B) disables the flip-flop when LOCAL LOOP is low to prevent data from being transmitted when the multiplexer is in local loop. If. XMT MBS CLK is low and the Q output of IC26A (IC45B) is low, the output of IC36A (IC65C) will be low. Each time this occurs the states of the Q and Q outputs of IC16A (IC56B) are reversed. The outputs are then ANDed with the data to produce an output from either IC6C (IC55B) or IC6B (IC55A), depending upon the states of the Q and Q outputs of IC16A (IC56B). The outputs of IC6C (IC55B) and IC6B (IC55A) are ac-coupled to drivers Q4 (Q1) and Q5 (Q2) which drive transformer T1. If Q5 (Q2) is being driven the current flow in the primary is from one to two and the output of T1 will be 5+ and 7-. Conversely, if Q4 (Q1)

is being driven, current flow in the primary will be from three to two and the output will be -5 and 7+. Switch S2 connects the output of the 100-ohm bipolar MBS DATA OUT driver or the 78-ohm balanced MBS DATA OUT driver to the MBS DATA OUT connector and to the +MBS DATA and -MBS DATA test points.

(14) *78-ohm bat MBS DATA OUT driver, 78-ohm bal NRZ MBS CLK OUT driver, and 78-ohm bal MASTER CLK OUT driver* (fig. FO-4, sheet 3 or 6). These drivers are identical so only the 78-ohm bal MBS DATA OUT driver is dis-

cussed. The XMT MBS CLOCK signal is applied to the input of two differential output line drivers with characteristic 78-ohm impedance. One driver provides a master clock and the other provides MBS clock. An identical 78-ohm balanced driver provides the MBS DATA output. All three circuits function identically, although the first two provide clocks and the latter data. The latter driver functions will be described. The synchronously clocked data from the output of IC26A (IC45B) is presented to two pairs of phase splitters: Q9/Q13 (Q9/Q10) and Q6/Q10 (Q3/ Q4). Each pair is common-emitter coupled, with the Q10 (Q4) and Q13 (Q10) bases referred to system ground. An input signal level approaching -5V cuts off Q9 (Q9) and turns on Q6 (Q3), causing Q13 (Q10) to conduct heavily and Q10 (Q4) to be cut off. The collector outputs of these phase splitter pairs provide the input signals to the push-pull driver pairs of Q8/Q12 (Q7/Q8), and Q7/Q11 (Q5/Q6). Under the given conditions, Q7 (Q5) and Q12 (Q8) are cut off while Q8 (Q7) and Q11 (Q6) are conducting heavily. This causes R25 (R42) to be sourced with approximately +5V and R28 (R49) with approximately -5V and heavy current flow from R39 (R43) and the external load. This push-pull differential current driver is capable of driving long distances over a twinaxial cable of 78-ohm characteristic impedance with minimum losses and reflections when properly terminated.

(15) *Loss of output detector* (fig. FO-4, sheet 3 or 6). The loss of output detector consists of IC67A (IC64A), IC67B (IC64B), IC66B (IC63B), IC66A (IC63A), IC33D (IC53D) and DS3. XMT MBS CLK and XMT MBS DATA are monitored by retriggerable monostable multivibrators IC67A (IC64A) and IC67B (IC64B). If clock and data signals are present, the monostable multivibrators remain in the triggered state. If either clock or data is missing the applicable monostable will time out causing the Q output to go high and the Q to go low. If either of the monostables times out, IC33D (IC53D) will illuminate OUTPUT LOSS lamp DS3 and IC66A (IC63A) will produce the LOSS OF OUTPUT signal.

d. RCVR Unit. Subparagraphs (1) through (21) below describe the individual circuits for all configurations of the RCVR unit shown in schematic figure FO-5 (configurations RCV02, 04, 06, and 08). The Reference Designation Effectivity List indicates all changes in reference designation. The columns marked RCV06 and RVC08 compare to the reference designations shown in the schematic. Columns marked RCV02 and RCV04 indicate what these components were labeled in earlier configurations. The integrated circuit (IC) reference designations were not changed and therefore are not shown. Table 3-1 in chapter 3 specifies what serial numbers were built to each configuration.

(1) *78-ohm data receiver* (fig. FO-5, sheet 2). For NRZ operation, data is applied to a 3 dB attenuator consisting of R21, R22, R23, and R24. The data at the output of the attenuator is clamped to 3.3 volts by CR10, CR11, CR12 and CR13 and applied to a differential line receiver, IC41A. The polarity of the signal at pin 1 is compared by IC41A with the signal at pin 2. If pin 1 is more positive than pin 2, the output at pin 4 will be a logic 1. If the signal at pin 1 is negative with respect to pin 2, the output will be a logic 0. The output of IC41A is applied to the input (pin 3) of IC51A. IC51A is a level shifter which shifts the 0 to +5 volt output of IC41A to a 0 to -5 volt level required by the logic in the data timing group.

(2) *78-ohm clock receiver* (fig. FO-5, sheet 2). Operation of the 78-ohm clock receiver is identical to the 78-ohm data receiver.

(3) *Bipolar receiver* (fig. FO-5, sheet 2). Bipolar data is applied to a 3 dB pad to terminate the input and to minimize reflections caused by input transformer T1. The secondary of T1 is center-taped which provides two outputs to differential line receiver IC44. The noninverting inputs, pins 1 and 12, are biased at approximately 0.7 volt. Due to the 180° phase shift of T1, IC44 will produce a pulse for positive data transitions (pin 4) and negative data transitions (pin 9). The outputs of IC44 are ORed together by IC54B to produce an output regardless of the polarity of the bipolar transition.

(4) *Bipolar clock recovery* (fig. FO-5, sheet 4). Bipolar data from the bipolar receiver is used to clock flip-flop IC64B. The J input is connected to the QD output of ÷15/16/17 counter IC74. The QD output of IC74 is inverted by IC55D and applied to the K input of IC64B. If the signal from the bipolar receiver transitions from high to low during the time the QD output of IC74 is high, the Q output of IC64B will be high. The Q output is NANDed by IC54A with the output of bipolar receiver and DC LOAD. The output of IC54A provides an up-clock signal to up/down ÷16 counter IC75. If the bipolar data transition occurs during the time QD of IC74 is low, the Q output of IC64B will be high. This is NANDed with the bipolar data and DC LOAD by IC54C

which supplies a down clock to IC75. If the phase of the bipolar data leads the QD output of IC74, the Q output of IC64B will be low more often than it will be high. Conversely, if the phase of the bipolar data lags the QD output of IC74, the Q output of IC64B will be high more often than it is low. Due to the difference in the number of up and down clocks produced by IC64B, IC54A and IC54B, IC75 will eventually overflow or underflow, causing IC65 to increment or decrement by 1. Initially, IC64B is preset to a 0001 condition so that it will not provide an output to the ÷15/ 16/17 counter until there has been a total of 128 more error pulses in one direction than in the other. Each time a borrow or carry pulse is produced by IC65, a DC LOAD is generated, which sets IC65 to 0001 and IC75 to 0000. When a carry is produced, the carry output of IC65 goes low. The carry is applied to the J input of IC62B, inverted by IC55B, and applied to the K input. When the 24.704 MHz clock from IC52 goes low, the data at the J and K inputs are transferred to the Q and Q outputs. Since the previous Q output of IC62B was a zero, the Q of IC62A will be a zero and the Q a one. Since the output to IC73A is low only when Q of IC62B and Q of IC62A are both high, the one from IC62B is shifted to the Q output of IC62A at the fall of the next clock. This produces a negative-going pulse one clock period wide. The output of IC73A is used to disable the parallel-enable input of IC74 when a carry pulse occurs. Variable length counter IC74 divides by 15, 16 or 17 depending on the conditions presented by the borrow and carry outputs of IC65. Since a carry pulse has occurred and the parallel enable is low, the counter will be loaded with 0001. This causes the counter to divide by 15. If no borrow or carry pulse occurs when the counter reaches its maximum count, no load pulse will occur and the counter will divide by 16. If a borrow is generated by IC65, flip-flop IC63B is set to a 1 at the fall of the first clock after the borrow occurs. The Q output of IC63B is NANDed with the TC output of IC74. Each time IC74 reaches its maximum count TC is produced. When TC occurs and Q of IC63B is set, the output of IC73 goes low and loads the counter to the 0000 state. The L input of IC74 remains low for one clock period which lengthens the time that the counter will count until ATC is generated by one clock, making the counter divide by 17. Each time a borrow or carry is produced, IC73B sets the Q output of IC63A low until the next TC occurs to reset IC65 and IC75. When the first clock after TC occurs, the Q output of IC63A is set to 1 and the sequence is repeated. The QD output of IC74 is used to enable the K input and is also inverted by IC55D and applied to the J input of IC64A. The Q output of IC64A is the recovered clock which is selected by the NRZ/bipolar MUX when the multiplexer set is configured for bipolar operation.

(5) *Bipolar data recovery* (fig. FO-5, sheet 2). The output of the bipolar receiver is applied to the J input of IC72A. The receiver output is also inverted and applied to the K input. The recovered bipolar clock is applied to the clock input of IC72A. If the bipolar receiver output is high at the clock transition, the output of the bipolar data recovery circuit will be a one-for-one clock period.

(6) *NRZ-bipolar MUX (*fig. FO-5, sheet 2). NRZ clock and data or bipolar clock and data are selected by the bipolar MUX. If S3G is open, the output of the bipolar data recovery circuits is selected by the multiplexer. Conversely, if S3G is closed, the output of the NRZ clock and data receivers are selected.

(7) *Loop MUX* (fig. FO-5, sheet 2). The loop MUX selects either the output of the NRZ/ bipolar MUX or the loopback clock and loopback data from the DRIVER unit. In the normal configuration, the output of the NRZ/bipolar MUX is selected by the loop MUX. If the loop switch is in the loop position or an external loopback command is present, the loop MUX connects loop back clock and loopback data to the clock recovery and FIFO circuits.

(8) *Loss of input detector.* (fig. FO-5, sheet 2). The loss of input detector consists of retriggerable monostable multivibrators IC77A and IC77B. The time constant of the monostable multivibrators is longer than the period of the clock and data pulses. As long as clock and data pulses are present, the output of the monostable remains in the triggered condition. If there is a loss of clock or data, the respective monostable multivibrator will go low causing the output of IC37C to go high. This produces a LOSS OF INPUT signal which is supplied to the alarm module. The LOSS OF INPUT signal is also supplied, via inverter IC36F, to INPUT LOSS lamp DS2 to cause the lamp to illuminate.

(9) *Phase detector* (fig. FO-5, sheet 3). The clock output of the loop MUX is divided by eight by the FIFO latch control and applied to the V input of IC57. The R input of phase comparator IC57 is driven by RCV MBS CLK and divided by eight by IC67. If the rising edge of the signal at input V occurs before the rising edge of the signal at the R input, the D1 input will go low, causing Q13 to conduct. Q11 pulls the base of Q12 to

ground, which causes it to conduct. This places -12V at the collector of Q12. If the phase relationships are reversed, the D1 output turns Q11 on, which places a ground level at the collector.

(10) *Loop filter* (fig. FO-5, sheet 3). The loop filter is a two-pole active low pass filter, which averages the number and width of the pulses from Q11 and Q12 and produces a voltage proportional to the average at the output. The output of the loop filter is clamped by VR5 to prevent the control voltage to the VCO from exceeding -5 volts and to prevent the voltage from going positive.

(11) *24.704 MHz VC0* (fig. FO-5, sheet 3). The 24.704 MHz VC0, IC45B, produces a square wave output. The frequency at which IC45B oscillates is determined by C38 (C36), C43 (C56) and the voltage from the loop filter.

(12) *Clock source select* (fig. FO-5, sheet 3). The clock source select circuit consists of IC46A, B and D and IC40B. This circuit is included for board-level testing. In normal operation, clock from the VCO passes through IC46B and IC46A. For test, the TST RCV CLK ENABLE is brought low. This disables IC46B and enables IC46A.

(13) *Clock divide chains* (fig. FO-5, sheet 3). The 24.704 MHz clock is divided by 16 by IC18 to produce 1.544 MHz for 24-channel operation. The 24.704 MHz is also divided by a ratio of 192/193 × 8 by IC47, IC49, IC38A, IC38B, IC39A, IC39B, and IC28B to produce a frequency of 3.072 MHz. The 3.072 MHz is further divided by IC27 to produce 768 kHz, 384 kHz and 192 kHz. The 24.704 MHz clock is also divided by a ratio of 192/193 × 3 by IC28A, IC48 and IC58 to produce 4.096 MHz. The 4.096 MHz clock is further divided by IC26 to produce 512 kHz and 256 kHz clocks. The Q of IC28A is buffered by IC37D, which drivers the receive 4.096 MHz clock bus.

(14) *Clock MUX* (fig. FO-5, sheet 3). The clock divider outputs with the exception of the 4.096 MHz clock are applied to the inputs of the clock MUX which selects one of the clocks. The clock selected by the MUX is dependent upon the control signals from the mode select. The outputs of the clock MUX are buffered by IC37A and IC37B to produce RCV MBS CLK and RCV MBS CLK. IC40C and IC40E buffer the RCV MBS CLOCK signal at the RCV MBS CLK test point.

(15) *FIFO* (fig. FO-5, sheet 3). The FIFO consists of 8-bit serial-to-parallel shift register IC80, which is clocked by CLOCK IN. When eight bits of data have been clocked through the register, the FIFO latch control strobes 4-bit latches IC69 and IC70, which hold the eight data bits as parallel data until parallel-to-serial shift register IC60 has clocked out the previous eight bits. When the last bit has been clocked out of IC60, the FIFO output control provides a load pulse, which loads the contents of the two 4-bit latches IC60 and the process is repeated. The OH and OH outputs of the FIFO output register are applied to the J and K inputs of IC50A. IC50A reclocks the data. The Q of IC50A is inverted by IC29B to become RCV MBS DATA which is buffered by IC40A and F for test point 2.

(16) *FIFO latch control* (fig. FO-5, sheet 3). The FIFO latch control consists of IC78, IC49D, IC68B and IC39C which produces a pulse one clock wide every eight clocks to load the FIFO latch.

(17) *FIFO output control* (fig. FO-5, sheet 3). The FIFO output control consists of 4-bit counter IC67, which is clocked by RCV MBS CLK. The eighth and 16th states of the counter are decoded by IC59B, IC59C, and IC68A. The output of IC68A loads the FIFO output register every eight clocks.

(18) *All ones remote/loop detector* (fig. FO5, sheet 2). The data output (pin 7) of the NRZ/ bipolar MUX is monitored for an all-ones condition by monostable multivibrator IC34A. In an all-ones situation where there are no transitions from high to low, IC34A times-out. The output of 1C34A is then inverted by IC55F to produce the remote alarm signal.

(19) *Frame search inhibit* (fig. FO-5, sheet 4). The frame search inhibit consists of IC9A, a MIL-133B line receiver and IC19C, which shifts the level from a 0 to +5 volt level from the line receiver to a 0 to -5V level for use by the DEMUX unit.

(20) *Fault detector* (fig. FO-5, sheet 3). The fault detector consists of IC76, IC73C, IC36C, IC36B, and DS1. IC76A and IC76B are retriggerable monostable multivibrators with inputs supplied from the clock MUX, and clock divide chains, respectively. With the data period being much shorter than the time constant of the monostable multivibrators, the Q output of each monostable will be low as long as the input signals are present. The outputs of the monostables are NANDed by IC73C and supplied to inverters IC36B and IC36C. The inverters supply a FAULT ALARM BUS signal as an output from the RECEIVER unit and illuminate DS1, respectively.

(21) *78-ohm bal REC RCV CLK driver* (fig. FO-5, sheet 4). The RCV MBS CLK signal is sup-

plied to the input of the differential output line driver and applied to phase splitters Q3/Q5 and Q2/Q4. Each pair is common-emitter coupled, with Q4 and Q5 bases tied to system ground. An input signal level approaching -5V cuts off Q3 and turns on Q2, causing Q5 to conduct heavily and Q4 to be cut off. The collector outputs of these phase splitter pairs provide the input signals to the push-pull driver pairs of Q9/Q7 and Q8/ Q6. Under the given conditions, Q8 and Q7 are cut off while Q9 and Q6 are conducting heavily, causing R8 to be sourced with approximately +5V and R9 with approximately -5V. This will cause heavy current flow from R10 and the external load. This push-pull differential current driver is capable of driving long distances over a twinaxial cable of 78-ohm characteristic impedance with minimum losses and reflections when properly terminated.

e. DEMUX Unit. Subparagraphs (1) through (14) below describe the individual circuits of the DEMUX unit.

(1) *Data input shift register* (fig. FO-6, sheet 2). The data input shift register consists of IC64A, IC40B, C, D and F, IC24, IC37, IC38 and IC39. RCV MBS DATA is reclocked and applied to a 32 bit serial shift register. The Q_A outputs of IC37, IC38 and IC39 provide the frame bit candidates to the frame bit prediction and check logic. Data from the Q_H output of IC37 is applied to IC24A and B inputs and to the fault monitor. The serial data is converted by IC14 to an 8-bit parallel word for use by the remote alarm detector. The Q_A output of IC24 is buffered by IC32A and IC32B and presented to the RCV PCM test point. It is also buffered by IC32F which drives the RCV DATA BUS. RCV MBS CLOCK is inverted by IC40F and reinverted by IC40B which supplies clock to the channel counter. The output of IC40B is inverted again by IC40C which supplies the clock for the data prediction and check logic. The output of IC40C is also inverted by IC40D and used to clock the input registers.

(2) *Remote alarm detector* (fig. FO-6, sheet 2). The remote alarm detector consists of IC23, IC25B, IC25C, IC25D, IC33, IC4D, IC34B and IC32D. IC25B, IC25D, IC23C and IC23D, IC23B, IC33C, IC23A and IC25C detect the 00001111 remote alarm pattern. If the RCV FULL ALARM SEL is low, and a remote alarm condition exists B2 will cause the output of IC33D to go low at the end of the channel time by the RCV CONT BUS. If the RCV FULL ALARM SEL is high, the output of the 00001111 detector appears at the output of IC33D. The output of IC33D is reclocked by IC34B only when the DEMUX is in the frame mode. The Q output of IC34B is buffered by IC32D and presented to the power unit and alarm unit via the REMOTE ALARM line.

(3) *24-channel pattern storage* (fig. FO-6, sheet 3). The 24-channel pattern storage consists of IC45, IC46, IC57B, IC65C, IC65D and IC68A. Data from the data prediction and check circuit is loaded into the DO input of IC45. The 00, 01, and 02 outputs of IC46 are loaded into the D1, D2 and D3 inputs, respectively, of IC45 on the falling edge of CLK. During the first four states of the cycle counter, IC68A is enabled by OGAT. IC68A then provides 16 write pulses to IC46, IC61 and IC66. During state 0 (the first state) of the cycle counter, inverted data is written into the first 16 locations of IC46. During the next 3 states of the cycle counter, data is shifted from the first 16-bit register, via the second latch in IC45, into the second 16-bit register. This continues until at the end of the first 4 states of the cycle counter, all four 16-bit registers are full. Addressing for IC46 is provided by the cycle counter. At the end of 4 cycles a history of the data of the previous 4 frames is contained in the 24-channel pattern storage circuit. Q_0, Q_1, Q_2, and Q_3 of IC45 are decoded by IC57B, IC65C and IC65D to provide the super-frame marker to the control unit.

(4) *Data prediction and check logic* (fig. FO-6, sheet 3). The data prediction and check logic consists of IC47, IC48, IC49F, IC57A, IC58A, IC35D, IC49D, IC55B, IC55C and IC35A. The 00, 01, 02 and 03 outputs of IC46 address IC47 and IC48 with 03 inverted at the enable input (pin 7) of IC47. The inputs of IC47 and IC48 are connected to -5, ground, or data inverted by IC49F. When the address is applied to IC47 and IC48, a bit equal to the next expected frame bit appears at the output of IC57A. If the address is not a valid frame pattern, the data bit appears at the output of IC57A. The predicted data passes to IC35D via data selector IC58A as enabled by CH-24. The predicted bit is compared by IC35D with the next frame bit candidate on the data line and produces a 1 if the data and predicted bit are the same and a 0 if they are different. The predicted bit is also applied to IC35A which feeds the predicted bit back to the 24-channel pattern storage if the frame bit candidate was good and inverts the predicted bit if the frame candidate was bad. The output of IC55B is also used to remove a 1 from the sieve memory if the frame bit candidate was bad.

(5) *Sieve memory* (fig. FO-6, sheet 3). The

sieve memory consists of IC66, IC55D, ICS5A, and IC46C. During states 0 through 3 of the cycle counter, one input of IC55A is held low which causes IC64C to remain in the set condition. The Q output of IC64C loads the first 16 bits of IC66 with 1's. During the acquisition sequence, ICS5A pin 3 is brought low. If the output of the data prediction and check circuit is then low, the output of IC55D will go low. A low output at IC55A will cause the Q output of IC64C to be low and a 1 to be left in the sieve memory. If the output of the data prediction and check logic is high, the 1 will be replaced by a zero. A zero indicates that the location in the 24-channel pattern storage is a valid candidate. If, at the end of 16 attempts to acquire frame, a candidate is not found, IC68D as gated by OGAT will cause the Q output of IC64B to go high. IC64B generates a reset signal which is used by the acquisition counter load logic.

(6) *Acquisition counter* (fig. FO-6, sheet 3). The acquisition counter consists of IC21, IC31, IC42, IC51A, IC51D, IC41D and IC41E. Clocks for the acquisition counter are inverted by IC11D and applied to the clock input of IC21, IC31 and IC41. The division ratio of the acquisition counter is determined by preset signals from the mode select circuit and applied to the A, B, C and D inputs of IC21, IC31 and IC41. The counters are preset each time the load of the acquisition counter load logic output goes low. The carry (RCO) outputs from IC21 and IC31 are applied to IC51A. When both counters overflow, the output of IC51A goes low. Each time this happens IC42 is advanced one count. The output IC21 and IC51A are used by the acquisition counter load logic to produce early and late load pulses in the 24-channel mode. The carry from IC42 and the output of IC51A are inverted by IC41D and applied to IC51D. This produces the enable for the cycle counter and provides the late load enable to the acquisition counter load logic in the 3-, 6-, or 12-channel mode. The Q_D output of IC42 is used to provide the early load enable. The outputs of IC21 and IC31 are used to address the 24-channel pattern storage circuit, the low rate pattern storage and the sieve memory.

(7) *Acquisition counter load logic* (fig. FO-6, sheet 3). The load logic consists of IC51B, IC51C, IC52D, IC63A and IC63B. The load logic presets the acquisition counter each time the counter overflows. The load logic also provides a load pulse if the sieve is empty and the acquisition counter overflows. When this condition exists, the cycle counter is loaded With zeros and the load to the acquisition counter is held off for 16 clocks. This shifts the acquisition window by 16 bits.

(8) *Cycle counter* (fig. FO-6, sheet 3). The cycle counter consists of IC3A, IC11A, IC52C, IC43, IC52A, IC52B, IC41F and IC44. IC3A and IC11A are used to buffer the RESET BIT COUNTER signal is used during test. Either the shift preset or state 4 is applied by IC52C from the control logic to the load input of IC44. If the load pulse is received from the load logic, the counter will be loaded with zeros. If the load pulse is produced by the control logic, the counter will be preset to state 11. Each time the acquisition counter overflows, the P input of IC43 is enabled. This causes the counter to advance one state. The Q_A, Q_B, Q_C and Q_D outputs of IC43 are decoded by IC52A, IC52B, IC53A and IC41F to produce a high when the counter is in state zero. This signal is applied to the D1 input of IC44. The output of IC52A is applied to the D1 input. The ZD output of IC44 is used by the sieve memory to load l's into each location in the sieve at the beginning of the acquisition cycle. The BO and B1 inputs of IC44 are connected to the carry outputs of the acquisition counter. The signal at BO is 16 clocks wide and occurs during the last 16 cycles of the acquisition counter. The signal at the B1 input is 256 clocks wide and occurs during the last 256 states of the acquisition counter. The ZB output is the operational gate. The CO input of IC44 is the RCO signal from IC43. Signal RCO indicates that the counter is in state 16 and the clock is low. The C1 input of IC44 is the Q_C output of IC44 which indicates that the counter has reached state 4. The ZC output is NANDed with OGAT to produce the END OF CYCLE signal.

(9) *Control unit* (fig. FO-6, sheet 3). The control unit consists of IC53B, IC68B, IC56A, IC64D, IC67D, IC56C, IC;56D, IC53C, IC65A, IC63D, 1C65B, IC67B, IC63C, IC67C, IC54, IC32C, IC3E, IC53B, IC59C, IC69A, IC57C, IC57D, IC60B, IC34A, IC49A and IC49B. At the beginning of the acquisition cycle IC54 is in state 0. When the end of frame signal is received by IC63D, and the first 1 in the sieve memory is encountered, the load (LD) input of IC54 is brought low by IC63C which causes the Q_C output to go high. When IC54 Q_C goes high, 1C63D is disabled. After the cycle counter has completed the frame search portion of the cycle, both inputs of IC68B will be high causing the output to go low. The signal from IC68B travels through IC56A, IC67D, IC65B and IC63C which pulls the load input of IC54 low. Since IC54 Q_C is high, the

Q_A, Q_C and Q_D outputs will be high. The Q_D output also enables the T (toggle enable) input. Since he counter has now entered state 13, the frame error monitor enters the monitor mode. The Q and Q outputs of IC64D are applied to one input of IC56C and IC56D, respectively. The other input of IC56C and IC56D is disabled by IC53C when the CTPRE signal is low or the FRAME SEARCH INHIBIT line is high. IC28B inverts t} e frame search inhibit signal. The output of I56D will go low if the data and predicted bit 9o not match. IC56D enables IC54 via the P input ,which allows the counter to advance 1 state. It 'also clears prime flip-flop IC60B to 0, via IC57D, and supplies an error pulse to the D input of IC34A. The output of IC34A, as clocked by CLK 2, is buffered by IC49A and IC49B to supply frame error information to the user. The output of IC56C remains high so long as a frame bit error does not occur. The output of IC56C is gated through IC69A as long as the prime flipflop is set. The output of IC69A is inverted by IC59C and applied to IC65A to allow IC54 to be loaded to state 13 each time a match occurs. Integrated circuit IC65B also enables IC67B. IC67B is used to gate the output of the superframe detector to prevent the frame counter from being set by SFPR if a wrong superframe indication or frame error occurs. The output of IC67B also disables IC67C when the SFPR signal occurs. The output of IC67B provides the PRI signal to the channel counter as long as the DEMUX unit is in frame and the candidate and predicted bit compare favorably. When a good bit is received following a bad bit, prime flip-flop IC60B is set via IC57C and IC57D.

(10) *Low rate pattern storage* (fig. FO-6, sheet 3). The low rate pattern storage consists of RAM IC61. IC61 receives 8 addresses from the acquisition counter. Clocked write enable pulses are applied to the WE input of IC61 during the period of OGAT to cause data from the 24-channel pattern storage circuit to be written into the memory. Data read from the memory is supplied to the data prediction and check logic.

(11) *Bit/channel/frame counter and decoder* (fig. FO-6, sheet 2). The bit/channel/frame counter and decoder consists of IC4A, IC4B, IC7A, IC7B, IC8, IC9, IC10, IC7E, IC7F, IC3D, IC6C, IC6D, IC29A, IC5D, IC5C, IC6A, IC4C, IC5A, IC5B, IC50A, IC29D, IC50B, IC60A, IC50D, IC28E, IC20, IC18, IC17, IC27D, IC28A, IC27A, IC12A, IC12B, IC12F, IC27C, IC7D IC27B, IC26, IC30A, IC28C, IC28D, IC30C, IC19, IC7C, IC30D, IC29C, IC6B, IC59E, and IC59F. The 3CH, 6CH, 12-24 and 6-8CH signals from the mode select logic are applied to IC5D, IC5C, IC6C and IC6D. The Q_A, Q_B, Q_C and Q_D outputs of IC20 are applied to the other input of each gate. The output of IC50A provides a preset pulse to the channel counters which occurs when the selected number of channels has been reached. Bit counter IC19 is clocked by RCV MBS CLK and preset to either 7 or 8 to produce a ÷9 or ÷8 counter. In the 24-channel mode IC30C is enabled by 24CH. This allows the counter to be preset to 7 rather than 8 each time PRI occurs. This is done to allow one additional bit time at the beginning of each frame to correct for the frame bit. IC30A loads the bit counter with the 4 bit binary word at the A, B, C, and D inputs of IC19 each time an RCO is produced by IC19 or a load pulse is generated by IC50A. RCO from IC19 is reclocked by IC60A, to delay the pulse by a half-clock period. IC50B, by delaying clock by approximately 50 ns, produces a narrow pulse which is resynchronized by IC29D. The output of IC29D is NANDed with the QD output of IC19 and applied to channel counter decoders IC8, 9 and 10 to disable the decoders while the multiplexer set is receiving framing information. Channel counter decoders IC8, 9 and 10 are three-to-eight line decoders. Each decoder has 3 enable lines (2 active low and 1 active high). One of the enable inputs of each decoder is used in the 24-channel mode to prevent the frame bit from being recognized as data. The 2 remaining inputs are used to select the appropriate chip for the channel being selected. Pin 4 (active low enable input) and pin 6 (active high input) are connected to the Q_C and Q_D outputs of IC20 to enable IC8 when Q_C is low and Q_D is high. IC9 is enabled when Q_C is high and Q_D is low and since IC7C inverts the Q_D, output of IC20, IC10 is enabled when both Q_C and Q_D are low. The RCV RESET TO CH 1 signal is generated by IC7A, IC7B, IC4A, R3 and C4. IC7B inverts the RCV CH CTR 1 signal and applies it to R3 and IC4A. R3 and C4 provide a delay of approximately 30 ns so that IC7A receives the signal after IC4A. Since the inverter is connected to the other input of IC4A, both inputs will be high until C4 charges. This causes the output of IC4A to go low until the state at the output of IC7A goes low. The RCV DATA BUS CLK is produced when IC6B gates MBS CLK with the Q output of IC60A. IC17 functions as the frame counter and is preset to 0010 each time CTPRE occurs or when the counter overflows. By initially setting the counter to 4, frame 6 is decoded from the Q_B and Q_D outputs by IC29C and frame 18 is decoded by IC27D from

the Q_A and Q_C outputs. The Q_D output is buffered by IC59F to drive the 12 FRAME test point. IC18 is a 4-bit binary counter which produces the CTPRE signal in the 24-channel mode. It also produces the third address bit required only in the 24-channel mode and the 24 FRAME test signal from the QA output. A quad 2-line-to-1-line data selector (IC26) is used to select CTPRE for high and low rate modes and to provide presets to the bit/channel/frame counter and decoder.

(12) *Fault monitor* (fig. FO-6, sheet 2). The fault monitor consists of IC16, IC15, IC25A, IC14, IC13, IC12D, IC12E, IC30B, IC22B, IC62D, IC62A, IC59A, IC62C, IC62B, DS1, DS2 and DS3. Integrated circuits IC15 and IC16 are 8-line-to-1-line data selectors. The inputs monitor sieve memory activity, acquisition load counter activity, frame counter activity and the carry output of the bit counter. The outputs of IC15 and 1C16 are ORed by IC30B and applied to 4-bit binary counter IC13. The RCO output of IC13 clocks IC14 and IC22B. When 16 pulses have occurred at the clock input of IC13, a pulse is produced at the RCO output. This output is inverted by IC12E and applied to the clock input of IC14. Address information is provided by IC14 to IC15 and IC16. Each time the counter is clocked, the address to the data selectors is advanced by one bit and the next point being monitored is examined. If any of the signals at the inputs to IC15 and IC16 are missing, the output from IC13 will be missing. If this occurs, IC22B, a retriggerable monostable multivibrator which is being constantly triggered by IC13, is allowed to time out. When this occurs, the Q output will go high causing IC62D to pull the FAULT ALARM BUS low and IC62A to light the FAULT lamp. The sync loss lamp is driven by IC62C when the DEMUX unit is not in frame. The external FRAME SEARCH INHIBIT signal drive IC62B and illuminates the FRAME SEARCH INHIBIT lamp to indicate that an external inhibit signal is applied. All indicator lamps are illuminated by IC59A when the FAULT TEST pushbutton is pressed, making one input of IC62C, IC62D and IC25A high.

(13) *Pattern detector* (fig. FO-6, sheet 3). The pattern detector consists of IC35, IC36, IC40, IC56 and IC58. Each time a 011 or 100 pattern is detected by IC35B, IC35C, and IC36B, the output of IC36B will go low. The output of IC36B is applied to data selector IC58 and used in the 3-, 6- or 12-channel modes to indicate frame bit candidates. NOR gate IC56B is used as a negative logic NAND gate to detect the 011 pattern. The output of IC56B is applied to IC58 and used as the low rate superframe marker by the control unit. The output from the input shift register is buffered by IC40A and IC40E and applied to the RCV PCM BUS.

(14) *Mode select logic* (fig. FO-6, sheet 3). The mode select logic consists of IC1, IC2, IC3 and IC11. The RCV 12/24 CH MODE, RCV 4/8/24 CH MODE, and RCV 6/8 CH MODE signals from the RCVR unit are inverted by IC3B, C, and F and applied to 3-line-to-8-line decoder IC2. The outputs from IC2 are recoded by IC1 and IC11 to provide preset signals for the acquisition counter.

f. *PCD Unit*. Subparagraphs (1) through (10) below describe the individual circuits of the PCD unit.

(1) *Serial-to-parallel converter* (fig. FO-7, sheet 2). The serial-to-parallel converter receives PCM data on the RCV PCM BUS as buffered by IC12D. The data is clocked into the B input of IC52 by RCV MBS CLK from IC12C. The eight parallel outputs of IC52 are strobed into 8-bit latch IC62 by RCV ADV CH CTR, which is buffered by IC12E and IC11B. The outputs of the eight bit latch are then applied to the inputs of 8-bit D-to-A converter IC72 in the D-to-A converter.

(2) *D-to-A converter* (fig. FO-7, sheet 2). The D-to-A converter consists of IC72 which is a companding converter that produces a differential current output at the IOD+ and IOD- outputs. The gain of IC72 is adjustable by R110, a front panel gain control potentiometer.

(3) *Current driver* (fig. FO-7, sheet 2). The current outputs of IC72 are converted to a voltage by differential amplifier AR1. The output of AR1 is isolated by R118 and applied to the front panel PAM test point. The PAM signal is also applied to the channel decode circuit.

(4) *Channel decode* (fig. FO-7, sheet 3). The channel decode circuit consists of IC81, IC82, IC73, IC74, and IC75. The PAM output of AR1 from the current driver is applied to DR inputs of three-line-to-eight-line decoders IC73, IC74, and IC75. The decoders decomutate the PAM data and apply it to 24 sample and hold circuits. The channel select signals (A SEL, B SEL, and C SEL) and the multiplexer select signals (MUX 1, MUX 2, and MUX 3) are buffered by IC81 from the channel count decoder output select and channel count decoder select, respectively. The registers used for level shifting are contained in IC82. The multiplexer select signals are used to enable the decoders in sequence for eight channel times.

The channel select signals select the individual channels in the three decoders.

(5) *Output sample circuits* (fig. FO-7, sheets 3 and 4). Since the 24 output sample circuits are identical, only one will be described (Channel 1). The PAM pulse is stored by C143 and IC54A, which hold the voltage at the output of IC54A at the same level as the PAM pulse until the next CHAN 1 PAM pulse is strobed into the sample and hold. The output of the sample and hold IC54B and IC54A is connected to a low pass filter. This limits the bandwidth of the signal to reduce switching and sampling noise and provides a clean sine wave output to the VF module.

(6) *Channel count decoder output select* (fig. FO-7, sheet 2). The channel count decoder output select circuit consists of IC12A, IC21E, IC31A, IC31B and IC41B. IC31A, IC31B and IC41B comprise a 3-bit binary counter which produces A SEL, B SEL, and C SEL signals. The RCV RESEL TO CH 1 signal, is buffered by IC12A and IC21E to reset the counter.

(7) *Channel count decoder select* (fig. FO-7, sheet 2). The channel count decoder select circuit consists of IC11C, IC41A, IC51A and IC51B. IC51A and IC51B are clocked by RCV ADV CH CTR and are connected with IC41A to form a three stage shift register. If the outputs of IC51A and IC51B are both low, a 1 is loaded into IC51A and IC11C at the next RCV ADV CH CTR. The bit at the output is shifted into IC51B at the next RCV ADV CH CTR pulse. When the bit is shifted into the last counter, a 1 is produced at the D input of IC51A. When the next RCV ADV CH CTR occurs, the 1 at the input of IC51A is clocked to the Q output and the Q output of IC41A goes low.

(8) *Sample enable* (fig. FO-7, sheet 2). The sample enable consists of 8-stage shift register IC1, IC11A and IC11D which function as an RS flip-flop. When the RCV ADV CH COTR goes high it is loaded into the input of the shift register. The register is clocked by RCV MBS CLK which shifts a 1 in the first stage one bit at each negative clock transition. At the fall of the second clock the RS flip-flop is set. At this time the output of the channel count decoder select circuit is gated through NAND gates IC71D, IC71C, and IC71A to enable the decoders. When the register has been shifted by 4 more bits the RS flip-flop is reset, and the NAND gates disabled.

(9) *Signaling* (fig. FO-7, sheet 2). The 1Q output of IC62 is applied to the D input of IC61A. Each time RCV ADV CH CTR goes high, the data at the D input is stored for one channel time. When RCV FRAME 6/18 is high, IC71B passes the Q output of IC61A and inverts the signal. The RCV SIG A bus is isolated from IC71B by R2. IC21C inverts the output of IC71B, which drives the SIGNAL test point on the front panel of the module.

(10) *Fault monitor* (fig. FO-7, sheet 2). The fault monitor circuit consists of one-shot multivibrators IC32 and IC42 which are triggered by the MUX 1 SEL, MUX 2 SEL, MUX 3 SEL, and B SEL signals. The time constants of the oneshots are longer than the time between trigger pulses. This causes them to remain triggered. If any of the signals being monitored are missing, the associated one-shot will timeout and the output will go low. The outputs of the one-shots are ORed together by IC22. If any one-shot timesout the FAULT lamp on the unit will light and the FAULT ALM BUS will go low. When the FAULT TEST pushbutton is pressed, all of the one-shots are reset. This will light the FAULT lamp, the ALL FAULT TEST lamp and will pull the FAULT ALM BUS low.

Section III. VF MODULE

2-7. General Information

The VF module (fig. FO-8) provides the multiplexer set voice frequency channel interface with a 4-wire telephone trunk. The VF module converts the office trunk VF signals to a standard format for transmission and returns received signals (from far-end) to trunk format. To accomplish this, the VF module adjusts the levels of transmitted and received VF signals, processes idle/busy signal status, and responds to carrier group alarm (CGA) by terminating all calls.

2-8. Major Functions

The VF module (fig. 2-23) is functionally divided into three sections; transmit, receive, and signaling. These functions are described in subparagraphs a through c below.

a. Transmit Function. In the transmit branch, transformer T1 couples the VF from the T-R leads into the variable gain transmit amplifier with approximately 1 db insertion loss. The gain of this amplifier may be adjusted to obtain a nominal 0 dBm at the XMT LINE-UP jack.

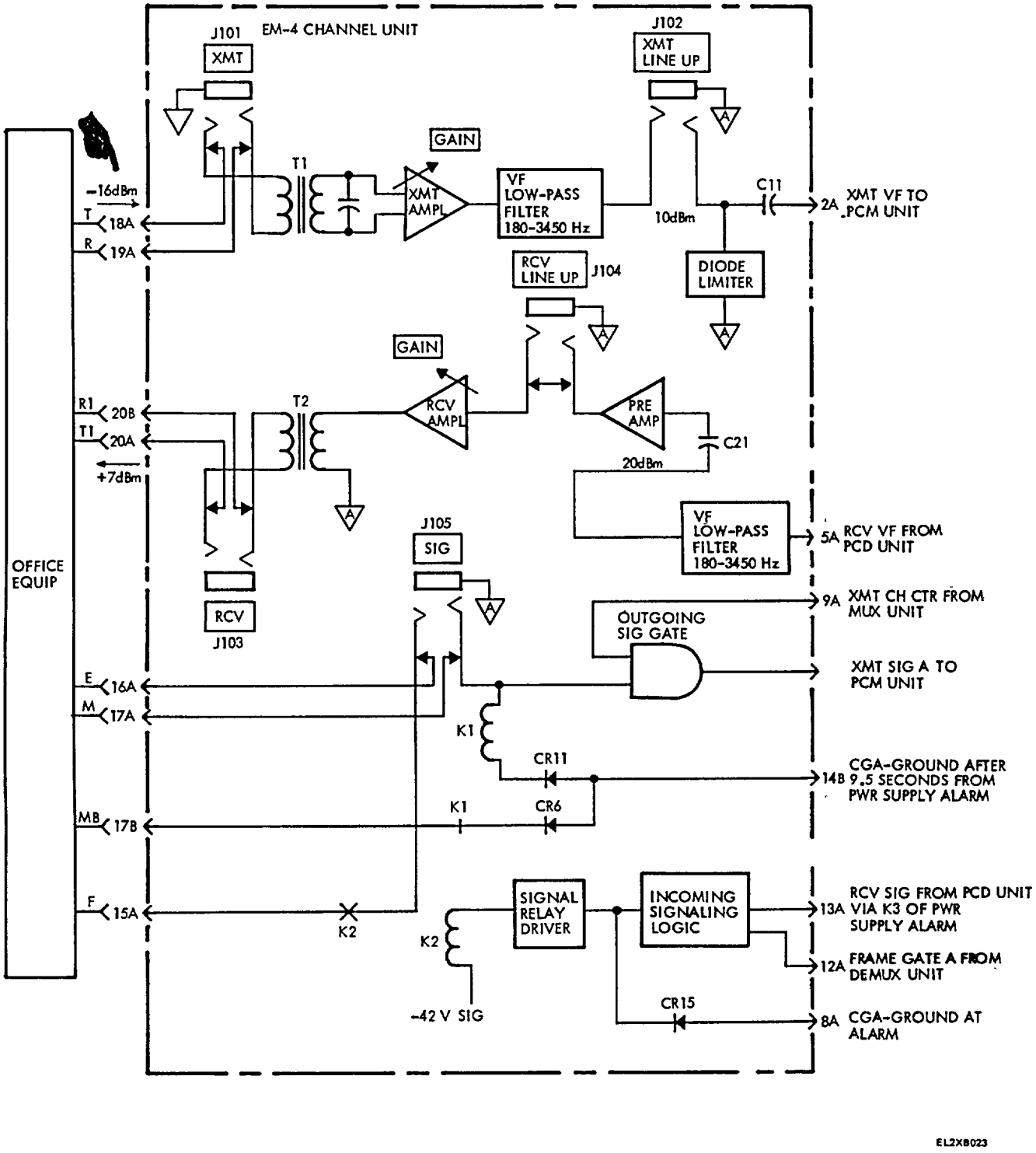


Figure 2-23. VF Module Block Diagram.

The low-pass filter limits the VF to 3450 Hz. The diode limiter limits the signal level to ±1.2V (3 dBm 0) to prevent crosstalk at the sampling gates of the PCM unit.

b. Receive Function. The incoming prefiltered VF data from the PCD unit analog demultiplexer are frequency limited in the low-pass filter, preamplified and applied to the input of the variable gain receive amplifier. The VF signal level at the RCV LINE-UP jack is nominally -20 dBm. The gain of the RCV amplifier may be adjusted to obtain a nominal +7 dBm at the RCV jack after approximately 1 dB attenuation through transformer T2.

c. Signaling Function. The VF signaling circuits process the E, M, F, and MB leads associated with the office trunks. The VF module recognizes an open circuit ground on the M lead as the on-hook or idle condition; office battery on the M lead indicates the off-hook or busy condition. The outgoing signal gate senses the state of the M lead. When enabled by the XMT CH CTR pulse, the gate transfers an idle/busy indication to the MUX unit for transmission to the far-end. Incoming signaling from the PCD unit appears on the RCV SIG input to the incoming signal gate. The RCV CH CTR pulse, applied to the incoming signal gate when the frame gate is in the proper state, allows this bus to be sampled at the proper time for that VF channel. The condition of the bus at the time it is sampled determines whether relay K2 will be operated or released by the relay driver. Relay K2 operates when the far-end is off-hook and closes the connection between the E and F leads. When the far-end is on-hook, relay K2 releases, and the E lead is left open. The VF module terminates existing calls by making them appear on-hook (E lead open) if a CGA occurs. In addition, a CGA makes all idle channels appear busy by grounding the MB lead. This is accomplished in the following manner:

(1) All outgoing calls are terminated by forcing the far-end on-hook and releasing the appropriate selectors. If the M lead is ground (on hook) at this time, the MB lead remains at ground until the alarm clears. If the M lead is at the office battery potential (off-hook), the MB lead goes to ground, and relay K1 operates to open the MB lead. The MB lead remains open until the office selector is released. When the M lead goes to ground (on-hook), K1 releases and the MB lead returns to ground until the alarm clears.

(2) Incoming calls, regardless of the idle/ busy condition, are made to appear on-hook (idle) by a CGA. When this occurs, CGA, through CR15, forces the signal relay driver to release K2, and the E lead connection to the F lead is opened.

2-9. Circuit Descriptions

The VF module consists basically of four circuits, transmit, receive, transmit signaling, and receive signaling. Each of these circuits is described in detail in subparagraphs a through d below.

a. Transmit Circuit (fig. FO-8). The voice-frequency (ring and tip) transmit leads enter the VF module and are applied via jack J101 to input transformer T1. The front-panel XMT jack (J101) allows insertion of a test signal into the transmit path. The resistance of the transformer windings, plus resistors R1 and R2, form the 600 ohm input impedance of the VF module, which terminates the trunk. Capacitor C2 contributes to the internal inductance-capacitance characteristics of the transformer. Its purpose is to adjust the transformer's return loss value to meet specified requirements at the high end of the voice band. Resistors R1 and R2 form a voltage divider that allows the VF module to accept either of two different nominal input signal levels. Where the voice frequency signal applied to the VF module is referenced to a test signal of -16 dBm, strapping across A terminals connects the divider high point to transmit amplifier Q1. Where the voice frequency signal applied to the VF module is referenced to a test signal of 0 dBm, strapping across B terminals connects the divider intermediate tap to transmit amplifier Q1. The divider low point connects to ac ground via capacitors C3 and C4.

(1) Transistor Q1 forms the transmit amplifier. Resistors R8 and R9 establish the dc potentials on their collector and emitter, respectively. Resistor R5 is the base-current-limiting resistor. Base bias is provided by voltage divider R3-R4 via R1, R2 and the secondary winding of T1.

(2) Resistors R6 and R7, and potentiometer R101, form a gain controlling network for Q1. The network operates by placing a variable resistance bypass across R9, which alters the value of R9 as seen by the ac signal at Q1 emitter. This changes the circuit's negative feedback, which changes its gain.

(3) Resistor R8 provides input termination for the transmit VF filter, which consists of L1, L2, C5, C7A and C7B, C8, and C9. The filter cuts off components of the voice frequency signal above 3250 Hz. Resistor R10 and capacitor C6 bypass R9 to increase the gain of Q1 for frequencies around 3 kHz. The adjustment compensates

for an irregularity in the characteristic curve of the filter. Output termination for the filter is a 604-ohm resistor across a 0.068 micro-farad capacitor, both of which are located in the PCM unit.

(4) Diode network CR1 through CR4 limits the signal level at the output to -1.2 volts. The front panel XMT LINE-UP jack (J102) permits measurement of the VF module output signal to the PCM unit. Capacitors C10 and C11 block dc potentials which may be present in the test equipment connected to J102 from feeding back into the VF module or forward into the PCM unit.

b. Receive Circuit (fig. FO-8). The prefiltered VF data signal from the PCD unit is applied to the receive VF filter ,the low-pass action of which restores the signal to VF form. The filter consists of L3, L4, C23, C24, C25, and C26 on the VF module circuit board. Two more components, a 2.2k ohm resistor in parallel with a .018 micro-farad capacitor across the filter input, are located on the PCD unit. The filter output is applied to a preamplifier consisting of transistors Q5, Q6 and associated components. Resistor R30 establishes the base bias on Q6; resistor R31 and capacitor C22 provide additional power supply filtering, and C20 bypasses Q6 emitter to ac ground. Capacitor C19 and resistor R26 provide frequency-selective bypassing of the feedback path from Q5 emitter to Q6 base. This bypass increases the gain of the preamplifier at frequencies around 3 kHz, compensating for the irregularity in the curve of the receive filter.

(1) In addition to providing external compensation for the receive filter, the preamplifier provides impedance matching between the filter output and the tip terminal of J104, the RCV LINE-UP jack. The RCV LINE-UP jack permits a dB meter to be connected to measure the received signal. When so connected, the meter termination is provided by R24. Capacitor C18 provides dc isolation between the meter and Q5.

(2) Jack J104 may also be used to inject a test signal toward the receive amplifier, which consists of transistors Q2, Q3, Q4, and associated components. The test signal generator is connected to the J104 ring terminal, capacitor C16 provides dc isolation between the generator and Q4, and R22 provides termination for the generator input.

(3) The three-transistor receive amplifier has adjustable overall negative feedback through gain control R102. Gain control R102 permits the output power at J103 to be adjusted for one of the two required nominal output levels: +7 dBm or 0 dBm. For the 0 dBm, option strap C is installed so resistor R16 parallels R102. If the nominal +7 dBm output level is required, strap C should not be used. With strapping terminals C connected, the output range is -7 dBm to +3 dBm. Without the strap, the range is 0 to +10 dBm. In this amplifier, only Q4 emitter is bypassed (C15). The R17-C14 network is a frequency selective negative feedback path for Q3 that decreases Q3 gain at the high end of the voice band. This network, and the one consisting of R23 and C17 in the input to the amplifier, are designed to reduce noise through the circuit.

(4) Capacitor C13 provides dc isolation for the output transformer, T1. Resistors R13 and R12 terminate the trunk to which the transformer connects. Capacitor C12, like its counterpart in the transmit path of the unit, contributes to the reflected impedance characteristics of the transformer.

c. Transmit Signaling (fig. FO-8). Transistor Q8 converts M lead action to the logic levels required by the PCM unit (low = -5.0V, high = 0.0V). When battery appears on the M lead, indicating off-hook signaling in the transmit direction, -48 volts appears at Q8 base, biasing the transistor off. With the transistor off, pin 10A remains high when the channel counter pulse arrives to interrogate the unit. When ground or an open appears on the M lead, indicating on-hook signaling in the transmit direction, Q8 base is held at 0 volt through R35. This biases the transistor on. When the channel counter pulse arrives to interrogate the unit, the low-pulse passes through the transistor to the SIG A lead. The MAKE BUSY output (pin 17B) normally appears to the office equipment as an open. A CGA results in a ground at pin 14B 9.5 seconds later. If a CGA occurs while the M lead indicates an off-hook condition, relay K1 operates. Its 3-4 contacts open, placing an open on the MAKE BUSY lead to the central office equipment. When the off-hook condition on the M lead ceases, K1 releases. Its 3-4 contacts close, placing a ground on the MAKE BUSY lead. With no CGA in effect, the MAKE BUSY lead appears as an open from the open on pin 14B. If a CGA occurs with the M lead indicating on-hook, ground appears on the MAKE BUSY lead as soon as pin 14B goes to ground.

d. Receive Signaling (fig. FO-8). The receive signaling from the PCD unit appears on the REC

SIG A bus and reflects the status of B8 bit. This signal is high for on-hook. and goes low for off-hook during signaling frame. FRAME GATE A goes low during signaling frame A. The RCV CH CTR pulse goes low for a particular channel at all frames. When REC CH CTR occurs and FRA)FE GATE A enables gate IC1D, differentiator circuit CR30/R42 produces a short high pulse, setting the signaling flip-flop made up of gates IC1A and IC1B3. The REC CH CTR pulse also enables gate 1C1C and resets the flip-flop if RCV SIG A is low. If REC SIG A is high, the flip-flop remains set after REC CH CTR. When the output IC1B-2 goes low, Q7 is turned on, activating relay K2. When K2 operates, it closes its normally open contacts 1 and 5, connecting E and F leads (pins 16A and 15A). Normally. the F lead is connected to ground, providing ground to E lead during the far-end off-hook state and open during the on-hook state. For tandem operation (option E) when ground and -42 Vdc are required on the E lead, F lead is connected to the -42 Vdc. Strap E provides ground through relay K2 normally closed contacts 1 and 4. Capacitor C28 and resistor R33 serve as protection for the relay K2 1-5 or 1-4 contact. Strap D1 provides contact protection for normally open relay 1(2 contacts in the normal signaling convention. When using the tandem signaling convention, strap D2 is installed to protect normally closed relay K2 contacts.

Section IV. 0-20 KB/S DATA MODULE

2-10. General Information

The 0-20 kb/s module (fig. FO-9) is a full duplex data module transmitting synchronous data at any rate from 0 to 20 kb/s. It provides a 135-ohm balanced interface for transmit and receive data. The module can be used with all configurations of the multiplexer set and replaces one voice frequency module. It operates by encoding asynchronous data in a 2-bit transitional code, which is then transmitted at a synchronous rate of 56 kb/s.

2-11. Major Functions

The 0-20 kb/s data module block diagram is shown in figure 2-24. Transmitted data is received by a 135-ohm balanced transmit interface and sent to a 2-bit transitional encoder. The output of the encoder is a synchronous 56 kb/s data stream. This data stream is buffered in an elastic buffer where a dummy 1 is added after each 7 bits to produce a 64 kb/s data stream. It is then transferred to the MBS data bus in bursts of seven bits at the MBS data rate. The major functions of the module are described in subparagraphs a through d below.

a. Transmit Timing and Control Circuits. These circuits control the encoding and data transfer from the DRIVER unit to the XMT MBS DATA bus. It uses the XMT 4.096 MHZ clock to derive the 56 kb/s and other timing pulses necessary for operating the transmit portion of the module.

b. Receive Data. This data enters the module in bursts of seven bits at the MBS rate. The bursts are buffered in the receive FIFO buffer and sent to the 2-bit transitional decoder, which removes the coding to restore the original 0-20 kb/s asynchronous data stream. This data stream is transferred to the interface unit, which produces a 135-ohm balanced NRZ signal.

c. Receive Timing and Control Circuits. These circuits control the data transfer from the RCV MABS DATA bus to the receive data buffer and to the transitional decoding of the buffer output. It uses the RCV 4.096 MHZ clock to derive the 56 kb/s and the RCH COUNT signal from the DEMUX unit for operating the receive portion of the module.

d. 2-Bit Transitional Coding/Decoding. This coding and decoding process is shown in figure 2-25. Shown on the top line is a sample of asynchronous data; on the second line is the 2-bit transitionally encoded data. Asynchronous data bits continually of the same polarity result in the same continuous data bit polarity in the encoded data. A transition from one polarity to the other in the asynchronous data results in the same transition in the encoded data. The exception is that the second bit (the bit immediately following the first bit of changed polarity) contains information as to whether the asynchronous transition took place during the first (early) or second (late) half of the synchronous 56 kb/s clock period. The second bit is a logic 1 for an early transition and a 0 for a late transition. Except for this bit, the encoded data is the asynchronous data sampled by the 56 kb/s clock. However, due to the early/ late information carried by the second bit, the sampling has a time resolution equivalent to a 112 kb/s clock. The alarm circuit monitors the XMT MBS CLK, 56 kb/s XMT CLK, RCV MBS

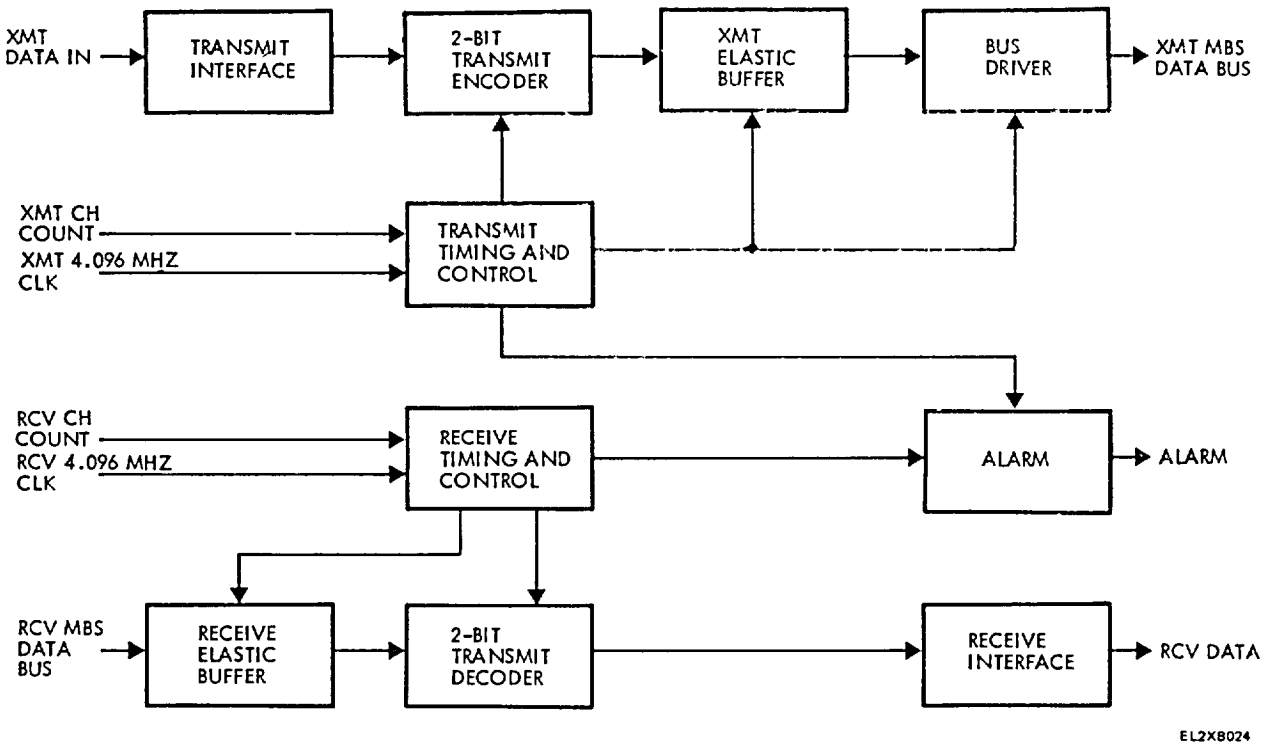


Figure 2-24. 0-20 kb/s data module block diagram.

CLK and the 56 kb/s RCV CLK. If any of these signals are missing, an alarm is generated by the module.

2-12. Detailed Descriptions

The 0-20 kb/s data module consists of transmit interface, 2-bit transitional encoder, transmit elastic buffer, bus driver, transmit timing and control, receive elastic buffer, 2-bit transitional decoder, receive interface, receive timing and control, and alarm circuits. These circuits are described in subparagraphs a through j below.

a. Transmit Interface Circuitry (fig. FO-9). This circuitry consists of differential amplifier IC2B, resistors R1 through R5, XMT DATA IN jack J1, exclusive OR gate IC11B, and XMT DATA test point TP1. The 0 to 20 kb/s asynchronous data from the user terminal is applied to differential amplifier IC2B. Resistors R1 through R5 provide IC2B with a balanced input impedance of 135 ohms. XMT DATA IN test jack (J1) permits test data signals from BITE to be inserted in the 0-20 kb/s data channel. Exclusive OR gate IC11B permits the IC2B output to be monitored at XMT DATA test point TP1 while isolating the amplifier from test equipment loading.

b. 2-bit Transitional Encoder Circuitry. This circuitry consists of the following: flip-flops IC4A, IC4B, IC9A, IC9B. IC15A, and IC15B; exclusive OR gates IC11A and IC11C; AND gates IC7B, IC7C, and IC7D. Asynchronous data are applied to the two D inputs of IC4. The two halves of IC4 are clocked by opposite phases of the 56 kb/s clock with IC4-3 considered the early clock and IC4-11 considered the late clock. A transition of the asynchronous data is first reflected in the level on IC4-5 if it occurs prior to the rising edge of the early clock but later than the rising edge of the previous late clock cycle. If the asynchronous data transition occurs too late to be caught by the early clock, it is first reflected by a transition on IC4-9. Because the width of the asynchronous data bit is greater than one cycle of the 56 kb/s clock, the transition occurs on both IC4-5 and IC4-9.

(1) The two halves of IC4 feed exclusive OR gates, the other inputs of which are fed the same asynchronous data as the D inputs of IC4. An asynchronous data transition that has not yet been registered by IC4 produces a high on the exclusive OR outputs. Their logic states are latched into one half of IC9 and IC15 respectively, using the same early and late clocks as the two halves of IC4. This results in IC9-5 and IC15-5 both producing a high of a width equal to one 56 kb/s

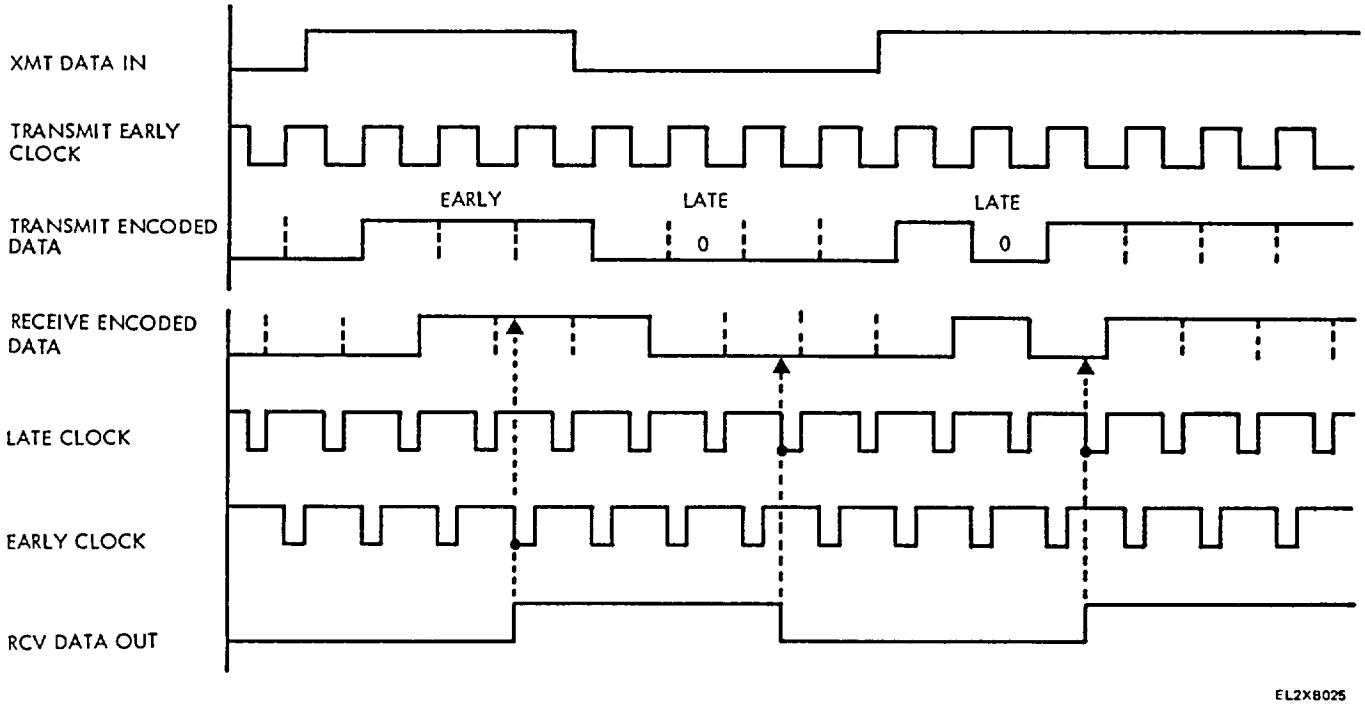


Figure 2-25. 2-bit transitional encoding and decoding.

clock period for every transition of the asynchronous data. If the transition was early, IC9-5 produces the high first, followed by IC15-5. If the transition was late the pulse on IC15-5 occurs before the pulse on IC9-5.

(2) Flip-flop IC15-5 is used as a clock for the second half of IC9. Data for the second half of IC9 comes from IC9-5. The late transition pulse is used to clock the early transition pulse into the second half of IC9. If the asynchronous transition is early, IC9-5 goes high because IC9-5 generates a high in advance of IC15-5. If the asynchronous transition is late, IC9-5 is still low when IC15-5 goes high, and a low is latched on IC9-9.

(3) The second half of IC15 retimes the late transition pulse to give it a one-bit delay with respect to IC9-9. Pins 8 and 9 of IC15 control the data select circuit formed by the three IC7 gates. The normal data path is from pin 12 to pin 6 of IC7. This produces a data stream on pin 6 of IC7, which is the asynchronous data retimed by the late 56 kb/s clock in the second half of IC4. When a transition occurs, it is reflected by a changed level of IC4-9 at the rising edge of the late clock. Simultaneously, IC15-5 goes high, causing IC9-9 to go high or low, depending upon whether the transition was early or late. The logic high on IC15-5 is transferred to IC15-9 by the next rising edge of the late clock. For one bit time of the 56 kb/s clock, the normal data path from IC7-12 to IC7-6 is maintained. For the next bit, IC15-8 and -9 switch polarity to establish the data path from IC7-9 to IC7-6. This lasts for one clock period only; then the normal path is restored. One data bit of changed polarity is gated through from pin 12 to IC7, followed by one bit of early/late information. The data path is then restored until the next transition.

c. Transmit Elastic Buffer Circuitry. This circuitry consists of serial-to-parallel converter IC36, 4-bit latches IC30 and IC37, and parallel-to-serial converter IC31. The early clock serial loads the 2-bit encoded data from IC7B into serial-to-parallel converter IC36 at a 56 kb/s rate. The 7-bit contents of the loaded IC36 are transferred in parallel to a 7-bit latch consisting of IC30 and IC37. This latch provides temporary storage for the 7 bits of data while the next 7 bits of data are being serially loaded into IC36. The 7 bits in the latch are transferred in parallel into IC31, which serially shifts this data to the bus driver at the MBS CLK rate. The serial shift by IC31 is permitted only when the transmit channel counter enables the channel in which the data module is located. Parallel to serial converter IC31 adds an

eighth dummy 1 bit to the 7 bits of data received from the latch to produce an overall transfer rate of 64 kb/s between the data module and the transmit data bus.

d. Bus Driver Circuitry. This circuitry consists of parallel-to-serial converter IC32, gates IC22C, IC14B, and IC14D, and inverter IC8. When the transmit channel counter reaches the channel (time slot) in which the 0-20 kb/s data module is located, the input to IC22C-8 goes low. If IC32 contains all 0s, the QH output is low, enabling IC22C to permit NAND-gate IC14D to transfer the 8-bit burst of data to the DTG at the MBS rate. At the same time, the input to IC14B-5 is high. This causes the XMT CNTRL bus to go low during the channel time of the data burst, provided IC32 contains all Os. The purpose of IC32 is to monitor the XMT CNTRL bus via inverter IC8 and load Os if this bus is already low at the time the channel counter attempts to enable transmission. If IC32 contains is, it disables gates IC14B and IC22C, thereby inhibiting the transmit data and control busses.

e. Transmit Timing and Control Circuitry. This circuitry consists of the following: counter IC40 and IC41; flip-flops IC35A, IC35B, IC29A, and IC29B; gates IC22A, IC22B, IC34C, and IC42C; and inverters SC3F, IC8F, IC3D, IC10E, and IC10C. These circuits control the encoding and data transfer from the transmit interface to the transmit data bus. The 4.096-MHz clock from the DTG is applied via inverter IC3F to a binary counter circuit (IC40 and IC41). This counter circuit divides the 4.096-MHz clock to produce a 224 kb/s output to IC35A. The 224-kb/s input is divided in half by IC3SA to produce a 112 kb/s output to IC35B. IC35B divides the 112 kb/s in half to produce the 56 kb/s early (IC35B-9) and late (IC35B-8) clocks for the 2-bit transitional encoder. Inverter IC8E applies the XMT MBS CLK from the DTG to the bus driver to shift out the data bursts at the MBS rate. The XMT MBS CLK is also applied to clock bus detection circuit IC13A in the alarm logic. The XMT CHN CNT signal is sent by inverters IC3SD and IC10E, defining the channel time for enabling the data and control busses. Flip-flops IC29A and IC29B, with associated gates IC22A, IC22B, and IC42C, synchronize the 56 kb/s early and late clocks with the transmit channel counter.

f. Receive Elastic Buffer Circuitry. This circuitry consists of serial-to-parallel converter IC24, 4-bit latches IC18 and IC25, and parallel-to-serial converter IC19. The 7-bit data burst at the receive channel time is clocked into serial-to-parallel converter IC24 at the MBS CLK rate. At the end of the receive channel time, the 7 bits of data in IC24 are transferred in parallel to 7-bit latch IC18 and IC25. This latch provides temporary storage for the 7 bits of data while the previous 7 bits of data are serially shifted out of IC19; flip-flops IC26A/B cause the 7 bits in the latch to be parallel-loaded into IC19 to the 2-bit transitional decoder at the 56 kb/s synchronous rate. Prior to receive channel time, parallel-to-serial converter IC20 is loaded with Os via inverter IC8A, since the RCV CNTRL BUS is normally high due to the low at gate IC14A-2. During the receive channel time, gate IC14A-2 goes high and the Os (inverted at IC20-7) are applied serially as eight Is at the MBS rate. This produces a low RCV CNTRL BUS signal for eight MBS clock periods. If the RCV CNTRL BUS signal is already low at the beginning of the receive channel time, inverter IC8A loads Is into IC20, inhibiting gate IC14A.

g. 2-Bit Transitional Decoder Circuitry. This circuitry consists of the following: flip-flops IC16A/B and IC23A/B; exclusive OR gate IC11D; gates IC17A/B/C and IC28A/B/D; and inverter IC10F. Early and late clocks are provided by IC34-3, and IC34-6, respectively. The late clock is applied to IC19, which is the output shift register in the receive data buffer. Encoded data is thus supplied in a steady 56 kb/s stream to IC11-12, IC10-13, IC17-3, and IC28-5. As long as there are no transitions in the data, IC11-13 has the same level as IC11-12, and IC11-11 is low, causing IC23-9 to remain in a logic zero state. The logic zero is reclocked in the other half of IC23, and IC23-5 also remains low. The first two sections of IC17 are enabled and pass the data polarity in an inverted form to IC16. IC16-5 and -6 therefore show the polarity of the input data, with pin 6 having true polarity.

(1) IC23-6 maintains a logic high, which disables the last two sections of IC17. Pins 11 and 12 of IC16 are both low, and pin 9 therefore remains in whatever state it was made to go to by the previous transition. Clock on IC16-13 is the early clock if data polarity is a logic high, the late clock if data polarity is a logic zero. Clock selection is made through three sections of IC28. Clock on IC23-13 and IC16-1 lags the early clock by one fourth of a clock period. Clock on IC23-1 lags the late clock by the same amount.

(2) The first of the encoded bits to show a polarity change causes the level on IC11-11 to go

to a logic high. This is latched as a logic high on IC23-9 one half into the bit duration. At the same time, the new data polarity is registered on IC16-5 and -6. The level on IC1111 then returns to a logic zero. At the end of the bit duration, the logic one on IC23-9 is transferred to IC23-5. IC16 -2 and -3 are made logic zero. which prevents IC16-5 and -6 from changing. On the other hand, pills I1 and 12 are allowed to assume high and low data polarity, respectively.

(3) During second bit, the early/late clock selection in IC28 provides an early clock to IC1613 if the second bit is a logic high. A late clock is selected if the second bit is a logic low. The transition in data polarity on IC16-9 occurs at a time that is early or late, depending on the polarity of the bit immediately following the first bit to show a changed polarity. The polarity of the data on IC16-9 reflects the polarity of the first bit to change.

(4) The level on IC11-11 is a logic high or a logic low, depending upon whether the second bit has different or the same polarity as the first bit to change. In either case, IC23-9 goes back to a logic low in the middle of the second bit. Nothing happens at this clock edge on pins 5 and 6 of JC16 pins 5 and 6 since pins 2 and 3 are held low.

(5) At the end of the second bit, the logic low on IC23-9 is transferred to IC23-5. This enables IC16-S and -6 to follow the data polarity once more, but IC16-11 and -12 are made low and TC16-9 remains in an unchanged state until the next data polarity causes the above sequence to be repeated.

h. Receive Interface Circuitry. This circuitry consists of NAND-gate IC42D, transistor Q1, exclusive OR gates IC6A and IC6B, and drivers IC1A and ICSA. The decoded 0-20 kb/s asynchronous data from IC16B is applied to NAND-gate IC42D. In the absence of a CGA, IC42D-13 is high. The asynchronous data is allowed to pass to the base of level shifter Q1, which applies it to exclusive OR gates IC6A/B. These gates provide positive and negative drive to a balanced pushpull amplifier (IC1A and IC5A). This amplifier provides 3-volt peak-to-peak NRZ asynchronous data to the near-end user over a 135-ohm impedance line. If a CGA occurs, NAND-gate IC42D will be disabled and the input to the base of Q1 will be held high. This produces an all is output to the near-end user to indicate the CGA condition.

i. Receive Timing and Control Circuitry. This circuitry consists of the following: counter IC38 and IC39; flip-flops IC33A, IC33B, IC27A, and IC27B; gates IC21C/D, and IC34D; and inverters IC10A, IC10B, IC3A and IC3C. These circuits control the decoding and data transfer from the receive data bus to the 135-ohm impedance output to the near-end user. The receive 4.096-MHz clock from the DTG is applied by inverter IC3A to binary counter IC38 and IC39. The counter divides the 4.096 MHz input to obtain a 224 kb/s output. This output is divided by IC33B to produce 56 kb/s early and late clocks. The RCV MBS CLK is applied by inverters IC8D and IC21A to the elastic buffer and clock loss detection flip-flop IC13B in the alarm logic. The RCV CHN CNT signal is sent via inverters IC3C and IC10B to define the receive channel time to the elastic buffer. IC27A/B, with associated gates IC21C, IC21D, and IC34D, synchronize the 56 kb/s receive clocks with the receive channel counter.

j. Alarm Circuitry. This circuitry consists of the following: flip-flops IC13A and IC13B; one-shot multivibrators IC12A and IC12B; gates IC7A and IC14C; and switch S1. IC12B is triggered by the toggle action of IC13A, which is caused by the presence of the XMT MBS CLK and the 56 kb/s transmit clock. IC12A is triggered by the toggle action of flip-flop IC13B, which is caused by the presence of the RCV MBS CLK and the 56 kb/s receive clock. As long as IC12-5 and -6 are held high and the input triggers are present, the one-shot outputs remain high (no alarm condition). Switch S1 can be used to test the alarm circuit by forcing IC12B pin 11 low, preventing the triggering of the one-shot. The output of IC12B goes low preventing the triggering of IC12A, the output of which also goes low. This low output illuminates the FAULT indicator and causes gates IC7A and IC14C to force the fault alarm bus low.

Section V. 50 KB/S DATA MODULE

2-13. General Information

The 50 kb/s asynchronous data module (fig. FO-10) is a full duplex data module that transmits data at 50 kb/s $\pm$250 parts per million (ppm). It uses pulse stuffing with a nominal stuff ratio of 0.5 to achieve the synchronizing function and

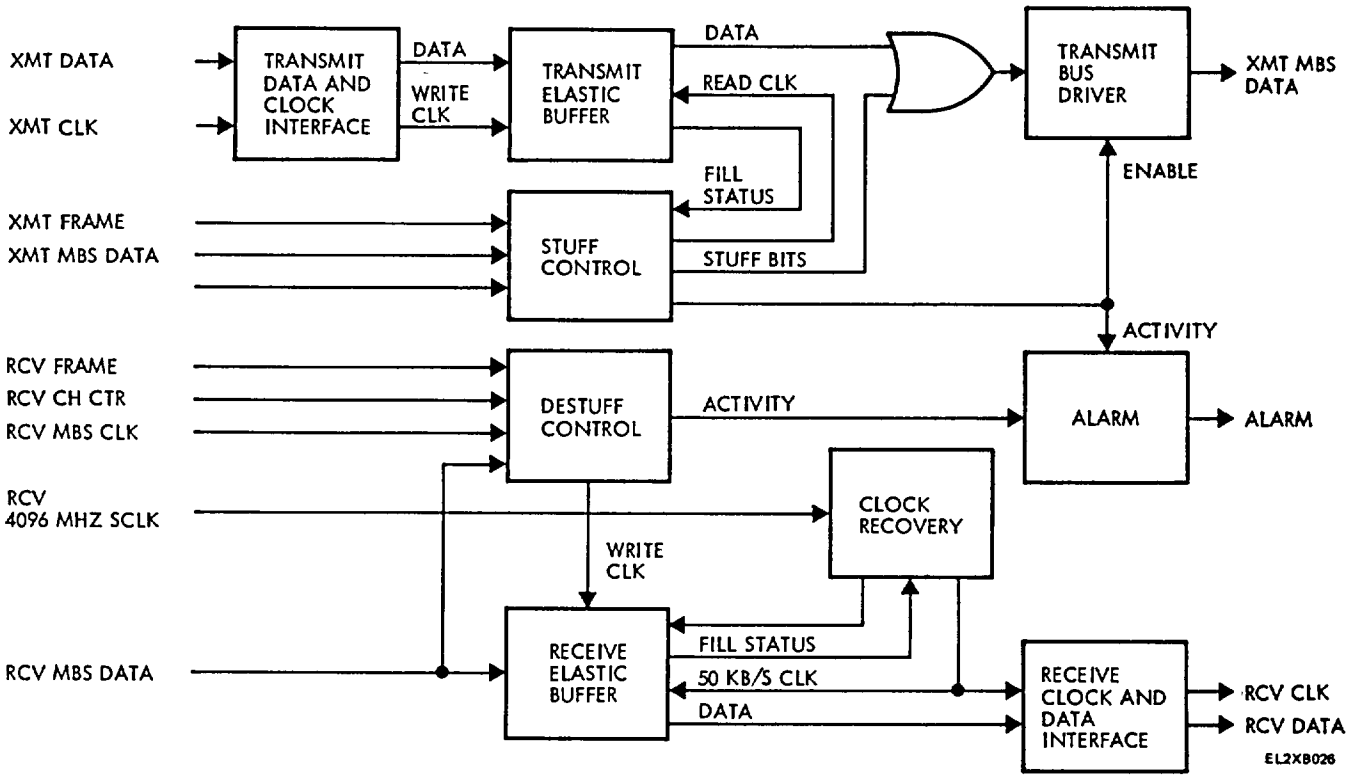


Figure 2-26. 50 kb/s asynchronous data module block diagram.

a narrow bandwidth phase-locked loop to restore the original clock rate on the receive side. The data module can be used with all configurations of the multiplexer set and replaces one VF module.

2-14. Major Functions

The 50 kb/s module block diagram is shown in figure 2-26. Transmitted data and clock are received and converted to logic levels by the transmit data and clock interface, which is strapped to accept the signals in 78-ohm balanced format. The signals are then sent to the transmit elastic buffer. From there, under control of the stuff circuit, it is read out in bursts of six or seven bits at the MBS rate. Additional bits are added to the stream by the stuff circuit so that the effective data transfer rate between the data module and the XMT MBS data bus is 64 kb/s. The major functions are described in subparagraphs a through g below.

a. Stuff Control. The stuff control circuit generates a frame format of the data stream, which permits the data module to operate in synchronization with the frame format of the multiplexer set. The frame format is as shown in table 2-1.

b. Destuff Control. The RCV data enters the data module in bursts of eight bits at the MBS rate. The data content is analyzed by the destuff control circuit in order to decide when the eighth bit of frame 5 contains a data bit and when it is a dummy bit that has to be removed from the bit stream. A four-of-seven majority voting technique is used in monitoring the C and C bits of frames 2, 3, 4 and 5 in order to prevent bit errors from inhibiting destuff circuit operation.

c. Receive Elastic Buffer. The destuff control circuit sends a WRITE CLK signal to the receive elastic buffer for all data bits that are part of the original 50 kb/s data stream. Only these data bits are loaded into the receive elastic buffer. Simultaneously, the clock recovery circuit sends a pulse to a second data track in the buffer and gives a 50 kb/s READ CLK to the buffer. This pulse appears on the output after a number of READ CLK pulses. The number of pulses indicates the fill status of the buffer. The average rate of data written into the buffer is 50 kb/s +250 ppm. If the READ CLK signal has the same speed, the average fill status of the buffer remains constant. No data is lost even though data is written in short bursts and is read at a slow, continuous rate.

d. Clock Recovery. To maintain the READ CLK at the same speed as the average of the WRITE CLK, the buffer fill status is used as a speed control signal. If the buffer tends to fill up more

Table 2-1. Frame Format 50 kb/s Asynchronous Data Module

FRAME	DATA BITS 1-6	BIT 7	BIT 8
1	DATA	1	DATA
2	DATA	C	C
3	DATA	C	C
4	DATA	C	C
5	DATA	C	DATA IF C = 1 1 IF C= 0
6	DATA	1	*0

* When strapped for 3, 6, or 12 channel operation with a 50 Kb/s module inserted in channels 1, 2, or 3, this bit is a multiplexer framing bit.

and more, the READ CLK is increased to bring it back to center as an average. If the buffer tends to deplete, the clock recovery circuit produces a slower READ CLK. Low-pass filtering is employed in this loop to reduce jitter and make its maximum slew rate 1 radian in 3200 bit times. The RCV 4096 KB/S CLK is used to recreate the 50 KB/S CLK in a circuit that combines digital and analog phase-locked loop techniques to achieve the required performance.

e. Data Transfer Rate. The data transfer rate between the 50 kb/s asynchronous data module and the MBS data buss is 65 kb/s. The additional bits inserted by the stuff control circuit and removed by the destuff control circuit must therefore have a bit rate of 14 kb/s plus and minus the 250 ppm tolerance of the 50 kb/s data rate. In other words, approximately 50 out of every 64 bits transferred to and from the MIBS data buss contain payload data. An additional such bit is occasionally inserted to accommodate the positive tolerance of the asynchronous input rate, and one is removed if the asynchronous rate falls in its negative tolerance margin.

f. Frame Format. The frame format shown in table 2-1 is used to achieve the desired addition of 14 kb/s of dummy bits. It repeats in intervals of six frames of the multiplexer frame format. The first six of the eight bits per frame always contain payload data. The eighth bit of the first frame also always contains payload, whereas the eighth bit of frame 5 contains payload data only about every other time. This frame format guarantees a logic 1 density of no less than two per sixteen bits. This is important for clock recovery purposes when the high speed data transmission link does not furnish a clock separate from the data.

g. Monitor and Alarm Function. The 50 kb/s asynchronous data module contains circuits that monitor the function of the module. If activity ceases in the transmit or receive portion of the module due to loss of the XMT CLK, RCV MBS CLK or failure of the stuff or destuff circuit, a FAULT indicator on the front panel is illuminated. At the same time the fault alarm bus is pulled to a logic 0. An all-1 data stream output to the near-end user is produced if the CGA bus is pulled to a logic 0 by the DTG. No failure indication is given by the data module as a result of this CGA condition.

2-15. Circuit Descriptions

The 50 kb/s data module consists of transmit data and clock interfaces, transmit elastic buffer and stuff control, transmit bus driver, receive elastic buffer and destuff control, clock recovery, receive clock and data interface, and alarm circuits. Each of these circuits is described in detail in subparagraphs a through g below.

a. Transmit Data and Clock Interface Circuit (fig. FO-10). This circuit consists of differential amplifiers IC15A and IC15B, switches S1 and S2, and associated components. Switches S1 and S2 permit selection of 50-ohm unbalanced or 78-ohm balanced impedance for the incoming XMT DATA and XMT CLK. For normal operation (78-ohm balanced), all S1 switches are closed and all S2 switches are open. The XMT DATA and XMT CLK jacks (J1-A and J1-B) permit insertion of BITE test signals into the data channel. The incoming XMT DATA and XMT CLK signals are applied to differential amplifiers IC15A and IC15B, which produce output levels compatible with the transistor-to-transistor logic circuits of the module.

b. Transmit Elastic Buffer and Stuff Control Circuit (fig. FO-10). This circuit consists of elastic buffer IC31, frame gate generator IC6, shift register IC24, gates IC3, IC13, IC29, IC30 and IC35, and flip-flops IC17 through IC20.

(1) The control circuits develop the sequential gates that identify the sequential frames 1 through 6 in system synchronization. They also generate the control bus gates for the data module during each of its time slots. These circuits generate a FAULT ALARM RESET pulse each frame, and generate gates that identify the seventh and eighth bit periods during each of the assigned channel time slots for the data module. The latter is for the purpose of making stuffing decisions. All the above control signals are developed

from inputs of MBS CLK, channel counter gate, and the system frame sync pulse. The XMT CH CTR gate applied to IC2C pin 5 is low during the data module assigned time slot. IC17A is clocked by forcing its output low. When not in its channel time slot, MBS CLK is applied to IC17-3. When the transmit control bus is high, the input to IC23B is low during its clocking period. This puts the input to shift register IC24-1 high, and when IC24-2 is also high, the shift register is enabled. For example, a multirate data module such as a 128 kb/s data module, preempts two time slots. If the preceding module to the 50 kb/s data module is a 128 kb/s data module in adjacent mode operation, its control bus driver holds the control bus low during the eighth bit of its first assigned time slot. This low state is converted to a high by IC2A and applied as the input to IC17A. In this case the IC17 pin 3 just preceding the channel counter gate to the module, causes the Q output of IC17A to transition to a high and its Q output to transition to a low, which disables IC13C and IC24. This inhibits the generation of frame gates, and bit 7 and 8 gates and also prevents IC3D from providing a low to the control bus.

(2) Under normal operation, when the transmit control bus is not busy during the assigned time slot, a gated clock essentially in phase with the MBS CLK, is generated by IC13D. This clock is inverted by IC35B to provide the bit clock for shift register IC24 and flip-flop IC17B. Since IC13C produces high during this gate period, IC17B then provides a positive leading edge to clock IC6. This occurs once per assigned time slot (once per frame), producing the sequential frame gates (1 through 6) generated by the six serially coupled D-type flip-flops of IC6.

(3) The desired frame format for the transmission of 50 kb/s data on the MBS is shown in table 2-1. IC31 is a 16 X 4 bit FIFO shift register. The 50 kb/s data is applied to the input pin D2 and clocked in by the complement of its accompanying 50 kb/s clock at the parallel load (PL) pin. During the leading edge of each clock pulse, the data enters the D2 register cell. This causes the input-register-full (IRF) terminal to go low, and causes the data bit to be output at Q2. As soon as the data bit leaves D2, the IRF output returns to high and the input is ready to receive another clocked bit.

(4) When the channel counter gate for the data module occurs, the bus grant line goes high, applying eight gated XMT MBS CLKs to IC35C. The complement of the XMT MBS CLK is continually applied to the clock input of flip-flop IC18A, providing for eight bits of outputs from the FIFO. Since there are 8,000 frames per second and 8 bits per frame from a given module, the circuitry generates 64 kb/s with 50 kb/s of input. The gated XMT MBS CLKs are applied to FIFO IC31 for the first six bits during each bus grant time slot. This yields only 48 kb/s; however, the seventh bit is a control code, the eighth bit of the first frame is always data, and the eighth bit of the fifth frame is data only when the control code allows, which provides exactly 50,000 data bits plus 14,000 control code bits. To achieve this control, the DO input of the FIFO receives a high level during frame 1 of each six frame group. If the FIFO is near depletion, the QO output will be high at the same time the DO input is high, causing IC30B to output a low which latches IC30C and holds the output from IC30B low. During the bit 7 period, a high is applied to IC2913. During the bit 8 period, a high is applied to IC29-12, IC29-2, IC25-2, IC25-9, IC25-12, and IC25-13. During the bit 7 and 8 periods, IC29-11 provides a high to IC35-1 and, with the exception of frame 1, bit 8, and frame 5, bit 8, IC25-8 provides a high to IC35-2. This causes its output to go low, which inhibits passage of the gated clock through IC35C.

c. Transmit Bus Driver (fig. FO-10). This circuit consists of NAND-IC3C and IC3D, and inverter IC2A. If the transmit control bus is low at the time the data module is enabled by transmit channel counter, inverter IC2A applies a low to flip-flop IC17A, which prevents the BUS GRANT signal from being generated. Normally, the transmit control bus is high at this time and the transmit channel counter gate enables IC13C to produce the BUS GRANT signal. This signal permits IC3C to transfer 64 kb/s of data (includes stuff bits) to the DTG at the MBS rate during the channel time slot of the module. At the same time, the BUS GRANT signal causes IC3D to force the transmit control bus to a low condition. The transmit control bus will be low for seven bit periods, then at bit 8, both inputs to exclusive OR gate IC29C are high and IC3D is inhibited.

d. Receive Buffer and Destuff Control Circuit (fig. FO-10). This circuit consists of FIFO buffer IC7, frame gate generator IC5, shift register IC22, counter IC34, gates IC3, IC4, IC12, IC27, IC28, and IC33, and flip-flops IC14, IC18, IC23, and IC36. The RCV FRAME, RCV CH CTR, and RCV MBS CLK signals are used to produce the frame and bit signals that control the destuff

operation. The bit 7 and bit 8 signals are generated by shift register IC22, and the frame 1 and 5 signals are produced by IC5 in the same manner as previously described for the transmit control circuit.

(1) The incoming receive data, inverted by IC4B, is loaded into buffer IC7 by the WRITE CLK. No WRITE CLKs are generated for the dummy bits; consequently, they are eliminated. The data bits are shifted out of FIFO buffer IC7 by the recovered 50 KB/S CLK. The operation of buffer IC7 is basically the same as that described for buffer IC31 in the transmit circuit.

(2) The destuff control circuit generates WRITE CLKs for incoming bits that contain data and inhibits WRITE CLK generation for dummy bits. When frame 1 occurs, exclusive OR gate IC27C produces a low during bits 1 through 6 (bit 7 or 8 not present) and IC33A generates a high data slot signal. The high data slot signal enables gate IC33C to pass the RCV MBS CLK as the write clock to load bits 1 through 6 into buffer IC7. At bit 7, IC27C produces a high and the WRITE CLK is inhibited. At bit 8 of frame 1, both IC28-6 and IC28-8 go low to reset counter IC34 and force the data slot signal high (enable WRITE CLK). Counter IC34 is permitted to count RCV MBS CLKs only when pins 7 and 10 are both high. IC34-10 is high during the no data periods of bit 7 and 8 of frames 2 through 5 (fig. 2-4). IC34-7 is high or low depending on the coding of bits 7 and 8 of frames 1 through 5. If this coding indicates bit 8 of frame 5 contains data, then IC34-7 will be high, permitting the counter to be advanced by the RCV MBS CLK. This is accomplished by exclusive OR gate IC27D, which produces a high output when incoming data (at pin 12B) bit 7 is high or bit 8 is low. When hit 8 of frame 5 contains data, counter IC34 advances during bits 7 and 8 in frames 2, 3, and 4, and in bit 7 of frame 5. This produces a high output at IC34-12 (Q2), and a WRITE CLK is generated for bit 8 of frame 5. It should be noted that Q2 of IC34 will be high if any four of the seven counts are detected. This prevents a few isolated bit errors from inhibiting destuff operations. When bit 8 of frame 5 does not contain data, incoming data (at pin 12B) bit 7 is low and bit 8 is high. Then, counter IC34 does not advance and generation of a WRITE CLK for bit 8 of frame 5 is inhibited.

e. Clock Recovery Circuit (fig. FO-10). This circuit consists of voltage controlled oscillator IC26; low-pass filter amplifier IC21; counters IC37A and IC37B; exclusive OR gates IC38A, IC38B, IC38C, and IC38D; and flip-flops IC14A, IC23B, IC32B, and IC36A. A smooth, continuous 50 kb/s data rate is restored by the action of the clock recovery circuit. The payload data, extracted from the RCV DATA signal by the WRITE CLK and furnished by the destuff .control circuit, is written into FIFO buffer IC7. On another IC7 data track, a low pulse present during frame 1 is written in by the same clock. During bit 8 of frame 1 a reset pulse is generated and sent to RS flip-flop IC14A. Data and the FRAME 1 pulse are read out of the buffer by the steady 50 kb/s clock. Depending on the fill status of the buffer, they appear on the outputs for a shorter or longer amount of time after they were written into the buffer by the bursts of fast WRITE CLKs. The low FRAME 1 pulse sets the RS flipflop. The flip-flop output, therefore, is a pulsewidth-modulated measurement of the buffer fill status. Low-pass filtering of this signal produces a dc level input to amplifier IC21 that is proportional to the fill status. The de level output of IC21 controls the frequency of voltage-controlled oscillator IC26. The oscillator output is reclocked by flip-flops IC32A and IC32B with a delay such that the edge of the signal occurs with a 90-phase shift with respect to the 4096 KB/S CLK. These two signals are applied to exclusive OR gate IC38C. The output of the gate is a 4096 KB/S CLK whenever the retimed 4 kb/s clock remains in a fixed logic state. However, for every transition of this signal, a half period of the 4096 KB/S CLK is transformed into a full cycle of 8192 KB/S CLK. As a consequence, the clock on the output of gate 1C38C has a rate that is exactly the sum of the rate of the two inputs. This sum varies from the nominal 4100 kb/s over a +1.23 kb/s range as controlled by the fill status of buffer TC7. The clock drives a ÷41 counter made up by a 7 bit counter (IC37A and IC37B) and a D flip-flop (IC36A). These generate a reset to the counter when it reaches count 40. The ÷41 output is divided by two by toggling flip-flop IC23A to achieve symmetry of the waveform. Since the input clock to the counter has a 4100 kb/s rate, the output rate is this rate divided by 82, or 50 kb/s.

f. Receive Clock and Data Interface Circuit (fig. FO-10). This circuit consists of level shifters IC20A and IC20D; exclusive OR gates TIC16A, IC16B, IC16C, and IC16D; drivers ICSA, IC9A, IC10A, and IC11A; and switches S1 and S2. Two differential driver circuits are provided. one for the 50 kb 's output of the clock recovery

circuit and the other for the data output from buffer IC7. Since these circuits function identically only the data channel is described. The 50 kb/s asynchronous data from buffer QO of IC7 is applied to level shifter IC20A through IC14 and IC4. The output of IC20A drives exclusive OR gates IC16A and IC16B, which serve as phase splitters. The exclusive OR gate outputs are connected to push-pull line drivers IC9A and IC11A, which provide the required drive for the transmission line. Switches S1 and S2 permit selection of a 50-ohm unbalanced or 78-ohm balanced transmission line. For normal operation (78-ohm balanced) all S1 switches are closed and all S2 switches are open.

g. Alarm Circuit (fig. FO-10). This circuit consists of flip-flop IC19B; drivers IC15C and IC15D; gates IC3B and IC4C; switch S3, and fault indicator DS1. Flip-flop IC14B is used to monitor the activity of the transmit and receive circuits. If activity in either of these circuits ceases due to failure of the MBS clock, channel counter, or control circuits, a fail signal is applied to drivers IC15C and IC15D. Upon receipt of the fail signal, IC15D produces a high output to IC3B, which forces the alarm bus to a low condition. At the same time, the output of driver IC15C goes low, causing fault indicator DS1 to illuminate. Receipt of a CGA signal disables gate IC4C, thereby producing an all-is data output to the near-end user.

Section VI. MULTIRATE SYNCHRONOUS DATA MODULE

2-16. General Information

The multirate synchronous data module (fig. FO-11) is a full duplex data module that can be strapped by switches on the module to handle 56, 64, 128, 256 or 512 kb/s data rates. When configured for either 56 or 64 kb/s data rates, the data module replaces one voice channel module. In the higher rate configurations (i.e., 128, 256 or 512 kb/s), the data module electrically replaces two, four and eight voice channel modules, respectively. At the higher rates, the data module can be configured to replace either adjacent or alternate voice channel modules. For example, if strapped for 256 kb/s and plugged into the physical space for channel 3, the data module can replace either channels 3, 4, 5, and 6 or 3, 5, 7, and 9. Further strap selection allows the data module to use either the clock, which may be furnished with the incoming transmit data, or to run by an internally generated clock that is automatically adjusted in phase to the incoming data stream.

2-17. Major Functions

The block diagram for the multirate module is shown in figure 2-27. The major functions are described in subparagraphs a through d below.

a. Data and Clock Input. The XMT DATA and XMT CLK signals are received on balanced 78 ohm lines by the transmit interface and converted to the required logic levels. The DATA signal is applied directly to the transmit elastic buffer. A synchronous WRITE CLK is also applied to the buffer by the clock select circuit. This clock car be either the XMT CLK from the transmit interface or one generated by the transmit clock generator. The transmit clock generator produces two synchronous clock signals. One clock signal is controlled in phase by the XMT DATA and applied to the clock select circuit. The second clock signal has the same rate as the first but with a phase which is independent of the XMT DATA. This second clock is sent to the transmit clock output interface. It is then converted to a 78-ohm balanced format for use by external equipment.

b. Timing. Data is transferred from the transmit elastic buffer in bursts at the MBS rate. The data is shifted out of the buffer by a READ CLK provided by the transmit timing circuit. The circuit generates the READ CLK bursts of a length and format determined by the strapping switches. The total number of MBS clock pulses per frame is the selected IBS data rate divided by 8000. The transmit timing circuit also enables the data bus driver at the corresponding channel slot times to read data from the buffer onto the XMT MBS DATA bus.

c. Data Buffering. The receive MBS DATA is loaded into the receive elastic buffer by clock bursts generated by the receive timing circuit. These bursts are at the MBS rate and the same length and format as those generated by the transmit timing circuit. Due to the action of the RCV CHAN CTR pulses. the clock bursts from the receive timing circuit are timed to sample only the MBS data bits belonging to the channel slot in which the module is located. The data thus entered into the receive elastic buffer is read out by a clock generated by the receive clock generator. The rate is controlled by the strapping switches to

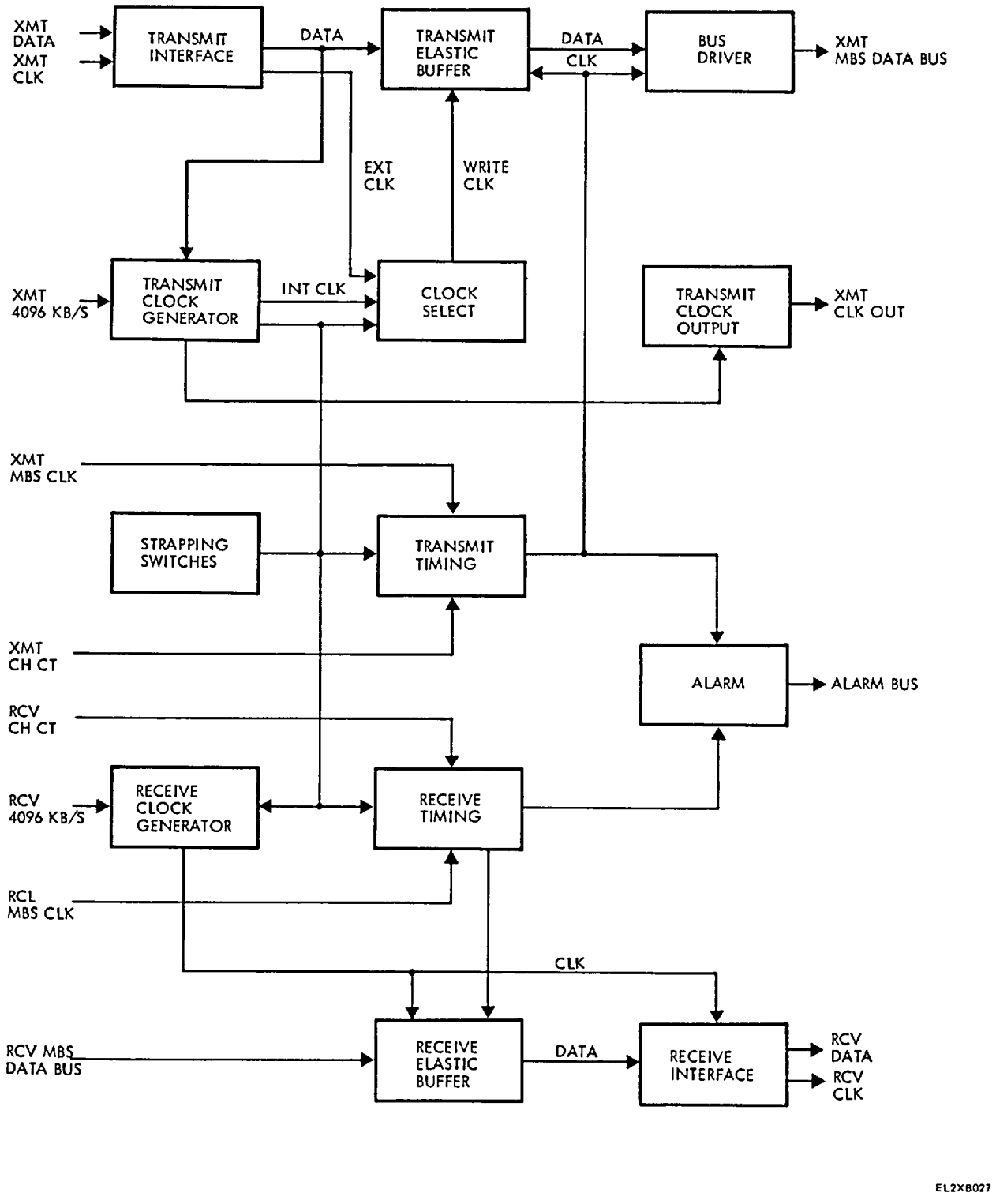


Figure 2-27. Multirate synchronous date module block diagram.

agree with the rate of the transmit clock generator and the length and format of the above-mentioned clock bursts, such that the average rate for all is the same. The elastic buffers are

therefore able to function without under- or overflowing. They are automatically centered at application of power.

d. Outputs. The buffer READ CLK and the output data are applied to the receive interface, where they are converted to 78-ohm balanced format. The multirate synchronous data module contains detectors that monitor the activity of both the transmit and receive portions of the unit. A loss of activity due to the failure of a monitored circuit causes the FAULT indicator on the front panel to illuminate and the alarm bus to be pulled to a logic 0. An all-1s receive data stream is generated if the CGA bus is pulled to a logic 0. This does not trigger the module failure detectors.

2-18. Circuit Descriptions

The multirate synchronous data module consists of interface, elastic buffer, timing, clock generator, mastor reset, and alarm circuits for both transmit and receive functions. Each of these circuits is described in subparagraphs *a* through *f* below. When the transmit and receive functions of the circuit are identical, only one function is described.

a. Transmit and Receive Interface Circuits (fig. FO-11). These identical circuits use balanced differential receivers and drivers. A typical balanced differential receiver (IC47A) is provided for the XMT DATA IN signal. The XMT DATA IN circuit presents an approximately 78 ohms load to the transmission line. The signal is applied to differential line receiver IC47A, which is a current-sensing device capable of responding to input signals from +0.2 Vdc to +6.0 Vdc and presenting a TTL-compatible signal at its output. A typical balanced differential driver is provided for the XMT CLK OUT signal. This circuit comprises IC17D, IC16A and IC16B, IC4 and IC10. The TTL input signal is applied to the base of N-P-N transistor IC17D, which provides the level shift of the signal necessary for the phase-splitting action of exclusive OR gates IC16A and IC16B. The output of these gates is integrated sufficiently to eliminate excessive overshoots and undershoots and is applied to pushpull line drivers IC4 and IC10. These line drivers provide a 78-ohm balanced output drive for the transmission line.

b. Elastic Buffers (fig. FO-11). In each multirate synchronous data module, there is a transmit and a receive elastic buffer. The transmit elastic buffer (IC29 and IC30) receives data at the selected rate, but is required to transmit the data in 8-bit bursts at the MBS rate. The receive elastic buffer (IC33 and IC34) must acquire data from the MBS in eight-bit bursts during its preempting channel slot times and output the data at its steady selected bit rate. Since the operation of both elastic buffers is similar, only the transmit circuit is described. The elastic storage for the transmit data is provided by two FIFO shift registers (IC29 and IC30). Serial data is presented at the DS input of IC30, the serial-to-parallel converter. When four bits have been serially clocked in by CPS1, the XMT INPUT REGISTER FULL (XMT IRF) transitions to a logic low, which is applied to TRANSFER-TOSTACK (TTS). When TTS goes low, the data ripples through the 16-word stack until it is full, thus stacking 4-bit words in this register. When a word arrives at the bottom register of the stack, the OUTPUT REGISTER EMPTY (ORE) transitions to a logic high. This disables the TRANSFER OUT SERIAL (TOS) of IC30 and enables the PARALLEL LOAD (PL) control of IC29, the parallel-to-serial converter. This loading occurs if TRANSFER OUT PARALLEL (TOP) is high, enabling the parallel output of IC30. As long as IC29 is not full, its IRF output is high, assuring that TOP of IC30 is high. As soon as the parallel word is transferred into the input register of the IC29 stack, its IRF goes low. This forces TTS low and initiates the ripple-through of parallel data in the IC29 stack. The IRFs go high immediately after the word leaves the input register of the stack. IC37 is a ÷16 counter which, upon the 15th empty-to-full transition of IRF, outputs a carry high. The carry high is inverted by IC36F and applied to the P input of IC37, inhibiting any further clocking. This low is applied to the SERIAL OUTPUT ENABLE (SOE), permitting the serial clocking of data. The purpose of the 16 counter is to fill the register stack of IC29 after power up (or a master reset) before starting serial transmission of the acquired data. Since the elastic buffer is half full at this time, the elasticity accommodates variations in neither the CPS1 clock of IC30 or the CPSO clock of IC29. To accommodate stack transition times, the output data at Q(S) of IC29 is presented to flip-flop IC14B where it is clocked by a phase-delayed CPSO clock and further gated by IC1C to the XMT CONTROL BUS out.

c. Transmit and Receive Timing Circuits (fig. FO-11). The transmit timing circuit generates the READ CLK for the parallel-to-serial converter of the elastic buffer. The receive timing circuit generates the WRITE CLK for the serial-to-parallel

converter of the receive elastic buffer. The waveshapes associated with both timing circuits are shown in figure 2-28. Since the transmit and receive timing circuits are identical, only transmit timing is described. This description is explained with the aid of two possible strapping options: the 128 kb/s occupying adjacent channels and the 128 kb/s occupying alternate channels. The generation of a burst sequence of clocks is always initiated with the falling edge of the XMT CHAN CTR. This edge triggers the IC15B flip-flop to the complement of the control bus state, making 0 go high and forcing the control bus low by the action of open collector gate IC1B. Since the strapping option has selected adjacent channel preempting, the output of IC7B always remains high, enabling IC1B and IC7A. Note that there is a one-clock delay before the output of IC15A reflects the new status of the control bus. Thus, IC38A enables IC8A for one clock period and allows it to generate a negative pulse one half clock period wide, which presets IC41 to its strapping option count of 10. Prior to the XMT CHAN CTR, the preset of IC21 was held at a binary count of 14. Thus, a single clocking of this counter generates a set pulse for IC15B and terminates the clock burst until the next XMT CHAN CTR pulse. Note that the first of the burst pulse occurs synchronously with the preset pulse for IC41, and that the count to 11 does not occur until the second burst pulse is initiated. The counter must count from 10 through 15 to 0 and up to 8 to develop the leading edge trigger for IC21. The following clock then disables IC7C, terminating the clock burst. The result is a burst of 16 consecutive clock pulses for the adjacent strapping option of 1C7-8 waveshape. The fifteenth successive clocking pulse causes a termination of the control bus gate pulse. This allows a succeeding channel one bit period to define that the upcoming channel time slot is available for its use. When the strapping option is changed to 128 kb/s alternate-channel operation, IC41 is present to a 2 count and IC21 is loaded to a 13 count. The alternate strapping enables IC7B, permitting it to disable IC7A during the IC41 count of 8 through 15 (Q D outputs a logic 1). The burst clock output gate IC7C is enabled for 8 clocks during the XMT CHAN CTR lower period by IC38A. During the 8 through 15 count of IC41, both IC38A and IC38C are disabled. This disables IC7C, inhibiting any burst clock pulses. At the count of 8 at IC41, IC21 is clocked to a count of 14. At the counts of 0 through 7 at IC41. IC38C enables IC7C to output a burst of clock pulses. At the count of 8 at IC41, IC21 is clocked for the second time to a count of 15. This generates the set pulse applied to IC15B and terminates the burst sequence.

d. Receive and Transmit Clock Generators (fig. FO-11). In the synchronous data mode of operation, the received and transmitted data to and from user terminals are accompanied by a synchronous clock. In the internal clock mode, this clock originates from the sending user. In the external clock mode, the multirate data module generates the clock and transmits it to the user, where transmitted data is synchronized to this clock. Either the XMT CLK IN, presented to IC48-1, or the clock derived from the XMT 4.096 MHZ bus presented to IC48-9 is employed, depending upon the position of switch 2-7. If switch 2-7 is open, the XMT CLK IN from the user terminal is selected and furnished as an output by IC48-. If switch 2-7 is closed, the derived clock (internal clock) is selected and furnished as an output by IC48-8. The functioning of the internal clock requires definition. The strapping options set up the divisor for IC27 and its counterpart, IC26, in the receive circuit. IC26 and IC27 are rate multipliers. Their Z output will be eight times the clock rate for the user data stream. For all rates except 56 kb/s, the strapping option causes IC46 to select its A inputs as the source for its Y outputs. IC46-9 presents a clock that is eight times the data rate to IC49 (a ÷8 counter) and IC50, which is an 8-bit P/O shift register. The Q(C) output of IC49 is the 4-bit output that cycles once per 8 clock inputs. IC5C presents four sequential samples, plus four sequential complementary samples, of the incoming data bit to IC43. These two devices act as a data transition detector, which presets IC49 to a four count and yields a synchronized XMT CLK IN from IC48-8. IC42 divides the IC27 clock by eight and presents it to IC46-2A for output by its 2Y terminal as the XMT CLK OUT input to the balanced driver output circuit. When the 56 kb/s is selected, IC46 selects the B inputs as sources for its Y outputs. IC27 and IC42 are then employed as serial dividers to furnish the three Y outputs of IC46.

e. Master Reset Circuit (fig. FO-11). The MASTER RESET signal at the output of IC40B is generated by a circuit consisting basically of gates IC8B, IC32D, and IC48A, and flip-flops IC14A, IC23A, and IC23B. As long as IC23A and IC23B remain in their set position, no MASTER RESET signal can be generated, since the input to IC14A is low. If either or both IC23A and IC23B are reset, IC8B presents a high input to

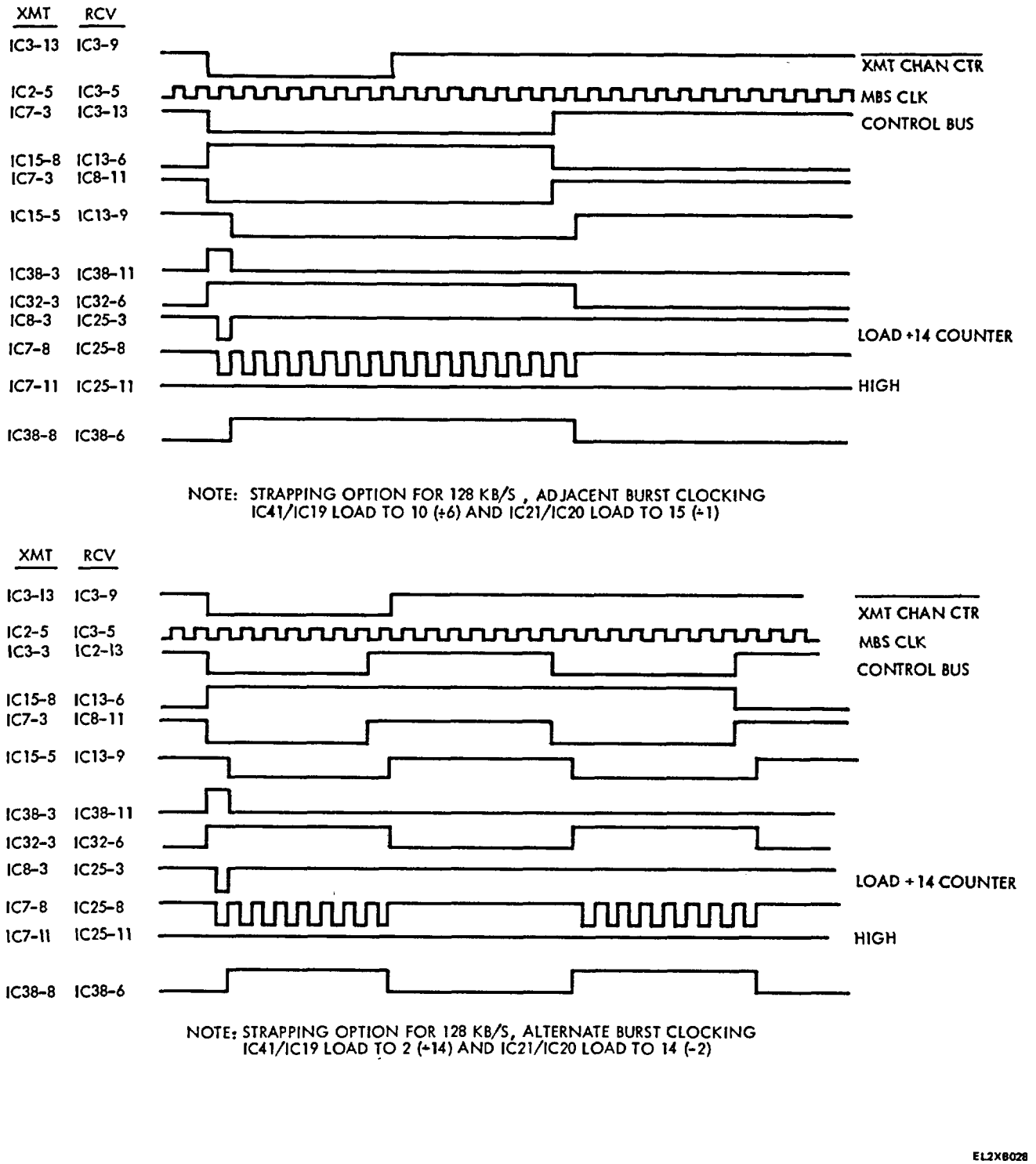


Figure 2-28. Multirate synchronous data module timing diagram.

IC14A. This sets IC8B, causing a master reset state to reset both elastic buffers and their load counters. IC23B is set during the initial loading period of the transmit elastic buffer by the carry

output of loading counter IC37. The IC23B-13 input originates from transmit output elastic buffer IC29 control OUTPUT REGISTER EMPTY (ORE). Whenever the output clock and ORE get out of synchronization; i.e., when the output FIFO is completely empty, IC23B resets causing a master reset output. IC23A is set by the 0 output of IC14A when IC23A or IC23B is in the reset condition. IC23A can be reset by clocking an out-of-synchronization k state or by presentating a low to its reset input. IC48A generates a low output if the serial input clock (CPSI) gets out of synchronization with its INPUT REGISTER FULL control and/or the serial output clock (CPSO) gets out of synchronization with its OUTPUT REGISTER EMPTY control. Rapid response to these out-of-synchronization control states is assured by application of the 4.096 MHz clock to IC14A, providing a worst case master reset response within approximately 250 nanoseconds.

f. Alarm Circuits (fig. FO-11). The fault alarm monitoring circuits use IC39B and IC39A to monitor clocking activity in the transmit and receive elastic buffers, respectively. The transmit serial input clock sets flip-flop IC395, and the burst serial clock out gate resets it. The receive serial clock out sets flip-flop IC34A, and the burst serial clock in gate resets it. The Q outputs of the two flip-flops trigger retriggerable one-shots IC45A and IC45B. The time constants of the one-shots exceed the period of triggering when clocking activity is normal. Thus, the Q outputs of these one-shots remain high and the frontpanel mounted FAULT light is extinguished. The Q output of IC45B will be a low, which is inverted by ICI-D and IC2-E to provide a high to the FAULT ALARM bus and IC14-10 set lead. If clock or reset activity ceases at the input to either IC39A or IC39B, they fail to retrigger the retriggerable one-shots. One-shot IC45B automatically resets itself by failure to retrigger. It also resets if IC45A is not retriggered before it resets by presenting a reset pulse from its Q output to the reset pin of IC45B. FAULT test switch S3 mounted on the front panel disables the triggering of IC45A when depressed. This will cause the FAULT light to illuminate and a low to appear on the FAULT ALARM BUS.

Section VII. BITE MODULE

2-19. General Information

The BITE module (fig. FO-12), in conjunction with the monitor and alarm circuits of the PWR SPLY unit, provides a built-in capability for monitoring system operation, isolating malfunctions, aligning modules and verifying operation of replacement modules. The BITE module is utilized for VF channel gain alignment, E and M lead testing, data channel bit error assessment, synchronous data channel phase adjustment, dc supply voltage measurement, and self-test.

2-20. Major Functions

BITE module circuits are divided functionally into two major sections, analog and digital. They are described in subparagraphs a and b below.

a. Analog Section. This section (fig. 2-29) is used for aligning VF channels of the multiplexer set and for measuring the power supply output voltages. It contains an audio frequency test oscillator, switch-controlled attenuator pads with associated amplification stages, a dc voltage selector, ac and dc metering circuits, a front-panel meter, a self-test circuit, and an E and M signaling test circuit.

(1) The test oscillator produces a 0 dBm, 1020 sine wave audio signal for use in test, alignment, and troubleshooting of VF channels. The oscillator test signal can be applied to the XMT, transmit and receive LINE-UP jacks on the VF modules by means of a patch cable.

(2) Switch-controlled attenuator pads internally connect the 0 dBm oscillator output to the VF OSC jack on BITE. Attenuators are switched in between the oscillator output and the VF OSC jack to provide required test signal levels. The VF FUNCTION and OSC LEV switches on the front panel are used to control the level of the output at the VF OSC jack. When the VF FUNCTION switch is set to CHAN LEV XMT or LOOP TEST position, the outputs are controlled by the OSC LEV toggle switch, which can be used to select either 0 dBm or -16 dBm oscillator levels. If the VF FUNCTION switch is set to either SELF TEST or CHAN LEV RCV, a 20 dBm signal is placed in series with the oscillator output to provide a -20 dBm signal for BITE self test, or for patching into the VF module receive LINE-UP jack when adjusting channel level receive. A 10 dBm attenuator is switched in series with the oscillator output if the VF FUNCTION

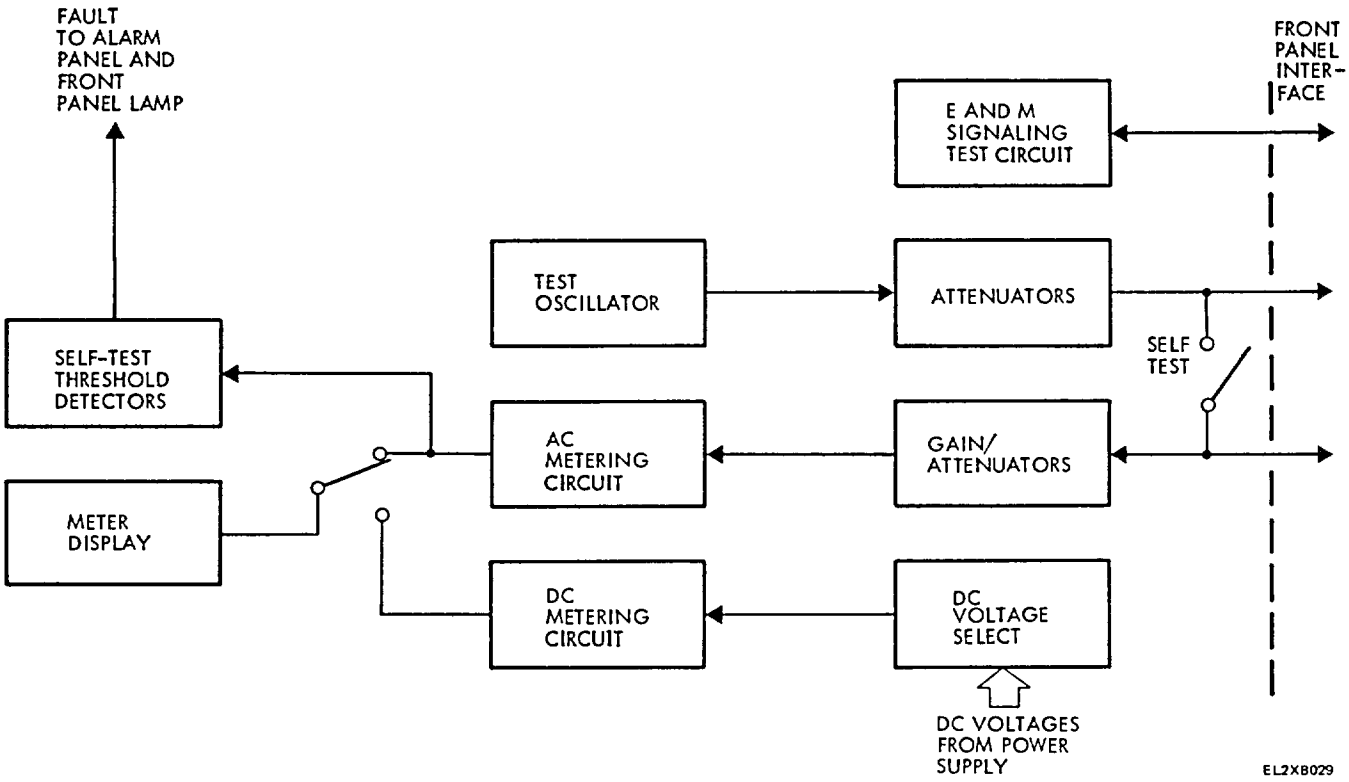


Figure 2-29. BITE analog section block diagram.

switch is set to COM GAIN XMT position. This produces a -10 dBm test signal output at the VF OSC jack, which can be patched into the VF module transmit LINE-UP jack for gain alignment.

(3) Signals of various levels are patched into the BITE meter (VF METER jack) during alignment and testing. Amplification and attenuation controlled by front-panel switches, are used to condition input signals so that the BITE meter will indicate 0 dBm when alignment is correct. Since the meter's full-scale indication is +2 dB, the METER ATTEN switch must be set to 10 dB to measure RCV jack outputs (-3 dB meter indication) of a VF module strapped to produce +7 dBm. The relationships between control settings and the various test signals produced and measured by the BITE analog circuits is shown in table 2-2. Gain or attenuation required to condition test signals for measurement can be determined by comparison of the VF METER jack input level with the meter indication listed in table 2-2. The VF METER jack 10 dBm and -20 dBm inputs require amplification to 0 dBm at the meter; the +7 dBm input requires 10 dB attenuation to bring the meter within scale.

(4) The BITE meter measures dc voltages selected by the DC SUPPLY SELECT rotary switch on the front panel. This switch is enabled only when the VF FUNCTION switch is set to DCV. The supply voltages that can be selected for measurement are -42, -38, -12, -7, -5, +7, +12, and -48 Vdc. The dc metering circuit connects the supply voltage selected for measurement to the meter and provides the proper meter scaling. When -48, -42, and -38 are selected, the metering circuit sets the meter to a scale having a maximum reading of 75 volts. For all other selected voltages, the meter scale is set to a 15 volts maximum reading.

(5) The ac metering circuit provides what is essentially full-wave rectification and filtration of the input VF test signals to produce an equivalent dc voltage for measurement. The de voltage output of the ac metering circuit is equal to the average value of the input ac (VF) signal and the BITE meter is scaled to indicate this value in decibels.

(6) The front panel meter has a 0 to 100 microampere movement. All dc voltages (VF signal levels) are presented on a scale of -15 dB to +2 dB. Use of the 10 DB position of the METER ATTEN switch extends the full scale reading to an equivalent +12 dB. The de voltages measured can be of positive or negative polarity and are

Table 2-2. BITE VF Test Signal Relations

VF module strapping	BITE switch settings	BITE VF OSC jack output	BITE VF METER jack input	BITE meter indication
0 dmB trunk input level	VF FUNCTION to CHAN LEV XMT and OSC LEV to 0 DBM	0 dBm	-10 dBm	0 dBm
-16 dBm trunk input level	VF FUNCTION to CHAN LEV XMT and OSC LEV to -16 DBM	-16 dBm	-10 dBm	0 dBm
0 dBm trunk output level	VF FUNCTION to CHAN LEV RCV and METER ATTEN to 0 DB	-20 dBm	0 dBm	0 dBm
+7 dBm trunk output level	VF FUNCTION to CHAN LEV RCV and METER ATTEN to 10 DB	-20 dBm	+7 dBm	-3 dBm
Not applicable	VF FUNCTION to COM GAIN XMT	-10 dBm	-20 dBm	0 dBm
Not applicable	VF FUNCTION to COM GAIN RCV	------	-20 dBm	0 dBm
0 dBm trunk input and output level	VF FUNCTION to LOOP TEST METER ATTEN to 0 DB and OSC LEV to 0 DBM	0 dBm	0 dBm	0 dBm
-16 dBm trunk input and +7 dBm trunk output	VF FUNCTION to LOOP TEST METER ATTEN to 10 DB and OSC LEV to -16 DBM	-16 dBm	+7 dBm	-3 dBm

presented on two scales; 0 to 15 Vdc or 0 to 75 Vdc.

(7) A self-test circuit is used to check the oscillator, attenuators, amplification, ac metering, and meter circuits for proper operation. The SELF TEST position of the VF FUNCTION switch connects the 0 dB oscillator output, attenuated by 20 dB, to the input signal amplification stage. An ac metering circuit provides full-wave rectification of the self-test oscillator signal and applies a dc voltage equivalent to 0 dB to the frontpanel meter and to threshold detectors. These detectors use comparison circuits to verify that the self-test signal is 0 $\pm$1.5 dB. If the self-test signal is above or below the required level, the threshold detectors light the front-panel SELF TEST FAIL indicator and send a fault signal to the alarm panel on the PWR SPLY module.

(8) A BITE test circuit is also provided for testing VF channel E and M signaling. This circuit is connected to the channel under test by means of a patch cable between the SIG jack on BITE and the VF module SIG jack. This connects the E-lead (far-end signaling) to a test circuit that illuminates the OFF-HOOK lamp on the BITE front panel if an off-hook condition is detected. A toggle switch on the BITE front panel permits the test circuit to place the M-lead (near-end signaling) in an off-hook or on-hook condition.

b. Digital Section. This section of the BITE module (fig. 2-30) employs a digital test pattern generator and receiver to detect bit errors on asynchronous and synchronous data channels. The digital section consists of a master clock generator, a test pattern generator, a test pattern detector and a self-test circuit.

(1) The master clock generator circuit divides an external 4.096 MHz transmit clock from the DTG into frequencies of 320 kHz, 50 kHz, and 20 kHz. The DIGITAL FUNCTION rotary switch on BITE permits selection of either the 50 kHz or 20 kHz master clock generator output for the test pattern XMT CLK. An external clock can be patched into the XMT CLK IN jack and selected for the test pattern XMT CLK by setting the DIGITAL FUNCTION rotary switch to EXT CLK.

(2) The test pattern generator circuit consists of a word generator, a transmit sync generator, an error injector and drivers. The word generator is driven at the selected clock rate and produces a pseudo-random binary sequence 2047 bits in length. This pseudo-random test pattern and input clock are sent to the drivers for amplification. The drivers apply the test pattern and clock signals to the XMT DATA OUT and XMT CLK OUT jacks on BITE. The transmit sync generator produces a sync pulse once during each data frame when it detects an all-1 bit sequence from the word generator. The XMT SYNC pulse is applied to the XMT SYNC on the BITE panel so it may be used to synchronize an oscilloscope

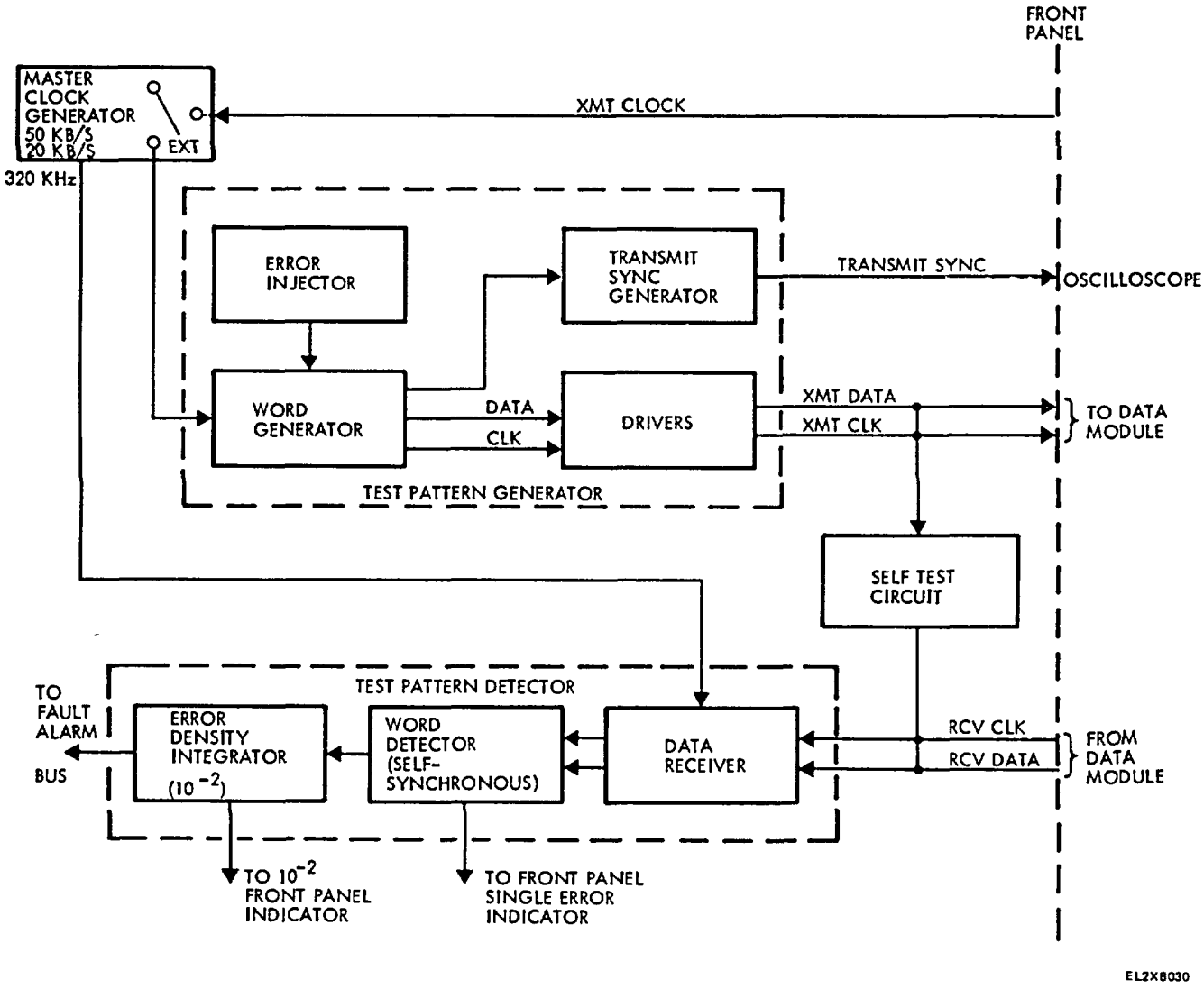


Figure 2-30. BITE digital section block diagram.

when viewing the test pattern. The test pattern also contains an error injector for producing a one-bit error in the transmitted test pattern. When the XMT ERROR INJ switch on the BITE panel is pressed, this circuit inverts one bit in the pseudo-random data stream, injecting an error in the test pattern.

(3) The test pattern detector consists of a data receiver, word detector, and error density integrator. The BITE test pattern signal output is patched through the data channel being tested and patched back into the front-panel RCV DATA IN jack. The data receiver is operative only for 20 kb/s and self-test (also 20 kb/s) data. The 320 kHz clock from the master clock generator is used to shift the incoming data through the data receiver.

Each time a data transition (bit-edge) is detected, the data receiver counts 16 of the 320 kHz (16 X 20 kHz) clocks and produces a midbit clock at the eighth count. The mid-bit clock is sent to the word detector as substitute for the RCV CLK, which is not provided with 20 kb/s asynchronous data. The word detector receives the incoming DATA and CLK (either mid-bit or from RCV CLK IN jack) from the data receiver.

(4) The word detector produces the same pseudo-random test pattern as was transmitted by the word generator, and compares it with the data being received. The word detector is self-synchronizing and requires only 16 clocks to achieve frame synchronization. The word detector illuminates the SYNC indicator on the front panel

as long as frame synchronization is being maintained. If the word detector stops receiving the clocks from the data receiver, it illuminates the RCV CLK LOSS indicator on the front panel. When the word detector comparison circuit senses a difference (error) between the pseudo-random test pattern and the incoming data, it illuminates the BIT ERROR indicator on the front panel and sends a single error signal to the error density integrator.

(5) The error density integrator accumulates the single-bit error signals from the word detector and determines if the total bit error rate exceeds 10^{-2}. This is accomplished by generating a 16,384 bit window time and counting the number of bit errors occurring during that period. If the number of bit errors in the 16,384 bit period exceeds 164, the error density integrator illuminates the BER $>10^{-2}$ indicator on the front panel and inhibits further error counting until the word detector achieves synchronization.

(6) The BITE digital section self-test circuits are enabled by setting the DIGITAL FUNCTION switch to SELF TEST. This causes the 20 kb/s master clock to be selected to drive the test pattern generator. The resulting XMT DATA output is internally routed to the test pattern detector. If the bit error rate of the self-test data exceeds 10-2, the test pattern detector illuminates the SELF TEST FAIL and BER 10^{-2} indicators on the front panel and sends a fault signal to the alarm panel on the PWR SPLY module.

2-21. BITE Module Analog Section Circuit Descriptions

The BITE module (FO-12) consists of the analog section and the digital section. Both sections are described in subparagraphs a and b below.

a. Analog Section. This section consists of six major circuits: test oscillator, output signal attenuators, input signal attenuators and amplifier, ac metering, dc voltage select and metering, selftest, and E and M signaling. These circuits are described in detail in subparagraphs (1) through (7) below.

(1) Test oscillator circuit (fig. FO-12). The analog section oscillator (IC2-A) generates a 0 dBm, 1020 Hz sine wave signal output that is used as a stimulus for VF module alignment and troubleshooting. The output of the test oscillator is available at the XMT VF OSC jack of the BITE module. A Wein Bridge network provides positive feedback to the noninverting input of the oscillator. Phase shift is zero at the correct frequency of oscillation. The frequency is controlled by an AGC loop through Q1 and IC2-B. Peak output of the oscillator at the noninverting input (IC2-B) is 2.192 volts. This voltage is controlled by a Zener diode (VR2) reference voltage. If the amplitude of the oscillator increases, the gain of the oscillator is reduced. If the amplitude of the oscillator decreases, the gain of the oscillator is increased. The feedback is sufficient in either case to restore the correct amplitude.

(2) Output signal attenuators (fig. FO-12). The VF FUNCTION switch and selectable attenuation pads are the key elements of the analog section of BITE. These elements can be used to connect the output of the test oscillator to the VF OSC jack through selectable attenuation pads. When the VF FUNCTION switch is set to CHAN LEV XMT or LOOP TEST, the output level can be set to either 0 dBm or -16 dBm depending on the position of the OSC LEVEL switch. With the VF FUNCTION switch set to SELF TEST or CHAN LEV, a 20 dB attenuator is inserted in series with the oscillator output to provide -20 dBm excitation to the channel level receiver, and a BITE self-test signal. In the COM GAIN XMT position, a 10-dB attenuator provides a -10 dBm signal for use in aligning common gain receivers.

(3) Input signal attenuators and amplifier (fig. FO-12). Signal inputs at the VF METER jack, varying from -20 dBm to +10 dBm can be measured with the BITE module. All signals are conditioned by switched combinations of gain and attenuation to provide an indicated value of 0 dBm on the BITE meter wherever alignment is correct. The input signal attenuators and amplifier elements are: a 10 dB input attenuator, a 20 dB amplifier stage IC1B, and a 10 dB meter attenuation pad. With the VF FUNCTION switch at 4 or 6, the VF METER jack can be either 0 dBm or +7 dBm depending on the strapping option of the channel level receiver. For a 0 dBm input, the BITE meter is capable of displaying a signal from -7 dBm to +2 dBm. For a +7 dBm input, the 10 dBm attenuator must be switched in, allowing the meter to display a signal range from +3 dBm to +12 dBm. The full scale value of the meter is +2 dBm. The METER ATTEN switch can extend this to +12 dBm. At position 3 (and 2) of the VF FUNCTION switch, a -20 dBm signal is accepted from the common gain transmitter. This signal is applied directly to the 20 dB gain stage IC1B to provide an output of 0 dBm. With the switch at position 5, the VF METER jack accepts the -10 dBm output from a channel level transmitter and is attenuated an additional 10 dB by the 10 dB

pad, producing a signal level of -20 dBm at the input to the amplifier. The amplifier provides 20 dB of gain to provide an output of 0 dBm.

(4) Ac metering circuit (fig. FO-12). The ac metering circuit consists of a full-wave rectifier and filter. The signal from the input attenuators and gain stage are buffered by amplifier IC3. A 600-ohm resistor at the noninverting input to IC3 provides the proper termination of the input signals. Amplifiers IC4 and IC1A constitute the fullwave rectifier and filters. Amplifier IC4 is a halfwave rectifier. When an input signal is positive, the output of the amplifier goes negative. When the input voltage is negative, the output of IC4 goes positive. The positive output swing of IC4 is limited to prevent saturation of the amplifier. The circuit becomes a full wave rectifier with the addition of amplifier IC1A. Amplifier IC1A sums the half-wave rectified signal and the input signal to provide a full-wave output. For negative input signals, the output of IC4 is zero. For positive signals, the output of IC1A is the absolute value of the input.

(5) DC voltage select and metering (fig. FO-12). This circuit consists of the DC SUPPLY SELECT switch, multiplier resistors, and the panel meter. To monitor the dc supply voltages, the VF FUNCTION switch is set to DCV, and the DIGITAL FUNCTION switch is set to any position except POWER OFF. This disconnects the panel meter from the ac metering circuit and connects it to DC SUPPLY SELECT switch. Multiplying resistors convert full scale deflection of the meter to 7o and 15 Vdc, respectively.

(6) Self-test (fig. FO-12). To implement analog section self-test, the VF FUNCTION switch is set to 1. This routes the 0 dBm output of oscillator IC2 through an attenuator to the 20 dB amplifier IC1B which amplifies it to provide a 0 dBm level to buffer amplifier IC3. The signal is then converted to de by a full wave rectifier in IC4 and IC1A. The output is attenuated and applied to the inverting input of high limit comparator IC6 and the noninverting input of low limit comparator IC7. The threshold of the high-limit comparator is set to a voltage representing +1.5 dBm. The threshold of the low-limit comparator is set to a voltage representing -1.5 dBm. If the output of the ac voltmeter exceeds either of these limits, an error signal (VF SELF TEST FAIL) goes to -5 volts and an error indication is generated.

(7) E and M signaling (fig. FO-12). VF module signaling can be patched into the front-panel SIG jack. The tip connection applies the E-lead to inverter IC5A, and the ring connection applies the M-lead status selected by on-hook/off-hook switch to the VF module. The E-lead comes from a VF module relay contact that either opens or shorts the E-lead to ground. When the E-lead is at ground, the input to IC5A-1 is pulled to a logic high. This turns on the inverter, which illuminates the OFF HOOK lamp. When the E-lead is opened, the input to the inverter is pulled to a logic low, turning off the inverter and the OFF HOOK lamp. The M-lead actuates a signaling relay in the VF module. An on-hook condition is represented by grounding the M-lead, and is simulated by connecting the M-lead to -42 Vdc. A current limiter protects the -42 Vdc supply from possible damage due to shorts to ground in the signaling relay by limiting M-lead current to approximately 20 mA.

b. *Digital Section.* This section consists of four major circuits: a master clock generator, a test pattern generator, a test pattern detector, and a self-test circuit. These circuits are described in detail in subparagraphs (1) through (4) below.

(1) Master clock generator circuit (fig. FO-12). The generator divides a 4.096: MHz clock received from the DRIVER module into frequencies of 320 kHz, 50 kHz, and 20 kHz. The 4.096MHz clock is applied by amplifier IC102C and inverter IC106C to a ÷9 circuit (IC107). This 9 circuit is followed by a second ÷9 circuit (IC109) to provide a total division of 9 × 9 + X. The value of X is 1 or 0 and is selected by ÷13, counter IC113. The X value is used to synthesize 50 kHz from the 4.096-MHz, with 2 Hz accuracy. The output is provided by NAND gate IC111A to the selecton gates of IC104. The 4.096-MHz clock is also applied to a ÷13 circuit (IC108) to produce a 320-kHz clock used for shifting the incoming 20 kb/s test pattern in the data receiver circuit. The 320-kHz clock is also sent to a ÷16 circuit (IC110) to produce a 20-kHz output to the selection gates of IC104. These gates are controlled by the DIGITAL FUNCTION switch, which permits manual selection of either 50-kb/s, 20-kb/s, external, or self-test (20 kb/s) clocks for application to the test pattern generator circuit.

(2) Test pattern generator circuit (fig. FO-12). Selected transmit clocks from the selection gates (IC104) are applied via inverter IC101C to an 11-bit feedback register consisting, of IC114 and IC115. At the incoming clock rate, this 11-bit register generates pseudo-random binary sequences 2047 bits in length. NAND-gate IC116

and exclusive OR gate IC1170 provide feedback to the register. When the feedback registers start up in an all-1 state, NAND gate IC116 is enabled to place a zero in the shift register to avoid a lockup condition. Once each frame, when an all-1 state is reached, the momentary zero output of NAND gate IC116 is applied via inverter IC131C to the XMT SYNC jack to provide oscilloscope synchronization when viewing the test pattern. Errors are inserted into the outgoing test pattern by pressing the XMT ERROR INJ switch. This applies a low input to NOR gate IC119D, which produces a high output each frame when NAND gate IC116 momentarily goes low. This momentary high output of IC119D inverts one bit in the data stream output of NOR gate IC119C, thereby introducing a one-bit error into the test pattern sequence (frame). The transmit clock and data are applied by drivers IC121 through IC124 to output jacks J208 and J209, respectively. The drivers are capable of driving a 78-ohm load while maintaining an output voltage greater than ±3 volts.

(3) Test pattern detector circuit (fig. FO-12). Incoming test data can be patched into the front-panel RCV DATA IN jack (J206) and routed to the gating circuit of IC105A. If the DIGITAL FUNCTION switch is not set to SELF TEST, the IC105A gating circuit routes the incoming data to gating circuit IC136 via inverter IC131F. As long as the switch is not set to 20 kb/s or SELF TEST, inverter IC131A enables gating circuit IC136 to pass incoming data directly to the word detector register (IC125 and IC126).

(a) If the incoming data is 20 kb/s asynchronous data, then it must be sampled to detect the bit edges so a mid-bit clock can be generated. This is accomplished by clocking incoming 20 kb/s data into transition detector IC132 at a 320-kHz rate. This rate is 16 times the 20-kHz rate. Transition detector IC132 contains a pair of two-bit registers connected to exclusive NOR gate IC117B. Data is clocked into the first gate of the first two-bit register, and exclusive NOR gate IC117B compares the logic level of the two bits. When they differ, as in any transition of data, exclusive NOR gate IC117B provides a positive pulse to the second two-bit register. The contents of this register will be logic Os except when a data transition bit is clocked through its two stages. A 16-bit shift register (IC133 and IC134) is reset by appearance of the transition bit in the first cell of the second two-bit register. The gating circuit of IC119A receives the bit content of the second cell of the second two-bit register and the sixteenth cell of register IC134. This gating circuit provides a 1 input to the register when a count of 16 is reached or if a second data transition is detected.

(b) The mid-bit clock is generated as follows: upon sensing a positive or negative-going data bit edge, transition detector IC132 generates a start pulse and enables shift registers IC133 and IC134 to start shifting 16 clock pulses. When eight clock pulses from the data bit edge have occurred a 3-microsecond mid-bit clock is obtained from the QF output of IC133. If no other data edge appears after shifting 16 clock pulses, the last pulse loops back to the input of the shift register. The new incoming data edge resets the register and starts shifting 16 new clock pulses. In the 20-kb/s (or self-test) mode, gating circuit IC136 routes the mid-bit clock to the word detection circuit. For the other data rates, gating circuit IC136 selects the incoming clock from the RCV CLK IN jack (J205).

(c)The word detector circuit consists of an 11-bit register (IC125 and IC126) with closed-loop feedback via gating circuit IC105B. The register generates the same pseudo-random 2047 bit sequence generated by the test pattern generator. The RCV DATA 1 signal is loaded into an open loop feed-forward register (IC125, IC126, and IC105B). If the received data contains no errors, the output of the register is identical to the RCV DATA 1 input, just as though it were supplying its own input, and the register becomes a feedback register. The received data is fed to the forward register, but it is compared with the output of the register in exclusive OR gate IC117C. Whenever the received data differs from the output of the register, exclusive OR gate IC117C outputs a 1. These outputs of exclusive OR gate IC117C are accumulated for bit error rate measurements. At start up, the register is out of frame synchronization. After 16 bits, the register is loaded with valid RCV DATA and stops generating errors. SYNC flip-flop IC127A goes low, initiating the transfer of the output back to the input of the register. The feedforward register now becomes a feedback register. In this manner, BITE achieves automatic synchronization. As long as synchronization is maintained, the SYNC flip-flop IC127A Q output is low and the SYNC lamp (DS204) is illuminated.

(d) In the error density integrator circuit, an error window counter (IC137, IC138, IC140, IC142) and IC143A generates a 16,384-bit window-time. During each window-time, the bit

errors are accumulated in a bit error counter (IC139 and IC141). If more than 164 bit errors are counted, the bit error rate density detector (IC128A and IC128C), sets the IC143B latch, which in turn causes the BER > 10^{-2} lamp (DS203) to illuminate. Further error counting is also inhibited until SYNC is achieved, and an input to the SELF TEST FAIL indicator is provided if the system is in its self-test mode.

(e) The test pattern detector circuit has the capability of monitoring different functions for detection of faults and providing visual and electrical alarms when faults occur. The RCV CLK LOSS lamp (DS205) circuits includes IC129B and IC130C. A retriggerable one-shot multivibrator (IC129B) normally presents a high level to inverter IC130C by pin 12 when no transitions (loss of clock) have occurred. This high level input to the inverter forces its output low, which results in sufficient current to illuminate the RCV CLK LOSS lamp. When a transition occurs, the one-shot changes state momentarily, creating a low-level at the inverter input, and turning the lamp off. After the one-shot returns to its original state, the lamp is re-illuminated. A periodic clock at the input to the one-shot, will cause the lamp to remain off if the period of the clock is less than that of the one-shot. If the clock is lost for as long as 30 milliseconds (approximately), the RCV CLK LOSS lamp will be on.

(f) The BIT ERROR lamp (DS202) is part of a circuit that includes IC129A and IC130A. This alarm functions identically to the RCV CLK LOSS alarm with the exception that its one-shot period is longer (approximately 1 second) and the lamp is illuminated upon triggering of the one-shot instead of the absence of a trigger. An ERROR DISABLE signal is forwarded to an error bit density network to clear the bit density alarm and turn off the BER > 10^{-2} lamp (DS203) when further errors have not been detected for approximately one second.

(g) The SYNC lamp (DS204) indicates when the system is in sync (lamp out). The sync circuit includes IC127A, IC118C, and IC130B. The circuit receives inputs from the other alarm circuits described in the preceding paragraphs (LOSS CLK SET, 16 COUNT, and BER > 10^{-2}). Typically, the circuit is forced high by the 16 COUNT signal. This signal essentially generates a sync window that is 16 receive clock bits long (i.e., the system is rechecked for sync every 16 bits). Once the SYNC lamp is illuminated, a RCV CLK LOSS sends the LOSS CLK SET signal to set input IC127A and causes SYNC to go low. When SYNC goes low, it reverse biases the junction of DS204, causing it to extinguish and indicate loss of sync. Since IC127A is a D flip-flop configured in a toggle mode, the BER exceeding 10^{-2} causes the SYNC signal to complement its last state. Since the BER signal is a function of the RCV CLK and is also related to 16 COUNT, the BER > 10-2 signal only occurs when the SYNC signal is high.

(4) Self-test circuit (fig. FO-12). The self test circuit is used to check operation of the BITE, and consists of IC111C, IC135D, IC135A, IC130E, IC130D, and the SELF TEST FAIL lamp (DS206). When DIGITAL FUNCTION switch (S207A) is set to SELF-TEST, gating circuits IC104 and IC105A divert the 20-kHz signal from the master clock generator to XMT CLK, and puts XMT DATA on the RCV DATA line. These diversions result in a loop back condition where the two test pattern generators are compared, and the self-sync ability of the word detector is tested. The SELF TEST FAIL lamp may be illuminated by several different failures. For instance, if the BER limit is exceeded, a high at IC135D is generated. IC35D, when enabled by the SELF TEST ENABLE signal, generates a fail signal. In addition, NAND gate IC111C accepts the self-test results, and when enabled by the VF SELF TEST ENABLE signal, also generates a fail signal.

Section VIII. POWER SUPPLY GROUP

2-22. General Information

The multiplexer set can be equipped with either an ac or dc power supply group. Because the power supply groups are similar, the following description applies to both groups. Where differences in these two groups exist, they will be described.

2-23. Major Functions

A block diagram for the power supply group is shown in figure 2-31. The power supply group performs two separate functions: conversion of primary power to multiplexer set operating voltages, and alarm monitoring. The -48 Vdc office primary power is converted by a dc-to-dc converter

NOTE:

THE MULTIPLEXER SET IS CONFIGURED FOR AC ONLY OR DC ONLY.

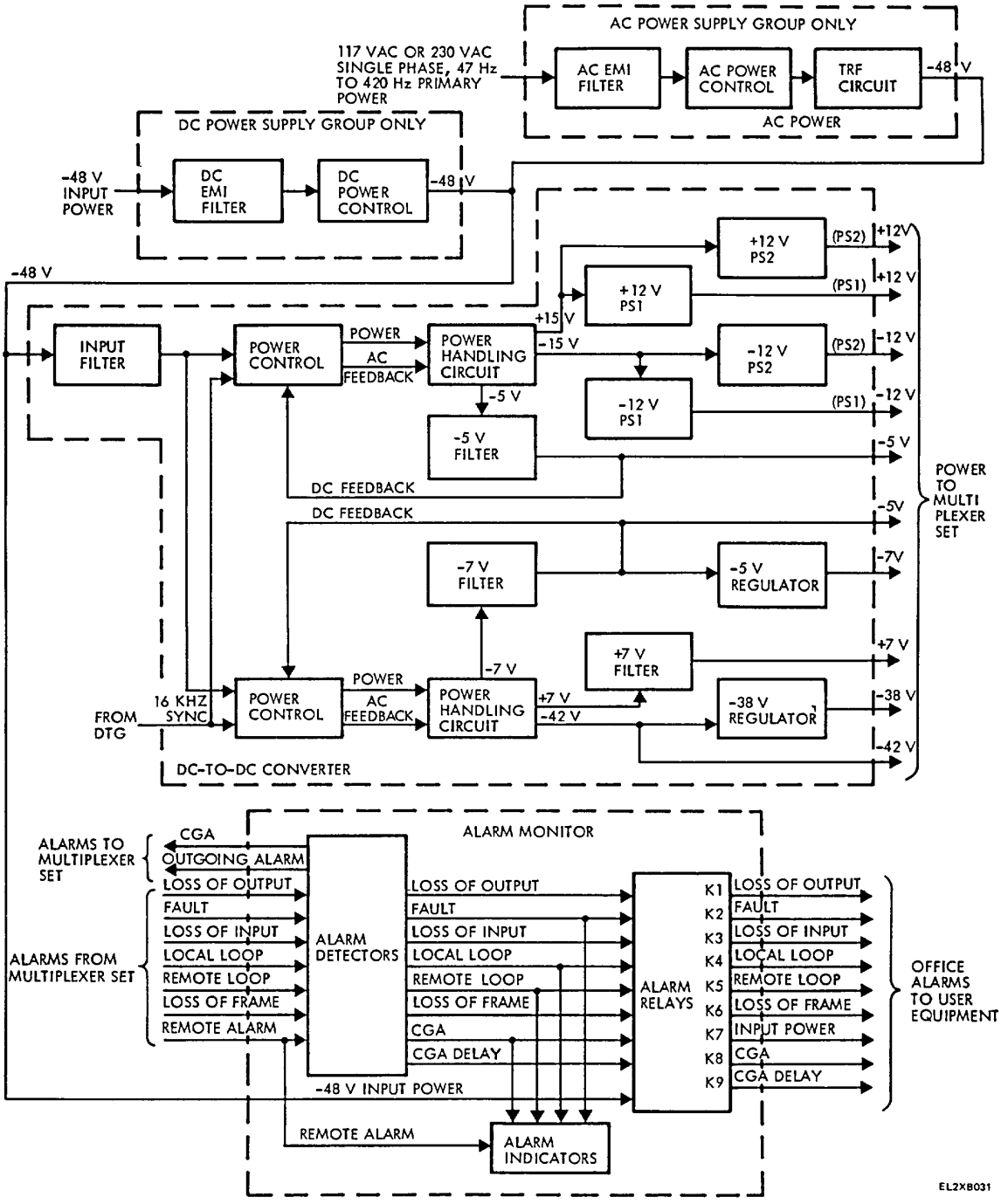


Figure 2-31. Power supply group block diagram.

verter into the regulated voltages required by the multiplexer set. The alarm monitor collects the system alarms and provides the necessary front- panel indication and office alarm relay outputs to

the user equipment. The major functions are described in subparagraphs a through d below.

a. Ac Input Section. The ac input section, which exists only in the ac power supply group, converts ac primary power to the -48 Vdc (nominal) input power required by the dc-to-dc converter. The ac input power passes through an EMI filter, which minimizes the effects of high frequency signals above 10 kHz. The EMI filter output is applied to the AC PWR CONT unit. This unit has an on-off toggle switch and an associated power-on lamp to permit front-panel control and monitoring of input power. In addition, the AC PWR CONT unit contains two 5-ampere fuses, one for each leg of the single-phase primary input. The front panel ON-OFF switch applies ac power to the TRF unit. The TRF unit contains a transformer rectifier filter circuit that converts the ac primary input from the EMI filter to the -48 Vdc (nominal) input required by the dc-to-dc converter. The transformer can be strapped to accept either a 117-Vac or 230-Vac single-phase input at any frequency between 47 Hz and 420 Hz.

b. Dc Input Section. The dc input section, which exists only in the dc power supply group, filters and controls dc primary power application to the dc-to-dc converter. The -48 Vdc officer battery power is applied to the dc power control unit by a dc EMI filter. Operation of the EMI filter and dc PWR CONT unit is identical to that described for the ac input section except that only a single 5-ampere fuse is used for the dc primary power.

c. Dc-to-Dc Converter. The dc-to-dc converter receives a -48 Vdc (-44 Vdc to -64 Vdc) input from either the ac or the dc input section. This input is applied to a filter that attenuates low frequency noise on the primary input that is not removed by the EMI filter. Two separate power handling and control circuits are employed. One is enabled by the positive half cycles of a 16-kHz clock input, and the other is enabled by the negative half cycles. Since loads on the outputs of the two circuits are approximately equal, the input current supplies first one-half the load, then the other half. Power handling and control circuit operation is identical, therefore only one is described. Energy is stored in a transformer in the power handling circuit and delivered to the output regulators as needed. The input current required to resupply the energy in the power handling circuit is provided by the power control circuit. A feedback network is utilized by the power control circuit to assure an adequate energy level in the power handling circuit to maintain the output voltage level. Feedback information is obtained from two sources. A dc feedback monitors the output voltage with the tightest regulation (-5 Vdc for side 1 and -7 Vdc for side 2). In normal operation, filter capacitors cause output voltage variations to occur slowly. Therefore, a secondary ac feedback is used to achieve faster reaction. This feedback anticipates possible shifts in the output level by monitoring the energy stored in the power handling circuit. As the energy level drops, the circuit's ability to supply an increased load decreases. The ac feedback then causes the control circuit to provide more input current. One output of each power handling circuit is regulated by the dc feedback loop, and the others employ additional regulation. The +12 Vdc (PS1) outputs have tighter tolerances on deviation and ripple, so a discrete dissipative regulator is used for each output. The +12 Vdc (PS2) outputs have less restrictive tolerances, so IC post-regulators are used for these outputs.

d. Alarm Monitor. The alarm monitor detects internal or external multiplexer set faults, protects user from the consequences of faults, and provides maintenance personnel with an indication of the nature of the fault. Indicators on the power supply group front panel are provided for FAULT, LOCAL LOOP, REMOTE LOOP, REMOTE ALARM, and CGA alarms. Alarm relays provide contact closures to inform central office equipment of any alarm condition including failure of the -48 Vdc input to the dc-to-de converter. If the alarm monitor receives LOSS OF INPUT or LOSS OF FRAME signals from the DTG, it generates an OGA signal that causes the DTG to send the appropriate alarm code to the far-end terminal. Receipt of any one or more of LOSS OF OUTPUT, LOSS OF INPUT, LOCAL LOOP, REMOTE LOOP, LOSS OF FRAME, or REMOTE ALARM signals causes the alarm monitor to produce a CGA signal.

2-24. Circuit Descriptions

The power supply group ac input, de input, dc-to-dc converter, and alarm monitor circuits are described in detail in the following subparagraphs a through d below.

a. Ac Input Circuit (fig. FO-13). The primary ac power is applied through a passive-type EMI fitler that attenuates reflected currents and voltages on the input power bus. This filter is primarily effective for signals above 10 kHz. The filter output is applied to the AC PWR CONT unit. Toggle switch S1 applies each leg of the ac

input to 5 ampere fuses F1 and F2, respectively. Neon lamp DS1 provides panel indication of power application to the TRF unit. The TRF unit consists of a step-down transformer, full-wave rectifier, single section LC filter. This unit can be strapped at TB2 to accept either 117 Vac or 230 Vac single-phase primary power at any frequency between 47 and 420 Hz. The selected primary power is applied to transformer T1, the output of which is converted to -48 Vdc (nominal) by full wave rectifier CR1 and an LC filter consisting of L1 and C1. The output at TB1, pins 3 and 4, is a -44 to -64 Vdc signal with 1.1 volt peak-to-peak maximum ripple. The output remains within this regulation band for input primary voltage and frequency variations, normal output load changes, and environmental operating conditions.

*b. Dc Input Circuit (*fig. FO-13). The dc input circuit filters and controls application of -48 Vdc (-44 to -64 Vdc office battery power to the dc-to-dc converter). This circuit has an EMI filter and a dc power control unit whose function is similar to that described for the ac input circuit with the exception that a single 5 ampere fuse is employed.

c. Dc-to-Dc Converter (fig. FO-13). A single section LC input filter attenuates low-frequency switching noise on the -48 Vdc primary input to prevent this noise, particularly between 200 to 300 Hz and 1500 Hz range, from being transmitted to the office power distribution system. This filter also reduces ripple from the TRF unit and provides a low-impedance source for the switching regulators. Two fully independent switching regulators provide the required outputs. The regulators are timed by a common clock that is synchronized by a 16-kHz clock from the DTG (after power has been established). Since these circuits are similar only one will be described.

(1) Energy is stored in transformer T3 when transistor switch Q3 is turned on. When Q3 is turned off, the stored energy is transferred to the load. Output regulation is obtained by controlling the on time of switch Q3. A feedback network maintains an adequate energy level to maintain the output voltage level. The current drive circuit is transformer-coupled transistor Q3 switching network.

(2) The turn-on of the control logic is initiated by the start clock circuit, which is synchronized to a 16-kIIz signal derived from the channel counter generator in the DRIVER unit. In the absence of this input, the start clock free runs at approximately 13 kHz. At the power polarity of the start clock signal, the digital logic turns on current drive circuit Q3. Circuit Q3 passes dc current to transformer T3, the power handling circuit. The amount of current supplied is sensed in current transformer T1.

(3) Turn-off is controlled by one of two means. In normal operation, enough current is allowed to flow to supply the output load as determined by the normal feedback path. If the current transformer peak current detector senses an overload condition, the digital logic turns off the current drive. If there is a failure in the digital logic at overload, an override current limit signal is forwarded directly to turn off the current drive.

(4) Feedback information for normal control of the proportional current input is obtained from two sources. A dc feedback path monitors the output voltage with the tightest regulation (-5V -1 for side 1, -7V for side 2). In normal operation, the output voltage variations occur slowly because of the filter capacitors. A secondary ac feedback path anticipates possible shifts in the output level by monitoring the energy stored in the power handling circuit. A drop in this energy level indicates an increased load and a requirement for more input current. The dc and ac feedback levels are integrated and compared to a fixed reference by threshold detector IC7B. The resultant output signal is amplified by high-gain amplifier IC3A. If the output has changed sufficiently, a control signal input to the digital logic changes the on cycle of switch Q3 accordingly. The threshold is set high enough to prevent instability in the feedback loop.

(5) Power for the logic and control circuits is obtained from both side I and side 2 in a redundant configuration with diode isolation. If one power handling circuit fails, control logic for the other is still available. Upon initial turn-on, there is no power for any of the system logic; there is, therefore, no 16-kHz SYNC signal or power supply control logic. A starting circuit is employed that is powered directly from the -48 Vdc input and consists of low-frequency oscillator Q9 and Q10. The initial few cycles of this oscillator drive the current drive circuit directly to raise the output voltage quickly; then the normal control circuits take over. One output from each power handling circuit is regulated by the feedback loop. The others employ additional regulation. On side 1, the +12 Vdc (-1) outputs have a tighter tolerance on percent deviation and ripple, so a discrete dissipative regulator is used on each output. The +12 Vdc (-2) has a less restrictive

regulation requirement, so IC post-regulators are preregulated based on the -5 Vdc (-1) load. Thus, if a short circuit develops in the system logic, it will affect the 12 Vdc supplies as well as the -5 Vdc supply. A reference voltage for the 12 Vdc (-1) supplies is obtained from a Zener diode across the output. Each discrete regulator also contains a vernier screwdriver adjustment for initial zero setting of the regulator.

d. Alarm Monitor (fig. FO-14). The internal and external alarm signals are received by the alarm monitor and applied to relay and lamp drivers Q8 through Q22. Relays K1 through K9 provide contact closures that inform the central office equipment of the alarm condition and create OGA and CGA signals. Table 2-3 defines the alarms, their cause, and result. NAND gate IC9 produces a CGA signal if any one or more inputs is in an alarm state (LO). This CGA signal can be inhibited by pressing CGA DEFEAT switch S2. Switch S1 illuminates all the alarm indicators for lamp testing.

Table 2-3. Alarm Circuit Operation

Alarm	Cause	Result
LOSS OF OUTPUT	DTG detects no transmit data or timing for 100 milliseconds or more and forces LOSS OF OUTPUT signal high.	Relay K1 is energized.
FAULT	Malfunction occurs in one or more plug-in modules and FAULT signal goes low.	FAULT lamp DS1 is illuminated and relay K2 is energized.
LOSS OF INPUT	DTG detects no receive data or timing for 100 milliseconds or more and forces LOSS OF INPUT signal low.	Relay K3 is energized.
LOCAL LOOP	DTG loops transmit data back to receive, sends all ls to far end, and forces LOOP signal high.	LOCAL LOOP lamp DS2 is illuminated and relay K4 is energized.
REMOTE LOOP	DTG detects all is in far-end data and forces REMOTE LOOP signal high.	REMOTE LOOP lamp DS3 is illuminated and relay K5 is energized.
LOSS OF FRAME	DTG detects loss of framing and 'forces LOSS OF FRAME signal high.	Relay K6 is energized.
REMOTE ALARM	DTG detects OGA code (B2 = 0 or 00001111) in the incoming bit stream and forces REMOTE ALARM signal high.	REMOTE ALARM lamp DS5 is illuminated.
OGA	Alarm monitor detects loss of frame or loss of input alarm.	High OGA signal causes OGA code to be sent to far-end. (Code is determined by strapping of DTG).
CGA	Alarm monitor detects presence of any one or more of LOSS OF INPUT, LOSS OF OUTPUT, LOCAL LOOP, REMOTE LOOP, LOSS OF FRAME, and REMOTE ALARM signals.	C.G.A. lamp DS4 is illuminated, relay K8 is energized, and CGA signal is sent to multiplexer.
INPUT POWER	-48 Vdc power input is below -24 Vdc.	Relay K7 is deenergized.
CGA DELAY	CGA exists for 10 seconds.	Relay K1 is energized 10 seconds after start of CGA.
FORCE ALL 1s OUTPUT	LOCAL LOOP alarm is detected.	FORCE ALL is OUTPUT command is sent to DTG.

CHAPTER 3
GENERAL SUPPORT MAINTENANCE

Section I. GENERAL

3-1. Scope of Maintenance

This chapter contains instructions for general support maintenance of the individual modules/ units comprising Multiplexer Set AN/FCC-98 (V). The instructions cover troubleshooting, disassembly/reassembly, repairing, readjusting/ aligning, and performance testing of individual modules. Various types of maintenance support data, such as waveforms and parts location diagrams, are also provided. For convenience, the support data is arranged by module and associated troubleshooting procedure. Detailed schematic diagrams for each functional assembly are placed in foldout (FO) pages at the back of the manual.

a. Resistance Data. Values for individual resistors are provided on the detailed schematic diagrams at the back of the manual. Procedures for determining values of resistors that must be selected in test (SIT) are provided in section IV.

b. Voltage Data. Special voltages developed within modules/units are provided where applicable. The voltages represent a module operating in a normal condition, or as described by the associated troubleshooting procedure.

c. Waveforms. Waveforms are provided for significant digital and analog functions. Waveforms are representative of the operating/test conditions described in the associated troubleshooting or performance test procedures for the module.

3-2. Standard Maintenance Instructions

Unless otherwise specified, instructions in this manual for performing standard maintenance actions have the meanings defined in the following subparagraphs.

CAUTION

All plug-in units in the MXTF upper bay can be damaged by being installed or removed with power applied to the MXTF. Always ensure that the MXTF power switch on the PWR CONT module is set to OFF when performing such actions. It is also recommended that the same precautions be taken when probing or strapping during test or troubleshooting procedures.

a. Checking Signals. Signals are checked by observing the signal (waveform) at the point specified, using an AN/USM-281C and 1X (direct) probe. The left probe of the AN/USM-281C is always used to check signals unless otherwise specified. Instructions are provided in the procedures for selecting main AN/USM-281C functions.

(1) Volts-per-vertical division setting are specified as VOLTS/DIV, left and right. Unless otherwise specified, settings on waveform illustrations indicate use of IX (direct) probes. If 10X probes are used, the indicated settings must be multiplied by 10 to maintain waves hape representation as illustrated.

(2) Time-per-horizontal division settings are specified as TIME/DIV.

(3) Trigger selections are specified as TRIG SOURCE LEFT, TRIG SOURCE RIGHT, or SOURCE EXT. The left and right selections mean to use internal (SOURCE INT) trigger.

(4) Coupling instructions are specified as ac or dc.

(5) VERT MODE switch settings should be made as required to select left or right vertical amplifiers.

b. Measuring Resistance. Instructions for measuring resistance means to do so using the DMM or the AN/USM-223, with appropriate mode and range selections.

c. Checking TTL Logic States. Logic state voltage bands may be measured with either the DMM, AN/USM-223, AN/USM-281C or the voltmeter

on the PMTF, all set for dc input. Multiplexer Set AN/FCC-98(V) circuits primarily utilize low-level logic (LO) with a logic high (HI) represented by a zero or slightly negative voltage. In this manual, unless specified otherwise, HI logic voltage is 0 Vdc to less than -2.4 Vdc, and LO logic voltage is greater than -2.4 Vdc to -5.5 Vdc.

d. Measuring Frequency. Instructions for measuring frequency means to use the CP-772A/ U, an electronic counter, to determine the frequency of the signal.

e. Identification of Modules/Units. Modules or units being repaired are referred to in this manual as units under repair (UUR). This reference is used whether troubleshooting, repair, or testing is actually involved.

f. Lamp Conditions. Unless specified otherwise, in all troubleshooting and test instructions, only the lamps specified should be observed. Other lamp conditions, especially those on BITE, should be disregarded.

g. Configuration Coding. Most of the subassemblies were built to more than one configuration. Table 3-1 contains all the data required to cross reference the subassembly serial numbers to a configuration code. The first column specifies the nomenclature which identifies the specific unit. The second column shows the serial numbers (production units only) which correspond to the configuration code. The third column specifies the configuration code. The first three alphanumerics identify the subassembly and the remaining two digits reflect the actual differences in configuration. The last two columns specify the applicable parts location (P/L) diagram and schematic.

3-3. Maintenance Setups and Module Strapping

All operational maintenance procedures in this chapter (troubleshooting, testing, etc.) deal with UURs being installed, on extender boards if necessary, in either the PMTF or the MXTF. For these setups, both the module type and its strapping must be considered. Complete information on module strapping and channel usage is contained in TM 11-5805-711-13. A summary of strapping data is contained in table 3-3. Although instructions in this manual specify which strapping and channels are to be used, maintenance personnel should be aware of the following rules:

a. DTG. The DTG can be strapped to operate in any one of four channel modes, 3, 6, 12, or 24 channels. In the 24-channel mode the output may be NRZ or bipolar mode, with zero either suppressed or unsuppressed. It can be strapped for either voice or data outgoing alarms.

b. VF Modules. VF modules can be used in any of the 24-channel positions of the multiplexer set. They do not preempt (make unusable) any other channel.

Table 3-1. Configuration Coding

Unit Nomenclature	S/N Effectivity	Code	Applicable P/L Diagram	Applicable Schematic
PCI	5-29	PCM02	3-3	FO-2
	30-555	PCM04	3-3	FO-2
	556-Subs	PCM06	3-3	FO-2
MUX	5-572	MUX02	3-6	FO-3
	573 and Subs	MUX04	3-6	FO-3
DRIVER	5-355	DVR02	3-9	FO-4
	356 and Subs	DVR01	3-9	FO-4
RCVR	5-61	RCV02	3-12	FO-5
	62-355	RCV04	3-12	FO-5
	356-1060	RCV06	3-12	FO-5
	1061 and Subs	RCV08	3-12	FO-5
DEMUX	5-355	DMX02	3-15	FO-6
	356-960	DMX04	3-15	FO-6
	961 and Subs	DMX06	3-15	FO-6
PCD	5-29	PCD02	3-18	FO-7
	30 and Subs	PCD04	3-18	FO-7
BITE Analog	25-136	BIA02	3-32	FO-12
	137-626	BIA04	3-32	FO-12
	627-1102	BIA06	3-32	FO-12
	1103 and Subs	BIA08	3-32	FO-12

Table 3-1. Configuration Coding-Continued

Unit Nomenclature	S/N Effectivity	Code	Applicable P/L Diagram	Applicable Schematic
BITE Digital	25-458	BID02	3-32	FO-12
	459-711	BID04	3-32	FO-12
	712-1016	BID06	3-32	FO-12
	1017 and Subs	BID08	3-32	FO-12
AC Power Control	26-329	ACP02	3-35	FO-15
	330 and Subs	ACP04	3-35	FO-15
DC Power Control	14-400	DCP02	3-35	FO-15
	401 and Subs	DCP04	3-35	FO-15
Power Supply	33-47	DCC02	3-35	FO-13
DC to DC	48-91	DCC04	3-35	FO-13
Converter	92 and Subs	DCC06	3-35	FO-13
Power Supply	33-47	PMA02	3-35	FO-14
Monitor and	48-91	PMA04	3-35	FO-14
Alarm	92-148	PMA02	3-35	FO-14
	149-302	PMA04	3-35	FO-14
	303-722	PMA06	3-35	FO-14
	723-819	PMA08	3-35	FO-14
	820-1084	PMA10	3-35	FO-14
	1085-1482	PMA12	3-35	FO-14
	1483 and Subs	PMA14	3-35	FO-14
DC EMI Filter	14-1035	DCE02	3-35	FO-16
	1036 and Subs	DCE04	3-35	FO-15
AC EMI Filter	29-657	ACE02	3-35	FO-15
	658 and Subs	ACE04	3-35	FO-15
0-20 kb/s	28-341	20K02	3-24	FO-9
	342	20K04	3-24	FO-9
	343-493	20K02	3-24	FO-9
	494	20K04	3-24	FO-9
	495-518	20K02	3-24	FO-9
	519	20K04	3-24	FO-9
	520-555	20K02	3-24	FO-9
	556	20K04	3-24	FO-9
	557	20K02	3-24	FO-9
	558	20K04	3-24	FO-9
	559-567	20K02	3-24	FO-9
	568	20K04	3-24	FO-9
	569-597	20K02	3-24	FO-9
	598	20K04	3-24	FO-9
	599-606	20K02	3-24	FO-9
	607	20K04	3-24	FO-9
	608-631	20K02	3-24	FO-9
	632	20K04	3-24	FO-9
	633	20K02	3-24	FO-9
	634	20K04	3-24	FO-9
	635-659	20K02	3-24	FO-9
	660	20K04	3-24	FO-9
	661-726	20K02	3-24	FO-9
	727	20K04	3-24	FO-9
	728-777	20K02	3-24	FO-9
	778	20K04	3-24	FO-9
	779-788	20K02	3-24	FO-9
	789	20K04	3-24	FO-9
	790-794	20K02	3-24	FO-9
	795	20K04	3-24	FO-9
	796	20K02	3-24	FO-9
	797	20K04	3-24	FO-9
	798-824	20K02	3-24	FO-9

Table 3-1. Configuration Coding-Continued

Unit Nomenclature	S/N Effectivity	Code	Applicable P/L Diagram	Applicable Schematic
0-20 kb/s	825	20K04	3-24	FO-9
	826-829	20K02	3-24	FO-9
	830	20K04	3-24	FO-9
	831-840	20K02	3-24	FO-9
	841	20K04	3-24	FO-9
	842-870	20K02	3-24	FO-9
	871	20K04	3-24	FO-9
	872-887	20K02	3-24	FO-9
	888	20K04	3-24	FO-9
	889-946	20K02	3-24	FO-9
	947	20K04	3-24	FO-9
	948-968	20K02	3-24	FO-9
	969	20K04	3-24	FO-9
	970-988	20K02	3-24	FO-9
	989	20K04	3-24	FO-9
	990-1013	20K02	3-24	FO-9
	1014	20K04	3-24	FO-9
	1015 and Subs	20K02	3-24	FO-9
50 khls	16-46	50K04	3-27	FO-10
	47	50K02	3-27	FO-10
	48 and 49	50K04	3-27	FO-10
	50 and 51	50K02	3-27	FO-10
	52-54	50K04	3-27	FO-10
	55	50K02	3-27	FO-10
	56-80	50K04	3-27	FO-10
	81	50K02	3-27	FO-10
	82-131	50K04	3-27	FO-10
	132 and 133	50K02	3-27	FO-10
	134-140	50K04	3-27	FO-10
	141	50K02	3-27	FO-10
	142-144	50K04	3-27	FO-10
	145	50K02	3-27	FO-10
	146-154	50K04	3-27	FO-10
	155	50K02	3-27	FO-10
	156-163	50K04	3-27	FO-10
	164-166	50K02	3-27	FO-10
	167	50K04	3-27	FO-10
	168	50K02	3-27	FO-10
	169-171	50K04	3-27	FO-10
	172	50K02	3-27	FO-10
	173 and 174	50K04	3-27	FO-10
	175	50K02	3-27	FO-10
	176 and 177	50K04	3-27	FO-10
	178	50K02	3-27	FO-10
	179-181	50K04	3-27	FO-10
	182	50K02	3-27	FO-10
	183-188	50K04	3-27	FO-10
	189	50K02	3-27	FO-10
	190-197	50K04	3-27	FO-10
	198	50K02	3-27	FO-10
	199	50K04	3-27	FO-10
	200-202	50K02	3-27	FO-10
	203-205	50K04	3-27	FO-10
	206	50K02	3-27	FO-10
	207	50K04	3-27	FO-10
	208-210	50K02	3-27	FO-10
	211 and 212	50K04	3-27	FO-10
	213-217	50K02	3-27	FO-10
	218	50K04	3-27	FO-10
	219	50K02	3-27	FO-10
	220	50K04	3-27	FO-10

Table 3-1. Configuration Coding - Continued

Unit Nomenclature	S/N Effectivity	Code	Applicable P/L Diagram	Applicable Schematic
50 kb/s	221-233	50K02	3-27	FO-10
	234-238	50K04	3-27	FO-10
	239 and 240	50K02	3-27	FO-10
	241-250	50K04	3-27	FO-10
	251 and 252	50K02	3-27	FO-10
	253 and 254	50K04	3-27	FO-10
	255	50K02	3-27	FO-10
	256 and 257	50K04	3-27	FO-10
	258 and 259	50K02	3-27	FO-10
	260 and 261	50K04	3-27	FO-10
	262	50K02	3-27	FO-10
	263-265	50K04	3-27	FO-10
	266	50K02	3-27	FO-10
	267-288	50K04	3-27	FO-10
	289	50K06	3-27	FO-10
	290-293	50K04	3-27	FO-10
	294	50K02	3-27	FO-10
	295	50K04	3-27	FO-10
	296	50K02	3-27	FO-10
	297-311	50K04	3-27	FO-10
	312	50K06	3-27	FO-10
	313	50K04	3-27	FO-10
	314	50K06	3-27	FO-10
	315-321	50K04	3-27	FO-10
	322	50K06	3-27	FO-10
	323-327	50K04	3-27	FO-10
	328	50K02	3-27	FO-10
	329	50K04	3-27	FO-10
	335	50K06	3-27	FO-10
	336-354	50K04	3-27	FO-10
	355	50K06	3-27	FO-10
	356	50K04	3-27	FO-10
	357	50K06	3-27	FO-10
	358	50K04	3-27	FO-10
	359	50K06	3-27	FO-10
	360 and 361	50K04	3-27	FO-10
	362	50K06	3-27	FO-10
	363-375	50K04	3-27	FO-10
	376-379	50K06	3-27	FO-10
	380	50K04	3-27	FO-10
	381 and 382	50K06	3-27	FO-10
	383	50K04	3-27	FO-10
	384	50K06	3-27	FO-10
	385	50K04	3-27	FO-10
	386	50K06	3-27	FO-10
	387	50K04	3-27	FO-10
	388	50K06	3-27	FO-10
	389-394	50K04	3-27	FO-10
	395-397	50K06	3-27	FO-10
	398-402	50K04	3-27	FO-10
	403	50K06	3-27	FO-10
	404-407	50K04	3-27	FO-10
	408	50K06	3-27	FO-10
	409-413	50K04	3-27	FO-10
	414	50K06	3-27	FO-10
	415-423	50K04	3-27	FO-10
	424	50K06	3-27	FO-10
	425-429	50K04	3-27	FO-10
	430	50K06	3-27	FO-10
	431-450	50K04	3-27	FO-10
	451	50K06	3-27	FO-10
	452-458	50K04	3-27	FO-10

Table 3-1. Configuration Coding-Continued

Unit Nomenclature	S/N Effectivity	Code	Applicable P/L Diagram	Applicable Schematic
50 kb/s	459	50K06	3-27	FO-10
	460-468	50K04	3-27	FO-10
	469	50K06	3-27	FO-10
	470-480	50K04	3-27	FO-10
	481	50K06	3-27	FO-10
	482-485	50K04	3-27	FO-10
	486	50K06	3-27	FO-10
	487	50K04	3-27	FO-10
	488	50K06	3-27	FO-10
	489-499	50K04	3-27	FO-10
	500	50K06	3-27	FO-10
	501-509	50K04	3-27	FO-10
	510	50K06	3-27	FO-10
	511-514	50K04	3-27	FO-10
	515	50K06	3-27	FO-10
	516 and 517	50K04	3-27	FO-10
	518 and 519	50K06	3-27	FO-10
	520-522	50K04	3-27	FO-10
	523	50K06	3-27	FO-10
	524-532	50K04	3-27	FO-10
	533	50K06	3-27	FO-10
	534-538	50K04	3-27	FO-10
	539	50K06	3-27	FO-10
	540	50K04	3-27	FO-10
	541	50K06	3-27	FO-10
	542 and 543	50K04	3-27	FO-10
	544	50K06	3-27	FO-10
	545 and 546	50K04	3-27	FO-10
	547	50K06	3-27	FO-10
	548-559	50K04	3-27	FO-10
	560	50K06	3-27	FO-10
	561-568	50K04	3-27	FO-10
	569	50K06	3-27	FO-10
	570 and 571	50K04	3-27	FO-10
	572	50K06	3-27	FO-10
	573	50K04	3-27	FO-10
	574	50K06	3-27	FO-10
	575-598	50K04	3-27	FO-10
	599	50K06	3-27	FO-10
	600-607	50K04	3-27	FO-10
	608-610	50K06	3-27	FO-10
	611-617	50K04	3-27	FO-10
	618 and 619	50K06	3-27	FO-10
	620-622	50K04	3-27	FO-10
	623 and 624	50K06	3-27	FO-10
	625 and 626	50K04	3-27	FO-10
	627	50K06	3-27	FO-10
	628	50K04	3-27	FO-10
	629	50K06	3-27	FO-10
	630-634	50K04	3-27	FO-10
	635	50K06	3-27	FO-10
	636-641	50K04	3-27	FO-10
	642	50K06	3-27	FO-10
	643 and 644	50K04	3-27	FO-10
	645	50K06	3-27	FO-10
	646-648	50K04	3-27	FO-10
	649	50K06	3-27	FO-10
	650 and 651	50K04	3-27	FO-10
	652	50K06	3-27	FO-10
	653-657	50K04	3-27	FO-10
	658	50K06	3-27	FO-10
	659-662	50K04	3-27	FO-10

Table 3-1. Configuration Coding-Continued

Unit Nomenclature	S/N Effectivity	Code	Applicable P/L Diagram	Applicable Schematic
50 kb/s	663 and 664	50K06	3-27	FO-10
	665-669	50K04	3-27	FO-10
	670 and 671	50K06	3-27	FO-10
	672-675	50K04	3-27	FO-10
	676	50K06	3-27	FO-10
	677-681	50K04	3-27	FO-10
	682	50K06	3-27	FO-10
	683	50K04	3-27	FO-10
	684	50K06	3-27	FO-10
	685-688	50K04	3-27	FO-10
	689-691	50K06	3-27	FO-10
	692	50K04	3-27	FO-10
	693	50K06	3-27	FO-10
	694-697	50K04	3-27	FO-10
	698	50K06	3-27	FO-10
	699	50K04	3-27	FO-10
	700 and 701	50K06	3-27	FO-10
	702-704	50K04	3-27	FO-10
	705	50K06	3-27	FO-10
	706-710	50K04	3-27	FO-10
	711 and 712	50K06	3-27	FO-10
	713	50K04	3-27	FO-10
	714	50K06	3-27	FO-10
	715	50K04	3-27	FO-10
	716	50K06	3-27	FO-10
	717 and 718	50K04	3-27	FO-10
	719	50K06	3-27	FO-10
	720 and 721	50K04	3-27	FO-10
	722	50K06	3-27	FO-10
	723-725	50K04	3-27	FO-10
	726	50K06	3-27	FO-10
	727	50K04	3-27	FO-10
	728 and 729	50K06	3-27	FO-10
	730-733	50K04	3-27	FO-10
	734	50K06	3-27	FO-10
	735-738	50K04	3-27	FO-10
	739	50K06	3-27	FO-10
	740-745	50K04	3-27	FO-10
	746	50K06	3-27	FO-10
	747 and 748	50K04	3-27	FO-10
	749	50K06	3-27	FO-10
	750	50K04	3-27	FO-10
	751 and 752	50K06	3-27	FO-10
	753	50K04	3-27	FO-10
	754 and 755	50K06	3-27	FO-10
	756	50K04	3-27	FO-10
	757 and 758	50K06	3-27	FO-10
	759-764	50K04	3-27	FO-10
	765	50K06	3-27	FO-10
	766	50K04	3-27	FO-10
	767 and 768	50K06	3-27	FO-10
	769 and 770	50K04	3-27	FO-10
	771	50K06	3-27	FO-10
	772-776	50K04	3-27	FO-10
	777	50K06	3-27	FO-10
	778-782	50K04	3-27	FO-10
	783 and 784	50K06	3-27	FO-10
	785	50K04	3-27	FO-10
	786	50K06	3-27	FO-10
	787	50K04	3-27	FO-10
	788-790	50K06	3-27	FO-10
	791	50K04	3-27	FO-10

Table 3-1. Configuration Coding-Continued

Unit Nomenclature	S/N Effectivity	Code	Applicable P/L Diagram	Applicable Schematic
50 kb/s	792 and 793	50K06	3-27	FO-10
	794	50K04	3-27	FO-10
	795-797	50K06	3-27	FO-10
	798-800	50K04	3-27	FO-10
	801	50K06	3-27	FO-10
	802-804	50K04	3-27	FO-10
	805	50K06	3-27	FO-10
	806	50K04	3-27	FO-10
	807 and 808	50K06	3-27	FO-10
	809-812	50K04	3-27	FO-10
	813-816	50K06	3-27	FO-10
	817 and 818	50K04	3-27	FO-10
	819-821	50K06	3-27	FO-10
	822	50K04	3-27	FO-10
	823	50K06	3-27	FO-10
	824 and 825	50K04	3-27	FO-10
	826 and 827	50K06	3-27	FO-10
	828-834	50K04	3-27	FO-10
	835	50K06	3-27	FO-10
	836	50K04	3-27	FO-10
	837	50K06	3-27	FO-10
	838 and 839	50K04	3-27	FO-10
	840	50K06	3-27	FO-10
	841-847	50K04	3-27	FO-10
	848	50K06	3-27	FO-10
	849 and 850	50K04	3-27	FO-10
	851 and 852	50K06	3-27	FO-10
	853	50K04	3-27	FO-10
	854	50K06	3-27	FO-10
	855-857	50K04	3-27	FO-10
	858	50K06	3-27	FO-10
	859	50K04	3-27	FO-10
	860	50K06	3-27	FO-10
	861-865	50K04	3-27	FO-10
	866	50K06	3-27	FO-10
	867-869	50K04	3-27	FO-10
	870	50K06	3-27	FO-10
	871-873	50K04	3-27	FO-10
	874	50K06	3-27	FO-10
	875-882	50K04	3-27	FO-10
	883	50K06	3-27	FO-10
	884-886	50K04	3-27	FO-10
	887	50K06	3-27	FO-10
	888-890	50K04	3-27	FO-10
	891	50K06	3-27	FO-10
	892-896	50K04	3-27	FO-10
	897	50K06	3-27	FO-10
	898-902	50K04	3-27	FO-10
	903-906	50K06	3-27	FO-10
	907-911	50K04	3-27	FO-10
	912 and 913	50K06	3-27	FO-10
	914	50K04	3-27	FO-10
	915	50K06	3-27	FO-10
	916	50K04	3-27	FO-10
	917 and 918	50K06	3-27	FO-10
	919-923	50K04	3-27	FO-10
	924 and 925	50K06	3-27	FO-10
	926 and 927	50K04	3-27	FO-10
	928-931	50K06	3-27	FO-10
	932 and 933	50K04	3-27	FO-10
	934-939	50K06	3-27	FO-10
	940-957	50K04	3-27	FO-10

Table 3-1. Configuration Coding-Continued

Unit Nomenclature	S/N Effectivity	Code	Applicable P/L Diagram	Applicable Schematic
50 kb/s	958	50K06	3-27	FO-10
	959-961	50K04	3-27	FO-10
	962	50K06	3-27	FO-10
	963-966	50K04	3-27	FO-10
	967-969	50K06	3-27	FO-10
	970	50K04	3-27	FO-10
	971	50K06	3-27	FO-10
	972 and 973	50K04	3-27	FO-10
	974	50K06	3-27	FO-10
	975-977	50K04	3-27	FO-10
	978	50K06	3-27	FO-10
	979	50K04	3-27	FO-10
	980 and 981	50K06	3-27	FO-10
	982	50K04	3-27	FO-10
	983	50K06	3-27	FO-10
	984-994	50K04	3-27	FO-10
	995	50K06	3-27	FO-10
	996-1036	50K04	3-27	FO-10
	1037	50K06	3-27	FO-10
	1038 and 1039	50K04	3-27	FO-10
	1040	50K06	3-27	FO-10
	1041	50K04	3-27	FO-10
	1042-1045	50K06	3-27	FO-10
	1046	50K04	3-27	FO-10
	1047-1050	50K06	3-27	FO-10
	1051	50K04	3-27	FO-10
	1052 and 1053	50K06	3-27	FO-10
	1054 and Subs	50K04	3-27	FO-10
Multirate	36-76	MTR04	3-30	FO-11
	77-105	MTR02	3-30	FO-11
	106	MTR04	3-30	FO-11
	107	MTR02	3-30	FO-11
	108	MTR04	3-30	FO-11
	109-159	MTR02	3-30	FO-11
	160	MTR04	3-30	FO-11
	161	MTR02	3-30	FO-11
	162	MTR04	3-30	FO-11
	163-166	MTR02	3-30	FO-11
	167	MTR04	3-30	FO-11
	168-180	MTR02	3-30	FO-11
	181	MTR04	3-30	FO-11
	182-192	MTR02	3-30	FO-11
	193	MTR04	3-30	FO-11
	194-197	MTR02	3-30	FO-11
	198	MTR04	3-30	FO-11
	199-205	MTR02	3-30	FO-11
	206	MTR04	3-30	FO-11
	207-210	MTR02	3-30	FO-11
	211	MTR04	3-30	FO-11
	212	MTR02	3-30	FO-11
	213-215	MTR04	3-30	FO-11
	216 and 217	MTR02	3-30	FO-11
	218 and 219	MTR04	3-30	FO-11
	220-222	MTR02	3-30	FO-11
	223 and 224	MTR04	3-30	FO-11
	225 and 226	MTR02	3-30	FO-11
	227	MTR04	3-30	FO-11
	228	MTR02	3-30	FO-11
	229-234	MTR04	3-30	FO-11

Table 3-1. Configuration Coding--Continued

Unit Nomenclature	S/N Effectivity	Code	Applicable P/L Diagram	Applicable Schematic
Multirate	235-240	MTR02	3-30	FO-11
	241	MTR04	3-30	FO-11
	242-257	MTR02	3-30	FO-11
	258	MTR04	3-30	FO-11
	259	MTR02	3-30	FO-11
	260	MTR04	3-30	FO-11
	261	MTR02	3-30	FO-11
	262 and 263	MTR04	3-30	FO-11
	264 and 265	MTR02	3-30	FO-11
	266-268	MTR04	3-30	FO-11
	269	MTR02	3-30	FO-11
	270 and Subs	MTR04	3-30	FO-11

c. 0-20 and 50 kb/s Data Modules. Asynchronous 0-20 and 50 kb/s data modules can be used in any channel position from 1 through 12, and in any odd channel position from 13 through 23. They do not preempt any other channels.

d. Multirate Data Modules. Limitations as to the testing of multirate data modules in an MIXFT depend upon both the data rate they are strapped to handle and, in some cases, the adjacent or alternative mode in which they are strapped to operate.

(1) *56 kb/s and 4 kb/s strapping*. Each module requires one (only) channel, and can be used in any channel position from 1 through 12 and in any odd channel position from 13 through 23.

(2) *128 kb/s strapping*. Each module can be used in any channel position 1 through 12 or in odd positions 13 through 23. Operation of modules at 128 kb/s preempts one other channel besides the one in which the module is being used. Which particular channel is preempted depends upon whether the module is strapped to operate in an adjacent or an alternate mode.

(a) *Adjacent mode (128 kb/s).* In an adjacent mode of operation, each module operating at 128 kb/s preempts the next higher channel. For example, if the module is being used in channel position 5, it preempts channel 6; or, if it is used in channel 12 position, it preempts channel 13.

(b) *Alternate mode (128 kb/s.)* In an alternate mode of operation, each module operating at 128 kb/s preempts the second-next higher channel. For example, if the module is used in channel 6 position, it preempts channel 8; or, if it is used in channel 12 position, it preempts channel 14. If it is used in channel 23 position, it preempts channel 1. It should be noted that by-passed channels are usable by other modules.

(3) *256 kb/s strapping*. Modules can be used in channel 1 through 12 positions or odd-channel 13 through 23 positions. Using modules at 256 kb/s also preempts three additional channels. Which specific channels are preempted depends upon whether the module is strapped to operate in an adjacent or an alternate mode.

(a) *Adjacent mode (256 kb/s)*. In an adjacent mode of operation, each module operating at 256 kb/s preempts the next three higher channels. For example, if the module is being used in channel 6 position, it preempts channels 7, 8, and 9; or if it is being used in channel 12 position, it preempts channels 13, 14, and 15. If it is used in channel 23 position, it preempts channels 24, 1, and 2.

(b) *Alternate mode (256 kb/s)*. In an alternate mode of operation, each module operating at 256 kb/s preempts three higher channels, but in an alternate manner. For example, if the module is being used in channel 2 position, it preempts channels 4, 6, and 8; if it is being used in channel 11 position, it preempts channels 13, 15, and 17; or if it is being used in channel 21 position, it preempts channels 23, 1, and 3. It should be noted that the bypassed channels are usable with other modules.

(4) *512 kb/s strapping*. A module can be tested in channel 1 through 12 positions or odd channel 13 through 23 positions. Operation of modules at 512 kb/s preempts seven additional high channels. Which specific channels are preempted depends upon whether the module is strapped to operate in an adjacent or alternate mode.

(a) *Adjacent mode (512 kb/s)*. In an adjacent

mode of operation, each module operating at 512 kb/s preempts the next seven higher channels. For example, if the module is being used in channel 2 position, it preempts channels 3 through 9; if it is being used in channel 12 position, it preempts channels 13 through 19; or if it is being used in channel 21 position, it preempts channels 22, 23, 24, 1, 2, 3, and 4.

(b) *Alternate mode (512 kb/s).* In an alternate mode of operation each module operating at 512 kb/s preempts seven additional higher channels in an alternate manner. For example, if the module is being used in channel 2 position, it preempts channels 4, 6, 8, 10, 12, 14, and 16; or if it is being used in channel 15 position, it preempts channels 17, 19, 21, 23, 1, 3, and 5. Note that the bypassed channels are usable with other types of modules.

Section II. TOOLS AND TEST EQUIPMENT

3-4. General

All tools and test equipment authorized for general support maintenance are identified in this section (table 3-2). Additional information for each tool is provided by the Maintenance Allocation Chart (MAC) in TM 11-5805-711-13.

3-5. Multiplexer Test Fixture (MXTF)

Except for power supply group units, all troubleshooting and test procedures in this chapter require that the UUR be installed in an MXTF. The MXTF is a special version of Multiplexer Set AN/FCC-98(V) and is set up and operated in a manner similar to that described in TM 11-5805-711-13.

a. *MXTF Accessories*. The MXTF includes a set of extender boards and test cables (types A through N). These accessories are listed in table 3-3.

b. Use of Extender' Boards. The extender boards provided with the MXTF permit UURs to be operated under normal conditions with circuit parts accessible while they are out of the MXTF. Except for connector keys, the rear (female) connector on each extender board is the same as the plug-in connectors on the backplane of the MXTF. The A and B pins of the UUR can be accessed via the printed strips on each side of the extender boards. See figure 3-1 for typical uses of extender boards.

CAUTION

Due to the possibility of causing an electrical short by unevenly seating a module into an extender board, the MXTF power should always be turned off before the module is inserted.

Table 3-2. General Support Level Tools and Equipment

Designation	Short Form Name
Tool Kit, Electronic Equipment TK-100/G	TK-100/G
Tool Kit, PCC Repair, PACE	PCC repair kit
Tool Kit, Electronic Equipment TK-186/FRC-81 (V)	TK-186
Transmission and Noise Measuring Set TA-855/U	TA-855/U
Test Set, Telephone TS-3329/U	TS-3329/U
Oscilloscope AN/USM-281C	AN/USM-281C
Digital Frequency Counter CP-772A/U	CP-772A/U
Transmission Impairment Measuring Set HP-4940A	TIMS
Digital Multimeter ME-498-U	DMM
Digital Multimeter, Display ID-2101/U	(p/o DMM)
Multimeter AN/USM-223	AN/USM-233
Signal Generator, Wavetek Mod 142	WAVETEK 142
Test Set Data Transmission (Checktran) 350B/355/356	Checktran
Test Fixture TRW 17900-020	MXTF
Power Module Test Fixture TRW 17320-010 (includes one TRF adapter cable and shield, and two test leads for external voltage/amperage measurements)	PMTF
VICOM Test Unit Vidar 3015-01 M1	VICOM unit

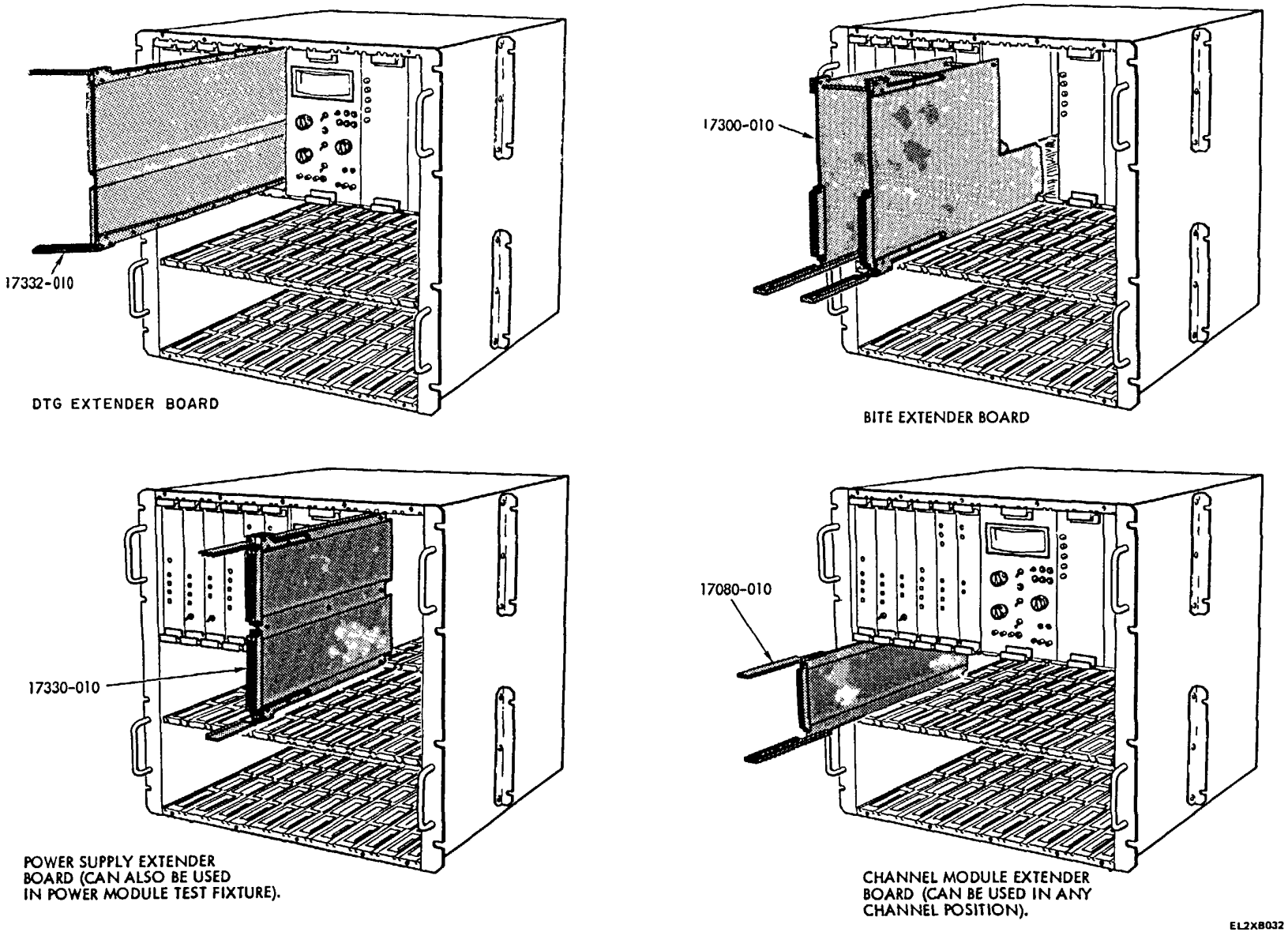


Figure 3-1. Use of extender boards.

Table 3-3. MXTF Accessories

Name	TRW part no.	Quantity
DTG Extender Board	17332-010	1
BITE Extender Board	17300-010	1
PWR SPLY Extender Board	17330-010	1
Channel Module Extender Board	17080-010	4
Type A Test Cable, Bantam to Bantam	17436-010	3
Type A Test Cable, Turret to Turret	17358-010	3
Type C Test Cable, BNC to BNC	17271-010	2
Type D Test Cable, MS Cannon 310 to Telephone 310	17272-010	1
Type E Test Cable, Telephone 310 to Telephone 310	17273-010	1
Type J Test Cable, Bantam to BNC	17277-010	1
Type L Test Cable, DB Conn to DB Conn	17279-010	1
Type M Test Cable, MS Cannon to Bantam	17269-010	1
Type N Test Cable, BNC to CLIP	17268-010	1
Power Cable, MS3126E12-3S to AC Wall Jack	17287-010	1

c. *MXTF Configuration*. The MXTF is equipped with an ac or dc power supply group, a BITE, and a data timing group, all of which are top shelf components. For troubleshooting or testing, these units can be replaced with a UUR. VF and data channel modules, either UURs or spare (known good) modules, can be installed in the two lower bays as required.

Section III. TROUBLESHOOTING

3-6. General

This section contains data and procedures for troubleshooting modules/units of the multiplexer set. The coverage for each module/unit includes a list of tools and test equipment, setup procedures or diagrams, applicable supporting data, and tabulated instructions. (Note that BITE indicators not specifically addressed in procedures should be disregarded.) Strapping options are shown in table 3-4. References to the detailed schematic diagram for each module/unit are also provided.

3-7. Initial Inspection

Before troubleshooting any module/unit, inspect it visually. Perform the inspection under good light to see that none of the following conditions exist:

a. Indication of a part having been overheated.

b. Corrosion.

c. Loose components.

d. Loose wire terminations.

e. Cracks.

Table 3-4. Module Strapping and Switch Settings

DTG STRAPPING					
Channel rate					
Channels	DRIVER and-RCVR unit strapping				
	S3-1	S3-2	S3-3	S3-4	S3-5
24	open	open	open	open	closed
12	open	open	open	closed	open
6	open	closed	open	open	open
3	open	open	open	open	open
Outgoing alarms (OGA)					
Option	DRIVER and RCVR unit strapping				
B2 = 0	S3-8 open				
B2 = 0 + 00001111	S3-8 closed				
Zero suppression					
Option	DRIVER unit strapping				
Disable	S3-6 open				
Enable	S3-6 closed				
Format					
Option	DRIVER unit module	RCVR unit strapping			
Bipolar	S2-C1	S3-7 open	S4-C1		
NRZ	S2-C2	S3-7 closed	S4-C2		

Table 3-4. Module Strapping and Switch Settings-Continued

VF MODULE STRAPPING	
Option	Strapping
-16 dBm VF input level	A strap in
+ 7 dBm VF output level	C strap in
0 dBm VF input level	B strap in
0 dBm VF output level	C strap in
Normal (balanced) E lead signaling with on-hook open and off-hook ground. F lead must be grounded in power supply by compatible E strapping.	D1 strap in

NOTE
Asynchronous 0-20 kb/s data modules have no strapping options.

50 KB/S DATA MODULE STRAPPING		
Option	Strapping	
	S1 (all sections)	S2
Balanced (78 ohms)	Closed (on)	Open (off)
Unbalanced (50 ohms)	Open (off)	Closed (on)

MULTIRATE DATA MODULE STRAPPING															
			S1 switch position					S2 switch position							
Rate kb/s	Clk	Chan use	1	2	3	4	5	1	2	3	4	5	*7	8
56	INT	ALT	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON
56	EXT	-	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON
64	INT	-	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	ON	ON
64	EXT	-	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	ON
128	INT	ALT	OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON	ON	ON	OFF
128	EXT	ALT	OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF
128	INT	ADJ	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON
128	EXT	ADJ	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON
256	INT	ALT	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	OFF
256	EXT	ALT	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON	ON	OFF	OFF
256	INT	ADJ	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON	ON
256	EXT	ADJ	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	ON
512	INT	ALT	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	ON	OFF
512	EXT	ALT	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
512	INT	ADJ	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
512	EXT	ADJ	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON

*S2-6 not used.

3-8. Troubleshooting PCM Unit

The following instructions and data are for use in troubleshooting faulty PCM units. Refer to figure FO-2 and figure 3-3 for parts location.

a. Tools and Test Equipment.

(1) TK-100/G.
(2) AN/USM-281C.
(3) DMIM.
(4) TIMS.
(5) MXTF with the following accessories:

Extender board TRW 17332-010
Spare VF module
Type C test cables (2)
Type G test cables (2)
Type A test cables (2).

b. Initial Equipment Setup. Set up test equipment and faculty PCM module as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.
(2) Strap RCVR and DRIVER units for 24-channel NRZ operation (table 3-4).
(3) Using extender board, install UUR in place of MXTF PCM unit.
(4) Connect test equipment as shown in figure 3-2.

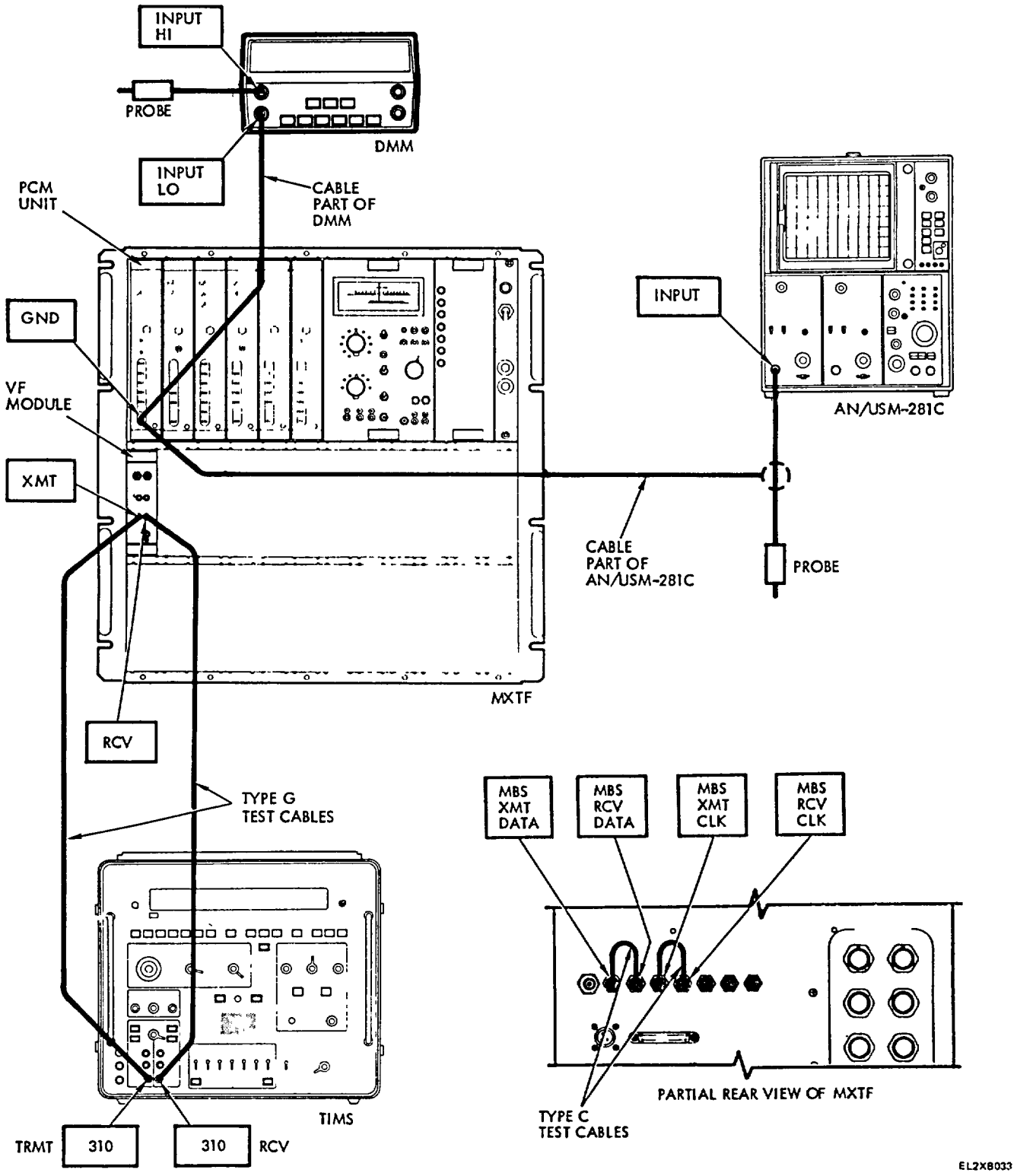


Figure 3-2. PCM unit troubleshooting setup diagram.

(5) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
AN/USM-281C	TIME/DIV	1 ms
	VOLTS/DIV	2V
	AC/GND/DC	DC
	TRIG SOURCE	LEFT
	VERT MODE	LEFT
	POWER	PULL
DMM	POWER	ON
	FUNCTION	DCV
	RANGE	10V
TIMS	SETUP CONTROLS	NORMAL TEST
		TEST WITHOUT HOLD
		TALK BATTERY OFF
		TERM 600
		NO SF SKIP
		NORMAL TEST
	MEASUREMENT	LEVEL & FREQUENCY
	DISPLAY CONNECTED TO	TRMT
	NOISE FILTER	C-MSG
	FREQUENCY CONTROL	STEP 100Hz
	RECEIVE/TRANSMIT	Down position
	JACKS switch	
	POWER	ON
	OUTPUT LEVEL	-16 dBm for A strapped VF module
		0 dBm for B strapped VF module
MXTF (PWR CONT)	Power	ON

NOTE

Allow equipment to warm up for 5 minutes before proceeding with test.

c. *Fault Location.* Troubleshoot in accordance with the following procedure to locate malfunctioning areas of the PCM unit.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
1			Check ANALOG INPUT MULTIPLEXER circuit (IC35, IC37, and IC39). If result of any check is incorrect, isolate and replace faulty component.	
	TIMS			
	STEP 100 Hz:	204 Hz	a. Check signal at IC39-8.	a. Waveform A.
			b. Move VF module to progressively higher channels, repeating a above in each. Replace VF module in channel 1.	b. Waveform A.
2			Check ODD and EVEN GROUP SAMPLE AND HOLD circuits (IC47, IC59 and IC67). If result of either check is incorrect, isolate and replace faulty component.	
			a. Check ODD GROUP SAMPLE AND HOLD circuit by checking signal at PAM ODD test point on UUR.	a. Waveform B.
			b. Move VF module to channel 2.	b. None.
			c. Check EVEN GROUP SAMPLE AND HOLD circuit by checking signal at PAM EVEN test point on UUR.	c. Waveform B.
3			Check CONVERSION CONTROL LOGIC circuit (IC2, IC12, IC21, IC22, IC23, IC33, IC42 and IC52). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	5 µs	a. Check signal at SMPL ODD test point on UUR.	a. Waveform C.
			b. Check signal at SMPL EVEN test point on UUR.	b. Waveform C.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
			c. Check signal at IC23-9.	c. Waveform D.
			d. Check signal at IC32-9.	d. Waveform E.
	TIME/DIV:	2 µs	e. Check signal at IC22-3.	e. Waveform F.
4			Check ODD and EVEN GROUPS A-D CONVERTER circuits (IC56, IC66, IC51, IC55, IC64, IC53 and IC77). If result of any check is incorrect, isolate and replace faulty component.	
	AN/ USM-281C			
	TIME/DIV:	5 µs	a. Check signal at IC53-5.	a. Waveform G.
			b. Check signal at IC53-9.	b. Waveform G.
			c. Connect jumper (not supplied) between P1-3B and TP-12. Check signal at IC65-9.	c. Waveform H.
			d. Check signal at IC55-9.	d. Waveform H.
			e. Connect a second jumper between P1-3B and TP11. Check signal at IC65-9.	e. Waveform H.
			f. Remove jumper from TP11 and connect to TP10. Check signal at IC55-9.	f. Waveform H.
			CAUTION **In the following step, remove jumpers at TP12 and TP10 ends first to prevent damage to component.**	
	TIME/DIV:	2 µs	g. Remove jumpers between TP12 and TP10 and P1-3B. Check signals at IC42-11 and IC42-8.	g. Waveform I.
	MAG:	X10 (OUT)	h. Move VF module to channel 1.	h. Waveform J.
	TRIG SOURCE:	RIGHT	Connect right probe to 24 FRAME test	
	TIME/DIV:	20 µs	point on DEMIX unit. Check signal at IC43-1. Adjust horizontal position to center waveform.	
			i. Move VF module to channel 2. Check signal at IC43-10.	i. Waveform J.
	TIME/DIV:	5 µs	j. Check signal at IC51-3.	j. Waveform K.
	MAG:	X1 (IN)		
			k. Check signal at IC51-6.	k. Waveform K.
5	AN/USM-281C		Check ODD and EVEN GROUP ZERO-IZER circuits (IC45, IC46, IC47, IC49, IC50, IC58, IC59, IC60, IC68, IC69, IC70, IC78 and IC79). If result of any check is incorrect, isolate and replace faulty com-component.	
	TIME/DIV:	50 ms		
	TRIG SOURCE:	LEFT		
			a. Connect jumper between P1-3B and TP-12. Check signal at IC47-1.	a. Waveform L. (Waveform appears as moving dot.)
			b. Check signal at IC47-7.	b. Waveform L. (Waveform appears as moving dot.)
			NOTE **Ignore any lamps which light for remainder of test.**	

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
			c. Connect a second jumper between P1-3B and TP11. Check signal at IC47-1.	c. Waveform M. (Waveform appears as a moving dot.)
			d. Remove jumper from TP11 and connect to TP10. Check signal at IC47-7. moving dot.)	d. Waveform M. (Waveform appears as a
			CAUTION **In the following step, remove jumpers at TP12 and TP10 ends first to prevent damage to component.**	
			e. Remove jumpers between P1-3B and TP12 and TP10.	e. None.
	AN /USM-281C			
	TIME/DIV:	2 µs	f. Check signal at IC78-5.	f. Waveform N.
			g. Check signal at IC49-5.	g. Waveform N.
6			Check EVEN and ODD OUTPUT CONTROL circuits (IC22, IC31, IC41, IC42, IC52 and IC71). If result of either check is incorrect, isolate and replace faulty component.	
			a. Check signal at IC42-9.	a. Waveform O.
			b. Check signal at IC42-8.	b. Waveform I.
	AN/ USM-281 C			
	TIME/DIV:	5 µs	c. Check signal at IC22-11.	c. Waveform P.
7			Check ODD and EVEN P TO VERTER circuits (IC44, IC74). If result of any check is incorrect, isolate and replace faulty component.	S CON-
	AN'/USM-281C		a. Move VF module to channel 1.	a. None.
	TRIG SOURCE:	RIGHT		
			b. Connect TIMS 310 TRMT jack to lower XMT jack of VF module.	b. None.
			c. Check signal at IC43-1.	c. Similar to waveform Q.
			d. Move spare VF module to channel 2 and repeat b and c above, checking signal at IC43-10 instead of IC43-1.	4. Similar to waveform Q.
8			Check OUTPUT MULTIPLEXER circuit (IC43 and IC52). If result of check is incorrect, replace faulty component.	
			a. Disconnect TIMS 316 TRMT jack from lower XMT jack of VF module.	a. None.
	MXTF (BITE)			
	VF FUNCTION:	LOOP	b. Connect BITE VF OSC jack to lower XMT jack of VF module in channel 2, using type A cable.	b. None.
	OSC, LEV-	As required by VF, module strapping		
	AN/USM-28C			
	TIME/DIV:	10 µs		

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
			c. Check signal at the MUX data test point on UUR.	c. Waveform R.
9			Check SIGNALING CONTROL circuit (IC1, IC11, IC21 and Q1). If results of any checks are incorrect, isolate and replace faulty component.	
	MXTF (BITE) OFF HOOK/ ON HOOK: AN/USM-281C	ON HOOK	a. Connect type A cable from SIG jack of VF module to BITE SIG jack.	a. None.
	TIME/DIV:	20 µs		
	TRIG SOURCE:	LEFT	b. Check signal at IC11-7.	b. Waveform S.
			c. Check signal at IC11-15.	c. Waveform T.
	MXTF (BITE) ON HOOK/ OFF HOOK:	OFF HOOK	d. Check signal at IC11-15.	d. Waveform U. BITE OFF HOOK lamp illuminates.
10			Check FAULT MONITOR circuit (IC61, IC62, IC63, and IC71). If result of check is incorrect, isolate and replace faulty component.	
			On UUR, press FAULT TEST switch and observe lamp conditions.	FAULT and ALL FAULT TEST lamps illuminate.

3-9. Troubleshooting MUX Unit

The following instructions and data are for use in troubleshooting faulty MUX units. Refer to figure FO-3 and figure 3-6 for parts location.

a. Tools and Test Equipment.

(1) TK-100/G.
(2) AN/USM-281C.
(3) DMM.
(4) MXTF with the following accessories:
Extender board TRW 17332-101
Type A test cables (3)
Type B test cable
Type C test cables (2)
Spare VF module
Spare 0-20 kb/s data module.

b. Initial Setup. Set up test equipment and faulty MUX unit for troubleshooting as follows:

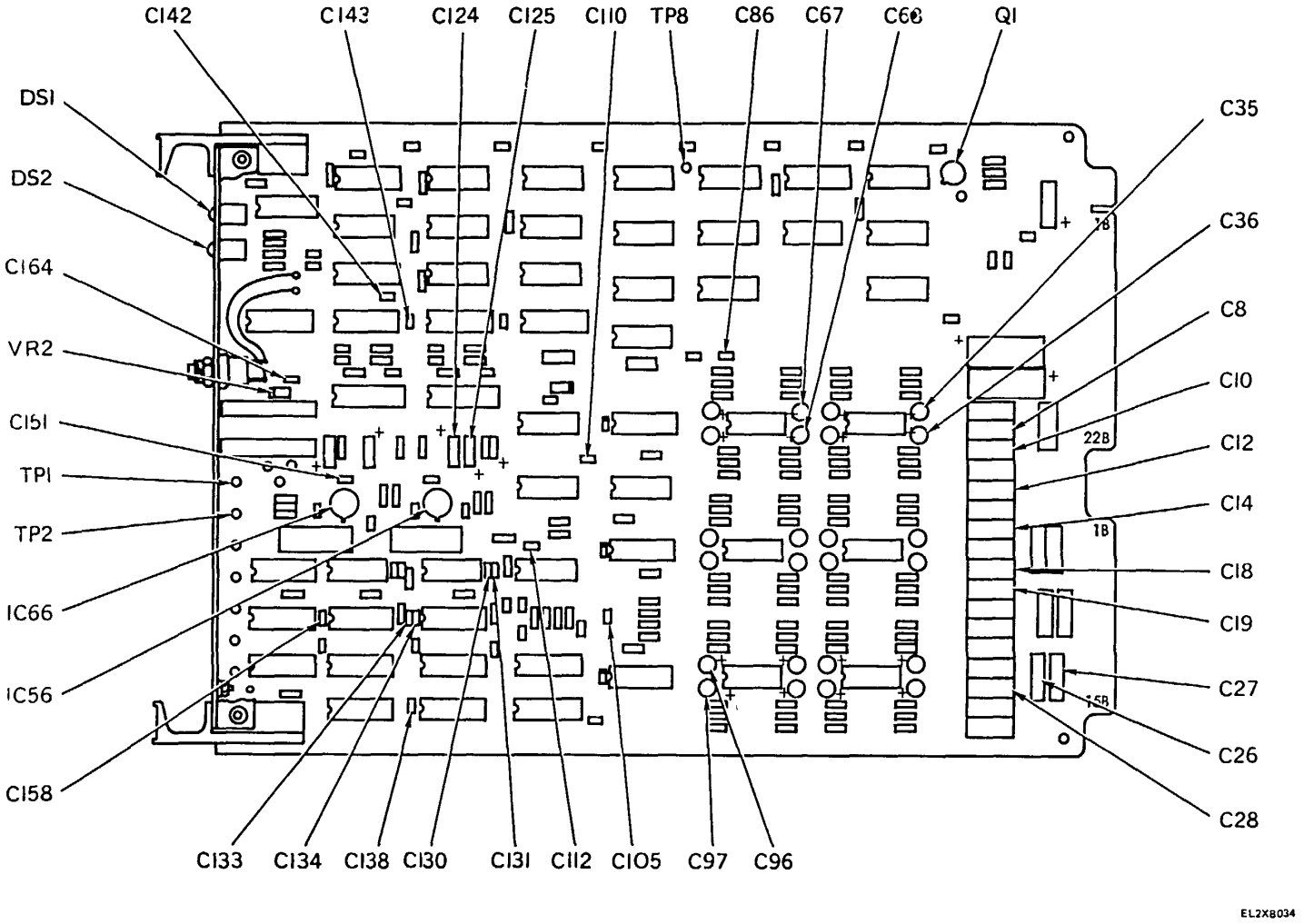
(1) Set power switch on MXTF PWR CONT unit to OFF.
(2) Remove MUX unit from MXTF and, using extender board, install UUR.
(3) Connect test equipment as shown in figure 3-5.
(4) Note whether A strap or B strap is installed in the VF module. This determines the VF input level, -16 dBm (A strap) or 0 dBm (B strap), for the module. The VF module should be installed in channel 1 position and the 0-20 kb/s data module in channel 2 position of the MXTF.
(5) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
AN/USM-281C	VOLTS/DIV (left)	2V
	VOLTS/DIV (right)	2V
	VERT MODE	LEFT
	TIME/DIV	2)s
	TRIG SOURCE	LEFT
	AC/GND/DC	EC
	POWER	Pull
MXTF (PWR CONT)	Power	On

NOTE

Allow equipment to warm up for 5 minutes before proceeding with test.

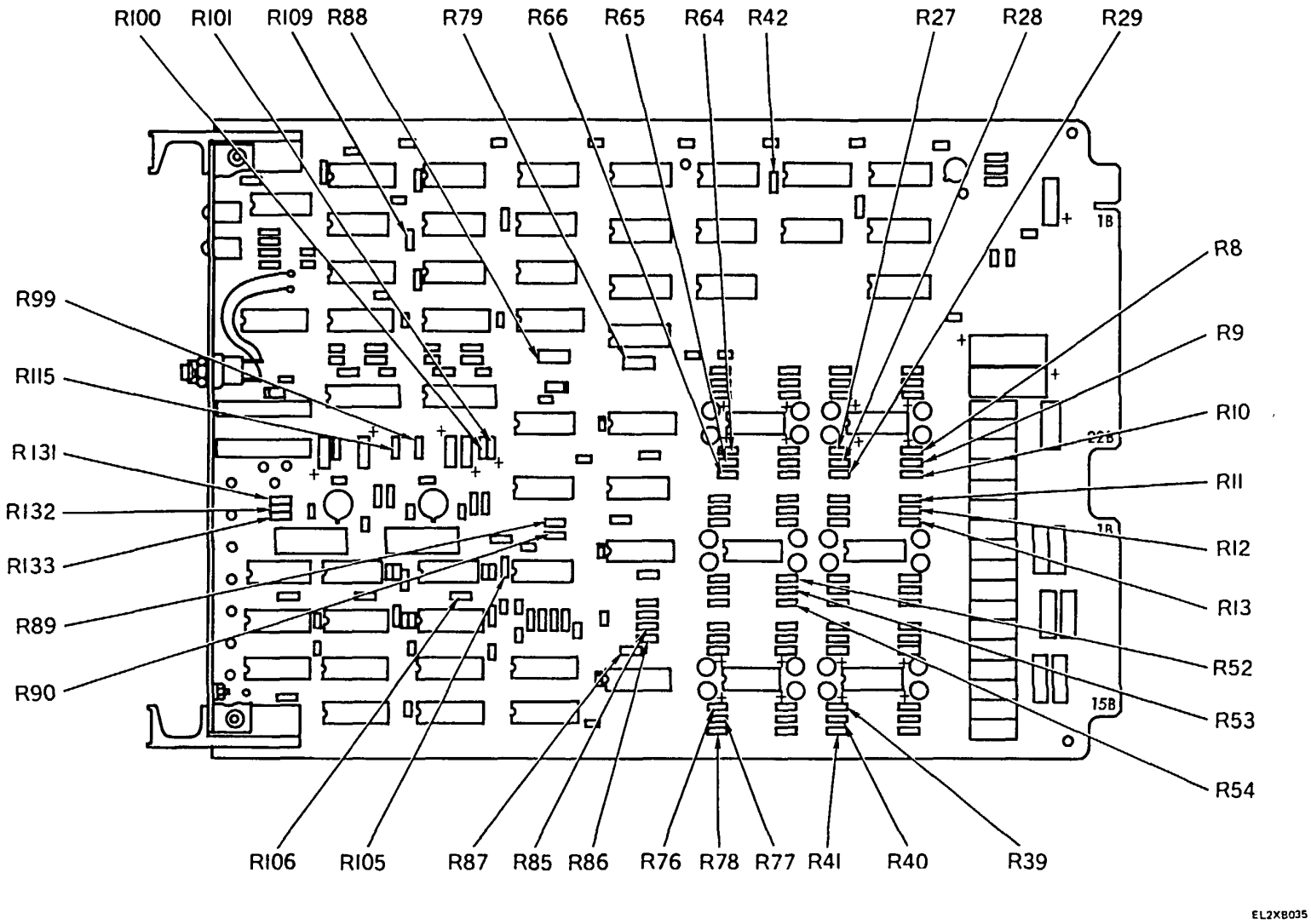
c. Fault Location. Troubleshoot in accordance with the following procedure to locate malfunctioning areas of the MUX unit.



NOTE:

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, ASIDE OPPOSITE.

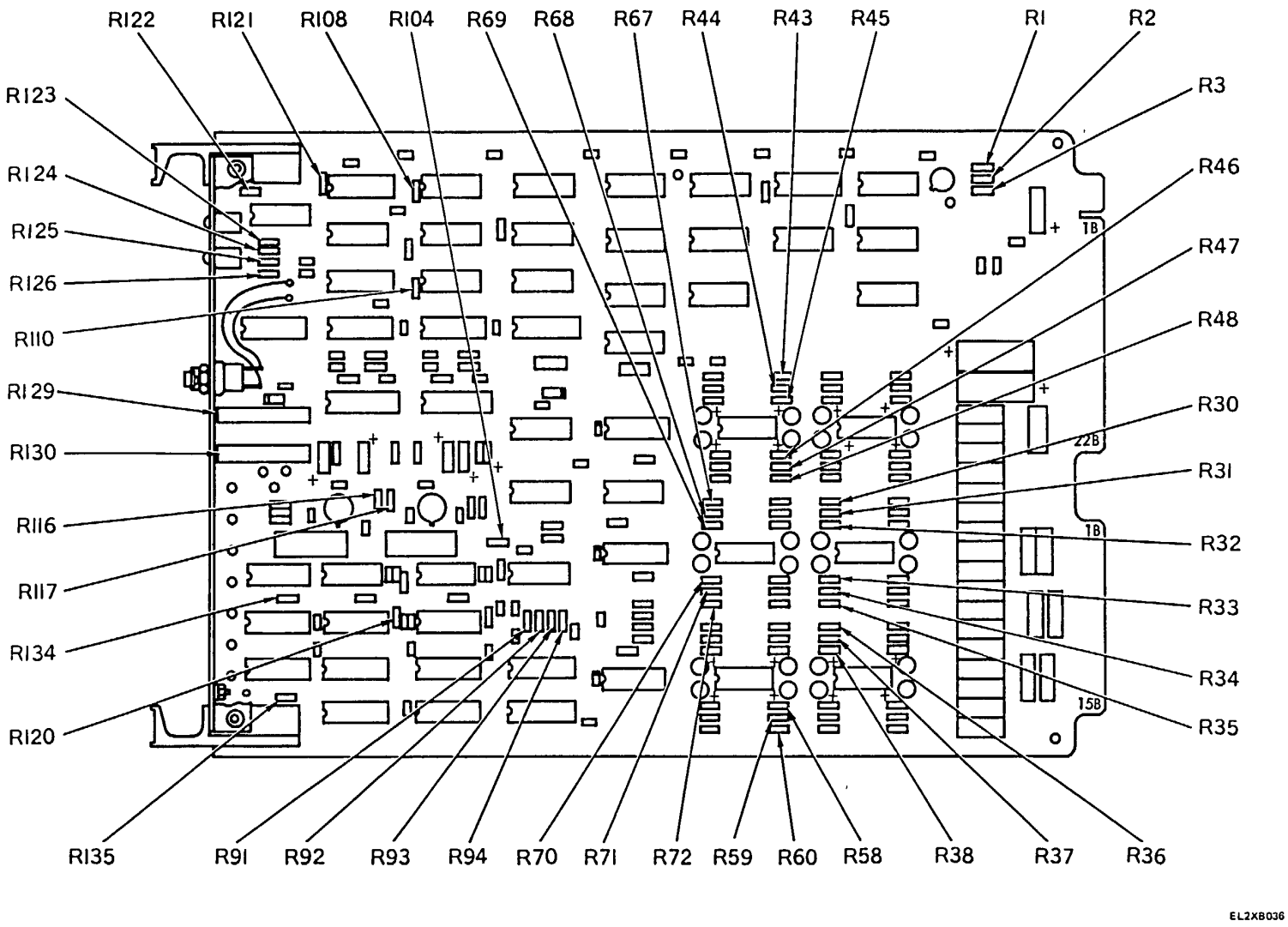
Figure 3-3. PCM unit parts location diagram (sheet 1 of 14) PCM02 and PCM04.



NOTE:

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A SIDE AND 158-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

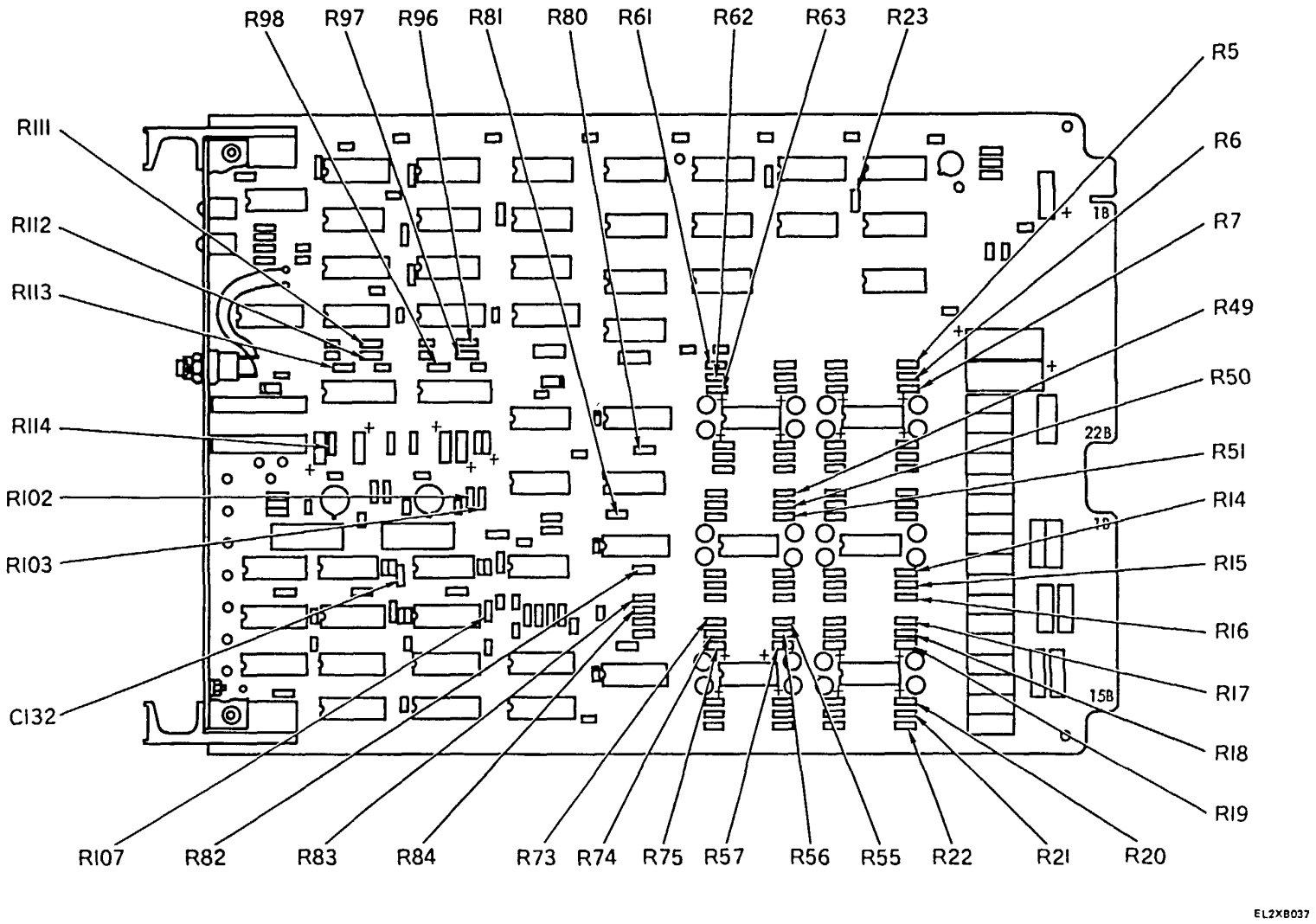
Figure 3-3. PCM unit parts location diagram (sheet 2 of 14) PCM02 and PCM04.



NOTE:

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

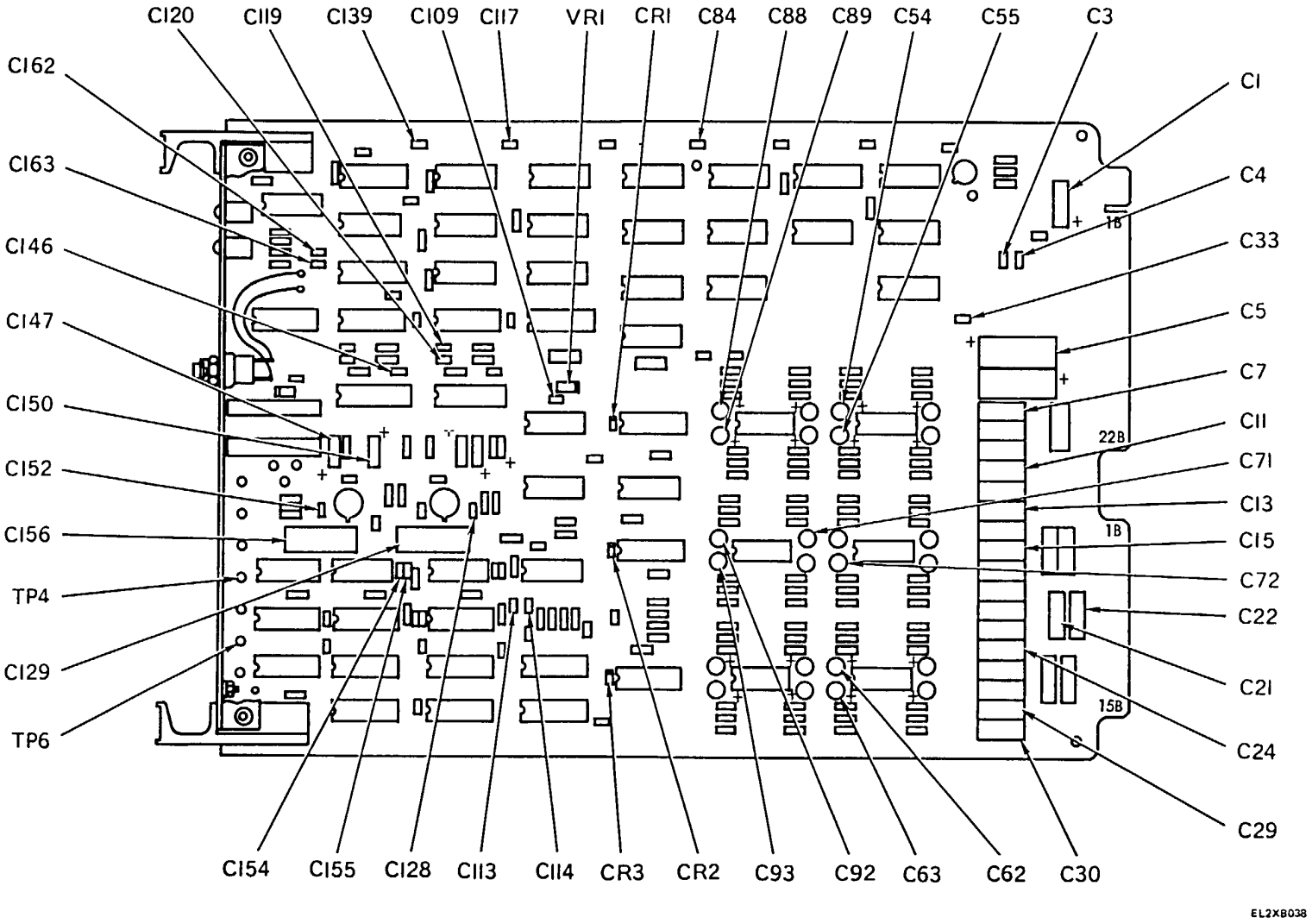
Figure 3-3. PCM unit parts location diagram (sheet 3 of 14) PCM02 and PCM04.



NOTE:

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

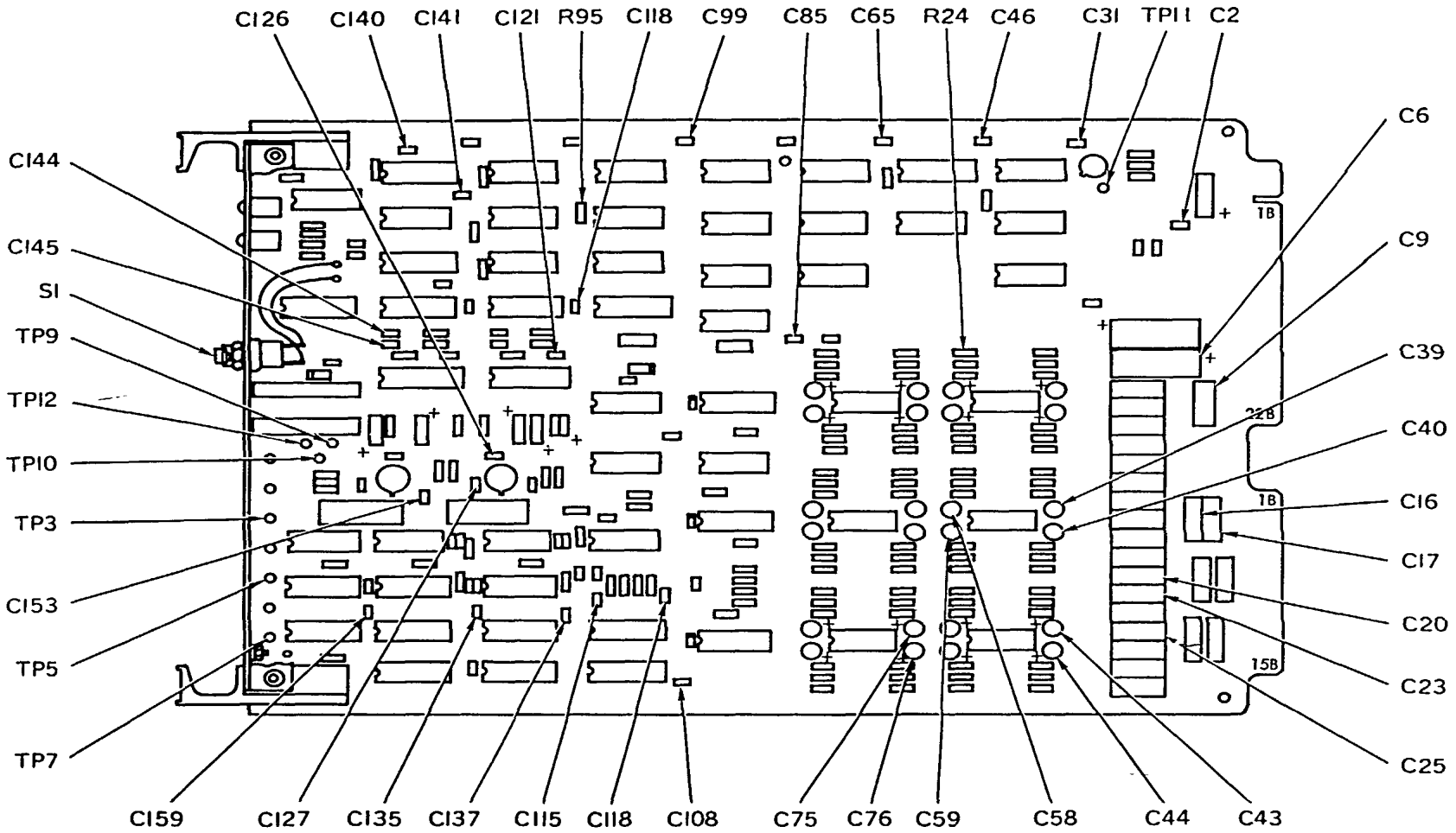
Figure 3-3. PCM unit parts location diagram (sheet 4 of 14) PCM02 and PCM04.



NOTE:

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

Figure 3-3. PCM unit parts location diagram (sheet 5 of 14) PCM02 and PCM04.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2X8039

Figure 3-3. PCM unit parts location diagram (sheet 6 of 14) PCMos and PCM04.

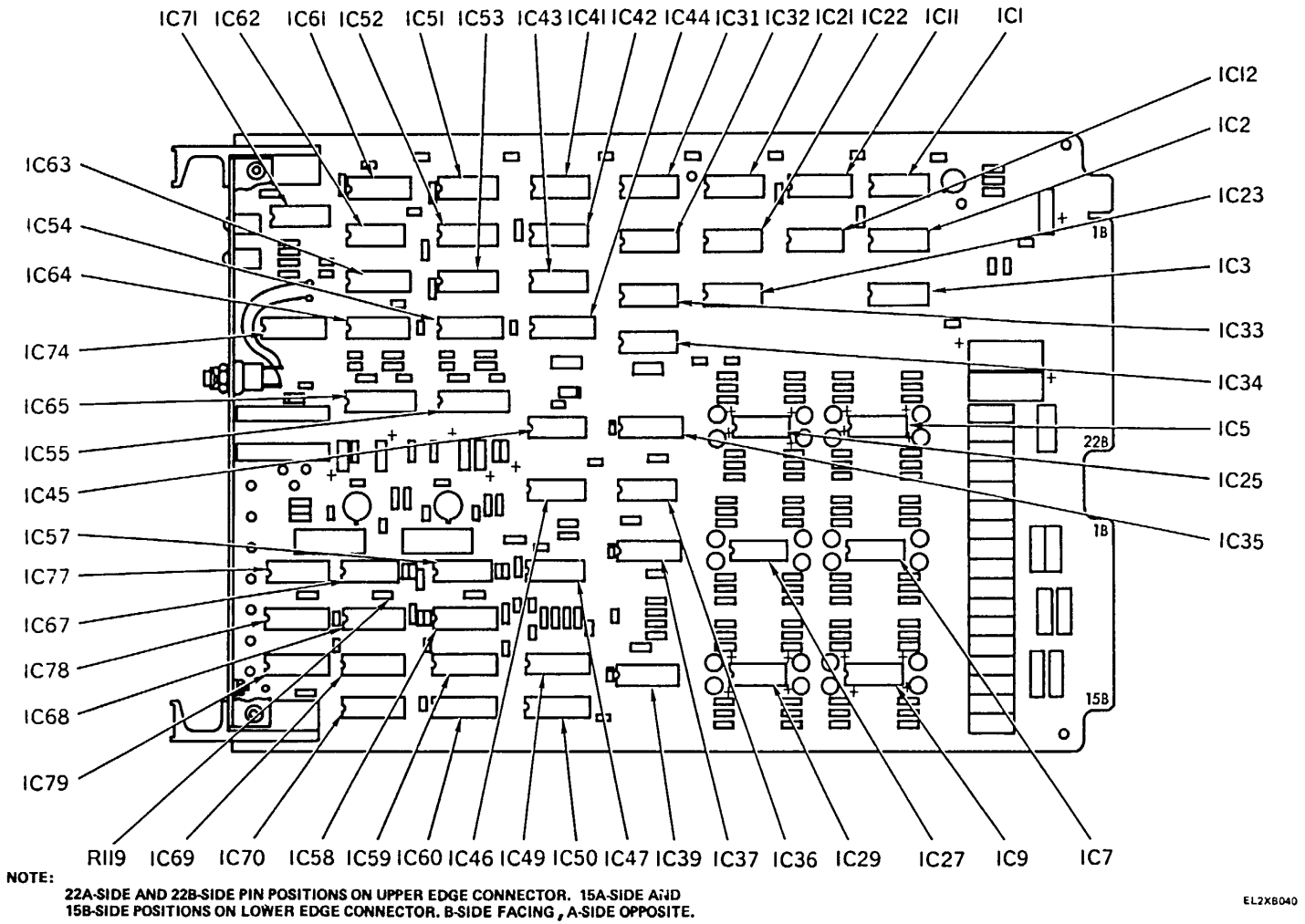
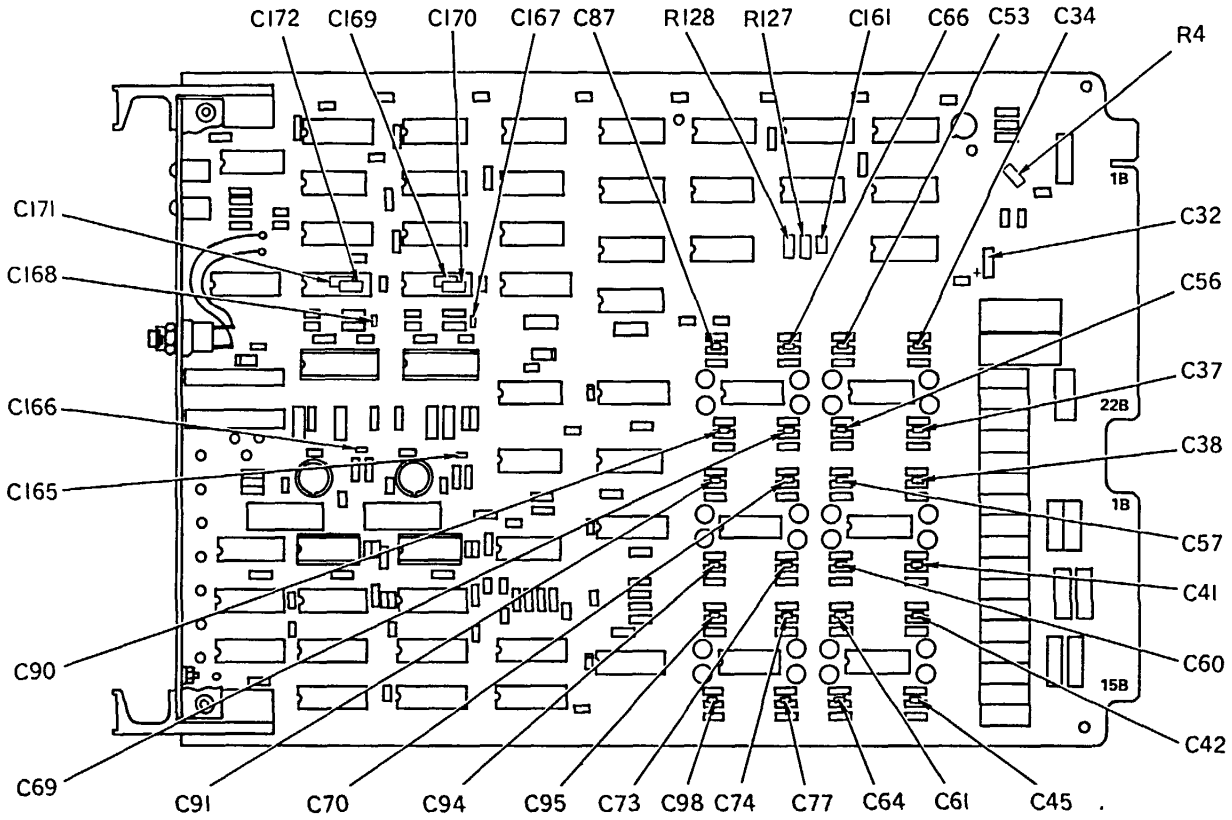


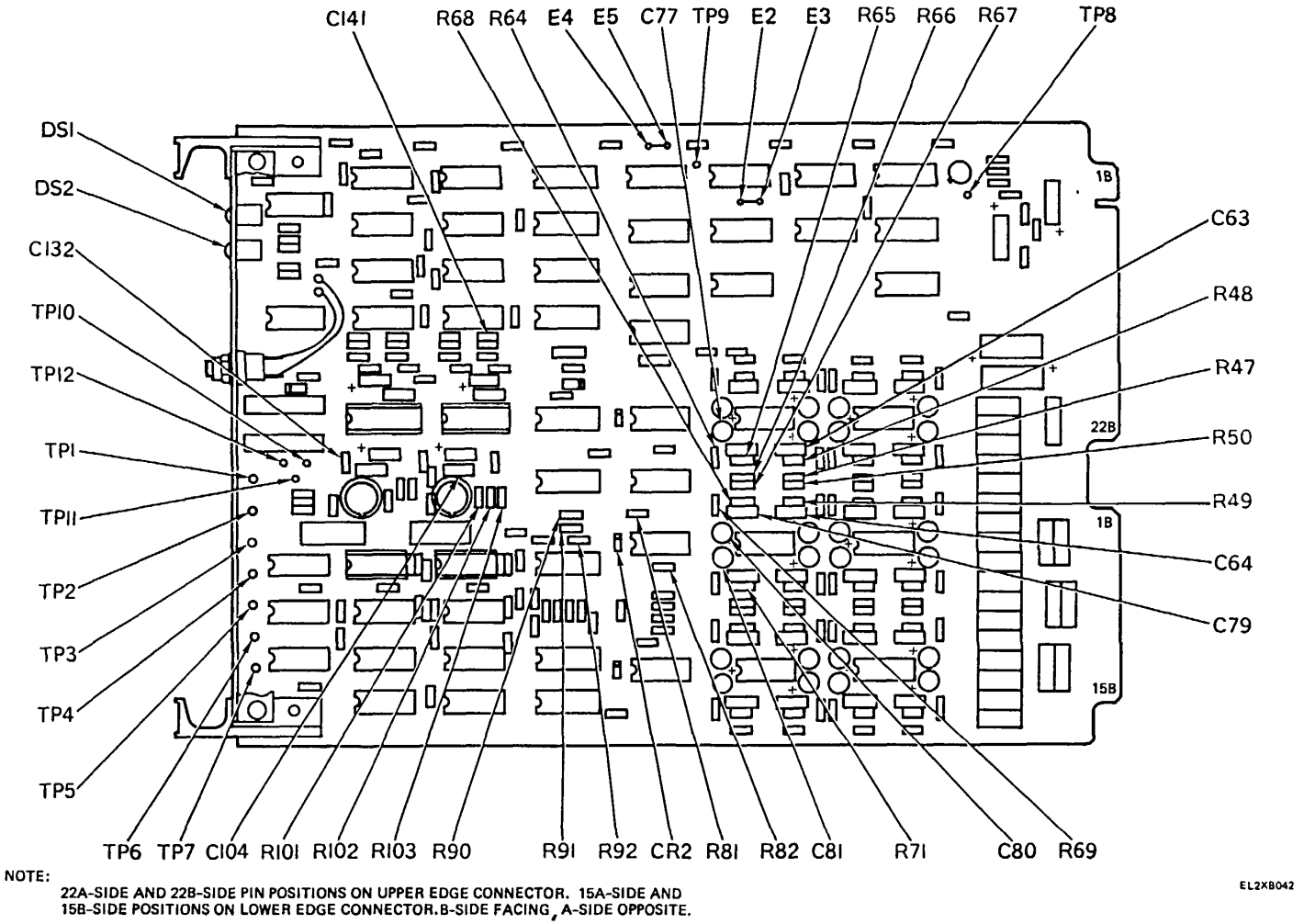
Figure 3-3. PCM unit parts location diagram (sheet 7 of 14) PCM02 and PCM04.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2X8041

Figure 3-3. PCM unit parts location diagram (sheet 8 of 14) PCM02 and PCM04.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR.B-SIDE FACING, A-SIDE OPPOSITE.

Figure 3-3. PCM unit parts location diagram (sheet 9 of 14) PCM06.

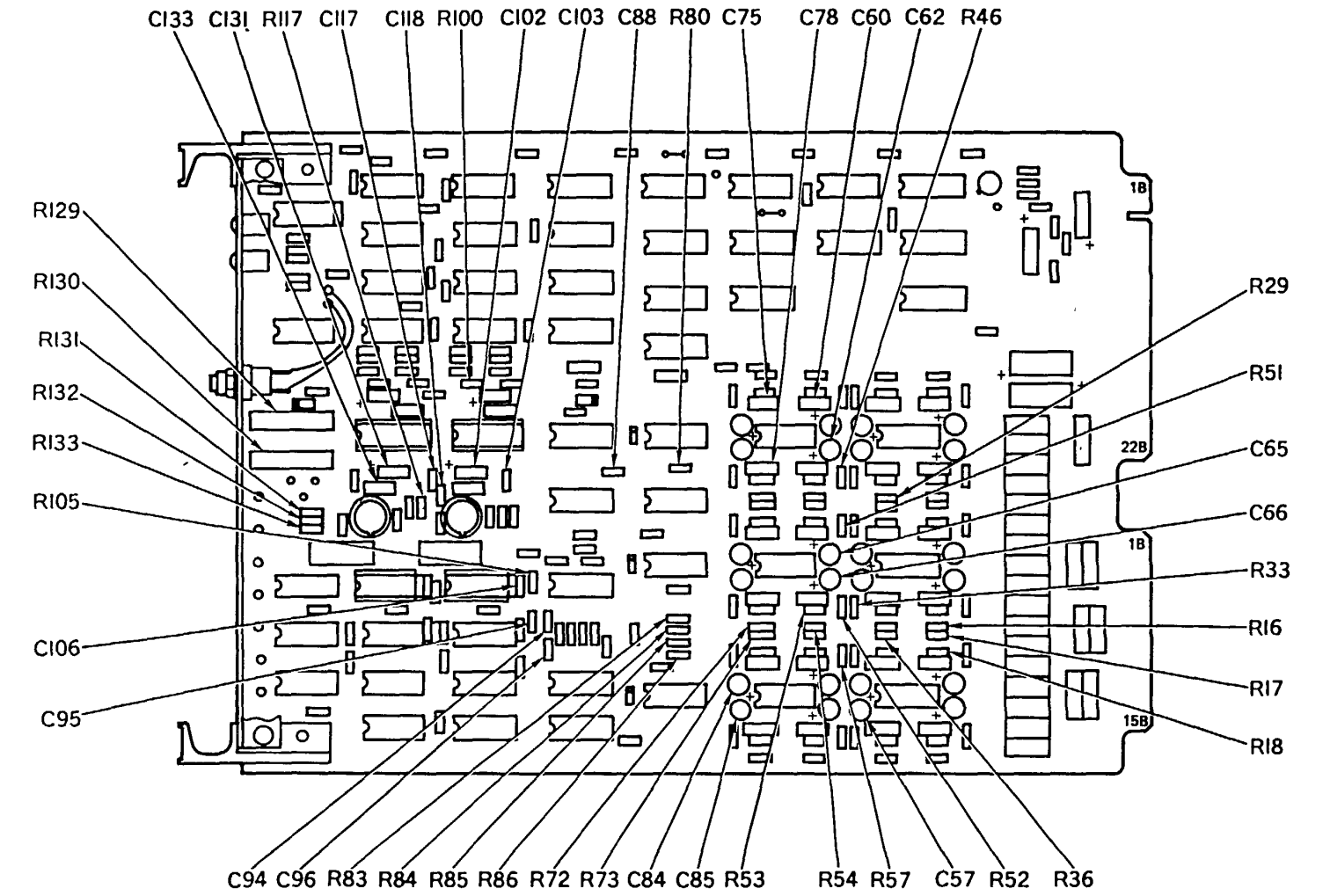


Figure 3-3. PCM unit parts location diagram (sheet 10 of 14) PCM06.

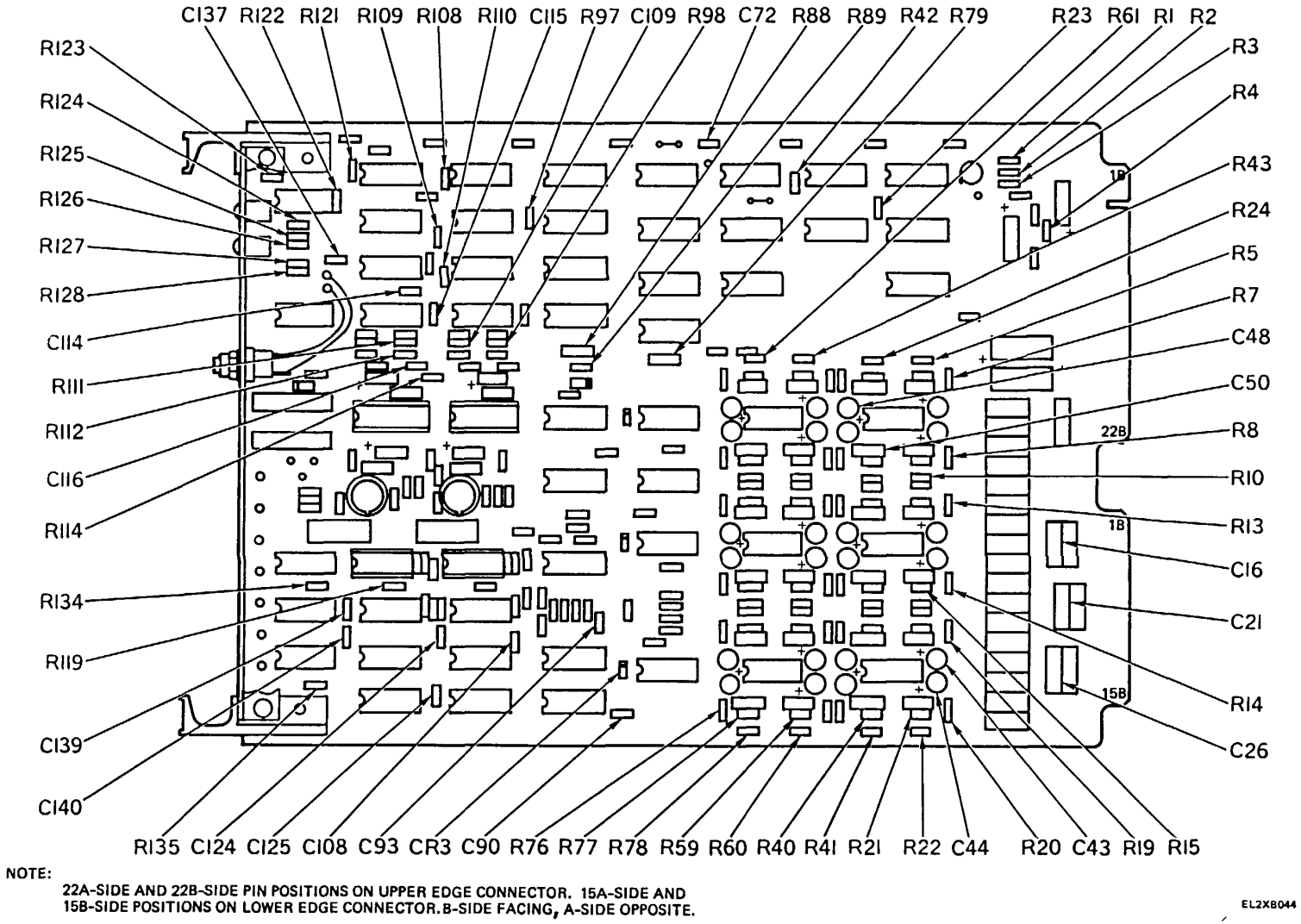


Figure 3-3. PCM unit parts location diagram (sheet 11 of 14) PCM06.

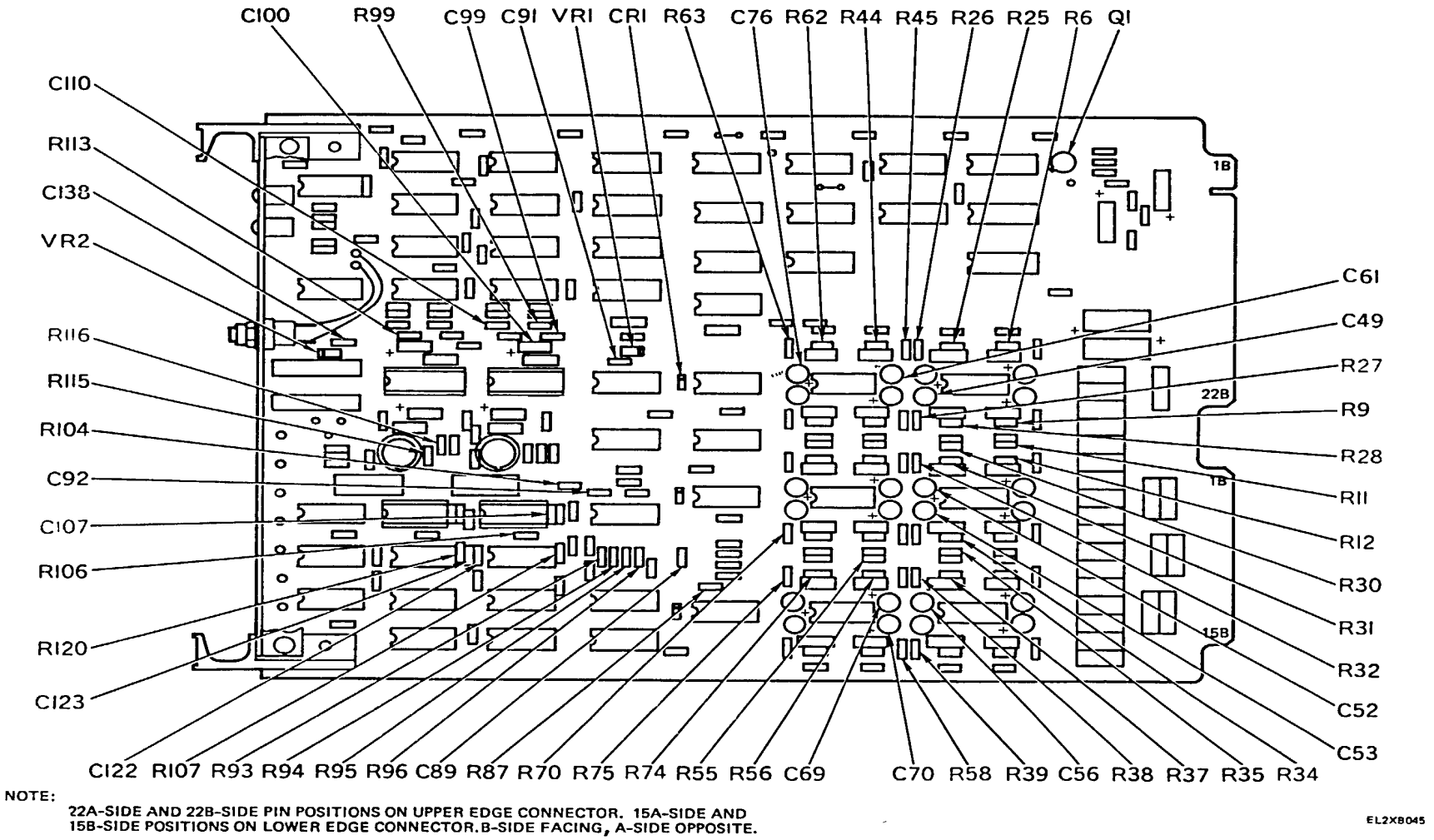
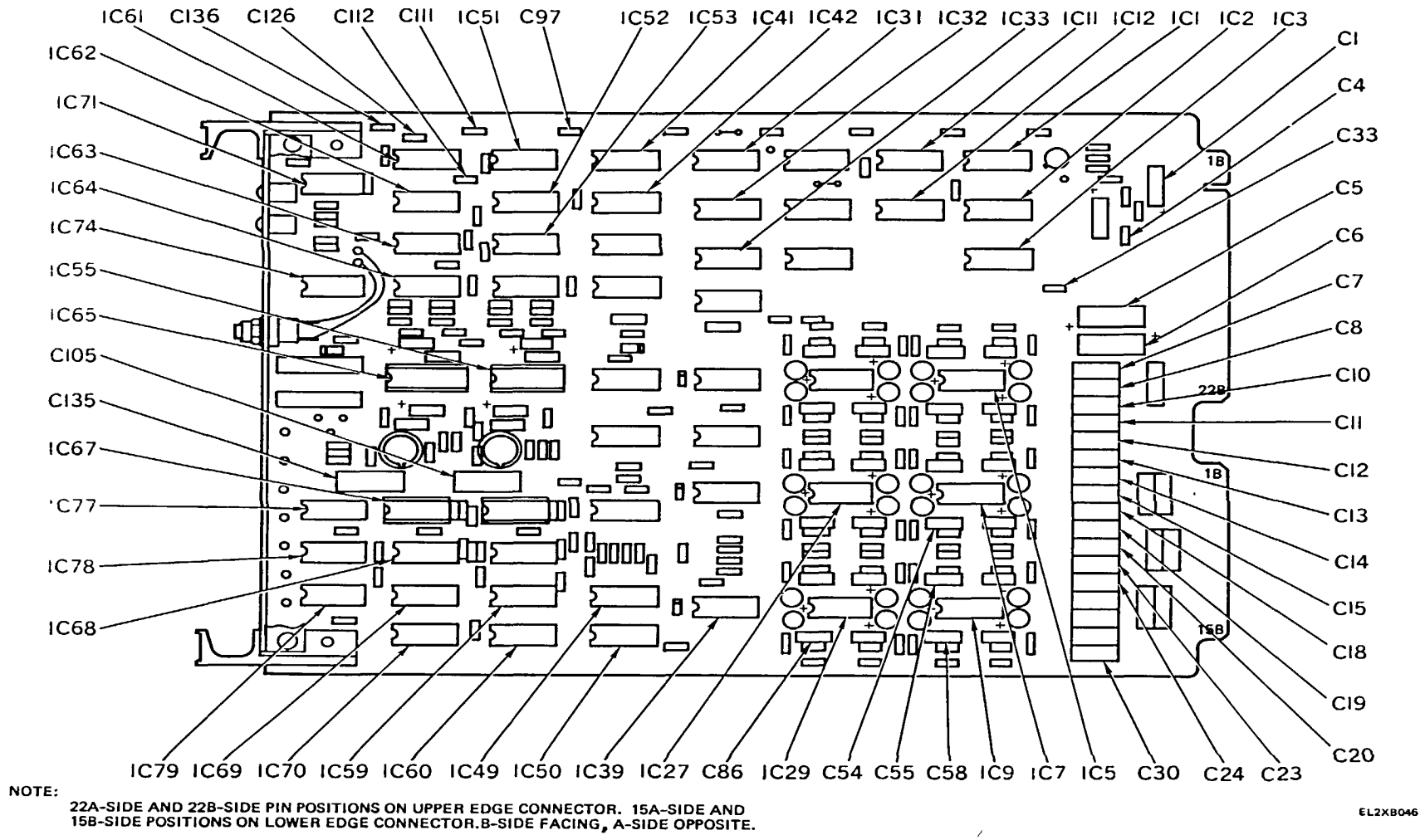


Figure 3--3. PCM unit parts location diagram (sheet 12 of 14) PCM06.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR.B-SIDE FACING, A-SIDE OPPOSITE.

Figure 3-3. PCM unit parts location diagram (sheet 13 of 14) PCM06.

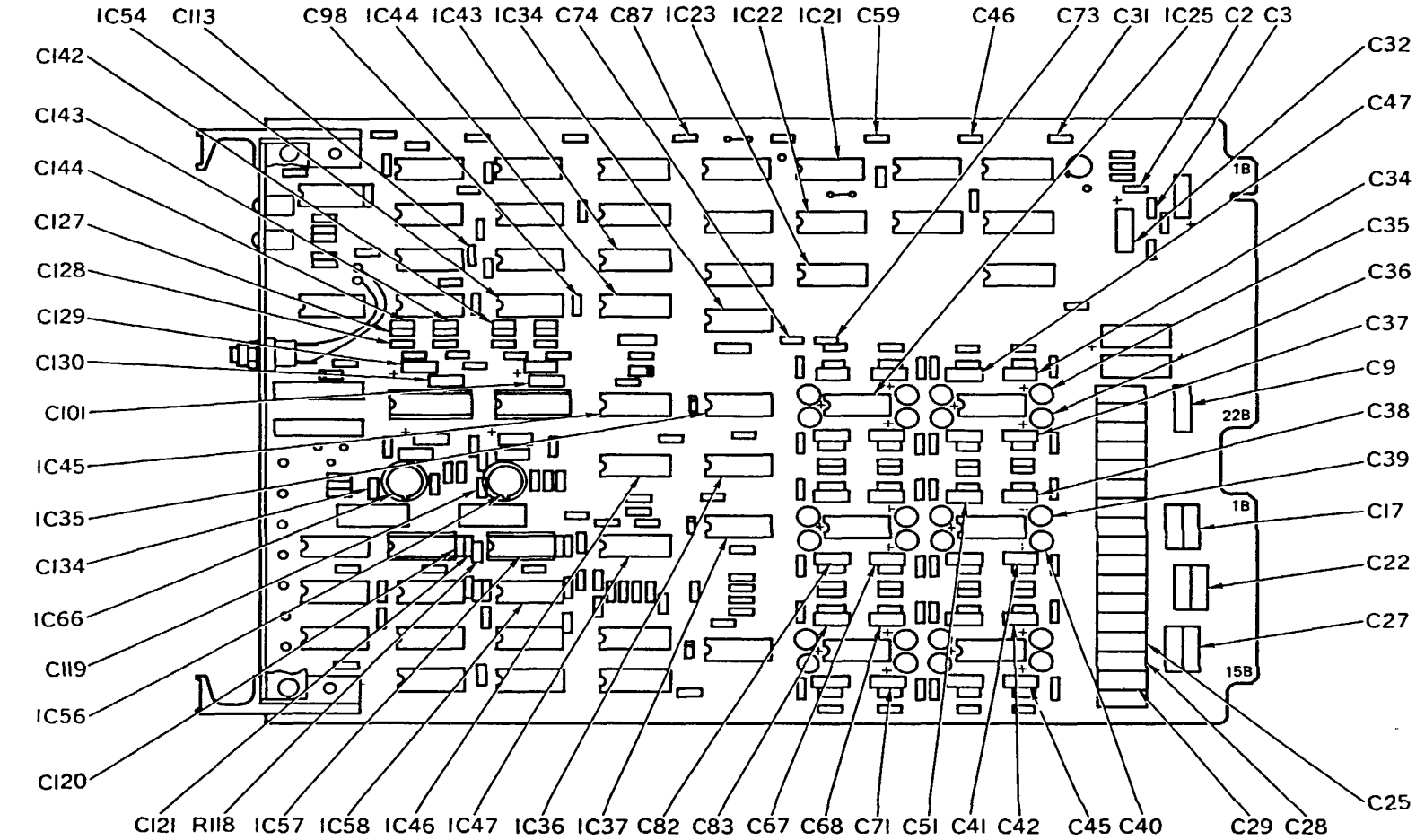


Figure 3-3. PCM unit parts location diagram (sheet 14 of 14) PCM06.

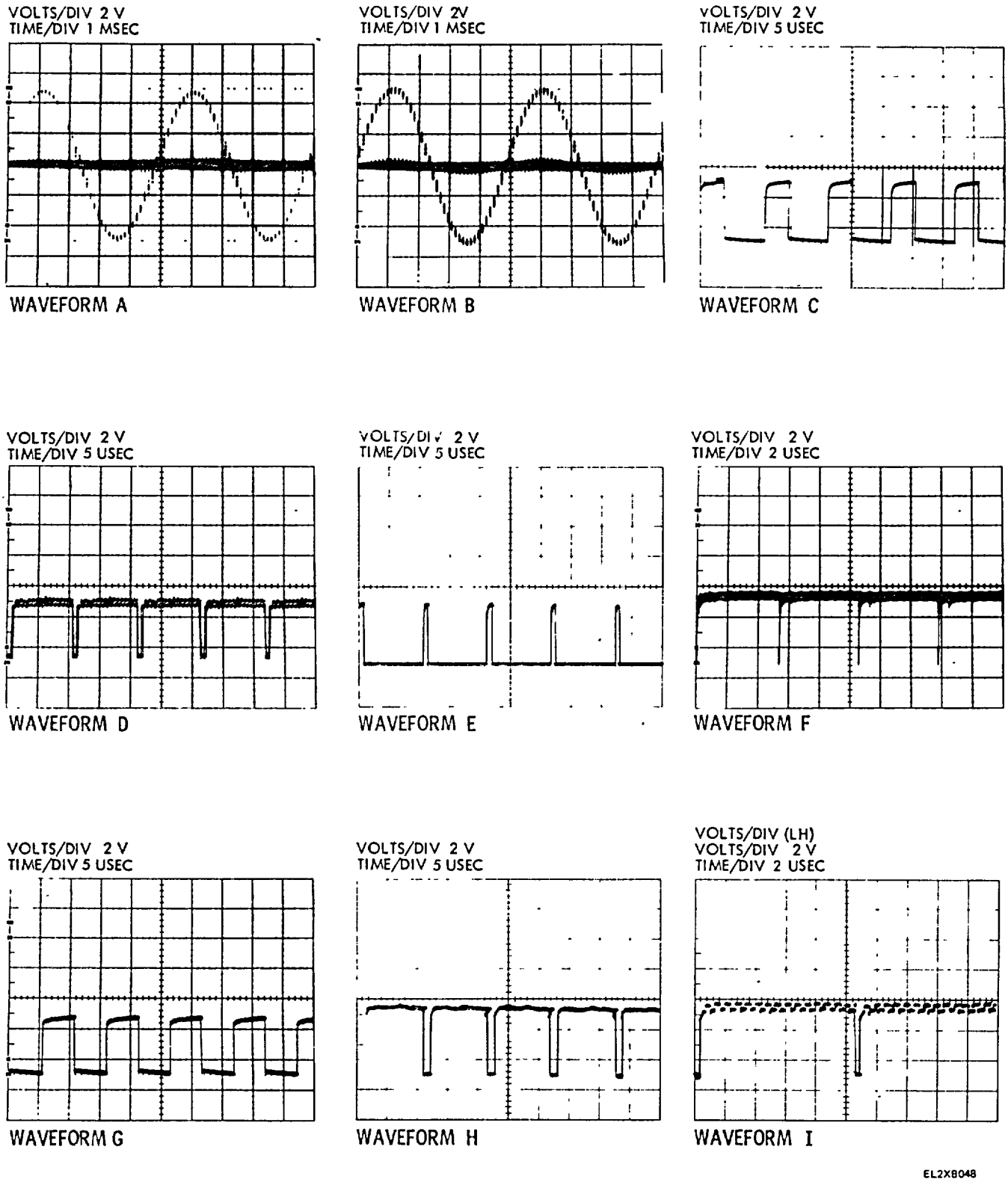


Figure 3-4. PCM unit troubleshooting waveforms (sheet 1 of 5).

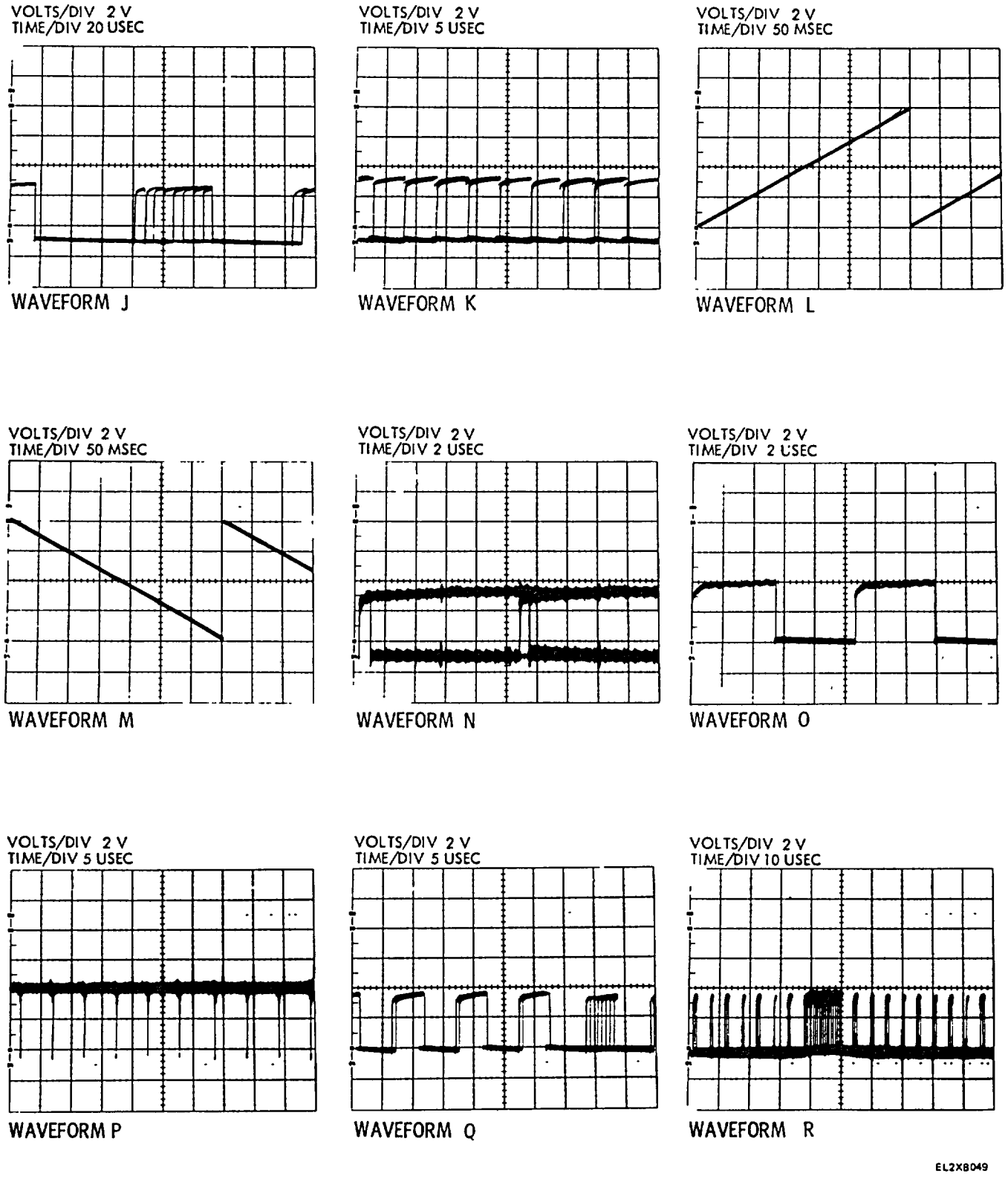


Figure 3-4. PCM unit troubleshooting waveforms (sheet 2 of 3).

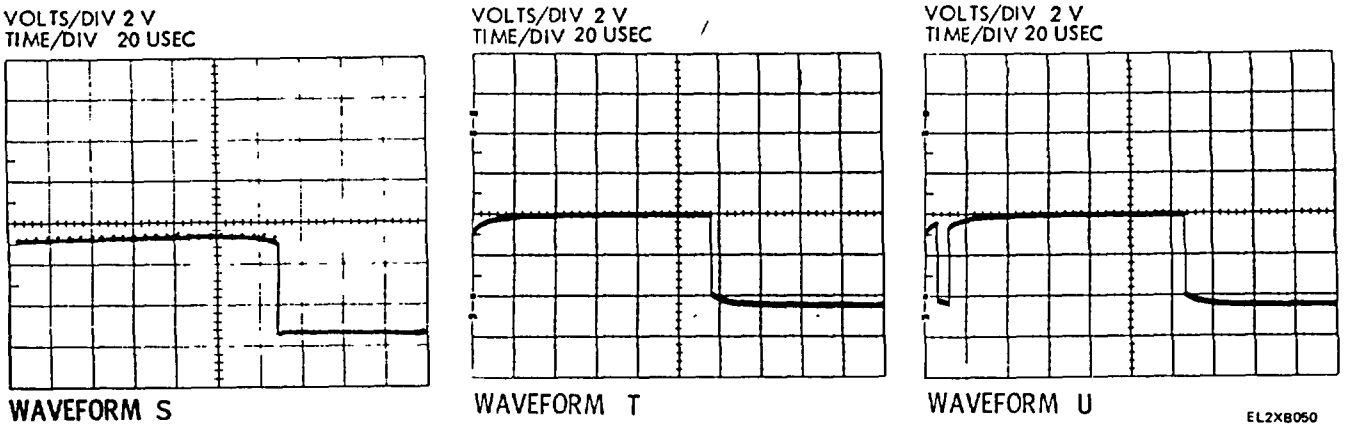


Figure 3-4. PCM unit troubleshooting waveforms (sheet 3 of 3).

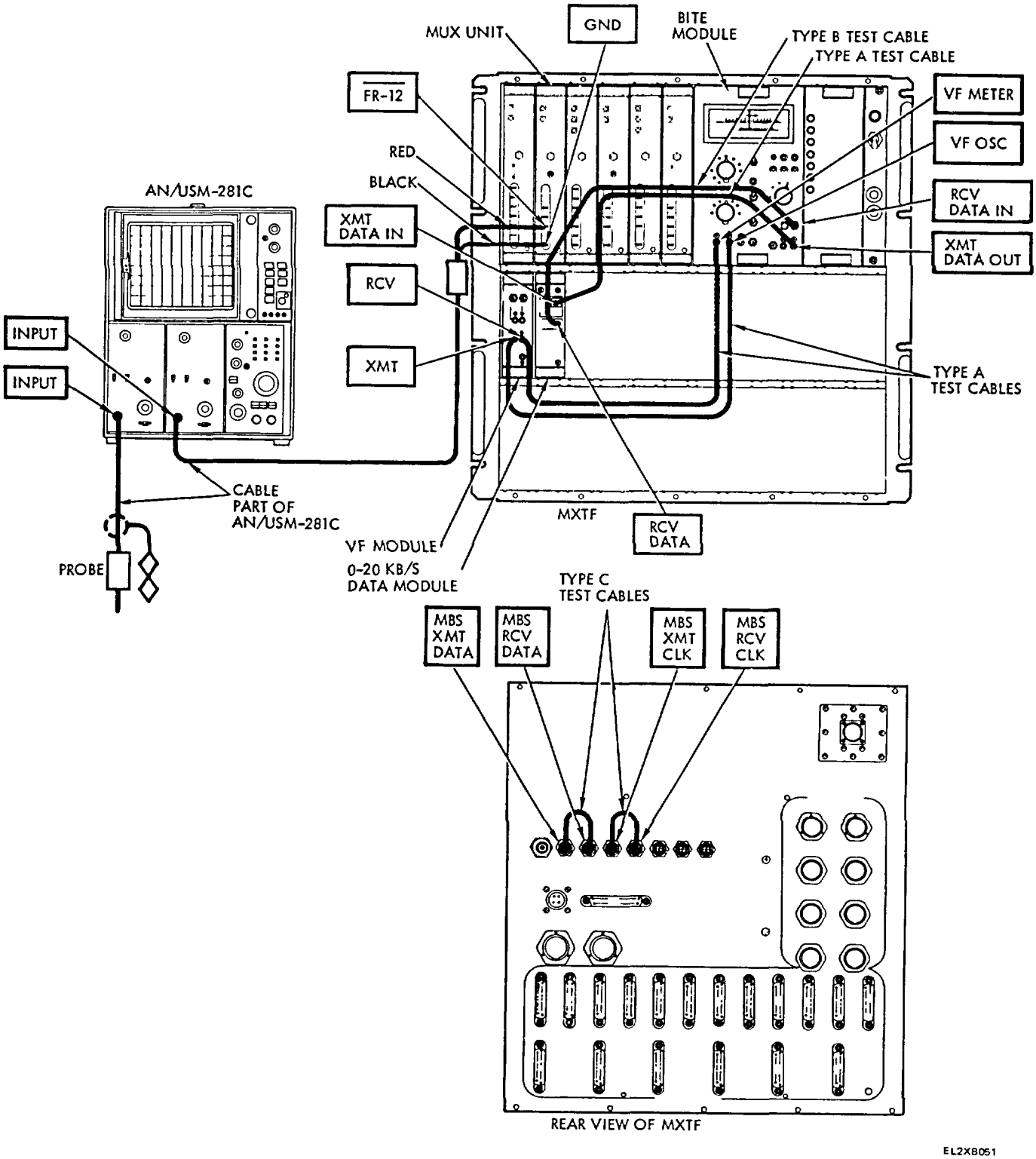


Figure 3-5. MUX unit troubleshooting setup diagram.

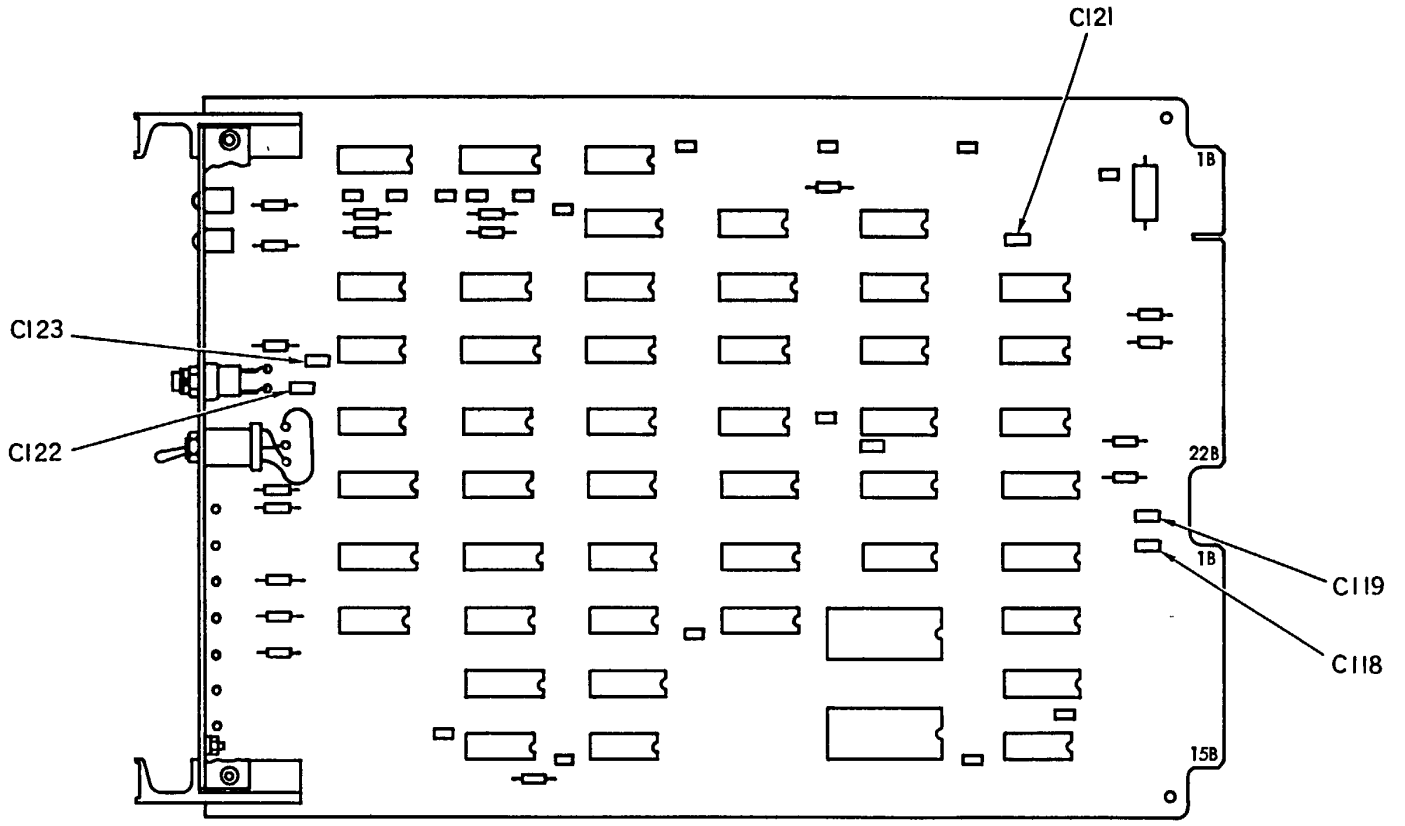
Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-7
1			Check MBC clock functions (IC4 and IC5). If result of any check is incorrect, isolate and replace faulty component.	
			a. Check signal at IC5-4.	*a.* Waveform A.
			b. Check signal at IC5-6.	*b.* Waveform A.
			c. Check signal at IC4-12.	*e.* Waveform A.
2			Check bit counter functions (IC27). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-2S1C			
	TIME/DIV:	5 µs	*a.* Check signal at IC27-14.	*a.* Waveform B.
	TIME/DIV:	1 µs	*b.* Check signal at IC27-13.	*b.* Waveform C.
	TIME/DIV:	2 µs	*c.* Check Qc output signal at IC27-12.	*c.* Waveform D.
3			Check channel counter functions (IC10, IC17, and IC27). If result of any check is incorrect, isolate and replace faulty component.	
			a. Check channel counter EC2 output signal at IC10-6.	*a.* Waveform E.
	AN/USM-281C			
	TIME/DIV:	10 µs	*b.* Check channel counter EC21 output signal at IC10-4.	*b.* Waveform F.
	TIME/DIV:	20 µs	*c.* Check channel counter EC2' output signal at IC10-2.	*c.* Waveform G.
	TIME/DIV:	50 µs	*d.* Check channel counter EC2' output signal at IC10-8.	*d.* Waveform H.
			e. Check channel counter EC2' output signal at IC10-10.	*e.* Waveform I.
4	AN/USM-281C		Check CHANNEL COUNTER DECODE	
	TIME/DIV:	10 µs	circuit (IC6, IC7, IC8, IC9, IC18 and	
	TRIG SOURCE:	RIGHT	IC19). If result of any check is incorrect, isolate and replace faulty component.	
			NOTE **The negative-going pulse in the waveform should move about 8 µsec to the right as the channel numbers increase.**	
			a. Connect right probe of AN/USM-281C to IC6-2.	*a.* None.
			b. Check $\overline{\text{XMT CH CTR 1}}$ at signal IC6-2.	*b.* Waveform J.
			c. Check $\overline{\text{XMT CH CTR 2}}$ signal at IC6-5.	*c.* Similar to waveform J.
			d. Check $\overline{\text{XMT CH CTR 3}}$ signal at IC6-7.	*d.* Similar to waveform J.
			e. Check $\overline{\text{XMT CH CTR 4}}$ signal at IC6-10.	*e.* Similar to waveform J.
			f. Check $\overline{\text{XMT CH CTR 5}}$ signal at IC6-12.	*f.* Similar to waveform J.
			g. Check $\overline{\text{XMT CH CTR 6}}$ signal at IC-15.	*g.* Similar to waveform J.
			h. Connect right probe of AN/USM-281C to IC7-2. Check $\overline{\text{XMT CH CTR 7}}$ signal at IC7-2.	*h.* Similar to waveform J.
			i. Check $\overline{\text{XMT CH CTR 8}}$ signal at IC7-5.	*i.* Similar to waveform J.
			j. Check $\overline{\text{XMT CH CTR 9}}$ signal at IC7-7.	*j.* Similar to waveform J.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-7
			k. Check XMT CH CTR 10 signal at IC7-10.	*k.* Similar to waveform J.
			l. Check XMT CH CTR 11 signal at IC7-12.	*1.* Similar to waveform J.
			m. Check XMT CH CTR 12 signal at IC7-15.	*m*. Similar to waveform J.
			n. Check XMT CH CTR 13 signal at IC8-2.	*n.* Similar to waveform J.
			o. Check XMT CH CTR 14 signal at IC8-5.	*o.* Similar to waveform J.
			p. Check XMT CH CTR 15 signal at IC8-7.	*p.* Similar to waveform J.
			q. Check XMT CH CTR 16 signal at IC8-10.	*q.* Similar to waveform J.
			r. Check XMT CH CTR 17 signal at IC8-12.	*r.* Similar to waveform J.
			s. Move right probe to IC8-15. Check XMT CH CTR 18 signal at IC8-15.	*s.* Similar to waveform J.
			t. Check XMT CH CTR 19 signal at IC9-2.	*t.* Similar to waveform J.
			u. Check XMT CH CTR 20 signal at IC9-5.	*u.* Similar to waveform J.
			v. Check XMT CH CTR 21 signal at IC9-7.	*v.* Similar to waveform J.
			w. Check XMT CH CTR 22 signal at IC9-10.	*w.* Similar to waveform J.
			x. Check XMT CH CTR 23 signal at IC9-12.	*x.* Similar to waveform J.
			y. Check XMT CH CTR 24 signal at IC9-15.	*y.* Similar to waveform J.
5	AN/USM-281C		Check XMT DATA BUS CLK function at	*W*aveform K.
	TRIG SOURCE:	LEFT	IC3-12. If result of check is incorrect,	
	TIME/DIV:	5 µs	isolate and replace faulty component.	
6			Check end of frame function (IC15). If result of any check is incorrect, replace faulty component.	
	AN/USM-281C		*a*. Check signal at IC15-6.	*a.* Waveform L.
	TIME/DIV:	50 µs	*b*. Restrap DRIVER and RCVR units for 3-channel mode (table 3-4). Check signal at IC15-6.	*b*. Waveform AH.
	TIME/DIV:	50 µs	*c*. Restrap DRIVER and RCVR units for 6-channel mode (table 3-4). Check signal at IC15-6.	*c.* Waveform AI.
	TIME/DIV:	20 µs	*d*. Restrap DRIVER and RCVR units for 12-channel mode (table 3-4). Check signal at IC15-6.	*d.* Waveform N.
7			Check BIT COUNTER DECODE circuit (IC16, IC26, IC28, IC46, IC55, IC56, and IC67). If result of any check is incorrect, isolate and replace faulty component.	
			a. Restrap DRIVER and RCVR units for 24-channel mode (table 3-4).	*a.* None.
	AN/USM-281C			
	TIME/DIV:	5 µs	*b*. Check SD1+SD2 at IC57-4.	*b*. Waveform L.
	TIME/DIV:	1 µs	*c.* Check SD6+SD7 at IC57-7.	*c.* Waveform M.
	TIME/DIV:	20 µs	*d.* Check CH2 signal at IC56-14.	*d.* Waveform N.
	TIME/DIV:	1 µs	*e.* Check XMTADV CH CTR signal at IC3-10.	*e.* Waveform M.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-7
			f. Check SD7+SD8 at IC58-8.	*f.* Waveform M.
			g. Check SD7+SD8 at IC14-10.	*g.* Waveform M.
8			Check CHANNEL COUNTER CONTROL & RESET circuit (IC12, IC15, IC16, and IC25). If result of either check is incorrect, isolate and replace faulty component.	
	AN/ USM-281C			
	TIME/DIV:	20 µs	*a.* Check XMT RESET TO CH 1 signal at IC3-2.	*a.* Waveform O.
			b. Check CCLK at IC16-15.	*b*. Waveform O.
9			Check ZERO SUPPRESS circuit (IC4, IC5, IC1l (Note), IC14, IC24, IC35, IC36, IC45, IC46 and IC55). If result of any check is incorrect, isolate and replace faulty component.	
			NOTE **IC11 is used in configuration MUX04 only.**	
	MXTF (PWR CONT)			
	Power	OFF	*a.* Remove PCM unit from MXTF.	*a.* None.
			b. Connect jumper wire (not supplied) between P3-3A and P3-12A on UUR.	*b*. None.
			c. Strap DRIVER unit for 24-channel, zero suppress operation and RCVR for 24-channel operation.	*c.* None.
			d. Remove type A test cable from XMT DATA IN jack on 0-20 kb/s data module.	*d.* None.
			NOTE **Ignore any fault lamps which are illuminated for the remainder of step 9.**	
	MXTF (PWR CONT)			
	Power	ON		
	AN/USM-281C			
	TRIG SOURCE:	RIGHT		
	TIME/DIV:	50 µs	*e*. Connect right probe of AN/USM-281C to FR12 test point on UUR and check signal at IC35-6.	*e.* Waveform P.
			f. Check signal at IC45-8.	*f.* Waveform P.
			g. Check zero suppressor output signal at IC35-9.	*g.* Waveform P.
	MXTF (PWR CONT)			
	Power	OFF	*h*. Remove jumper installed in b above.	*h.* None.
			i. Connect type A test cable (previously disconnected in d above) to XMT DATA IN jack on 0-20 kb/s data module.	*i.* None.
			j. Reinstall the PCM unit removed in a above.	*j.* None.
10			Verify 1 KHZ DIGITAL TONE GENERATOR circuit (IC13, IC22, IC23 and IC34). If result of any check is incorrect, isolate and replace faulty component.	
	MXTF (PWR CONT)			
	Power	ON		
	AN/USM-281C			
	TIME/DIV:	50 µs	*a.* Check 1 kHz shift register load pulse at IC34-5.	*a.* Waveform R.
	TRIG SOURCE:	LEFT		
	TIME/DIV:	.5 ms	*b*. Check counter output signal at IC22-5.	*b*. Waveform Q.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-7
	TIME/DIV:	2 µs	*c*. Check 1 KHZ DIGITAL TONE GENERATOR output at IC23-7.	*c.* Waveform S.
11			Verify VOICE/ZERO SUPPRESS/1 KHZ TONE MUX circuit (IC24, IC31, IC46). If result of any check is incorrect, isolate and replace faulty component.	
			a. Connect right probe of AN/USM-281C to FR12.	*a.* None.
	AN/USM-281C			
	TRIG SOURCE:	RIGHT	*b*. Check VOICE/DATA/1 KHZ MUX	*b*. Waveform T.
	TIME/DIV:	5 µs	output signal at IC24-8.	
	UUR			
	1KHZ TONE:	ON for step	*c.* Check VOICE/DATA/1 KHZ MUX output signal at IC24-8.	*c.* Waveform U.
12	Check 24 channel FRAME		PATTERN GENERATOR function (IC28, IC38, IC39, IC40, IC48, IC58). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USAI-281C			
	TIME/DIV:	.2 ms	*a.* Check counter output signal at IC39-11.	*a.* Waveform V.
	TIME/DIV:	.5 ms	*b*. Check 24 channel frame pattern output signal at IC40-6.	*b*. Waveform W.
			c. Check XMT FRAME 6+12 signal at P3-15B.	*c.* Waveform X.
			d. Check FR-12 test point on front panel of UUR.	*d.* Waveform Y.
			e. Check signal at FR BIT PATT test point on UUR.	*e.* Waveform Z.
13			Check 3-6-12 channel FRAME PATTERN GENERATOR function (IC22, IC25, IC28, IC37, IC38, IC47, IC48, IC58, IC40). If result of any check is incorrect, isolate and replace faulty component.	
			a. Strap DRIVER and RCVR units for 3-channel operation (table 3-4).	*a.* None.
	AN/ USM-281 C			
	TIME/DIV:	.5 ms	*b.* Check frame pattern signal at IC37-3.	*b*. Waveform AA.
			c. Check reset signal at IC47-1.	*c.* Waveform AB.
	TRIG SOURCE:	LEFT	*d.* Check polarity signal at IC22-9.	*d.* Waveform AC.
	TIME/DIV:	1 ms		
	TRIG SOURCE:	RIGHT	*e.* Check clear pulse signal at IC28-2.	*e.* Waveform AD.
	TIME/DIV:	.2 ms	*f.* Check frame bit enable signal at IC37-6.	*f.* Waveform AE.
14			Check DATA/VOICE/FRAME MUX circuit (IC32). If result of either check is incorrect, isolate and replace faulty component.	
	AN/USM-221C			
	TIME/DIV:	.5 ms	*a*. Check framing bit pattern signal at FR BIT PATT test point on UUR.	*a.* Waveform AF.
	TIME/DIV:	50 µs	*b*. Check XMT MBS DATA signal at XMT MBS DATA test point on UUR.	*b*. Waveform AG.
15			Check ACTIVITY MONITOR circuit (IC41, IC51, IC53, IC54). If result of check is incorrect, isolate and replace faulty component.	

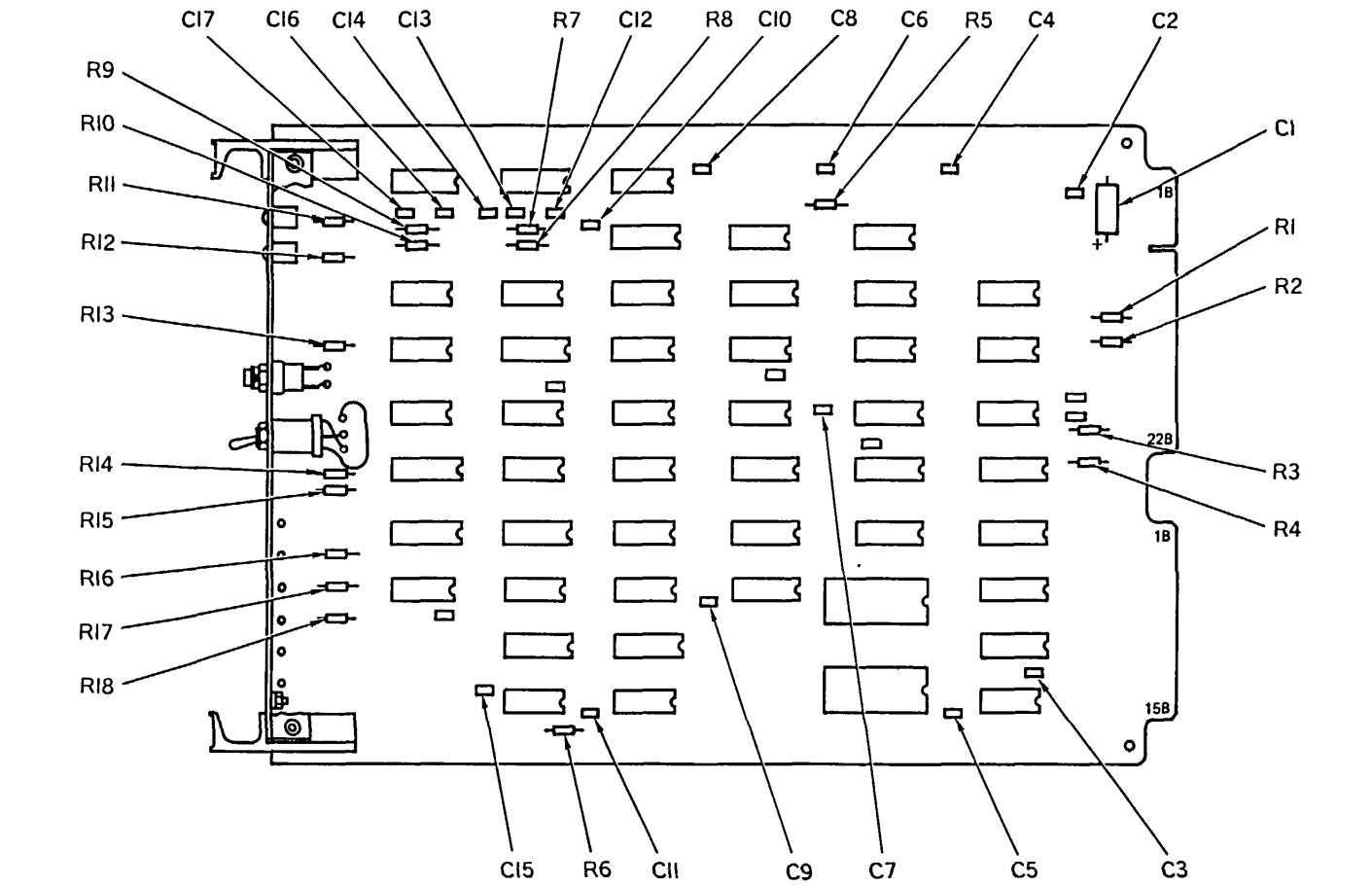
Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-7
			Press FAULT TEST button on UUR and observe lamp conditions.	*MXTF (PWR SPLY)* FAULT lamp illuminates. *UUR* FAULT lamp illuminates. ALL FAULT TEST lamp illuminates.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB062

Figure 3-6. MUX unit parts location diagram (sheet 1 of 5) MUX02.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB063

Figure 3-6. MUX unit parts location diagram (sheet 2 of 5) MUX02, MUX04 and MUX06.

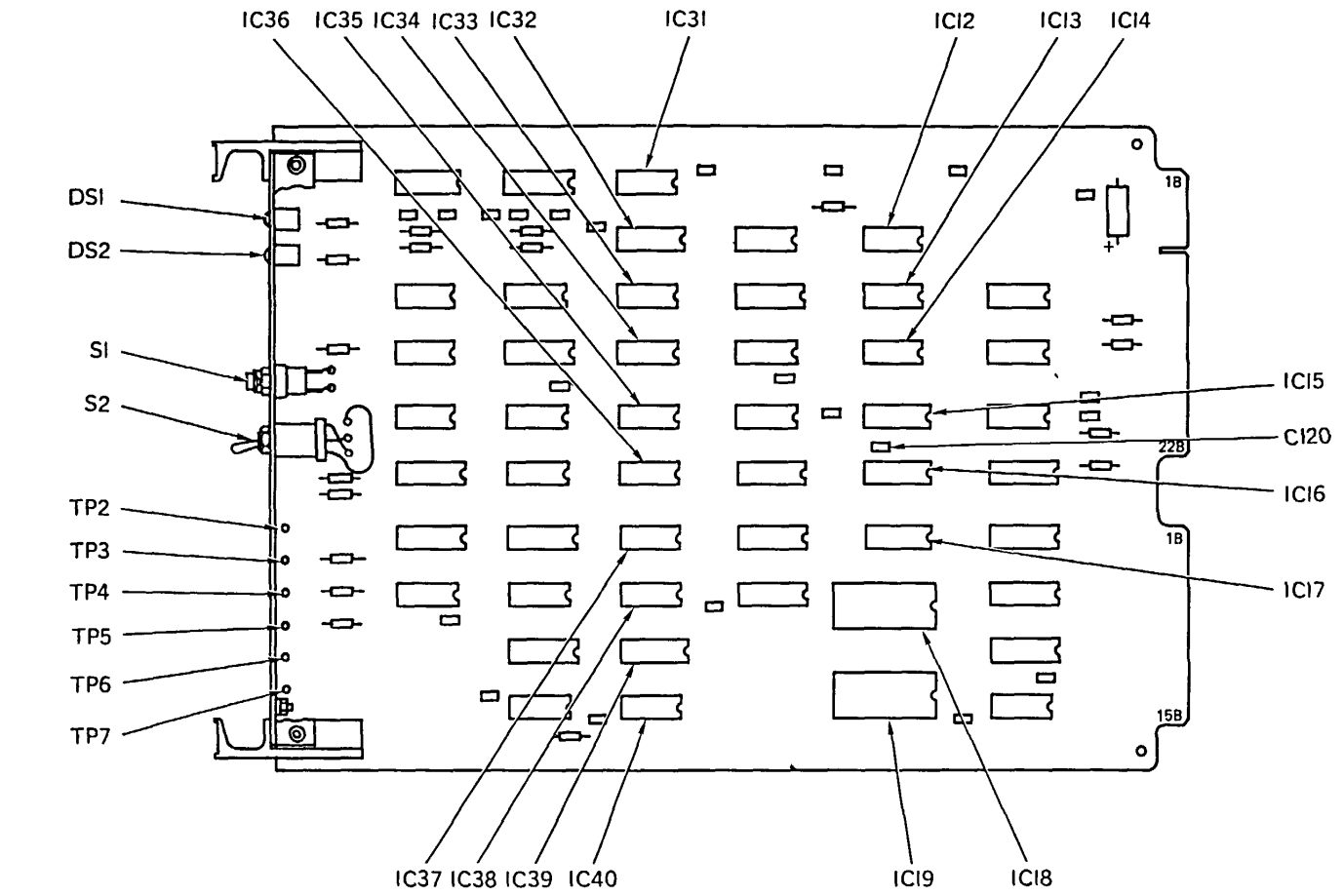


Figure 3-6. MUX unit parts location diagram (sheet 3 of 5) MUX02, MUX04 and MUX06.

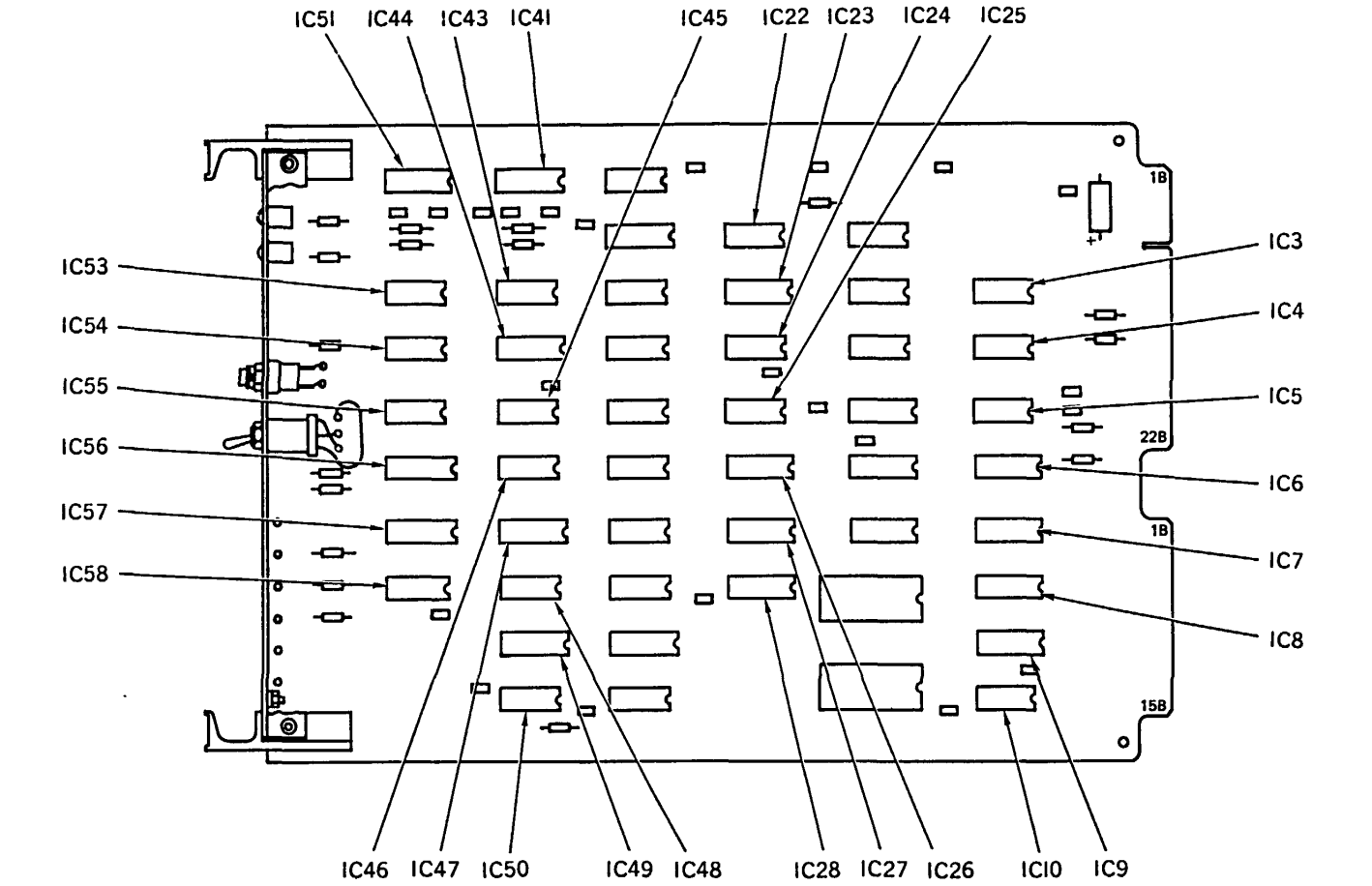
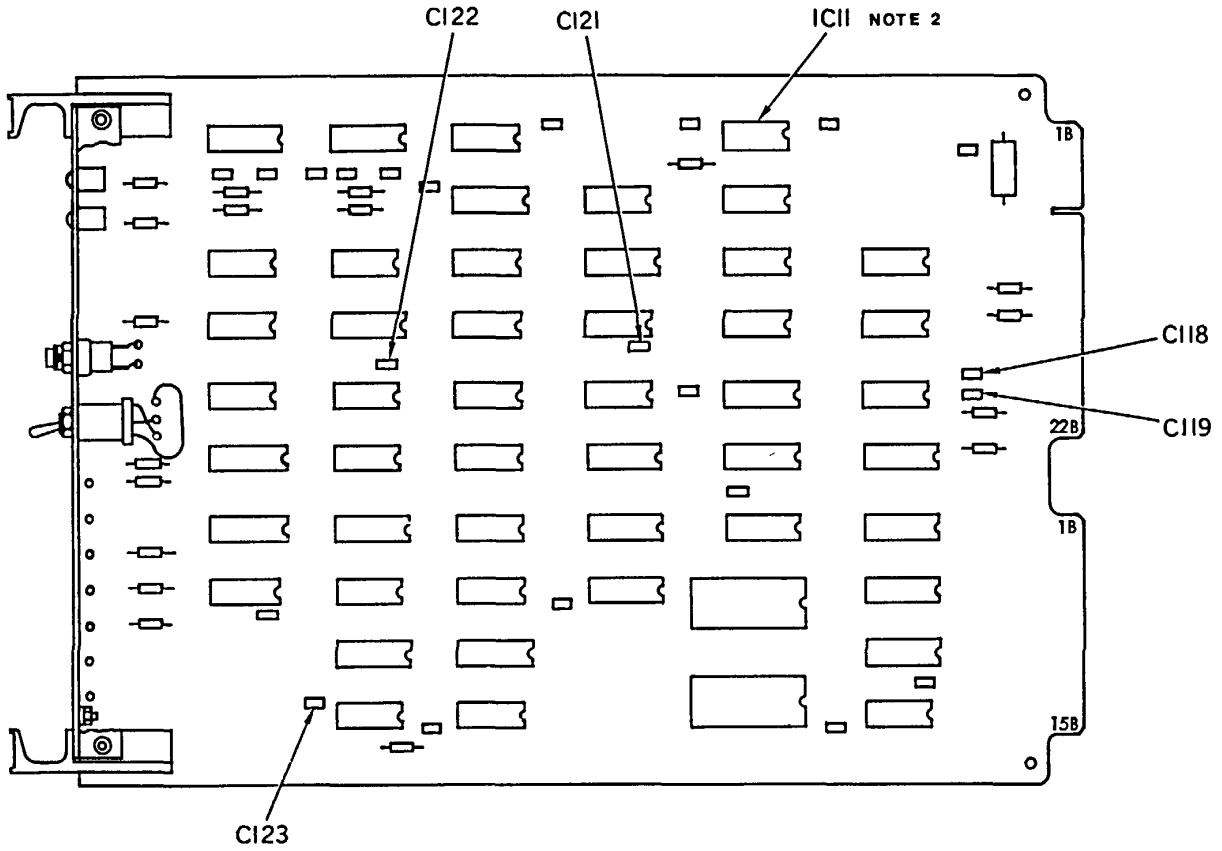


Figure 3-6. MUX unit parts location diagram (sheet 4 or 5) MUX02, MUX04 and MUX06.



NOTES:
1. 22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING A-SIDE OPPOSITE.
2. USED IN CONFIGURATION 04 ONLY.

EL2XB066

Figure 3-6. MUX unit parts location diagram (sheet 5 of 5) MUX04 aid MUX06.

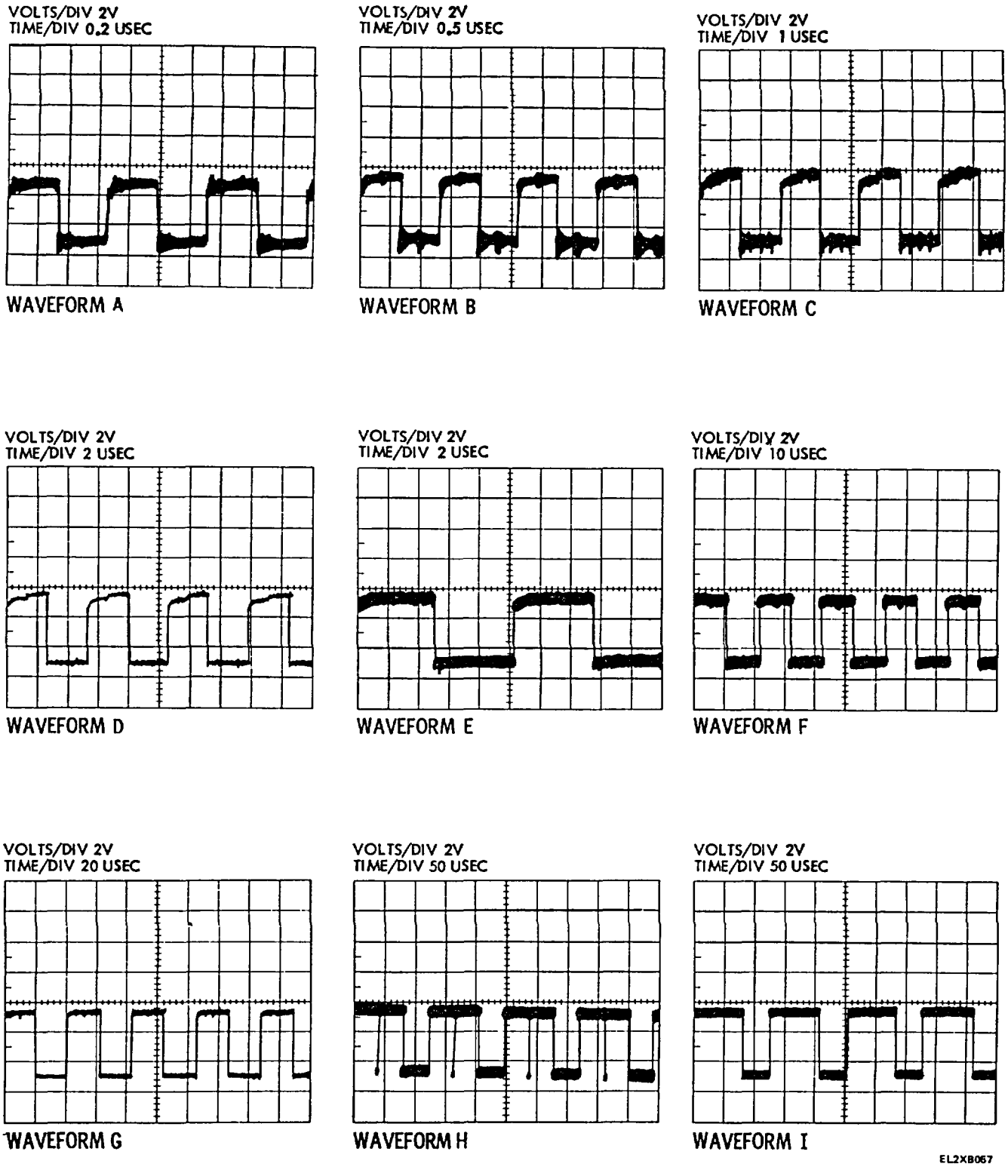


Figure 3-7. MUX unit troubleshooting waveforms (sheet 1 of 4).

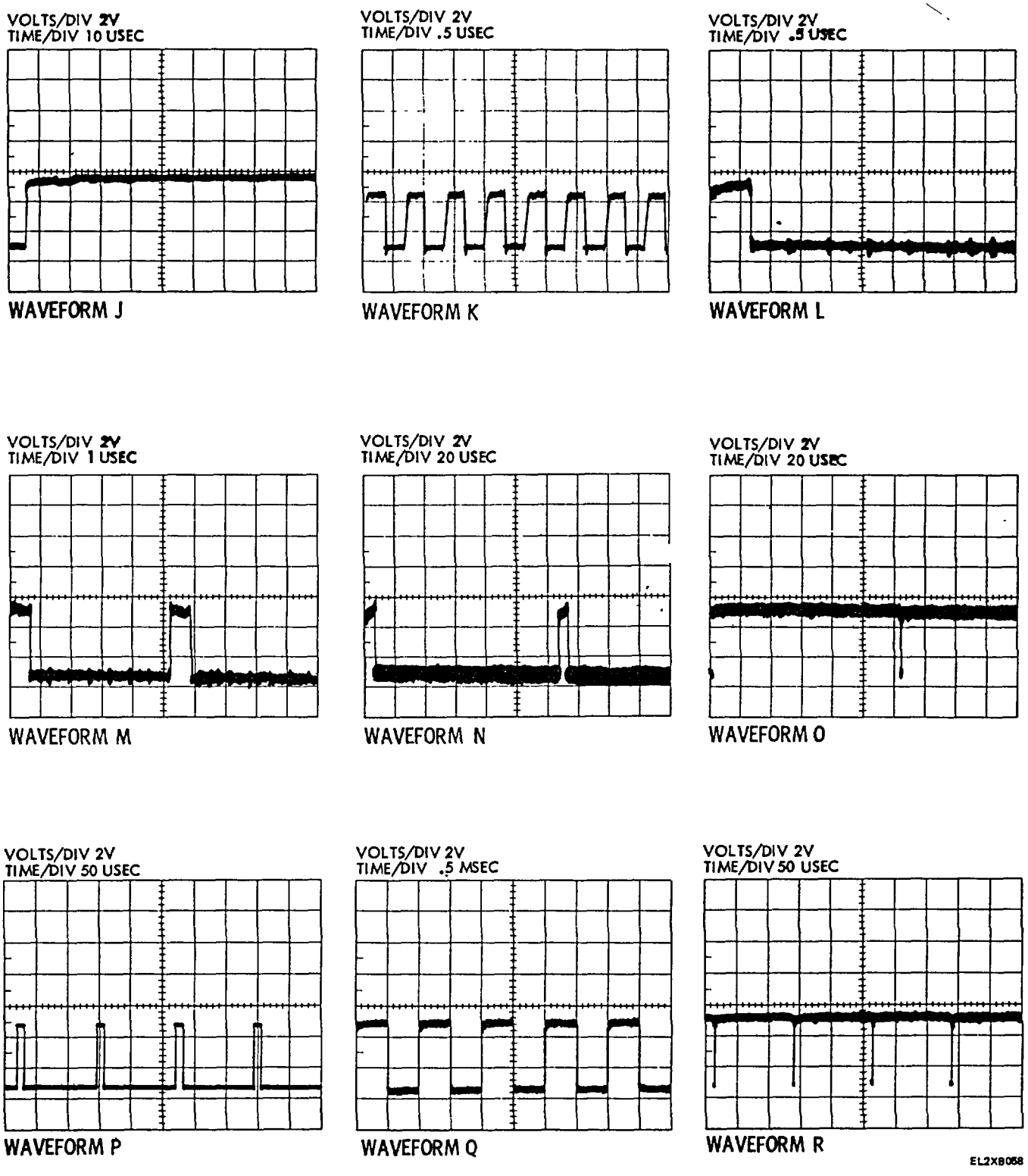


Figure 3-7. MUX unit troubleshooting waveforms (sheet 2 of 4).

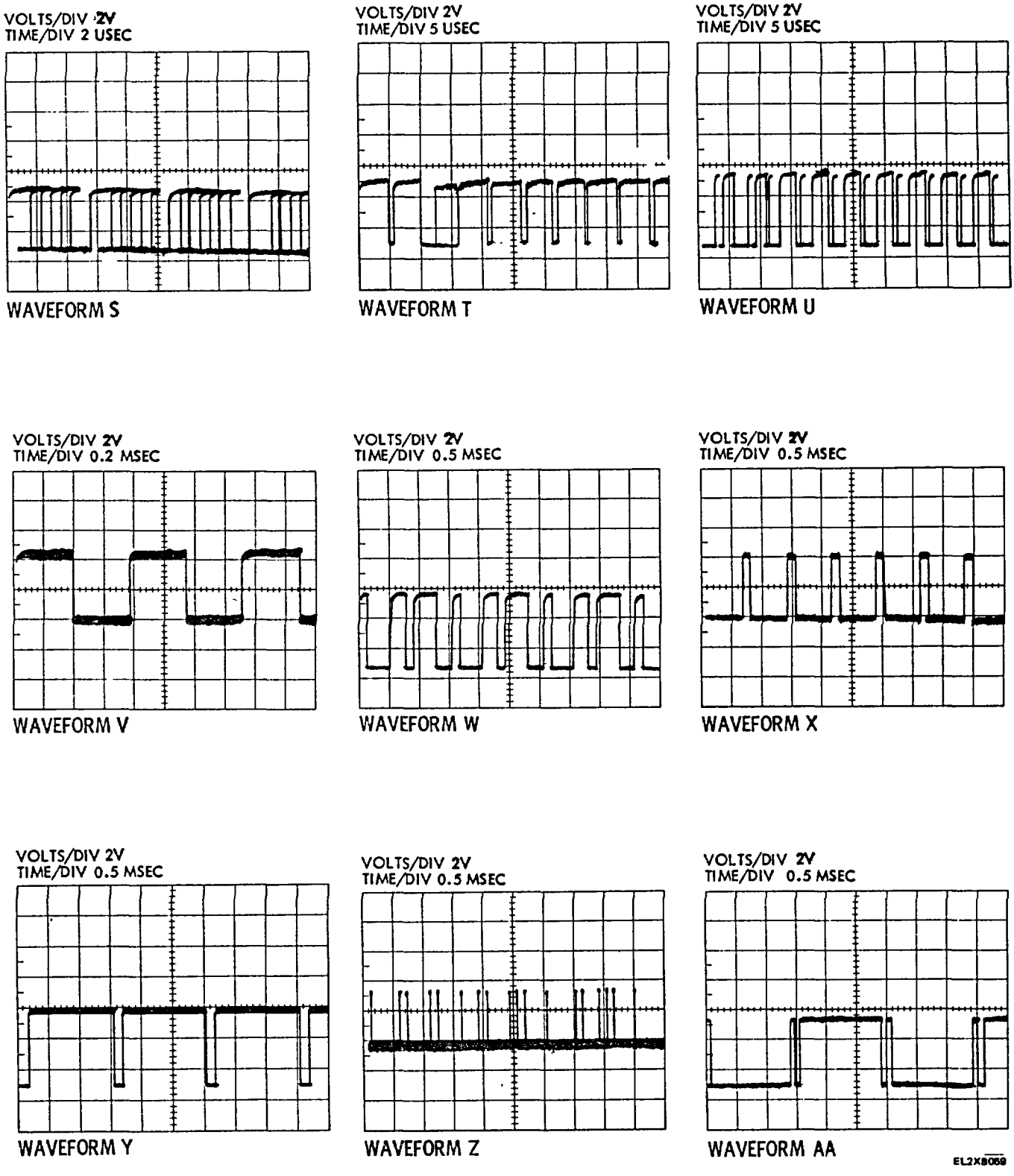


Figure 3-7. MUX unit troubleshooting waveforms (sheet 3 of 4).

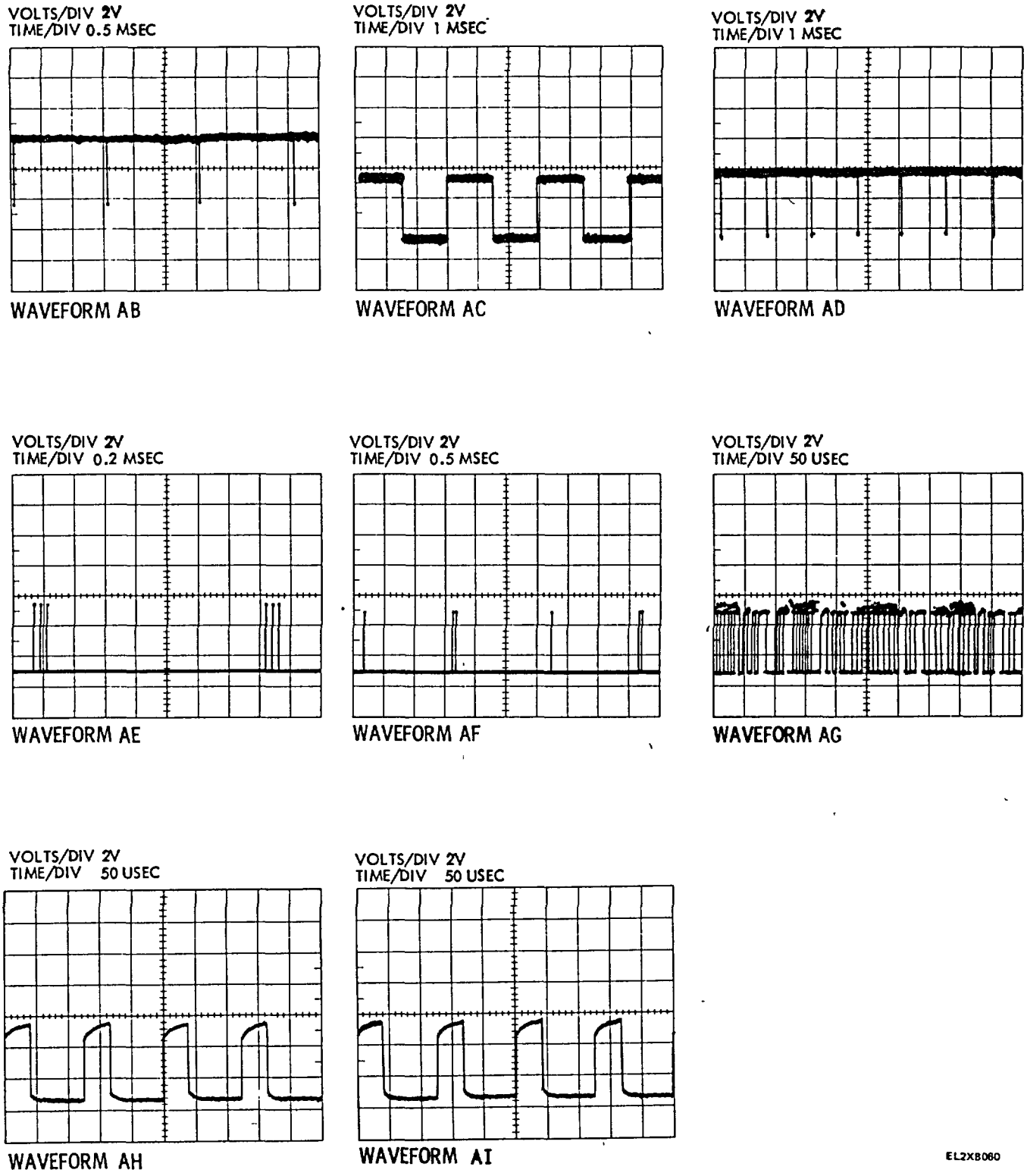


Figure 3-7. MUX unit troubleshooting waveforms (sheet 4 of 4).

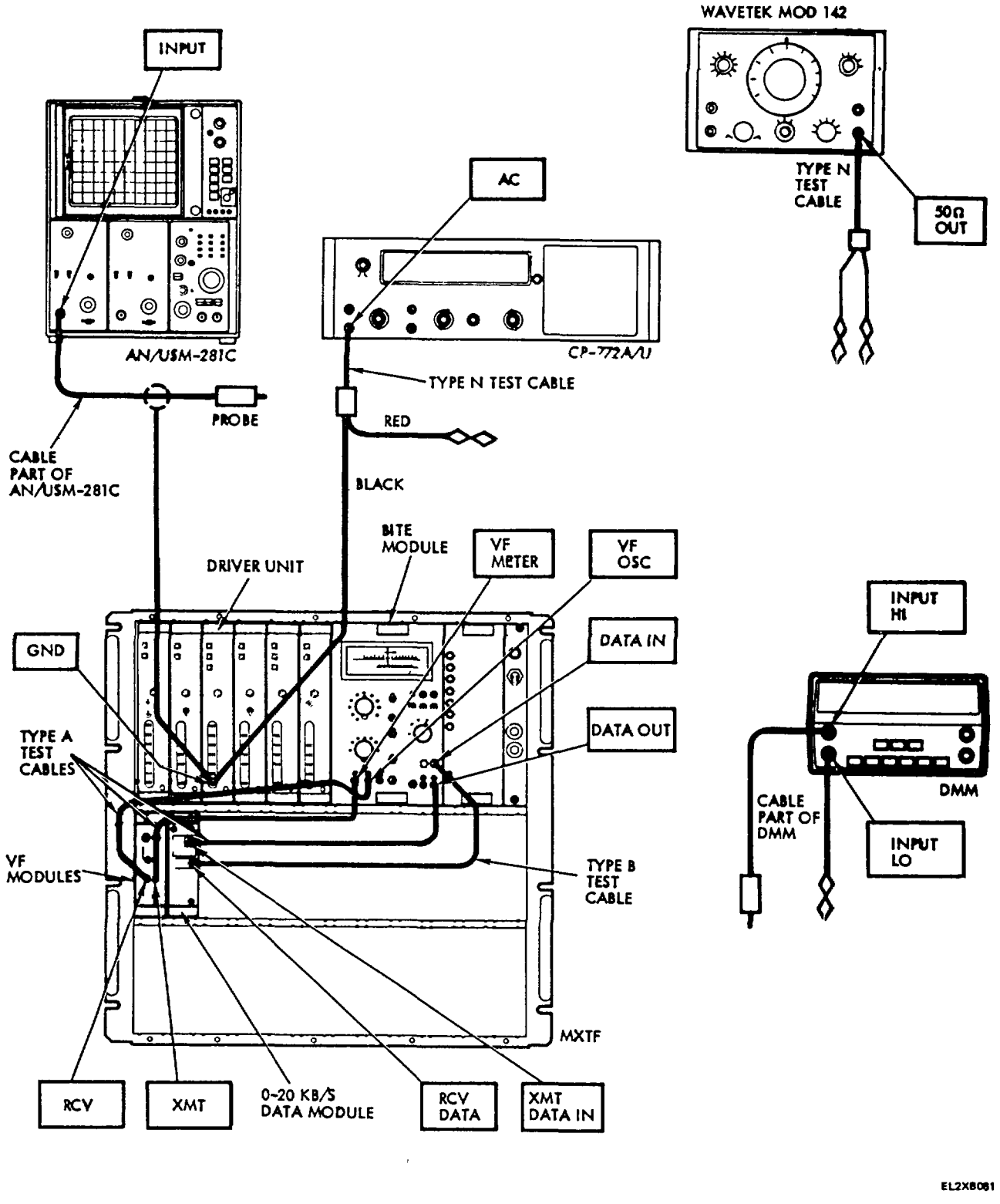


Figure 3-8. DRIVER unit troubleshooting setup diagram.

3-10. Troubleshooting DRIVER Unit

The following instructions and data are for use in troubleshooting faulty DRIVER units. Refer to figure FO-4 and figure 3-9 for parts location.

a. Tools and Test Equipment

(1) TK-100/G.
(2) AN/USM-281C.
(3) DMM.
(4) CP-772A/U.
(5) WAVETEK 142.
(6) MXTF with the following accessories:
Extender board TRW 17332-010
Type A test cables (3)
Type B test cable
Type C cables (2)
Type N cables (2)
Spare VF module
Spare 0-20 kb/s data module.

b. Initial Equipment Setup. Set up test equipment and faulty DRIVER unit as follows:

(1) Set power switch on PWR CONT unit to OFF.
(2) Strap UUR and RCVR unit for 24-channel NRZ operation (table 3-4).
(3) Using extender board, insert UUR in place of DRIVER unit.
(4) Connect test equipment as shown in figure 3-8.
(5) Set test equipment switches as follows:

Unit	*Control*	*Setting*
AN/USM-281C	TIME/DIV	5 µs
	VERT MODE	LEFT
	TRIG SOURCE	LEFT
	MODE	AUTO
	COUPLING	DC
	SOURCE	INT
	VOLTS/DIV (left and right)	2V
	AC/GND/DC	DC
WAVETEK 142	FREQ Hz	1M
	FUNCTION	⊓_
	30 V P-P MAX	FULLY CCW
	DC OFFSET	OFF
	OUTPUT ATTEN (dB)	-10
	Frequency	1.544 MHz
	VERNIER	CAL
DMM	FUNCTION	DCV
	RANGE	10V
	POWER	ON
CP-772A/U	FUNCTION	FREQUENCY
	TIME BASE	i s
	SENSITIVITY	1
	SAMPLE RATE	Rotate ¼ turn clockwise

NOTE

Allow equipment to warm up for 5 minutes before proceeding.

c. Fault Location. Troubleshoot in accordance with the following procedures.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-10
			NOTE **All reference designations for configuration DVR02 are shown in parenthesis.**	
1			Check 78-ohm BAL EXT TIMING SOURCE RECEIVER and LEVEL TRANSLATOR-IC12 (IC5), IC62 (IC15). If result of any check is incorrect, isolate and replace faulty component.	
	Wavetek 142			
	Frequency	1.544 MHz	*a*. Connect type N cable from 50n output of Wavetek 142 to AC input of CP-772A/U. Adjust Wavetek 142 to 1.544 MHz ±1 kHz.	*a*. 1.544 MHz 1 kHz.
	AMPLITUDE:	As req.	*b*. Connect 50 q output on Wavetek 142 to P29-1A and P29-1B on extender board using type N cable. Connect left probe of AN/USM-281C to P29-1A.	*b*. None.
			c. Adjust OUTPUT ATTEN (db) control on Wavetek 142 for 2V peak-to-peak square wave indication on AN/USM-281C.	*c*. 2Vp-p square wave.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-10
			d. Check signal at IC12-9 (IC5-9).	*d*. Waveform A.
			e. Check signal at EXT CLK test point on UUR.	*e*. Waveform B.
2			Check PHASE DETECTOR circuit consisting of IC51 (IC4), IC52 (IC14), IC61 (IC21), Q11 (Q1), Q12 (Q2) and Q13 (Q3). If result of check is incorrect, isolate and replace faulty component.	
	AN/USM-281C		Connect left probe of AN/USM-281C to	Waveform C.
	TIME/DIV:	2 µs	IC51-3 (IC4-3) and right probe to IC51-	
	VERT MODE:	ALT	1 (IC4-1) and verify PLL operation.	
3			Check LOOP FILTER circuit IC31 (IC3). If result of either check is incorrect, isolate and replace faulty component.	
			a. Using DMM, measure voltage at IC21-1 (IC13-1).	*a*. -1 to-2 Vdc.
			b. Disconnect leads from Wavetek 142 to P29-1A and P29-1B. Measure voltage at IC21-1 (IC13-1).	*b*. -2.1 +0.25 Vdc.
4			Check 24.704 MHZ VCO circuit IC14 (IC 32). If result of check is incorrect, isolate and replace faulty component.	
	AN/ USM-281C			
	VERT/MODE:	LEFT	*a*. Reconnect Wavetek 142 to P29-1A and P29-1B.	*a*. None.
	TIME/DIV:	05 µs	*b*. Check waveform at IC22-5 (IC12-5).	*b*. Waveform D.
			c. Disconnect Wavetek 142 from P29-1A and P29-1B.	*c*. None.
5			Check CLOCK SOURCE SELECT and EXTERNAL CLOCK ACTIVITY MONITOR circuits consisting of ICS (IC44), IC22 (IC12), IC24 (IC23), IC32 (IC22) and IC53 (IC33). If result of any check is incorrect, isolate and replace faulty component.	
			a. Check signal at IC36-14 (IC56-14)	*a*. Waveform E.
			b. Check signal at IC46-8 (IC42-8).	*b*. Waveform E.
			c. Check signal at IC25-8 (IC31-8).	*a*. Waveform F.
	AN/USM-281C			
	TIME/DIV:	1 µs	*d.* Check signal at IC26-12 (IC41-12).	*d*. Waveform G.
			e. Check signal at IC26-11 (IC41-11).	*e*. Waveform H.
	TIME/DIV:	1 µs	*f.* Check signal at IC34-12 (IC53-12).	*f.* Waveform I.
			g. Check signal at IC44-8 (IC54-8).	*g*. Waveform J.
			h. Check signal at IC65-12 (IC36-12).	*h*. Waveform K.
	TIME/DIV:	1µs	*i.* Check signal at IC44-6 (IC54-6).	*i.* Waveform L.
	TIME/DIV:	2 µs	*j.* Check signal at IC55-10 (IC6-10).	*j.* Waveform M.
			k. Check signal at IC45-6 (IC46-6).	*k*. Waveform N.
			l. Check signal at IC14-11 (IC43-11).	*l.* Waveform O.
			m. Check signal at IC14-12 (IC43-12).	*m*. Waveform P.
			n. Check signal at IC14-13 (IC43-13).	*n*. Waveform Q.
	TIME/DIV:	5 µs	*o.* Check signal at IC33-11 (IC52-11).	*o*. Waveform R.
6			Check CLOCK MUX circuit IC34 (IC53). result of any check is incorrect, isolate and replace faulty component.	
			NOTE **Ignore any FAULT lamps which may light.**	

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig. 3-10
			a. Strap UUR for 3-channel operation (table 3-4).	*a*. None.
	AN/USM-281C			
	TIME/DIV:	2 ms	*b*. Check signal at MBS CLOCK test point on UUR.	*b*. Waveform S.
			c. Strap UUR for 6-channel operation (table 3-4).	*c*. None.
			d. Check signal at MBS CLOCK test point.	*d*. Waveform T.
			e. Strap UUR for 12-channel operation (table 3-4).	*e*. None.
	AN/USM-281C			
	TIME/DIV:	1 ms	*f*. Check signal at MBS CLOCK test point.	*f*. Waveform U.
			g. Strap UUR for 24-channel operation (table 3-4).	*g*. None.
	TIME/DIV	.5 ms	*h*. Check signal at MBS CLOCK test point.	*h*. Waveform V.
7			Check 16 KHZ PHASE LOCK LOOP circuit IC42 (IC51), IC24 (IC23) and IC25 (IC31). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	20 ms	*a*. Check signal at test point E2.	*a*. Waveform W.
			b. Check signal at IC25-5 (IC31-5).	*b*. Waveform X.
			c. Check signal at 16 KPPS test point (TP5).	*c*. Waveform Y.
8			Check 100-ohm BIPOLAR MBS DATA OUT DRIVER IC45 (IC46), IC55 (IC6), IC56 (IC16), IC65 (IC36), Q1 (Q4) and Q2 (Q5). If result of any check is incorrect, isolate and replace faulty component.	
			a. Strap UUR and RCVR units for 24-channel bipolar operation (table 3-4).	*a*. None.
	AN/USM-281C			
	TIME/DIV:	.2 ms	*b*. Check signal at IC65-6 (IC36-6).	*b*. Waveform Z.
	TIME/DIV:	.5 µs	*c*. Check signal at IC55-4 (IC6-4).	*c*. Waveform AA.
			d. Check signal at IC55-1 (IC6-1).	*d*. Waveform AA.
	VOLTS/DIV:	5V	*e*. Check signal at collector of Q1 (Q4).	*e*. Waveform AB.
			f. Check signal at collector of Q2 (QS).	*f*. Waveform AB.
9			Check 78-ohm BAL NRZ MBS CLK OUT DRIVER and 78-ohm BAL MASTER CLK OUT DRIVER circuits-Q14 thru Q29. If result of any check is incorrect, isolate and replace faulty component.	
			a. Strap UUR and RCVR units for 24-channel NRZ operation (table 3-4).	*a*. None.
	AN/USM-281C			
	VOLTS/DIV:	2V	*b*. Check signal at collector of Q14 (Q22) and Q15 (Q26).	*b*. Waveform AC.
			c. Check signal at collector of Q16 (Q23) and Q17 (Q27).	*c*. Waveform AD.
			d. Check signal at collector of Q20 (Q25) and Q21 (Q29).	*d*. Waveform AE.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-10
			e. Check signal at collector of Q22 (Q14) and Q23 (Q18).	*e*. Waveform AC.
			f. Check signal at collector of Q24 (Q15) and Q25 (Q19).	*f.* Waveform AD.
			g. Check signal at collector of Q28 (Q17) and Q29 (Q21).	*g*. Waveform AE.
			NOTE **If the MASTER CLOCK OUT is not loaded with 78-ohm, its waveform will have a larger peak-to-peak voltage than that shown in waveform AF.**	
			h. Check signal at P5-19B and P5-20B.	*h*. Waveform AF.
			i. Check signal at P5-19A and P5-20A.	*i.* Waveform AF.
10			Check 78-ohm BAL MBS DATA OUT DRIVER circuit-Q3 (Q6) thru Q10 (Q13). If result of any check is incorrect, isolate and replace faulty component.	
			a. Remove type A test cables between XMT DATA IN jack on 0-20 kb/s data module and BITE XMT DATA OUT jack and between XMT jack on VF module and BITE VF OSC jack.	*a*. None.
	AN/USM-281C			
	TIME/DIV:	1 ms	*b*. Check signal at collector of Q3 (Q6).	*b*. Waveform AG.
			c. Check signal at collector of Q4 (Q10).	*c*. Waveform AH.
			d. Check signal at collector of Q5 (Q7).	*d*. Waveform AI.
			e. Check signal at collector of Q6 (Q11).	*e*. Waveform AJ.
			f. Check signal at collector of Q9 (Q9).	*f.* Waveform AK.
			g. Check signal at collector of Q10 (Q13).	*g*. Waveform AL.
			h. Check signal at +MBS DATA test point on UUR.	*h*. Waveform AM.
			i. Check signal at -MBS DATA test point on UUR.	*i*. Waveform AN.
11			Check LOSS OF OUTPUT DETECTOR circuit IC53 (IC33), IC63 (IC66) and IC64 (IC67). If result of any check is incorrect, isolate and replace faulty component.	
	MXTF (RCVR)			
	LOOP-NORMAL:	LOOP	*a*. Observe OUTPUT LOSS lamp on UUR.	*a*. OUTPUT LOSS lamp illuminates. Ignore other illuminated lamps.
			b. Using DMM, measure voltage at pin PS-13B.	*b*. +0.1 to -1.5 Vdc
	LOOP-NORMAL:	NORMAL	*c*. Observe OUTPUT LOSS lamp.	*c*. OUTPUT LOSS lamp out.
			d. Using DMM, measure voltage at P5-13B.	*d*. -3.5 to -5 Vdc.
12			Check FAULT MONITOR circuit IC43 (IC25), IC53 (IC33) and IC54 (IC24). If result of either check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	20 ms	*a*. Check signal at IC43-9.	*a*. Waveform AO.
	TIME/DIV:	.2 ms	*b*. Check signal at IC43-5.	*b*. Waveform AP.

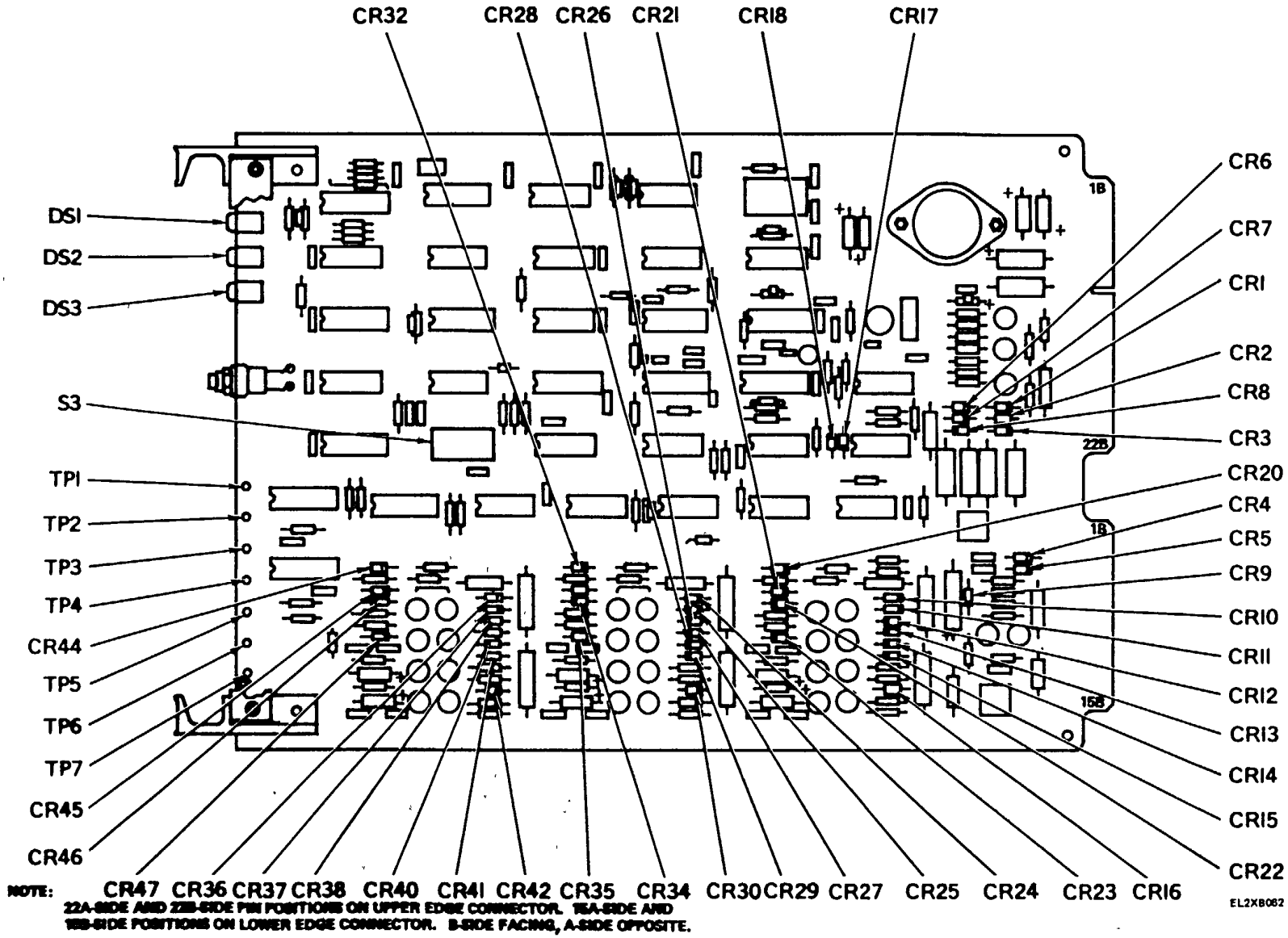
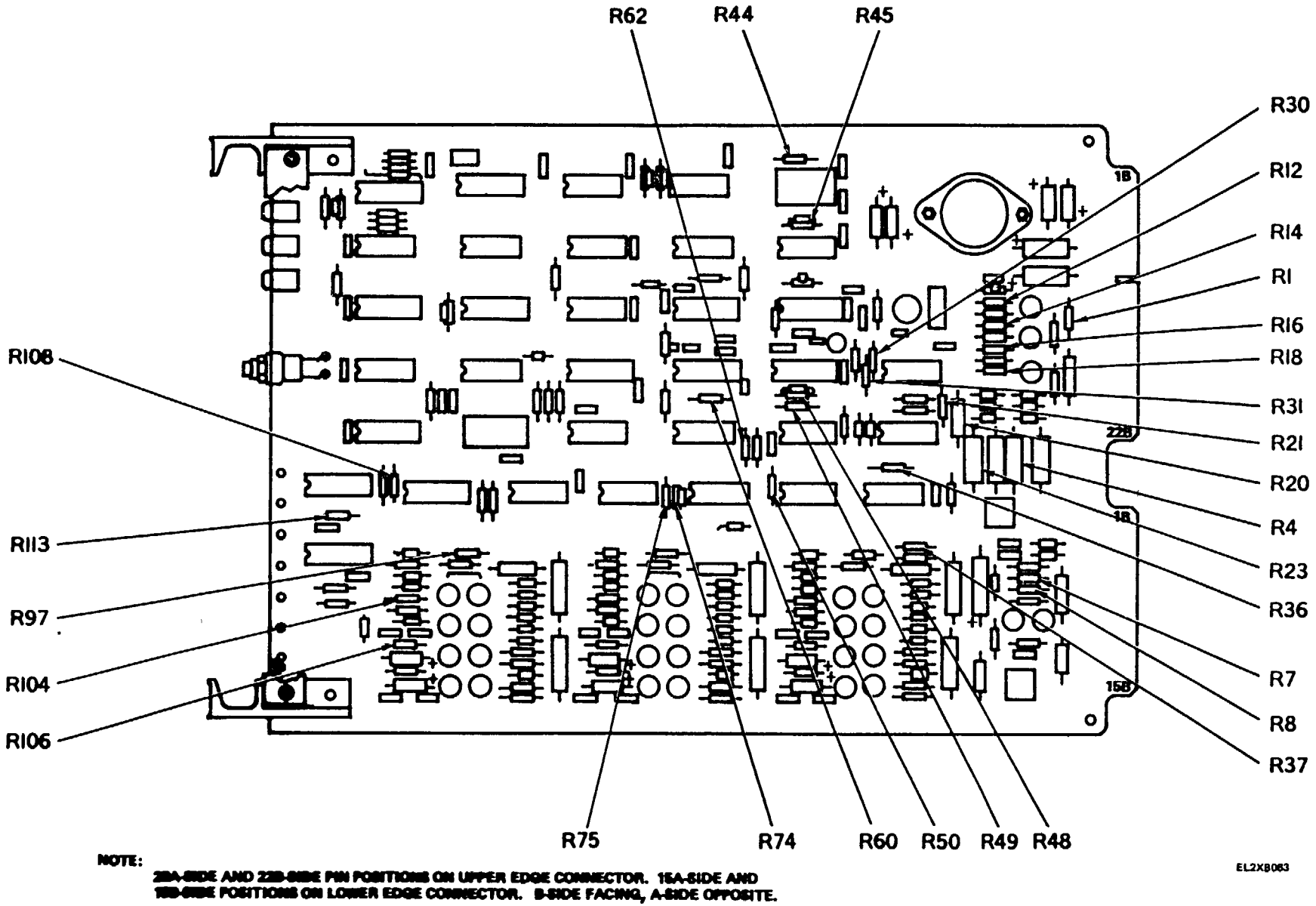
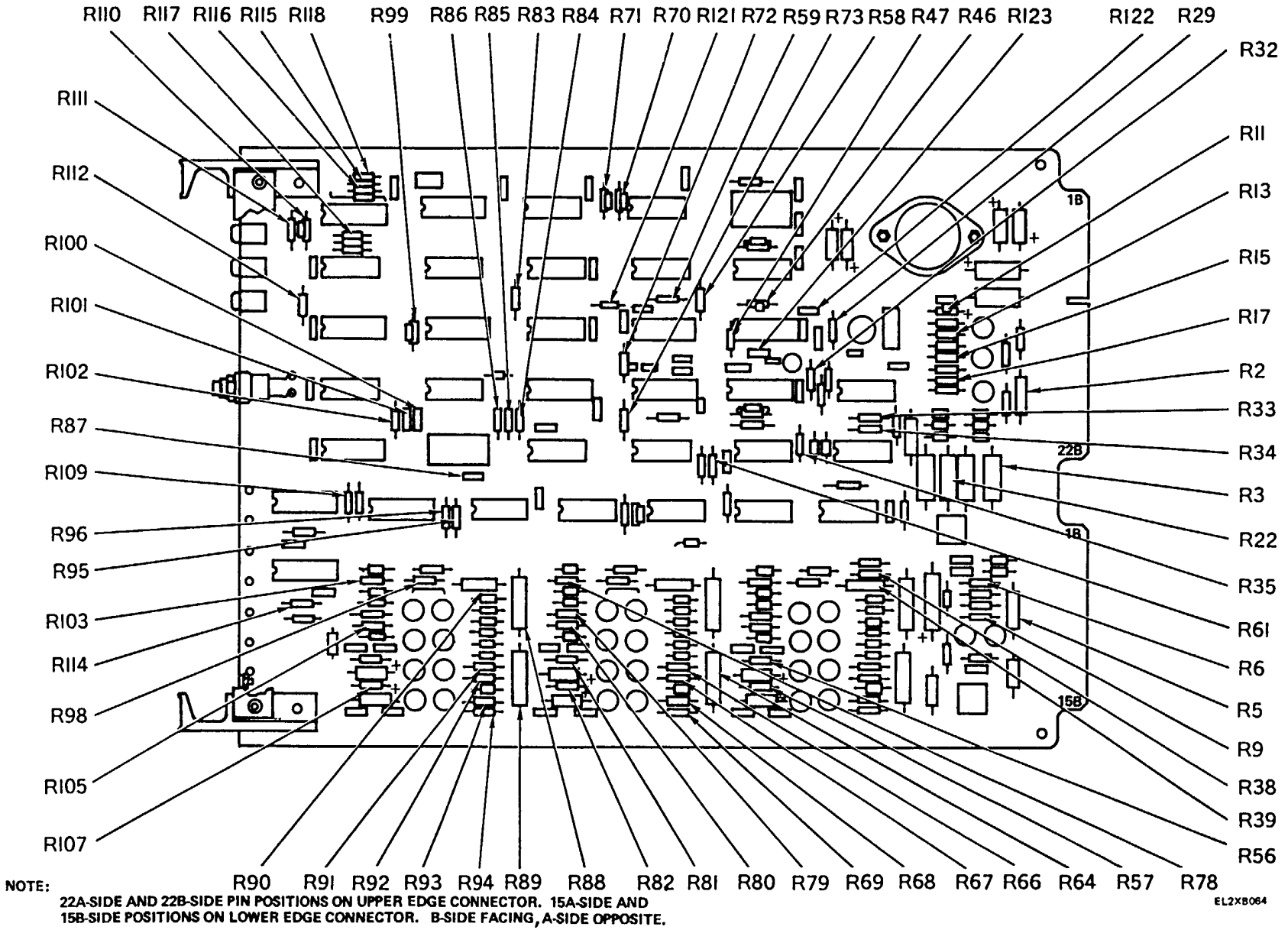


Figure 3-9. DRIVER unit parts location diagram (sheet 1 of 14) DVR02.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

Figure 3-9. DRIVER unit parts location diagram (sheet 2 of 14) DVR02.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

Figure 3-9. DRIVER unit parts location diagram (sheet 3 of 14) DVR02.

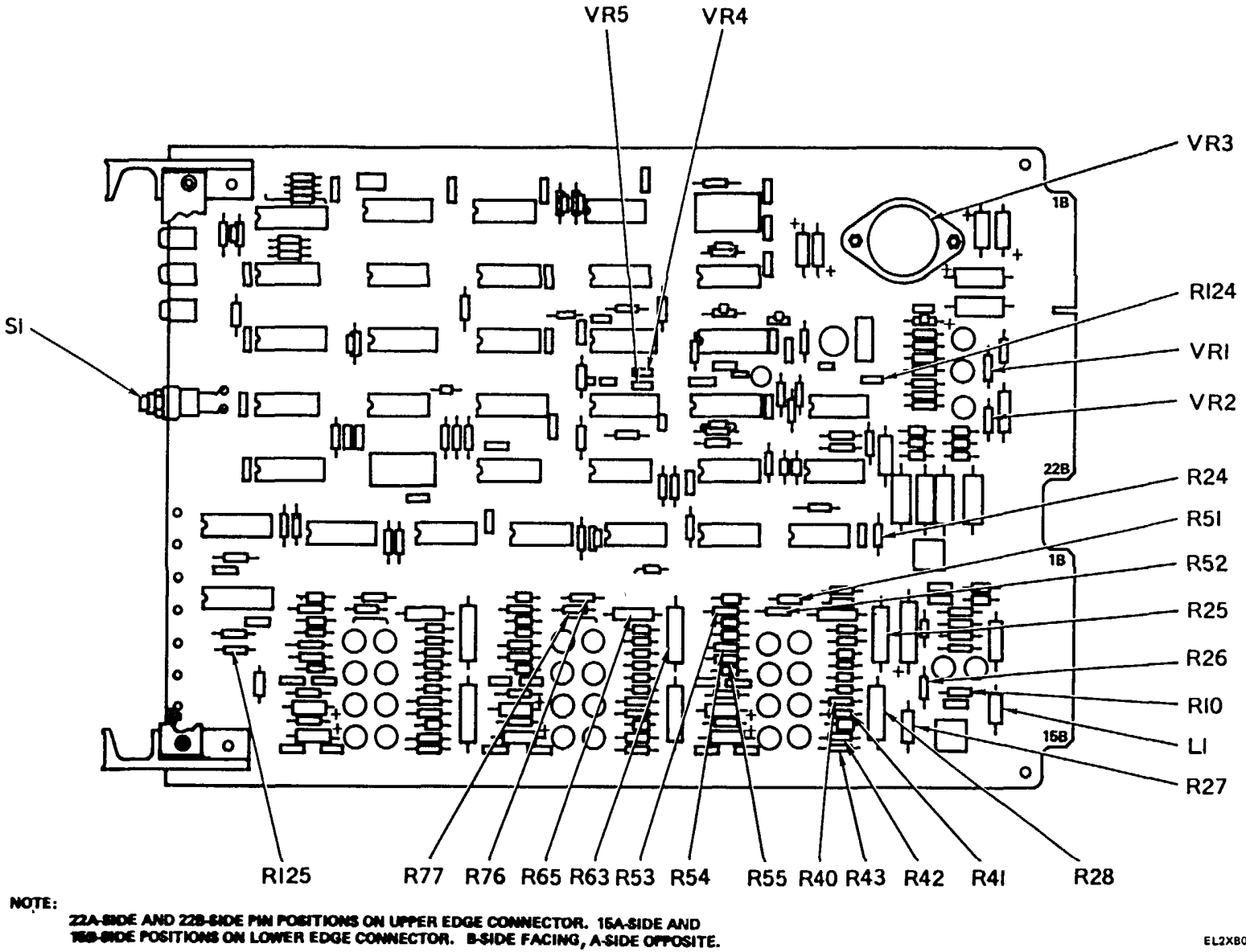


Figure 3-9. DRIVER unit parts location diagram (sheet 4 of 14) DVR02.

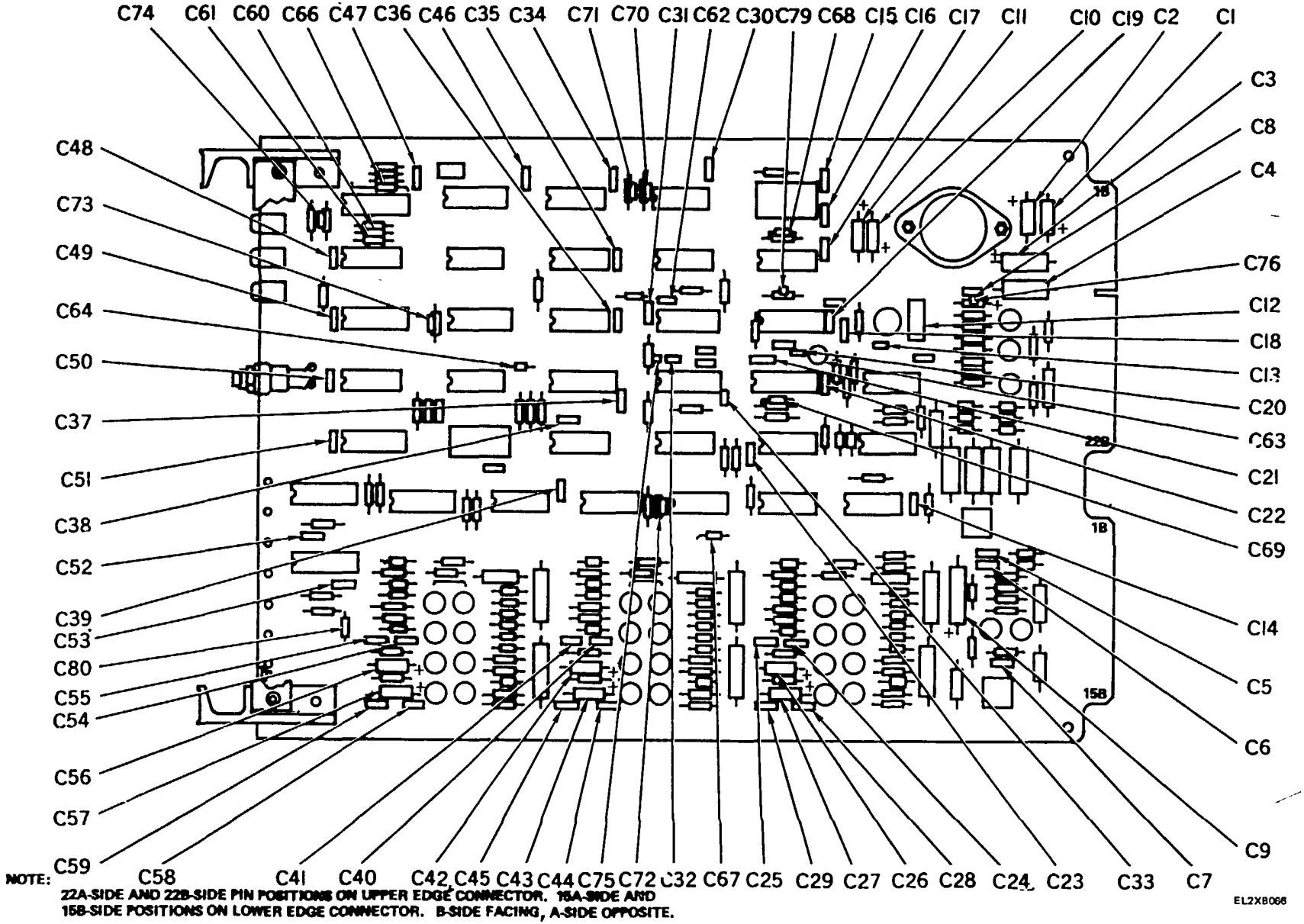
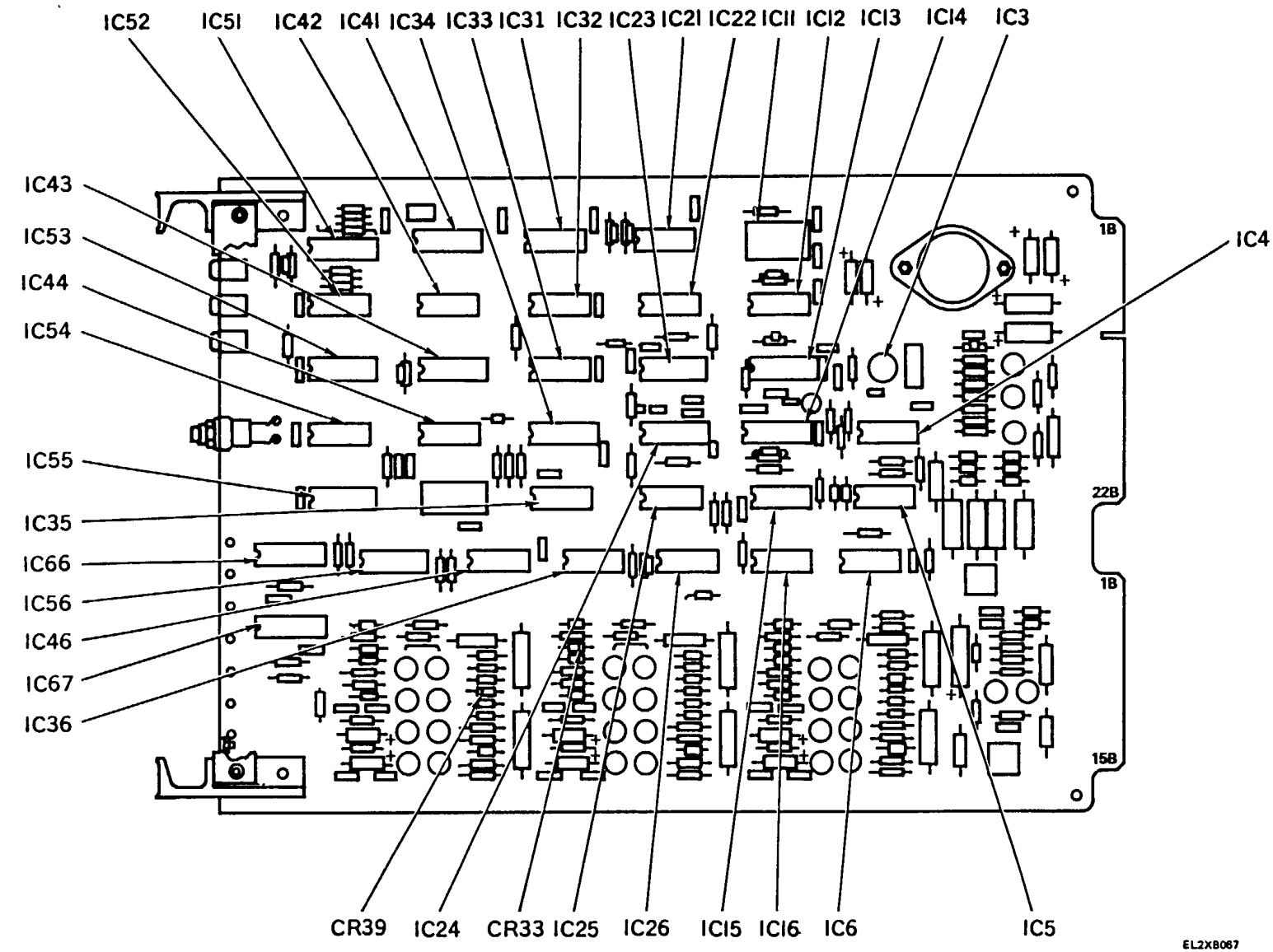


Figure 3-9. DRIVER unit parts location diagram (sheet 5 of 14) DVR02.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

Figure 3-9. DRIVER unit parts location diagram (sheet 6 of 14) DVR02.

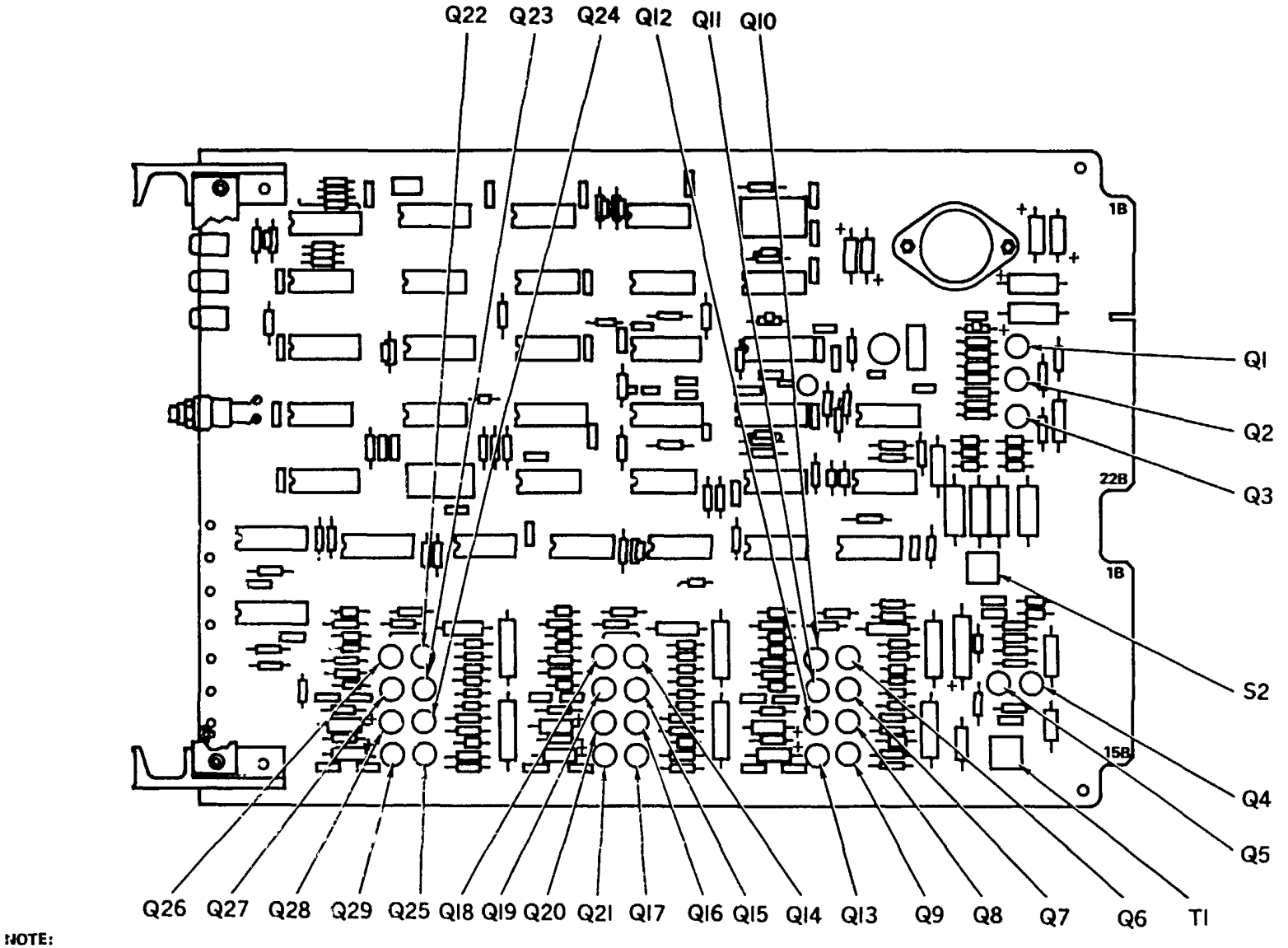
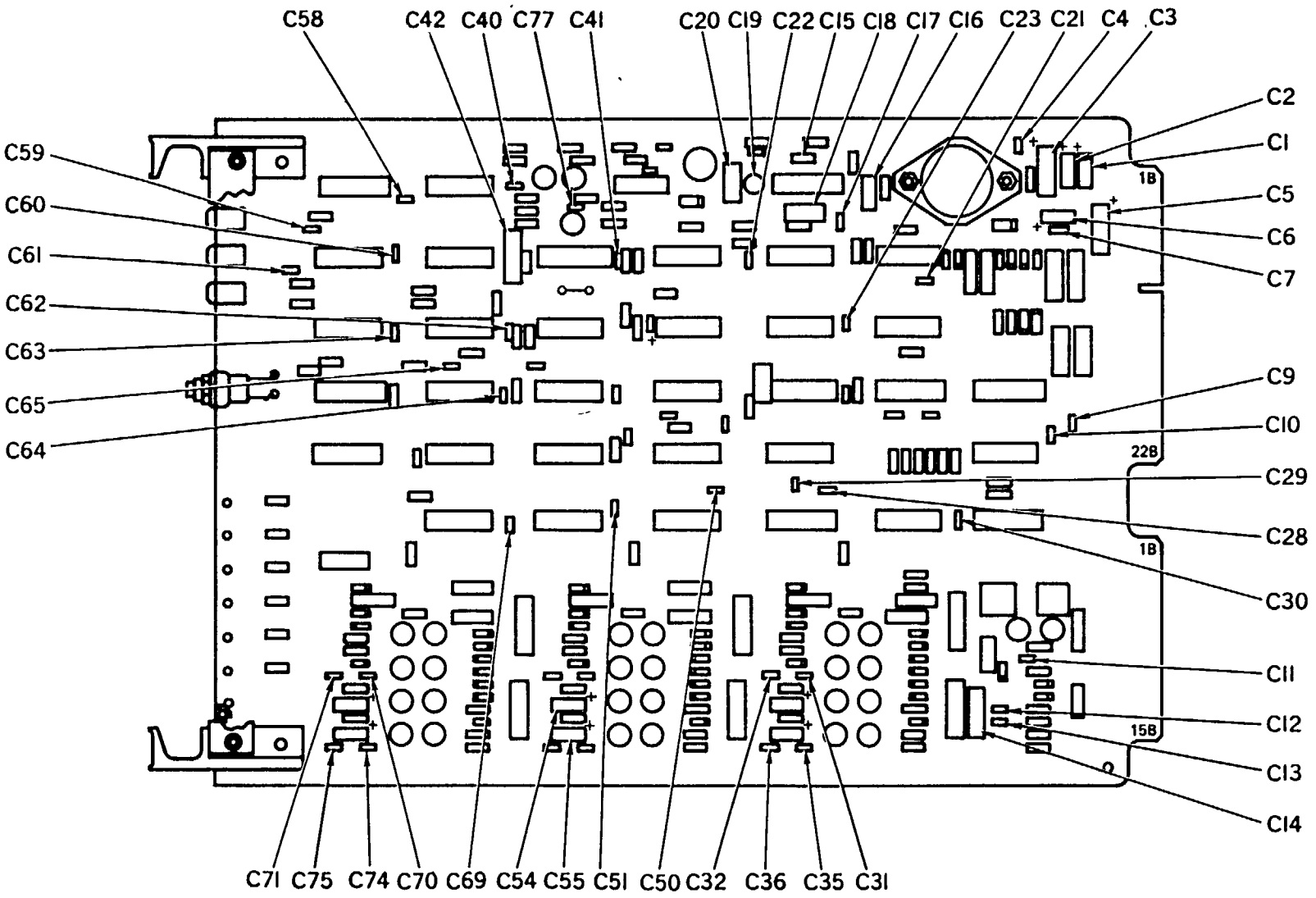


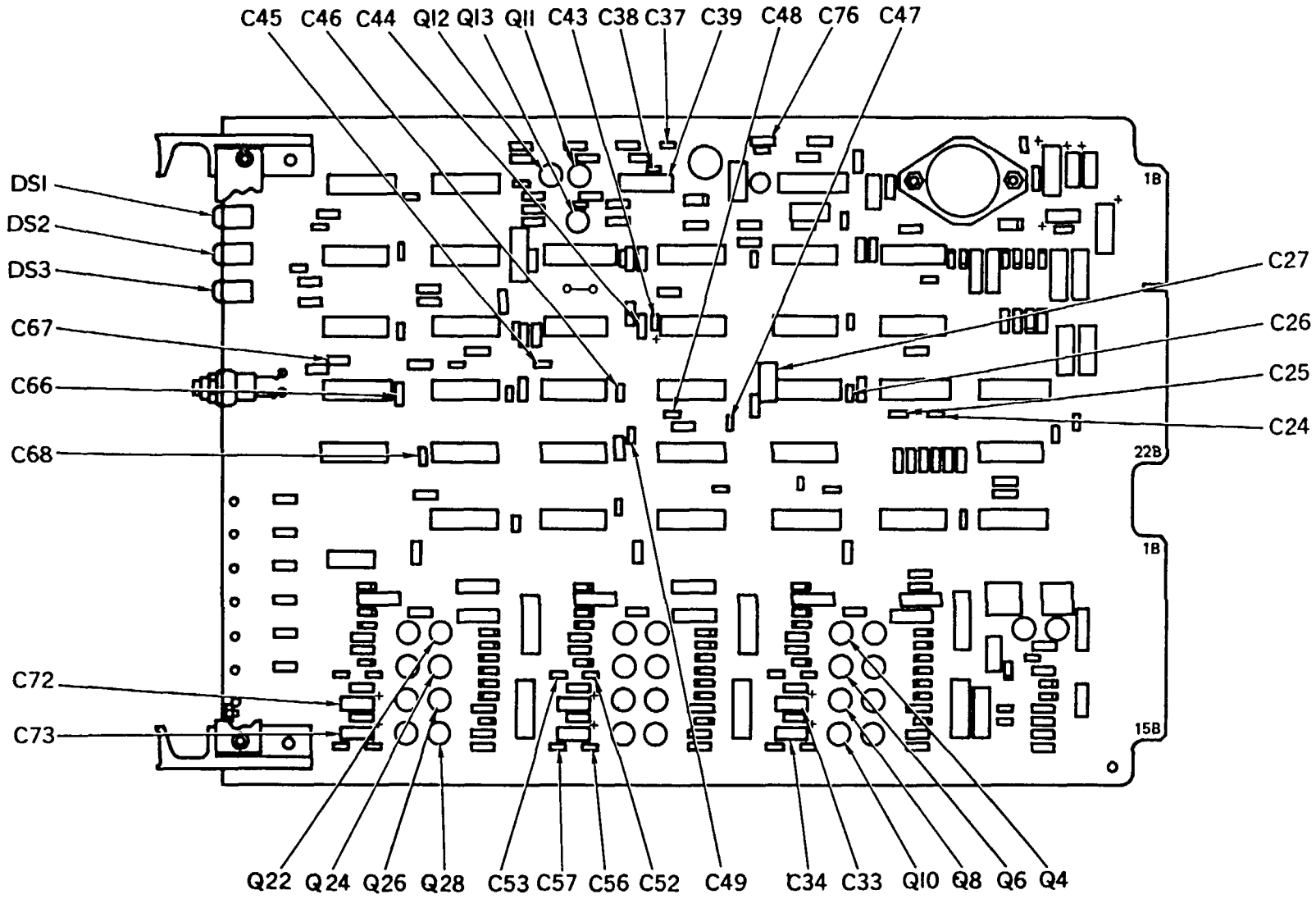
Figure 3-9. DRIVER unit parts location diagram (sheet 7 of 14) DVR02.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB069

Figure 3-9. DRIVER unit parts location diagram (sheet 8 of 14) DVR04.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB070

Figure 3-9. DRIVER unit parts location diagram (sheet 9 of 14) DVR04.

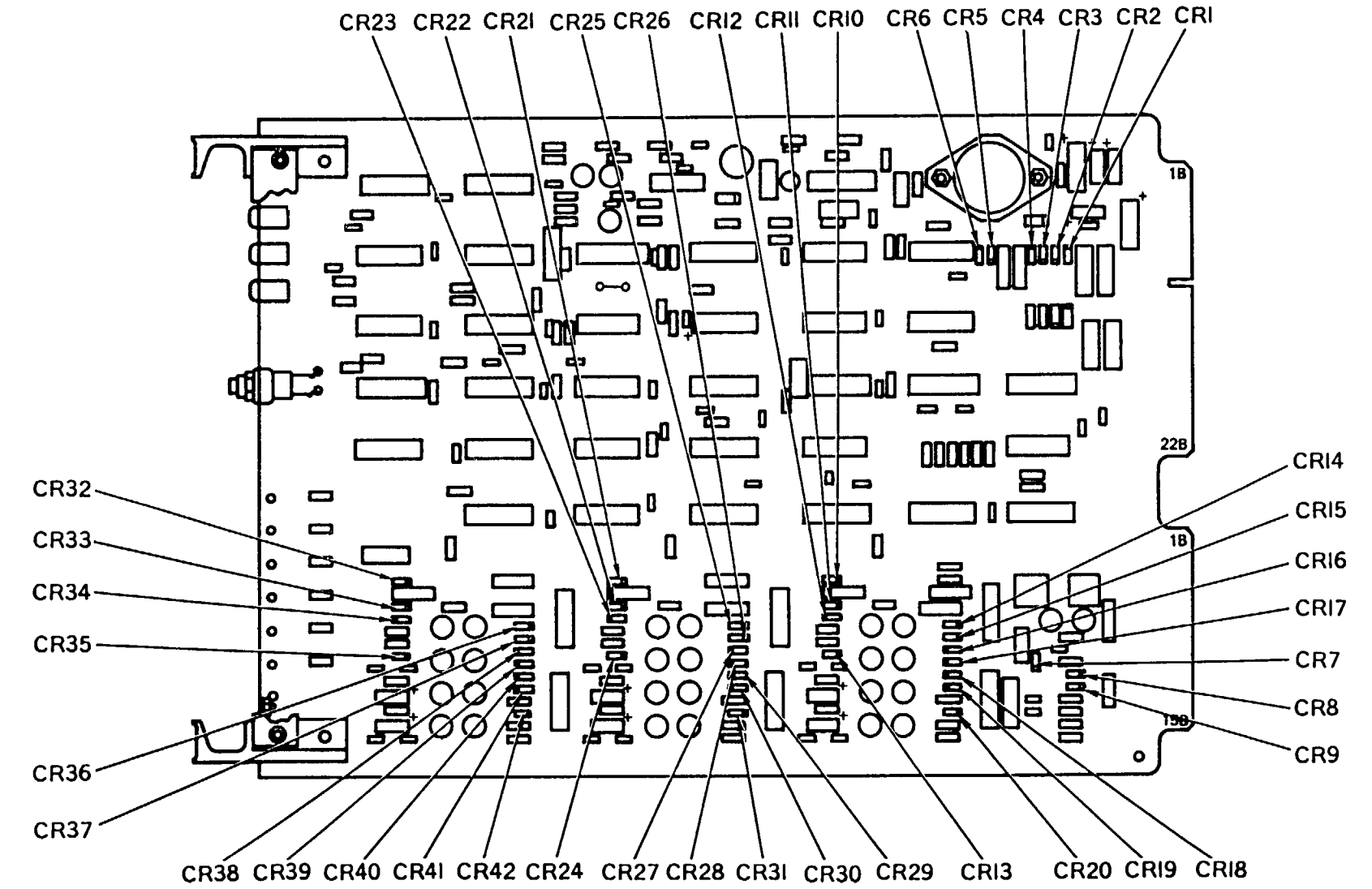
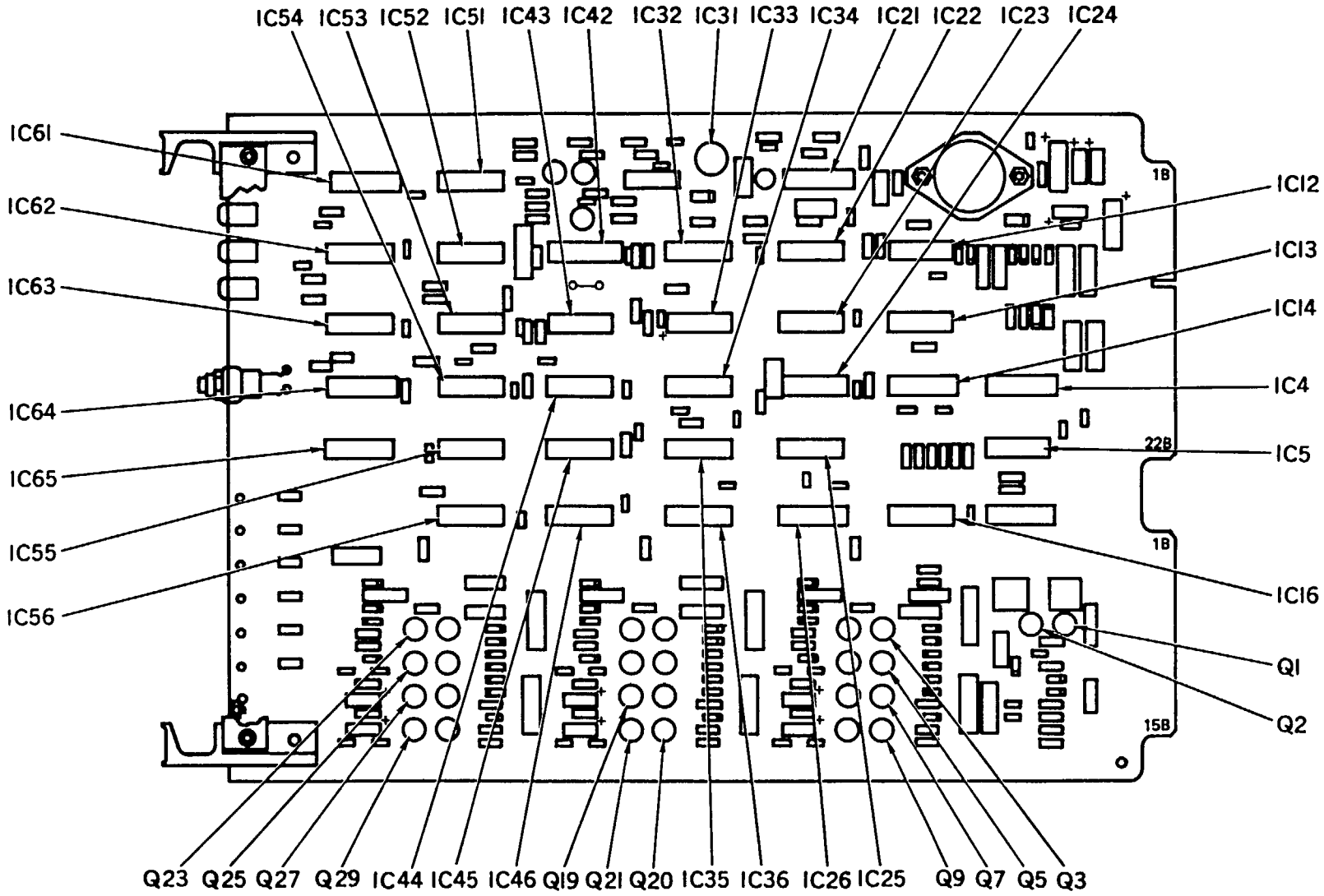


Figure 3-9. DRIVER unit parts location diagram (sheet 10 of 14) DVR04.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB072

Figure 3-9. DRIVER unit parts location diagram (sheet 11 of 14) DVR04.

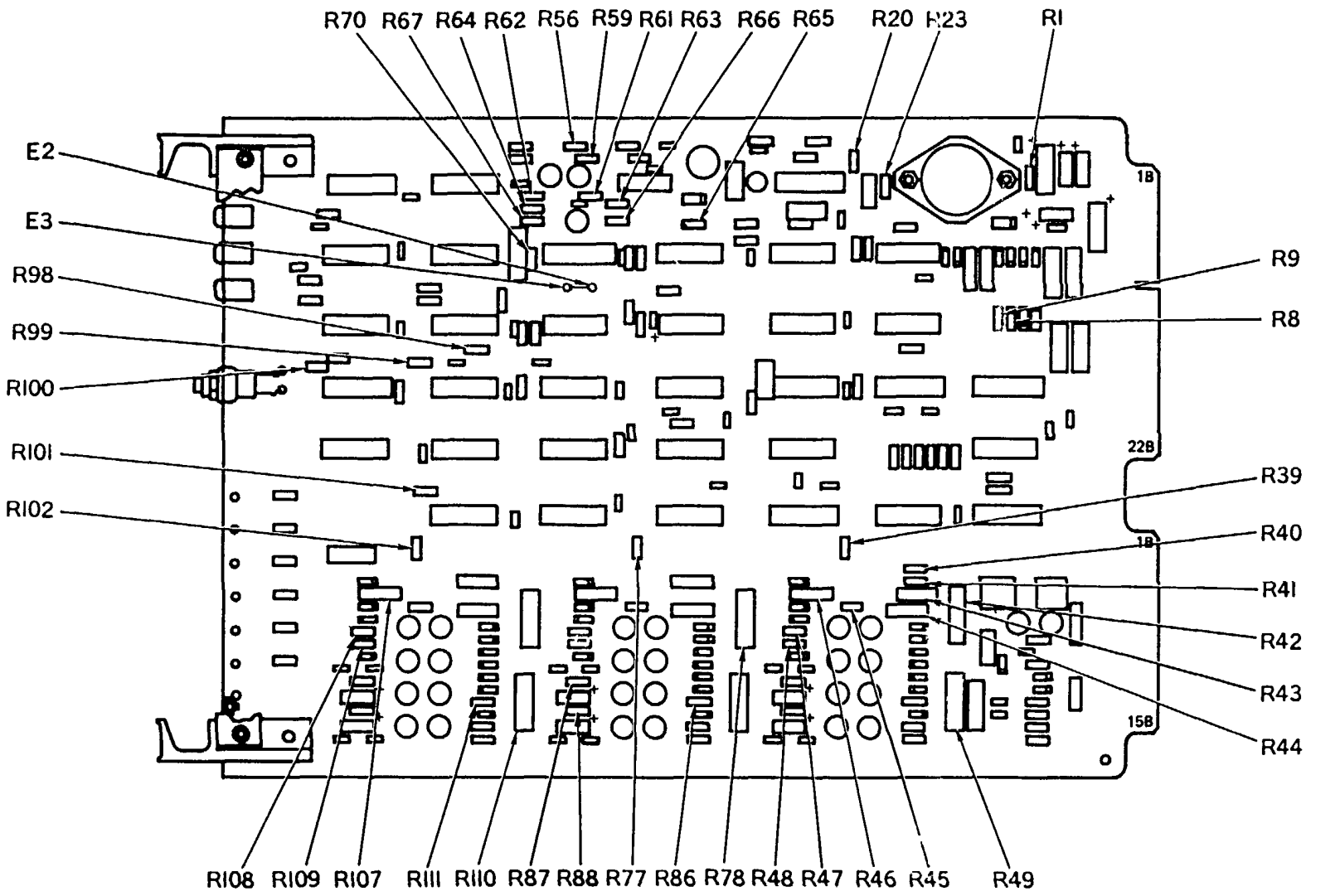
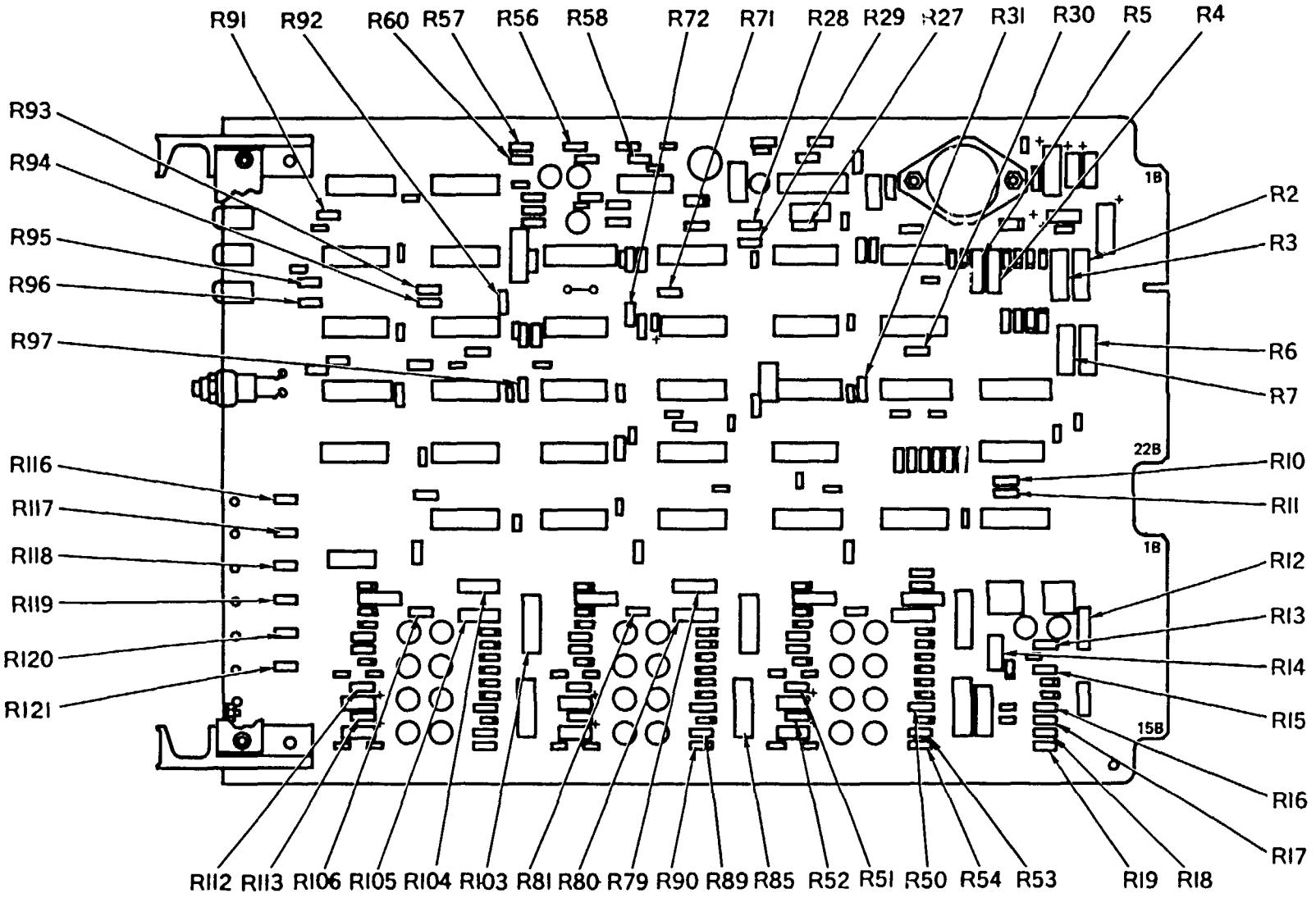


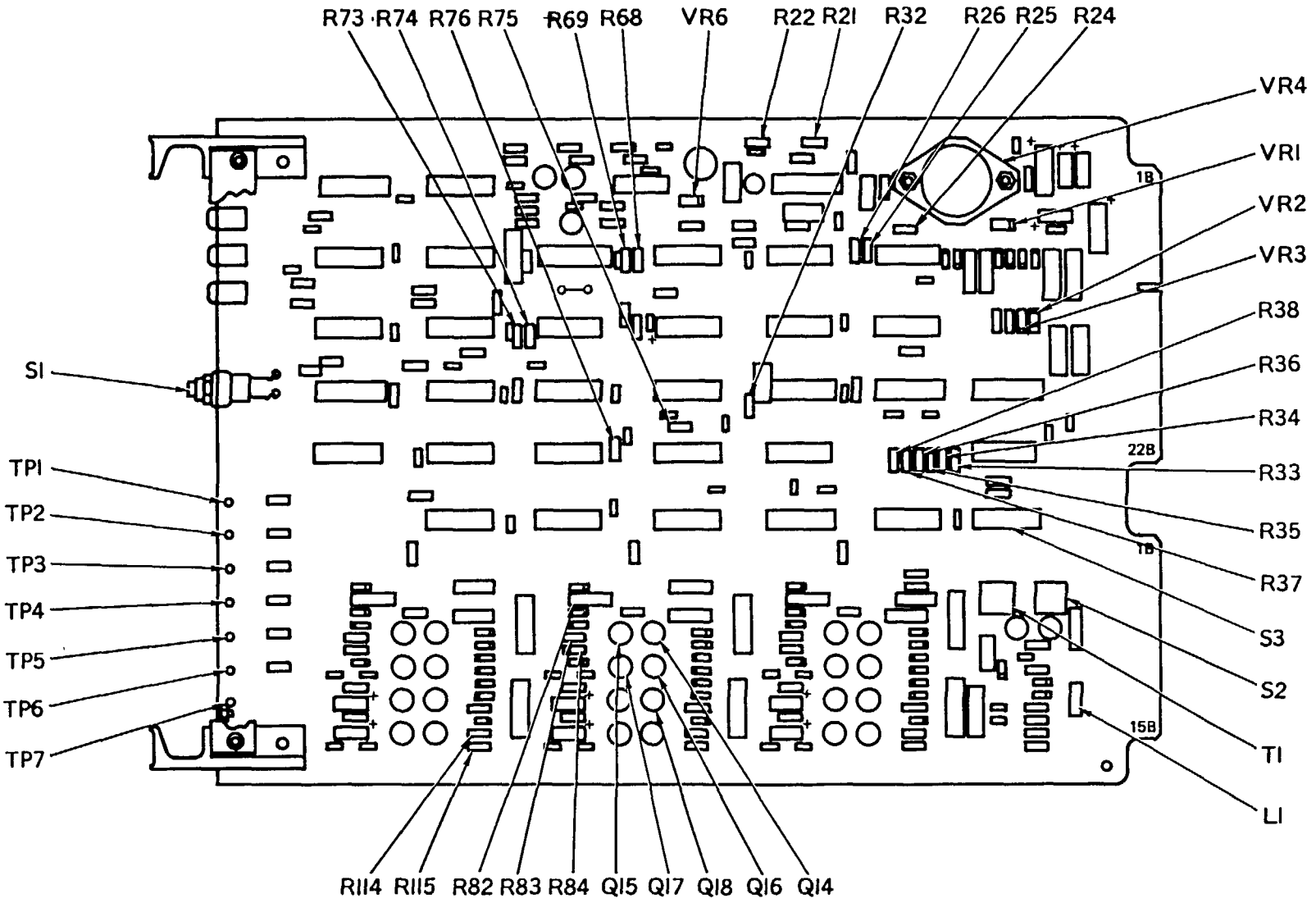
Figure 3-9. DRIVER unit parts location diagram (sheet 12 of 14) DVR04.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB074

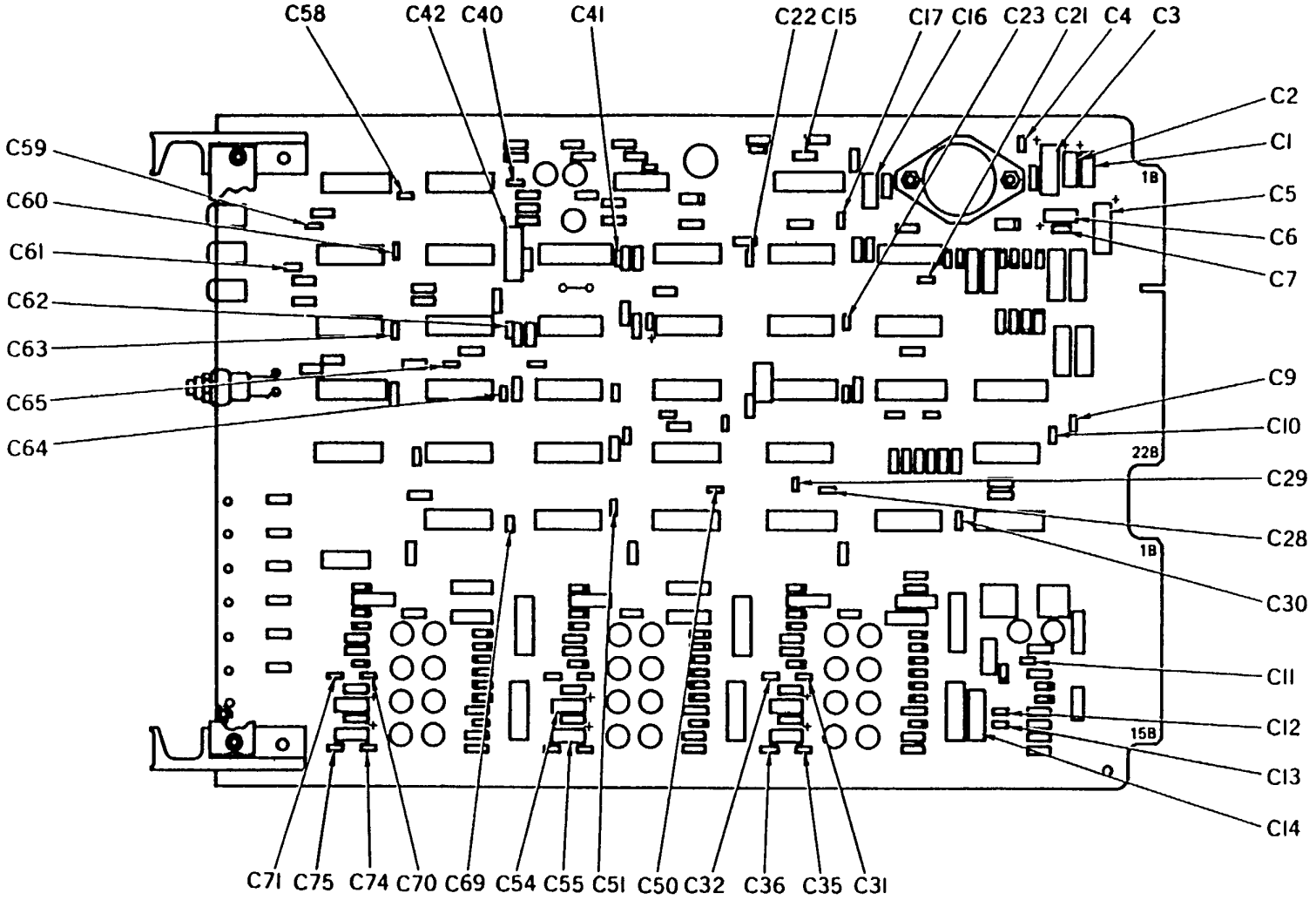
Figure 3-9. DRIVER unit parts location diagram (sheet 13 of 14) DVR04.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB075

Figure 3-9. DRIVER unit parts location diagram (sheet 14 of 14) DVR04.

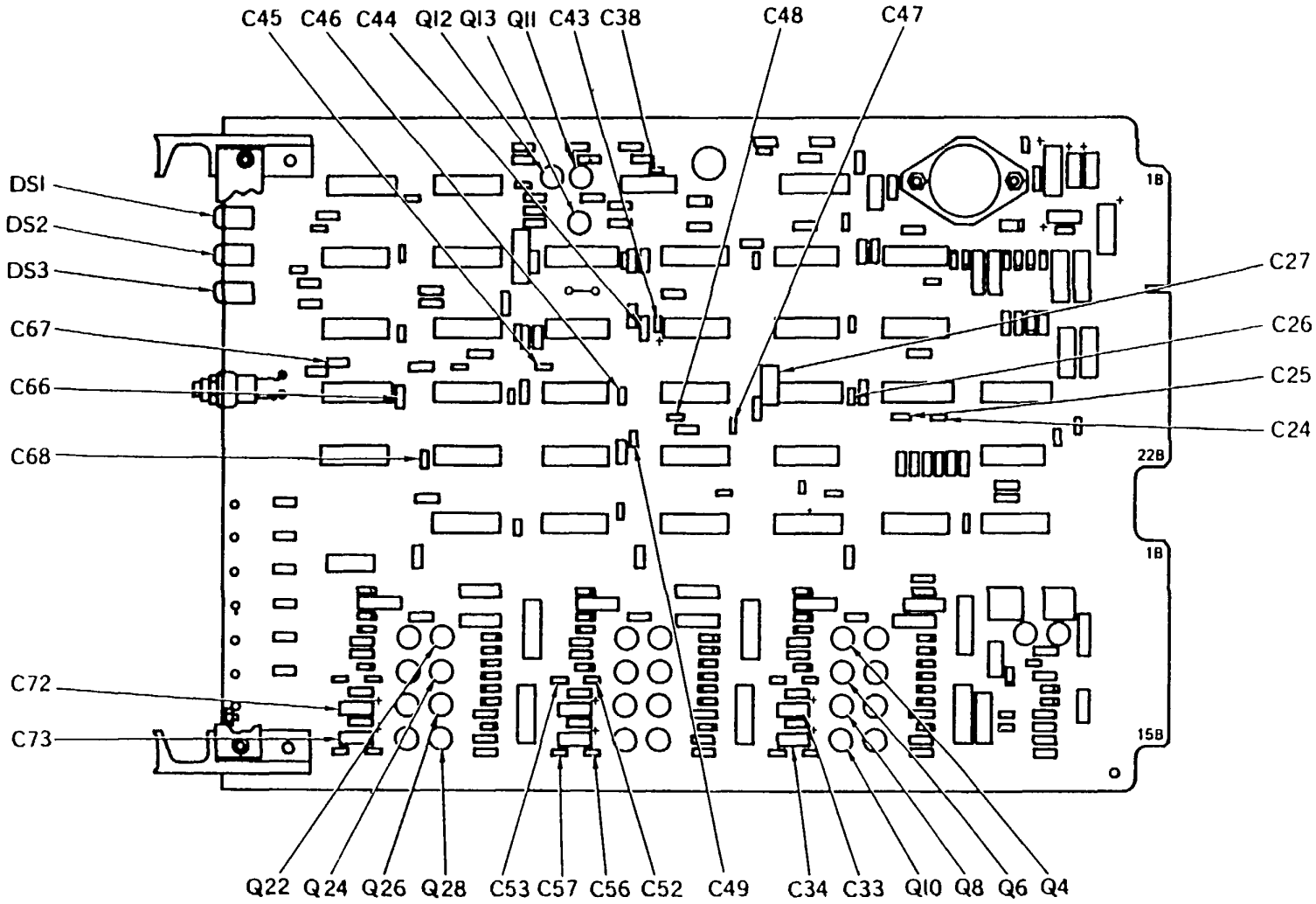


NOTE

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE

5107-003

Figure 3-9A. DRIVER unit (with bipolar loopback) parts location diagram (sheet 1 of 7)

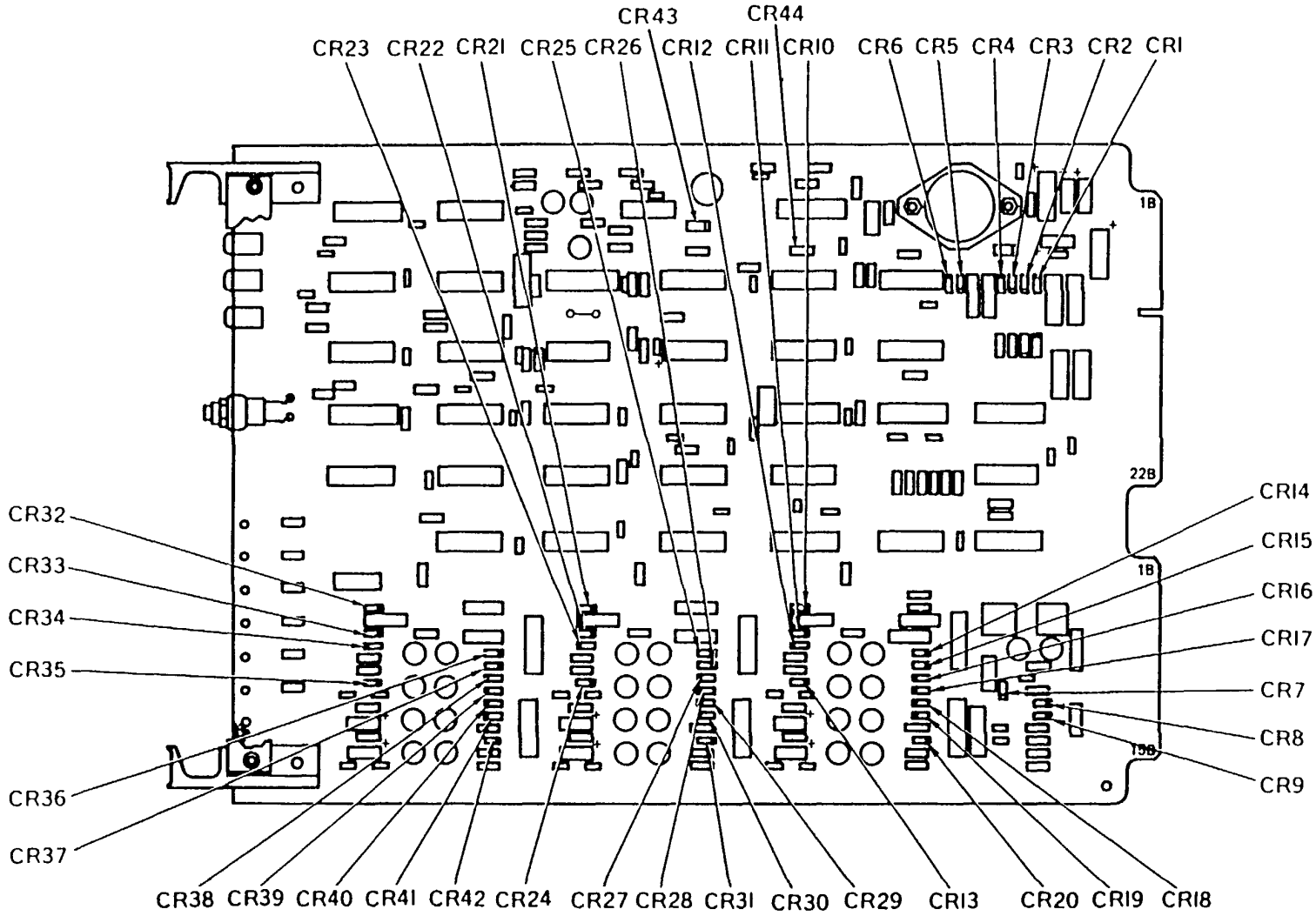


NOTE

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE

5107-004

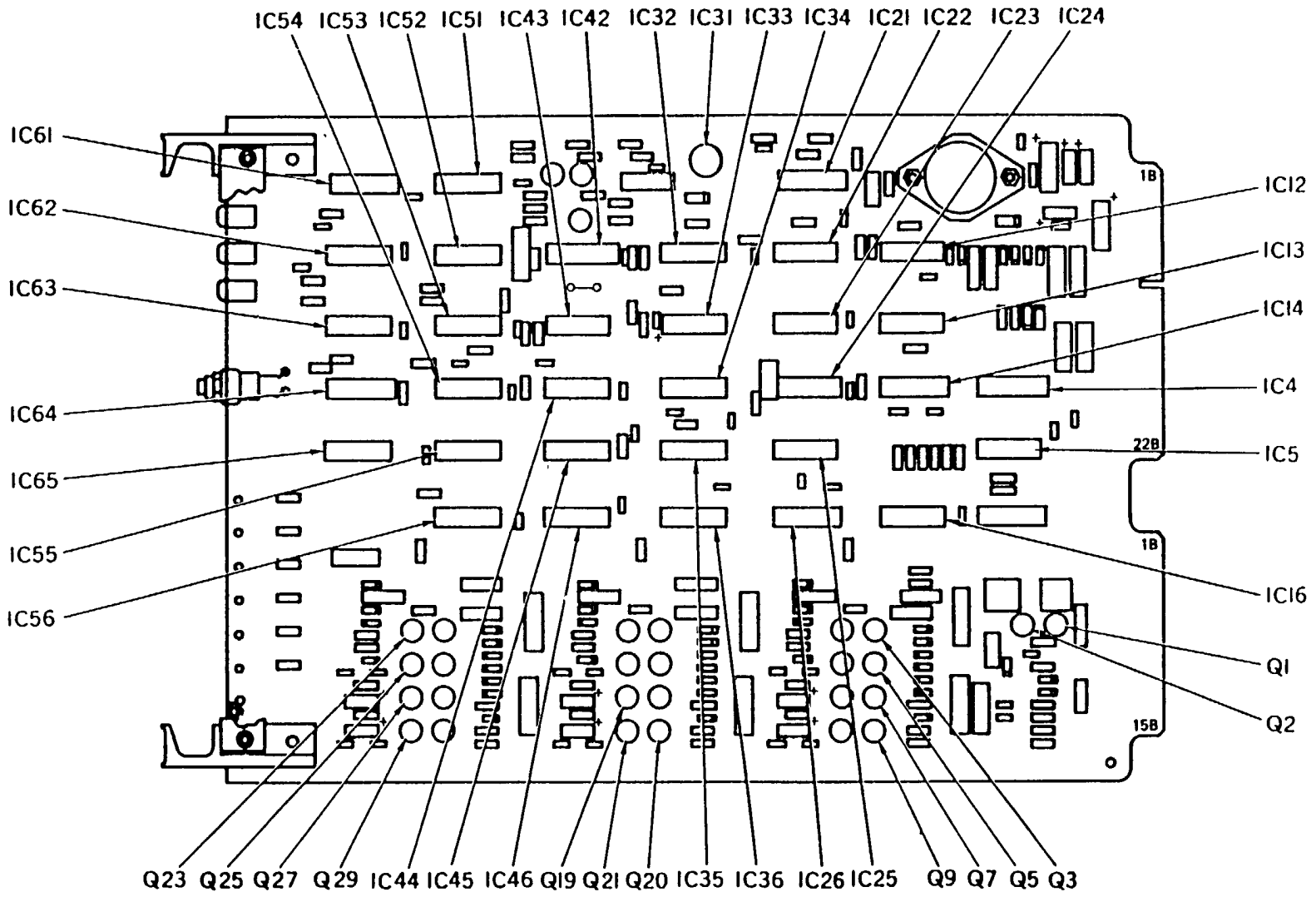
Figure 3-9A. DRIVER unit (with bipolar loopback) parts location diagram (sheet 2 of 7)



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR B-SIDE FACING, A-SIDE OPPOSITE

5107-005

Figure 3-9A. DRIVER unit (with bipolar loopback) parts location diagram (sheet 3 of 7)

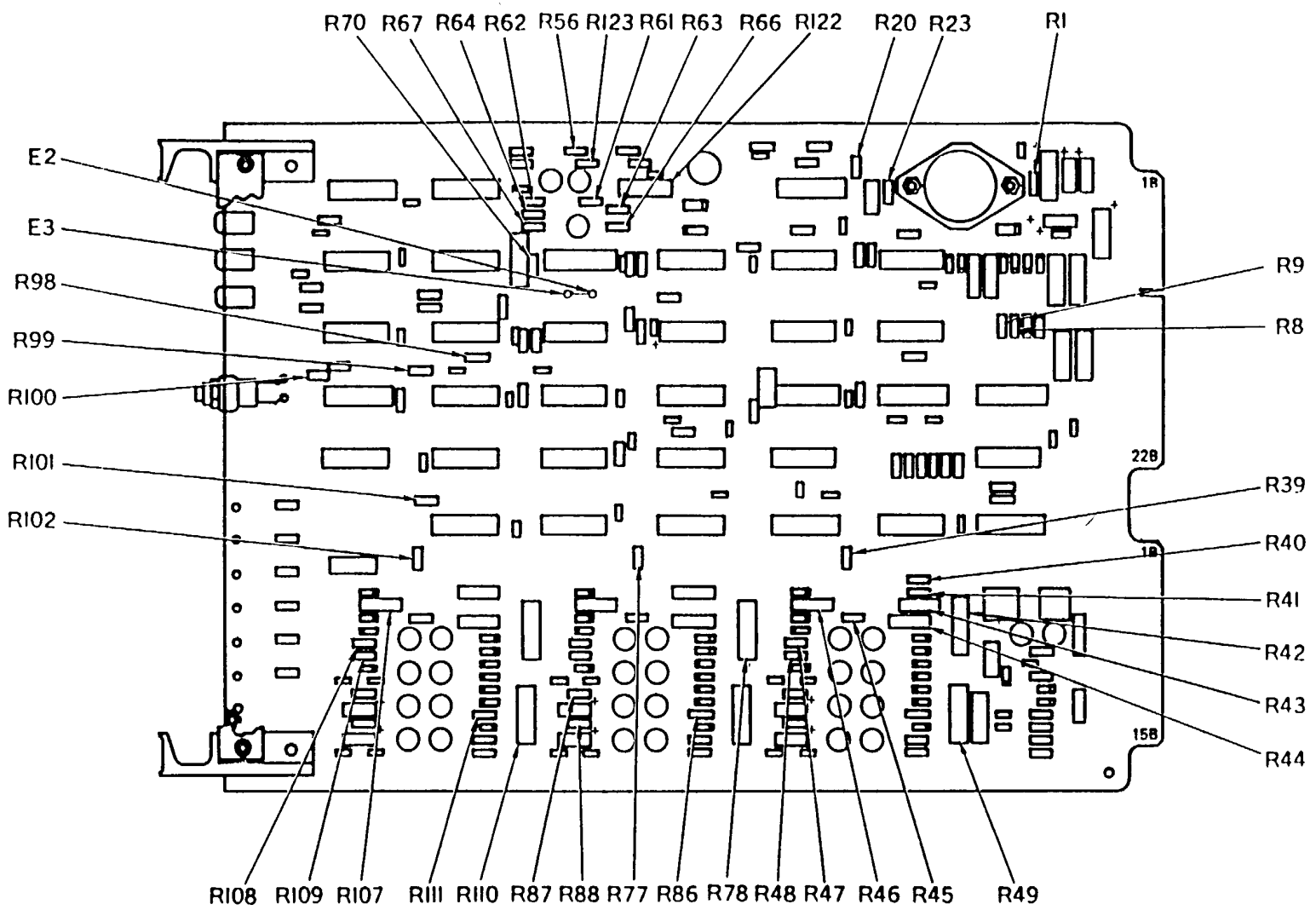


NOTE

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

5107-006

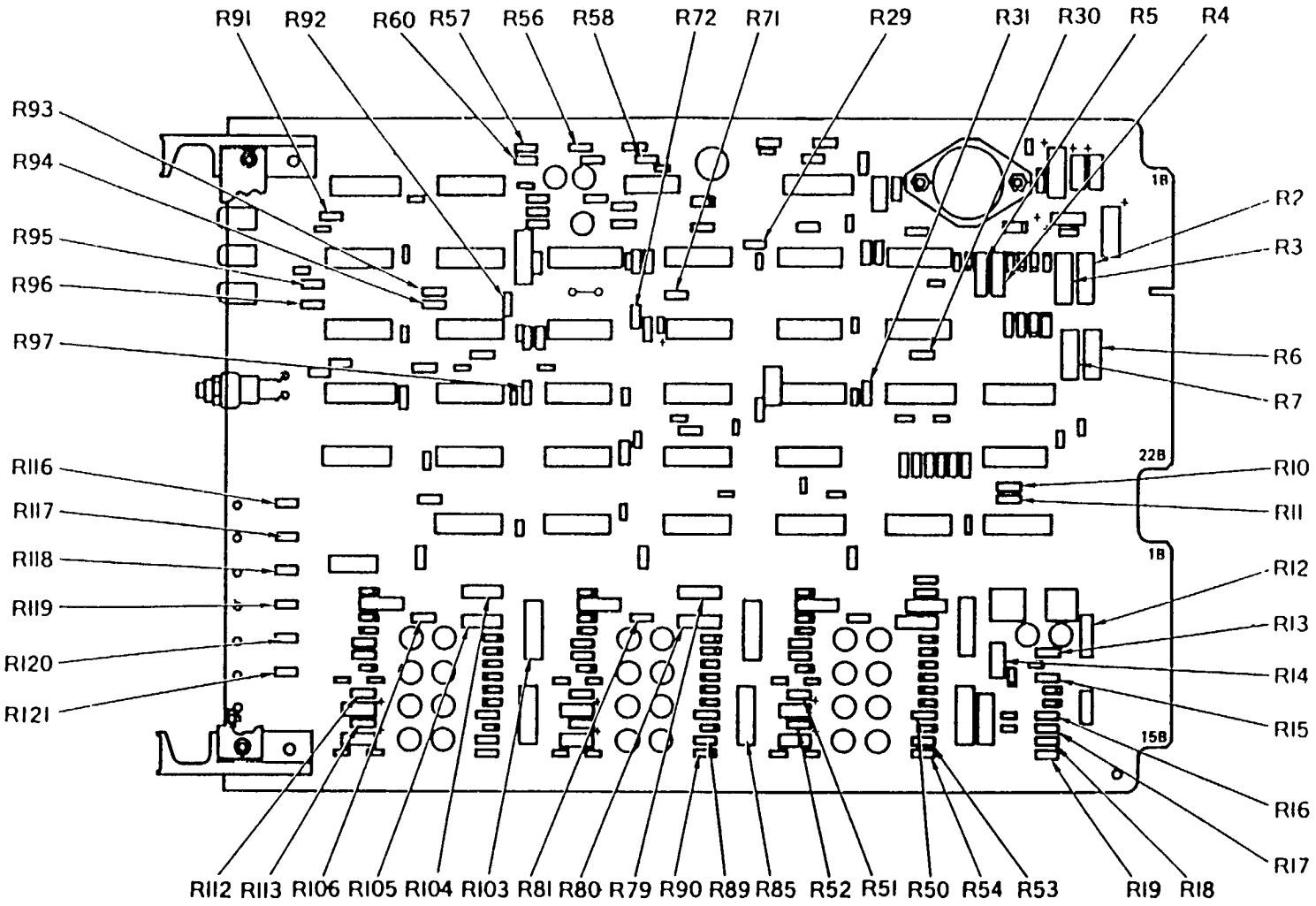
Figure 3-9A. DRIVER unit (with bipolar loopback) parts location diagram (sheet 4 of 7).



NOTE

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR B-SIDE FACING, A-SIDE OPPOSITE

Figure 3-9A. DRIVER unit (with bipolar loopback) parts location diagram (sheet 5 of 7).

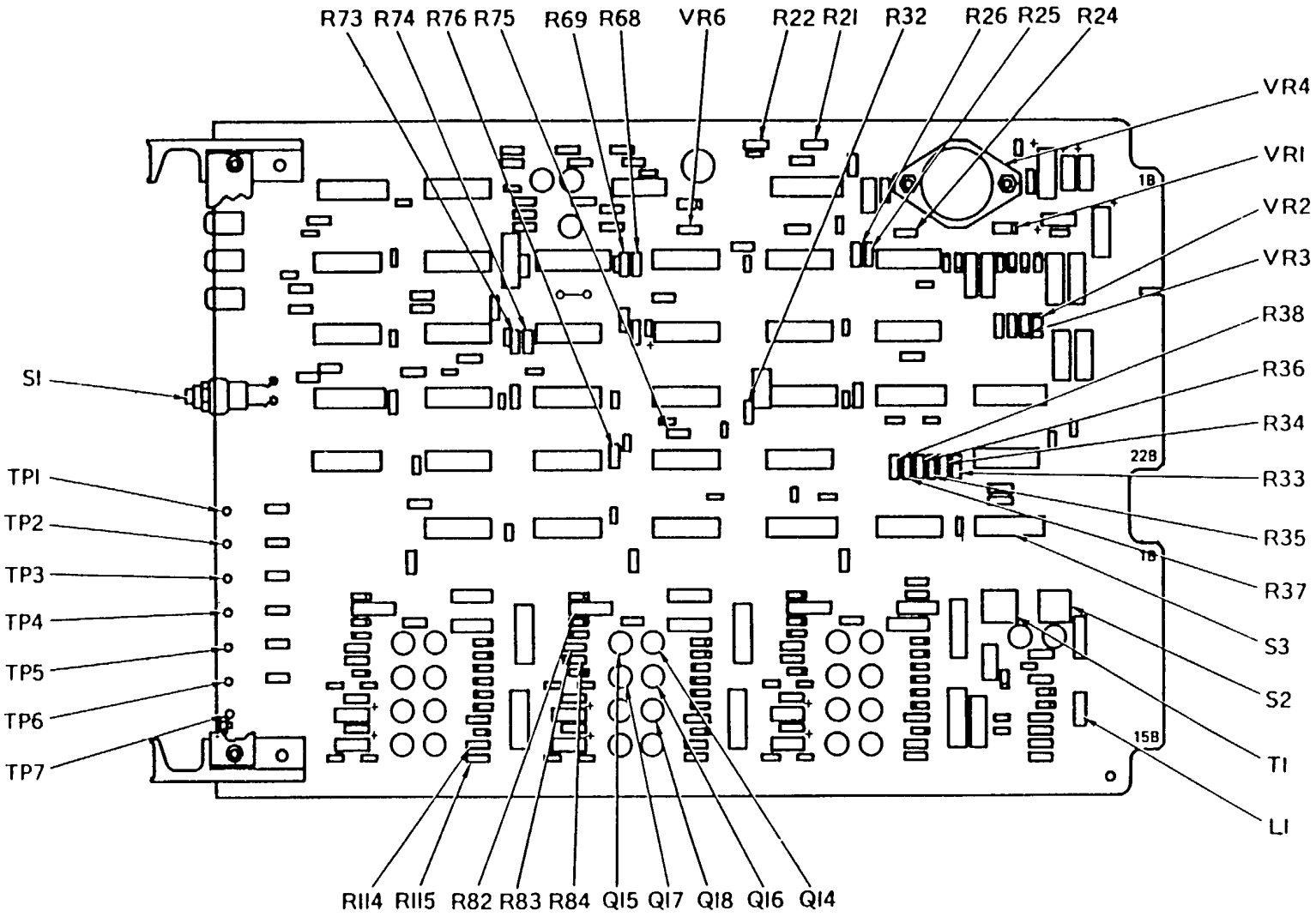


NOTE

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR B-SIDE FACING, A-SIDE OPPOSITE.

5107-008

Figure 3-9A. DRIVER unit (with bipolar loopback) parts location diagram (sheet 6 of 7)



NOTE

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR B-SIDE FACING, A-SIDE OPPOSITE

5107-009

Figure 3-9A. DRIVER unit (with bipolar loopback) parts location diagram (sheet 7 of 7)

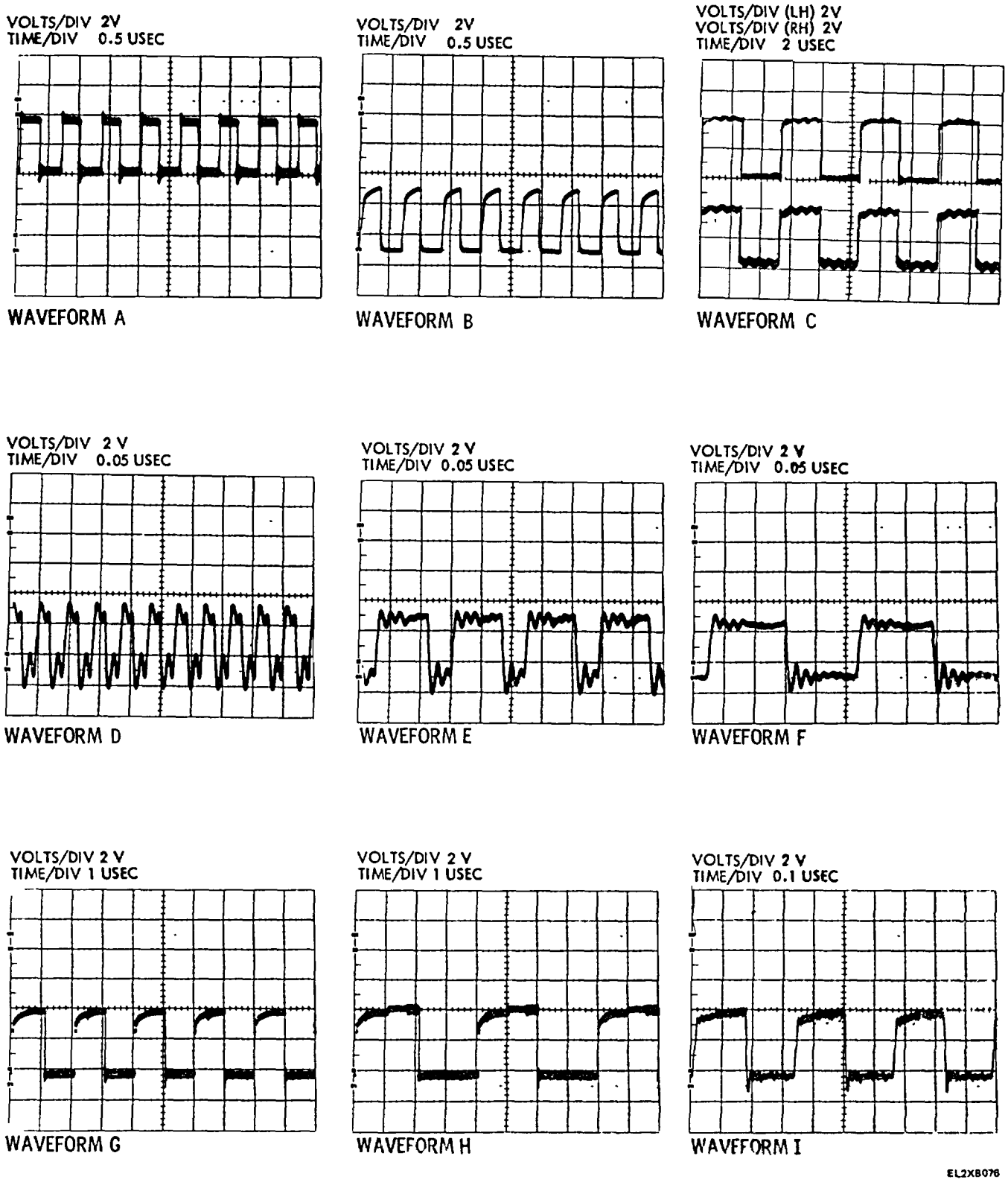


Figure 3-10. DRIVER unit troubleshooting waveforms (sheet 1 of 5).

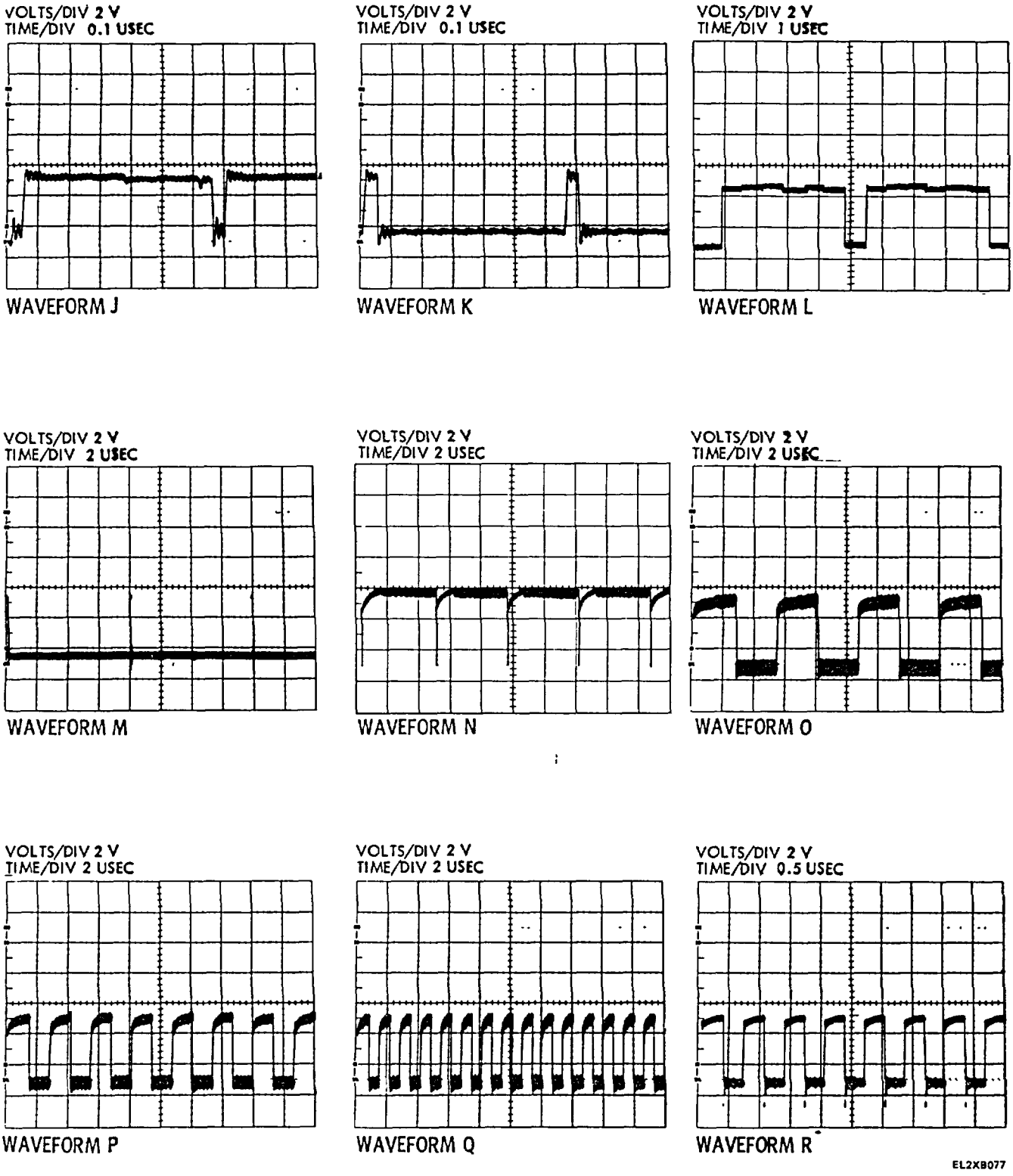


Figure 3-10. DRIVER unit troubleshooting waveforms (sheet 2 of 5).

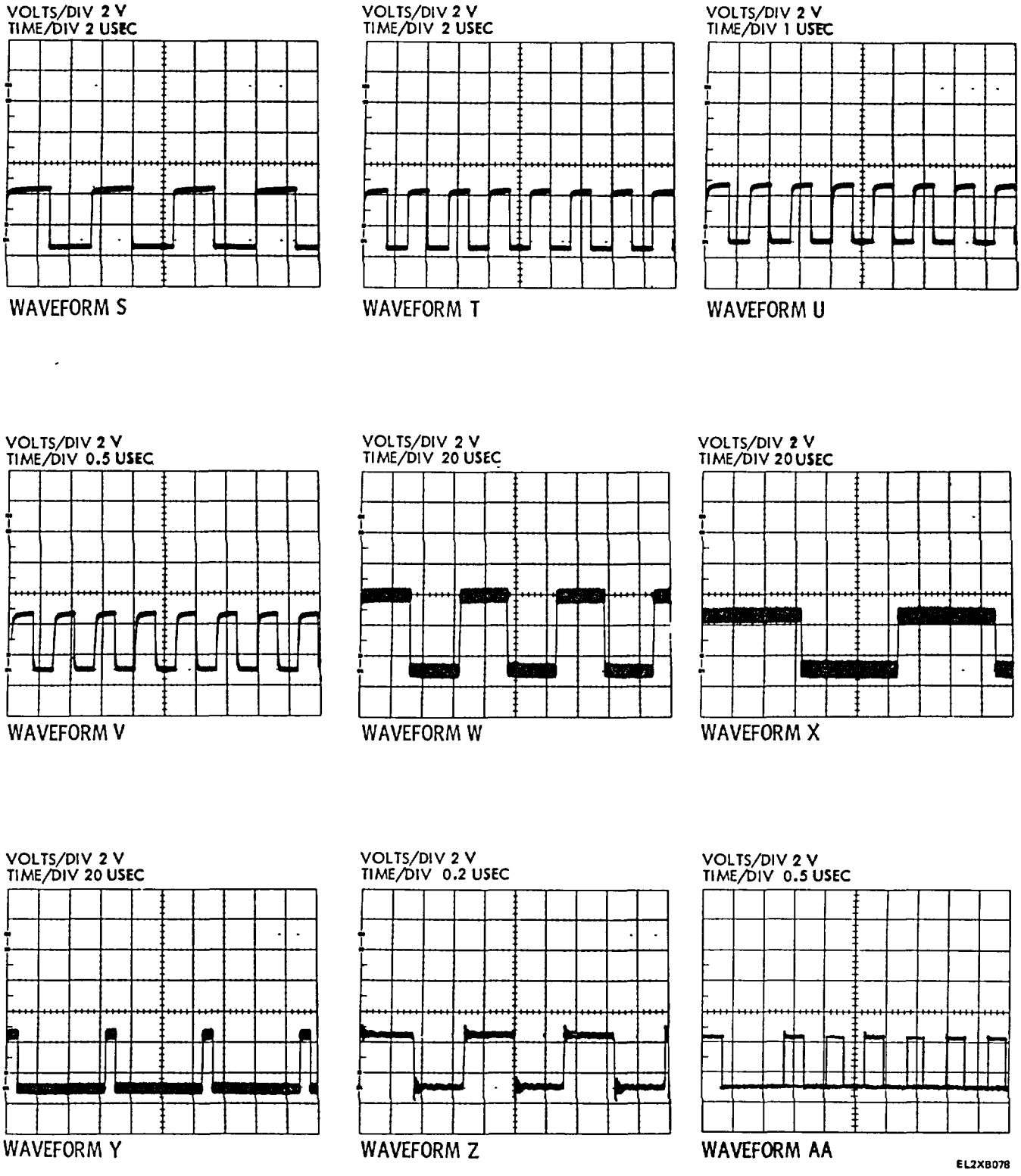


Figure 3-10. DRIVER unit troubleshooting waveforms (sheet 3 of 5).

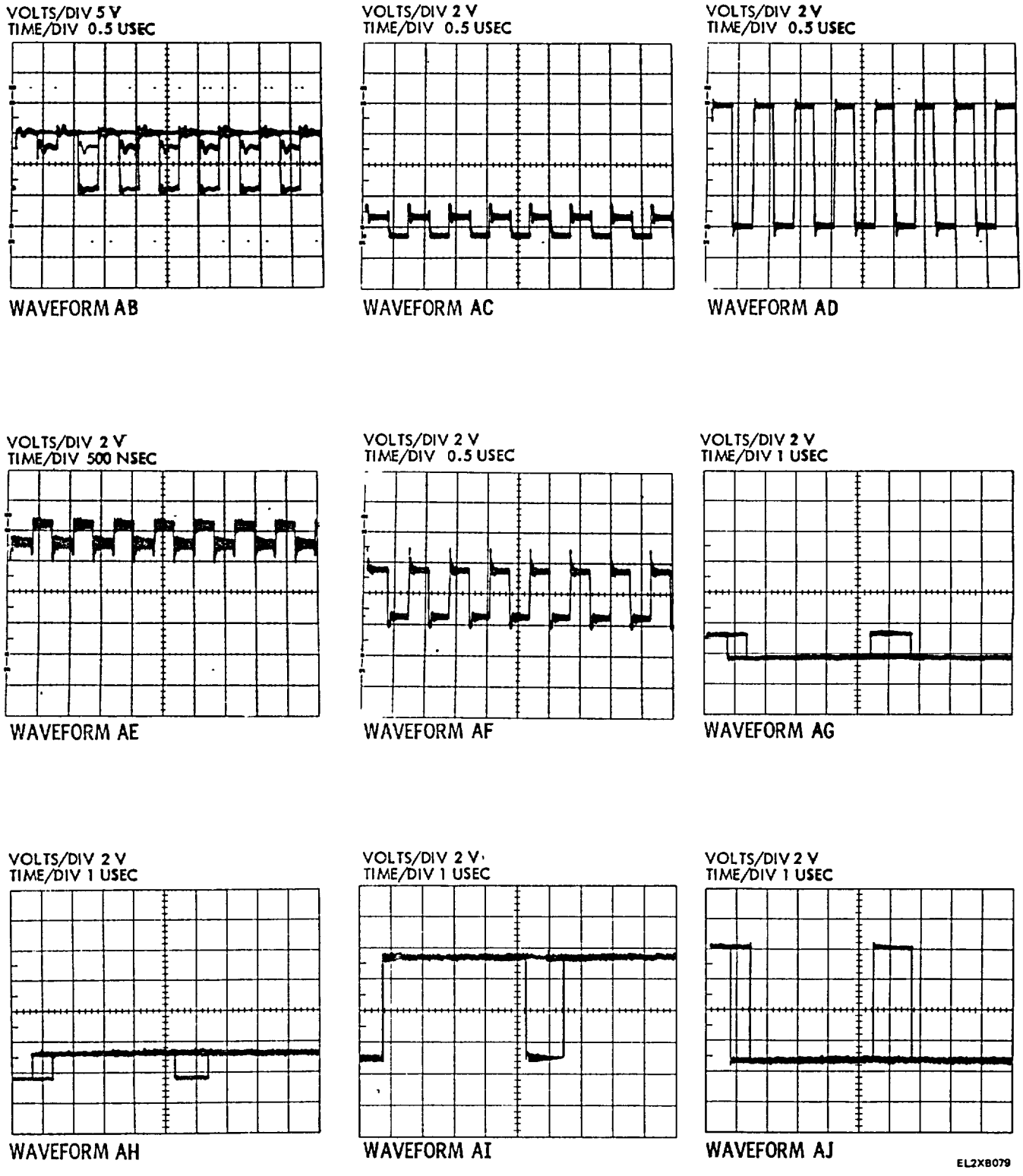


Figure 3-10. DRIVER unit troubleshooting waveforms (sheet 4 of 5).

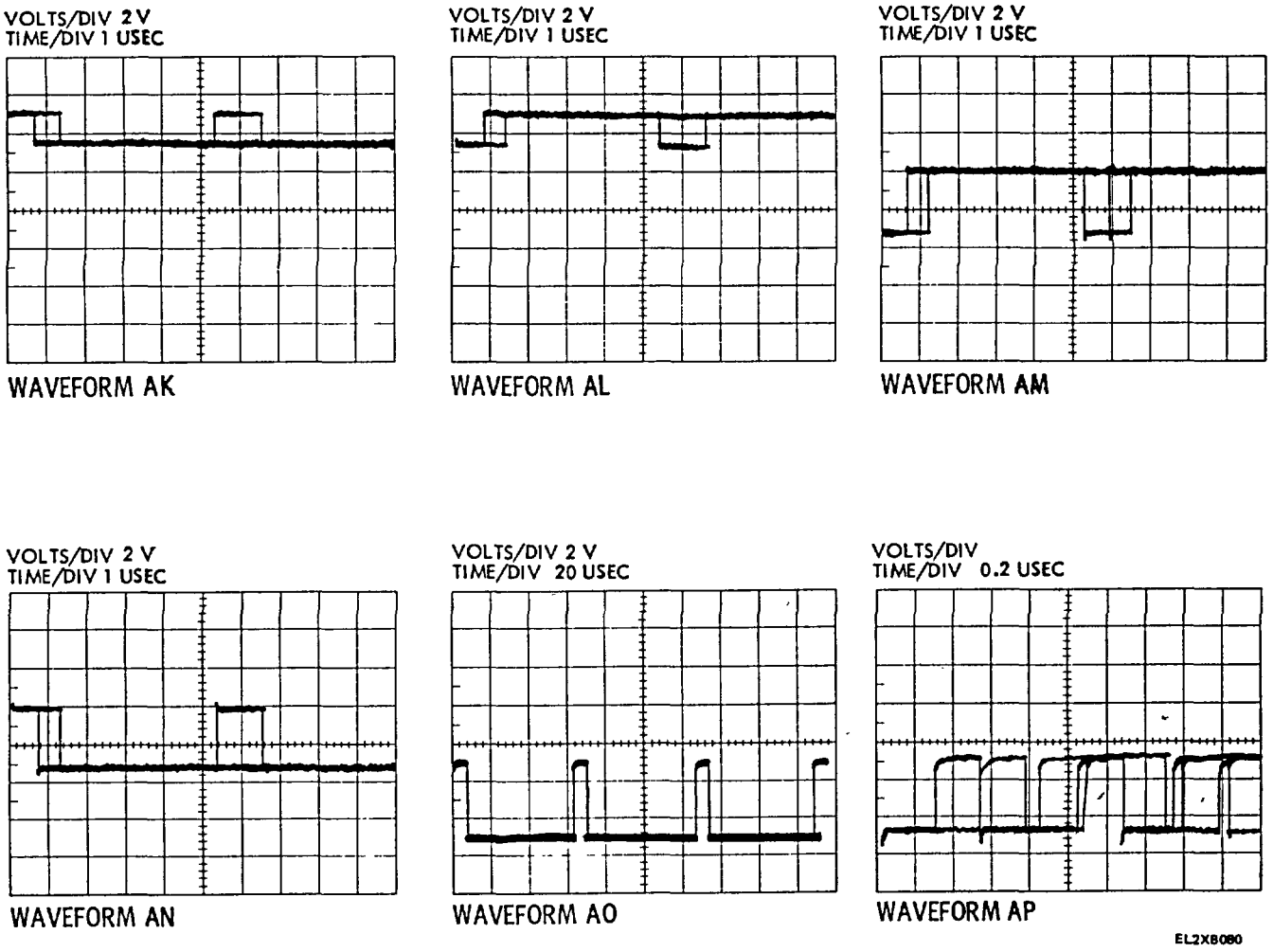


Figure 3-10. DRIVER unit troubleshooting waveforms (sheet 5 of 5).

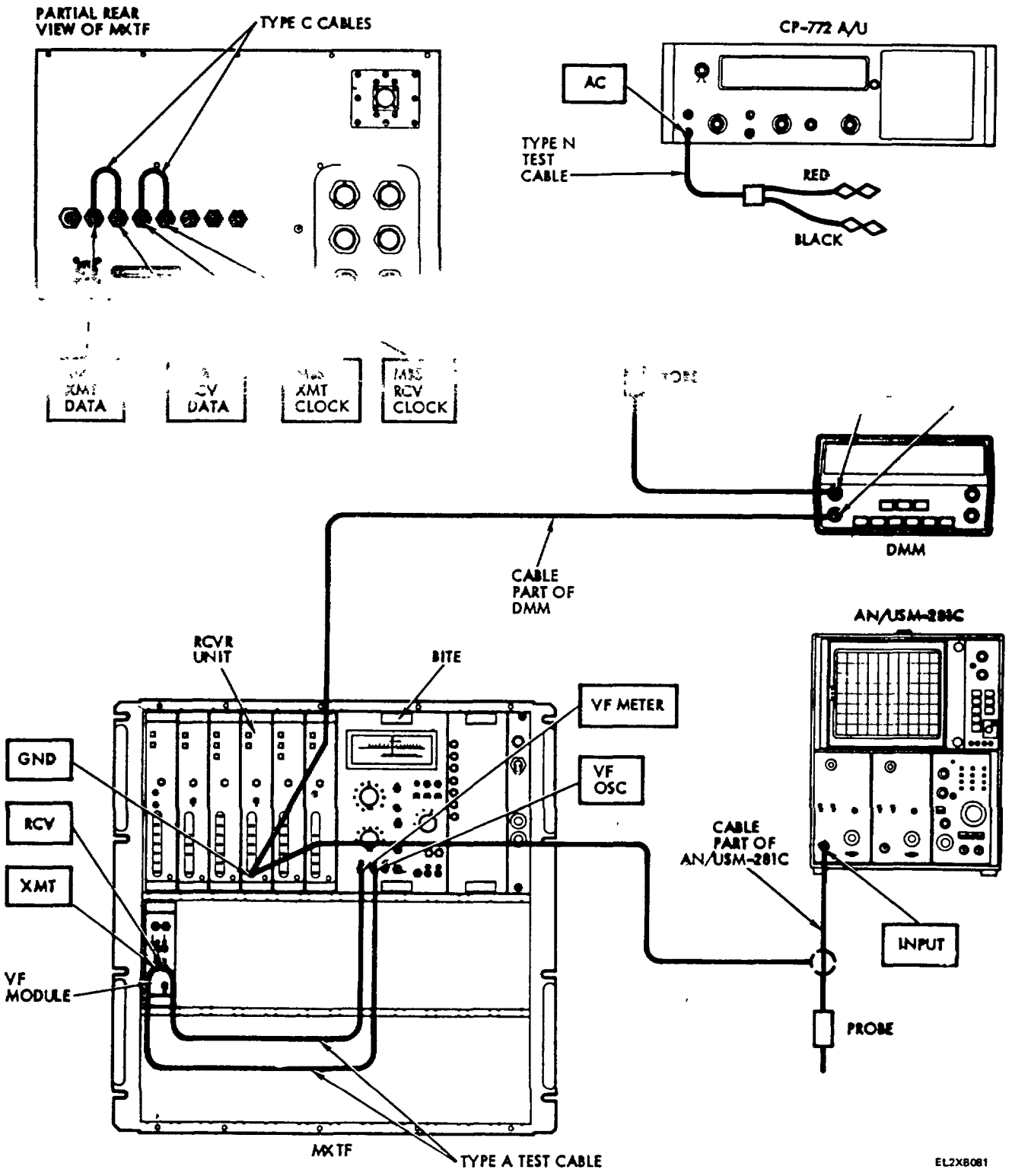


Figure 3-11. RCVR unit troubleshooting setup diagram.

3-11. Troubleshooting RCVR Unit

The following instructions and data are for use in troubleshooting faulty RCVR units. Refer to figure FO-5 and figure 3-12 for parts locations.

a. Tools and Test Equipment

(1) -100/G.
(2) AN/USM-281C.
(3) DMM.
(4) CP-772A/U.
(5) MXTF with the following accessories:
Extender board TRW 17332-010
Type C test cables (2)
Type A test cables (2)
Spare VF module
(6) 75-ohm 1/2 watt carbon resistor

b. Initial Setup. Set up the test equipment and any RCVR Input for troubleshooting as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.

(2) Insert spare VF module into channel 1 position of MXTF.

(3) Strap UUR and MXTF DRIVER for 24-channel operation (table 3-4).

(4) Remove RCVR unit from MXTF. Using extender board, install UUR in MXTF.

(5) Connect test equipment as shown in figure 3-11.

(6) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
AN/USM-281C	VOLTS/DIV (left)	2
	TIME/DIV	1 µs
	AC/GND/DC	DC
	POWER	Pull
DDM	Power	ON
CP-772A/U	SAMPLE RATE	Rotate 1/2 turn clockwise
	FUNCTION	FREQUENCY
	TIME BASE	.1 s
MXTF (PWR CONT)	Power	ON

NOTE
Allow equipment to warm up for 5 minutes before proceeding with test.

c. Fault Location. Troubleshoot in accordance with the following procedure. Reference designators within parenthesis apply to configurations RVR06 and RVR08. Reference designators not within parenthesis apply to configurations RVR02 and RVR04.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-13
1			Check reference and regulator voltages. If result of any check is incorrect, isolate and replace faulty component.	
			a. Using DMM, measure voltage at VR1 pin 2 (upper pin).	*a.* +5V ±200 mV.
			b. Using DMM, measure voltage at junction of R7 and CR1 anode.	*b.* 1.35V ±200 mV.
			c. Using DMM, measure voltage at cathode of VR3.	*c.* +2.45V ±200 mV
			d. Using DMM, measure voltage at anode of VR2.	*d.* -2.45V ±200 mV.
2			Check 78-ohm CLOCK RECEIVER and 78-ohm DATA RECEIVER circuits (IC41). If result of either check is incorrect, isolate and replace faulty component.	
			a. Check signal at IC41-9.	*a.* Waveform A.
	MXTF (MUX) 1 KHZ TONE:	ON for step	b. Check signal at IC41-4.	*b.* Waveform B.
3			Check LEVEL TRANSLATOR circuit (IC51). If result of either check is incorrect, isolate and replace faulty component.	
			a. Check signal at IC51-8.	*a.* Waveform C.
	MXTF (MUX) 1 KHZ TONE:	ON for step	*b.* Check signal at IC51-6.	*b.* Waveform D.

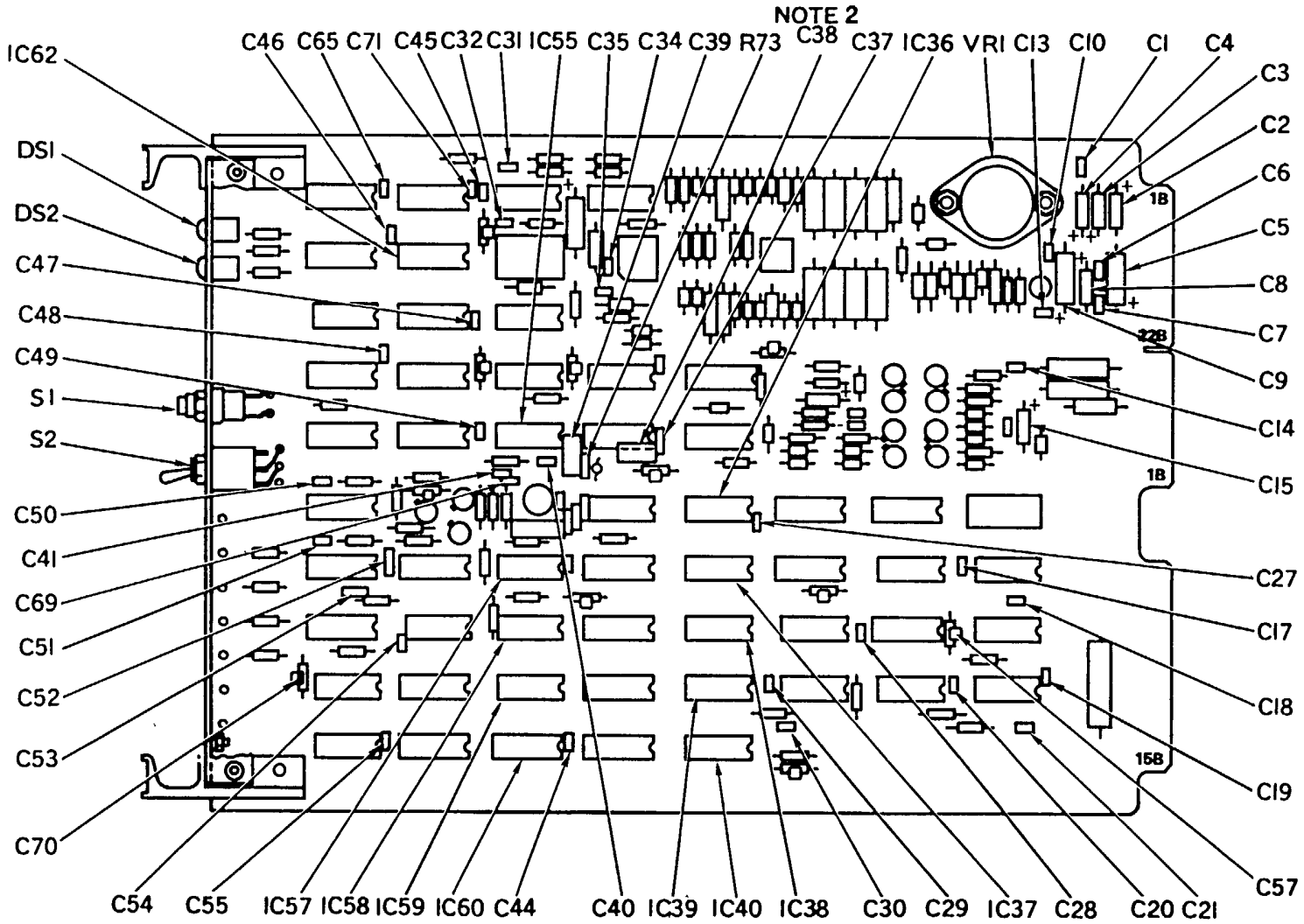
Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-13
4			Check LOOPBACK SELECT and LEVEL SHIFTER circuit (IC29, IC39, IC19, and IC9). If result of any check is incorrect, isolate and replace faulty component.	
			a. Connect DMM to P31-10B.	*a*. -3.5 to -5V.
			b. Set LOOP-NORMAL switch on URR to LOOP.	*b*. 0 to -0.8V.
			c. Set LOOP-NORMAL switch on UUR to NORMAL. Connect jumper between P31-4B and ground. Observe the following lamp conditions.	Limps illuminate.
			Unit: DRIVER, PWR SPLY — Lamp: OUTPUT LOSS, LOCAL LOOP, REMOTE LOOP, C.G.A.	
			d. Remove jumper between P31-4B and ground.	*d*. None.
5			Check BIPOLAR RECEIVER circuit (IC44 and IC54). If result of any check is incorrect, isolate and replace faulty component.	
			a. Strap UUR and DRIVER for bipolar operation (table 3-4).	*a*. None.
	AN/USM-281C			
	TIME/DIV:	2 µs	*b*. Check signal at IC44-4.	*b*. Waveform E.
			c. Check signal at IC44-9.	*c*. Waveform E.
	TIME/DIV:	1 µs	*d*. Check signal at IC54-6.	*d*. Waveform F.
6			Check BIPOLAR CLOCK RECOVERY circuit (IC53, IC74, IC73, IC63, IC53, IC65, IC75, IC54, IC64). If result of any check is incorrect, isolate and replace faulty component.	
	AN/ USM-281 C			
	TIME/DIV:	.05 µs	*a*. Check signal at IC53-4.	*a*. Waveform G.
	TIME/DIV:	.5 µs	*b*. Check signal at IC74-15.	*b*. Waveform H.
	TIME/DIV:	.1 µs	*c*. Check signal at IC74-3.	*c*. Waveform I.
	TIME/DIV:	20 µs	*d*. Check signal at IC63-6.	*d*. Waveform J.
			e. Use CP-772A/U to measure frequency at IC53-4.	*e*. 24.704 MHz -1000 Hz.
	TIME/DIV:	.2 µs	*f*. Check signal at IC65-12.	*f*. Waveform K.
	TIME/DIV:	20 µs	*g*. Check signal at IC65-13.	*g*. Waveform L. (Pulses may flicker.)
	TIME/DIV:	.2 us	*h*. Check signal at IC75-13.	*h*. Waveform M.
	TIME/DIV:	.2 us	*i*. Check signal at IC54-12.	*i*. Waveform N.
			j. Check signal at IC54-8.	*j*. Waveform N.
			k. Check signal at IC64-12.	*k*. Waveform O.
7			Check BIPOLAR DATA RECOVERY (IC55 and IC72). If result of either check is incorrect, isolate and replace faulty component.	
			a. Using DMM, check voltage at IC55-2.	*a*. 0 to -0.2 Vdc.
	AN/USM-281C			
	TIME/DIV:	2 µs	*b*. Check signal at IC72-5.	*b*. Waveform P.
	MXTF (MUX)			
	1 KHZ TONE:	ON for step		
8			Check NRZ/BIPOLAR MUX circuit (IC61). If result of any check is incorrect, replace IC61.	

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-13
	AN/USM-281C			
	TIME/DIV:	.2 μs	*a*. Check signal at IC61-4.	*a*. Waveform Q.
	TIME/DIV:	1 μs	*b*. Check signal at IC61-7.	*b*. Waveform R.
	MXTF (MUX)			
	1 KHZ TONE:	ON for step		
			c. Restrap UUR and DRIVER units for NRZ operation (table 3-4).	*c*. None.
	AN/USM-281C			
	TIME/DIV:	.2 μs	*d.* Check signal at IC61-4.	*d*. Waveform Q.
	TIME/DIV:	1 μs	*e*. Check signal at IC61-7.	*e*. Waveform R.
	MXTF (MUX)			
	1 KHZ TONE:	ON for step		
9			Check LOOP MUX circuit (IC71). If result of any check is incorrect, replace IC71.	
	AN/USM-281C			
	TIME/DIV:	.2 μs	*a*. Check signal at IC71-4.	*a*. Waveform Q.
	MXTF (MUX)			
	1 KHZ TONE:	ON for step		
	AN/USM-281C			
	TIME/DIV:	1 μs	*b*. Check signal at IC71-7.	*b*. Waveform R.
	UUR			
	LOOP-NORMAL:	LOOP		
	AN/USM-281C			
	TIME/DIV:	.2 μs	*c*. Check signal at IC71-4.	*c*. Waveform Q.
			d. Observe the following lamp conditions. Unit: DRIVER, PWR SPLY Lamp: OUTPUT LOSS, LOCAL LOOP, REMOTE LOOP, C.G.A.	*d*. Lamp illuminate.
	AN/USM-281C			
	TIME/DIV:	1 μs	*e*. Check signal at IC71-7.	*e*. Waveform R.
	MXTF (MUX)			
	1 KHZ TONE:	ON for step		
			f. Observe the following lamp conditions. Unit: DRIVER, PWR SPLY Lamp: OUTPUT LOSS, LOCAL LOOP, REMOTE LOOP, C.G.A.	*f.* Lamps illuminate.
10	*UUR*		Check PHASE DETECTER circuit (IC45, IC46, IC56 and IC57). If result of any check is incorrect, isolate and replace faulty component.	
	LOOP-NORMAL:	NORMAL		
	AN/USM-281C			
	VERT MODE:	ALT		
	TRIG SOURCE:	LEFT		
	TIME/DIV:	1 μs	*a*. Connect left probe to IC57-1 and right probe to IC57-3.	*a.* Waveform S.
			b. Using DMM, measure voltage at cathode of VR5.	*b.* 3.5 ±1V.
	TIME/DIV:	.05 μs	*c*. Check signal at IC45-10.	*c.* Waveform T.
	VERT MODE:	LEFT		
			d. Using CP-772A/U, measure frequency at IC46-3.	*d.* 24.704 MHz +500 Hz.
	AN/USM-281C			
	TIME/DIV:	2 us	*f.* Check signal at IC57-2.	*f.* Waveform V
	VOLTS/DIV:	5		
			g. Check signal at IC57-13.	*g.* Waveform W.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-13
11			Check 24.704 MHz VCO circuit (IC45) and CLOCK SOURCE SELECT circuit (IC40 and IC46). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281 C			
	VOLTS/DIV:	2	*a.* Check signal at IC45-10.	*a.* Waveform X.
	TIME/DIV:	.05 µs		
			b. Check signal at IC46-6.	*b.* Waveform Y.
			c. Check signal at IC46-3.	*c.* Waveform U.
12			Check CLOCK DIVIDER CHAINS circuit (IC18, IC26, IC27, IC28, IC37, IC38, IC47, IC48 and IC49). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C		*a*. Check signal at IC38-4.	*a.* Waveform Z.
	TIME/DIV:	2 µs	*b*. Check signal at IC39-4.	*b*. Waveform AA.
	TIME/DIV:	2 µs	*c*. Check sign 1l it IC39-1.	*c.* Waveform AB.
			d. Check signal at IC28-8.	*d.* Waveform AC.
	TIME/DIV:	1 µs	*e*. Check signal at IC27-13.	*e.* Waveform AD.
			f. Check signal at IC27-12.	*f.* Waveform AE.
			g. Check signal at IC27-11.	*g.* Waveform AF.
	TIME/DIV:	.05 µs	*h*. Check signal at IC58-8.	*h.* Waveform AG.
	TIME/DIV:	1 µs	*i.* Check signal at IC28-5.	*i.* Waveform AH.
	TIME/DIV:	.5 µs	*j.* Check signal at IC26-12.	*j.* Waveform AI.
	TIME/DIV:	1 µs	*k*. Check signal at IC26-11.	*k*. Waveform AJ.
	TIME/DIV:	.2 µs	*l.* Check signal at IC18-11.	*l.* Waveform AK.
13			Check CLK SOURCE SELECT circuit. If result of any check is incorrect, isolate and replace faulty component.	
			NOTE **Ignore any fault lamps which may light during this test.**	
			a. Set switches S3-1, -2, -3, -4, -5, -6, and -8 to open position.	*a.* None.
			b. Using DMM, measure voltage to P7-20A.	*b*. 0 to -0.8V.
			c. Set S3-8 to closed position.	*c.* -5 Vdc ±500 mV.
			d. Using DMM, measure voltage to P7-22B.	*d.* 0 to -0.8 Vdc.
			e. Set S3-1 to closed position.	*e.* -5V ±500 mV.
			f. Using DMM, measure voltage to P7-21B.	*f.* 0 to -0.8V.
			g. Set S3-2 to closed position.	*g.* -5V ±500 mV.
			h. Using DMM, measure voltage to P7-19A.	*h.* 0 to -0.8V.
			i. Set S3-3 to closed position.	*i.* -5V ±500 mV.
			j. Using DMM, measure voltage to P7-20B.	*j.* 0 to -0.8V.
			k. Set S3-4 to closed position.	*k*. -5 -±500 mV.
			l. Using DMM, measure voltage to P7-14A.	*l.* 0 to -0.8V.
			m. Set S3-5 to closed position.	*m*. -5V ±500 mV.
			n. Using CP-722, measure frequency at MBS CLK OUT test point on UUR. Observe condition of FRAME LOSS lamp on DEMUX unit.	*n.* 1.544 MHz ±20 Hz. Lamp out.
			o. Strap UUR and DRIVER units for 3-channel operation (table 3-4).	*o.* None.
			p. Using CP-772A/U, measure frequency at MBS CLK OUT test point. Observe condition of FRAME LOSS lamp on UUR.	*p.* 192 kHz ±100 Hz. Lamp out.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-13
			q. Strap UUR and DRIVER units for 6-channel operation (table 3-4).	*q.* None.
			r. Using CP-772A/U, measure frequency at MBS CLK OUT test point. Observe condition of FRAME LOSS lamp on DEMUX unit.	*r.* 384 kHz ±100Hz. Lamp out.
			s. Strap UUR and DRIVER units for 12-channel operation (table 3-4).	*s.* None.
			t. Using CP-772A/U, measure frequency at MBS CLK OUT test point. Observe condition of FRAME LOSS lamp on DEMUX unit.	*t.* 768 kHz ±100 Hz. Lamp out.
			u. Using CP-772A/U, measure frequency at P31-3A.	*u.* 4.096 MHz ±100 Hz.
			v. Set S3-1, -2, -3, -4 and -5 to open position.	*v.* None.
			w. Using DMM, measure voltage at P7-17A, P7-18A and P7-16A	*w.* P7-17A -4 to -5V. P7-18A -4 to -5V. P7-16A -4 to -5V.
			x. Set S3-2 to closed condition and using DMM, check P7-17A, P7-18A and P7-16A.	*x.* P7-17A -4 to -5V. P7-18A 0 to -1V. P7-16A -4 to -5V.
			y. Set S3-2 to open position.	*y.* None.
			z. Set S3-4 to closed position.	*z.* None.
			aa. Using DMM, measure voltage at P7-17A, P7-18A and P7-16A. P7-16A 0 to -1V.	*aa*. P7-17A -4 to -5V. P7-18A -4 to -5V.
			ab. Set S3-4 to open position.	*ab*. None.
			ac. Set S3-5 to closed position and using DMM, check P7-17A, P7-18A P7-16A.	*ac*. P7-17A 0 to -1V. and P7-18A -4 to -5V. P7-16A 0 to -1V.
			ad. Strap DRIVER unit for 24-channel operation (table 3-4).	*ad*. None.
14			Check CLOCK MUX circuit (IC16). If result of either check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	.2 μs	*a*. Check signal at IC37-3.	*a.* Waveform AK.
			b. Check signal at MBS CLK OUT test point.	*b*. Waveform AN.
15			Check FIFO INPUT CONTROL circuit (IC39, IC59 and IC68). If result of either check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	.2 μs	*a.* Check signal at IC39-3.	*a.* Waveform AL.
	TIME/DIV:	2 μs	*b*. Check signal at IC68-8.	*b*. Waveform AM.
16			Check FIFO OUTPUT CONTROL circuit (IC59 and IC68). If either check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	.2 μs	*a.* Check signal at IC59-6.	*a.* Waveform AN.
	TIME/DIV:	2 μs	*b*. Check signal at IC68-6.	*b*. Waveform AO.
17			Check FIFO circuit (IC69, IC70 and IC80). If result of any check is incorrect, isolate and replace faulty component.	
			a. Check signal at IC80-3.	*a.* Waveform AP.
			b. Check signal at IC80-4.	*b*. Waveform AP.
			c. Check signal at IC80-5.	*c.* Waveform AP.
			d. Check signal at IC80-6.	*d.* Waveform AP.
			e. Check signal at IC80-10.	*e.* Waveform AP.
			f. Check signal at IC80-11.	*f.* Waveform AP.
			g. Check signal at IC80-12.	*g.* Waveform AP.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-13
			h. Check signal at IC80-13.	*h*. Waveform AP.
	TIME/DIV:	5 µs	*i.* Check signal at IC69-14.	*i.* Waveform AQ.
			f. Check signal at IC69-13.	*j.* Waveform AQ.
			k. Check signal at IC69-12.	*k*. Waveform AQ.
			l. Check signal at IC69-11.	*L*. Waveform AQ.
			m. Check signal at IC70-14.	*m*. Waveform AQ.
			n. Check signal at IC70-13.	*n*. Waveform AQ.
			o. Check signal at IC70-12.	*o*. Waveform AQ.
			p. Check signal at IC70-11.	*p*. Waveform AQ.
	TIME/DIV:	2 µs	*q.* Check signal at MBS DATA OUT test point on UUR.	*q*. Waveform AR.
18			Check operation of FRAME SEARCH INHIBIT circuit (IC9, IC19 and IC29). If either check is incorrect, isolate and replace faulty component.	
			a. Using DMM, measure voltage IC29-2.	*a.* -4 to -5V.
			b. Connect jumper wire from P31-2B to ground. Using DMM, measure voltage at IC29-2.	*b.* 0 to -0.8V.
19			Check 75-ohm DRIVER circuit (Q1, IC35). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C		*a*. Connect a 75-ohm watt carbon	*a.* Waveform AS.
	TIME/DIV:	50 µs	resistor between P31-1B and ground. Disconnect type C cable from RCV MBS DATA connector on rear of MXTF. Connect AN/USM-281C probe to P31-1B.	
			Check BAL REC RCV CLKC DRIVER circuit (Q2-Q9). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281 C			
	TIME/DIV:	1 µs	*b*. Check waveform at collector of Q3.	*b*. Waveform AT.
			c. Check waveform at collector of QS.	*c*. Waveform AT.
			d. Check waveform at collector of Q2.	*d*. Waveform AU.
			e. Check waveform at collector of Q4.	*e*. Waveform AU.
			f. Check waveform at P7-15B.	*f.* Waveform AV.
			g. Check waveform at P7-15A.	*g*. Waveform AV.



NOTES:

1. 22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING A-SIDE OPPOSITE.
2. PART OF CONFIGURATION RVR04 ONLY.

EL2XB082

Figure 3-12. RCVR unit parts location diagram (sheet 1 of 10) RVR02 and RVR04.

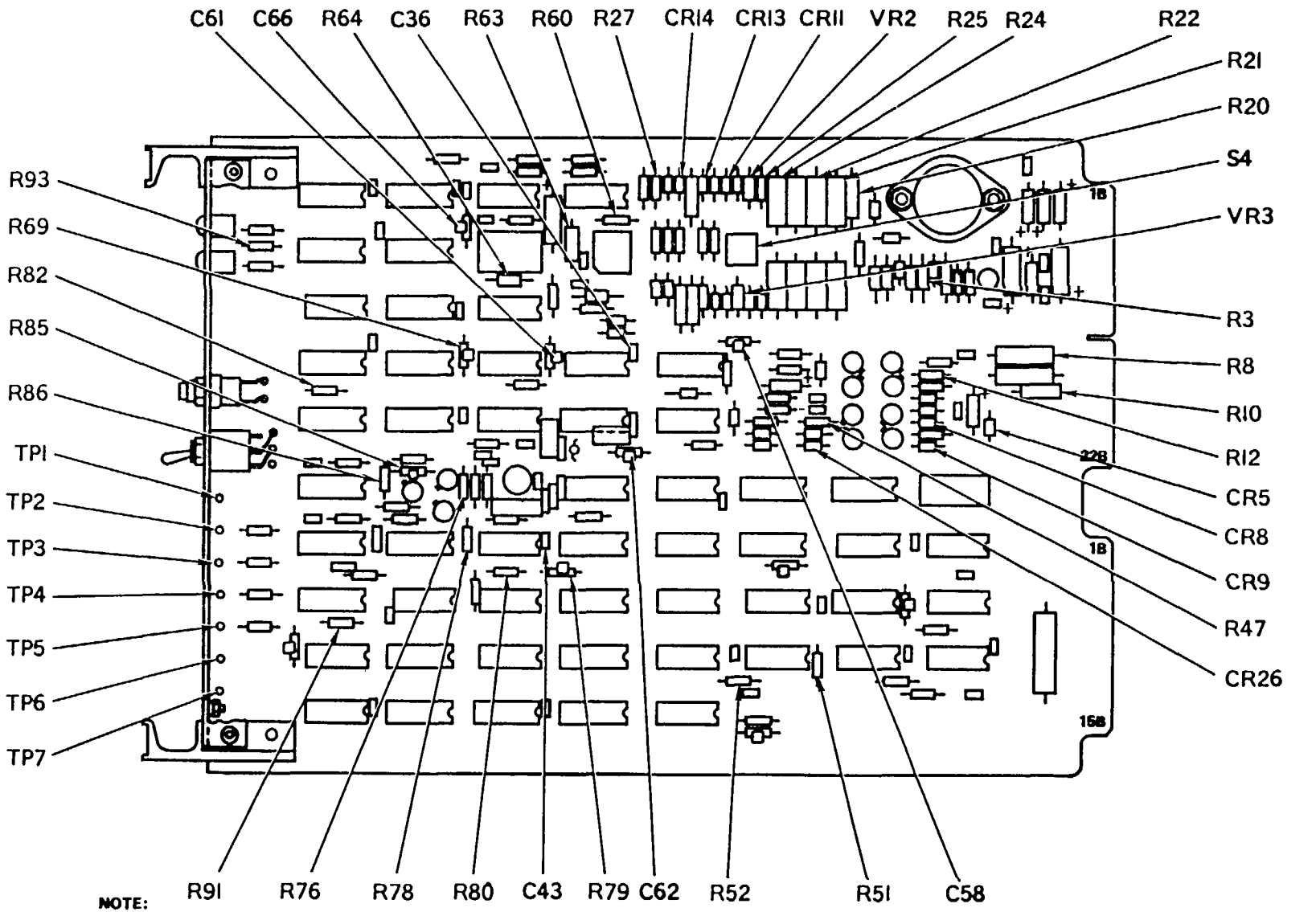


Figure 3-12. RCVR unit parts location diagram (sheet 2 of 10) RVR02 and RVR04.

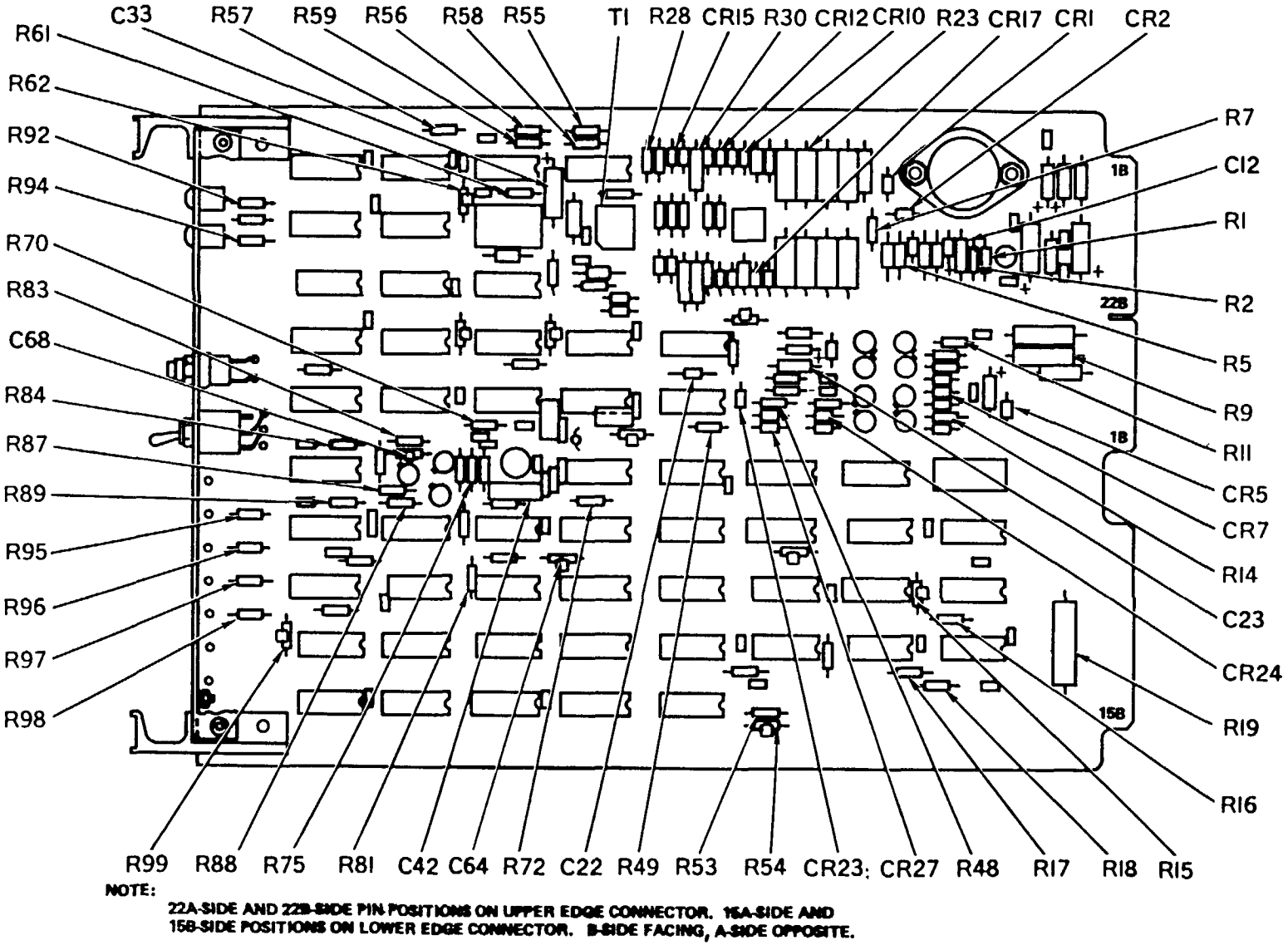


Figure 3-12. RCVR unit parts location diagram (sheet 3 of 10) RVR02 and RVR04.

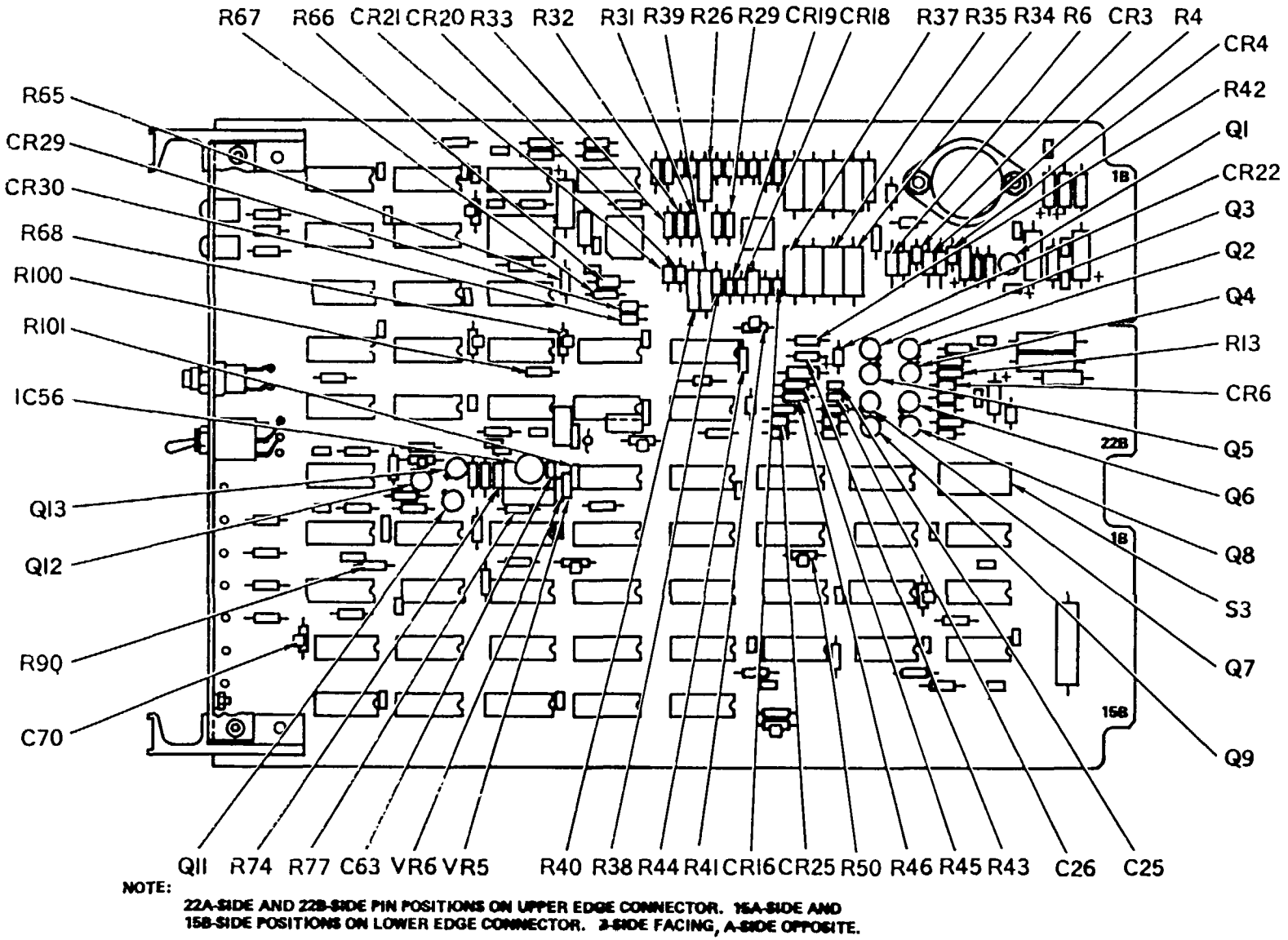


Figure 3-12. RCVR unit parts location diagram (sheet 4 of 10) RVR02 and RVR04.

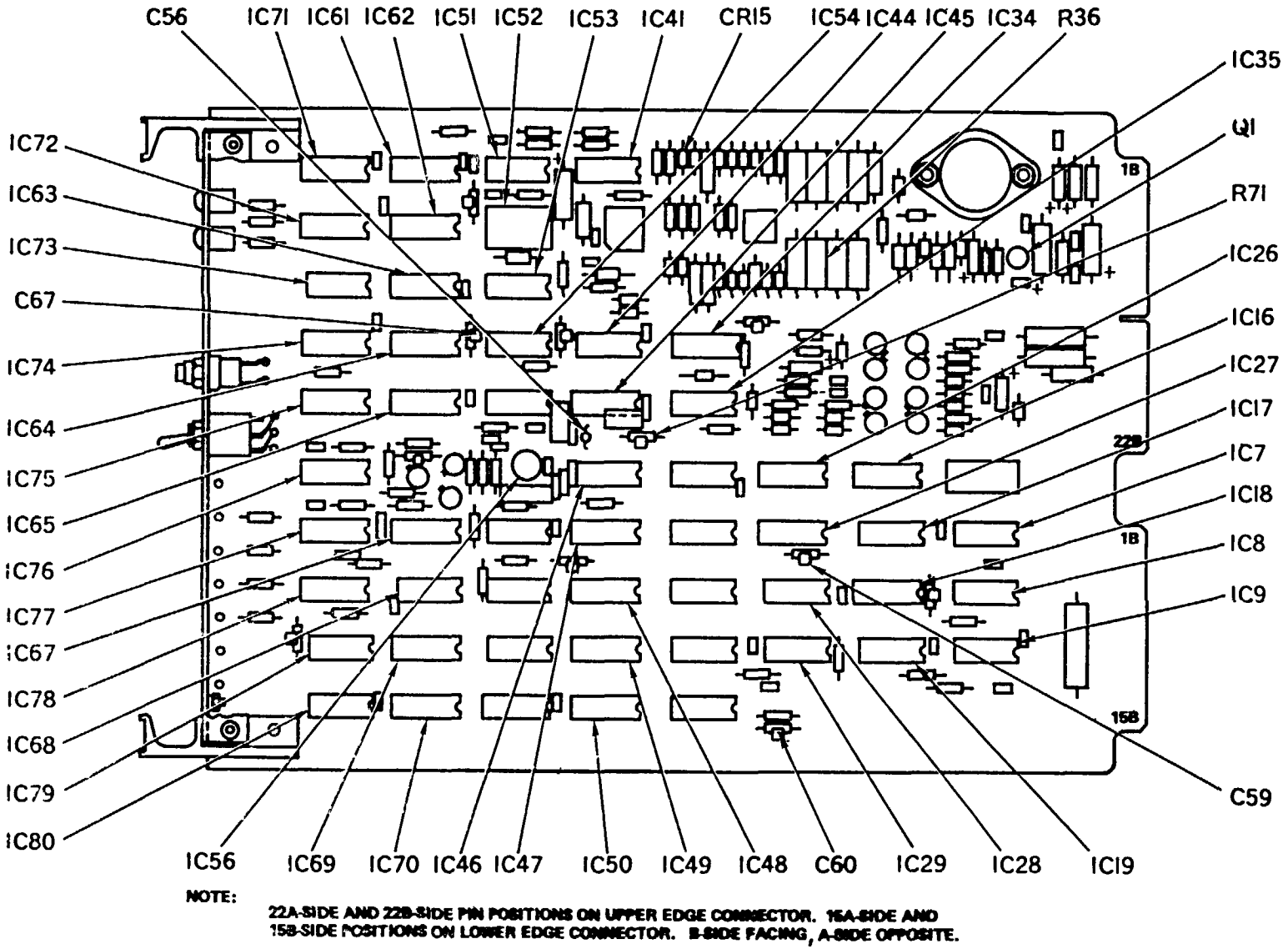
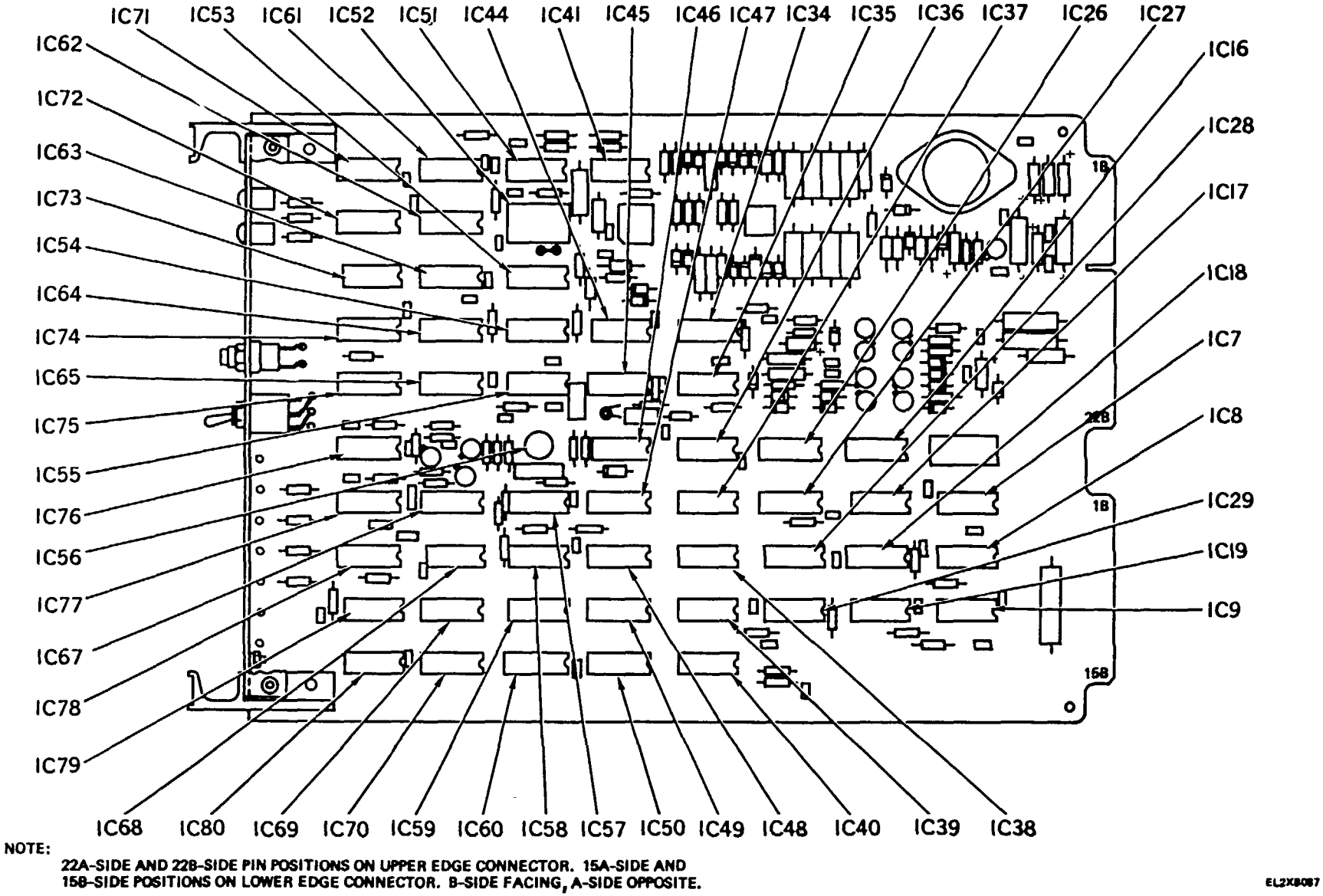


Figure 3-12. RCVR unit parts location diagram (sheet 5 of 10) RVR02 and RVR04.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

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Figure 3-12. RCVR unit parts location diagram (sheet 6 of 10) RVR02 and RVR04.

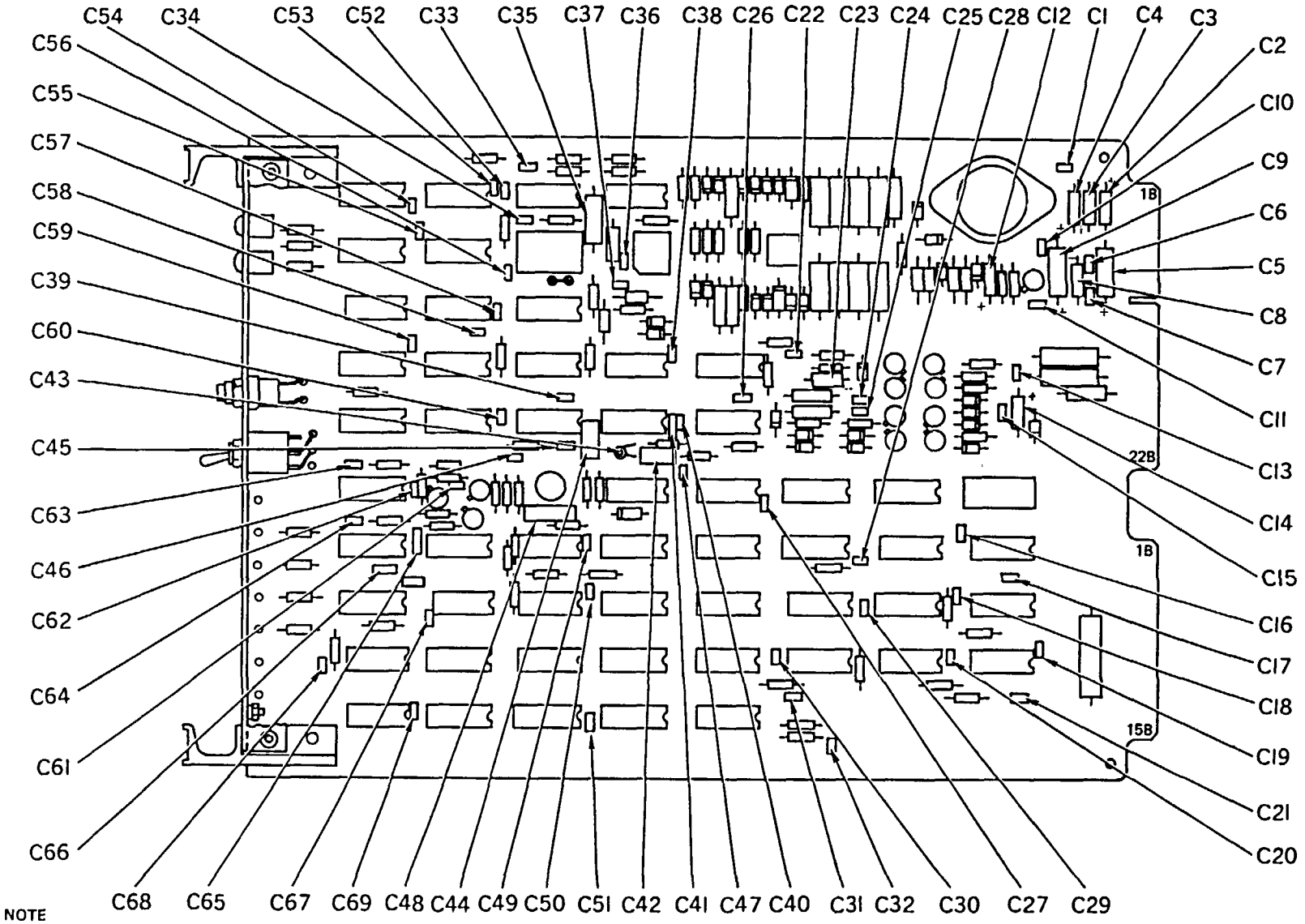
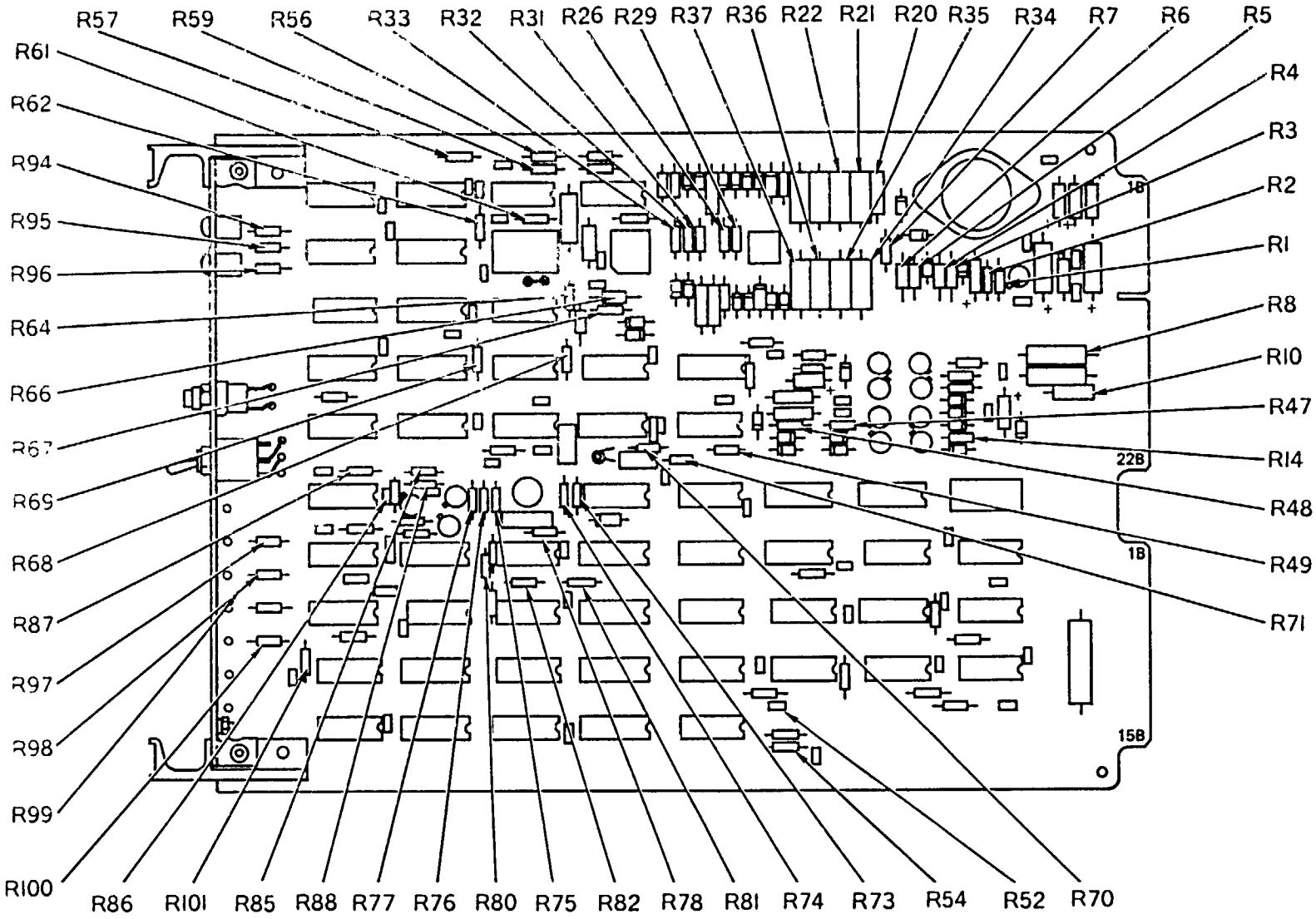


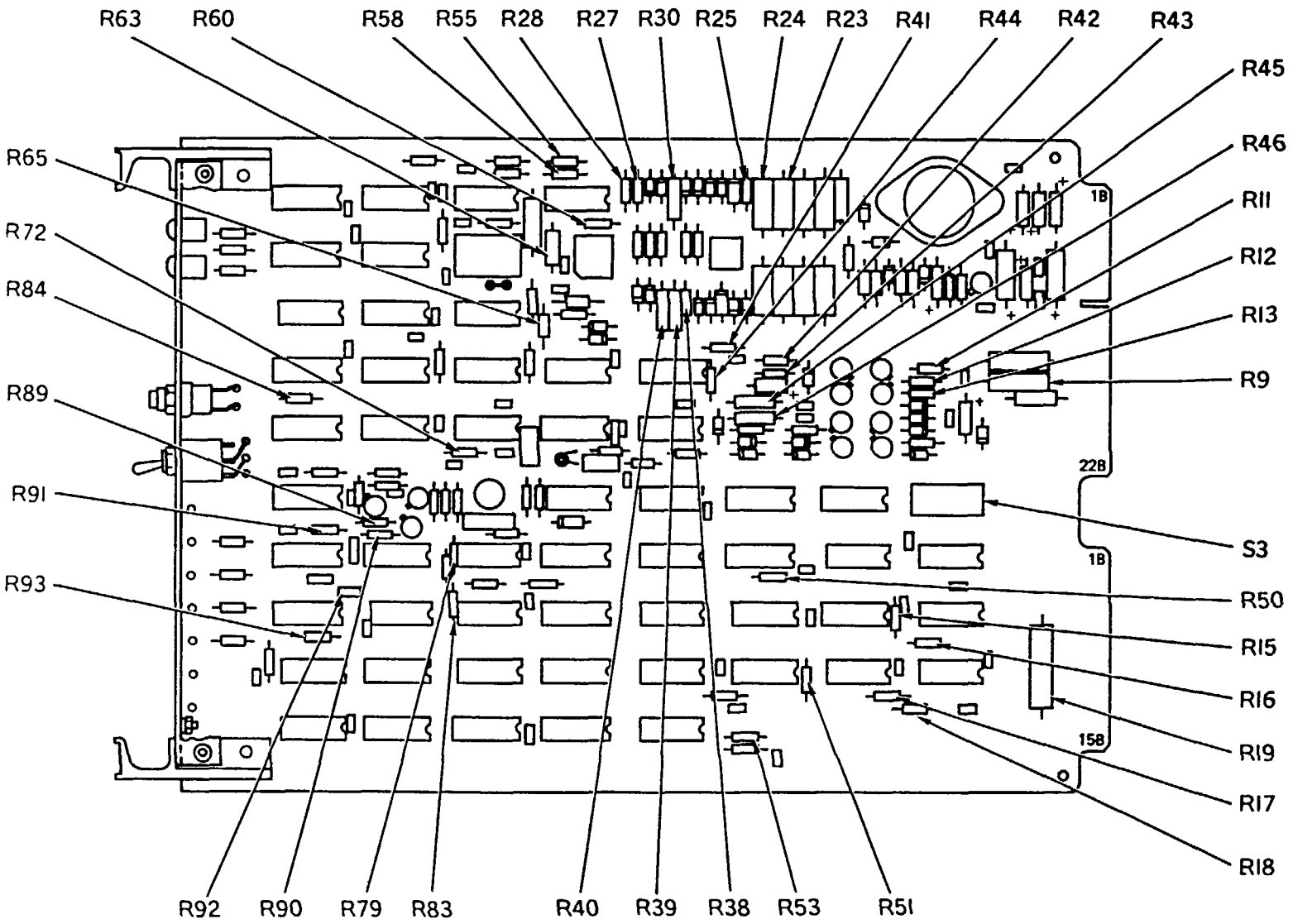
Figure 3-12. RCVR unit parts location diagram (sheet 7 of 10) RVR02 and RVR04.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB089

Figure 3-12. RCVR unit parts location diagram (sheet 8 of 10) RVR02 and RVR04.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2X8090

Figure 3-12. RCVR unit parts location diagram (sheet 9 of 10) RVR02 and RVR04.

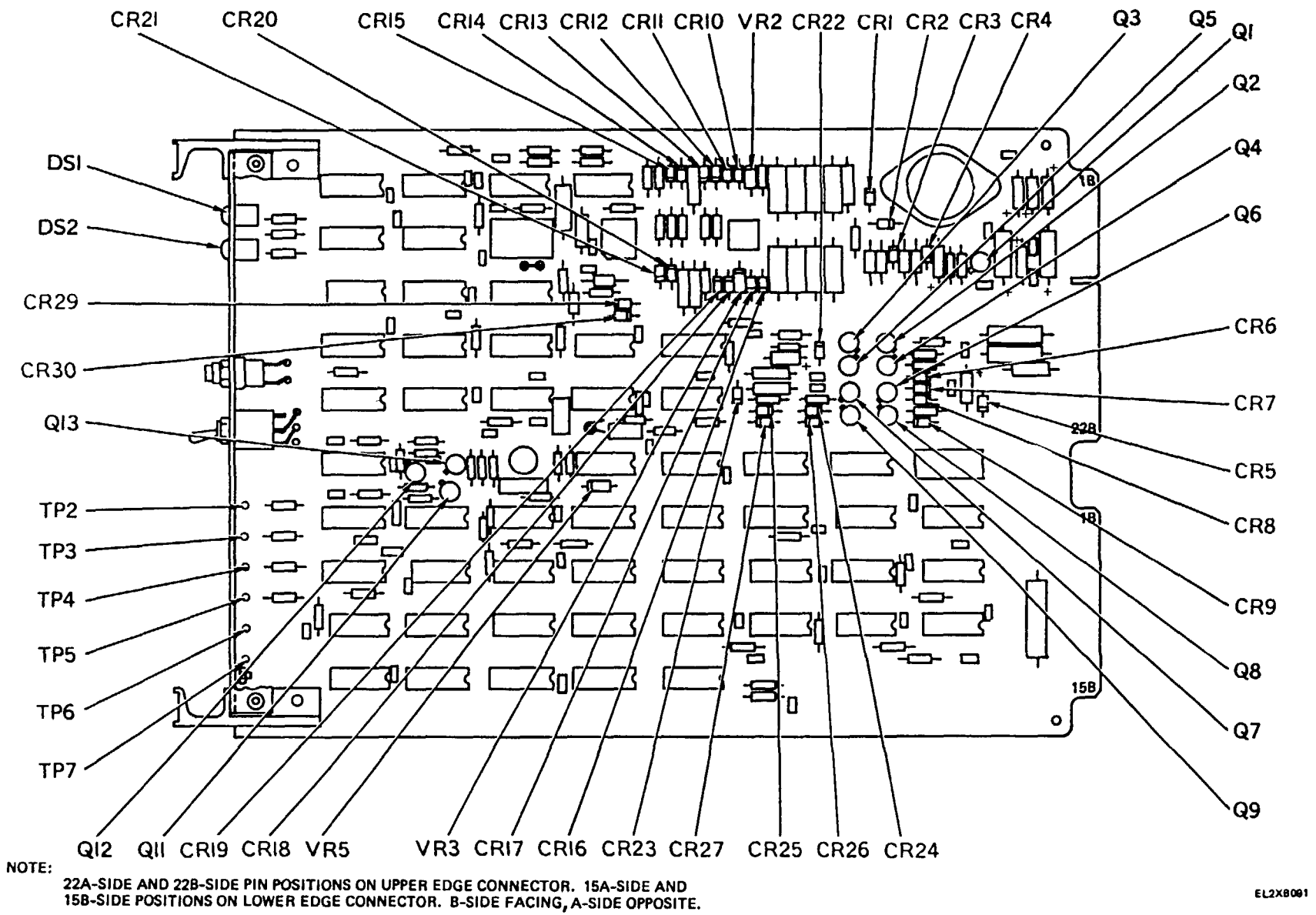


Figure 3-12. RCVR unit parts location diagram (sheet 10 of 10) RVR02 and RVR04.

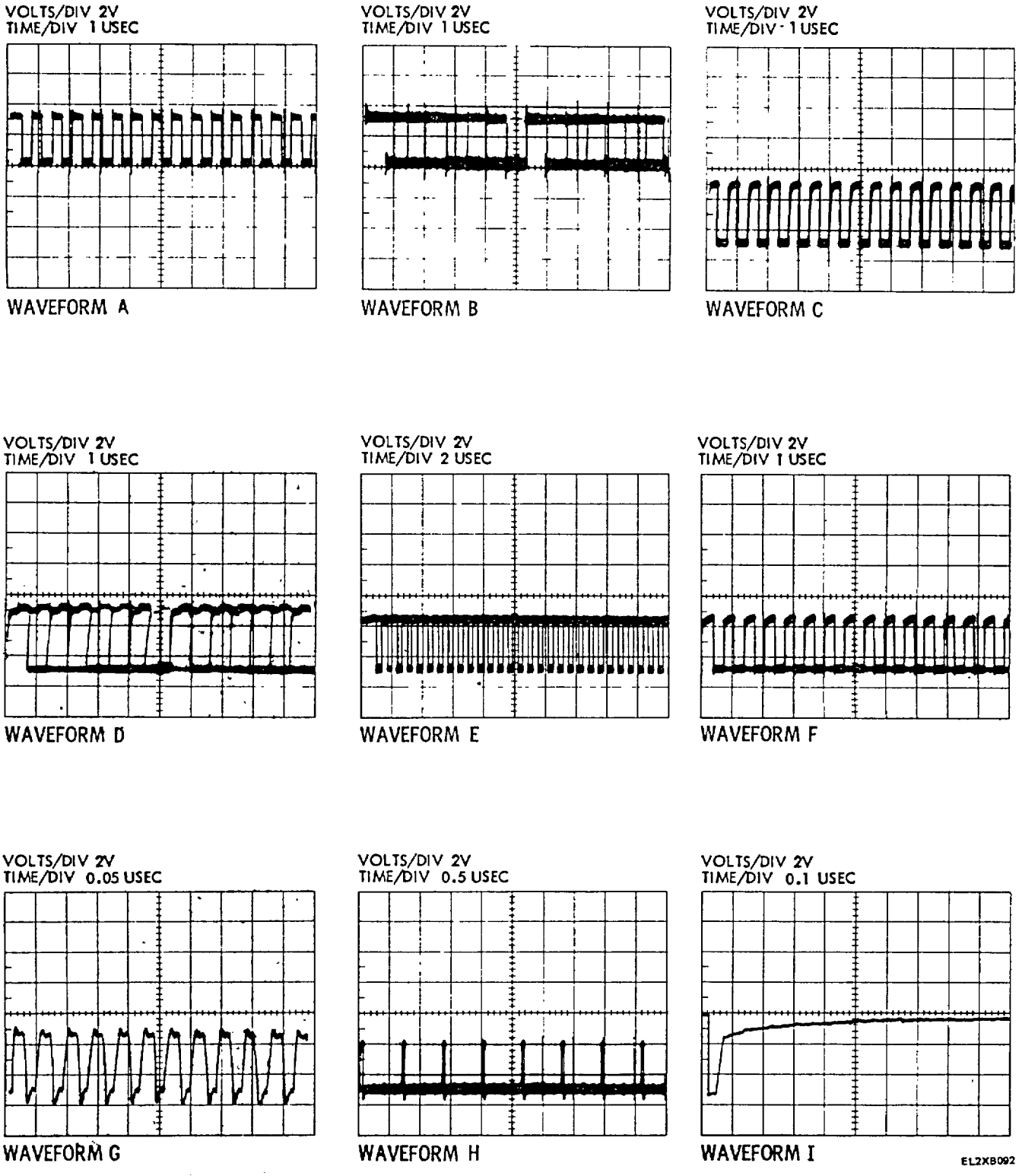


Figure 3-13. RCVR unit troubleshooting waveforms (sheet 1 of 6).

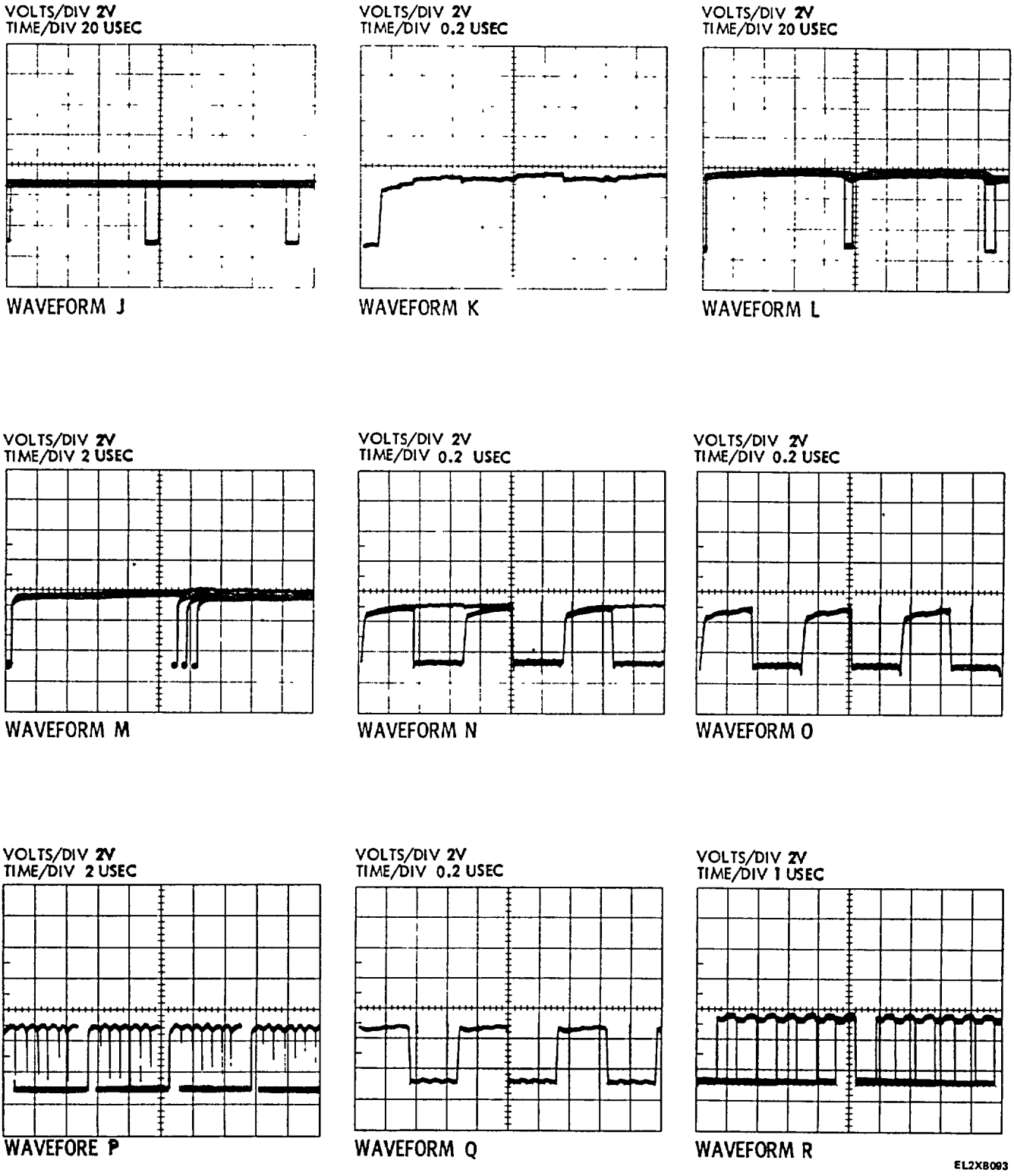


Figure 3-13. RCVR unit troubleshooting waveforms (sheet 2 of 6).

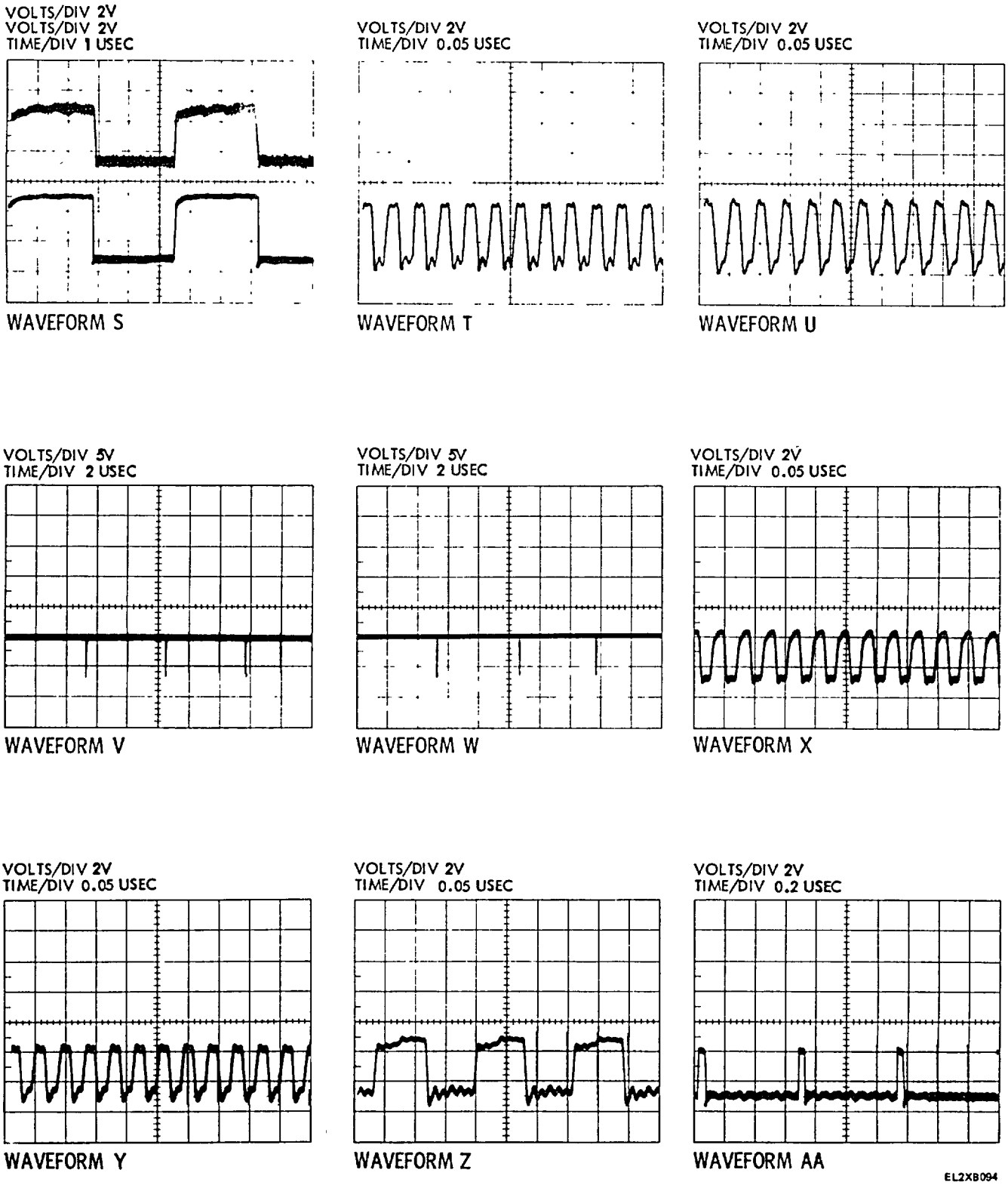


Figure 3-13. RCVR unit troubleshooting waveforms (sheet 3 of 6).

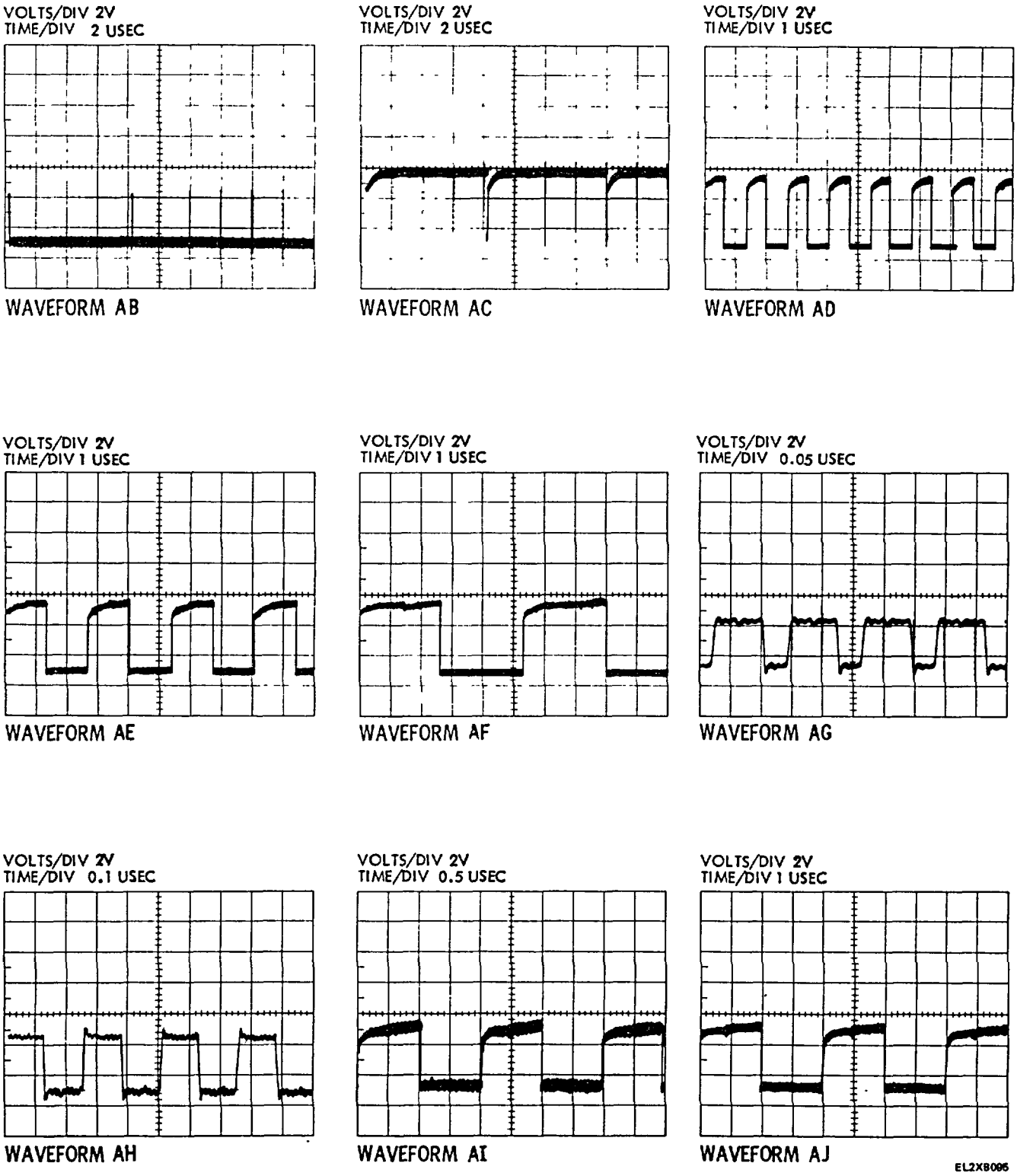


Figure 3-13. RCVR unit troubleshooting waveforms (sheet 4 of 6).

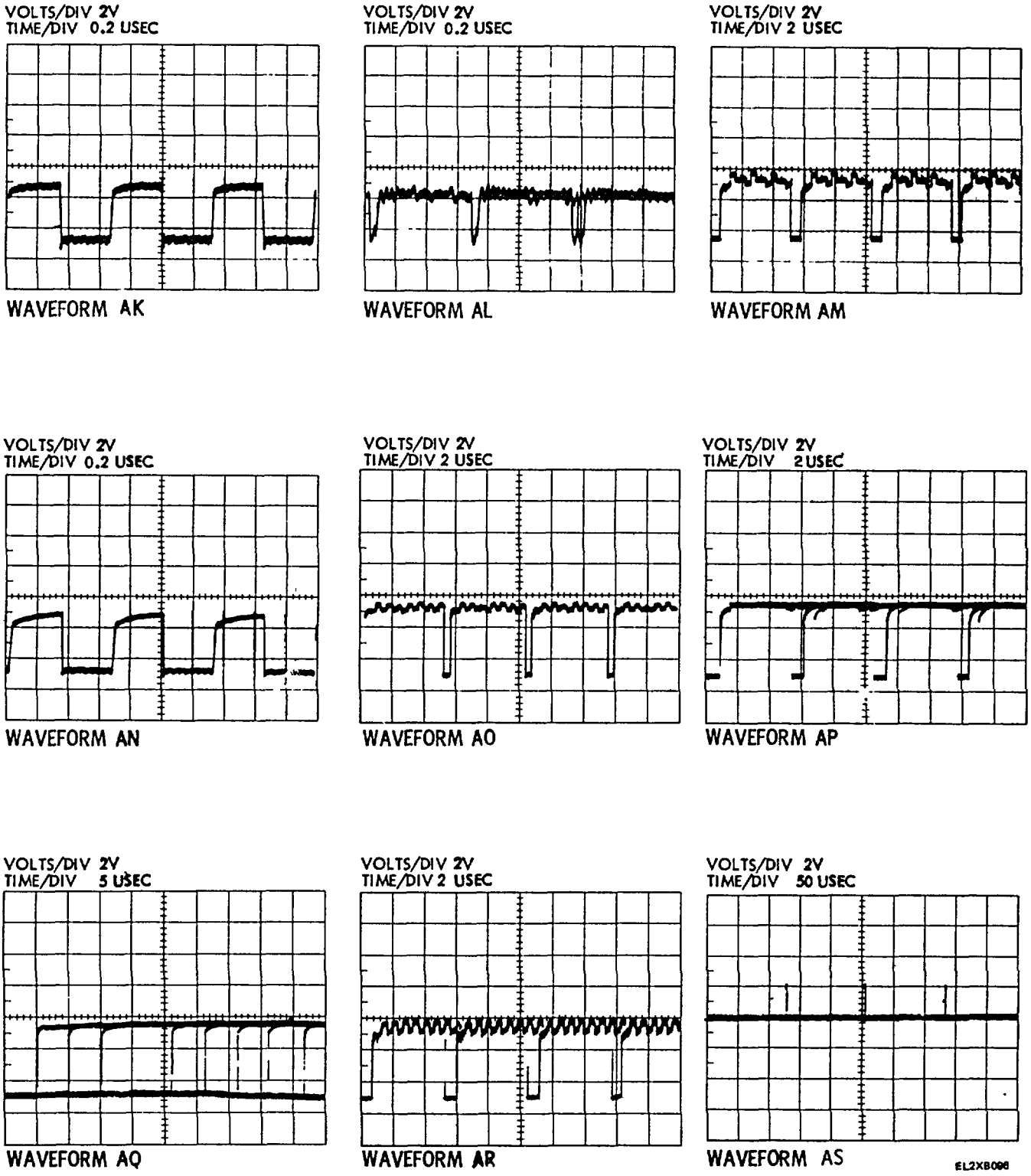


Figure 3-13. RCVR unit troubleshooting waveforms (sheet 5 of 6).

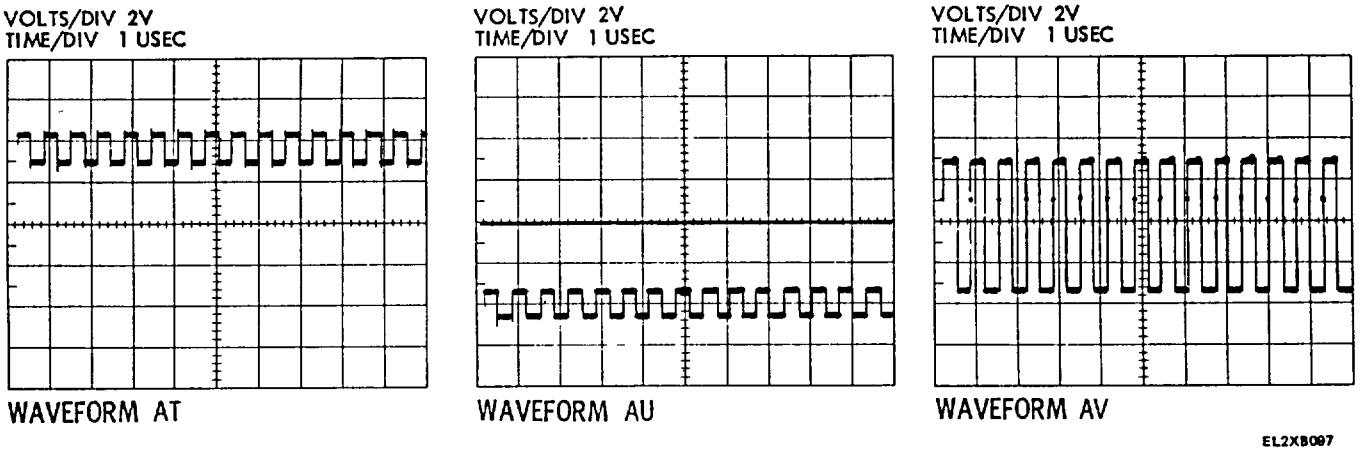


Figure 3-13. RCVR unit troubleshooting waveforms (sheet 6 of 6).

3-12. Troubleshooting the DEMUX Unit

The following procedures and data are to be used for troubleshooting the DEMUX unit. Refer to figure FO-6 and figure 3-15 for parts location.

a. Tools and Test Equipment

(1) K-100/G.
(2) N/USM-281C.
(3) MM.
(4) MXTF with the following accessories:
Extender board TRW 17332-010.
Type A test cable.
Type B test cable.
Type C test cables (2).
Spare 0-20 kb/s data module.

b. Initial Setup. Set up test equipment and faulty DEMUX unit for troubleshooting as follows:

(1) Set switch on MXTF PWR CONT unit to OFF.

(2) Install spare 0-20 kb/s data module in channel 1 location of MXTF.

(3) Remove MXTF DEMUX unit and, using extender board, install UUR in MXTF.

(4) Connect test equipment as shown in figure 3-14.

(5) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
AN/USM-281C	VOLTS/DIV (left and right)	2 V
	TIME/DIV	5 μs
	AC/GND/DC	DC
	TRIG SOURCE	LEFT
	POWER	Pull
MXTF (BITE)	DIGITAL FUNCTION	20 Kb/S
(PWR CONT)	Power	ON

NOTE

Allow equipment to warm up for five minutes before proceeding.

c. Fault Location. Troubleshoot in accordance with the following procedure to locate malfunctioning areas of the DEMUX unit.

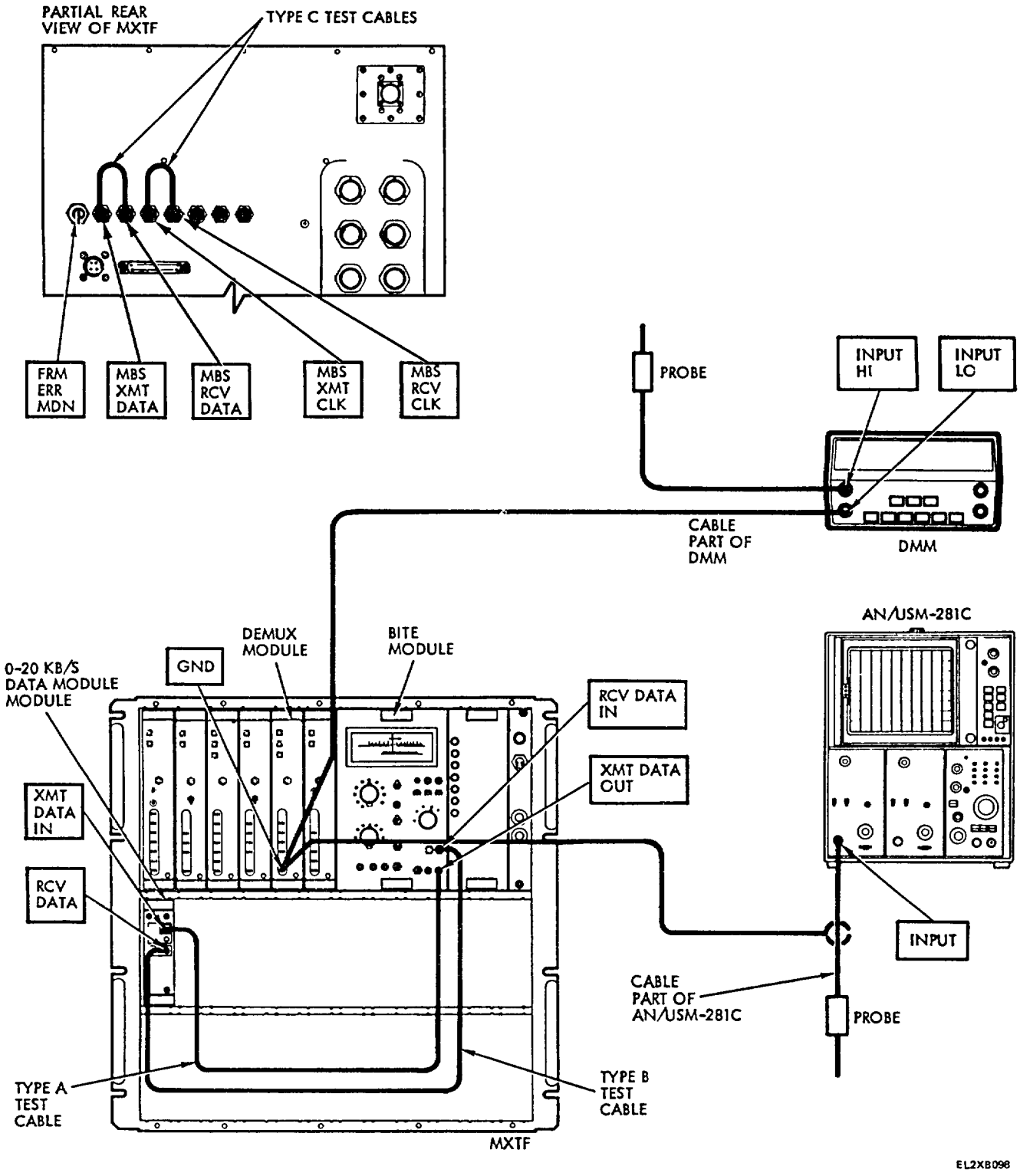


Figure 3-14. DEMUX unit troubleshooting setup diagram.

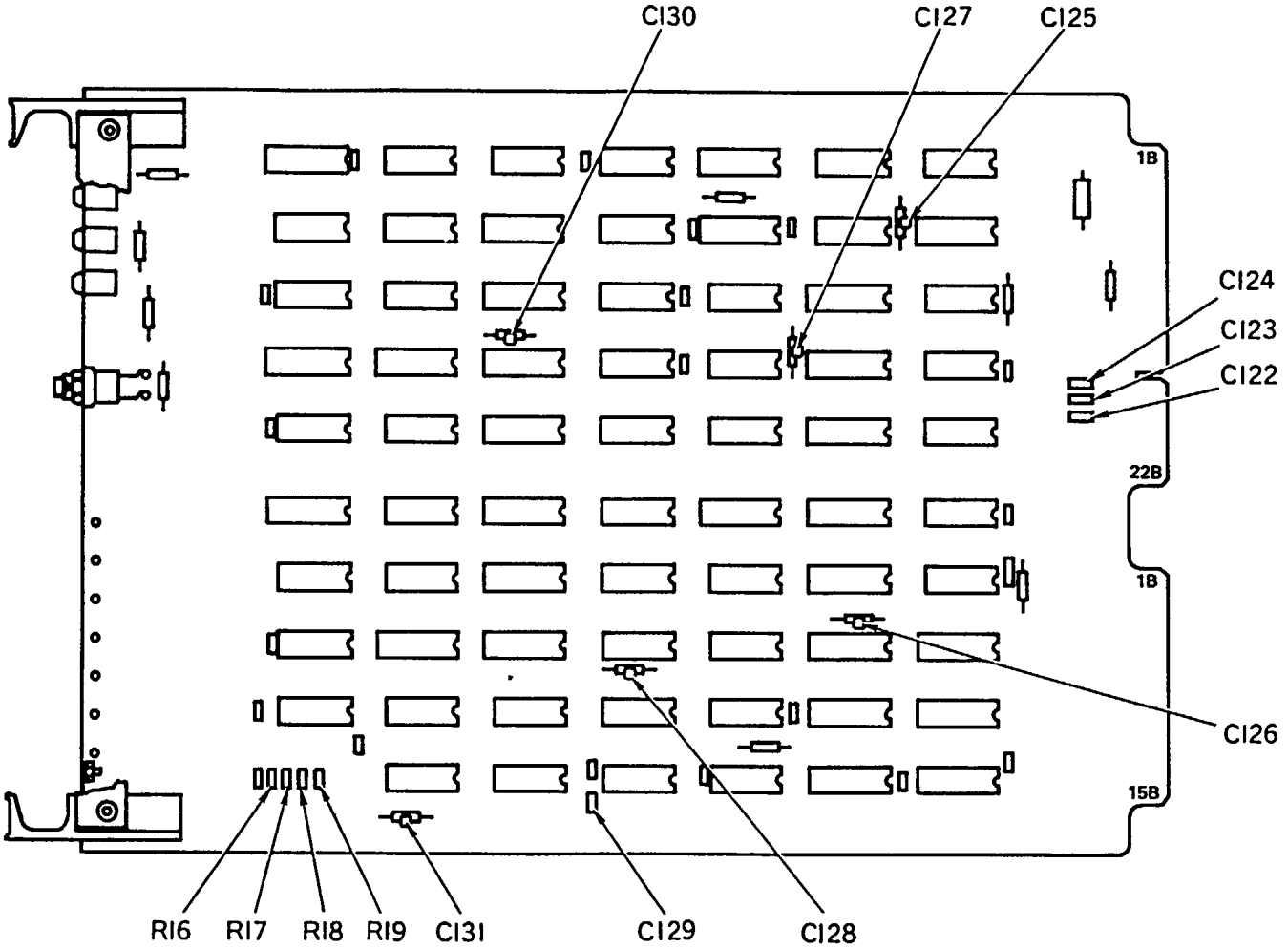
Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
1			Check DATA INPUT SHIFT REGISTER circuit (IC37, IC38, IC39 and IC40). If result of any check is incorrect, isolate and replace faulty component.	
			a. Verify that DRIVER and RCVR units are strapped for 24-channel operation (table 3-4).	*a*. None.
	AN/USM-281C			
	TIME/DIV:	.5 µs	*b*. Check clock signal at IC40-8.	*b*. Waveform A.
	TIME/DIV:	2 µs	*c.* Check data signal at IC39-3.	*c*. Waveform B.
			d. Check data signal at IC38-3.	*d*. Waveform B.
			e. Check data signal at IC37-3.	*e*. Waveform B.
2	*DMM*	10 VDC Scale	Check MODE SELECT LOGIC circuit (IC1, IC2, IC3 and IC11) using DMM. If result of any check is incorrect, isolate and replace faulty component.	
			a. Check signal level at IC2-11.	*a*. -4 to -5 VDC.
			b. Check signal level at IC11-4.	*b*. -4 to -5 VDC.
			c. Check signal level at IC11-6.	*c*. 0 to -1 VDC.
			d. Check signal level at IC1-6.	*d*. 0 to -1 VDC.
			e. Check signal level at IC1-8.	*e*. -4 to -5 VDC.
			f. Check signal level at IC11-10.	*f.* 0 to -1 VDC.
			g. Check signal level at IC2-7.	*g*. -4 to -5 VDC.
			h. Strap DRIVER and RCVR units for 3-channel operation (table 3-4).	*h*. None.
			i. Check signal level at IC11-4.	*i.* 0 to -1 VDC.
			j. Check signal level at IC11-6.	*j.* -4 to -5 VDC.
			k. Check signal level at IC1-6.	*k.* 0 to -1 VDC.
			l. Check signal level at IC1-8.	*l.* 0 to -1 VDC.
			m. Check signal level at IC11-10.	*m*. -4 to -5 VDC.
			n. Strap DRIVER and RCVR units for 6-channel operation (table 3-4).	*n*. None.
			o. Check signal level at IC2-12.	*o*. -4 to -5 VDC.
			p. Check signal level at IC11-4.	*p*. 0 to -1 VDC.
			q. Check signal level at IC11-6.	*q*. -4 to -5 VDC.
			r. Check signal level at IC1-6.	*r.* -4 to -5 VDC.
			s. Check signal level at IC1-8.	*s*. 0 to -1 VDC.
			t. Check signal level at IC11-10.	*t.* 0 to -1 VDC.
			u. Strap DRIVER and RCVR units for 12-channel operation (table 3-4).	*u*. None.
			v. Check signal level at IC2-10.	*v*. 0 to -1 VDC.
			w. Check signal level at IC11-4.	*w.* 0 to -1 VDC.
			x. Check signal level at IC11-6.	*x*. -4 to -5 VDC.
			y. Check signal level at IC1-6.	*y*. -4 to -5 VDC.
			z. Check signal level at IC1-8.	*z*. -4 to -5 VDC.
			aa. Check signal level at IC11-10.	*aa*. 0 to -1 VDC.
3			Check ACQUISITION COUNTER circuit (IC21, IC31, IC41, IC42 and IC51). If result of check is incorrect, isolate and replace faulty component.	
			a. Strap DRIVER and RCVR units for 3-channel operation (table 3-4).	*a*. None.
	AN/USM-281C			
	TIME/DIV:	20 µs	*b*. Check signal at IC21-15.	*b*. Waveform C.
	TIME/DIV:	.5 ms	*c*. Check signal at IC31-15.	*c*. Waveform D.
			d. Check signal at IC41-8.	*d*. Waveform E.
			e. Check signal at IC41-10.	*e*. Waveform F.
	TIME/DIV:	5 µs	*f.* Check signal at IC21-14.	*f.* Waveform G.
	TIME/DIV:	10 µs	*g*. Check signal at IC21-13.	*g*. Waveform H.
			h. Check signal at IC21-12.	*h*. Waveform I.
			i. Check signal at IC21-11.	*i.* Waveform J.
	TIME/DIV:	.5 ms	*j.* Check signal at IC31-14.	*j.* Waveform K.
			k. Check signal at IC31-13.	*k.* Waveform L.
			l. Check signal at IC31-12.	*l.* Waveform M.
			m. Check signal at IC31-11.	*m*. Waveform N.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
			n. Remove type C cable from MBS DATA connector on rear of MXTF. Observe condition of FRAME LOSS lamp on UUR	*n*. Lamp illuminates.
			NOTE **Ignore lamps which light during remainder of step.**	
	TIME/DIV:	2 ms	*o.* Check signal at IC42-11.	*o.* Waveform O.
			p. Reconnect type C cable to MBS RCV DATA connector.	*p.* None.
4			Check ACQUISITION COUNTER LOAD LOGIC circuit (IC51, IC52 and IC63). If result of check is incorrect, isolate and replace faulty component.	
	AN/USM-281C		*a.* Strap DRIVER and RCVR units for 24-channel operation (table 3-4.	*a.* None.
	TIME/DIV:	50 µs	*b*. Check signal at IC63-1.	*b*. Waveform P.
5			Check CYCLE COUNTER circuit (IC3, IC11, IC41, IC43, IC44, IC52 and IC53). If result of any check is incorrect, isolate and replace faulty component.	
			a. Remove type C cable from MBS RCV DATA connector on rear of MXTF. Observe condition of FRAME LOSS lamp on UUR.	*a.* Lamp illuminates.
			NOTE **Ignore lamps which light during remainder of step.**	*AN/USM-281C*
	TIME/DIV:	.2 µa	*b*. Check signal at IC43-9.	*b*. Waveform Q.
	TIME/DIV:	.2 ms	*c.* Check signal at IC43-14.	*c.* Waveform R.
			d. Check signal at IC43-13.	*d.* Waveform S.
	TIME/DIV:	.1 ms	*e*. Check signal at IC52-4.	*e*. Waveform T.
			f. Check signal at IC41-12.	*f.* Waveform U.
	MXTF (RCVR) LOOP-NORMAL:	LOOP	*g.* Using DMM, check signal level at IC43-14.	*g.* 0 to -1.5 VDC.
			h. Using DMM, check signal at IC43-13.	*h.* 0 to -1.5 VDC.
			i. Using DMM, check signal level at IC43-12.	*i.* -4 to -5 VDC.
			j. Check signal at IC44-7.	*j.* Waveform V.
			k. Using DMM, check signal level at IC44-12.	*k*. -4 to -5 VDC.
			l. Using DMM, check signal level at IC44-9.	*l.* -4 to-5 VDC.
	MXTF (RCVR) LOOP-NORMAL: NORMAL		*m*. Check signal at IC43-9.	*in*. Waveform W.
	AN/USM-281C TIME/DIV:	2 µs		
			n. Strap DRIVER and RCVR units for 12-channel operation (table 3-4).	*n.* None.
	TIME/DIV:	1 ms	*o*. Check signal at IC43-14.	*o.* Waveform X.
	TIME/DIV:	1 ms	*p*. Check signal at IC43-13.	*p.* Waveform Y.
			q. Check signal at IC52-4.	*q.* Waveform X.
			r. Check signal at IC41-12.	*r.* Waveform X.
			s. Check signal at IC44-12.	*8.* Waveform X.
			t. Check signal at IC44-7.	*t.* Waveform Z.
			u. Reconnect type C cable to MBS RCV DATA connector on rear of MXTF.	*u.* None.
6			Check 24 CHANNEL PATTERN STORAGE circuit (IC45, IC46, IC49, IC57,	

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
			IC65 and IC68). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C		a. Strap DRIVER and RCVR units for 24-channel operation (table 3-4).	a. None.
	TIME/DIV:	2 µs	b. Check signal at IC68-3.	b. Waveform AA.
			c. Check signal at test point E3.	c. Waveform AB.
			d. Check signal at IC45-2.	d. Waveform AB.
			e. Check signal at IC45-6.	e. Waveform AB.
			f. Check signal at IC45-11.	f. Waveform AB.
			g. Check signal at IC45-14.	g. Similar to waveform B.
			h. Check signal at IC57-4.	h. Waveform AC.
7			Check DATA PROMOTION AND CHECK LOGIC circuit (IC45, IC47, IC48, IC49, IC55 and IC58). If result of any check is incorrect, isolate and replace faulty component.	
			a. Check signal at IC47-5.	a. Waveform AB.
			b. Check signal at IC48-5.	b. Waveform AD.
			c. Check signal at IC57-1.	c. Waveform AB.
			d. Check signal at IC58-4.	d. Waveform AE.
			e. Check signal at IC35-3.	e. Waveform AB.
			f. Check signal at IC55-10.	f. Waveform AD.
	TIME/DIV:	5 µs	g. Check signal at IC58-4.	g. Waveform AF.
			h. Strap DRIVER and RCVR units for 3-channel NRZ operation (table 3-4).	h. None.
			i. Check signal at IC55-10.	i. Waveform AG.
8			Check SIEVE MEMORY circuit (IC55, IC64, IC65 and IC68). If result of any check is incorrect, isolate and replace faulty component.	
			a. Remove jumper between F4 and E5. Check condition of A TILT lamps on UUR and PWR SPLY unit.	a. Lamps illuminate.
			b. Connect jumper between P9-3B and E4. Check signal at IC66-6. Check condition of C.G.A. lamp on PWR SPLY unit and FRAME LOSS on UUR.	b. Waveform logic level high (straight line). Lamps illuminate.
	AN/USM-281C			
	TIME/DIV:	2 µs	c. Remove jumper from P9-3B and connect to IC64-1.	c. Waveform AH.
			d. Remove jumper between E4 and IC64-1. Replace jumper between E4 and E5.	d. None.
	AN/USM-281C		e. Connect right probe to IC44-7 and left probe to IC64-11.	e. Waveform similar to Al (bottom trace may have 1 or 2 pulses).
	TRIG SOURCE:	RIGHT		
	VERT MODE:	CHOP		
	TIME/DIV:	.5 ms		
	AN/USM-281C			
	TIME/DIV:	1 ms	f. Remove type C cable from MBS RCV DATA connector. Check signal at IC64-7.	f. Similar to waveform AJ.
	MXTF (RCVR)			
	LOOP-NORMAL:	LOOP		
	TIME/DIV:	5 ms	g. Check signal at IC64-7.	g. Similar to waveform AK.
9			Check CONTROL UNIT circuit (IC34, IC49, IC53, IC56, IC59, IC60, IC63, IC64, IC65, IC67, IC68 and IC69). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	VERT MODE:	LEFT		
	TRIG SOURCE:	LEFT		
			a. Check signal at IC67-1.	a. Logic level low.
			b. Check signal at IC63-9.	b. Logic level low.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
			c. Check signal at IC53-6.	*c*. Logic level high.
	MXTF (RCVR)		*d*. Check signal at FRAME BIT	*d*. Waveform BQ.
	LOOP-NORMAL:	NORMAL	ERROR test point on UUR.	
	AN/USM-281C			
	TIME/DIV:	1 ms		
			e. Check signal at IC53-11.	*e*. Any activity at this point
			indicates correct operation.	
			f. Check signal at IC56-13.	*f*. Logic level low.
			g. Check signal at IC67-6.	*g*. Logic level high.
			h. Check signal at IC67-8.	*h*. Logic level low.
			i. Check signal at IC54-11.	*i*. Logic level low.
10			Check LOW RATE PATTERN STORAGE circuit (IC61). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	VERT MODE:	CHOP	*a*. Remove jumper between E2 and E3.	*a*. Waveform AL.
	TRIG SOURCE:	RIGHT	Connect right probe to IC44-7. Check	(disregard relay chatter)
	MXTF (RCVR)		signal with left probe at IC61-6.	
	LOOP-NORMAL:	LOOP	(Disregard relay chatter.)	
			b. Connect jumper between P9-3B and	*b*. None.
			E2.	
			c. Check signal at IC61-6.	*c*. Logic level high.
			d. Install jumper between E2 and E3.	*d*. None.
11			Check PATTERN DETECTOR circuit (IC35, IC36, IC40 and IC56). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	5 µs	*a*. Check signal at IC36-6.	a. Waveform AM.
	TRIG SOURCE:	LEFT		
	VERT MODE:	LEFT		
			b. Check signal at IC56-4.	*b*. Waveform AN.
12			Check BIT/CHANNEL/FRAME COUNTER AND DECODER circuit (IC3, IC4, IC5, IC6, IC7, IC8, IC9, IC10, IC17, IC18, IC19, IC20, IC26, IC27, IC28, IC29 and IC50). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	20 µs	*a*. Check signal at IC30-13.	*a*. Waveform AO.
			b. Check signal at IC26-12.	*b*. Waveform AP.
			c. Check signal at IC30-1.	*c*. Waveform AQ.
			d. Check signal at IC20-14.	*d*. Waveform AR.
			e. Check signal at IC20-13.	*e*. Waveform AR.
			f. Check signal at IC20-12.	*f*. Logic level low.
			g. Check signal at IC20-11.	*g*. Logic level low.
	TIME/DIV:	50 µs	*h*. Check signal at IC10-15.	*h*. Similar to waveform AS.
			i. Check signal at IC10-14.	*i*. Waveform AS.
			j. Check signal at IC10-13.	*j*. Waveform AS.
			k. Check signal at IC4-3.	*k*. Waveform AT.
	TIME/DIV:	.2 ms	*l*. Check signal at IC12-4.	*l*. Waveform AU.
	TIME/DIV:	.5 ms	*m*. Check signal at 12 FRAME test point	*m*. Waveform AV.
			on front panel of UUR.	
	TIME/DIV:	20 µs	*n*. Check signal at IC30-13.	*n*. Waveform AW.
			o. Strap DRIVER and RCVR units for	*o*. None.
			6-channel operation (table 3-4).	
			p. Check signal at IC26-12.	*p*. Waveform AX.
			q. Check signal at IC30-1.	*q*. Waveform AY.
			r. Check signal at IC20-14.	*r*. Waveform AZ.
			s. Check signal at IC20-13.	*s*. Waveform BA.
			t. Check signal at IC20-12.	*t*. Similar to waveform BA.
			u. Check signal at IC20-11.	*u*. Logic level low.
			v. Check signal at IC10-15.	*v*. Waveform BB.

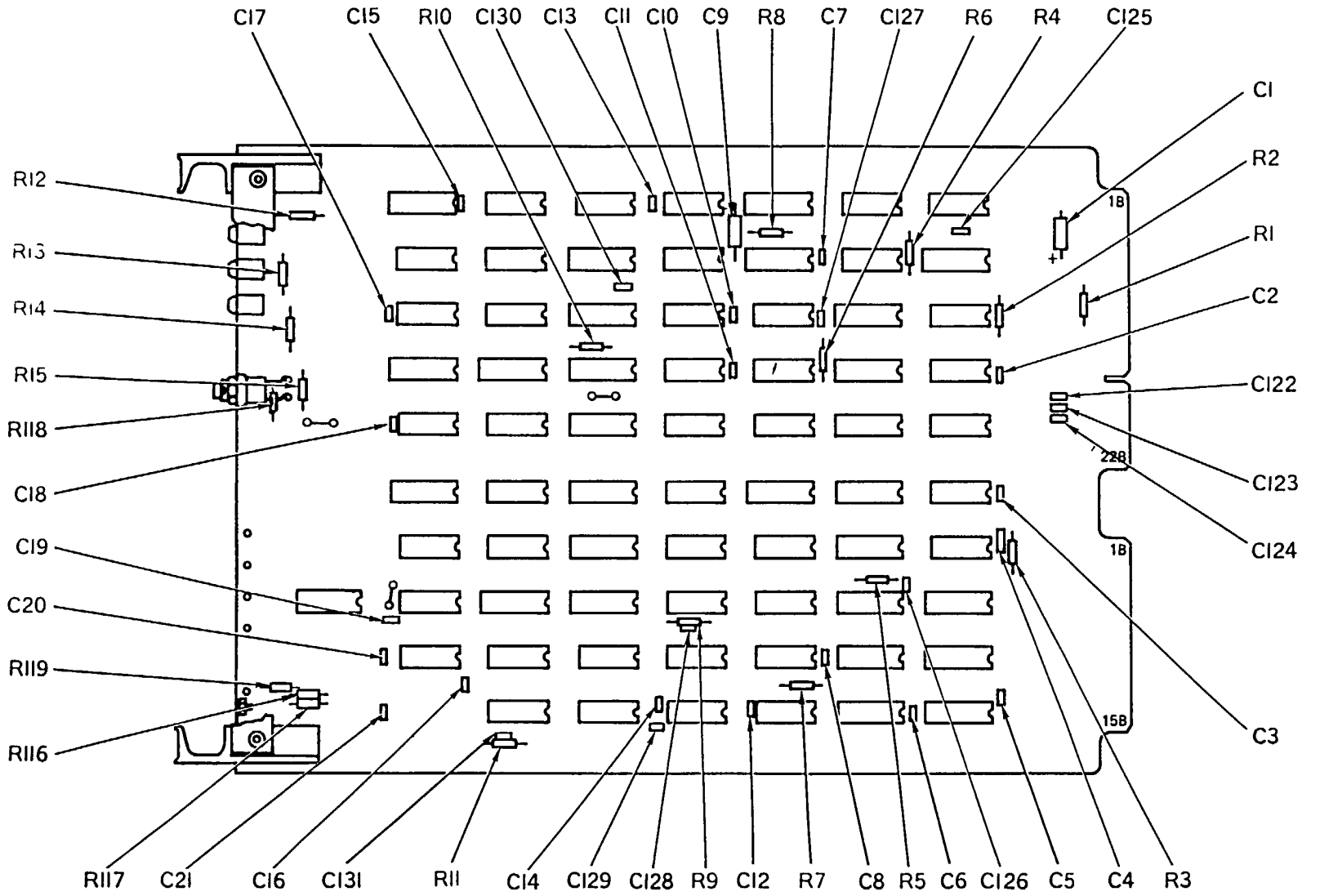
Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
			w. Check signal at IC10-14.	*w.* Waveform BB.
			x. Check signal at IC10-13.	*x.* Waveform BB.
			y. Check signal at IC10-12.	*y.* Waveform BB.
			z. Check signal at IC10-11.	*z.* Logic level high.
			aa. Check signal at IC10-10.	*aa*. Logic level high.
			ab. Check signal at IC10-9.	*ab*. Logic level high.
	TIME/DIV:	.2 ms	*ac.* Check signal at IC12-4.	*ac*. Waveform AU.
	TIME/DIV:	.5 ms	*ad.* Check signal at 12 FRAME test point on UUR.	*ad*. Waveform AV.
			ae. Strap DRIVER and RCVR for 12-channel operation.	*ae*. None.
	TIME/DIV:	20 µs	*af.* Check signal at IC30-13.	*af.* Waveform BC.
			ag. Check signal at IC26-12.	*ag*. Waveform BD.
			ah. Check signal at IC30-1.	*ah*. Waveform BE.
			ai. Check signal at IC20-14.	*ai.* Waveform BF.
			aj. Check signal at IC20-13.	*aj.* Waveform BG.
			ak. Check signal at IC20-12.	*ak.* Waveform BH.
			al. Check signal at IC20-11.	*al.* Waveform BH.
			am. Check signal at IC10-15.	*am*. Waveform BI.
			an. Check signal at IC10-14.	*an*. Waveform BI.
			ao. Check signal at IC10-13.	*ao*. Waveform BI.
			ap. Check signal at IC10-12.	*ap*. Waveform BI.
			aq. Check signal at IC9-15.	*aq*. Waveform BI.
			ar. Check signal at IC9-14.	*ar.* Waveform BI.
			as. Check signal at IC9-13.	*as*. Waveform BI.
			at. Check signal at IC9-12.	*at.* Waveform BI.
			au. Check signal at IC8-15.	*au*. Waveform BI.
			av. Check signal at IC8-14.	*av*. Waveform BI.
			aw. Check signal at IC8-13.	*aw.* Waveform BI.
			ax. Check signal at IC8-12.	*ax*. Waveform BI.
	TIME/DIV:	.2 ms	*ay.* Check signal at IC12-4.	*ay*. Waveform AU.
	TIME/DIV:	.5 ms	*az*. Check signal at 12 FRAME test point on UUR.	*az*. Waveform AV.
			ba. Strap DRIVER and RCVR units for 24-channel operation (table 3-4).	*ba*. None.
	TIME/DIV:	20 µs	*bb*. Check signal at IC30-13.	*bb*. Waveform BJ.
			be. Check signal at IC26-12.	*be*. Waveform BK.
			bd. Check signal at IC30-1.	*bd*. Waveform BL.
			be. Check signal at IC20-14.	*be*. Waveform BM.
			bf. Check signal at IC20-13.	*bf.* Waveform BN.
			bg. Check signal at IC20-12.	*bg*. Waveform BO.
			bh. Check signal at IC20-11.	*bh*. Waveform BO.
			bi. Check signal at IC10-9.	*bi.* Waveform BP.
			bj. Check signal at IC10-7.	*bi.* Waveform BP.
			bk. Check signal at IC9-11.	*bk.* Waveform BP.
			bl. Check signal at IC9-10.	*bl.* Waveform BP.
			bm. Check signal at IC9-9.	*bm*. Waveform BP.
			bn. Check signal at IC9-7.	*bn*. Waveform BP.
			bo. Check signal at IC8-11.	*bo*. Waveform BP.
			bp. Check signal at ICS-10.	*bp*. Waveform BP.
			bq. Check signal at IC8-9.	*bq*. Waveform BP.
			br. Check signal at IC8-7.	*br.* Waveform BP.
	TIME/DIV:	.5 ms	*bs.* Check signal at 12 FRAME test point on UUR.	*bs*. Waveform AV.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2X8099

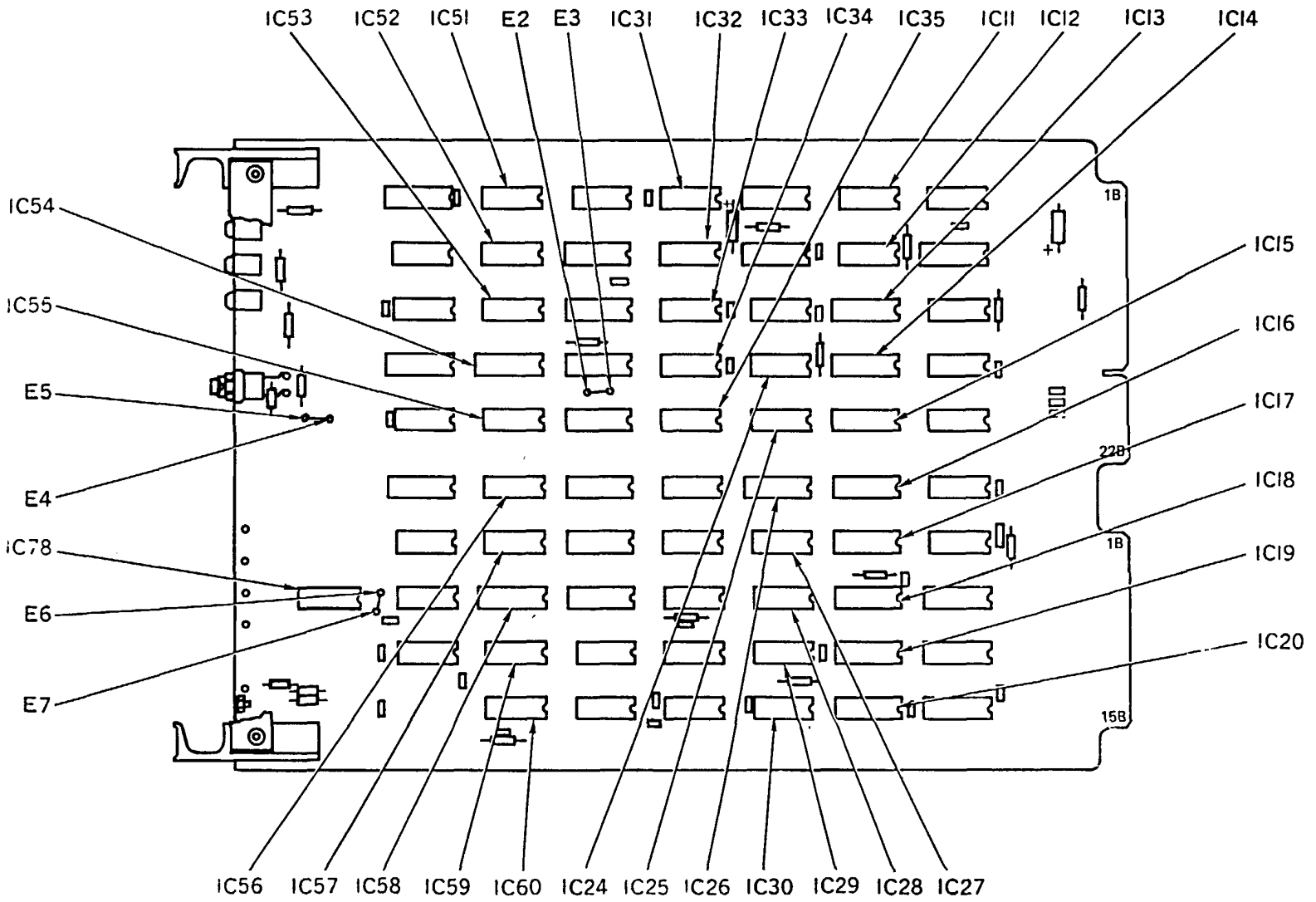
Figure 3-15. DEMUX unit parts location diagram (sheet 1 of 4) DMX02.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2X8100

Figure 3-15. DEMUX unit parts location diagram (sheet 2 of 4) DMX02, DMX04, and DMX06.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB101

Figure 3-15. DEMUX unit parts location diagram (sheet 3 of 4) DMX_{02}, DMX_{04}, and DMX_{06}.

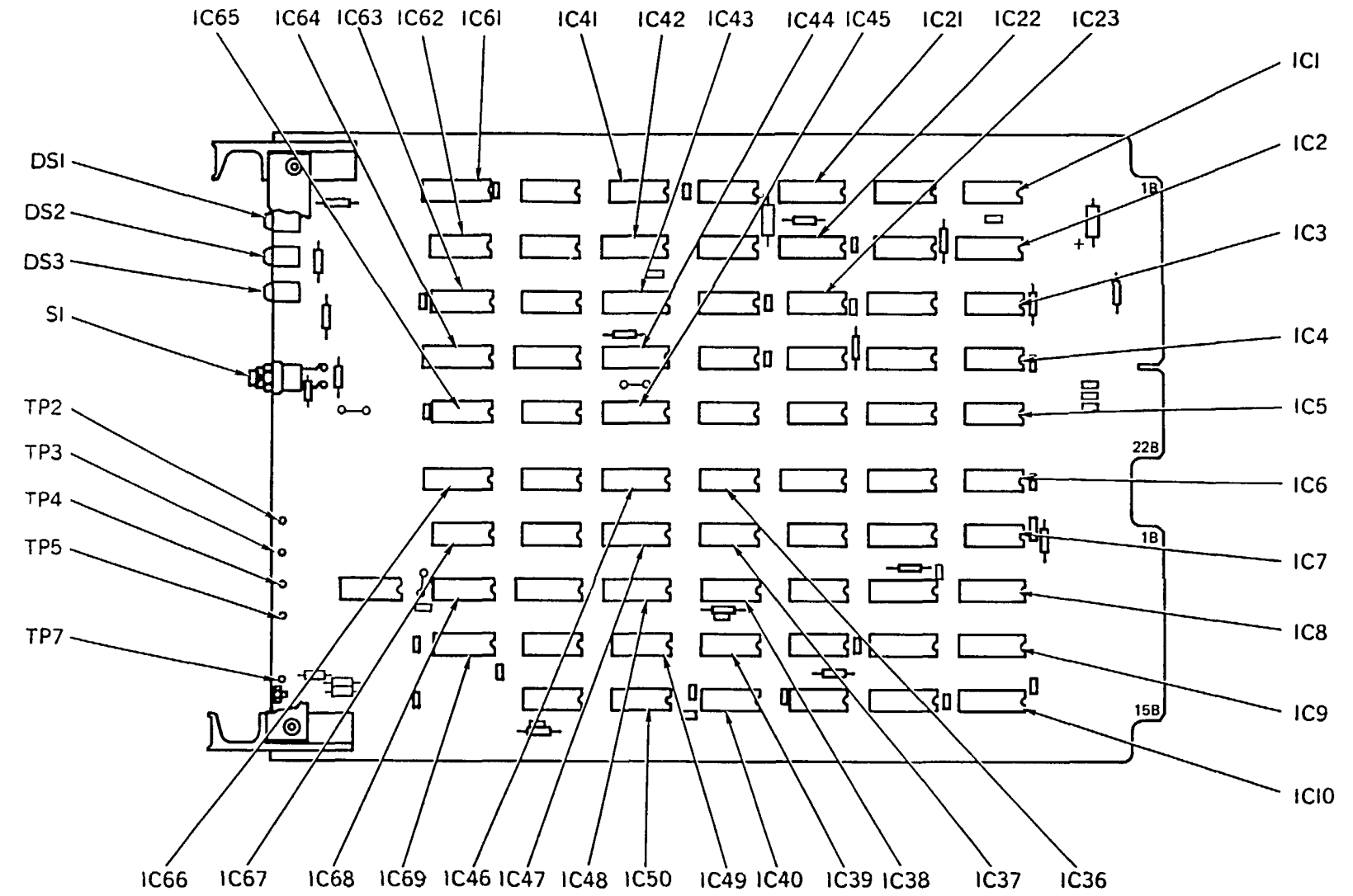


Figure 3-15. DEMUX unit parts location diagram (sheet 4 of 4) DMX_{02}, DMX_{04}, DMX_{06}.

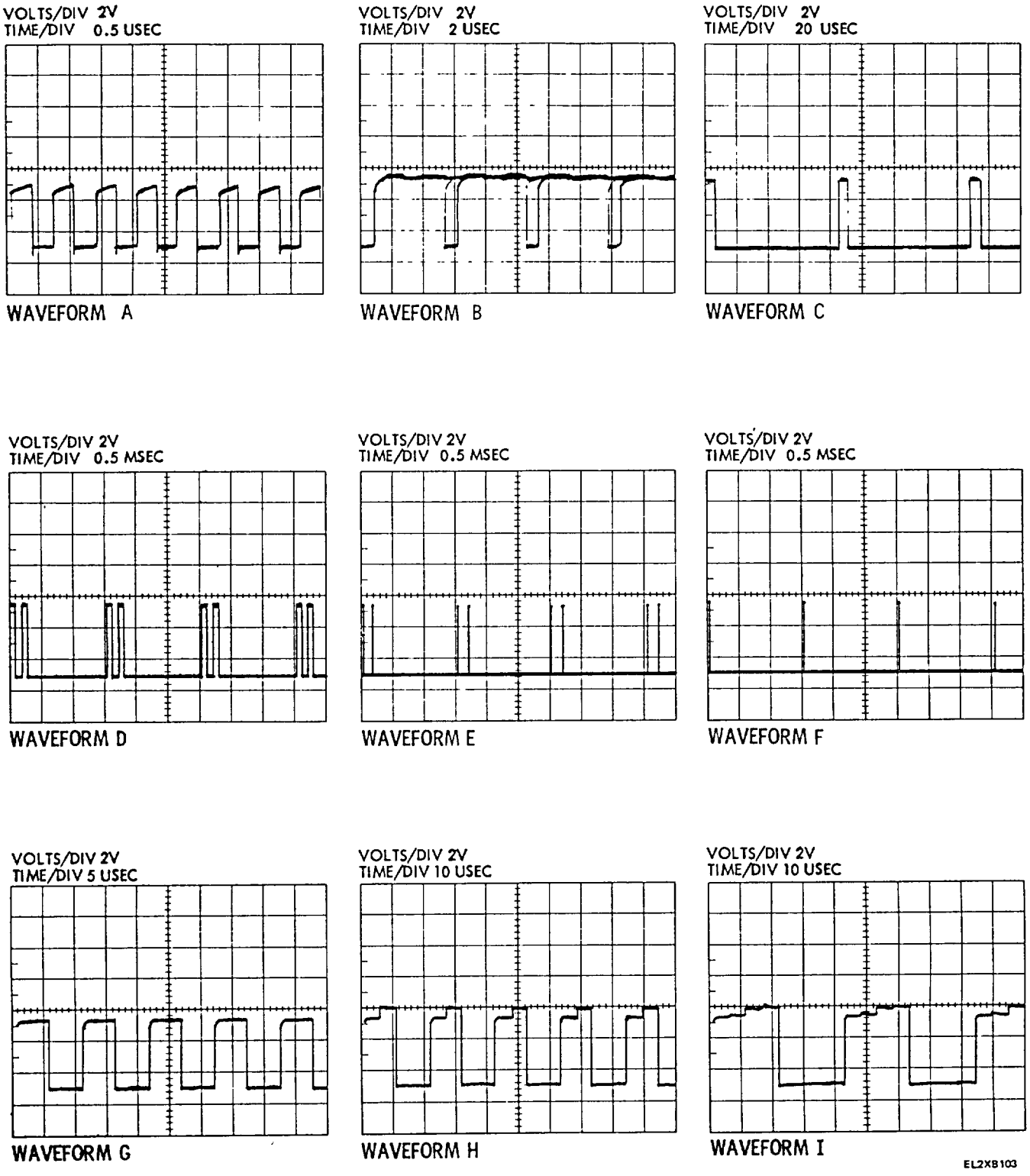


Figure 3-16. DEMUX unit troubleshooting waveforms (sheet 1 of 8).

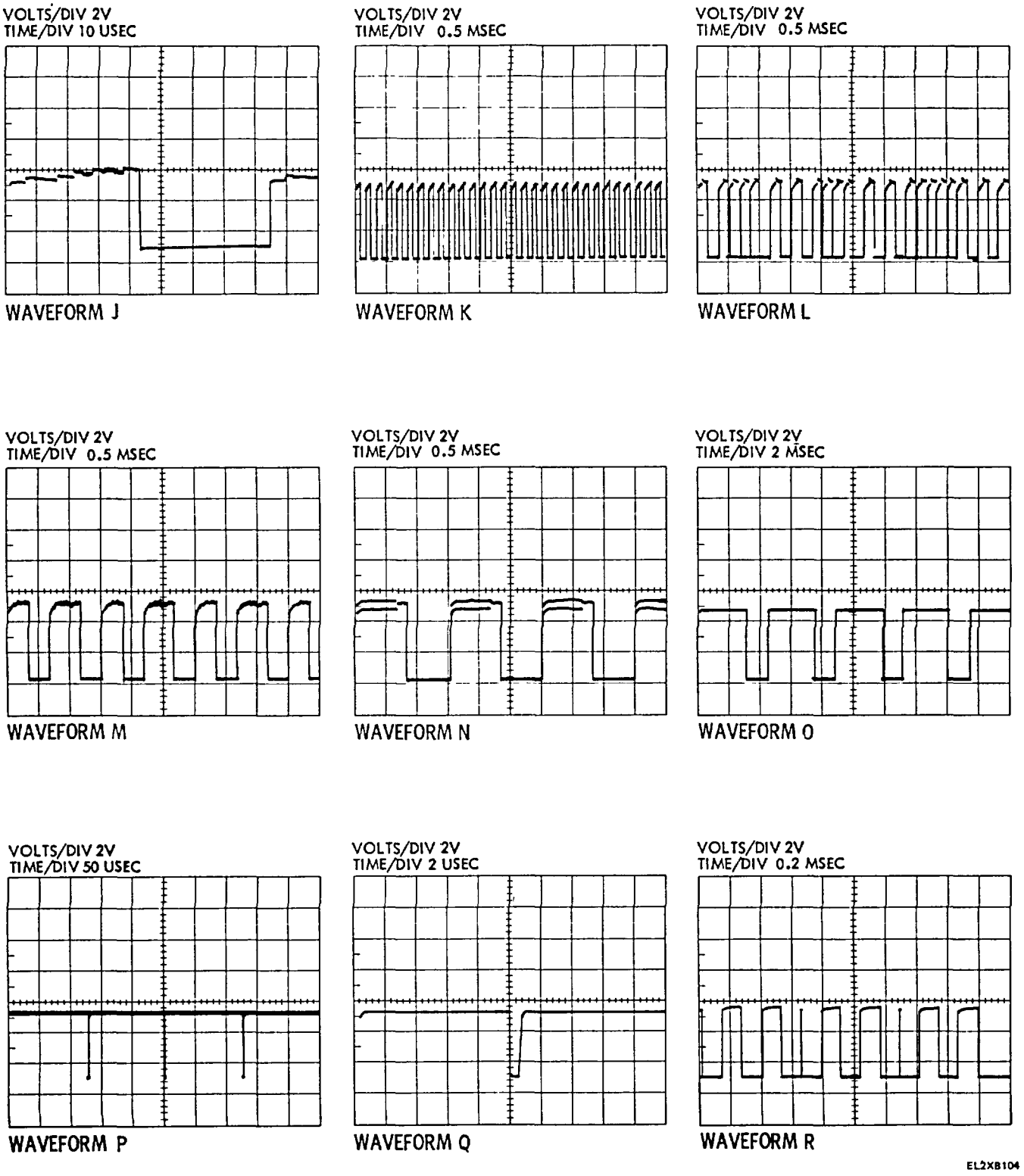


Figure 3-16. DEMUX unit troubleshooting waveforms (sheet 2 of 8).

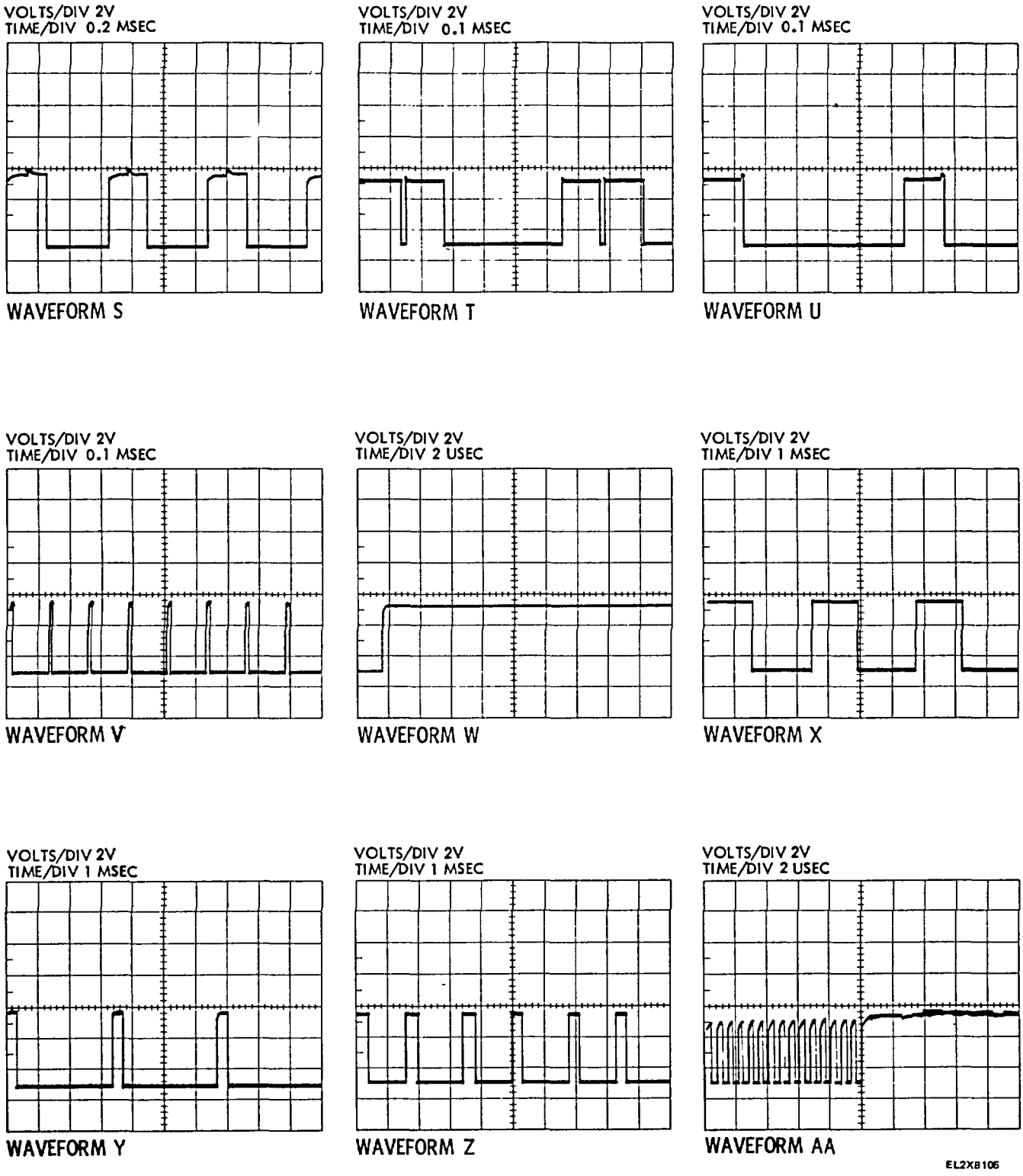


Figure 3-16. DEMUX unit troubleshooting waveforms (sheet 3 of 8).

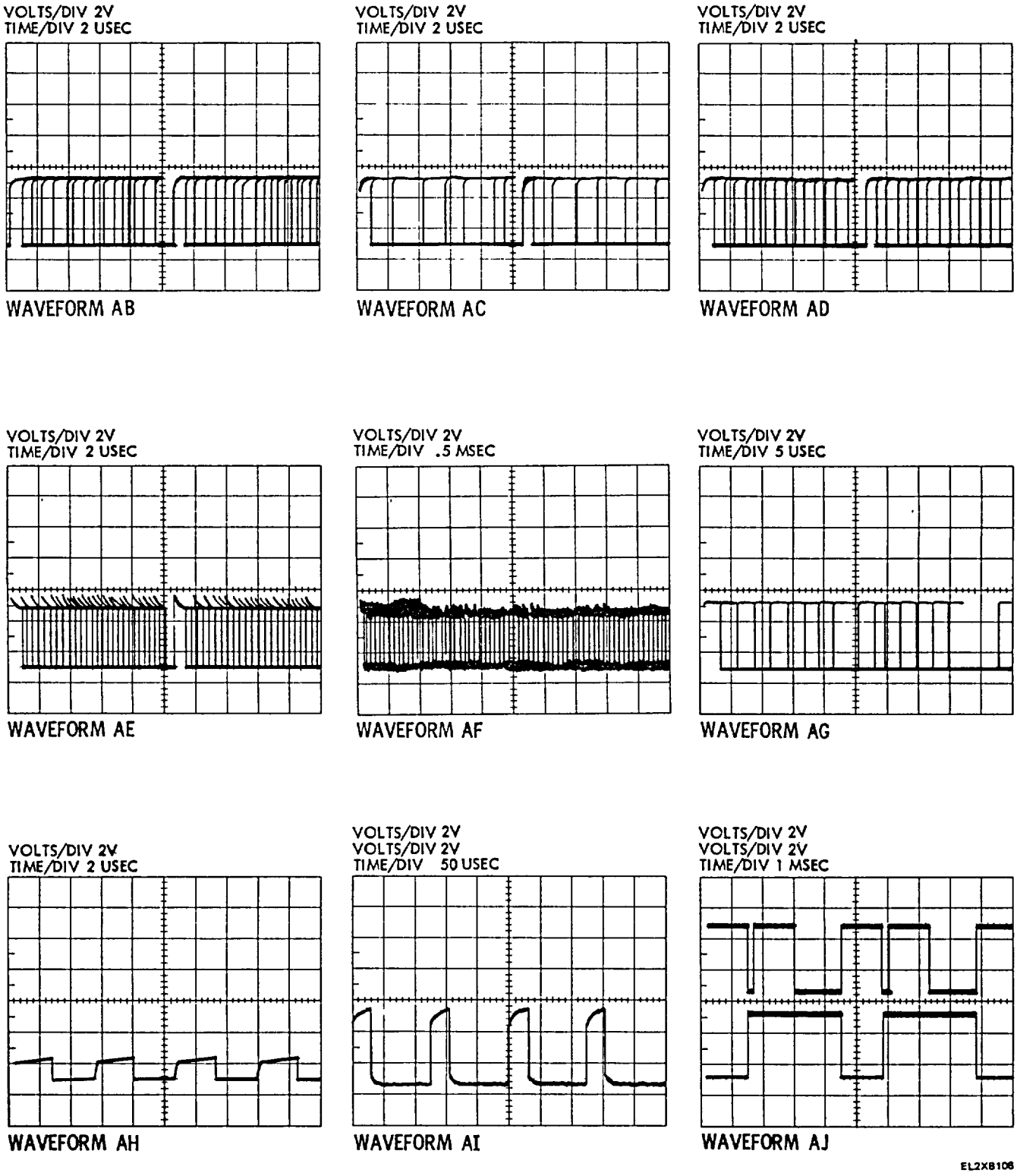


Figure 3-16. DEMUX unit troubleshooting waveforms (sheet 4 of 8).

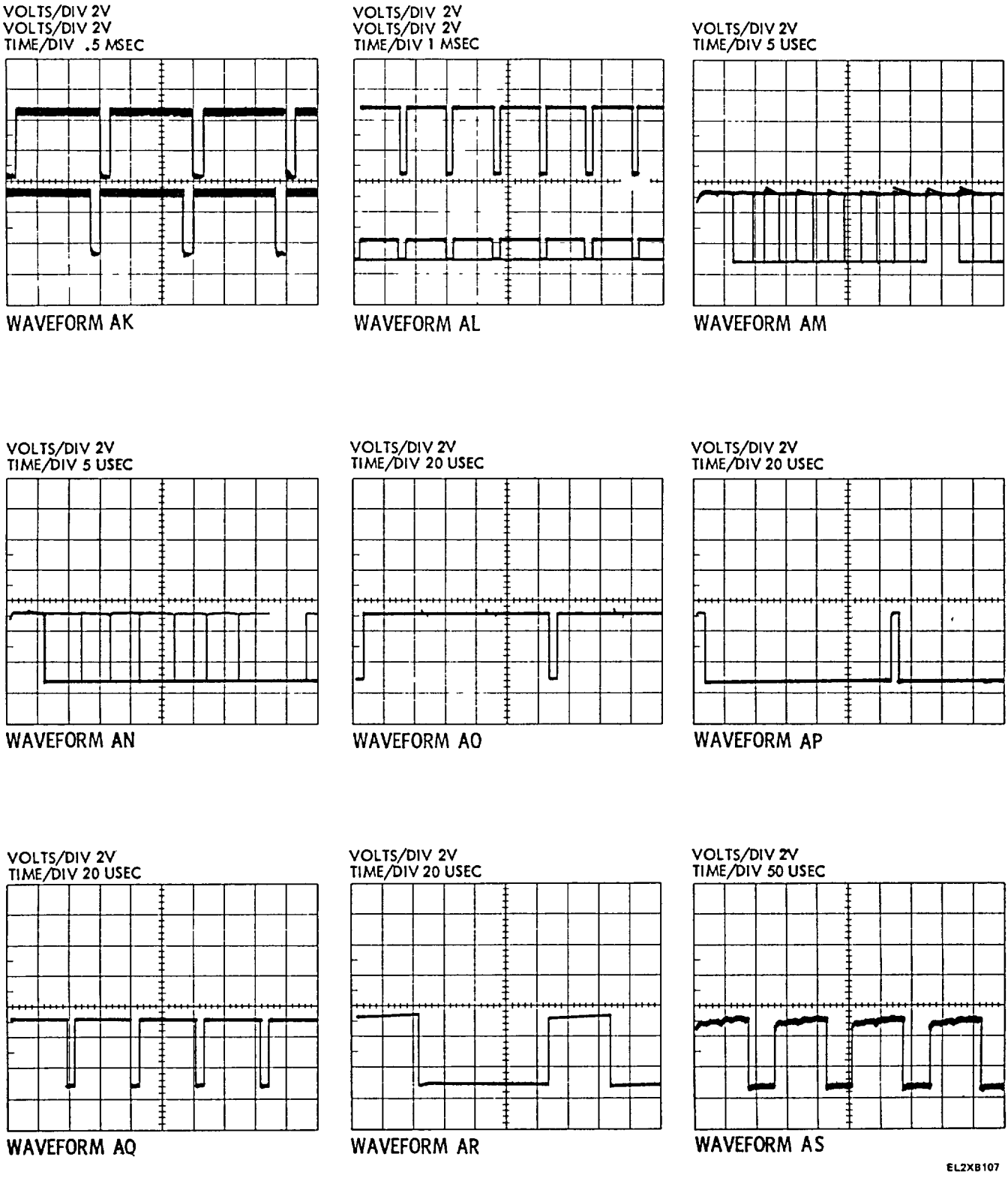


Figure 3-16. DEMUX unit troubleshooting waveforms (sheet 5 of 8).

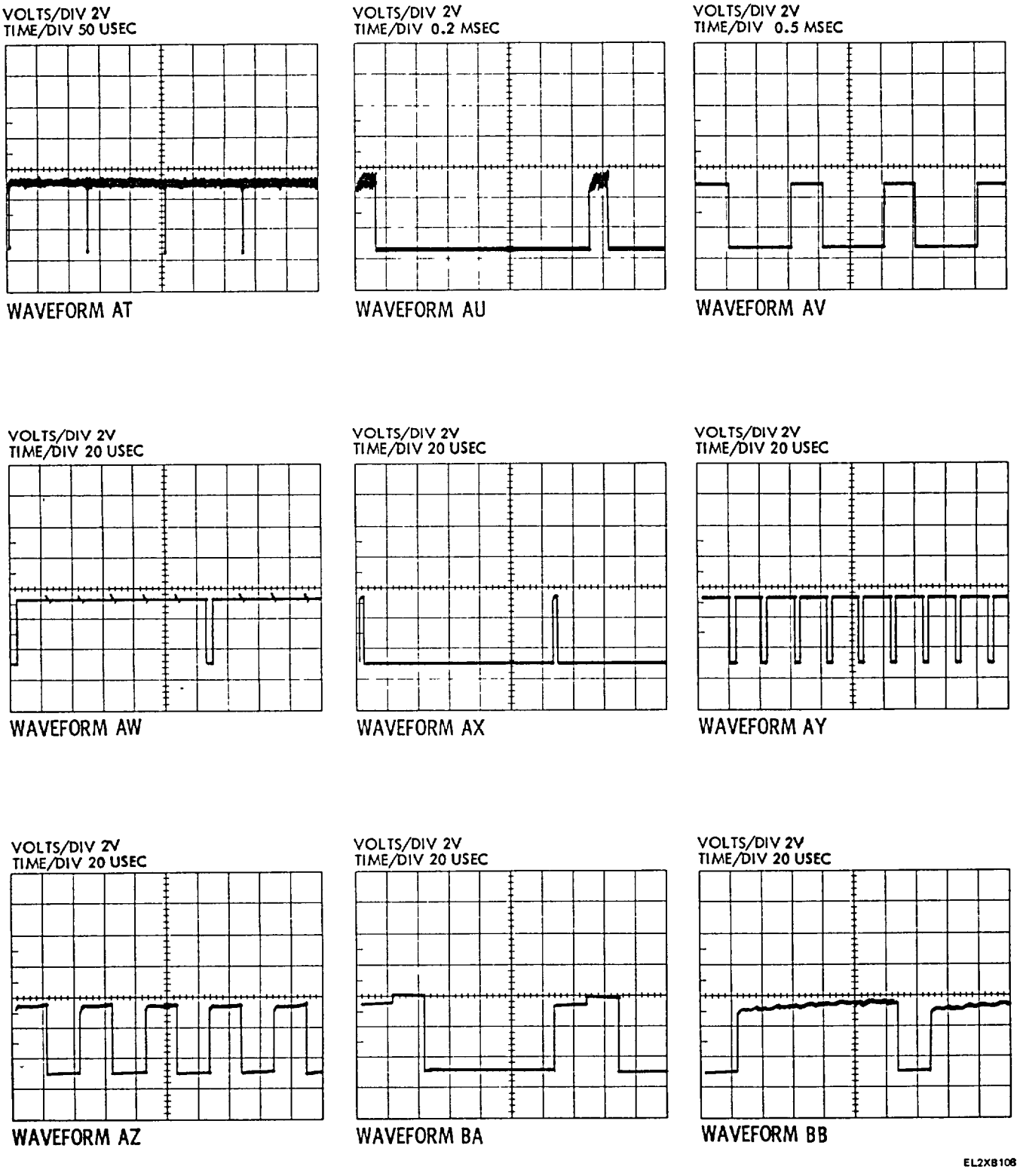


Figure 3-16. DEMUX unit troubleshooting waveforms (sheet 6 of 8).

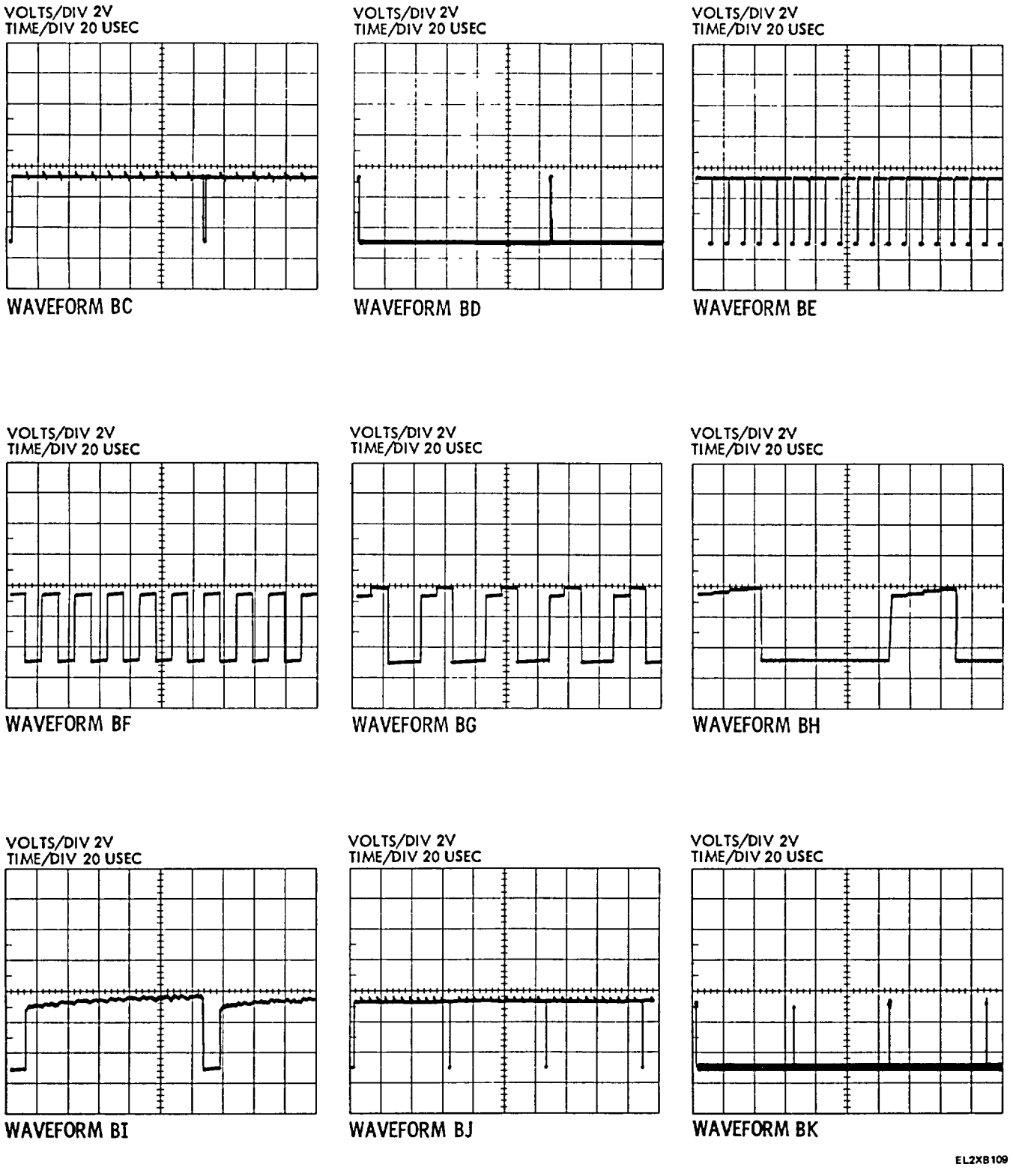


Figure 3-16. DEMUX unit troubleshooting waveforms (sheet 7 of 8).

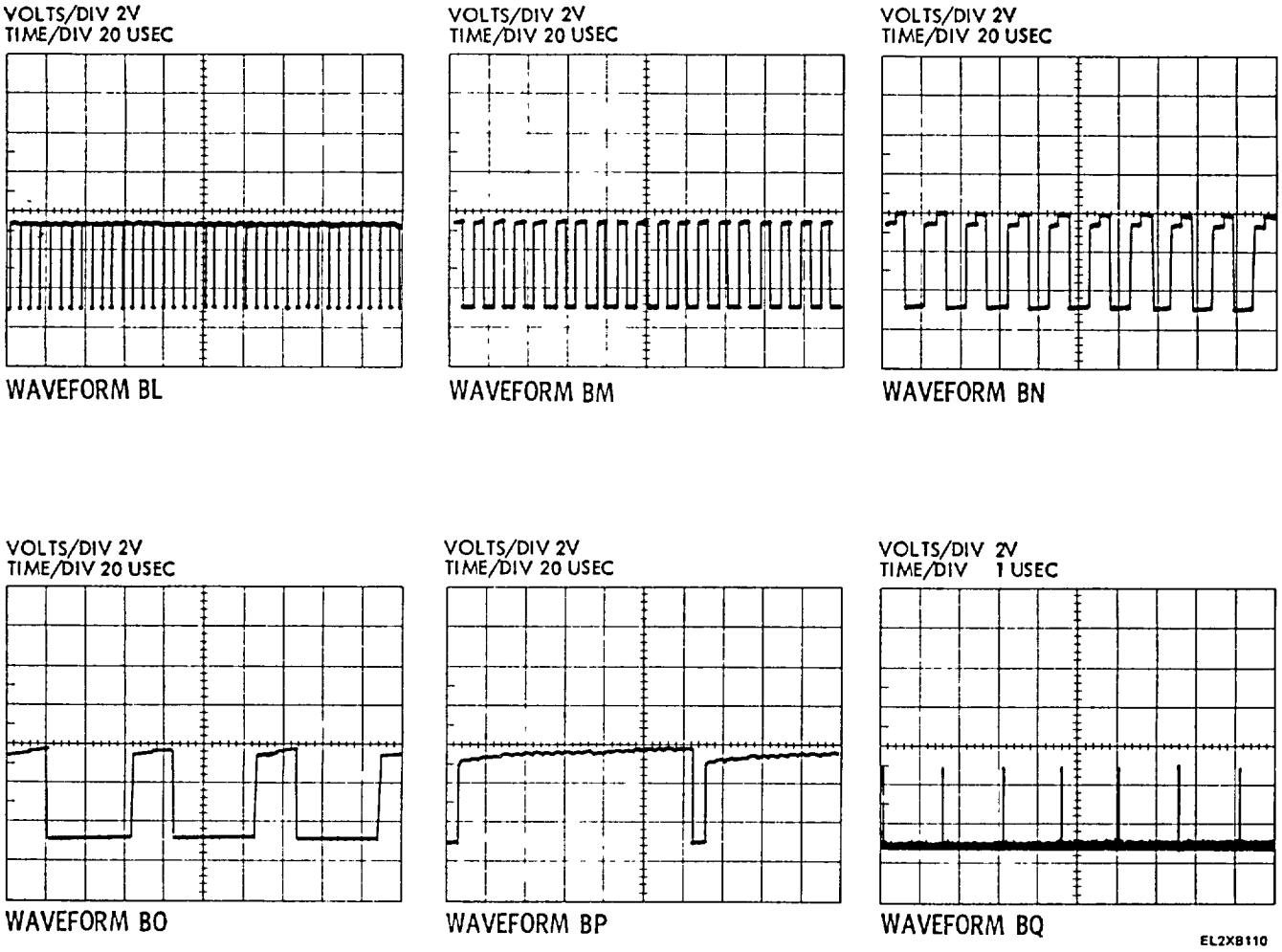


Figure 3-16. DEMUX unit troubleshooting waveforms (sheet 8 of 8).

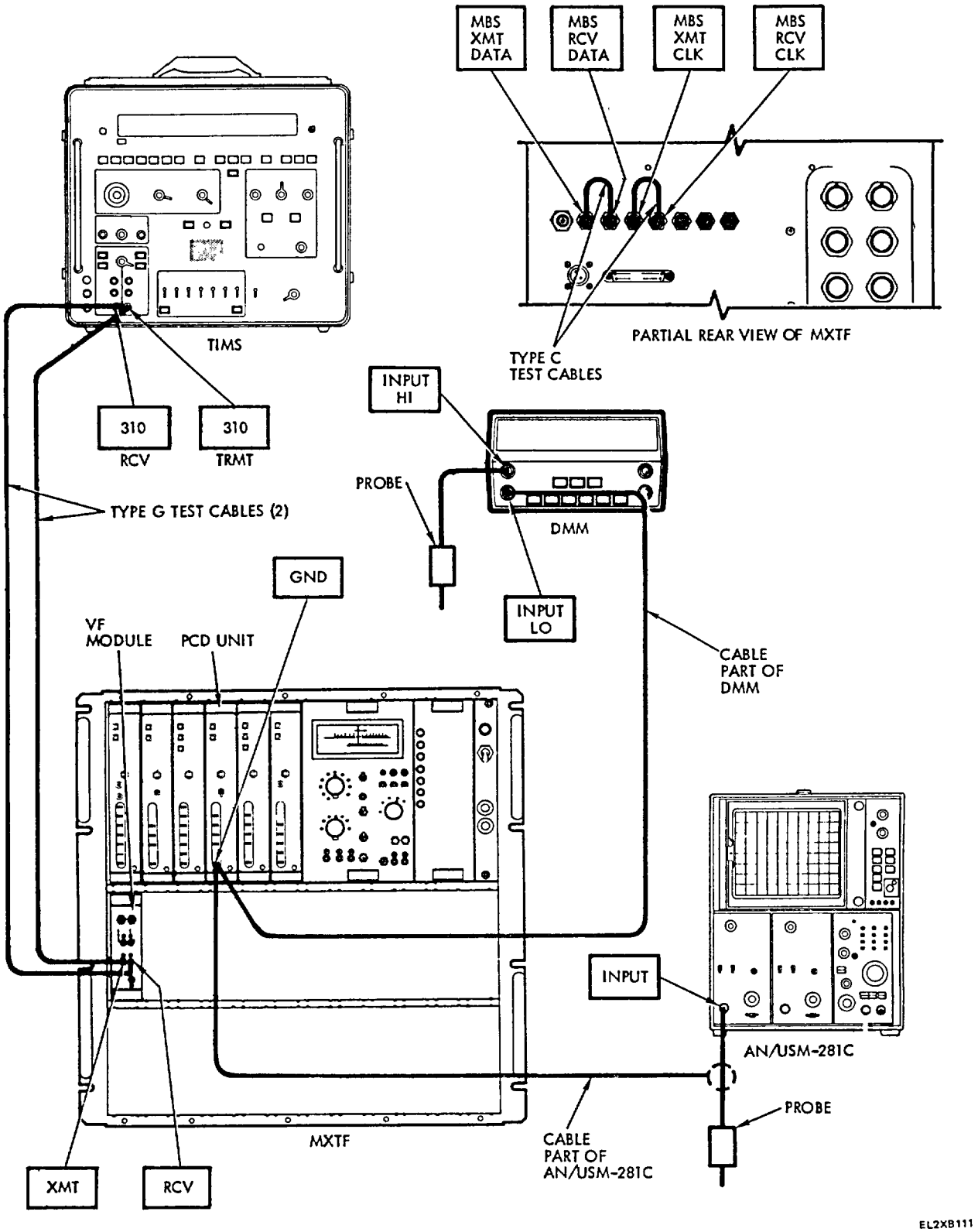


Figure 3-17. PCD unit troubleshooting diagram.

3-13. Troubleshooting PCD Unit

The following instructions and data are for use in troubleshooting faulty PCD units. Refer to figure FO-7 and figure 3-18 for parts location.

a. Tools and Test Equipment

(1) TK-100/G.
(2) AN/USM-281C.
(3) TIMS.
(4) DMM.
(5) MXTF with the following accessories:
Extender board TRW 17332-010
Type A test cables (2)
Type C test cables (2)
Type G test cables (2)
Spare VF modules (2).

b. Initial Equipment Setup. Set up equipment and UUR in accordance with the following instructions:

(1) Set power switch on MXTF PWR CONT to OFF.

(2) Remove MXTF PCD module, and using extender board, install UUR.

(3) Connect UUR and test equipment as shown in figure 3-17.

(4) Set test equipment switches as follows:

Unit	*Control*	*Setting*
AN/USM-281C	VOLTS/DIV (LEFT)	2
	TIME/DIV	.5 µs
	TRIG SOURCE	RIGHT
	MODE	LEFT
	POWER	Pull
DMM	RANGE	1 VOLT
	POWER	On
TIMS	MEASUREMENT	LEVEL and FREQUENCY
	FREQUENCY CONTROL	STEP 100 Hz
	FREQUENCY	1004
	DISPLAY CONNECTED TO	RCV
	SETUP CONTROLS	NORMAL TEST
		TEST WITHOUT HOLD
		TALK BATTERY OFF
		TERM 600
		NO SF SKIP
		NORMAL TEST
	RECEIVE/TRANSMIT JACKS switch	Up position
	POWER	ON
MXTF (PWR CONT)	Power	ON

NOTE

Allow equipment to warm up for 5 minutes before proceeding with test.

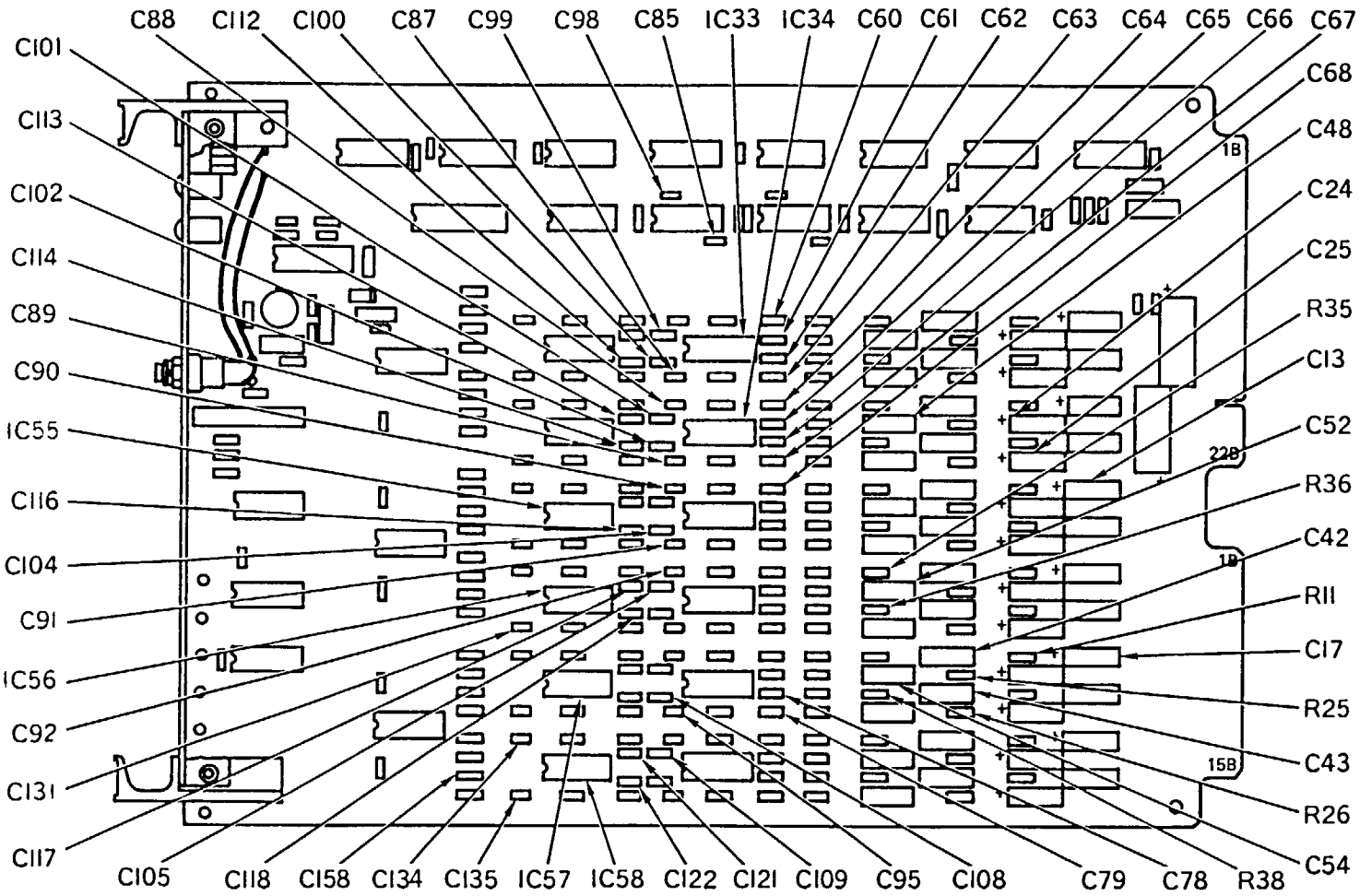
c. Fault Location. Troubleshoot in accordance with the following procedure to locate malfunctioning area of the PCD unit.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-19
1			Check input buffers. If result of any check is incorrect, isolate and replace faulty component.	
			a. Adjust TIMS OUTPUT LEVEL control until TIMS display indicates correct level for VF module strapping indicated.	*a.* VF module *strapping* / TIMS *display*: A strap in / -16 dBm; B strap in / 0 dBm
	AN/USM-281C		*b*. Check signal at IC12-6.	*b*. Waveform A.
	TIME/DIV:	2 µs	*c*. Check signal at PCM DATA test point on UUR.	c. Waveform B.
	MXTF (MUX)			
	1 KHZ TONE:	ON for step		
			d. Using DMM, check signal level at IC72-11.	*d*. 0 to ±0.1 Vdc.
			e. Using DMM, check signal level at IC72-12.	*e*. 0 to ±0.1 Vdc.
2			Check SERIAL-TO-PARALLEL CONVERTER circuit (IC52 and IC62). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-19
	TIME/DIV:	20 µs	*a.* Check signal at IC62-2.	*a.* Waveform C.
	TIME/DIV:	50 µs	*b.* Check signal at IC62-5.	*b.* Waveform D.
			c. Check signal at IC62-6.	*c.* Waveform D.
	TIME/DIV:	.2 ms	*d.* Check signal at IC62-9.	*d.* Waveform E.
			e. Check signal at IC62-12.	*e.* Waveform F.
			f. Check signal at IC62-15.	*f.* Waveform F.
			g. Check signal at IC62-16.	*g.* Waveform F.
	TIME/DIV:	10 µs	*h.* Check signal at IC62-19.	*h.* Waveform G.
3			Check D TO A CONVERTER circuit (IC72). If result of either check is incorrect, isolate and replace faulty component.	
	MXTF (MUX)			
	1 KHZ TONE:	ON for steps *a* and *b*		
	AN/ USM-281C			
	VOLTS/DIV:	.5V		
	TIME/DIV:	.5 ms	*a.* Check signal at IC72-16.	*a.* Waveform H.
			b. Check signal at IC72-17.	*b.* Waveform H.
4			Check CURRENT DRIVER circuit (AR1). If result of check is incorrect, isolate and replace faulty component.	
	MXTF (MUX)		Check signal at PAM test point on UUR.	Waveform *J*.
	1 KHZ TONE:	ON for this step		
5			Check SAMPLE ENABLE circuit (IC1, IC11 and IC12). If result of either check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	2 µs	*a.* Check signal at IC1-2.	*a.* Waveform K.
	TIME/DIV:	2V	*b.* Check signal at IC11-13.	*b.* Waveform L.
6			Check CHANNEL COUNT DECODER SELECT circuit (IC11, IC41, IC51 and IC71). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C		*a.* Check signal at IC11-4.	*a.* Waveform M.
	TIME/DIV:	10 µs	*b.* Check signal at IC71-8.	*b.* Waveform N.
			c. Check signal at IC71-11.	*c.* Waveform P.
7			Check SIGNALING circuit (IC12, IC21, IC61 and IC71). If result of check is incorrect, isolate and replace faulty component.	
			Check signal at SIG test point on UUR.	Waveform Q.
8			Check CHANNEL COUNT DECODER OUTPUT SELECT circuit (IC21, IC31, and IC41). If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	5 µs	*a.* Check signal at IC41-8.	*a.* Waveform R.
	TIME/DIV:	10 µs	*b.* Check signal at IC31-8.	*b.* Waveform S.
	TIME/DIV:	20 µs	*c.* Check signal at IC31-6.	*c.* Waveform T.
9	*MXTF (BITE)*		Check CHANNEL DECODE circuit (IC73, IC74, IC75 and IC81). If result of any check is incorrect, isolate and replace faulty component.	
	DIGITAL FUNCTION:	SELF TEST		
	VF FUNCTION:	LOOP TEST		

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-19
	OSC LVL: (Set for VF module strapping indicated)	*Vf* Module *Straps* A strap in -16 dBm B strap in 0 dBm		
	(RCVR) LOOP/NORMAL:	LOOP		
	(PWR CONT) Power:	ON		
	TIMS MEASUREMENT:	MESSAGE CIRCUIT NOISE		
	NOISE FILTER:	C-MSG		
			a. Install spare VF modules in channels 1 (left) and 2 (right).	*a.* None.
			b. Connect VF OSC jack on BITE to lower XMT jack on VF module in left channel, using type A cable.	*b.* None.
			c. Connect illuminated 310 RCV jack on TIMS to lower RCV jack on right VF module, using type G cable.	*c.* None.
			d. Verify TIMS display for VF module strapping indicated. Disconnect both cables.	*d.* VP module *strapping TIMS display* C strap in ≤25 DBRN C strap out ≤32 DBRN
			e. Connect VF OSC on BITE to lower XMT jack on right VF module, using type A cable.	*e.* None.
			f. Connect illuminated 310 RCV jack on TIMS to lower RCV jack on left VF module.	*f.* None.
			g. Verify TIMS display for VF module strapping indicated. Disconnect both cables.	*g.* VF module *straps TIMS display* C strap in ≤25 DBRN C strap out ≤32 DBRN
			h. Move left VF module to next open channel in MXTF.	*h.* None.
			i. Repeat steps e through h until all channels have been checked.	*i.* None.
			j. Remove VF modules from MXTF.	*j.* None.
10			Check FAULT MONITOR circuit (IC32, IC42, and IC22). If result of any check is incorrect, isolate and replace faulty component.	
	UUR FAULT TEST:	Push	*a.* Observe FAULT and ALL FAULT TEST lamps on UUR.	*a.* Lamps illuminate.
			b. Check signals at IC32-2, IC32-10, IC42-2 and IC42-10.	*b.* Activity at each input.
			c. Check signals at IC32-13, IC32-5, IC32-5, IC42-13 and IC42-5.	*c.* Logic level high.
			d. Check signal at IC22-8.	*d.* Logic level low.
11			Check output filters (IC33, IC34, IC35, IC36, IC37, IC38, IC53, IC54, IC55, IC56, IC57, IC58, IC73, IC74, IC75, IC76, IC77, and IC78). If result of any check is incorrect, isolate and replace faulty component.	

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-19
	TIMS		*a.* Install spare VF module in channel 1 slot.	*a.* None.
	FUNCTION:	LEVEL and FREQUENCY	*b.* Connect 310 RCV jack on TIMS to lower RCV jack on VF module, using type G cables. Connect 310 TRMT jack on TIMS to lower XMT jack on VF module, using type G cables.	*b.* None.
			c. Verify TIMS display for VF module strapping indicated.	*c.* VF module *straps* — *TIMS display* C strap in — 0 ±.2 dBm C strap out — 7 ±.2 dBm
			d. Move VF module to progressively higher channels, repeating step c. If any channel does not meet the requirements in c above, troubleshoot output filters in accordance with the procedure in step 12 above.	*d.* None.
12			Troubleshoot sample and hold and output filters. If result of any check is incorrect, isolate and replace faulty component.	
	AN/USM-281C			
	TIME/DIV:	5 ms	*a.* Check output signal of demultiplexer for defective channel (refer to table 3-5 for pin location).	*a.* Waveform U.
	VOLTS/DIV:	IV	*b.* Check output signal of sample and hold circuit for defective channel (refer to table 3-5 for pin location).	*b.* Waveform U.
			c. Check output signal of output filter for defective channel (refer to table 3-5 for pin location).	*c.* Waveform V.

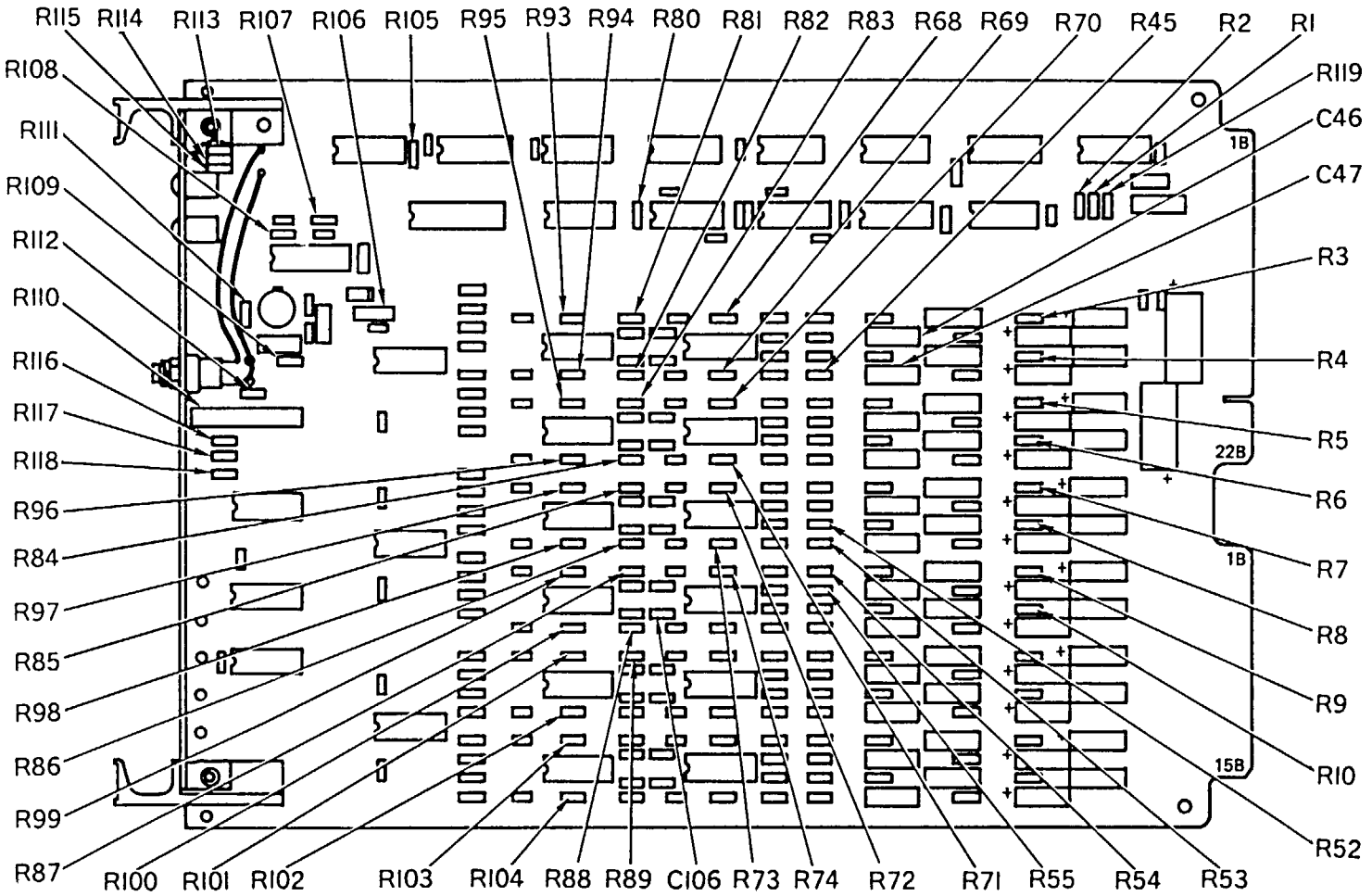


NOTE:

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB112

Figure 3-18 . PCD unit parts location diagram (sheet 1 of 6).

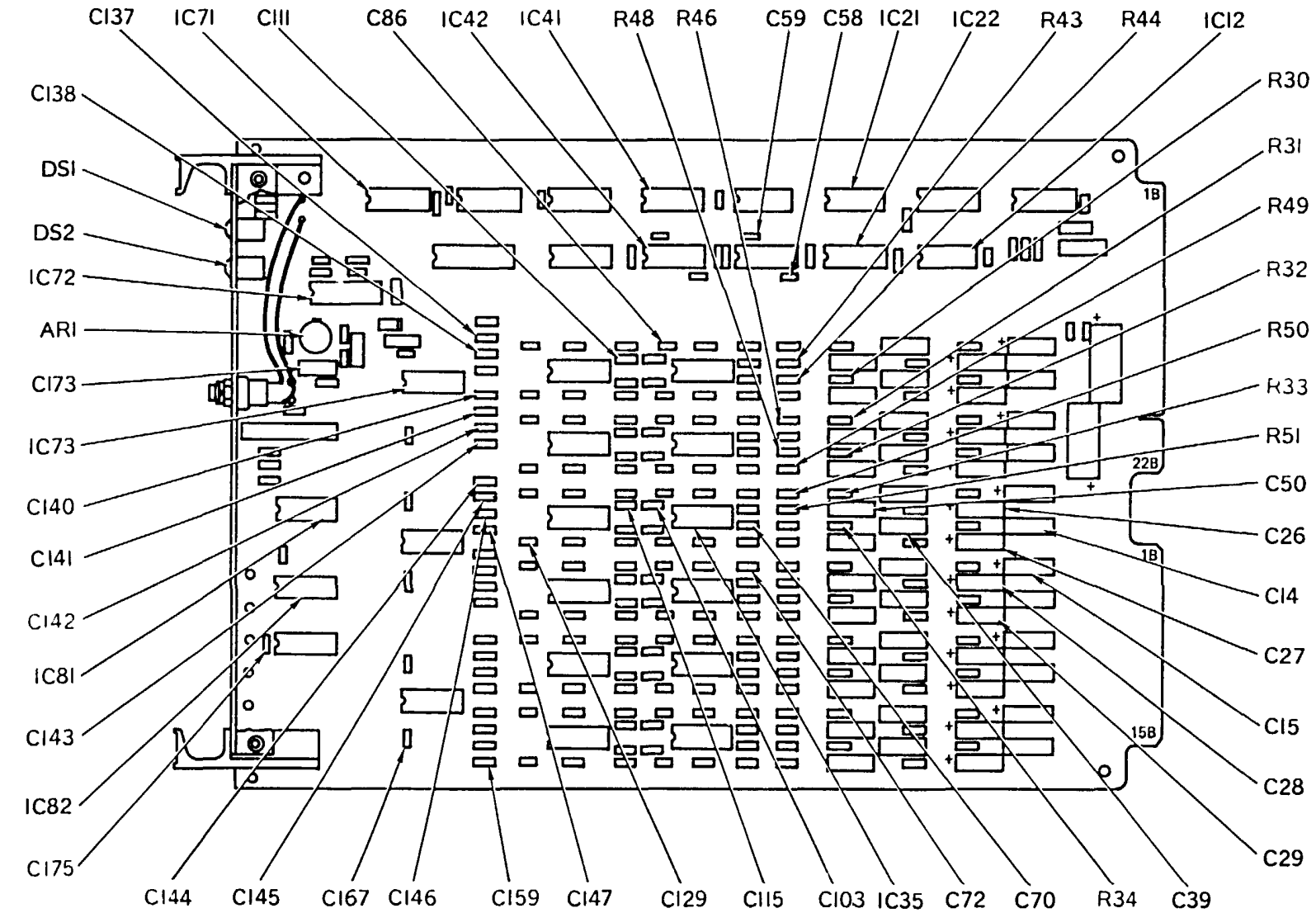


NOTE:

22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR, B-SIDE FACING A-SIDE OPPOSITE.

EL2XB113

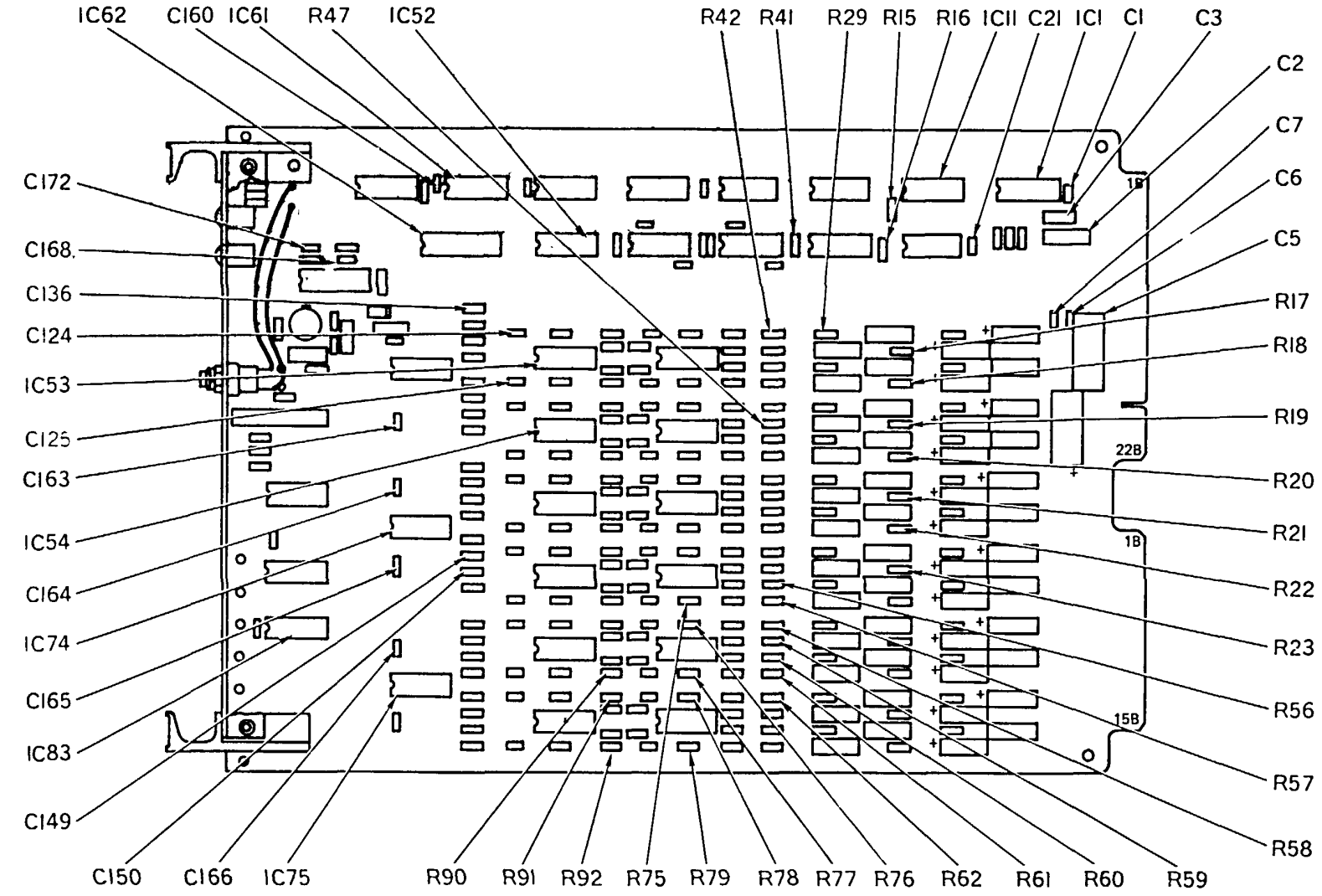
Figure 3-18. PCD unit parts location diagram (sheet 2 of 6).



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING A-SIDE OPPOSITE.

EL2XB114

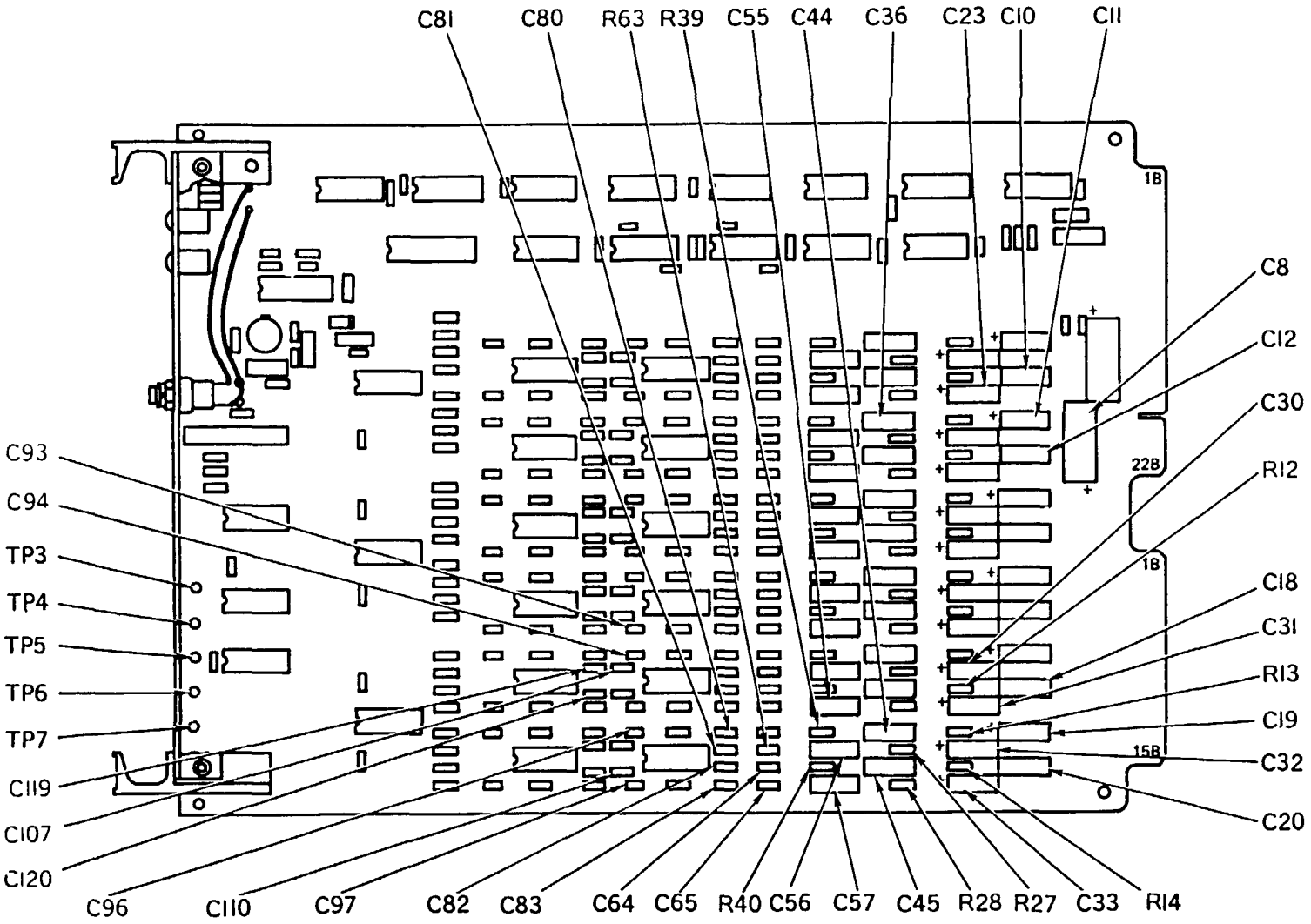
Figure 3-18. PCD unit parts location diagram (sheet 3 of 6).



NOTE.
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB115

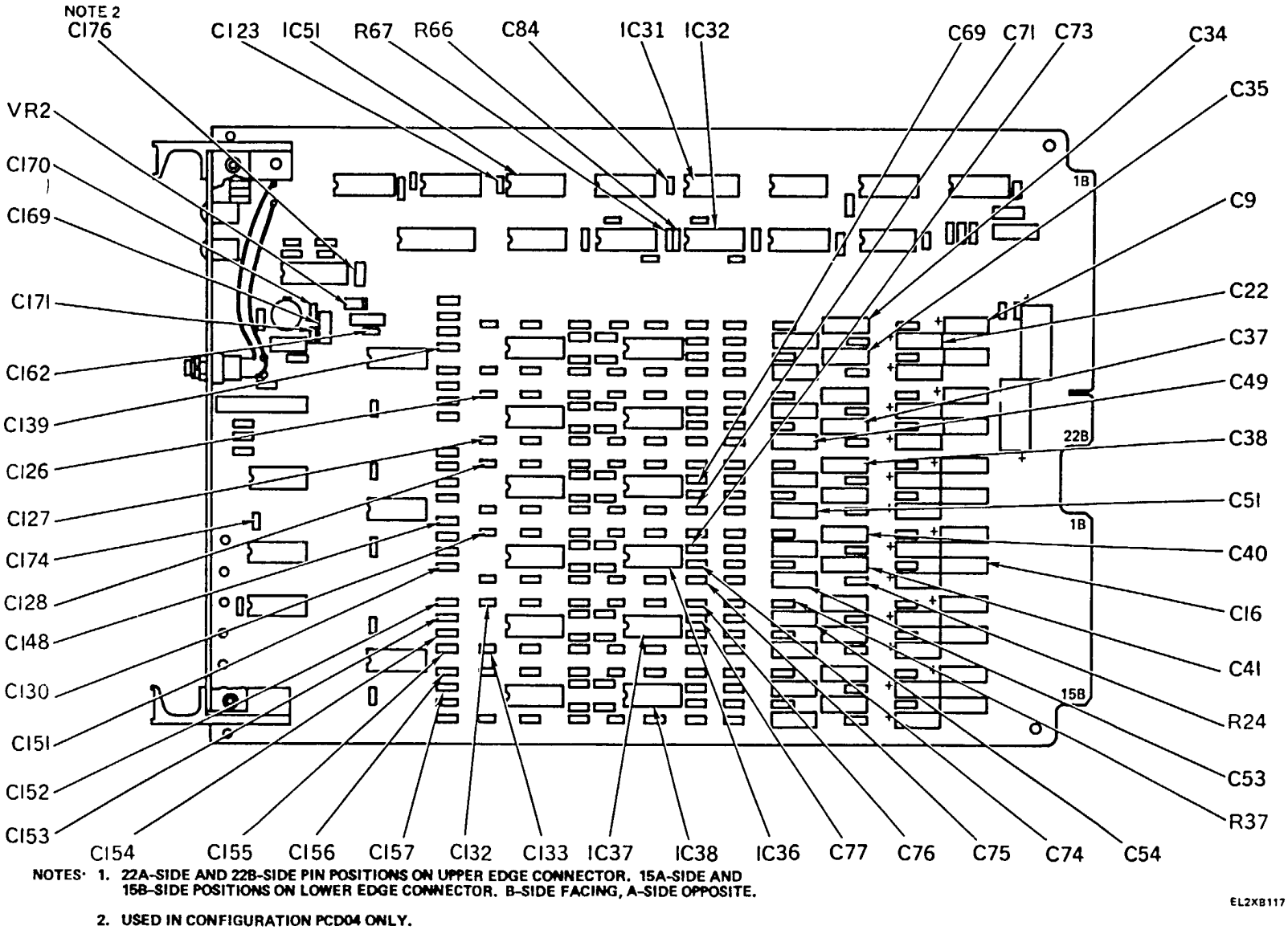
Figure 3-18. PCD unit parts location diagram (sheet 4 of 6).



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING A-SIDE OPPOSITE.

EL2XB116

Figure 3-18. PCD unit parts location diagram (sheet 5 of 6).



NOTES: 1. 22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

2. USED IN CONFIGURATION PCD04 ONLY.

Figure 3-18. PCD unit parts location diagram (sheet 6 of 6).

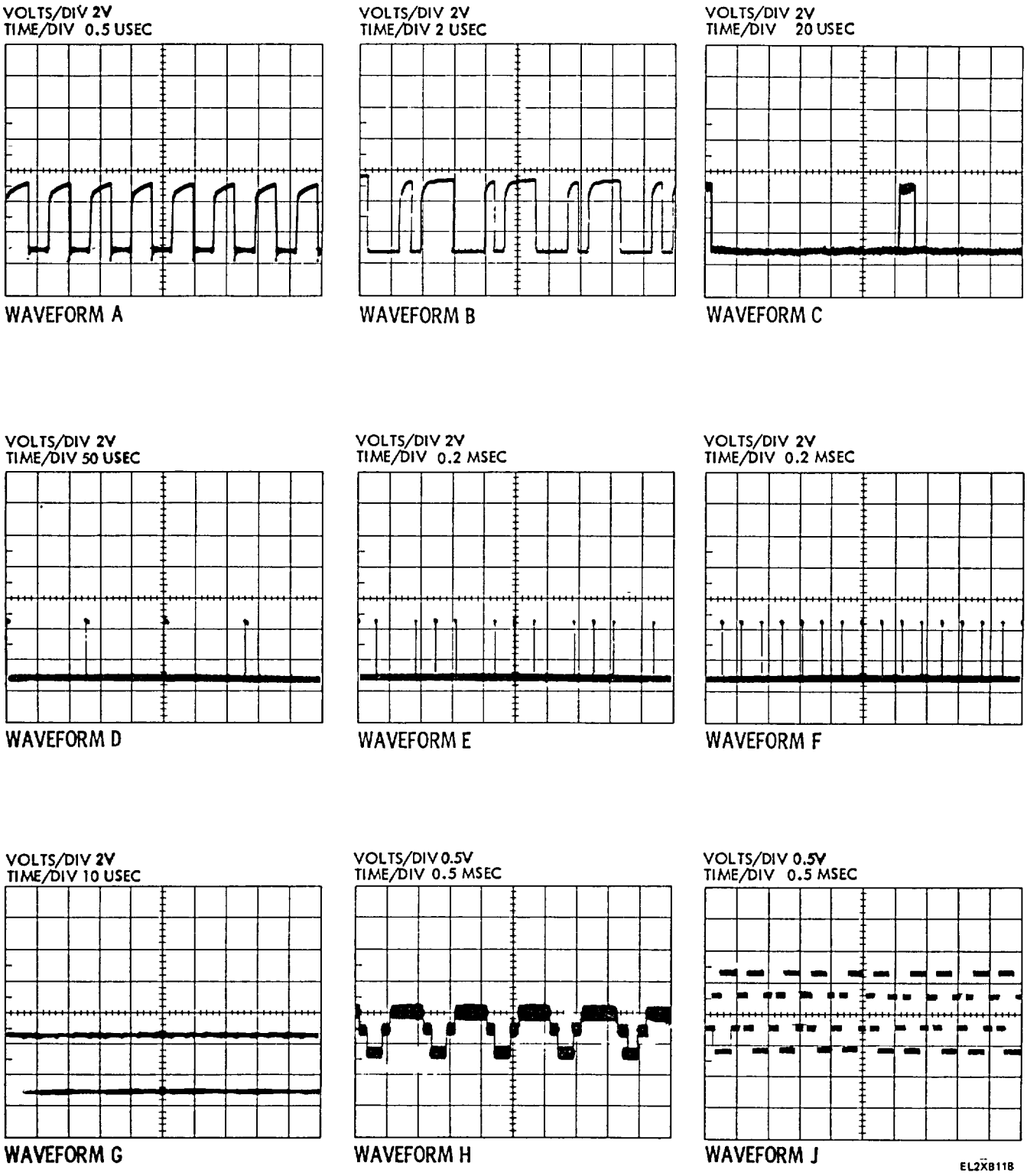


Figure 3-19. PCD unit troubleshooting waveforms (sheet 1 of 3).

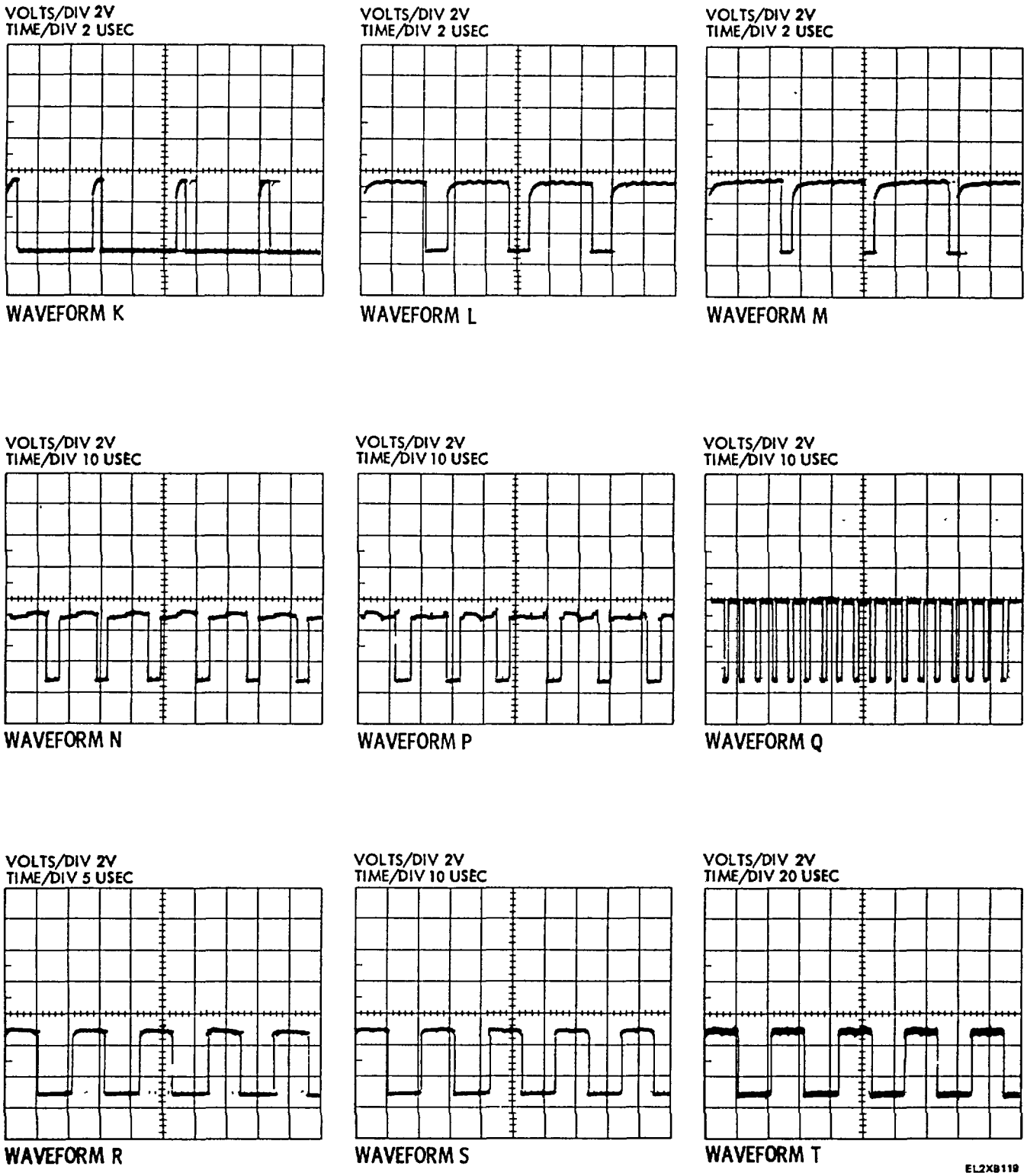


Figure 3-19. PCD unit troubleshooting waveforms (sheet 2 of 3).

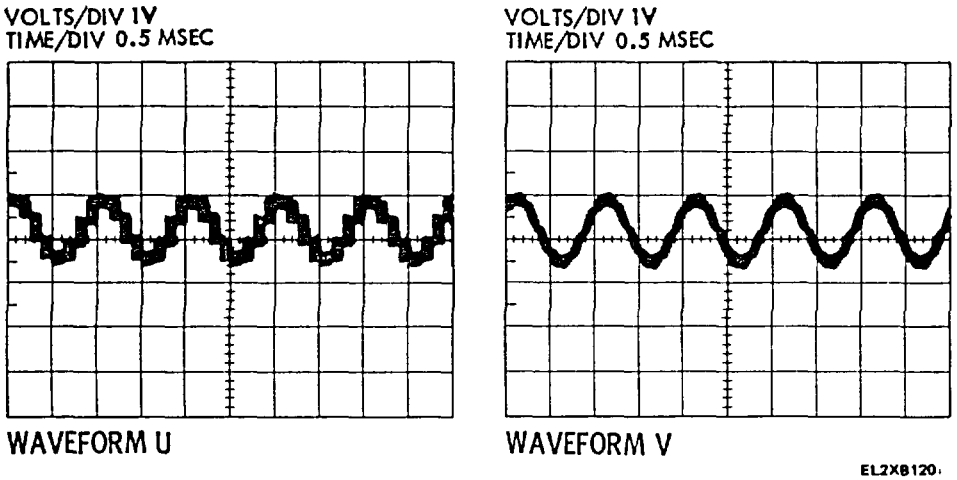


Figure 3-19. PCD unit troubleshooting waveforms (sheet 3 of 3).

Table 3-5. Demultiplexer, sample and hold, and filter outputs

Chan.	Demultiplexer output	Sample and hold output	Filter output
1	IC73 Pin 4	IC54 Pin 1	IC54 Pin 7
2	IC74 Pin 5	IC36 Pin 1	IC36 Pin 7
3	IC75 Pin 6	IC38 Pin 14	IC38 Pin 8
4	IC73 Pin 7	IC54 Pin 14	IC54 Pin 8
5	IC74 Pin 12	IC55 Pin 14	IC55 Pin 7
6	IC75 Pin 11	IC37 Pin 14	IC37 Pin 8
7	IC73 Pin 10	IC33 Pin 1	IC33 Pin 7
8	IC74 Pin 9	IC55 Pin 1	IC55 Pin 7
9	IC75 Pin 9	IC58 Pin 1	IC58 Pin 7
10	IC73 Pin 5	IC34 Pin 1	IC34 Pin 7
11	IC74 Pin 6	IC36 Pin 14	IC36 Pin 8
12	IC75 Pin 7	IC58 Pin 14	IC58 Pin 8
13	IC73 Pin 12	IC53 Pin 8	IC53 Pin 14
14	IC74 Pin 11	IC35 Pin 14	IC35 Pin 8
15	IC75 Pin 10	IC37 Pin 1	IC37 Pin 7
16	IC73 Pin 9	IC53 Pin 1	IC53 Pin 7
17	IC74 Pin 4	IC56 Pin 1	IC56 Pin 7
18	IC75 Pin 5	IC38 Pin 1	IC38 Pin 7
19	IC73 Pin 6	IC34 Pin 14	IC34 Pin 8
20	IC74 Pin 7	IC56 Pin 14	IC56 Pin 8
21	IC75 Pin 12	IC57 Pin 14	IC57 Pin 8
22	IC73 Pin 11	IC33 Pin 14	IC33 Pin 8
23	IC74 Pin 10	IC35 Pin 1	IC35 Pin 7
24	IC75 Pin 9	IC57 Pin 1	IC57 Pin 7

3-14. Troubleshooting VF Module

Instructions and data for use in isolating VF module faults are given in the following subparagraphs. Refer to figure FO-8 and figure 3-21 for parts location.

a. Tools and Test Equipment.

(1) TK-100/G.
(2) TA-855/U.
(3) TS-3329/U.
(4) An/USM-281C with external sync cable.
(5) AN/USM-223.
(6) MXTF and the following accessories:
Extender board TRW 17080-010
Type A (bantam) test cable
Type C test cables (2)
Type G test cables (2).

b. *Initial Setup*. Set up test equipment and faulty VF module for troubleshooting as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.

(2) Strap UUR for -16 dB input, normal signaling, and +7 dB output in accordance with table 3-4.

(3) Using extender board, install UUR into channel 1 position in MXTF.

(4) Connect test equipment to VF module as shown in figure 3-20.

(5) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
TS-3329/U	FUNCTION	600
	FREQUENCY RANGE	X100
	OUTPUT LEVEL DBM	-16
	FREQUENCY Hz	10.2
	POWER	ON
TAA-855/U	RESPONSE	DAMP
	INPUT	TMS-TERM
	FUNCTION VF Nm	600 BAL
	RANGE	-10 dBm
	POWER	ON
AN/USM-281C	VOLTS/DIV (left)	.1V
	TIME/DIV	.2 ms
	AC/GND/DC	AC
	Power	Pull
MXTF (RCVR)	LOOP-NORMAL	NORMAL
(PWR CONT)	Power	ON

NOTE

Allow equipment to warm up for 5 minutes before proceeding.

c. Fault Location. Troubleshoot in accordance with the following procedure to locate malfunctioning areas of the UUR.

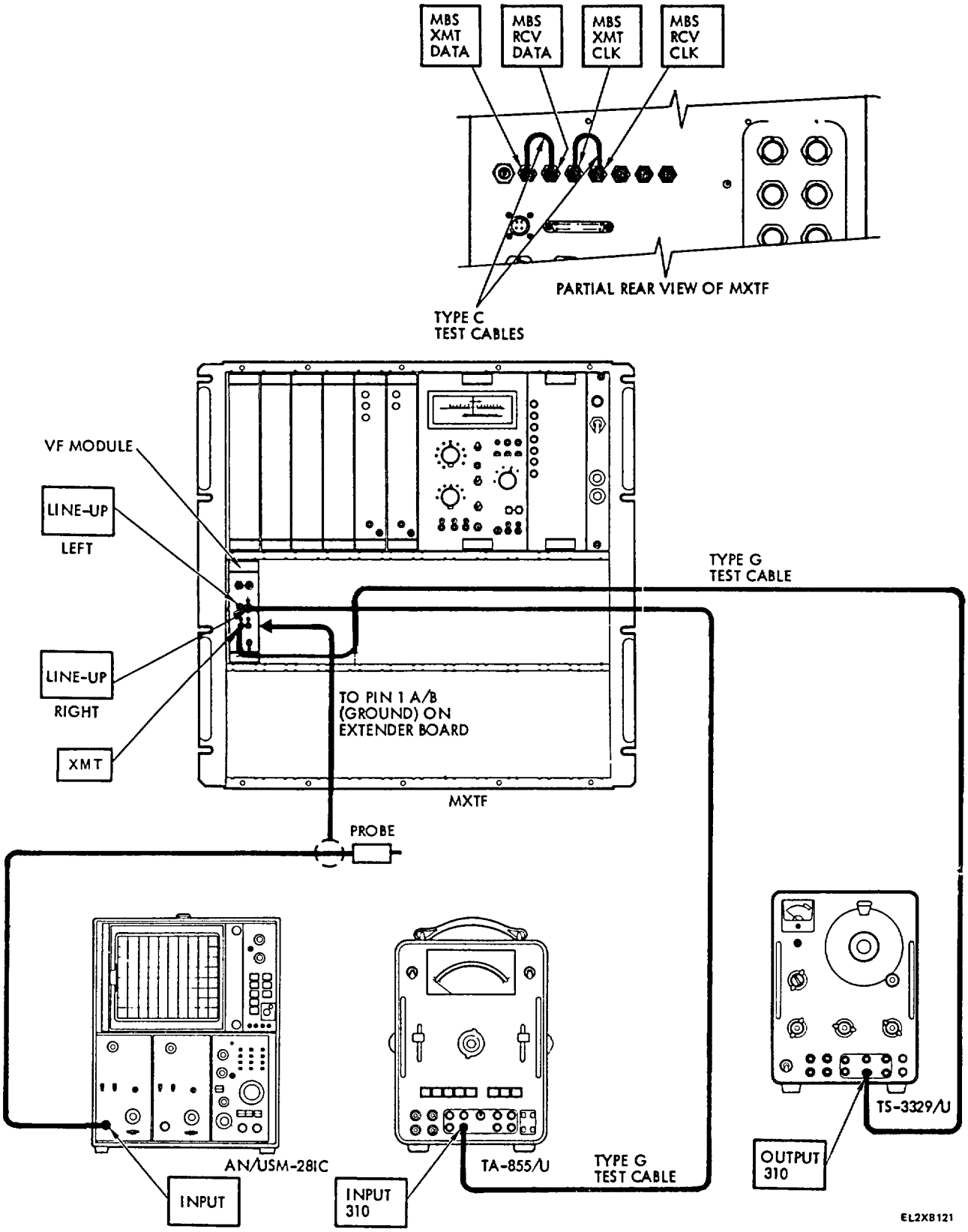
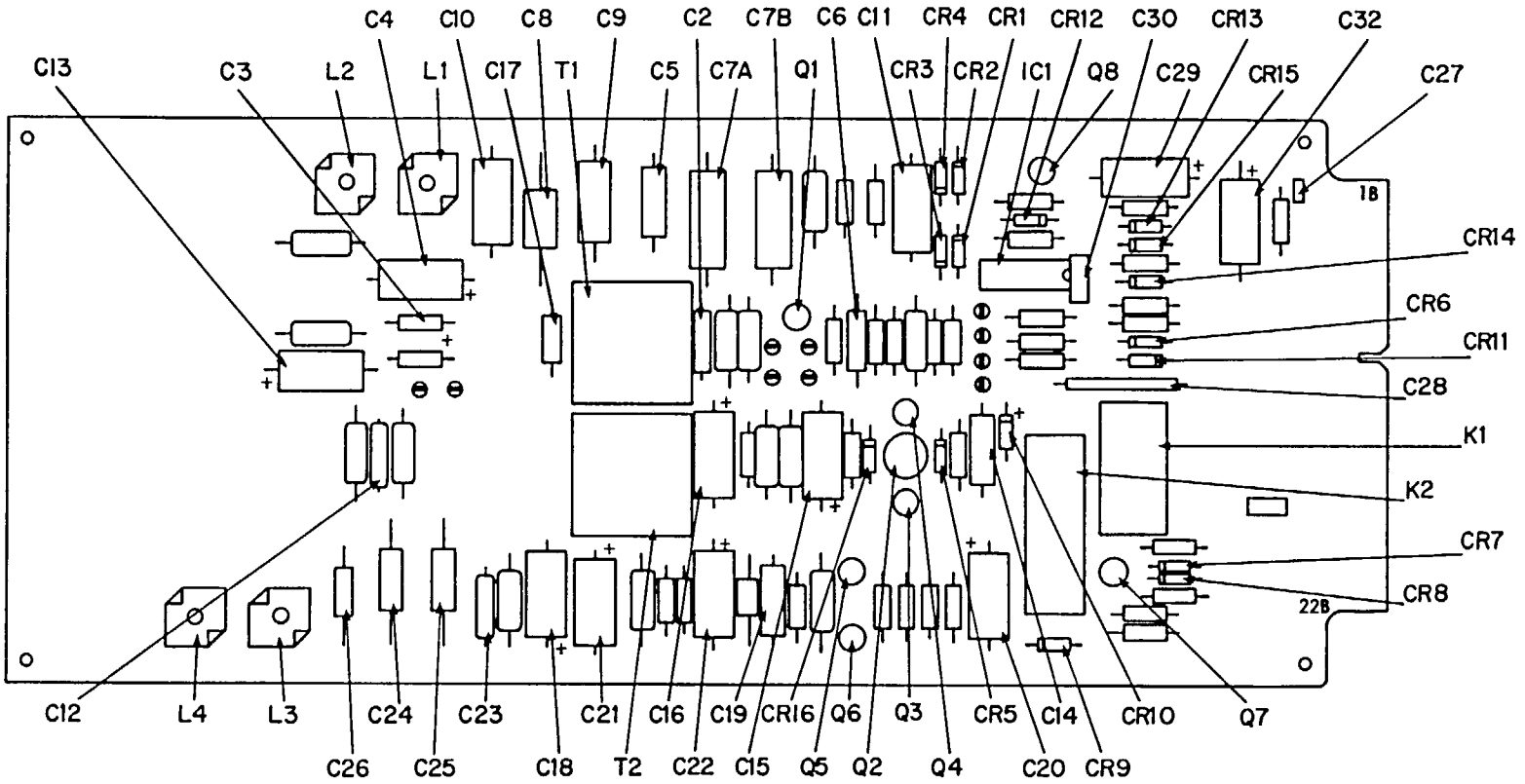


Figure 3-20. VF module troubleshooting setup diagram.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-22
1			Verify VF transmit function (Q1) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
			NOTE **The XMT GAIN control on the VF module has no mechanical stop. It has reached its limit of adjustment when the TS-855/U meter ceases to change.**	
			a. Rotate XMT GAIN control on UUR to clockwise and counterclockwise limits of adjustment while observing TA-855/U meter. Verify range of control is normal.	*a.* At least -11 dBm to -16 dBm range of control.
			b. Rotate XMT GAIN control on UUR as necessary to obtain normal gain indication on TA-855/U dBm meter. If indication is correct, proceed to step 2.	*b.* -13.75 +0.25 dBm.
			c. Check VF signal input at the bottom of R1. Connect ground lead of AN/USM-281C probe to pin 1B.	*c.* Waveform A.
			d. Check amplifier Q1 input at top of resistor R5.	*d.* Waveform B.
			e. Disconnect type G test cable between left-hand LINE-UP (transmit) and TA-855/U jacks.	*e.* None.
	AN/USM-281C			
	VOLTS/DIV:	2V	*f.* Check VF transmit output signal at pin 2A.	*f.* Waveform C.
2			Verify transmit signaling function (Q8) as follows. If either result is unsatisfactory, isolate and replace faulty component.	
	MXTF (BITE)		*a.* Connect type A (bantam) test cable between SIG jack on BITE and SIG jack on UUR, and observe OFF HOOK lamp on BITE.	*a.* Lamp illuminated.
	DIGITAL FUNCTION:	EXT CLK		
	ON HOOK-OFF HOOK:	OFF HOOK		
	MXTF (BITE)		*b.* Using external sync cable, synchronize AN/USM-281C externally at pin 9A and observe ON HOOK signal at pin 10A.	*b.* Waveform D.
	ON HOOK-OFF HOOK:	ON HOOK		
	AN/USM-281C			
	VOLTS/DIV:	1V		
	TIME/DIV:	1 µs		
	SOURCE:	EXT		
3			Verify VF receive preamplifier functions (Q5 and Q6) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
			a. Connect type G test cable between INPUT 310 jack on TA-855/U and right-hand LINE-UP (receive) jack on UUR.	*a.* None.
	MXTF (MUX)		*b.* Hold 1KHZ switch in up position and adjust GAIN control on PCD unit to obtain normal indication on TA-855/U meter.	*b.* -23.5 ±0.2 dBm.
	1 KHZ TONE:	ON for this step		

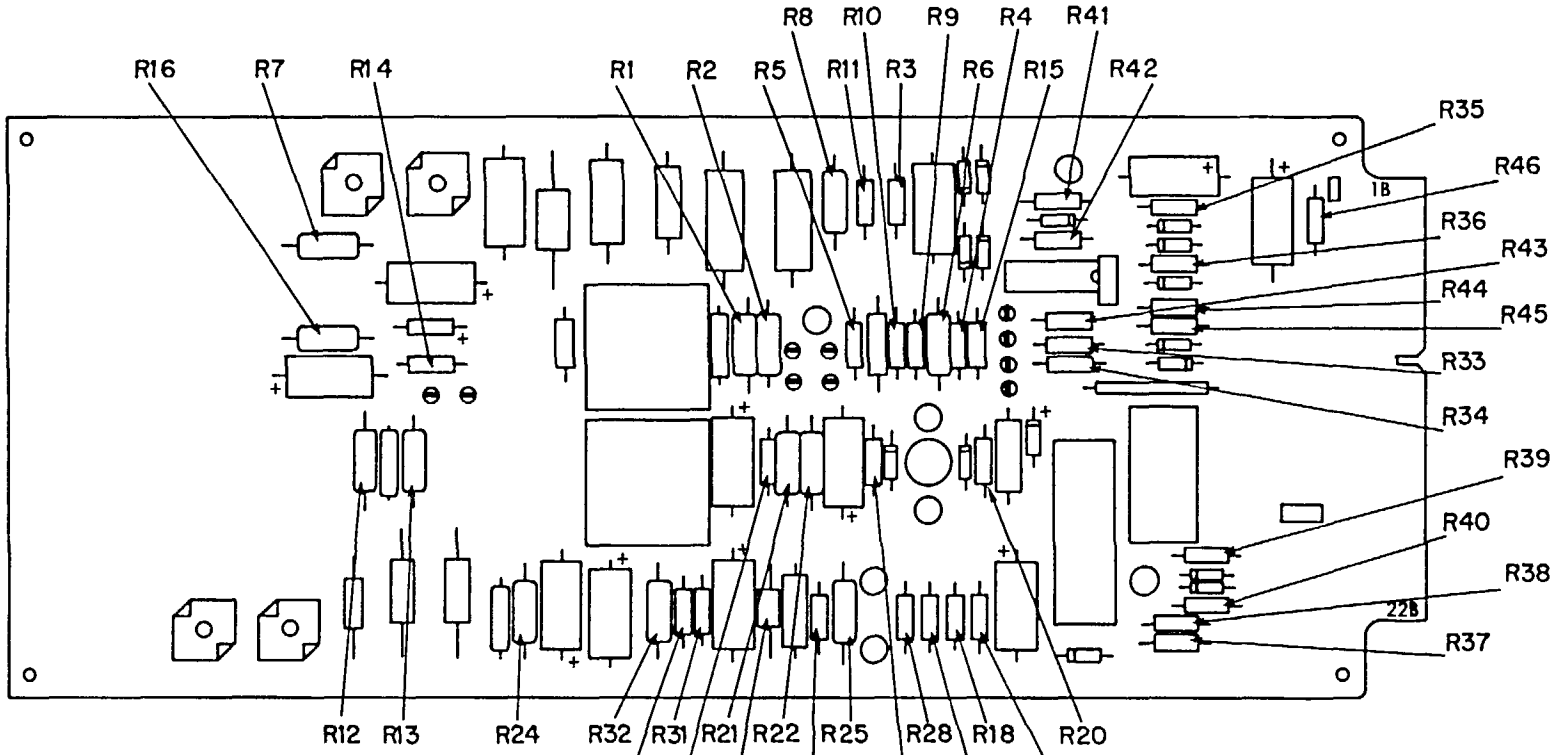
Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-19
	(PCM)		*c.* Adjust GRP-1 GAIN control to obtain normal indication on TA-855/U meter. If satisfactory TA-855/U indication can be obtained, proceed to step 4.	*c.* -23.5 -0.2 dBm.
	ODD GAIN:	As required		
	AN/USM-281C		*d.* Check receive VF filter output at the bottom of R28.	*d.* Waveform E.
	VOLTS/DIV:	1V		
	TIME/DIV:	2 ms	*e.* Using AN/USM-281C, check receive preamplifier output at the bottom of R25.	*e.* Waveform F.
	TRIG SOURCE:	LEFT		
4	TA-855/U		Verify VF receive amplifier function (Q2, Q3, and Q4) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	RANGE:	+10 dBm		
			a. On UUR, disconnect type G test cable from the right-hand LINE-UP (receive) jack and connect it to the RCV jack.	*a.* None.
			NOTE **The RCV control on the VF module has no mechanical stop and has reached its limit of adjustment when the meter ceases to change.**	
	UUR		*b.* Rotate RCV GAIN control on UUR to clockwise and counterclockwise limits adjustment while observing TA-855/U meter. Verify range of control is in accordance with normal indication.	*b.* At least -7 dbm to +12 dBm.
	RCV GAIN:	As required		
	UUR		*c.* Rotate RCV GAIN control on UUR as necessary to obtain normal indication on TA-855/U meter. If indication is correct, proceed to step 5.	*c.* +7 ±0.25 dBm.
	RCV GAIN:	As required		
			d. Check receiver amplifier input at the top of R23.	*d.* Waveform G.
	AN/USM-281C		*e.* Check Q3 output at top of R18.	*e.* Waveform H.
	VOLTS/DIV:	5V		
	AN/USM-281C		*f.* Check receive amplifier output at rear of C13 (junction with R16).	*f.* Waveform I.
	VOLTS/DIV:	2V		
5			Verify receive signaling function (Q7 and IC1) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	MXTF (BITE)			
	ON HOOK-			
	OFF HOOK:	OFF HOOK		
	AN/USM-281C			
	TIME/DIV:	0.5µs	*a.* Synchronize AN/USM-281C externally at pin 12A and observe signal at pin 13A.	*a.* Waveform J.
	AC/GND/DC:	DC		
	SOURCE:	EXT		
			b. Using AN/USM-223 measure voltage at CR9 to verify K2 relay coil is energized.	*b.* -1.5 0.5V.
	MXTF (RCVR)		*c.* Measure voltage at diode CR9 cathode while C.G.A. lamp on PWR SPLY is illuminated.	*c.* -40 ±2V.
	LOOP-NORMAL:	LOOP		
	LOOP-NORMAL:	NORMAL	*d.* Measure for continuity between UUR pins 15A and wiring point 22 (located above R24).	*d.* Continuity.
			e. Observe OFF HOOK lamp on BITE.	*e.* Lamp illuminated.



NOTE: 22 A-SIDE PIN POSITIONS AND 22 B-SIDE PIN POSITIONS ON EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

EL2XB122

Figure 3-21. VF module parts location diagram (sheet 1 of 3).



NOTE: 22 A-SIDE PIN POSITIONS AND 22 B-SIDE PIN POSITIONS ON EDGE CONNECTOR. B-SIDE FACING, A-SIDE OPPOSITE.

Figure 3-21. VF module parts location diagram (sheet 2 of 3).

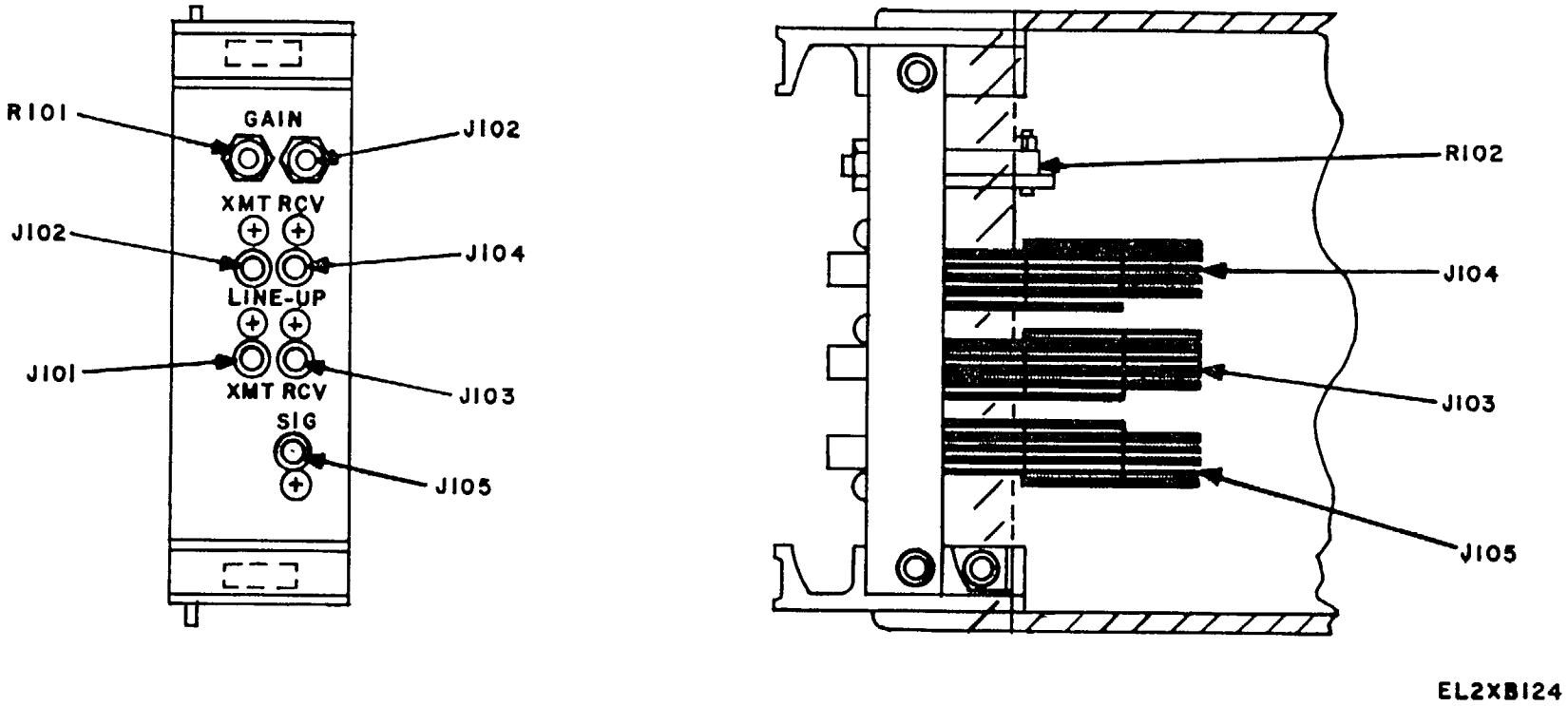


Figure 3-21. VF module parts location diagram (sheet 3 of 3).

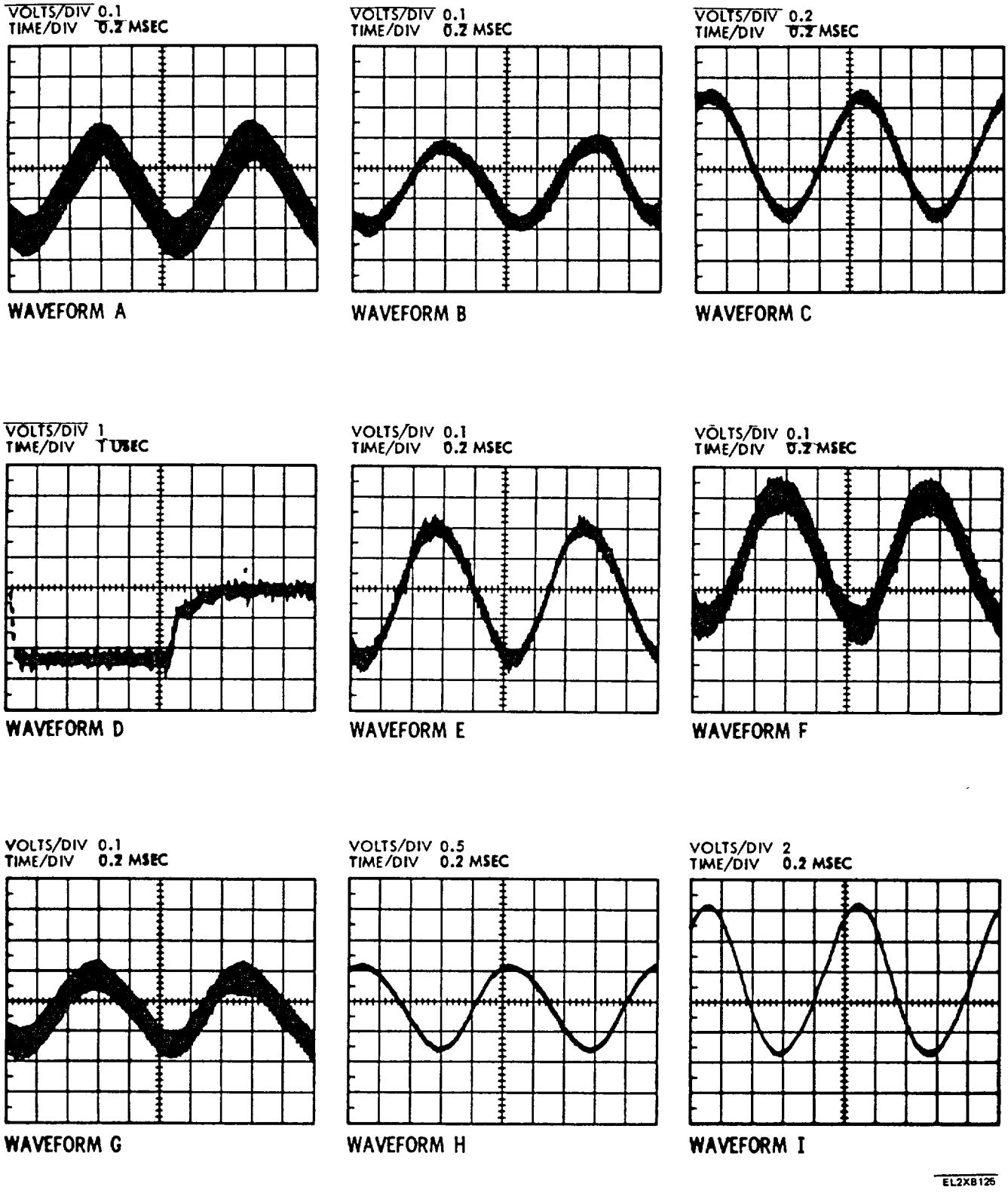


Figure 3-22. VF module troubleshooting waveforms (sheet 1 of 2).

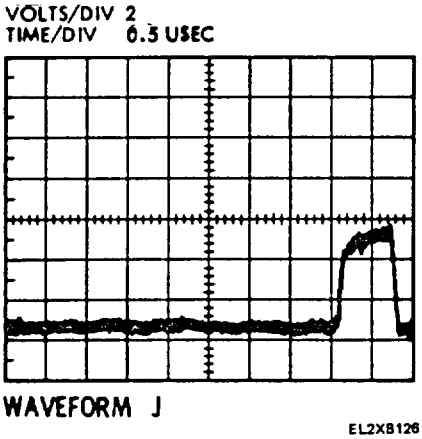


Figure 3-22. VF module troubleshooting waveforms (sheet 2 of 2).

3-15. Troubleshooting 0-20 Kb/s Data Module

Instructions and data for use in isolating faulty 0-20 kb/s data modules are provided in the following subparagraphs. Refer to figure FO-9 and to figure 3-24 for parts location.

a. Tools and Test Equipment.

(1) TK-100/G.

(2) AN/USM-281C.

(3) MXTF with the following accessories:
Extender board TRW 17080-010
Type A (bantam) test cable
Type B (turret) test cable
Type C test cables (2)
Type K test cable.

b. Initial Setup. Set up test equipment and faulty 0-20 kb/s data module as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.

(2) Using extender board, insert UUR into data channel 2 position of MXTF.

(3) Connect test equipment as shown in figure 3-23.

(4) Set equipment switches as follows:

Unit	*Switch*	*Setting*
AN/USM-281C	VOLTS/DIV (left)	2V
	TIME/DIV	50 µs
	AC/DC/GND	DC
	SOURCE	EXT
MXTF (BITE)	DIGITAL FUNC-TION	CLK RATE 20 Kb/S
(PWR CONT)	Power	ON

c. Fault Location. Troubleshoot in accordance with the following procedure to locate malfunctioning areas of the UUR.

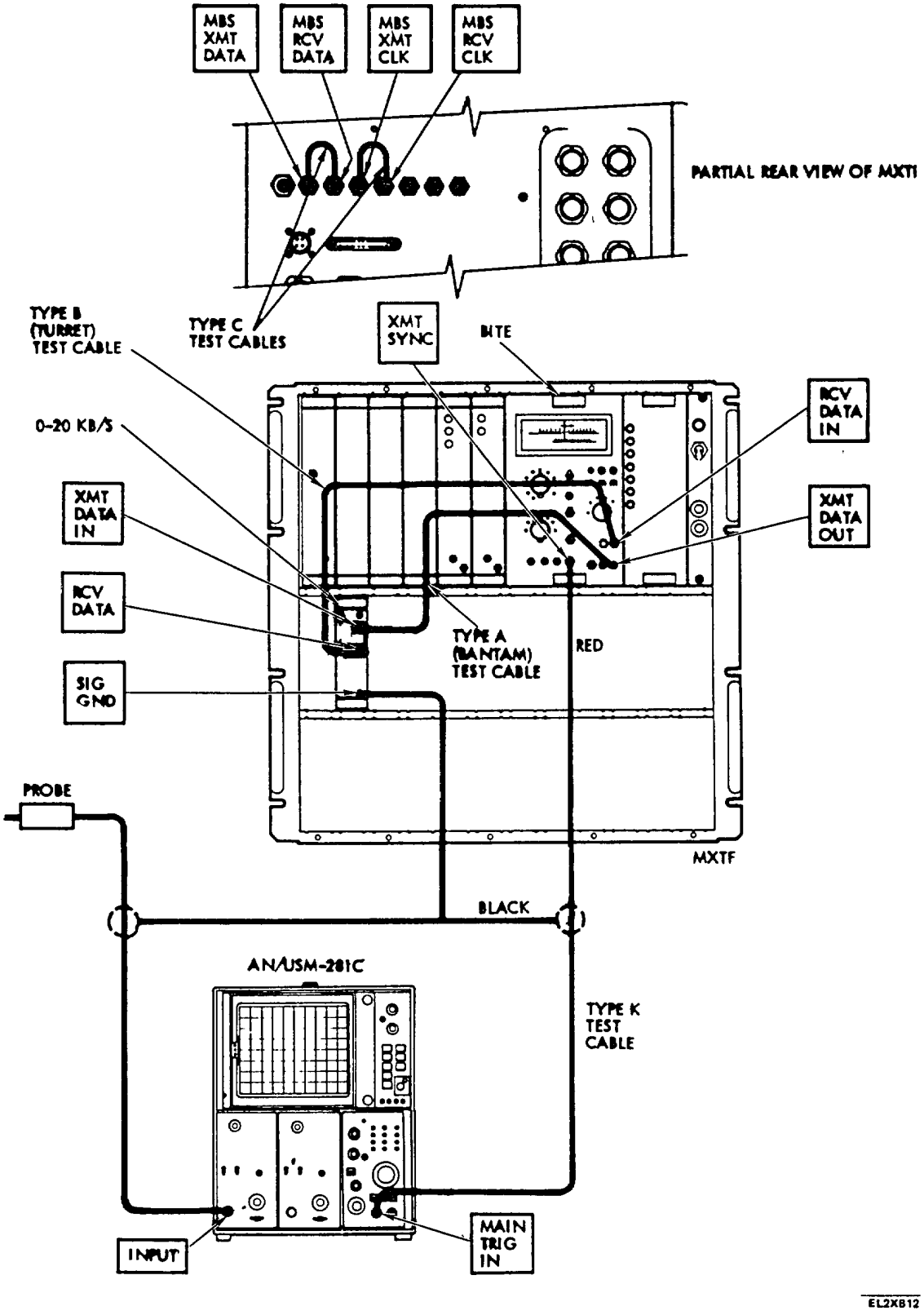
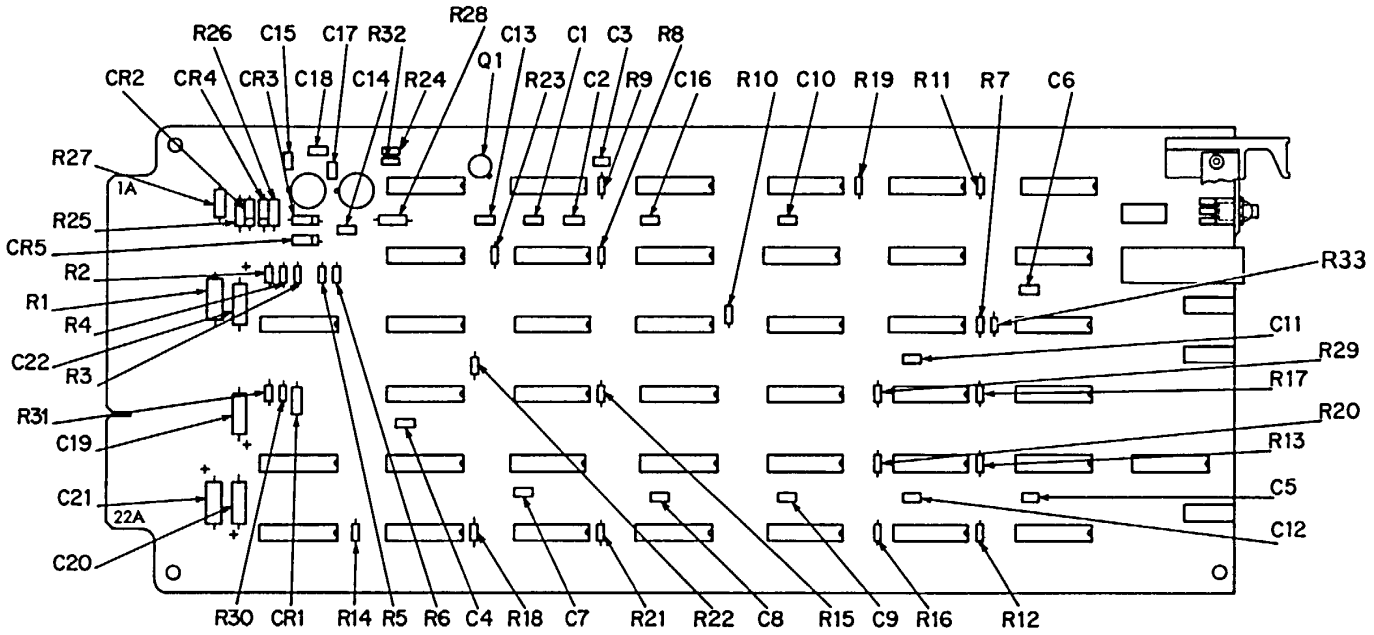


Figure 3-23. 0-20 kb/s data module troubleshooting setup diagram.

Step	Control	Setting	Trouble sectionalization check	Normal indication or fig 3-25
1			Verify receive data function (IC1, IC6, IC17, IC19, and IC42) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
			a. Check receive data outputs at pin 20A and pin 20B. If signals are correct, proceed to step 2 below.	*a.* Waveform A (pin 20A), waveform B (pin 20B).
	AN/USM-281C		*b*. Connect AN/USM-281C external	*b*. Waveform C.
	TIME/DIV:	.5 µs	trigger to pin 11A of UUR, and check ps eudo-random RCV DATS TO PIN 11A of UUR, and check pseudo-random RCV DATA input at 1C8-3.	
			c. Reconnect AN/USM-281C external trigger to XMT SYNC test point on BITE.	*c.* None.
	TIME/DIV:	.1 ms	*d*. Check parallel-to-serial register output at IC19-13.	*d.* Waveform D.
			e. Check signal at IC17-4.	*e.* Waveform D.
			f. Check signal at IC17-11.	*f.* Waveform E.
			g. Check signal at RCV DATA test point TP-2.	*g.* Waveform E.
			h. Check signal at IC42-11.	*h.* Waveform E.
	TIME/DIV:	5V	*i.* Check exclusive or-gate output at IC6-3.	*i.* Waveform F.
			j Check exclusive or-gate output at IC6-4.	*j* Waveform G.
2	AN/USM-281C		Verify receive MBS clock logic (IC8, IC13,	
	VOLTS/DIV:	2V	IC14, IC21) as follows. If any result is	
	TIME/DIV:	.5 µs	unsatisfactory, isolate and replace faulty	
	TRIG SOURCE:	LEFT	component.	
			a. Check RCV MBS CLK input at IC8-8.	*a.* Waveform H.
			b. Check serial-to-parallel converter load clock at IC21-1.	*b*. Waveform H.
			c. Check MBS CLK input to activity monitor at IC13-11.	*c*. Waveform H.
	AN/USM-281C		*d.* Connect AN/USM-281C external	*d.* Waveform I.
	TIME/DIV:	.5 µs	trigger at pin 9A and check RCV	
	SOURCE:	EXT	CONTROL BUS signal at IC14-3.	
3			Verify receive clock logic (IC3, IC13, IC19, IC21, IC23, IC26, IC28, IC34, IC38, and IC39) as follows. If any check is unsatisfactory, isolate and replace faulty component.	
			a. Check late CLK at IC34-3, IC19-7, IC28-6, and IC21-9.	*a.* Waveform J.
			b. Check early CLK at IC34-6 and IC 28-3.	*b*. Waveform K.
			c. Check late-plus-90-degree CLK at IC33-9, IC13-12, IC23-1, and IC26-11.	*c.* Waveform L.
	AN/USM-281C		*d*. Check CLK at IC33-6.	*d*. Waveform M.
	TRIG SOURCE:	LEFT		
	TIME/DIV:	2 µs	*e*. Check 224-KB/S CLK at IC39-11.	*e*. Waveform N.
	TIME/DIV:	.5 µs	*f.* Check 3.584-MHZ CLK at IC38-5.	*f.* Waveform O.

Step	Control	Setting	Trouble sectionalization check	Normal indication or fig. 3-25
4	AN/USM-281C SOURCE:	EXT	Connect AN/USM-281C external trigger to pin 11A, and check 4.096-MHZ CLK at IC3-2.	Waveform P.
5			Verify transmit data function (IC4, IC7, IC31, and IC36) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
			a. Connect AN/USM-281C external triger to pin 9A and check XMT DATA output at pin 10B. If signal is correct proceed to step 5 below.	*a*. Waveform Q.
			b. Connect AN/USM-281C external trigger XMT SYNC test point on BITE.	*b*. None.
	AN/USAI-281C TIM/DIV:	.2 ms	*c*. Check input signal at XMT DATA test point TP-1.	*c.* Waveform R.
			d. Check early and late clock sampling of incoming data at IC4-5 and IC4-9.	*d*. Waveform R.
			e. Check XMT DATA input to serial-to-parallel converter at IC7-6.	*e*. Waveform S.
			f. Check XMT DATA parallel output at IC36-3, IC26-4, IC36-5, IC36-6, IC 36-10, IC36-11, and IC36-12.	*f.* Waveform S.
6	AN/USM-281C TIME/DIV:	1 µs	Connect AN/USM-281C external trigger to pin 9A, and check parallel-to-serial converter output at IC31-7.	Waveform T.
7	AN/USM-281C TIME/DIV: TRIG SOURCE:	.5 µs LEFT	Verify transmit MBS clock logic (IC8, IC13, IC31, and IC32) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
			a. Check XMT MBS CLK to parallel-to-serial converters at IC31-2 and IC32-2.	*a.* Waveform H.
			b. Check XMT CLK input at IC8-10.	*b*. Waveform H.
			c. Check XMT MBS CLK input to activity monitor at IC13-3.	*c.* Waveform II.
8			Verify transmit clock logic (IC3, IC4, IC9, IC13, IC15, IC34, IC35, IC36, IC40, and IC41) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	AN/USM-281C SOURCE:	EXT	*a*. Connect AN/USM-281C external trigger to pin 11A CLK at IC35-8, IC4-11, IC15-3, and IC15-11.	*a.* Waveform U. and check late
	TIME/DIV:	5 µs	*b*. Check early CLK at IC35-9, IC34-9, IC36-8, IC4-3, IC9-3, and IC13-2.	*b*. Waveform L.
			c. Check CLK at IC35-5.	*c.* Waveform M.
	TIME/DIV:	2µs	*d*. Check 224-Kb/s CLK to IC41-11.	*d.* Waveform N.
	TIME/DIV:	.5 µs	*e*. Check 3.584-MHz CLK at IC40-5.	*e.* Waveform O.
9			Connect AN/USM-281C external trigger to pin 9A and check 4.096-MHz CLK at IC3-12.	Waveform P.



NOTE:
22 A-SIDE AND 22 B-SIDE PIN POSITIONS ON EDGE CONNECTOR.
A-SIDE FACING, B-SIDE OPPOSITE.

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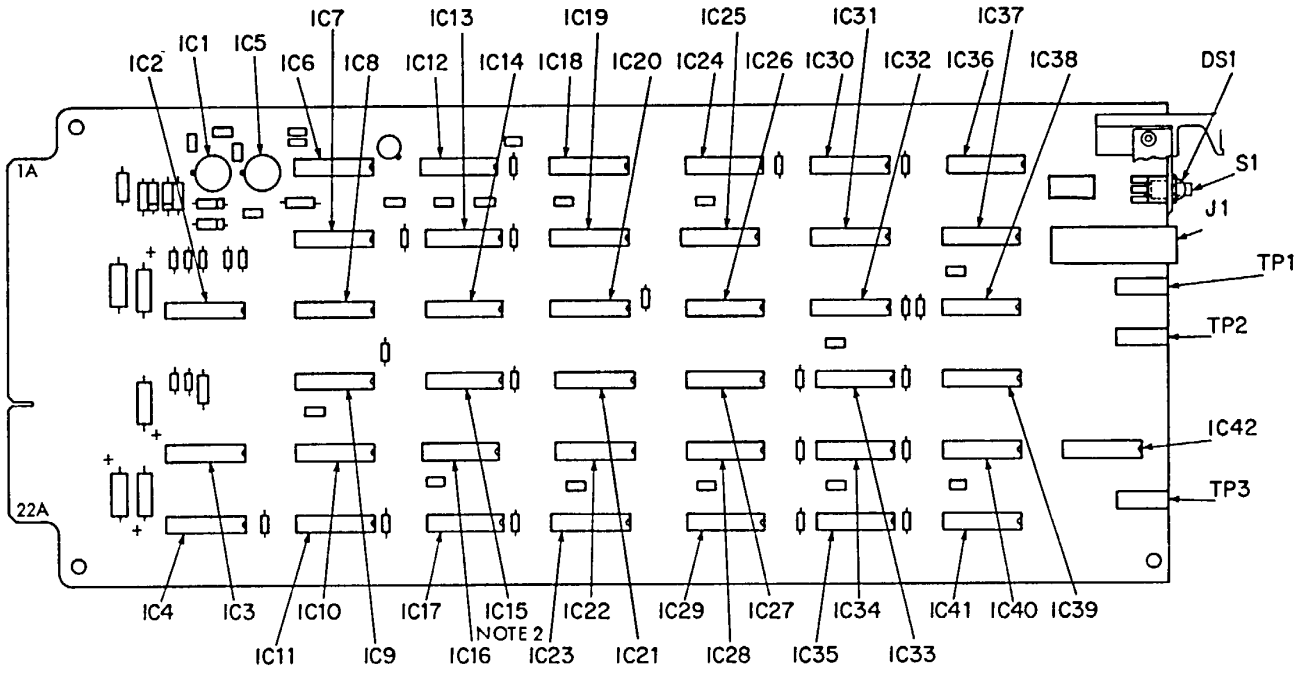
Figure 3-24. 0-20 kb/s data module parts location diagram (sheet 1 of 2).



NOTES:

1. 22 A-SIDE AND 22 B-SIDE PIN POSITIONS ON EDGE CONNECTOR. A-SIDE FACING, B-SIDE OPPOSITE.
2. USED IN CONFIGURATION 20K04 ONLY.

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Figure 3-24. 0-20 kb/s data module parts location diagram (sheet 2 of 2).

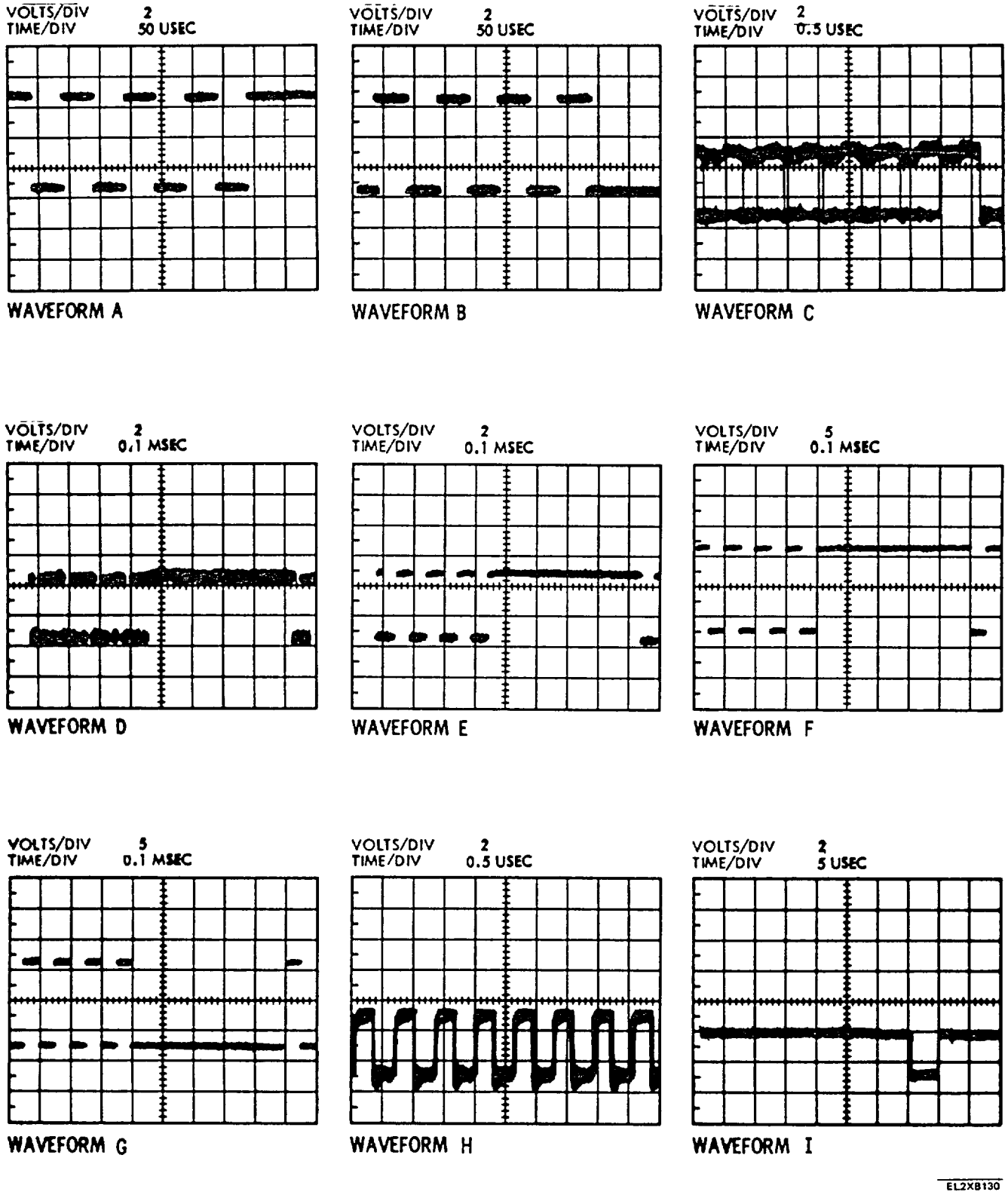


Figure 3-25. 0-20 kb/s data module troubleshooting waveforms (sheet 1 of 3).

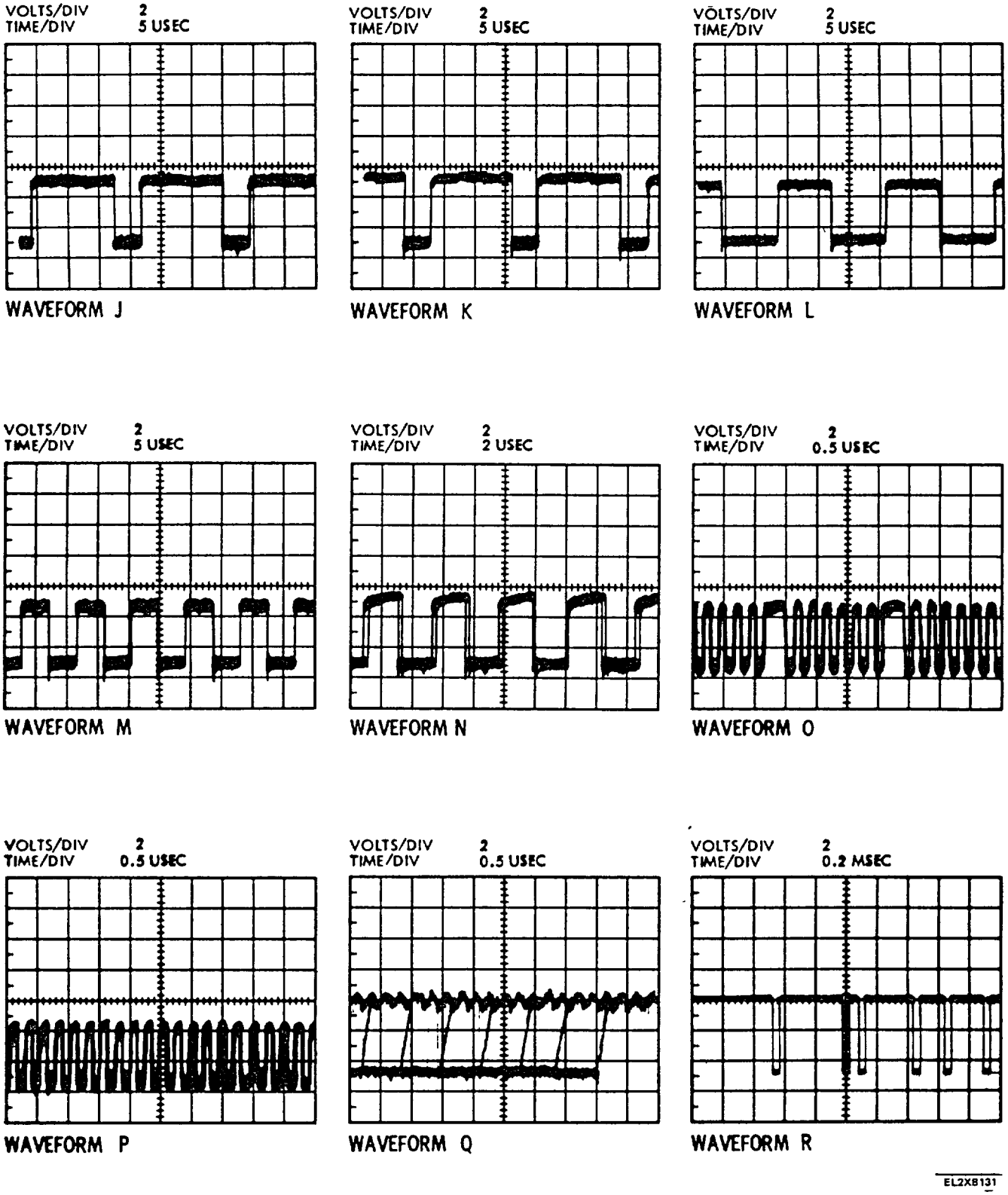


Figure 3-25. 0-20 kb/s data module troubleshooting waveforms (sheet 2 of 3).

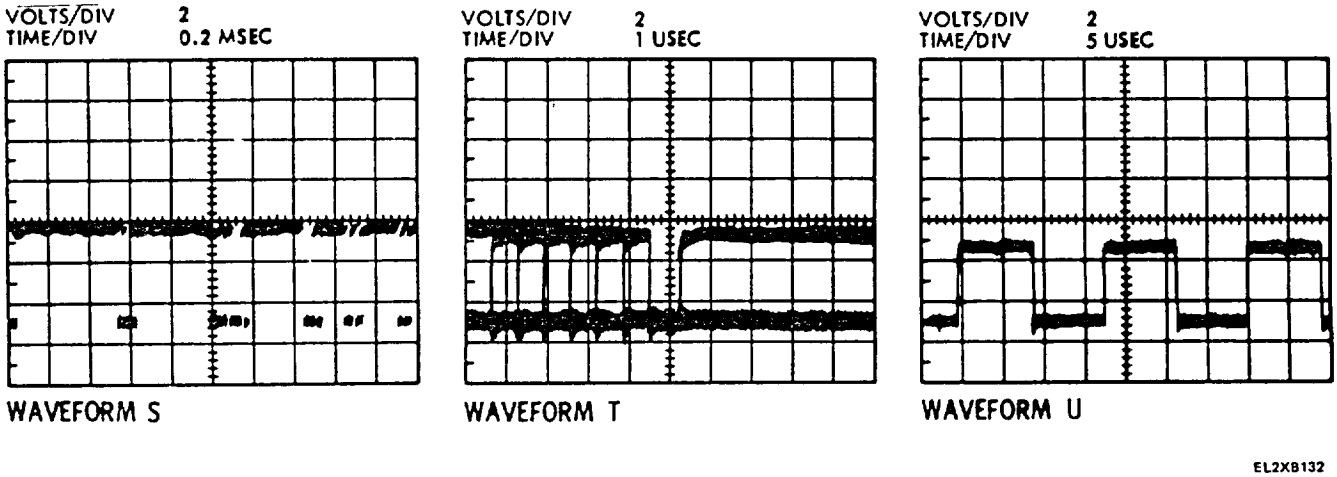


Figure 3-25. 0-20 kb/s data module troubleshooting waveforms (sheet 3 of 3).

3-16. Troubleshooting 50 Kb/S Data Module

The following instructions and data are for use in troubleshooting faulty 50 kb/s data modules. Refer to figure FO-10 and to figure 3-27 for parts location.

a. Tools and Test Equipment.

(1) TK-100/G.
(2) AN/USM-281C.
(3) Checktran.
(4) MXTF with the following accessories:
Extender board TRW 17080-010
Type C test cables (2)
Type L test cable.

b. Initial Equipment Setup. Set up test equipment and faulty 50 kb/s data module as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.

(2) Strap UUR for 78-ohm balanced interface by closing all contacts of S1 and opening all contacts of S2.

(3) Using extender board, insert UUR into channel 13 position of MXTF.

(4) Connect test equipment as shown in figure 3-26.

(5) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
AN/USM-281C	TIME/DIV	10 μS
	VOLTS/DIV (left)	1V
	AC/GND/DC	DC
	POWER	Pull
	TRIG	RIGHT
Checktran	DATA RATE	3754
	DATA BITS	8
	STOP UNIT	2
	SYNC	AUTO in
	PATTERN	1-0
	ERROR COUNT	in
	EXT CLK	out
	POWER	ON
MXTF (RCVR)	LOOP-NORMAL	NORMAL
(PWR CONT)	Power	ON

NOTE
Allow equipment to warm up for 5 minutes before proceeding.

c. Fault Location. Troubleshoot in accordance with the following procedure to locate malfunctioning areas of the UUR.

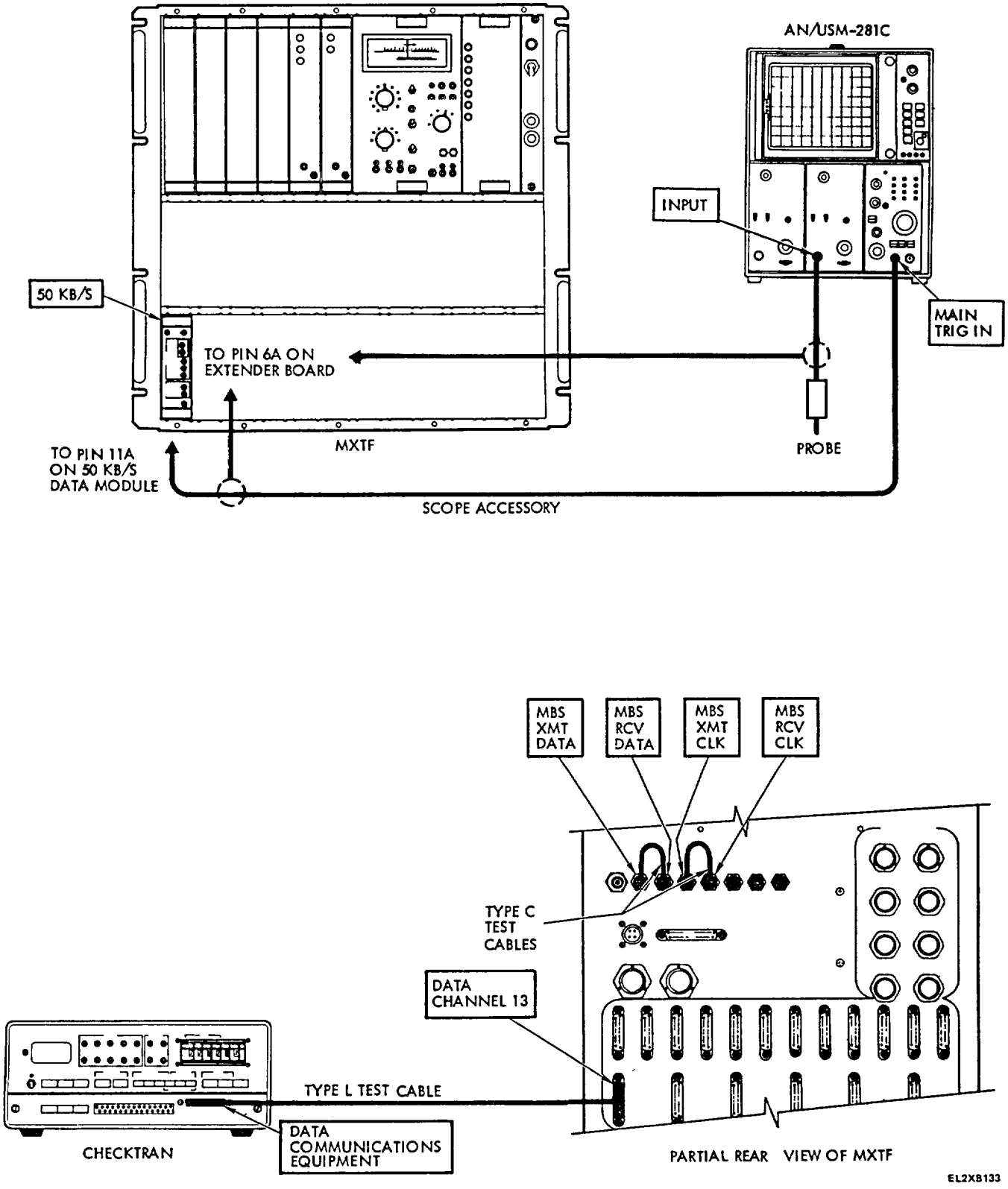
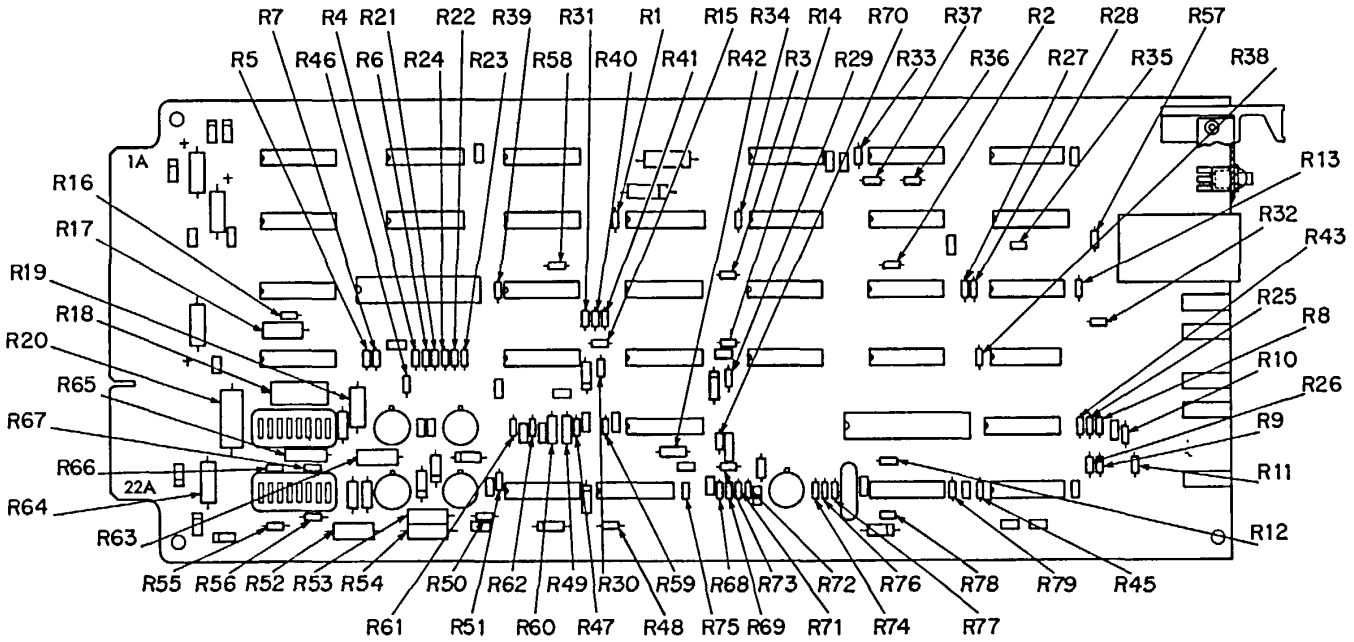


Figure 3-26. 50 kb/s data module troubleshooting setup diagram.

Step	Control	Setting	Trouble sectionalization check	Normal indication or fig 3-28
1			Verify receive data functions (IC4, IC7, IC16, IC20, and IC29) as follows: If any result is unsatisfactory, isolate and repair faulty component.	
			a. Check RCV DATA outputs at pins 20A and 20B. If signals are correct, proceed to step 2.	*a*. Waveform A.
	AN/USM-281C		*b*. Check RCV DATA input at IC4-6.	*b*. Waveform B.
	VOLTS/DIV:	2	*c*. Check FIFO output at IC7-21.	*c*. Waveform C.
	TIME/DIV:	.5 µs	*d*. Check signal at RCV DATA test point TP-6.	*d*. Waveform C.
	SOURCE:	EXT		
			e. Check signal at IC4-8.	*e*. Waveform C.
	TIME/DIV:	10 µs	*f*. Check signal at IC20-1.	*f*. Waveform D.
	TRIG SOURCE:	RIGHT	*g*. Check signal at IC4-8.	*g*. Waveform C.
			h. Check signal at IC20-1.	*h*. Waveform D.
			i. Check exclusive or gate outputs at IC16-4 and IC16-3.	*i*. Waveform E.
2			Verify receive clock input logic function (IC5 and IC12) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	AN/USM-281C		*a*. Check RCV CLK outputs at pins 17A and 17B. If signals are correct, proceed to step 3.	*a*. Waveform F.
	VOLTS/DIV:	1V		
	TIME/DIV:	5 µs		
	VOLTS/DIV:	2V	*b*. Check RCV CLK at IC12-1 and IC12-13.	*b*. Waveform G.
	VOLTS/DIV:	5 µs		
	TIME/DIV:	2 ms	*c*. Check FRAME 1 output at IC5-5.	*c*. Waveform H.
3			Verify receive write clock logic (IC20, IC27, and IC33) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
			a. Check .-16 counter output at IC34-12.	*a*. Waveform I.
	AN/USM-281C		*b*. Connect AN/USM-281C external trigger at pin 11A and check CLK signal at IC33-3.	*b*. Waveform J.
	TIME/DIV:	20 µs		
	SOURCE:	EXT		
			c. Check RCV WRITE CLK signal at IC33-8.	*c*. Waveform J.
	TRIG SOURCE:	RIGHT	*d*. Synchronize AN/USM-281C internally.	*d*. None.
	TIME/DIV:	.5 µs	*e*. Check signal at RCV WRITE CLK test point TP-5.	*e*. Waveform K.
	TIME/DIV:	.1 ms	*f*. Check oscillator control signal at IC20-7.	*f*. Waveform L.
4			Connect AN/USM-281C external trigger to pin 11A, and verify receive 4.096 MB/S CLK logic (IC16, IC20, IC23, IC32, IC36, and IC38) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	AN/USM-281C		*a*. Check signal at IC38-6.	*a*. Waveform O.
	TIME/DIV:	5 µs		
	SOURCE:	EXT		
	TRIG SOURCE:	RIGHT	*b*. Check CLK signal at IC36-3. If indication is satisfactory, proceed to substep g below.	*b*. Waveform O.

Step	Control	Setting	Trouble sectionalization check	Normal indication or fig. 3-28
	TIME/DIV:	50 µs	*c.* Check oscillator output at IC32-3. (Slight side to side movement of waveform is normal.)	*c*. Waveform M.
			d. Check oscillator clock at IC32-12 and IC32-9 (slight side to side movement of waveform is normal).	*d*. Waveform N.
	TIME/DIV:	2 µs	*e*. Check CLK signal at IC36-2.	*e*. Waveform P.
	TIME/DIV:	5 µs	*f.* Check signal at RCV CLK test point TP-7.	*f.* Waveform Q.
			g. Check CLK signal at IC20-14.	*g*. Waveform R.
			h. Check exclusive or gate CLK signal outputs at IC16-10 and IC16-11.	*h*. Waveform S.
5			Verify transmit data channel logic (IC15, IC18, IC25, and IC31) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	TIME/DIV:	1 µs	*a.* Check XMT DATA at pin 10B. If signal is correct, proceed to step 4.	*a*. Waveform T.
	TIME/DIV:	20 µs	*b*. Check incoming signal at XMT DATA test point TP-3.	*b*. Waveform U.
	TIME/DIV:	1 µs	*c.* Check FIFO DATA output at IC31-19.	*c*. Waveform V.
			d. Check data signal at IC18-5.	*d*. Waveform W.
			e. Check data signal at IC25-6.	*e*. Waveform X.
6			Verify transmit clock logic (IC2, IC4, IC6, IC13, IC15, IC17, IC18, IC25, IC29, IC30, IC31, and IC35) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	AN/USM-281		*a*. Check signal input at XMT CLK test point TP-1.	*a*. Waveform Y.
	TIME/DIV:	10 µs		
	TIME/DIV:	5 µs	*b*. Check FIFO LOAD CLK at IC31-2.	*b*. Waveform Z.
	TIME/DIV:	.5 µs	*c*. Check XMT MBS CLK input at IC2-4.	*c*. Waveform G.
			d. Check gated CLK signal at IC-13-13.	*d*. Waveform AA.
			e. Check CLK signal at IC35-6.	*e*. Waveform AB.
			f. Check XMT READ CLK at TP-4.	*f.* Waveform AC.
	TIME/DIV:	20 µs	*g*. Check CLK signal at IC17-9.	*g*. Waveform AD.
	TIME/DIV:	.2 ms	*h*. Check FRAME 1 signal at IC6-5.	*h*. Waveform H.
	TIME/DIV:	.5 ms	*i.* Check STUFF CONTROL signal at IC30-6.	*i.* Waveform AE. (some flicker is normal).
	TIME/DIV:	50µs	*j.* Check exclusive or gate output at IC29-11.	*j.* Waveform AF.



NOTE:
22A-SIDE AND 22B-SIDE PIN POSITIONS ON EDGE CONNECTOR. A-SIDE FACING, B-SIDE OPPOSITE.

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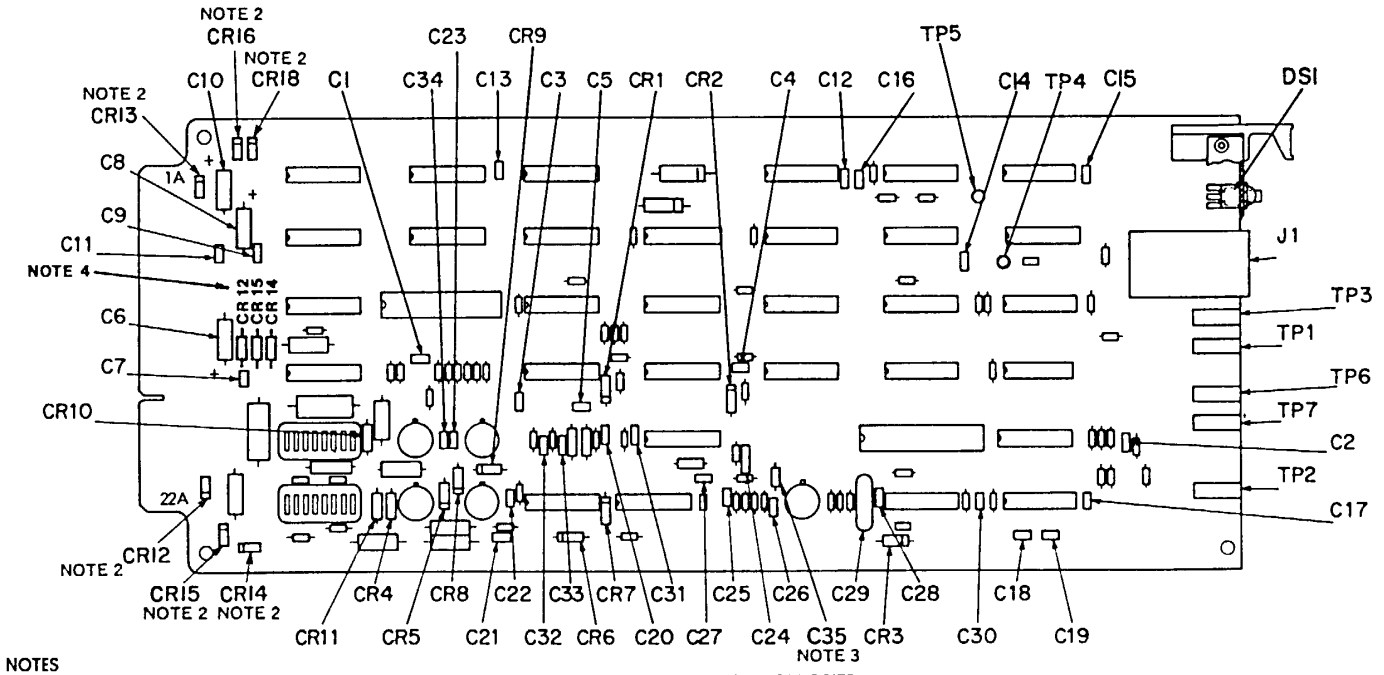
Figure 3-27. 50 kb/s data module parts location diagram (sheet 1 of 3).



NOTES
1. 22A-SIDE AND 22B-SIDE PIN POSITIONS ON EDGE CONNECTOR. A-SIDE FACING, B-SIDE OPPOSITE.
2. USED IN CONFIGURATIONS 50K04 AND 50K06 ONLY.
3. USED IN CONFIGURATION 50K06 ONLY.
4. LOCATION OF CR12, CR14, AND CR15 USED IN CONFIGURATION 50K08 ONLY.

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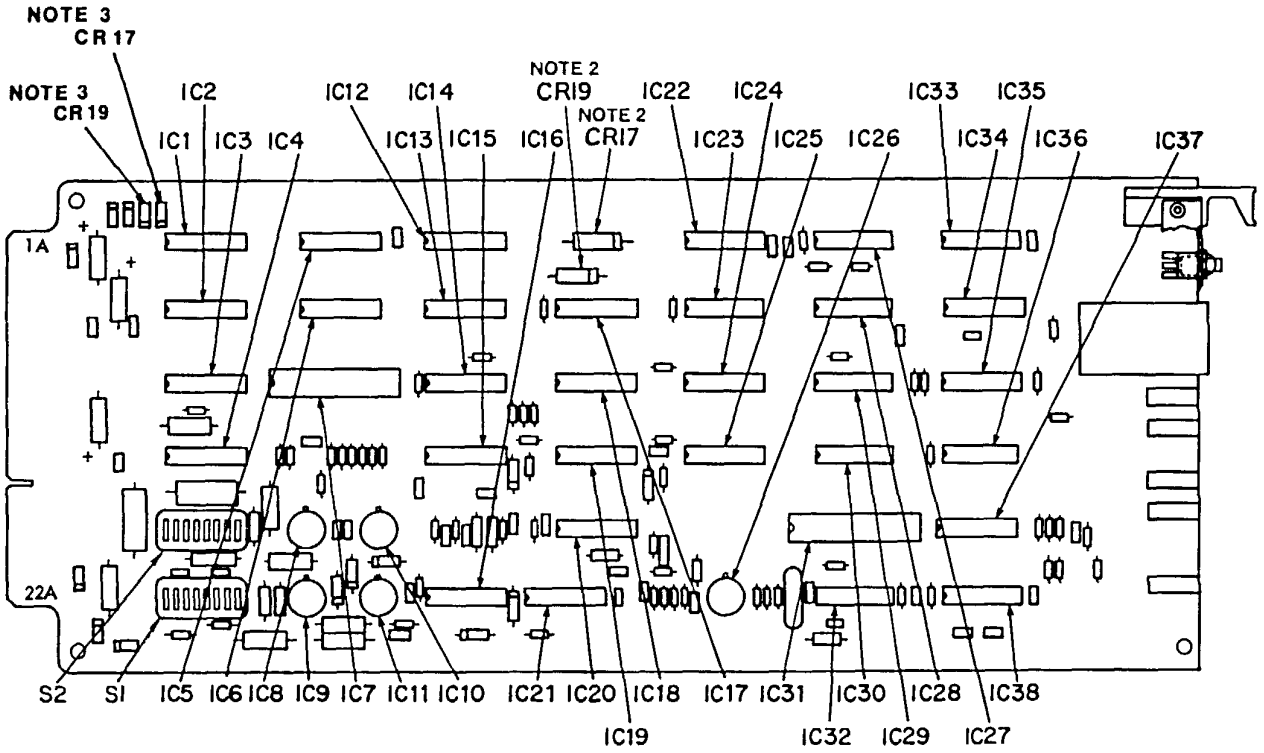
Figure 3-27. 50kb/s data module parts location diagram (sheet 2 of 3).



NOTES:
1. 22A-SIDE AND 22B-SIDE PIN POSITIONS ON EDGE CONNECTOR. A-SIDE FACING, B-SIDE OPPOSITE.
2 USED IN CONFIGURATIONS 50K04 AND 50K06 ONLY.
3. USED IN CONFIGURATION 50K08 ONLY.

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Figure 3-27. 50kb/s data module parts location diagram (sheet 3 of 3).

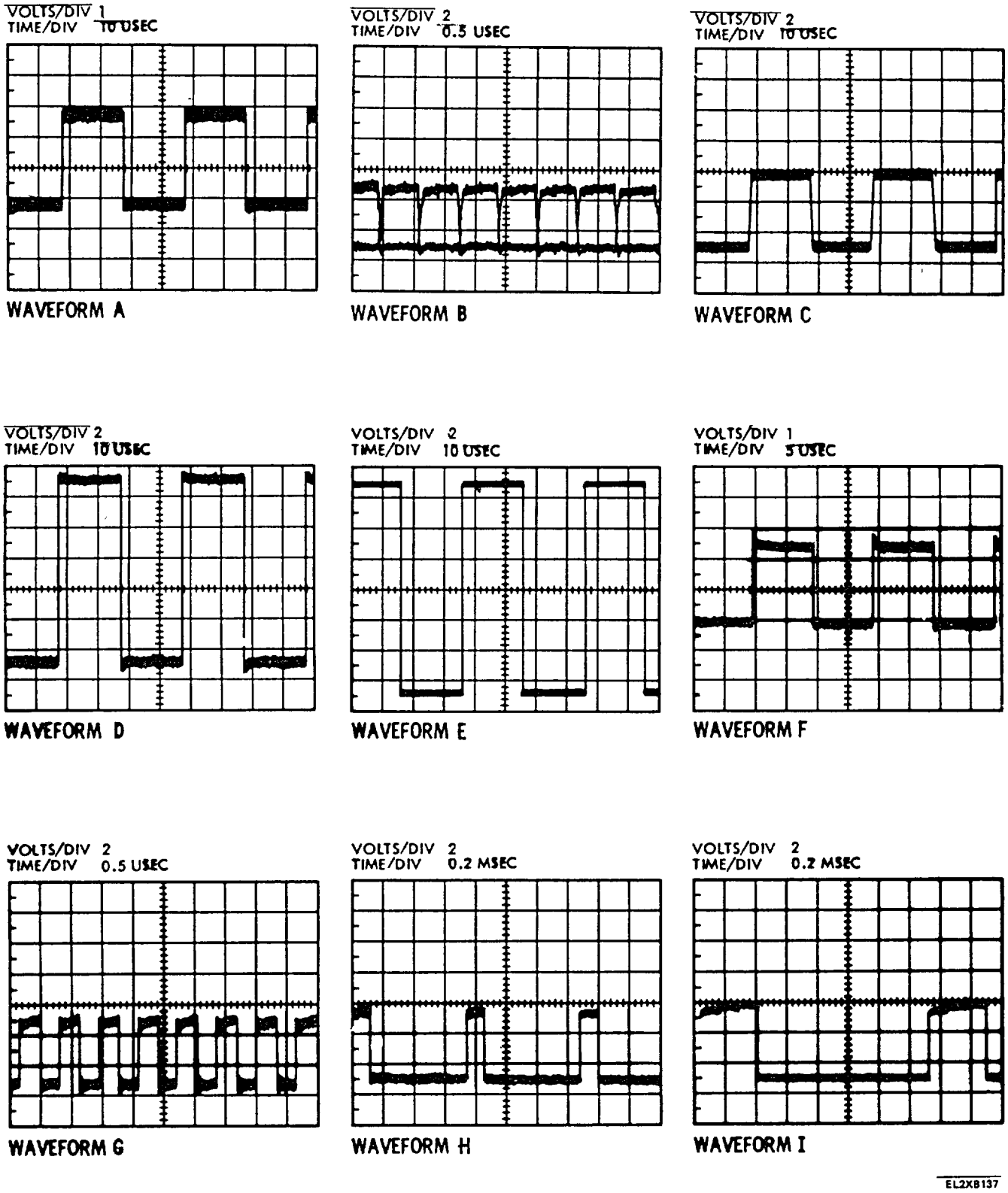


Figure 3-28. 50 kb/s module troubleshooting waveforms (sheet 1 of 4).

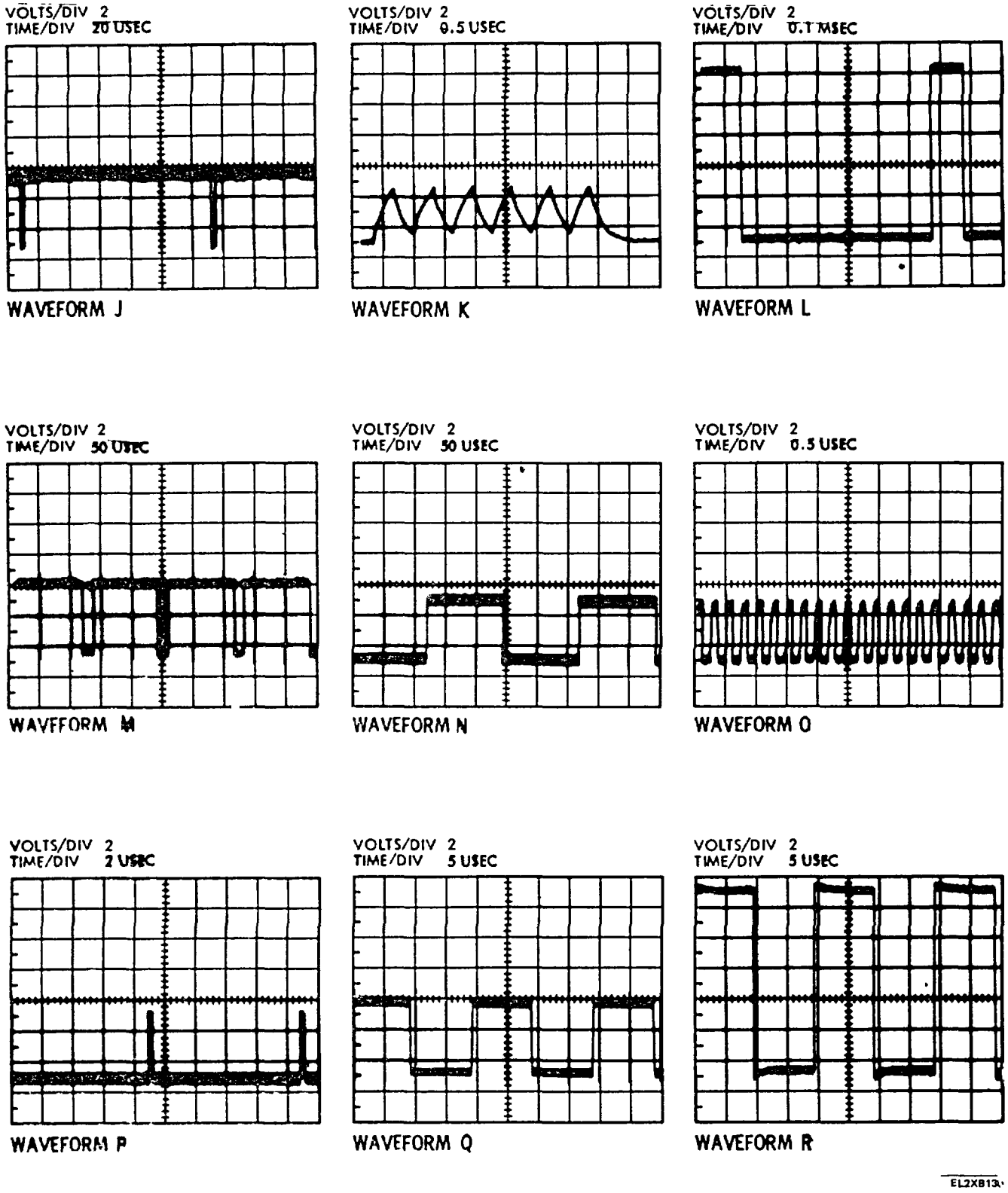


Figure 3-28. 50 kb/s module troubleshooting waveforms (sheet 2 of 4).

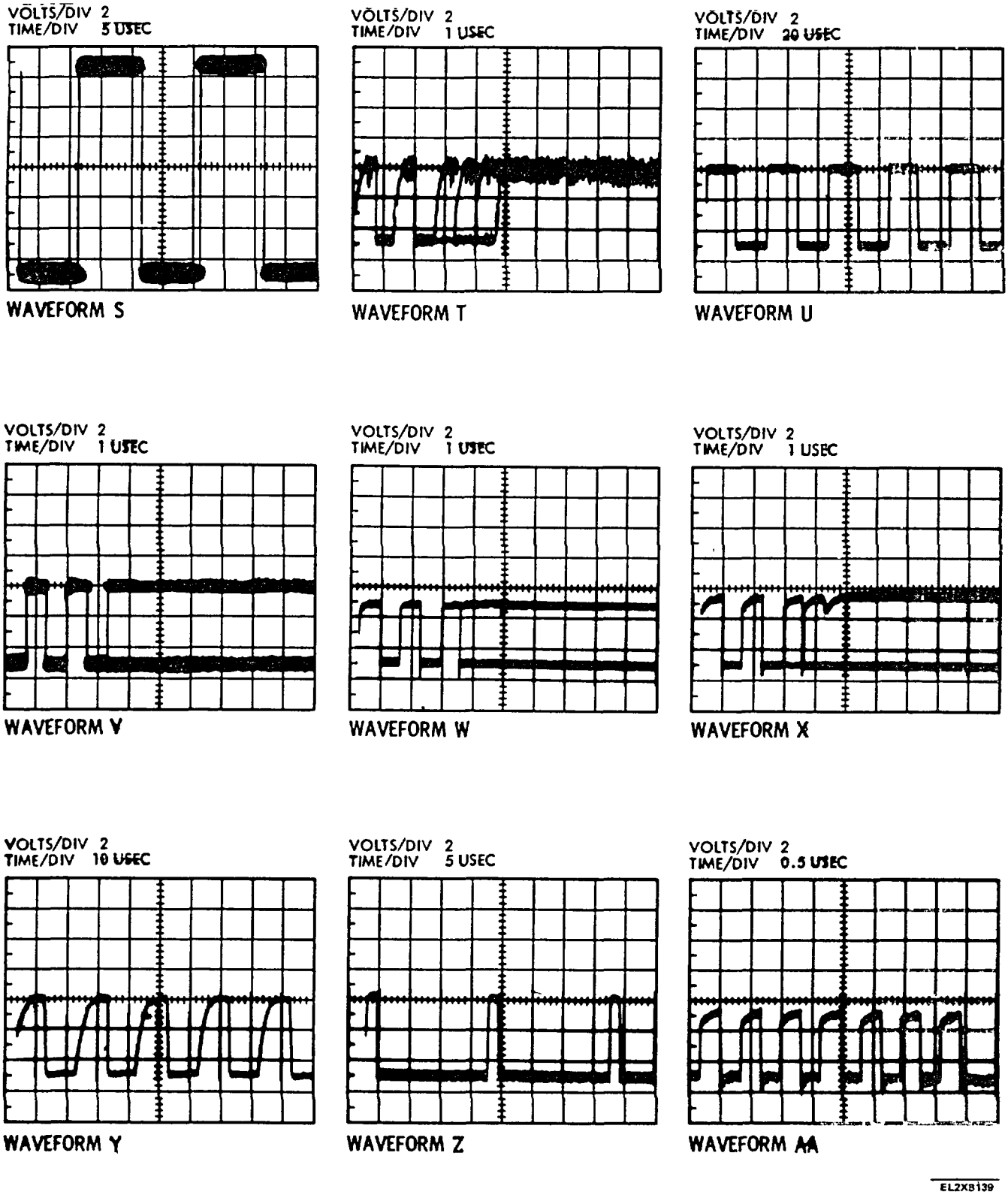


Figure 3-28. 50 kb/s module troubleshooting waveforms (sheet 3 of 4).

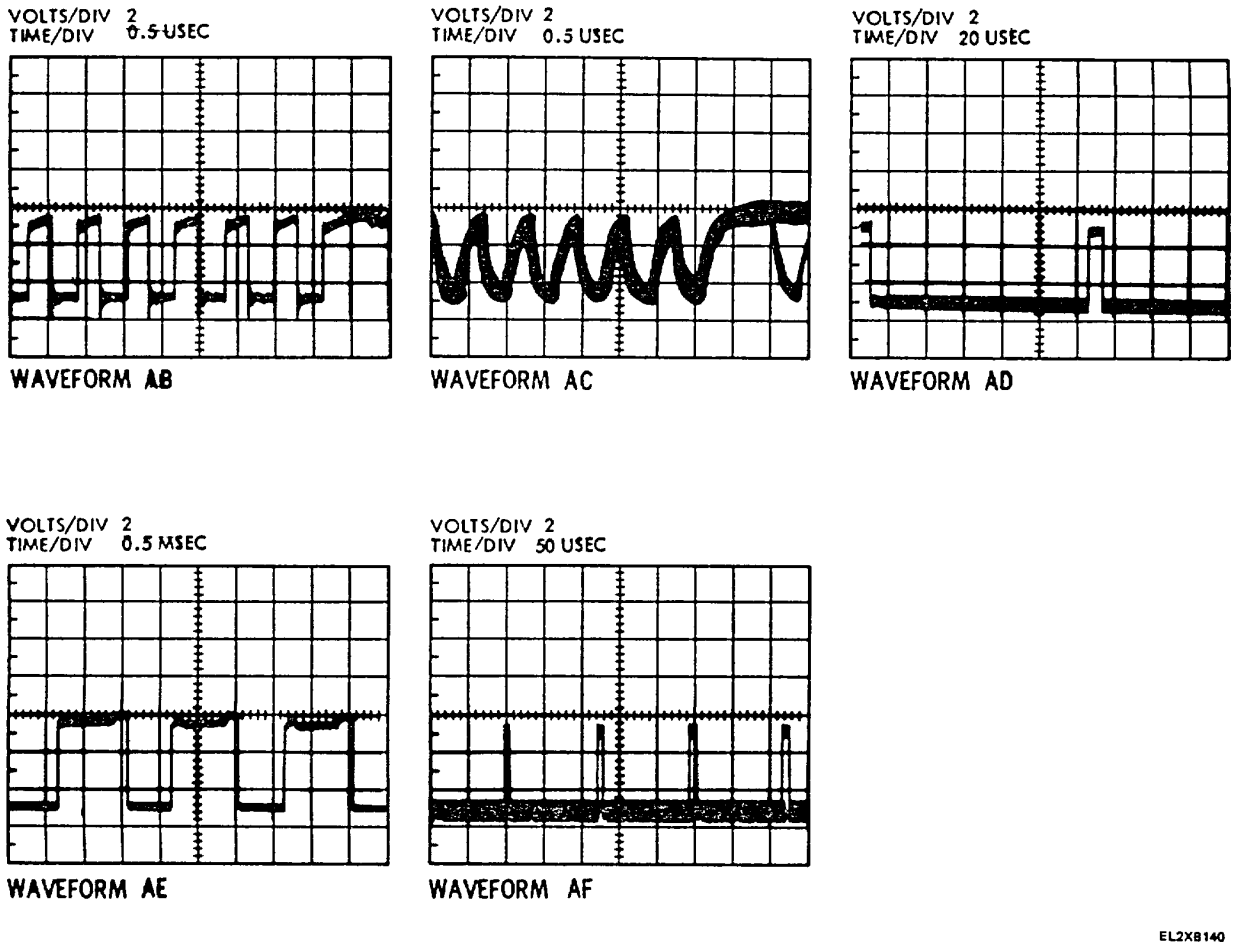


Figure 3-28. 50 kb/s module troubleshooting waveforms (sheet 4 of 4).

3-17. Troubleshooting Multirate Data Module

Instructions and data for use in isolating malfunctions in faulty multirate data modules are provided in the following subparagraphs. Refer to figure FO-11 and to figure 3-30 for parts location.

a. Tools and Test Equipment.

(1) TK-100/G.
(2) AN/USM-281C with external sync cable.
(3) Checktran.
(4) MXTF with the following accessories:
Extender board TRW 17080-010
Type A (bantam) test cable
Type B (turret) test cable
Type C test cables (2)
Type L test cable.

b. Initial Equipment Setup. Set up test equipment and faulty multirate data module as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.

(2) Strap UUR for 512-kb/s adjacent channel internal clock operation by setting strapping switches in accordance with table 3-4.

(3) Using extender board, insert UUR in channel 13 position of MXTF.

(4) Connect test equipment as shown in (figure 3-29).

Unit	*Setting*	*Setting*
AN/USM-281C	TIME/DIV	2
	VOLTS/DIV (left)	2V
	AC/GND/DC	DC
	POWER	Pull
Checktran	DATA BITS	8
	DATA RATE	7767
	STOP UNIT	2
	SYNC AUTO	in
	PATTERN 1-0	in
	ERROR COUNT	in
	EXT CLK	in
	POWER	ON
MXTF (RCVR)	LOOP-NORMAL	NORMAL
(PWR CONT)	Power	ON

NOTE

Allow equipment to warm up for 5 minutes before proceeding.

c. Fault Location. Troubleshoot in accordance with the following procedure to locate malfunctioning areas of the UUR.

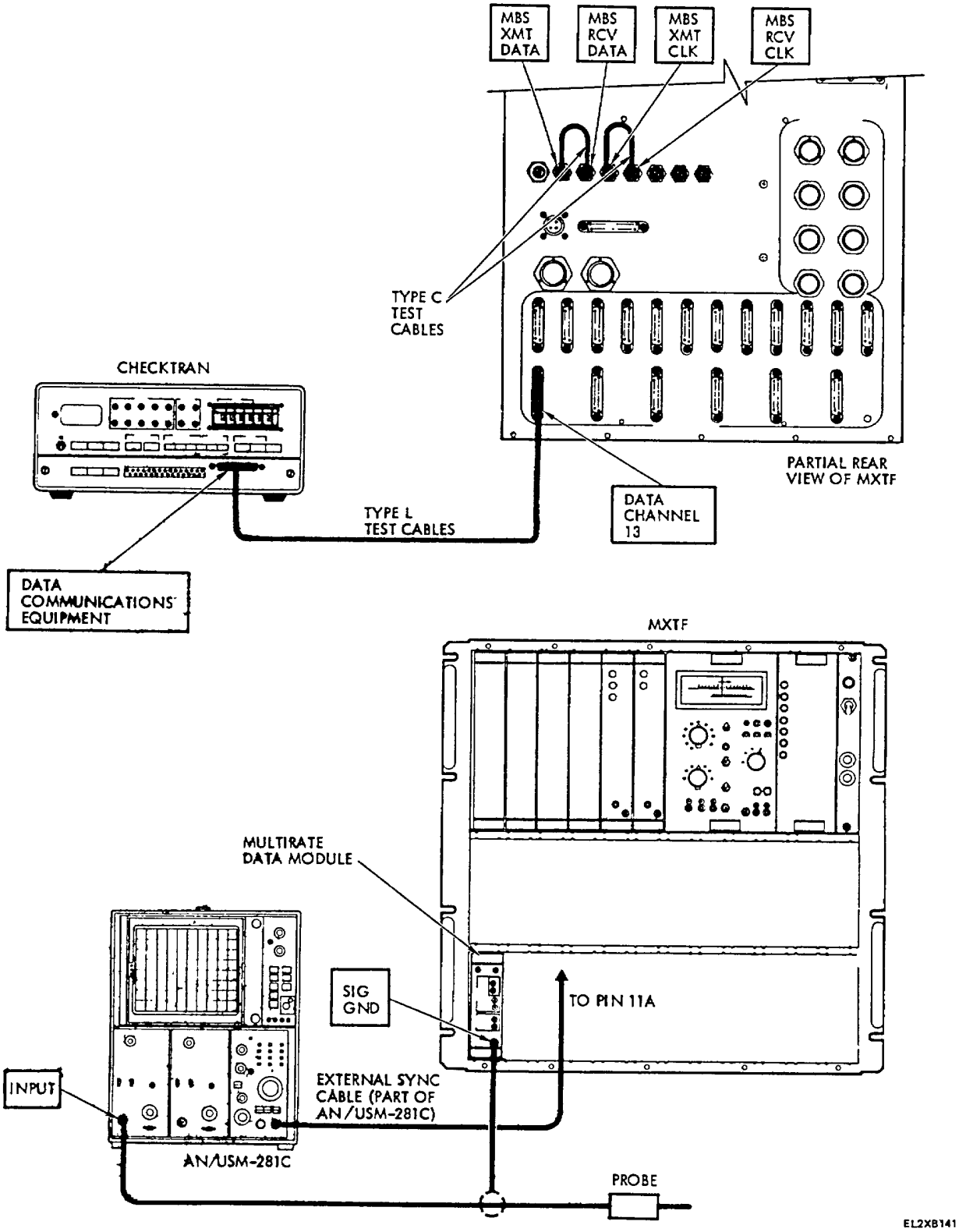


Figure 3-29. Multirate data module troubleshooting setup diagram.

Step	Control	Setting	Trouble sectionalization check	Normal indication or fig 3-31
1			Verify receive data channel (IC3, IC18, IC24, IC25, and IC33) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	AN/USM-281C		*a*. Check DATA signal outputs at pins	*a*. Waveform A.
	TRIG SOURCE:	LEFT	20A and 20B. If outputs are correct, proceed to step 2 below.	
	AN/USM-281C		*b*. Using external sync cable, connect	*b*. Waveform B.
	TIME/DIV:	1 µs	AN/USM-281C external trigger to	
	SOURCE:	EXT	pin 11A, and check DATA signal input at IC3-2.	
	AN/USM-281C		*c*. Check DATA signal FIFO at IC33-	*c*. Waveform C.
	TIME/DIV:	2 µs	22.	
	AN/USM-281C		*d*. Check DATA signal at RCV DATA	*d*. Waveform D.
	TIME/DIV:	1 µs	test point TP-4 and IC25-6.	
	AN/USM-281C		*e*. Check DATA signal at IC18-3 and	*e*. Waveform E.
	VOLTS/DIV:	5V	IC18-4.	
2			Verify receive clock logic (IC18, IC26, IC31, IC33, and IC46) at follows. If any result is unsatisfactory, isolate and replace faulty component.	
	AN/USM-281C		*a*. Check CLK signal outputs at pins	*a*. Waveform F.
	VOLTS/DIV:	1V	17A and 17B. If outputs are correct,	
	TRIG SOURCE:	LEFT	proceed to step 3 below.	
	VOLTS/DIV:	2V	*b*. Check CLK signal at RCV CLK test point TP-5. If CLK signal is correct, proceed to step 2g.	*b*. Waveform G.
	TIME/DIV:	.5 µs	*e*. Check rate multiplier output at IC26-5.	*e*. Waveform H.
	TIME/DIV:	1 µs	*d*. Check 7-bit counter output at IC31-9.	*d*. Waveform I.
			e. Check 2-to-1 multiplexer output at IC46-4.	*e*. Waveform I.
			f. Check FIFO CLK input at IC33-16.	*f*. Waveform J.
	VOLTS/DIV:	5V	*g*. Check exclusive or gate clock outputs at IC18-10 and IC18-11.	*g*. Waveform K.
3			Verify receive MBS speed control logic (IC3, IC13, IC25, IC32, and IC38) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	AN/USM-281C		*a*. Connect AN/USM-281C external	*a*. Waveform L.
	VOLTS/DIV:	2V	trigger to pin 11A, and check FIFO	
	TIME/DIV:	5 µs	LOAD CLK at IC25-8.	
	SOURCE:	EXT		
			b. Connect AN/USM-281C external	*b*. None.
	AN/USM-281C	trigger to pin 9A.		
	TIME/DIV:	20 µs	*c*. Check RCV CH CTR input at IC3-8.	*a*. Waveform M.
	TIME/DIV:	.5 µs	*d*. Check RCV MBS CLK at IC3-6.	*d*. Waveform L.
	TIME/DIV:	50 µs	*e*. Check control flip-flop output at IC13-6.	*e*. Waveform N.
			f. Check CLK signal at IC13-8, IC38-6, and IC32-6.	*f*. Waveform N.
4			Verify transmit data channel (IC14, IC29, and IC30) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
			a. Connect AN/USM-281C external trigger to pin 9A.	*a*. None.
	AN/USM-281C		*b*. Check XMT DATA output at pin	*b*. Waveform O.
	TIME/DIV:	2 µs	10B. If signal is correct, proceed to step 5 below.	

Step	Control	Setting	Trouble sectionalization check	Normal indication or fig 3-31
			c. Check signal at XMT DATA test point TP-1.	*c.* Waveform P.
	TIME/DIV:	1 µs	*d*. Check FIFO output at IC14-12.	*d.* Waveform Q.
5			Verify XMT CLK IN logic (IC43, IC46, and IC48) as follows. If any result is unsatisfactory, isolate and remove faulty component.	
			a. Check signal at XMT CLK IN test point TP-2. If signal is correct, proceed to step 6.	*a.* Waveform R.
	MXTF (BITE)		*b.* Connect cables between BITE	*and* b. None.
	DIGITAL	EXT CLK	UUR as follows:	
	FUNCTION:		**Test Cable**	
			Type BITE Jack UUR Jack	
			A (bantam) XMT CLK OUT CLK IN	
			B (turret) XMT CLK IN CLK OUT	
			c. Check EXT CLK input at IC48-1.	*c.* Waveform R.
			d. Disconnect cables between BITE and UUR.	*d.* None.
	CHECKTRAN		*e.* Check CLK signal at IC48-9.	*e.* Waveform G.
	RESET:	Press for test		
			f. Check 8-bit shift register output at IC43-8.	*f.* Waveform S.
	AN/USM-281C		*g.* Check 2-to-1 multiplexer output at	*g.* Waveform H.
	TIME/DIV:	.5 µs	IC46-9.	
6			Verify XMT CLK OUT function (IC16, IC27, IC42, and IC46) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	AN/USM-281C		*a*. Check XMT CLK outputs at pins	*a.* Waveform F.
	VOLTS/DIV:	1V	16A and 16B. If outputs are correct,	
	TIME/DIV:	1 µs	proceed to step 7 below.	
	TIME/DIV:	5V	*b*. Check exclusive or gate outputs at IC16-3 and IC16-4.	*b.* Waveform K.
	TIME/DIV:	2V	*c.* Check signal at XMT CLK OUT test point TP-3.	*c.* Waveform R.
	TIME/DIV:	.5 µs	*d*. Check rate multiplier output at IC27-5.	*d.* Waveform H.
	TIME/DIV:	1 µs	*e*. Check 7-bit counter output at IC42-9.	*e.* Waveform I.
7			Verify MBS transmit speed control functions (IC2, IC3, IC9, IC15, IC32, and IC38) at follows. If any result is unsatisfactory, isolate and replace faulty component.	
			a. Connect AN/USM-281C external trigger to pin 9A.	*a.* None.
	AN/USM-281C		*b*. Check FIFO output CLK at IC9-8.	*b.* Waveform L.
	TIME/DIV:	5 µs	If signal is incorrect proceed with step c below.	
			c. Check MBS CLK input at IC2-6.	*c.* Waveform L.
			d. Connect AN/USM-281C external trigger to pin 11A.	*d.* None.
	TIME/DIV:	50 µs	*e*. Check XMT CH CTR input at IC3-12.	*e.* Waveform T.
			f. Check control bus status at IC3-4.	*f.* Waveform N.
			g. Check CLK signal at IC15-6.	*g.* Waveform N.
			h. Check CLK signal at IC38-8.	*h.* Waveform N.
			i. Check CLK signal at IC32-3.	*i.* Waveform N.

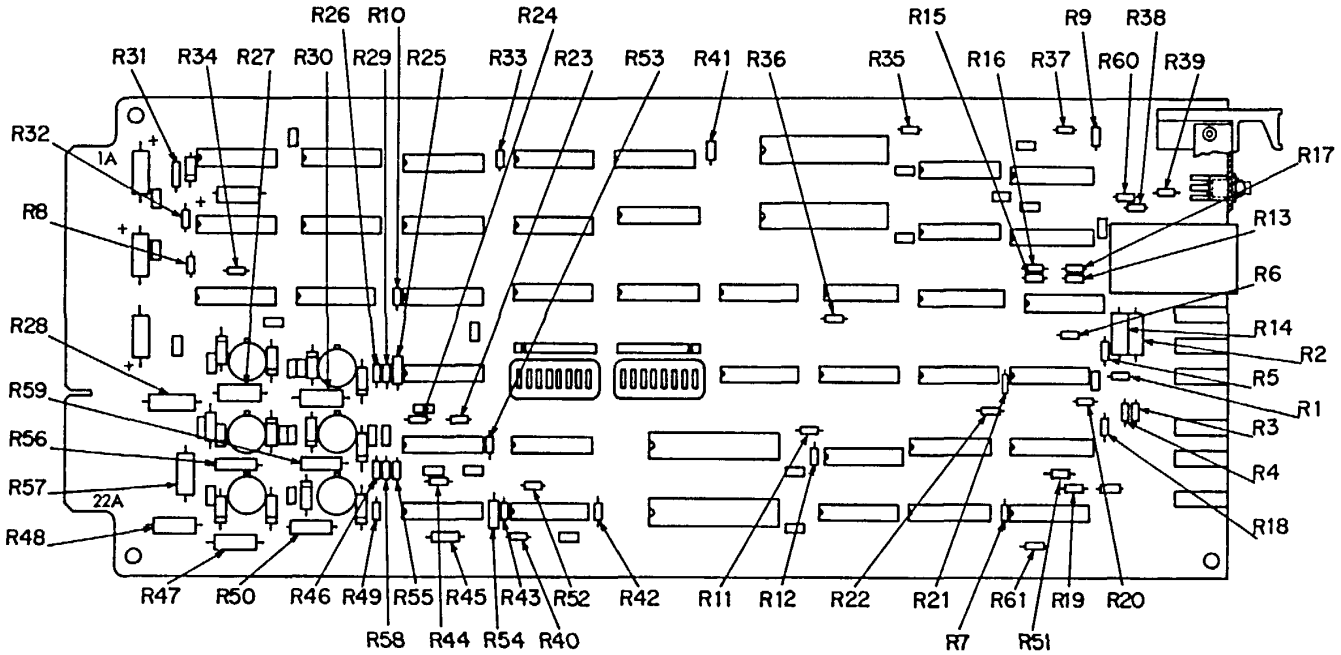


Figure 3-30. Multirate data module parts location diagram (sheet 1 of 3).

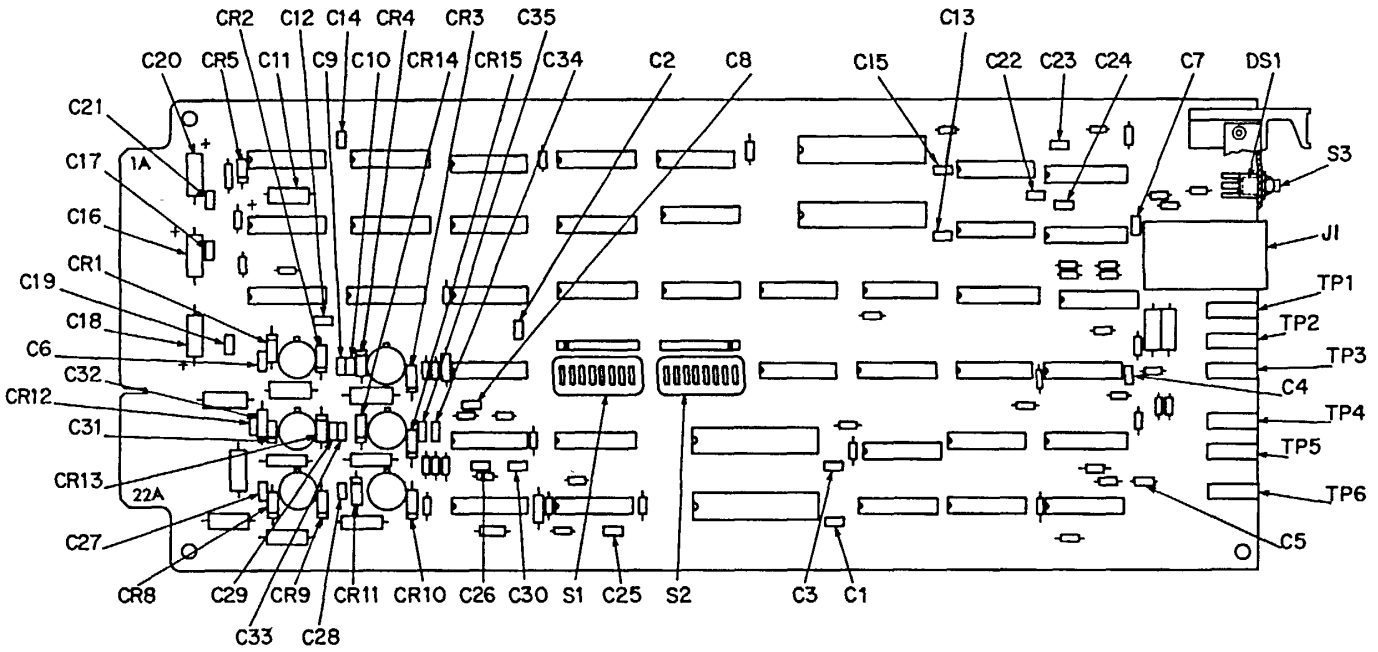


Figure 3-30. Multirate data module parts location diagram (sheet 2 of 3).

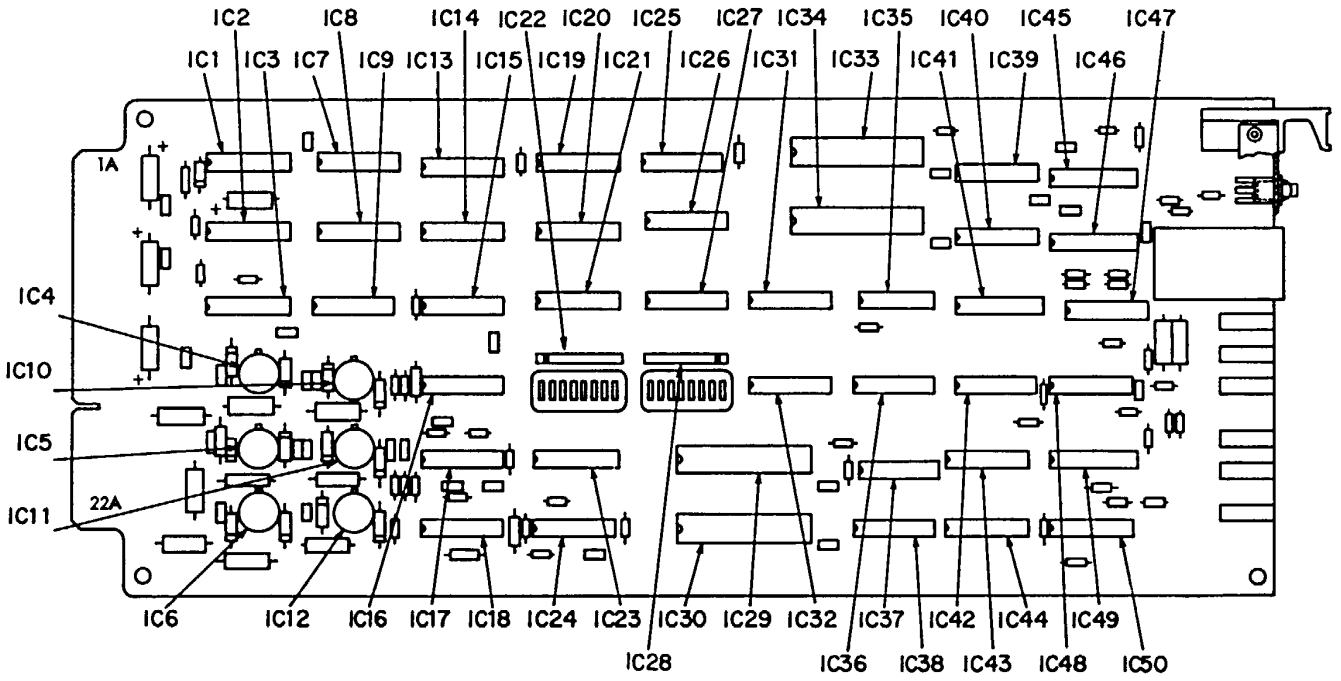


Figure 3-30. Multirate data module parts location diagram (sheet 3 of 3).

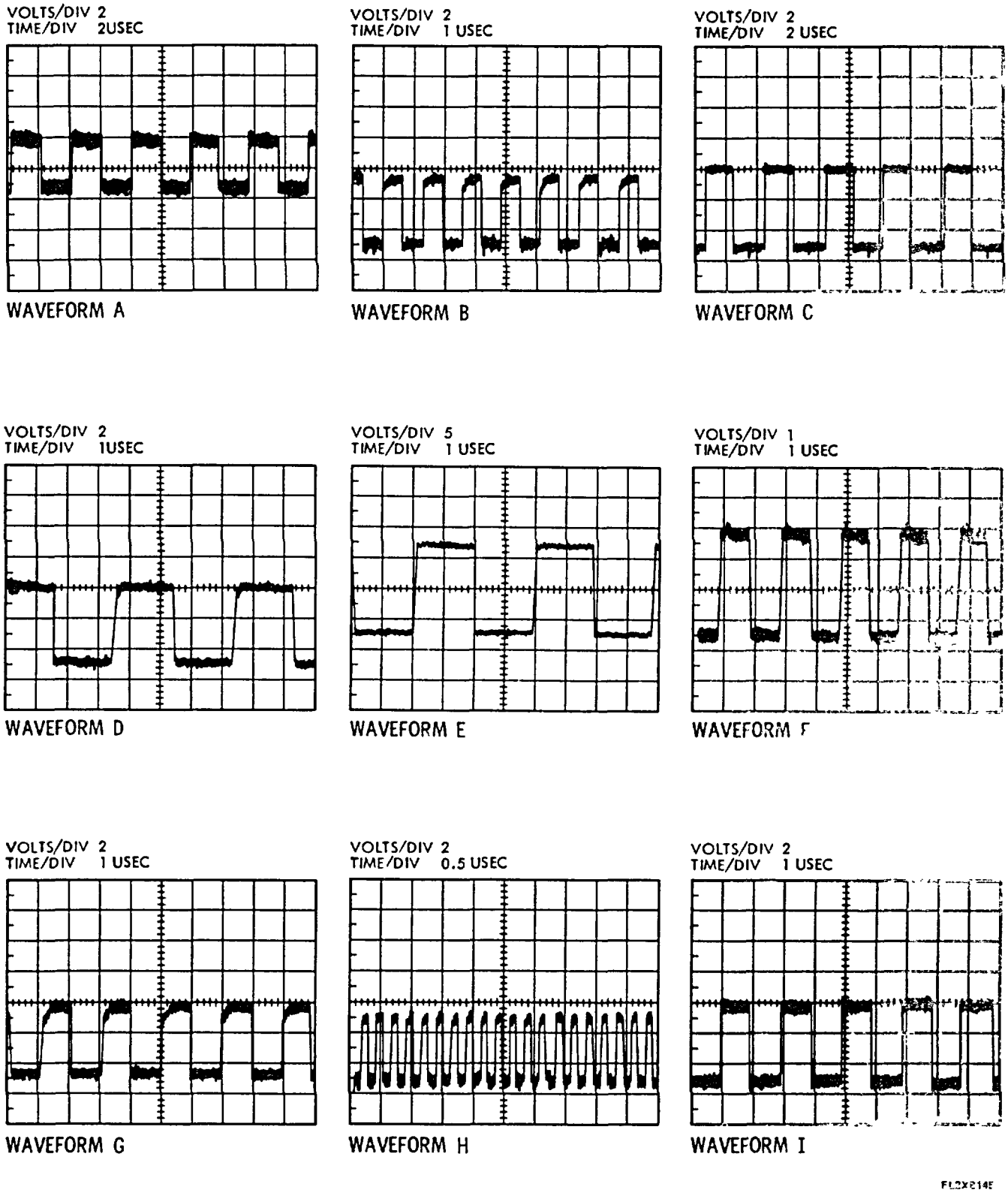


Figure 3-31. Multirate data module troubleshooting waveforms (sheet 1 of 3.).

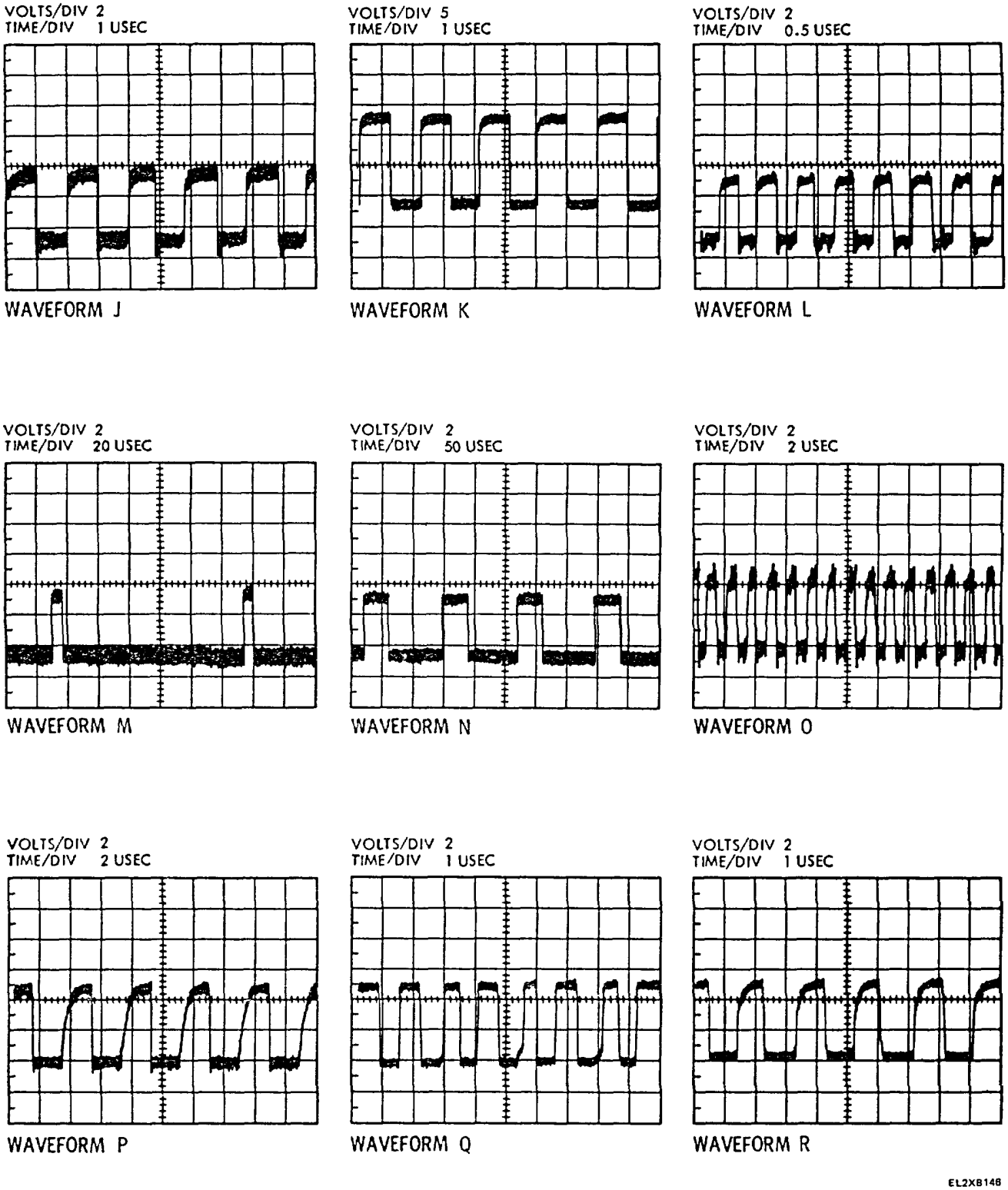


Figure 3-31. Multirate data module troubleshooting waveforms (sheet 2 of 3).

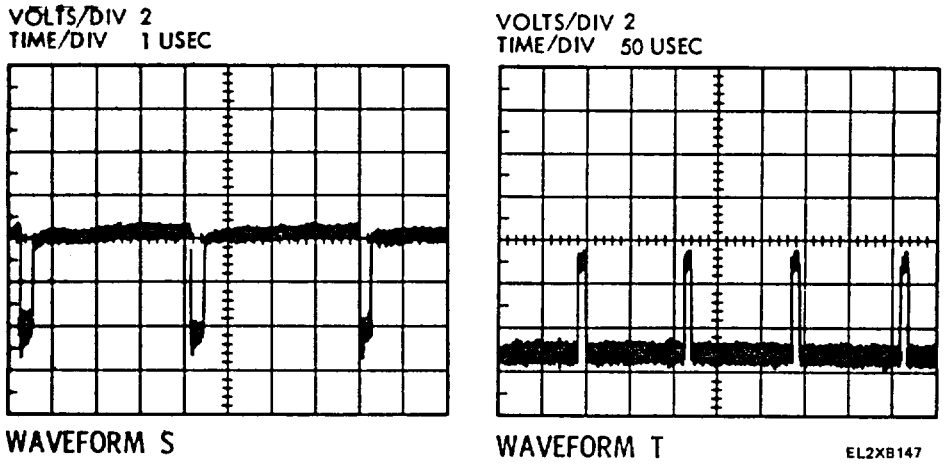


Figure 3-31. Multirate data module troubleshooting waveforms (sheet 3 of 3).

3-18. Troubleshooting BITE

The following instructions and data are for use in troubleshooting faulty BITE. Refer to figure FO-12 and figure 3-32 for parts location.

a. Tools and Test Equipment.

(1) TK-100/G.
(2) TA-855/U.
(3) AN/USM-281C.
(4) TS-3329/U.
(5) CP-772A/U.
(6) DMM.
(7) MXTF with the following accessories:
Extender board TRW 17191-010
Type A (bantam) test cables (2)
Type B (turret) test cables (3)
Type G test cable
Type J test cable.
Spare multirate data module.

b. Troubleshooting Preparation and Initial Equipment Setup. Prepare test equipment and faulty BITE module for troubleshooting as follows:

(1) Apply power to CP-772A/U by rotating SAMPLE RATE control 1/2 turn clockwise.

(2) Apply power to AN/USM-281C by pulling POWER switch to on position.

(3) Using extender board, replace BITE in MXTF with UUR.

(4) Set power switch PWR CONT unit in MXTF to ON.

c. Fault Location (Voltage Measurement Circuits). Troubleshoot in accordance with the following procedure to locate malfunctioning areas of BITE voltage measurement function.

Step	Control	Setting	Trouble sectionalization check	Normal indication or fig 3-33
			NOTE **The following checks verify the dc voltage measurement circuit (S201 and M201) of BITE. If any result is unsatisfactory, isolate and replace faulty component.**	

Step	Control	Setting	Trouble sectionalization check	Normal indication or fig 3-33
1	(*UUR*) DIGITAL FUNCTION:	 CLK RATE 20 kb/s	With DMM, measure and record exact dc input voltages of BITE analog board (left connector) between pin 15A (ground) and each listed pin. **NOTE** **These readings are used to verify accuracy of the UUR dc metering circuit, and should be within the voltage range indicated below.**	As listed below.
			Pin 14B 7B 6B 2A 9B 1A 2B 3B 8B 3A	 -52 ±6V -42 ±4V -38 ±2V -13 ±2V -13 ±2V -7 ±1V -5 ±0.7V +7 ±1V +13 ±2V +13 ±2V
2	(*UUR*) VF FUNCTION: DC SUPPLY SELECT:	 DCV as required	Rotate DC SUPPLY SELECT switch to each of its positions and compare indications on UUR meter with voltage recorded in step 1 above. Any difference between voltages should be within the recorded voltage tolerance listed below:	

Switch position	**Extender board connector pins**	**Recorded voltage tolerance**
-48V	**14B**	**±2.OV**
-42V	**7b**	**±2.OV**
-38V	**6B**	**±2.0V**
-12V PS2	**2A**	**±1.OV**
-12V PS1	**9B**	**±1.OV**
-7V	**1A**	**±0.7V**
-5V	**2B**	**±0.5V**
+7V	**SB**	**±0.7V**
+12V PS1	**8B**	**±1.OV**
+12V PS2	**3A**	**±1.OV**

If indication observed in step 2 above is None. correct, proceed to paragraph 3-18d.

d. Fault Location (VF Oscillator Circuits). Troubleshoot in accordance with the following procedure to locate faults in the BITE VF oscillator circuits.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-33
			NOTE **The following checks verify the VF oscillator functions (IC2, Q1, S202A, and S202B) of BITE. If any result is unsatisfactory, isolate and replace faulty component.**	
1	*UUR* DIGITAL FUNCTION: *TA-855/U* RESPONSE: NOISE WTG: INPUT: RANGE: VF/Nm:	 POWER OFF DAMP C-MSG TMS TERM 0 dBm 600 BAL	Connect type G test cable between VS OSC jack on UUR and INPUT 310 jack on TA-855/U.	None.
2	*UUR* DIGITAL FUNCTION: TA-855/U POWER:	 EXT CLK ON	Set VF FUNCTION and OSC LEV switches on UUR to positions indicated in a through f below and observe TA-855/U meter indication is normal. If any indication is incorrect proceed to step 6.	See indicators listed below.
			VF FUNCTION Switch Position / OSC LEV Switch Position *a*. CHAN LEV XMT — 0 dB *b*. CHAN LEV XMT — -16 dB *c*. CHAN LEV RCV — 0 dB *d*. LOOP TEST — 0 dB *e*. LOOP TEST — -16 dB *f*. COM GAIN XMT — 0dB	*a*. 0 ±0.5 dBm *b*. -16 ±0.5 dBm *c*. -23.5 ±0.5 dBm *d* 0 ±0.5 dBm *e*. -16 ±0.5 dBm *f*. -13.5 ±0.5 dBm
3	*TA-855/U* POWER:	 OFF	Remove type G test cable between TA-855/U and UUR.	None.
4	*CP-772/U* TIME BASE: FUNCTION:	 1S FREQ	Check frequency of VF oscillator as follows: *a*. Connect type J test cable between VF OSC jack on UUR and AC SIGNAL INPUT connector on CP-772/U. *b*. Verify that VF oscillator frequency displayed on CP-722/U is correct. If indicator is incorrect, proceed to step 6. *c*. Remove type J test cable between UUR and CP-772/U.	 *a*. None. *b*. 1020 ±20 Hz. *c*. None.
5	*UUR* VF FUNCTION:	 SELF-TEST	Verify VF oscillator self-test function as follows: *a*. Set METER ATTN switch on UUR to 0 dB and observe SELF TEST FAIL lamp on UUR. If indication is incorrect, proceed to step 6.	 *a*. Lamp is off.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-33
			b. Set METR ATTN switch on UUR to -10 dB and verify condition of SELF TEST FAIL lamp on UUR. If indication is correct, proceed to paragraph e below.	*b*. Lamp illuminated.
6	*AN/USM-281C*		Check VF oscillator circuit as follows:	
	VOLTS/DIV: (right)	1V	*a*. Observe oscillator output at front of R58 on analog board.	*a*. Waveform A.
	TIME/DIV:	2 ms		
	TRIG:	RIGHT		
	VERT MODE:	RIGHT		
	AC/GND/DC:	DC		
	AN/USM-281C		*b*. Observe oscillator feedback at junction of CR3 and R60 on left side of analog board.	*b*. Waveform B.
	VOLTS/DIV: (right)	2V		

e. Fault Location (VF Meter Circuits). Troubleshoot in accordance with the following procedure to locate faults in the BITE VF meter circuits.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-33
			NOTE **The following checks verify VF meter circuits (IC1, IC3, IC4, S202D, S202E, S202F, and S203). If any result is unsatisfactory, isolate and replace faulty component.**	
1	*TS-3329/U*		Verify VF meter circuit as follows:	
	FREQ RANGE:	X100	*a*. Connect type G test cable between VF METER jack on UUR and OUTPUT 310 jack on TS-3329/U.	*a*. None.
	FREQ HZ:	10.2		
	FUNCTION:	600		
	OUTPUT LEVEL:	-16.5 dBm	*b*. Set TS-3329/U and UUR controls as listed below and observe meter on UUR for normal indication. If indication is incorrect, proceed to step 4.	*b*. See indication listed below.
	POWER:	ON		

TS-3329/U Output Level	UUR VF Position	UUR METER ATTN	
-16.5 dBm	COM GAIN RCV	0dB	0 ±0.4 dB
-16.5 dBm	COM GAIN XMT	0 dB	0 ±0.4 dB
0 dBm	LOOP TEST	0 dB	0 ±0.4 dB
0 dBm	LOOP TEST	-10 dB	-10 ±2 dB
-6.4 dBm	CHAN LEV XMT	0 dB	0 ±0.4 dB
0 dBm	CHAN LEV RCV	0 dB	0 ±0.4 dB
0 dBm	CHAN LEV RCV	-10 dB	-10 ±2 dB

2	*TS-3329/U*		Disconnect type G test cable between VF METER jack on UUR and OUTPUT 310 jack on TS-3329/U.	
	POWER:	OFF		

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-33
3	*(UUR)* METER ATTN: VF FUNCTION:	 0 dB SELF TEST	Check metering circuit using VF oscillator as follows: *a.* Observe dB meter indication on UUR. If indication is incorrect, proceed to step 4. *b.* Observe SELF TEST FAIL lamp on UUR. *c.* Set METER ATTN switch on UUR to -10 dB and observe SELF TEST FAIL lamp and meter on UUR. If indication is correct, proceed to paragraph f below.	 *a.* 0 -0.4 dB. *b.* Lamp off. *c.* Lamp illuminates and meter indicates -10 ±2 dB.
4	*(UUR)* METER ATTN: *AN/USM-281C* VOLTS/DIV: (left) TIME/DIV: TRIG SOURCE: VOLTS/DIV: (left) VOLTS/DIV: (right)	 0 dB 1V 2 ms LEFT 5V IV	Check VF meter circuit waveforms as follows: *a.* Check amplifier output at IC1-9 on left side of analog board. *b.* Check amplifier output at IC3-6 on left side of analog board. *c.* Check amplifier output at IC4-6 on left side of analog board.	 *a.* Waveform C. *b.* Waveform D. *c.* Waveform E.

f. Fault Location (VF Signaling). Troubleshoot in VF signaling circuits. accordance with the following to locate faults in the BITE

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-33
1	*(UUR)* ON HOOK-OFF HOOK	 ON HOOK	Verify signaling output circuit (IC5) as follows. If any result is unsatisfactory, isolate and replace faulty component. *a.* Patch one end of type A test cable into SIG jack on UUR. Use DMM to measure voltage between ring and shield of loose end of cable. **CAUTION** **Do not permit loose end of type A test cable to short -42V OFF-HOOK signal to ground.** *b.* Set ON HOOK-OFF HOOK switch to OFF HOOK position momentarily, and use DMM to measure off hook voltage between ring and shield of loose end of cable.	 *a.* 0 0.5V. *b.* -41 ±3V.
2			Verify signaling input circuit (Q2 and Q3) as follows. If any result is unsatisfactory, isolate and replace faulty component. *a.* At loose end of type A test cable, momentarily short tip to shield and observe OFF HOOK lamp on UUR.	 *a.* Lamp illuminates.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-33
			b. Measure voltage between tip and shield of loose end of type A test cable. If indication is satisfactory, proceed to paragraph g below.	*b*. -4.5 ±0.5V.

g. Fault Location (Digital Function Clock Circuits). Troubleshoot in accordance with the following procedure to locate faults in the digital function clock circuits.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-33
1	*UUR* DIGITAL FUNCTION: *AN/USM-281C* VOLTS/DIV: (right) TIME/DIV: TRIG SOURCE:	 CLK RATE 20 kb/s 2V 20 µs LEFT	*a*. Patch one end of type A test cable into XMT CLK OUT jack on UUR. *b*. Check signal at tip of loose end of type A cable. If indication is incorrect, proceed to step 6.	*a*. None. *b*. Waveform F.
2	*UUR* DIGITAL FUNCTION: *AN/USM-281C* TIME/DIV:	 CLK RATE 50 kb/s 10 µs	Check signal at tip of loose end of type A test cable. If indication is incorrect, proceed to step 6.	Waveform G.
3	*UUR* DIGITAL FUNCTION:	 CLK RATE 20 kb/s	Connect type J test cable between AC SIGNAL INPUT connector on CP-722A/U and XMT CLK OUT jack on UUR and observe output frequency. If indication is incorrect, proceed to step 6.	19.693 ±0.5 kHz.
4	*UUR* DIGITAL FUNCTION:	 CLK RATE 50 kb/s	Connect type J test cable between AC SIGNAL INPUT connector on CP-772A/U and XMT CLK OUT jack on UUR and observe output frequency. If indication is incorrect, proceed to step 6.	50.000 ±0.012 kHz.
5	*UUR* DIGITAL FUNCTION:	 EXT CLK	Verify acceptance by UUR of external clock as follows: *a*. Install spare multirate data module strapped for 64 kb/s (table 3-4) in channel 1 position on MXTF. *b*. Connect type B (turret) test cable between XMT CLK OUT jack on multirate data module and XMT CLK IN jack on UUR. *c*. Connect type J test cable between AC SIGNAL INPUT connector on CP-772A/U and XMT CLK OUT jack on UUR and observe frequency. If indication is incorrect, proceed to step 6. If indication is satisfactory, proceed to paragraph h below.	 *a*. None. *b*. None. *c*. 64 ±0.001 kHz.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-33
6	*MXTF (UUR)* DIGITAL FUNCTION:	 CLK RATE 50 kb/s	Verify clock input circuits (IC101, IC102, and IC104), divide by circuits (IC106, IC107, IC108, IC109, IC110, IC111, IC112, and IC113), and output circuits (IC118, IC120, and IC124). If any result is unsatisfactory, isolate and replace faulty component.	
	AN/USM-281 TIME/DIV:	 .2 µs	*a*. Check 4.096 MHz CLK input at IC102-11 (waveform inverted), IC106-6, IC107-2, IC108-2, IC109-2, IC110-2, IC112-3, and IC113-2 on digital board.	*a*. Waveform H.
	TIME/DIV:	1 µs	*b*. Check first ÷9 circuit output at IC107-12 on digital board.	*b*. Waveform I.
	TIME/DIV:	10 µs	*c*. Check second ÷ 9 circuit output at IC109-12 on digital board.	*c*. Waveform J.
	TIME/DIV:	.1 ms	*d*. Check ÷13 counter output at IC113-15 on digital board.	*d*. Waveform K,
	TIME/DIV:	10 µs	*e*. Check 50-kHz clock rate at IC111-3, IC104-6, and IC118-8 on digital board.	*e*. Waveform L. (typical 50-kHz clock).
			f. Check 50-kHz output at IC120-11 on digital board.	*f*. Waveform M.
			g. Check driver output at IC124-4 on digital board.	*g*. Waveform M.
	TIME/DIV:	1 µs	h. Check the 32n-kHz output of the ÷ 13 circuit at IC108-11.	*h*. Waveform N.
	TIME/DIV:	20 µs	*i*. Check the 20-kHz output on the ÷ 16 circuit at IC110-11.	*i*. Waveform O.

h. Fault Location (Test Data Transmit and Receive Circuits). Troubleshoot in accordance with the following to locate faults in the test data transmit and receive circuits.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-33
1	*UUR* DIGITAL FUNCTION:	 EXT CLK	Verify data transmit and receive function as follows:	
			a. Connect test cables between multirate data module and UUR as follows:	*a*. None.

Test Cable Type	UUR Jack	Multirate Data Module Jack
B (turret)	RCV CLK IN	XMT CLK IN
B (turret)	RCV DATA IN	XMT DATA
B (turret)	XMT CLK IN	XMT CLK OUT
A (bantam)	XMT CLK OUT	XMT CLK IN
A (bantam)	XMT DATA OUT	XMT DATA IN

	b. Observe SYNC, RCV CLK LOSS, BIT ERROR, and BER > 10^{-2} lamps on UUR. If indication is unsatisfactory, proceed to step 2. If indication is correct, data transmit and receive circuits are good.	*b*. SYNC lamp illuminated and RCV CLK LOSS, BIT ERROR, BER > 10^{-2} lamps are off.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-33
2	*AN/USM-281C*		Connect AN/USM-281C external trigger to XMT SYNC jack on UUR, and verify data transmit and receive (IC105, IC125, IC126, IC129, and IC136) circuit as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	VOLTS/DIV: (left)	2V		
	TIME/DIV:	50 µs		
	SOURCE:	EXT		
			a. Check 8-bit feedback register output at IC114-13 on digital board.	*a*. Waveform P.
			b. Check 3-bit feedback register output at IC115-5 on digital board.	*b*. Waveform Q.
			c. Check XMT DATA output at IC119-10 on digital board.	*c*. Waveform R.
			d. Check MXT DATA driver outputs at IC120-6 and IC121-4 on digital board.	*d*. Waveform S.
			e. Check RCV DATA driver output at IC102-5 on digital board.	*e*. Waveform Q.
			f. Check RCV DATA output of selection gate at IC105-8.	*f*. Waveform R.
			g. Check RCV DATA output at IC136-8.	*g*. Waveform R.
			h. Check 8-bit register output at IC125-13.	*h*. Waveform T.
			i. Check 3-bit register output at IC126-7.	*i*. Waveform U.
	AN/USM-281C		*j*. Momentarily disconnect type B test cable from XMT CLK OUT jack on multirate data module and observe error pulses at IC129-2 on digital board.	*j*. Waveform V.
	TIME/DIV:	10 µs		
	TRIG SOURCE:	RIGHT		

3-19. Troubleshooting Power Supply Group

The power control units (ac and dc) and the EMI units do not require specialized troubleshooting procedures. This paragraph contains troubleshooting procedures for the dc converter, PWR SPLY unit monitor and alarm board, and the TRF unit. Refer to figures FO-13 and FO-14, and to figure 3-35 for parts locations.

WARNING

Do not attempt to remove any part of the power supply group without first disconnecting external power from the multiplexer set. Hazardous voltages will be exposed while troubleshooting the PWR SPLY unit. Avoid voltage contact.

NOTE

Instructions to verify voltage in the following paragraphs mean to read the voltage on the VOLTS display on the PMTF. Instruction to make continuity checks means to use AN/USM-223.

a. Tools and Test Equipment.

(1) TK-100/G.
(2) AN/USM-281C.
(3) DMM.
(4) PMTF with the following accessories:
TRF adapter cable
Extender board TRW 17330-010
External leads for voltage measurements
Type K test cable.
(5) AN/USM-223.

b. Initial Setup. Prepare test equipment and faulty power supply module for troubleshooting as follows:

(1) Set PMTF controls as follows:

Switch	*Position*
POWER	OFF
LOADS (all)	MIN
OUTPUT SELECT	-48
MODULE TEST	MOD INPUT INT

(2) Using extender board, install faulty PWR SPLY module into receptacle of PMTF.

(3) Connect type K test cable between SCOPE SYNC and SYNC jacks PMTF and MAIN TRIG IN jack on AN/USM-281C (black cable tip goes to SYNC jack).

(4) Install MXTF test leads in EXTERNAL

VOLT jacks on PMTF (purple jack is common lead).

(5) Set test equipment switches as follows:

Unit	*Switch*	*Position*
AN/USM-281C	POWER	ON
	AC/GND/DC	AC
PMTF	POWER	ON
	TRF INPUT LINE ADJUST	120

(6) On PMTF, adjust INTERNAL -48V ADJ control to obtain -48 ±0.1V indication on VOLTS DC display.

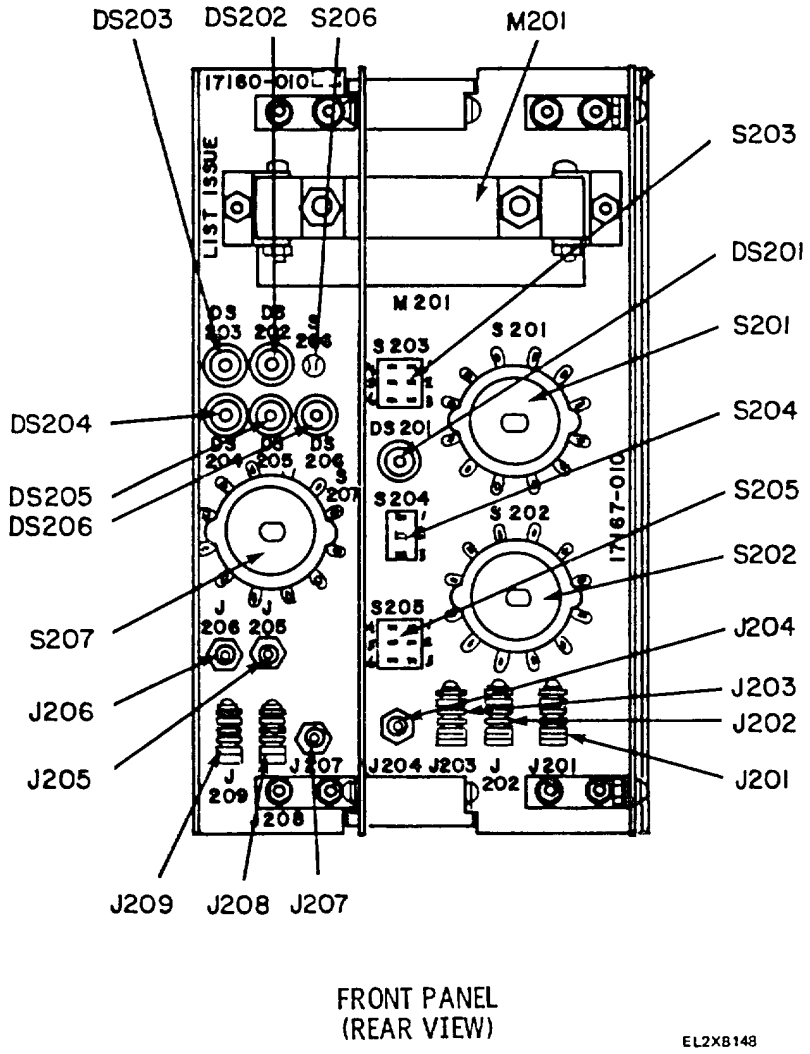


Figure 3-32. BITE parts location diagram (sheet 1 of 4).

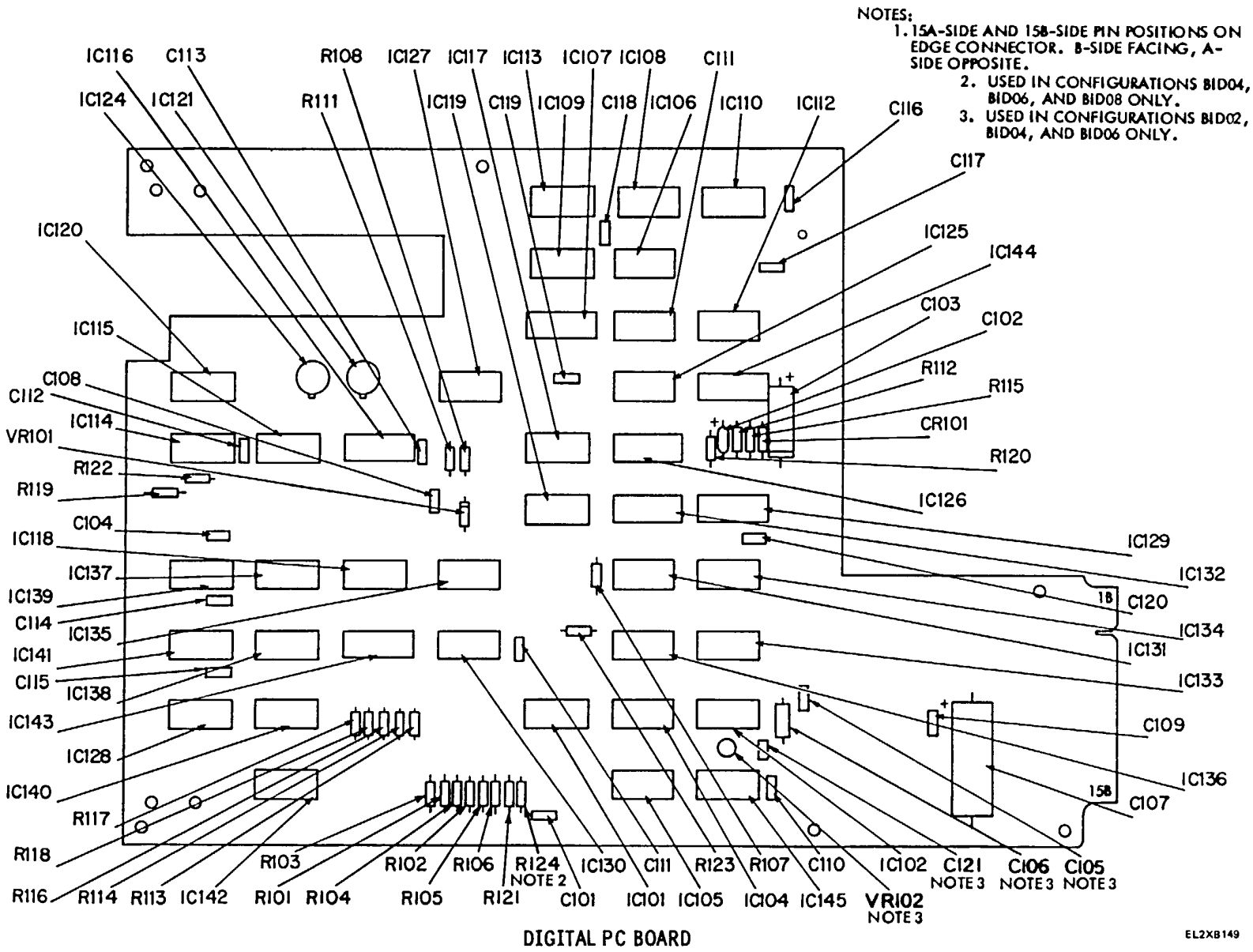


Figure 3-32. BITE parts location diagram (sheet 2 of 4).

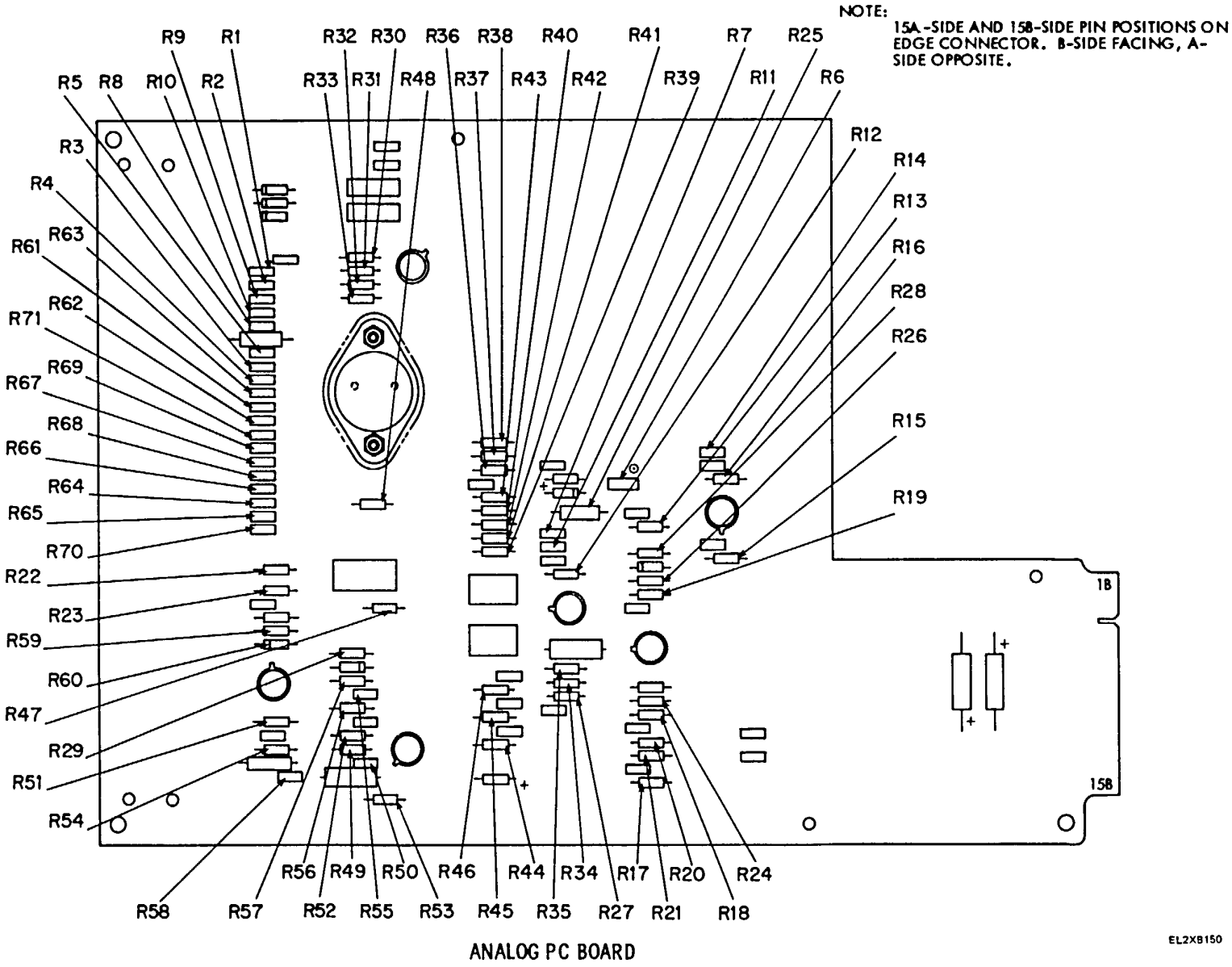


Figure 3-32. BITE parts location diagram (sheet 3 of 4).

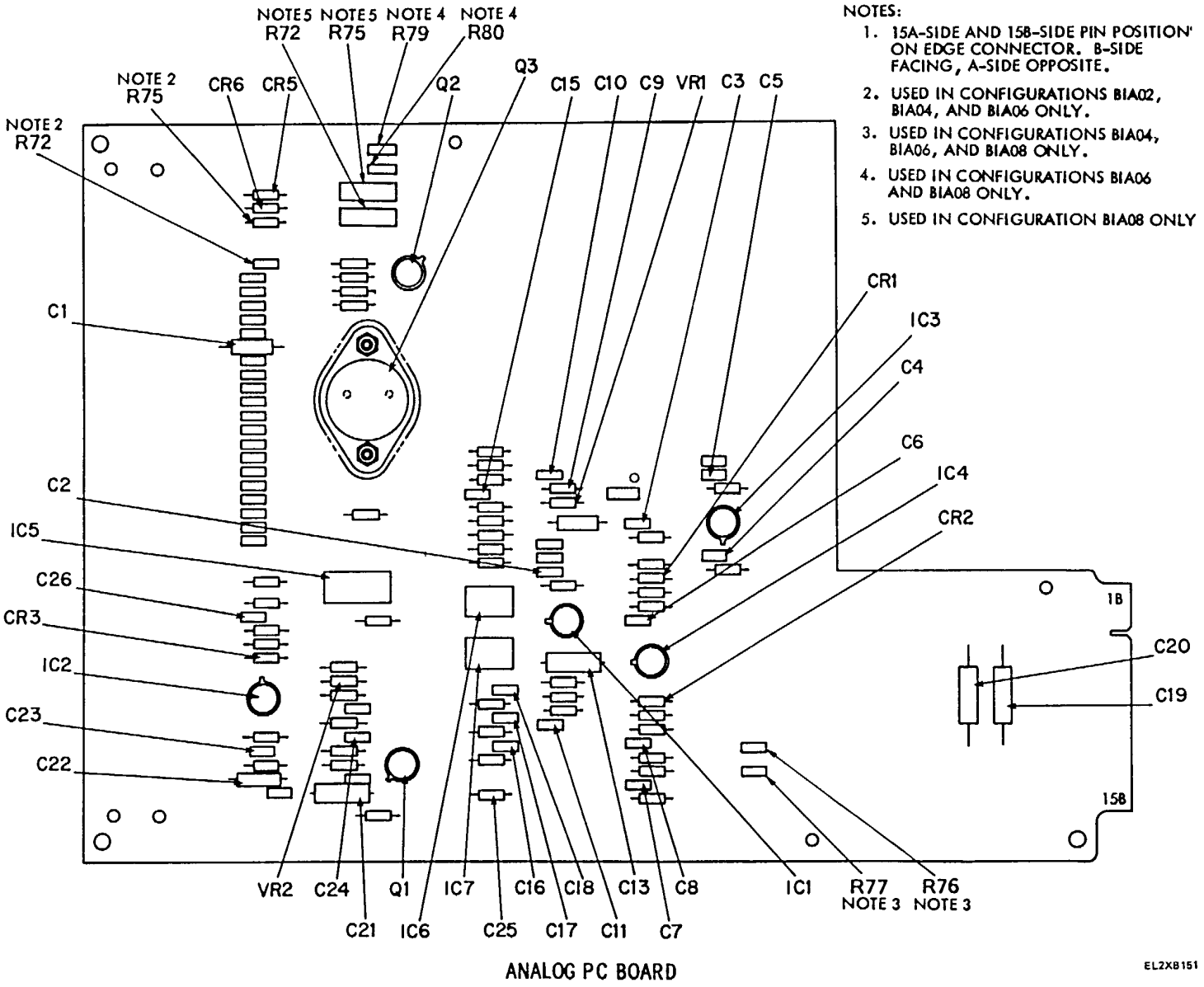


Figure 3-32. BITE parts location diagram (sheet 4 of 4).

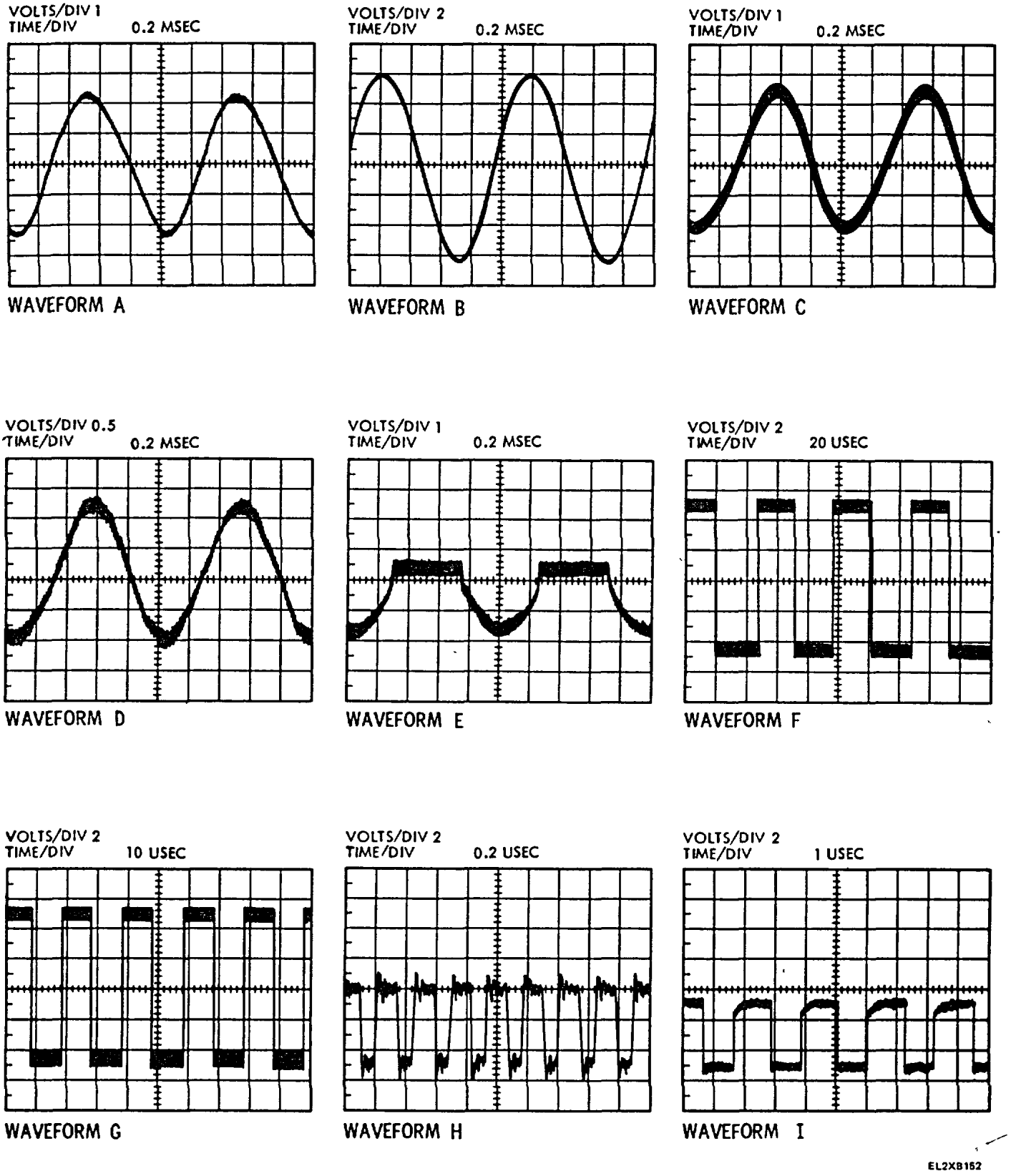


Figure 3-33. BITE troubleshooting waveforms (sheet 1 of 3).

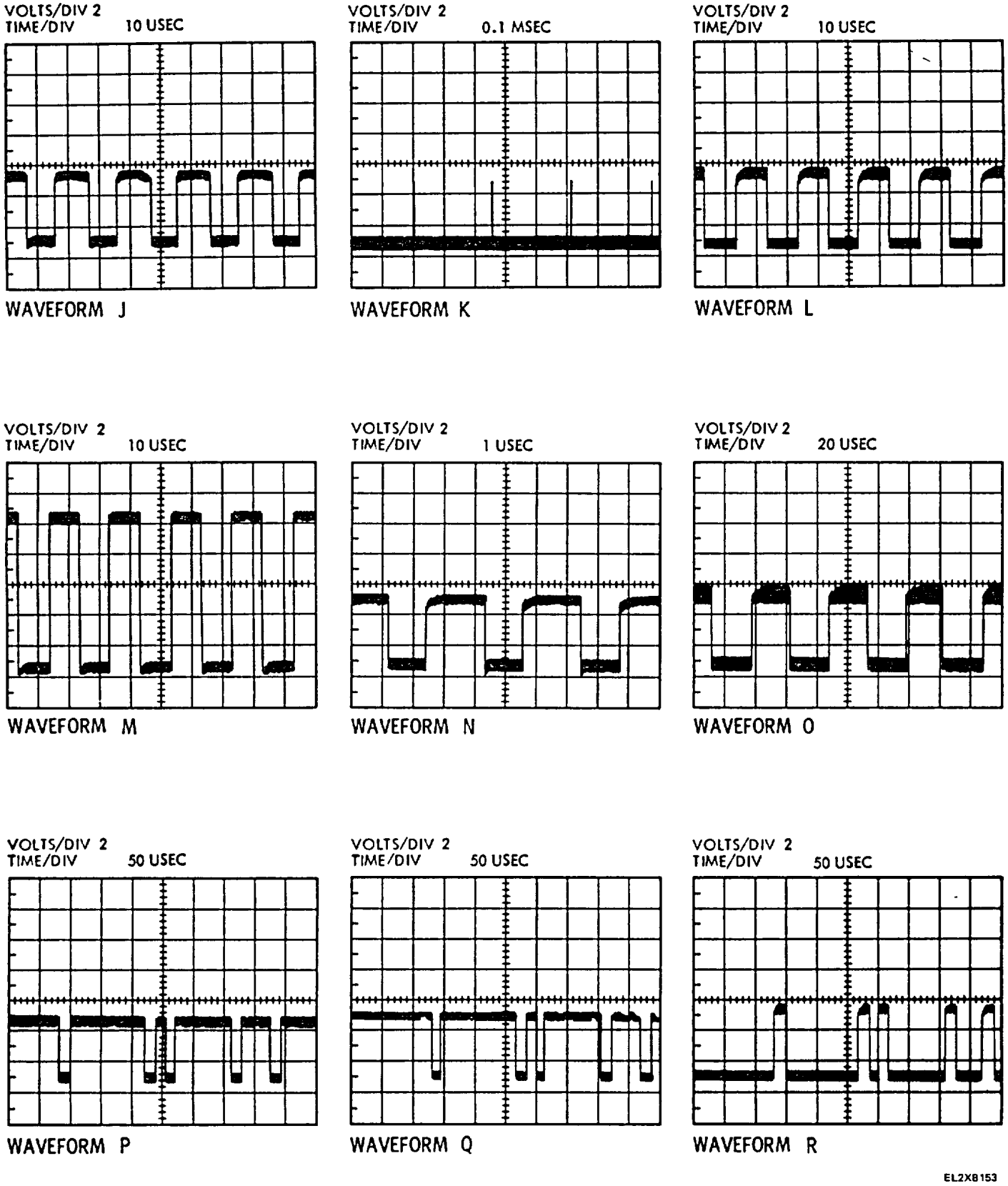


Figure 3-33. BITE troubleshooting waveforms (sheet 2 of 3).

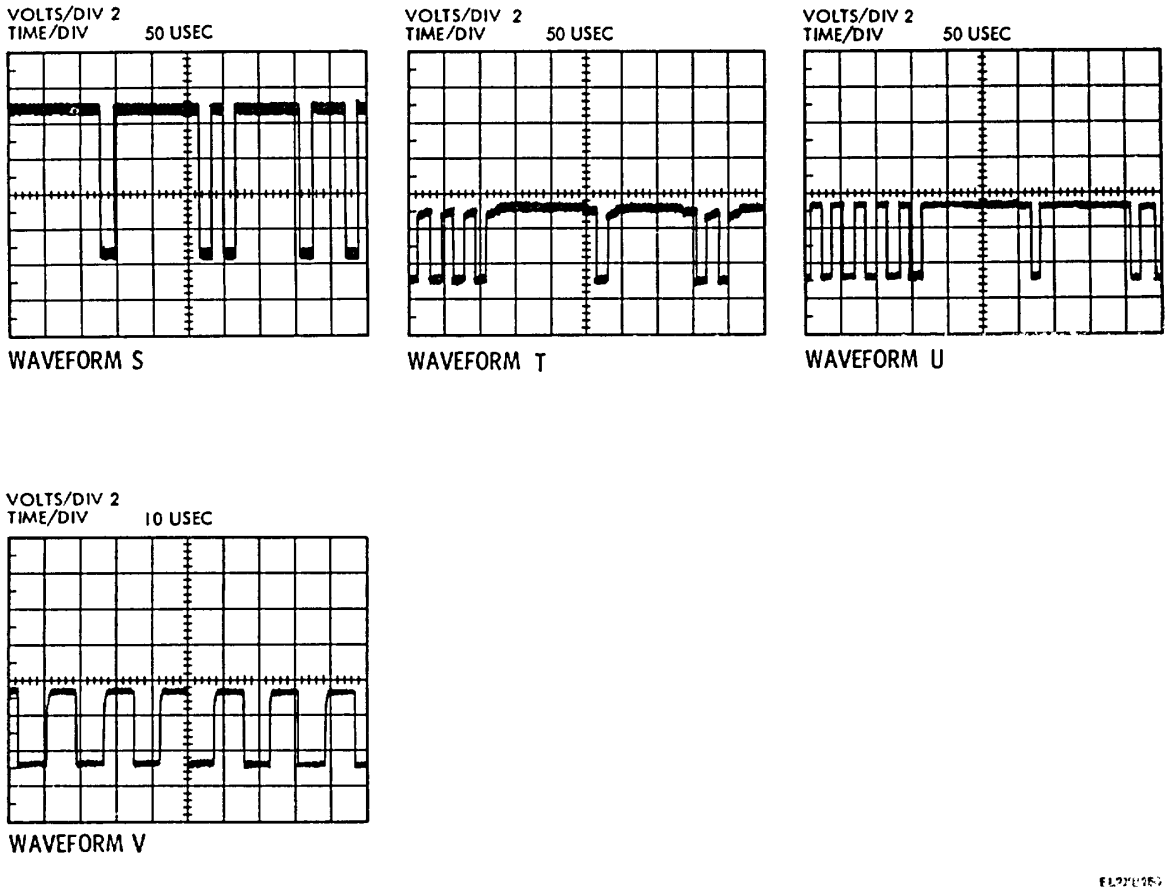


Figure 3-33. BITE troubleshooting waveforms (sheet 3 of 3).

c. Fault Location (Dc Converter Board). Troubleshoot in accordance with the following procedure to locate malfunctions in the de corverter circuits in the UUR.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-34
1	*AN/USM-281C* VOLTS/DIV: TIME/DIV:	 20V 20 µs	Check signal at collector case of Q3 on dc converter card.	Waveform A.
2			Check signal at collector case of Q12.	Waveform B.
3			Verify T6 voltage outputs. If any voltage is unsatisfactory, isolate and replace faulty component.	
	PMTF OUTPUT SELECT:	 -42	*a*. Verify voltage (PMTF internally connected to pins P2-12B and P1-21B).	*a*. -39 to -44 Vdc,.
		-7	*b*. Verify voltage (PMTF internally connected to pins P2-10B and P1-21B).	*b*. -6.5 to -7.5 Vdc.
		+7	*c*. Verify voltage (PMTF internally connected to pins P2-6B and pins P1-2B).	*c.* +6 5 to +7.5 Vdc

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-34
4	*PMTF* OUTPUT SELECT:	EXT	Using EXTERNAL VOLT leads, check de voltages at IC7-6, and at IC7-7 with common lead connected to + (lower) end of C27.	(IC7-6) 4.5 to 5 Vdc, (IC7-7 4.5 to 5 Vdc.
5			Verify T3 voltage outputs. If any voltage is unsatisfactory, isolate and replace faulty component.	
	PMTF OUTPUT SELECT:	+15	*a*. Verify voltage (PMTF internally connected to pins P1-6B and P1-21B).	*a*. +13 to +17 Vdc.
		+12(2)	*b*. Verify voltage (PMTF internally connected to pins P1-5B and P1-21B).	*b*. +11 to +13 Vdc.
		-15	*c*. Verify voltage (PMTF internally connected to CR10 anode and P1-21B).	*c*. -13 to -17 Vdc.
		-12(2)	*d*. Verify voltage (PMTF internally connected to pins P1-2B and P1-21B).	*d*. -11 to -13 Vdc.
		-5(2)	*e*. Verify voltage (PMTF internally connected to pins P1-8B and P1-21B).	*e*. -4.5 to -5.5 Vdc.
6	*PMTF* OUTPUT SELECT:	EXT	Using EXTERNAL VOLT leads, check de voltages at IC7-1 and at IC7-2 with common lead connected to C27 + (lower end).	(IC7-1) -4.5 to -5.2 Vdc. (IC7-2) -4.5 to -5.2 Vdc.
7			Using EXTERNAL VOLT leads, measure voltage between IC1-14 and IC1-7. Use IC1-7 as common.	-4.5 to -5.5 Vdc.
8			Verify clock logic (IC1, IC2, IC3, IC9, and Q11). If any result is unsatisfactory, isolate and replace faulty component.	None.
	AN/USM-281C VOLTS/DIV: TIME/DIV:	2V 20 µs	*a*. Check sync signal at upper end of R81.	*a*. Waveform C.
			b. Check signal at IC9-8 and IC2-2.	*b*. Waveforms D and E.
			c. Check CLK signal at IC1-13 and IC1-6.	*c*. Waveforms E and F.
	AN/USM-281C VOLTS/DIV:	5V	*d*. Check signal at collector (case) of Q11.	*d*. Waveform G.
9			Verify drive functions (IC3, IC7, IC8, and Q4). If any result is unsatisfactory, isolate and replace faulty component.	None.
	AN/USM-281C VOLTS/DIV:	.5V	*a*. Check at IC7-12.	*a*. Waveform H.
	VOLTS/DIV:	5V	*b*. Check signal at R46 (bottom end).	*b*. Waveform L
	VOLTS/DIV:	1V	*c*. Check signal at IC7-10.	*c*. Waveform J.
	VOLTS/DIV:	5V	*d*. Check signal at R36 (bottom side).	*d*. Waveform I.
	VOLTS/DIV:	1V	*e*. Check signal at IC3-8.	*e*. Waveform K.
	VOLTS/DIV:	5V	*f*. Check signal at IC1-4 (CR36 anode).	*f*. Waveform L..
	VOLTS/DIV:	5V	*g*. Check signal at collector of Q4 (T2 terminal 20).	*g*. Waveform M.

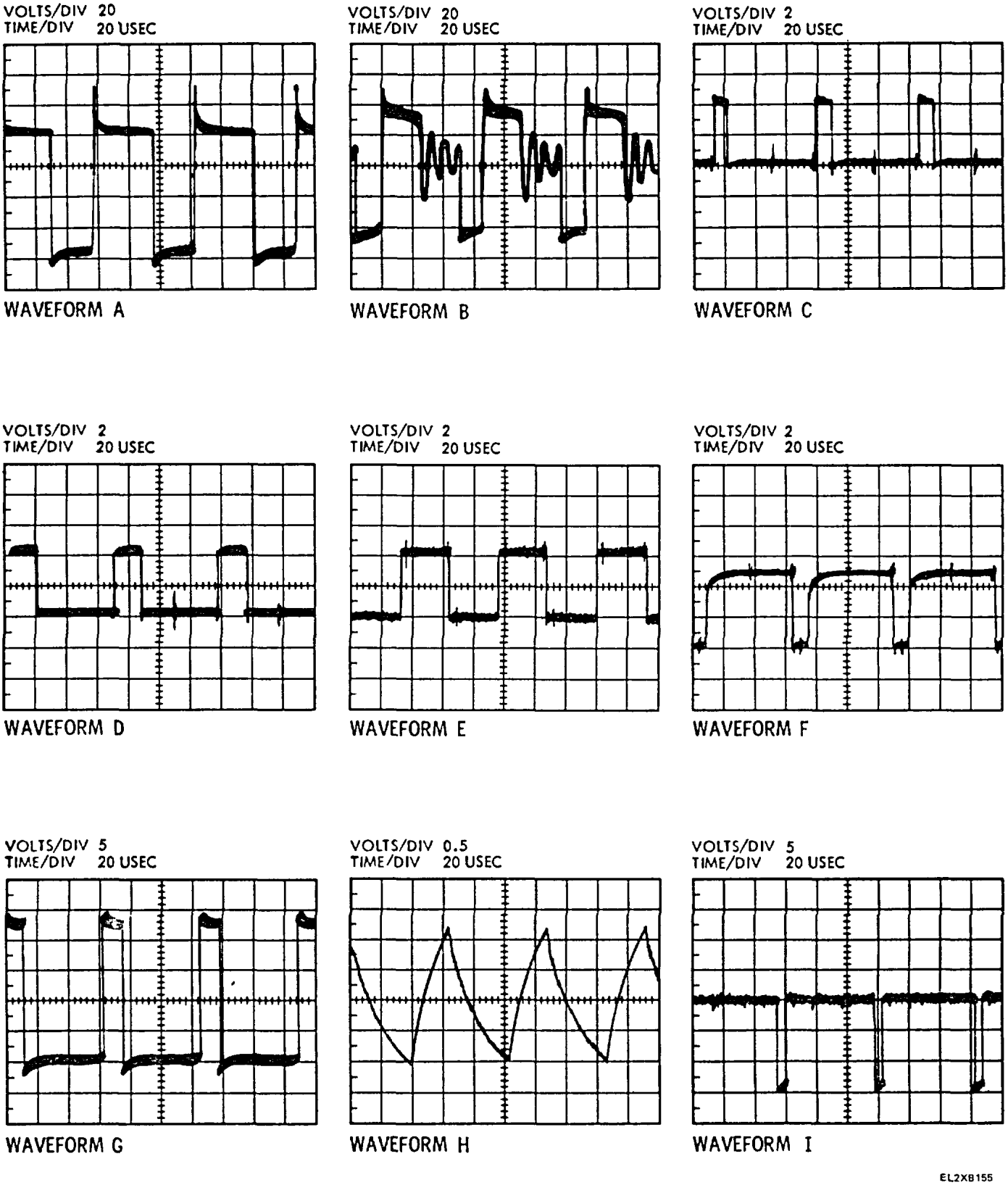


Figure 3-34. PWR SPLY dc converter troubleshooting waveforms (sheet 1 of 2).

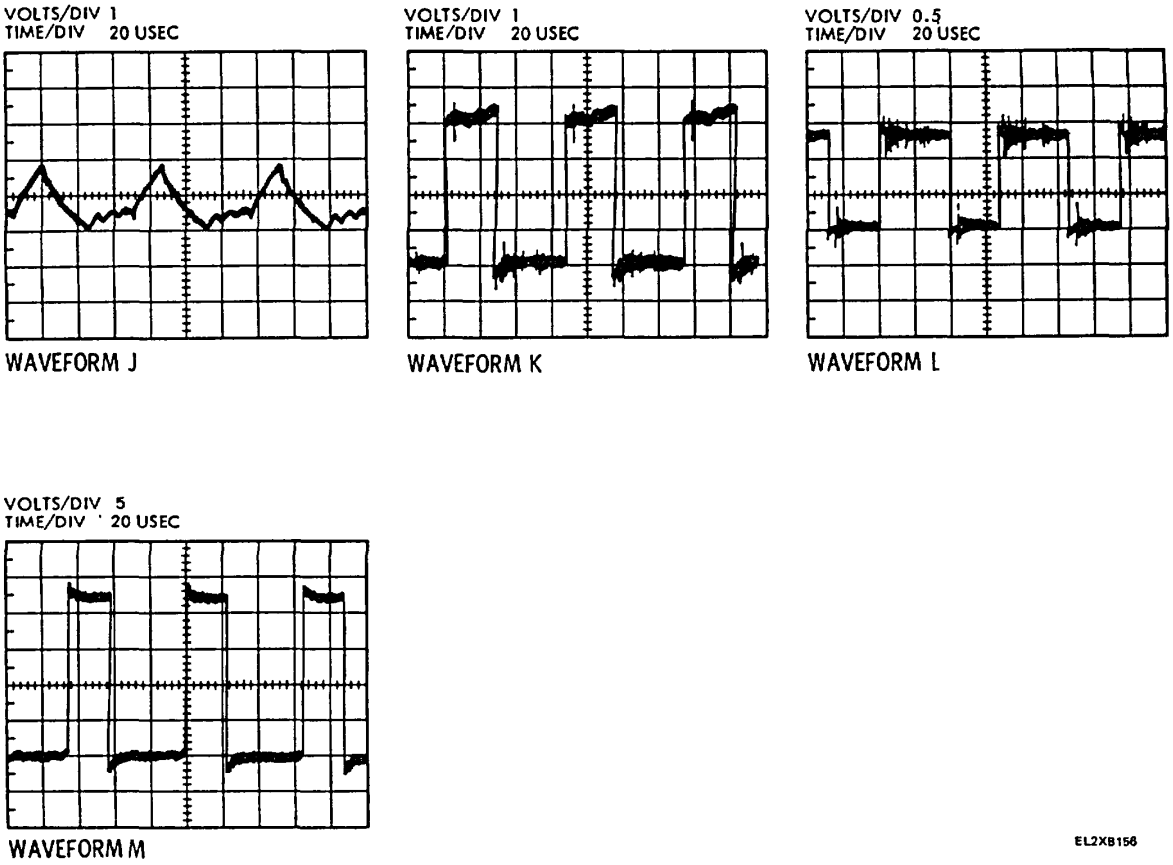


Figure 3-34. PWR SPLY dc converter troubleshooting waveforms (sheet 2 of 2).

d. Fault Location (Monitor and Alarm Circuits). Troubleshoot in accordance with the following procedure to locate malfunctions in the PWR SPLY monitor and alarm circuits.

Step	Control	Setting	Trouble sectionalization chart	Normal indication
1	*PMTF* FAULT SIMULATION LSOUT:	FAULT	Verify loss-of-output functions (IC3, IC4, and IC7 through IC10; relays K1, K8, and K9; and transistors Q8 and Q17 through Q20) as follows. If any result is unsatisfactory, isolate and replace faulty component. **NOTE** **The following loss-of-output troubleshooting also covers all other monitor and alarm circuits that are common with the loss-of-output circuit.** *a*. On front panel of UUR, observe C.G.A. lamp. *b*. Using EXTERNAL VOLT leads, measure voltage states at following	*a*. Lamp illuminated.

Step	Control	Setting	Trouble sectionalization chart	Normal indication
			points (common lead connected to C17 positive side).	
			(1) IC3-4.	(1) LO.
			(2) IC9-8.	(2) HI.
			(3) IC8-6.	(3) LO.
			(4) IC8-8.	(4) HI.
			(5) IC4-10.	(5) LO.
			(6) IC4-2.	(6) -3.0 to -4.4 Vdc.
			(7) Q18 collector.	(7) LO.
			c. Check condition of K1 on PMTF front-panel test points.	*c*. Continuity between C and NO.
			d. Measure voltage states at following points:	
			(1) QS collector.	(1) LO.
			(2) IC3-2.	(2) -3.0 to -4.4 Vdc.
			e. Check condition of K8 at PMTF test points.	*e*. Continuity between C and NO.
			f. Measure voltage status at the following points:	
			(1) Q17 collector.	(1) LO.
			(2) IC4-6.	(2) -3.0 to -4.4 Vdc.
			(3) IC4-10.	(3) LO.
			g. Check condition of K9 at PMTF front-panel test points.	*g*. Continuity between C and NO (delay after power application).
			h. Measure voltage states at following points:	
			(1) Q21 collector.	(1) LO (delay after power application).
			(2) IC7-14.	(2) HI (delay after power application).
			(3) IC10-2.	(3) HI (at slow rate).
			i. Check condition of CGA bus by measuring voltage states at the following points:	
			(1) Output pin P1-3A.	(1) HI.
			(2) IC10-10.	(2) -3.0 to -4.4 Vdc.
			(3) Q20 collector.	(3) LO.
			(4) Q19 collector.	(4) HI.
2	*PMTF*		Verify fault alarm functions (IC3, IC4, K2, Q9 and Q10) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	FAULT SIMULATION LSOUT:	NORMAL		
	FAULT SIMULATION FLTBUS:	FAULT	*a*. Observe FAULT LAMP on front panel of UUR.	*a*. Lamp illuminated.
			b. Measure voltage states at the following points:	
			(1) Q10 collector.	(1) LO.
			(2) IC3-10.	(2) -3.0 to -4.4 Vdc.
			c. Check condition of K2 at PMTF test points.	*c*. Continuity between C and NO.
			d. Measure voltage states at following locations:	
			(1) Q9 collector.	(1) LO.
			(2) IC3-6.	(2) -3.0 to -4.4 Vdc.
3	*PMTF*		Verify loss-of-input functions (IC3, IC5, IC8, IC10, K3, and Q11) as follows. If result of any check is unsatisfactory, isolate and replace faulty component.	
	FAULT SIMULATION FLTBUS:	NORMAL		
	FAULT SIMULATION LSIN:	FAULT	*a*. On UUR front panel, observe C.G.A. lamp.	*a*. Lamp illuminated.

Step	Control	Setting	Trouble sectionalization chart	Normal indication
			b. Check condition of K3 at test points on PMTF front panel.	*b*. Continuity between NO and C.
			c. Measure voltage states at the following points:	
			(1) Q11 collector.	(1) LO.
			(2) IC3-12.	(2) -3.0 to -4.4 Vdc.
			d. Check condition of OGA bus by measuring voltage states at the following points:	
			(1) Pin P1-1A (upper connector).	(1) HI.
			(2) IC8-3.	(2) HI.
			(3) IC5-2.	(3) LO.
4	*PMTF*		Verify loop functions (IC4, IC5, K4, Q12, and Q13) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	FAULT SIMULATION LSIN:	NORMAL		
	FAULT SIMULATION LOCLP:	FAULT	*a*. Observe LOCAL LOOP and C.G.A. lamps on UUR front panel.	*a*. Lamps illuminated.
			b. Measure voltage states at the following points:	
			(1) Q13 collector.	(1) LO.
			(2) IC5-8.	(2) -3.0 to -4.4 Vdc.
			(3) IC5-6.	(3) LO.
			c. Check condition of K4 at PMTF front-panel test points.	*c*. Continuity between C and NO.
			d. Measure voltage states at following points:	
			(1) Q12 collector.	(1) LO.
			(2) IC5-4.	(2) -3.0 to -4.4 Vdc.
			e. Check all-is output by measuring voltage state at IC4-12.	*e*. HI.
5	*PMTF*		Verify remote loop alarm functions (IC5, IC6, K5, Q14, and Q15) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	FAULT SIMULATION LOCLP:	NORMAL		
	FAULT SIMULATION REMLP:	FAULT	*a*. On UUR, observe REMOTE LOOP and C.G.A. lamps.	*a*. Lamps illuminated.
			b. Measure voltage states at following points:	
			(1) Q14 collector.	(1) LO.
			(2) IC5-10.	(2) -3.0 to -4.4 Vdc.
			(3) IC5-12.	(3) LO.
			c. Check condition of K5 at PMTF front-panel test points.	*c*. Continuity between C and NO.
			d. Measure voltage states at following points:	
			(1) Q15 collector.	(1) LO.
			(2) IC6-2.	(2) -3.0 to -4.4 Vdc.
6	*PMTF*		Verify loss-of-frame functions (IC6, IC7, IC8, IC10, K6, and Q16) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	FAULT SIMULATION REMLP:	NORMAL		
	FAULT SIMULATION LSFR:	FAULT	*a*. On UUR, observe C.G.A. lamp.	*a*. Lamp illuminated.
			b. Measure voltage states at the following points:	
			(1) Output pin P1-1A (upper connector).	(1) HI.
			(2) IC6-6.	(2) LO.
			(3) IC6-8.	(3) HI.
			(4) IC10-4.	(4) HI.
			(5) IC10-8.	(5) HI.
			(6) IC7-1.	(6) LO.
			(7) IC8-3.	(7) HI.

Step	Control	Setting	Trouble sectionalization chart	Normal indication
			c. Measure condition of K6 at PMTF front-panel test points.	*c*. Continuity between C and NO.
			d. Measure voltage states at the following points:	
			(1) Q16 collector.	(1) LO.
			(2) IC6-4.	(2) -3.0 to -4.4 Vdc.
7	*PMTF*		Verify remote alarm functions (IC4, IC6, IC7, IC10, and Q22) as follows. If any result is unsatisfactory, isolate and replace faulty component.	
	FAULT SIMULATION LSFR:	NORMAL		
	FAULT SIMULATION REMAL:	FAULT	*a*. On UUR, observe REMOTE ALARM and C.G.A. lamps.	*a*. Lamps illuminated.
			b. Measure voltage states at the following points:	
			(1) IC6-10.	(1) LO.
			(2) IC6-12.	(2) HI.
			(3) IC10-6.	(3) HI.
			(4) IC7-2.	(4) LO.
			(5) IC4-4.	(5) -3.0 to -4.4 Vdc after delay.
			(6) Q22 collector.	(6) LO.

WARNING

Hazardous voltages will be exposed while troubleshooting PWR SPLY units. Take care at all times to avoid contact with open electrical circuits. Do not attempt to perform any maintenance on the TRF unit unless the large capacitor is carefully discharged.

e. Fault Location (TRF Unit). The TRF unit does not require specialized troubleshooting procedures. To determine the probable cause of a TRF failure, test the faulty unit in accordance with paragraph 3-40; then analyze the test results as follows:

Test Failure Symptom	*Probable Cause*
No (zero) voltage outputs.	T1 secondary or L1 open.
Low voltage outputs, ripple is acceptable.	One T1 primary section open, or section(s) of CRs faulty.
Voltage outputs OK, but ripple is excessive.	C1 or R9 faulty (loss of capacitance or increased resistance).
Voltage outputs low and ripple excessive.	C1 or R9 faulty (leaky capacitor or decreased resistance).
Voltage and ripple OK, but current outputs are low.	CR1 faulty or T1 windings shorted.

3-20. Troubleshooting Rear Assembly

Troubleshooting procedures for the rear assembly of a multiplexer set consist of a visual inspection and point-to-point continuity checks.

a. Visual Checks. Visual inspection should concentrate on front (module) and rear (cable) connections. The connectors should be inspected closely for any evidence of corrosion or damage such as arcing or bent pins.

b. Continuity Checks. Continuity checks should be made with an AN/USM-233. The data for such checks is contained in the wire list in appendix B.

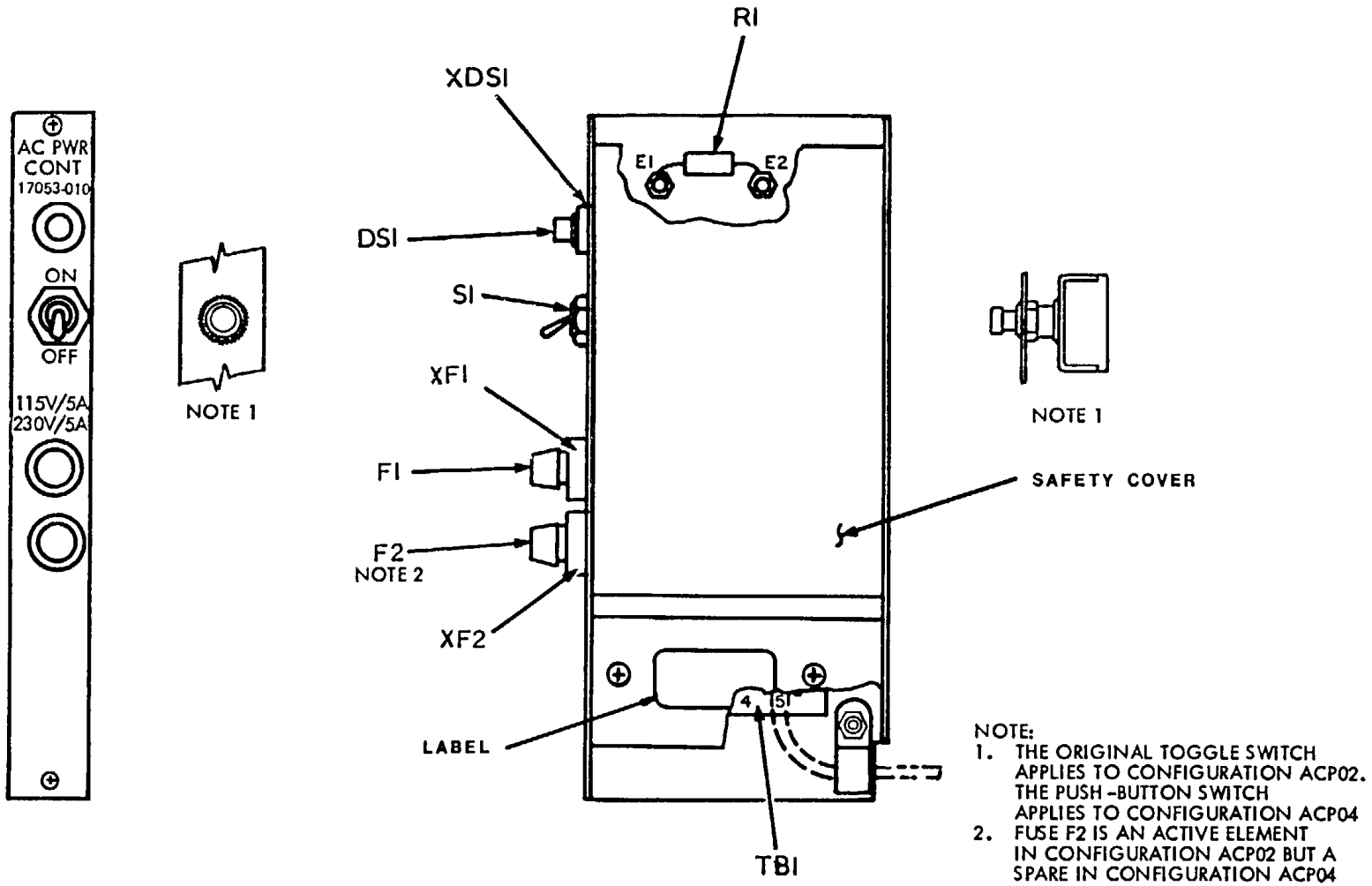


Figure 3-35. Power supply group parts location diagram (sheet 1 of 19).

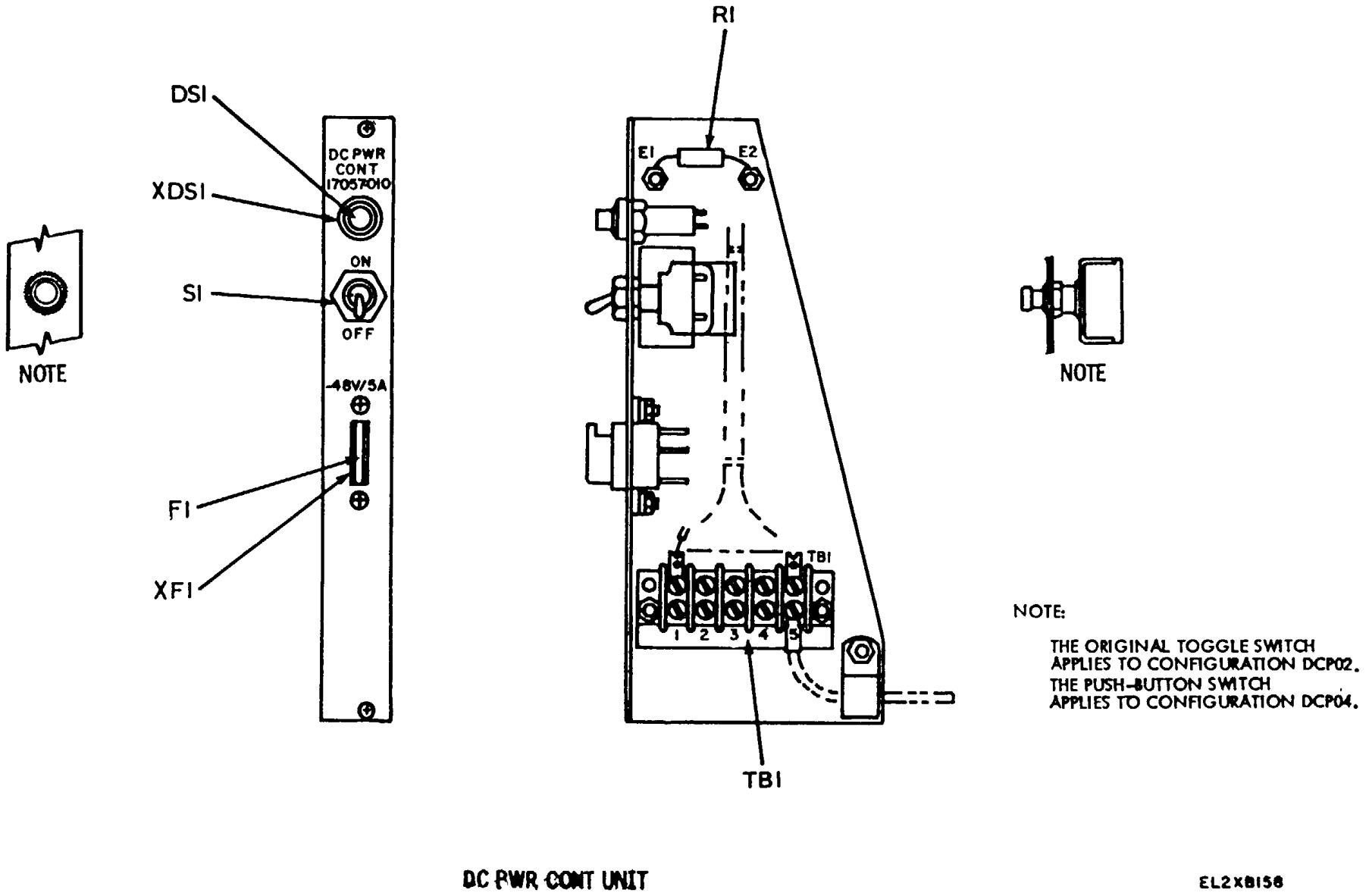


Figure 3-35. Power supply group parts location diagram (sheet 2 of 19).

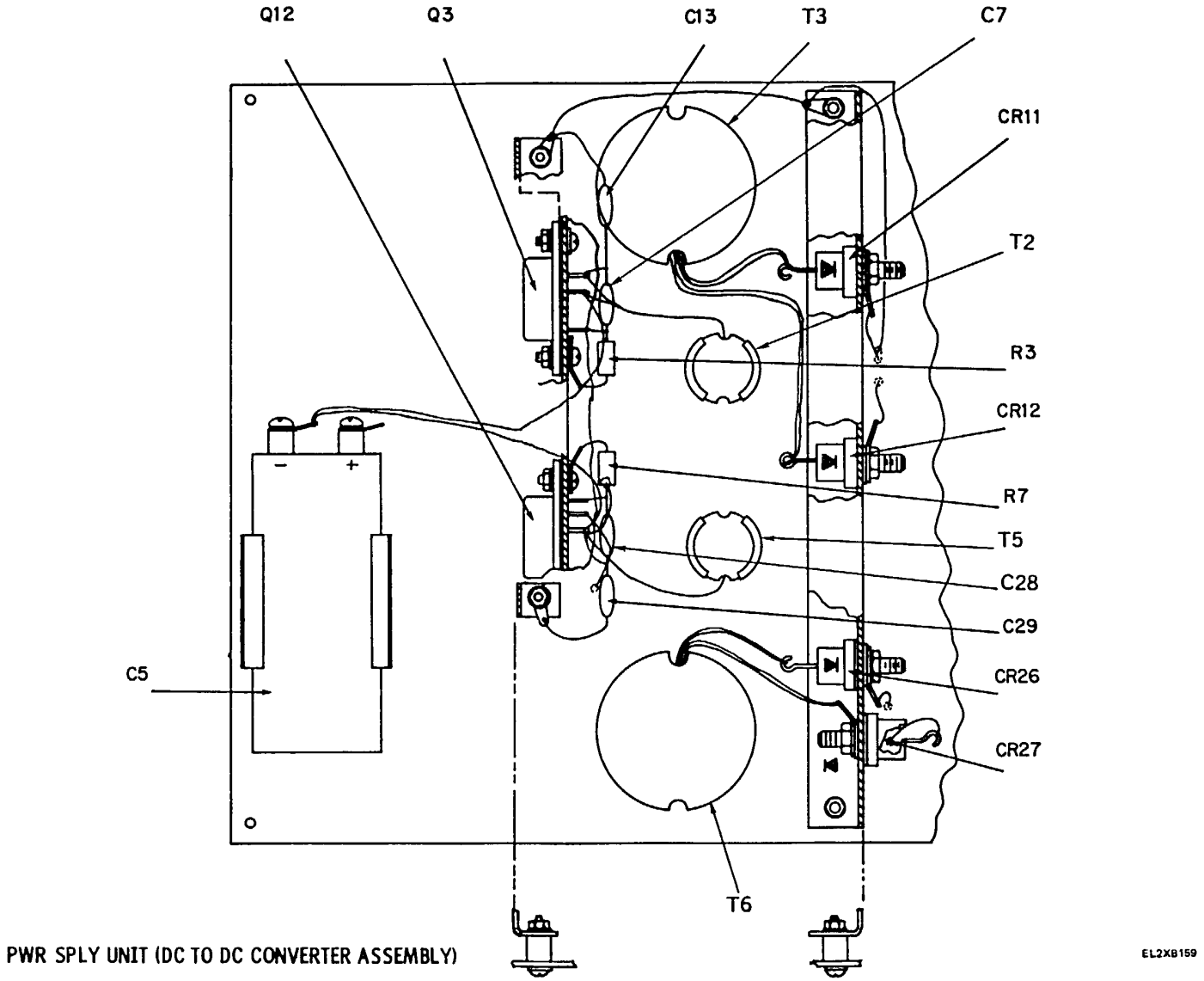


Figure 3-35. Power supply group parts location diagram (sheet 3 of 19).

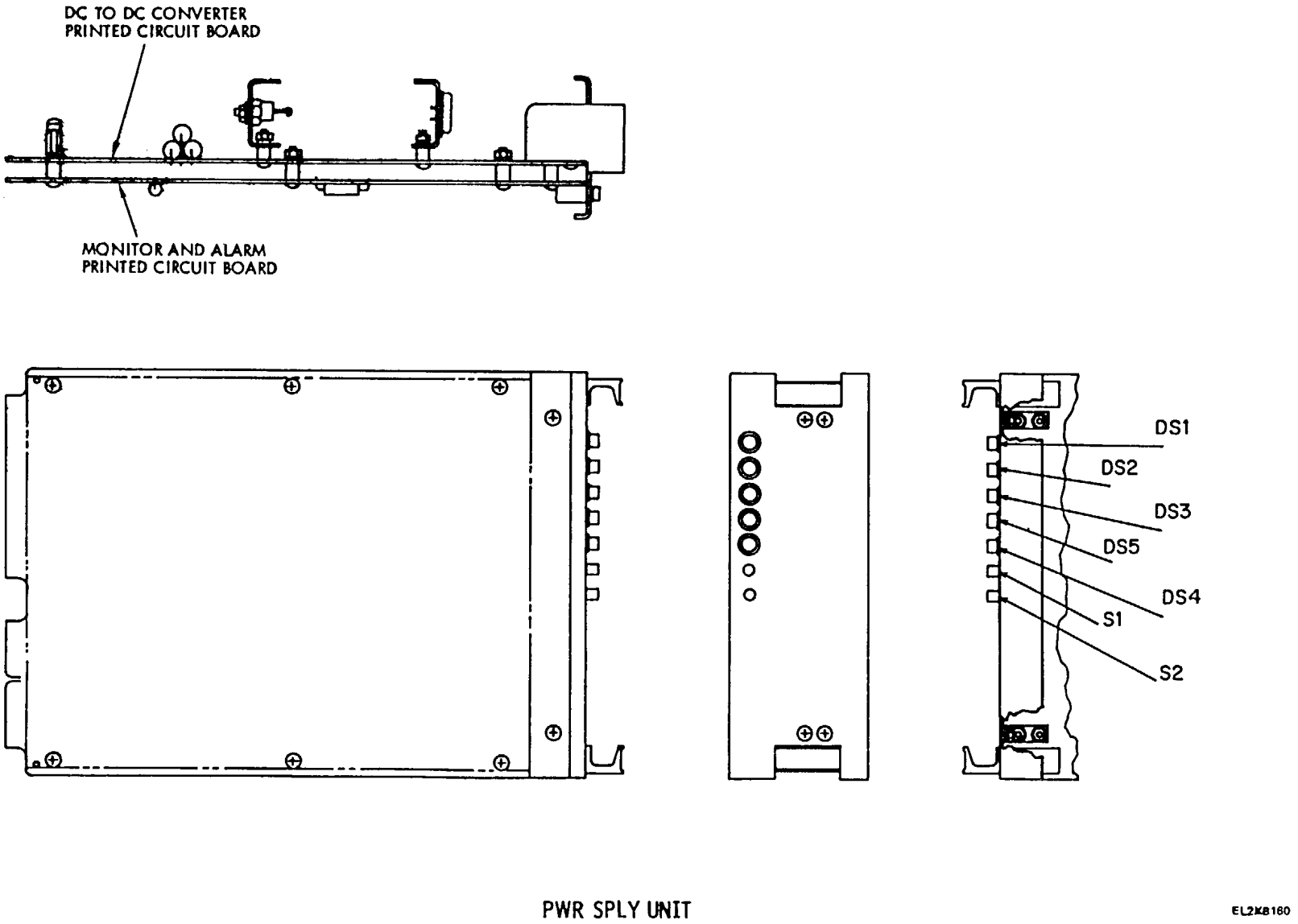


Figure 3-35. Power supply group parts location diagram (sheet 4 of 19).

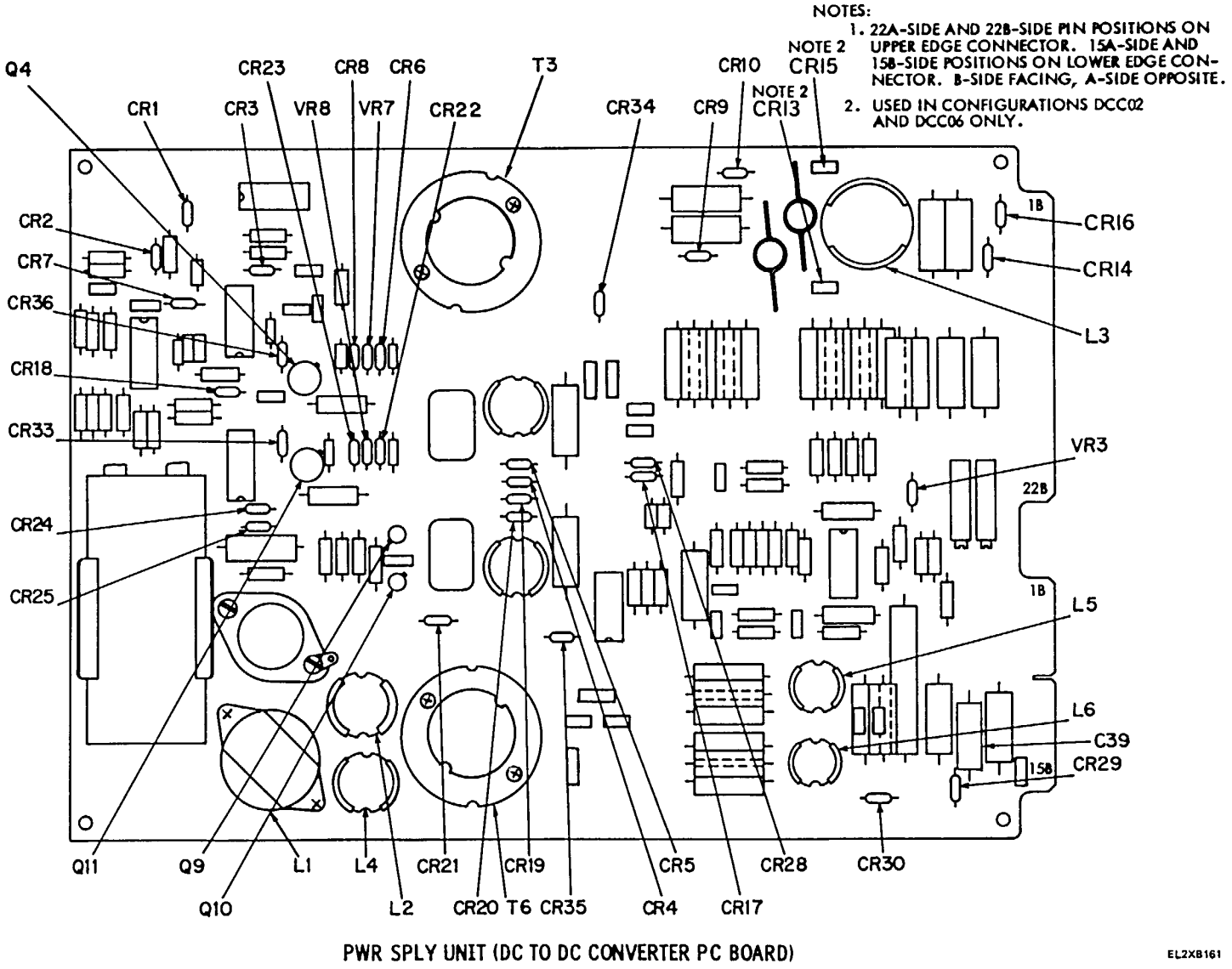


Figure 3-35. Power supply group parts location diagram (sheet 5 of 19).

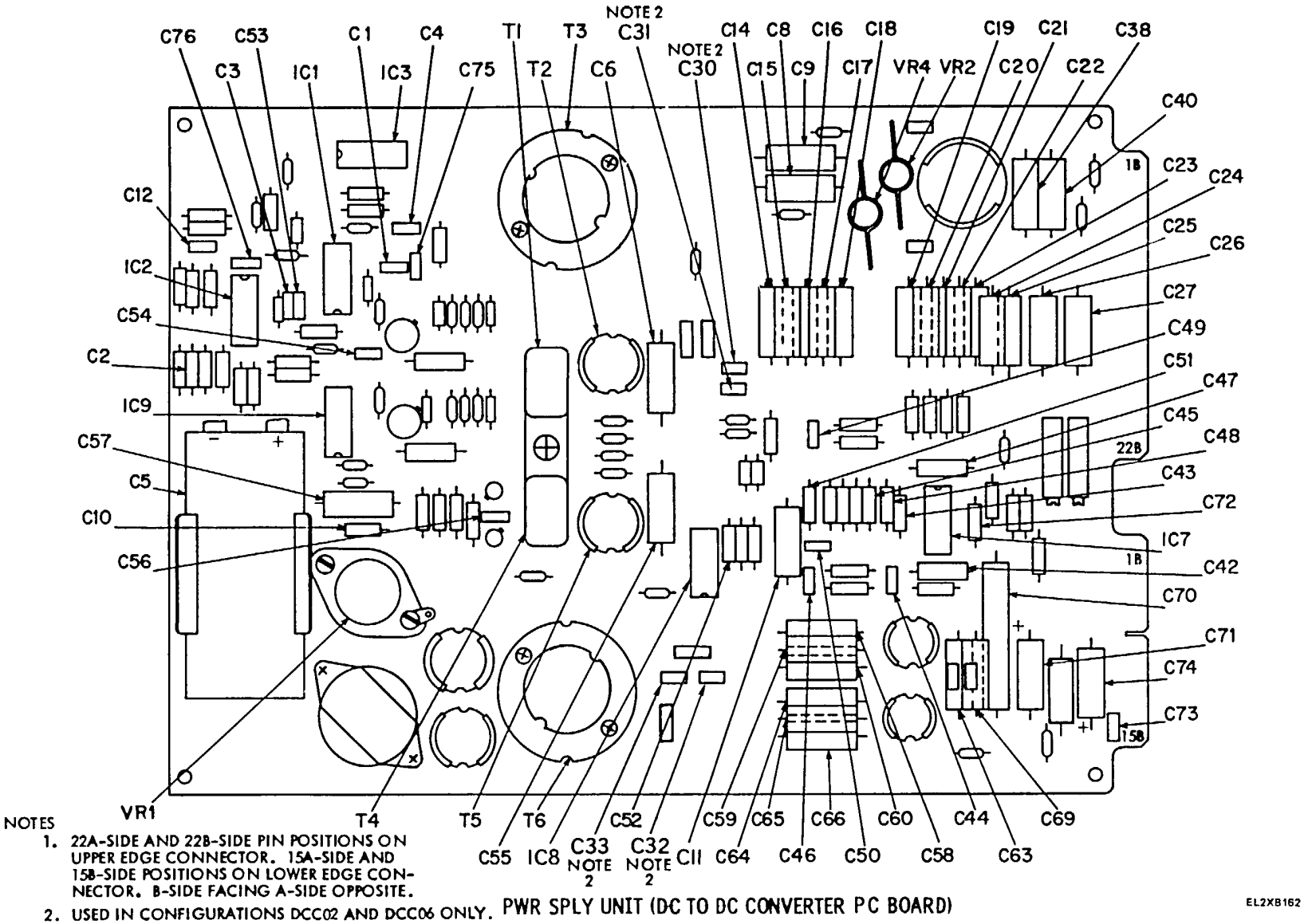


Figure 3-35. Power supply group parts location diagram (sheet 6 of 19).

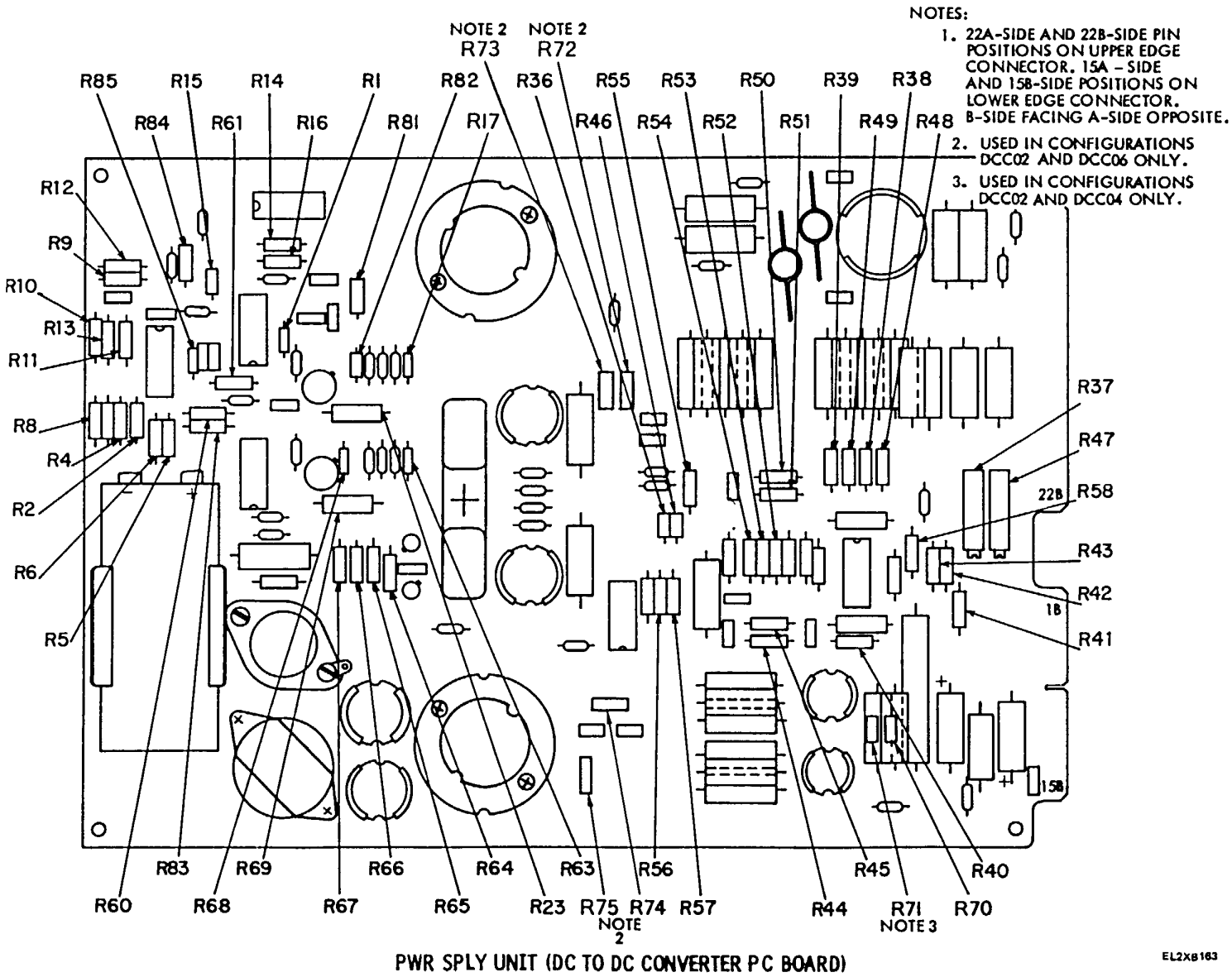


Figure 3-35. Power supply group parts location diagram (sheet 7 of 19).

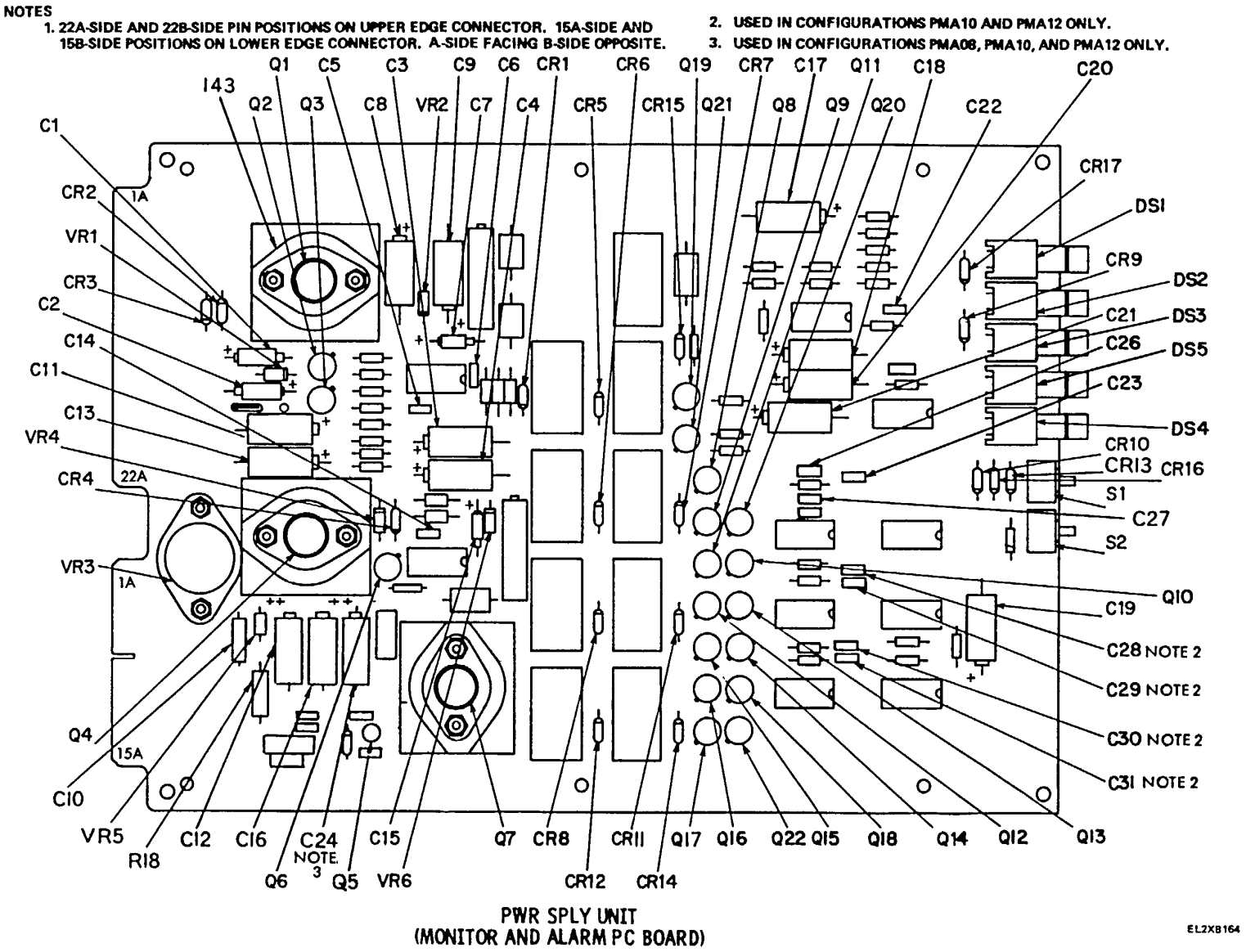


Figure 3-35. Power supply group parts location diagram (sheet 8 of 19) PMA02, PMA08, PMA10, and PMA12.

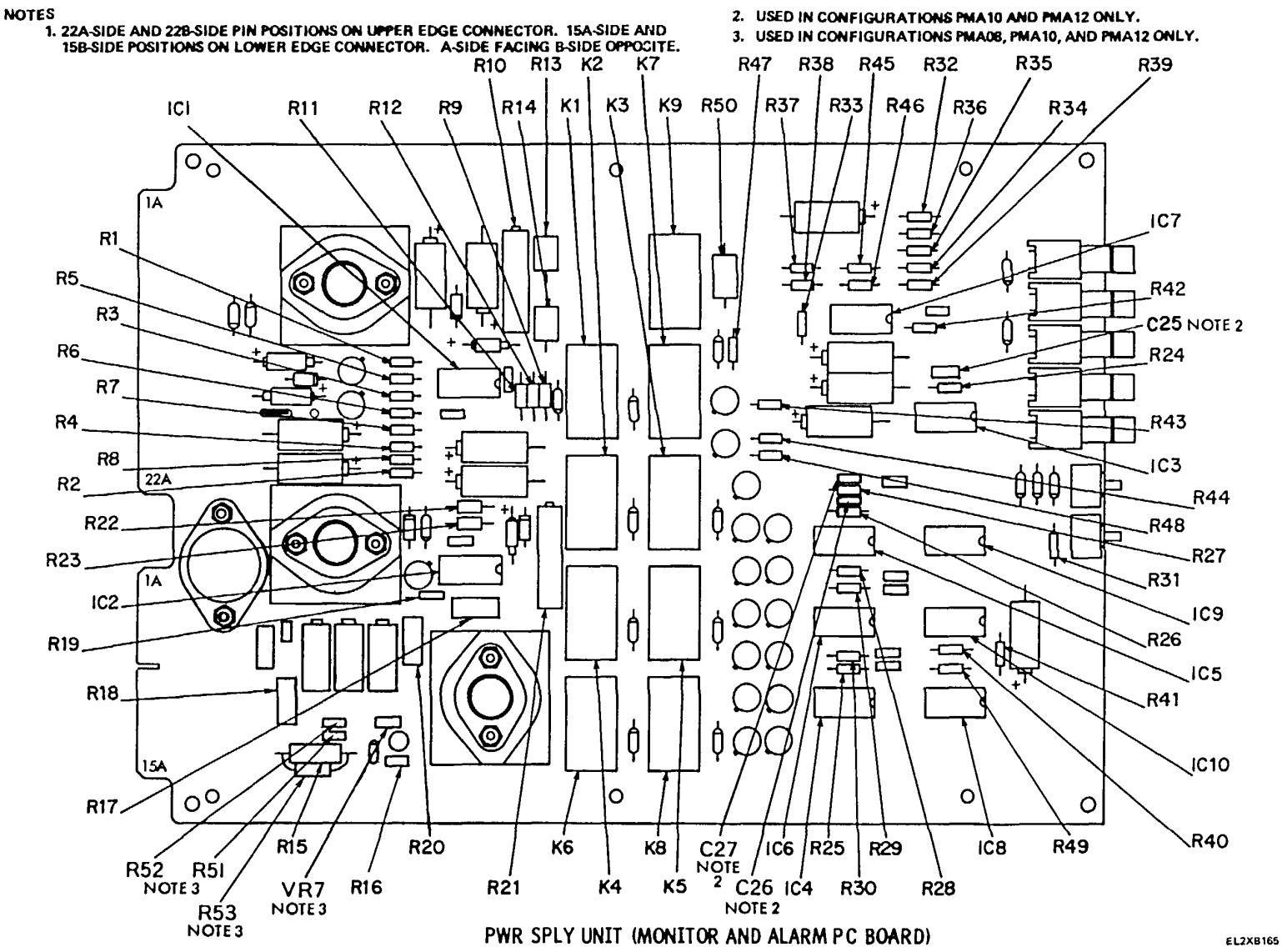


Figure 3-35. Power supply group parts location diagram (sheet 9 of 19) PMA02, PMA08, PMA10, and PMA12.

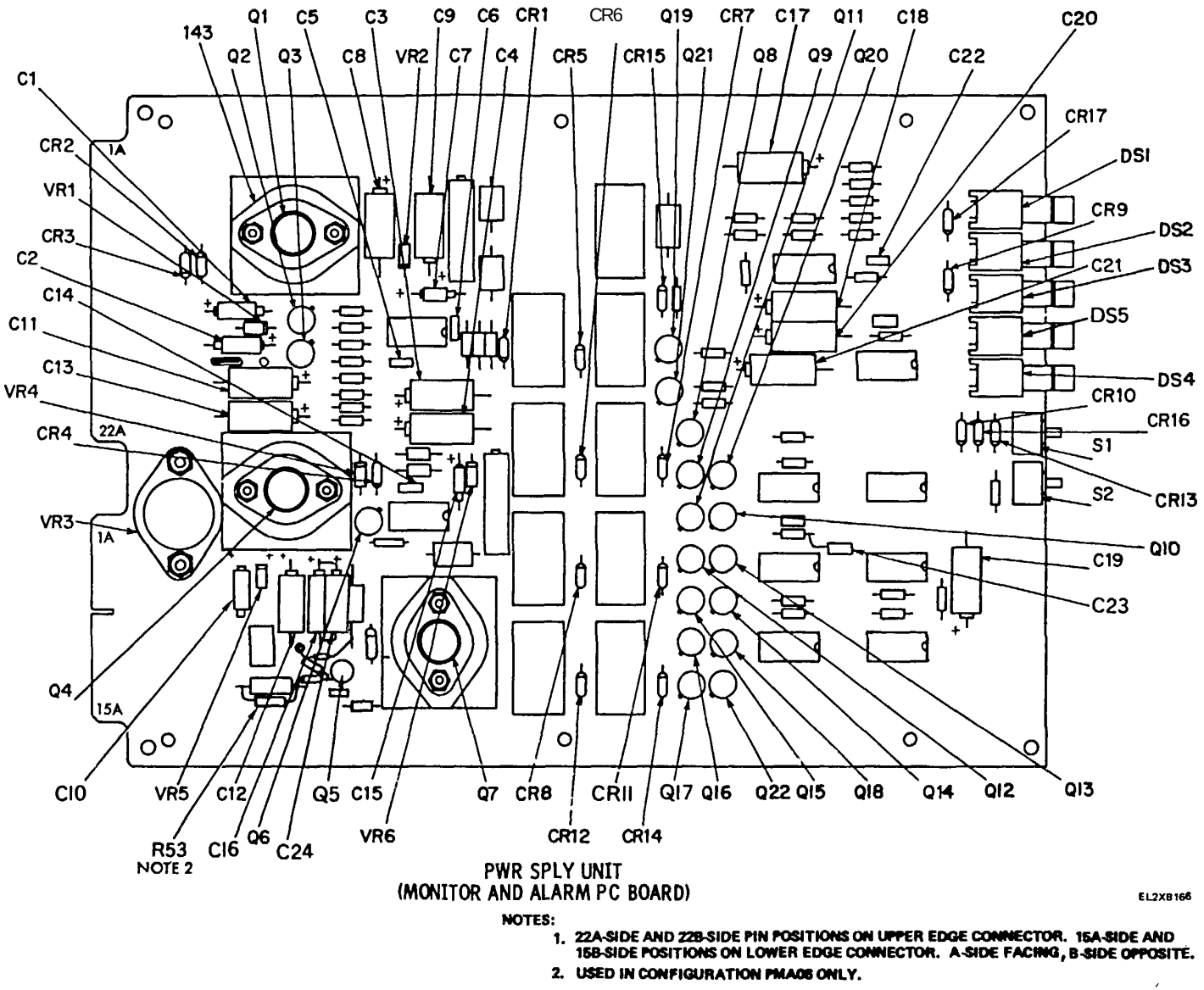
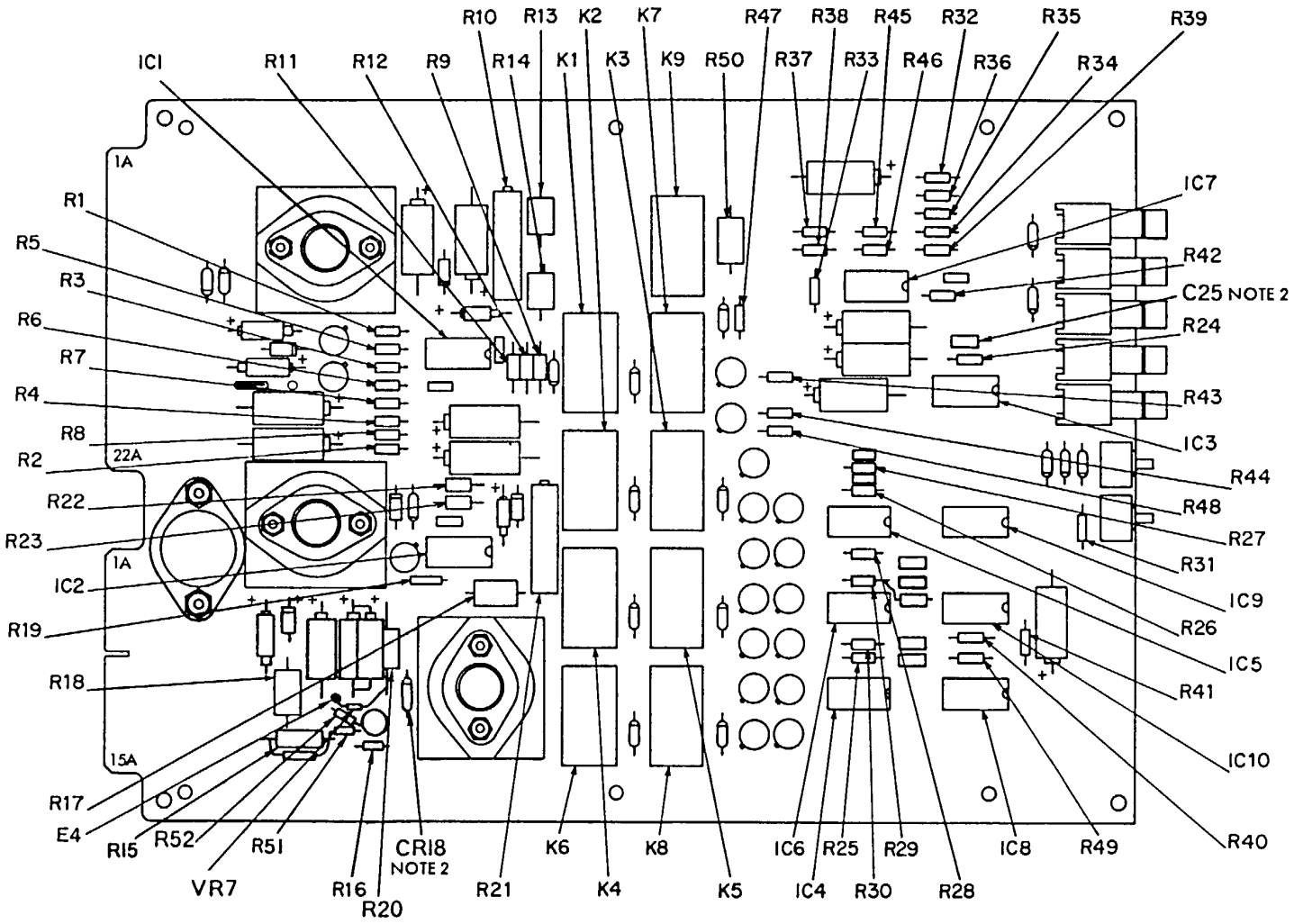


Figure 3-35. Power supply group parts location diagram (sheet 10 of 19) PMA04 and PMA06.



NOTES

1. 22A-SIDE AND 22B-SIDE PIN POSITIONS ON UPPER EDGE CONNECTOR. 15A-SIDE AND 15B-SIDE POSITIONS ON LOWER EDGE CONNECTOR. A-SIDE FACING, B-SIDE OPPOSITE.
2. USED IN CONFIGURATION PMA06 ONLY.

Figure 3-45. Power supply group parts location diagram (sheet 11 of 19) PMA04 and PMA05.

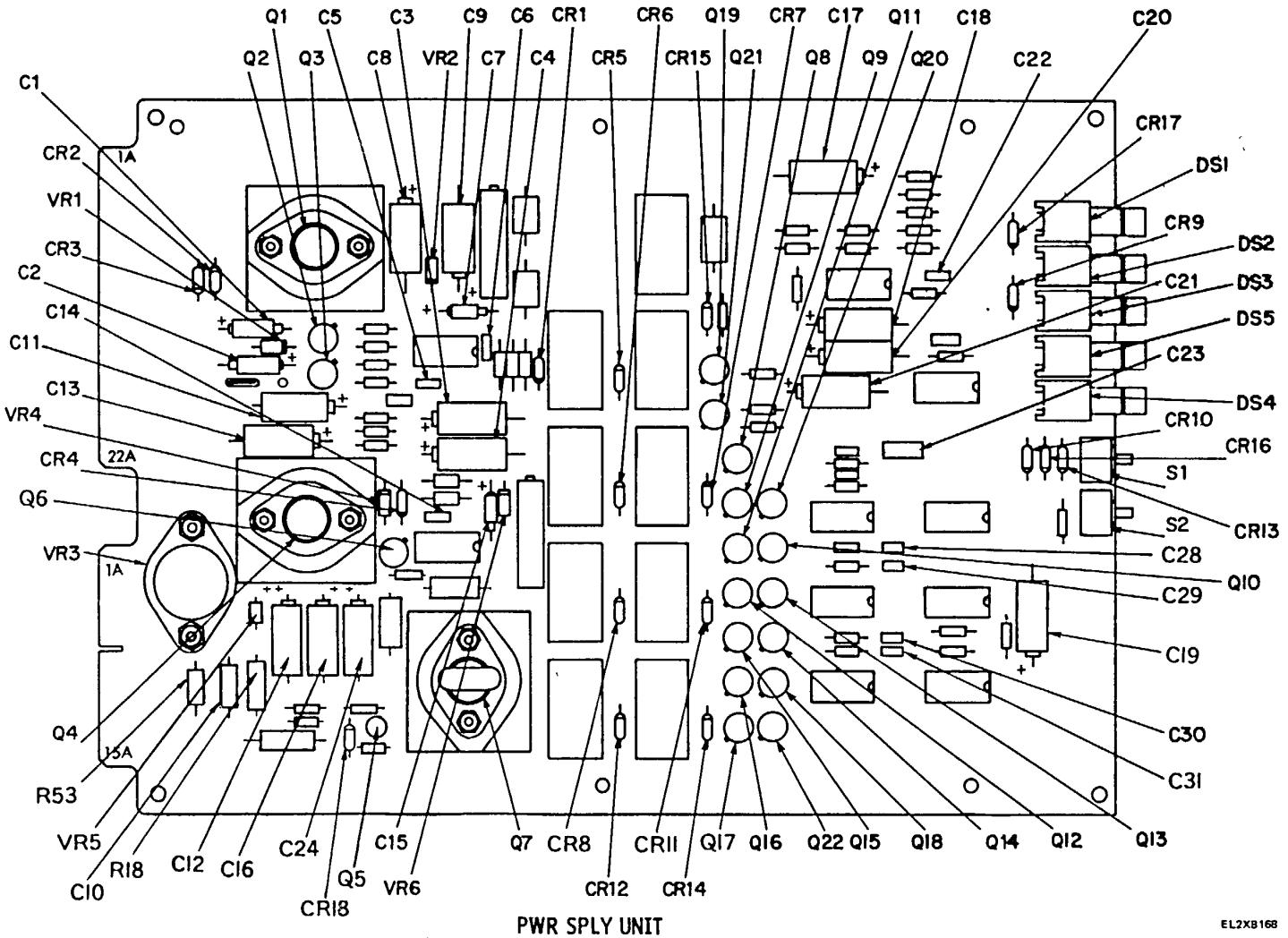


Figure 3-35. Power supply group parts location diagram (sheet 12 of 19) PMA14.

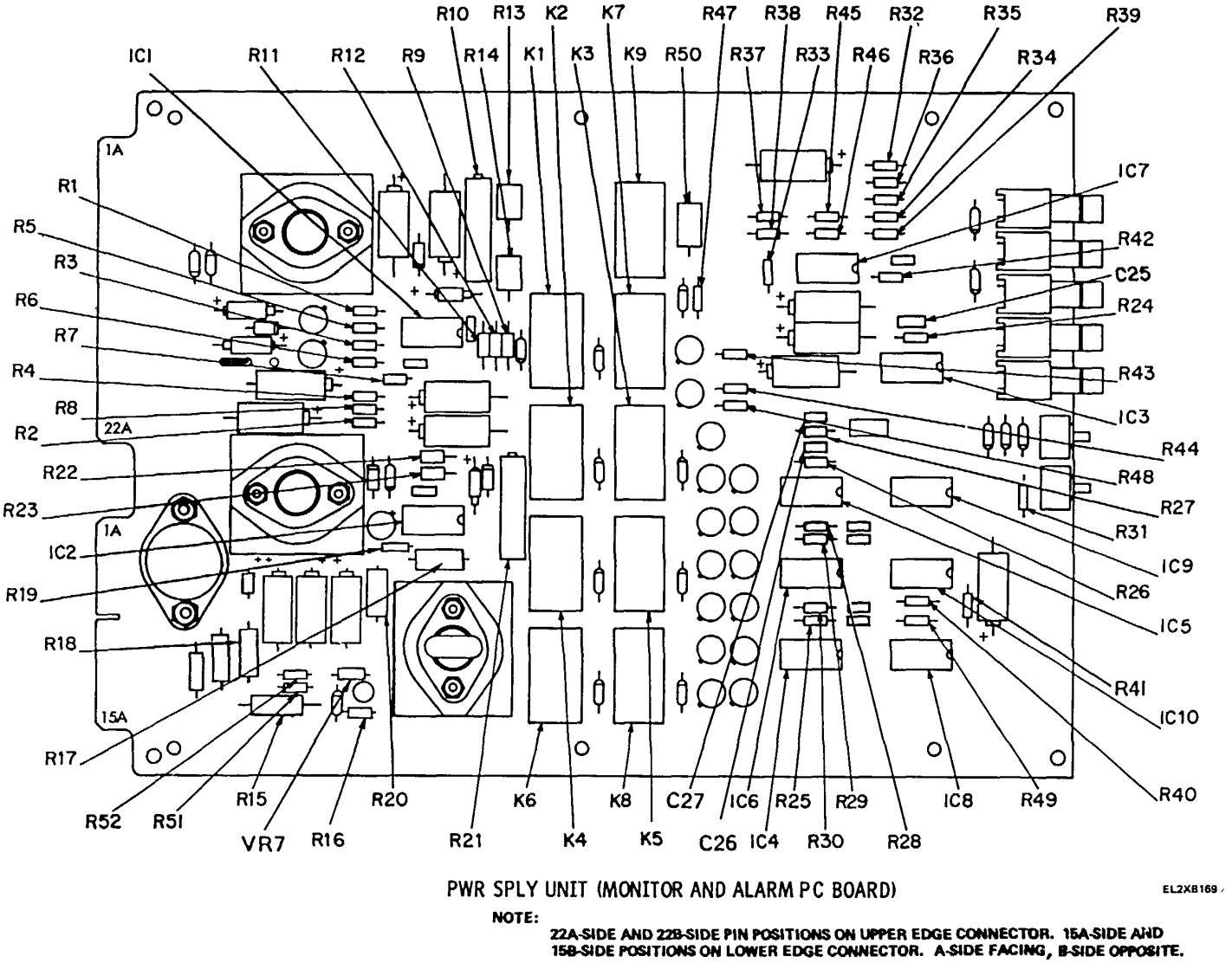


Figure 3-35. Power supply group parts location diagram (sheet 13 of 19) PMA14.

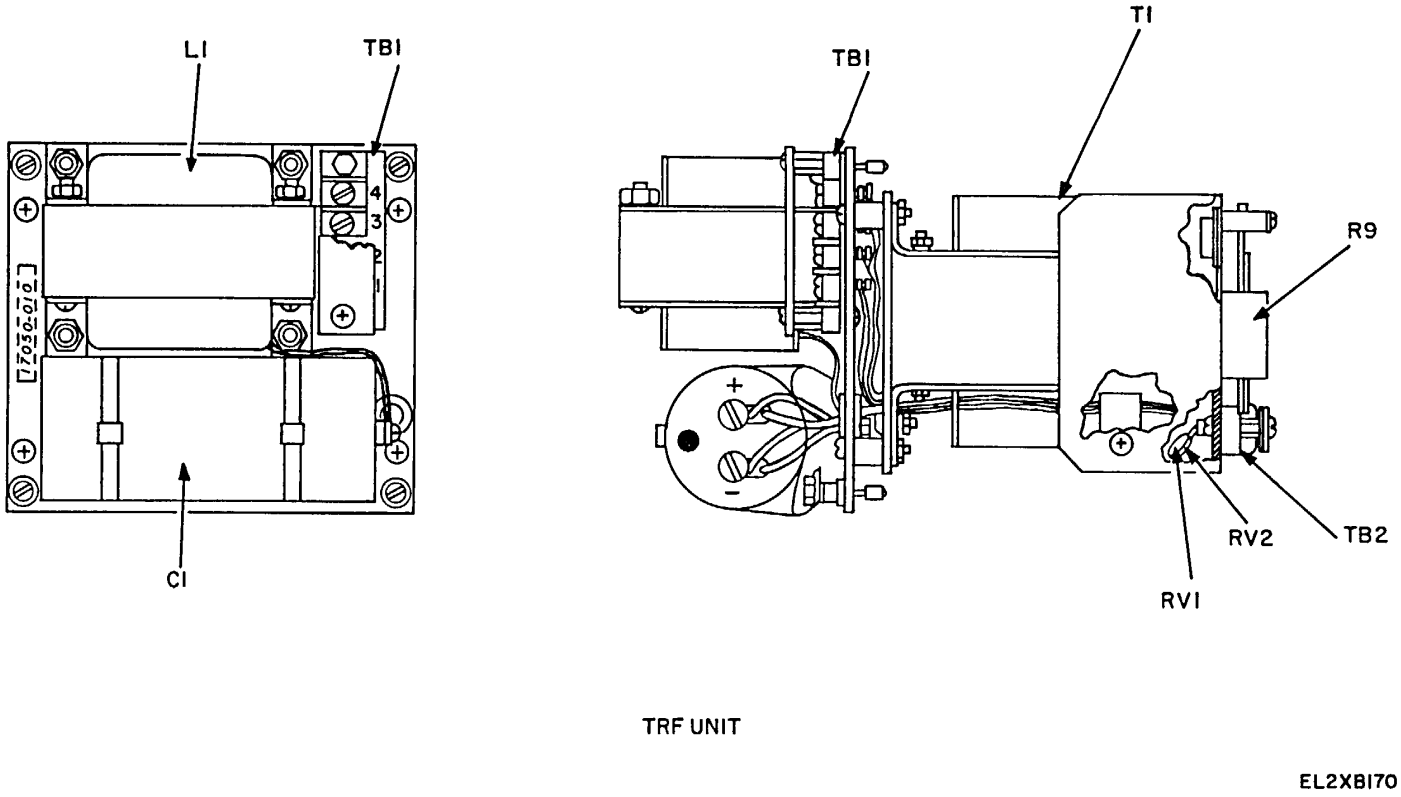


Figure 3-35. Power supply group parts location diagram (sheet 14 of 19).

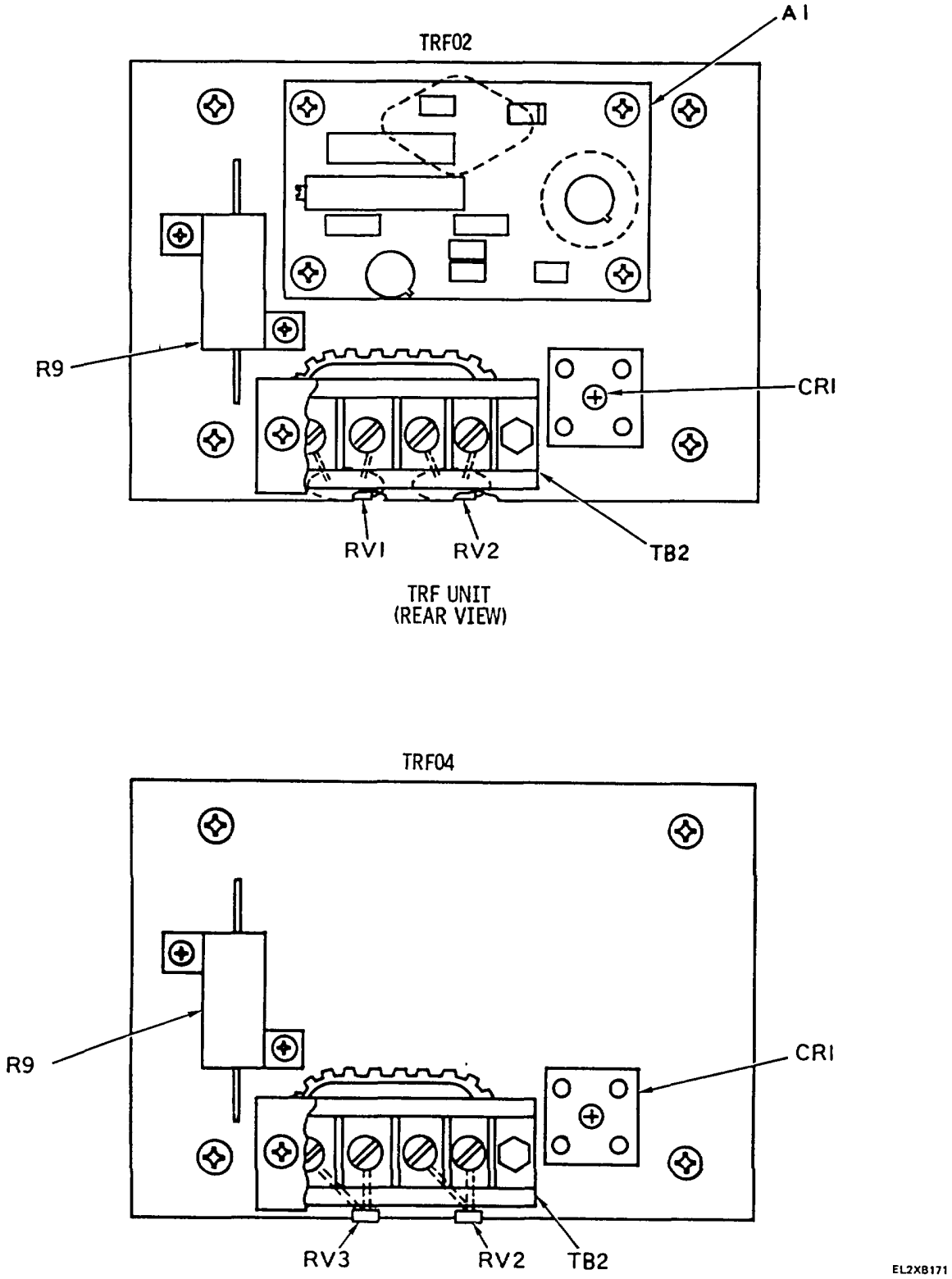


Figure 3-35. Power supply group parts location diagram (sheet 15 of 19).

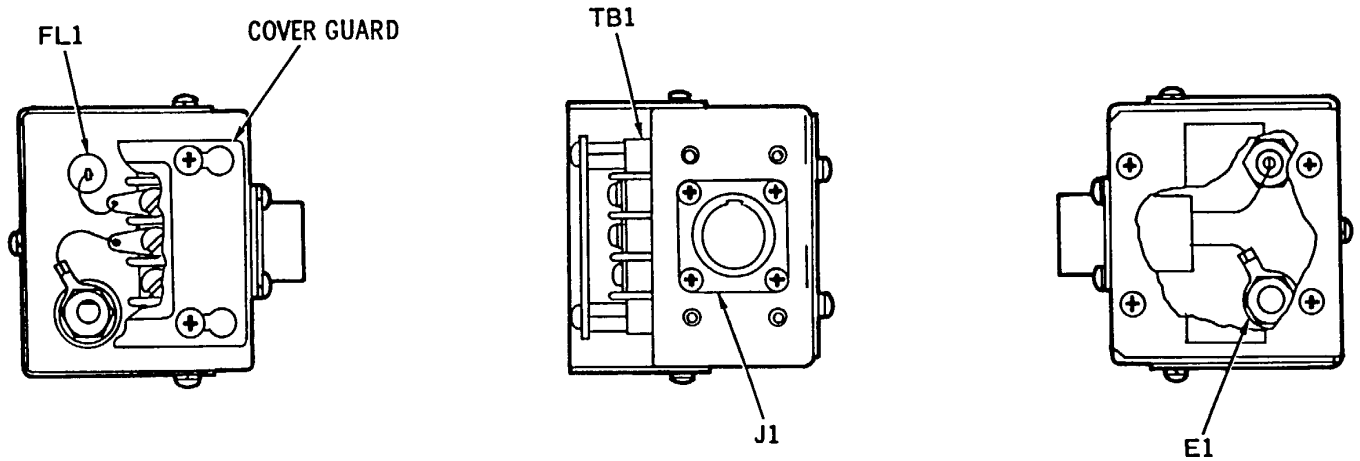


Figure 3-35. Power supply group parts location diagram (sheet 16 of 19) DCE02.

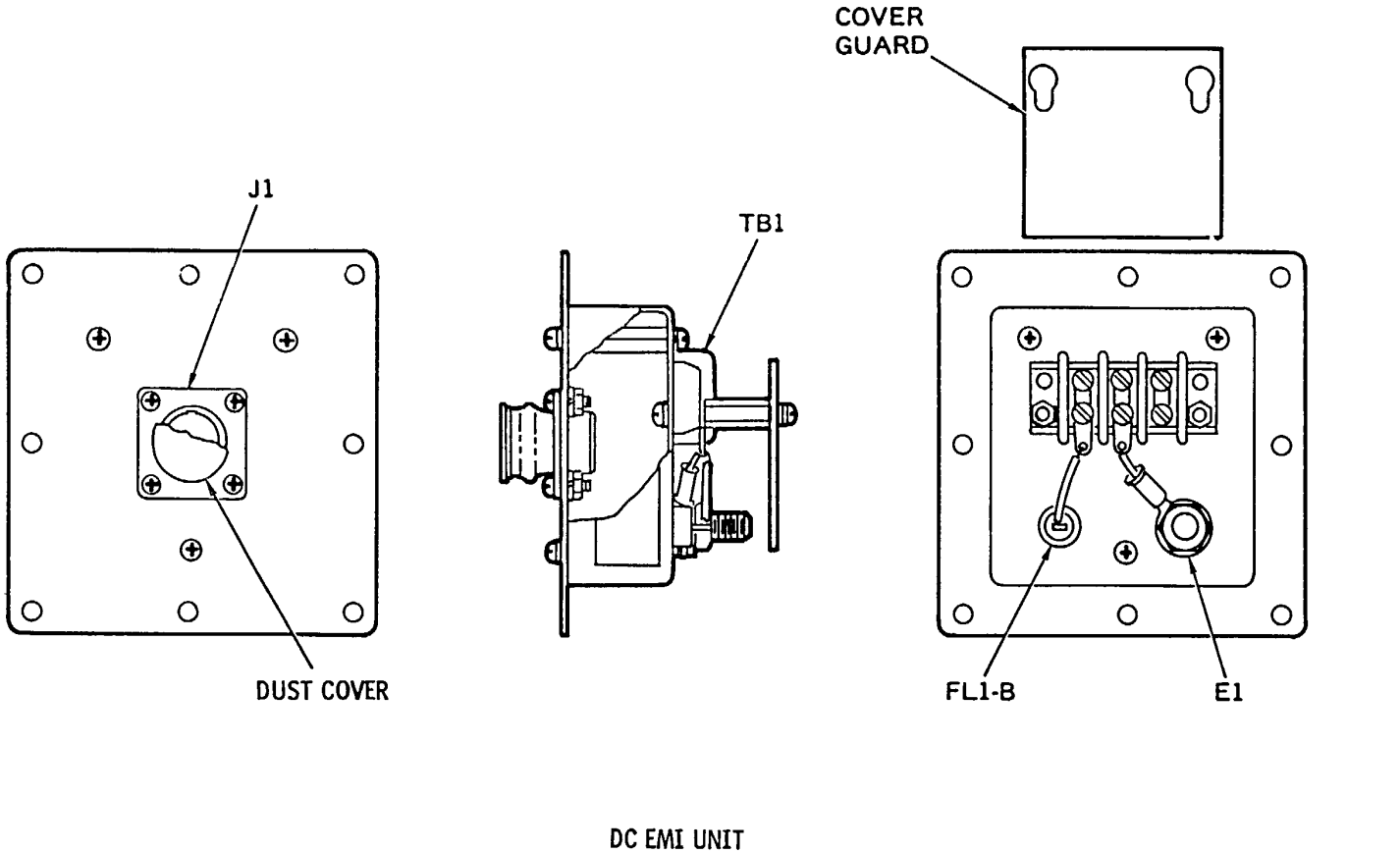


Figure 3-45. Power supply group parts location diagram (sheet 17 of 19) DCE04.

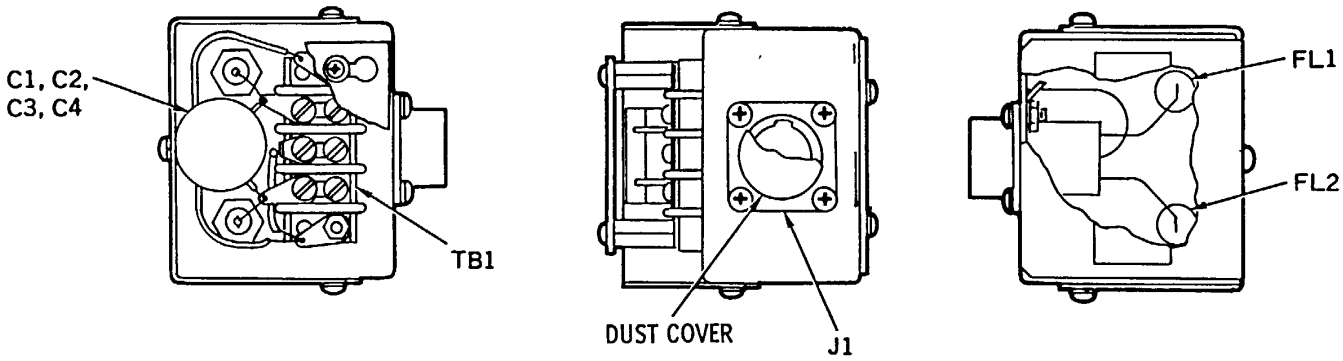


Figure 3-45. Power supply group parts location diagram (sheet 18 of 19) ACE02.

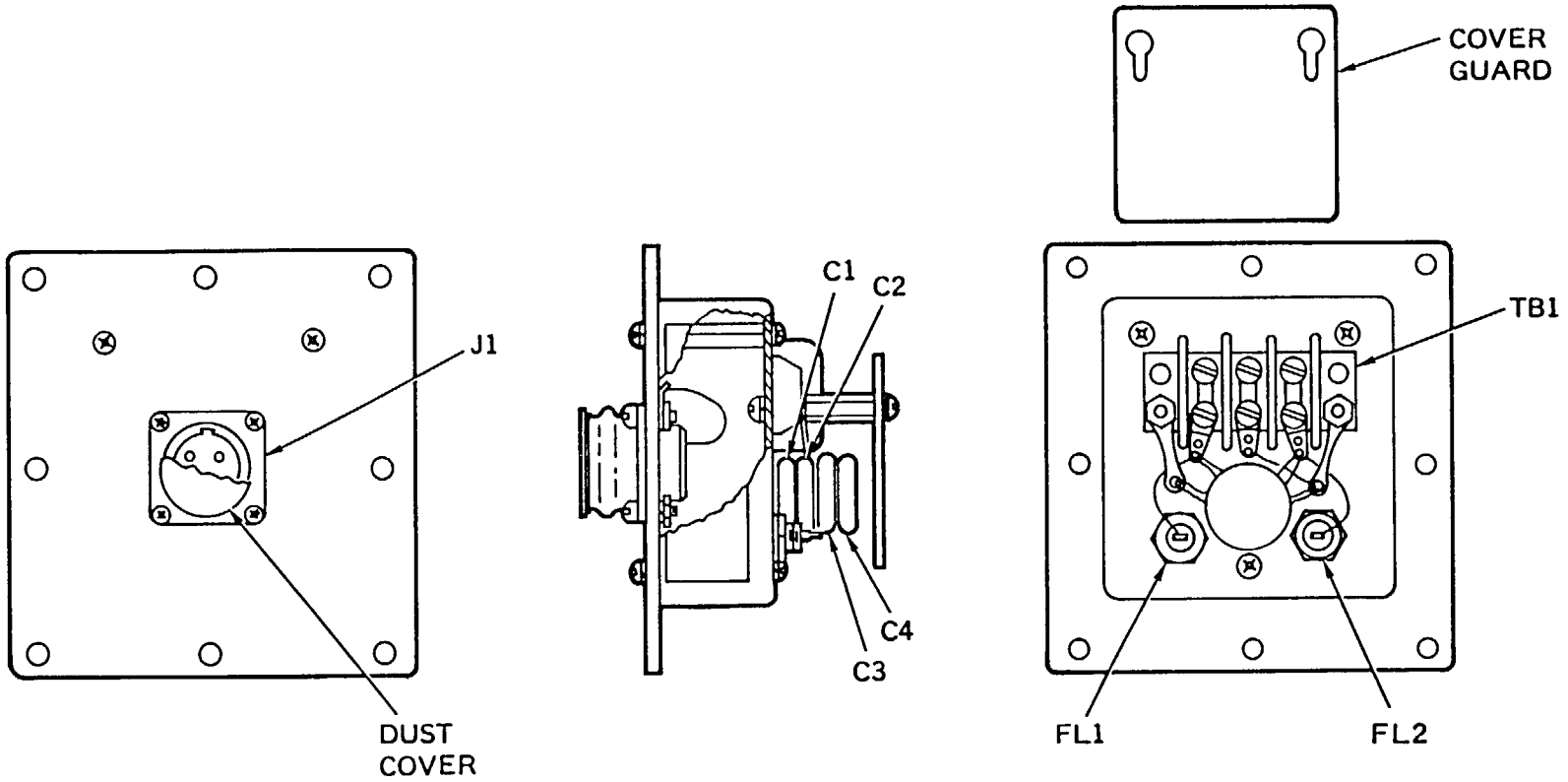


Figure 3-35. Power supply group parts location diagram (sheet 19 of 19) ACE04.

Section IV. MAINTENANCE

WARNING

Hazardous voltage will be exposed when the BITE module or the rear assembly is removed. Do not start removal procedures without first disconnecting the external power cord ant' all cables (for rear assembly).

WARNING

To be usable for cleaning, compressed air sources must limit the nozzle pressure to no more than 29 pounds per square inch gage (PSIG). Goggles must be worn at all times while cleaning with compressed air.

3-21. General

This section contains instructions and data for use in repair of faulty (repairable) modules and units of the multiplexer set. The instructions cover disassembly and reassembly, repair and replacement of modules and components, and replacement of components.

3-22. Disassembly/Reassembly of BITE

a. *Disassembly.* Refer to figure 3-36 and disassemble BITE in accordance with the following procedure:

(1) Remove four screws, nuts, flatwashers, and lockwashers securing analog circuit board to front panel.

(2) Remove three screws, nuts, flatwashers, and lockwashers securing spacers to digital circuit board.

(3) Disconnect and tag wires necessary to remove analog circuit board.

(4) Remove spacers from analog circuit board.

(5) Remove analog circuit board.

(6) Remove four screws, flatwashers, and lockwashers securing digital circuit board to brackets.

(7) Disconnect and tag wires necessary to remove digital circuit board.

(8) Remove digital circuit board.

(9) Loosen two nuts holding meter M201 screws; back screws away from front panel.

(10) Remove two screws, nuts, and meter brackets.

(11) Disconnect and tag wires to meter.

(12) Remove meter.

(13) Remove other front-panel panel controls and indicators as necessary. Tag all wires that are disconnected.

b. Reassembly of BITE. Refer to figure 3-32 for identity (reference designations) of front panel controls and indicators, figure FO-12 for wire connections, and figure 3-36 for exploded view of BITE. Following reassembly, verify performance of BITE in accordance with paragraph 3-38. Reassemble the BITE in accordance with the following procedure:

(1) Connect wires between digital circuit board and panel, matching tags.

(2) Secure digital circuit board to brackets, replacing screws, flatwashers and lockwashers.

(3) Connect wires between analog circuit board and panel, matching tags.

(4) Secure analog circuit board to front panel, replacing four screws, flatwashers and lockwashers.

(5) Attach spacers between digital circuit board and analog circuit board.

3-23. Disassembly/Reassembly of PWR SPLY Group

a. Disassembly. Disassemble the PWR SPLY group in accordance with the following procedure:

(1) Remove six screws, flatwashers, and lockwashers securing monitor and alarm board to dc converter board.

(2) Remove two screws, flatwashers, lockwashers and spacers securing outer end of monitor and alarm board to dc converter board.

(3) Remove monitor and alarm board.

(4) Remove screw, flatwasher, lockwasher, and nut securing dc converter board to front panel bracket.

(5) Remove dc converter board.

b. Reassembly of Power Supply Groups. Following reassembly of the power supply group, verify performance of the UUR in accordance with (paragraph 3-39). Reassembly procedure is as follows:

(1) Secure dc converter board to front panel bracket with screw, flatwasher, lockwasher and nut.

(2) Secure monitor and alarm board to dc converter board, using six screws, flatwashers and lockwashers.

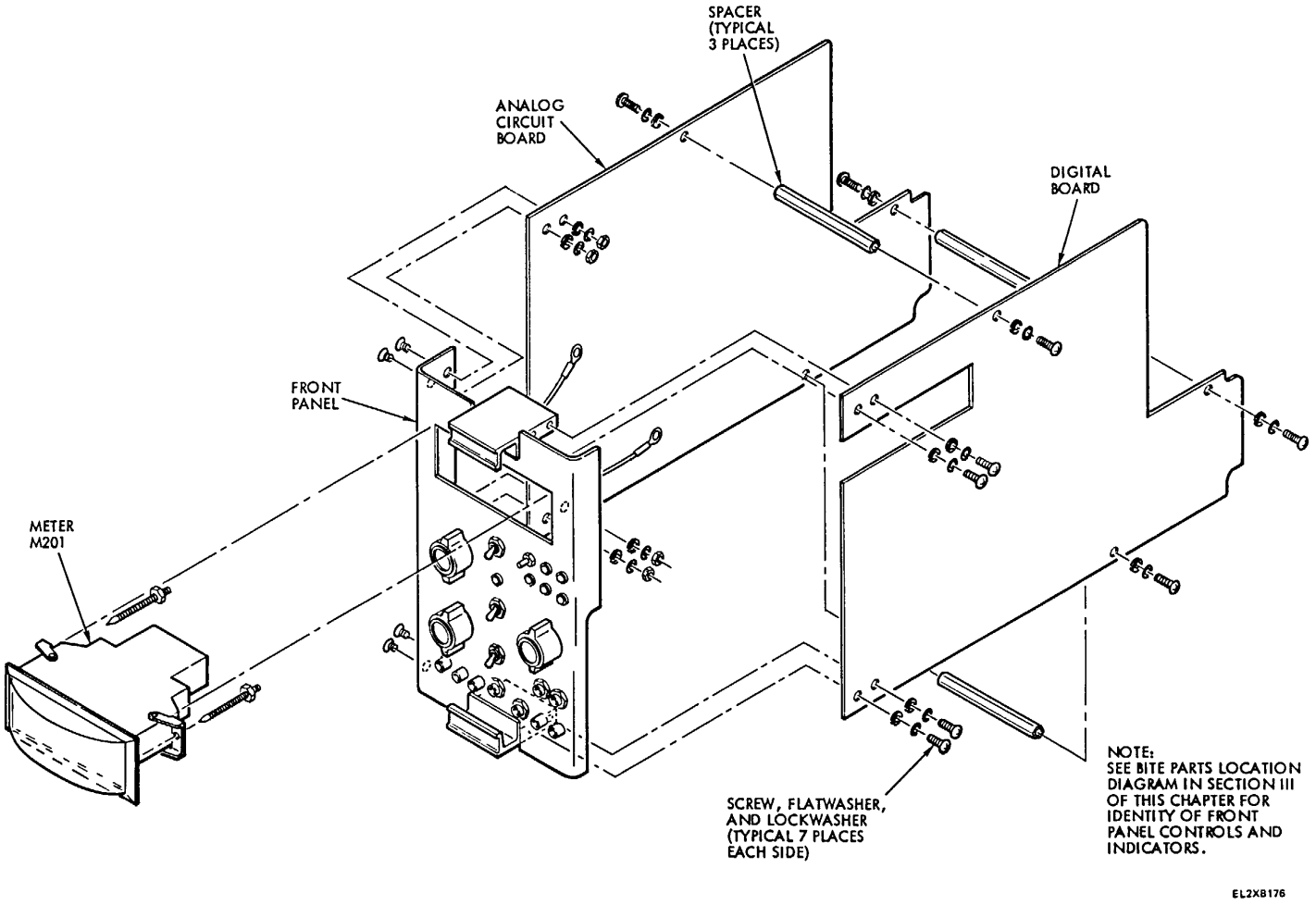


Figure 3-36. BITE assembly exploded view.

3-24. Disassembly/Reassembly of Multiplex Set Cabinet

For repair purposes at the general support level, the multiplexer set cabinet consists of a front cover, a card cage, and a rear assembly. The latter consists of a frame (backplane) on which module edge connectors are mounted, a rear cover on which the external connectors of the multiplexer are mounted and the wire harness for the set.

a. *Disassembly/Reassembly of Front Cover* (fig. 3-37). The plastic windows for the PWR SPLY alarm lamps, the LAMP TEST button assembly, and the captive thumbscrew can be removed.

(1) Replace plastic windows if they are broken or chipped. Each is held in place with a single retainer.

(2) The LAMP TEST button assembly should never require replacement, but if it does, it is held in place by one nut.

(3) If the captive thumbscrew becomes bent, it should be straightened if possible. If it breaks, it can be replaced by forcing its retainer from the door.

b. *Disassembly/Reassembly* of Card Cage (fig. 3-37). The card cage can be disassembled/reassembled to the riveted level.

(1) The four cabinet handle installations are identical. Each is held in place by two screws. Bent handles should be straightened. Broken handles, or handles with stripped or cross threads should be replaced. Secure handles are safety necessities.

(2) The four cabinet mounting bracket installations are identical. Each is secured with three screws and lockwashers. All screws must be in place and properly tightened to ensure a safe installation.

(3) The upper and lower cabinet screen installations are identical. Each is secured with 31 screws and lockwashers. Bent screens should be straightened. If they break, they should be replaced. Sound screens with all screws in place are important in controlling EMI.

(4) Cabinet shelves (card guides) and upper, lower, and side panels are riveted together and are not replaceable during cabinet repair. If any panel or shelf is bent, it should be straightened. If it cracks, the cabinet should be replaced.

c. Removal of Rear Assembly. The rear assembly can be removed as a single unit (fig. 3-38).

(1) Remove ten upper/lower attach screws securing rear cover to cabinet.

(2) Remove five side attach screws on each side of cabinet securing angles riveted to the rear cover.

(3) Remove twelve screws securing backplane to module shelf of card cage (access from front of cabinet) and slide rear assembly out of card cage.

d. Replacement of Rear Assembly. To replace the rear assembly in the cabinet:

(1) Place rear assembly into cabinet and secure with ten upper/lower attach screws on rear cover.

(2) Fasten five side attach screws securing riveted angles of rear cover to cabinet.

(3) Fasten backplane of rear assembly to module shelf of card cage with 12 screws (access from front of cabinet).

e. Disassembly of Rear Assembly. After the rear assembly has been detached from the cabinet, it can be disassembled (fig. 3-39).

(1) Remove four screws and lockwashers securing backplane to spacers.

(2) Remove six screws, lockwashers, and spacers securing three angles to backplane.

(3) Remove angles.

(4) Remove four screws and lockwashers securing two standoffs and two spacers to rear cover.

(5) Remove rear cover.

f. Reassembly of Rear Assembly. To reassemble the rear assembly, perform the following procedure (fig. 3-39).

(1) Attach rear cover to two standoffs and two spacers using four screws and lockwashers.

(2) Secure angles to backplane using six screws, lockwashers and spacers.

(3) Secure backplane to spacers using four screws and lockwashers.

(4) Verify performance of rear assembly in accordance with paragraph 3-42.

3-25. Repair and Replacement

The following subparagraphs cover standard and special replacement of components and general repair information. Special replacement procedures cover replacement of special components the values of which must be individually selected in test (SIT).

a. Removal of Components on Printed Circuit Boards. Components such as resistors and capacitors may be removed from printed circuit boards in accordance with the following procedure.

(1) Remove conformal coating from area of the component to be replaced by heating area with a heat gun.

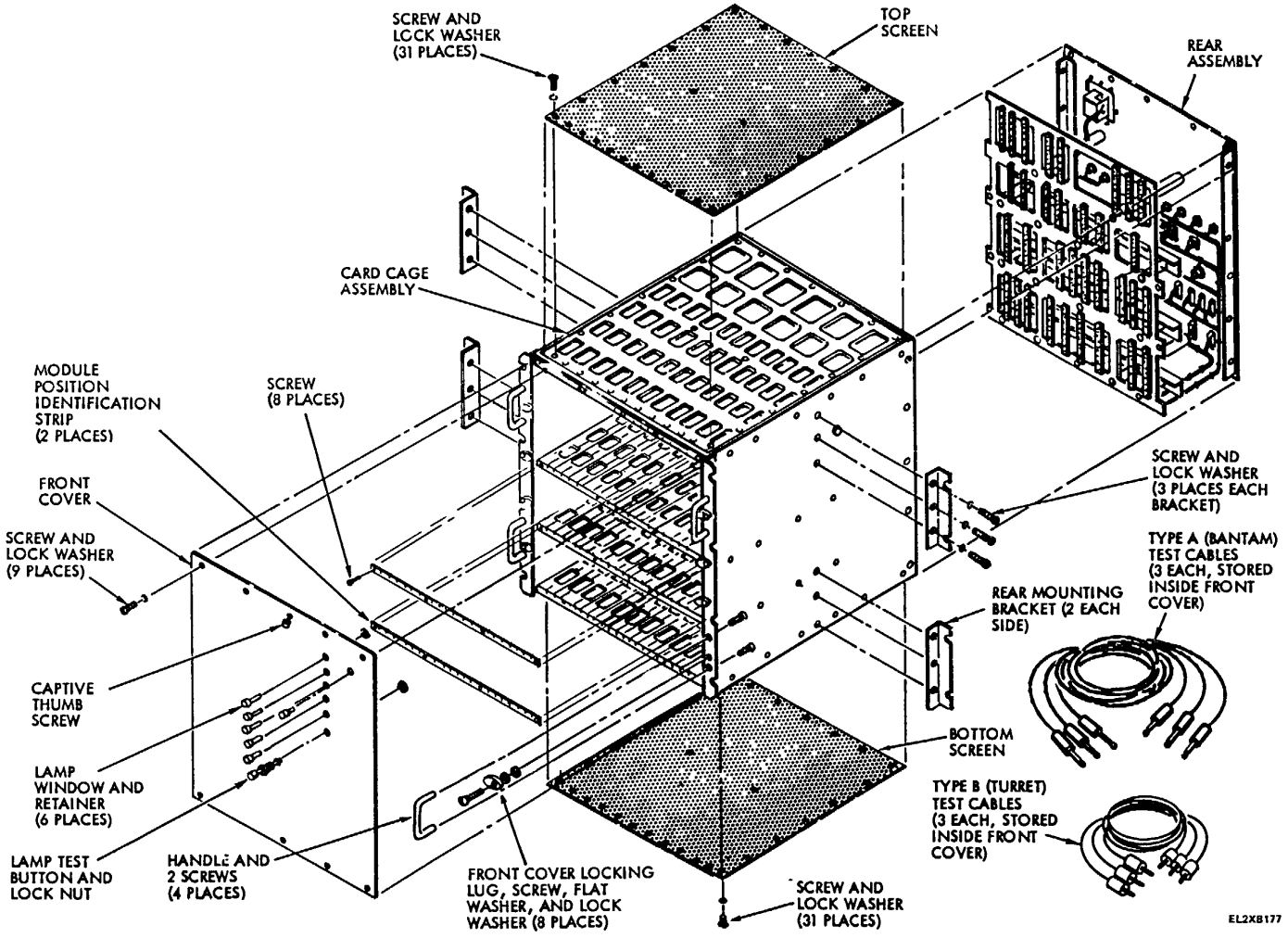


Figure 3-37. Multiplexer set cabinet, exploded view.

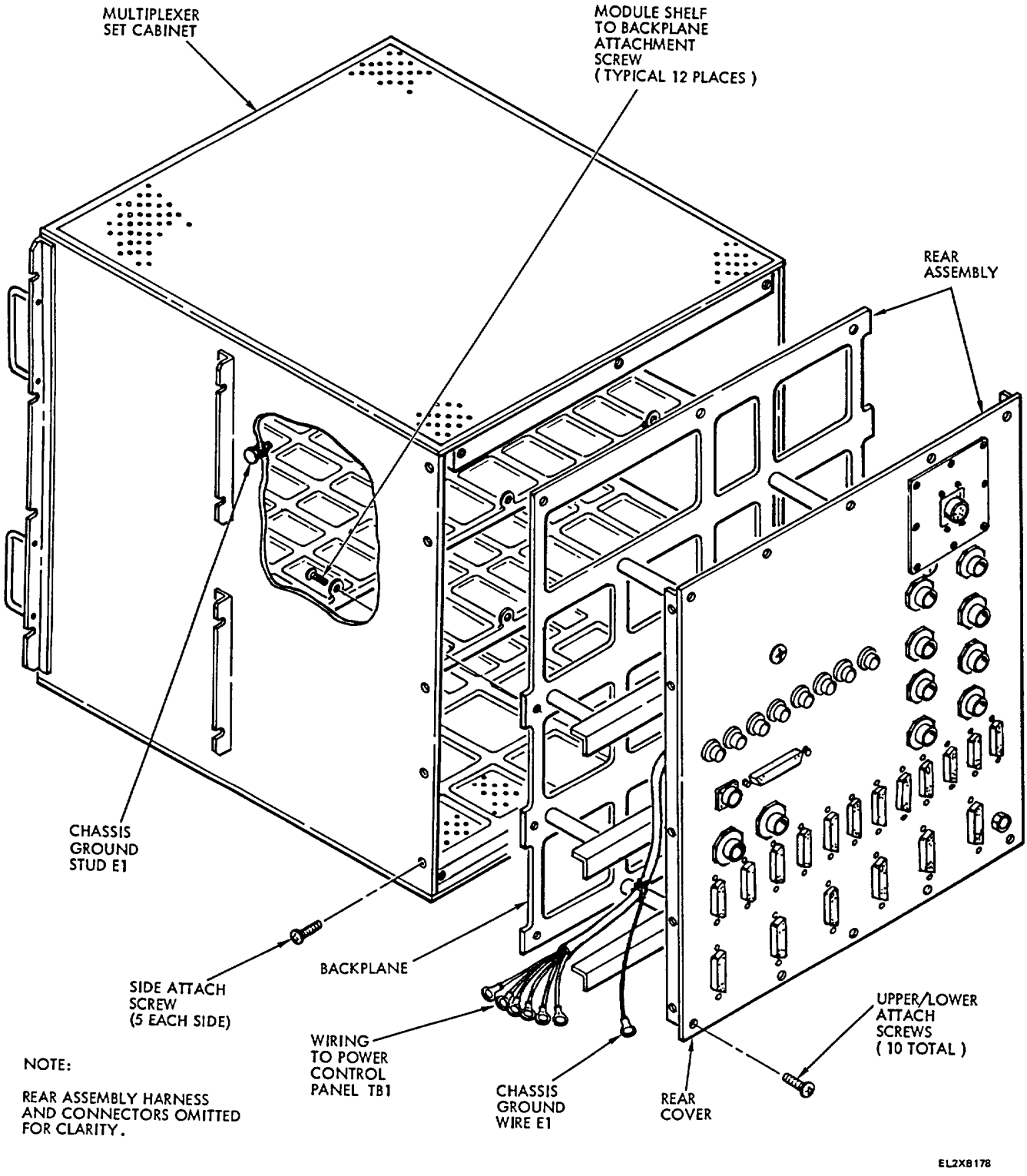


Figure 3-38. Removal/replacement of rear assembly.

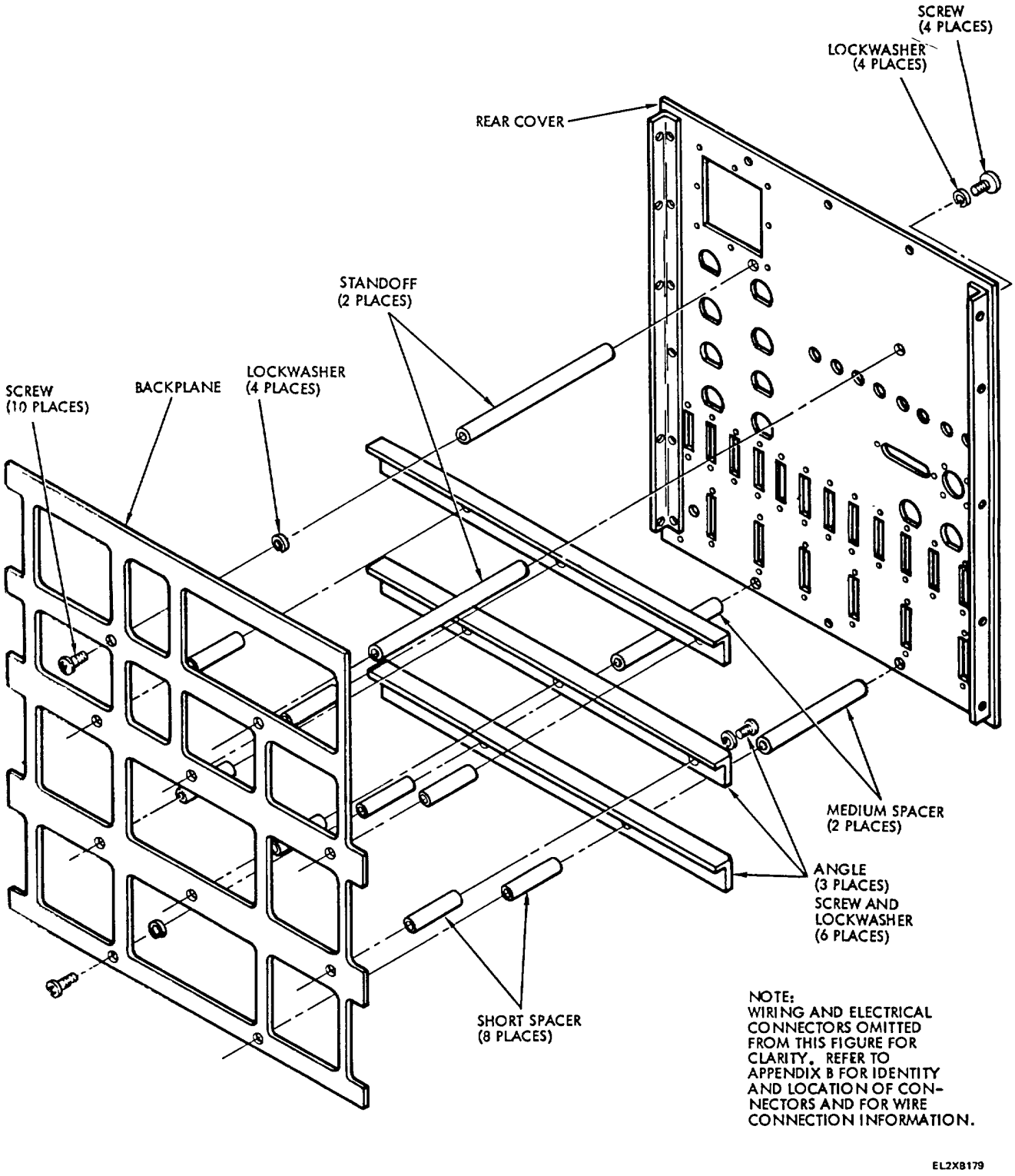


Figure 3-39. Rear assembly, exploded view.

(2) When conformal coating has softened, use an orange stick or other blunt instrument to scrape coating away from component.

(3) Clean conformal coating from pads on rear of board per paragraph 3-25a (1) and (2) above.

(4) Remove solder from plated-through holes using a vacuum solder removal system or a wicking method.

(5) Remove the component to be replaced.

(6) If the component cannot be removed after the above steps have been performed, repeat 3-25a (1) through (4) above.

b. *Replacement of Multilead Components*. Multilead components should be replaced in accordance with the following procedure.

(1) Clean conformal coating from area of component to be replaced per a(1) through (3) above.

(2) Remove solder from all plated-through holes associated with component being removed.

CAUTION

All solder must be removed from plated-through holes and leads must be free of plating. If this is not done, the plating will separate from the board material and will be removed along with the component.

(3) Remove dual in-line integrated circuits and resistor arrays by cutting the leads as close to the component body as possible.

(4) Use a heat gun to soften the conformal coating.

(5) Using an orange stock or other blunt tool, lift the component away from the board.

(6) Heat the leads from the back of the board and remove them with a pair of pliers.

(7) Form leads of new part to conform with circuit board hole pattern.

(8) Install new part into board.

(9) Solder all leads.

CAUTION

Heat sinks should be used on heat sensitive parts such as integrated circuits, transistors and diodes.

WARNING

Adequate ventilation should be provided while using trichlorotrifluoroethane, Prolonged breathing of vapor should be avoided. The solvent should not be near heat or open flame. Since trichlorotrifluoroethane dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

c. *Application of Conformal Coating*. After a component is replaced, the conformal coating must be restored to the board (per MIL-STD-275) by the following procedure:

(1) Clean the area to be recoated of all foreign matter with trichlorotrifluoroethane.

(2) Prepare conformal coating material in accordance with manufacturers instructions.

CAUTION

Mix conformal coating material in a well-ventilated area.

(3) Apply coating material to board with a small brush.

(4) Use a heat gun to cause coating material to flow under the component and form a fillet.

(5) Apply more coating material as required to fill any voids or air bubbles.

(6) Allow board to air cure until conformal coating has cured. If a curing oven is available, coating may be oven-cured. A sample of coating material should be allowed to cure as an indicator of coating quality.

(7) After one side has fully cured, repeat

(1) through (6) above for the back of the printed circuit board.

d. Repair of Damaged Circuit-Boards. Damaged circuit boards should be repaired in accordance with the following procedure:

(1) Broken conductors may be bridged with bare tinned copper wire if the distance to be bridged does not exceed 3/8 inch.

(2) If the break exceeds a/8 inch, use insulated wire or bare-tinned wire with an insulated sleeve.

(3) If the length of the wire used is greater than 1/2 inch, use epoxy resin to attach it to the board.

(4) Reattach lifted pads by removing all traces of flux and other foreign matter with trichlorotrifluoroethane.

(5) Reattach lifted pad by using epoxy resin. Do not allow epoxy resin to come in contact with the top side of the pad.

e. *Replacement of Select-In-Test (SIT) Resistors.* The BITE unit contains resistors whose original values were individually selected by testing. These select-in-test resistors are identified in the detailed schematics by the letters SIT. If they must be replaced, the new resistor should

have the same resistance, wattage and tolerance as printed on the original. However, SIT resistors may also require replacement because of other circuit value changes. In this event, determine new SIT values in accordance with the following instructions.

(1) *BITE SIT resistor R29*. To replace R29 on BITE analog board TRW 17165-010, perform the following steps:

(a) If original R29 is known to be faulty, replace it with a trial resistor of a like value. If the printed value of the faulty resistor cannot be read, use a trial resistor of 210 kilohms, I/8 watt, 1%, metal film.

(b) Install faulty BITE module into MXTF using extender board TRW 17300-010.

(c) Connect test lead between VF OSC jack on BITE and AC SIGNAL INPUT on CP-772A/U.

(d) Set CP-772A/U controls as follows:

Switch	*Position*
SENSITIVITY	2
TIME BASE	1S
FUNCTION	FREQUENCY
SAMPLE RATE	% turn clockwise.

(e) Set power switch on PWR CONT unit in MXTF to ON, and set BITE switches as follows:

Switch	*Setting*
VF FUNCTION	LOOP TEST
OSC LEVEL	0 DB
DIGITAL FUNCTION	CLK RATE 20 Kb/S/

(f) If CP-772A/U indicates a frequency of less than 1000 Hz, replace trial resistor with resistor having 5 kilohms of increased resistance, and proceed to (h) below.

(g) If CP-772A/U indicates a frequency of more than 1040 Hz, replace trial resistor with resistor having 5 kilohms less resistance, and proceed to (h) below.

(h) Repeat (f) and (g) above until CP-772A/U indicates a frequency of 1020 +20 Hz, which indicates that value of R29 is satisfactory.

(2) *BITE SIT resistor R56*. To replace R56 of BITE analog board TRW 17165/010, perform the following steps:

(a) If original R56 is known to be faulty, replace it with a trial resistor of like value. If the printed value of the faulty resistor cannot be read, use a trial resistor of 46.4 kilohms, Y8 watt, 1%, metal film.

(b) Install faulty BITE module into MXTF using extender board TRW 17300-010.

(c) Connect type G test cable between VF OSC jack on BITE and INPUT 310 jack on TA-855/U.

(d) Set TA-855/U switches as follows:

Switch	*Position*
RESPONSE	DAMP
NOISE WTG	C-MSG
INPUT TMS	TERM
RANGE	0 dBm
FUNCTION	600 BAL
POWER	ON

(e) Set MXTF controls as follows:

Unit	*Switch*	*Position*
BITE	VF FUNCTION	LOOP TEST
BITE	OSC LEVEL	0 DB
BITE	DIGITAL FUNCTION	CLK RATE 20 Kb/S.
PWR CONT	Power	ON

(f) If TA-855/U indicates a reading of less than -0.1 dBm, replace trial resistor with new resistor having 1 kilohm of increased resistance, and proceed to (It) below.

(g) If TA-855/U indicates a reading of more than +0.2 dBm, replace trial resistor with resistor having 1 kilohm less resistance, and proceed to (h) below.

(h) If TA-855/U indicates a reading of 0 ±0.1 dBm, value of R56 is satisfactory.

(3) BITE SIT resistor R34. To replace resistor R34 on BITE analog board TRW 17165-010, perform the following steps:

(a) If R34 is known to be faulty, replace it with trial resistor of like value. If the printed value of the faulty resistor cannot be read, use a trial resistor of 732 kilohms, V8 watt, 1% metal film.

(b) Install faulty BITE module into MXTF using extender board TRW 17300-010.

(c) Connect type A test cable between VF OSC and VF METER jacks on BITE.

(d) Set MXTF controls as follows:

Unit	*Switch*	*Position*
BITE	VF FUNCTION	COM GAIN XMT
BITE	OSC LEVEL	0 DB
BITE	METER ATTEN	10 DB
PWR CONT	Power	ON

(e) If BITE meter reading is less than -0.1 dBm, replace trial resistor with new resistor having 15 kilohms of increased resistance, and proceed to (g) below.

(f) If BITE meter reading is greater than +0.1 dBm, replace trial resistor with a resistor having 15 kilohms less resistance, and proceed to (g) below.

(g) If BITE meter reading is 0 -+0.1 dBm, value of R34 is satisfactory.

f. Replacement of VF Module Inductors. The following instructions and data are for use in aligning inductors L1, L2, L3, and L4 on faulty VF modules after replacement of one or more inductors. Refer to figure FO-8.

(1) Tools and test equipment.

(a) TK-100/G.

(b) AN/USM-281C.

(c) CP-772A/U.

(d) Type K test cable.

(e) TS-3329/U.

(2) Initial setup. Set up test equipment and faulty VF module to effect replacement as follows:

(a) Connect test equipment as shown in figure 3-40.

(b) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
AN/USM-281C	VOLTS/DIV (left)	1V
	TIME/DIV	2ms
	TRIG	LEFT
POWER	ON	
TS-3329/U	FREQUENCY RANGE	X100
	FREQUENCY Hz	44.2
	FUNCTION	600
	OUTPUT LEVEL	-3dbm
	POWER	ON
CP-772A/U	TIME BASE	1 sec
	SAMPLE RATE	MIN
	POWER	ON

(3) Alignment instructions for L1 and L2. Proceed in accordance with the following:

(a) Adjust the output frequency of TS-3329/U for a reading of 4420 Hz -±-10 Hz on CP-772A/U.

(b) Connect the TS-3329/U TIP binding post output to the junction of R8 and the collector of Q1.

(c) Connect AN/USM-281C input to the junctions of CR1 and CR3.

(d) Adjust the slug of L1 for a minimum signal (null) on AN/USM-281C.

(e) Adjust the output frequency of TS-3329/U for a reading of 6420 Hz ±10 Hz.

(f) Adjust the slug of L2 for a minimum signal (null) on AN/USM-281C.

(4) *Alignment instructions for L3 and L4.* Proceed in accordance with the following:

(a) Adjust the output frequency of TS-3329/U for a reading of 4420 Hz -+10 Hz on CP-772A/U.

(b) Connect TS-3329/U TIP binding post output to the junction of L4 and C26.

(c) Connect AN/USM-281C input to the base of Q4.

(d) Adjust the slug of L3 for a minimum signal (null) on AN/USM-281C.

(e) Adjust the output frequency of TS-3329/U for a reading of 6420 Hz +10 Hz.

(f) Adjust the slug of L4 for a minimum signal (null) on AN/USM-281C.

g. Component Location. Location of electrical/ electronic parts are shown on the parts location diagrams accompanying each troubleshooting procedure in section III.

h. Backplane Wiring Repairs. When repairing wire wrap connections on the backplane assembly, proceed in accordance with the following procedures.

(1) Disassemble and spread rear assembly open far enough to provide access to wiring that is to be repaired. (Refer to paragraph 3-24.)

(2) Use wire list in appendix B to locate both ends of defective wire.

(3) With a 24-gage unwrapping tool, remove both ends of wire.

(4) Wrap new wire using a hand wrapping tool or a wire wrap gun with a 24-gage bit.

(5) If wire to be replaced is a part of a twisted pair, replace both conductors.

NOTE

If a wire is unwrapped, it may not be straightened and rewrapped. If the length of the wire is sufficient, the bare wire may be cut off and the wire stripped and rewrapped.

Section V. GENERAL SUPPORT TESTING

3-26. General

This section contains procedures for conducting performance tests on repaired modules/units of the multiplexer set to determine if they are satisfactory for return to users. A stand-alone test is provided for each module/unit and identifies necessary test equipment, test setups, and test instructions. The procedural steps must be accomplished in the order given, and all controls must be set accurately (para 3-2). Refer to tables

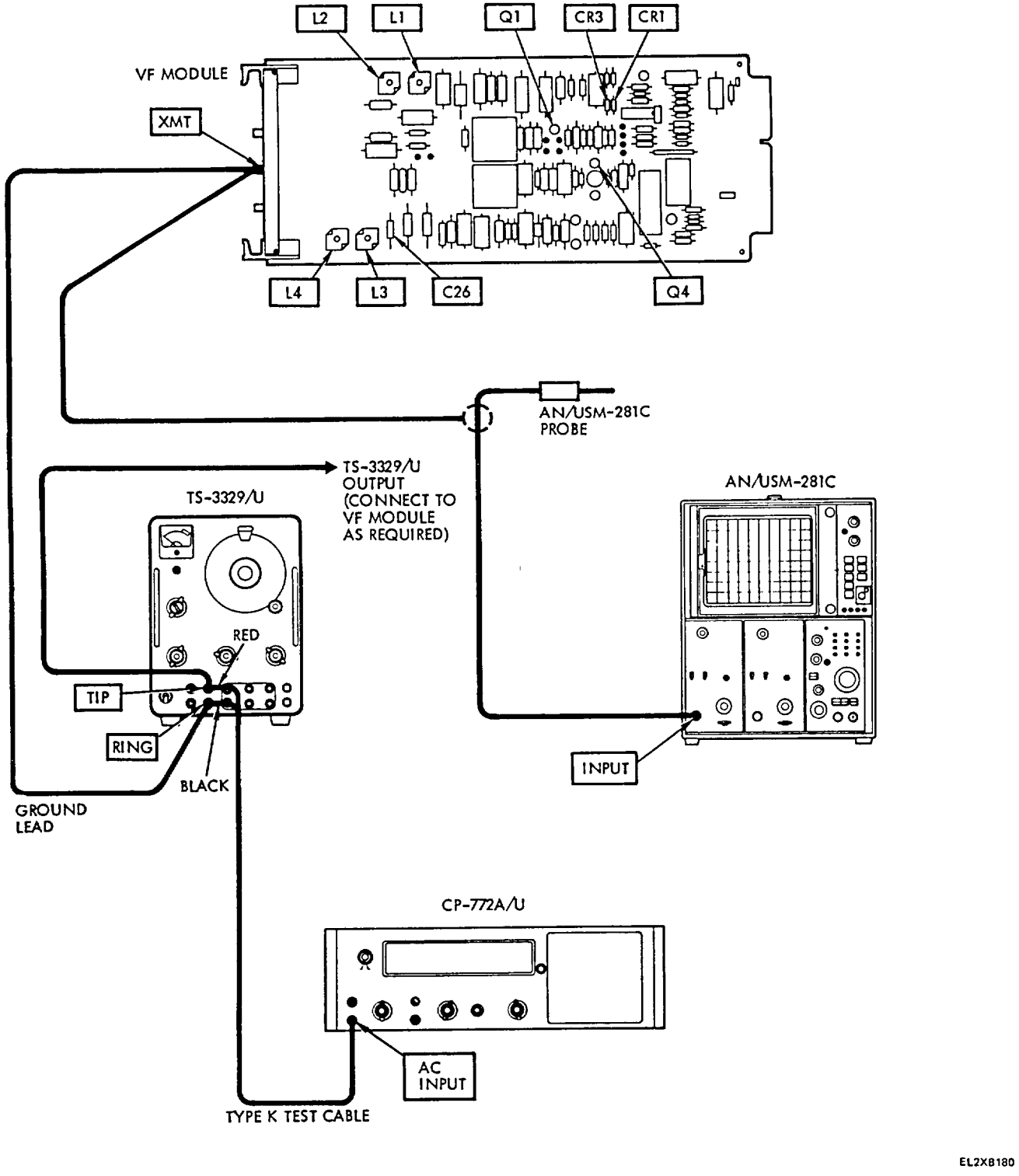


Figure 3-40. Setup diagram for alignment of VF module inductors.

3-1 and 3-2 for general support test equipment. If modules/units do not successfully pass test, refer to troubleshooting procedures, section III.

3-27. Testing Data Timing Group

Instructions for testing the performance of individual DTG units are provided in the following paragraphs.

3-28. Testing PCM Unit

This test will verify that the PCD unit will decode PCM data and distribute the resulting analog information to the channel modules. Successful completion of the test qualifies the unit for return to users.

a. *Test Equipment*.

(1) AN/USM-281C.

(2) TIMS.

(3) MXTF with the following accessories:

Type A test cables (2)
Type C test cables (2)
Type G test cables (2)
Spare VF module.

b. *Initial Equipment Setup*.

(1) Set switch on MXTF PWR CONT to OFF.

(2) Remove MXTF PCM unit and install UUR.

(3) Install spare VF module in the channel 1 location of the MXTF.

(4) Strap MXTF RCVR and DRIVER units for 24-channel NRZ operation (table 3-4).

(5) Connect type A test cable between BITE VF METER jack and lower RCV jack on VF module.

(6) Connect type A test cable between BITE VF OSC jack and lower XMT jack on VF module.

(7) Set test equipment controls as follows:

Unit	*Switch*	*Setting*
TIMS	DISPLAY CONNECTED TO	TRMT
	MEASUREMENT	NOISE-WITH-TONE
	NOISE FILTER	C-MSG
	POWER	ON
	SETUP CONTROLS	NORMAL TEST TEST WITHOUT HOLD TALK BATTERY OFF TERM 600 NO SF SKIP NORMAL TEST
	RECEIVE/TRANSMIT JACK switch	Down position
MXTF (BITE) OSC LEV	Set for VF module strapping indicated	VF module strapping A strap in -16 DB B strap in ODB
	METER ATTEN	VF module strapping
	Set for VF module strapping indicated	C strap in 0 dBm C strap out 10 dBm
	ON HOOK/OFF HOOK	ON

NOTE

Allow equipment to warm up for 5 minutes before proceeding with the test.

c. Test Procedures. Verify performance of the UUR in accordance with the following procedure.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
1	MXTF (RCVR) LOOP-NORMAL:	LOOP	Check input filter functions.	
			a. Perform DTG common VF gain adjustment and channel level gain procedures in TM 11-5805-711-13.	a. None.
			b. Verify BITE meter reading for VF module strapped as indicated.	b. **VF module strapping / BITE VF meter reading** C strap in 0±0.5 dBm C strap out +7 ±0.5 dBm
			c. Move VF module to progressively higher channels repeating step b above until all channels have been checked.	c. None.
2			Check the ODD and EVEN GROUP A TO D CONVERTER circuits.	

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
			ODD GROUP:	
			a. Set TIMS OSC level for VF module strap as indicated.	*a.* VF module TIMS Strapping OSC LEV A strap in -16 dBm B strap in 0 dBm
	TIMS DISPLAY CONNECTED TO:	RCV	*b.* Install spare VF module in channel 1 location of MXTF.	*b.* None.
			c. Connect TIMS 310 TRMT jack to lower XMT jack of VF module using type G cable.	*c.* None.
			d. Connect TIMS 310 RCV jack to lower RCV jack of VF module using type G cable.	*d.* None.
			e. Record TIMS display.	*e.* None.
	MEASUREMENT: MESSAGE CIRCUIT NOISE		*f.* Record new TIMS display reading and subtract from number recorded in e above.	*f.* Ž32 dB.
			EVEN GROUP:	
			g. Move VF module to channel 2 and repeat e and f above for EVEN GROUP A TO D CONVERTER circuit.	*g.* None.
3	MXTF (RCVR)		Check SIGNALING CONTROL circuit.	
	LOOP-NORMAL: NORMAL		*a.* Connect type C test cable between MBS RCV DATA and MBS XMT DATA connectors on rear of MXTF.	*a.* None.
			b. Connect type C test cable between MBS RCV CLK and MBS XMT clock connector on rear of MXTF.	*b.* None
			c. Install VF module in channel 1 location of MXTF.	*c.* None.
	MXTF (BITE) ON HOOK/ OFF HOOK:	ON HOOK	*d.* Connect BITE SIG jack to VF module SIG jack using a type A cable. Observe BITE OFF HOOK lamp.	*d.* Lamp out.
	ON HOOK/ OFF HOOK:	OFF HOOK	*e.* Observe BITE OFF HOOK lamp.	*e.* Lamp illuminates.
4			Check FAULT MONITOR circuit by pressing FAULT TEST switch on UUR. Observe the following lamp conditions: Unit — Lamp UUR — FAULT ALL FAULT TEST PWR SPLY — FAULT	Lamps illuminate.

3-29. Testing MUX Unit

This test will verify that the MUX unit will address each channel module, generate frame bits, and interleave framing, encoded voice and data. Zero suppression will also be checked in the 24-channel bipolar mode. Successful completion of the test qualifies the unit for return to users.

a. Test Equipment.

(1) AN/USM-281C.
(2) Checktran.
(3) CP-7772A/U.
(4) MXTF with the following accessories:
Extender board TRW 17332-010
Type A test cables (2)

Type C test cables (2)
Type L test cable
Type J test cable
Spare VF module
Spare 0-20 kb/s data module.

b. Initial Equipment Setup. Set up test equipment and repaired MUX unit as follows:

(1) Set power switch on PWR CONT unit to OFF.

(2) Remove MUX unit from MXTF and install UUR in its place.

(3) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
Checktran	PATTERN	ASYNC
	PR CODE	2047
	SYNC	AUTO
	EXT CLK	PUSH
	DATA RATE	764082
MXTF (PWR CONT)	Power	OFF
MXTF (RCVR)	LOOP-NORMAL	NORMAL
CP-772A/U	TIME BASE	1 s
	SAMPLE RATE	Rotate h turn clockwise
	FUNCTION	MANUAL START
	SENSITIVITY	1
AN/USM-281C	VOLTS/DIV (left and right)	2V
	AC/GND/DC	DC
	TIME/DIV	5 ms
	TRIG SOURCE	LEFT

(3) Verify RCVR and DRIVER units are strapped for 24-channel operation (table 3-4).

(4) Install spare VF module in channel 1 position of MXTF.

(5) Install spare 0-20 kb/s in channel 2 position.

(6) Connect type C cable between MBS RCV DATA and MBS XMT DATA connectors on rear of MXTF.

(7) Connect type C test cable between MBS RCV CLK and MBS XMT CLK connector on rear of MXTF.

(8) On front of MXTF, connect VF OSC jack on BITE to lower XMT jack on VF module using type A cable. Connect VF METER jack on BITE to lower RCV jack on VF module with type A cable.

(9) Connect Checktran, using type L test cable, to channel 2 data connector on rear of MXTF.

(10) Connect AC INPUT of AN/USM-281C to FRM ERR MON connector on rear of MXTF.

(11) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
MXTF (BITE)	VF FUNCTION	LOOP TEST
	DIGITAL FUNCTION	CLK RATE 20 Kb/S
	METER	
	ATTEN	*VF module strapping*
	OSC LEVEL	C strap in 0 dBm
		C strap out 10 dBm
		Vf module strapping
		B strap in 0 dBm
		A strap in -16 dBm
MXTF (PWR CONT)	Power	ON
AN/USM-281C	POWER	Pull
CHECKTRAN	Power	On

NOTE

Allow equipment to warm up for 5 minutes before proceeding with test.

c. Test Procedure. Verify performance of the UUR in accordance with the following procedure. Performance Standard

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
1			Verify operation of frame bit generator and DATA/VOICE/FRAME MUX circuit.	
	AN/USM-*281C*		*a.* Check frame pattern signal at FR BIT PATT test point on UUR.	*a.* Waveform A.
	TIME/DIV: 10 µs		*b.* Check XMT MBS DATA signal at XMT MBS DATA test point on UUR.	*b.* Waveform B.
			c. Remove type C cable from MBS RCV DATA connector on rear of MXTF. Adjust CP-772A/U SENSITIVITY control until counter counts continuously. Reconnect type C cable to MBS RCV DATA connector on rear of MXTF and verify that CP-772A/U stops counting.	*c.* None.
			d. Press CP-772A/U RESET button. Allow 5 minutes for errors to accumulate.	*d.* No errors in 5 minutes.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
			e. Restrap MXTF for 3-, 6- and 12-channel operation (table 3-4), repeating d above for each mode of operation.	*e.* No errors in 5 minutes.
			f. Restrap MXTF for 24-channel operation (table 3-4).	*f.* None.
2			Verify CHANNEL COUNTER and VF inter-leaving function.	
			a. Check output of VF module in channel 1 for strapping indicated using BITE meter.	*a.* **VF module strapping BITE** C strap in 0 dBm +1 C strap out +7 dBm
			b. Remove 0-20 kb/s data module.	*b.* None.
			c. Move VF module to progressively higher channels, repeating a above until all 24 channels have been checked.	*c.* Same as a above.
			d. Move VF module to channel 1.	*d.* None.
3			Verify data interleaving functions.	
			a. Install 0-20 kb/s data module in channel 2.	*a.* None.
			b. Press Checktran RESET switch and allow 15 minutes for errors to accumulate.	*b.* No errors in 15 minutes.
4	*CF-772A/U* SENSITIVITY: FUNCTION:	1 FRE-QUENCY	Verify 1 klHz digital tone generator operation. *a.* Connect CP-772A/U AC input jack to lower RCV jack on VF module in channel 1, using type J cable.	*a.* None.
	UUR 1 KHZ TONE:	ON for step	*b.* Check 1 kHz frequency.	*b.* 1000 Hz ±10 Hz.
	AN/US.M-281C TTME/DTV:	2 ms	*c.* Disconnect cable from CP-772A/U AC input jack and connect to AN/USM-281C left INPUT jack. Check 1 kHz signal for distortion.	*c.* Waveform C.
	UUR 1 KHTZ TONE:	ON for step	*d.* Connect lower RCV jack on VF module in channel 1 to BITE VP METER jack using type A cable. Check 1 kHz level for VF module strapping indicated.	*d.* **VF module strapping BITE** C strap in 0 dBm ±1 dBm C strap Out +7 dBm ±1 dBm
5			Verify ZERO SUPPRESS circuit.	
			a. Remove PCM module from MXTF.	*a.* None.
			b. Remove UUR and install on extender board. Install jumper from P3-3A to P3-12A on UUR.	*b.* None.
	AN/USM-281C TRIG SOURCE:	RIGHT	*e.* Connect right probe of AN/USM-281C to FR-12 test point on UUR.	*c.* None.
			d. Restrap DRIVER and RCVR units for 24-channel bipolar zero suppressor operation (table 3-4).	*d.* None.
	TIME/DIV:	10 µs	*e.* Check zero suppressor output signal at MBS XMT DATA test point.	*e.* Waveform D.
6			Verify OGA circuits.	
			a. Restrap DRIVER and RCVR units, for 24-channel NRZ, B2 = 0 operation (table 3-4).	*a.* None.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
			b. Remove jumper installed in 5b above.	*b*. None.
			c. Replace PCM unit.	*c*. None.
			d. Remove type C cable at MBS XMT CLK connector on rear of MXTF. Observe the following lamp conditions:	*d*. Lamps illuminate.
			Unit **Lamp** RCVR INPUT LOSS DEMUX FRAME LOSS PWR SPLY C.G.A. REMOTE ALARM	
	AN/USM-281C		*e*. Check B2 = 0 OGA output at XMT MBS DATA test point on UUR.	*e*. Waveform E.
	TIME/DIV:	5 µs	*f*. Restrap DRIVER unit for B2 = 0 + 00001111 (table 3-4).	*f*. None.
			g. Check B2 = 0 + 00001111 OGA pattern at XMT MBS DATA test point on UUR.	*g*. Waveform F.
7			Verify activity monitor operation as follows:	
			a Reconnect type C cable to MBS XMT CLK.	*a*. None.
			b. Check operation of fault monitor. Press FAULT TEST switch and observe condition of FAULT and ALL FAULT TEST lamps on UUR.	*b*. Lamps illuminate.

3-30. Testing the DRIVER Unit

This test will verify the ability of the DRIVER unit to transmit MBS data in NRZ or bipolar modes, generate clock for the DTG and transmit NRZ BIPOLAR CLOCK. Successful completion of the test qualifies the unit for return to users.

a. Test Equipment.

(1) AN/USM-281C.

(2) CP-772A/U.

(3) Wavetek 142.

(4) MXTF with the following accessories:

Extender board TRW 17332-010
Type A test cables (3)
Type B test cable
Type C test cables (2)
Type N test cables (2).

b. Initial Equipment Setup.

(1) Set power switch on MXTF PWR CONT to OFF.

(2) Using extender board, install UUR in place of MXTF DRIVER unit.

(3) Strap UUR and RCVR unit for 3-channel operation (table 3-4).

(4) Set test equipment controls as follows:

Unit	*Control*	*Setting*
AN/USM-281C	TIME/DIV	5 us
	VOLTS/DIV (left and right)	2V
	VERT MODE	LEFT
	TRIG SOURCE	LEFT
	MODE	AUTO
	COUPLING	DC
	SOURCE	INT
	AC/GND/DC	DC
	FREQ Hz	1M
WAVETEK 142	FUNCTION	L
	30 V P-P MAX	FULLY CCW
	DC OFFSET	OFF
	OUTPUT ATTEN (dB)	-10
	Frequency	1.544 MHz
	VERNIER	CAL
CP-772A/U	SAMPLE RATE	Rotate % turn clockwise
	FUNCTION	FREQUENCY
	TIME BASE	1 s

NOTE

Allow equipment to warm up for 5 minutes before proceeding with test.

c. Test Procedure. Verify performance of the UUR in accordance with the following procedure.

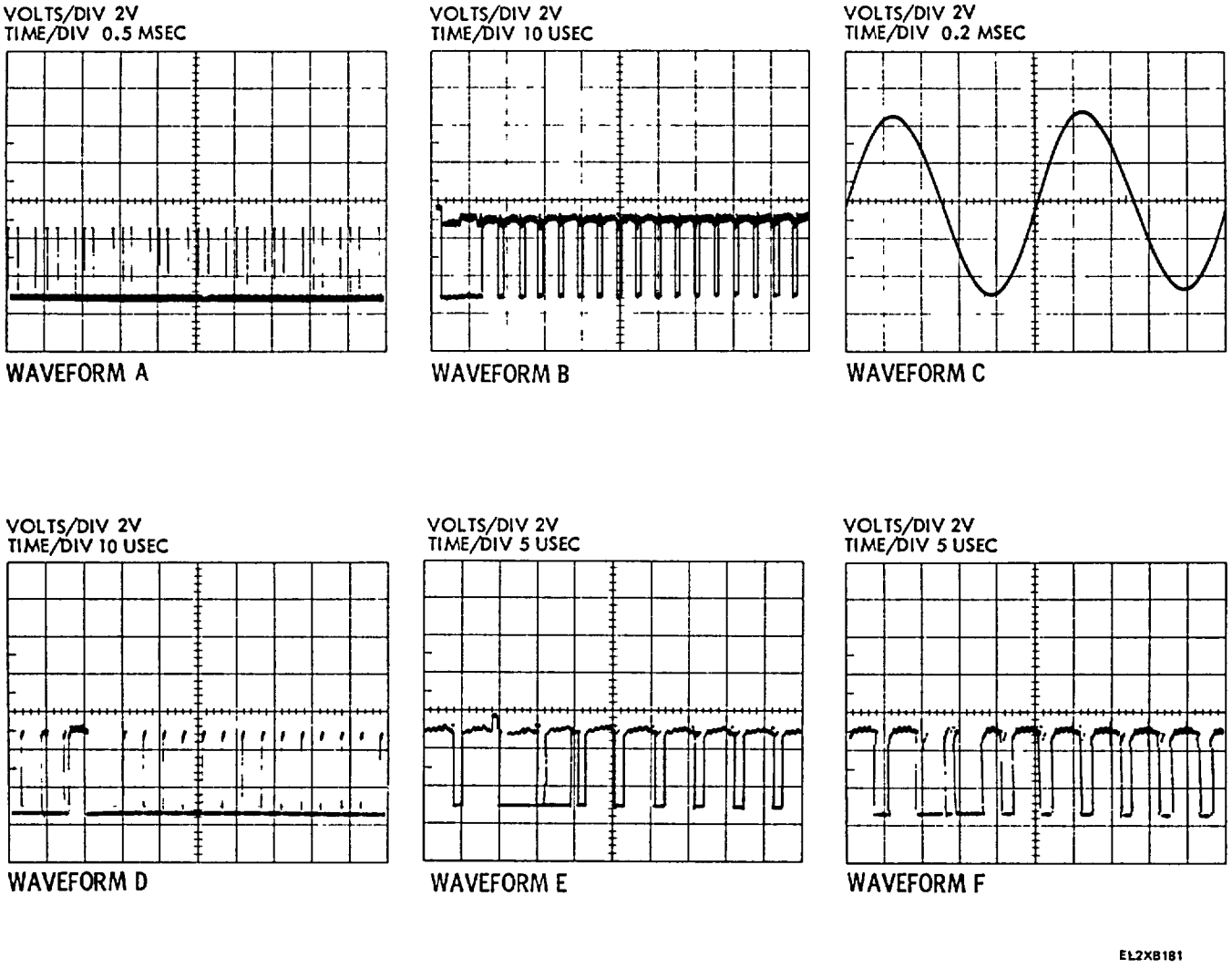


Figure 3-41. MUX test waveforms.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
1			Verify MBS CLOCK functions.	
			NOTE **Ignore any fault lamps which light during this test.**	
			a. Using type N cable, connect CP-772A/U AC input to MBS CLOCK test point on front of UUR.	*a.* 192 kHz ±1 kHz.
			b. Strap UUR for 6-channel operation (table 3-4).	*b.* 384 kHz ±1 kHz.
			c. Strap UUR for 12-channel operation (table 3-4).	*c.* 768 kHz ±1 kHz.
			d. Strap UUR for 24-channel operation (table 3-4).	*d.* 1544 kHz ±1 kHz.
2			Verify performance of EXT SOURCE RECEIVER circuit.	TIMING
			a. Connect Wavetek 142 50 0 output jack to left INPUT jack of AN/USM-281C. Adjust OUTPUT ATTEN (dB) on Wavetek 142 to produce a two-volt peak-to-peak square wave on AN/USM-281C.	*a.* 2V peak-to-peak square wave.
			b. Connect type N cable from 50 n output of Wavetek 142 to AC input of CP-772A/U. Adjust Wavetek 142 to 1.544 MHz ±1 kHz.	*b.* 1.544 MHz ±1 kHz.
			c. Using type N test cable connect 50 0 output of Wavetek 142 to EXT TMG SRCE at pins P29-1A (red) and P29-1B (black) on extender board.	*c.* None.
			d. Connect CP-772A/U AC input to EXT CLOCK test point on UUR.	*d.* 1.544 kHz± 1 kHz.
			e. Observe condition of EXT TIMING SOURCE lamp on DRIVER unit.	*e.* Lamp illuminates.
3			Verify performance of 78-ohm NRZ MBS CLK OUT DRIVER circuit.	
			NOTE **Ignore any fault lamps which light during this test.**	
			a. Disconnect type C test cable from MBS XMT CLK connector on rear of MXTF.	*a.* None.
			b. Check waveform at male pin of MBS XMT CKL connector.	*b.* Waveform A.
			c. Check signal at female pin of MBS XMT CLK connector.	*c.* Waveform A.
			d. Verify condition of EXT TIMING SOURCE lamp on UUR.	*d.* Lamp illuminates.
			e. Disconnect cable from CP-772/AU AC input.	*e.* None.
			f. Connect CP-772/AU AC input to MBS CLOCK test point on UUR.	*f.* 1.544 MHz ±kl kHz.
			g. Vary the frequency of Wavetek 142 slightly above and below 1.544 MHz (approx. 3.5 kHz).	*g.* MBS CLOCK frequency on CP-772A/U tracks Wavetek 142.
			h. Reconnect type C test cable to MBS XMT CLK connector on rear of MXTF.	*h.* None.
			i. Disconnect type N cable from P29-1A and P29-1B.	*i.* EXT TIMING SOURCE lamp off.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
4			Check 78-ohm BAL MASTER CLOCK OUT DRIVER circuit.	
			a Check signal at male pin of MA CLK connector on rear of MXTF	*a* Waveform A.
			b. Check signal at female pin of MA CLK con-connector.	*b*. Waveform A.
5			Check 78-ohm BAL MBS DATA OUT DRIVER circuit.	
			a. Disconnect type C test cable from MBS XMT DATA connector on rear of MXTF. On MXTF RCVR unit set LOOP/NORMAL switch to NORMAL.	*a* None.
	AN/USM-281C			
	TIMEIDIV	2 µs	*b*. Check signal at male pin of MBS XMT DATA connector.	*b*. Waveform C.
			c Check signal at female pin of MBS XMT DATA connector.	*c.* Waveform B.
6			Check BIPOLAR MBA DATA DRIVER circuit.	
			a. Strap DRIVER and RCVR units for bipolar operation (table 3-4).	*a* None.
	AN/USM-281C			
	TIMEIDIV:	5 µs	*b*. Check signal atmalepin of MBS XMT DATA connector.	*b*. Waveform D.
			a Check signal at female pin of MBS XMT DATA connector.	*c*. Waveform D.
			d. Reconnect type C cable to MBS XMT Data connector.	*d* No fault lamps illuminate.
7			Check LOSS OF OUTPUT DETECTOR circuit.	
			a Set LOOP NORMAL switch on RCVR unit to LOOP. Observe the following lamps: Unit Lamp DRIVER OUTPUT LOSS PWR SPLY LOCAL LOOP REMOTE LOOP C.G.A.	*a* Lamp silluminate.
			b. Set LOOP-NORMAL switch to NORMAL.	*b*. No lamps illuminate.
8			Check FAULT MONITOR circuit.	
			a Press FAULT TEST switch on UUR and observe FAULT lamp on UUR.	*a*. Lamp illuminates.
			b. Release FAULT TEST switch.	*b*. FAULT lamp out.

3-31. Testing RCVR Unit

This test verifies that the RCVR unit is capable of receiving MBS clock and MBS data, regenerating the clock, resynchronizing data to the regenerated clock, and providing REC RCV clock to user equipment. Loss of input and fault monitor circuits are also checked. Successful completion of the test qualifies a unit for return to users.

a. Test Equipment.

(1) ANIUSM-281C.

(2) CP-772AIU.

(3) MXTF with the following accessories:

Type A test cables (3)
Type B test cable
Type C test cables (2)
Type N test cable
Spare VF module
Spare 0-20 kb/s data module.

b. Initial Equipment Setup. Set up test equipment and repaired RCVR unit as follows: ',.

(1) Set power switch on MXTF PWR CONT unit to OFF.

(2) Set strapping on UUR (table 3-4) as follows:

Repaired RCVR Unit:	24-Channel NZR; full-alarm select (B2 = 0 +00001111)
MXTF DRIVER Unit:	24-Channel NRZ; full-alarm select (B2 = 0 + 00001111).

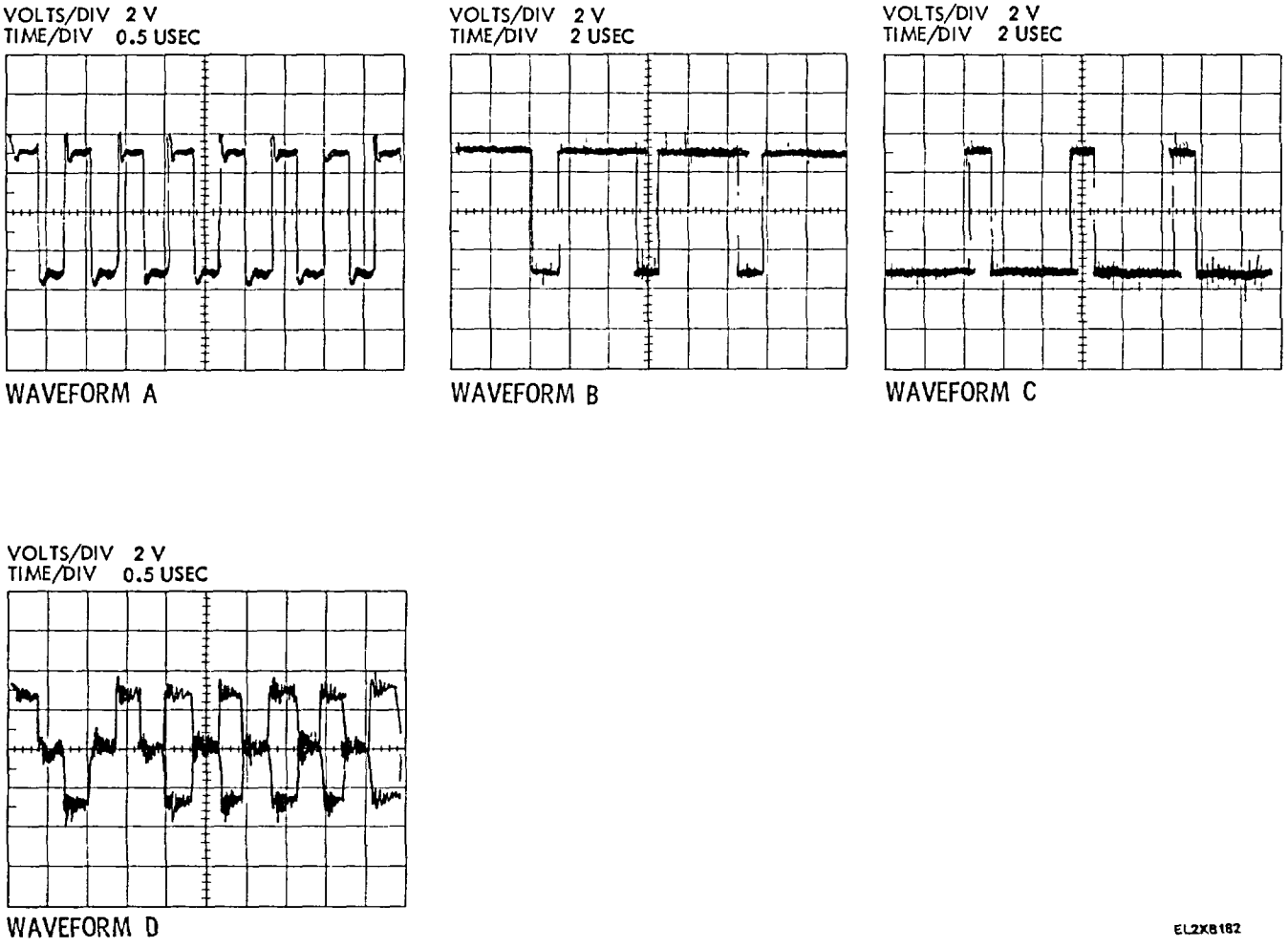


Figure 3-42. DRIVER test waveforms

(3) Remove RCVR unit from MXTF and install UUR.

(4) Install spare VF module in channel 1 location of MXTF.

(5) Install spare 0-20 kb/s data module in channel 2 location of MXTF.

(6) Connect VF OSC jack on BITE to lower XMT jack on VF module using type A cable.

(7) Connect VF METER jack on BITE to lower RCV jack on VF module using type A cable.

(8) Connect DATA OUT jack on BITE to DATA IN jack of 0-20 kb/s module using type A cable.

(9) Connect RCV DATA IN jack on BITE to RCV DATA jack of 0-20 kb/s module using type B cable.

(10) Connect type C cable between MBS RCV DATA and MBS XMT DATA connectors on rear of MXTF.

(11) Connect type C test cable between MBS RCV CLK and MBS XMT CLK connector on rear of MXTF.

(12) Set test equipment switches as shown below.

Unit	*Control*	*Setting*
MXTF (BITE)	DIGITAL FUNCTION	20 kb/s
	VF FUNCTION	LOOP TEST
(PWR CONT)	Power	ON
AN/USM-281C	POWER	Pull
	VOLTS/DIV (left)	2V
	AC/GND/DC	DC
	TIME/DIV	5 ,s
	TRIG SOURCE	LEFT
	VERT MODE	LEFT
CP-772A/U	SAMPLE RATE	Rotate % turn clockwise
	FUNCTION	FREQUENCY
	TIME BASE	1 s

NOTE

Allow equipment to warm up for 5 minutes before proceeding with test.

c. Test Procedure. Verify performance of UUR in accordance with the following test procedure. Performance Standard

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
1			Check MBS data circuits.	
			a. Verify condition of FAULT and INPUT LOSS lamps on UUR.	*a.* Lamps off.
			b. Verify that VF METER on MSTF BITE indicates proper receive level for VF module strapping.	*b.* VF module strapping BITE C strap out -7 dBm C strap in 0 dBm
2	*MXTF (RCVR)* LOOP-NORMAL:	LOOP	Verify loop back functions by checking the following lamp conditions: **Unit** **Lamp** DRIVER OUTPUT LOSS PWR SPLY LOCAL LOOP REMOTE LOOP C.G.A	Lamps illuminate.
3	*MXTF (RCVR)* LOOP-NORMAL:	NORMAL	Check recovered clock functions.	
			a. Check signal at top pin of REC RCV CLK connector on rear of MXTF.	*a.* Waveform A.
			b. Check signal at bottom pin of REC RCV CLK connector.	*b.* Waveform A.
4			Check loss of input monitor. Disconnect type C cable from MBS RCV DATA connector on rear of MXTF and check the following lamp conditions: **Unit** **Lamp** RCVR INPUT LOSS DEMUX FRAME LOSS PWR SPLY C.G.A BITE BIT ERROR BER >10-2	Lamps illuminate.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
5			Check loss of clock monitor.	
			a Reconnect cable removed in step 4 and disconnect type C cable from MBS RCV CLK connector on rear of MXTF.	*a* Lamps illuminate.
			Check the following lamp conditions: *Unit* — *Lamp* RCVR — INPUT LOSS DEMUX — FRAME LOSS PWR SPLY — C.G.A. BITE — BIT ERROR BER > 10-2	
			b. Reconnect cable to MBS RCV CLK connector.	*b*. None.
6			Check BIPOLAR RECEIVER circuit.	
			a. Restrap UUR and MXTF for bipolar operation (table 3-4).	*a* None.
			b. Observe condition of lamps on all DTG units and PWR SPLY unit.	*b*. Lamps off.
7	*AN/USM-281C* TIMEIDIV:	2µs	Check clock recovery function.	
			a Check signal at MBS DATA OUT test point on UUR.	*a.* Waveform B.
			b. Using type N cable, connect CP-772A/U to MBS CLOCK OUT test point on UUR.	*b*. 1.544MHz+100 Hz.
			c. Strap UUR and DRIVER for 3-channel NRZ operation (table 3-4).	*c.* None.
			d Verify that MXTF acquired frame by observing all lamps on DTG units and PWR SPLY unit.	*d*. Lamps off.
			e. Verify clock frequency by observing CP-772AIU display.	*e*. 192 kHz=100 Hz.
			f. Restrap for 6- and 12-channel operation and repeat *d* and *e* above.	*f.* All lamps off. 6-channel-384 kHz +100 Hz 12-channel-768 kHz.
8			Check external loopback functions.	
			a Connect a jumper between pin B of the EXTERNAL COMMANDS connector on the rear of the MXTF and pin C.	*a.* None.
			b. Check the following lamp conditions: *Unit* — *Lamp* DRIVER — OUTPUT LOSS PWR SPLY — LOCAL LOOP REMOTE LOOP C.G.A.	*b*. Lamps illuminate.
9			Check frame switch inhibit receiver. Connect jumper between pins A and C of the EXTERNAL COMMANDS connector on the rear of the MXTF and observe SEARCH INHIBIT lamps on DEMUX with.	*a* Lamp illuminates

3-32. Testing DEMUX Unit

This test will verify that the DEMUX unit will recognize frame pattern, provide the correct number of channel counter pulses and detect remote alarm condition in the far-end set. Successful completion of the test qualifies the unit for return to users.

a. Test Equipment.

(1) AN/USM-281C.

(2) CP-772A/U.

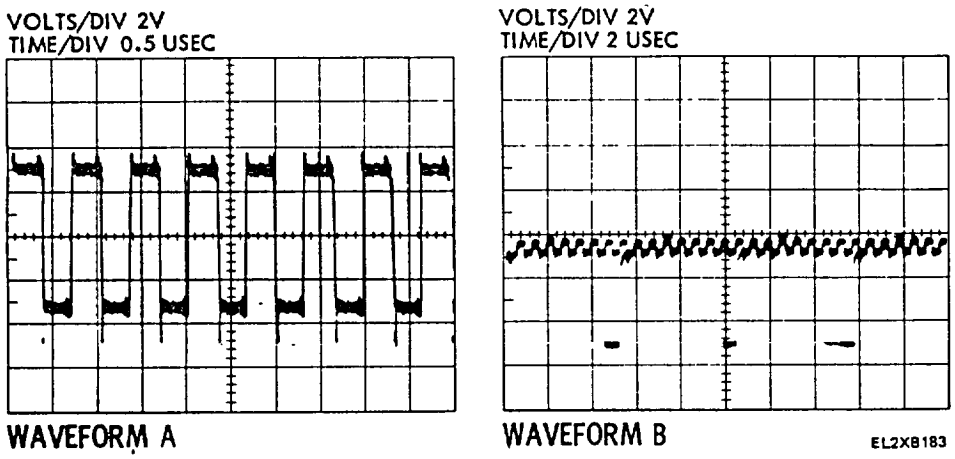


Figure 3-43. RCVR test waveforms.

(3) MXTF with the following accessories:
Type A test cable
Type B test cable
Type C test cables (2)
Type N test cable
Spare 0-20 kb/s data module.

b. Initial Equipment Setup. Set up test equipment and repaired DEMUX unit as follows:

(1) Set switch on MXTF PWR CONT unit to OFF.

(2) Remove MXTF DEMUX unit and replace with UUR.

(3) Install 0-20 kb/s module in channel 2 location.

(4) Connect test equipment as follows:

Test cable type	*Unit/Jack*	*Unit/Jack*
A	BITE XMT	0-20 kb/s XMT DATA IN
	DATA OUT	
B	BITE RCV	0-20 kb/s RCV DATA
	DATA IN	

(5) Connect type C cable between MBS RCV DATA and MBS XMT DATA connector on rear of MXTF.

(6) Connect type C test cable between MBS RCV CLK and MBS XMT CLK connector on rear of MXTF.

(7) Strap DRIVER and RCVR units for 24-channel operation (table 3-4).

(8) Set test equipment switches as follows:

Unit	*Control*	*Setting*
MXTF BITE	DIGITAL FUNCTION	CLK RATE 20 Kb/s
MXTF PWR CONT	Power	ON
RCVR	LOOP-NORMAL	NORMAL
AN/USM-281C	TIME/DIV	50 µs
	VOLTS/DIV (left)	2V
	AC/GND/DC	DC
	TRIG SOURCE	LEFT
	VERT MODE	LEFT
CP-772A/U	SAMPLE RATE	Rotate % turn clockwise
	SENSITIVITY	.1
	FUNCTION	MANUAL START

NOTE

Allow equipment to warm up 5 minutes before proceeding with test.

c. Test Procedure. Verify performance of the UUR in accordance with the following procedure. Normal indication

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
1			Verify frame acquisition operation.	
			NOTE	
			Ignore any fault lamps which light during this test.	
			a. Remove cable from MBS RCV DATA connector on rear of MXTF.	a. None.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-45
			b. Using type N test cable, connect CP-772A/U AC input to FRAME BIT ERROR test point on UUR.	b. None.
			c. Adjust CP-772A/U LEVEL control until counter display counts continuously.	c. None.
	MXTF (RCVR) LOOP-NORMAL: LOOP		d. Reset CP-772A/U and allow 5 minutes for errors to accumulate.	d. No errors in 5 minutes.
			e. Restrap for 3-, 6-, and 12-channel modes and repeat a through d for each mode.	e. No errors in 5 minutes.
2			Check channel counter functions.	
			a. Strap DRIVER and RCVR units for 24-channel operation (table 3-4).	a. None.
			b. Verify lamp condition on BITE. ERROR and BER > 10- lamps out.	b. SYNC lamp illuminates.
			c. Move 0-20 kb/s module to the next channel which will accept a data module repeating a and b above until all channels have been checked.	c. As in b.
3			Verify remote alarm functions.	
	MXTF (RCVR) LOOP-NORMAL: NORMAL		a. On PWR SPLY unit, observe REMOTE ALARM and C.G.A. lamps.	a. Lamps illuminate.
			b. Check signal at FRAME BIT ERROR test point on UUR.	b. Waveform A.
4	Check RCV PCM BUS function. AMXTF (RCVR) LOOP-NORMAL: LOOP AN/USM-281C			
	TIME/DIV:	5 µs	a. Check signal at RCV PCM test point on UUR.	a. Waveform B.
	TIME/DIV:	.5 ms	b. Check signal at 12 FRAME test point on UUR.	b. Waveform C.

3-33. Testing the PCD Unit

This test verifies that the repaired PCD unit converts PCM data to analog VF data and distributes the analog data to each of the 24-channel slots. The test also verifies the ability of the PCD unit to recover signaling information and distribute it to the correct channel. Successful completion of the test qualifies the unit for return to users.

a. Test Equipment

(1) AN/USM-281C.

(2) DMM.

(3) TIMS.

(4) MXTF with the following accessories:

Type A test cables (3)
Type G test cables (2)
Spare VF modules (2).

b. Initial Equipment Setup

(1) Set power switch on PWR CONT unit of MXTF to OFF.

(2) Remove PCD unit from MXTF; install UUR.

(3) Verify that DTG is strapped for 24-channel operation (table 3-4).

(4) Install spare VF module in channel 1 position of MXTF.

(5) Set test equipment control as follows:

Unit	*Switch*	*Setting*
MXTF (RCVR)	LOOP-NORMAL	LOOP
(PWR CONT)	Power	ON
AN/USM-281C	POWER	Pull
	VOLTS/DIV	1V
	TIME/DIV	1 As
	TRIG SOURCE	LEFT
	AC/GND/DC	DC
TIMS	DISPLAY CONNECTED TO	TRMT
	MEASUREMENT	LEVEL & FREQUENCY
	FREQUENCY CONTROL	Set to indicate 10004 Hz
	NOISE FILTER	C-MSG

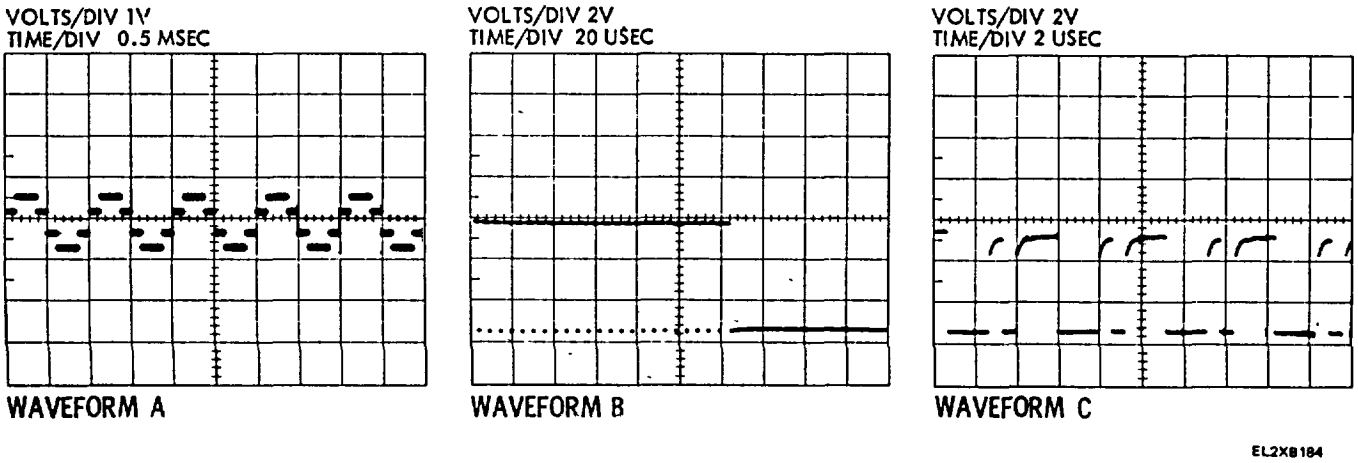


Figure 3-44. PCD test waveforms.

Unit	*Switch*	*Setting*
	POWER	ON
	SETUP	NORMAL TEST
	CONTROLS	TEST WITHOUT HOLD
		TALK BATTERY
		OFF
		TERM
		600
		NO SF SKIP
		NORMAL TEST

Unit	*Switch*	*Setting*
	RECEIVE/ TRANSMIT JACKS switch	Down position

NOTE
Allow equipment to warm up for 5 minutes before proceeding with test.

c. Test Procedure. Verify performance of the UUR in accordance with the following procedure.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-44
1			Perform a VF gain test.	
			a. Install spare VF module in channel 1 location of MXTF.	a. None.
			b. Perform DTG common VF gain adjustment and VF module channel level receive and transmit adjustments as specified in TM 11-5805-711-13.	b. None.
			c. Connect type G test cable between TIMS 310 TRMT jack and VF module lower XMT jack. Connect type G test cable between TIMS 310 RCV jack and lower RCV jack of VF module.	c. None.
			d. Adjust TIMS OUTPUT LEVEL control until TIMS display indicates correct level for VF module strapping.	d. **VF module strapping** / **TIMS display**: A strap in / -16 dBm; B strap in / 0 dBm
	TIMS DISPLAY CONNECTED TO:	RCV	e. Verify that TIMS display indicates correct level for VF module strapping.	e. **VF module strapping** / **TIMS display**: C strap in / 0 ±0.5 dBm; C strap out / +7 ±0.5 dBm
			f. Move VF module to progressively higher channels, repeating e above until all channels have been checked.	f. None.
2			Perform a signaling test.	
			a. Install a spare VF module in the channel 1 location of the MXTF.	a. None.
			b. Connect type A test cable from MXTF BITE SIG jack to SIG jack on VF module. Set BITE ON HOOK/OFF HOOK switch to OFF HOOK. Press CGA DEFEAT switch on PWR SPLY module. Observe OFF HOOK lamp.	b. Lamp illuminates.
			c. Set BITE ON HOOK/OFF HOOK switch to ON HOOK. Press CGA DEFEAT switch on PWR SPLY module and observe OFF HOOK lamp.	c. Lamp off.
			d. Move VF module to progressively higher channels, repeating b and c above until all channels have been checked.	d. As in b and c above.
3			Perform a signal-to-quantizing noise test.	
			a. Install spare VF module in channel 1 of MXTF.	a. None.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-44
			b. Connect type G test cable from TIMS 310 TRMT jack to lower XMT jack of module. Connect type G test cable from TIMS RCV 310 jack to lower RCV jack of VF module.	b. None.
	TIMS DISPLAY CONNECTED TO: MEASUREMENT:	TRMT NOISE-WITH-TONE	c. Adjust TIMS OUTPUT LEVEL control to correct level for VF module strapping indicated.	c. **VF module strapping / TIMS display** A strap in / -16 dBm B strap in / 0 dBm
	TIMS DISPLAY CONNECTED TO: MEASUREMENT:	RCV NOISE-WITH-TONE		
	NOISE FILTER: MEASUREMENT:	C-MSG MESSAGE CIRCUIT NOISE	d. Record the TIMS display reading. e. Subtract the new reading on the TIMS display from the reading recorded in d, using the VF module strapping indicated. f. Move the VF module to progressively higher channels, repeating d and e above until all channels have been checked.	d. **None.** e. **VF module strapping / S/N-Quantizing** C strap in / ≥ 25 dBm C strap out / ≥ 33 dBm f. As in e above.
4			Perform a cross talk-test.	
	MXTF (BITE) VF FUNCTION	LOOP TEST	a. Install spare VF modules in channels 1 and 2 of MXTF. Connect the MXTF BITE VF OSC jack to the channel 1 (left) VF module lower XMT jack using a type A test cable.	a. None.
			b. Set BITE OSC LEV to correct level for VF module strapping indicated.	b. **VF module strapping / BITE OSC LEV** A strap in / -16 dBm B strap in / 0 dBm
			c. Connect TIMS 310 RCV jack to channel 2 (right) VF module lower RCV jack using type G test cable.	c. None.
			d. Verify that TIMS display indicates correct level for VF module strapping indicated.	d. **VF module strapping / TIMS display** C strap in / ≤ 25 dBm C strap out / ≤ 32 dBm
			e. Connect BITE VF OSC jack to lower XMT jack on right VF module using type A cable.	e. None.
			f. Connect the TIMS 310 RCV jack to lower RCV jack of left VF module, using type G cable.	f. None.
			g. Verify that TIMS display indicates correct level for VF module strapping indicated.	g. **VF module strapping / TIMS display** C strap in / ≤ 25 dBm C strap out / ≤ 32 dBm
			h. Move left VF module to next open channel and repeat a through g until all channels have been checked.	h. As in d and g above.
5			Perform a test point check.	
	AN/ US,-281 C TIME/DIV:	.5 ms	a. Check signal at PAM test point on UUR.	a. Waveform A.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-4
	MXTF (MUX)			
	1 KHZ TONE:	ON for steps a, b and c		
	AN/USM-2RI8C			
	TIME/DIV:	20 ;s	b. Check signal at SIG test point on UUR.	b. Waveform B.
	VOLTS /DIV:	2V		
	TIME/DIV:	2 us	c. Check signal at PCM DATA test point on UUR.	c. Waveform C.
6			Perform a fault test by observing the following lamps:	Lamps illuminate.
	UUR		Unit / Lamp	
	FAULT TEST	Push	UUR / FAULT	
			ALL FAULT TEST	
			PWR SPLY / FAULT	

3-34. Testing VF Module

This test will verify the bandpass of the VF module, its idle channel noise, and impulse noise. It will also qualify a VF module for return to users.

a. Test Equipment.

(1) TIMS.

(2) MXTF with the following accessories:
Type A (bantam) test cable
Type D test cable
Type G test cables (2).

b. Initial Equipment Setup. Set up test equipment and repaired VF module as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.

(2) Inspect UUR. Record presence or absence of A, B, C, D1, D2, and E straps.

(3) Install UUR in channel 1 position of MXTF.

(4) Connect test equipment as follows:

Test cable type	*TIMS jack*	*VF module jack*
G	310 (right)	Left-hand LINE-UP (transmit)
G	310 (left)	XMT

CAUTION

Do not place any object, such as manuals, clipboards, etc., on top of TIMS. Restriction of airflow can cause overheating and damage to the set.

(5) Set test equipment switches as follows:

Unit	*Control*	*Setting*
TIMS	TERM/BRIDGE RECEIVE	TERM
	600/900	600
	NO SF SKP/SF SKP	NO SF SKP
	NORMAL TEST	NORMAL TEST
	OUTPUT LEVEL	full CCW
	RECEIVE/TRANSMIT JACKS SWITCH	TRMT (down)
	MEASUREMENT	LEVEL and FREQUENCY
	DISPLAY CONNECTED	TRMT
	FREQUENCY CONTROL	STEP 100 HZ
	POWER	ON
MXTF (PWR CONT)	Power	ON
(RCVR)	LOOP-NORMAL	LOOP

NOTE
Allow equipment to warm up for 5 minutes before proceeding with test.

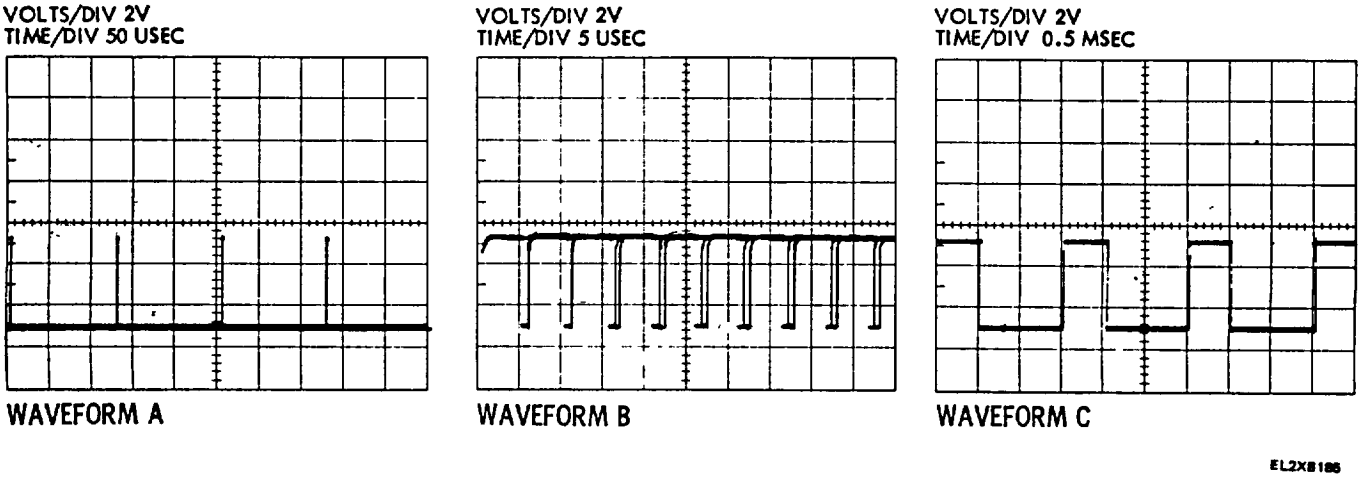


Figure 3-45. DEMUX test Waveforms

c. Test Procedure. Verify performance of a UUR in accordance with the following test procedure.

Step	Control	Settings	Test procedure	Performance standard
1	*TIMS* DOWN/UP: OUTPUT LEVEL:	 As required. As required.	On TIMS, adjust OUTPUT LEVEL control clockwise until display is obtained. Use DOWN/UP pushbuttons to obtain input frequency of 1004 -1 Hz.	None.
2	*TIMS* OUTPUT LEVEL:	 As required.	On TIMS, observe DBM right display, and adjust OUTPUT LEVEL control clockwise to obtain correct input level for strapping (recorded in setup procedures) as follows: a. A strap installed: OUTPUT LEVEL b. B strap installed: OUTPUT LEVEL	 a. -16 ±0.2 dBm. b. 0 ±0.1 dBm.
3	*TIMS* DISPLAY CONNECTED TO:	 RCV	On TIMS, observe DBM display. If necessary, adjust XMT GAIN on UUR.	-13.5 +-0.2 dBm.
4			For receive channel level gain test, connect test equipment as follows: **Test Cable Type** / **TIMS Jack** / **VF MODULE Jack** G / 310 (left) / LINE-UP (right) G / 310 (right) / RCV	None.
5	*TIMS* DOWN/UP: DISPLAY CONNECTED TO:	 As required. TRMT	On TIMS, while using DOWN/UP pushbuttons, observe TRMT HZ center display, and verify 1004 ±1 HZ input frequency.	
6	*TIMS* OUTPUT LEVEL:	 As required.	On TIMS observe DBM display. Adjust OUTPUT LEVEL control clockwise to obtain -16.0 ±0.1 dBm input level.	
7	*TIMS* DISPLAY CONNECTED TO:	 RCV	On TIMS, observe DBM display. If necessary, adjust RCV GAIN control on UUR to obtain correct reading. a. VF module: C strap installed. b. VF module: C strap not installed.	 a. 0 ±0.5 dBm. b. +7 ±0.5 dBm.
8	*MXTF (PWR CONT)* Power: *TIMS* POWER:	 OFF OFF	Remove type G test cables and use type D test cable to connect TIMS to MXTF as follows (other channel jacks than those specified are not used): **D Test Cable Connector** / **Unit** / **Unit Connector** VF channels / MXTF (rear) / VF CHANNELS 1-3 XMT IN CH 1 / TIMS jack / left-hand 310 RCV OUT CH 1 / TIMS / right-hand 310 jack	None.
9	*MXTF (PWR CONT)* Power: *(RCVR)* LOOP-NORMAL: *TIMS* POWER: DOWN/UP: DISPLAY CONNECTED TO:	 ON LOOP ON As required. TRMT	On TIMS, while using DOWN/UP pushbuttons, observe TRMT HZ center display, and verify 1004 HZ input frequency.	

Step	Control	Settings	Test procedure	Performance standard
10	*TIMS* OUTPUT LEVEL:	As required.	On TIMS observe DBM display. Adjust OUTPUT LEVEL control clockwise to obtain correct input level for strapping (recorded in setup procedures) as follows:	
			a. VF module: A strap installed.	a. -16 -0.1 dBm.
			b. VF module: B strap installed.	b. 0 ±0.1 dBm.
11	*TIMS* DISPLAY CONNECTED TO:	RCV	On TIMS observe RCV HZ display.	1004 ±5 Hz.
12			On TIMS observe DBM display and verify output level is correct for strapping (recorded in setup procedures) as follows:	
			a. VF module: C strap installed.	a. -0 5 -0.5 dBm.
			b. VF module: C strap not installed.	b. +7 ±-0.5 dBm.
13	*TIMS* DOWN/UP: DISPLAY CONNECTED TO:	As required TRMIT	On TIMS, while using DOWN/UP pushbuttons, observe TRMT HZ display and verify 304 ±1 Hz low frequency input.	
14	*TIMS* OUTPUT LEVEL:	As required.	On TIMS, observe DBMI display. Adjust OUTPUT LEVEL control clockwise to obtain correct input level for strapping (recorded in setup procedures) as follows:	
			a. VF module: A strap installed.	a. -16 -0.1 dBm.
			b. VF module: B strap installed.	b. 0 ±0.1 dBm.
15	*TIMS* DISPLAY CONNECTED TO:	RCV	On TIMS, observe RCV HZ display.	304 +5 Hz.
16			On TIMS, observe DBMI display. Verify output level is correct for strapping (recorded in setup procedures) as follows:	
			a. VF module: C strap installed.	a. -0.5 -0.5 dBm.
			b. VF module: C strap not installed.	b. +7 -0.5 dBm.
17	*TIMS* DOWN/UP: DISPLAY CONNFCTED TO:	As required TRMIT	On TIMS, while using DOWN/UP pushbuttons, observe TRMT HZ center display. Verify high frequency input of 3004 ±1 Hz.	
18	*TIMS* OUTPUT LEVEL:	As required.	On TIMS, observe DBAM display. Adjust OUTPUT LEVEL control clockwise to obtain correct input level for strapping (recorded in setup procedures) as follows:	
			a. VF module: A strap installed.	a. -16 -0.1 dBm.
			b. VF module: B strap installed.	b. 0 ±0.1 dBm.
19	*TIMS* DISPLAY CONNECTED TO:	RCV	On TIMS, observe RCV HZ display.	3004 ±5 Hz.
20			On TIMS, observe DBM right display. Verify output level is correct for strapping (recorded in setup procedures) as follows:	
			a. VF module: C strap installed.	a. -0.5 -0.5 dBm.
			b. VF module: C strap not installed.	b. +7 ±0.5 dBm.

Step	Control	Settings	Test procedure	Performance standard
21	*TIMS*		Verify idle channel noise dots not exceed following values for strapping (recorded in setup procedures):	
	MEASUREMENT:	MESSAGE CIRCUIT NOISE		
	DISPLAY CONNECTED TO:	RCV	a. VF module: C strap installed.	a. 23 dBm.
	NOISE FILTER:	C-MSG	b. VF module: C strap not installed.	b. 30 dBm.
22	*TIMS*		On TIMS, while using DOVOIN/UP pushbuttons, observe TRMT IH center display. Verify input frequency of 1004 ±1 Hz.	
	MEASUREMENT:	3-LEVEL IMPULSE NOISE HITS and DROPOUTS		
	DOWN/UP:	As required.		
	DISPLAY CONNECTED TO:	TRMT		
23			On TIMS, observe DBM right display. Adjust OUTPUT LEVEL control to obtain correct input level for strapping (recorded in set up procedures) as follows:	
			a. VF module: A strap installed.	a. -29 dBm.
			b. VF module: B strap installed.	b. -13 dBm.
24	*TIMS*		On TIMS, rotate IMPULSE NOISE LO THRESHOLD control to correct level for strapping (recorded in setup procedures) as follows:	
	DISPLAY CONNECTED TO:	RCV	a. VF module, C strap installed: 55 dBm threshold.	a. None.
	COUNT RATE:	BELL STD	b. VF module, C strap not installed: 62 dBm threshold.	b. None.
	COUNT TIME 15 MIN:	ON		
	IMPULSE NOISE LO:	As required.		
	THRESHOLD DISPLAY:	IMPULSE NOISE		
25	*TIMS*		Observe number of impulse noise hits exceeding threshold during 15 minute count time.	Counts HI; not to exceed 1 noise count per 15 minutes.
	PUSH TO START:	press	**CAUTION** **Follow test cable connection, sequence specified in the following step to preclude possible shorting of -42 volt BITE signal output.**	
26	*MXTF (RCVR)*		Connect type A (bantam) test cable first to SIG jack on VF module and, then to SIG jack on BITE.	None.
	LOOP-NORMAL:	LOOP		
	(BITE)			
	DIGITAL FUNCTION:	CLK RATE 50 Kb/S		
27	*MXTF (BITE)*		Verify CGA circuit in UUR forces E lead on hook by observing OFF HOOK lamp on BITE.	Lamp off.
	ON HOOK-OFF HOOK:	OFF HOOK		
' 28 -	*XTF (PWR SPLY)*		Depress C.G.A. DEFEAT switch land observe OFF HOOK lamp on BITE.	Lamp illuminates.
	C.G.A. DEFEAT:	press		

Step	Control	Settings	Test procedure	Performance standard
29	*MXTF (PWR SPLY)* C.G.A. DEFEAT: *(BITE)* ON HOOK-OFF HOOK:	 press ON HOOK	Press C.G.A. DEFEAT switch and observe OFF HOOK lamp on BITE.	Lamp off.

3-35. Testing 0-20 Kb/s Data Module

This test will verify that a 0-20 kb/s data module processes data without introducing errors, and will qualify the module for return to users.

a. Test Equipment.

(1) Checktran.

(2) MXTF with the following accessories:
Type C test cables (2)
Type L test cable.

b. Initial Equipment Setup. Set up test equipment and repaired data module as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.

(2) Install UUR into channel 2 position of MXTF.

(3) Connect test equipment as follows:

Test Cable Type	*MXTF Rear Panel Connectors*	*Unit/Jack*
L	DATA CHANNELS 2	Checktran, DATA COMMUNICATIONS EQUIPMENT
C	MBS XMT DATA	MXTF Rear panel, MBS RCV DATA
C	MBS XMT CLK	MXTF rear panel, RCV MBS CLK

(4) Set test equipment switches as follows:

Unit	Switch	Setting
Checktran	DATA RATE	7640
	DATA BITS	8
	STOP UNIT	2
	POWER	ON
	PATTERN SYNC	ASYNC
	SYNC	AUTO
	EXT CLK	Out
MXTF (PWR CONT)	Power	ON
(RCVR)	LOOP-NORMAL	NORMAL

c. Test Procedure. Verify performance of UUR in accordance with the following test procedure.

Step	Control	Settings	Test procedure	Performance standard
1	*CHECKTRAN* RESET: ERROR COUNT:	 press press	Observe accumulated error count on 3-digit readout of Checktran after 15 minutes.	Not more than 5 errors.
2	*MXTF (RCVR)* LOOP-NORMAL:	 LOOP	Observe Checktran 3-digit readout to verify 0-20 kb/s data module responds to CGA by forcing all is output (maximum errors).	Readout indicates errors and OVERFLOW lamp illuminates within 10 seconds.
3	*MXTF (RCVR)* LOOP-NORMAL: *CHECKTRAN* RESET: ERROR COUNT:	 NORMAL press press	Observe that 3-digit Checktran readout for approximately 30 seconds.	000 (error free).
4	*UUR* FAULT:	 press	Verify manual fault test capability of UUR by observing the following: a. FAULT lamp on PWR SPLY unit. b. FAULT lamp on UUR. illuminates.	 a. Lamp illuminates. b. Lamp illuminates.

3-36. Testing 50 kb/s Data Module

This test will verify that a 50 kb/s data module processes data with acceptable error rates, and will qualify the unit for return to users.

a. Test Equipment.

(1) Checktran.

(2) MXTF with the following accessories:
Type C test cables (2)
Type L test cable.

b. Initial Equipment Setups. Set up test equipment and repaired 50 kb/s data module as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.

(2) Install UUR into channel 2 position of MXTF.

(3) Connect test equipment as follows:

Test Cable Type	*MXTF Rear Panel Connectors*	*Unit/Jack*
L	DATA CHANNELS 2	Checktran, DATA COMMUNICATIONS EQUIPMENT
C	MBS XMT DATA	MXTF rear panel, MBS RCV DATA
C	MBS XMT CLK RCV CLK	MXTF rear panel, MBS

(4) Set Checktran switches as follows:

Unit	*Switches*	*Setting*
	DATA RATE	3754
	DATA BITS	6
	STOP UNIT	2
	POWER	ON
	PR CODE	2047
	PATTERN PR	on
	EXT CLK	**IN**
	SYNC	AUTO
MXTF (PWR CONT)	Power	ON
(RCVR)	LOOP-NORMAL	NORMAL

NOTE

Allow equipment to warm up for 5 minutes before proceeding with test.

c. Test Procedure. Verify performance of the UUR in accordance with the following test procedure.

Step	Control	Settings	Test procedure	Performance standard
1	CHECKTRAN RESET: ERROR COUNT:	 press press	Observe accumulated error count on Checktran 3-digit readout after 24 minutes.	Not more than 3 errors.
2	MXTF (RCVR) LOOP-NORMAL: CHECKTRAN PATTERN 1-0:	 LOOP press	Observe Checktran 3-digit readout to verify UUR data module responds to CGA by forcing all 1s output (maximum errors). Observe OVERFLOW lamp on Checktran.	Readout indicates errors, lamp illuminates within 10 sec.
3	MXTF (RCVR) LOOP-NORMAL: CHECKTRAN RESET:	 NORMAL press	Press Checktran ERROR COUNT pushbutton and observe 3-digit readout indicates error free operation for approximately 30 seconds.	Readout indicates 000 (error free).
4	UUR FAULT:	 press for stop	Verify manual fault test capability of 50 kb/s data module by observing the following: a. FAULT lamp on PWR SPLY panel. b. FAULT lamp on 50 kb/s data module.	 a. Lamp illuminates. b. Lamp illuminates.

3-37. Testing Multirate Data Module

This test will verify that a multirate data module processes data with acceptable error rates, and will qualify a module for return to users.

a. Test Equipment.

(1) Checktran,

(2) MXTF with the following accessories:

Type A test cables (2)
Type B test cables (3)
Type C test cables (2)
Type L test cable.

b. Initial Equipment Setup. Set up test equipment and repaired data module as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.

(2) Remove any channel modules that may be installed in MXTF.

(3) Connect test equipment as follows:

Test Cable Type	*MXTF Rear Panel Connectors*	*Unit/Jack*
L	DATA CHANNELS 2	Checktran, DATA COMMUNICATIONS EQUIPMENT
C	MBS XMT DATA	MXTF rear panel, MBS RCV DATA
C	MBX XMT CLK	MXTF rear panel, MBS RCV CLK

(4) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
Checktran	DATA RATE	7767
	DATA BITS	8
	STOP UNIT	2
	POWER	ON
	PATTERN PR	ON
	PR CODE	2047
	SYNC	AUTO
	EXT CLK	OUT
MXTF (PWR CONT)	Power	ON
(RCVR)	LOOP-NORMAL	NORMAL

NOTE

Allow equipment to warm up for 5 minutes before proceeding with test.

c. Test Procedure. Perform the following steps to verify the performance of a multirate data module.

NOTE

Disregard all fault and alarm indications that occur during strapping changes in the following procedure.

Step	Control	Settings	Test procedure	Performance standard
			Check 512 kb/s, internal clocks, adjacent channel operation as follows:	
1			a. Set strapping switches on UUR for 512 kb/s, internal clock, adjacent channel operation (table 3-4), and install in channel 2 position of MXTF.	a. None.
	CHECKTRAN RESET: ERROR COUNT:	 press press	b. Check 512 kb/s operation of data module on internal clock, adjacent channel condition, by observing 3-digit Checktran display.	b. Not more than 30 counts within 10 min of pressing ERROR COUNT switch.
2			Check 256 kb/s, internal clock, adjacent channel operation as follows:	
			a. Set strapping s witches on UUR for 256 kb/s, internal clock, adjacent channel operation (table 3-4), and install in channel 2 position of MXTF.	a. None.
	CHECKTRAN DATA R ATE: RESET: ERROR COUNT:	 7756 press press	b. Check 256 kb/s operation of data module with internal clock and adjacent channel selected by observing accumulated error count on 3-digit Checktran display.	b. Not more than 15 counts within 10 min of pressing ERROR COUNT switch.
3			Check 128 kb/s, internal clock, adjacent channel operation as follows:	
			a. Set strapping switches on UUR for 128 kb/s, internal clock, adjacent channel operation (table 3-4), and install in channel 2 position of MXTF.	a. None.
	CHECKTRAN DATA RATE: RESET: ERROR COUNT:	 7734 press press	b. Check 128 kb/s operation of data module with internal clock and adjacent channel selected by observing accumulated error count on 3-digit Checktran display.	b. Not more than 8 counts within 10 min of pressing ERROR COUNT switch.
4			Check 64 kb/s, internal clock, operation as follows:	
			a. Set strapping switches on UUR for 64 kb/s, internal clock, (table 3-4), and install in channel 2 position of MXTF.	a. None.
	CHECKTRAN DATA RATE: RESET: ERROR COUNT:	 7712 press press	b. Check 64 kb/s operation of data module with- internal clock by observing accumulated error count on Chectran display.	b. Not more than 4 counts within 10 min of pressing ERROR COUNT switch.

Step	Control	Settings	Test procedure	Performance standard
5			Check 56 kb/s, internal clock operation as follows:	
			a. Set strapping switches on UUR for 56 kb/s, internal clock operation (table 3-4), and install in channel 2 position of MXTF.	a. None.
	CHECKTRAN		b. Check 56 kb/s operation by observing 3-digit Checktran display.	b. Not more than 3 counts within 9 min of pressing ERROR COUNT switch.
	DATA RATE:	7735		
	RESET:	press		
	ERROR COUNT:	press		
6	*CHECKTRAN*		Observe Checktran 3-digit readout to verify UUR responds to CGA by forcing all is output (maximum errors). Observe OVERFLOW lamp on Checktran.	Readout indicates errors; lamp illuminates within 10 sec.
	PATTERN 1-0:	down		
	RESET:	press		
	ERROR COUNT:	press		
	MXTF (RCVR)			
	LOOP-NORMAL	LOOP		
7	*MXTF (BITE)*		Check 56 kb/s, external clock, operation as follows:	
	DIGITAL FUNCTION:	EXT CLK	a. Set strapping switches on UUR for 56 kb/s external clock (table 3-4), and install in channel 1 position of MXTF.	a. None. operation
			b. Connect test cables between BITE and UUR as follows:	b. None.

Test Cable Type	BITE Jack	UUR Jack
B (turret)	RCV CLK IN	RCV CLK
B (turret)	RCV DATA IN	RCV DATA
B (turret)	XMT CLK IN	XMT CLK OUT
A (bantam)	XMT CLK OUT	XMT CLK IN
A (bantam)	XMT DATA OUT	XMT DATA IN

			c. Observe SYNC BIT ERROR, and BER > 10^{-2} lamps on BITE. > 10^{-2} lamps off.	c. SYNC lamp illuminates on BIT ERROR and BER
8	*UUR*		Verify manual fault test capability of data module by observing lamps as follows.	
	FAULT:	press for steps a and b	a. FAULT lamp on PWR SPLY unit.	a. Lamp illuminates.
			b. FAULT lamp on multirate data module.	b. Lamp illuminates.
9			Check loss of external clock response as follows:	
			a. Disconnect type B test cable from XMT CLK IN on BITE.	a. None.
			b. Check response of UUR to loss of external clock by observing SYNC, BIT ERROR, and BER > 10^{-2} lamps on BITE.	b. SYNC lamp off; BIT ERROR and BER > 10^{-2} lamps illuminate.

3-38. Testing BITE Module

This test will measure the BITE module's VF oscillator outputs and will test BITE metering circuits using known VF inputs. It will also verify the accuracy of the BITE dc metering circuits and check BITE digital circuit clock outputs.

This test will qualify a BITE module for return to users.

a. Test Equipment.

(1) TA-855/U.

(2) TS-3329/U.

(3) AN/USM-281C.

(4) CP-772A/U.
(5) DMM.
(6) MXTF with the following accessories:
Extender board TRW 17191-010
Type A (bantam) test cables (2)
Type B (turret) test cables (3)
Type G test cable
Type J test cable

(7) Spare multirate data module.

b. Initial Equipment Setup. Set up test equipment and repaired BITE module as follows:

(1) Set power switch on PWR CONT unit in MXTF to OFF.

(2) Extend UUR in MXTF.

(3) Rotate SAMPLE RATE control 1/2-turn clockwise to apply power to CP-772A/U.

(4) Pull POWER switch on AN/USM-281C to on position.

(5) Set power switch on PWR CONT unit in MXTF to ON.

NOTE
Allow equipment to warm up for 5 minutes before proceeding with test.

c. Test Procedure. Verify performance of the UUR in accordance with the following test procedure.

Step	Control	Settings	Test procedure	Performance standard or fig. 3-46
1	*UUR* DIGITAL FUNCTION:	 CLK RATE 20 kb/s	With DMM, measure and record exact dc input voltages of BITE analog board (left connector) between pin 15A (ground) and each listed pin. **NOTE** **Although these readings are used only to verify accuracy of the UUR dc metering circuit, they should be within the voltage range indicated below.**	As listed below.
			Pin	
			14B	-52 ±6V
			7B	-42 ±4V
			6B	-38 ±2V
			2A	-13 ±2V
			9B	-13 ±2V
			1A	-7 ±1V
			2B	-5 ±0.7V
			3B	+7 ± 1V
			8B	+13 ±2V
			3A	+13 ±2V
2	*UUR* VF FUNCTION: DC SUPPLY SELECT:	 DCV As required	Rotate DC SUPPLY SELECT switch to each of its positions and compare indications on UUR meter with voltage recorded in step 1 above. Any difference between voltages should be within the recorded voltage tolerance listed below:	As listed below.

Switch Position	Extender Board Connector Pins	Recorded Voltage Tolerance
-48V	14B	±2.0V
-42V	7B	±2.0V
-38V	6B	±2.0V
-12V PS2	2A	±1.0V
-12V PS1	9B	±1.0V
-7V	1A	±0.7V
-5V	2B	±0.5V
+7V	SB	±0.7V
+12V PS1	8B	±1.0V
+12V PS2	3A	±1.0V

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-46
3	*UUR* DIGITAL FUNCTION: *MXTF (PWR CONT)* Power: TA-855/U RESPONSE: NOISE WTG: INPUT: RANGE: VF IN FUNCTION:	 POWER OFF OFF DAMP C-MSG TMS TERM 0 dBm 600 BAL	Connect type G test cable from VF OSC jack on UUR panel to INPUT 310 jack on TA-855/U.	
4	*MXTF (PWR CONT)* Power: *TA-855/U* POWER: *UUR* DIGITAL FUNCTION: VF FUNCTION: OSC LEV:	 ON ON CLK RATE 20 kb/s As required As required	Set VF FUNCTION and OSC LEV switches to positions indicated in a through f below, and observe performance standard on TA-855/U dBm meter. **VF FUNCTION Switch Position** / **OSC LEV Switch Position** a. CHANLEVXMT — 0 dB b. CHAN LEV XMT — -16 dB c. CHAN LEV RCV — 0 dB d. LOOP TEST — 0 dB e. LOOP TEST — -16 dB f. COM GAIN XMT — 0 dB	As listed below. a. 0 ±0.5 dBm. b. -16 ±0.5 dBm. c. -23.5 ±0.5 dBm. d. 0 ±0.5 dBm. e. -16 ±0.5 dBm. f. -13.5 ±0.5 dBm.
5	*TA-855/U* POWER:	 OFF	Remove type G test cable from between TA-855/U and UUR.	None.
6	*CP-772A/U* SENSITIVITY: TIME BASE: FUNCTION: *UUR* VF FUNCTION:	 1 1 µs FREQ COM GAIN XMT	Check oscillator frequency as follows: a. Connect type J between VF OSC jack on UUR and AC SIGNAL INPUT connector on CP-772A/U. Turn SAMPLE RATE control 1/2-turn clockwise to apply power to CP-772A/U. b. Measure frequency at VF OSC jack on UUR. Remove type J test cable between UUR and CP-772A/U.	a. None. b. 1020 ±20 Hz.
7	*TS-J329/U* FREQUENCY RANGE: FREQ Hz: FUNCTION: OUTPUT LEVEL: POWER:	 X100 10.2 600 -16.5 dBm ON	Connect type G test cable between VF METER jack on UUR panel and OUTPUT 310 jack on TS-3329/U.	None.
8	*TS-3329/U* OUTPUT LEVEL: *UUR* VF FUNCTION: METER ATTEN:	 As required As required	Set controls/switches as listed below, and observe performance standard for each As required setting on UUR meter. **OUTPUT LEVEL (TS-3329/U)** / **VF FUNCTION (UUR)** / **METER ATTEN (UUR)** -16.5 DBM — COM GAIN RCV — 0 dB -16.5 DBM — COM GAIN XMT — 0 dB 0 DBM — LOOP TEST — 0 dB 0 DBM — LOOP TEST — 10 dB -6.4 DBM — CHAN LEV XMT — 0 dB 0 DBM — CHAN LEV RCV — 0 dB 0 DBM — CHAN LEV RCV — 10 dB	As listed below. 0 ±0.4 dB 0 ±0.4 dB 0 .0.4 dB -10 ±2 dB 0 ±0.4 dB 0 ±0.4 dB -10 ±2 dB.

Step	Control	Setting	Trouble sectionalization chart	Normal indication or fig 3-46
9	*TS-3329/U*		Disconnect type G test cable from between	
	POWER:	OFF	VF METER jack on UUR and OUT-	
	UUR		PUT 310 jack on TS-3329/U. Observe	
	METER ATTEN:	0 DB	the following meter and lamp conditions:	
	VF FUNCTION:	SELF TEST	a. SELF TEST FAIL LAMP on BITE.	a. Lamp does not illuminate.
			b. UUR meter.	b. 0 ±0.4 dB.
10	*UUR*		Observe the following meter and lamp con-	
	METER ATTEN:	10 DB	ditions:	
			a. SELF TEST FAIL LAMP on UUR.	a. Lamp illuminates.
			b. UUR meter.	b. -10 ±1 dB.
11			Reconnect test cables and check the follow-	
I			ing:	
	UUR		a. Connect one end of type A (bantam)	a. 0V.
	ON HOOK-		test cable into SIG jack on UUR. Use	
	OFF HOOK:	ON HOOK	DMM to measure voltage between	
			ring and shield (ground) of loose	
			end.	
			CAUTION	
			Do not permit loose end of type A (bantam) test cable to short -42V off hook signal to ground.	
	UUR		b. Place switch in OFF HOOK position.	b. -41 ±3V.
	ON HOOK-		Use DMM to verify off hook voltage	
	OFF HOOK:	OFF HOOK	between ring (-42V) and shield of	
			loose end of type A (bantam) test	
			cable.	
12	*UUR*		At loose end of type A (bantam) test cable,	Lamp illuminates.
	ON HOOK-		short tip to shield and observe OFF	
	OFF HOOK:	ON HOOK	HOOK lamp on UUR.	
13	*UUR*		Observe SYNC and SELF TEST FAIL	SYNC lamp illuminates; SELF
	DIGITAL	SELF TEST	lamps on UUR.	TEST FAIL lamp is off.
	FUNCTION:			
	METER ATTEN:	0 DB		
14	*UUR*		Observe SYNC, BIT ERROR and BER	SYNC and BIT ERROR illumi-
	XMT ERROR	hold for step	$> 10^{-2}$ lamps on UUR.	nated; BER $> 10^{-2}$ is off.
	INJ:			
15	*UUR*		Connect type J cable between XMT CLK	Waveform A.
	DIGITAL	CLK RATE	OUT jack on UUR and the left channel	
	FUNCTION:	20 kb/s	input of the AN/USM-281C.	
	AN/US11-281C			
	VOLTS/DIV:	2V		
	(left)			
	TIME/DIV:	20 µs		
	TRIG SOURCE:	LEFT		
16	*UUR*		Check signal at XMT CLK OUT jack on	Waveform B.
	DIGITAL	CLK RATE	UUR.	
	FUNCTION:	50 kb/s		
	ANV/ US-281C			
	TIME/DIV:	10 µs		
17	*UUR*		Connect type J test cable between AC SIG-	19.693 ±0.5 kHz.
	DIGITAL	CLK RATE	NAL INPUT connector on CP-772A/U	
	FUNCTION:	20 kb/s	and XMT CLK OUT jack on UUR, and	
			observe output frequency.	
18	*UUR*		Leaving type J cable between AC SIGNAL	50.000 ±0.012 kHz.
	DIGITAL	CLK RATE	INPUT connector on CP-772A/U and	
	FUNCTION:	50 kb/s	XMT CLK OUT jack on UUR, observe	
			output frequency.	

Step	Control	Settings	Test procedure	Performance standard or fig. 3-46
19	*UUR* DIGITAL FUNCTION:	EXT CLK	Disconnect type J test cable. Install spare multirate data module in one of MXTF data channel positions, and verify UUR acceptance of external clock input as follows:	As listed below.
			Test Cable Type / **UUR Jack** / **Multirate Data Module Jack** B (turret) RCV CLK IN to RCV CLK B (turret) RCV DATA IN to RCV DATA B (turret) XMT CLK IN to XMT CLK OUT A (bantam) XMT CLK OUT to XMT CLK IN A (bantam) XMT DATA OUT to XMT DATA IN	
	MXTF (RCVR) LOOP-NORMAL:	LOOP	a. Observe SYNC, RCV CLK LOSS, BIT ERROR, and BER BER > 10^{-2} lamps on UUR.	a. SYNC lamp illuminates; RCV CLK LOSS, BIT ERROR, BER > 10^{-2} lamps off.
	LOOP-NORMAL:	NORMAL	b. Observe SYNC, RCV CLK LOSS, BIT ERROR, and BER > 10^{-2} lamps on UUR.	b. SYNC and RCV CLK LOSS lamp off; BIT ERROR, and BER > 10^{-2} lamps illuminate.

3-39. Testing Power Supply Group

The only power supply units that require performance testing are the TRF unit and the PWR SPLY unit. Instructions for testing these units are provided in the following paragraphs.

3-40. Testing TRF Unit

This test will verify that a TRF unit transforms ac input power into correct dc output power with acceptable ripple, and will qualify a unit for return to users.

WARNING

Hazardous voltage may be exposed during the following test. Follow all power-on and power-off instructions exactly, and avoid contact with electrical circuits at all times.

a. Test Equipment.

(1) AN/USM-281C.

(2) PMTF with the following accessories:
TRF test cable

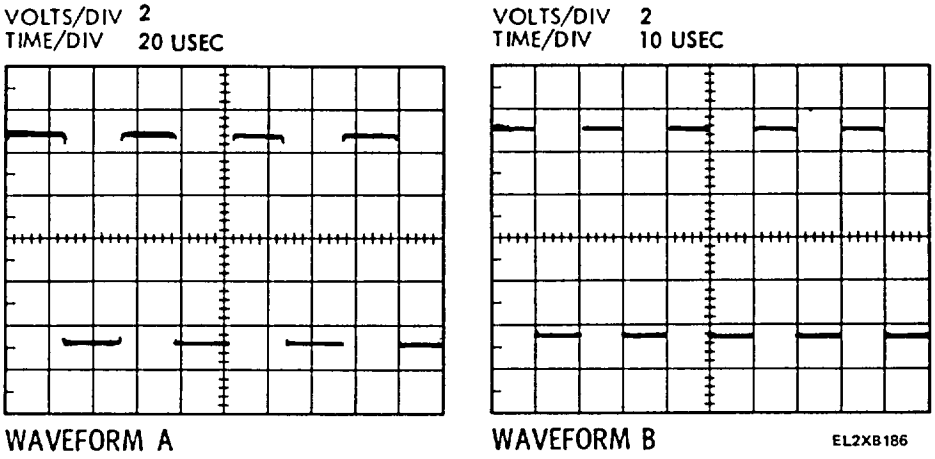


Figure 3-46. BITE test waveforms.

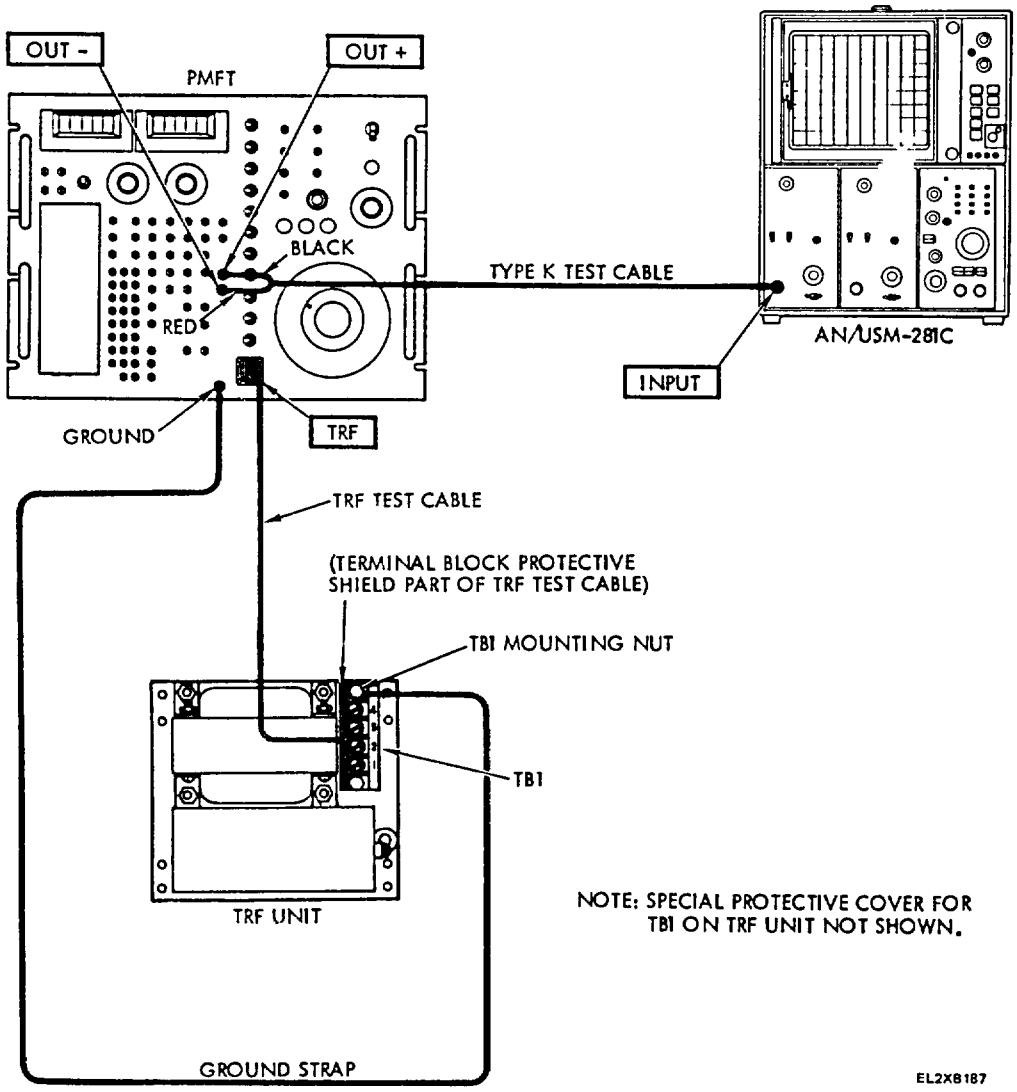


Figure 3-47. TRF unit performance test setup diagram.

Type K test cable

TRF cover with ground strap.

b. Initial Equipment Setup. Set up test equipment and repaired TRF unit as follows:

(1) Set POWER switch on PMTF to OFF.

(2) Remove protective cover from TB1 on UUR.

(3) Connect test equipment as shown in figure 3-47.

(4) Install special protective cover (supplied with PMTF) over TB1 on UUR; then, attach ground strap on cover to ground bus on PMTF.

(5) Verify that 230 Vac jumper is not installed between terminals 2 and 3 of TB2 on UUR, and that 117 Vac jumper is installed between terminals 1 and 3, and 2 and 4.

NOTE

Testing TRF in 117 volt configuration also verifies 230-volt operation.

(6) Set test equipment switches as follows:

Unit	*Switch*	*Setting*
PMTF	LOAD (11 switches)	OFF
	MODULE TEST	TRF TEST
	TRF INPUT LINE ADJUST	0 Vac
	OUTPUT SELECT	TRFIN
	FAULT SIMULATION (seven switches)	NORMAL
	POWER	ON
AN/USM-281C	VOLTS/DIV (left)	0.5V
	TIME/DIV	5.0 ms
	TRIG	LEFT
	COUPLING	AC
	POWER	Pull

NOTE

Allow equipment to warm up for 5 minutes before proceeding with test.

c. Test Procedure. Verify performance of the UUR in accordance with the following procedure.

Step	Control	Settings	Test procedure	Performance standard or fig. 3-47
1	*PMTF* TRF INPUT LINE ADJUST:	127 Vac	Observe UUR input on VOLTS readout on PMTF, and slowly turn TRF INPUT LINE ADJUST control.	127 ± 0.5 Vac.
2	*PMTF* OUTPUT SELECT:	TRFOUT	Observe performance standard on VOLTS display on PMTF.	-70 ± 2V.
3	*PMTF* TRF INPUT LINE ADJUST: LOADS TRF: OUTPUT SELECT:	115 Vac MIN TRFIN	Observe UUR input on PMTF VOLTS readout, and slowly turn TRF INPUT LINE ADJUST control to obtain exact input reading.	115 ± 0.5 Vac.
4	*PMTF* OUTPUT SELECT:	TRFOUT	Observe performance standard VOLTS and AMPS displays on PMTF.	-52 -6V. 1.0 ± 0.2 A.
5	*PMTF* LOADS TRF:	max	Verify maximum load performance of UUR by checking indication VOLTS and AMPS displays on PMTF.	-50 -6V. 3.4 ± 0.4A.
6			Check ripple content of -50 Vdc UUR output at OUT - and OUT + test points ON PMTF.	Ripple does not exceed 2.5V peak-to-peak.
7	*PMTF* TRF INPUT LINE ADJUST: POWER: TRF LOAD:	0 OFF OFF	Test is complete. Disconnect test equipment from UUR as follows: **WARNING** **Verify that POWER switch on PMTF is set to OFF.** a. Remove special protective cover from UUR TB1, and disconnect ground strap to PMTF.	None. a. None.

Step	Control	Settings	Test procedure	Performance standard or fig. 3-47
			b. Disconnect TRF test cable from TB1 terminals 1 through 4 on UUR from TRF connector on PMTF.	b. None.
			c. If necessary, restore user configuration of jumpers at TB2.	c. None.
			d. Reinstall normal protective cover on TB1.	d. None.

3-41. Testing PWR SPLY Unit

The PWR SPLY unit contains a monitor and alarm section and a dc-to-de converter. The unit is identical in both ac and dc power supply group configurations. This test will verify that both parts of the unit are functioning correctly, and will qualify the unit for return to users.

a. Test Equipment.

(1) AN/USM-281C (with X10 probe).

(2) AN/USM-223.

(3) PMTF.

b. Initial Equipment Setup. Set up test equipment and repaired PWR SPLY unit as follows:

(1) Set POWER switch on PMTF to OFF.

(2) Insert PWR SPLY unit into test position of PMTF.

(3) Set test equipment switches as follows:

Unit	*Switches*	*Setting*
PMTF	LOADS (all except TRF)	MIN
	OUTPUT SELECT	-48V
	MODULE TEST	INT MOD INPUT
	POWER	ON
AN/USM-281C	VOLTS/DIV (left)	02V
	TIME/DIV	10 ,s
	TRIG SOURCE	LEFT
	COUPLING	AC
	POWER	Pull
DMM	POWER	ON

NOTE

Allow equipment to warm up for 5 minutes before proceeding with test.

c. Test Procedure. Verify performance of the UUR in accordance with the following test procedure.

Step	Control	Settings	Test procedure	Performance standard
1	*PMTF* INTERNAL -48V ADJ:	As required	Adjust vernier control to obtain correct reading on VOLTS readout on PMTF.	-48 ± 0.1V.
2	OUTPUT SELECT: LOADS -42:	-42 MAX	Check supply maximum load reading on VOLTS and AMPS readouts on PMTF.	-42 ±4V 0.103 ±0.02 A.
3	*PMTF* LOADS -42:	MIN	Check supply minimum load reading on VOLTS and AMPS readouts on PMTF.	-42 +4V, 0.000 A.
4	PMTF OUTPUT SELECT: LOADS -38:	-38 MAX	Check supply maximum load reading on VOLTS and AMPS readouts on PMTF.	-38 2V 0.809 ±0.09 A.
5	*PMTF* LOADS -38:	MIN	Check supply minimum load reading on VOLTS and AMPS readouts on PMTF.	-38 ±2V 0.165 ±0.03 A.
6	*PMTF* OUTPUT SELECT: LOADS +7:	+7 MAX	Check supply maximum load reading on VOLTS and AMPS readouts on PMTF.	+6.7 -0.3V 2.231 ±0.3 A.
7	*PMTF* LOADS +7:	MIN	Check supply minimum load reading on VOLTS and AMPS readouts on PMTF.	+7 ±0.3V 0.410 ±0.04 A.
8	*PMTF* OUTPUT SELECT: LOADS -7:	-7 MAX	Check supply maximum load reading on VOLTS and AMPS readouts on PMTF.	-7 ±0.3V 2.03 ±0.2A.

Step	Control	Settings	Test procedure	Performance standard
9	*PMTF*		Check supply minimum load reading on	-7 +0.3V
	LOADS -7:	MIN	VOLTS and AMPS readouts on PMTF.	0.000A.
10	*PMTF*		Check supply maximum load reading on	-5 ±0.3V
	OUTPUT		VOLTS and AMPS readouts on PMTF.	0.294 ±0.03 A.
	SELECT:	-5(2)		
	LOADS -5(2):	MAX		
11	*PMTF*		Check supply minimum load reading on	-5 -0.3V
	LOADS -5(2):	MIN	VOLTS and AMPS readouts on PMTF.	0.000 A.
12	*PMTF*		Check supply maximum load reading on	-5 +0.3V
	OUTPUT		VOLTS and AMPS readouts on PMTF.	12.43 ±1.2 A.
	SELECT:	-5(1)		
	LOADS -5(1):	MAX		
13	*PMTF*		Check supply minimum load reading on	-5 -0.3V
	LOADS -5(1):	MIN	VOLTS and AMPS readouts on PMTF.	5.94 ±0.6 A.
14	*PMTF*		Check supply maximum load reading on	+12 ±0.5V
	OUTPUT		VOLTS and AMPS readouts on PMTF.	0.207 ±0.05 A.
	SELECT:	+12(1)		
	LOADS +12(1):	MAX		
15	*PMTF*		Check supply minimum load reading on	+12 ±0.5V
	LOADS +12(1):	MIN	VOLTS and AMPS readouts on PMTF.	0.185 ±0.02 A.
16	*PMTF*		Check supply maximum load reading on	-12 -±0.5V
	OUTPUT		VOLTS and AMPS readouts on PMTF.	0.214 ±0.02 A.
	SELECT:	-12(1)		
	LOADS -12(1):	MAX		
17	*PMTF*		Check supply minimum load reading on	-12 -0.5V
	LOADS -12(1):	MIN	VOLTS and AMPS readouts on PMTF.	0.157 ±0.02 A.
18	*PMTF*		Check supply maximum load reading on	+12 ±0.5V
	OUTPUT		VOLTS and AMPS readouts on PMTF.	0.015 ±0.002 A.
	SELECT:	+12%2)		
	LOADS +12(2):	MAX		
19	*PMTF*		Check supply minimum load reading on	+12 ±0.5V
	LOADS +12(2):	MIN	VOLTS and AMPS readouts on PMTF.	0.00 A.
20	*PMTF*		Check supply maximum load reading on	-12 -0.5V
	OUTPUT		VOLTS and AMPS readouts on PMTF.	0.029 ±0.003 A.
	SELECT:	-12(2)		
	LOADS -12(2):	MAX		
21	*PMTF*		Check supply minimum load reading on	-12 0.5V
	LOADS -12(2):	MIN	VOLTS and AMPS readouts on PMTF.	0.014 ±0.003 A.
22	*PMTF*		Check supply reading on VOLTS readout	+15 ±2V.
	OUTPUT		on PMTF.	
	SELECT:	+15		
23	*PMTF*		Check supply reading on VOLTS readout	-15 -2V.
	OUTPUT		on PMTF.	
	SELECT	-15		
24	*PMTF*		Momentarily place SHORT TEST switch	+5.9 ±0.6V
	OUTPUT		in the TEST position and observe VOLTS.	5.45 ±0.56 A.
	SELECT:	+7	and AMPS readout on PMTF.	
	SHORT TEST:	+7		
	LOADS +7:	MAX		
25	*PMTF*		Momentarily place the SHORT TEST	-7 ±-0.6V
	OUTPUT		switch in TEST position, and observe	5.7 ±0.6 A.
	SELECT:	-7	VOLTS and AMPS readouts on PMTF.	
	SHORT TEST:	-7		
	LOADS +7:	MIN		
	LOADS -7:	MAX		

Step	Control	Settings	Test procedure	Performance standard
26	*PMTF*		Perform the following:	
	OUTPUT SELECT:	-5(1)	a. Momentarily place the SHORT TEST switch in TEST position, and observe VOLTS and AMPS readouts on PMTF.	a. -5 -±0.3V 12.15 ±1.2 A.
	LOADS -7:	MIN		
	SHORT TEST:	-5		
	LOADS -5(1):	MAX		
			b. After performing step a above, set	b. None.
	LOAD -5(1) switch to MIN.			
27			Connect 10 to 1 probe of AN/USM-281C to each of the following test points. Connect ground lead to probe to DGD test point on PMTF. Check that peak-to-peak switching noise does not exceed performance standards indicated below: Less than	As listed below.
			a. -38	a. 2.0V p top
			b. -5(1)	b. 1.5V p to p
			c. -42	c. 2.0V p top
			d. +12(1)	d. 1.5V p to p
			e. +7	e. 1.5V p to p
			f. +12(2)	f. 1.5V p to p
			g. -12(1)	g. 2.0V p to p
			h. -7	h 1.5V p to p
			i. -12(2)	i. 2.0V p to p
			i. -5(2)	j. 1.5V p to p
28	*UUR*		Check ALARMS lamps on PWR SPLY unit.	Lamps illuminate.
	LAMP TEST:	press		
29	*PAMTF*		Check loss of output simulation by observing C.G.A. lamp on UUR.	Lamp illuminates.
	LSOUT:	FAULT		
30	*PMTF*		Check fault simulation activates FAULT lamp on UUR.	Lamp illuminates.
	LSOUT:	NORMAL		
	FLTBUS:	FAULT		
31	*PMTF*		Check loss of input simulation by observing C.G.A. lamp on UUR.	Lamp illuminates.
	FLTBUS:	NORMAL		
	LSIN:	FAULT		
32	*PMTF*		Check local loop simulation by observing LOCAL LOOP and C.G.A. lamps on UUR.	Lamps illuminate.
	LSIN:	NORMAL		
	LOCLP:	FAULT		
33	*PMTF*		Check remote loop simulation by observing REMOTE LOOP and C.G.A. lamps on UUR.	Lamps illuminate.
	LOCLP:	NORMAL		
	REMLP:	FAULT		
34	*PMTF*		Check loss of frame simulation by observing C.G.A. lamp on UUR.	Lamp illuminates.
	REMLP:	NORMAL		
	LSFR:	FAULT		
35	*PMTF*		Check remote alarm simulation by observing REMOTE ALARM and C.G.A. lamps on UUR.	Lamps illuminate.
	LSFR:	NORMAL		
	REMAL:	FAULT		
36	*PMTF*			
	REMAL:	NORMAL		
37			Using AN/USM-223, measure resistance between relay contacts for each of the PMTF control settings listed below:	
	PMTF		**Relay** **Contacts**	**Condition**
	LSOUT:	FAULT	a. K1 NO to C NC to O	a. Continuity Open.
		NORMAL	b. K1 NC to C NO to C	b. Continuity Open.

Step	Control	Settings	Test procedure			Performance standard	
				Relay	Contacts		Condition
	FLTBUS:	FAULT	c.	K2	NO to C	e.	Continuity
					NC to C		Open.
		NORMAL	d.	K2	NC to C	d.	Continuity
					NO to C		Open.
	LSIN:	FAULT	a.	KS	NO to C	a.	Continuity
					NC to C		Open.
		NORMAL	f.	K3	NC to C	f.	Continuity
					NO to C		Open.
	LOCLP:	FAULT	g.	K4	NO to C	g.	Continuity
					NC to C		Open.
		NORMAL	h.	K4	NC to C	h.	Continuity
					NO to C		Open.
	REMLP:	FAULT	i.	K5	NO to C	i.	Continuity
					NC to C		Open.
		NORMAL	j.	KS	NC to C	j.	Continuity
					NO to C		Open.
	LSFR:	FAULT	k.	K6	NO to C	k.	Continuity
					NC to C		Open.
		NORMAL	I.	K6	NC to C	I.	Continuity
					NO to C		Open.
	Power:	OFF	m.	K7	NC to C	m.	Continuity
					NO to C		Open.
		ON	n.	K7	NO to C	n.	Continuity
					NC to C		Open.
	LSIN:	FAULT	o.	K8	NO to C	o.	Continuity
					NC to C		Open.
		NORMAL	p.	K8	NC to C	p.	Continuity
					NO to C		Open.
	LSIN:	FAULT	q.	K9	NO to C	q.	Continuity (after approximately 15 ±5 seconds).
		NORMAL					None.
38			Using the AN/USM-223, check signal level between DGD (ground) test point on PMTF and each of following test points.				
	LOCLP:	NORMAL	a.	Measure force-all-ones output at FRC1 test point.		a.	-5 ± 0.6V
	LOCLP:	FAULT	b.	Measure force-all-ones output at FRC1 test point.		b.	0 ± 0.8V
	LOCLP. LSOUT.	NORMAL NORMAL	c.	Measure CGA output at CGA test point.		c.	-5 ± 0.5V
	LSOUT:	FAULT	d.	Measure CGA output at CGA test point.		d.	0 ± 0.5V
	LSOUT: LSIN	NORMAL NORMAL	e.	Measure CGA bus output at CGAB test point		e.	-5 ± 0.5V
	LSIN:	FAULT	f.	Measure CGA bus output at CGAB test point.		f.	0 ± 0.5V
	LSFR: LSIN	FAULT NORMAL	g.	Measure $\overline{\text{CGA}}$ bus output at $\overline{\text{CGAB}}$ test point.		g.	-5 ± 0.5V
	LSFR:	NORMAL	h.	Measure $\overline{\text{CGA}}$ bus output at $\overline{\text{CGAB}}$ test point.		h.	0 ± 0.5V
	REMAL:	NORMAL	i.	Measure CGA delay output at CGADLY test point.		i.	-5 ± 0.5V

Step	Control	Settings	Test procedure	Performance standard
	REMAL:	FAULT	j. Measure CGA delay output at CGADLY test point after approximately 15 ±5 seconds.	j. 0 ± 0 8V after 15 ± 5 seconds
	RMAL LSLN.	NORMAL NORMAL	k. Measure OGA output at OGA test point.	k. -5 ± 0.5V
	LSIN:	FAULT	l. Measure OGA output at OGA test point	l. 0 0.V
	LSIN: LSFR	NORMAL NORMAL	m. Measure OGA output at OGA test point.	n. -5 ± 0.5V
	LSFR:	FAULT	n. Measure OGA output at OGA test point.	n. 0 ±0.5V
39	PMTF LSFR: UUR CGA DEFEAT:	 FAULT press for step	Verify CGA DEFEAT switch prevents illumination of CGA lamp on UUR.	Lamp off.

3-42. Rear Assembly Testing

a. Test Equipment. The only test equipment required is the AN/USM-223.

b. Test Conditions and Connections. The rear assembly is tested by using the AN/USM-223 to verify wiring continuity and absence of shorts in accordance with the wiring data contained in appendix B.

c. Initial Test Equipment Settings. The rear assembly is placed on a bench, with no operating voltage applied. The multimeter is used to verify correct resistance readings for the repaired wiring in accordance with the wiring data. Normally these resistance readings will be open circuit or continuity and require no tolerance. If the acceptability of a particular reading is in doubt, remove all the units from the MXTF and perform the same point-to-point measurement for a correct reading for comparison.

APPENDIX A
REFERENCES

DA Pam 25-30	Consolidated Index of Technical Publications.
DA Pam 738-750	The Army Maintenance Management System (TAMMS).
TM 11-5102	Resistors, Decade ZM-16/U (NSN 6625-00-669-0266), ZM-16A/U, and ZM-16B/U.
TM 11-5805-617-14-4	Operator's, Organizational, Direct Support, and General Support Maintenance Manual Including Repair Parts and Special Tools Lists (Including Depot Maintenance Repair Parts and Special Tools List): Wescom Line Conditioning Equipment Network, Hybrid Circuit TA-855/G (Wescom Model No. 714B) and Terminating Unit, Telephone TA-852/G (Wescom Model No. 714H).
TM 11-5805-711-13	Operator's, Organizational and Direct Support Maintenance Manual: Multiplexer Sets AN/FCC-98(V)1 and AN/FCC-98(V)1X.
TM 11-6625-654-14	Operator's, Organizational, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools List) for Multimeter AN/USM-223.
TM 11-6625-1548-15	Organizational, Direct Support, General Support, and Depot Maintenance Manual: Counter, Electronic, Digital CP-772/U (Hewlett-Packard Model 5345).
TM 11-6625-2658-14	Operator's, Organizational, Direct Support, and General Support Maintenance Manual for Oscilloscope AN/USM-281C (NSN 6625-00-106-9622).
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

APPENDIX B

REAR ASSEMBLY WIRING DATA

B-1. General

This appendix contains a point-to-point list of rear assembly wiring connections for Multiplexer Set AN/FCC-98(V) (multiplexer set). It also contains electrical connector location and pin/socket arrangement diagrams.

B-2. Electrical Connectors

The locations of all electrical connectors used in the rear assembly are shown in figures B-1 and B-2. Figure B-1 shows the internal plug-in unit edge connector receptacles on the backplane grid, and figure B-2 shows the external connectors on the rear cover of the MXTF.

B-3. Electrical Pin/Socket Arrangement Diagram

Pin/socket arrangement diagrams for all electrical connectors used in the rear assembly are shown in figure B-3.

B-4. Wire Connection List

An alphanumeric double-entry list of all FROM-TO connections used in the rear assembly including spare connections, are contained in table B-1. Instructions for using the list are given below:

a. FROM column. Locate known connector-pin in the alphanumerically arranged FROM column. All pins are listed one time, and only one time, in this column. If a pin is connected to more than a single pin in the TO column, the FROM column will be blank until all common TO connections have been listed. Each such multiple connection arrangement is considered a network in which the single FROM connection is considered, for reference purpose, as the network identifier. When one of the TO column pins appears in the FROM columns, reference will be made to the associated network instead of repeating all common connections.

b. TO Column. Determine which connector pin is electrically connected to the known pin in the FROM column by reading across the page to the listing in the adjacent TO column. If a network reference is listed in the TO column, locate the network referenced in the FROM column.

c. Descriptor Column. If necessary, determine data carried on a wire by reference to its descriptor. Each descriptor is an abbreviation of the purpose the wire fulfills. It may be more detailed than the actual signal names used in the text and on schematics. For example, XMTCHCTR2 means the wire carries channel counter transmit data for channel 2. The descriptions may also be used to determine common wiring connections, i.e., all wires having identical descriptors have common connection points in the rear assembly.

d. REF DES Column. The REF DES column contains alpha codes for signals common to the multiple connections of the DTG. These codes serve as useful aids in several ways. They-permit ready identification of link common to the same signal and they provide an easy-to-locate wire list of signals on the

schematics in the back of the manual. The first character of the REF DES also identifies the module from which the signal originates. The module code is as listed below:

REF DES code (first letter)	*DTG module*
A,B,C	PCM module
D,E,F,G	MUX module
H,I,J,K	DRIVER module
L,M,N,O,P	RCVR module
Q,R,S,T	DEMUX module
Q,V,W,X,Y,Z	PCD module

e. List Continuation. The wire connection list is arranged in the same manner as text in a two-column book, i.e., the bottom of the leftmost FROM column is continued at the top of the rightmost FROM column. That column is continued at the top of the leftmost FROM column on the following page.

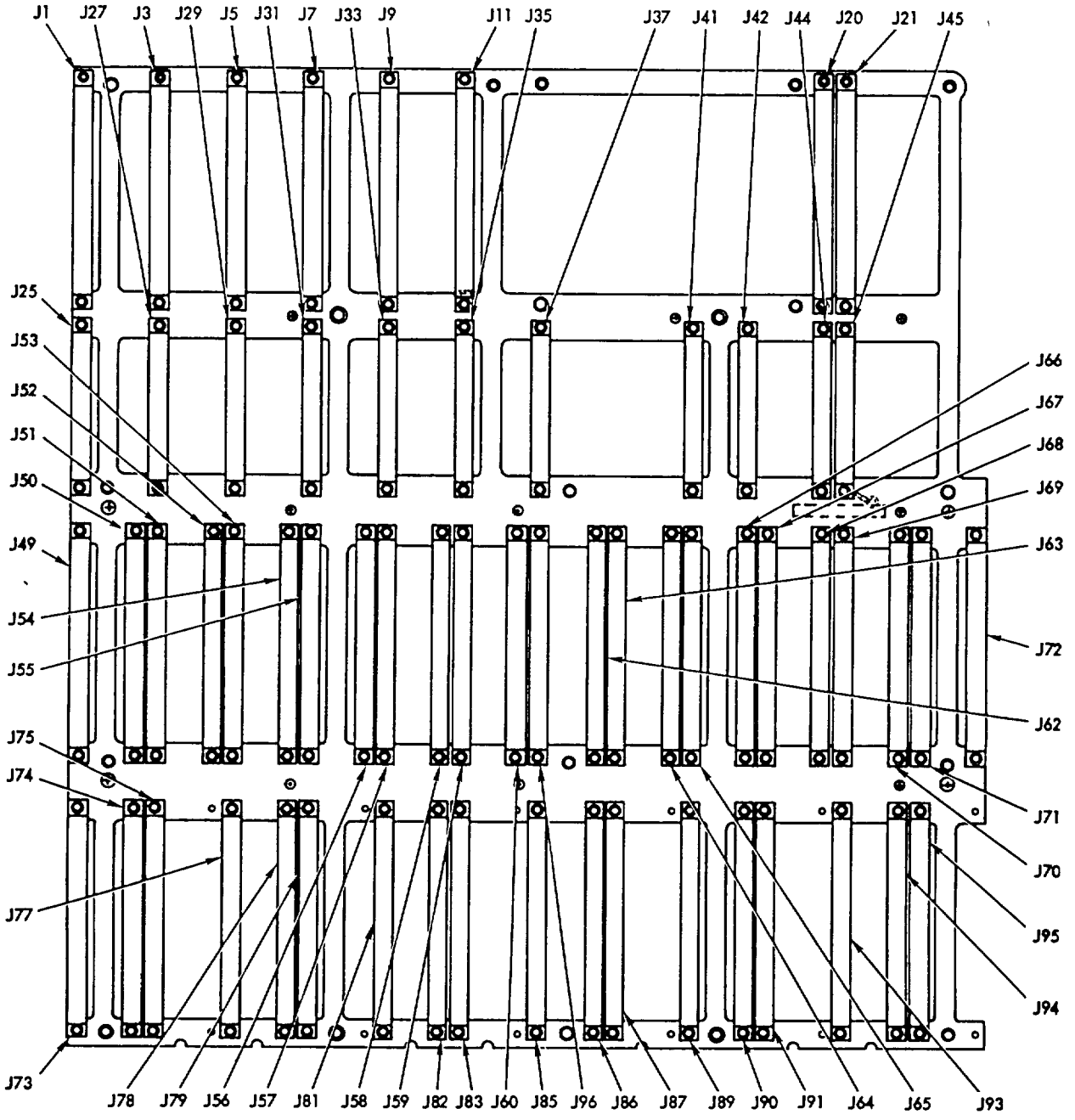


Figure B-1. Internal electrical connector location diagram, rear view.

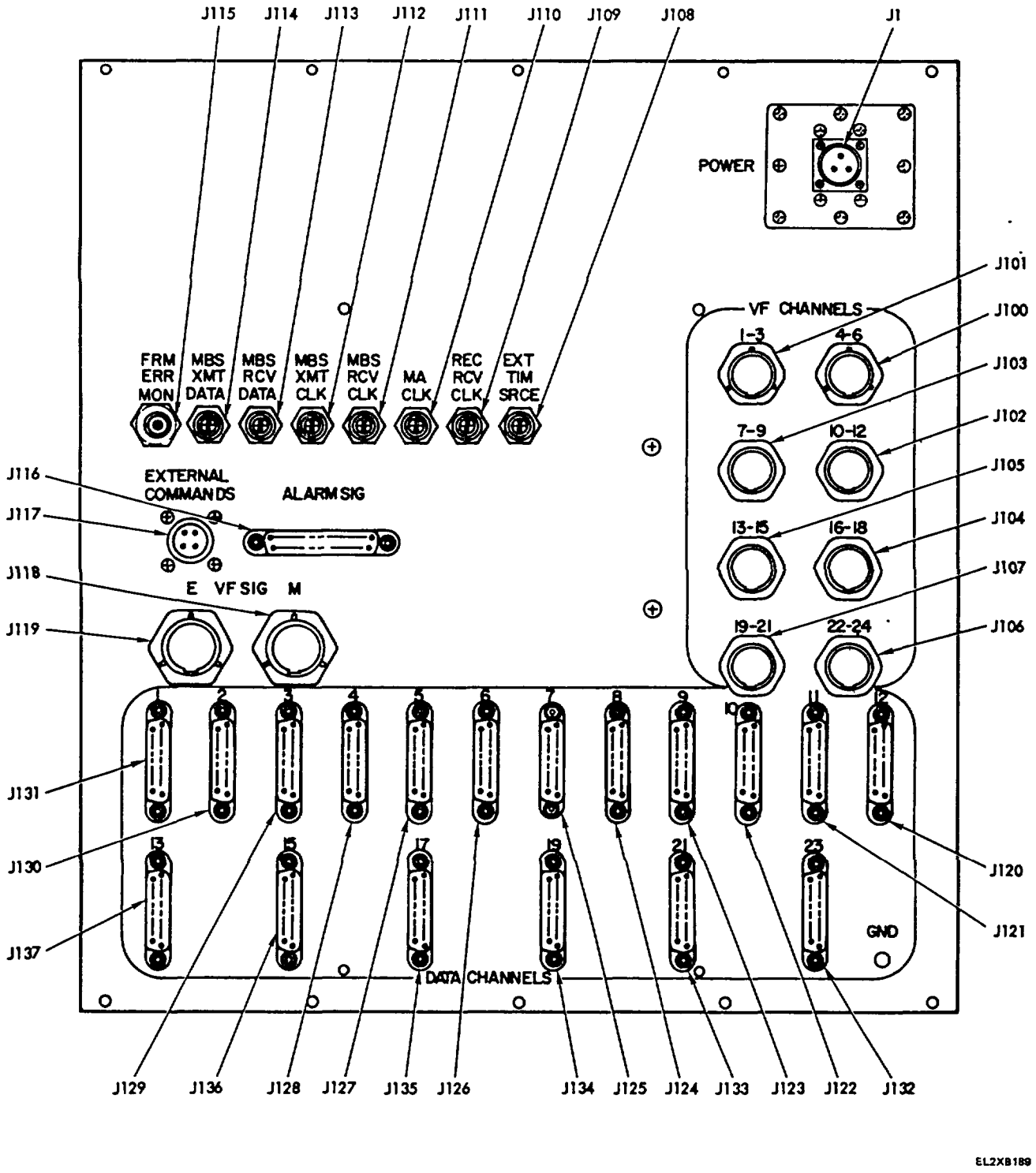


Figure B-2. External electrical connector location diagram.

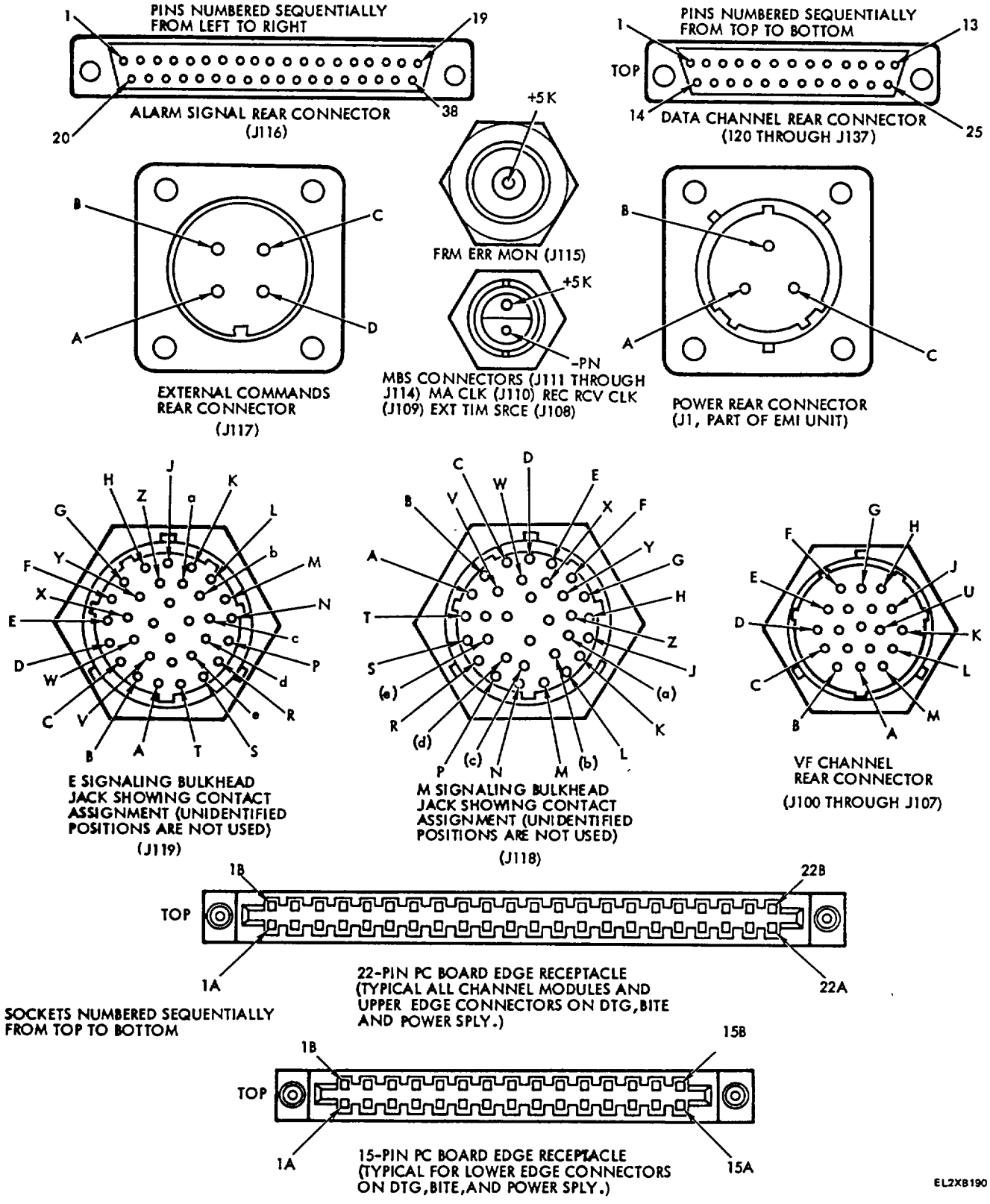


Figure B-3. Electrical pin/socket arrangement diagrams.

Table B-1. Rear Assembly Wire Connection List

FROM	TO	REF. DESG.	SIGNAL NAME
E 1-2	E 101	AAE	CHASSISGND
	E 102	AAE	CHASSISGND
	E 103	AAE	CHASSISGND
	E 104	AAE	CHASSISGND
	E 105	AAE	CHASSISGND
	E 106	AAE	CHASSISGND
	E 107	AAE	CHASSISGND
	E 108	AAE	CHASSISGND
	E 109	AAE	CHASSISGND
	E 110	AAE	CHASSISGND
	E 111	AAE	CHASSISGND
	E 112	AAE	CHASSISGND
	E 113	AAE	CHASSISGND
	E 114	AAE	CHASSISGND
	E 115	AAE	CHASSISGND
	E 116	AAE	CHASSISGND
	E 117	AAE	CHASSISGND
	E 118	AAE	CHASSISGND
	E 119	AAE	CHASSISGND
	E 120	AAE	CHASSISGND
	E 121	AAE	CHASSISGND
	E 122	AAE	CHASSISGND
	E 123	AAE	CHASSISGND
	E 124	AAE	CHASSISGND
	E 125	AAE	CHASSISGND
	E 126	AAE	CHASSISGND
	E 127	AAE	CHASSISGND
	E 128	AAE	CHASSISGND
	E 129	AAE	CHASSISGND
	J21 7A	AAE	CHASSISGND
	J21 7B	AAE	CHASSISGND
	J100 -U	¬¬¬	CHASSGNDVFCH
	J101 -U	¬¬¬	CHASSGNDVFCH
	J102 -U	¬¬¬	CHASSGNDVFCH
	J103 -U	¬¬¬	CHASSGNDVFCH
	J104 -U	¬¬¬	CHASSGNDVFCH
	J105 -U	¬¬¬	CHASSGNDVFCH
	J106 -U	¬¬¬	CHASSGNDVFCH
	J107 -U	¬¬¬	CHASSGNDVFCH
	J116 19	¬¬¬	CHASSISGND
	J118 -J	¬¬¬	CHASMSIGGND
	J119 -J	¬¬¬	CHASESIGGND
	J120 1	¬¬¬	CHASSGNDCH12
	J121 1	¬¬¬	CHASSGNDCH11
	J122 1	¬¬¬	CHASSGNDCH10
	J123 1	¬¬¬	CHASSGNDCH9
	J124 1	¬¬¬	CHASSGNDCH8
	J125 1	¬¬¬	CHASSGNDCH7
	J126 1	¬¬¬	CHASSGNDCH6
	J127 1	¬¬¬	CHASSGNDCH5
	J128 1	¬¬¬	CHASSGNDCH4
	J129 1	¬¬¬	CHASSGNDCH3
	J130 1	¬¬¬	CHASSGNDCH2
	J131 1	AAF	CHASSGNDCH1
	J132 1	¬¬¬	CHASSGNDCH23
	J133 1	¬¬¬	CHASSGNDCH21
	J134 1	¬¬¬	CHASSGNDCH19
	J135 1	¬¬¬	CHASSGNDCH17
	J136 1	¬¬¬	CHASSGNDCH15
	J137 1	¬¬¬	CHASSGNDCH13
E 101	REFER TO NETWORK		E 1-2
E 102	REFER TO NETWORK		E 1-2
E 103	REFER TO NETWORK		E 1-2
E 104	REFER TO NETWORK		E 1-2
E 105	REFER TO NETWORK		E 1-2
E 106	REFER TO NETWORK		E1-2
E 107	REFER TO NETWORK		1-2

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
E 108	REFER TO NETWORK		E 1-2
E 109	REFER TO NETWORK		E 1-2
E 110	REFER TO NETWORK		E 1-2
E 111	REFER TO NETWORK		E 1-2
E 112	REFER TO NETWORK		E 1-2
E 113	REFER TO NETWORK		E 1-2
F 114	REFER TO NETWORK		E 1-2
E 115	REFER TO NETWORK		E 1-2
E 116	REFER TO NETWORK		E 1-2
E 117	REFER TO NETWORK		E 1-2
E 118	REFER TO NETWORK		E 1-2
E 119	REFER TO NETWORK		E 1-2
E 120	REFER TO NETWORK		E 1-2
E 121	REFER TO NETWORK		E 1-3
E 122	REFER TO NETWORK		E 1-2
E 123	REFER TO NETWORK		E 1-2
E 124	REFER TO NETWORK		E 1-2
E 125	REFER TO NETWORK		E 1-2
E 126	REFER TO NETWORK		E 1-2
E 127	REFER TO NETWORK		E 1-2
E 128	REFER TO NETWORK		E 1-2
E 129	REFER TO NETWORK		E 1-2
J1 1A	J1 1H	AAA	XMT+12V-1
	J3 1A	AAA	XMT+12V-1
	J3 1B	AAA	XMT+12V-1
	J5 1A	AAA	XMT+12V-1
	J5 1B	AAA	XMT+12V-1
	J20 14B	AAA	XMT+12V-1
J1 1B	REFER TO NETWORK		J1 1A
J1 10A	J27 4A		FG EC23-
J1 10B	J11 8A		AAG -38V
	J37 6B		AAG -38VBITE
	J42 1B		AAG -38VVF
	J42 2B		AAG -38VVF
	J42 3B		AAG -38VVF
	J42 4B		AAG -38VVF
	J44 3A		AAG -38V
	J44 4A		AAG -38VVF
	J49 3A		AAG -38VVF
	J49 3B		AAG -38VVF
	J51 3A		AAG -38VVF
	J51 3B		AAG -38VVF
	J53 3A		AAG -38VVF
	J53 3B		AAG -38VVF
	J55 3A		AAG -38VVF
	J55 3B		AAG -3AVVF
	J57 3A		AAG -39VVF
	J57 3B		AAG -38VVF
	J59 3A		AAG -38VVF
	J59 3B		AAG -33VVF

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
	J61 3A	AAG	-38VVF
	J61 3B	AAG	-38VVF
	J63 3A	AAG	-38VVF
	J63 3B	AAG	-38VVF
	J65 3A	AAG	-38VVF
	J65 3B	AAG	-38VVF
	J67 3A	AAG	-38VVF
	J67 3B	AAG	-33VVF
	J69 3A	AAG	-38VVF
	J69 3B	AAG	-38VVF
	J71 3A	AAG	-38VVF
	J71 3B	AAG	-38VVF
	J73 3A	AAG	-38VVF
	J73 3B	AAG	-38VVF
	J75 3A	AAG	-38VVF
	J75 3B	AAG	-38VVF
	J77 3A	AAG	-38VVF
	J77 3B	AAG	-38VVF
	J79 3A	AAG	-38VVF
	J79 3B	AAG	-38VVF
	J81 3A	AAG	-38VVF
	J81 3B	AAG	-38VVF
	J83 3A	AAG	-38VVF
	J83 3B	AAG	-38VVF
	J85 3A	AAG	-38VVF
	J85 3B	AAG	-38VVF
	J87 3A	AAG	-38VVF
	J87 3B	AAG	-38VVF
	J89 3A	AAG	-38VVF
	J89 3B	AAG	-38VVF
	J91 3A	AAG	-38VVF
	J91 3B	AAG	VF-38V
	J93 3A	AAG	-38VVF
	J93 3B	AAG	-3BVVF
	J95 3A	AAG	-38VVF
	J95 3B	AAG	-38VVF
J1 11A	J3 11B	AZ	XMTBFSCLK

FROM	TO	REF. DESG.	SIGNAL NAME
	J5 11A	AZ	XMTMBSCLK
	J31 11A	AZ	LOOBACKCLK
J1 11B	J3 16B	AY	XMT1.544MHZCL
	J5 12A	AY	XMT1.544MHZCL
J1 12A	J3 12A	CA	XMTPCM
J1 12B	J49 10A	A	XMTSIGA
	J51 10A	AE	XMTSIGA
	J53 10A	AE	XMTSIGA
	J55 10A	AE	XMTSIGA
	J57 10A	AE	XMTSIGA
	J59 10A	AE	XMTSIGA
	J61 10A	AF	XMTSIGA
	J63 10A	AE	XMTSIGA
	J65 10A	AE	XMTSIGA
	J67 10A	AE	XMTSIGA
	J69 10A	AE	XMTSIGA
	J71 10A	AE	XMTSIGA
	J73 10A	AE	XMTSIGA
	J75 10A	AE	XMTSIGA
	J77 10A	AE	XMTSIGA
	J79 10A	AE	XMTSIGA
	J81 10A	AE	XMTSIGA
	J83 10A	AE	XMTSIGA
	J85 10A	AE	XMTSIGA
	J87 10A	AE	XMTSIGA
	J89 10A	AE	XMTSIGA
	J91 10A	AE	XMTSIGA
	J93 10A	AE	XMTSIGA
	J95 10A	AE	XMTSIGA
J1 13A	J27 1A	FD	EC20-
J1 13B	J3 10A	AX	XMTADVCHCTR-
J1 14A	J53 2A	CD	XMTVFIN3

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J1 14B	J27 13B	FS	SAMPLESTD-
J1 15A	J51 2A	CC	XMTVFIN2
J1 15B	J27 14B	FT	A/DSTART
J1 16A	J49 2A	CB	XMTVFIN1
J1 16B	J27 11B	FU	EC0-
J1 17A	J61 2A	CH	XMTVFIN7
J1 17B	J27 12B	FV	EC1-
J1 18A	J55 2A	CE	XMTVFIN4
J1 18B	J5 18B	¬¬¬	XMT24CHMODE-
J1 19A	J59 2A	CG	XMTVFIN6
J1 19B	J3 19A	FR	A/DCLK
J1 2A	J1 2B	AAB	XMT-12V-1
	J3 2A	AAB	XMT-12V-1
	J3 2B	AAB	XMT-12V-1
	J5 2A	AAB	XMT-12V-1
	J5 2B	AAB	XMT-12V-1
	J20 22B	AAB	XMT-12V-1
J1 2B	REFER TO NETWORK J1 2A		
J1 20A	J57 2A	CF	XMTVFIN5
J1 20B	J1 22B	AAL	AGND
	J25 11B	AAL	AGND
	J25 5B	AAL	AGND
	J44 2B	AAL	AGND
	J53 1B	RD	XMTVFRET3
	J55 1B	BE	XMTVFRET4
	J57 1B	BF	XMTVFRET5
	J59 1B	BG	XMTVFRET6
	J69 1B	RL	XMTVFRET11
	J73 1B	BN	XMTVFRET13
	J81 1B	BR	XMTVFRET17
J1 21A	J63 2A	CI	XMTVFIN8
J1 21B	J49 1B	BB	XMTVFRET1
	J51 1B	BC	XMTVFRET2
	J61 1B	RH	XMTVFRET7
	J63 1B	BI	XMTVFRET8
J1 22A	J69 2A	CL	XMTVFIN11
J1 22B	REFER TO NETWORK J1 20B		
J1 34	J1 3B	AAC	-5V-1
	J3 18B	AAC	-5V-1
	J3 3A	AAC	-5V-1
	J3 3B	AAC	-5V-1
	J5 13A	AAC	-5V-1
	J5 3A	AAC	-5V-1
	J5 3B	AAC	-5V-1
	J7 3A	AAC	-5V-1
	J7 3B	AAC	-5V-1
	J9 3A	AAC	-5V-1
	J9 3B	AAC	-5V-1
	J11 3A	AAC	-5V-1
	J11 3B	AAC	-5V-1
	J20 5A	AAC	-5V-1
	J20 6A	AAC	-5V-1
	J21 10B	AAC	-5V-1
	J21 11B	AAC	-5V-1
	J21 8A	AAC	-5V-1
	J21 8B	AAC	-5V-1

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J21	9A	AAC	-5V-1
J21	9B	AAC	-5V-1
J27	15B	AAC	-5V-1
J29	10A	AAC	-5V-1
J29	11A	AAC	-5V-1
J29	11B	AAC	-5V-1
J29	12A	AAC	-5V-1
J29	12B	AAC	-5V-1
J29	13A	AAC	-5V-1
J29	13B	AAC	-5V-1
J29	14A	AAC	-5V-1
J29	14B	AAC	-5V-1
J29	15A	AAC	-5V-1
J29	15B	AAC	-5V-1
J29	9A	AAC	-5V-1
J49	7A	A4C	-5V-1
J49	7B	AAC	-5V-1
J50	7A	AAC	-5V-1
J50	7B	AAC	-5V-1
J51	7A	AAC	-5V-1
J51	7B	AAC	-5V-1
J52	7A	AAC	-5V-1
J52	7B	AAC	-5V-1
J53	7A	AAC	-5V-1
J53	7B	AAC	-5V-1
J54	7A	AAC	-5V-1
J54	7B	AAC	-5V-1
J55	7A	AAC	-5V-]
J55	7B	AAC	-5V-I
J56	7A	AAC	-5V-1
J56	7B	AAC	-5V-1
J57	7A	AAC	-5V-1
J57	7B	AAC	-5V-1
J58	7A	AAC	-5V-1
J58	7B	AAC	-5V-1
J59	7A	AAC	-5V-1
J59	7B	AAC	-5V-1
J60	7A	AAC	-5V-1
J60	7B	AAC	-5V-1
J61	7A	AAC	-5V-1
J61	7B	AAC	-5V-1
J62	7A	AAC	-5V-1
J62	7B	AAC	-5V-1
J63	7A	AAC	-5V-1
J63	7B	AAC	-5V-1
J64	7A	AAC	-5V-1
J64	7B	AAC	-5V-1
J65	7A	AAC	-5V-1
J65	7B	AAC	-5V-1
J66	7A	AAC	-5V-1
J66	7B	AAC	-5V-1
J67	7A	AAC	-5V-1
J67	7B	AAC	-5V-1
J68	7A	AAC	-5V-1
J68	7B	AAC	-5V-1
J69	7A	AAC	-5V-1
J69	7B	AAC	-5V-1
J70	7A	AAC	-5V-1
J70	7B	AAC	-5V-1
J71	7A	AAC	-5V-1
J71	7B	AAC	-5V-1
J72	7A	AAC	-5V-1
J72	7B	AAC	-5V-1
J73	7A	AAC	-5V-1
J73	7B	AAC	-5V-1
J74	7A	AAC	-5V-1
J74	7B	AAC	-5V-1
J75	7A	AAC	-5V-1
J75	7B	AAC	-5V-1
J77	7A	AAC	-5V-1
J77	7B	AAC	-5V-1
J78	7A	AAC	-5V-1
J78	7B	AAC	-5V-1
J79	7A	AAC	-5V-1
J79	7B	AAC	-5V-1
J81	7A	AAC	-5V-1

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
	J81 7B	AAC	-5V-1
	J82 7A	AAC	-5V-1
	J82 7B	AAC	-5V-1
	J83 7A	AAC	-5V-1
	J83 7B	AAC	-5V-1
	J85 7A	AAC	-5V-1
	J85 7B	AAC	-5V-1
	J86 7A	AAC	-5V-1
	J86 7B	AAC	-5V-1
	J87 7A	AAC	-5V-1
	J87 7B	AAC	-5V-1
	J89 7A	AAC	-5V-1
	J89 7B	AAC	-5V-1
	J90 7A	AAC	-5V-1
	J90 7B	AAC	-5V-1
	J91 7A	A4C	-5V-1
	J91 7B	AAC	-5V-1
	J93 7A	AAC	-5V-1
	J93 7B	AAC	-5V-1
	J94 7A	AAC	-5V-1
	J94 7B	AAC	-5V-1
	J95 7A	AAC	-5V-1
	J95 7B	AAC	-5V-1
J1 3B	REFER TO NETWORK	J1 34	
J1 4B	J3 13A	FN	SD7+SD8
J1 5A	J27 5A	FH	EC24-
J1 5B	J3 10B	AW	XMTRESETTOCH1
	J5 21B	AW	XMTPESETTOCH1
J1 6A	J1 6B	AAF	DGND
	J3 6A	AAF	DGND
	J3 6B	AAF	DGND
	J5 6A	A4F	DGND
	J5 6B	AAF	DGND
	J5 9A	AAF	DGND
	J7 6A	AAF	DGND
	J7 6B	AAF	DGND
	J9 6A	AAF	DGND
	J9 6B	AAF	DGND
	J11 6A	AAF	DGND
	J11 6B	AAF	DGND
	J20 18A	AAF	FLEADRET
	J21 17B	AAF	DGND
	J21 18B	AAF	DGND
	J21 20B	AAF	CHUDGNO
	J21 21A	AAF	CHUDGND
	J21 21B	AAF	DGND
	J29 2A	AAF	DGND
	J31 11B	AAF	DGND
	J31 12A	AAF	DGND
	J31 12B	AAF	DGND
	J31 13B	AAF	DGND
	J31 14A	AAF	DGND
	J31 15A	AAF	DGND
	J31 4A	AAF	DGND
	J31 5A	AAF	DGND
	J31 6A	AAF	DGND
	J31 7B	AAF	DGND
	J31 8A	AAF	DGND
	J31 8B	AAF	DGND
	J31 9A	AAF	DGND
	J31 9B	AAF	DGND
	J33 2B	AAF	DGND
	J41 9A	AAF	DGNDBITE
	J41 9B	AAF	DGNDBITE
	J50 6A	AAF	DGND
	J50 6B	AAF	DGND
	J52 6A	AAF	DGND
	J52 6B	AAF	DGND
	J54 6A	AAF	DGND
	J54 6B	AAF	DGND
	J56 6A	AAF	DGND

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
	J56 6B	AAF	DGND
	J58 6A	AAF	DGND
	J58 6B	AAF	DGND
	J60 6A	AAF	DGND
	J60 6B	AAF	DGND
	J62 6A	AAF	DGND
	J62 6B	AAF	DGND
	J64 6A	AAF	DGND
	J64 6B	AAF	DGND
	J66 6A	AAF	DGND
	J66 6B	AAF	DGND
	J68 6A	AAF	DGND
	J68 6B	AAF	DGND
	J70 6A	AAF	DGND
	J70 6B	AAF	DGND
	J72 6A	AAF	DGND
	J72 6B	AAF	DGND
	J73 6A	AAF	DGND
	J73 6B	AAF	DGND
	J74 6A	AAF	DGND
	J74 6B	AAF	DGND
	J75 6A	AAF	DGND
	J75 6B	AAF	DGND
	J77 6A	AAF	DGND
	J77 6B	AAF	DGND
	J78 6A	AAF	DGND
	J78 6B	AAF	DGND
	J79 6A	AAF	DGND
	J79 6B	AAF	DGND
	J81 6A	AAF	DGND
	J81 6B	AAF	DGND
	J82 6A	AAF	DGND
	J82 6B	AAF	DGND
	J83 6A	AAF	DGND
	J83 6B	AAF	DGND
	J85 6A	AAF	DGND
	J85 6B	AAF	DGND
	J86 6A	AAF	DGND
	J86 6B	AAF	DGND
	J87 6A	AAF	DGND
	J87 6B	AAF	DGND
	J89 6A	AAF	DGND
	J89 6B	AAF	DGND
	J90 6A	AAF	DGND
	J90 6B	AAF	DGND
	J91 6A	AAF	DGND
	J91 6B	AAF	DGND
	J93 6A	AAF	DGND
	J93 6B	AAF	DGND
	J94 6A	AAF	DGND
	J94 6B	AAF	DGND
	J95 6A	AAF	DGND
	J95 6B	AAF	DGND
	J117 -C	AAF	DGND
	J119 -BB	¬¬¬	FLEADRET
	J120 7	¬¬¬	CH12SIGNALGND
	J121 7	¬¬¬	CH11SIGNALGND
	J122 7	¬¬¬	CH10SIGNALGND
	J123 7	¬¬¬	CH9SIGNALGND
	J124 7	¬¬¬	CH8SIGNALGND
	J125 7	¬¬¬	CH7SIGNALGND
	J126 7	¬¬¬	CH6SIGNALGND
	J127 7	¬¬¬	CH5SIGNALGND
	J128 7	¬¬¬	CH4SIGNALGND
	J129 7	¬¬¬	CH3SIGNALGND
	J130 7	¬¬¬	CH2SIGNALGND
	J131 7	¬¬¬	CH1SIGNALGND
	J132 7	¬¬¬	CH23SIGNALGND
	J133 7	¬¬¬	CH21SIGNALGND
	J134 7	¬¬¬	CH19SIGNALGND
	J135 7	¬¬¬	CH17SIGNALGND
	J136 7	¬¬¬	CH15SIGNALGND
	J137 7	¬¬¬	CH13SIGNALGND
J1 68		REFER TO NETWORK	J1 6A
J1 76	J45 4B	AAO	+7V

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
	J45 5B	AAO	+7VDCU
	J45 6B	AAO	+7V
	J74 14A	AAO	+7VDCU
	J74 14B	AAO	+7VDCU
	J78 14A	AAO	+7VDCU
	J78 14B	AAO	+7VDCU
	J82 14A	AAO	+7VDCU
	J82 14B	AAO	+7VDCU
	J86 14A	AAO	+7VDCU
	J86 14B	AAO	+7VDCU
	J90 14A	AAO	+7VDCU
	J90 14B	AAO	+7VDCU
	J94 14A	AAO	+7VDCU
	J94 14B	AAO	+7VDCU
J1 8A	J27 2A	FE	EC21-
J1 8B	J3 8B	FJ	FLTALMBUS-
	J5 8B	FJ	FLTALMBUS-
	J7 8B	FJ	FLTALMBUS-
	J9 8B	FJ	FLTALMBUS-
	J11 8B	FJ	FLTALMBUS-
	J20 7B	FJ	FLTALMBUS-
	J50 18B	FJ	FLTALMBUS-
	J52 18B	FJ	FLTALMBUS-
	J54 18B	FJ	FLTALMBUS-
	J56 18B	FJ	FLTALMBUS-
	J58 18B	FJ	FLTALMBUS-
	J60 18B	FJ	FLTALMBUS-
	J62 18B	FJ	FLTALMBUS-
	J64 18B	FJ	FLTALMBUS-
	J66 18B	FJ	FLTALMBUS-
	J68 18B	FJ	FLTALMBUS-
	J70 18B	FJ	FLTALMBUS-
	J72 18B	FJ	FLTALMBUS-
	J74 18B	FJ	FLTALMBUS-
	J78 18B	FJ	FLTALMBUS-
	J82 18B	FJ	FLTALMBUS-
	J86 18B	FJ	FLTALMBUS-
	J90 18B	FJ	FLTALMBUS-
	J94 18B	FJ	FLTALMBUS-
J1 9A	J27 3A	FF	EC22-
J1 9B	J3 9A	AV	XNTFRAME6+12-
J3 1A	REFER TO NETWORK		J1 1A
J3 1B	REFER TO NETWORK		J1 1A
J3 10A	REFER TO NETWORK		J1 13B
J3 10B	REFER TO NETWORK		J1 5B
J3 11A	J50 19B	DP	XMTDATABUSCLK
	J52 19B	DP	XMTDATABUSCLK
	J54 19B	DP	XMTDATABUSCLK
	J56 19B	DP	XMTDATABUSCLK
	J58 19B	DP	XMTDATABUSCLK
	J60 19B	DP	XMTDATABUSCLK
	J62 19B	DP	XMTDATABUSCLK
	J64 19B	DP	XMTDATABUSCLK
	J66 19B	DP	XMTDATABUSCLK
	J68 19B	DP	XMTDATABUSCLK
	J70 19B	DP	XMTDATABUSCLK
	J72 19B	DP	XMTDATABUSCLK
	J74 19B	DP	XMTDATABUSCLK
	J78 19B	DP	XMTDATABUSCLK
	J82 19B	DP	XMTDATABUSCLK
	J86 19B	DP	XMTDATABUSCLK
	J90 19B	DP	XMTDATABUSCLK
	J94 19B	DP	XMTDATABUSCLK
J3 11B	REFER TO NETWORK		J1 11A
J3 12A	REFER TO NETWORK		J1 12A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J3 12B	J50 10B	DC	XMTDATA
	J52 10B	DC	XMTDATA
	J54 10B	DC	XMTDATA
	J56 10B	DC	XMTDATA
	J58 10B	DC	XMTDATA
	J60 10B	DC	XMTDATA
	J62 10B	DC	XMTDATA
	J64 10B	DC	XMTDATA
	J66 10B	DC	XMTDATA
	J68 10B	DC	XMTDATA
	J70 10B	DC	XMTDATA
	J72 10B	DC	XMTDATA
	J74 10B	DC	XMTDATA
	J78 10B	DC	XMTDATA
	J82 10B	DC	XMTDATA
	J86 10B	DC	XMTDATA
	J90 10B	DC	XMTDATA
	J94 10B	DC	XMTDATA
J3 13A	REFER TO NETWORK J1 4B		
J3 13B	J29 8B	HC	7BROSUPPPESS-
J3 14A	J20 1A	DE	DGA
J3 14B	J50 13B	DD	XMTCONTROLBUS
	J52 13B	DD	XMTCONTROLBUS
	J54 13B	DD	XMTCONTROLBUS
	J56 13B	DD	XMTCONTROLBUS
	J58 13B	DD	XMTCONTROLBUS
	J60 13B	DD	XMTCONTROLBUS
	J62 13B	DD	XMTCONTROLBUS
	J64 13B	DD	XMTCONTROLBUS
	J66 13B	DD	XMTCONTROLBUS
	J68 13B	DD	XMTCONTROLBUS
	J70 13B	DD	XMTCONTROLBUS
	J72 13B	DD	XMTCONTROLBUS
	J74 13B	DD	XMTCONTROLBUS
	J78 13B	DD	XMTCONTROLBUS
	J82 13B	DD	XMTCONTROLBUS
	J86 13B	DD	XMTCONTROLBUS
	J90 13B	DD	XMTCONTROLBUS
	J94 13B	DD	XMTCONTROLBUS
J3 15A	J7 13A	DB	LOOPBACKDATA
	J29 3A	DB	XMTMBSDATA
J3 15B	J50 11B	AU	XMTFRAME6+12
	J52 11B	AU	XMTFRAME6+12
	J54 11B	AU	XMTFRAME6+12
	J56 11B	AU	XMTFRAME6+12
	J58 11B	AU	XMTFRAME6+12
	J60 11B	AU	XMTFRAME6+12
	J62 11B	AU	XMTFRAME6+12
	J64 11B	AU	XMTFRAME6+12
	J66 11B	AU	XMTFRAME6+12
	J68 11B	AU	XMTFRAME6+12
	J70 11B	AU	XMTFRAME6+12
	J72 11B	AU	XMTFRAME6+12
	J74 11B	AU	XMTFRAME6+12
	J78 11B	AU	XMTFRAME6+12
	J82 11B	AU	XMTFRAME6+12
	J86 11B	AU	XMTFRAME6+12
	J90 11B	AU	XMTFRAME6+12
	J94 11B	AU	XMTFRAME6+12
J3 16A	J5 14A	DW	XMT12/24CHMOD
J3 16B	REFER TO NETWORK J1 11B		
J3 17A	J5 15A	DU	XMT6/8CHMODE
J3 17B	J29 7B	IA	XMTFULLALMSEL
J2 18A	J5 16A	DV	XMT4/8/224CHMO

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J3 18B	REFER TO NETWORK	J1 3A	
J3 19A	REFER TO NETWORK	J1 19B	
J3 19B	J51 9A	EB	XMTCHCTR2-
	J52 9A	EB	XMTCHCTR2-
J3 2A	REFER TO NETWORK	J1 2A	
J3 2B	REFER TO NETWORK	J1 2A	
J3 20A	J5 17A	DR	XMT24CHMODE-
J3 20B	J53 9A	EC	XMTCHCTR3-
	J54 9A	EC	XMTCHCTR3-
J3 21B	J55 9A	ED	XMTCHCTR4-
	J56 9A	ED	XMTCHCTR4-
J3 22B	J49 9A	EA	XMTCHCTR1-
	J50 9A	EA	XMTCHCTR1-
J3 3A	REFER TO NETWORK	J1 3A	
J3 3B	REFER TO NETWORK	J1 3A	
J3 4A	J3 4B	AAD	XMT+7V
	J5 4A	AAD	XMT+7V
	J5 4B	AAD	XMT+7V
	J7 4A	AAD	RCV+7V
	J7 4B	AAD	RCV+7V
	J9 4A	AAD	RCV+7V
	J9 4B	AAD	RCV+7V
	J11 4A	AAD	RCV+7V
	J11 4B	AAD	RCV+7V
	J37 3B	AAD	+7VBITE
	J45 4A	AAD	+7VDCU
	J45 5A	AAO	+7V
	J45 6A	AAO	+7V
	J50 14A	AAO	+7VDCU
	J50 14B	AAO	+7VDCU
	J52 14A	AAO	+7VDCU
	J52 14B	AAO	+7VDCU
	J54 14A	AAO	+7VDCU
	J54 14B	AAO	+7VDCU
	J56 14A	AAO	+7VDCU
	J56 14B	AAO	+7VDCU
	J58 14A	AAO	+7VDCU
	J58 14B	AAO	+7VDCU
	J60 14A	AAO	+7VDCU
	J60 14B	AAO	+7VDCU
	J62 14A	AAO	+7VDCU
	J62 14B	AAO	+7VDCU
	J64 14A	AAO	+7VDCU
	J64 14B	AAO	+7VDCU
	J66 14A	AAO	+7VDCU
	J66 14B	AAO	+7VDCU
	J68 14A	AAO	+7VDCU
	J68 14B	AAO	+7VDCU
	J70 14A	AAO	+7VDCU
	J70 14B	AAO	+7VDCU
	J72 14A	AAO	+7VDCU
	J72 14B	AAO	+7VDCU
J3 4B	REFER TO NETWORK	J3 4A	
J3 5A	J3 5B	AAI	XMT+12V-2
	J5 5A	AAI	XMT+12V-2
	J5 5B	AAI	XMT+12V-2
	J21 5A	AAI	XMT+12V-2
	J37 3A	AAI	+12V-2BITE
J3 5B	REFER TO NETWORK	J3 5A	
J3 6A	REFER TO NETWORK	J1 6A	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J3 6B	REFER TO NETWORK	J1 64	
J3 7A	J3 7B	AAH	XMT-5V-2
	J5 7A	AAH	XMT-5V-2
	J5 76	AAH	XMT-5V-2
	J20 21B	AAH	XMT-5V-2
J3 7B	REFER TO NETWORK	J3 7A	
J3 8B	REFER TO NETWORK	J1 8B	
J3 9A	REFER TO NETWORK	J1 9B	
J5 1A	REFER TO NETWORK	J1 1A	
J5 1B	REFER TO NETWORK	J1 1A	
J5 10A	J41 2A	HQ	XMT4MHZCLK
	J50 10A	HQ	XMT4MHZCLK
	J52 10A	HQ	XMT4MHZCLK
	J54 10A	HQ	XMT4MHZCLK
	J56 10A	HQ	XMT4MHZCLK
	J58 10A	HQ	XMT4MHZCLK
	J60 10A	HQ	XMT4MHZCLK
	J62 10A	HQ	XMT4MHZCLK
	J64 10A	HQ	XMT4MHZCLK
	J66 10A	HQ	XMT4MHZCLK
	J68 10A	HQ	XMT4MHZCLK
	J70 10A	HQ	XMT4MHZCLK
	J72 10A	HQ	XMT4MHZCLK
	J74 10A	HQ	XMT4MHZCLK
	J78 10A	HQ	XMT4MHZCLK
	J82 10A	HQ	XMT4MHZCLK
	J86 10A	HQ	XMT4MHZCLK
	J90 10A	HQ	XMT4MHZCLK
	J94 10A	HQ	XMT4MHZCLK
J5 10B	J21 2B	AAQ	-12V-2
J5 11A	REFER TO NETWORK	J12 11A	
J5 12A	REFER TO NETWORK	J1 11B	
J5 13A	REFER TO NETWORK	J1 3A	
J5 13B	J20 8B	HR	LOSSOFOUTPUT
J5 14A	REFER TO NETWORK	J3 16A	
J5 15A	REFER TO NETWORK	J3 17A	
J5 16A	REFER TO NETWORK	J3 18A	
J5 17A	REFER TO NETWORK	J3 20A	
J5 18B	REFER TO NETWORK	J1 18B	
J5 19A	J112 -PIN	HI	NRZMBSCLKOUT(
J5 19B	J112 +SKT	HH	NRZMBSCLKOUT(
J5 2A	REFER TO NETWORK	J1 2A	
J5 2B	REFER TO NETWORK	J1 2A	
J5 20A	J110 -PIN	HK	MASTERCLKOUT(
J5 20B	J110 +SKT	HJ	MASTERCLKOUT(
J5 21B	REFER TO NETWORK	J1 5B	
J5 22A	J114 -PIN	HA	MBSDATAOUT(-)
J5 22B	J114 +SKT	HB	MBSDATAOUT(+)
J5 3A	REFER TO NETWORK	J1 3A	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J5 3B	REFER TO NETWORK	J1	3A
J5 4A	REFER TO NETWORK	J3	4A
J5 4B	REFER TO NETWORK	J3	4A
J5 5A	REFER TO NETWORK	J3	5A
J5 5B	REFER TO NETWORK	J3	5A
J5 6A	REFER TO NETWORK	J1	6A
J5 6B	REFER TO NETWORK	J1	6A
J5 7A	REFER TO NETWORK	J3	7A
J5 7B	REFER TO NETWORK	J3	7A
J5 8B	REFER TO NETWORK	J1	8B
J5 9A	REFER TO NETWORK	J1	6A
J5 9B	J21 1A	HO	16KPPSSYNC
J7 1A	J7 1B	AAA	RCV+12V-1
	J9 1A	AAA	RCV+12V-1
	J9 1B	AAA	RCV+12V-1
	J11 1A	AAA	RCV+12V-1
	J11 1B	AAA	RCV+12V-1
	J20 15B	AAA	RCV+12V-1
	J37 8B	AAA	+12V-1BITE
J7 1B	REFER TO NETWORK	J7	1A
J7 10A	J11 -PIN	L1	RCVMBSNRZCLK(
J7 10B	J9 9B	V7	RCVMBSCLK
	J11 10A	VZ	RCVMBSCLK
J7 11A	J113 +SKT	LF	RCVMBSDATA(+)
J7 12A	J113 -PIN	LG	RCVMBSDATA(-)
J7 13A	REFER TO NETWORK	J3	15A
J7 13B	J20 5B	LK	LOSSOFINPUT
J7 15A	J109 +SKT	LB	RECRCVCLK(+)
J7 15B	J109 -PIN	LA	RECRCVCLK(-)
J7 16A	J9 16B	QW	RCV12/24CHMOD
J7 16B	J20 4B	LM	RMTLOOPALM
J7 17A	J9 17B	QS	RCV4/8/24CHMO
J7 18A	J9 18B	QU	RCV6/8CHMODE
J7 2A	J7 2B	AAB	RCV-12V-1
	J9 2A	AAB	RCV-12V-1
	J9 2B	AAB	RCV-12V-1
	J11 2A	AAB	RCV-12V-1
	J11 2B	AAB	RCV-12V-1
	J20 22A	AAB	RCV-12V-1
	J37 9B	AAB	-12V-1BITE
J7 2B	REFER TO NETWORK	J7	2A
J7 20A	J9 20B	DF	RCVFULLALMSEL
J7 22A	J9 22B	LO	FRMBITERRMNTT
J7 3A	REFER TO NETWORK	J1	3A
J7 3B	REFER TO NETWORK	J1	3A

Table B-1. Rear Assembly Wire Connection Unit - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J7 4A	REFER TO NETWORK J3 4A		
J7 4B	REFER TO NETWORK J3 4A		
J7 5A	J7 5B	AAI	RCV+12V-2
	J9 5A	AAI	RCV+12V-2
	J9 5B	AAI	RCV+12V-2
	J11 5A	AAI R	RCV+12V-2
	J11 5B	AAI	RCV+12V-2
	J21 5B	AAI	RCV+12V-2
J7 5B	REFER TO NETWORK J7 5A		
J7 6A	REFER TO NETWORK J1 6A		
J7 6B	REFER TO NETWORK J1 6A		
J7 7A	J7 7B	AAH	RCV-5V-2
	J9 7A	AAH	RCV-5V-2
	J9 7B	AAH	RCV-5V-2
J11	7A	AAH	RCV-5V-2
	J11 7B	AAH	RCV-5V-2
	J20 21A	AAH	RCV-5V-2
J7 7B	REFER TO NETWORK J7 7A		
J7 8B	REFER TO NETWORK J1 8B		
J7 9A	J111 +SKT	LH	RCVMBSNRZCLK(
J7 9B	J21 2A	AAO	-12V-2BITE
	J37 2A	AAQ	-12V-2BITE
J9 1A	REFER TO NETWORK J7 1A		
J9 1B	REFER TO NETWORK J7 1A		
J9 10B	J50 12A	OR	RCVFRAME6/18
	J52 12A	QB	RCVFRAME6/18
	J54 12A	QB	RCVFRAME6/18
	J56 12A	QB	RCVFRAME6/18
	J58 12A	QB	RCVFRAME6/18
	J60 12A	QB	RCVFRAME6/18
	J62 12A	QB	RCVFRAME6/18
	J64 12A	QB	RCVFRAME6/18
	J66 12A	QB	RCVFRAME6/18
	J68 12A	QB	RCVFRAME6/18
	J70 12A	QB	RCVFRAME6/18
	J72 12A	QB	RCVFRAME6/18
	J74 12A	QB	RCVFRAME6/18
	J78 12A	QB	RCVFRAME6/18
	J82 12A	QB	RCVFRAME6/18
	J86 12A	QB	RCVFRAME6/18
	J90 12A	QB	RCVFRAME6/18
	J94 12A	QB	RCVFRAME6/18
J9 11B	J50 5B	QX	RCVCONTROLBUS
	J52 5B	QX	RCVCONTROLBUS
	J54 5B	QX	RCVCONTROLBUS
	J56 5B	QX	RCVCONTROLBUS
	J58 5B	QX	RCVCONTROLBUS
	J60 5B	QX	RCVCONTROLBUS
	J62 5B	QX	RCVCONTROLBUS
	J64 5B	QX	RCVCONTROLBUS
	J66 5B	QX	RCVCONTROLBUS
	J68 5B	QX	RCVCONTROLBUS
	J70 5B	QX	RCVCONTROLBUS
	J72 5B	QX	RCVCONTROLBUS
	J74 5B	QX	RCVCONTROLBUS
	J78 5B	QX	RCVCONTROLBUS
	J82 5B	QX	RCVCONTROLBUS
	J86 5B	QX	RCVCONTROLBUS
	J90 5B	QX	RCVCONTROLBUS
	J94 5B	QX	RCVCONTROLBUS
J9 12B	J31 5B	OT	RCVMBSDATA

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J9 13B	J31 6B	QJ	FRMSCHINH
J9 14B	J50 12B	SD	RCVDATABUS
	J52 12B	SD	RCVDATABUS
	J54 12B	SD	RCVDATABUS
	J56 12B	SD	RCVDATABUS
	J58 12B	SD	RCVDATABUS
	J60 12B	SD	RCVDATABUS
	J62 12B	SD	RCVDATABUS
	J64 12B	SD	RCVDATABUS
	J66 12B	SD	RCVDATABUS
	J68 12B	SD	RCVDATABUS
	J70 12B	SD	RCVDATABUS
	J72 12B	SD	RCVDATABUS
	J74 12B	SD	RCVDATABUS
	J78 12B	SD	RCVDATABUS
	J82 12B	SD	RCVDATABUS
	J86 12B	SD	RCVDATABUS
	J90 12B	SD	RCVDATABUS
	J94 12B	SD	RCVDATABUS
J9 16B	REFER TO NETWORK	J7	16A
J9 17B	REFER TO NETWORK	J7	17A
J9 18B	REFER TO NETWORK	J7	18A
J9 19A	J11 9B	SA	RCVPCMBUS
J9 19B	J20 2B	O0	REMOTEALARM
J9 2A	REFER TO NETWORK	J7	2A
J9 2B	REFER TO NETWORK	J7	2A
J9 20A	J11 12A	VW	RCVRESETTOCH1
J9 20B	REFER TO NETWORK	J7	20A
J9 22A	J11 11A	VV	RCVFRAMEY/18-
	J49 12A	VV	RCVFRAMEY/18-
	J51 12A	VV	RCVFRAMEY/18-
	J53 12A	VV	RCVFRAMEY/18-
	J55 12A	VV	RCVFRAMEY/18-
	J57 12A	VV	RCVFRAMEY/18-
	J59 12A	VV	RCVFRAMEY/18-
	J61 12A	VV	RCVFRAMEY/18-
	J63 12A	VV	RCVFRAMEY/18-
	J65 12A	VV	RCVFRAMEY/18-
	J67 12A	VV	RCVFRAMEY/18-
	J69 12A	VV	RCVFRAMEY/18-
	J71 12A	VV	RCVFRAMEY/18-
	J73 12A	VV	RCVFRAMEY/18-
	J75 12A	VV	RCVFRAMEY/18-
	J77 12A	VV	RCVFRAMEY/18-
	J79 12A	VV	RCVFRAMEY/18-
	J81 12A	VV	RCVFRAMEY/18-
	J83 12A	VV	RCVFRAMEY/18-
	J85 12A	VV	RCVFRAMEY/18-
	J87 12A	VV	RCVFRAMEY/18-
	J89 12A	VV	RCVFRAMEY/18-
	J91 12A	VV	RCVFRAMEY/18-
	J93 12A	VV	RCVFRAMEY/18-
	J95 12A	VV	RCVFRAMEY/18-
J9 22B	REFER TO NETWORK	J7	22A
J9 3A	REFER TO NETWORK	J1	3A
J9 3B	REFER TO NETWORK	J1	3A
J9 4A	REFER TO NETWORK	J3	4A
J9 4B	REFER TO NETWORK	J3	4A
J9 5A	REFER TO NETWORK	J7	5A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM		TO		REF. DESG.	SIGNAL NAME
J9	5B	REFER TO NETWORK		J7	5A
J9	6A	REFER TO NETWORK		J1	6A
J9	6B	REFER TO NETWORK		J1	6A
J9	7A	REFER TO NETWORK		J7	7A
J9	7B	REFER TO NETWORK		J7	7A
J9	8A	J20	3B	SB	LOSSOFFRAME
J9	8B	REFER TO NETWORK		J1	8B
J9	9B	REFER TO NETWORK		J7	10B
J11	1A	REFER TO NETWORK		J7	1A
J11	1B	REFER TO NETWORK		J7	1A
J11	10A	REFER TO NETWORK		J7	10B
J11	10B	J31	1A	LT	RCV1.544MHZCL
J11	11A	REFER TO NETWORK		J9	22A
J11	12A	REFER TO NETWORK		J9	20A
J11	13A	J49	13A	UD	RCVSIGABS
		J51	13A	UD	RCVSIGABS
		J53	13A	UD	RCVSIGABS
		J55	13A	UD	RCVSIGABS
		J57	13A	UD	RCVSIGABS
		J59	13A	UD	RCVSIGABS
		J61	13A	UD	RCVSIGABS
		J63	13A	UD	RCVSIGABS
		J65	13A	UD	RCVSIGABS
		J67	13A	UD	RCVSIGABS
		J69	13A	UD	RCVSIGABS
		J71	13A	UD	RCVSIGABS
		J73	13A	UD	RCVSIGABS
		J75	13A	UD	RCVSIGABS
		J77	13A	UD	RCVSIGABS
		J79	13A	UD	RCVSIGABS
		J81	13A	UD	RCVSIGABS
		J83	13A	UD	RCVSIGABS
		J85	13A	UD	RCVSIGABS
		J87	13A	UD	RCVSIGABS
		J84	13A	UD	RCVSIGABS
		J91	13A	UD	RCVSIGABS
		J93	13A	UD	RCVSIGABS
		J95	13A	UD	RCVSIGABS
J11	14A	J73	5A	WI	RCVVFOUT13
J11	14B	J73	1A	XI	RCVVFRTN13
J11	15A	J91	5A	WH	RCVVFOUT22
J11	15B	J91	1A	XH	RCVVFRTN22
J11	16A	J61	5A	WG	RCVVFOUT7
J11	16B	J11	20B	AAL	AGND
		J35	11B	AAL	AGND
		J35	5B	AAL	AGND
		J44	1B	AAL	AGND
		J61	1A	XG	RCVVFRTN7
		J67	1A	XC	RCVVFRTN10
		J69	1A	XK	RCVVFRTN11
		J95	1A	XV	RCVVFRTN24
J11	17A	J79	5A	WF	RCVVFOUT16
J11	17B	J79	1A	XF	RCVVFRTN16

Table B-1. Rear Assembly Wife Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J11 18A	J55 5A	WD	RCVVFOUT4
J11 18B	J55 1A	XD	RCVVFRTN4
J11 19A	J85 5A	WR	RCVVFOUT19
J11 19B	J85 1A	XB	RCVVFRTN19
J11 2A	REFER TO NETWORK	J7	2A
J11 2B	REFER TO NETWORK	J7	2A
J11 20A	J67 5A	WC	RCVVFOUT10
J11 20B	REFER TO NETWORK	J11	16B
J11 21A	J49 5A	WE	RCVVFOUT1
J11 21B	J49 1A	XF	RCVVFRTN1
J11 22A	J57 5A	WQ	RCVVFOUT5
J11 22B	J57 1A	XQ	RCVVFRTN5
J11 3A	REFER TO NETWORK	J1	3A
J11 3B	REFER TO NETWORK	J1	3A
J11 4A	REFER TO NETWORK	J3	4A
J11 4B	REFER TO NETWORK	J3	4A
J11 5A	REFER TO NETWORK	J7	5A
J11 5B	REFER TO NETWORK	J7	5A
J11 6A	REFER TO NETWORK	J1	6A
J11 6B	REFER TO NETWORK	J1	6A
J11 7A	REFER TO NETWORK	J7	7A
J11 7B	REFER TO NETWORK	J7	7A
J11 8A	REFER TO NETWORK	J1	10B
J11 8B	REFER TO NETWORK	J1	8B
J11 9A	J33 3A	VX	PCVADVCHCTP
J11 9B	REFER TO NETWORK	J9	19A
J20 1A	REFER TO NETWORK	J3	14A
J20 10A	J116 2	¬¬¬	N/CCINPWRRK7
J20 10B	J21 6B	AAS	+15V
J20 11A	J116 3	¬¬¬	COMCINPWRRK7
J20 11B	J116 4	¬¬¬	COMCLOUTRK1
J20 12A	J21 20A	AAV	-49VINPUTRET
	J45 15A	AAV	-48VINPUTRET
	J45 15B	AAV	-48VINPIITRET
J20 12B	J116 5	¬¬¬	N/OCLOUTRK1
J20 13B	J116 6	¬¬¬	N/CCLOUTRK1
J20 14A	J37 14B	AAR	-48VDCBITE
	J45 13A	AAR	-48VINPUTPWR
	J45 13B	AAR	-48VINPUTPWR
J20 14B	REFER TO NETWORK	J1	1A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM		TO		REF. DESG.	SIGNAL NAME
J20	15B		REFER TO NETWORK	J7	1A
J20	16A	J20	18B	AAT	D/AGMD
		J21	17A	MAT	D/AGND
		J21	18A	AAT	D/AGND
		J37	15A	AAL	AGNDBITE
		J37	15B	AAL	AGNDBITE
J20	16B	J21	6A	AAS	+15V
J20	18A		REFER TO NETWORK	J1	6A
J20	18B		REFER TO NETWORK	J20	16A
J20	19A	J49	15A	¬¬¬	F-LEAD
		J51	15A	¬¬¬	F-LEAD
		J53	15A	¬¬¬	F-LEAD
		J55	15A	¬¬¬	F-LEAD
		J57	15A	¬¬¬	F-LEAD
		J59	15A	¬¬¬	F-LEAD
		J61	15A	¬¬¬	F-LEAD
		J63	15A	¬¬¬	F-LEAD
		J65	15A	¬¬¬	F-LEAD
		J67	15A	¬¬¬	F-LEAD
		J69	15A	¬¬¬	F-LEAD
		J71	15A	¬¬¬	F-LEAD
		J73	15A	¬¬¬	F-LEAD
		J75	15A	¬¬¬	F-LEAD
		J77	15A	¬¬¬	F-LEAD
		J79	15A	¬¬¬	F-LEAD
		J81	15A	¬¬¬	F-LEAD
		J83	15A	¬¬¬	F-LEAD
		J85	15A	¬¬¬	F-LEAD
		J87	15A	¬¬¬	F-LEAD
		J89	15A	¬¬¬	F-LEAD
		J91	15A	¬¬¬	F-LEAD
		J93	15A	¬¬¬	F-LEAD
		J95	15A	¬¬¬	F-LEAD
J20	19B	J21	3A	AAU	-15V
J20	2A	J50	8A	¬¬¬	CGABUSDIG-
		J52	8A	¬¬¬	CGABUSDIG-
		J54	8A	¬¬¬	CGABUSDIG-
		J56	8A	¬¬¬	CGABUSDIG-
		J58	8A	¬¬¬	CGABUSDIG-
		J60	8A	¬¬¬	CGABUSDIG-
		J62	8A	¬¬¬	CGABUSDIG-
		J64	8A	¬¬¬	CGABUSDIG-
		J66	8A	¬¬¬	CGABUSDIG-
		J68	8A	¬¬¬	CGABUSDIG-
		J70	8A	¬¬¬	CGABUSDIG-
		J72	8A	¬¬¬	CGABUSDIG-
		J74	8A	¬¬¬	CGABUS DIG-
		J78	8A	¬¬¬	CGABUSDIG-
		J82	8A	¬¬¬	CGABUSDIG-
		J86	8A	¬¬¬	CGABUSDIG-
		J90	8A	¬¬¬	CGABUSDIG-
		J94	8A	¬¬¬	CGABUSDIG--
J20	2B		REFER TO NETWORK	J9	19B
J20	20A	J119	-Y	¬¬¬	FLEAD
J20	20B	J37	1A	AAN	-7VBITE
		J45	10B	AAN	-7VDCU
		J45	8B	AAN	-7V
		J45	9B	AAN	-7V
		J50	4A	AAN	-7VDCU
		J50	4B	AAN	-7VDCU
		J52	4A	AAN	-7VDCU
		J52	4B	AAN	-7VOCU
		J54	4A	AAN	-7VCCU
		J54	4B	AAN	-7VDCU
		J56	4A	AAN	-7VDCU

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
	J56 4B	AAN	-7VDCU
	J58 4A	AAN	-7VDCU
	J58 4B	AAN	-7VDCU
	J60 4A	AAN	-7VDCU
	J60 4B	AAN	-7VDCU
	J62 4A	AAN	-7VDCU
	J62 4B	AAN	-7VDCU
	J64 4A	AAN	-7VDCU
	J64 4B	AAN	-7VDCU
	J86 4A	AAN	-7VDCU
	J86 4B	AAN	-7VDCU
	J90 4A	AAN	-7VDCU
	J90 4B	AAN	-7VDCU
	J94 4A	AAN	-7VDCU
	J94 4B	AAN	-7VDCU
J20 21A	REFER TO NETWORK	J7	7A
J20 21B	REFER TO NETWORK	J3	7A
J20 22A	REFER TO NETWORK	J7	2A
J20 22B	REFER TO NETWORK	J1	2A
J20 3A	J49 8A	¬¬¬	CGALMVF
	J51 8A	¬¬¬	CGALMVF
	J53 8A	¬¬¬	CGALMVF
	J55 8A	¬¬¬	CGALMVF
	J57 8A	¬¬¬	CGALMVF
	J59 8A	¬¬¬	CGALMVF
	J61 8A	¬¬¬	CGALMVF
	J63 8A	¬¬¬	CGALMVF
	J65 8A	¬¬¬	CGALMVF
	J67 8A	¬¬¬	CGALMVF
	J69 8A	¬¬¬	CGALMVF
	J71 8A	¬¬¬	CGALMVF
	J73 8A	¬¬¬	CGALMVF
	J75 8A	¬¬¬	CGALMVF
	J77 8A	¬¬¬	CGALMVF
	J79 8A	¬¬¬	CGALMVF
	J81 8A	¬¬¬	CGALMVF
	J83 8A	¬¬¬	CGALMVF
	J85 8A	¬¬¬	CGALMVF
	J87 8A	¬¬¬	CGALMVF
	J89 8A	¬¬¬	CGALMVF
	J91 8A	¬¬¬	CGALMVF
	J93 8A	¬¬¬	CGALMVF
	J95 8A	¬¬¬	CGALMVF
J20 3B	REFER TO NETWORK	J9	8A
J20 4A	J21 19B	AAF	DGND
	J49 6A	AAF	DGND
	J49 6B	AAF	DGND
	J51 6A	AAF	DGND
	J51 6B	AAF	DGND
	J53 6A	AAF	DGND
	J53 6B	AAF	DGND
	J55 6A	AAF	DGND
	J55 6B	AAF	DGND
	J57 6A	AAF	DGND
	J57 6B	AAF	DGND
	J59 6A	AAF	DGND
	J59 6B	AAF	DGND
	J61 6A	AAF	DGND
	J61 6B	AAF	DGND
	J63 6A	AAF	DGND
	J63 6B	AAF	DGND
	J65 6A	AAF	DGND
	J65 6B	AAF	DGND
	J67 6A	AAF	DGND
	J67 6B	AAF	DGND
	J69 6A	AAF	DGND
	J69 6B	AAF	DGND
	J71 6A	AAF	DGND
	J71 6B	AAF	DGND

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J20 4B	REFER TO NETWORK	J7 16B	
J20 5A	REFER TO NETWORK	J1 3A	
J20 5B	REFER TO NETWORK	J7 13B	
J20 6A	REFER TO NETWORK	J1 3A	
J20 6B	J31 10B	LN	LOCALLOOPALM
J20 7B	REFER TO NETWORK	J1 8B	
J20 8A	J49 14B	¬¬¬	CGAGNDALM9.5
	J51 14B	¬¬¬	CGAGNDALM9.5
	J53 14B	¬¬¬	CGAGNDALM9.5
	J55 14B	¬¬¬	CGAGNDALM9.5
	J57 14B	¬¬¬	CGAGNDALM9.5
	J59 14B	¬¬¬	CGAGNDALM9.5
	J61 14B	¬¬¬	CGAGNDALM9.5
	J63 14B	¬¬¬	CGAGNDALM9.5
	J65 14B	¬¬¬	CGAGNDALM9.5
	J67 14B	¬¬¬	CGAGNDALM9.5
	J69 14B	¬¬¬	CGAGNDALM9.5
	J71 14B	¬¬¬	CGAGNDALM9.5
	J73 14B	¬¬¬	CGAGNDALM9.5
	J75 14B	¬¬¬	CGAGNDALM9.5
	J77 14B	¬¬¬	CGAGNDALM9.5
	J79 14B	¬¬¬	CGAGNDALM9.5
	J81 14B	¬¬¬	CGAGNDALM9.5
	J83 14B	¬¬¬	CGAGNDALM9.5
	J85 14B	¬¬¬	CGAGNDALM9.5
	J87 14B	¬¬¬	CGAGNDALM9.5
	J89 14B	¬¬¬	CGAGNDALM9.5
	J91 14B	¬¬¬	CGAGNDALM9.5
	J93 14B	¬¬¬	CGAGNDALM9.5
	J95 14B	¬¬¬	CGAGNDALM9.5
J20 8B	REFER TO NETWORK	J5 13B	
J20 9A	J116 1	¬¬¬	N/OCINPWRRK7
J21 1A	REFER TO NETWORK	J5 9B	
J21 10A	J37 28	AAC	-5V-1
J21 10B	REFER TO NETWORK	J1 3A	
J21 11B	REFER TO NETWORK	J1 3A	
J21 17A	REFER TO NETWORK	J20 16A	
J21 17B	REFER TO NETWORK	J1 6A	
J21 18A	REFER TO NETWORK	J20 16A	
J21 18B	REFER TO NETWORK	J1 6A	
J21 19B	REFER TO NETWORK	J20 4A	
J21 2A	REFER TO NETWORK	J7 9B	
J21 2B	REFER TO NETWORK	J5 10B	
J21 20A	REFER TO NETWORK	J20 12A	
J21 20B	REFER TO NETWORK	J1 6A	
J21 21A	REFER TO NETWORK	J1 6A	
J21 21B	REFER TO NETWORK	J1 6A	
J21 3A	REFER TO NETWORK	J20 19B	
J21 5A	REFER TO NETWORK	J3 5A	
J21 5B	REFER TO NETWORK	J7 5A	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J21 6A	REFER TO NETWORK	J20 16B	
J21 6B	REFER TO NETWORK	J20 10B	
J21 7A	REFER TO NETWORK	E 1-2	
J21 7B	REFER TO NETWORK	E 1-2	
J21 8A	REFER TO NETWORK	J1 3A	
J21 8B	REFER TO NETWORK	J1 3A	
J21 9A	REFER TO NETWORK	J1 3A	
J21 9B	REFER TO NETWORK	J1 3A	
J25 1A	J71 2A	CM	XMTVFIN12
J25 1B	J71 1B	CM	XMTVFRET12
J25 10A	J83 2A	CS	XMTVFIN18
J25 10B	J83 1B	QS	XMTVFRET18
J25 11A	J81 2A	CR	XMTVFIN17
J25 11B	REFER TO NETWORK	J1 20B	
J25 12A	J91 2A	CW	XMTVFIN22
J25 12B	J91 2B	BW	XMTVFRET22
J25 13A	J89 2A	CV	XMTVFIN21
J25 13B	J89 1B	BV	XMTVFRET21
J25 14A	J93 2A	CX	XMTVFIN23
J25 14B	J93 1B	BX	XMTVFRET23
J25 15A	J95 2A	CY	XMTVFIN24
J25 15B	J95 1B	BY	XMTVFRET24
J25 2A	J67 2A	CK	XMTVFIN10
J25 2B	J67 1B	BK	XMTVFRET10
J25 3A	J65 2A	CJ	XMTVFIN9
J25 3B	J65 1B	BJ	XMTVFRET9
J25 4A	J75 2A	CO	XMTVFIN14
J25 4B	J75 1B	BO	XMTVFRET14
J25 5A	J73 2A	CN	XMTVFIN13
J25 5B	REFER TO NETWORK	J1 20B	
J25 6A	J77 2A	CP	XMTVFIN15
J25 6B	J77 1B	BP	XMTVFRET15
J25 7A	J79 2A	CQ	XMTVFIN16
J25 7B	J79 1B	BQ	XMTVFRET16
J25 8A	J85 2A	CT	XMTVFIN19
J25 8B	J85 1B	BT	XMTVFRET19
J25 9A	J87 2A	CU	XMTVFIN20
J25 9B	J87 1B	BU	XMTVFRET20

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J27 1A	REFER TO NETWORK	J1 13A	
J27 1B	J63	9A EH	XMTCHCTR8-
	J64	9A EH	XMTCHCTR8-
J27 10A	J81	9A EQ	XMTCHCTR17-
	J82	9A EQ	XMTCHCTR17-
J27 10B	J73	9A EM	XMTCHCTR13-
	J74	9A EM	XMTCHCTR13-
J27 11A	J77	9A EO	XMTCHCTR15-
	J78	9A EO	XMTCHCTR15-
J27 11B	REFER TO NETWORK	J1 16B	
J27 12A	J85	9A ES	XMTCHCTR19-
	J86	9A ES	XMTCHCTR19-
J27 12B	REFER TO NETWORK	J1 17B	
J27 13A	J87	9A ET	XMTCHCTR20-
J27 13B	REFER TO NETWORK	J1 14B	
J27 14A	J95	9A EX	XMTCHCTR24-
J27 14B	REFER TO NETWORK	J1 15B	
J27 15A	J91	9A EV	XMTCHCTR22-
J27 15B	REFER TO NETWORK	J1 3A	
J27 2A	REFER TO NETWORK	J1 8A	
J27 2B	J61	9A EG	XMTCHCTR7-
	J62	9A EG	XMTCHCTR7-
J27 3A	REFER TO NETWORK	J1 9A	
J27 3B	J79	9A ER	XMTCHCTR16-
J27 4A	REFER TO NETWORK	J1 10A	
J27 4B	J57	9A EE	XMTCHCTR-
	J58	9A EE	XMTCHCTR5-
J27 5A	REFER TO NETWORK	J1 5A	
J27 5B	J67	9A EJ	XMTCHCTR10-
	J68	9A FJ	XMTCHCTR10-
J27 6A	J59	9A EF	XMTCHCTR6-
	J60	9A EF	XMTCHCTR6-
J27 6B	J69	9A EK	XMTCHCTR11-
	J70	9A FK	XMTCHCTR11-
J27 7A	J65	9A EI	XMTCHCTR9-
	J66	9A EI	XMTCHCTR9-
J27 7B	J93	9A EW	XMTCHCTR23-
	J94	9A EW	XMTCHCTR23-
J27 8A	J71	9A EL	XMTCHCTR12-
	J72	9A EL	XMTCHCTR12-
J27 8B	J83	9A ER	XMTCHCTR18-
J27 9A	J75	9A EN	XMTCHCTR14-
J27 9B	J89	9A EU	XMTCHCTR21-
	J90	9A EU	XMTCHCTR21-
J29 1A	J108	+SKT HM	EXTTIMINGSRC(

Table B-1. Rear Assembly Wire Connection List - Continued

FROM		TO		REF. DESG.	SIGNAL NAME	
J29	1B	J108	-PIN	HL	EXTTIMINGSRC(	
J29	10A		REFER TO NETWORK		J1	3A
J29	11A		REFER TO NETWORK		J1	3A
J29	11B		REFER TO NETWORK		J1	3A
J29	12A		REFER TO NETWORK		J1	3A
J29	12B		REFER TO NETWORK		J1	3A
J29	13A		REFER TO NETWORK		J1	3A
J29	13B		REFER TO NETWORK		J1	3A
J29	14A		REFER TO NETWORK		J1	3A
J29	14B		REFER TO NETWORK		J1	3A
J29	15A		REFER TO NETWORK		J1	3A
J29	15B		REFER TO NETWORK		J1	3A
J29	2A		REFER TO NETWORK		J1	3A
J29	3A		REFER TO NETWORK		J3	15A
J29	6B	J31	3B	HE	LOCALLOOP-	
J29	7B		REFER TO NETWORK		J3	17B
J29	8B		REFER TO NETWORK		J3	13B
J29	9A		REFER TO NETWORK		J1	3A
J31	1A		REFER TO NETWORK		J11	10B
J31	1B	J115	+SKT	LC	FRMBITERRMN	
J31	10A	J45	8A	AAF	DGND	
J31	10B		REFER TO NETWORK		J20	6B
J31	11A		REFER TO NETWORK		J1	11A
J31	11B		REFER TO NETWORK		J1	6A
J31	12A		REFER TO NETWORK		J1	6A
J31	12B		REFER TO NETWORK		J1	6A
J31	13B		REFER TO NETWORK		J1	6A
J31	14A		REFER TO NETWORK		J1	6A
J31	15A		REFER TO NETWORK		J1	6A
J31	2B	J117	-A	LD	INHFRMSCH	
J31	3A	J50	8B	LQ	RCV4MHZCLKBUS	
		J52	8B	LQ	RCV4MHZCLKBUS	
		J54	8B	LQ	RCV4MHZCLKBUS	
		J56	8B	LQ	RCV4MHZCLKBUS	
		J58	8B	LQ	RCV4MHZCLKBUS	
		J60	8B	LQ	RCV4MHZCLKBUS	
		J62	8B	LQ	RCV4MHZCLKBUS	
		J64	8B	LQ	RCV4MHZCLKBUS	
		J66	8B	LQ	RCV4MHZCLKBUS	
		J68	8B	LQ	RCV4MHZCLKBUS	
		J70	8B	LQ	RCV4MHZCLKBUS	
		J72	8B	LQ	RCV4MHZCLKBUS	
		J74	8B	LQ	RCV4MHZCLKBUS	
		J78	8B	LQ	RCV4MHZCLKBUS	
		J82	8B	LQ	RCV4MHZCLKBUS	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
	J86 8B	LQ	RCV4MHZCLKBUS
	J90 8B	LQ	RCV4MHZCLKBUS
	J94 8B	LQ	RCV4MHZCLKBUS
J31 3B	REFER TO NETWORK	J29 6B	
J31 4A	REFER TO NETWORK	J1 6A	
J31 4B	J117 -B	LB	EXTLOOPBACK-
J31 5A	REFER TO NETWORK	J1 6A	
J31 5B	REFER TO NETWORK	J9 12B	
J31 6A	REFER TO NETWORK	J1 6A	
J31 6B	REFER TO NETWORK	J9 13B	
J31 7A	J45 10A	AAN	-7VDCU
	J66 4A	AAN	-7VDCU
	J66 4B	AAN	-7VDCU
	J68 4A	AAN	-7VDCU
	J68 4B	AAN	-7VDCU
	J70 4A	AAN	-7VDCU
	J70 4B	AAN	-7VDCU
	J72 4A	AAN	-7VDCU
	J72 4B	AAN	-7VDCU
	J74 4A	AAN	-7VDCU
	J74 4B	AAN	-7VDCU
	J78 4A	AAN	-7VDCU
	J78 4B	AAN	-7VDCU
	J82 4A	AAN	-7VDCU
	J82 4B	AAN	-7VDCU
J31 7B	REFER TO NETWORK	J1 6A	
J31 8A	REFER TO NETWORK	J1 6A	
J31 8B	REFER TO NETWORK	J1 6A	
J31 9A	REFER TO NETWORK	J1 6A	
J31 9B	REFER TO NETWORK	J1 6A	
J33 10A	J83 11A	RR	RCVCHCTR18-
J33 10B	J81 11A	PQ	RCVCHCTR17-
	J82 11A	RQ	RCVCHCTR17-
J33 11A	J87 11A	RT	RCVCHCTR20-
J33 11B	J85 11A	RS	RCVCHCTR19-
	J86 11A	RS	RCVCHCTR19-
J33 12A	J77 11A	RO	RCVCHCTR15-
	J78 11A	RO	RCVCHCTR15-
J33 12B	J79 11A	RP	RCVCHCTR16-
J33 13A	J73 11A	RM	RCVCHCTR13-
	J74 11A	RM	RCVCHCTR13-
J33 13B	J75 11A	RN	RCVCHCTR14-
J33 14A	J53 11A	RC	RCVCHCTR3-
	J54 11A	RC	RCVCHCTR3-
J33 14B	J55 11A	RD	RCVCHCTR4-
	J56 11A	RD	RCVCHCTR4-
J33 15A	J49 11A	RA	RCVCHCTR1-
	J50 11A	RA	RCVCHCTR1-
J33 15B	J51 11A	RB	RCVCHCTR2-
	J52 11A	RB	RCVCHCTR2-
J33 2B	REFER TO NETWORK	J1 6A	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J33 3A	REFER TO NETWORK J11 9A		
J33 3B	J50 13A	QP	RCVDATABUSCLK
	J52 13A	QP	RCVDATABUSCLK
	J54 13A	QP	RCVDATABUSCLK
	J56 13A	QP	RCVDATABUSCLK
	J58 13A	QP	RCVDATABUSCLK
	J60 13A	QP	RCVDATABUSCLK
	J62 13A	QP	RCVDATABUSCLK
	J64 13A	QP	RCVDATABUSCLK
	J66 13A	QP	RCVDATABUSCLK
	J68 13A	QP	RCVDATABUSCLK
	J70 13A	QP	RCVDATABUSCLK
	J72 13A	QP	RCVDATABUSCLK
	J74 13A	QP	RCVDATABUSCLK
	J78 13A	QP	RCVDATABUSCLK
	J82 13A	QP	RCVDATABUSCLK
	J86 13A	QP	RCVDATABUSCLK
	J90 13A	QP	RCVDATABUSCLK
	J94 13A	QP	RCVDATABUSCLK
J33 4A	J93 11A	RW	RCVCHCTR23-
	J94 11A	RW	RCVCHCTR23-
J33 4B	J95 11A	RX	RCVCHCTR24-
J33 5A	J89 11A	RU	RCVCHCTR21-
	J90 11A	RU	RCVCHCTR21-
J3A 5B	J91 11A	RV	RCVCHCTR22-
J33 6A	J69 11A	RK	RCVCHCTR11-
	J70 11A	RK	RCVCHCTR11-
J33 6B	J71 11A	RLI	RCVCHCTR12-
	J72 11A	RL	RCVCHCTR12-
J33 7A	J65 11A	RI	RCVCHCTR9-
	J66 11A	RI	RCVCHCTR9-
J33 7B	J67 11A	RJ	RCVCHCTR10-
	J68 11A	RJ	RCVCHCTR10-
J33 8A	J61 11A	RG	RCVCHCTR7-
	J62 11A	RG	RCVCHCTR7-
J33 8B	J63 11A	RH	RCVCHCTR8-
	J64 11A	RH	RCVCHCTR8-
J33 9A	J57 11A	RE	RCVCHCTR5-
	J58 11A	RE	RCVCHCTR5-
J33 9B	J59 11A	RF	RCVCHCTR6-
	J60 11A	RF	RCVCHCTR6-
J35 1A	J75 5A	WP	RCVVFOUT14
J35 1B	J75 1A	YP	RCVVFRTN14
J35 10A	J77 5A	WW	RCVVFOUT15
J35 10B	J77 1A	XW	RCVVFRTN15
J35 11A	J95 5A	WV	RCVVFOUT24
J35 11B	REFER TO NETWORK J11 16B		
J35 12A	J71 5A	WR	RCVVFOUT12
J35 12B	J71 1A	XR	RCVVFRTN12
J35 13A	J53 5A	WS	RCVVFOUT3
J35 13B	J53 1A	XS	RCVVFRTN3
J35 14A	J83 5A	WT	RCVVFOUT18

Table B-1. Rear Assembly Wire Connection List -.Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J35 14B	J83 1A	XT	RCVVFRTN18
J35 15A	J65 5A	WU	RCVVFOUT9
J35 15B	J65 1A	XU	RCVVFRTN9
J35 2A	J93 5A	WO	RCVVFOUT23
J35 2B	J93 1A	XO	RCVVFRTN23
J35 3A	J63 5A	WN	RCVVFOUT8
J35 3B	J63 1A	XN	RCVVFRTN8
J35 4A	J87 5A	WJ	RCVVFOUT20
J35 4B	J87 1A	XJ	RCVVFRTN20
J35 5A	J69 5A	WK	RCVVFOUT11
J35 5B	REFER TO NETWORK	J11 16B	
J35 6A	J51 5A	WL	RCVVFOUT2
J35 6B	J51 1A	XL	RCVVFRTN2
J35 7A	J81 5A	WM	RCVVFOUT17
J35 7B	J81 1A	XM	RCVVFRTN17
J35 8A	J89 5A	WY	RCVVFOUT21
J35 8B	J89 1A	XY	RCVVFRTN21
J35 9A	J59 5A	WX	RCVVFOUT6
J35 9B	J59 1A	XX	RCVVFRTN6

FROM	TO	REF. DESG.	SIGNAL NAME
J37 1A	REFER TO NETWORK	J20 20B	
J37 10B	J41 4A	¬¬¬	VFSELFTESTEN
	J41 4B	¬¬¬	VFSELFTESTEN
J37 13B	J41 3A	¬¬¬	VFSFLFTESTFA
	J41 3B	¬¬¬	VFSELFTESTFA
J37 14B	REFER TO NETWORK	J20 14A	
J37 15A	REFER TO NETWORK	J20 16A	
J37 15B	REFER TO NETWORK	J20 16A	
J37 2A	REFER TO NETWORK	J7 9B	
J37 2B	REFER TO NETWORK	J21 10A	
J37 3A	REFER TO NETWORK	J3 5A	
J37 3B	REFER TO NETWORK	J3 4A	
J37 6B	REFER TO NETWORK	J1 10B	
J37 7B	J44 5B	AAP	-42V
	J45 12B	AAP	-42VBITE
J37 8B	REFER TO NETWORK	J7 1A	
J37 9B	REFER TO NETWORK	J7 2A	
J41 2A	REFER TO NETWORK	J5 10A	
J41 3A	REFER TO NETWORK	J37 13B	
J41 3A	REFER TO NETWORK	J37 13B	
J41 4A	REFER TO NETWORK	J37 10B	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM		TO		REF. DESG.	SIGNAL NAME
J41	4B	REFER TO NETWORK		J37	10B
J41	9A	REFER TO NETWORK		J1	6A
J41	9B	REFER TO NETWORK		J1	6A
J42	1B	REFER TO NETWORK		J1	10B
J42	2B	REFER TO NETWORK		J1	10B
J42	3B	REFER TO NETWORK		J1	10B
J42	4B	REFER TO NETWORK		J1	10B
J44	1B	REFER TO NETWORK		J11	16B
J44	10A	J116	13	¬¬¬	N/CCRLRK5
J44	10B	J116	16	¬¬¬	N/CCRLRK4
J44	11A	J116	14	¬¬¬	N/OCRLRK5
J44	11B	J116	17	¬¬¬	N/OCRLRK4
J44	12A	J116	15	¬¬¬	COMCRLRK5
J44	12B	J116	18	¬¬¬	COMCLLRK4
J44	13A	J116	20	¬¬¬	N/CCCGARK8
J44	13B	J116	23	¬¬¬	N/CCLOFRK6
J44	14A	J116	21	¬¬¬	N/OCCGARK8
J44	14B	J116	24	¬¬¬	N/OCLOFRK6
J44	15A	J116	22	¬¬¬	COMCCGARK8
J44	15B	J116	25	¬¬¬	COMCLOFRK6
J44	2B	REFER TO NETWORK		J1	20B
J44	3A	REFER TO NETWORK		J1	10B
J44	4A	REFER TO NETWORK		JA	10B
J44	5B	REFER TO NETWORK		J37	7B
J44	7A	J116	7	¬¬¬	N/CCLINRK3
J44	7B	J116	10	¬¬¬	N/CCFAULTRK2
J44	8A	J116	8	¬¬¬	N/OCLINRK3
J44	8B	J116	11	¬¬¬	N/OCFAULTRK2
J44	9A	J116	9	¬¬¬	COMCLINRK3
J44	9B	J116	12	¬¬¬	COMCFAULTRK2
J45	10A	REFER TO NETWORK		J31	7A
J45	10B	REFER TO NETWORK		J20	20B
J45	12A	J49	22A	AAP	-42VVF
		J49	22B	AAP	-42VVF
		J51	22A	AAP	-42VVF
		J51	22B	AAP	-42VVF
		J53	22A	AAP	-42VVF
		J53	22B	AAP	-42VVF
		J55	22A	AAP	-42VVF
		J55	22B	AAP	-42VVF
		J57	22A	AAP	-42VVF
		J57	22B	AAP	-42VVF
		J59	22A	AAP	-42VVF

Table B-1. Rear Assembly Wire Connection List - Continued

FROM		TO		REF. DESG.	SIGNAL NAME
		J59	22B	AAP	-42VVF
		J61	22A	AAP	-42VVF
		J61	22B	AAP	-42VVF
		J63	22A	AAP	-42VVF
		J63	22B	AAP	-42VVF
		J65	22A	AAP	-42VVF
		J65	22B	AAP	-42VVF
		J67	22A	AAP	-42VVF
		J67	22B	AAP	-42VVF
		J69	22A	AAP	-42VVF
		J69	22B	AAP	-42VVF
		J71	22A	AAP	-42VVF
		J71	22B	AAP	-42VVF
		J73	22A	AAP	-42VVF
		J73	22B	AAP	-42VVF
		J75	22A	AAP	-42VVF
		J75	22B	AAP	-42VVF
		J77	22A	AAP	-42VVF
		J77	22B	AAP	-42VVF
		J79	22A	AAP	-42VVF
		J79	22B	AAP	-42VVF
		J81	22A	AAP	-42VVF
		J81	22B	AAP	-42VVF
		J83	22A	AAP	-42VVF
		J83	22B	AAP	-42VVF
		J85	22A	AAP	-42VVF
		J85	22B	AAP	-42VVF
		J87	22A	AAP	-42VVF
		J87	22B	AAP	-42VVF
		J89	22A	AAP	-42VVF
		J89	22B	AAP	-42VVF
		J91	22A	AAP	-42VVF
		J91	22B	AAP	-42VVF
		J93	22A	AAP	-42VVF
		J93	22B	AAP	-42VVF
		J95	22A	AAP	-42VVF
		J95	22B	AAP	-42VVF
J45	12B	REFER TO NETWORK		J37	7R
J45	13A	REFER TO NETWORK		J20	14A
J45	13B	REFER TO NETWORK		J20	14A
J45	15A	REFER TO NETWORK		J20	12A
J45	15B	REFER TO NETWORK		J20	12A
J45	4A	REFER TO NETWORK		J3	4A
J45	4B	REFER TO NETWORK		J1	7B
J45	5A	REFER TO NETWORK		J3	4A
J45	5B	REFER TO NETWORK		J1	7B
J45	6A	REFER TO NETWORK		J3	4A
J45	6B	REFER TO NETWORK		J1	7B
J45	8A	REFER TO NETWORK		J31	10A
J45	8B	REFER TO NETWORK		J20	20B
J45	9B	REFER TO NETWORK		J20	20B
J49	1A	REFER TO NETWORK		J11	21B
J49	1B	REFER TO NETWORK		J1	21B
J49	10A	REFER TO NETWORK		J1	12B
J49	11A	REFER TO NETWORK		J33	15A
J49	12A	REFER TO NETWORK		J9	22A
J49	13A	REFER TO NETWORK		J11	13A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J49 14B	REFER TO NETWORK	J20 8A	
J49 15A	REFER TO NETWORK	J20 19A	
J49 16A	J119 -C	¬¬¬	CHAN1ESIG
J49 17A	J118 -C	¬¬¬	CHAN1MSIG
J49 18A	J101 -A	¬¬¬	CH1XMTVFINT
J49 19A	J101 -B	¬¬¬	CH1XMTVFINR
J49 2A	REFER TO NETWORK	J1 16A	
J49 20A	J101 -C	¬¬¬	C1RCVVFOUTT
J49 20B	J101 -D	¬¬¬	C1RCVVFOUTB
J49 22A	REFER TO NETWORK	J45 12A	
J49 22B	REFER TO NETWORK	J45 12A	
J49 3A	REFER TO NETWORK	J1 10B	
J49 3B	REFER TO NETWORK	J1 10B	
J49 5A	REFER TO NETWORK	J11 21A	
J49 6A	REFER TO NETWORK	J20 4A	
J49 6B	REFER TO NETWORK	J20 4A	
J49 7A	REFER TO NETWORK	J1 3A	
J49 7B	REFER TO NETWORK	J1 3A	
J49 8A	REFER TO NETWORK	J20 3A	
J49 9A	REFER TO NETWORK	J3 228	
J50 1A	131 5	¬¬¬	CH1SIG1(+)
J50 1B	131 6	¬¬¬	CH1SIG1(-)
J50 10A	REFER TO NETWORK	J5 10A	
J50 10B	REFER TO NETWORK	J3 12B	
J50 11A	REFER TO NETWORK	J33 15A	
J50 11B	REFER TO NETWORK	J3 15B	
J50 12A	REFER TO NETWORK	J9 10A	
J50 12B	REFER TO NETWORK	J9 14B	
J50 13A	REFER TO NETWORK	J33 3B	
J50 13B	REFER TO NETWORK	J3 14B	
J50 14A	REFER TO NETWORK	J3 4A	
J50 14B	REFER TO NETWORK	J3 4A	
J50 15A	J131 24	¬¬¬	CH1XMTCLKIN(+
J50 15B	J131 23	¬¬¬	CH1XMTCLKIN(-
J50 16A	J131 15	¬¬¬	CH1XMTCLKOT(+
J50 16B	J131 16	¬¬¬	CH1XMTCLKOT(-
J50 17A	J131 17	¬¬¬	CH1RCVCLK(+)
J50 17B	J131 18	¬¬¬	CH1RCVCLK(-)

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J50 18A	J131 2	¬¬¬	CH1XMTDATA(+)
J50 18B	REFER TO NETWORK	J1	8B
J50 19A	J131 14	¬¬¬	CH1XMTDATA(-)
J50 19B	REFER TO NETWORK	J3	11A
J50 2A	J131 8	¬¬¬	CH1SIG2(+)
J50 2B	J131 9	¬¬¬	CH1SIG2(-)
J50 20A	J131 3	¬¬¬	CH1RCVDATA(+)
J50 20B	J131 19	¬¬¬	CH1RCVDATA(-)
J50 21A	J131 12	¬¬¬	CH1SIG4(+)
J50 21B	J131 13	¬¬¬	CH1SIG4(-)
J50 3A	J131 10	¬¬¬	CH1SIG3(+)
J50 3B	J131 11	¬¬¬	CH1SIG3(-)
J50 4A	REFER TO NETWORK	J20	20B
J50 4B	REFER TO NETWORK	J20	20B
J50 5B	REFER TO NETWORK	J9	11B
J50 6A	REFER TO NETWORK	J1	6A
J50 6B	REFER TO NETWORK	J1	6A
J50 7A	REFER TO NETWORK	J1	3A
J50 7B	REFER TO NETWORK	J1	3A
J50 8A	REFER TO NETWORK	J20	2A
J50 8B	REFER TO NETWORK	J31	3A
J50 9A	REFER TO NETWORK	J3	22B
J51 1A	REFER TO NETWORK	J35	6B
J51 1B	REFER TO NETWORK	J1	21B
J51 10A	REFER TO NETWORK	J1	12B
J51 11A	REFER TO NETWORK	J33	15B
J51 12A	REFER TO NETWORK	J9	22A
J51 13A	REFER TO NETWORK	J11	13A
J51 14B	REFER TO NETWORK	J20	9A
J51 15A	REFER TO NETWORK	J20	19A
J51 16A		¬¬¬	CHAN2ESIG
J51 17A	J118 -B	¬¬¬	CHAN2MSIG
J51 18A	J101 -B	¬¬¬	CH2XMTVFINT
J51 19A	J101 -K	¬¬¬	CHZXMTVFINR
J51 2A	REFER TO NETWORK	J20	15A
J51 20A	J101 -L	¬¬¬	C2RCVVFOUTT
J51 20B	J101 -M	¬¬¬	C2RCVVFOUTR
J51 22A	REFER TO NETWORK	J45	12A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM		TO		REF. DESG.	SIGNAL NAME
J51	22B		REFER TO NETWORK	J45	12A
J51	3A		REFER TO NETWORK	J1	10B
J51	3B		REFER TO NETWORK	J1	10B
J51	5A		REFER TO NETWORK	J35	6A
J51	6A		REFER TO NETWORK	J20	4A
J51	6B		REFER TO NETWORK	J20	4A
J51	7A		REFER TO NETWORK	J1	3A
J51	7B		REFER TO NETWORK	J1	3A
J51	8A		REFER TO NETWORK	J20	3A
J51	9A		REFER TO NETWORK	J3	19B
J52	1A	J130	5	¬¬¬	CH2SIG1(+)
J52	1B	J130	6	¬¬¬	CH2SIG1(-)
J57	10A		REFER TO NETWORK	J5	10A
J52	10B		REFER TO NETWORK	J3	12B
J52	11A		REFER TO NETWORK	J33	15B
J52	11B		REFER TO NETWORK	J3	15B
J52	12A		REFER TO NETWORK	J9	10B
J52	12B		REFER TO NETWORK	J9	14B
J52	13A		REFER TO NETWORK	J33	3B
J52	13B		REFER TO NETWORK	J3	14B
J52	14A		REFER TO NETWORK	J3	4A
J52	14B		REFER TO NETWORK	J3	4A
J52	15A	J130	24	¬¬¬	CH2XMTCLKIN(+
J52	15B	J130	23	¬¬¬	CH2XMTCLKIN(-
J52	16A	J130	15	¬¬¬	CH2XMTCLKOT(+
J52	16B	J130	16	¬¬¬	CH2XMTCLKOT(-
J52	17A	J130	17	¬¬¬	CH2RCVCLK(+)
J52	17B	J130	18	¬¬¬	CH2RCVCLK(-)
J52	18A	J130	2	¬¬¬	CH2XMTDATA(+)
J52	18B		REFER TO NETWORK	J1	8B
J52	19A	J130	14	¬¬¬	CH2XMTDATA(-)
J52	19B		REFER TO NETWORK	J3	11A
J52	2A	J130	8	¬¬¬	CH2SIG2(+)
J52	2B	J130	9	¬¬¬	CH2SIG2(-)
J52	20A	J130	3	¬¬¬	CH2RCVDATA(+)
J52	20B	J130	19	¬¬¬	CH2RCVDATA(-)
J52	21A	J130	12	¬¬¬	CH2SIG4(+)
J52	21B	J130	13	¬¬¬	CH2SIG4(-)

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J52 3A	J130 10	¬¬¬	CH2SIG3(+)
J52 3B	J130 11	¬¬¬	CH2SIG3(-)
J52 4A	REFER TO NETWORK	J20	20B
J52 4B	REFER TO NETWORK	J20	20B
J52 5B	REFER TO NETWORK	J9	11B
J52 6A	REFER TO NETWORK	J1	6A
J52 6B	REFER TO NETWORK	J1	6A
J52 7A	REFER TO NETWORK	J1	3A
J52 7B	REFER TO NETWORK	J1	3A
J52 8A	REFER TO NETWORK	J20	2A
J52 8B	REFER TO NETWORK	J31	3A
J52 9A	REFER TO NETWORK	J3	19B
J53 1A	REFER TO NETWORK	J35	13B
J53 1B	REFER TO NETWORK	J1	20B
J53 10A	REFER TO NETWORK	J1	12B
J53 11A	REFER TO NETWORK	J33	14A
J53 12A	REFER TO NETWORK	J9	22A
J53 13A	REFER TO NETWORK	J11	13A
J53 14B	REFER TO NETWORK	J20	8A
J53 15A	REFER TO NETWORK	J20	19A
J53 16A	J119 -V	¬¬¬	CHAN3ESIG
J53 17A	J118 -V	¬¬¬	CHAN3MSIG
J53 18A	J101 -E	¬¬¬	CH3XMTVFINT
J53 19A	J101 -F	¬¬¬	CH3XMTVFINR
J53 2A	REFER TO NETWORK	J1	14A
J53 2A	J101 -G	¬¬¬	C3RCVVFOUTT
J53 20B	J101 -H	¬¬¬	C3RCVVFOUTR
J53 22A	REFER TO NETWORK	J45	12A
J53 22B	REFER TO NETWORK	J45	12A
J53 3A	REFER TO NETWORK	J1	10B
J53 3B	REFER TO NETWORK	J1	10B
J53 5A	REFER TO NETWORK	J35	13A
J53 6A	REFER TO NETWORK	J20	4A
J53 6B	REFER TO NETWORK	J20	4A
J53 7A	REFER TO NETWORK	J1	3A
J53 7B	REFER TO NETWORK	J1	3A
J53 8A	REFER TO NETWORK	J20	3A
J53 9A	REFER TO NETWORK	J3	20B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J54 1A	J129 5	¬¬¬	CH3SIG1(+)
J54 1B	J124 6	¬¬¬	CH3SIG1(-)
J54 10A	REFER TO NETWORK	J5	10A
J54 10B	REFER TO NETWORK	J3	12B
J54 11A	REFER TO NETWORK	J33	14A
J54 11B	REFER TO NETWORK	J3	15B
J54 12A	REFER TO NETWORK	J9	10B
J54 12B	REFER TO NETWORK	J9	14B
J54 13A	REFER TO NETWORK	J33	3B
J54 13B	REFER TO NETWORK	J3	14B
J54 14A	REFER TO NETWORK	J3	4A
J54 14B	REFER TO NETWORK	J3	4A
J54 15A	J129 24	¬¬¬	CH3XMTCLKIN(+
J54 15B	J129 23	¬¬¬	CH3XMTCLKIN(-
J54 16A	J129 15	¬¬¬	CH3XMTCLKOT(+
J54 16B	J129 16	¬¬¬	CH3XMTCLKOT(-
J54 17A	J129 17	¬¬¬	CH3RCVCLK(+)
J54 17B	J129 18	¬¬¬	CH3RCVCLK(-)
J54 18A	J129 2	¬¬¬	CH3XMTDATA(+)
J54 18B	REFER TO NETWORK	J1	8B
J54 19A	J129 14	¬¬¬	CH3XMTDATA(-)
J54 19B	REFER TO NETWORK	J3	11A
J54 2A	J129 8	¬¬¬	CH3SIGR(+)
J54 2B	J129 9	¬¬¬	CH3SIG2(-)
J54 20A	J129 3	¬¬¬	CH3RCVDATA(+)
J54 20B	J129 19	¬¬¬	CH3RCVDATA(-)
J54 21A	J129 12	¬¬¬	CH3SIG4(+)
J54 21B	J129 13	¬¬¬	CH3SIG4(-)
J54 3A	J129 10	¬¬¬	CH3SIG3(+)
J54 3B	J129 11	¬¬¬	CH3SIG3(-)
J54 4A	REFER TO NETWORK	J20	20B
J54 4B	REFER TO NETWORK	J20	20B
J54 5B	REFER TO NETWORK	J9	11B
J54 6A	REFER TO NETWORK	J1	6A
J54 6B	REFER TO NETWORK	J2	6A
J54 7A	REFER TO NETWORK	J2	3A
J54 7B	REFER TO NETWORK	J1	3A
J54 8A	REFER TO NETWORK	J20	2A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J54 8B	REFER TO NETWORK	J31 3A	
J54 9A	REFER TO NETWORK	J3 20B	
J55 1A	REFER TO NETWORK	J11 18B	
J55 1B	REFER TO NETWORK	J1 20B	
J55 10A	REFER TO NETWORK	J1 12B	
J55 11A	REFER TO NETWORK	J33 14B	
J55 12A	REFER TO NETWORK	J9 22A	
J55 13A	REFER TO NETWORK	J11 13A	
J55 14B	REFER TO NETWORK	J20 8A	
J55 15A	REFER TO NETWORK	J20 19A	
J55 16A	J119 -A	¬¬¬	CHAN4ESIG
J55 17A	J118 -A	¬¬¬	CHAN4MSIG
J55 18A	J100 -A	¬¬¬	CH4XMTVFINT
J55 19A	J100 -B	¬¬¬	CH4XMTVFINR
J55 2A	REFER TO NETWORK	J1 18A	
J55 20A	J100 -C	¬¬¬	C4RCVVFOUTT
J55 20B	J100 -D	¬¬¬	C4RCVVFOUTR
J55 22A	REFER TO NETWORK	J45 12A	
J55 22B	REFER TO NETWORK	J45 12A	
J55 3A	REFER TO NETWORK	J1 10B	
J55 3B	REFER TO NETWORK	J1 10B	
J55 5A	REFER TO NETWORK	J11 18A	
J55 6A	REFER TO NETWORK	J20 4A	
J55 6B	REFER TO NETWORK	J20 4A	
J55 7A	REFER TO NETWORK	J1 3A	
J55 7B	REFER TO NETWORK	J1 3A	
J55 8A	REFER TO NETWORK	J20 3A	
J55 9A	REFER TO NETWORK	J3 21B	
J56 1A	J128 5	¬¬¬	CH4SIG1(+)
J56 1B	J128 6	¬¬¬	CH4SIG1(-)
J56 10A	REFER TO NETWORK	J5 10A	
J56 10B	REFER TO NETWORK	J3 12B	
J56 11A	REFER TO NETWORK	J33 14B	
J56 11B	REFER TO NETWORK	J3 15B	
J56 12A	REFER TO NETWORK	J9 10B	
J56 12B	REFER TO NETWORK	J9 14B	
J56 13A	REFER TO NETWORK	J33 3B	
J56 13B	REFER TO NETWORK	J3 14B	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM		TO		REF. DESG.	SIGNAL NAME
J56	14A		REFER TO NETWORK	J3	4A
J56	14B		REFER TO NETWORK	J3	4A
J56	15A	J128	24	¬¬¬	CH4XMTCLKIN(+
J56	15B	J128	23	¬¬¬	CH4XMTCLKIN(-
J56	16A	J128	15	¬¬¬	CH4XMTCLKOT(+
J56	16B	J128	16	¬¬¬	CH4XMTCLKOT(-
J56	17A	J128	17	¬¬¬	CH4RCVCLK(+)
J56	17B	J128	18	¬¬¬	CH4RCVCLK(-)
J56	18A	J128	2	¬¬¬	CH4XMTDATA(+)
J56	18B		REFER TO NETWORK	J1	8B
J56	19A	J128	14	¬¬¬	CH4XMTDATA(-)
J56	19B		REFER TO NETWORK	J3	11A
J56	2A	J128	8	¬¬¬	CH4SIG2(+)
J56	2B	J128	9	¬¬¬	CR4SIG2(-)
J56	20A	J128	3	¬¬¬	CH4RCVDATA(+)
J56	20B	J128	19	¬¬¬	CH4RCVDATA(-)
J56	21A	J128	12	¬¬¬	CH4SIG4(+)
J56	21B	J128	13	¬¬¬	CH4SIG4(-)
J56	3A	J128	10	¬¬¬	CH4SIG3(+)
J56	3B	J128	11	¬¬¬	CH4S1G3(-)
J56	4A		REFER TO NETWORK	J20	20B
J56	4B		REFER TO NETWORK	J20	20B
J56	5B		REFER TO NETWORK	J9	11B
J56	6A		REFER TO NETWORK	J1	6A
J56	6B		REFER TO NETWORK	J1	6A
J56	7A		REFER TO NETWORK	J1	3A
J56	7B		REFER TO NETWORK	J1	3A
J56	8A		REFER TO NETWORK	J20	2A
J56	8B		REFER TO NETWORK	J31	3A
J56	9A		REFER TO NETWORK	J3	21B
J57	1A		REFER TO NETWORK	J11	22B
J57	1B		REFER TO NETWORK	J1	20B
J57	10A		REFER TO NETWORK	J1	12B
J57	11A		REFER TO NETWORK	J33	9A
J57	12A		REFER TO NETWORK	J9	22A
J57	13A		REFER TO NETWORK	J11	13A
J57	14B		REFER TO NETWORK	J20	8A
J57	15A		REFER TO NETWORK	J20	19A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J57 16A	J119 -T	¬¬¬	CHAN5ESIG
J57 17A	J118 -T	¬¬¬	CHAN5MSIG
J57 18A	J100 -J	¬¬¬	CH5XMTVFINT
J57 19A	J100 -K	¬¬¬	CH5XMTVFINR
J57 2A	REFER TO NETWORK	J1	204
J57 20A	J100 -L	¬¬¬	C5RCVVFOUTT
J57 20B	J100 -M	¬¬¬	C5RCVVFOUTR
J57 22A	REFER TO NETWORK	J45	12A
J57 22B	REFER TO NETWORK	J45	12A
J57 3A	REFER TO NETWORK	J1	10B
J57 3B	REFER TO NETWORK	J1	10B
J57 5A	REFER TO NETWORK	J11	22A
J57 6A	REFER TO NETWORK	J20	4A
J57 6B	REFER TO NETWORK	J20	4A
J57 7A	REFER TO NETWORK	J1	3A
J57 7B	REFER TO NETWORK	J1	3A
J57 8A	REFER TO NETWORK	J20	3A
J57 9A	REFER TO NETWORK	J27	4B
J58 1A	J127 5	¬¬¬	CH5SIG1(+)
J58 1B	J127 6	¬¬¬	CH5SIG1(-)
J58 10A	REFER TO NETWORK	J5	10A
J58 10B	REFER TO NETWORK	J3	12B
J58 11A	REFER TO NETWORK	J33	9A
J58 11B	REFER TO NETWORK	J3	15B
J58 12A	REFER TO NETWORK	J9	10B
J58 12B	REFER TO NETWORK	J9	14B
J58 13A	REFER TO NETWORK	J33	3B
J58 13B	REFER TO NETWORK	J3	14B
J58 14A	REFER TO NETWORK	J3	4A
J58 14B	REFER TO NETWORK	J3	4A
J58 15A	J127 24	¬¬¬	CH5XMTCLKIN(+
J58 15B	J127 23	¬¬¬	CH5XMTCLKIN(-
J58 16A	J127 15	¬¬¬	CH5XMTCLKOT(+
J58 16B	J127 16	¬¬¬	CH5XMTCLKOT(-
J58 17A	J127 17	¬¬¬	CH5RCVCLK(+)
J58 17B	J127 18	¬¬¬	CH5RCVCLK(-)
J58 8A	J127 2	¬¬¬	CH5XMTDATA(+)
J58 8B	REFER TO NETWORK	J1	8B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J58 19A	J127 14	¬¬¬	CH5XMTDATA(-)
J58 19B	REFER TO NETWORK	J3 11A	
J58 2A	J127 8	¬¬¬	CH5SIG2(+)
J58 2B	J127 9	¬¬¬	CH5SIG2(-)
J58 20A	J127 3	¬¬¬	CH5RCVDATA(+)
J58 20B	J127 19	¬¬¬	CH5RCVDATA(-)
J58 21A	J127 12	¬¬¬	CH5SIG4(+)
J58 21B	J127 13	¬¬¬	CH5SIG4(-)
J58 3A	J127 10	¬¬¬	CH5SIG3(+)
J58 3B	J127 11	¬¬¬	CH5SIG3(-)
J58 4A	REFER TO NETWORK	J20 20B	
J58 4B	REFER TO NETWORK	J20 20B	
J58 5B	REFER TO NETWORK	J9 11B	
J58 6A	REFER TO NETWORK	J1 6A	
J58 6B	REFER TO NETWORK	J1 6A	
J58 7A	REFER TO NETWORK	J1 3A	
J58 7B	REFER TO NETWORK	J1 3A	
J58 8A	REFER TO NETWORK	J20 2A	
J58 8B	REFER TO NETWORK	J31 2A	
J58 9A	REFER TO NETWORK	J27 4B	
J59 1A	REFER TO NETWORK	J35 9B	
J59 1B	REFER TO NETWORK	J1 20B	
J59 10A	REFER TO NETWORK	J1 12B	
J59 11A	REFER TO NETWORK	J33 9B	
J59 12A	REFER TO NETWORK	J9 22A	
J59 13A	REFER TO NETWORK	J11 13A	
J59 14B	REFER TO NETWORK	J20 8A	
J59 15A	REFER TO NETWORK	J20 19A	
J59 16A	J119 -EE	¬¬¬	CHAN6ESIG
J59 17A	J110 -EE	¬¬¬	CHAN6MSIG
J59 18A	J100 -E	¬¬¬	CH6XMTVFINT
J59 19A	J100 -F	¬¬¬	CH6XMTVFINR
J59 2A	REFER TO NETWORK	J1 19A	
J59 20A	J200 -G	¬¬¬	C6RCVVFOUTT
J59 20B	J100 -H	¬¬¬	C6RCVVFOUTR
J59 22A	REFER TO NETWORK	J45 12A	
J59 22B	REFER TO NETWORK	J45 12A	
J59 3A	REFER TO NETWORK	J1 10B	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J59 3B	REFER TO NETWORK	J1	10B
J59 5A	REFER TO NETWORK	J35	9A
J59 6A	REFER TO NETWORK	J20	4A
J54 6B	REFER TO NETWORK	J20	4A
J59 7A	REFER TO NETWORK	J1	3A
J59 7B	REFER TO NETWORK	J1	3A
J59 8A	REFER TO NETWORK	J20	3A
J59 9A	REFER TO NETWORK	J27	6A
J60 1A	J126 5	¬¬¬	CH6SIG1(+)
J60 1B	J126 6	¬¬¬	CH6SIG1(-)
J60 10A	REFER TO NETWORK	J5	10A
J60 10B	REFER TO NETWORK	J3	12B
J60 11A	REFER TO NETWORK	J33	9B
J60 11B	REFER TO NETWORK	J3	15B
J60 12A	REFER TO NETWORK	J9	10B
J60 12B	REFER TO NETWORK	J9	14B
J60 13A	REFER TO NETWORK	J33	3B
J60 13B	REFER TO NETWORK	J3	14B
J60 14A	REFER TO NETWORK	J3	4A
J60 14B	REFER TO NETWORK	J3	4A
J60 15A	J126 24	¬¬¬	CH6XMTCLKIN(+
J60 15B	J126 23	¬¬¬	CH6XMTCLKIN(-
J60 16A	J126 15	¬¬¬	CH6XMTCLKOT(+
J60 16B	J126 16	¬¬¬	CH6XMTCLKOT(-
J60 17A	J126 17	¬¬¬	CH6RCVCLK(+)
J60 17B	J126 18	¬¬¬	CH6RCVCLK(-)
J60 18A	J126 2	¬¬¬	CH6XMTDATA(+)
J60 18B	REFER TO NETWORK	J1	8B
J60 19A	J126 14	¬¬¬	CH6XMTDATA(-)
J60 19A	REFER TO NETWORK	J3	11A
J60 2A	J126 8	¬¬¬	CH6SIG2(+)
J60 2B	J126 9	¬¬¬	CH6SIG2(-)
J60 20A	J126 3	¬¬¬	CH6RCVDATA(+)
J60 20B	J126 19	¬¬¬	CH6RCVDATA(-)
J60 21A	J126 12	¬¬¬	CH6SIG4(+)
J60 21B	J126 13	¬¬¬	CH6SIG4(-)
J60 3A	J126 10	¬¬¬	CH6SIG3(+)
J60 3B	J126 11	¬¬¬	CH6SIG3(-)

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J60 4A	REFER TO NETWORK	J20	20B
J60 4B	REFER TO NETWORK	J20	20B
J60 5B	REFER TO NETWORK	J9	11B
J60 6A	REFER TO NETWORK	J1	6A
J60 6B	REFER TO NETWORK	J1	6A
J60 7A	REFER TO NETWORK	J1	3A
J60 7B	REFER TO NETWORK	J1	3A
J60 8A	REFER TO NETWORK	J20	2A
J60 8B	REFER TO NETWORK	J31	3A
J60 9A	REFER TO NETWORK	J27	6A
J61 1A	REFER TO NETWORK	J11	16B
J61 1B	REFER TO NETWORK	J1	21B
J61 10A	REFER TO NETWORK	J1	12B
J61 11A	REFER TO NETWORK	J33	8A
J61 12A	REFER TO NETWORK	J9	22A
J61 13A	REFER TO NETWORK	J11	13A
J61 14B	REFER TO NETWORK	J20	8A
J61 15A	REFER TO NETWORK	J20	19A
J61 16A	J119 -S	¬¬¬	CHAN7ESIG
J61 17A	J118 -S	¬¬¬	CHAN7MSIG
J61 18A	J103 -A	¬¬¬	CH7XMTVFINT
J61 19A	J103 -B	¬¬¬	CH7XMTVFINR
J61 2A	REFER TO NETWORK	J1	17A
J61 20A	J103 -C	¬¬¬	C7RCVVFOUTT
J61 20B	J103 -D	¬¬¬	C7RCVVFOUTR
J61 22A	REFER TO NETWORK	J45	12A
J61 22B	REFER TO NETWORK	J45	12A
J61 3A	REFER TO NETWORK	J1	10B
J61 3B	REFER TO NETWORK	J1	10B
J61 5A	REFER TO NETWORK	J11	16A
J61 6A	REFER TO NETWORK	J20	4A
J61 6B	REFER TO NETWORK	J20	4A
J61 7A	REFER TO NETWORK	J1	3A
J61 7B	REFER TO NETWORK	J1	3A
J61 8A	REFER TO NETWORK	J20	3A
J61 9A	REFER TO NETWORK	J27	2B
J62 1A	J125 5	¬¬¬	CH7SIG1(+)
J62 1B	J125 6	¬¬¬	CH7SIG1(-)

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J62 10A	REFER TO NETWORK	J5	10A
J62 10B	REFER TO NETWORK	J3	12B
J62 11A	REFER TO NETWORK	J33	8A
J62 11B	REFER TO NETWORK	J3	15B
J62 12A	REFER TO NETWORK	J9	10B
J62 12B	REFER TO NETWORK	J9	14B
J62 13A	REFER TO NETWORK	J33	3B
J62 13B	REFER TO NETWORK	J3	14B
J62 14A	REFER TO NETWORK	J3	4A
J62 14B	REFER TO NETWORK	J3	4A
J62 15A	J125 24	¬¬¬	CH7XMTCLKIN(+
J62 15B	J125 23	¬¬¬	CH7XMTCLKIN(-
J62 16A	J125 15	¬¬¬	CH7XMTCLKOT(+
J62 16B	J125 16	¬¬¬	CH7XMTCLKOT(-
J62 17A	J125 17	¬¬¬	CH7RCVCLK(+)
J62 17B	J125 18	¬¬¬	CH7RCVCLK(-)
J62 18A	J125 2	¬¬¬	CH7XMTDATA(+)
J62 18B	REFER TO NETWORK	J1	8B
J62 19A	J125 14	¬¬¬	CH7XMTDATA(-)
J62 19B	REFER TO NETWORK	J3	11A
J62 2A	J125 8	¬¬¬	CH7SIG2(+)
J62 2B	J125 9	¬¬¬	CH7SIG2(-)
J62 20A	J125 3	¬¬¬	CH7RCVDATA(+
J62 20B	J125 19	¬¬¬	CH7RCVDATA(-
J62 21A	J125 12	¬¬¬	CH7SIG4(+)
J62 21B	J125 13	¬¬¬	CH7SIG4(-)
J62 3A	J125 10	¬¬¬	CH7SIG3(+)
J62 3B	J125 11	¬¬¬	CH7SIG3(-)
J62 4A	REFER TO NETWORK	J20	20B
J62 4B	REFER TO NETWORK	J20	20B
J62 5B	REFER TO NETWORK	J9	11B
J62 6A	REFER TO NETWORK	J1	6A
J62 6B	REFER TO NETWORK	J1	6A
J62 7A	REFER TO NETWORK	J1	3A
J62 7B	REFER TO NETWORK	J1	3A
J62 8A	REFER TO NETWORK	J20	2A
J62 8B	REFER TO NETWORK	J31	3A
J62 9A	REFER TO NETWORK	J27	2B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J63 1A	REFER TO NETWORK	J35	3B
J63 1B	REFER TO NETWORK	J1	21B
J63 10A	REFER TO NETWORK	J1	12B
J63 11A	REFER TO NETWORK	J33	8B
J63 12A	REFER TO NETWORK	J9	22A
J63 13A	REFER TO NETWORK	J11	13A
J63 14B	REFER TO NETWORK	J20	8A
J63 15A	REFER TO NETWORK	J20	19A
J63 16A	J119 -R	¬¬¬	CHAN8ESIG
J63 17A	J118 -R	¬¬¬	CHAN8MSIG
J63 18A	J103 -J	¬¬¬	CH8XMTVFINT
J63 19A	J103 -K	¬¬¬	CH8XMTVFINR
J63 2A	REFER TO NETWORK	J1	21A
J63 20A	J103 -L	¬¬¬	C8RCVVFOUTT
J63 20B	J103 -M	¬¬¬	C8RCVVFOUTR
J63 22A	REFER TO NETWORK	J45	12A
J63 22B	REFER TO NETWORK	J45	12A
J63 3A	REFER TO NETWORK	J1	10B
J63 3B	REFER TO NETWORK	J1	10B
J63 5A	REFER TO NETWORK	J35	3A
J63 6A	REFER TO NETWORK	J20	4A
J63 6B	REFER TO NETWORK	J20	4A
J63 7A	REFER TO NETWORK	J1	3A
J63 7B	REFER TO NETWORK	J1	3A
J63 8A	REFER TO NETWORK	J20	3A
J63 9A	REFER TO NETWORK	J27	1B
J64 1A	J124 5	¬¬¬	CH8SIG1(+)
J64 1A	J124 6	¬¬¬	CH8SIG1(-)
J64 10A	REFER TO NETWORK	J5	10A
J64 10B	REFER TO NETWORK	J3	12B
J64 11A	REFER TO NETWORK	J33	8B
J64 11B	REFER TO NETWORK	J3	15B
J64 12A	REFER TO NETWORK	J9	10B
J64 12B	REFER TO NETWORK	J9	14B
J64 13A	REFER TO NETWORK	J33	3B
J64 13B	REFER TO NETWORK	J3	14B
J64 14A	REFER TO NETWORK	J3	4A
J64 14B	REFER TO NETWORK	J3	4A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J64 15A	J124 24	¬¬¬	CHBXMTCLKIN(+
J64 15B	J124 23	¬¬¬	CH8XMTCLKIN(-
J64 16A	J124 15	¬¬¬	CH8XMTCLKOT(+
J64 16B	J124 16	¬¬¬	CH8XMTCLKOT(-
J64 17A	J124 17	¬¬¬	CH3RCVCLK(+)
J64 17B	J124 18	¬¬¬	CH8RCVCLK(-)
J64 18A	J124 2	¬¬¬	CH8XMTDATA(+)
J64 18B	REFER TO NETWORK	J1 8B	
J64 19A	J124 14	¬¬¬	CH8XMTDATA(-)
J64 19B	REFER TO NETWORK	J3 114	
J64 2A	J124 8	¬¬¬	CH8SIG2(+)
J64 2B	J124 9	¬¬¬	CH8SIG2(-)
J64 20A	J124 3	¬¬¬	CH8RCVDATA(+)
J64 20B	J124 19	¬¬¬	CH8RCVDATA(-)
J64 21A	J124 12	¬¬¬	CH8SIG4(+)
J64 21B	J124 13	¬¬¬	CH8SIG4(-)
J64 3A	J124 10	¬¬¬	CH8SIG3(+)
J64 3B	J124 11	¬¬¬	CH8SIG3(-)
J64 4A	REFER TO NETWORK	J20 20B	
J64 4B	REFER TO NETWORK	J20 20B	
J64 5B	REFER TO NETWORK	J9 11B	
J64 6A	REFER TO NETWORK	J1 6A	
J64 6B	REFER TO NETWORK	J1 6A	
J64 7A	REFER TO NETWORK	J1 3A	
J64 7B	REFER TO NETWORK	J1 3A	
J64 8A	REFER TO NETWORK	J20 2A	
J64 8B	REFER TO NETWORK	J31 3A	
J64 9A	REFER TO NETWORK	J27 1B	
J65 1A	REFER TO NETWORK	J35 15B	
J65 1B	REFER TO NETWORK	J25 3B	
J65 10A	REFER TO NETWORK	J1 12B	
J65 11A	REFER TO NETWORK	J33 7A	
J65 12A	REFER TO NETWORK	J9 22A	
J65 13A	REFER TO NETWORK	J11 13A	
J65 14B	REFER TO NETWORK	J20 8A	
J65 15A	REFER TO NETWORK	J20 19A	
J65 16A	J119 -E	¬¬¬	CHAN9ESIG
J65 17A	J118 -E	¬¬¬	CHAN9MSIG

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J65 18A	J103 -E	¬¬¬	CH9XMTVFINT
J65 19A	J103 -F	¬¬¬	CH9XMTVFINR
J65 2A	REFER TO NETWORK	J25	3A
J65 20A	J103 -G	¬¬¬	C9RCVVFOUTT
J65 20B	J103 -H	¬¬¬	C9RCVVFOUTR
J65 22A	REFER TO NETWORK	J45	12A
J65 22B	REFER TO NETWORK	J45	12A
J65 3A	REFER TO NETWORK	J1	10B
J65 3B	REFER TO NETWORK	J1	10B
J65 5A	REFER TO NETWORK	J35	15A
J65 6A	REFER TO NETWORK	J20	4A
J65 6B	REFER TO NETWORK	J20	4A
J65 7A	REFER TO NETWORK	J1	3A
J65 7B	REFER TO NETWORK	J1	34
J65 8A	REFER TO NETWORK	J20	3A
J65 9A	REFER TO NETWORK	J P7	7A
J66 1A	J123 5	¬¬¬	CR9SIG1(+)
J66 1B	J123 6	¬¬¬	CH9SIG1(-)
J66 10A	REFER TO NETWORK	J5	10A
J66 10B	REFER TO NETWORK	J3	12B
J66 11A	REFER TO NETWORK	J33	7A
J66 11B	REFER TO NETWORK	J3	15B
J66 12A	REFER TO NETWORK	J9	10B
J66 12B	REFER TO NETWORK	J9	14B
J66 13A	REFER TO NETWORK	J33	4A
J66 13B	REFER TO NETWORK	J3	14B
J66 14A	REFER TO NETWORK	J3	4A
J66 14B	REFER TO NETWORK	J3	4A
J66 15A	J123 24	¬¬¬	CH9XMTCLKIN(+
J66 15B	J123 23	¬¬¬	CH9XMTCLKIN(-
J66 16A	J123 15	¬¬¬	CH9XMTCLKOT(+
J66 16B	J123 16	¬¬¬	CH9XMTCLKOT(-
J66 17A	J123 17	¬¬¬	CH9RCVCLK(+)
J66 17B	J123 18	¬¬¬	CH9RCVCLK(-)
J66 18A	J123 2	¬¬¬	CH9XMTDATA(+)
J66 18B	REFER TO NETWORK	J1	8B
J66 19A	J123 14	¬¬¬	CH9XMTDATA(-)
J66 19B	REFER TO NETWORK	J3	11A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J66 2A	J123 8	¬¬¬	CH9SIG2(+)
J66 2B	J123 9	¬¬¬	CH9SIG2(-)
J66 20A	J123 3	¬¬¬	CH9RCVDATA(+)
J66 20B	J123 19	¬¬¬	CH9RCVDATA(-)
J66 21A	J123 12	¬¬¬	CH9SIG4(+)
J66 21B	J123 13	¬¬¬	CH9SIG4(-)
J66 3A	J123 10	¬¬¬	CH9SIG3(+)
J66 3B	J123 11	¬¬¬	CH9SIG3(-)
J66 4A	REFER TO NETWORK	J31	7A
J66 4B	REFER TO NETWORK	J3	7A
J66 5B	REFER TO NETWORK	J9	11B
J66 6A	REFER TO NETWORK	J1	6A
J66 6B	REFER TO NETWORK	J1	6A
J66 7A	REFER TO NETWORK	J1	3A
J66 7B	REFER TO NETWORK	J1	3A
J66 8A	REFER TO NETWORK	J20	2A
J66 8B	REFER TO NETWORK	J31	3A
J66 9A	REFER TO NETWORK	J27	7A
J67 1A	REFER TO NETWORK	J11	16B
J67 1B	REFER TO NETWORK	J25	2B
J67 10A	REFER TO NETWORK	J1	12B
J67 11A	REFER TO NETWORK	J33	7B
J67 12A	REFER TO NETWORK	J9	22A
J67 13A	REFER TO NETWORK	J11	13A
J67 14B	REFER TO NETWORK	J20	8A
J67 15A	REFER TO NETWORK	J20	19A
J67 16A	J119 -D	¬¬¬	CHAN10ESIG
J67 17A	J118 -D	¬¬¬	CHAN10MSIG
J67 18A	J102 -A	¬¬¬	CH10XMTVFINT
J67 19A	J102 -B	¬¬¬	CH10XMTVFINR
J67 2A	REFER TO NETWORK	J25	2A
J67 20A	J102 -C	¬¬¬	C10RCVVFOUTT
J67 20B	J102 -D	¬¬¬	C10RCVVFOUTR
J67 22A	REFER TO NETWORK	J45	12A
J67 22B	REFER TO NETWORK	J45	12A
J67 3A	REFER TO NETWORK	J1	10B
J67 3B	REFER TO NETWORK	J1	10B
J67 5A	REFER TO NETWORK	J11	20A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J67 6A	REFER TO NETWORK	J20	44
J67 6B	REFER TO NETWORK	J20	4A
J67 7A	REFER TO NETWORK	J1	3A
J67 7B	REFER TO NETWORK	J1	3A
J67 8A	REFER TO NETWORK	J20	3A
J67 9A	REFER TO NETWORK	J27	5B
J68 1A	J122 5	¬¬¬	CH10SIG1(+)
J68 1B	J122 6	¬¬¬	CH10SIG1(-)
J68 10A	REFER TO NETWORK	J5	10A
J68 10B	REFER TO NETWORK	J3	12B
J68 11A	REFER TO NETWORK	J33	7B
J68 11B	REFER TO NETWORK	J3	15B
J68 12A	REFER TO NETWORK	J9	10B
J68 12B	REFER TO NETWORK	J9	14B
J68 13A	REFER TO NETWORK	J33	3B
J68 13B	REFER TO NETWORK	J3	14B
J68 14A	REFER TO NETWORK	J3	4A
J68 14B	REFER TO NETWORK	J3	4A
J68 15A	J122 24	¬¬¬	CH10XMTCLKIN(
J68 15B	J122 23	¬¬¬	CH10XMTCLKIN(
J68 16A	J122 15	¬¬¬	CH10XMTCLKOT(
J68 16B	J122 16	¬¬¬	CH10XMTCLKOT(
J68 17A	J122 17	¬¬¬	CH10RCVCLK(+)
J68 17B	J122 16	¬¬¬	CH10RCVCLK(-)
J68 18A	J122 2	¬¬¬	CH10XMTDATA(+
J68 18B	REFER TO NETWORK	J1	8P
J68 19A	J122 14	¬¬¬	CH10XTDATA(-
J68 19B	REFER TO NETWORK	J3	114
J68 2A	J122 8	¬¬¬	CH10SIG2(+)
J68 2B	J122 9	¬¬¬	CH10SIG2(-)
J68 20A	J122 3	¬¬¬	CH10RCVDATA(+
J68 20B	J122 19	¬¬¬	CH10RCVDATA(-
J68 21A	J122 12	¬¬¬	CH10SIG4(+)
J68 21B	J122 13	¬¬¬	CH10SIG4(-)
J68 3A	J122 10	¬¬¬	CH10SIG3(+)
J68 3B	J122 11	¬¬¬	CH10SIG3(-)
J68 4A	REFER TO NETWORK	J31	7A
J68 4B	REFER TO NETWORK	J31	7A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J68 5B	REFER TO NETWORK	J9	11B
J68 6A	REFER TO NETWORK	J1	6A
J68 6B	REFER TO NETWORK	J1	6A
J68 7A	REFER TO NETWORK	J1	3A
J68 7B	REFER TO NETWORK	J1	3A
J68 8A	REFER TO NETWORK	J20	2A
J68 8B	REFER TO NETWORK	J31	3A
J68 9A	REFER TO NETWORK	J27	5B
J69 1A	REFER TO NETWORK	J1	16B
J69 1B	REFER TO NETWORK	J1	20B
J69 10A	REFER TO NETWORK	J1	12B
J69 11A	REFER TO NETWORK	J33	6A
J69 12A	REFER TO NETWORK	J9	22A
J69 13A	REFER TO NETWORK	J11	13A
J69 14B	REFER TO NETWORK	J20	8A
J69 15A	REFER TO NETWORK	J20	19A
J69 16A	J119 -X	¬¬¬	CHAN11ESIG
J69 17A	J118 -X	¬¬¬	CHAN11MSIG
J69 18A	J102 -J	¬¬¬	CH11XMTVFINT
J69 19A	J102 -K	¬¬¬	CH11XMTVFINR
J69 2A	REFER TO NETWORK	J1	22A
J69 20A	J102 -L	¬¬¬	C11RCVVFOUTT
J69 20B	J102 -M	¬¬¬	C11RCVVFOUTR
J69 22A	REFER TO NETWORK	J45	12A
J69 22B	REFER TO NETWORK	J45	12A
J69 3A	REFER TO NETWORK	J1	10B
J69 3B	REFER TO NETWORK	J1	10B
J69 5A	REFER TO NETWORK	J35	5A
J69 6A	REFER TO NETWORK	J20	4A
J69 6B	REFER TO NETWORK	J20	4A
J69 7A	REFER TO NETWORK	J1	3A
J69 7B	REFER TO NETWORK	J1	3A
J69 8A	REFER TO NETWORK	J20	3A
J69 9A	REFER TO NETWORK	J27	6B
J70 1A	J121 5	¬¬¬	CH11SIG1(+)
J70 1B	J121 6	¬¬¬	CH11SIG1(-)
J70 10A	REFER TO NETWORK	J5	10A
J70 10B	REFER TO NETWORK	J3	123

Table B-1. Rear Assembly Wife Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J70 11A	REFER TO NETWORK	J33 6A	
J70 11B	REFER TO NETWORK	J3 15B	
J70 12A	REFER TO NETWORK	J9 10B	
J70 12B	REFER TO NETWORK	J9 14B	
J70 13A	REFER TO NETWORK	J33 3B	
J70 13B	REFER TO NETWORK	J3 14B	
J70 14A	REFER TO NETWORK	J3 4A	
J70 14B	REFER TO NETWORK	J3 4A	
J70 15A	J121 24	¬¬¬	CH11XMTCLKIN(
J70 15B	J121 23	¬¬¬	CH11XMTCLKIN(
J70 16A	J121 15	¬¬¬	CH11XMTCLKOT(
J70 16B	J121 16	¬¬¬	CH11XMTCLKOT(
J70 17A	J121 17	¬¬¬	CH11RCVCLK(+)
J70 17B	J121 18	¬¬¬	CH11RCVCLK(-)
J70 18A	J121 2	¬¬¬	CH11XMTDATA (+
J70 18B	REFER TO NETWORK		
J70 19A	J121 14	¬¬¬	CH11XMTDATA(-
J70 19B	REFER TO NETWORK	J3 11A	
J70 2A	J121 8	¬¬¬	CH11SIG2(+)
J70 2B	J121 9	¬¬¬	CH11SIG2(-)
J70 20A	J121 3	¬¬¬	CH11RCVDATA(+
J70 20B	J121 19	¬¬	CH11RCVDATA(-
J70 21A	J121 12	¬¬¬	CH11SIG4(+)
J70 21B	J121 13	¬¬¬	CH11SIG4(-)
J70 3A	J121 10	¬¬¬	CH11SIG3(+)
J70 3B	J121 11	¬¬¬	CH11SIG3(-)
J70 4A	REFER TO NETWORK	J31 7A	
J70 4B	REFER TO NETWORK	J31 7A	
J70 5B	REFER TO NETWORK	J9 11B	
J70 6A	REFER TO NETWORK	J1 6A	
J70 6B	REFER TO NETWORK	J1 5A	
J70 7A	REFER TO NETWORK	J1 3A	
J70 7B	REFER TO NETWORK	J1 3A	
J70 8A	REFER TO NETWORK	J20 2A	
J70 8B	REFER TO NETWORK	J31 3A	
J70 9A	REFER TO NETWORK	J27 6B	
J71 1A	REFER TO NETWORK	J35 12B	
J71 1B	REFER TO NETWORK	J25 1B	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J71 10A	REFER TO NETWORK	J1	12B
J71 11A	REFER TO NETWORK	J33	6B
J71 12A	REFER TO NETWORK	J9	22A
J71 13A	REFER TO NETWORK	J11	13A
J71 14B	REFER TO NETWORK	J20	8A
J71 15A	REFER TO NETWORK	J20	19A
J71 16A	119q	-W	¬¬¬	CHAN12ESIG
J71 17A	J118	-W	¬¬¬	CHAN12MSIG
J71 18A	J102	-E	¬¬¬	CH12XMTVFINT
J71 19A	J102	-F	¬¬¬	CH12XMTVFINR
J71 2A	REFER TO NETWORK	J25	1A
J71 20A	J102	-G	¬¬¬	C12RCVVFOUTT
J71 20B	J102	-H	¬¬¬	C12RCVVFOUTR
J71 22A	REFER TO NETWORK	J45	12A
J71 22B	REFER TO NETWORK	J45	12A
J71 3A	REFER TO NETWORK	J1	10B
J71 3B	REFER TO NETWORK	J1	10B
J71 5A	REFER TO NETWORK	J35	12A
J71 6A	REFER TO NETWORK	J20	4A
J71 6B	REFER TO NETWORK	J20	4A
J71 7A	REFER TO NETWORK	J1	3A
J71 7B	REFER TO NETWORK	J1	3A
J71 8A	REFER TO NETWORK	J20	3A
J71 9A	REFER TO NETWORK	J27	8A
J72 1A	J120	5	¬¬¬	CH12SIG1(+)
J72 1B	J120	6	¬¬¬	CH12SIG1(-)
J72 10A	REFER TO NETWORK	J5	10A
J72 10B	REFER TO NETWORK	J3	12B
J72 11A	REFER TO NETWORK	J33	6B
J72 11B	REFER TO NETWORK	J3	15B
J72 12A	REFER TO NETWORK	J9	10B
J72 12B	REFER TO NETWORK	J9	14B
J72 13A	REFER TO NETWORK	J33	3B
J72 13B	REFER TO NETWORK	J3	14B
J72 14A	REFER TO NETWORK	J3	4A
J72 14B	REFER TO NETWORK	J3	4A
J72 15A	J120	24	¬¬¬	CH12XMTCLKIN(
J72 15B	J120	23	¬¬¬	CH12XMTCLKIN(

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO		REF. DESG.	SIGNAL NAME
J72 16A	J120	15	¬¬¬	CH12XMTCLKOT(
J72 16B	J120	16	¬¬¬	CH12XMTCLKOT(
J72 17A	J120	17	¬¬¬	CH12RCVCLK(+)
J72 17B	J120	18	¬¬¬	CH12RCVCLK(-)
J72 18A	J120	2	¬¬¬	CH12XMTDATA(+
J72 18B	REFER TO NETWORK		J1	8B
J72 19A	J120	14	¬¬¬	CH12XMTDATA(-
J72 19B	REFER TO NETWORK		J3	11A
J72 2A	J120	8	¬¬¬	CH12SIG2(+)
J72 2B	J120	9	¬¬¬	CH12SIG2(-)
J72 20A	J120	3	¬¬¬	CH12RCVDATA(+
J72 20B	J120	19	¬¬¬	CH12RCVDATA(-
J72 21A	J120	12	¬¬¬	CH12SIG4(+)
J72 21B	J120	13	¬¬¬	CH12SIG4(-)
J72 3A	J120	10	¬¬¬	CH12SIG3(+)
J72 3B	J120	11	¬¬¬	CH12SIG3(-)
J72 4A	REFER TO NETWORK		J31	7A
J72 4B	REFER TO NETWORK		J31	7A
J72 5B	REFER TO NETWORK		J9	11B
J72 6A	REFER TO NETWORK		J1	6A
J72 6B	REFER TO NETWORK		J1	6A
J72 7A	REFER TO NETWORK		J1	3A
J72 7B	REFER TO NETWORK		J1	3A
J72 8A	REFER TO NETWORK		J20	2A
J72 8B	REFER TO NETWORK		J31	3A
J72 9A	REFER TO NETWORK		J27	8A
J73 1A	REFER TO NETWORK		J11	14B
J73 1B	REFER TO NETWORK		J1	20B
J73 10A	REFER TO NETWORK		J1	12B
J73 11A	REFER TO NETWORK		J33	13A
J73 12A	REFER TO NETWORK		J9	22A
J73 13A	REFER TO NETWORK		J11	13A
J73 14B	REFER TO NETWORK		J20	8A
J73 15A	REFER TO NETWORK		J20	19A
J73 16A	J119	-DD	¬¬¬	CHAN13ESIG
J73 17A	J118	-DD	¬¬¬	CHAN13MSIG
J73 18A	J105	-A	¬¬¬	CH13XMTVFINT
J73 19A	J105	-B	¬¬¬	CH13XMTVFINR

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J73 2A	REFER TO NETWORK	J25	5A
J73 20A	J105	-C	¬¬¬	C13RCVVFOUTT
J73 20B	J105	-D	¬¬¬	C13RCVVFOUTR
J73 22A	REFER TO NETWORK	J45	12A
J73 22B	REFER TO NETWORK	J45	12A
J73 3A	REFER TO NETWORK	J1	10B
J73 3B	REFER TO NETWORK	J1	10B
J73 5A	REFER TO NETWORK	J11	14A
J73 6A	REFER TO NETWORK	J1	6A
J73 6B	REFER TO NETWORK	J1	6A
J73 7A	REFER TO NETWORK	J1	3A
J73 7B	REFER TO NETWORK	J1	3A
J73 8A	REFER TO NETWORK	J20	3A
J73 9A	REFER TO NETWORK	J47	10B
J74 1A	J137	5	¬¬¬	CH13SIG1(+)
J74 1B	J137	6	¬¬¬	CH13SIG1(-)
J74 10A	REFER TO NETWORK	J5	10A
J74 10B	REFER TO NETWORK	J3	12B
J74 11A	REFER TO NETWORK	J33	13A
J74 11B	REFER TO NETWORK	J3	15B
J74 12A	REFER TO NETWORK	J9	10B
J74 12B	REFER TO NETWORK	J9	14B
J74 13A	REFER TO NETWORK	J33	3B
J74 13B	REFER TO NETWORK	J3	14B
J74 14A	REFER TO NETWORK	J1	7B
J74 14B	REFER TO NETWORK	J1	7B
J74 15A	J137	24	¬¬¬	CH13XMTCLKIN(
J74 15B	J137	23	¬¬¬	CH13XMTCLKIN(
J74 16A	J137	15	¬¬¬	CH13XMTCLKOT(
J74 16B	J137	16	¬¬¬	CH13XMTCLKOT(
J74 17A	J137	17	¬¬¬	CH13RCVCLK(+)
J74 17B	J137	18	¬¬¬	CH13RCVCLK(-)
J74 18A	J137	2	¬¬¬	CH13XMTDATA(+
J74 18B	REFER TO NETWORK	J1	8B
J74 19A	J137	14	¬¬¬	CH13XMTDATA(-
J74 19B	REFER TO NETWORK	J3	11A
J74 2A	J137	8	¬¬¬	CH13SIG2(+)
J74 2B	J137	9	¬¬¬	CH13SIG2(-)

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J74 20A	J137 3	¬¬¬	CH13RCVDATA(+
J74 20B	J137 19	¬¬¬	CH13RCVDATA(-
J74 21A	J137 12	¬¬¬	CH13SIG4(+)
J74 218B	J137 13	¬¬¬	CH13SIG4(-)
J74 3A	J137 10	¬¬¬	CH13SIG3(+)
J74 3B	J137 11	¬¬¬	CH13SIG3(-)
J74 4A	REFER TO NETWORK	J31 7A	
J74 4B	REFER TO NETWORK	J31 7A	
J74 5B	REFER TO NETWORK	J9 11B	
J74 6A	REFER TO NETWORK	J1 6A	
J74 6B	REFER TO NETWORK	J1 6A	
J74 7A	REFER TO NETWORK	J1 3A	
J74 7B	REFER TO NETWORK	J1 3A	
J74 8A	REFER TO NETWORK	J20 2A	
J74 8B	REFER TO NETWORK	J31 3A	
J74 9A	REFER TO NETWORK	J27 10B	
J75 1A	REFER TO NETWORK	J35 1B	
J75 1B	REFER TO NETWORK	J25 4B	
J75 10A	REFER TO NETWORK	J1 12B	
J75 11A	REFER TO NETWORK	J33 13B	
J75 12A	REFER TO NETWORK	J9 22A	
J75 13A	REFER TO NETWORK	J11 13A	
J75 14B	REFER TO NETWORK	J20 8A	
J75 15A	REFER TO NETWORK	J20 19A	
J75 16A	J119 -CC	¬¬¬	CHAN14ESIG
J75 17A	J118 -CC	¬¬¬	CHAN14MSIG
J75 18A	J105 -J	¬¬¬	CH14XMTVFINT
J75 19A	J105 -K	¬¬¬	CH14XMTVFINR
J75 2A	REFER TO NETWORK	J25 4A	
J75 20A	J105 -L	¬¬¬	C14RCVVFOUTT
J75 20B	J105 -M	¬¬¬	C14RCVVFOUTR
J75 22A	REFER TO NETWORK	J45 12A	
J75 22B	REFER TO NETWORK	J45 12A	
J75 3A	REFER TO NETWORK	J1 10B	
J75 3B	REFER TO NETWORK	J1 10B	
J75 5A	REFER TO NETWORK	J35 1A	
J75 6A	REFER TO NETWORK	J1 6A	
J75 6B	REFER TO NETWORK	J1 6A	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J75 7A	REFER TO NETWORK	J1	3A
J75 7B	REFER TO NETWORK	J1	3A
J75 8A	REFER TO NETWORK	J20	3A
J75 9A	REFER TO NETWORK	J27	9A
J77 1A	REFER TO NETWORK	J35	10B
J77 1B	REFER TO NETWORK	J25	6B
J77 10A	REFER TO NETWORK	J1	12B
J77 11A	REFER TO NETWORK	J33	12A
J77 12A	REFER TO NETWORK	J9	22A
J77 13A	REFER TO NETWORK	J11	13A
J77 14B	REFER TO NETWORK	J20	8A
J77 15A	REFER TO NETWORK	J20	19A
J77 16A	J119 -P	¬¬¬	CHAN15ESIG
J77 17A	J118 -P	¬¬¬	CHAN15MSIG
J77 18A	J105 -E	¬¬¬	CH15XMTVFINT
J77 19A	J105 -F	¬¬¬	CH15XMTVFINR
J77 2A	REFER TO NETWORK	J25	6A
J77 20A	J105 -G	¬¬¬	C15RCVVFOUJTT
J77 20B	J105 -H	¬¬¬	C15RCVVFOUTR
J77 22A	REFER TO NETWORK	J45	12A
J77 22B	REFER TO NETWORK	J45	12A
J77 3A	REFER TO NETWORK	J1	10B
J77 3B	REFER TO NETWORK	J1	10B
J77 5A	REFER TO NETWORK	J35	10A
J77 6A	REFER TO NETWORK	J1	6A
J77 6B	REFER TO NETWORK	J1	6A
J77 7A	REFER TO NETWORK	J1	3A
J77 7B	REFER TO NETWORK	J1	3A
J77 8A	REFER TO NETWORK	J20	3A
J77 9A	REFER TO NETWORK	J27	11A
J78 1A	J136 5	¬¬¬	CH15SIG1(+)
J78 1B	J136 6	¬¬¬	CH15SIG1(-)
J78 10A	REFER TO NETWORK	J5	10A
J78 10B	REFER TO NETWORK	J3	12B
J78 11A	REFER TO NETWORK	J33	12A
J78 11B	REFER TO NETWORK	J3	15B
J78 12A	REFER TO NETWORK	J9	10B
J78 12B	REFER TO NETWORK	J9	14B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J78 13A	REFER TO NETWORK	J33	3B
J78 13B	REFER TO NETWORK	J3	14B
J78 14A	REFER TO NETWORK	J1	7B
J78 14B	REFER TO NETWORK	J1	7B
J78 15A	J136 24	¬¬¬	CH15XMTCLKIN(
J78 15B	J136 23	¬¬¬	CH15XMTCLKIN(
J78 16A	J136 15	¬¬¬	CH15XMTCLKOT(
J78 16B	J136 16	¬¬¬	CH15XMTCLKOT(
J78 17A	J136 17	¬¬¬	CH15RCVCLK(+)
J78 17B	J136 18	¬¬¬	CH15RCVCLK(-)
J78 18A	J136 2	¬¬¬	CH15XMTDATA(+
J78 18B	REFER TO NETWORK	J1	8B
J78 19A	J136 14		CH15XMTDATA(-
J78 19B	REFER TO NETWORK	J3	114
J78 2A	J136 8	¬¬¬	CH15SIG2(+)
J78 2B	J136 9	¬¬¬	CH15SIG2(-)
J78 20A	J136 3	¬¬¬	CH15RCVDATA(+
J78 20B	J136 19	¬¬¬	CH15RCVDATA(-
J78 21A	J136 12	¬¬¬	CH15SIG4(+)
J78 21B	J136 13	¬¬¬	CH15SIG4(-)
J78 3A	J136 10	¬¬¬	CH15SIG3(+)
J78 3B	J136 11	¬¬¬	CH15SIG3(-)
J78 4A	REFER TO NETWORK	J31	7A
J78 4B	REFER TO NETWORK	J31	7A
J78 5B	REFER TO NETWORK	J9	11B
J78 6A	REFER TO NETWORK	J1	6A
J78 6B	REFER TO NETWORK	J1	6A
J78 7A	REFER TO NETWORK	J1	3A
J78 7B	REFER TO NETWORK	J1	3A
J78 8A	REFER TO NETWORK	J20	2A
J78 8B	REFER TO NETWORK	J31	3A
J78 9A	REFER TO NETWORK	J27	11A
J79 1A	REFER TO NETWORK	J11	17B
J79 1B	REFER TO NETWORK	J25	7B
J79 10A	REFER TO NETWORK	J1	12B
J79 11A	REFER TO NETWORK	J33	12B
J79 12A	REFER TO NETWORK	J9	22A
J79 13A	REFER TO NETWORK	J11	13A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J79 14B	REFER TO NETWORK	J20	8A
J79 15A	REFER TO NETWORK	J20	19A
J79 16A	J119 -N	¬¬¬	CHAN16ESIG
J79 17A	J118 -N	¬¬¬	CHAN16MSIG
J79 14A	J104 -A	¬¬¬	CH16XMTVFINT
J79 19A	J104 -B	¬¬¬	CH16XMTVFINR
J79 2A	REFER TO NETWORK	J25	7A
J79 20A	J104 -C	¬¬¬	C16RCVVFOUTT
J79 20B	J104 -D	¬¬¬	C16RCVVFOUTR
J79 22A	REFER TO NETWORK	J45	12A
J79 22B	REFER TO NETWORK	J45	12A
J79 3A	REFER TO NETWORK	J1	10B
J79 3B	REFER TO NETWORK	J1	10B
J79 5A	REFER TO NETWORK	J11	17A
J79 6A	REFER TO NETWORK	J1	6A
J79 6B	REFER TO NETWORK	J1	6A
J79 7A	REFER TO NETWORK	J1	3A
J79 7B	REFER TO NETWORK	J1	3A
J79 8A	REFER TO NETWORK	J20	3A
J79 9A	REFER TO NETWORK	J27	3B
J81 1A	REFER TO NETWORK	J35	7B
J81 1B	REFER TO NETWORK	J1	20B
J81 10A	REFER TO NETWORK	J1	12B
J81 11A	REFER TO NETWORK	J33	10B
J81 12A	REFER TO NETWORK	J9	22A
J81 13A	REFER TO NETWORK	J11	13A
J81 14B	REFER TO NETWORK	J20	8A
J81 15A	REFER TO NETWORK	J20	19A
J81 16A	J119 -F	¬¬¬	CHAN17ESIG
J81 17A	J118 -F	¬¬¬	CHAN17MSIG
J81 18A	J104 -J	¬¬¬	CH17XMTVFINT
J81 19A	J104 -K	¬¬¬	CH17XMTVFINR
J81 2A	REFER TO NETWORK	J25	11A
J81 20A	J104 -L	¬¬¬	C17RCVVFOUTT
J81 20B	J104 -M	¬¬¬	C17RCVVFOUTR
J81 22A	REFER TO NETWORK	J45	12A
J81 22B	REFER TO NETWORK	J45	12A
J81 3A	REFER TO NETWORK	J1	10B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J81 3B	REFER TO NETWORK	J1	10B
J81 5A	REFER TO NETWORK	J35	7A
J81 6A	REFER TO NETWORK	J1	6A
J81 6B	REFER TO NETWORK	J1	6A
J81 7A	REFER TO NETWORK	J1	3A
J81 7B	REFER TO NETWORK	J1	3A
J81 8A	REFER TO NETWORK	J20	3A
J81 9A	REFER TO NETWORK	J27	10A
J82 1A	J135 5	¬¬¬	CH17SIG1(+)
J82 1B	J135 6	¬¬¬	CH17SIG1(-)
J82 10A	REFER TO NETWORK	J5	10A
J82 10B	REFER TO NETWORK	J3	12B
J82 11A	REFER TO NETWORK	J33	10B
J82 11B	REFER TO NETWORK	J3	15B
J82 12A	REFER TO NETWORK	J9	10B
J82 12B	REFER TO NETWORK	J9	14B
J82 13A	REFER TO NETWORK	J33	3B
J82 13B	REFER TO NETWORK	J3	14B
J82 14A	REFER TO NETWORK	J1	7B
J82 14B	REFER TO NETWORK	J1	7B
J82 15A	J135 24	¬¬¬	CH17XMTCLKIN(
J82 15B	J135 23	¬¬¬	CH17XMTCLKIN(
J82 16A	J135 15	¬¬¬	CH17XMTCLKOT(
J82 16B	J135 16	¬¬¬	CH17XMTCLKOT(
J82 17A	J135 17	¬¬¬	CH17RCVCLK(+)
J82 17B	J135 18	¬¬¬	CH17RCVCLK(-)
J82 18A	J135 2	¬¬¬	CH17XMTDATA(+
J82 18B	REFER TO NETWORK	J1	8B
J82 19A	J135 14	¬¬¬	CH17XMTDATA(-
J82 19B	REFER TO NETWORK	J3	11A
J82 2A	J135 8	¬¬¬	CH17SIG2(+)
J82 2B	J135 9	¬¬¬	CH17SIG2(-)
J82 20A	J135 3	¬¬¬	CH17RCVDATA(+
J82 20B	J135 19	¬¬¬	CH17RCVDATA(-
J82 21A	J135 12	¬¬¬	CH17SIG4(+)
J82 21B	J135 13	¬¬¬	CH17SIG4(-)
J82 3A	J135 10	¬¬¬	CH17SIG3(+)
J82 3B	J135 11	¬¬¬	CH17SIG3(-)

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J82 4A	REFER TO NETWORK	J31 7A	
J82 4B	REFER TO NETWORK	J31 7A	
J82 5B	REFER TO NETWORK	J9 11B	
J82 6A	REFER TO NETWORK	J1 6A	
J82 6B	REFER TO NETWORK	J1 6A	
J82 7A	REFER TO NETWORK	J1 3A	
J82 7B	REFER TO NETWORK	J1 3A	
J82 8A	REFER TO NETWORK	J20 2A	
J82 8B	REFER TO NETWORK	J31 3A	
J82 9A	REFER TO NETWORK	J27 10A	
J83 1A	REFER TO NETWORK	J35 14B	
J83 1B	REFER TO NETWORK	J25 10B	
J83 10A	REFER TO NETWORK	J1 12B	
J83 11A	REFER TO NETWORK	J33 10A	
J83 12A	REFER TO NETWORK	J9 22A	
J83 13A	REFER TO NETWORK	J11 13A	
J83 14B	REFER TO NETWORK	J20 8A	
J83 15A	REFER TO NETWORK	J20 19A	
J83 16A	J119 -G	¬¬¬	CHAN18ESIG
J83 17A	J118 -G	¬¬¬	CHAN18MSIG
J83 18A	J104 -E	¬¬¬	CH18XMTVFINT
J83 19A	J104 -F	¬¬¬	CH18XMTVFINR
J83 2A	REFER TO NETWORK	J25 10A	
J83 20A	J104 -G	¬¬¬	C18RCVVFOUTT
J83 20B	J104 -H	¬¬¬	C18RCVVFOUTR
J83 22A	REFER TO NETWORK	J45 12A	
J83 22B	REFER TO NETWORK	J45 121	
J83 3A	REFER TO NETWORK	J1 10B	
J83 3B	REFER TO NETWORK	J1 10B	
J83 5A	REFER TO NETWORK	J35 14A	
J83 6A	REFER TO NETWORK	J1 6A	
J83 6B	REFER TO NETWORK	J1 6A	
J83 7A	REFER TO NETWORK	J1 3A	
J83 7B	REFER TO NETWORK	J1 3A	
J83 8A	REFER TO NETWORK	J20 3A	
J83 9A	REFER TO NETWORK	J27 8B	
J85 1A	REFER TO NETWORK	J11 19B	
J85 1B	REFER TO NETWORK	J25 8B	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J85 10A	REFER TO NETWORK	J1	12B
J85 11A	REFER TO NETWORK	J33	11B
J85 12A	REFER TO NETWORK	J9	22A
J85 13A	REFER TO NETWORK	J11	13A
J85 14B	REFER TO NETWORK	J20	8A
J85 15A	REFER TO NETWORK	J20	19A
J85 16A	J119 -H	¬¬¬	CHAN19ESIG
J85 17A	J118 -H	¬¬¬	CHAN19MSIG
J85 18A	J107 -A	¬¬¬	CH19XMTVFINT
J85 19A	J107 -8	¬¬¬	CH19XMTVFINR
J85 2A	REFER TO NETWORK	J25	8A
J85 20A	J107 -C	¬¬¬	C19RCVVFOUTT
J85 20B	J107 -D	¬¬¬	C19RCVVFOUTR
J85 22A	REFER TO NETWORK	J45	12A
J85 22B	REFER TO NETWORK	J45	12A
J85 3A	REFER TO NETWORK	J1	10B
J85 3B	REFER TO NETWORK	J1	10B
J85 5A	REFER TO NETWORK	J11	19A
J85 6A	REFER TO NETWORK	J1	6A
J85 6B	REFER TO NETWORK	J1	6A
J85 7A	REFER TO NETWORK	J1	3A
J85 7B	REFER TO NETWORK	J1	3A
J85 8A	REFER TO NETWORK	J20	3A
J85 9A	REFER TO NETWORK	J27	12A
J86 1A	J134 5	¬¬¬	CH19SIG1(+)
J86 1B	J134 6	¬¬¬	CH19SIG1(-)
J86 10A	REFER TO NETWORK	J5	10A
J86 10B	REFER TO NETWORK	J3	12B
J86 11A	REFER TO NETWORK	J33	11B
J86 11B	REFER TO NETWORK	J3	15B
J86 12A	REFER TO NETWORK	J9	10B
J86 12B	REFER TO NETWORK	J9	14B
J86 13A	REFER TO NETWORK	J33	3B
J86 13B	REFER TO NETWORK	J3	14B
J86 14A	REFER TO NETWORK	J1	7B
J86 14B	REFER TO NETWORK	J1	7B
J86 15A	J134 24	¬¬¬	CH19XMTCLKIN(
J86 15B	J134 23	¬¬¬	CH19XMTCLKIN(

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J86 16A	J134 15	¬¬¬	CH19XMTCLKOT(
J86 16B	J134 16	¬¬¬	CH19XMTCLKOT(
J86 17A	J134 17	¬¬¬	CH19RCVCLK(+)
J86 17B	J134 18	¬¬¬	CH19RCVCLK(-)
J86 18A	J134 2	¬¬¬	CH19XMTDATA(+
J86 18B	REFER TO NETWORK	J1	8B
J86 19A	J134 14	¬¬¬	CH19XMTDATA(-
J86 19B	REFER TO NETWORK	J3	11A
J86 2A	J134 8	¬¬¬	CH19SIG2(+)
J86 2B	J134 9	¬¬¬	CH19SIG2(-)
J86 20A	J134 3	¬¬¬	CH19RCVDATA(+
J86 20B	J134 19	¬¬¬	CH19RCVDATA(-
J86 21A	J134 12	¬¬¬	CH19SIG4(+)
J86 21B	J134 13	¬¬¬	CH19SIG4(-)
J86 3A	J134 10	¬¬¬	CH19SIG3(+)
J86 3B	J134 11	¬¬¬	CH19SIG3(-)
J86 4A	REFER TO NETWORK	J20	20B
J86 4B	REFER TO NETWORK	J20	20B
J86 5B	REFER TO NETWORK	J9	11B
J86 6A	REFER TO NETWORK	J1	6A
J86 6B	REFER TO NETWORK	J1	6A
J86 7A	REFER TO NETWORK	J1	3A
J86 7B	REFER TO NETWORK	J1	34
J86 8A	REFER TO NETWORK	J20	2A
J86 8B	REFER TO NETWORK	J31	3A
J86 9A	REFER TO NETWORK	J27	12A
J87 1A	REFER TO NETWORK	J35	4B
J87 1B	REFER TO NETWORK	J25	9B
J87 10A	REFER TO NETWORK	J1	12B
J87 11A	REFER TO NETWORK	J33	11A
J87 12A	REFER TO NETWORK	J4	22A
J87 13A	REFER TO NETWORK	J11	13A
J87 14B	REFER TO NETWORK	J20	8A
J87 15A	REFER TO NETWORK	J20	19A
J87 16A	J119 -Z	¬¬¬	CHAN20ESIG
J87 17A	J118 -Z	¬¬¬	CHAN20MSIG
J87 18A	J107 -J	¬¬¬	CH20XMTVFINT
J87 19A	J107 -K	¬¬¬	CH20XMTVFINR

Table B-1. Rear Assembly Wire Connection List - Continued

FROM		TO		REF. DESG.	SIGNAL NAME	
J87	2A		REFER TO NETWORK		J25	QA
J87	20A	J107	-L	¬¬¬	C20RCVVFOUTT	
J87	20B	J107	-M	¬¬¬	C20RCVVFOUTR	
J87	22A		REFER TO NETWORK		J45	12A
J87	22B		REFER TO NETWORK		J45	12A
J87	3A		REFER TO NETWORK		J1	10B
J87	3B		REFER TO NETWORK		J1	10B
J87	5A		REFER TO NETWORK		J35	4A
J87	6A		REFER TO NETWORK		J1	6A
J87	6B		REFER TO NETWORK		J1	6A
J87	7A		REFER TO NETWORK		J1	3A
J87	7B		REFER TO NETWORK		J1	3A
J87	8A		REFER TO NETWORK		J20	3A
J87	9A		REFER TO NETWORK		J27	13A
J89	1A		REFER TO NETWORK		J35	8B
J89	1B		REFER TO NETWORK		J25	13B
J89	10A		REFER TO NETWORK		J1	12B
J89	11A		REFER TO NETWORK		J33	5A
J89	12A		REFER TO NETWORK		J9	22A
J89	13A		REFER TO NETWORK		J11	13A
J89	14B		REFER TO NETWORK		J20	8A
J89	15A		REFER TO NETWORK		J20	19A
J89	16A	J119	-AA	¬¬¬	CHAN21ESIG	
J89	17A	J118	-AA	¬¬¬	CHAN21MSIG	
J89	18A	J107	-E	¬¬¬	CH21XMTVFTNT	
J89	19A	J107	-F	¬¬¬	CH21XMTVFINR	
J89	2A		REFER TO NETWORK		J25	13A
J89	20A	J107	-G	¬¬¬	C21RCVVFOUTT	
J89	20B	J107	-H	¬¬¬	C21RCVVFOUTR	
J89	22A		REFER TO NETWORK		J45	12A
J89	22B		REFER TO NETWORK		J45	12A
J89	3A		REFER TO NETWORK		J1	10B
J89	3B		REFER TO NETWORK		J1	10B
J89	5A		REFER TO NETWORK		J35	8A
J89	6A		REFER TO NETWORK		J1	6A
J89	6B		REFER TO NETWORK		J1	6A
J89	7A		REFER TO NETWORK		J1	3A
J89	7B		REFER TO NETWORK		J1	3A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J89 8A	REFER TO NETWORK	J20 3A	
J89 9A	REFER TO NETWORK	J27 9B	
J90 1A	J133 5	¬¬¬	CH21SIG1(+)
J90 1B	J133 6	¬¬¬	CH21SIG1(-)
J90 10A	REFER TO NETWORK	J5 10A	
J90 10B	REFER TO NETWORK	J3 12B	
J90 11A	REFER TO NETWORK	J33 5A	
J90 11B	REFER TO NETWORK	J3 15B	
J90 12A	REFER TO NETWORK	J9 10B	
J90 12B	REFER TO NETWORK	J9 14B	
J90 13A	REFER TO NETWORK	J33 3B	
J90 13B	REFER TO NETWORK	J3 14B	
J90 14A	REFER TO NETWORK	J1 7B	
J90 14B	REFER TO NETWORK	J1 7B	
J90 15A	J133 24	¬¬¬	CH21XMTCLKIN(
J90 15B	J133 23	¬¬¬	CH21XMTCLKIN(
J90 16A	J133 15	¬¬¬	CH21XMTCLKOT(
J90 16B	J133 16	¬¬¬	CH21XMTCLKOT(
J90 17A	J133 17	¬¬¬	CH21RCVCLK(+)
J90 17B	J133 18	¬¬¬	CH21RCVCLK(-)
J90 18A	J133 2	¬¬¬	CH21XMTDATA(+
J90 18B	REFER TO NETWORK	J1 8B	
J90 14A	J133 14	¬¬¬	CH21XMTDATA(-
J90 19B	REFER TO NETWORK	J3 11A	
J90 2A	J133 8	¬¬¬	CH21SIG2(+)
J90 2B	J133 9	¬¬¬	CH21SIG2(-)
J90 20A	J133 3	¬¬¬	CH21RCVDATA(+
J90 20B	J133 19	¬¬¬	CH21RCVDATA(-
J90 21A	J133 12	¬¬¬	CH21SIG4(+)
J90 21B	J133 13	¬¬¬	CH21SIG4(-)
J90 3A	J133 10	¬¬¬	CH21SIG3(+)
J90 3B	J133 11	¬¬¬	CH21SIG3(-)
J90 4A	REFER TO NETWORK	J20 20B	
J90 4B	REFER TO NETWORK	J20 20B	
J90 5B	REFER TO NETWORK	J9 118	
J90 6A	REFER TO NETWORK	J1 6A	
J90 6B	REFER TO NETWORK	J1 6A	
J90 7A	REFER TO NETWORK	J1 3A	

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J90 7B	REFER TO NETWORK	J1	3A
J90 8A	REFER TO NETWORK	J20	2A
J90 8B	REFER TO NETWORK	J31	3A
J90 9A	REFER TO NETWORK	J27	9B
J91 1A	REFER TO NETWORK	J11	15B
J91 1B	REFER TO NETWORK	J25	12B
J91 10A	REFER TO NETWORK	J1	12B
J91 11A	REFER TO NETWORK	J33	5B
J91 12A	REFER TO NETWORK	J9	22A
J91 13A	REFER TO NETWORK	J11	13A
J91 14B	REFER TO NETWORK	J20	8A
J91 15A	REFER TO NETWORK	J20	19A
J91 16A	J119 -K	¬¬¬	CHAN22ESIG
J91 17A	J118 -K	¬¬¬	CHAN22MSIG
J91 18A	J106 -A	¬¬¬	CH22XMTVFINT
J91 19A	J106 -B	¬¬¬	CH22XMTVFINR
J91 2A	REFER TO NETWORK	J25	12A
J91 20A	J106 -C	¬¬¬	C22RCVVFOUTT
J91 20B	J106 -D	¬¬¬	C22RCVVFOUTR

FROM	TO	REF. DESG.	SIGNAL NAME
J91 22A	REFER TO NETWORK	J45	12A
J91 22B	REFER TO NETWORK	J45	12A
J91 3A	REFER TO NETWORK	J1	10B
J91 3B	REFER TO NETWORK	J1	10B
J91 5A	REFER TO NETWORK	J11	15A
J91 6A	REFER TO NETWORK	J1	6A
J91 6B	REFER TO NETWORK	J1	6A
J91 7A	REFER TO NETWORK	J1	3A
J91 7B	REFER TO NETWORK	J1	3A
J91 7A	REFER TO NETWORK	J20	3A
J91 9A	REFER TO NETWORK	J27	15A
J93 1A	REFER TO NETWORK	J35	2B
J93 1B	REFER TO NETWORK	J25	14B
J93 10A	REFER TO NETWORK	J1	12B
J93 11A	REFER TO NETWORK	J33	4A
J93 12A	REFER TO NETWORK	J9	22A
J93 13A	REFER TO NETWORK	J11	13A
J93 14B	REFER TO NETWORK	J20	8A
J93 15A	REFER TO NETWORK	J20	19A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J93 16A	J119 -L	¬¬¬	CHAN23ESIG
J93 17A	J116 -L	¬¬¬	CHAN23MSIG
J93 18A	J106 -J	¬¬¬	CH23XMTVFINT
J93 19A	J106 -K	¬¬¬	CH23XMTVFINR
J93 2A	REFER TO NETWORK	J25	14A
J93 20A	J106 -L	¬¬¬	C23RCVVFOJTT
J93 20B	J106 -M	¬¬¬	C23RCVVFOUTP
J93 22A	REFER TO NETWORK	J45	12A
J93 22B	REFER TO NETWORK	J45	12A
J93 3A	REFER TO NETWORK	J1	10B
J93 3B	REFER TO NETWORK	J1	10B
J93 5A	REFER TO NETWORK	J35	2A
J93 6A	REFER TO NETWORK	J1	6A
J93 6B	REFER TO NETWORK	J1	6A
J93 7A	REFER TO NETWORK	J1	3A
J93 7B	REFER TO NETWORK	J1	3A
J93 8A	REFER TO NETWORK	J20	3A
J93 9A	REFER TO NETWORK	J27	7B
J94 1A	J132 5	¬¬¬	CH23SIG1(+)
J94 1H	J132 6	¬¬¬	CH23STG1(-)
J94 10A	REFER TO NETWORK	J5	10A
J94 10B	REFER TO NETWORK	J3	12B
J94 11A	REFER TO NETWORK	J33	4A
J94 11B	REFER TO NETWORK	J3	15B
J94 12A	REFER TO NETWORK	J9	10B
J94 12B	REFER TO NETWORK	J9	14B
J94 13A	REFER TO NETWORK	J33	3B
J94 13B	REFER TO NETWORK	J3	14B
J54 14A	REFER TO NETWORK	J1	7B
J94 14B	REFER TO NETWORK	J1	7B
J94 15A	J132 24	¬¬¬	CH23XMTCLKIN(
J94 15B	J132 23	¬¬¬	CH23XMTCLKIN(
J94 16A	J132 15	¬¬¬	CH23XMTCLKOT(
J94 16B	J132 16	¬¬¬	CH23XMTCLKOT(
J94 17A	J132 17	¬¬¬	CH23RCVCLK(+)
J94 17B	J132 18	¬¬¬	CH23RCVCLK(-)
J94 18A	J132 2	¬¬¬	CH23XMTDATA(+
J94 18B	REFER TO NETWORK	J1	8B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J94 19A	J132 14	¬¬¬	CH23XMTDA TA(-
J94 19B	REFER TO NETWORK	J3	11A
J94 2A	J132 8	¬¬¬	CH23SIG2(+)
J94 2B	J132 9	¬¬¬	CH23SIG2(-)
J94 20A	J132 3	¬¬¬	CH23RCVDATA(+
J94 20B	J132 19	¬¬¬	CH23RCVDATA(-
J94 21A	J132 12	¬¬¬	CH23SIG4(+)
J94 21B	J132 13	¬¬¬	CH23SIG4(-)
J94 3A	J132 10	¬¬¬	CH23SIG3(+)
J94 3B	J132 11	¬¬¬	CH23SIG3(-)
J94 4A	REFER TO NETWORK	J20	20B
J94 4B	REFER TO NETWORK	J20	20B
J94 5B	REFER TO NETWORK	J9	11B
J94 6A	REFER TO NETWORK	J1	6A
J94 6B	REFER TO NETWORK	J1	6A
J94 7A	REFER TO NETWORK	J1	3A
J94 7B	REFER TO NETWORK	J1	3A
J94 8A	REFER TO NETWORK	J20	2A
J94 8B	REFER TO NETWORK	J31	3A
J94 9A	REFER TO NETWORK	J27	7B
J95 1A	REFER TO NETWORK	J11	16B
J95 1B	REFER TO NETWORK	J25	15B
J95 10A	REFER TO NETWORK	J1	12B
J95 11A	REFER TO NETWORK	J33	4B
J95 12A	REFER TO NETWORK	J9	22A
J95 13A	REFER TO NETWORK	J11	13A
J95 14B	REFER TO NETWORK	J20	8A
J95 15A	REFER TO NETWORK	J20	19A
J95 16A	J119 -M	¬¬¬	CHAN24ESIG
J95 17A	J118 -m	¬¬¬	CHAN24MSIG
J95 18A	J106 -E	¬¬¬	CH24XMTVFINT
J95 14A	J106 -F	¬¬¬	CH24XMTVFINR
J95 2A	REFER TO NETWORK	J25	15A
J95 20A	J106 -G	¬¬¬	C24RCVVFOUTT
J95 20B	J106 -H	¬¬¬	C24RCVVFOUTR
J95 22A	REFER TO NETWORK	J45	12A
J95 22B	REFER TO NETWORK	J45	12A
J95 3A	REFER TO NETWORK	J1	10B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J95 3B	REFER TO NETWORK	J1	10B
J95 5A	REFER TO NETWORK	J35	11A
J95 6A	REFER TO NETWORK	J1	6A
J95 6B	REFER TO NETWORK	J1	6A
J95 7A	REFER TO NETWORK	J1	3A
J95 7B	REFER TO NETWORK	J1	3A
J95 8A	REFER TO NETWORK	J20	3A
J95 9A	REFER TO NETWORK	J27	14A
J100 -A	REFER TO NETWORK	J55	18A
J100 -B	REFER TO NETWORK	J55	19A
J100 -C	REFER TO NETWORK	J55	20A
J100 -D	REFER TO NETWORK	J55	20B
J100 -E	REFER TO NETWORK	J59	18A
J100 -F	REFER TO NETWORK	J59	19A
J100 -G	REFER TO NETWORK	J59	20A
J100 -H	REFER TO NETWORK	J59	20B
J100 -J	REFER TO NETWORK	J57	18A
J100 -K	REFER TO NETWORK	J57	19A
J100 -L	REFER TO NETWORK	J57	20A
J100 -M	REFER TO NETWORK	J57	20B
J100 -U	REFER TO NETWORK	E	1-2
J101 -A	REFER TO NETWORK	J49	18A
J101 -B	REFER TO NETWORK	J49	19A
J101 -C	REFER TO NETWORK	J49	20A
J101 -D	REFER TO NETWORK	J49	20B
J101 -E	REFER TO NETWORK	J53	18A
J101 -F	REFER TO NETWORK	J53	19A
J101 -G	REFER TO NETWORK	J53	20A
J101 -H	REFER TO NETWORK	J53	20B
J101 -J	REFER TO NETWORK	J51	18A
J101 -K	REFER TO NETWORK	J51	19A
J101 -L	REFER TO NETWORK	J51	20A
J101 -M	REFER TO NETWORK	J51	20B
J101 -U	REFER TO NETWORK	E	1-2
J102 -A	REFER TO NETWORK	J67	18A
J102 -B	REFER TO NETWORK	J67	19A
J102 -C	REFER TO NETWORK	J67	20A
J102 -D	REFER TO NETWORK	J67	20B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J102 -E	REFER TO NETWORK	J71	18A
J102 -F	REFER TO NETWORK	J71	19A
J102 -G	REFER TO NETWORK	J71	20A
J102 -H	REFER TO NETWORK	J71	20B
J102 -J	REFER TO NETWORK	J69	18A
J102 -K	REFER TO NETWORK	J69	19A
J102 -L	REFER TO NETWORK	J69	20A
J102 -M	REFER TO NETWORK	J69	20B
J102 -U	REFER TO NETWORK	E	1-2
J103 -A	REFER TO NETWORK	J1	18A
J103 -B	REFER TO NETWORK	J61	19A
J103 -C	REFER TO NETWORK	J61	20A
J103 -D	REFER TO NETWORK	J61	20B
J103 -E	REFER TO NETWORK	J65	18A
J103 -F	REFER TO NETWORK	J65	19A
J103 -G	REFER TO NETWORK	J65	20A
J103 -H	REFER TO NETWORK	J65	20B
J103 -J	REFER TO NETWORK	J63	18A
J103 -K	REFER TO NETWORK	J63	19A
J103 -L	REFER TO NETWORK	J63	20A
J103 -M	REFER TO NETWORK	J63	20B
J103 -U	REFER TO NETWORK	E	1-2
J104 -A	REFER TO NETWORK	J79	18A
J104 -B	REFER TO NETWORK	J79	19A
J104 -C	REFER TO NETWORK	J79	20A
J104 -D	REFER TO NETWORK	J79	20B
J104 -E	REFER TO NETWORK	J83	18A
J104 -F	REFER TO NETWORK	J83	19A
J104 -G	REFER TO NETWORK	J83	20A
J104 -H	REFER TO NETWORK	J83	20B
J104 -J	REFER TO NETWORK	J81	18A
J104 -K	REFER TO NETWORK	J81	19A
J104 -L	REFER TO NETWORK	J81	20A
J104 -M	REFER TO NETWORK	J81	20B
J104 -U	REFER TO NETWORK	E	1-2
J105 -A	REFER TO NETWORK	J73	18A
J105 -B	REFER TO NETWORK	J73	19A
J105 -C	REFER TO NETWORK	J73	20A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J105 -D	REFER TO NETWORK	J73	20B
J105 -E	REFER TO NETWORK	J77	18A
J105 -F	REFER TO NETWORK	J77	19A
J105 -G	REFER TO NETWORK	J77	20A
J105 -H	REFER TO NETWORK	J77	20B
J105 -J	REFER TO NETWORK	J75	18A
J105 -K	REFER TO NETWORK	J75	19A
J105 -L	REFER TO NETWORK	J75	20A
J105 -M	REFER TO NETWORK	J75	20B
J105 -U	REFER TO NETWORK	E	1-2
J106 -A	REFER TO NETWORK	J91	18A
J106 -B	REFER TO NETWORK	J91	19A
J106 -C	REFER TO NETWORK	J91	20A
J106 -D	REFER TO NETWORK	J91	20B
J106 -E	REFER TO NETWORK	J95	18A
J106 -F	REFER TO NETWORK	J95	19A
J106 -G	REFER TO NETWORK	J95	20A
J106 -H	REFER TO NETWORK	J95	20B
J106 -J	REFER TO NETWORK	J93	18A
J106 -K	REFER TO NETWORK	J93	19A
J106 -L	REFER TO NETWORK	J93	20A
J106 -M	REFER TO NETWORK	J93	20B
J106 -U	REFER TO NETWORK	E	1-2
J107 -A	REFER TO NETWORK	J85	18A
J107 -B	REFER TO NETWORK	J85	19A
J107 -C	REFER TO NETWORK	J85	20A
J107 -D	REFER TO NETWORK	J85	20B
J107 -E	REFER TO NETWORK	J89	18A
J107 -F	REFER TO NETWORK	J89	19A
J107 -G	REFER TO NETWORK	J89	20A
J107 -H	REFER TO NETWORK	J89	20B
J107 -J	REFER TO NETWORK	J87	18A
J107 -K	REFER TO NETWORK	J87	19A
J107 -L	REFER TO NETWORK	J87	20A
J107 -M	REFER TO NETWORK	J87	20B
J107 -U	REFER TO NETWORK	E	1-2
J108 +SKT	REFER TO NETWORK	J29	1A
J108 -PIN	REFER TO NETWORK	J29	1B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J109 +SKT	REFER TO NETWORK	J7	15A
J109 -PIN	REFER TO NETWORK	J7	15B
J110 +SKT	REFER TO NETWORK	J5	20B
J110 -PIN	REFER TO NETWORK	J5	20A
J110 +SKT	REFER TO NETWORK	J7	9A
J110 -PIN	REFER TO NETWORK	J7	10A
J112 +SKT	REFER TO NETWORK	J5	19B
J112 -PIN	REFER TO NETWORK	J5	19A
J113 +SKT	REFER TO NETWORK	J7	11A
J113 -PIN	REFER TO NETWORK	J7	12A
J114 +SKT	REFER TO NETWORK	J5	22B
J114 -PIN	REFER TO NETWORK	J5	22A
J115 +SKT	REFER TO NETWORK	J31	1B
J116 1	REFER TO NETWORK	J20	9A
J116 10	REFER TO NETWORK	J44	7B
J116 11	REFER TO NETWORK	J44	8B
J116 12	REFER TO NETWORK	J44	9B
J116 13	REFER TO NETWORK	J44	10A
J116 14	REFER TO NETWORK	J44	11A
J116 15	REFER TO NETWORK	J44	12A
J116 16	REFER TO NETWORK	J44	10B
J116 17	REFER TO NETWORK	J44	11B
J116 18	REFER TO NETWORK	J44	12B
J116 19	REFER TO NETWORK	E	1-2
J116 2	REFER TO NETWORK	J20	10A
J116 20	REFER TO NETWORK	J44	13A
J116 21	REFER TO NETWORK	J44	14A
J116 22	REFER TO NETWORK	J44	15A
J116 23	REFER TO NETWORK	J44	13B
J116 24	REFER TO NETWORK	J44	14B
J116 25	REFER TO NETWORK	J44	15B
J116 3	REFER TO NETWORK	J20	11A
J116 4	REFER TO NETWORK	J20	11B
J116 5	REFER TO NETWORK	J20	12B
J116 6	REFER TO NETWORK	J20	13B
J116 7	REFER TO NETWORK	J44	7A
J116 8	REFER TO NETWORK	J44	8A
J116 9	REFER TO NETWORK	J44	9A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J117 -A	REFER TO NETWORK	J31	2B
J 117 -B	REFER TO NETWORK	J31	4B
J117 -C	REFER TO NETWORK	J1	6A
J118 -A	REFER TO NETWORK	J55	17A
J118 -AA	REFER TO NETWORK	J89	17A
J118 -B	REFER TO NETWORK.	J51	17A
J118 -C	REFER TO NETWORK	J49	17A
J118 -CC	REFER TO NETWORK	J75	17A
J118 -D	REFER TO NETWORK	J67	17A
J118 -DD	REFER TO NETWORK	J73	17A
J118 -E	REFER TO NETWORK	J65	17A
J118 -EE	REFER TO NETWORK	J59	17A
J118 -F	REFER TO NETWORK	J81	17A
J118 -G	REFER TO NETWORK	J83	17A
J118 -H	REFER TO NETWORK	J85	17A
J118 -J	REFER TO NETWORK	E	1-2
J118 K	REFER TO NETWORK	J91	17A
J118 -L	REFER TO NETWORK	J93	17A
J118 -M	REFER TO NETWORK	J95	17A
J118 -N	REFER TO NETWORK	J79	17A
J118 -P	REFER TO NETWORK	J77	17A
J118 -R	REFER TO NETWORK	J63	17A
J118 -S	REFER TO NETWORK	J61	17A
J118 -T	REFER TO NETWORK	J57	17A
J118 -V	REFER TO NETWORK	J53	17A
J118 -W	REFER TO NETWORK	J71	17A
J118 -X	REFER TO NETWORK	J69	17A
J118 -Z	REFER TO NETWORK	J87	17A
J119 -A	REFER TO NETWORK	J55	16A
J119 -AA	REFER TO NETWORK	J89	16A
J119 -B	REFER TO NETWORK	J51	16A
J119 -BB	REFER TO NETWORK	J1	6A
J119 -C	REFER TO NETWORK	J49	16A
J119 -CC	REFER TO NETWORK	J75	16A
J119 -D	REFER TO NETWORK	J67	16A
J119 -DD	REFER TO NETWORK	J73	16A
J119 -E	REFER TO NETWORK	J65	16A
J119 -EE	REFER TO NETWORK	J59	16A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J119 -F	REFER TO NETWORK	J81	16A
J119 -G	REFER TO NETWORK	J83	16A
J119 -H	REFER TO NETWORK	J85	16A
J119 -J	REFER TO NETWORK	E	1-2
J119 -K	REFER TO NETWORK	J91	16A
J119 -L	REFER TO NETWORK	J93	16A
J119 -M	REFER TO NETWORK	J95	16A
J119 -N	REFER TO NETWORK	J79	16A
J119 -P	REFER TO NETWORK	J77	16A
J119 -R	REFER TO NETWORK	J63	16A
J119 -S	REFER TO NETWORK	J61	16A
J119 -T	REFER TO NETWORK	J57	16A
J119 -V	REFER TO NETWORK	J53	16A
J119 -W	REFER TO NETWORK	J71	16A
J119 -X	REFER TO NETWORK	J69	16A
J119 -Y	REFER TO NETWORK	J20	20A
J119 -Z	REFER TO NETWORK	J87	16A
J120 1	REFER TO NETWORK	E	1-2
J120 10	REFER TO NETWORK	J72	3A
J120 11	REFER TO NETWORK	J72	3B
J120 12	REFER TO NETWORK	J72	21A
J120 13	REFER TO NETWORK	J72	21B
J120 14	REFER TO NETWORK	J72	19A
J120 15	REFER TO NETWORK	J72	16A
J120 16	REFER TO NETWORK	J72	16B
J120 17	REFER TO NETWORK	J72	17A
J120 18	REFER TO NETWORK	J72	17B
J120 19	REFER TO NETWORK	J72	20A
J120 2	REFER TO NETWORK	J72	18A
J120 23	REFER TO NETWORK	J72	15B
J120 24	REFER TO NETWORK	J72	15A
J120 3	REFER TO NETWORK	J72	20A
J120 5	REFER TO NETWORK	J72	1A
J120 6	REFER TO NETWORK	J72	1B
J120 7	REFER TO NETWORK	J1	6A
J120 8	REFER TO NETWORK	J72	2A
J120 9	REFER TO NETWORK	J72	2B
J121 1	REFER TO NETWORK	E	1-2

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J121 10	REFER TO NETWORK	J70	3A
J121 11	REFER TO NETWORK	J70	3B
J121 12	REFER TO NETWORK	J70	21A
J121 13	REFER TO NETWORK	J70	21B
J121 14	REFER TO NETWORK	J70	19A
J121 15	REFER TO NETWORK	J70	16A
J121 16	REFER TO NETWORK	J70	16B
J121 17	REFER TO NETWORK	J70	17A
J121 18	REFER TO NETWORK	J70	17B
J121 19	REFER TO NETWORK	J70	20B
J121 2	REFER TO NETWORK	J70	18A
J121 23	REFER TO NETWORK	J70	15B
J121 24	REFER TO NETWORK	J70	15A
J121 3	REFER TO NETWORK	J70	20A
J121 5	REFER TO NETWORK	J70	1A
J121 6	REFER TO NETWORK	J70	1B
J121 7	REFER TO NETWORK	J1	6A
J121 8	REFER TO NETWORK	J70	2A
J121 9	REFER TO NETWORK	J70	2B
J122 1	REFER TO NETWORK	E	1-2
J122 10	REFER TO NETWORK	J68	3A
J122 11	REFER TO NETWORK	J68	3B
J122 12	REFER TO NETWORK	J68	21A
J122 13	REFER TO NETWORK	J68	21B
J122 14	REFER TO NETWORK	J68	19A
J122 15	REFER TO NETWORK	J68	16A
J122 16	REFER TO NETWORK	J68	16B
J122 17	REFER TO NETWORK	J68	17A
J122 18	REFER TO NETWORK	J68	17B
J122 19	REFER TO NETWORK	J68	20B
J122 2	REFER TO NETWORK	J68	18A
J122 23	REFER TO NETWORK	J68	15B
J122 24	REFER TO NETWORK	J68	15A
J122 3	REFER TO NETWORK	J68	20A
J122 5	REFER TO NETWORK	J68	1A
J122 6	REFER TO NETWORK	J68	1B
J122 7	REFER TO NETWORK	J1	6A
J122 8	REFER TO NETWORK	J68	2A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J122 9	REFER TO NETWORK	J68	2B
J123 1	REFER TO NETWORK	E	1-2
J123 10	REFER TO NETWORK	J66	3A
J123 11	REFER TO NETWORK	J66	3B
J123 12	REFER TO NETWORK	J66	21A
J123 13	REFER TO NETWORK	J66	21B
J123 14	REFER TO NETWORK	J66	19A
J123 15	REFER TO NETWORK	J66	16A
J123 16	REFER TO NETWORK	J66	16B
J123 17	REFER TO NETWORK	J66	17A
J123 18	REFER TO NETWORK	J66	17B
J123 19	REFER TO NETWORK	J66	20B
J123 2	REFER TO NETWORK	J66	18A
J123 23	REFER TO NETWORK	J66	15B
J123 24	REFER TO NETWORK	J66	15A
J123 3	REFER TO NETWORK	J66	20A
J123 5	REFER TO NETWORK	J66	1A
J123 6	REFER TO NETWORK	J66	1B
J123 7	REFER TO NETWORK	J1	6A
J123 8	REFER TO NETWORK	J66	2A
J123 9	REFER TO NETWORK	J66	2B
J124 1	REFER TO NETWORK	E	1-2
J124 10	REFER TO NETWORK	J64	3A
J124 11	REFER TO NETWORK	J64	3B
J124 12	REFER TO NETWORK	J64	21A
J124 13	REFER TO NETWORK	J64	21B
J124 14	REFER TO NETWORK	J64	19A
J124 15	REFER TO NETWORK	J64	16A
J124 16	REFER TO NETWORK	J64	16B
J124 17	REFER TO NETWORK	J64	17A
J124 18	REFER TO NETWORK	J64	17A
J124 19	REFER TO NETWORK	J64	20B
J124 2	REFER TO NETWORK	J64	18A
J124 23	REFER TO NETWORK R	J64	15B
J124 24	REFER TO NETWORK	J64	15A
J124 3	REFER TO NETWORK	J64	20A
J124 5	REFER TO NETWORK	J64	1A
J124 6	REFER TO NETWORK	J64	1B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J124 7	REFER TO NETWORK	J1	6A
J124 8	REFER TO NETWORK	J64	2A
J124 9	REFER TO NETWORK	J64	2B
J125 1	REFER TO NETWORK	E	1-2
J125 10	REFER TO NETWORK	J62	3A
J125 11	REFER TO NETWORK	J62	3B
J125 12	REFER TO NETWORK	J62	21A
J125 13	REFER TO NETWORK	J62	21B
J125 14	REFER TO NETWORK	J62	19A
J125 15	REFER TO NETWORK	J62	16A
J125 16	REFER TO NETWORK	J62	16B
J125 17	REFER TO NETWORK	J62	17A
J125 18	REFER TO NETWORK	J62	17B
J125 19	REFER TO NETWORK	J62	20B
J125 2	REFER TO NETWORK	J62	18A
J125 23	REFER TO NETWORK	J62	15B
J125 24	REFER TO NETWORK	J62	15A
J125 3	REFER TO NETWORK	J62	20A
J125 5	REFER TO NETWORK	J62	1A
J125 6	REFER TO NETWORK	J62	1B
J125 7	REFER TO NETWORK	J1	6A
J125 8	REFER TO NETWORK	J62	2A
J125 9	REFER TO NETWORK	J62	2B
J126 1	REFER TO NETWORK	E	1-2
J126 10	REFER TO NETWORK	J60	3A
J126 11	REFER TO NETWORK	J60	3B
J126 12	REFER TO NETWORK	J60	21A
J126 13	REFER TO NETWORK	J60	21B
J126 14	REFER TO NETWORK	J60	19A
J126 15	REFER TO NETWORK	J60	16A
J126 16	REFER TO NETWORK	J60	16B
J126 17	REFER TO NETWORK	J60	17A
J126 18	REFER TO NETWORK	J60	17B
J126 19	REFER TO NETWORK	J60	20B
J126 2	REFER TO NETWORK	J60	18A
J126 23	REFER TO NETWORK	J60	15B
J126 24	REFER TO NETWORK	J60	15A
J126 3	REFER TO NETWORK	J60	20A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J126 5	REFER TO NETWORK	J60	1A
J126 6	REFER TO NETWORK	J60	1B
J126 7	REFER TO NETWORK	J1	6A
J126 8	REFER TO NETWORK	J60	2A
J126 9	REFER TO NETWORK	J60	2B
J127 1	REFER TO NETWORK	E	1-2
J127 10	REFER TO NETWORK	J58	3A
J127 11	REFER TO NETWORK	J58	3B
J127 12	REFER TO NETWORK	J58	21A
J127 13	REFER TO NETWORK	J58	21B
J127 14	REFER TO NETWORK	J58	19A
J127 15	REFER TO NETWORK	J58	16A
J127 16	REFER TO NETWORK	J58	16B
J127 17	REFER TO NETWORK	J58	17A
J127 18	REFER TO NETWORK	J58	17B
J127 19	REFER TO NETWORK	J58	20B
J127 2	REFER TO NETWORK	J58	18A
J127 23	REFER TO NETWORK	J58	15B
J127 24	REFER TO NETWORK	J58	15A
J127 3	REFER TO NETWORK	J58	20A
J127 5	REFER TO NETWORK	J58	1A
J127 6	REFER TO NETWORK	J58	1B
J127 7	REFER TO NETWORK	J1	6A
J127 8	REFER TO NETWORK	J58	2A
J127 9	REFER TO NETWORK	J58	2B
J128 1	REFER TO NETWORK	E	1-2
J128 10	REFER TO NETWORK	J56	3A
J128 11	REFER TO NETWORK	J56	3B
J128 12	REFER TO NETWORK	J56	21A
J128 13	REFER TO NETWORK	J56	21B
J128 14	REFER TO NETWORK	J56	19A
J128 15	REFER TO NETWORK	J56	16A
J128 16	REFER TO NETWORK	J56	16B
J128 17	REFER TO NETWORK	J56	17A
J128 18	REFER TO NETWORK	J56	17B
J128 19	REFER TO NETWORK	J56	20B
J128 2	REFER TO NETWORK	J56	19A
J128 23	REFER TO NETWORK	J56	15B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J128 24	REFER TO NETWORK	J56	15A
J128 3	REFER TO NETWORK	J56	20A
J128 5	REFER TO NETWORK	J56	1A
J128 6	REFER TO NETWORK	J56	1B
J128 7	REFER TO NETWORK	J1	6A
J128 8	REFER TO NETWORK	J56	2A
J128 9	REFER TO NETWORK	J56	2B
J129 1	REFER TO NETWORK	E	1-2
J129 10	REFER TO NETWORK	J54	3A
J129 11	REFER TO NETWORK	J54	3B
J129 12	REFER TO NETWORK	J54	21A
J129 13	REFER TO NETWORK	J54	21B
J129 14	REFER TO NETWORK	J54	19A
J129 15	REFER TO NETWORK	J54	16A
J129 16	REFER TO NETWORK	J54	16B
J129 17	REFER TO NETWORK	J54	17A
J129 18	REFER TO NETWORK	J54	17B
J129 19	REFER TO NETWORK	J54	20B
J129 2	REFER TO NETWORK	J54	18A
J129 23	REFER TO NETWORK	J54	15B
J129 24	REFER TO NETWORK	J54	15A
J129 3	REFER TO NETWORK	J54	20A
J129 5	REFER TO NETWORK	J54	1A
J129 6	REFER TO NETWORK	J54	1B
J129 7	REFER TO NETWORK	J54	6A
J129 8	REFER TO NETWORK	J54	2A
J129 9	REFER TO NETWORK	J54	2B
J130 1	REFER TO NETWORK	E	1-2
J130 10	REFER TO NETWORK	J52	3A
J130 11	REFER TO NETWORK	J52	3B
J130 12	REFER TO NETWORK	J52	21A
J130 13	REFER TO NETWORK	J52	21B
J130 14	REFER TO NETWORK	J52	19A
J130 15	REFER TO NETWORK	J52	16A
J130 16	REFER TO NETWORK	J52	16B
J130 17	REFER TO NETWORK	J52	17A
J130 18	REFER TO NETWORK	J52	17B
J130 19	REFER TO NETWORK	J52	20B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J130 2	REFER TO NETWORK	J52	18A
J130 23	REFER TO NETWORK	J52	15B
J130 24	REFER TO NETWORK	J52	15A
J130 3	REFER TO NETWORK	J52	20A
J130 5	REFER TO NETWORK	J52	1A
J130 6	REFER TO NETWORK	J52	1B
J130 7	REFER TO NETWORK	J1	6A
J130 8	REFER TO NETWORK	J52	2A
J130 9	REFER TO NETWORK	J52	2B
J131 1	REFER TO NETWORK	E	1-2
J131 10	REFER TO NETWORK	J50	3A
J131 11	REFER TO NETWORK	J50	3B
J131 12	REFER TO NETWORK	J50	21A
J131 13	REFER TO NETWORK	J50	21B
J131 14	REFER TO NETWORK	J50	19A
J131 15	REFER TO NETWORK	J50	16A
J131 16	REFER TO NETWORK	J50	16B
J131 17	REFER TO NETWORK	J50	17A
J131 18	REFER TO NETWORK	J50	17B
J131 19	REFER TO NETWORK	J50	20B
J131 2	REFER TO NETWORK	J50	18A
J131 23	REFER TO NETWORK	J50	15B
J131 24	REFER TO NETWORK	J50	15A
J131 3	REFER TO NETWORK	J50	20A
J131 5	REFER TO NETWORK	J50	1A
J131 6	REFER TO NETWORK	J50	1B
J131 7	REFER TO NETWORK	J1	6A
J131 8	REFER TO NETWORK	J50	2A
J131 9	REFER TO NETWORK	J50	2B
J132 1	REFER TO NETWORK	E	1-2
J132 10	REFER TO NETWORK	J94	3A
J132 11	REFER TO NETWORK	J94	3B
J132 12	REFER TO NETWORK	J94	21A
J132 13	REFER TO NETWORK	J94	21B
J132 14	REFER TO NETWORK	J94	19A
J132 15	REFER TO NETWORK	J94	16A
J132 16	REFER TO NETWORK	J94	16B
J132 17	REFER TO NETWORK	J94	17A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J132 18	REFER TO NETWORK	J94	17B
J132 19	REFER TO NETWORK	J94	20B
J132 2	REFER TO NETWORK	J94	1A
J132 23	REFER TO NETWORK	J94	15B
J132 24	REFER TO NETWORK	J94	15A
J132 3	REFER TO NETWORK	J94	20A
J132 5	REFER TO NETWORK	J94	1A
J132 6	REFER TO NETWORK	J94	1B
J132 7	REFER TO NETWORK	J1	6A
J132 8	REFER TO NETWORK	J94	2A
J132 9	REFER TO NETWORK	J94	2B
J133 1	REFER TO NETWORK	E	1-2
J133 10	REFER TO NETWORK	J90	3A
J133 11	REFER TO NETWORK	J90	3B
J133 12	REFER TO NETWORK	J90	21A
J133 13	REFER TO NETWORK	J90	21B
J133 14	REFER TO NETWORK	J90	19A
J133 15	REFER TO NETWORK	J90	16A
J133 16	REFER TO NETWORK	J90	16B
J133 17	REFER TO NETWORK	J90	17A
J133 18	REFER TO NETWORK	J90	17B
J133 19	REFER TO NETWORK	J90	20B
J133 2	REFER TO NETWORK	J90	18A
J133 23	REFER TO NETWORK	J90	15B
J133 24	REFER TO NETWORK	J90	15A
J133 3	REFER TO NETWORK	J90	20A
J133 5	REFER TO NETWORK	J90	1A
J133 6	REFER TO NETWORK	J90	1B
J133 7	REFER TO NETWORK	J1	6A
J133 8	REFER TO NETWORK	J90	2A
J133 9	REFER TO NETWORK	J90	2B
J134 1	REFER TO NETWORK	E	1-2
J134 10	REFER TO NETWORK	J86	3A
J134 11	REFER TO NETWORK	J86	3B
J134 12	REFER TO NETWORK	J86	21A
J134 13	REFER TO NETWORK	J86	21B
J134 14	REFER TO NETWORK	J86	19A
J134 15	REFER TO NETWORK	J86	16A

Table B-1. Rear Assembly Wire Connection List - Continued

FROM	TO	REF. DESG.	SIGNAL NAME
J134 16	REFER TO NETWORK	J86	16B
J134 17	REFER TO NETWORK	J86	17A
J134 18	REFER TO NETWORK	J86	17B
J134 19	REFER TO NETWORK	J86	20B
J134 2	REFER TO NETWORK	J86	18A
J134 23	REFER TO NETWORK	J86	15B
J134 24	REFER TO NETWORK	J86	15A
J134 3	REFER TO NETWORK	J86	20A
J134 5	REFER TO NETWORK	J86	1A
J134 6	REFER TO NETWORK	J86	1B
J134 7	REFER TO NETWORK	J1	6A
J134 8	REFER TO NETWORK	J86	2A
J134 9	REFER TO NETWORK	J86	2B
J135 1	REFER TO NETWORK	E	1-2
J135 10	REFER TO NETWORK	J82	3A
J135 11	REFER TO NETWORK	J82	3B
J135 12	REFER TO NETWORK	J82	21A
J135 13	REFER TO NETWORK	J82	21B
J135 14	REFER TO NETWORK	J82	19A
J135 15	REFER TO NETWORK	J82	16A
J135 16	REFER TO NETWORK	J82	16B
J135 17	REFER TO NETWORK	J82	17A
J135 18	REFER TO NETWORK	J82	17B
J135 19	REFER TO NETWORK	J82	20B
J135 2	REFER TO NETWORK	J82	18A
J135 23	REFER TO NETWORK	J82	15B
J135 24	REFER TO NETWORK	J82	15A
J135 3	REFER TO NETWORK	J82	20A
J135 5	REFER TO NETWORK	J82	1A
J135 6	REFER TO NETWORK	J82	1B
J135 7	REFER TO NETWORK	J1	6A
J135 8	REFER TO NETWORK	J82	2A
J135 9	REFER TO NETWORK	J82	2B
J136 1	REFER TO NETWORK	E	1-2
J136 10	REFER TO NETWORK	J78	3h
J136 11	REFER TO NETWORK	J78	3B
J136 12	REFER TO NETWORK	J78	21A
J136 13	REFER TO NETWORK	J78	21B

Table B-1. Rear Assembly Wire Connection List - Continued

FROM		TO	REF. DESG.	SIGNAL NAME
J136	14	REFER TO NETWORK	J78	19A
J136	15	REFER TO NETWORK	J78	16A
J136	16	REFER TO NETWORK	J78	16B
J136	17	REFER TO NETWORK	J78	17A
J136	18	REFER TO NETWORK	J78	17B
J136	19	REFER TO NETWORK	J78	20B
J136	2	REFER TO NETWORK	J78	18A
J136	23	REFER TO NETWORK	J78	15B
J136	24	REFER TO NETWORK	J78	15A
J136	3	REFER TO NETWORK	J78	20A
J136	5	REFER TO NETWORK	J78	1A
J136	6	REFER TO NETWORK	J78	1B
J136	7	REFER TO NETWORK	J1	6A
J136	8	REFER TO NETWORK	J78	2A
J136	9	REFER TO NETWORK	J78	2B
J137	1	REFER TO NETWORK	E	1-2
J137	10	REFER TO NETWORK	J74	3A
J137	11	REFER TO NETWORK	J74	3B
J137	12	REFER TO NETWORK	J74	21A
J137	13	REFER TO NETWORK	J74	21B
J137	14	REFER TO NETWORK	J74	19A
J137	15	REFER TO NETWORK	J74	16A
J137	16	REFER TO NETWORK	J74	16B
J137	17	REFER TO NETWORK	J74	17A
J137	18	REFER TO NETWORK	J74	17B
J137	19	REFER TO NETWORK	J74	20B
J137	2	REFER TO NETWORK	J74	18A
J137	23	REFER TO NETWORK	J74	15B
J137	24	REFER TO NETWORK	J74	15A
J137	3	REFER TO NETWORK	J74	20A
J137	5	REFER TO NETWORK	J74	1A
J137	6	REFER TO NETWORK	J74	1B
J137	7	REFER TO NETWORK	J1	6A
J137	8	REFER TO NETWORK	J74	2A
J137	9	REFER TO NETWORK	J74	2B

GLOSSARY

Alarms Module	The module in the power supply unit which contains the Alarm logic and Alarm relays.
BF (Framing Bit)	A bit inserted into the MBS to synchronize the far end set.
BIPOLAR Data Format	Bit stream consisting of combined clock and data. Transmitted as a balanced signal for use with T-1 lines.
Bit Counter	A counter which is used to identify the individual bits in a channel.
Built-in Test Equipment (BITE)	Equipment built into the Multiplexer Set for circuit adjustment and module testing.
Channel Counter	A counter with up to 24 discrete output states. Provides channel timing for DTG and channel modules. The transmit and receive sections of the DTG each contain a separate Channel Counter.
Conversion Control Logic	The part of the PCM that determines whether the data is converted to PCM by the ODD or EVEN group A to D converters.
CTPRE	Counter Preset Acknowledge. This signal is produced by the Channel Counter in the DEMUX unit. The Channel Counter provides this signal to the control unit as an acknowledgment of the PR1 signal.
DAC	Digital-to-Analog Converter.
DEMUX Unit	The portion of the Multiplexer Set which synchronizes the receive functions to the framing bits and provides Channel Counter and signaling information to the PCD and channel modules. The DEMUX also recognizes the REMOTE ALARM condition from the far end set.
DTG	Data Timing Group. The section of the Multiplexer Set which performs the timing, multiplexing and PCM conversion for the transmit portion of the Multiplexer Set and performs the timing demultiplexing and PCM conversion for the receive half of the Multiplexer Set.
Data Module	Data interface to/from the user equipment to the Multiplexer Set.
Driver Unit	The portion of the Multiplexer Set which produces clocks for the transmit side of the Multiplexer Set and interfaces with user equipment.
$EC2^{0°}$, $EC2^{1}$, etc.	Encoded Channel Counter signals.
Encoded Channel Count	At 5-bit binary word generated by the Channel Counter in the MUX unit for use by the PCM unit to select the channel to be converted to PCM.
External Commands	User supplied signals which cause the Multiplexer Set to go into the Local Loop or Frame Search Inhibit mode.
EXT Timing Source	A timing signal supplied by external equipment for synchronization of the Multiplexer Set. When External Timing Source is active the internal clock is automatically switched off and the Multiplexer Set receives its timing from the external equipment.
FAULT ALM BUS	Fault Alarm Bus, common to all data timing group and data channel modules.
FR BIT ERR TTL	Frame Bit Error, TTL level. Frame Bit Error signal from the DEMUX unit. This signal occurs each time a frame bit and a predicted frame bit do not match.
Frame Bit Error Monitor	The Frame Bit Error Monitor provides 1 pulse to external equipment for each frame bit that is in error.

Frame Search Inhibit	A user supplied signal which prevents the Multiplexer Set from acquiring frame.
Idle Channel Noise	Noise on a channel with no user signal applied.
Local Loop	An operating condition which connects the output of the transmit section of the DTG to the receive section.
Loss of Frame	A signal produced by the control unit of the DEMUX unit which signals the user that the Multiplexer Set is not in frame.
MA Clock	Recovered receive clock for use by external equipment.
MBS RCVR Clock	Clock signal from the far end set. Used in NRZ mode only.
MBS RCVR Data	Data from the far end set may be NRZ or BIPOLAR format.
MBS XMT Clock	Clock from the Multiplexer Set to the far end set. Used in the NRZ mode only.
Master Clock Out	Clock from the transmit section of the Multiplexer Set for use by external equipment.
Mission Bit Stream (MBS)	A signal stream of data comprised of data from each channel of the Multiplexer Set plus framing and signaling information.
MUX Module	The portion of the Multiplexer Set which generates frame and Channel Count information. The MUX unit also combines the PCM from the PCM module data from the data channel modules, and framing information to form the MBS data. Alarm information is inserted into the MBS by the MUX unit.
NRZ (Non Return to Zero)	Format serial data which does not return to zero until the next data transition. NRZ data is used in conjunction with NRZ clock for timing formation.
ODD/EVEN Output Control	The circuit in the PCM which determines whether the output of the ODD or EVEN serial-to-parallel converters is placed on the PCM Bus.
OGA	Outgoing Alarm from the power supply to the MUX unit. When this line is active the data is sent as 00001111 if selected and B2=0 is inserted into each voice channel.
OGAT	Operational Gate. A signal produced by the Acquisition Counter in the DEMUX unit. This signal provides a window in which the frame bit candidate is located.
PAM	Pulse Amplitude Modification.
Parallel to Serial Converter	A circuit which converts bits of parallel data into a serial bit stream.
PCD Unit	Converts PCM data to an analog signal and distributes the data to the receive portions of the VF modules. Signaling information is also routed through this module.
PCM Data Bus	PCM data from the PCM unit to the MUX unit.
PCM Module	The DTG module which performs the analog multiplexing and PCM encoding functions of the Multiplexer Set.
PR1	Preset to channel 1. This signal presets the Channel Counter to Channel 1. This signal is produced by the control unit in the DEMUX. The signal occurs each time a good frame bit occurs in the 24-channel mode and once every time the 001 or 110 pattern is detected in the 3, 6, and 12.
$\overline{\text{RCV CH CTR 1 through 24}}$	Receive Channel Counter 1 through 24. Negative going signals one channel time wide. Used to gate channel modules to indicate that the DTG is ready to send data or signaling information to the module.
RCV DATA BUS CLK	Receive Data Bus Clock. 1.536 MHz clock to the data channel modules.
RCV FRAME 6/18	Signaling sync for receive side of Multiplexer Set.
RCV PCM BUS	PCM data to the PCD unit and data channel modules.

RCV RESET TO CH 1	Receive reset to Channel 1 signal from the DEMUX unit to the PCD unit.
RCV SIG A BUS	Signaling information to the VF modules.
RCV VF OUT 1 through 24	VF information to the VF channel modules.
RCVR Unit	The portion of the Multiplexer Set which receives MBS data and clock from user equipment. The RCVR also provides clocks to the receive section of the Multiplexer Set.
Recovered Clock	Clock which has been multiplied to 24.704 MHz and divided back to the MBS rate.
SFPR	Superframe Preset. 1-bit wide pulse which occurs at the beginning of each Superframe.
Sample and Hold	A circuit which samples a voltage for a short period of time and holds the level of the sampled voltage constant at the output of the Sample and Hold regardless of voltage changes at the input.
Sieve Memory	The Sieve Memory is located within the DEMUX unit. The function of this circuit is to provide a pointer within the OGAT time to indicate which bit is the frame bit candidate.
Signal to Quantizing Noise	Noise produced by the PCM encoding and decoding processes in VF channels.
Signaling Control	The circuit which places the signaling information onto the PCM Bus.
16 KPPS	Drive signal for the Power Converter unit in the supply module. This signal is produced by multiplying the XMT RESET TO CH 1 signal by 2 to produce the 16 KPPS signal.
TRF	Transformer rectifier filter unit. Used to supply de power to the power supply unit when the Multiplexer Set is operated from 115 Vac or 230 Vac.
Time Division Multiplexing	Combining a number of inputs by assigning a time slot for each input and sequentially sampling each signal to form a single stream of data containing information from all of the inputs.
VF Module	Voice frequency interface from the user equipment to the Multiplexer Set.
XMT ADV CHAN CTR	Transmit advance Channel Counter. Negative going pulse which occurs at the end of each channel time.
XMT CHAN CTR 1 to XMT CHAN CTR 24	Transmit Channel Counter 1 through 24. Negative going signals one channel time wide. Used to Gate channel modules to indicate that the DTG is, ready to accept data or signaling information from the module.
XMT CONT BUS	Transmit Control Bus. Signal from the data channel units that the channel being sampled is a data channel.
XMT DATA BUS	Data from data modules. Selected module places data on the bus when its XMT CHAN CTR line goes low.
XMT DATA BUS CLOCK	1.536 MHz clock from the MUX unit to the data channel units.
XMT FRAME 6+12	Transmit frame 6 or 12. Signaling sync to the VF modules and PCM unit.
XMT MBS CLOCK	Clock from the DRIVER unit. Rate dependent upon Multiplexer Set configuration.
XMT MBS CLK and XMT MBS CLK	Transmit MBS clock. Rate is dependent on the Multiplexer Set channel configuration.
XMT MBS DATA	Data from the Multiplexer Set to the far end set. May either be NRZ or BIPOLAR.
XMT MODE CONTROL (7)	These signals are used to program the MUX and PCM units for the various operating modes of the Multiplexer Set.
XMT PCM BUS	Common PCM Bus to MUX unit.

XMT RESET TO CH 1	Transmit reset to Channel 1. Negative going pulse which occurs at the end of each frame. In the 24-channel mode this signal is held off for one bit time to allow a space for the frame bit.
XMT SIG A BUS	Signaling Bus from VF channel modules.
XMT VF IN 1 to XMT VF IN 24	Voice frequency data from VF modules.
XMT VF RTN 1 to XMT VF RTN 24	Ground return for XMT VF IN 1 through VF IN 24.
XMT 1.544 MHz CLOCK	1.544 MHz clock to the MUX and PCM units.
XMT 4.096 MHz CLK BUS	4.096 MHz clock to the transmit section of the data channel modules.
Zeroizer Circuit	A circuit in the PCM unit which corrects for offset voltages in the Sample-and-Hold and Analog-to-Digital conversion circuits.
ZERO SUPPRESS	Enables the Zero Suppressor when low. From the DRIVER unit to the MUX unit.
Zero Suppressor	A circuit contained on the MUX unit. Used to provide keep-alive pulses for T-1 repeaters.

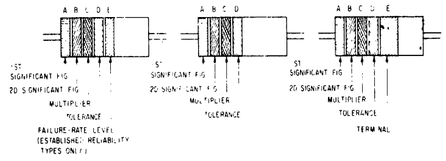
INDEX

INDEX-Continued

INDEX-Continued

INDEX-Continued

INDEX-Continued



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS

TABLE I

COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM
BLACK	0	BLACK	0	BLACK	1			BROWN	M 1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P 0.1	
RED	2	RED	2	RED	100			ORANGE	R 0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S 0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1000 HOURS). ON FILM RESISTORS THIS BAND SHALL BE APPROXIMATELY TWO TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

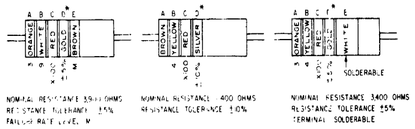
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE

2R7 = 2.7 OHMS, R010 = 0.010 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,920 OHMS
RESISTANCE TOLERANCE ±1%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 400 OHMS
RESISTANCE TOLERANCE ±10%

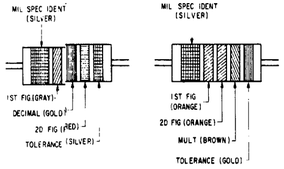
NOMINAL RESISTANCE 3400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE [illegible]

FILM TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTANCE TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS



(A) 82 UH ± 10%

(B) 330 UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF THE CODING FOR AN 82 UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED.

TABLE 2

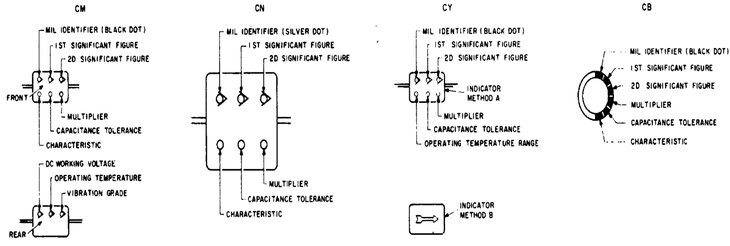
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES

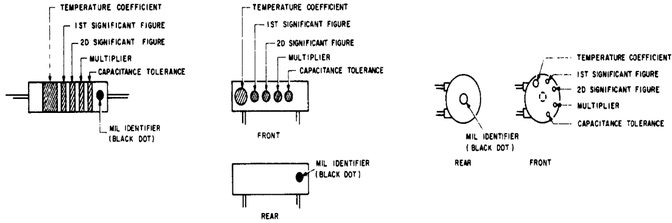
COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB





C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE				CHARACTERISTIC		DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY, CB	0	0	1			±20%	±20%		A			-55° TO +70°C	10-55 Hz
BROWN		1	1	10						B	E	B		
RED		2	2	100	±2%		±2%	±2%	C				-55° TO +85°C	
ORANGE		3	3	1,000		±30%				D		D	300	
YELLOW		4	4	10,000						E			-55° TO +125°C	10-2,000 Hz
GREEN		5	5		±5%					F			500	
BLUE		6	6										-55° TO +150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01[R]			
WHITE		9	9	0.1[R]	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1 THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.

2 LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-250, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.

3 LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.

4 TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

R OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

ESC FM 913 73

Figure FO-1. Color code marking for military standard inductors and capacitors

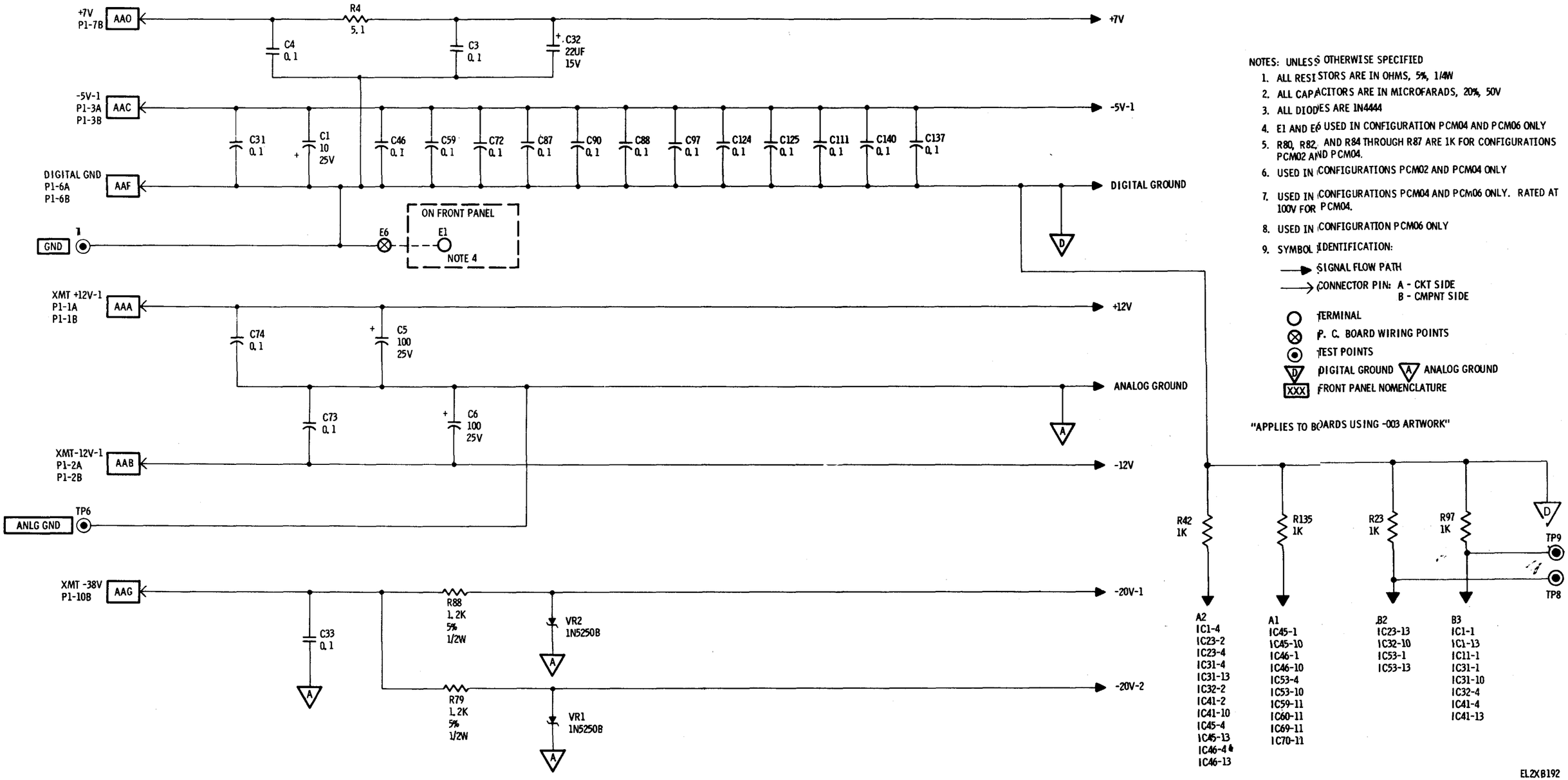


Figure FO-2. PCM unit schematic (sheet 1 of 3).

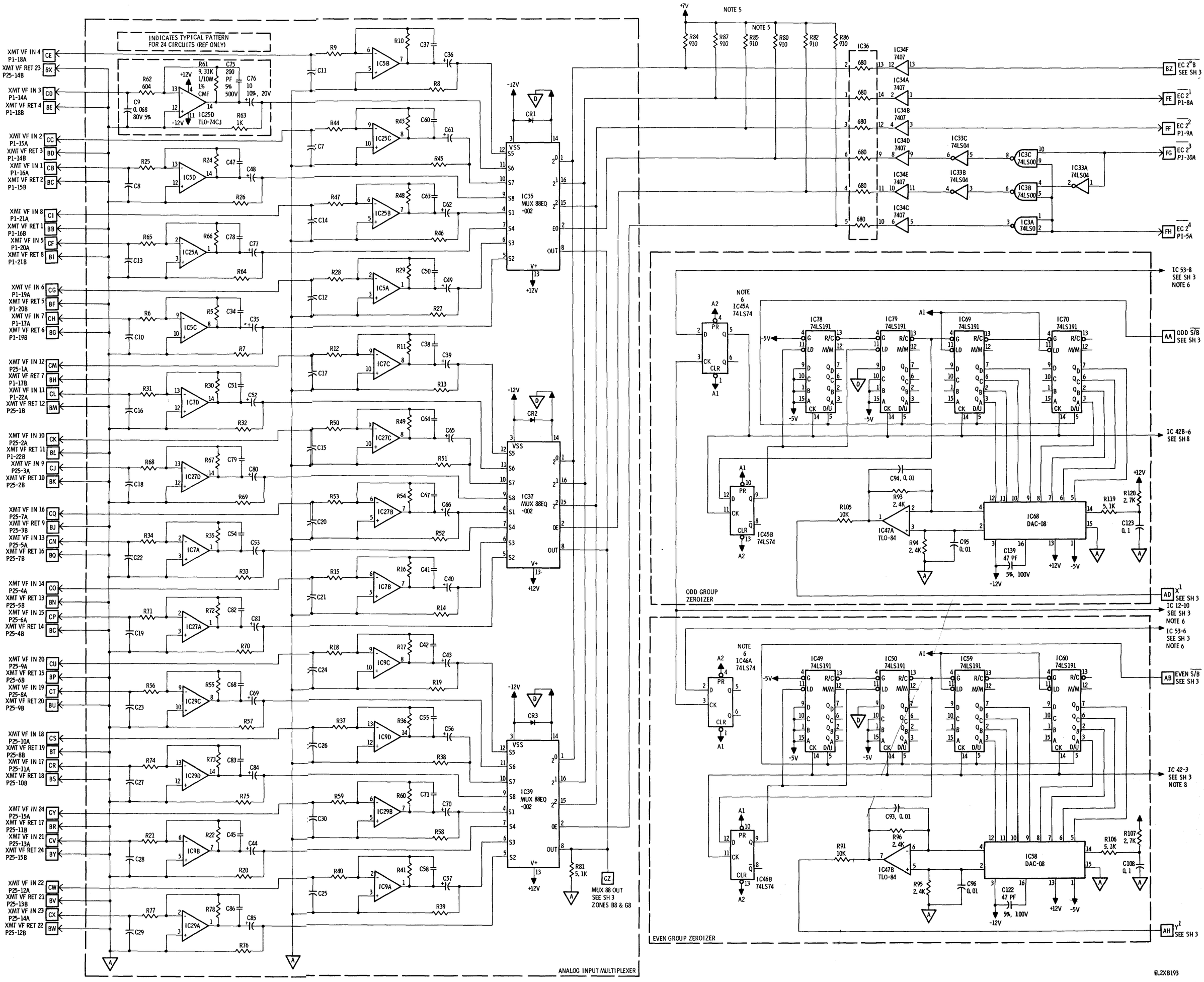


Figure FO-2. PCM unit schematic (sheet 2 of 3).

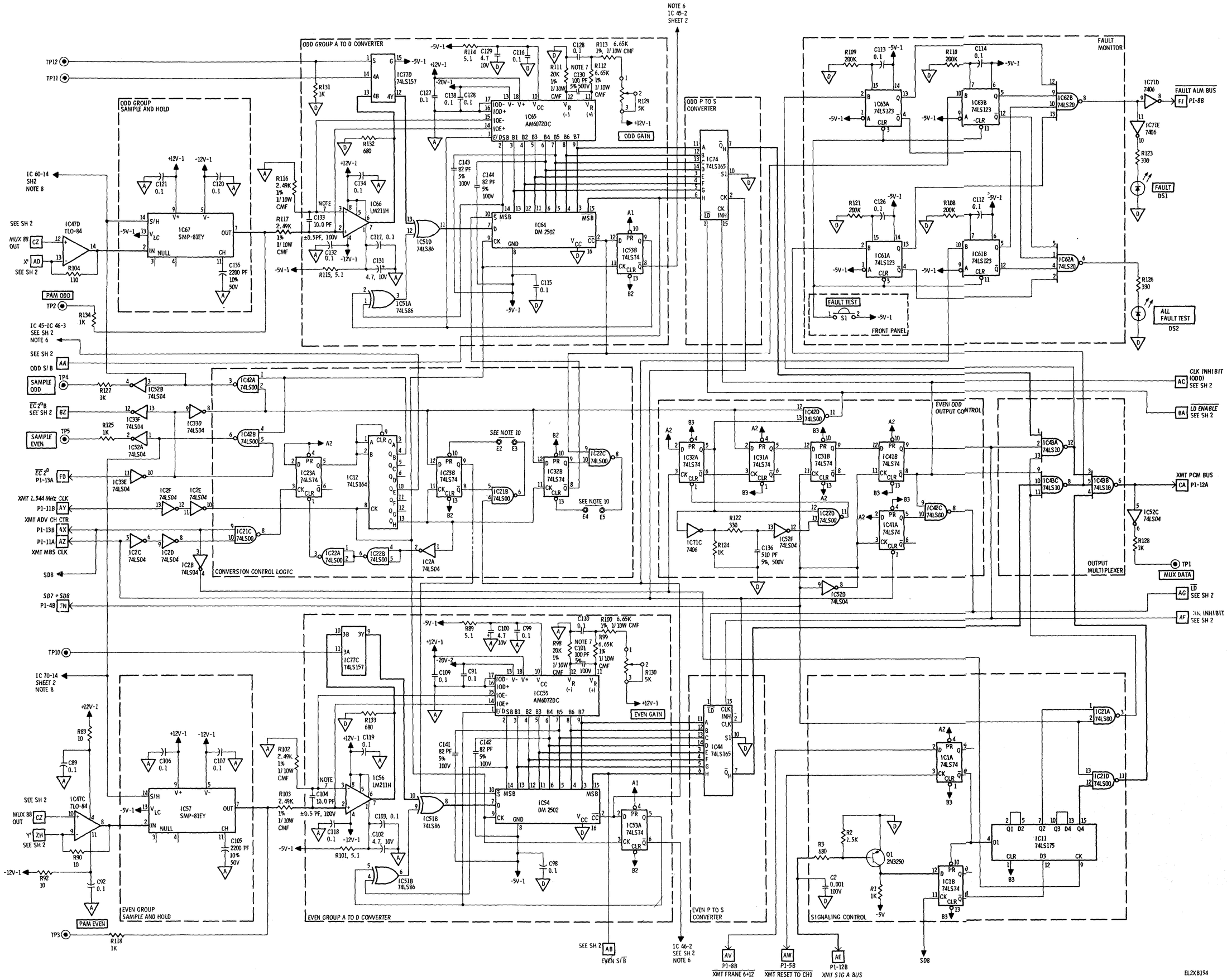
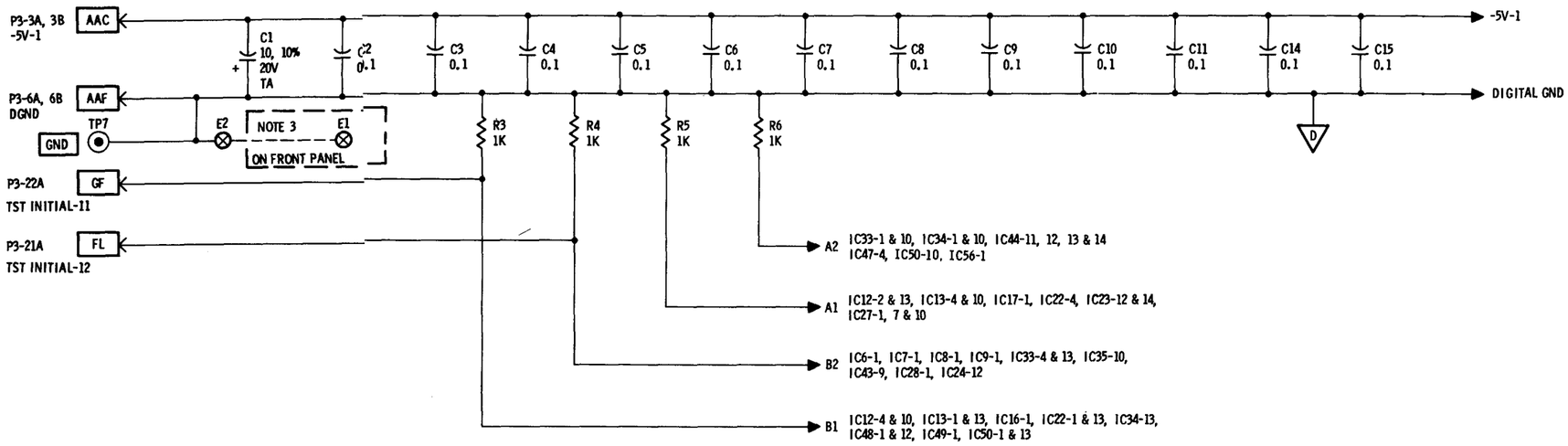
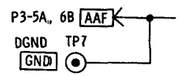


Figure FO-2. PCM unit schematic (sheet 3 of 3).



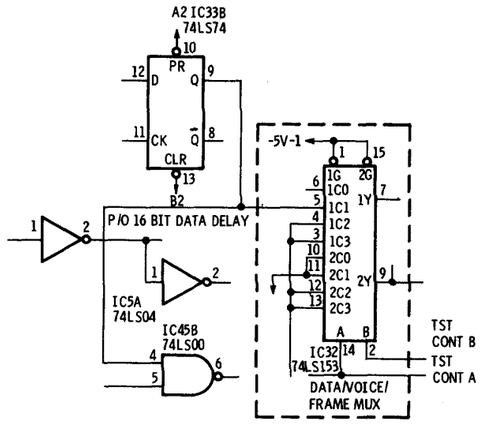
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%, CARBON
   ALL CAPACITORS ARE IN MICROFARADS, 20%, 50V, CERAMIC



2. IC11A USED IN CONFIGURATION MUX04 ONLY WITH OF IC33B CONNECTED DIRECTLY TO IC45B-4 AND THE 1C1 INPUT OF IC32 AS FOLLOWS :

P/O ZERO SUPPRESS CIRCUIT



3. E1 AND E2 USED IN CONFIGURATION MUX04 ONLY.

4. SYMBOL IDENTIFICATION:

- CONNECTOR PIN: A = SOLDER SIDE, B = COMPONENT SIDE
- TEST POINT
- XXX FRONT PANEL NOMENCLATURE
- D DIGITAL GROUND
- TA = TANITALUM
- ⊗ = WIRING POINT

EL2XB195

Figure FO-3. MUX unit schematic (sheet 1 of 3).

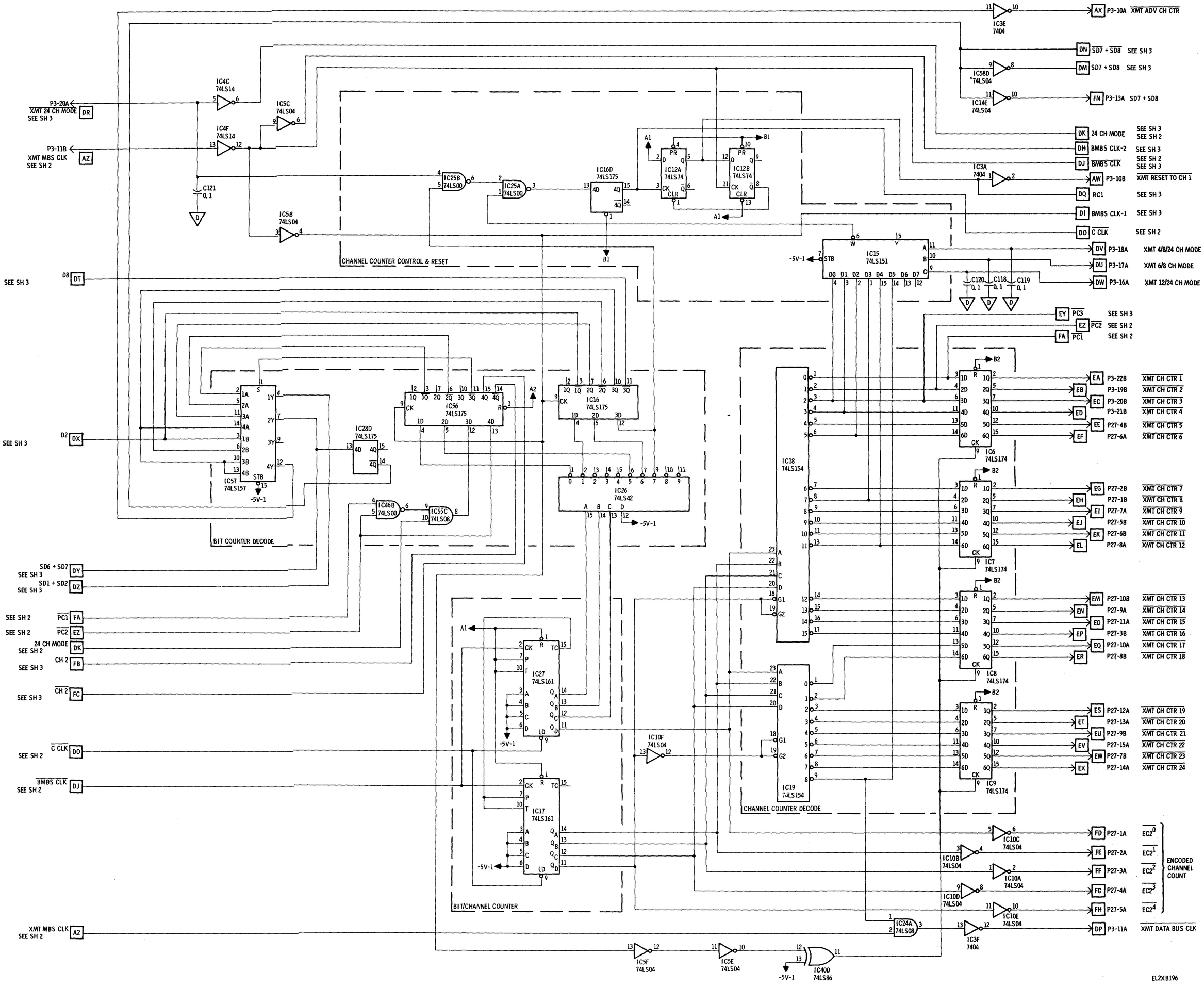


Figure FO-3. MUX unit schematic (sheet 2 of 3).

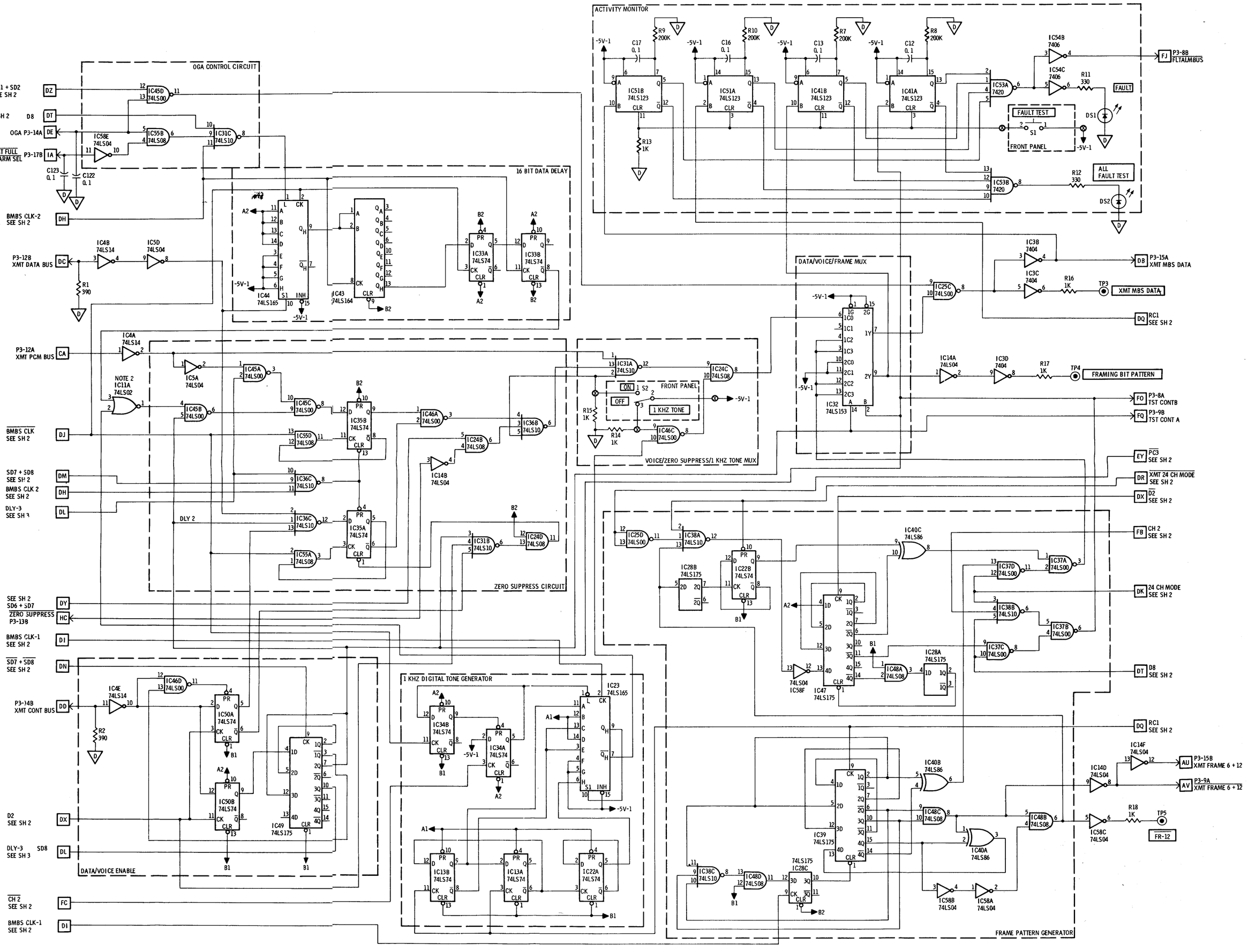


Figure FO-3. MUX unit schematic (sheet 3 of 3).

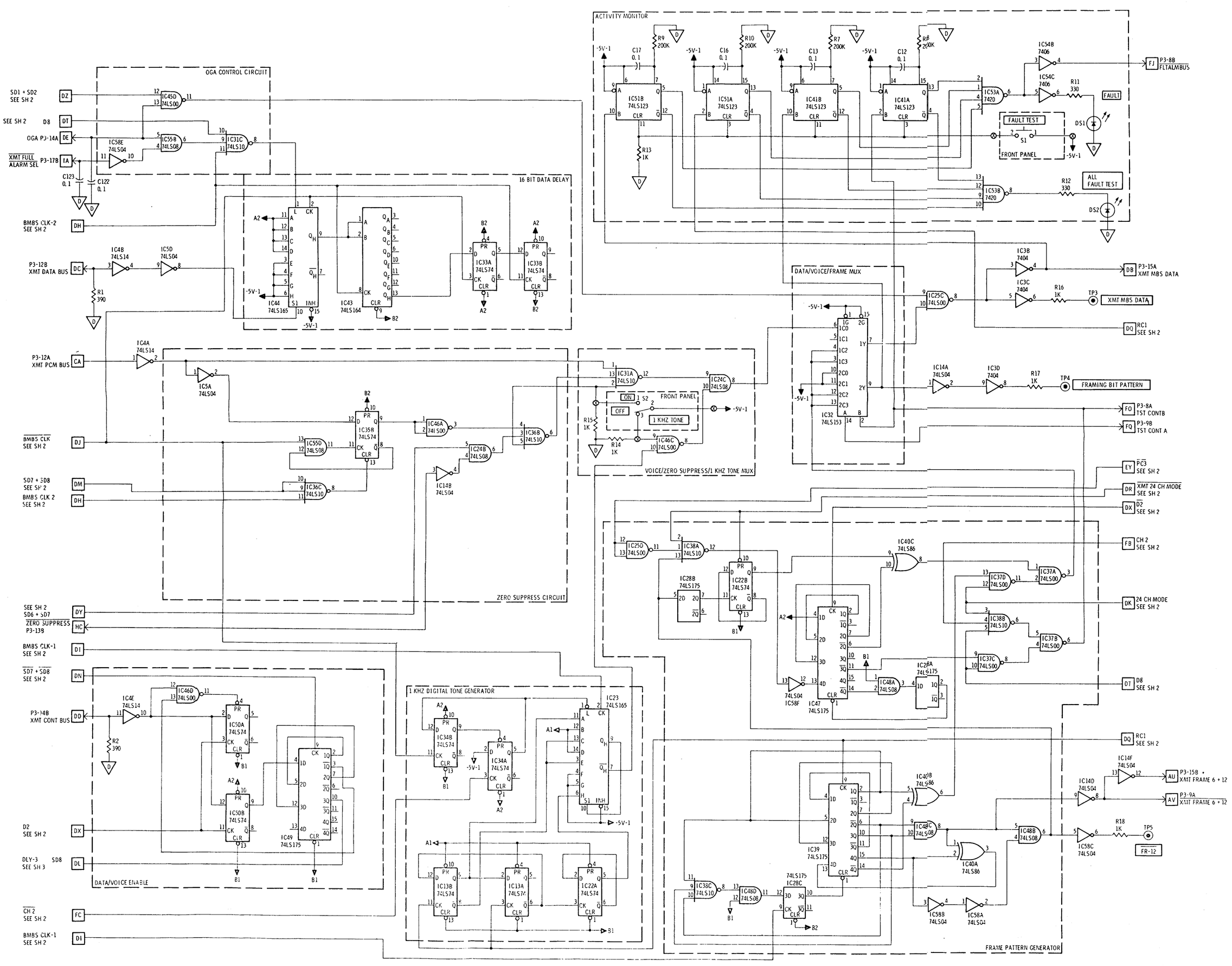
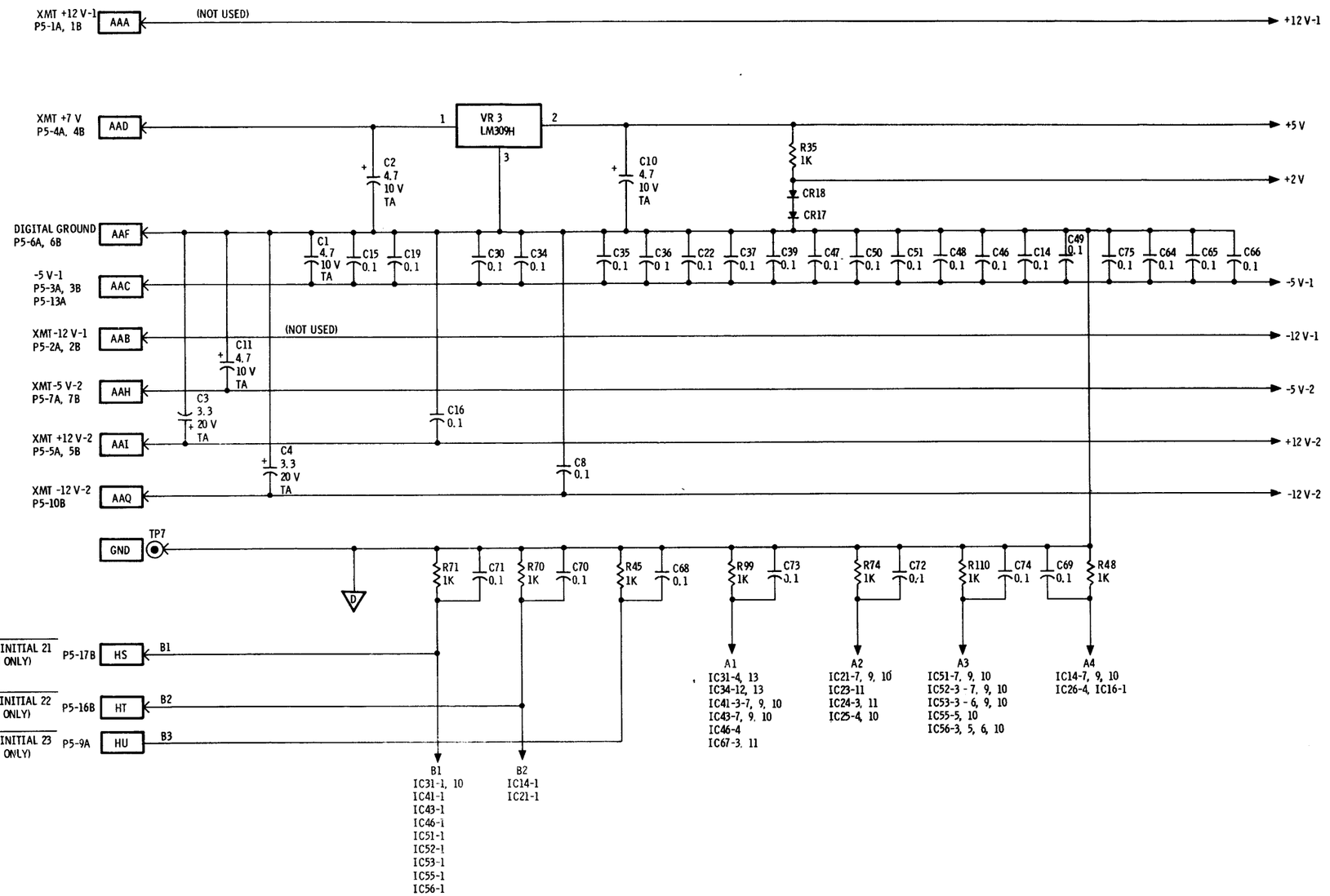


Figure FO-3A. MUX unit schematic (sheet 3.1 of 3)



NOTES UNLESS OTHERWISE SPECIFIED

1. USE WITH ASSY 17460-010 AND 17465-010.
2. ALL RESISTORS IN OHMS, ±5%, 1/4W, CARBON.
3. ALL CAPACITORS ARE IN MICROFARADS ±20%, 50 V, CERAMIC.
4. ALL DIODES ARE IN4444.
5. SYMBOL IDENTIFICATION:
   - TEST POINT
   - WIRING POINT
   - DIGITAL GROUND
   - XXX FRONT PANEL NOMENCLATURE
6. SELECT IN TEST COMPONENTS, INITIAL VALUE SHOWN

Figure FO-4. DRIVER unit schematic (sheet 1 of 6) DVR02.

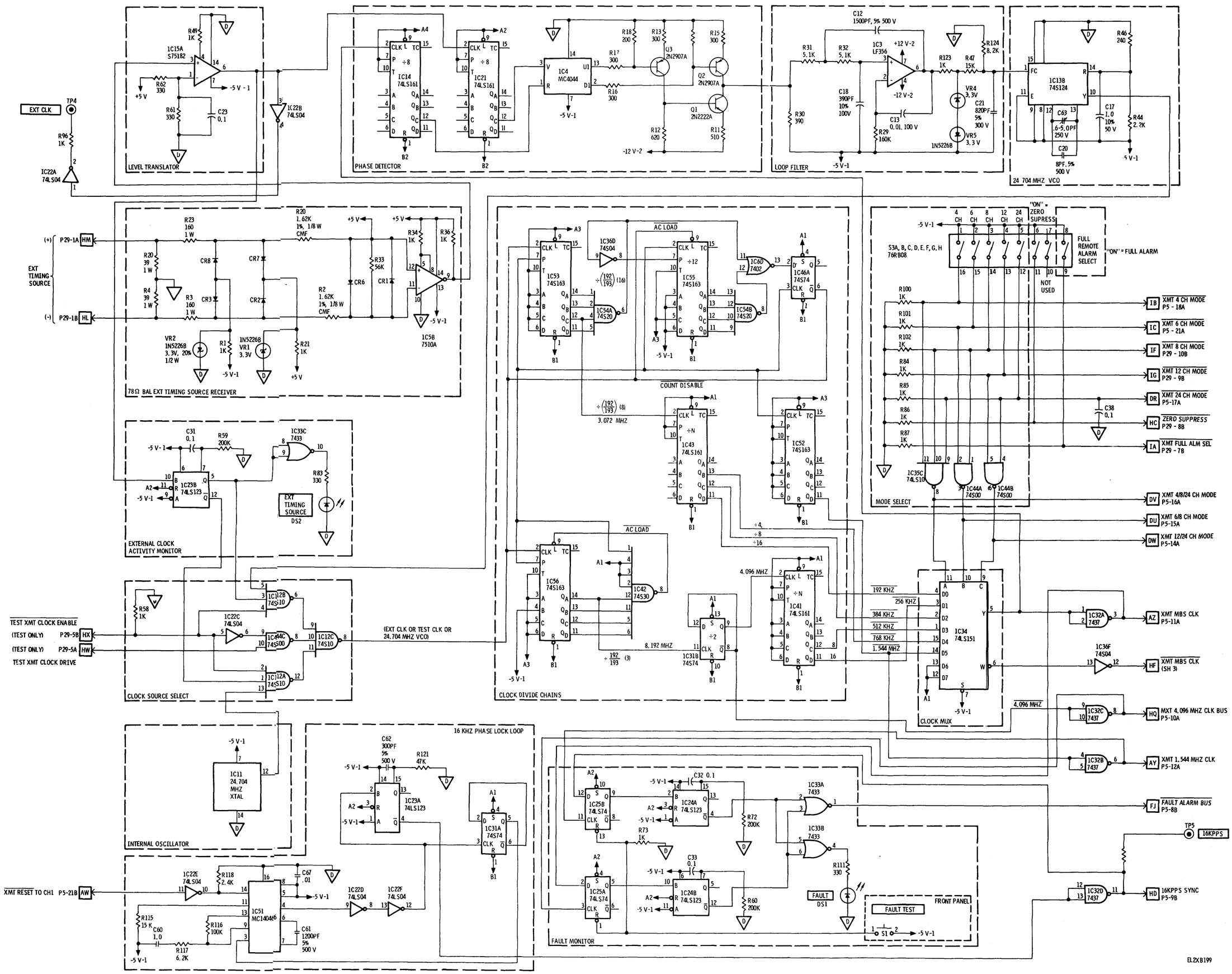


Figure FO-4. DRIVER unit schematic (sheet 2 of 6) DVR02.

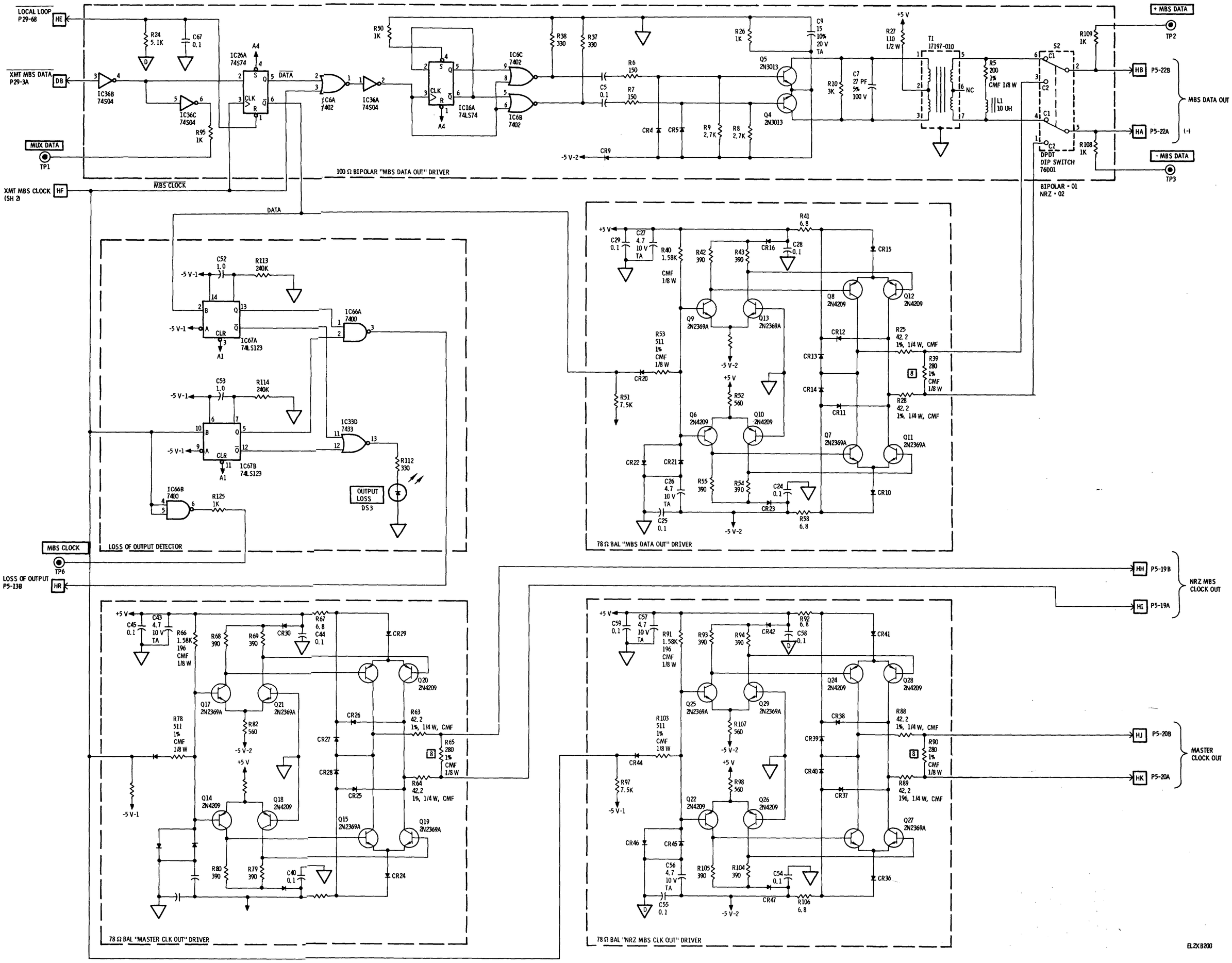


Figure FO-4. Driver unit schematic (sheet 3 of 6) DVR02.

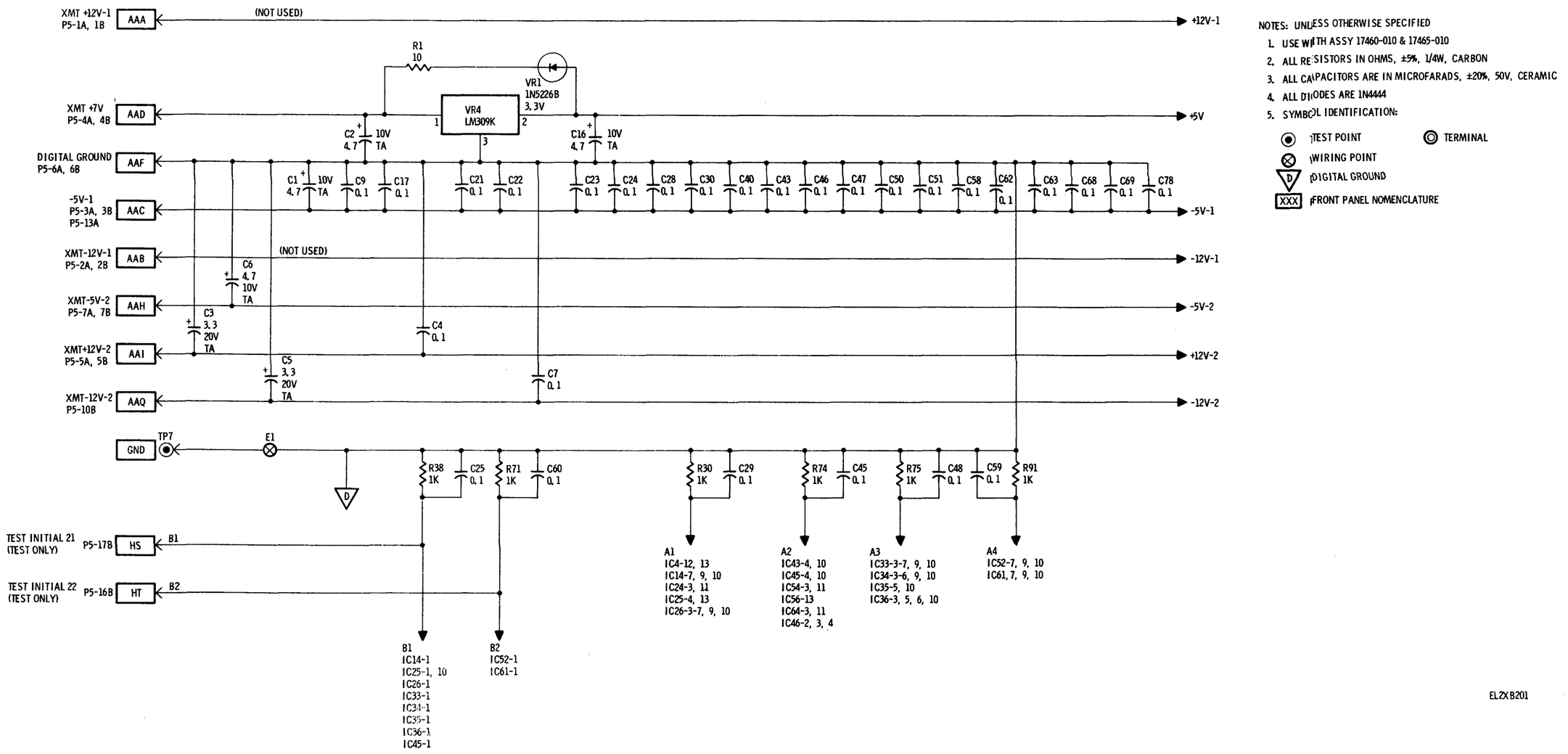


Figure FO-4. DRIVER unit schematic (sheet 4 of 6) DVR04.

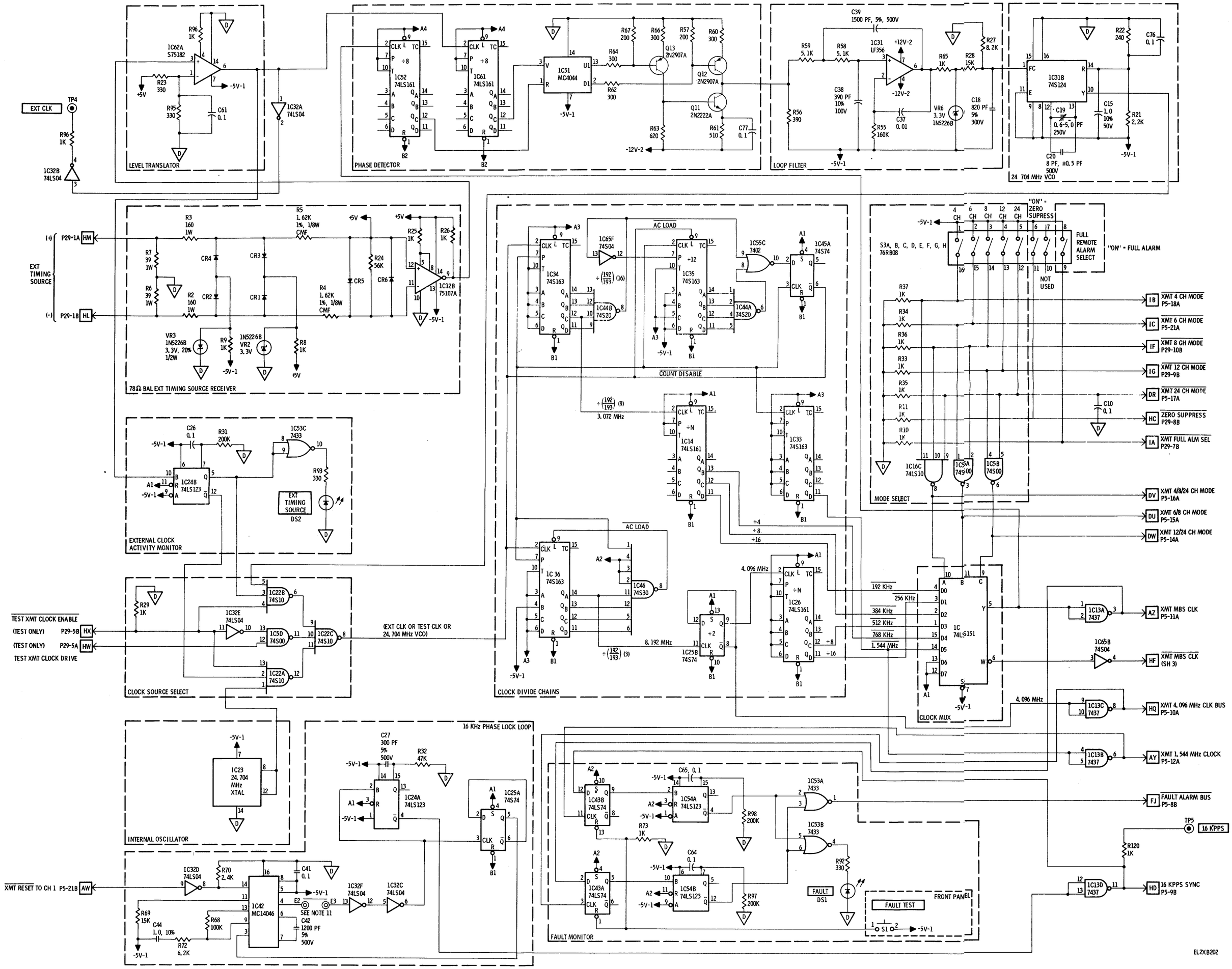


Figure FO-4. DRIVER unit schematic (sheet 5 of 6) DVR04.

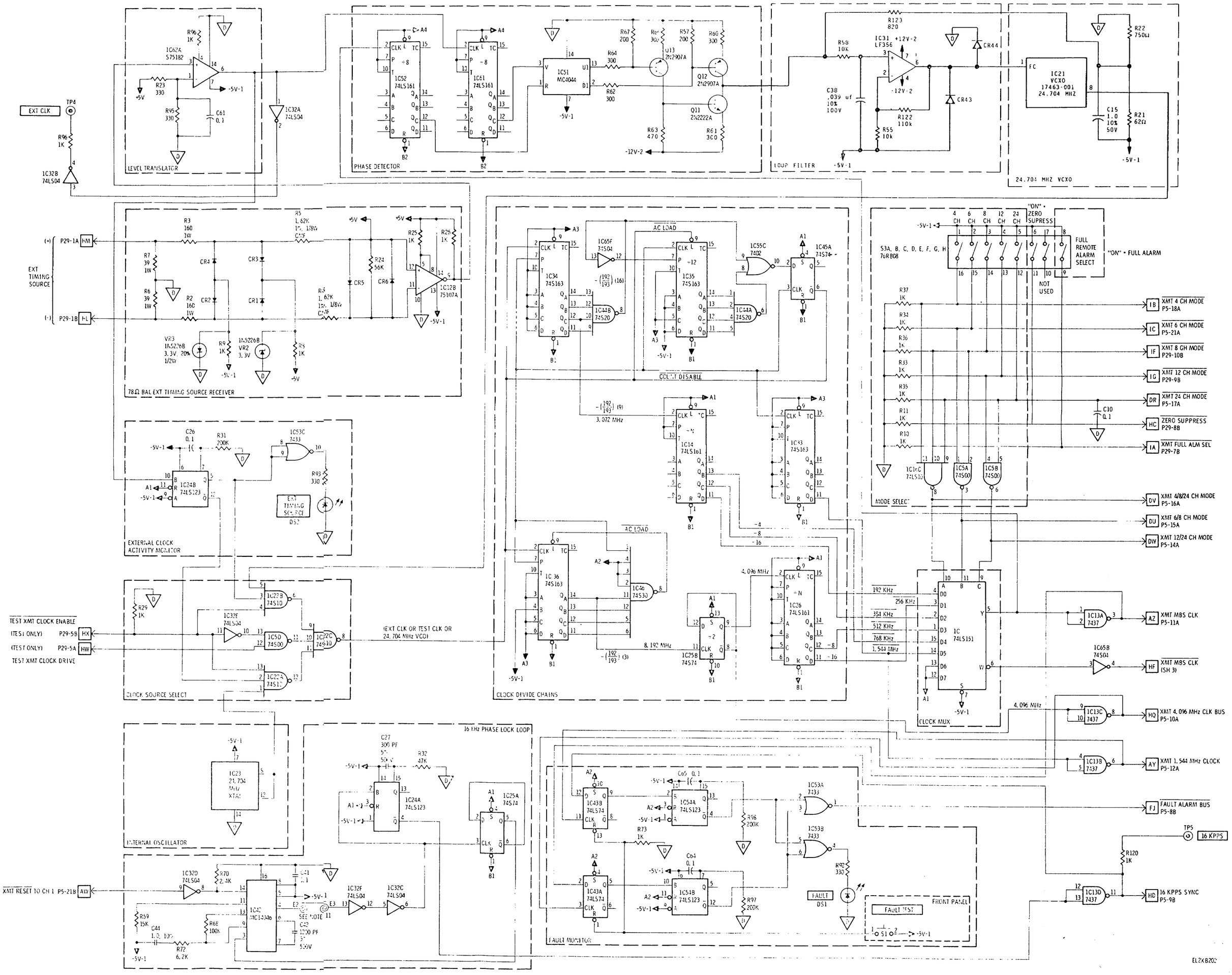


Figure FO-4A. DRIVER unit schematic (sheet 5.1 of 6) DVR04

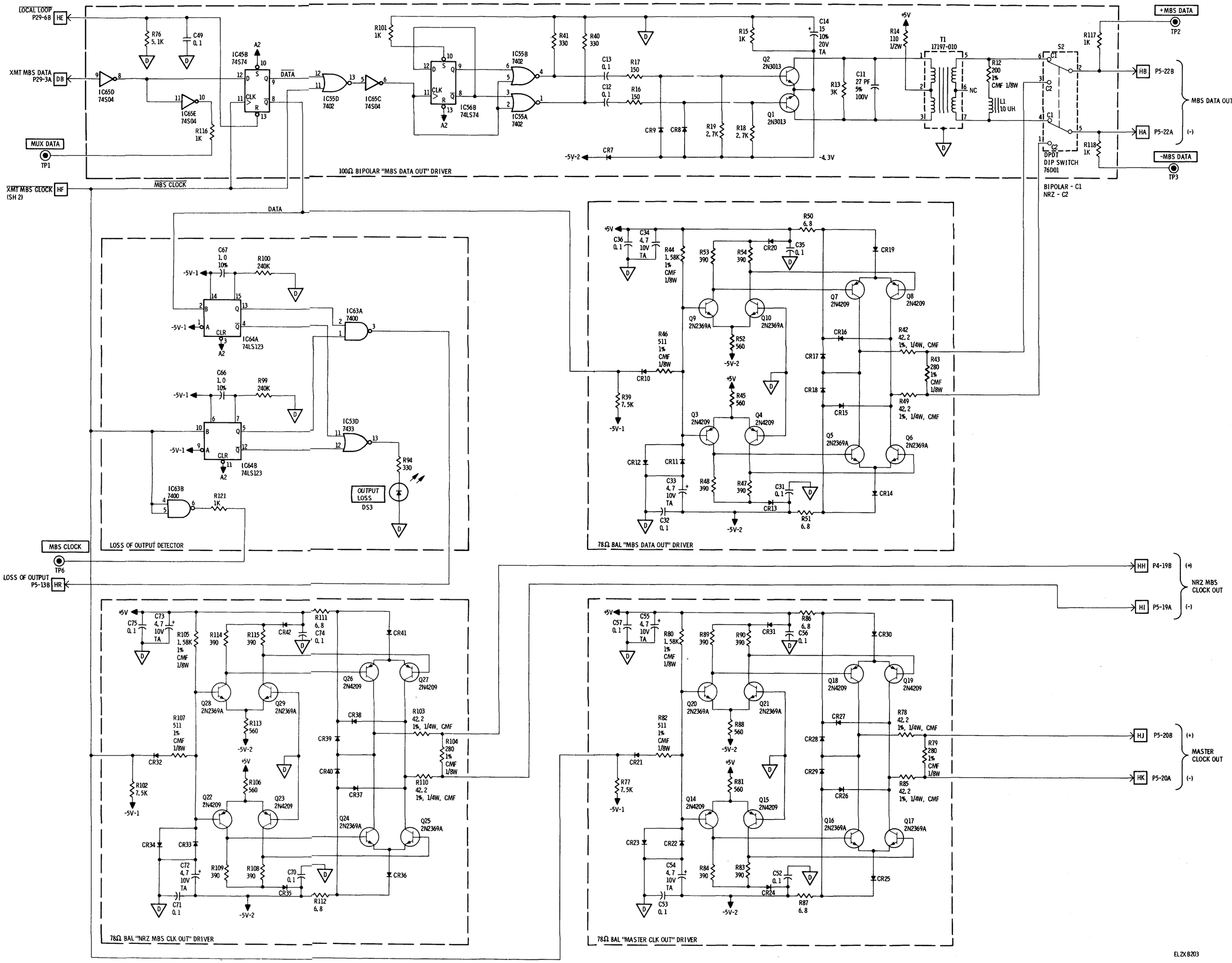
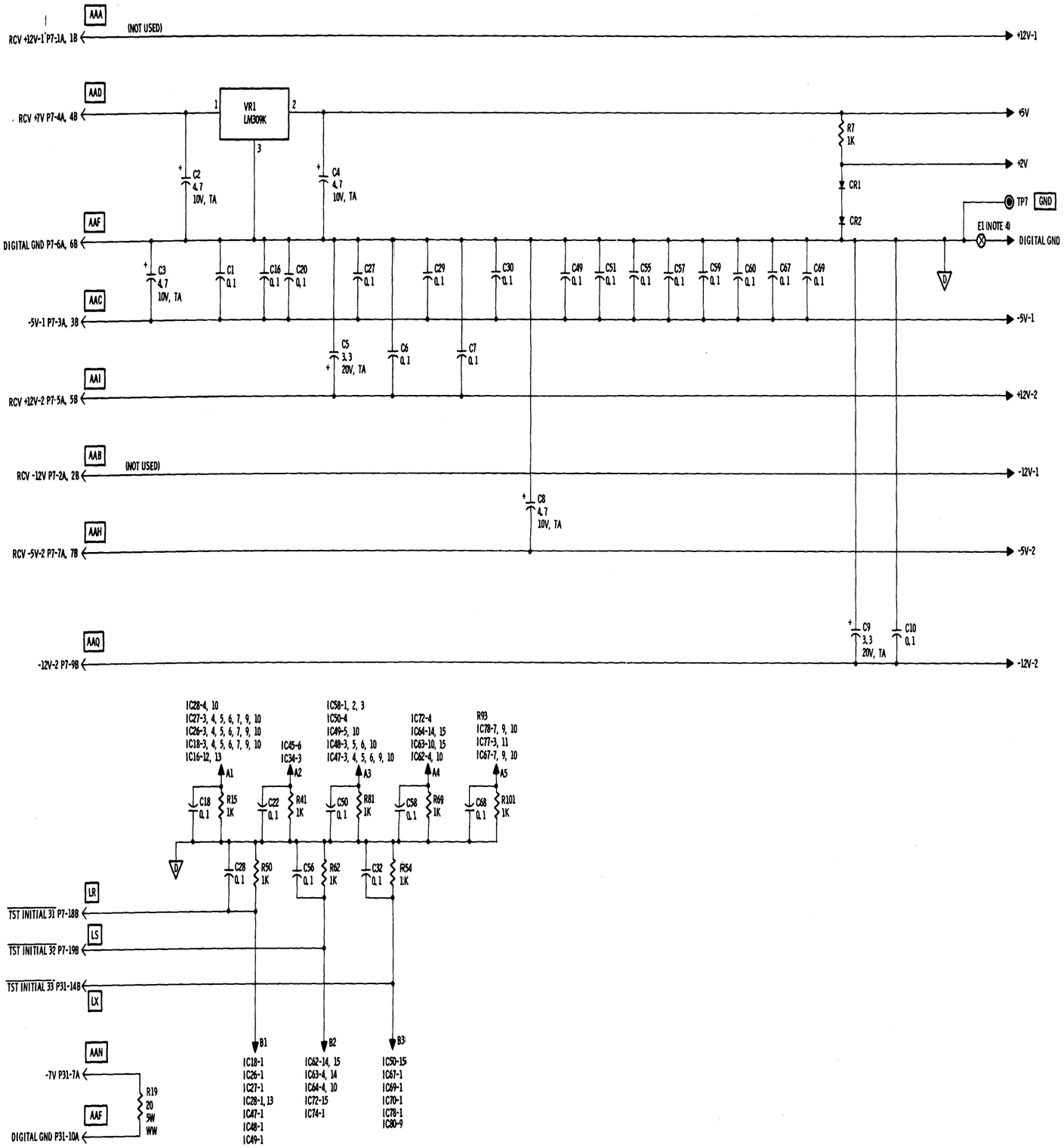


Figure FO-4. DRIVER unit schematic (sheet 6 of 6) DVR04.

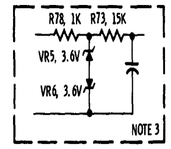


NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%, CARBON
   ALL CAPACITORS ARE IN MICROFARDS, 20%, 50V, CERAMIC
   ALL DIODES ARE 1N4444

2. VALUE FOR R63 IS:
   560 OHMS FOR RCVR06
   430 OHMS FOR RCVR08

3. VR5 IS AS SHOWN FOR CONFIGURATIONS RCVR06 AND RCVR08
   FOR CONFIGURATIONS RCVR02 AND RCVR04, THE CIRCUIT IS
   ALTERED AS FOLLOWS:



4. THE REFERENCE DESIGNATIONS ON SHEETS 1 THROUGH 4 APPLY TO CONFIGURATIONS RCVR06 AND RCVR08 ONLY. THE RESPECTIVE REFERENCE DESIGNATORS FOR RCV02 AND RCV04 ARE AS FOLLOWS:

RCVR06* AND RCVR08	RCVR02 AND RCVR04	RCVR06* AND RCVR08	RCVR02 AND RCVR04	RCVR06* AND RCVR08	RCVR02 AND RCVR04	RCVR06* AND RCVR08	RCVR02 AND RCVR04	RCVR06* AND RCVR08	RCVR02 AND RCVR04	RCVR06* AND RCVR08	RCVR02 AND RCVR04
C1	C1	C36	C34	CR4	CR4	R6	R6	R46	R46	R79	R77
C2	C2	C37	C35	CR5	CR5	R7	R7	R47	R47	R80	R78
C3	C3	C38	C36	CR6	CR6	R8	R8	R48	R48	R81	R79
C4	C4	C39	C61	CR7	CR7	R9	R9	R49	R49	R82	R80
C5	C5	C40	C62	CR8	CR8	R10	R10	R50	R50	R83	R81
C6	C6	C41	C37	CR9	CR9	R11	R11	R51	R51	R84	R82
C7	C7	C42	C38	CR10	CR10	R12	R12	R52	R52	R85	R83
C8	C8	C43	C56	CR11	CR11	R13	R13	R53	R53	R86	R86
C9	C9	C44	C39	CR12	CR12	R14	R14	R54	R54	R87	R84
C10	C10	C45	C40	CR13	CR13	R15	R15	R55	R55	R88	R85
C11	C13	C46	C41	CR14	CR14	R17	R17	R56	R56	R89	R87
C12	C12	C47	C63	CR15	CR15	R18	R18	R57	R57	R90	R88
C13	C14	C48	C42	CR16	CR16	R20	R20	R58	R58	R91	R89
C14	C15	C49	C43	CR17	CR17	R21	R21	R59	R59	R92	R90
C15	C16	C50	C64	CR18	CR18	R22	R22	R60	R60	R93	R91
C16	C17	C51	C44	CR19	CR19	R23	R23	R61	R61	R94	R92
C17	C18	C52	C45	CR20	CR20	R24	R24	R62	R62	R95	R93
C18	C57	C53	C71	CR21	CR21	R25	R25	R63	R63	R96	R94
C20	C20	C54	C65	CR22	CR22	R26	R26	R64	R64	R97	R95
C21	C21	C55	C46	CR23	CR23	R27	R27	R65	R65	R98	R96
C22	C58	C56	C66	CR24	CR24	R28	R28	R66	R66	R99	R97
C23	C23	C57	C47	CR25	CR25	R29	R29	R67	R67	R100	R98
C24	C25	C58	C67	CR26	CR26	R30	R30	R68	R68	R101	R99
C25	C26	C59	C48	CR27	CR27	R31	R31	R69	R69	VR1	VR1
C26	C22	C60	C49	CR29	CR28	R32	R32	R70	R71	VR2	VR2
C27	C27	C61	C68	CR30	CR29	R33	R33	R71	R72	VR3	VR3
C28	C59	C62	C69	E1	NOT USED	R34	R34	R72	R70	VR5	VR5 & VR6
C29	C28	C63	C50	E2	E2	R35	R35	R73	R73		
C30	C29	C64	C51	E3	E3	R36	R36	R74	R100		
C31	C30	C65	C52	R1	R1	R37	R37	R75	R74		
C32	C60	C66	C53	R2	R2	R38	R38	R76	R75		
C33	C31	C67	C54	R3	R3	R39	R39	R77	R76		
C34	C32	C68	C70	R4	R4	R40	R40	R78	R101		
C35	C33	C69	C55	R5	R5	R41	R41				
		CR1	CR1			R42	R43				
		CR2	CR2			R44	R44				
		CR3	CR3			R45	R45				

5. SYMBOL IDENTIFICATION:
   - → SIGNAL FLOW PATH
   - → CONNECTOR PIN: A = SOLDER SIDE; B = COMPONENT SIDE
   - ⊗ = WIRING POINT
   - ◉ = TEST POINT
   - XXX FRONT PANEL NOMENCLATURE
   - ▽ DIGITAL GROUND

   TA = TANTALUM
   CMF = COATED METAL FILM
   WW = WIRE WOUND
   ◎ = TERMINAL

6. STRAP SOLDERED IN PLACE AFTER MANUFACTURING TEST.

EL2X B204

Figure FO-5. RCVR unit schematic (sheet 1 of 4)

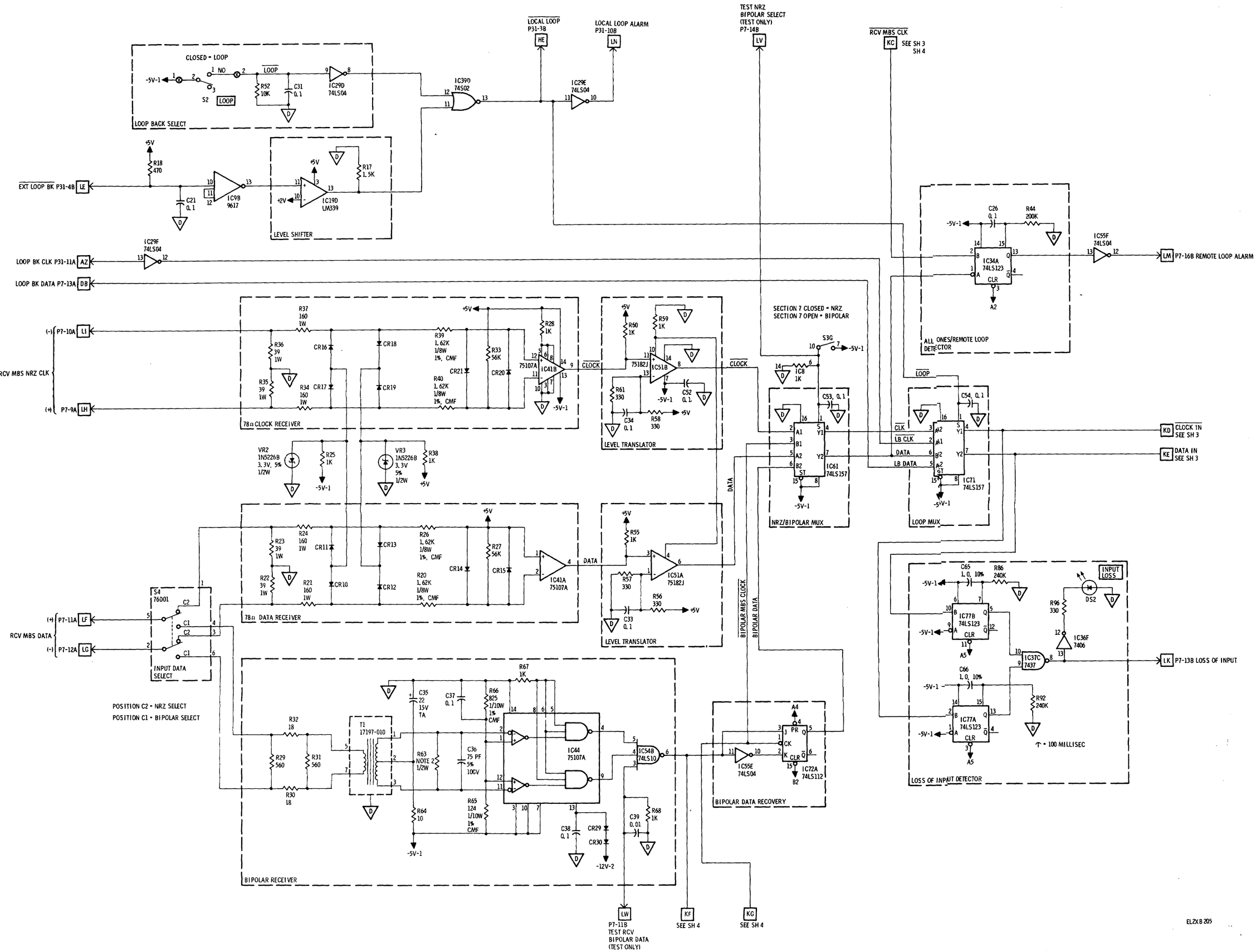


Figure FO-5. RCVR unit schematic (sheet 2 of 4)

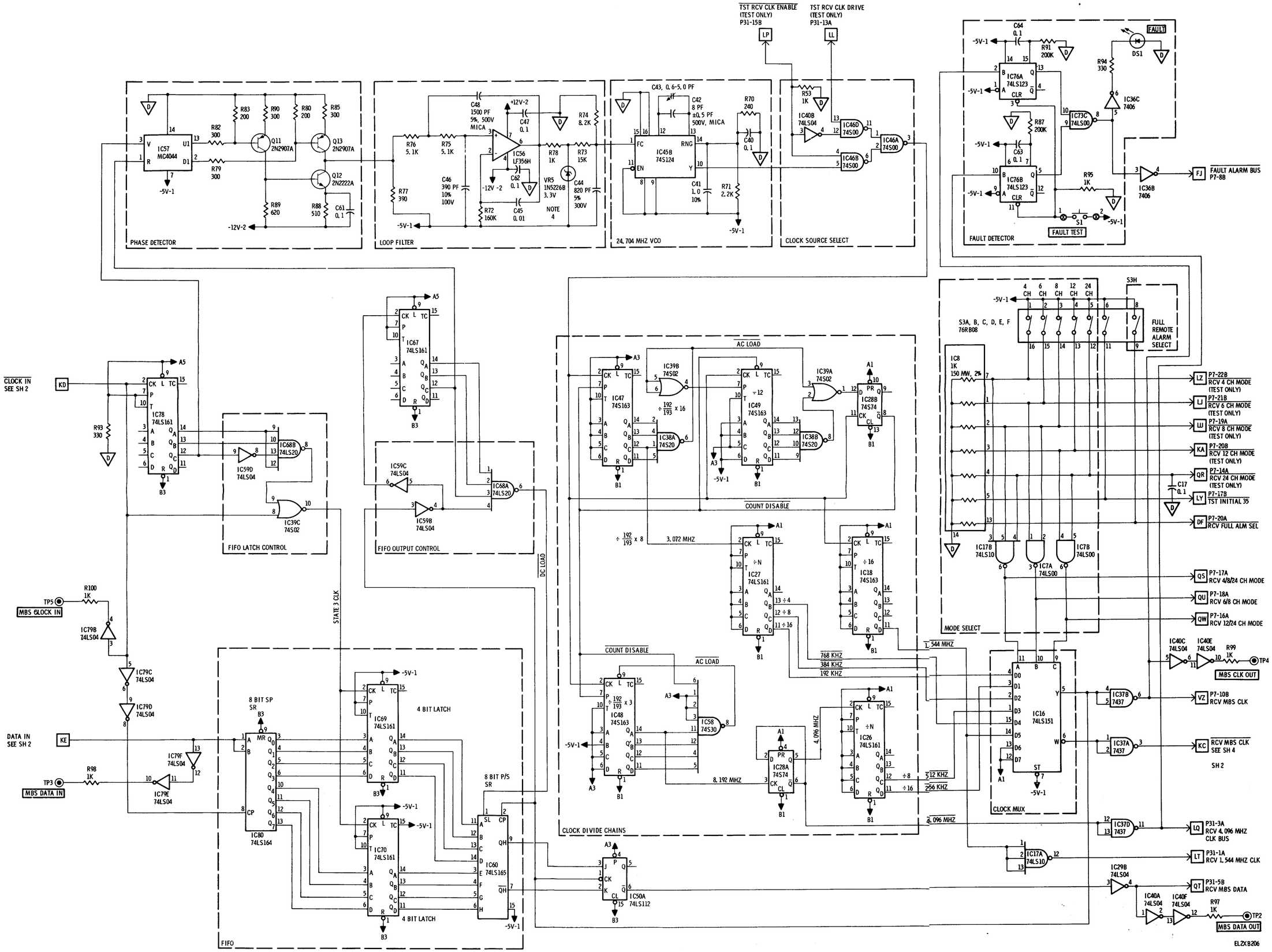


Figure FO-5. RCVR unit schematic (sheet 3 of 4

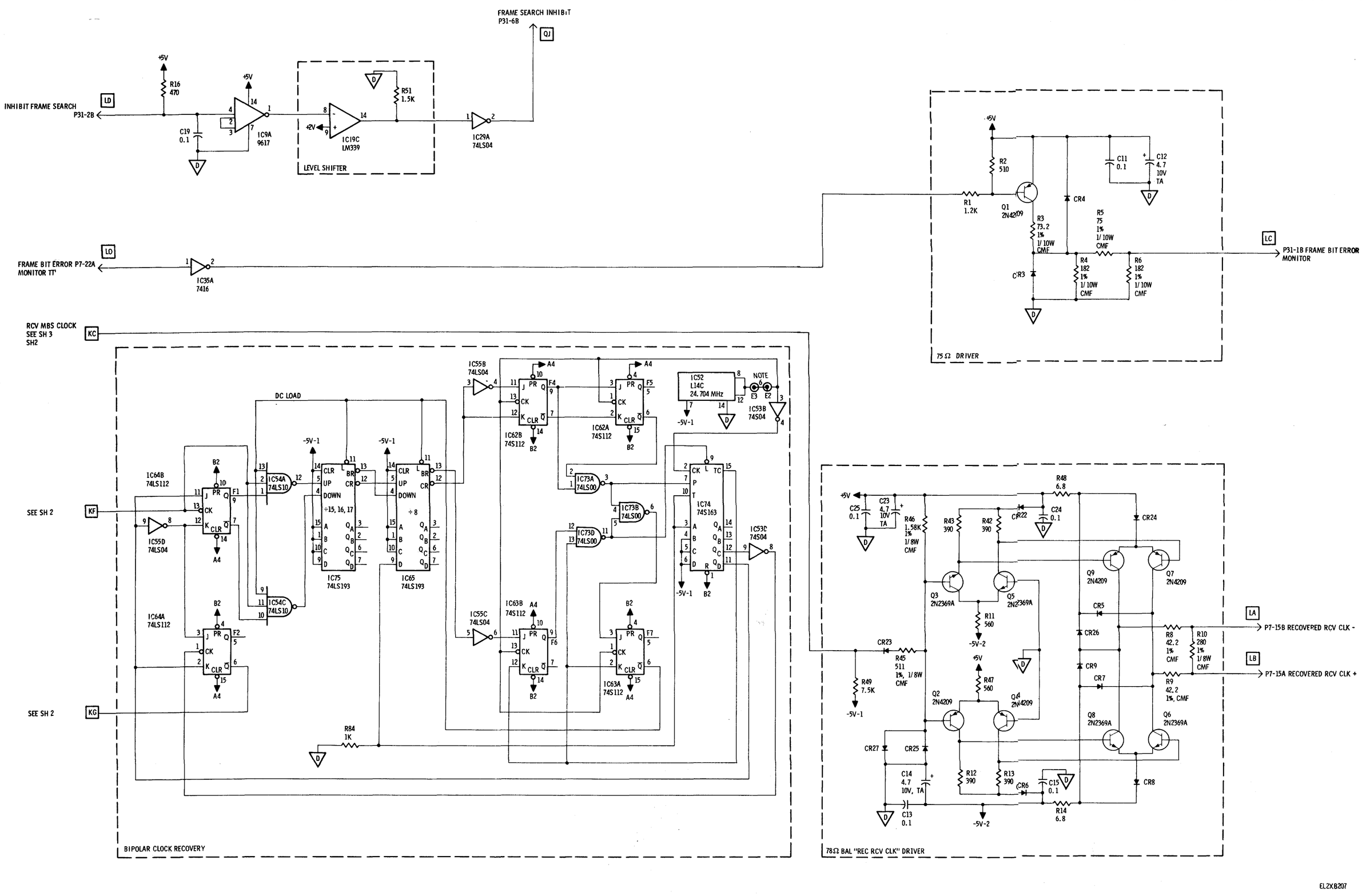
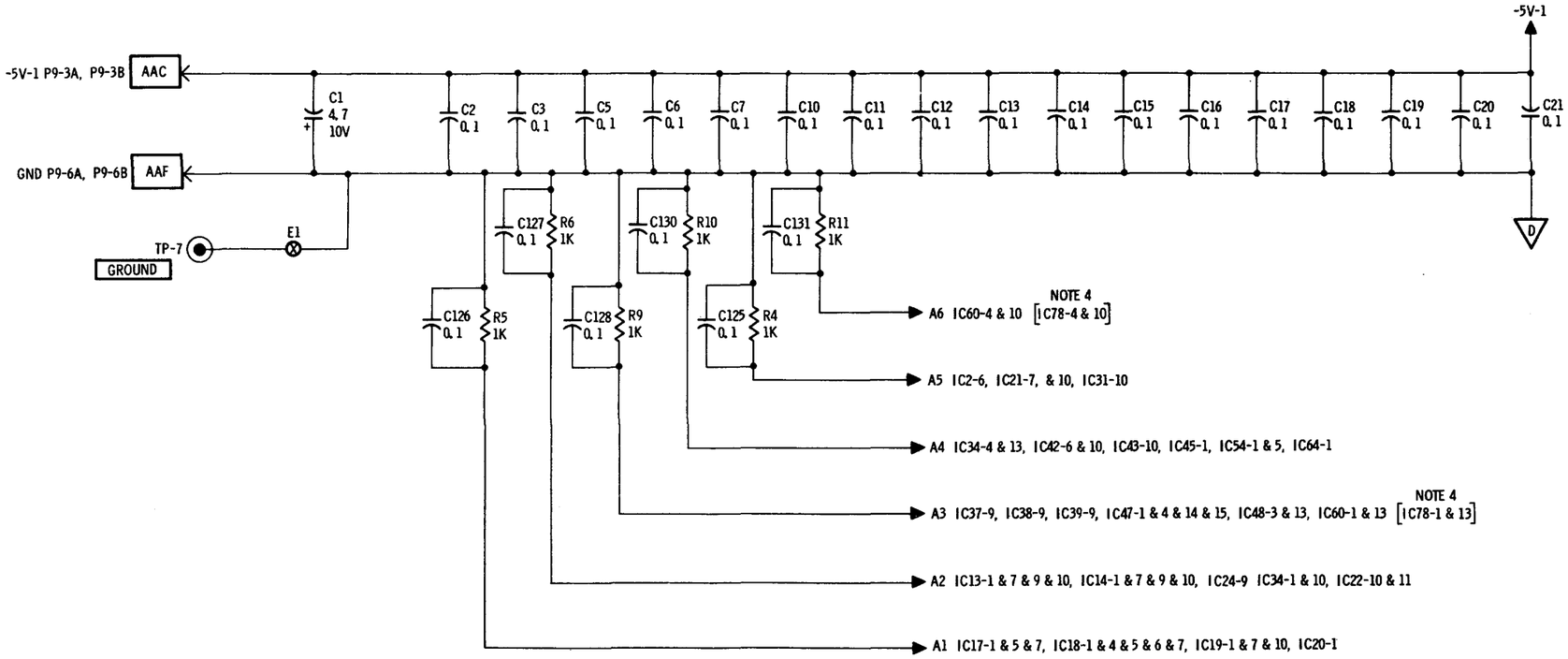
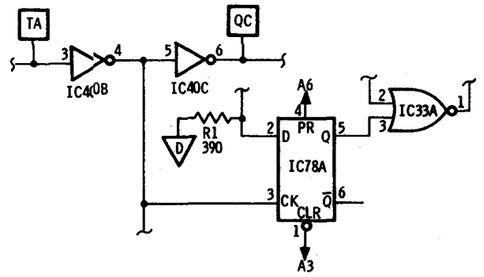


Figure FO-5. RCVR unit schematic (sheet 4 of 4)



NOTES: UNLESS OTHERWISE SPECIFIED

1. USE WITH ASSY 17485-010 & 17480-010
2. ALL RESISTORS VALUES ARE IN OHMS, ±5% 1/4W
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS ±20%, 50V
4. APPLIES TO CONFIGURATION DMX06 ONLY.
5. THE FOLLOWING CIRCUIT APPLIES TO CONFIGURATION DMX06 ONLY.



6. SYMBOL IDENTIFICATION:
   - ▽ D ▽ = DIGITAL GROUND
   - ⊙ = TEST POINT
   - ← = CONNECTOR PIN: A = SOLDER SIDE, B = COMP SIDE
   - [XXX] = FRONT PANEL NOMENCLATURE
   - ◎ = TERMINAL
   - ⊗ = WIRE CONNECTION POINT

EL2XB208

Figure FO-6. DEMUX unit schematic (sheet 1 of 3).

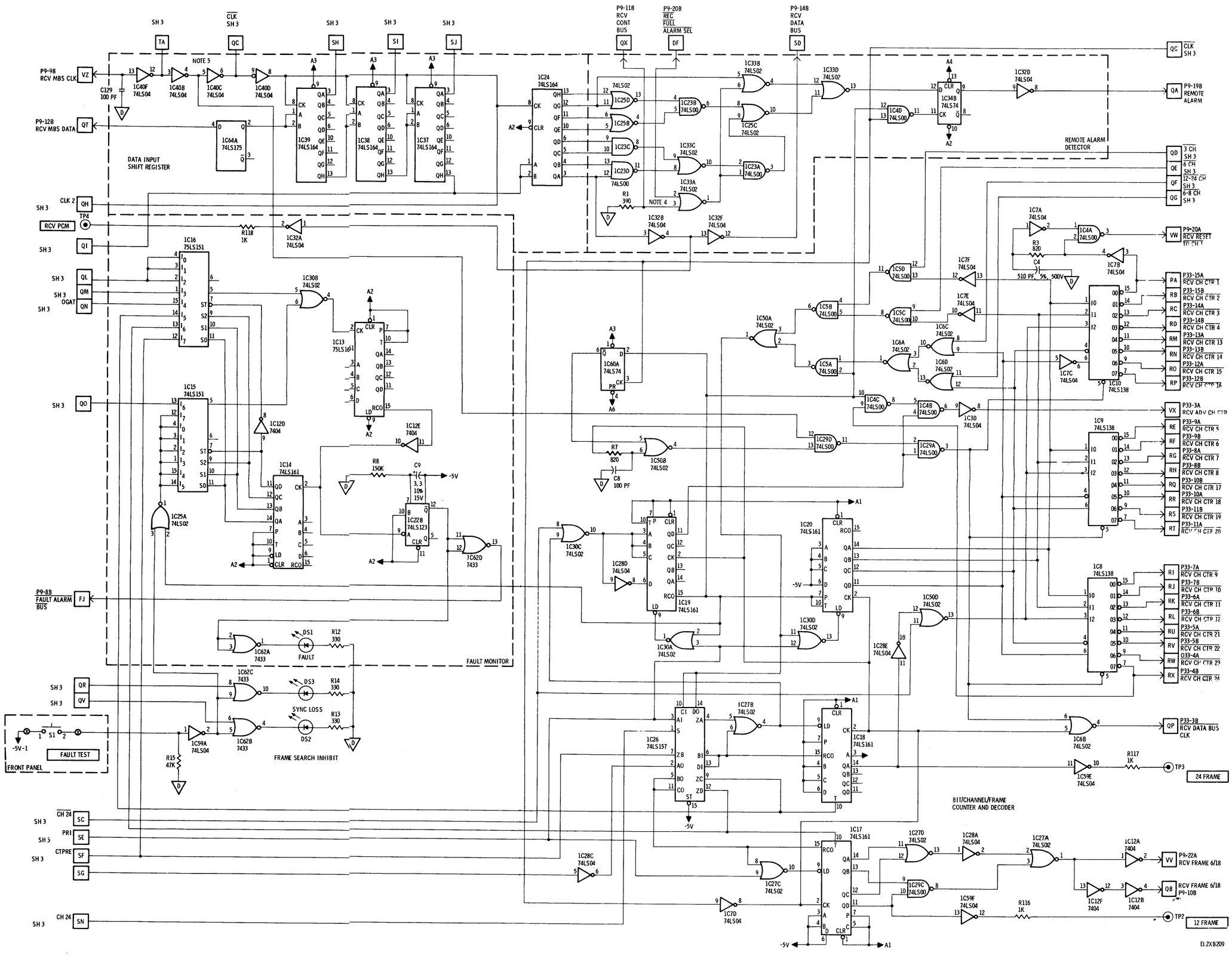


Figure FO-6. DEMUX unit schematic (sheet 2 of 3).

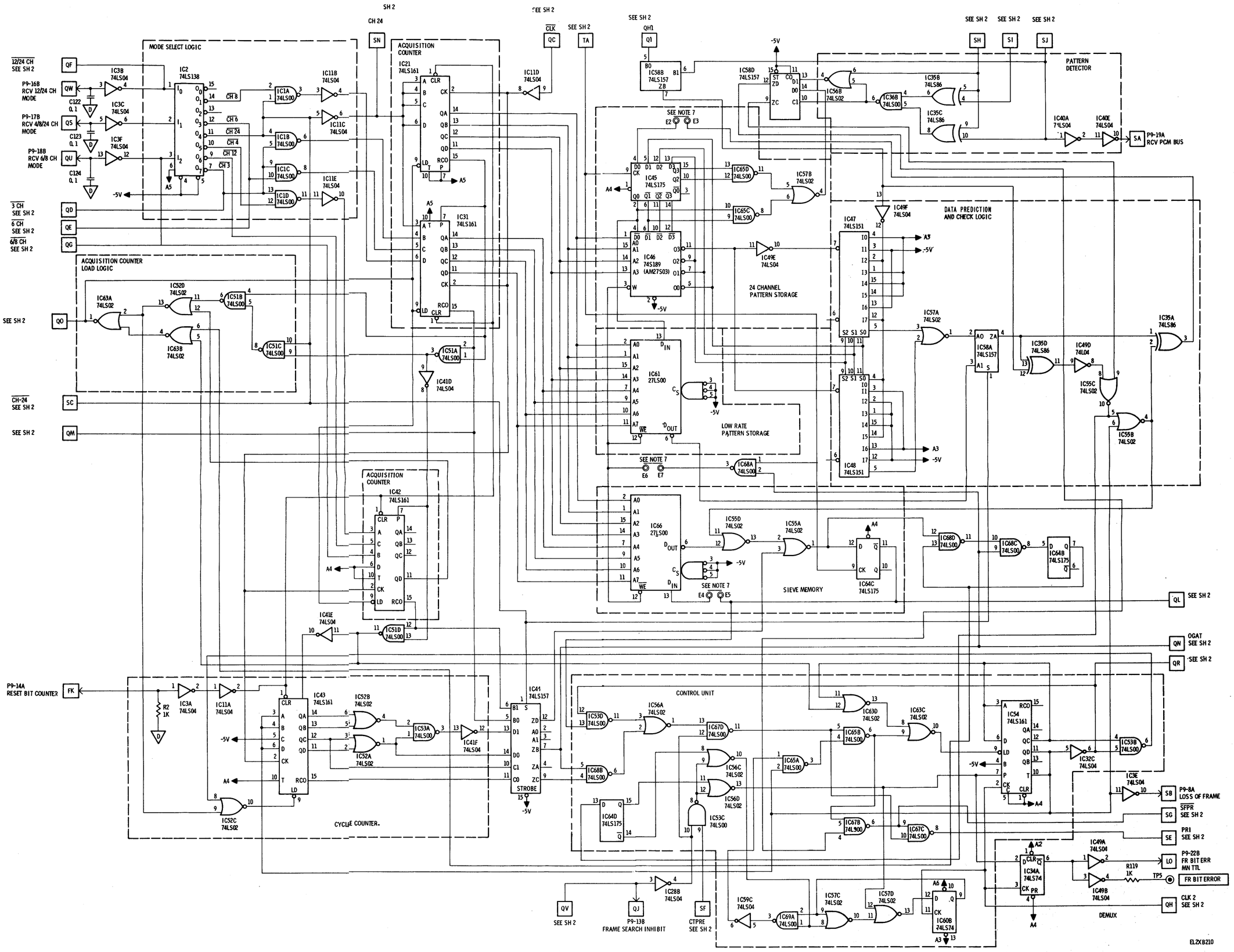


Figure FO-6. DEMUX unit schematic (sheet 3 of 3).

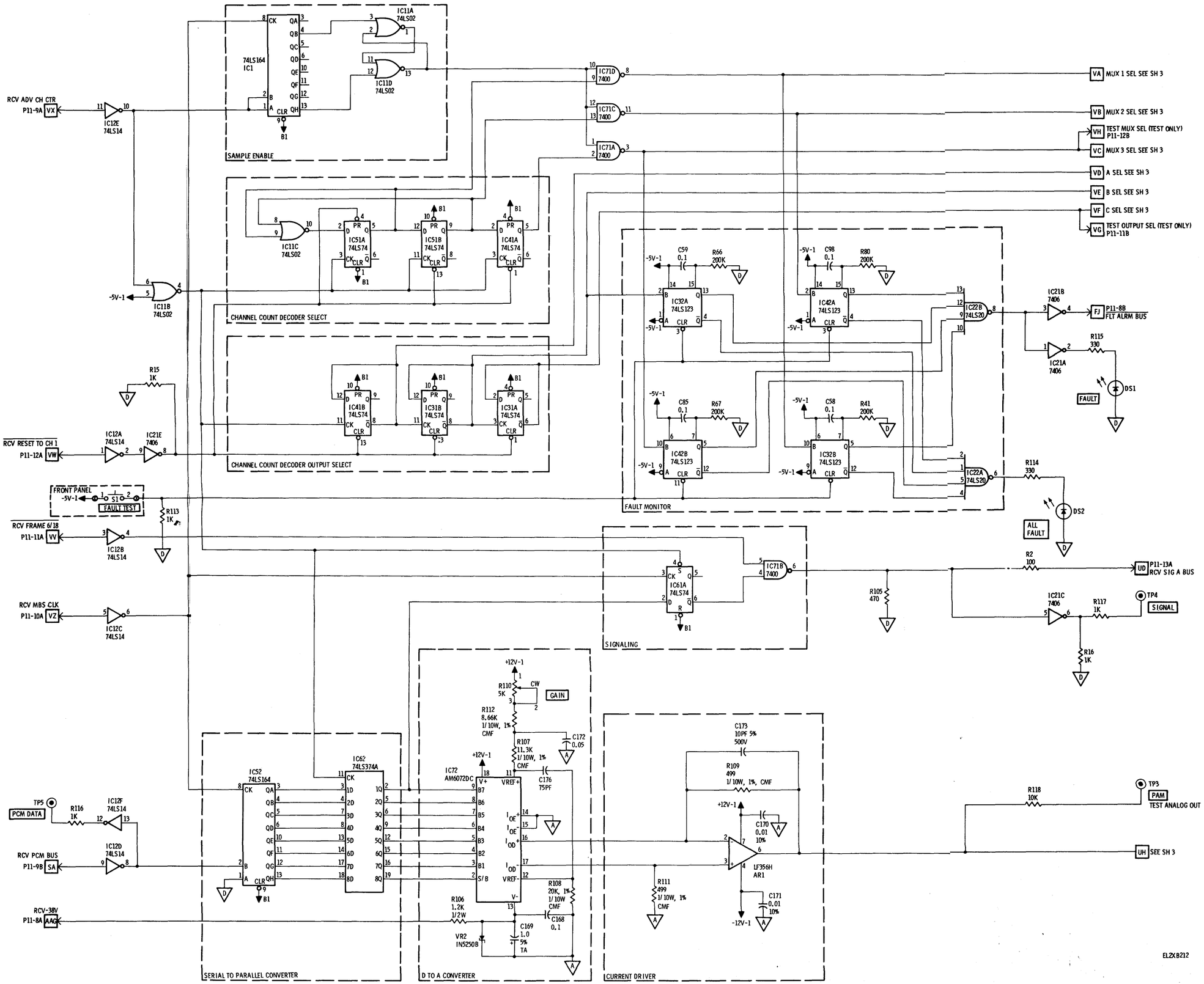
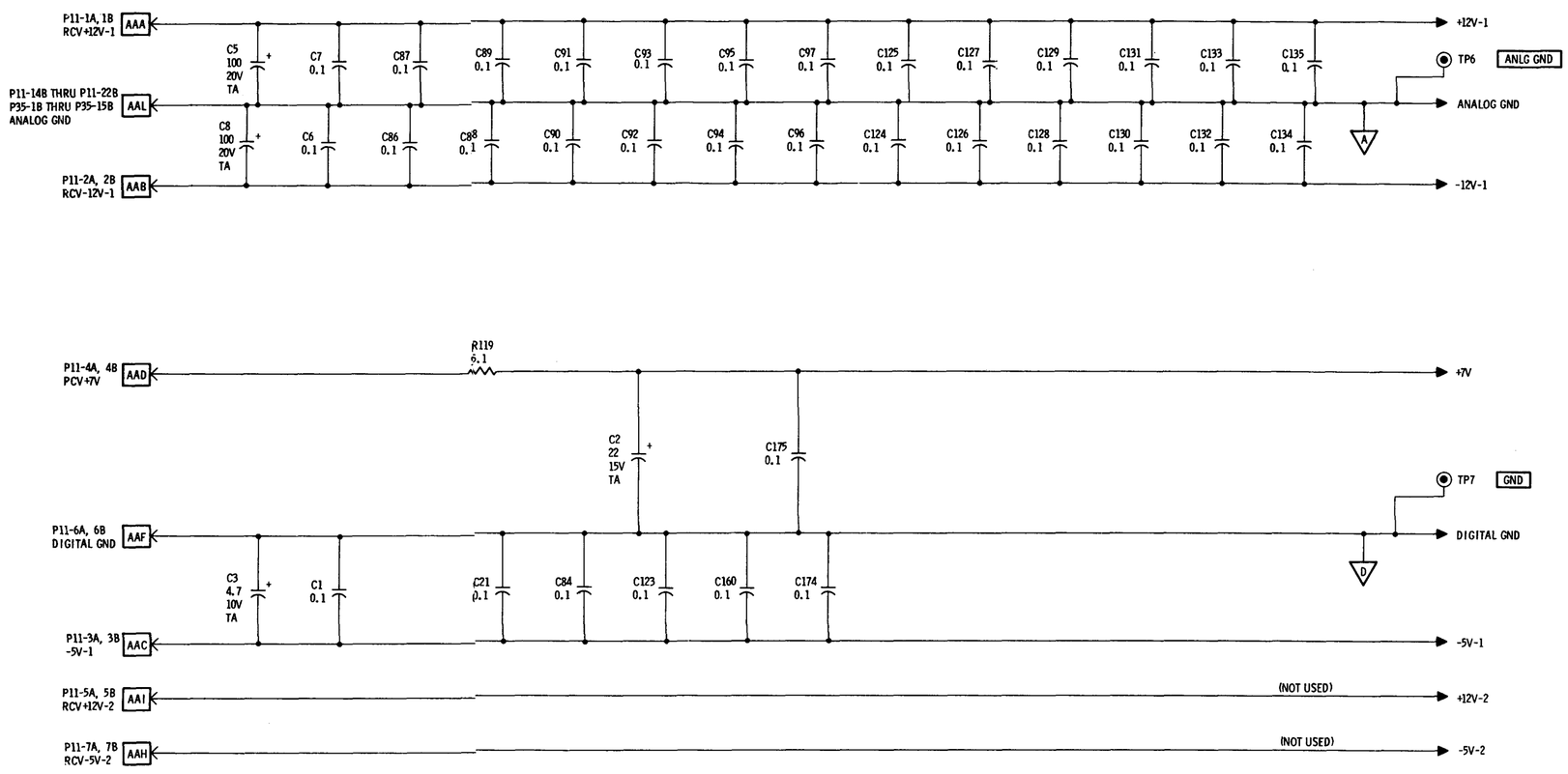


Figure FO-7. PCD unit schematic (sheet 1 of 4).



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%, CARBON
   ALL CAPACITORS ARE IN MICROFARADS, 20%, 50V, CERAMIC
2. SYMBOL IDENTIFICATION:

→ CONNECTOR PIN: A = SOLDER SIDE, B = COMPONENT SIDE

◉ TEST POINT

XXX FRONT PANEL NOMENCLATURE

D DIGITAL GROUND, TA = TANTALUM

A ANALOG GROUND, CMF = COATED METAL FILM

⊗ WIRING POINT

EL2XB211

Figure FO-7. PCD unit schematic (sheet 2 of 4).

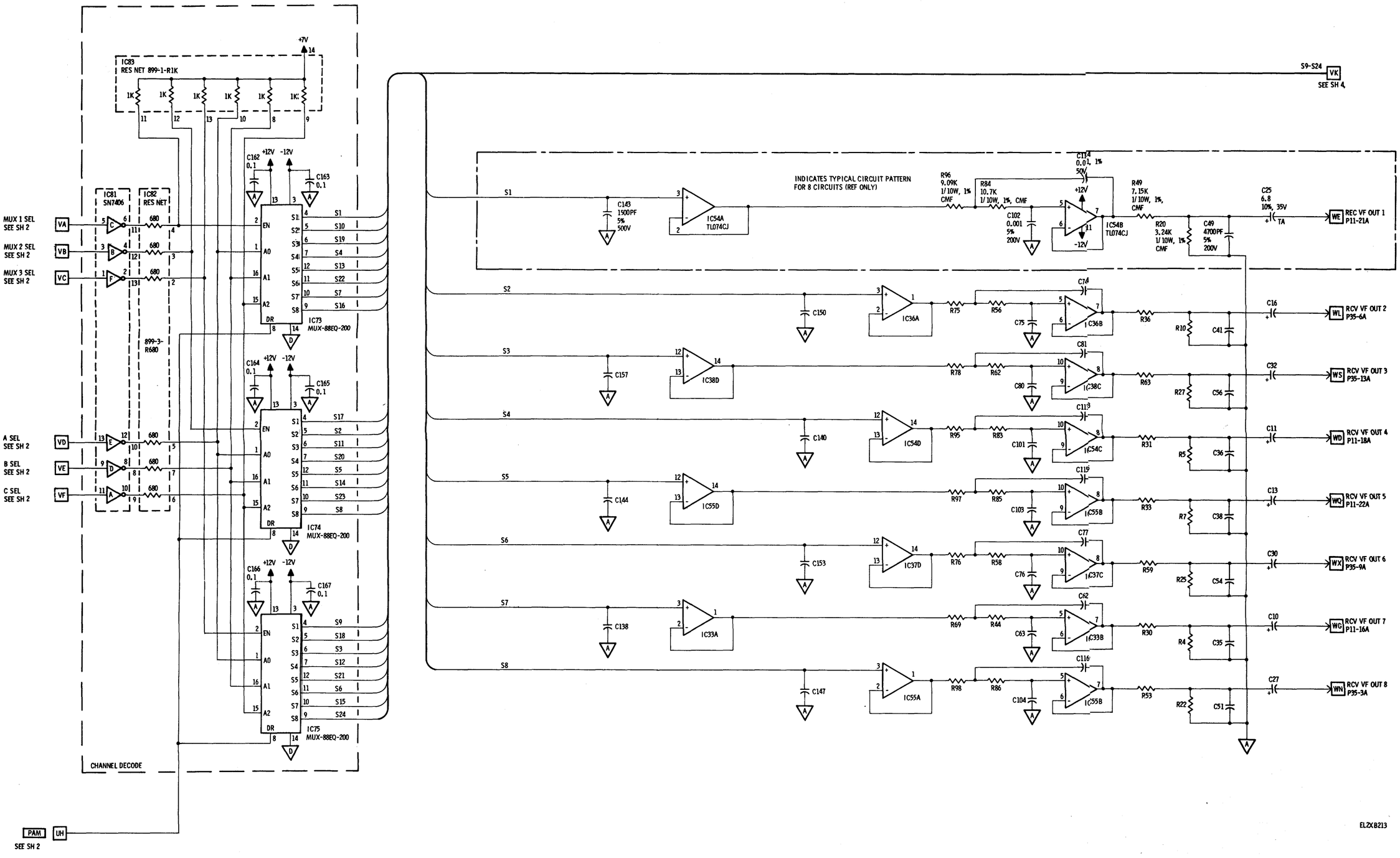


Figure FO-7. PCD unit schematic (sheet 3 of 4).

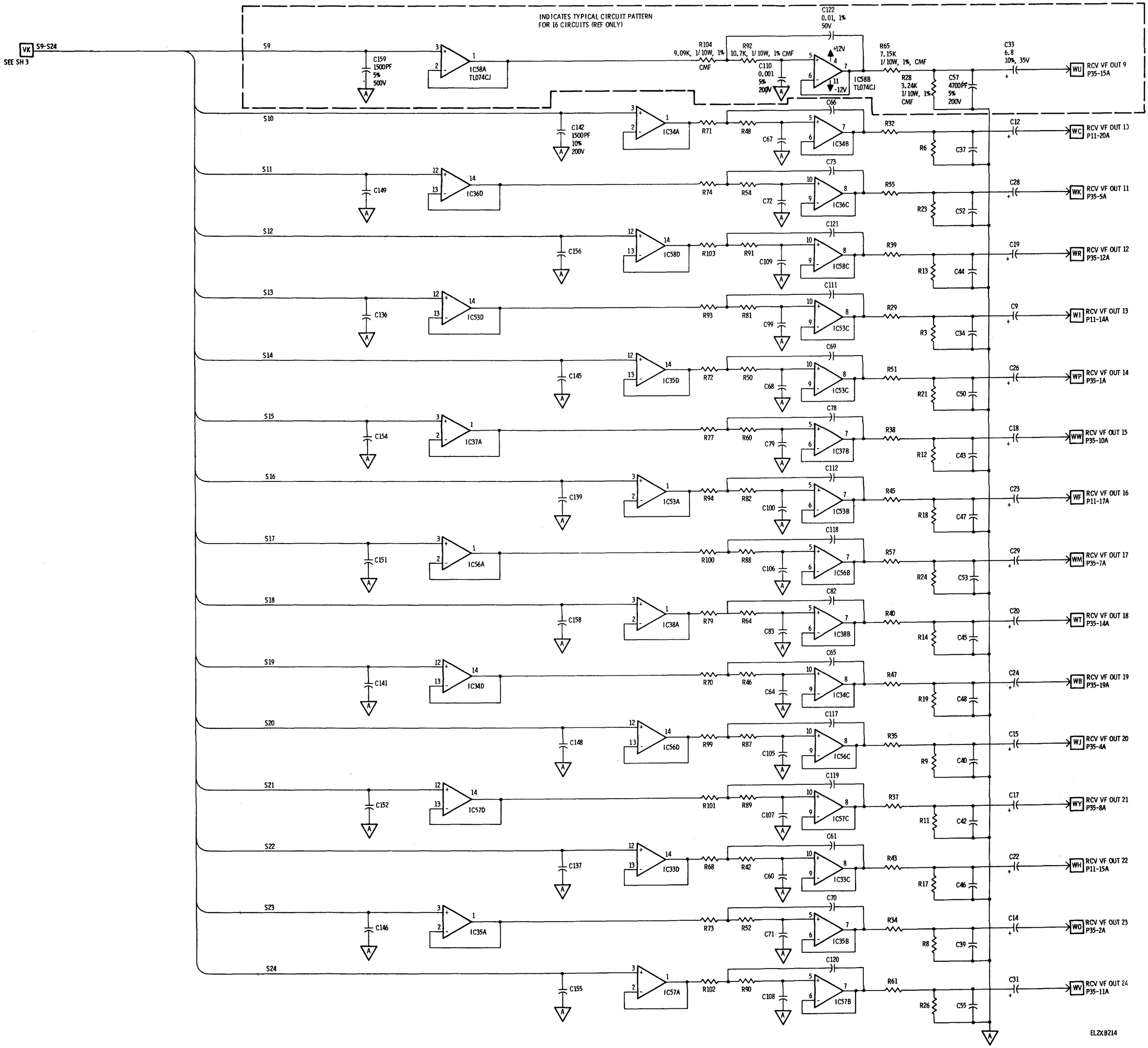
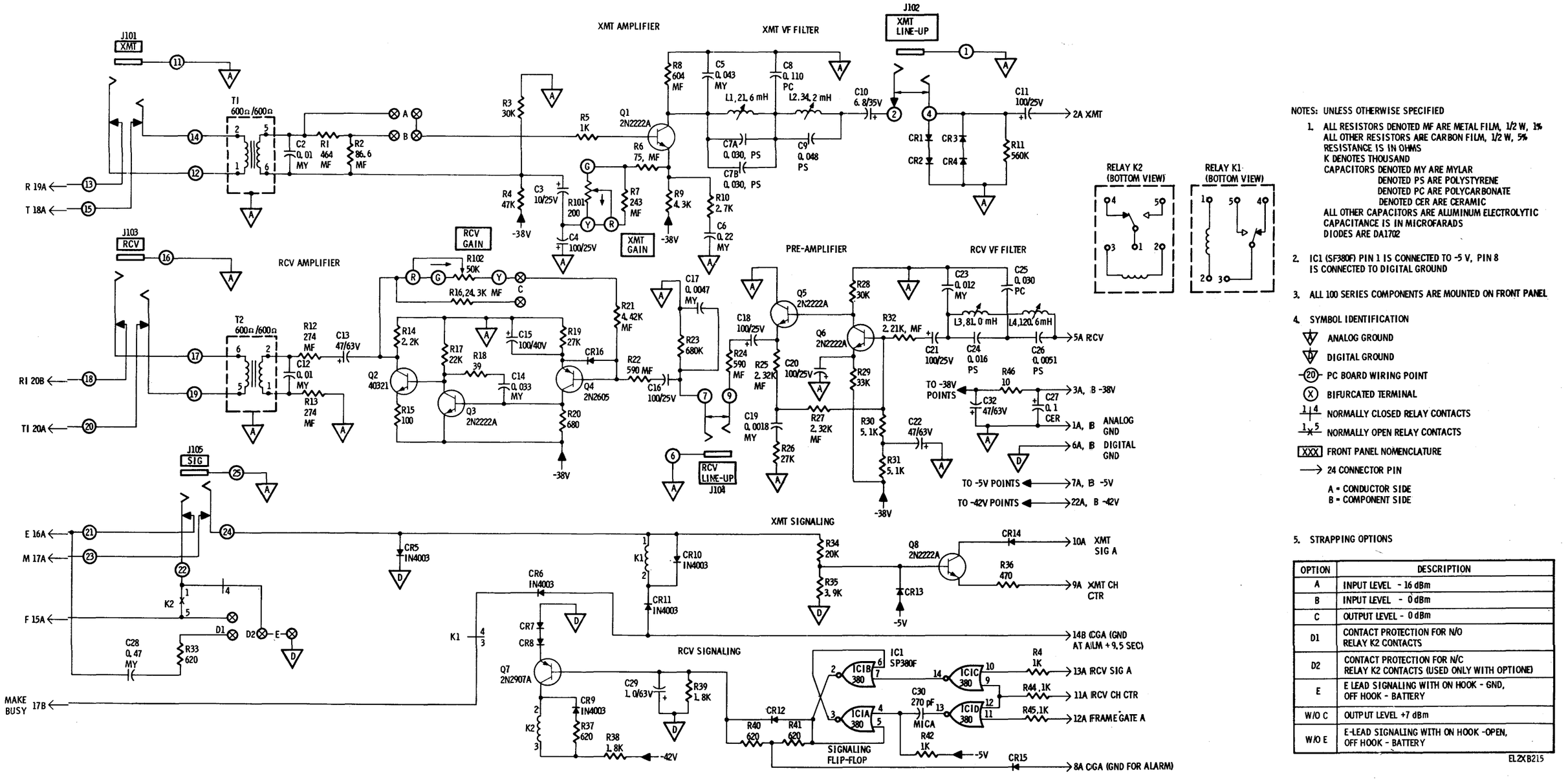


Figure FO-7. PCD unit schematic (sheet 4 of 4).



NOTES: UNLESS OTHERWISE SPECIFIED

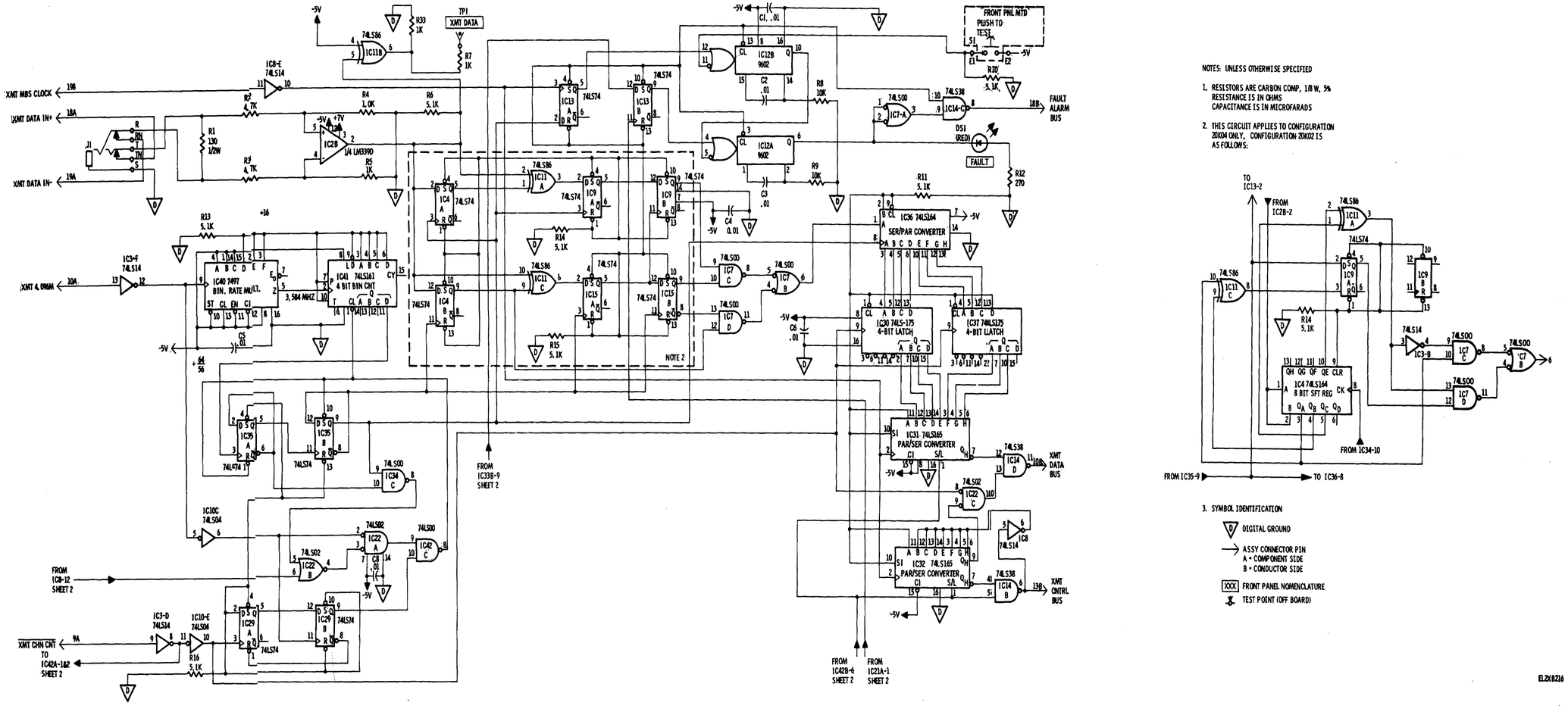
1. ALL RESISTORS DENOTED MF ARE METAL FILM, 1/2 W, 1%
   ALL OTHER RESISTORS ARE CARBON FILM, 1/2 W, 5%
   RESISTANCE IS IN OHMS
   K DENOTES THOUSAND
   CAPACITORS DENOTED MY ARE MYLAR
   DENOTED PS ARE POLYSTYRENE
   DENOTED PC ARE POLYCARBONATE
   DENOTED CER ARE CERAMIC
   ALL OTHER CAPACITORS ARE ALUMINUM ELECTROLYTIC
   CAPACITANCE IS IN MICROFARADS
   DIODES ARE DA1702
2. IC1 (SF380F) PIN 1 IS CONNECTED TO -5 V, PIN 8 IS CONNECTED TO DIGITAL GROUND
3. ALL 100 SERIES COMPONENTS ARE MOUNTED ON FRONT PANEL
4. SYMBOL IDENTIFICATION
   - ANALOG GROUND
   - DIGITAL GROUND
   - (20) PC BOARD WIRING POINT
   - (X) BIFURCATED TERMINAL
   - 1|4 NORMALLY CLOSED RELAY CONTACTS
   - 1×5 NORMALLY OPEN RELAY CONTACTS
   - XXX FRONT PANEL NOMENCLATURE
   - → 24 CONNECTOR PIN

     A = CONDUCTOR SIDE
     B = COMPONENT SIDE
5. STRAPPING OPTIONS

OPTION	DESCRIPTION
A	INPUT LEVEL - 16 dBm
B	INPUT LEVEL - 0 dBm
C	OUTPUT LEVEL - 0 dBm
D1	CONTACT PROTECTION FOR N/O RELAY K2 CONTACTS
D2	CONTACT PROTECTION FOR N/C RELAY K2 CONTACTS (USED ONLY WITH OPTION E)
E	E LEAD SIGNALING WITH ON HOOK - GND, OFF HOOK - BATTERY
W/O C	OUTPUT LEVEL +7 dBm
W/O E	E-LEAD SIGNALING WITH ON HOOK -OPEN, OFF HOOK - BATTERY

EL2XB215

Figure FO-8. VF. Module schematic.



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE CARBON COMP, 1/8 W, 5% RESISTANCE IS IN OHMS CAPACITANCE IS IN MICROFARADS
2. THIS CIRCUIT APPLIES TO CONFIGURATION 20K04 ONLY. CONFIGURATION 20K02 IS AS FOLLOWS:

3. SYMBOL IDENTIFICATION
   - DIGITAL GROUND
   - ASSY CONNECTOR PIN A = COMPONENT SIDE B = CONDUCTOR SIDE
   - XXX FRONT PANEL NOMENCLATURE
   - TEST POINT (OFF BOARD)

EL2X(8Z)16

Figure FO-9. 0-20 Kb/s data module schematic (sheet 1 of 2).

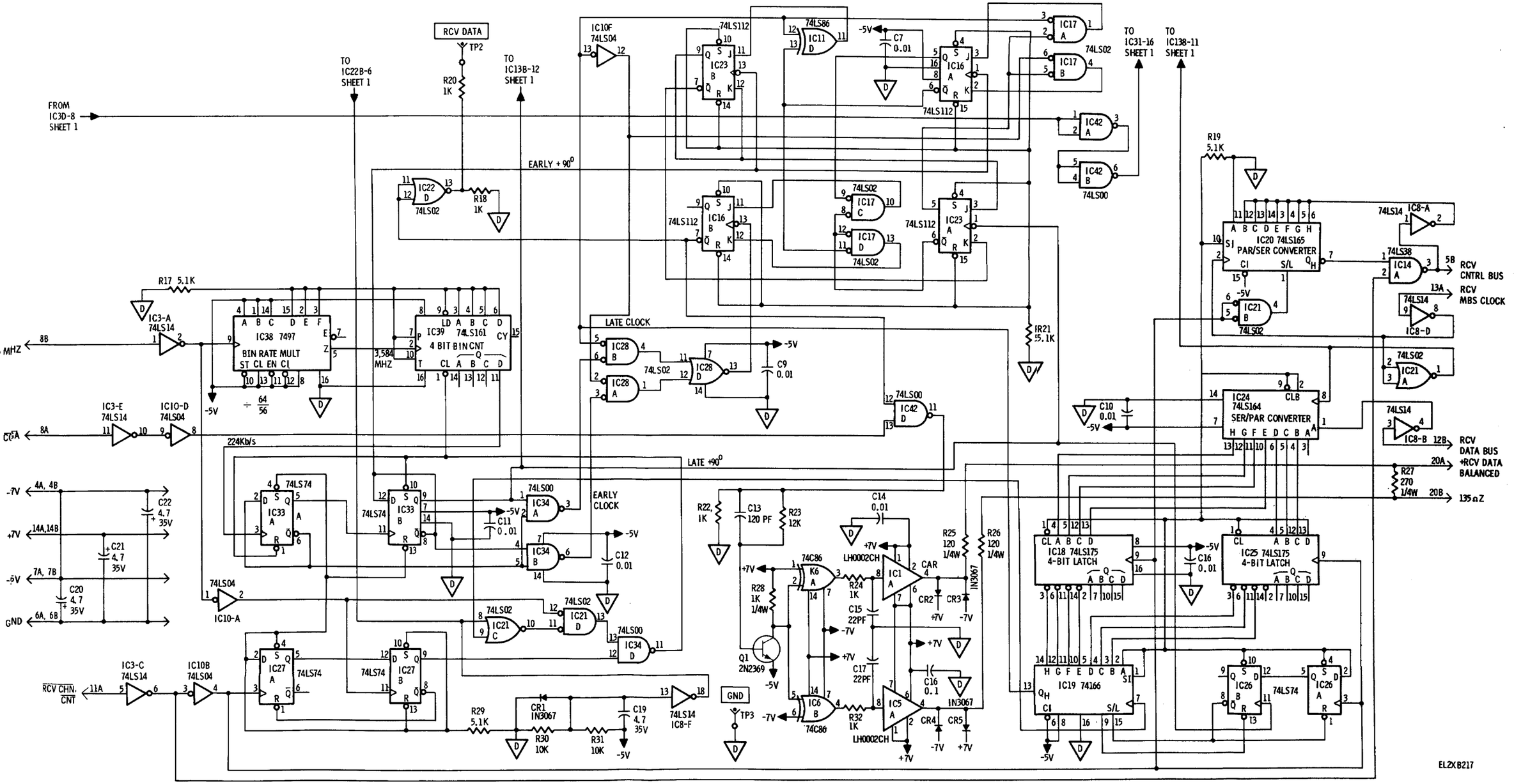
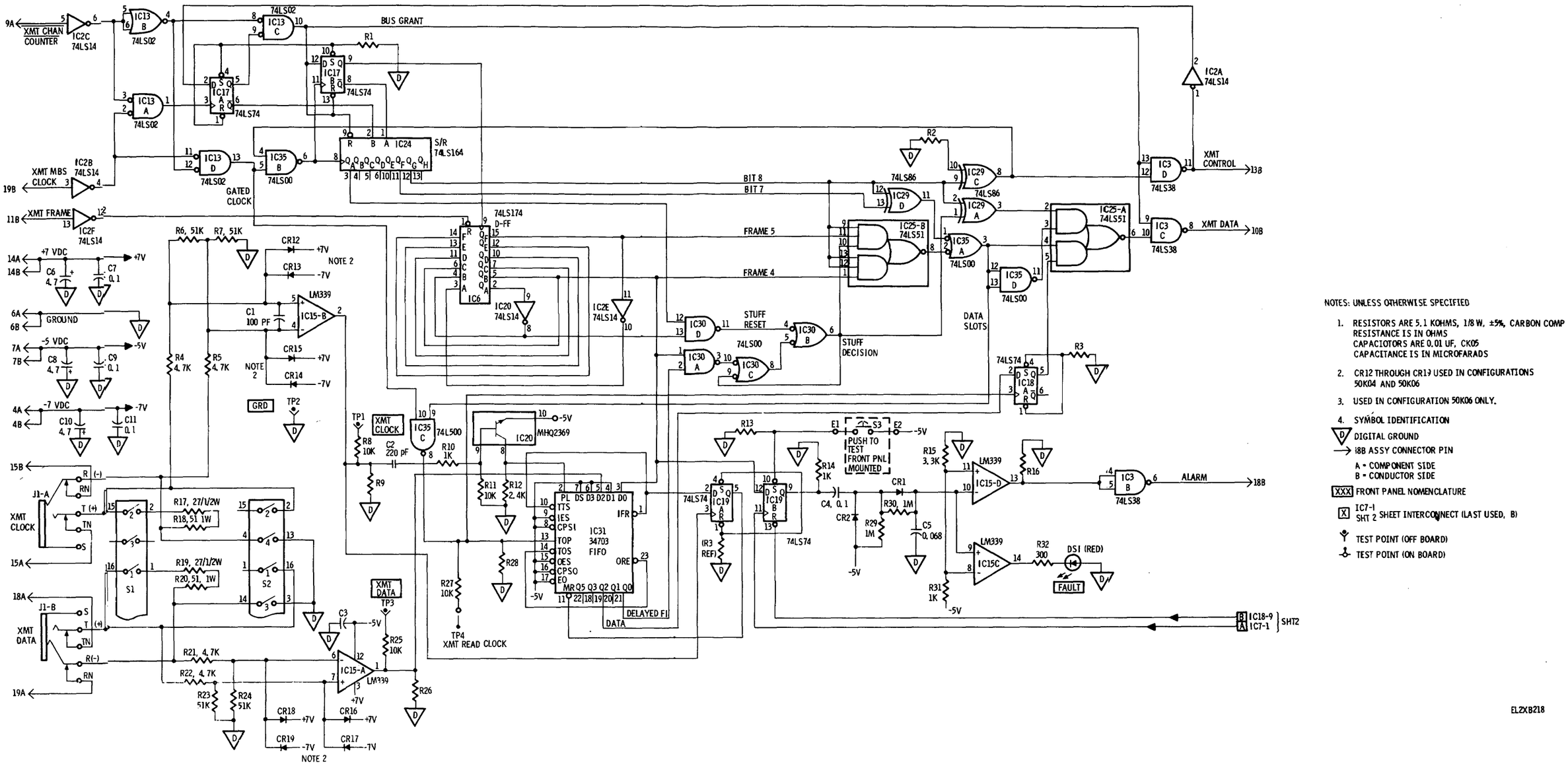


Figure FO-9. 0-20 Kb/s data module schematic (sheet 2 of 2)



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE 5.1 KOHMS, 1/8 W, ±5%, CARBON COMP
   RESISTANCE IS IN OHMS
   CAPACIOTORS ARE 0.01 UF, CK05
   CAPACITANCE IS IN MICROFARADS
2. CR12 THROUGH CR19 USED IN CONFIGURATIONS 50K04 AND 50K06
3. USED IN CONFIGURATION 50K06 ONLY.
4. SYMBOL IDENTIFICATION

D DIGITAL GROUND

→ I8B ASSY CONNECTOR PIN
A = COMPONENT SIDE
B = CONDUCTOR SIDE

XXX FRONT PANEL NOMENCLATURE

X IC7-1 SHT 2 SHEET INTERCONNECT (LAST USED, B)

TEST POINT (OFF BOARD)

TEST POINT (ON BOARD)

EL2XB218

Figure FO-10. 0-50 Kb/s data module schematic (sheet 1 of 2).

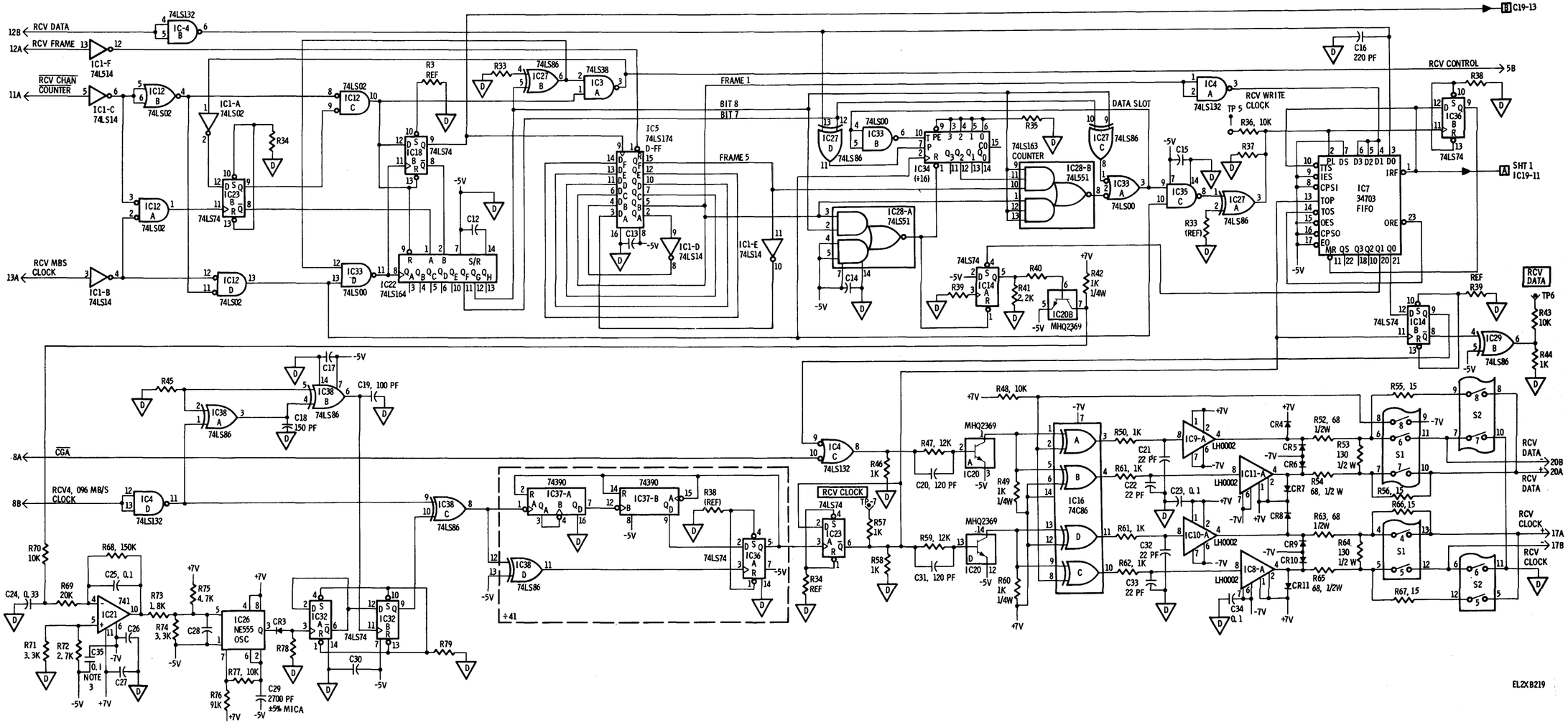


Figure FO-10. 0-50 Kb/s data module schematic (sheet 2 of 2).

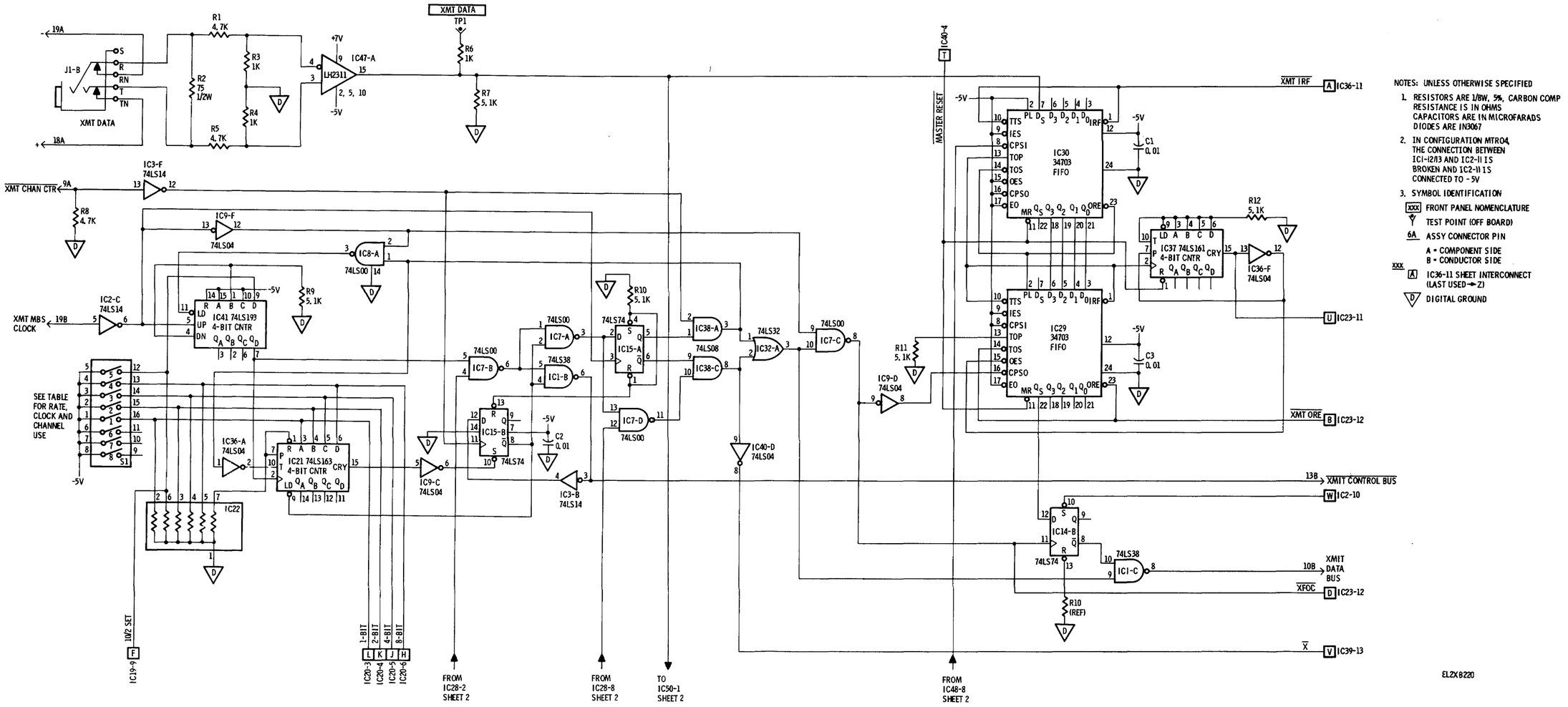


Figure FO-11. Multirate data module schematic (sheet 1 of 4).

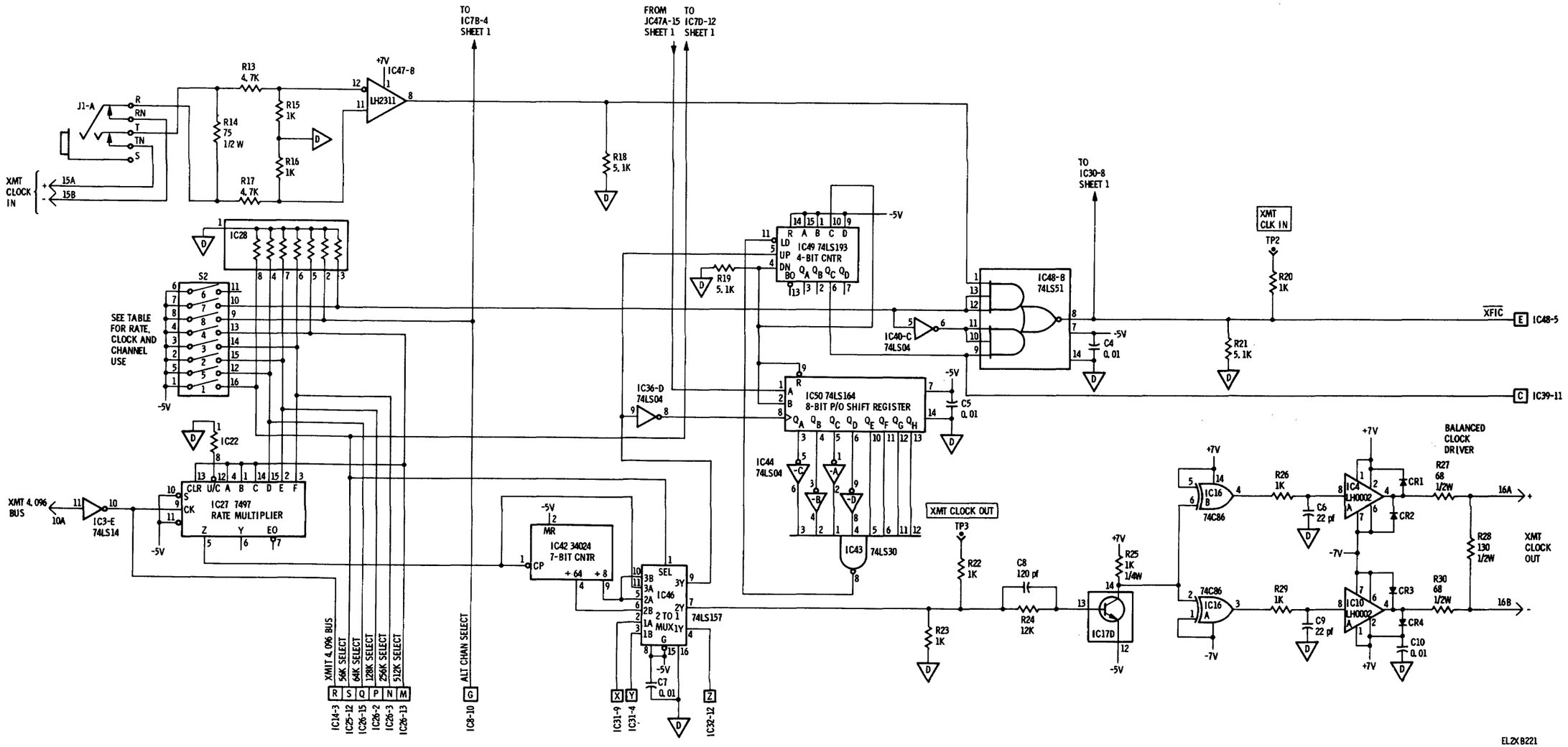


Figure FO-11. Multirate data module schematic (sheet 2 of 4).

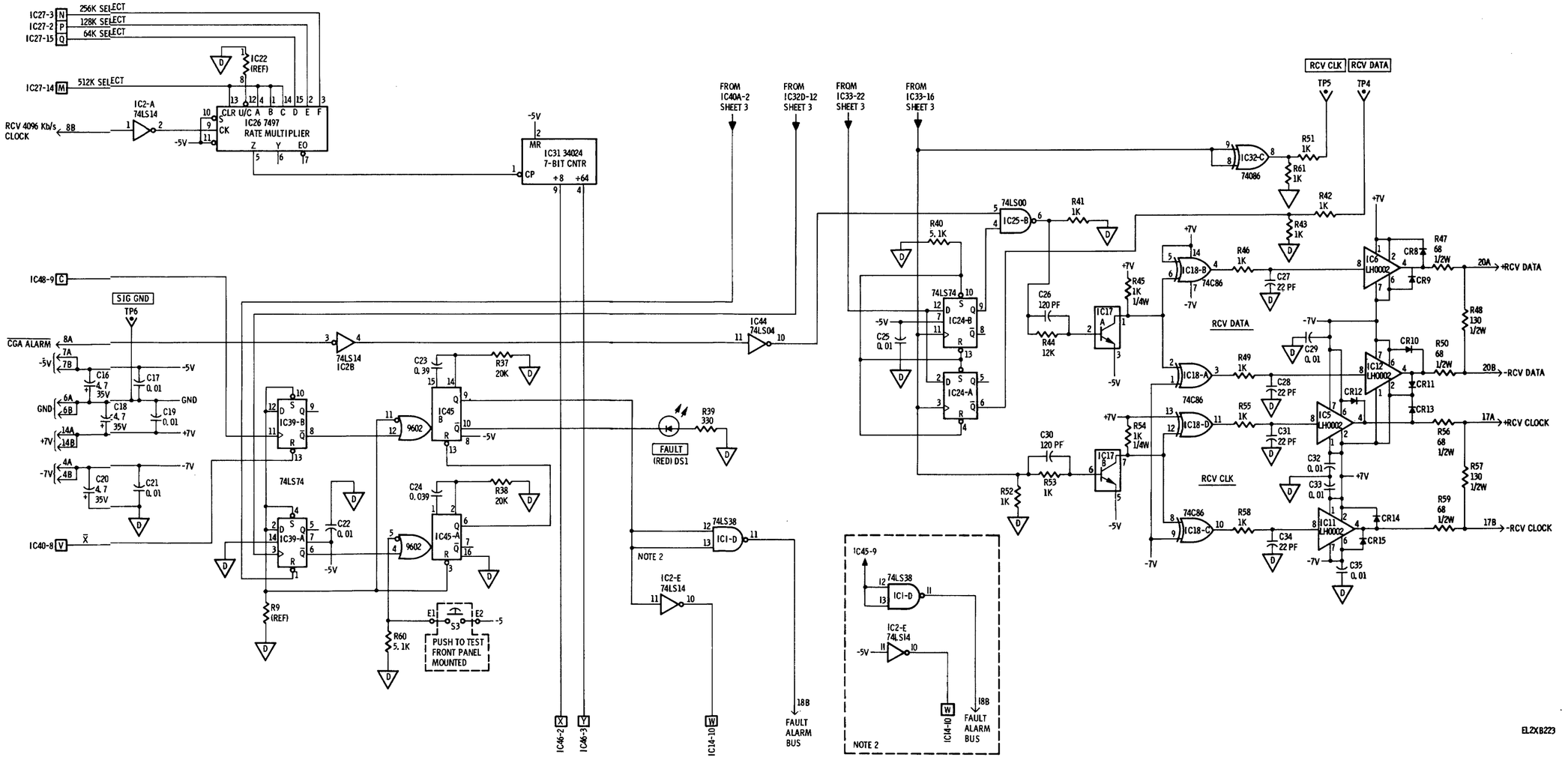


Figure FO-11. Multirate data module schematic (sheet 3 of 4).

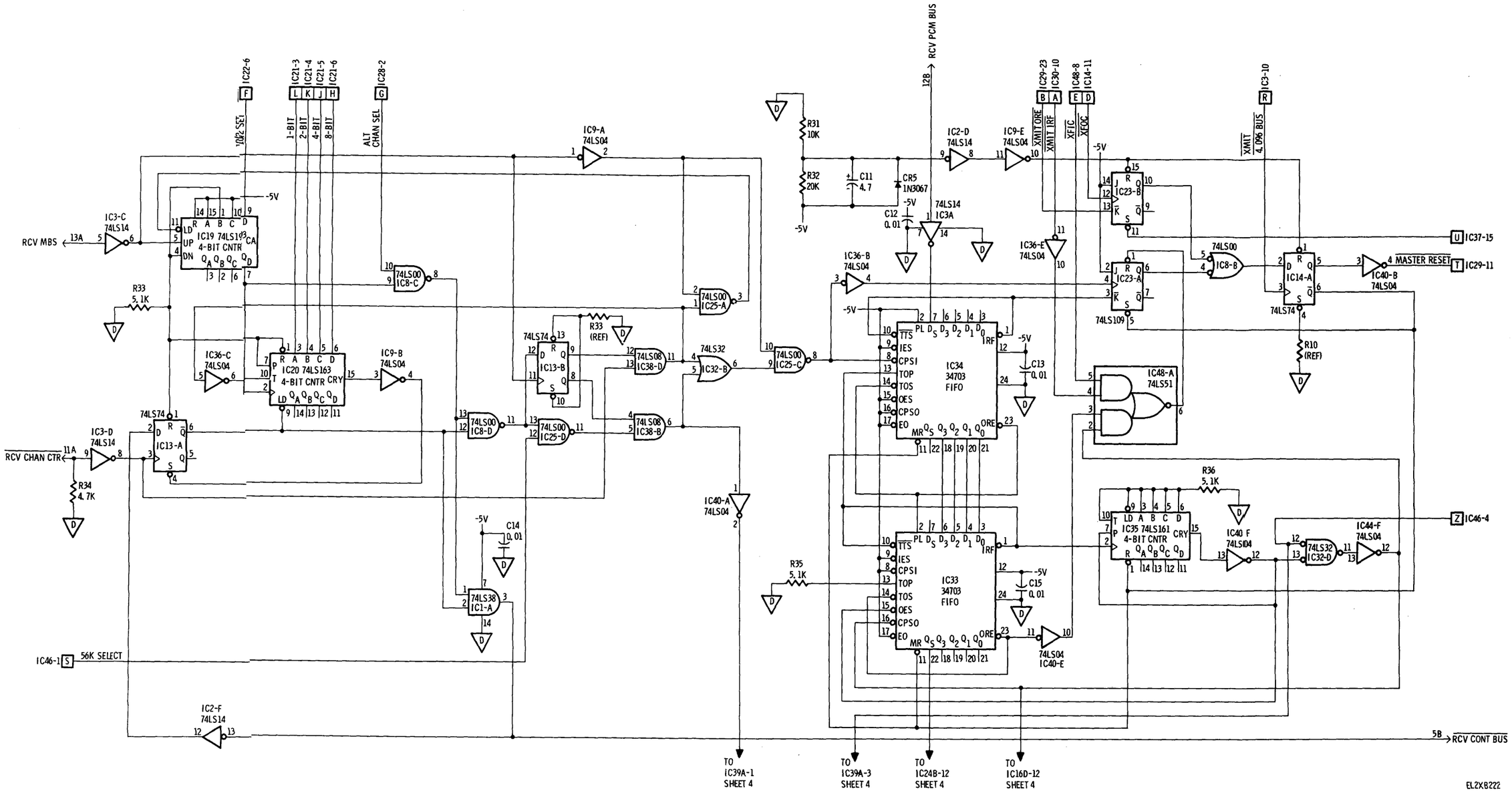
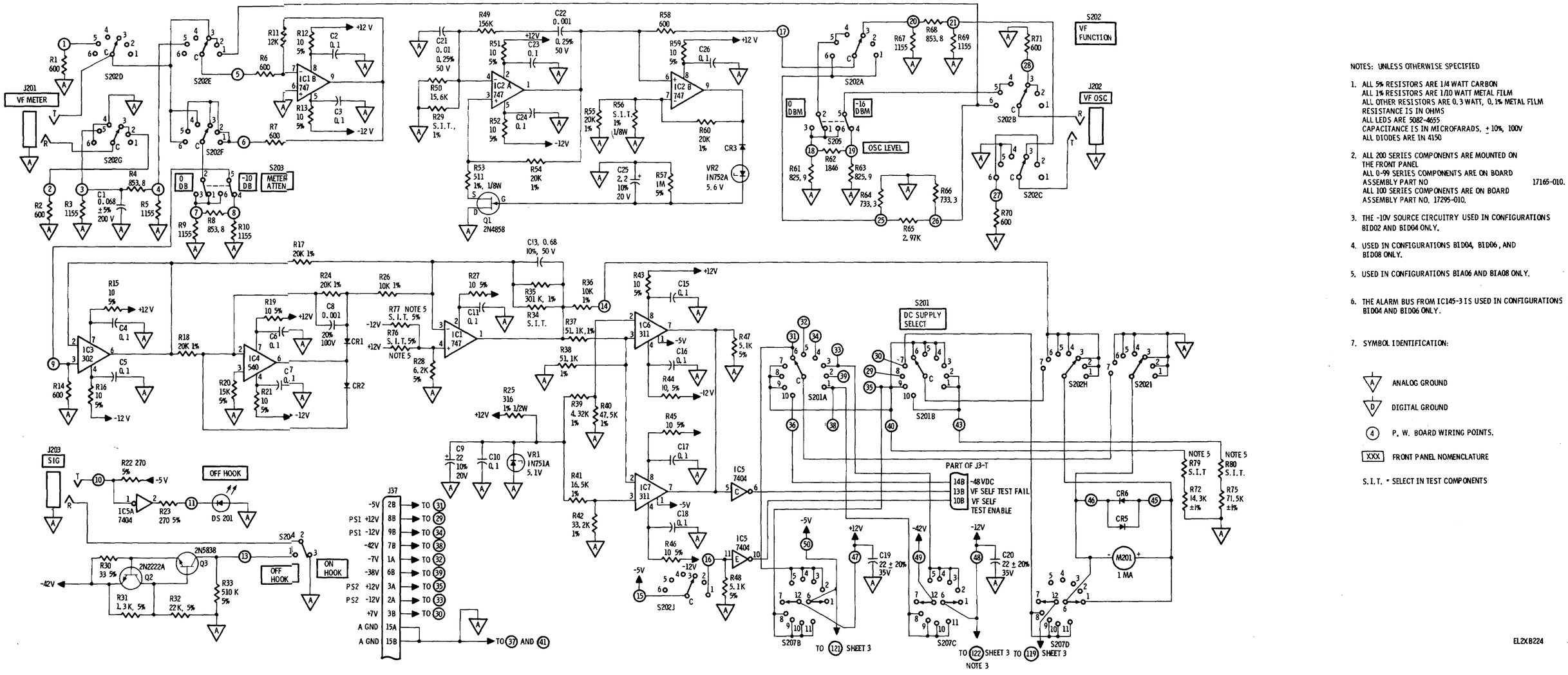


Figure FO-11. Multirate data module schematic (sheet 4 of 4).



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL 5% RESISTORS ARE 1/4 WATT CARBON
   ALL 1% RESISTORS ARE 1/10 WATT METAL FILM
   ALL OTHER RESISTORS ARE 0.3 WATT, 0.1% METAL FILM
   RESISTANCE IS IN OHMS
   ALL LEDS ARE 5082-4655
   CAPACITANCE IS IN MICROFARADS, ±10%, 100V
   ALL DIODES ARE IN 4150

2. ALL 200 SERIES COMPONENTS ARE MOUNTED ON THE FRONT PANEL
   ALL 0-99 SERIES COMPONENTS ARE ON BOARD ASSEMBLY PART NO 17165-010.
   ALL 100 SERIES COMPONENTS ARE ON BOARD ASSEMBLY PART NO. 17295-010.

3. THE -10V SOURCE CIRCUITRY USED IN CONFIGURATIONS BID02 AND BID04 ONLY.

4. USED IN CONFIGURATIONS BID04, BID06, AND BID08 ONLY.

5. USED IN CONFIGURATIONS BIA06 AND BIA08 ONLY.

6. THE ALARM BUS FROM IC145-3 IS USED IN CONFIGURATIONS BID04 AND BID06 ONLY.

7. SYMBOL IDENTIFICATION:

   ▽A ANALOG GROUND
   ▽D DIGITAL GROUND
   (4) P. W. BOARD WIRING POINTS.
   XXX FRONT PANEL NOMENCLATURE

S.I.T. = SELECT IN TEST COMPONENTS

EL2XB224

Figure FO-12. BITE Module schematic (sheet 1 of 3).

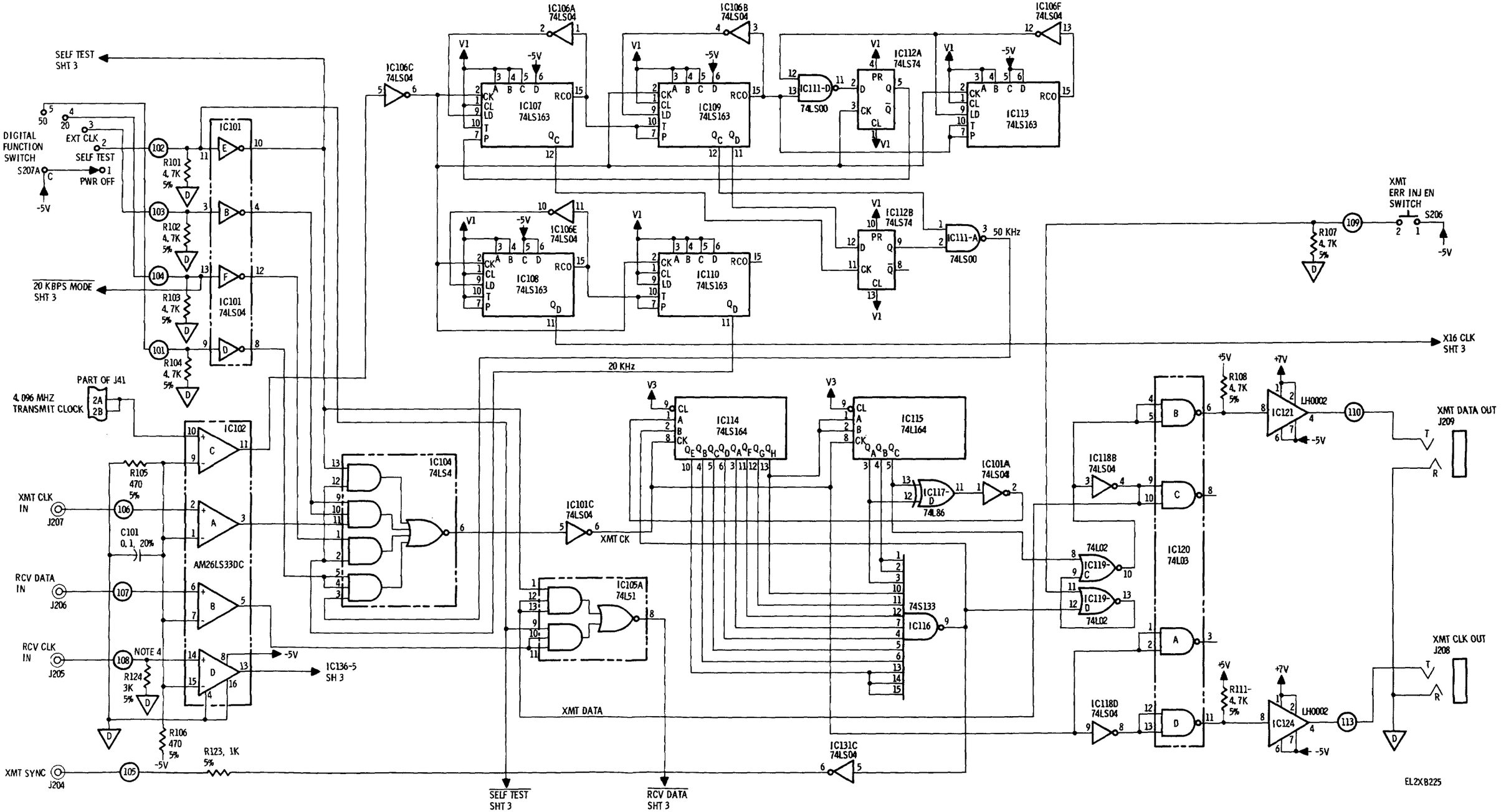


Figure FO-12. BITE module schematic (sheet 2 of 3).

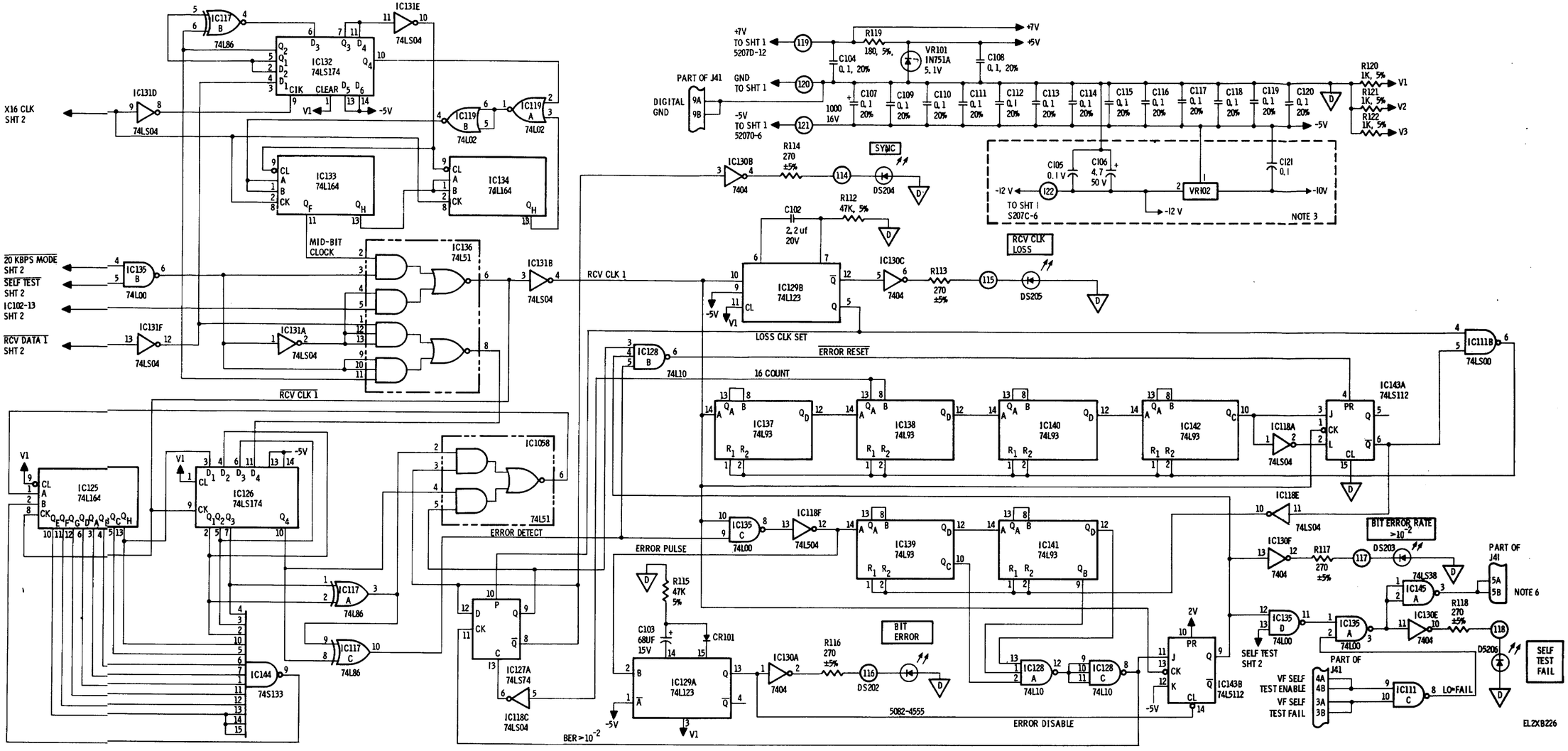
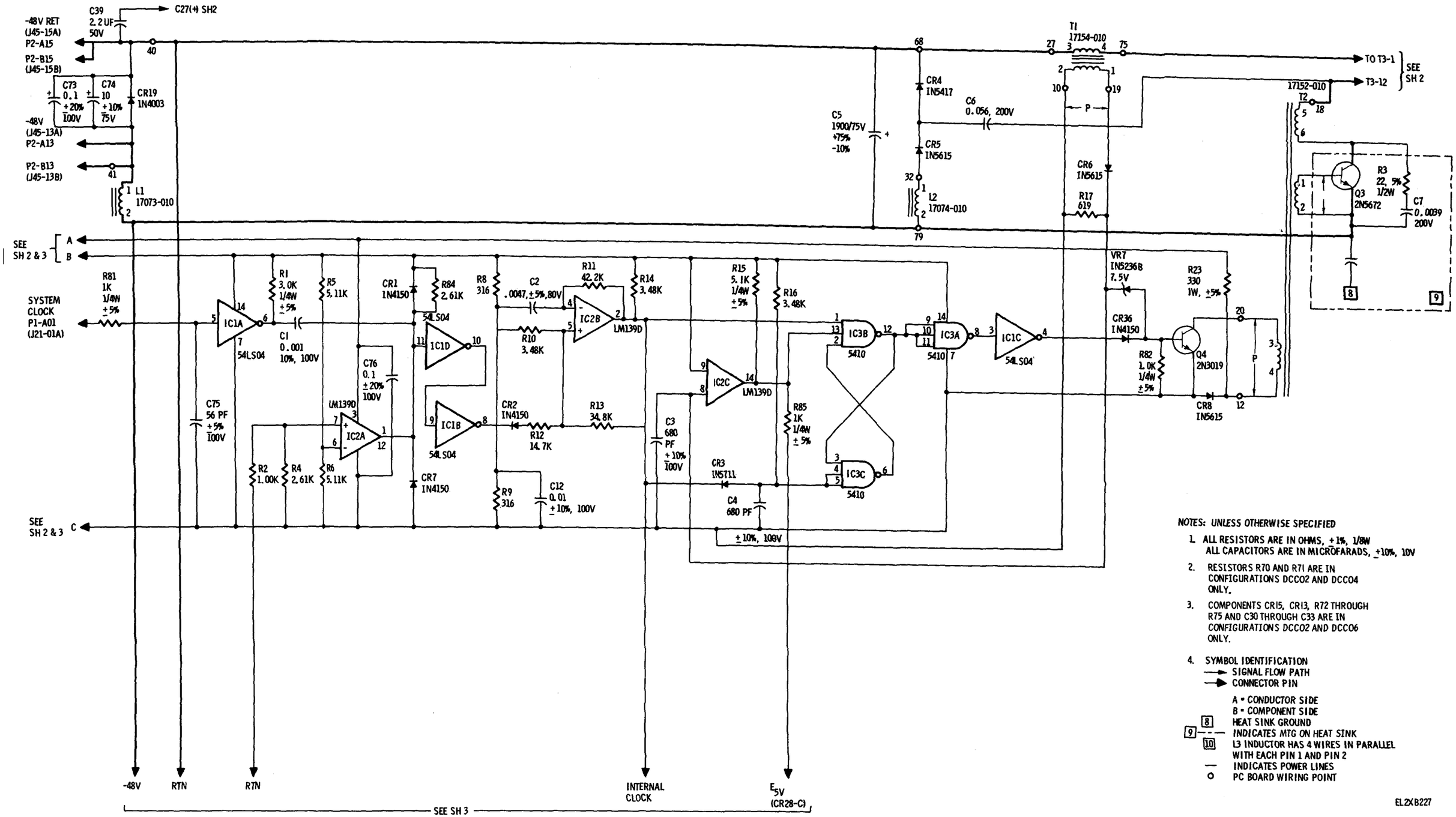


Figure FO-12. BITE module schematic (sheet 3 of 3).



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±1%, 1/8W
   ALL CAPACITORS ARE IN MICROFARADS, ±10%, 10V
2. RESISTORS R70 AND R71 ARE IN CONFIGURATIONS DCC02 AND DCC04 ONLY.
3. COMPONENTS CR15, CR13, R72 THROUGH R75 AND C30 THROUGH C33 ARE IN CONFIGURATIONS DCC02 AND DCC06 ONLY.
4. SYMBOL IDENTIFICATION
   - SIGNAL FLOW PATH
   - CONNECTOR PIN
   - A = CONDUCTOR SIDE
   - B = COMPONENT SIDE
   - [8] HEAT SINK GROUND
   - [9] INDICATES MTG ON HEAT SINK
   - [10] L3 INDUCTOR HAS 4 WIRES IN PARALLEL WITH EACH PIN 1 AND PIN 2
   - INDICATES POWER LINES
   - PC BOARD WIRING POINT

EL2XB227

Figure FO-13. PWR SPLY unit (dc converter assembly) schematic (sheet 1 of 3).

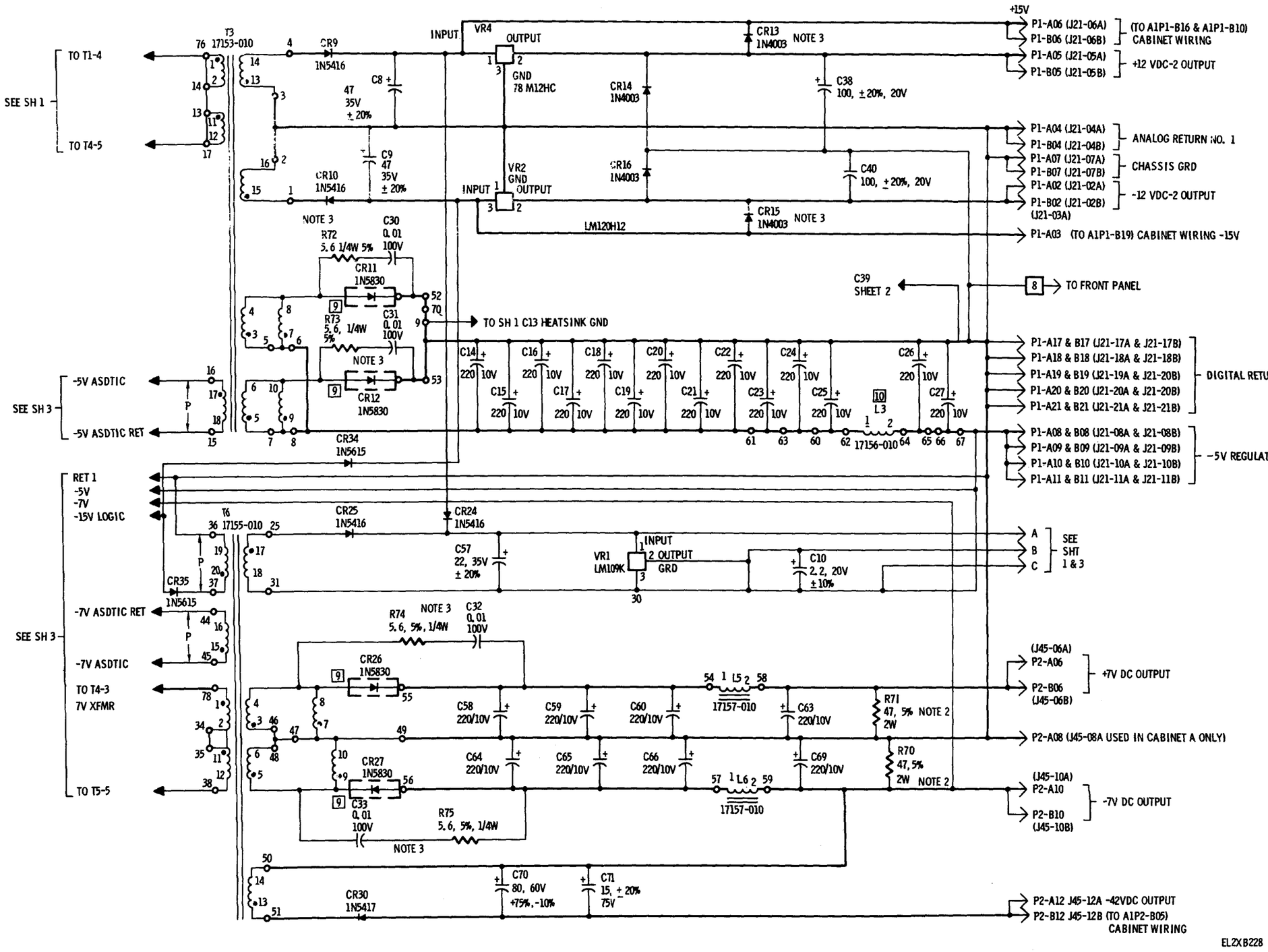


Figure FO-13. PWR SPLY unit (dc converter assembly) schematic (sheet 2 of 3).

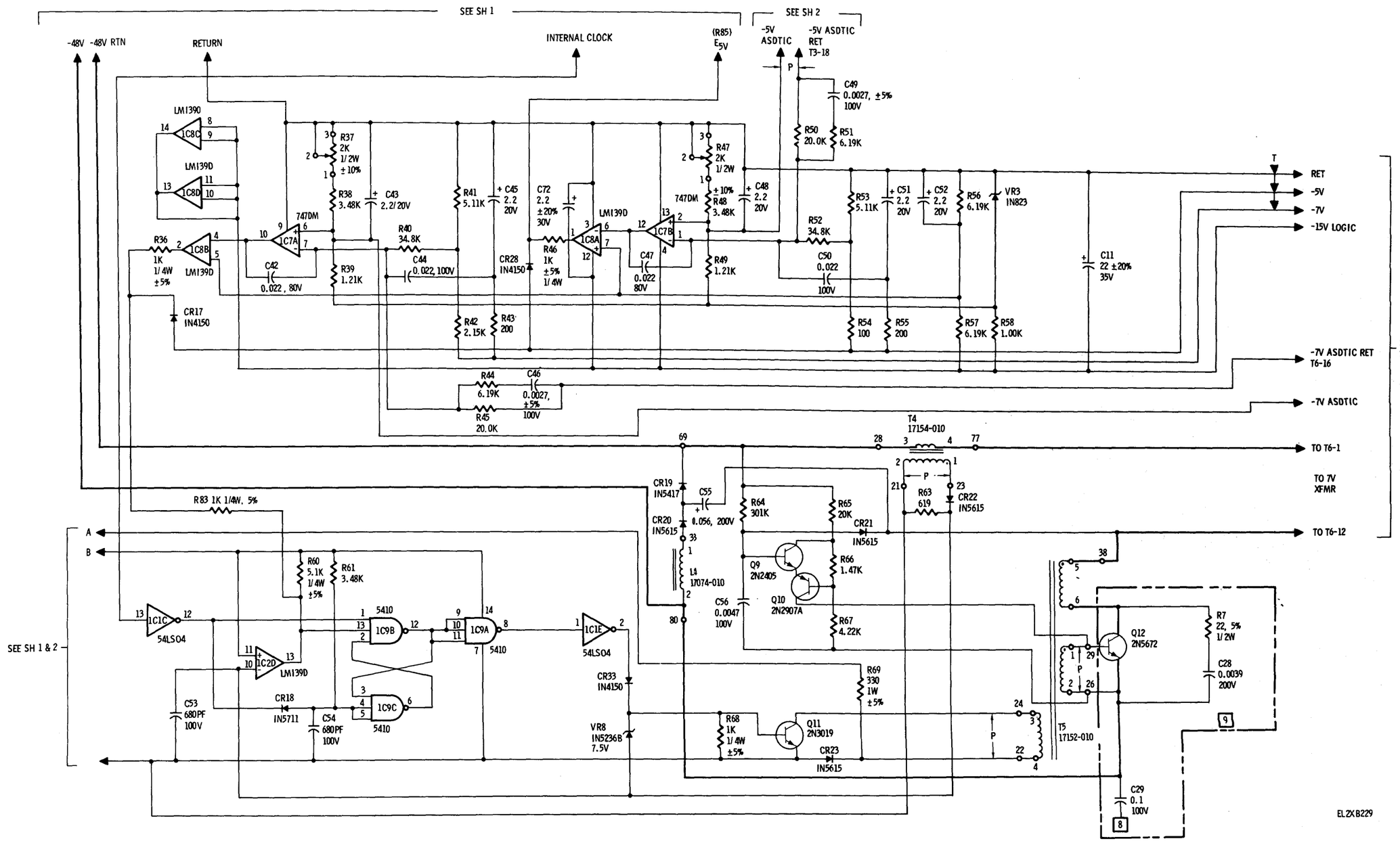
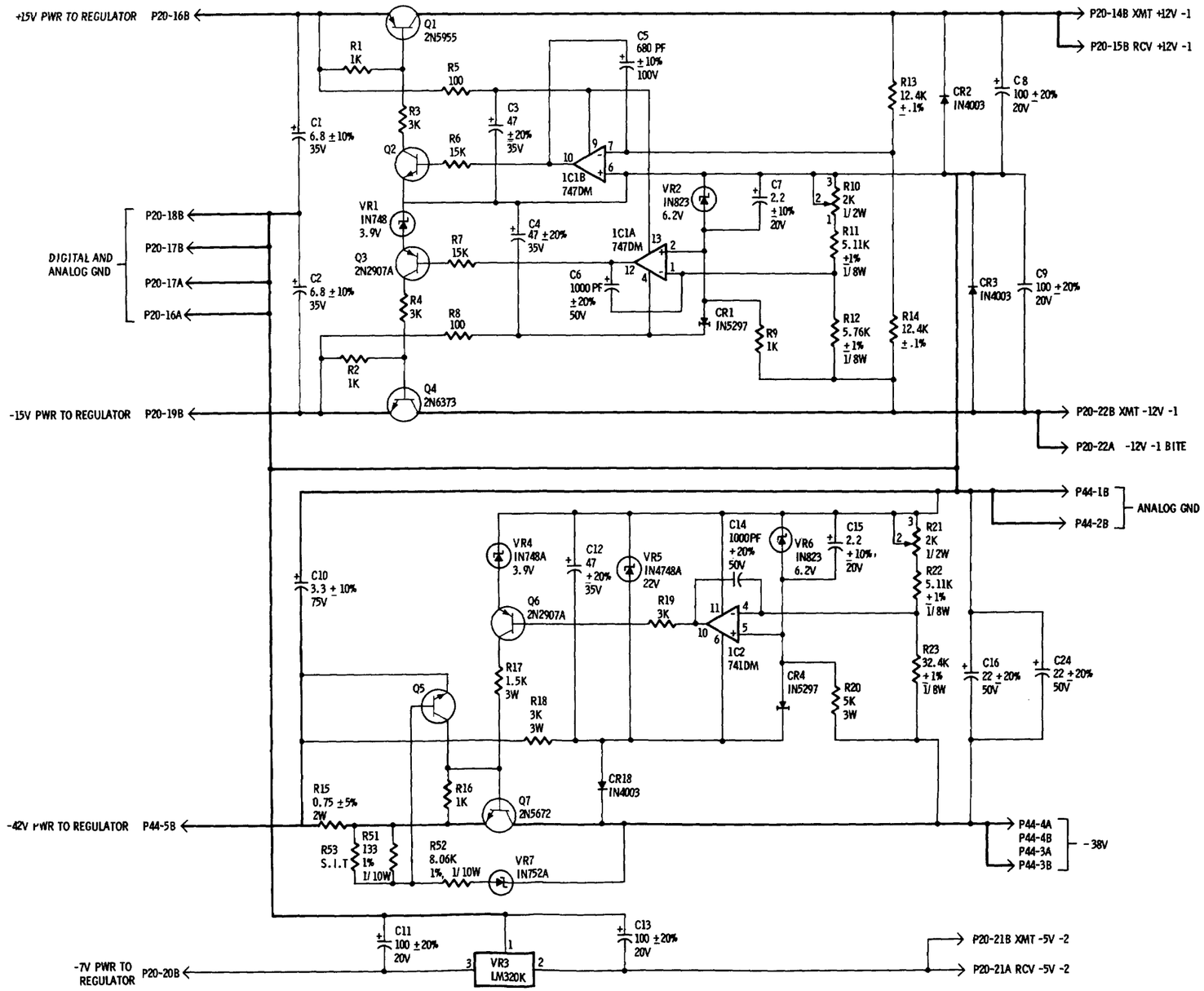


Figure FO-13. PWR SPLY unit (dc converter assembly) schematic (sheet 3 of 3).



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±5%, 1/4W
   ALL CAPACITORS ARE IN MICROFARADS
   ALL DIODES ARE IN4003
   RELAY K7 IS AZ2530-045-2
   RELAYS K1-K6, K8, & K9 ARE AZ2530-06-2
   ALL TRANSISTORS ARE 2N2222A
   DS1 IS 507-3951-1471-600
   DS2, DS3 & DS4 ARE 507-3951-1475-600
   DS5 IS 507-3951-1473-600
2. SYMBOL IDENTIFICATION
   → SIGNAL FLOW PATH
   → CONNECTOR PIN
   A = COMPONENT SIDE
   B = CIRCUIT SIDE
   ▽D DIGITAL GROUND
   S.I.T. SELECT IN TEST COMPONENTS
3. SELECT R53 SUCH THAT THE -38V SHORT CIRCUIT CURRENT IS 200 ±20 MA AT ROOM TEMPERATURE (24°±5° C)

EL2XB230

Figure FO-14. PWR SPLY unit (monitor and alarm board) schematic (sheet 1 of 4) PMA02, PMA04, PMA06, PMA08, and PMA10.

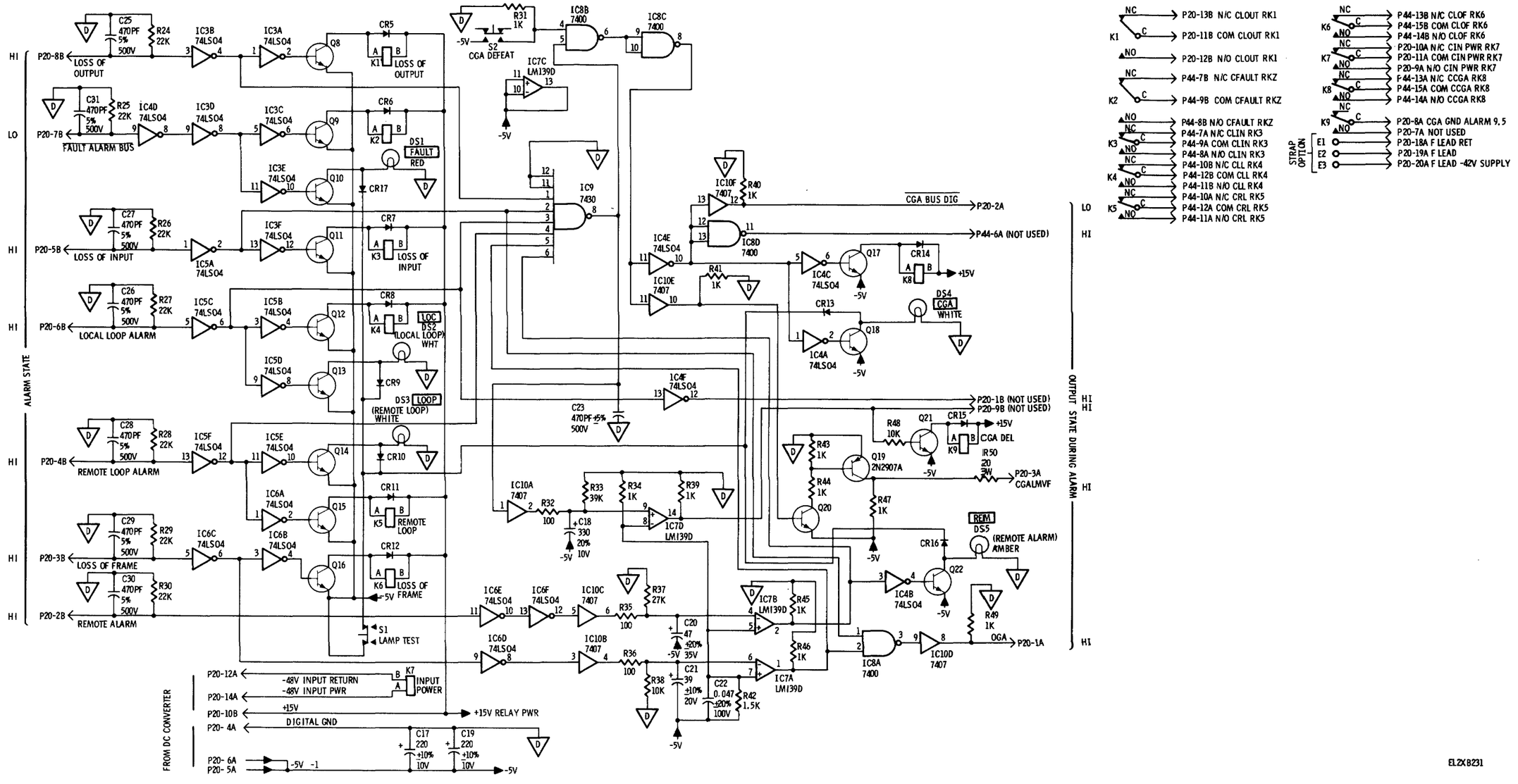
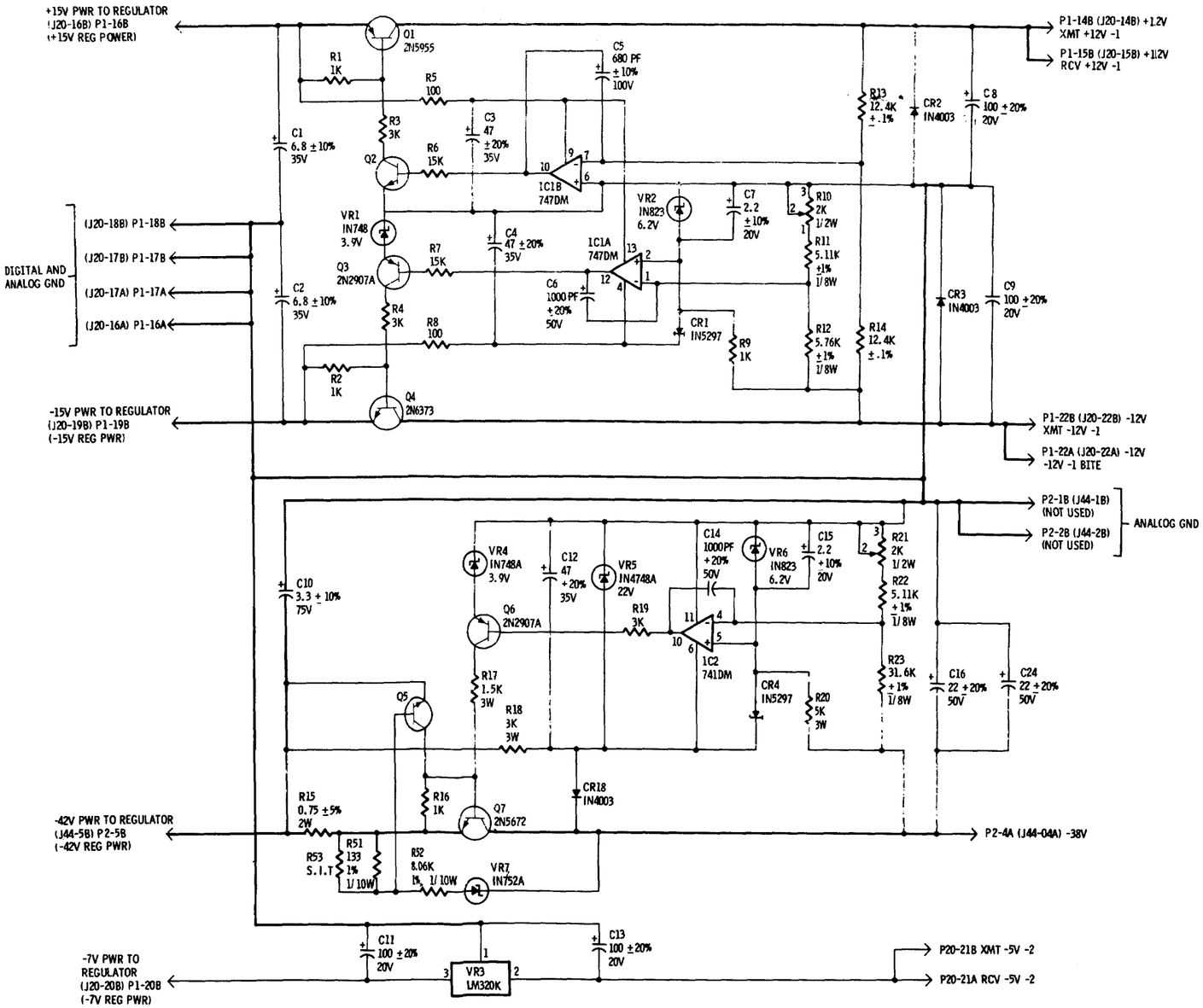


Figure FO-14. PWR SPLY unit (monitor and alarm board) schematic (sheet 2 of 4) PMA02, PMA04, PMA06, PMA08, and PMA10.



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±5%, 1/4W
   ALL CAPACITORS ARE IN MICROFARADS
   ALL DIODES ARE IN4003
   RELAY K7 IS AZ2530-045-2
   RELAYS K1-K6, K8, & K9 ARE AZ2530-06-2
   ALL TRANSISTORS ARE 2N2222A
   DS1 IS 507-3951-1471-600
   DS2, DS3 & DS4 ARE 507-3951-1475-600
   DS5 IS 507-3951-1473-600
2. SYMBOL IDENTIFICATION
   → SIGNAL FLOW PATH
   → CONNECTOR PIN
   A = COMPONENT SIDE
   B = CIRCUIT SIDE
   ▽ DIGITAL GROUND
   S.I.T. SELECT IN TEST COMPONENTS
3. SELECT R53 SUCH THAT THE -38V SHORT CIRCUIT CURRENT IS 200 ± 20 MA AT ROOM TEMPERATURE ($24^{0}_{-5}{}^{0}$ C)

Figure FO-14. PWR SPLY unit (monitor and alarm board) schematic (sheet 3 of 4) PMA12 and PMA14.

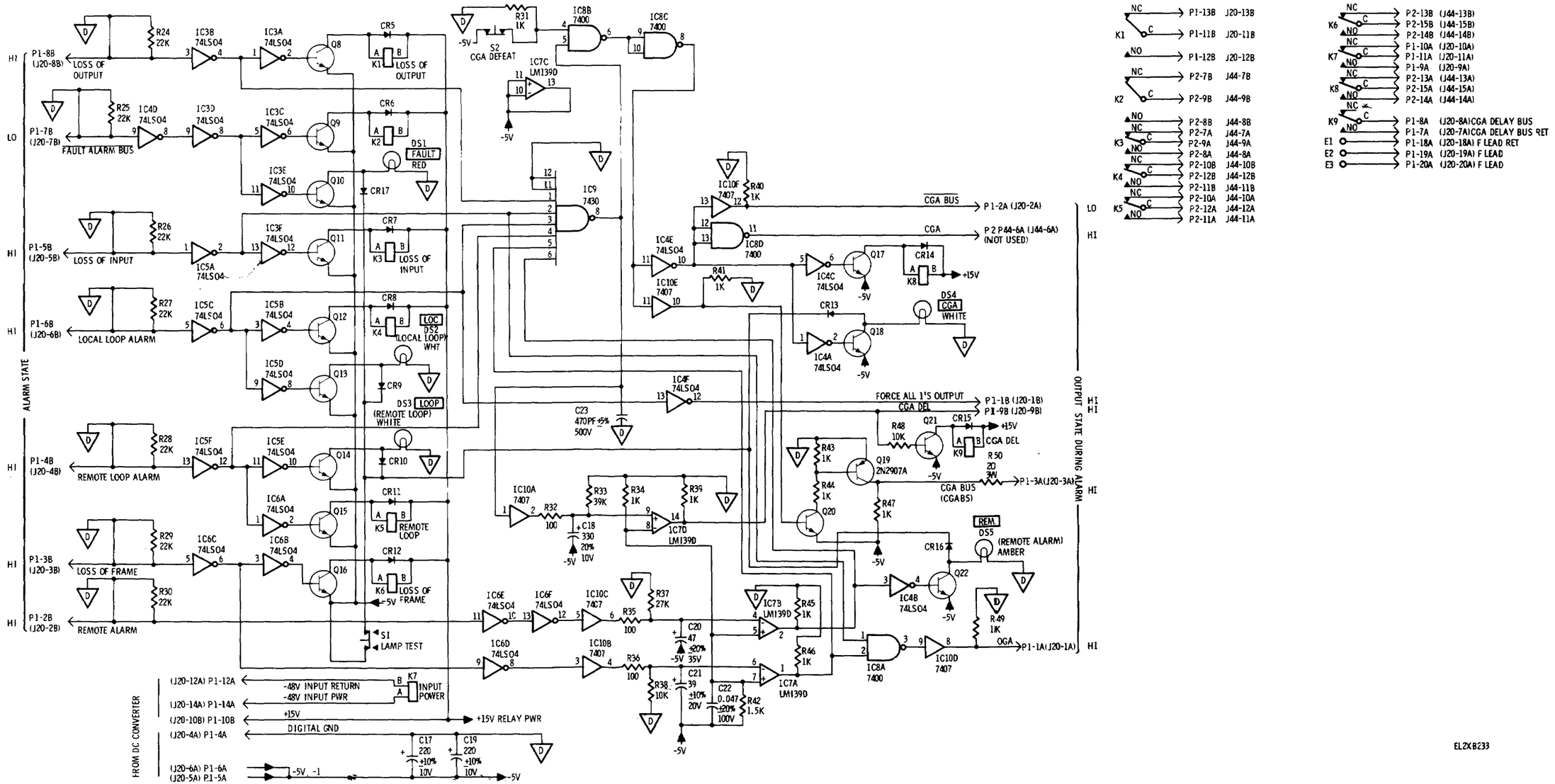
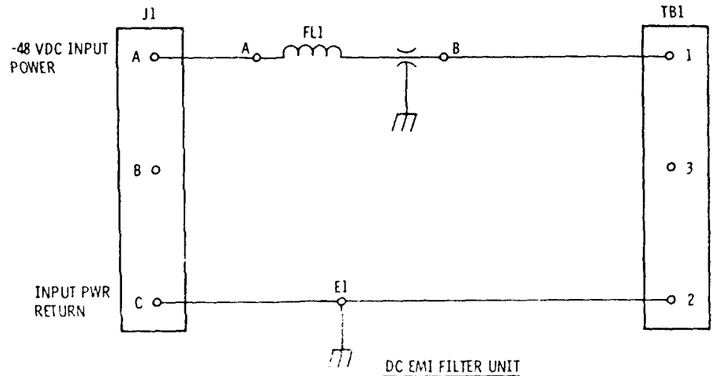
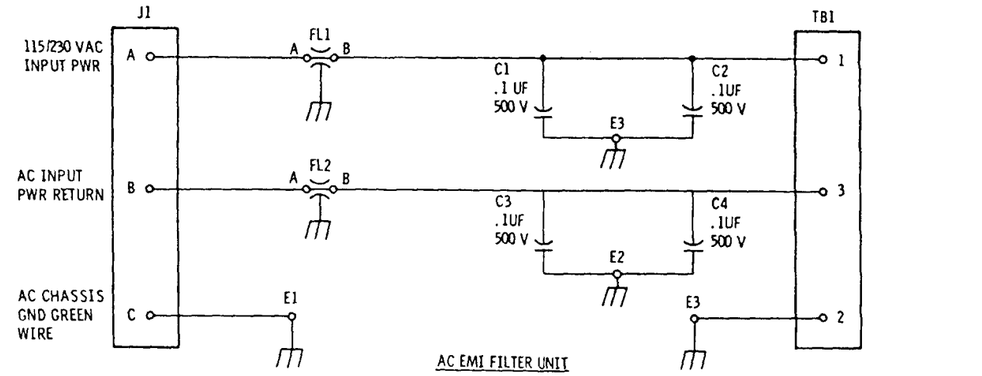


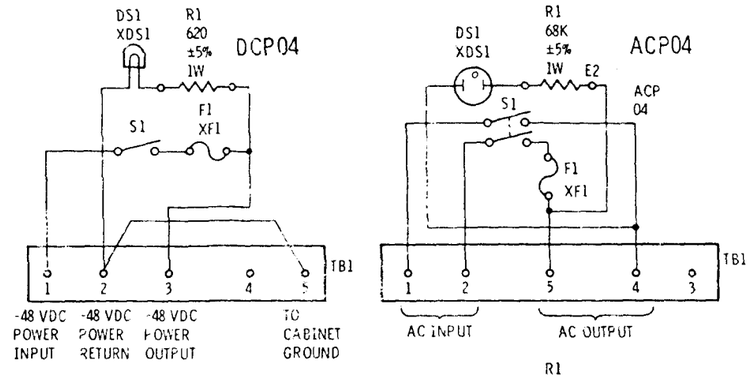
Figure FO-14. PWR SPLY unit (monitor and alarm board) schematic (sheet 4 of 4) PMA12 and PMA14.

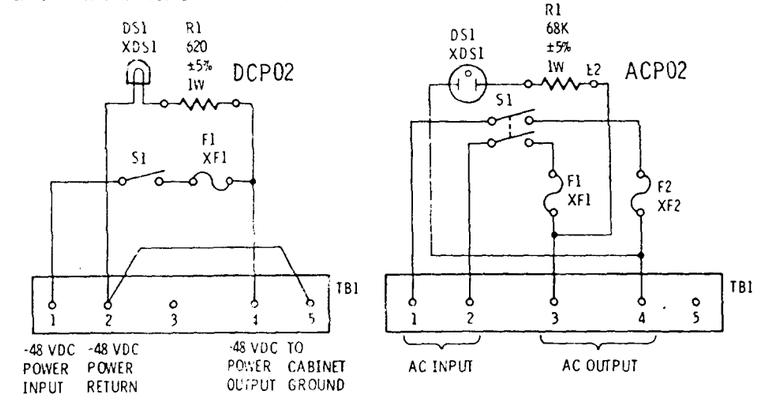


DC EMI FILTER UNIT



AC EMI FILTER UNIT

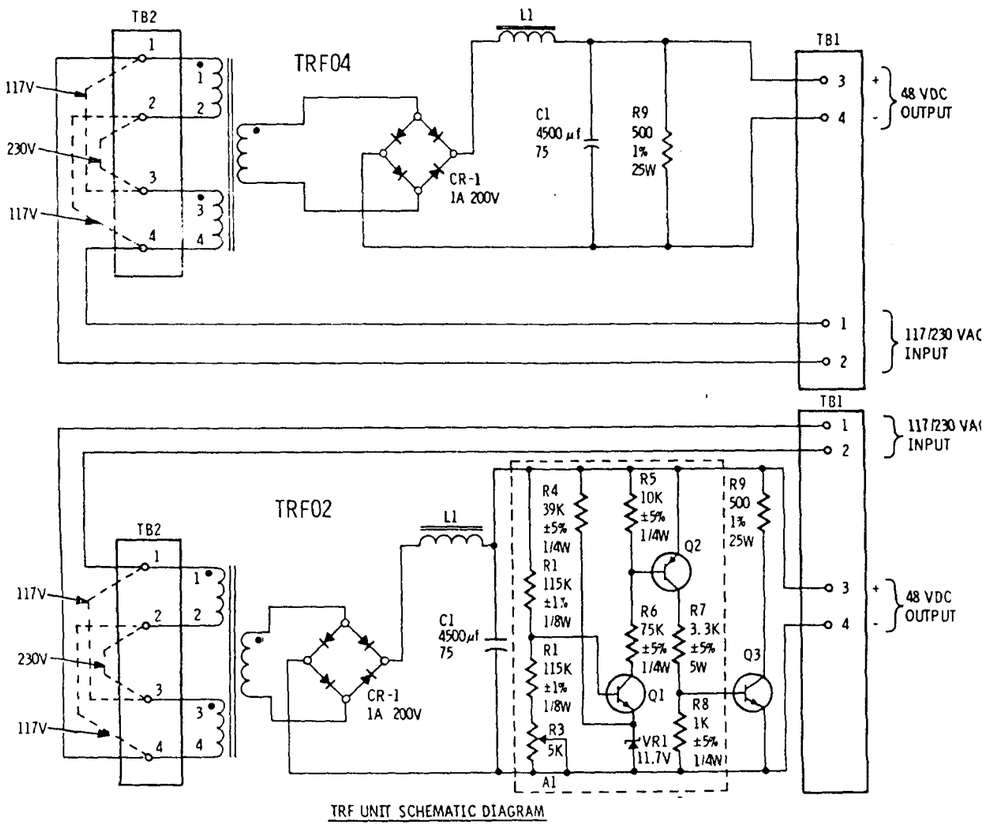




D. C. POWER CONTROL UNIT

AC POWER CONTROL UNIT

NOTE
FUSE F2 IS AN ACTIVE ELEMENT IN CONFIGURATION ACP02. IN CONFIGURATION ACP04, F2 IS A SPARE.



TRF UNIT SCHEMATIC DIAGRAM

EL2XB234

Figure FO-15. TRF unit and EMI filter schematics

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- USAIS (2)
- USAES (2)
- USAICS (3)
- MAAG (1)
- USARMIS (1)
- USAERDAA (1)
- USAERDAW (1)
- Army Dep (1) except
  - Ft Carson (5)
  - Ft Gordon (10)
  - Ft Gillem (10)
  - Ft Richardson (CECOM Ofc) (2)
  - SAAD (30)
  - TOAD (14)
  - SHAD (2)
- USA Dep (1)
- Sig Sec USA Dep (1)
- Units org under fol TOE: (2)
  - 29-207
  - 29-610

NG: None.

USAR: None.

For explanation of abbreviations used see, AR 310-50.

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DATE SENT
10 July 1975

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/PRC-76

BE EXACT PIN-POINT WHERE IT IS				IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
PAGE NO	PARA-GRAPH	FIGURE NO	TABLE NO	
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure the the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

SAMPLE

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER	SIGN HERE
SSG I. M. DeSpiritof 999-1776	SSG I. M. DeSpiritof

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PAGE NO	PARA-GRAPH	FIGURE NO	TABLE NO

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THE METRIC SYSTEM AND EQUIVALENTS

'NEAR MEASURE

. Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

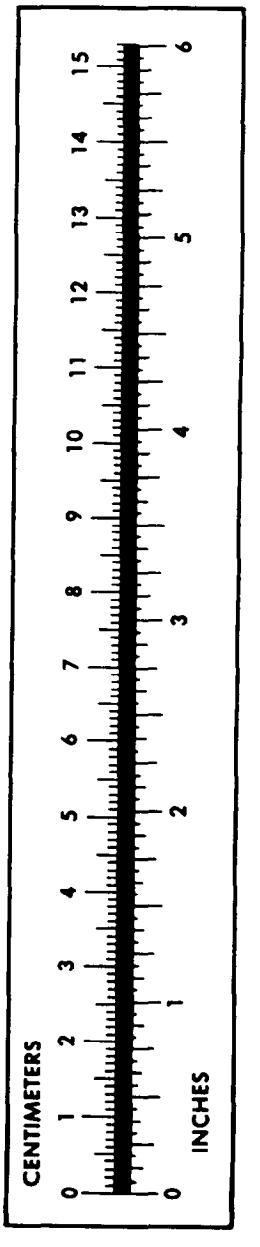
TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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