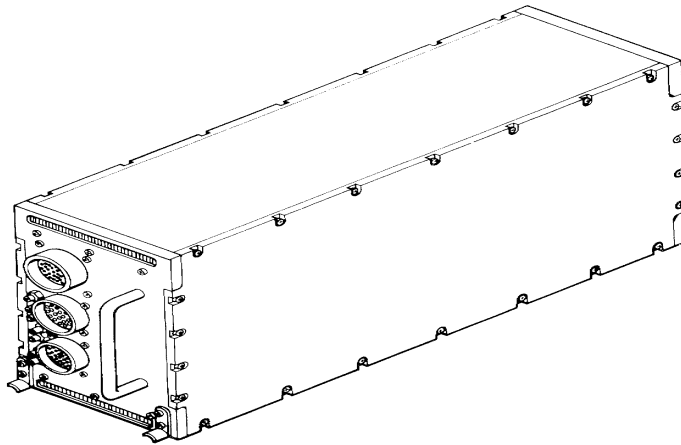


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TECHNICAL MANUAL

OPERATOR'S, UNIT, AND DIRECT SUPPORT  
MAINTENANCE MANUAL

PROCESSOR, INTERMEDIATE  
FREQUENCY CV-4008/U  
(NSN 5895-01-2993417) (EIC: N/A)



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HEADQUARTERS, DEPARTMENT OF THE ARMY

1 MAY 1994



**5**

**SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK**

**1**

**DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL**

**2**

**IF POSSIBLE, TURN OFF THE ELECTRICAL POWER**

**3**

**IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL**

**4**

**SEND FOR HELP AS SOON AS POSSIBLE**

**5**

**AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION**

## SAFETY SUMMARY

### WARNING

- Zinc chromate dust primer is highly toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate (para 5-34).
- Isopropyl alcohol is flammable and moderately toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate (para 5-34).
- Whenever possible, shut off the power source before beginning work inside unit to prevent electrical shock (para 5-7).

**B**

## HOW TO USE THIS MANUAL

1. **HOW DO I FIND INFORMATION?** To help you locate information, this manual has three types of indexes.
  - a. Table of Contents. Entries within the main table of contents duplicate the entries on the front cover and are highlighted. This is in case the cover is torn off or soiled beyond legibility.
  - b. Chapter Indexes. These indexes are located in the front of each chapter. The listings are in the order of appearance.
2. **HOW DO I GET FAMILIAR WITH THE EQUIPMENT?** See chapter 1 for physical and functional descriptions.
3. **DOES THE MANUAL CONTAIN OPERATOR INSTRUCTIONS?** See chapter 2 and 3 for applicability.
4. **WHAT IS THE EXTENT OF ORGANIZATIONAL MAINTENANCE?** See chapter 4. Normally, organizational maintenance is limited to quarterly preventive maintenance checks and services and replacement of defective line replaceable units (LRUs).
5. **WHERE IS DIRECT SUPPORT MAINTENANCE COVERED?** See chapter 5.
6. **ARE OTHER MANUALS REQUIRED?** Refer to appendix A for a list. Obtain these manuals through publication supply channels.
7. **WHAT TOOLS AND EQUIPMENT ARE REQUIRED?** Turn to appendix B (Maintenance Allocation) for a listing.
8. **HOW DO I GET SPARE PARTS?** Refer to paragraph 5-3.
9. **WHAT ACTIONS ARE TAKEN IF MISTAKES ARE FOUND IN THE MANUAL?** See the block on the table of contents for procedures.
10. **DO I NEED TO KNOW ANY SPECIAL SAFETY INSTRUCTIONS?** Ensure you understand the information on page A and B before you operate or maintain the equipment.

**HOW TO USE THIS MANUAL - Continued**

11. **WHAT OTHER FEATURES SHOULD I KNOW ABOUT THIS MANUAL?** You should know the use of NOTES, CAUTIONS, and WARNINGS. Definitions are:

**NOTE**

Highlights an essential operating or maintenance procedure, condition, or statement.

**CAUTION**

Highlights an essential operating or maintenance procedure, practice, condition, statement, etc., which, if not strictly observed, could result in damage to, or destruction of, equipment or loss of mission effectiveness,

**WARNING**

Highlights an essential operating or maintenance procedure, practice, condition, statement, etc. , which, if not strictly observed, could result in injury to, or death of, personnel or long term health hazards.

**D**

**OPERATOR'S, UNIT, AND DIRECT SUPPORT  
 MAINTENANCE MANUAL  
 PROCESSOR, INTERMEDIATE FREQUENCY  
 CV-4008/U  
 (NSN 5895-01-299-3417) (EIC: N/A)**

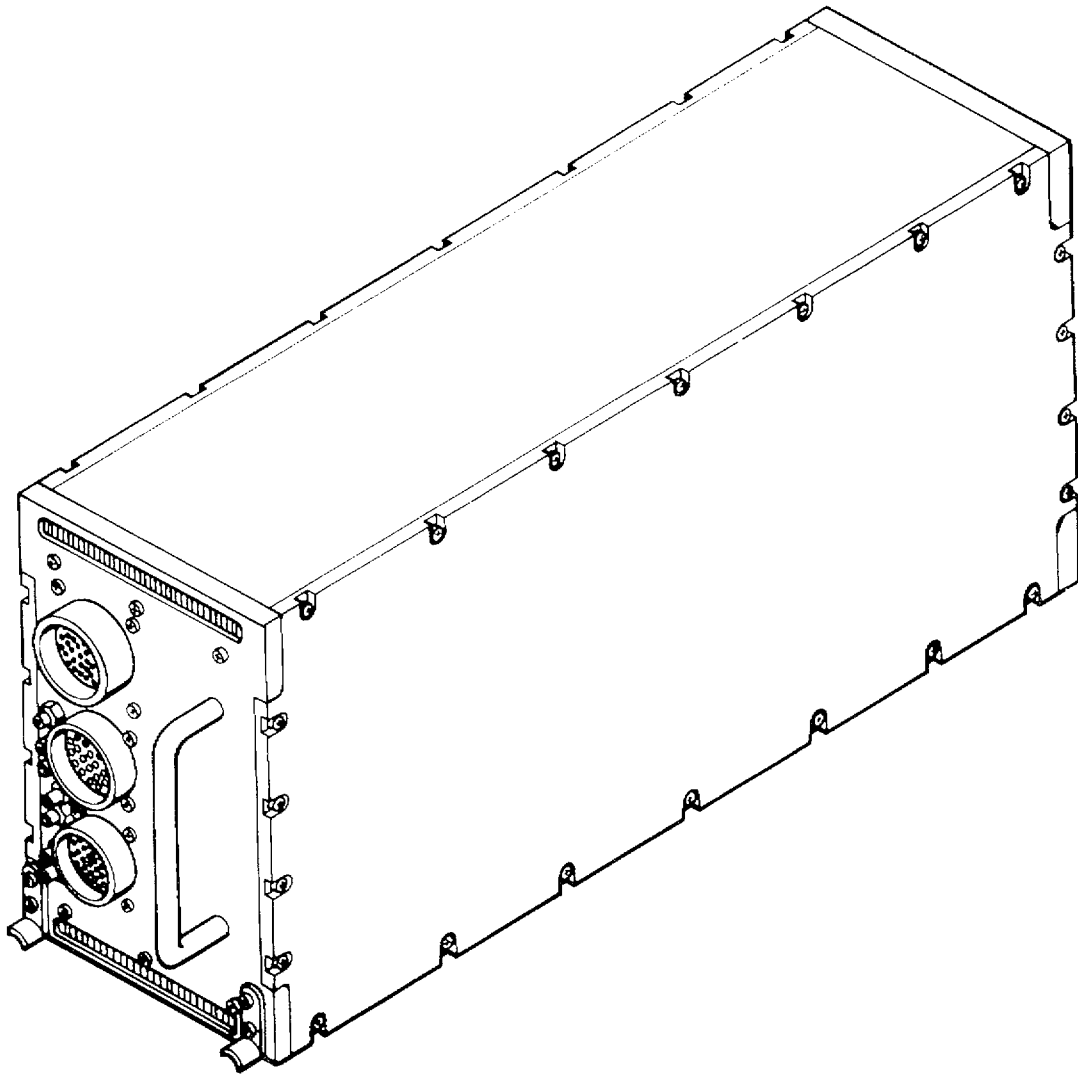
**REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS**

You can help improve this manual. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms) or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-LM-LT, Fort Monmouth, New Jersey 07703-5007. In either case a reply will be furnished direct to you.

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PROCESSOR, INTERMEDIATE FREQUENCY CV-4008/U



**CHAPTER 1**  
**INTRODUCTION**

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<b>Section I</b>	<b>General Information</b>	
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**Section I. GENERAL INFORMATION**

**1-1. SCOPE**

Type of Manual: Operator's, Organizational, and Direct Support Maintenance

Model Number and Equipment Name: CV-4008/U - Processor, Intermediate Frequency (IF Processor) (IFP).

Purpose of Equipment: Processes if. signals for signal qualification and signal confirmation.

**1-2. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS**

Refer to the latest issue of DA Pam 25-30 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

**1-3. MAINTENANCE FORMS, RECORDS, AND REPORTS**

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750, as contained in Maintenance Management Update.

b. Reporting of Item and Packaging Discrepancies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/SECNAVINST 4355.18/AFR 400-54/MCO 4430.3J.

c. Transportation Discrepancy Report (TDR) (SF 361). Fill out and forward Transportation Discrepancy Report (TDR) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

**1-4. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR)**

If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design or performance. Put it on an SF 368 (Product Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-ED-CFO, Fort Monmouth, New Jersey 07703-5023. We'll send you a reply.

**1-5. DESTRUCTION OF ARMY ELECTRONICS MATERIEL**

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

**1-6. ADMINISTRATIVE STORAGE**

Administrative storage of equipment issued to and used by Army activities will have Preventive Maintenance Checks and Services (PMCS) performed before storing. When removing the equipment from administrative storage, the PMCS checks should be performed to assure operational readiness.

**1-7. REFERENCE INFORMATION**

This listing includes the nomenclature cross reference list and list of abbreviations used in this manual.

a. Nomenclature Cross Reference List.

<u>Common Name</u>	<u>Official Nomenclature</u>
Computer processor (CP) .....	Computer Processor CP-1692/U
Control panel .....	Control Panel C-1 1804/ALQ
Electronic systems test set . (ESTS) .....	Test Set. Electronic Systems TS-4239/U
Frequency synthesizer (FS) .....	Frequency Synthesizer 0-1833/U
IF processor (IFP) .....	Processor, Intermediate Frequency CV-4008/U
IF switch (IFS) .....	Switch Assembly, Intermediate Frequency SA-2542/U
Interface unit (IU).....	Interface Unit J-4522/U
NAV set .....	Carousel IV-E High-Accuracy Inertial Navigation System
Operator terminal .....	Alphanumeric Display Station HP2645A
Operator terminal .....	Computer, Digital CP-1849/U (GRiDSE-T)
POD housing .....	Pod Housing
Quantizer-control group . (Q-C groups) .....	Quantizer-Control Group QA-9343/TSQ

1-7. REFERENCE INFORMATION - Continued

<u>Common Name</u>	<u>Official Nomenclature</u>
Radio frequency antenna (RFA).....	Antenna. Radio Frequency AS-3901/U
Receiver digital control (RDC).....	Control, Receiver, Digital C-1 1634/U
Receiver PS.....	Power Supply. Receiver PP-8184/U
Signal data recorder (SDR).....	Recorder, Signal Data RD-547/U
Storage battery.....	Battery, storage C5117400
System PS.....	Power Supply PP-8158/U
Wide band data link.....	Interoperable Airborne Data link
150 MHz IF (A1A1, A1A2, .A1A4, A1A5).....	Module Assy, 150 MHz IF Matched IF Set (A1A1, A1A2, A1A4, A1A5) (C5116718)
BIT (A1A3).....	Module Assy, Built-in test (A1A3) (C5116581)
180 MHz IF (USB) (A1A6).....	Module Assy, 180 MHz IF (A1A6) (C5116641)
120 MHz IF (LSB) (A1A7).....	Module Assy, 120 MHz IF (A1A7) (C5116641)
Coarse FRU (A1A8).....	Module Assy, Frequency Resolving Unit (A1A8) (C5116649)
150 MHz Intfc/log (A1A9).....	Module Assy, 150 MHz Limiter/Log Amplifier (A1A9) (C5116637)
Delay Line (A1A10).....	Module Assy, Delay line (A1A10) (C5116727)
FRU conv (A1A11).....	Module Assy, Converter-Frequency Resolving Unit (A1A11) (C5116530)
Quad phase det A (A1A12).....	Module Assy, Quad Phase Detector A (A1A12) (C5116630)
Quad phase det B (A1 A13).....	Module Assy, Quad Phase Detector B (A1A13) (C5116610)
Intfc logic (A2A1).....	Interface CCA (A2A1) (C5116606)
Confirm logic (A2A2).....	Confirm Logic CCA (A2A2) (C5090540)
Thr/gate gen (A2A3).....	Threshold Detector and Gate Generator CCA (A2A3) (C5116732)
Phase reversal det (A2A4).....	Phase Reversal Detector CCA (A2A4) (C5116720)
Dual phase S-H (A2A5, A2A6, . A2A7).....	Dual Sample/Hold Phase CCA (A2A5, A2A6, A2A7) (C5116596)
Dual FRU S-H (A2A8).....	Dual Sample/Hold Fine Frequency Resolving Unit CCA (A2A8) (C5116596)
Dual amptd S-H (A2A9).....	Dual Sample/Hold Amplitude CCA (A2A9) (C5116592)
Dual FRU S-H (A2A10).....	Dual Sample/Hold Frequency Resolving Unit CCA (A2A10) (C5116600)
DUAL FRU/amptd S-H (A2A11).....	Dual Sample/Hold Amplitude Frequency Resolving Unit (A2A11) (C5116602)

## 1-7. REFERENCE INFORMATION - Continued

b. List of Abbreviations.

ALC.....	Antenna logic converter
Amptd.....	amplitude
BIT.....	built-in test
cf.....	calibration factor
CH.....	channel
conv.....	converter
CP.....	computer processor
cw.....	clockwise
CW.....	continuous wave
ccw.....	counterclockwise
CCA.....	Circuit card assembly
dBm.....	decibels in reference to one milliwatt
det.....	detector
df.....	direction finding
DRU.....	Dynamic reference unit
ECL.....	emitter coupled logic
ESTS.....	electronic systems test set
FRU.....	frequency resolving unit
FS.....	frequency synthesizer
HB.....	high band
IFP.....	IF processor
IFS.....	IF switch
intfc.....	interface
I output.....	zero phase difference from reference
IU.....	interface unit
LB.....	low band
Lmtr.....	limiter
Log.....	logarithmic
LSB.....	lower sideband
MB.....	mid band
MHz.....	megahertz
MTE.....	mission test equipment
NB.....	narrow band
o-scope.....	oscilloscope
pls.....	pulse
P/O.....	part of
q-c group.....	quantizer-control group
Q output.....	90 degree phase difference from reference
R.....	reference
rf.....	radio frequency
RFA.....	radio frequency antenna
RDC.....	receiver digital control
S-H.....	sample and hold
SDR.....	signal data recorder
SSB.....	single sideband
T.....	termination
thr.....	threshold

1-7. REFERENCE INFORMATION - Continued

c. List of Abbreviations

TTL .....transistor transistor logic  
USB .....upper sideband  
V .....video  
Vp-p .....volts peak to peak  
VVM.....vector voltmeter  
WB.....wide band

**1-8. SAFETY, CARE, AND HANDLING**

- a. Safety. For artificial respiration, refer to FM 21-11. When lifting or handling heavy objects, use two persons to prevent possible back injury.
- b. Care. Do not use the equipment as a step or a seat.
- c. Handling. Do not drop the equipment or turn it over roughly. Avoid damage to connectors.

**Section II. EQUIPMENT DESCRIPTION****1-9. CHARACTERISTICS, CAPABILITIES, FEATURES****CHARACTERISTICS**

- LIGHTWEIGHT
- RACK-MOUNTED

**CAPABILITIES**

- ACCEPTS SIX BAND-SELECTED IF INPUT SIGNALS
- OUTPUTS ANALOG SIGNALS AND DIGITAL FLAGS TO INTERFACE UNIT

**FEATURES**

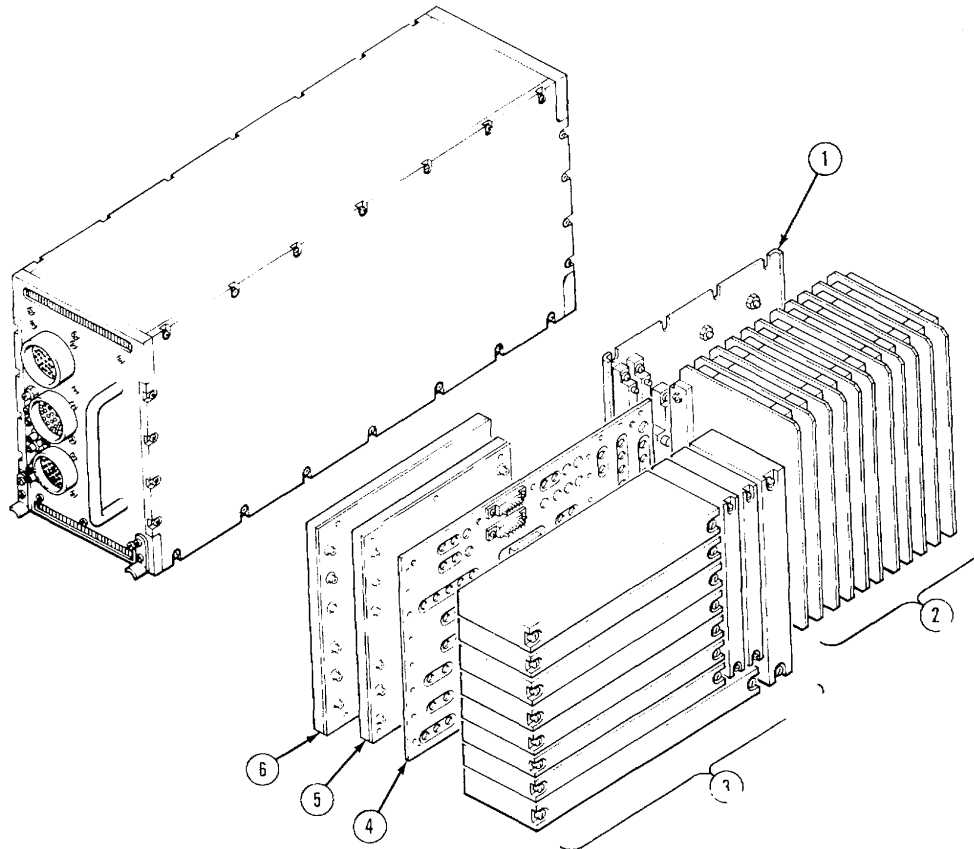
USES TRIGGER CHANNELS AND PHASE CHANNELS TO DETERMINE,

- PHASE
- FREQUENCY
- AMPLITUDE
- DYNAMIC RANGE
- SPURIOUS SIGNAL RESPONSE
- IF RECEIVED SIGNAL IS UPPER OR LOWER SIDEBAND

**1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS**

a. General Location. Refer to TM 11-5821-332-13.

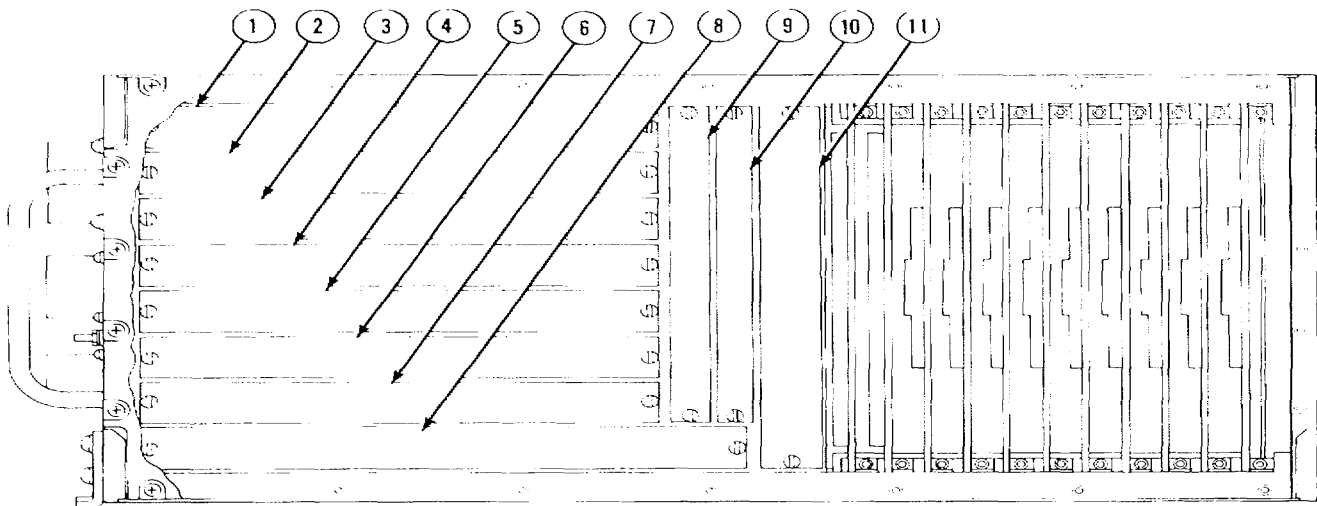
b. Major Components



- |                                      |  |
|--------------------------------------|--|
| (1) <b>CONNECTOR PLATE A.</b>        | Provides interface between modules and circuit cards |
| (2) <b>CIRCUIT CARD UNIT A2.</b>     | Contains circuit cards A2A1 through A2A11            |
| (3) <b>MODULE UNIT A1.</b>           | Contains modules A1A1 through A1A13                  |
| (4) <b>CONNECTOR PLATE B.</b>        | Provides interface between modules and circuit cards |
| (5) <b>QUAD PHASE DET A (A1A12).</b> | part of module unit A1                               |
| (6) <b>QUAD PHASE DET B (A1A13).</b> | Part of module unit A1                               |

1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS - Continued

c. Modules.

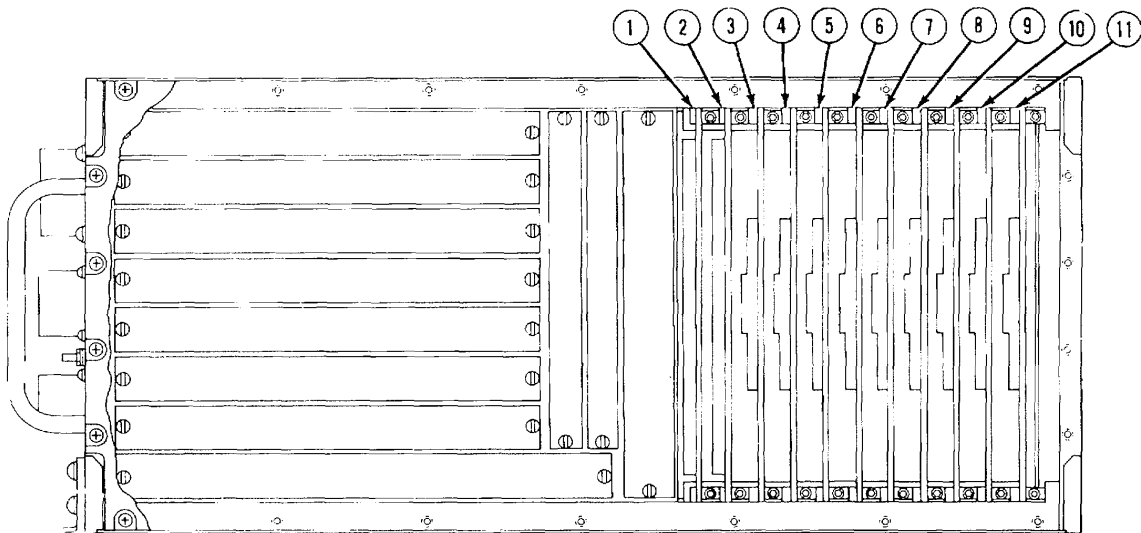


- |                              |   |
|------------------------------|---|
| (1) 150 MHz IF (A1A1).       | Amplifies CH A input                      |
| (2) 150 MHz IF (A1A2).       | Amplifies CH B input                      |
| (3) BIT (A1 A3).             | Provides BIT IF to all 150 MHz IF modules |
| (4) 150 MHz IF (A1A4).       | Amplifies CH C input                      |
| (5) 150 MHz IF (A1A5).       | Amplifies CH D input                      |
| (6) 120 MHz IF (LSB) (A1A7)  | Amplifies LSB signals                     |
| (7) 180 MHz IF (USB) (A1A6)  | Amplifies USB signals                     |
| (8) COARSE FRU (A1A8)        | Contains frequency resolving units        |
| (9) 150 MHz LMTR/LOG (A1A9). | Processes CH D signals                    |
| (10) DELAY LINE (AA10).      | Provides linear phase changes             |
| (11) FRU CONV (A1A11).       | Provides two Q and I outputs              |



1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS - Continued

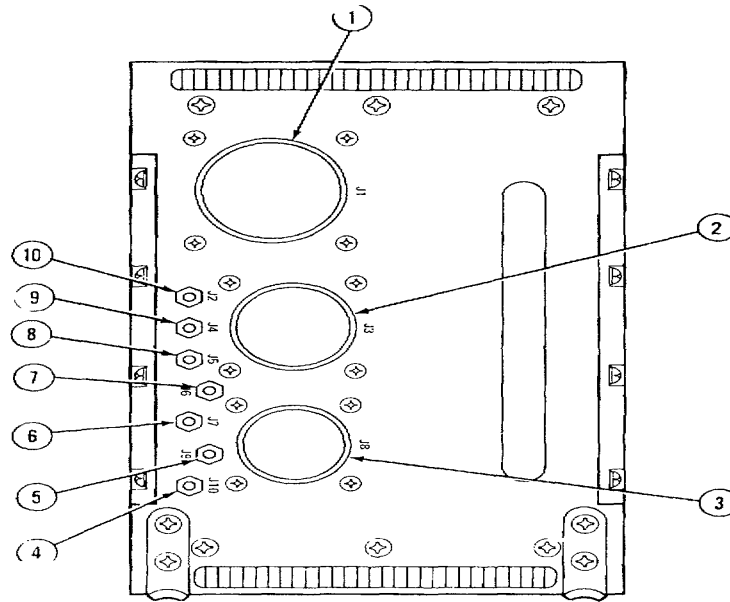
d. Circuit Cards.



- |   |   |
|---|---|
| (1) <b>INTFC LOGIC (A2A1).</b>          | Interfaces to RDC and IU  |
| (2) <b>CONFIRM LOGIC (A2A2).</b>        | Confirms signal quality of frequency, pulse width and amplitude |
| (3) <b>THRIGATE GEN (A2A3).</b>         | Generates S-H commands, sets receiver threshold                 |
| (4) <b>PHASE REVERSAL DET (A2A4).</b>   | Outputs new pulse based on phase reversal                       |
| (5) <b>DUAL PHASE S-H (A2A5).</b>       | Holds sample phase pulses                                       |
| (6) <b>DUAL PHASE S-H (A2A6).</b>       | Holds sample phase pulses                                       |
| (7) <b>DUAL PHASE S-H (A2A7).</b>       | Holds sample phase pulses                                       |
| (8) <b>DUAL PHASE S-H (A2A8).</b>       | Holds sample fine frequency pulses                              |
| (9) <b>DUAL AMPTD S-H (A2A9).</b>       | Holds sample amplitude pulses                                   |
| (10) <b>DUAL FRU S-H (A2A10).</b>       | Holds sample coarse frequency pulses                            |
| (11) <b>DUAL FRU/AMPTD S-H (A2A11).</b> | Holds sample frequency and amplitude pulses                     |

1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS - Continued

e. External Interfaces.



- |                 |                   |
|-----------------|-------------------|
| (1) <b>J1</b>   | Power input       |
| (2) <b>J3.</b>  | IU interface      |
| (3) <b>J8.</b>  | RDC interface     |
| (4) <b>J10.</b> | BIT output        |
| (5) <b>J9.</b>  | USB trigger input |
| (6) <b>J7.</b>  | LSB trigger input |
| (7) <b>J6.</b>  | CH D DF input     |
| (8) <b>J5.</b>  | CH C DF input     |
| (9) <b>J4.</b>  | CH B DF input     |
| (10) <b>J2.</b> | CH A DF input     |

**1-11. EQUIPMENT DATA**

**a. Physical**

Weight	26.40 lb (12.00 kg)
Height	7.63 in (19.38 cm)
Width	4.88 in (12.39 cm)
Length	16.75 in (42.54 cm)

**b. Functional**

Input Power	+ 15.0 Vdc @ 5.0 amp -15.0 Vdc @ 1.9 amp + 5.0 Vdc @ 1.8 amp -5.5 Vdc @ 7.7 amp
-------------	--

**Interface**

External	IF switch band selected signals
Internal	Processes data and holds samples for later digitalization
Output	DF, FRU, or log amplitude signals

**c. Environmental**

**Temperature**

Operating	-51 degree F (-46 degrees C) to + 131 degrees F (+ 55 degrees C)
Non-operating.....	- 60 degrees F (-51 degrees C) to + 185 degrees F (+ 85 degrees C)

**Altitude**

Operating .....	30,000 ft (9,144 m)
Non-operating.....	40,000 ft (12,192 m)

**Humidity**

..... 0 to 98 percent

**Fungus**

..... Fungus resistant

**Salt fog**

..... Prolonged exposure without degradation

**Sand and Dust**

..... Exposure without damage or degradation

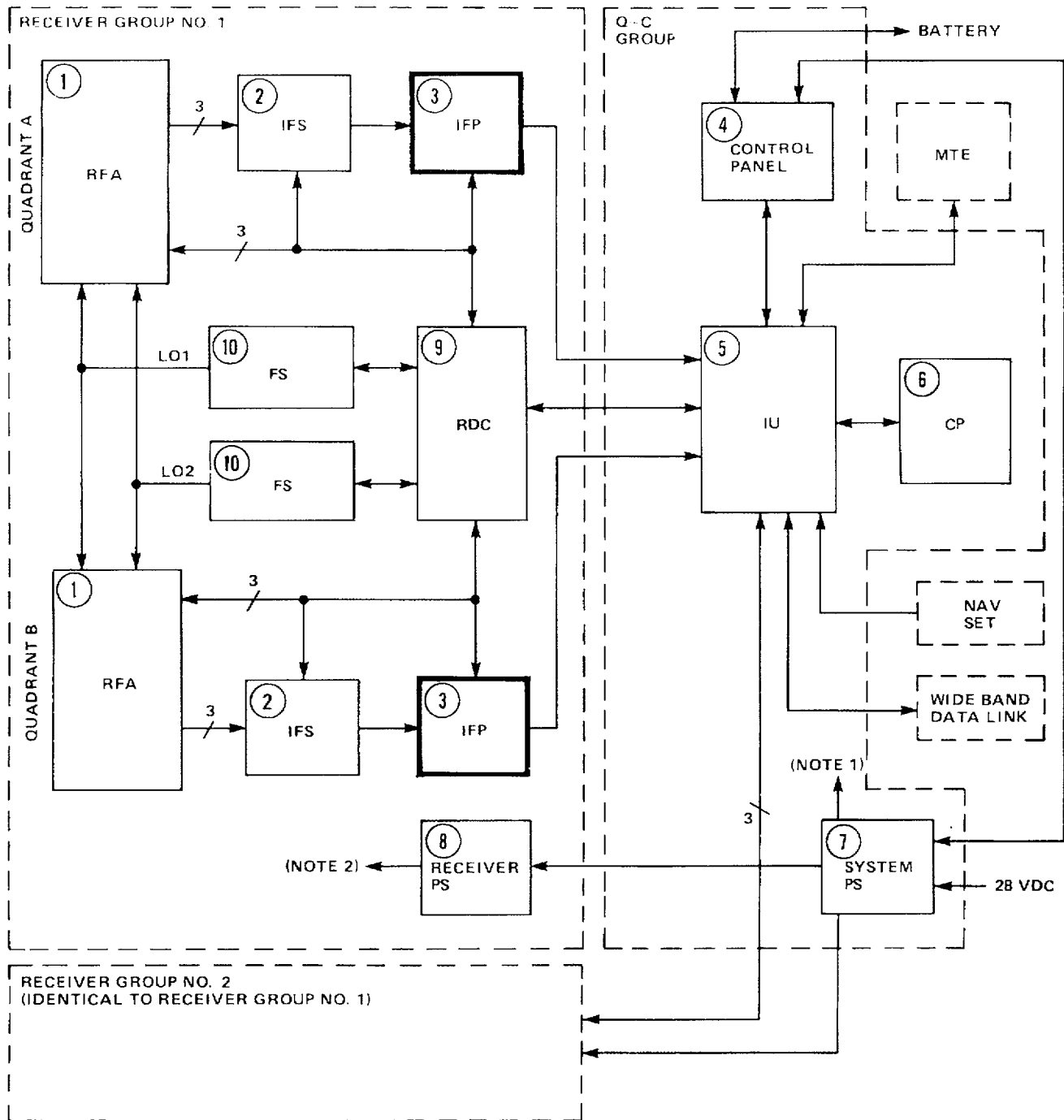
**Vibration**

..... Transportable by ground vehicle, watercraft, or aircraft

**Section III. TECHNICAL PRINCIPLES OF OPERATION****1-12. OVERVIEW**

- (1) **RADIO FREQUENCY ANTENNA (RFA)**. Intercepts rf emitter signals. Downconverts rf signals to produce phase and trigger if signal outputs.
- (2) **IF SWITCH (IFS)**. Filters RFA phase and trigger if signals. Routes if signals to IFP as directed by RDC
- (3) **IF PROCESSOR (IFP)**. Processes if signals for signal qualification and signal confirmation.
- (4) **CONTROL PANEL**. Controls system PS. Also used to zeroize CP memory.
- (5) **INTERFACE UNIT (IU)**. Provides interface and control of major system units.
- (6) **COMPUTER PROCESSOR (CP)**. Performs data computation and signal processing functions for quantizer-control group (Q-C group).
- (7) **SYSTEM PS**. Provides primary power for Q-C group.
- (8) **RECEIVER PS**. Provides power for receiver group.
- (9) **RECEIVER DIGITAL CONTROL (RDC)**. Provides digital control of receiver group and routing of data to Q-C group.
- (10) **FREQUENCY SYNTHESIZERS (FS)**. Generates phase lock loop local oscillator (LO) signals ( three bands) to rapidly tune RFA.

1-12 OVERVIEW - Continued

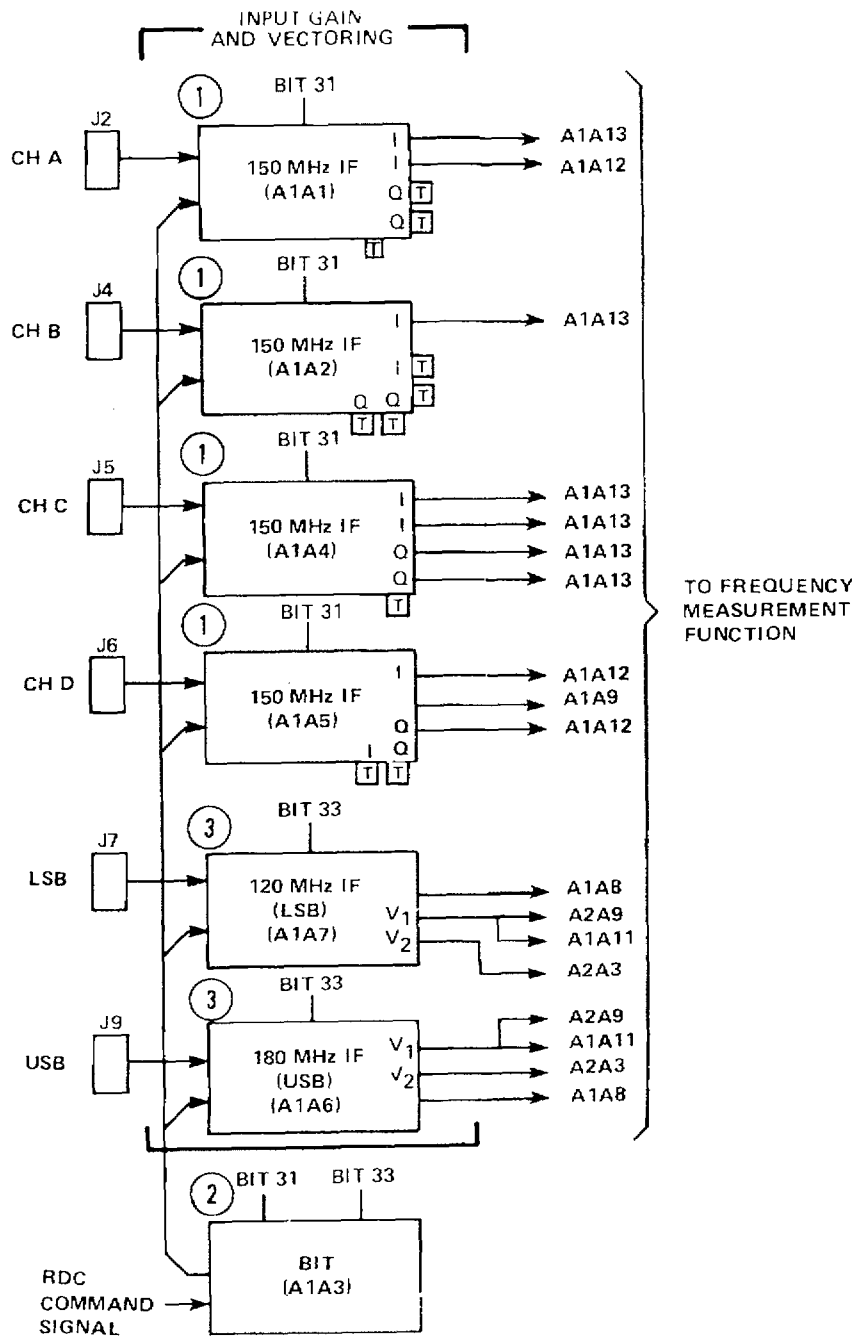


- NOTES:  
 1. TO Q-C GROUP.  
 2. TO ALL RECEIVER GROUP LRU'S.

**1-13. DETAILED OPERATION****a. Input Gain and Vectoring.**

- (1) **150 MHz IF (A1A1, A1A2, A1A4, A1A5).** Each module receives df signal from IFS or BIT signals from A1 A3. Either signal is processed, depending upon command received. Chosen signal is tuned by wideband bandpass filter, limited, amplified, and phase-shifted by 90-degree hybrid shift network. This provides two pairs of identical signals. except that one pair is 90-degree phase shifted.
- (2) **BIT (A1 A3).** Not a part of input gain and vectoring circuit. Generates signals that are input to 150 MHz IF modules (A1A1, A1A2, A1A4, A1A5), A1A6, and A1A7. A1A7 is controlled by command signal from RDC.
- (3) **180 MHz IF (USB) (A1A6), 120 MHz IF (LSB) (A1A7).** Each module receives trigger signals from IFS or BIT signals from A1A3. Either signal is processed, depending upon command received. Chosen signal is sharply tuned by bandpass filter. limited, and amplified. Two kinds of limited outputs are provided' a limited signal power output and a signal level dependent dc log voltage output.

1-13. DETAILED OPERATION - Continued



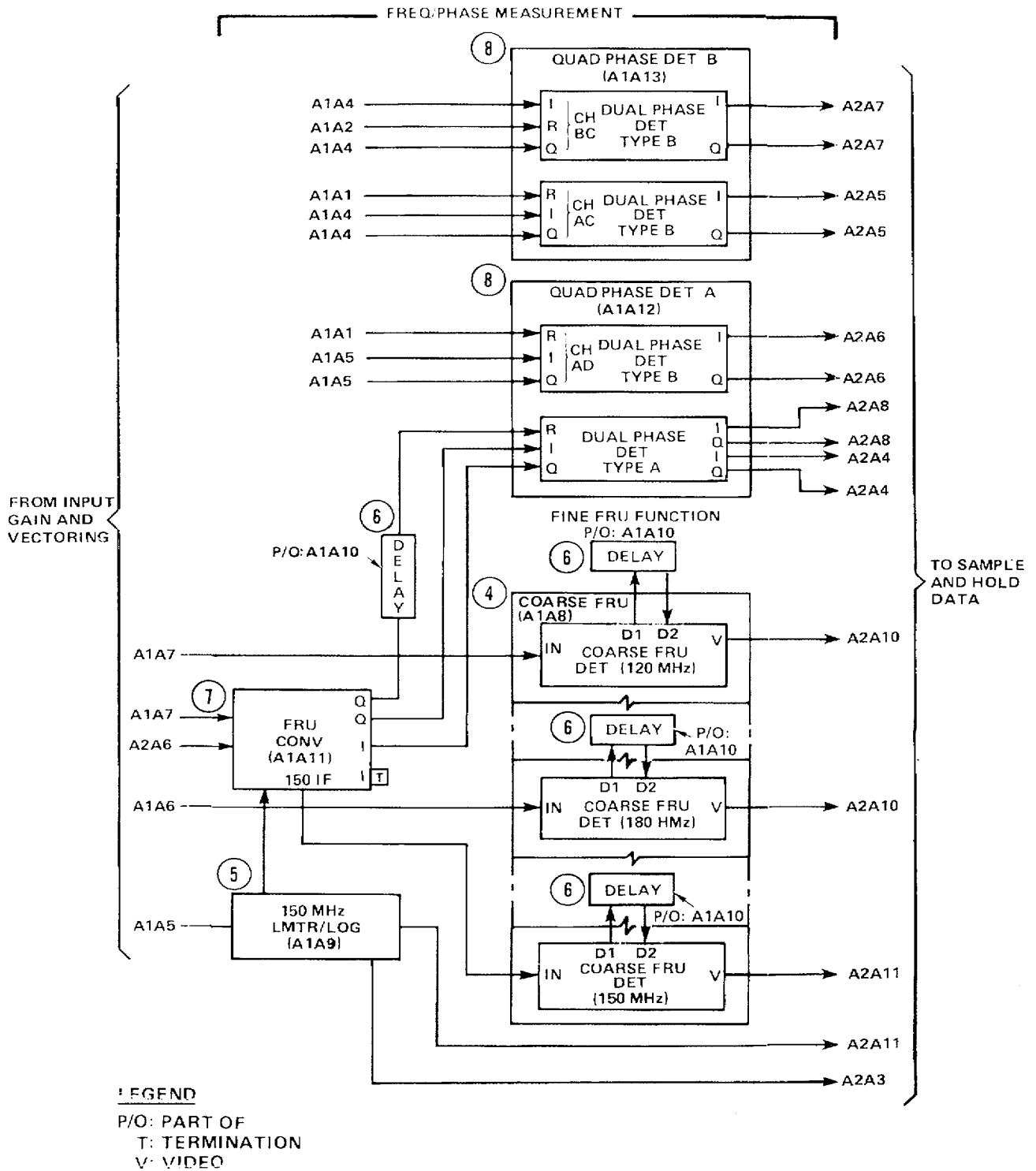
BIT, INPUT GAIN, AND VECTORING CIRCUITS BLOCK DIAGRAM

**1-13. DETAILED OPERATION-** Continuedb. Frequency/Phase Measurement

- (4) **COARSE FRU (A1A8).** Receives inputs from A1A9 and A1A11. Contains three coarse frequency resolving units. Frequency measurements are made in terms of phase shift measurements. Outputs are in amplitude variations that are proportional to frequency.
- (5) **150 MHz LMTR/LOG (A1A9).** Receives inputs from CH D 150 IF MHz (A1A5) and provides two kinds of outputs: limited if. signal power output and log dc signal level dependent on amplitude of input if signal.
- (6) **DELAY LINE (A1A10).** Consists of three separate delay lines. Works with coarse FRU (A1A8) and quad phase dot A (A1A12) to provide linear phase change for frequency measurement.
- (7) **FRU CONV (A1 A11).** Receives inputs from 150 MHz Imtr/log (A1A9). Outputs two Q and two I signals for frequency measurements. The Q output has a 90-degree phase difference from reference; the I outputs have a zero phase difference from the reference.
- (8) **QUAD PHASE DET (A1A12, A1A13).** Detects phase differences between in-phase channel inputs and quadrature channel inputs, generating analog voltage outputs. Quad phase detector module contains two dual phase detector subassemblies I and Q. Outputs are changing voltages that are proportional to input phase differences.



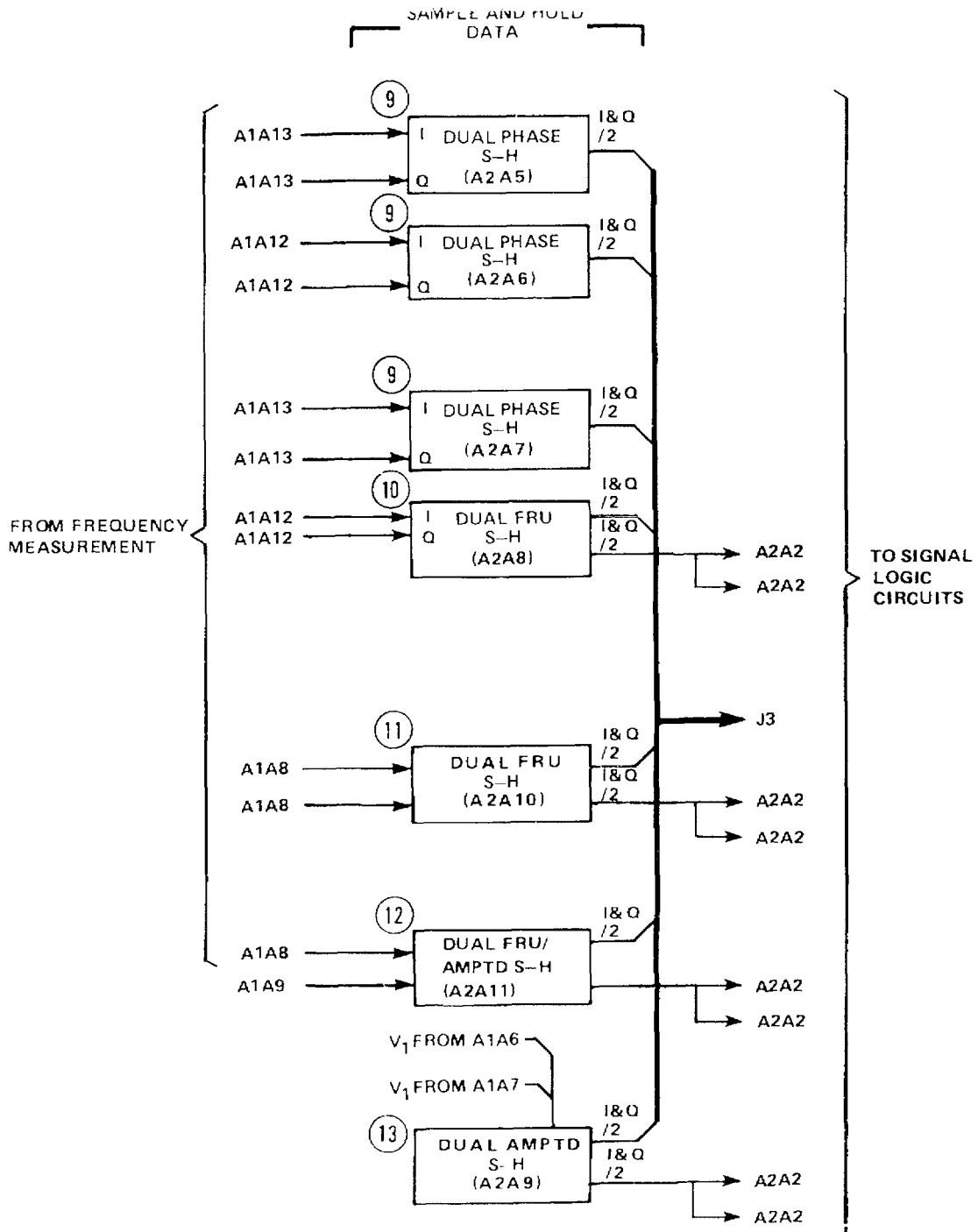
1-13. DETAILED OPERATION - Continued



**1-13. DETAILED OPERATION - Continued****c. Sample and Hold Data.**

- (9) **DUAL PHASE S-H (A2A5-A7).** Receives sample command from thr/gate gen (A2A3). Sample phase dependent voltage output from associated quad phase det (A1 A12 or A1 A13) and holds for computer processing.
- (10) **DUAL FRU S-H (A2A8).** Receives sample command from thr/gate gen (A2A3). Samples frequency dependent voltage output from dual phase det (A1A12) and holds for computer processing.
- (11) **DUAL FRU S--H (A2A10).** Samples frequency dependent output of coarse FRU (A1A8) 120 MHz and 180 MHz detectors, and holds for computer processing.
- (12) **DUAL FRU/AMPTD S-H (A2A11).** Consists of two subassemblies One subassembly input is amplitude dependent CH D from 150 MHz Imtr/log (A1A9). Other subassembly input is frequency dependent, 150 MHz detector output from coarse FRU (A1 A8). Each responds to sample commands from thr/gate gen (A2A3) through intfc logic (A2A1).
- (13) **DUAL AMPTD S-H (A2A9).** Samples amplitude dependent voltage output of 180 MHz IF (USB) (A1A6) and 120 MHz IF (LSB) (A1A7), and holds for computer processing.

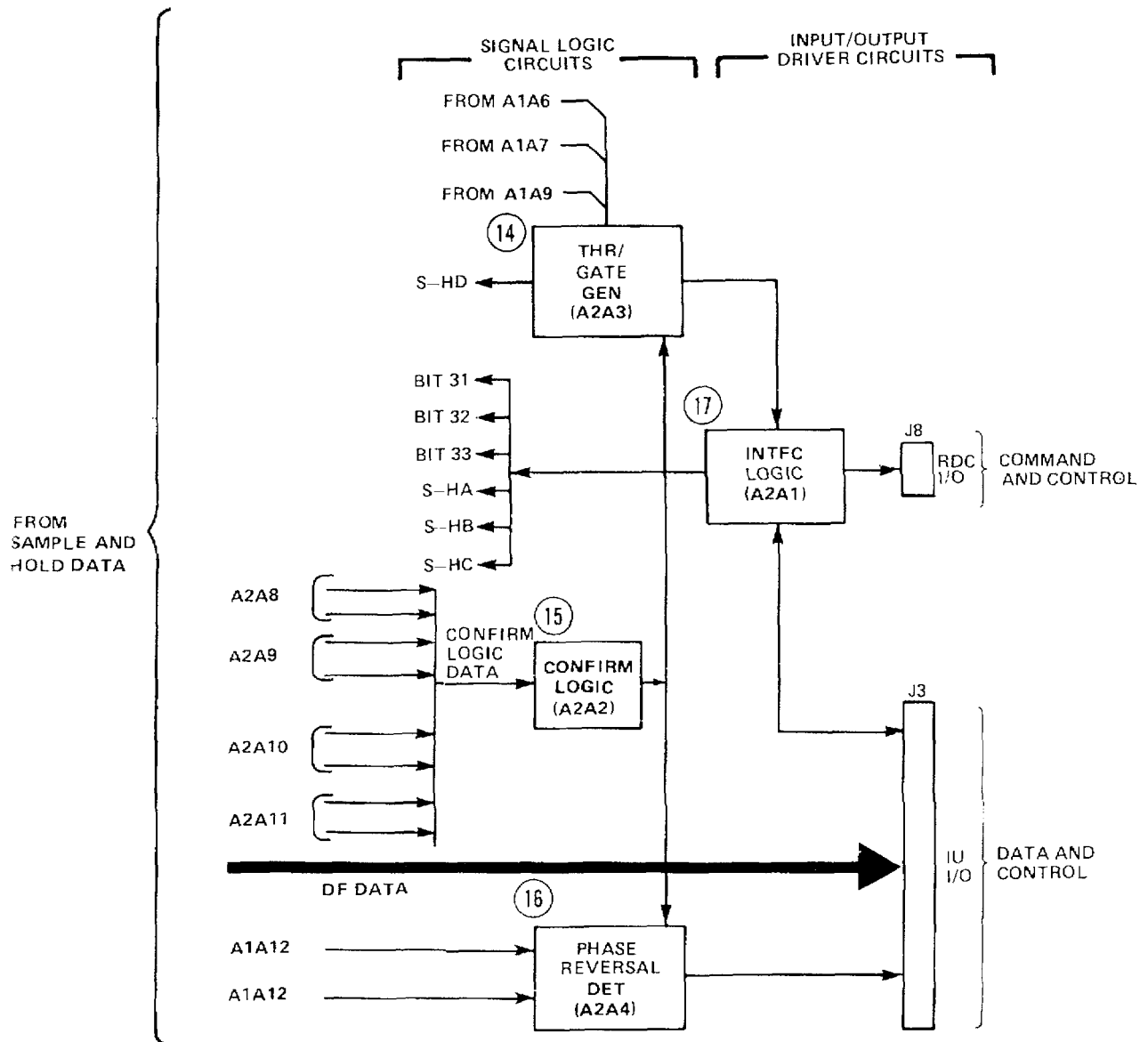
1-13. DETAILED OPERATION - Continued



**1-13. DETAILED OPERATION - Continued****d. Signal Logic and Input/Output**

- (14) **THR/GATE GEN (A2A3)**. Generates S-H commands and pulse width gate from either 180 MHz IF (USB) (A1A6) or 120 MHz IF (LSB) (A1A7) log outputs Sets receiver processing threshold.
- (15) **CONFIRM LOGIC (A2A2)**. Detects undesirable. spurious signals Outputs either a PW RESET signal which indicates a substandard signal, or a START TRIG which indicates signal quality is acceptable. Frequency, pulse width, and amplitude are checked.
- (16) **PHASE REVERSAL DET (A2A4)**. Receives I and Q inputs from quad phase det A (A1 A12), and outputs new pulse each time frequency change causes phase rollover.
- (17) **INTFC LOGIC (A2A1)**. Permits IFP to communicate with IU and RDC. Use for digital control signals only.

1-13. DETAILED OPERATION - Continued



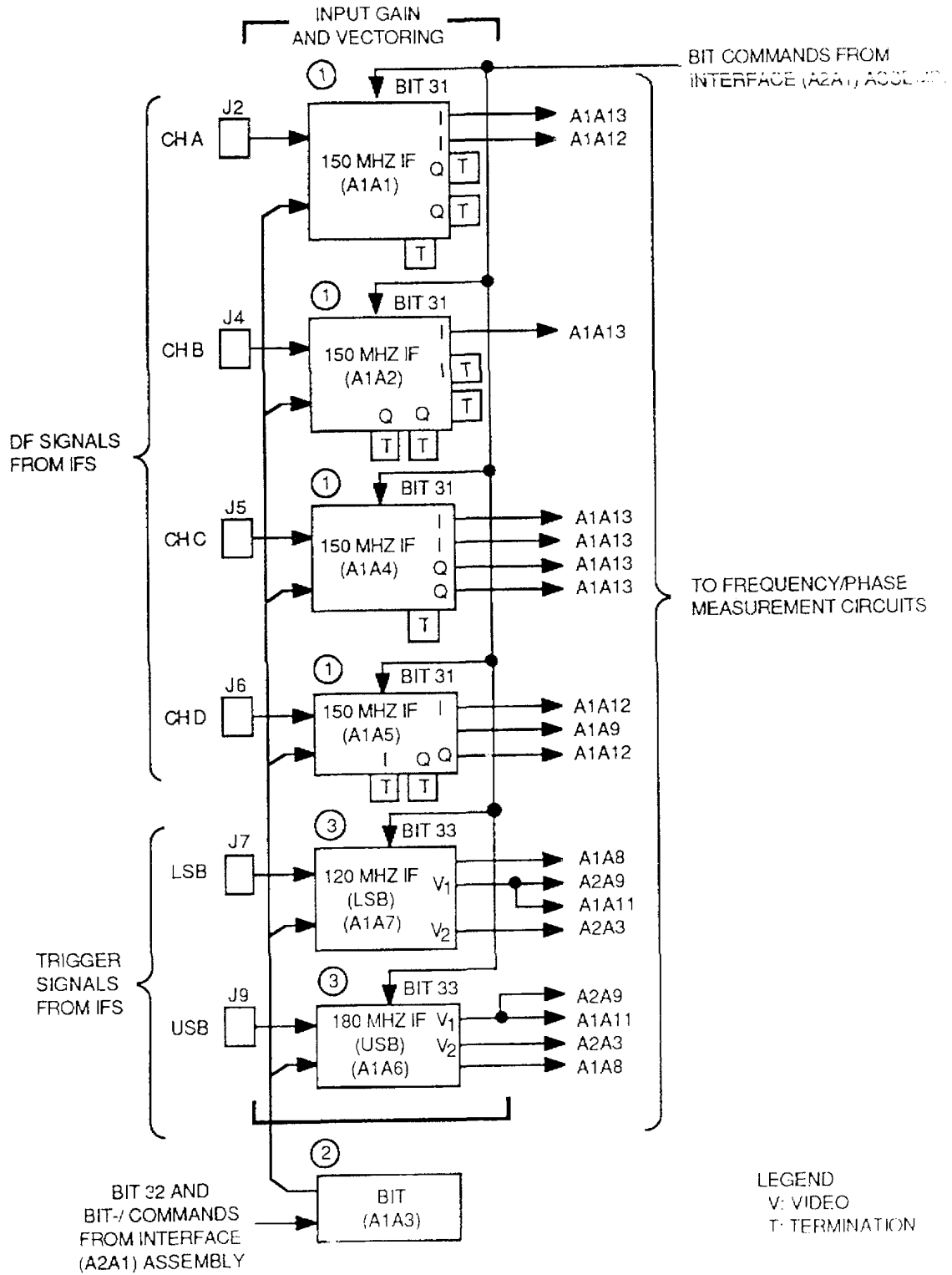
**1-13. DETAILED OPERATION - Continued**

The following is a more detailed coverage of the IFP operation. The detailed IFP overall functional block diagram is divided into four separate illustrations:

- Built-in-test (BIT), input gain, and vectoring circuits block diagram
- Frequency/phase measurement circuits block diagram
- Sample-and-hold data circuits block diagram
- Signal logic and input/output circuits block diagram

e. BIT. Input Gain and Vectoring Circuits. Refer to the BIT, input gain, and vectoring circuits block diagram.

- (1) **150 MHz IF (A1A1, A1A2, A1 A4, A1 A6).** Each of the four modules receives df signals from the IFS or test signals from the BIT (A1A3) assembly. Either signal is processed depending upon the BIT 31 command received from the RDC via the interface (A2A1) assembly.. BIT 31 command switches the inputs of the four modules from the DF signal to the test signal during BIT. The selected signals are tuned by the wideband bandpass filter, limited, amplified. and phase-shifted (by the 90-degree hybrid shift network). This provides two pairs of similar signals (one pair is 90-degree phase-shifted).
- (2) **BIT (A1A3).** The BIT (A1A3) assembly receives command signals from the RDC via the interface (A2A1) assembly and outputs test signals to each of the six if. assembly modules (A1 A1), A1 A2. A1 A5, A1A6, A1A7). The BIT -/ command is derived from BIT 31 and BIT 33 commands and is used to activate the test signal BIT 32 command is used to switch the test signal between the USB trigger and the LSB trigger channels.
- (3) **180 MHz IF UPPER SIDEBAND (USB) (A1A6), and 120 MHz IF LOWER SIDEBAND (LSB) (A1A7).** Each of the two modules receives trigger signals from the IFS or test signals from the Bit (A1A3) assembly. Either of the signals is processed depending upon RDC BIT 33 command received via the interface (A2A1) assembly. BIT 33 command switches the inputs of the two modules from the trigger signal to the test signal during BIT. The selected signals are bandwidth limited by the bandpass filter, limited, and amplified. Two kinds of limited outputs are provided: a limited signal power output and a dc log voltage output (input signal level dependent).



BIT, INPUT GAIN, AND VECTORING CIRCUITS BLOCK DIAGRAM

**1-13. DETAILED OPERATION - Continued**

- f. 150 MHz IF (A1A1, A1A2, A1A4, A1A5) Refer to the 150 MHz IF (A1A1, A1A2, A1A4, A1A5) block diagram and the BIT, input gain, and vectoring circuits block diagram Each of the four modules receives df signals from the IFS or test signals from the BIT (A1A3) assembly Either signal is processed depending upon the BIT 31 command received from the RDC via the Interface (A2A1) assembly BIT 31 command switches the inputs of the four modules from the DF signal to the test signal during BIT The selected signals are tuned by the wideband bandpass filter, limited, amplified, and phase-shifted (by the 90-degree hybrid shift network) This provides two pairs of similar signals (one pair is 90-degree phase-shifted).

**NOTE**

The four 150 MHz limiter if. modules (A1 A1 , A1 A2, A1 A4, A1 A5) are assigned serial numbers and supplied (and maintained) as a matched set. The following discussion is representative of each of the four 150 MHz limiter if modules.

(1) Inputs.

- **BIT 31**
- **TEST SIGNAL**
- **DFIN**

(2) Outputs.

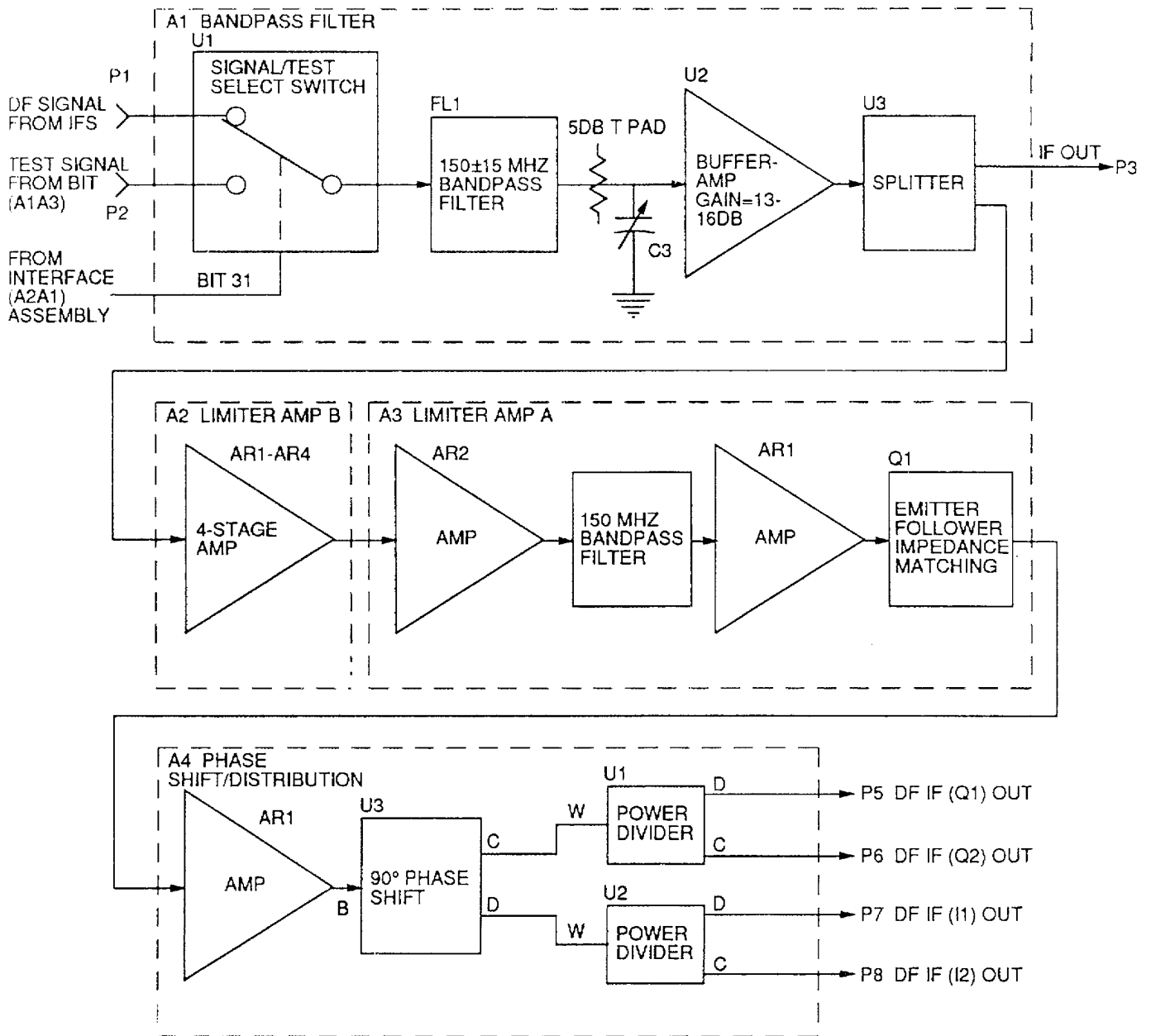
- **DF IF (11) OUT**
- **DF IF (12) OUT**
- **DF IF (Q1) OUT**
- **DF IF (Q2) OUT**
- **IF OUT**

(3) First Stage Signal Processing.

- Received mission signals enter the appropriate df channel if. module at coaxial connector P1. If selected, BIT signals enter at coaxial connector P2. Monolithic switch A1 U1, under control of the BIT control signal BIT 31, selects one of the two input signals for processing.
- The selected signal is applied to bandpass filter A1 FL1. A1 FL1 has a total 3 dB bandwidth of 30 MHz, centered at 150 MHz.
- The 5 dB T-pad following A1 FL1 performs several functions. it provides an accurate termination for filter A1 FL1, includes adjustable phase-shift compensation in the form of variable capacitor A1 C3, and prevents overloading amplifier A1 U2.
- The signals are amplified by A1 U2, a packaged very high frequency (VHF) amplifier with 13 to 16 dB of gain.
- From A1U2, the signals are sent to a two-way in-phase power divider, A1U3. One of the outputs of A1 U3 goes directly to IF OUT connector P3 This signal is used only on the df channel D if. module, from which it drives the 150 MHz limiter/log assembly and eventually the 150 MHz fine FRU.
- The second power divider output goes to the limiting amplifier chain



1-13. DETAILED OPERATION - Continued



150 MHz IF (A1A1, A1A2, A1A4, A1A5) BLOCK DIAGRAM

**1-13. DETAILED OPERATION - Continued**

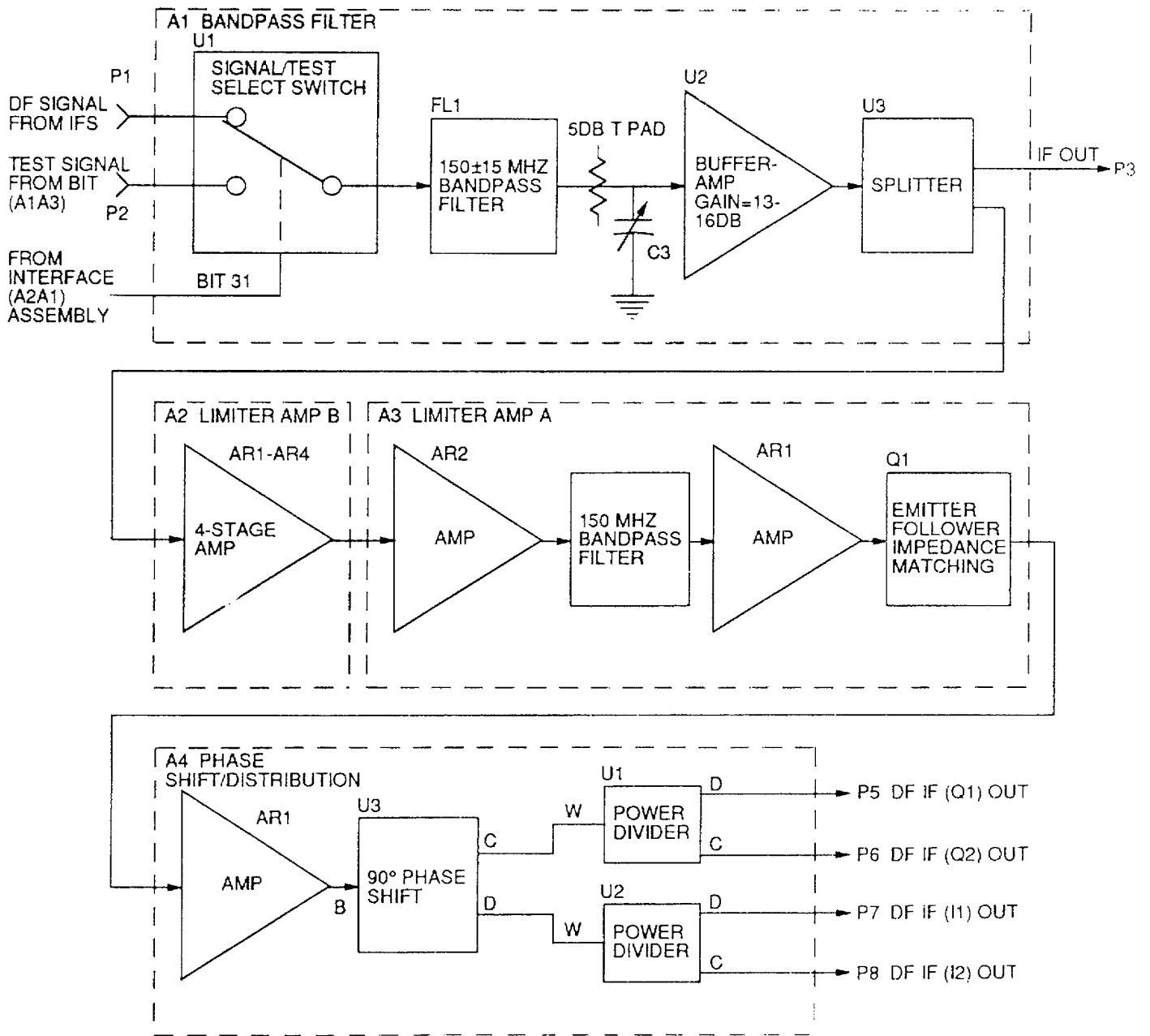
(4) Second Stage Signal Processing. The next section of the 150 MHz if. module is a six stage limiter composed of subassemblies A2 and A3.

- Subassembly A2 is limiter amplifier B, consisting of amplifiers A2AR1 through A2AR4.
- Subassembly A3 is limiter amplifier A, consisting of amplifiers A3AR2 and A3AR1. A simple 150 MHz bandpass filter is inserted before the last limiting amplifier stage to prevent overload from broadband noise originating in the receiver front end.
- Since the limiting amplifier cannot drive 50 ohm loads directly, emitter follower A3Q1 is used as an impedance matching stage.

(5) Third Stage Signal Processing. The last section of the 150 Mhz limiter if. module, the A4 subassembly, is a phase-shift and signal distribution circuit.

- The 1 volt peak-to-peak (zero dB) signal from the limiter section is amplified by 13 dB to 16 dB by A4AR1.
- From A4AR1, the amplified signals are sent to a 90-degree phase-shift hybrid, A4U3.
- Signals from the A4U3 in-phase output (port D) are split by power divide A4U2 and sent to output connectors P7 and P8 as the DF IF OUT (I) signals.
- Similarly, the A4U3 quadrature output signal (90-degree lagging in phase) from port C is split by A4U1 and becomes the DF IF OUT (Q) signals at P5 and P6.
- Signals at the four I and Q outputs (P5, P6, P7, P8) have an amplitude of approximately + 8 dBm. The I and Q outputs are compared in pairs by the quad df phase detectors (A1A12 and A1A13).

1-13. DETAILED OPERATION Continued



150 MHz (A1A1, A1A2, A1A4, A1A5) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION - Continued

g 180 MHz IF USB (A1A6) and 120 MHz IF LSB (A1A7). Refer to the 180 MHz IF (USB) (A1A6) and 120 MHz IF (LSB) (A1A7) block diagram and the BIT input gain and vector-ing circuits block diagram Each of the two modules receives trigger signals from the IFS or test signals from the BIT (A1A3) assembly Either of the signals is processed depending upon RDC BIT 33 command received via the interface (A2A1) assembly BIT 33 command switches the Inputs of the two modules from the trigger signal to the test signal during BIT The selected signals are bandwidth limited by the bandpass filter, limited, and amplified. Two kinds of limited outputs are provided: a limited signal power output and a dc log voltage output (input signal level dependent)

(1) Inputs.

- Trigger signals from the IFS
- Test signal from the BIT (A1A3) assembly
- BIT 33 from the interface (A2A1) assembly

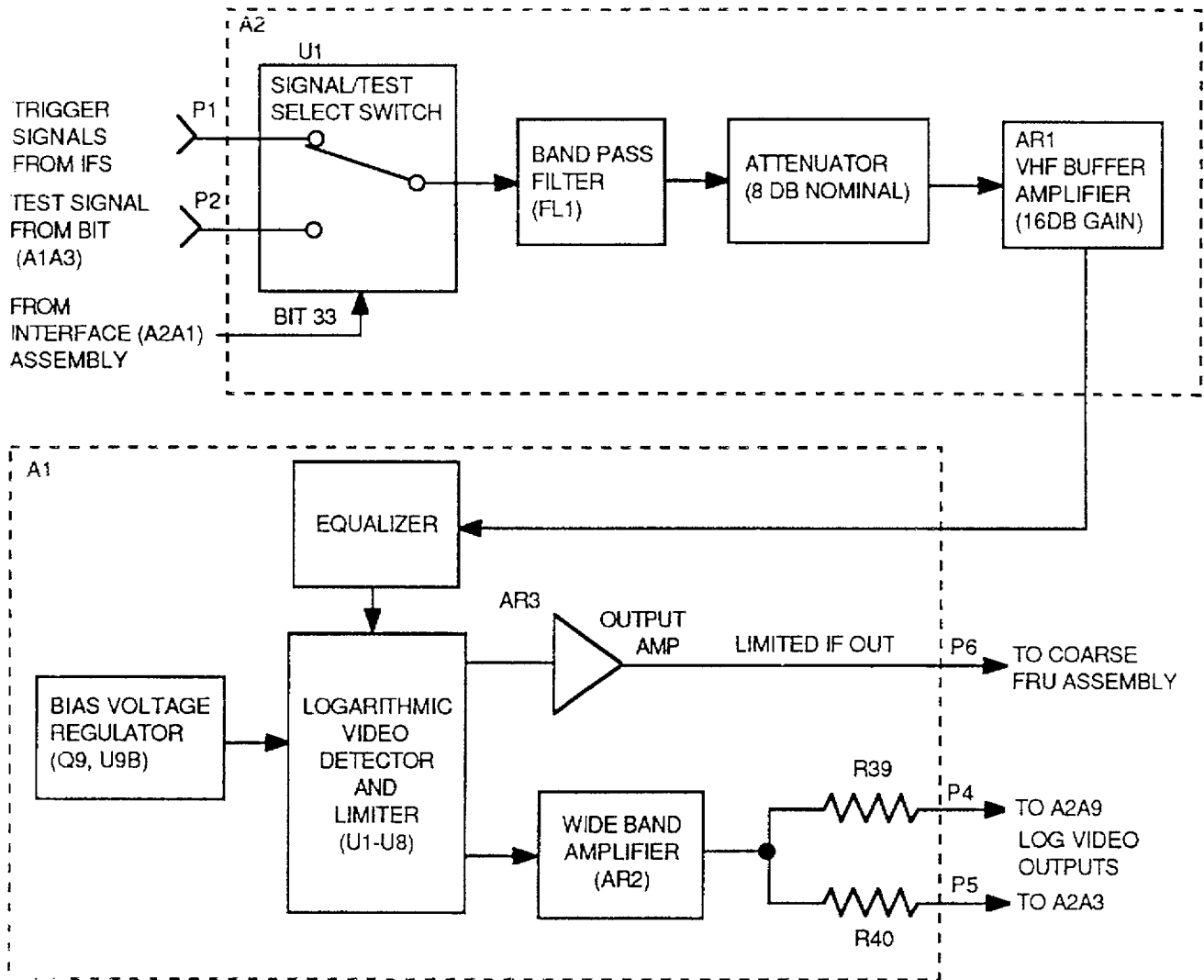
(2) Outputs.

- LIMITED IF OUT
- LOG VIDEO

(3) Signal Processing.

- Received mission signals enter the appropriate trigger channel module at coaxial connector P1. If selected, IFP built-in test (BIT) signals enter at P2. Monolithic switch A2U1, under control of the BIT control signal BIT 33, selects one of the two input signals for processing.
- The selected signal is applied to bandpass filter A2FL1, which has a total 3 dB bandwidth of 30 MHz, centered on the module's specified center frequency. The attenuator following A2FL1 provides an accurate termination as well as preventing overload of amplifier A2AR1.
- The signals are amplified by A2AR1, a packaged VHF amplifier with 13 to 16 dB of gain. From A2AR1, signals are sent to an equalizer circuit. The values of the equalizer components differ in the 120 MHz and 180 MHz modules to allow for the module's respective center frequency This circuit provides frequency response equalization, tending to flatten the response within FL1's passband.
- The next section of the if. module is a logarithmic video detector and limiter (U1-U8). The log video detector uses eight limiting amplifiers in a successive detection configuration with approximately 85 dB of dynamic range. The two types of if. modules use slightly different values of interstage coupling and compensation components between the log detector stages, due to their different center frequencies.
- The bias voltage regulator (Q1, U9B) controls the bias applied to the limiting amplifiers and therefore amplifier gain.
- The logarithmic video detector and limiter has two outputs. The first is an amplified i f. signal limited to 1 volt peak-to-peak The second is a log video signal.

1-13. DETAILED OPERATION -Continued

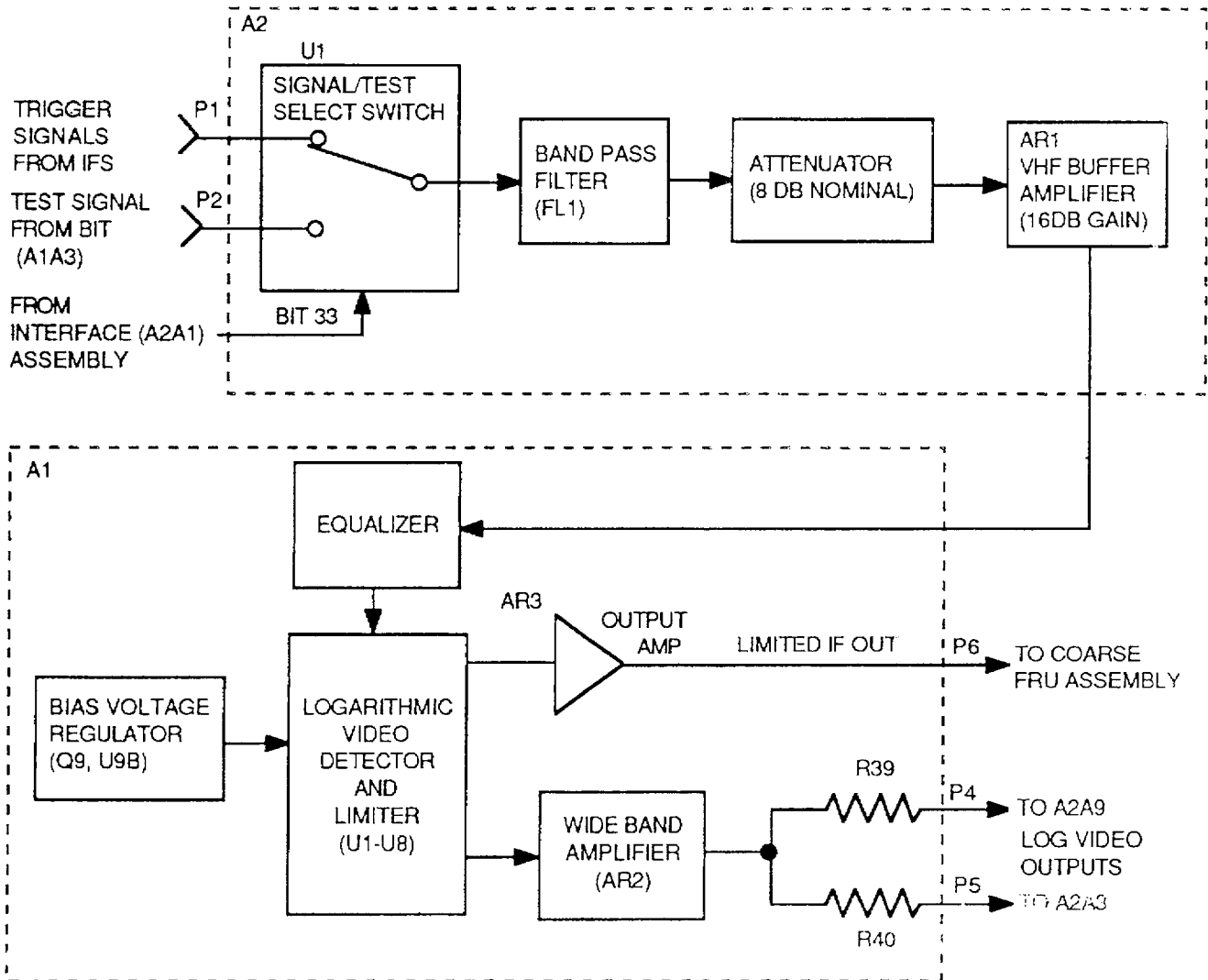


180 MHz IF (USB) (A1A6), AND 120 MHz IF (LSB) (A1A7) BLOCK DIAGRAM

**1-13. DETAILED OPERATION** - Continued

- The limited if. signal is buffered and amplified in A1AR3 to approximately 7.0dBm, then sent to the appropriate coarse FRU assembly via output coaxial connector P6. The log video signal is amplified by wideband op-amp A1 AR2 and sent to video output connectors P4 and P5.
- Resistors R39 and R40 establish a nominal 93 ohm characteristic impedance at the log video outputs, where the nominal signal levels (across a 93 ohm termination) range from 0.5V to 5.0V with a 75 mV/dB scale factor.

1-13. DETAILED OPERATION -Continued



180 MHz IF (USB) (A1A6), AND 120 MHz IF (LSB)(A1A7) BLOCK DIAGRAM

**1-13. DETAILED OPERATION** - Continued

h. BIT (AA 3). Refer to the BIT (A1A3) block diagram and the BIT, input gain, and vector-ing circuits block diagram. The BIT (A1A3) assembly receives command signals from the RDC via the interface (A2A1) assembly and outputs test signals (BIT outputs) to each of the six if assembly modules (A1A1, A1A2, A1A4, A1A5, A1A6, A1A7). The BIT-/ command is derived from BIT 31 and BIT 33 commands and is used to activate the test signal BIT 32 command is used to switch the test signal between the USB trigger and the LSB trigger channels.

(1) Inputs.

- BIT -/ Signal from interface (A2A1) assembly
- BIT 32 Signal from interface (A2A1) assembly

(2) Outputs.

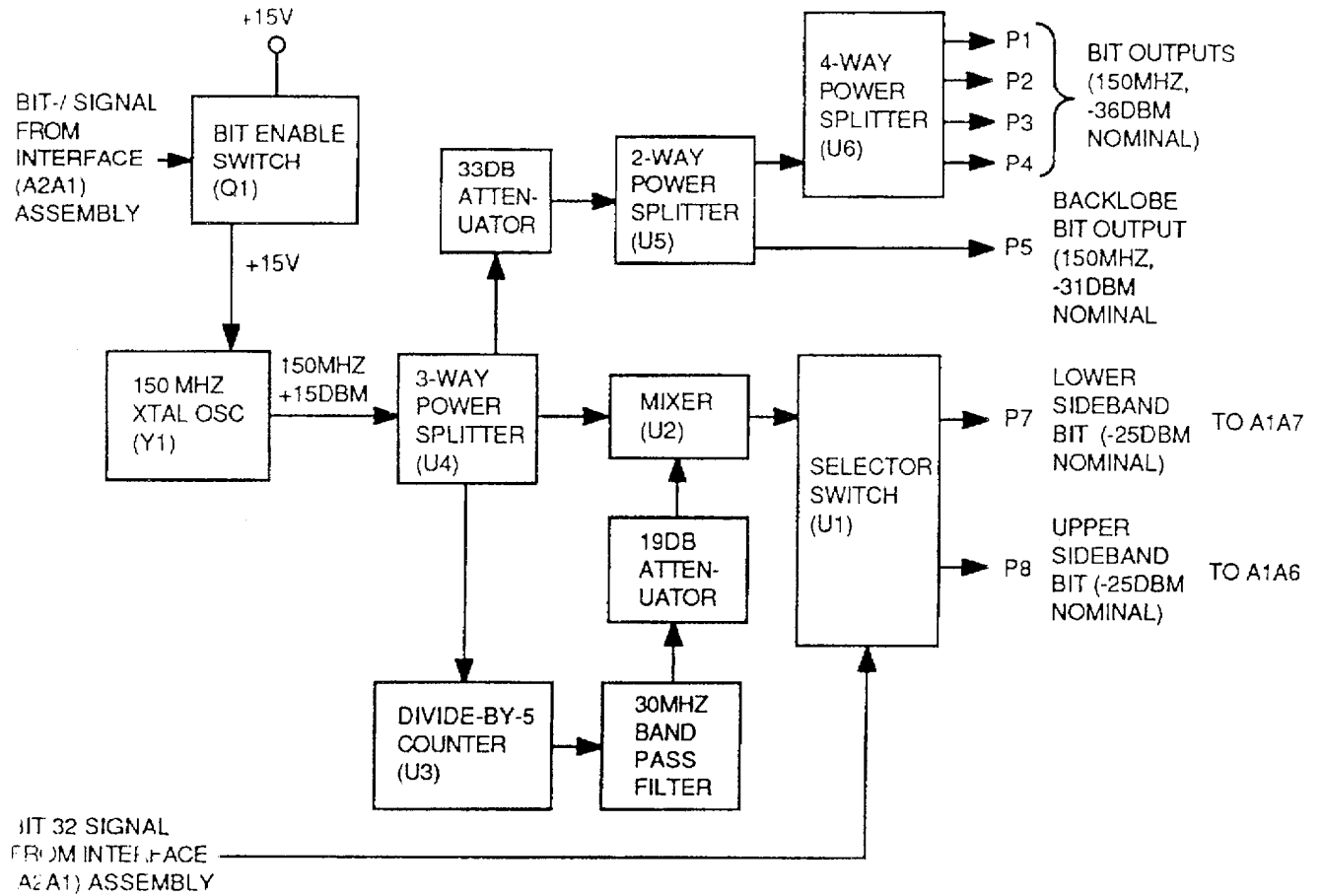
- Test Signals to 150 MHz if., 180 MHz if. and 120 MHz if. Modules
- Backlobe BIT Output (not used)

(3) Signal Processing.

- The required test signals originate in a modular 150 MHz crystal oscillator (Y1). Dual transistor Q1 forms a switch to apply power to the oscillator when the BIT -/ signal is a logic low. The logic low occurs when either of the two BIT modes is being requested. When power is not applied to Y1, there are no output signal from the IFP BIT assembly.
- Power splitter U4 splits the oscillator output signal into three signals, each with an amplitude of approximately + 5 dBm.
- One of the output signals from U4 is attenuated by 33 dB and further split by two-way power divider U5.
- One output from U5, BACKLOBE BIT OUTPUT, is not used in AQL. The other output from U5 is applied to four-way power splitter U6.
- The outputs from U6 are 150 MHz signals at approximately -36 dBm, and are routed via coaxial connectors P1 through P4 to the four df channels in the IFP.
- The other two outputs from three-way splitter U4 are used to create BIT signals for the USB and LSB trigger channels in the IFP
- One output from U4 feeds the input of divide-by-five counter U3 whose out-put is a 30MHz square wave. This square wave is filtered to remove harmonics and attenuated, leaving a 30 MHz sine wave at a level of approximately 30 dBm. This signal is mixed with the third output from U4 in double-balanced mixer U2. The mixer output consists primarily of the sum and difference frequencies of its input signals: 180 MHz (150 MHz plus 30 MHz) and 120 MHz (150 Mhz minus 30 MHz).



1-13. DETAILED OPERATION - Continued

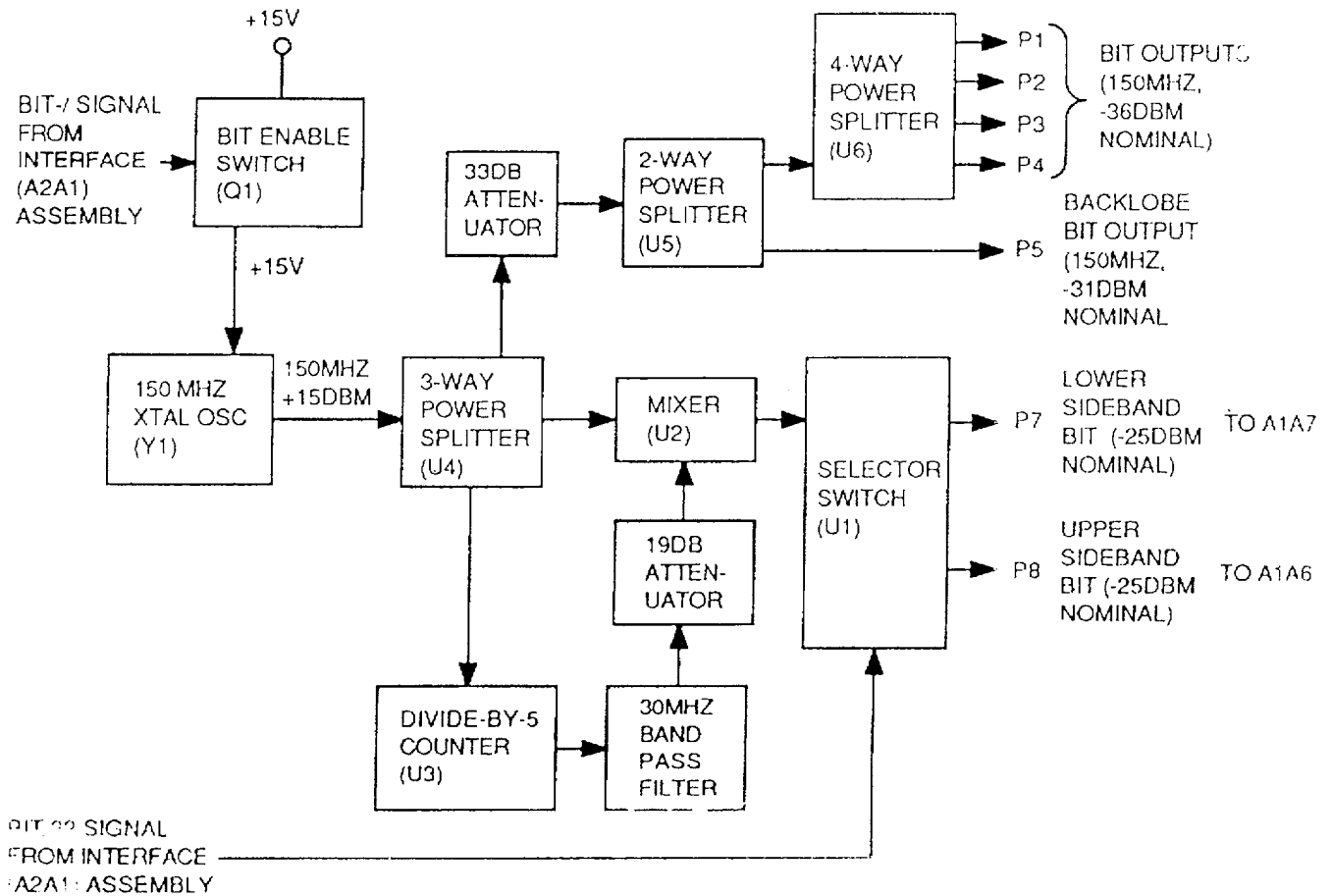


BIT (A1A3) BLOCK DIAGRAM

**1-13. DETAILED OPERATION** - Continued

- Selector switch U1, controlled by the BIT 32 signal, routes this composite test signal to either the LSB or USB test inputs in the trigger channel if. assemblies via connector P7 or P8. When BIT 32 is a logic high, the USB assembly receives the test signal. Conversely, a logic low on BIT 32 directs the test signal to the LSB channel. Although this test signal contains roughly equal power at both USB (180 MHz) and LSB (120 MHz) frequencies, filters in the trigger channel if. assemblies pass the appropriate signal and reject the opposite sideband frequencies.

1-13. DETAILED OPERATION - Continued

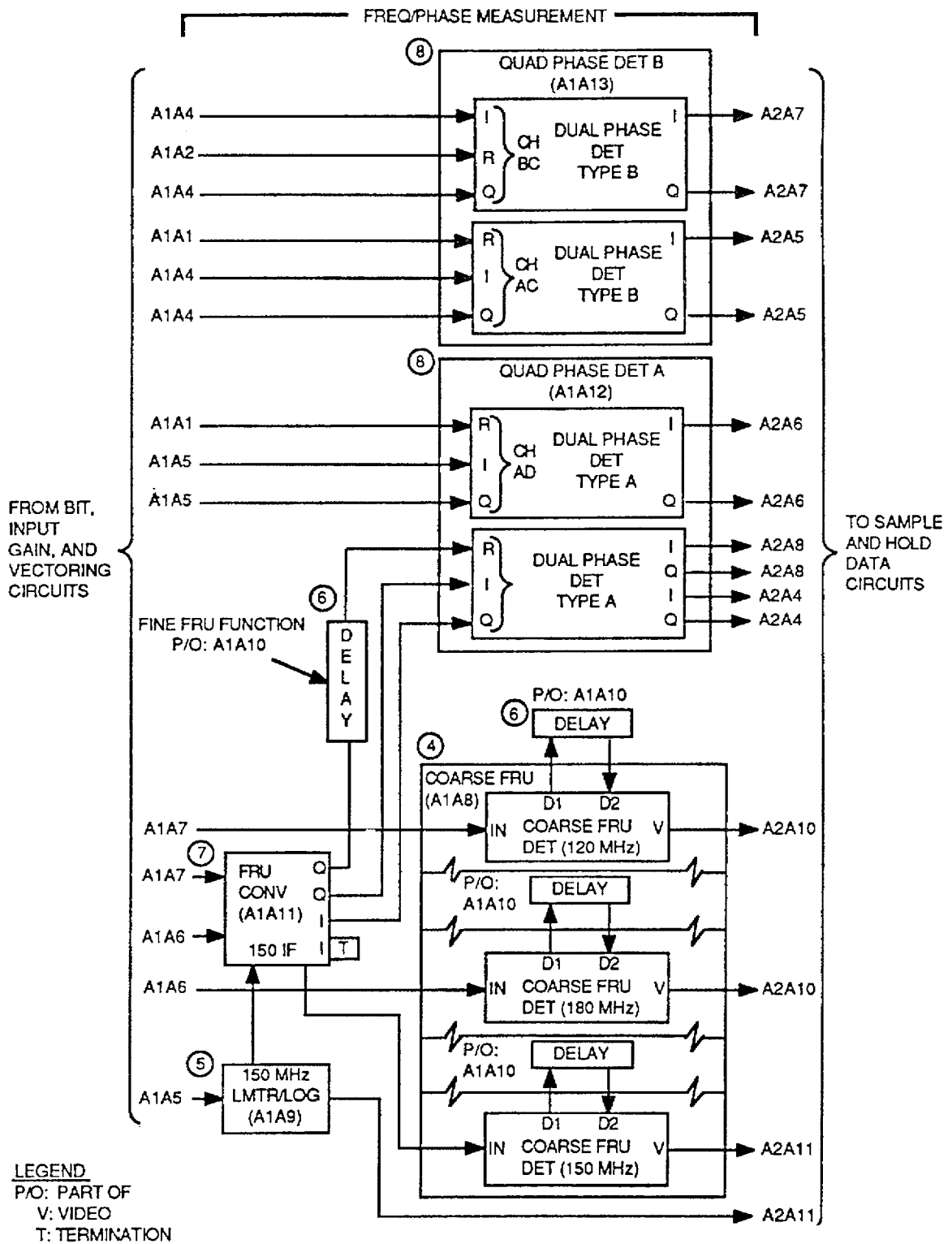


BIT (A1A3) BLOCK DIAGRAM

**1-13. DETAILED OPERATION** - Continued

- i. Frequency/Phase Measurement Circuits. Refer to the frequency/phase measurement circuits block diagram
- (4) **COARSE FREQUENCY RESOLVING UNIT (FRU) (A1A8).** Receives inputs from trigger channel if cards (A1A6 and A1A7) and df channel "D" (via A1A 11) Contains three coarse FRU Frequency measurements are made in terms of phase-shift measure-ments FRU output video signals with instantaneous voltage proportional to received signal frequencies.
- (5) **150 MHz LIMITER/LOG (A1 A9).** Receives inputs from CH D 150 MHz if. (A1A5) and provides two kinds of outputs: limited if. output signal and log video output (dependent on amplitude of input) signal. The limited if. output signal is an amplified and amplitude limited (+ 7dBm) signal which is applied to the FRU converter (A1A11) The log video output signal is the result of a logarithmic measurement of the received signal level in DF channel D as well as the upper and lower sideband channels. Therefore the log video output signal will vary from a do level to an instantaneous voltage. This signal is routed to the Dual Sample and Hold (A2A1 1) assembly.
- (6) **DELAY LINE (A1A10).** Consists of four separate delay lines: three used by the coarse FRU (A1A8), and one for the fine FRU (A1A12A1). Works with coarse FRU (A1A8) and quad phase det A (A1A12) to provide linear phase change for frequency measurement
- (7) **FRU CONVERTER (A1A11).** Receives inputs from 150 MHz limiter. log (A1A9). Outputs two Q and two I signals for frequency measurement. The quadrature (Q) output has a 90-degree phase difference from reference and the in-phase (I) outputs have a zero phase difference from the reference.
- (8) **QUAD PHASE DETECTOR (A1A12, A1A13).** Detects phase difference between inphase channel inputs and quadrature channel inputs, generating analog voltage out-puts Quad phase detector module contains two dual phase detector subassemblies. I and Q outputs are changing voltages proportional to input phase differences.

1-13. DETAILED OPERATION -Continued



FREQUENCY/PHASE MEASUREMENT CIRCUITS BLOCK DIAGRAM

**1-13. DETAILED OPERATION - Continued**

j. Coarse FRU (A1 A8) and Delay Line (A1A10). Refer to the coarse FRU (A1 A8) module block diagram and the frequency/phase measurement circuits block diagram. The coarse FRU receives inputs from the A1A6, A1A7, and A1A11 modules. The IFP measures the frequency of signals received on df channel D as well as both trigger channels (LSB and USB) using delay line discriminators composed of the delay line assembly and the coarse FRU. The coarse FRU actually contains three FRU detector circuits, one for each trigger channel and one for the 150 MHz df channel. The two trigger channel circuits are electrically identical; the df channel circuit is different in only one component choice. Frequency determinations are made in terms of phase-shift measurements. Outputs are in do amplitude variations proportional to frequency.

(1) Inputs.

- 120 MHz, 150 MHz, and 180 MHz IF

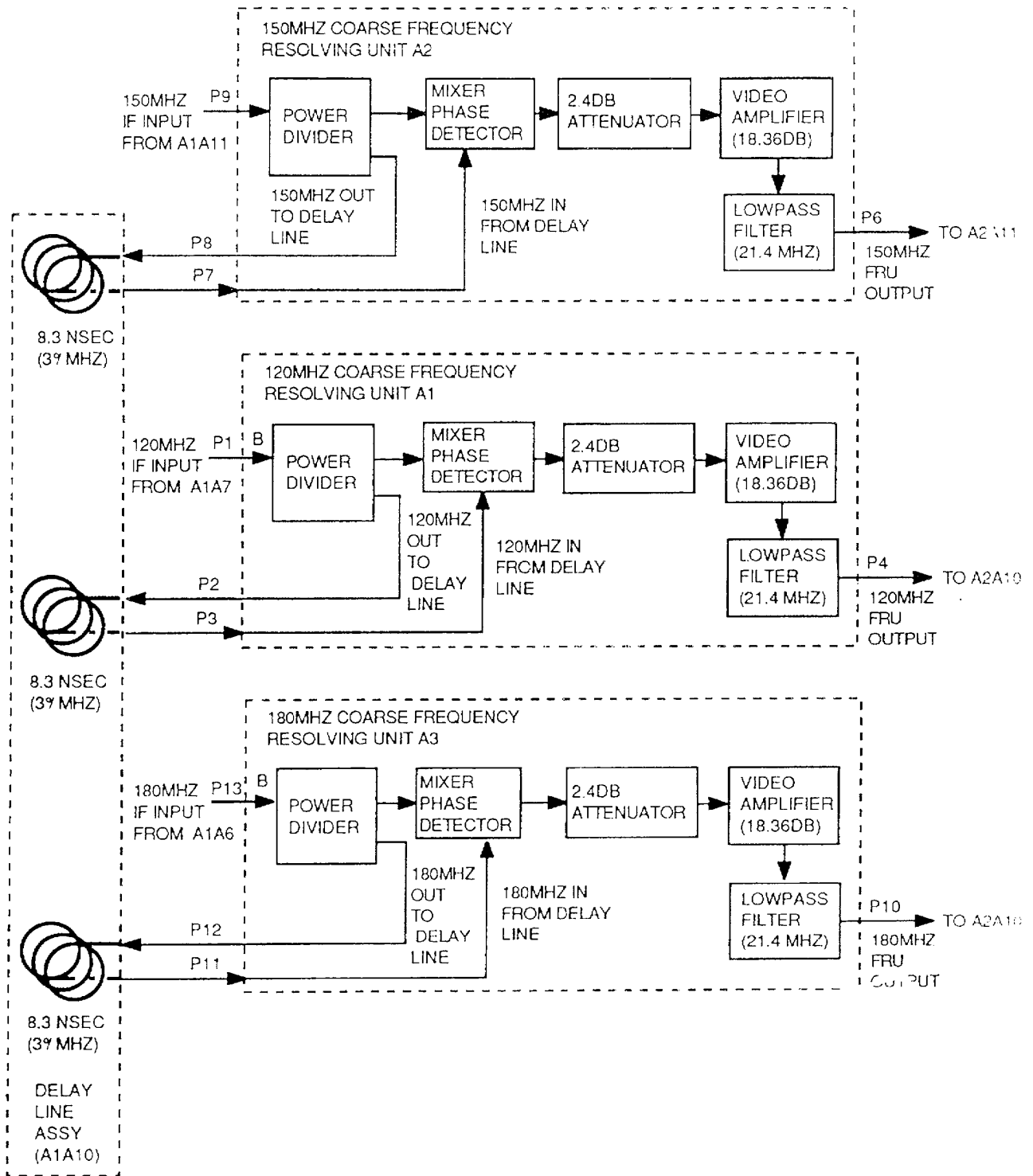
(2) Outputs.

- 120 MHz, 150 MHz, and 180 MHz FRU

(3) Signal Processing.

- Each FRU is a delay line discriminator circuit using a double-balanced mixer phase detector, followed by a 2.4 dB attenuator, an integrated circuit video amplifier and lowpass output filter. A delay line discriminator generates a dc voltage based on phase variations of the incoming signal frequency. The frequency is determined by comparing the phase of the original frequency and the phase of a delayed version of the original frequency. The delay time is fixed, therefore if the frequency varies, the phase difference also varies and subsequently the dc voltage output level.
- Signals entering each section (120, 150, 180 MHz) of the coarse FRU are first split by a power divider. One of the two divider outputs is applied directly to the mixer phase detector. The other output is routed through an 8.3 nsec delay line and is also applied to the mixer phase detector. These two signals are compared and the resulting phase shift is used by the mixer phase detector to generate a dc output voltage proportional to the phase shift.
- The mixer phase detector output passes through a 2.4 dB attenuator, which ensures a good resistive termination for the mixer's if, port, and then is applied to a video amplifier. The video amplifier stage is based on a high-speed operational amplifier integrated circuit.
- The video amplifier output passes through a 21.4 MHz lowpass filter before leaving the coarse FRU assembly to feed the appropriate sample-and-hold circuit. The video stage voltage gain, measured from the attenuator output to a 50 ohm termination on the FRU output, is 8.25 (18.4 dB).

1-13. DETAILED OPERATION-Continued



COARSE FRU (A1A8) BLOCK DIAGRAM

**1-13. DETAILED OPERATION** - Continued

k. 150 MHz LIMITER/LOG (A1A9). Refer to the 150 MHz limiter log (A1A9) block diagram and the frequency/phase measurement circuits block diagram. The 150 MHz limiter log module amplifies, limits, and logarithmically detects the signal from df channel D, and provides two kinds of outputs: limited if. output signal and log video output (signal level dependent on amplitude of input) signal.

(1) Inputs.

- 150 MHz IF

(2) Outputs.

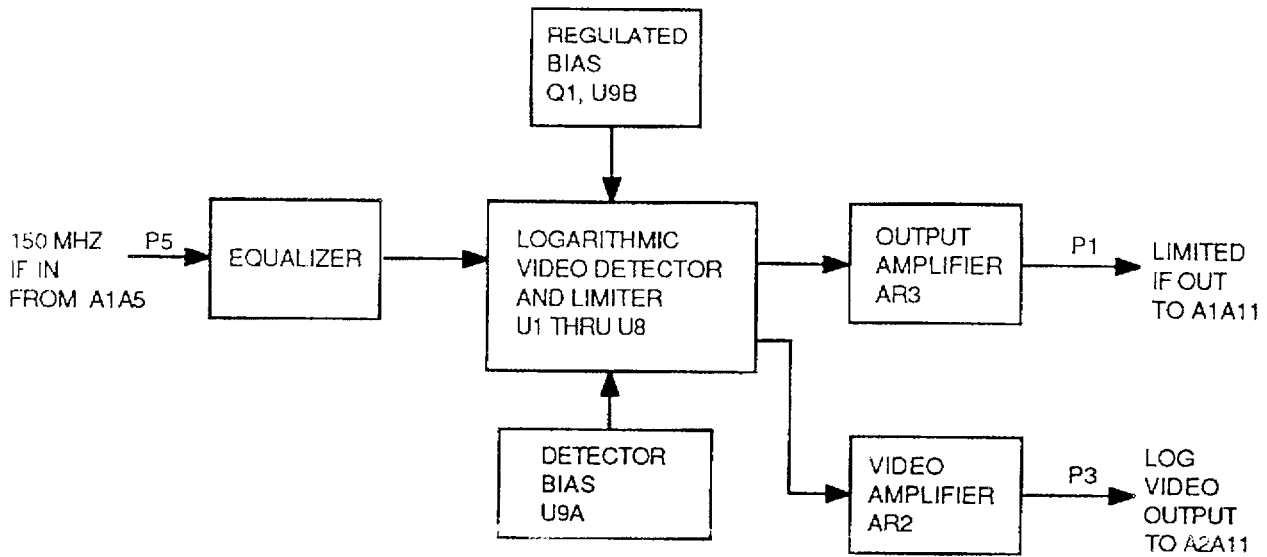
- LIMITED IF OUT
- LOG VIDEO OUTPUTS

(3) Signal Processing.

- Received mission signals, after filtering and amplification in the df channel D 150 MHz if. assembly, enter the 150 MHz limiter/log if. module at coaxial connector P5. The signals then pass through an equalizer circuit. This circuit provides frequency response equalization to flatten response within the 150 MHz passband.
- The next section of the if. module is a logarithmic video detector and limiter (U1 -U8). The log video detector uses seven limiting amplifiers in a successive detection configuration with approximately 85 dB of dynamic range. The two limiting stages associated with the very highest signal levels are driven through a simple voltage divider. Transistor Q1 and op-amp U9B form a series regulator for the limiting amplifier's bias voltage.
- The bias voltage regulator (Q1, U9B) controls the bias applied to the limiting amplifiers and therefore amplifier gain.
- Op-amp U9A provides a small forward bias current for the log video detector diodes. The small forward bias improves the accuracy of the detector's log curve.
- The log video detector and limiter has two outputs: an amplified if. signal limited to 1 volt peak-to-peak, and a log video signal. The limited if. signal is buffered and amplified in AR3 to approximately + 10.0 dBm, then sent to the 150 MHz FRU converter assembly via output coaxial connector P1. The log video output signal is amplified by wideband op-amp AR2 and sent to video output connectors P2 and P3.



1-13. DETAILED OPERATION - Continued



150 MHz LIMITER/LOG (A1A9) BLOCK DIAGRAM

**1-13. DETAILED OPERATION - Continued**

I. FRU CONVERTER (A1AA1). Refer to the FRU converter (A1A11) block diagram and the frequency/phase measurement circuits block diagram. The IFP FRU converter assembly performs two unrelated tasks. The first is amplifying and distributing 150 MHz signals from df channel D to the coarse and fine FRUs. The second is determining from the trigger channel log amplitude signals whether a received pulse is within a frequency range where the AQL system can accurately process it without re-tuning. The FRU converter outputs two Q and two I signals for frequency measurement. The 0 outputs have a 90-degree phase difference from reference and the I outputs have a zero phase difference from the reference.

**(1) Inputs.**

- IF IN
- USB VIDEO
- LSB VIDEO
- STROBE

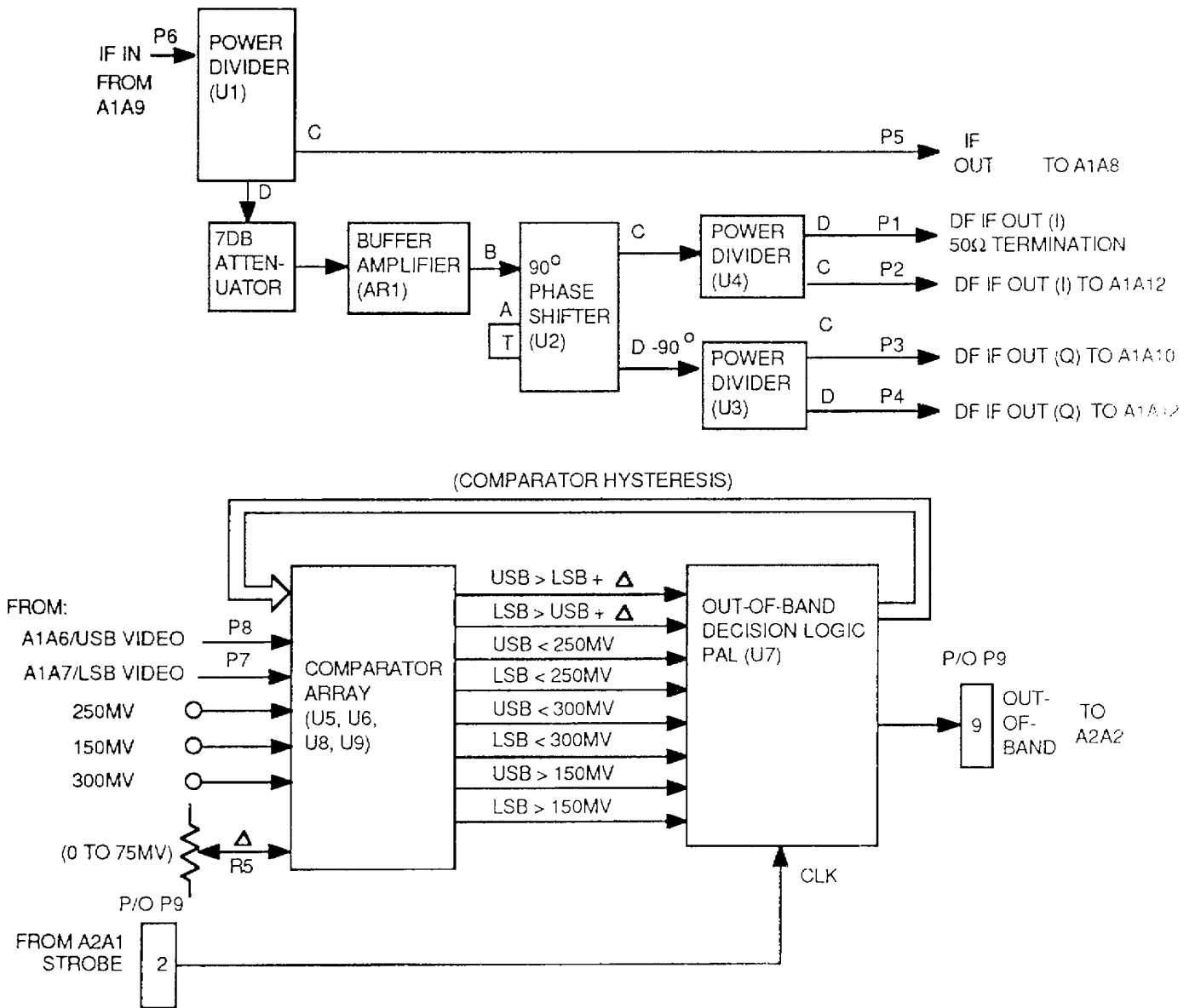
**(2) Outputs.**

- IF OUT
- DF IF OUT (I)
- DF IF OUT (Q)
- OUT-OF-BAND

**(3) Signal Processing.**

- 150 MHz signals from the df channel D if. assembly enter the FRU converter at P6 and are split by power divider (U1). One output from U1 goes directly to module output connector P5 and becomes the input signal to the 150 MHz coarse FRU. The other output from U1 passes through a 7 dB attenuator and is applied to AR1.
- AR1, a packaged VHF amplifier with 13 to 16 dB of gain, amplifies the signals and applies them to 90-degree hybrid U2. Signals from U2's in-phase output (port C) are split by power divider U4 and sent to output connectors P1 and P2 as DF IF OUT (I).
- Similarly, U2's quadrature output signal (90 degrees lagging in phase) from port D is split by power divider U3 and becomes DF IF OUT (Q) at P3 and P4. Signals at the I and Q outputs (P1 through P4) have approximately the same amplitude as the 150 MHz input signal at P6.
- The second function of the FRU converter is to determine from detected video signals whether or not a received signal is within a frequency band that can be accurately processed. The result of this determination is indicated by the OUT-OF-BAND signal (--L level) which is sent to the confirm logic assembly (A2A2).

1-13. DETAILED OPERATION - Continued



FRU CONVERTER (A1A11) BLOCK DIAGRAM

**1-13. DETAILED OPERATION** - Continued

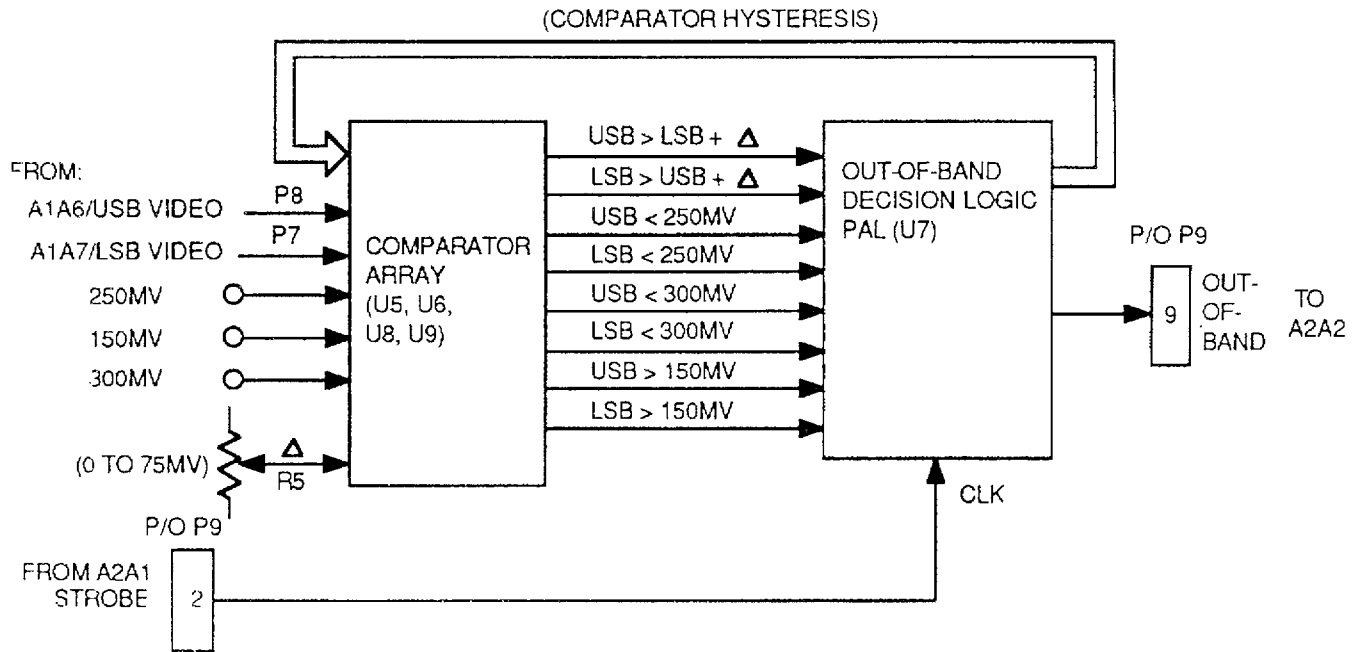
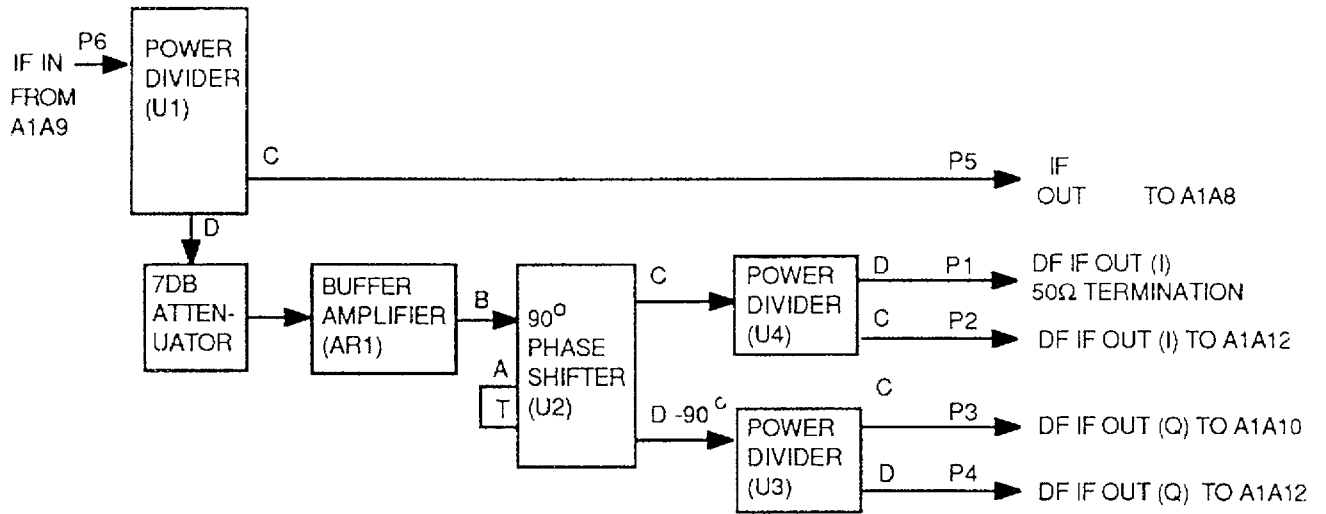
The out-of-band determination is made in two steps. First, the two trigger channel log amplitude signals, USB VIDEO and LSB VIDEO, are compared to various thresholds and each other in a comparator array consisting of U5, U6, U8, and U9. Each of the eight comparator logic outputs represents one of the following conditions:

- LSB Video > 150 mV
- LSB Video < 300 mV
- LSB Video < 250 mV
- LSB Video > (USB Video + A)
- USB Video > 150 mV
- USB Video < 300 mV
- USB Video < 250 mV
- USB Video > (LSB Video + A)

$\Delta$  is a threshold voltage which can be adjusted over the range of 0.0 to 75 mV by potentiometer R5. The other thresholds are set by resistive voltage dividers connected directly to the + 15 volt rail so they will track variations and noise on the dc supplies.

- The second step in the out-of-band decision is carried out in programmed array logic (PAL) device U7. This device combines the eight comparator out-puts in a logical sum-of-products operation to determine if the received signal is out-of-band.
- The resulting signal is clocked to the FRU converter output by the STROBE input. The PAL decides a received signal is in-band if one (or both) of the sideband video signals is greater than 250 mV, and at least one of the following two conditions is satisfied: one sideband video exceeds the other by at least "A", or one sideband video is greater than 300 mV, and the other is between 250 mV and 150 mV.
- The PAL forms intermediate logic results which are fed back to the comparators to add hysteresis, thus avoiding comparator toggling due to noise or signals of marginal quality.

1-13. DETAILED OPERATION - Continued



FRU CONVERTER (A1A1) BLOCK DIAGRAM

**1-13. DETAILED OPERATION - Continued**

m. Quad Phase Detector (A1A12, A1A13) Refer to the quad phase detector (A1A12, A1 A13) block diagram and the frequency/phase measurement circuits block diagram. The quad phase detector detects phase differences between in-phase channel inputs and quadrature channel inputs, generating analog voltage outputs. The quad phase detector module contains two dual phase detector subassemblies. The I and Q outputs from the phase detectors are changing voltages that are proportional to input phase differences.

(1) Inputs.

- IF IN (I)
- IF IN (Q)
- IF IN (REF)

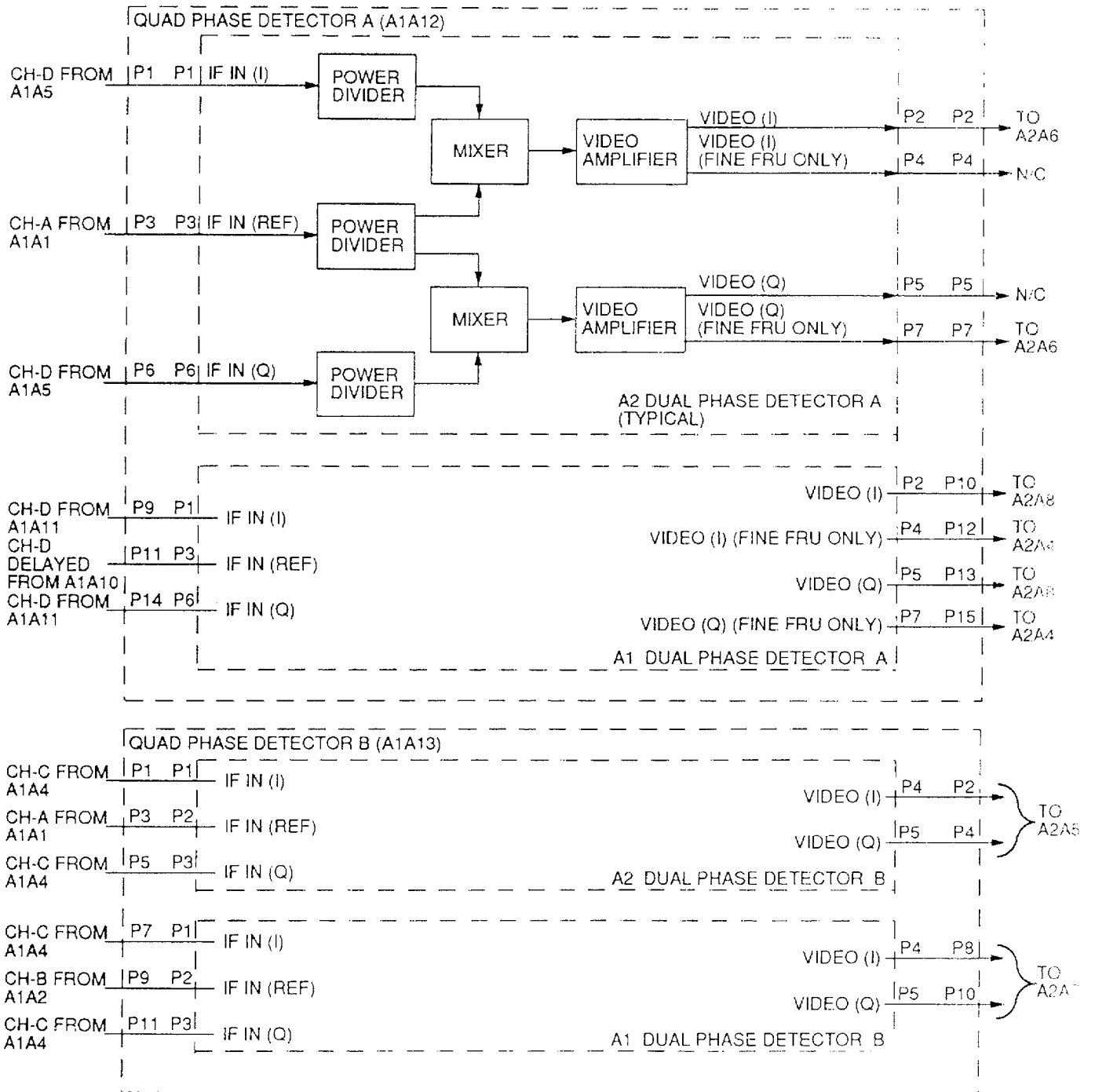
(2) Outputs.

- VIDEO (I)
- VIDEO (Q)
- VIDEO (I) (Fine FRU only)
- VIDEO (Q) (Fine FRU only)

(3) Signal Processing.

- The quad phase detector uses two types of dual phase detectors to measure the phase differences between signals on particular pairs of df channels and to perform the 150MHz fine FRU function. The output of each phase detector in A1A13 is fed to the input of a sample-and-hold circuit, then passed to the AQL IU to be digitized and further processed. Four outputs from AI A1I 2 are sent to sample-and-hold circuits and two are sent to phase reversal detector A2A4 for use in the signal logic and I/O circuits.
- The two types of dual phase detectors are virtually identical. The principal difference is that the A version adds a second, passively isolated output signal port. a Two dual phase detector A assemblies comprise quad phase detector A. One of these dual phase detectors compares the phase of df channel D to channel A, while the other performs the fine FRU function by comparing a df channel D signal to a time delayed version of itself. The additional output signal from this detector is used by the phase reversal detector to identify phase—coded signals.
- Quad phase detector B includes two dual phase detector B assemblies. These two dual phase detectors compare the phase of df channel C to channel B, and df channel C to channel A.
- A reference if. signal is applied to a power divider whose output is applied equally to the two double-balanced mixers. To maintain signal phasing, the I and Q inputs are passed through power dividers identical to the divider used for the reference signal, although only one output of each is used. The I channel signal and the reference are compared in one double-balanced mixer while the other processes the Q channel.

1-13. DETAILED OPERATION - Continued



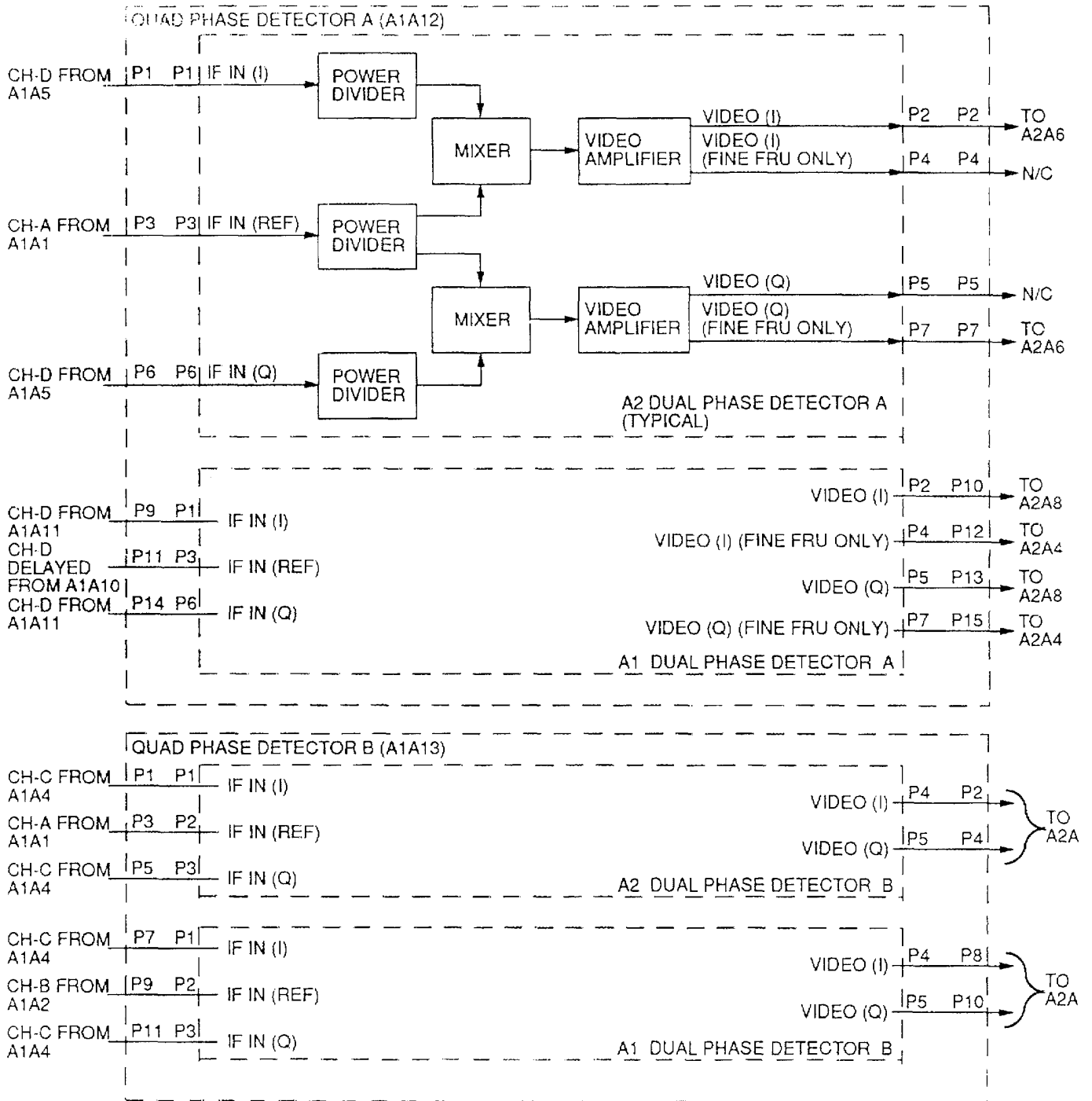
QUAD PHASE DETECTOR (A1A12, A1A13) BLOCK DIAGRAM

**1-13. DETAILED OPERATION** - Continued

- Each mixer output feeds a differential video amplifier stage with a voltage gain of 4.2 (12.5 dB). The video amplifiers use monolithic transistor arrays in a discrete circuit design which minimizes imbalance effects and temperature drift.
- The video amplifier outputs VIDEO (I) and VIDEO (Q) are applied to the appropriate sample-and-hold modules. The type A dual phase detectors include a second output which is used by the phase reversal detector module.



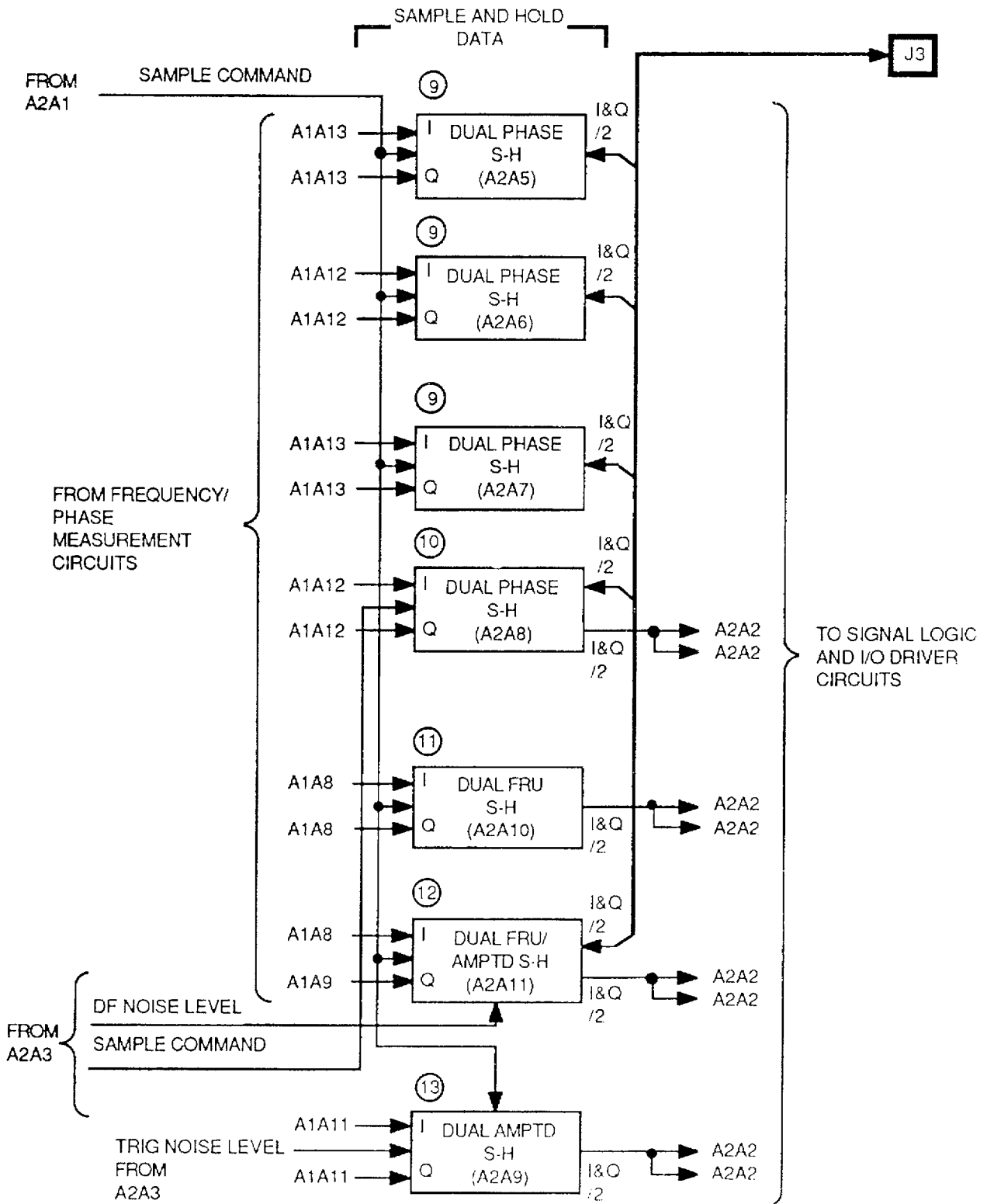
1-13. DETAILED OPERATION - Continued



QUAD PHASE DETECTOR (A1A12, A1A13) BLOCK DIAGRAM

**1-13. DETAILED OPERATION** - Continued

- n. Sample-and-Hold Data Circuits. Refer to the sample-and-hold data circuits block diagram.
- (9) **DUAL PHASE SAMPLE-AND-HOLD (A2A5, A2A6, A2A7)**. Receives sample command from interface (A2A1) assembly. Samples phase dependent voltage output from associated quad phase detector (A1A12 or A1A13) and holds for computer processing.
- (10) **DUAL PHASE SAMPLE-AND-HOLD (A2A8)**. Receives sample command from threshold/gate generator (A2A3). Samples phase dependent voltage output from quad phase detector (A1 A12) and holds for computer processing.
- (11) **DUAL FRU SAMPLE-AND-HOLD (A1A10)**. Receives sample command from interface (A2A1) assembly. Samples frequency dependent output of coarse FRU (A1A8) 120 MHz and 180 MHz detectors, and holds for computer processing..
- (12) **DUAL FRU/AMPLITUDE SAMPLE-AND-HOLD A2A11)**. Consists of two subassemblies. One subassembly input is amplitude dependent CH D from 150 MHz limiter log (A1A9). Other subassembly input is frequency-dependent, 150 MHz detector output from the coarse FRU (A1A8). Each responds to sample commands from threshold/gate generator (A2A3) through the interface assembly (A2A1).
- (13) **DUAL AMPLITUDE SAMPLE-AND-HOLD (A2A9)**. Samples amplitude dependent voltage output of 180 MHz if. (USB) (A1A6) and 120 MHz if. (LSB) (A1A7), and holds for computer processing.



SAMPLE-AND-HOLD DATA CIRCUITS BLOCK DIAGRAM

## 1-13. DETAILED OPERATION - Continued

O. Dual Phase Sample-and Hold (A2A5, A2A6, A2A7, A2A8). Refer to the dual phase sample-and-hold (A2A5, A2A6, A2A7, A2A8) block diagram and the sample-and-hold data circuits block diagram. The dual phase sample-and-hold circuit cards (A2A5-A2A7) receive sample commands from the interface (A2A1) assembly. The A2A8 circuit card receives sample commands from the threshold/gate generator (A2A3). In addition, the dual phase sample-and-hold circuit cards sample phase dependent voltage out-puts from quad phase detectors A1A12 and A1A13 and holds them for computer processing.

(1) Inputs.

- FRU VIDEO IN
- SAMPLE-AND-HOLD

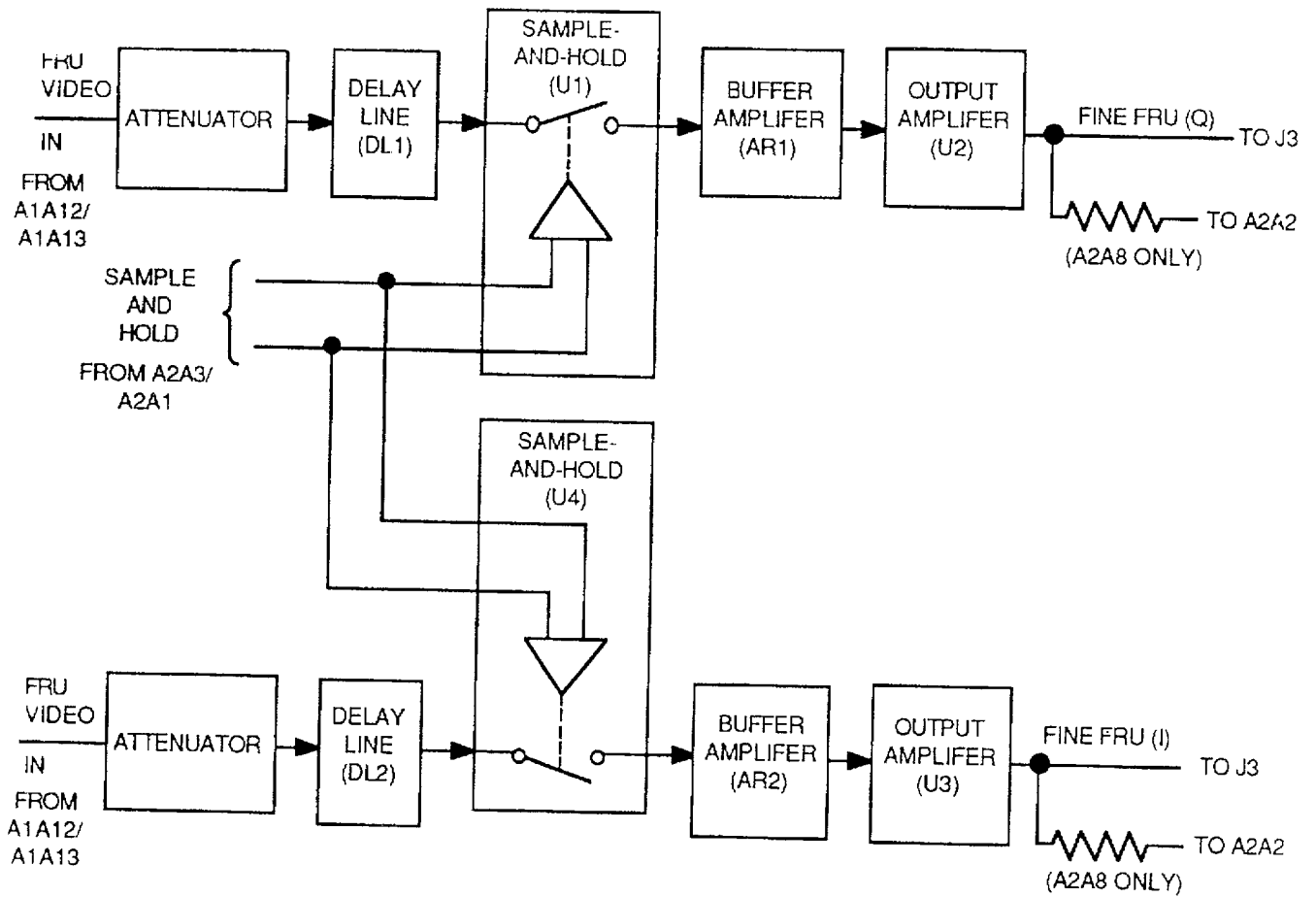
(2) Outputs.

- FINE FRU

(3) Signal Processing.

- The primary element of the sample-and-hold circuit is a high-speed hybrid integrated circuit sampling module, U1 or U4. The signal is applied to the sampling module after passing through a resistive attenuator and a tapped linear delay line (DL1 or DL2). The delay line tap is selected to assure coincidence of the sampling command pulse with its related signal. The attenuator provides impedance matching.
- The sampling command pulse originates in the threshold detector and gate generator (A2A3) and is applied to the dual sample-and-hold assembly. The sampling command pulse is applied directly to A2A8 and to A2A5 -A2A7 through interface assembly (A2A1). Both circuits in the dual sample-and-hold sample simultaneously.
- An integrated circuit buffer amplifier, AR1 or AR2, provides the voltage sample to the output amplifier without significantly discharging the "hold" capacitor (internal to the sampling module) between samples.
- The output amplifiers use a fast integrated circuit op-amp with a discrete transistor emitter follower output stage.
- The output amplifiers have two outputs, one of which is direct (low impedance) and the other using a resistor to establish a 100 ohm characteristic source impedance. The direct output is applied to J3 which is the system connection to the interface unit (IU). The 100 ohm impedance output is used only by the A2A8 circuit card.

1-13. DETAILED OPERATION- Continued



DUAL PHASE SAMPLE-AND-HOLD (A2A5, A2A6, A2A7, A2A8) BLOCK DIAGRAM

**1-13. DETAILED OPERATION - Continued**

p. Dual FRU Sample-and-Hold (A2A10). Refer to the dual FRU sample-and-hold block diagram and the sample-and-hold data circuits block diagram. The dual FRU sample-and-hold circuit card samples the frequency dependent outputs of the coarse FRU (A1A8) 120 MHz and 180 MHz detectors, and holds them for computer processing.

(1) Inputs.

- LSB FRU VIDEO IN
- USB FRU VIDEO IN
- SAMPLE AND HOLD

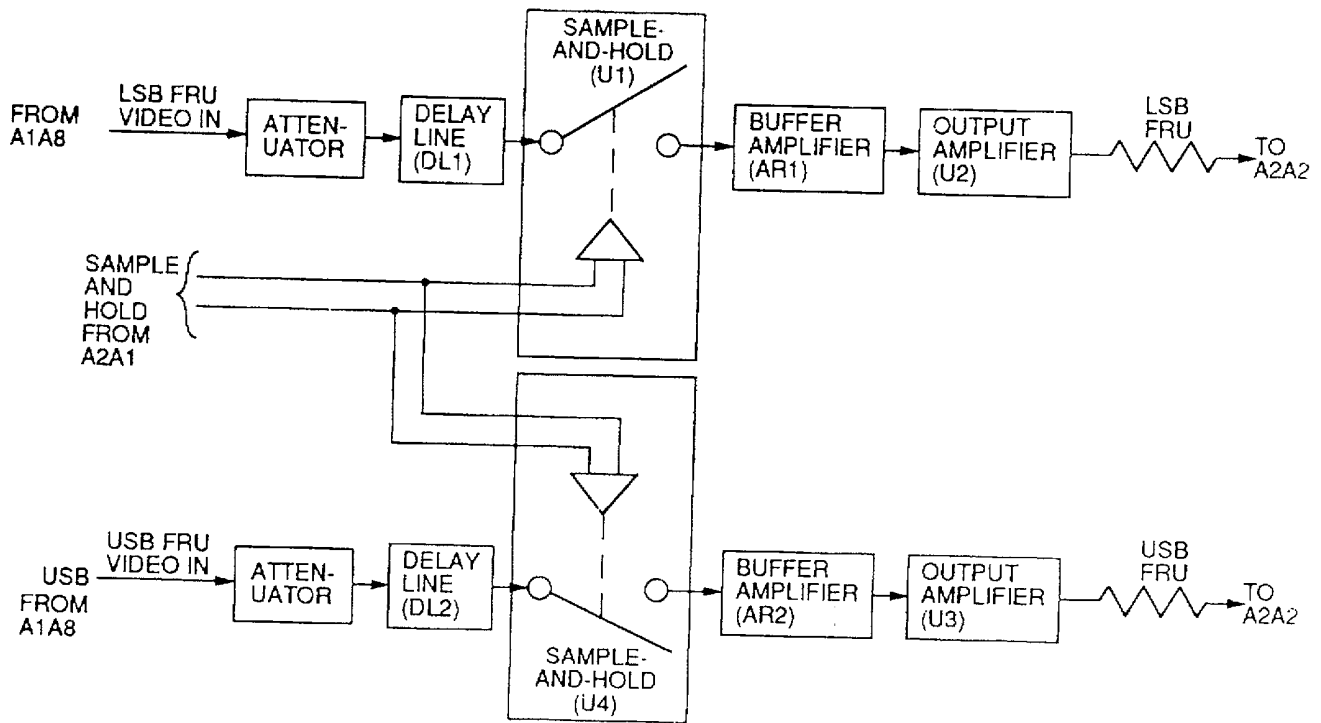
(2) Outputs.

- LSB FRU
- USB FRU

(3) Signal Processing.

- The primary element of the sample-and-hold circuit is a high-speed hybrid integrated circuit sampling module, U1 or U4. The signal is applied to the sampling module after passing through a resistive attenuator and a tapped linear delay line (DL1 or DL2). The delay line tap is selected to assure coincidence of the sampling command pulse with its related signal. The attenuator provides impedance matching.
- The sampling command pulse originates in the threshold detector and gate generator (A2A3) and is applied to the dual sample-and-hold assembly via the interface assembly (A2A1). Both circuits in the dual sample-and-hold sample simultaneously.
- An integrated circuit buffer amplifier, AR1 or AR2, provides the voltage sample to the output amplifier without significantly discharging the "hold" capacitor (internal to the sampling module) between samples.
- The output amplifiers use a fast integrated circuit op-amp with a discrete transistor emitter follower output stage.
- The amplifier outputs use resistors to establish a 100 ohm characteristic source impedance. Signal outputs of A2A10 are applied to the confirm logic circuit (A2A2).

1-13. DETAILED OPERATION - Continued



DUAL FRU SAMPLE-AND-HOLD (A2A10) BLOCK DIAGRAM

**1-13. DETAILED OPERATION - Continued**

g. Dual FRU/Amplitude Sample-and--Hold (A2A11) Refer to the dual FRU/amplitude sample-and-hold (A2A11) block diagram and the sample-and-hold data circuits block diagram. The dual FRU/amplitude sample-and-hold circuit card consists of two subassemblies. The input to one subassembly is amplitude dependent CH D from 150 MHz limiter/log (A1A9). The input to the second subassembly is frequency dependent. 150 MHz detector output from coarse FRU (A1A8). Each responds to sample commands from threshold/gate generator (A2A3) through interface logic (A2A1).

(1) Inputs.

- FRU VIDEO IN
- LOG VIDEO IN
- SAMPLE/HOLD
- DF NOISE LEVEL

(2) Outputs.

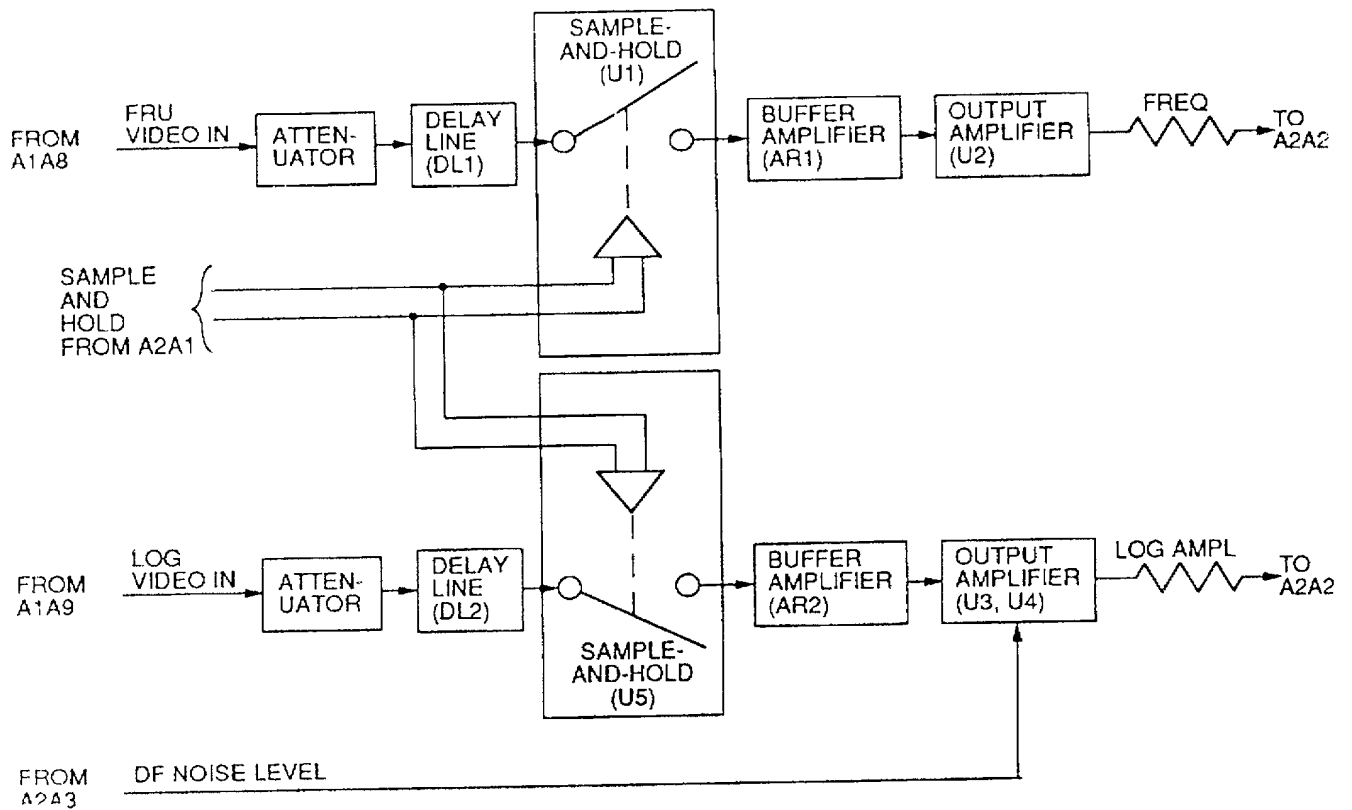
- FREQ
- LOG AMPL

(3) Signal Processing.

- The primary element of the sample-and-hold circuit is a high-speed hybrid integrated circuit sampling module, U1 or U5. The signal is applied to the sampling module after passing through a resistive attenuator and a tapped linear delay line (DL1 or DL2). The delay line tap is selected to assure coincidence of the sampling command pulse with its related signal. The attenuator provides level coordination and, where necessary, impedance matching between the 50 ohm characteristic of the delay lines and 92 ohm video amplifier outputs.
- The sampling command pulse originates in the threshold detector and gate generator and is applied to the dual sample-and-hold assembly via the threshold (A2A1). Both circuits in the dual sample-and-hold sample simultaneously.
- Integrated circuit buffer amplifier, AR1 or AR2, provides the voltage sample to the output amplifier without significantly discharging the "hold" capacitor (internal to the sampling module) between samples.
- The noise level input is from the threshold detector and gate generator (A2A3) and is applied to the inverting input of the operational amplifier U4. Normally, this input tracks the strongest video input noise from the trigger channels (USB/LSB); however, during the first 100 microseconds of a received pulse, this input is held at a constant level. If the A2A3 card detects a CW signal, this input is a fixed d.c. voltage.
- The output amplifiers use fast integrated circuit op-amps with discrete transistor emitter follower output stages. The log video stage uses an output amplifier with two op-amps, U3 and U4.
- The outputs of the amplifiers use resistors to establish a 100 ohm characteristic source impedance



1-13. DETAILED OPERATION - Continued I



DUAL FRU/AMPLITUDE SAMPLE-AND-HOLD (A2A11) BLOCK DIAGRAM

**1-13. DETAILED OPERATION-** Continued

r. Dual Amplitude Sample-and-Hold (A2A9). Refer to the dual amplitude sample-and-hold (A2A9) block diagram and the sample-and-hold data circuits block diagram.

(1) Inputs.

- USB LOG VIDEO
- LSB LOG VIDEO
- SAMPLE/HOLD
- TRIGGER NOISE LEVEL

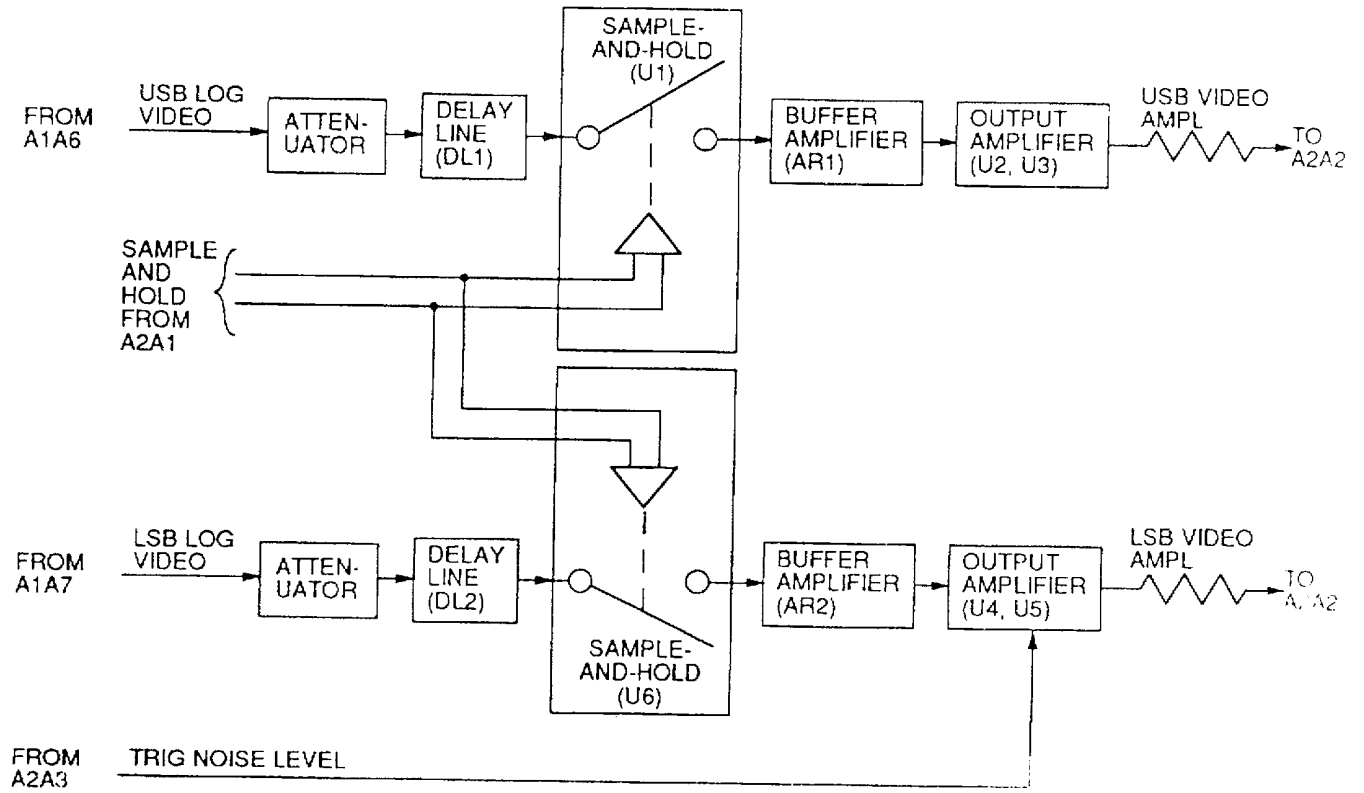
(2) Outputs.

- USB VIDEO AMPL
- LSB VIDEO AMPL

(3) Signal Processing.

- The primary element of the sample-and-hold circuit is a high-speed hybrid integrated circuit sampling module, U1 or U6. The signal is applied to the sampling modules after passing through a resistive attenuator and a tapped linear delay line (DL1 or DL2). The delay line tap is selected to assure coincidence of the sampling command pulse with its related signal. The attenuator provides level coordination and, where necessary, impedance matching between the 50 ohm characteristic of the delay lines and 93 ohm video amplifier outputs.
- The sampling command pulse originates in the threshold detector and gate generator and is applied to the dual sample-and-hold assembly. Both circuits in the dual sample-and-hold sample simultaneously.
- An integrated circuit buffer amplifier, AR1 or AR 2, provides the voltage sample to the output amplifier without significantly discharging the "hold" capacitor (internal to the sampling module) between samples.
- The output amplifiers use fast integrated circuit op-amps with discrete transistor emitter follower output stages. The USB log video channel uses an output amplifier with two op-amps, U2 and U3. The LSB log video channel uses an output amplifier with two op-amps, U4 and U5.
- Trigger noise level from the threshold detector and gate generator (A2A3) is applied to the inverting input of operational amplifiers U2 and U5. The input is either a sampled/held video noise from the strongest trigger channel or a fixed d.c. voltage when a CW signal is being received.
- The outputs of the amplifiers use resistors to establish a 100 ohm characteristic source impedance.

1-13 DETAILED OPERATION - Continued

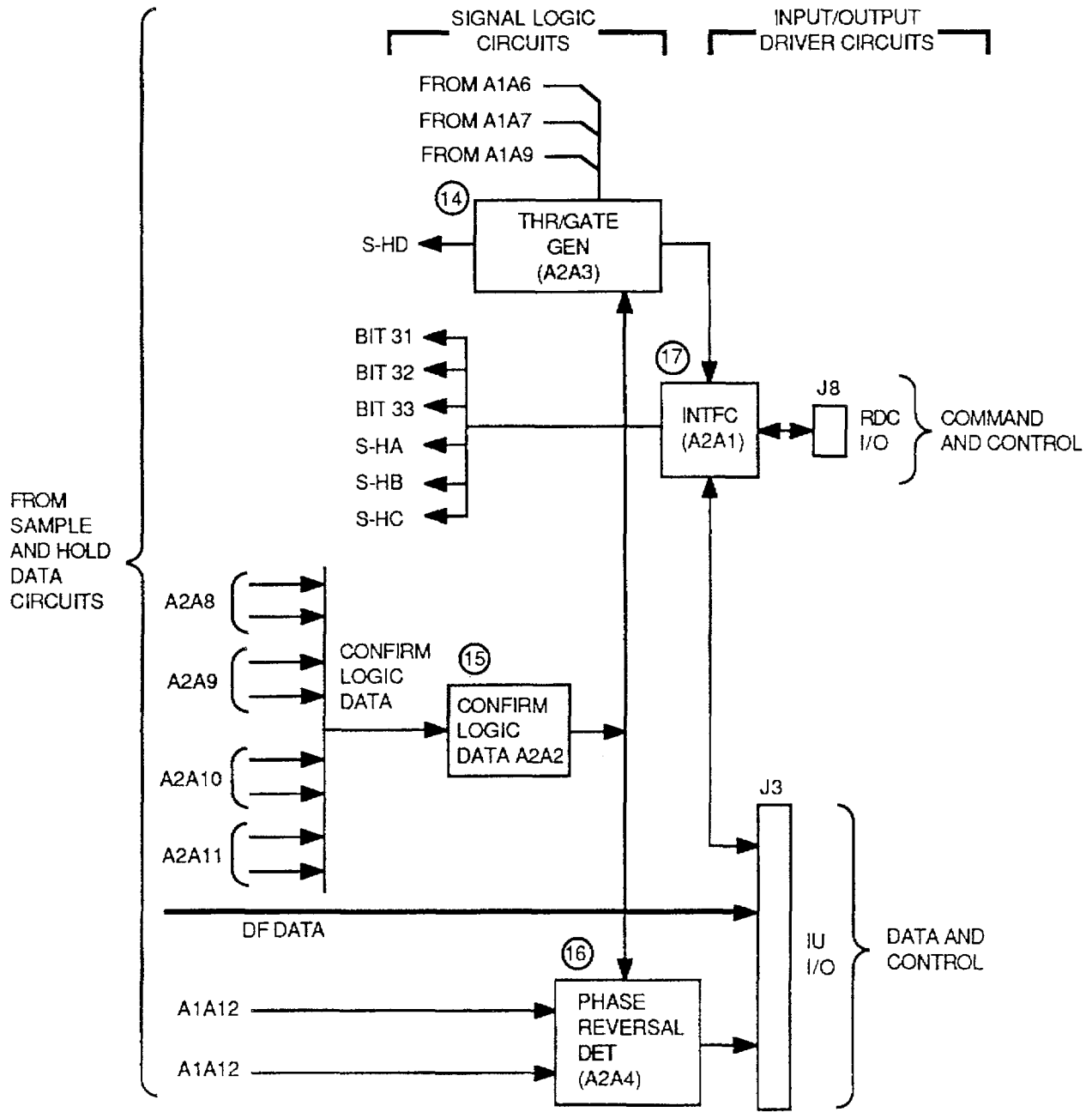


DUAL AMPLIFIER SAMPLE-AND-HOLD (A2A9) BLOCK DIAGRAM

**1-13. DETAILED OPERATION - Continued**

- s. Signal Logic and Input/Output Circuits Refer to the signal logic and input/output circuits block diagram.
- (14) **THRESHOLD/GATE GENERATOR (A2A3)**. Generates sample-and-hold commands and pulse width gate from either 180 MHz if (USB) (A1A6) or 120 MHz if. (LSB) (A1A7) log outputs. Sets receiver processing threshold.
- (15) **CONFIRM LOGIC (A2A2)**. Detects undesirable, spurious signals Outputs either a PW RESET signal which indicates a substandard signal, or a START TRIG which indicates signal quality is acceptable Frequency, pulse width, and amplitude are checked.
- (16) **PHASE REVERSAL DET (A2A4)**. Receives I and Q inputs from quad phase det A (A1A12), and outputs new pulse each time frequency change causes phase rollover.
- (17) **CINTERFACE (A2A1) ASSEMBLY**. Permits IFP to communicate with IU and RDC. Use for digital control signals only.

1-13. DETAILED OPERATION -Continued



SIGNAL LOGIC AND INPUT/OUTPUT CIRCUITS BLOCK DIAGRAM

**1-13. DETAILED OPERATION - Continued**

t. Threshold Detector and Gate Generator (A2A3). Refer to the threshold detector and gate generator (A2A3) block diagram and the signal logic and input/output circuits block diagram. The threshold detector and gate generator assembly monitors the detected trigger channel amplitude (video) to determine when a pulse is received and the width of the received pulses. It also provides trigger signals to sample-and-hold circuits in the lfp, activates a CW flag signal if a received signal is not pulsed and provides analog samples of detected receiver noise to the AQL digital processor. In addition, the threshold detector and gate generator produces a sample-and-hold command and a PWG from either 180 MHz if. (USB) (A1A6) or 120 MHz if. (LSB) (A1 A7) log output, and sets the receiver processing threshold.

**NOTE**

A dollar sign (\$) placed after a signal name indicates a logic low level or a negative sense emitter coupled logic (ECL) line. An asterisk (\*) placed after a signal name indicates a positive sense ECL line.

(1) Inputs.

- BW CMD
- EXTTHRESHOLD
- FRU ./TRIGGER
- LSB LOG VIDEO
- RCVR RST./
- USB LOG VIDEO

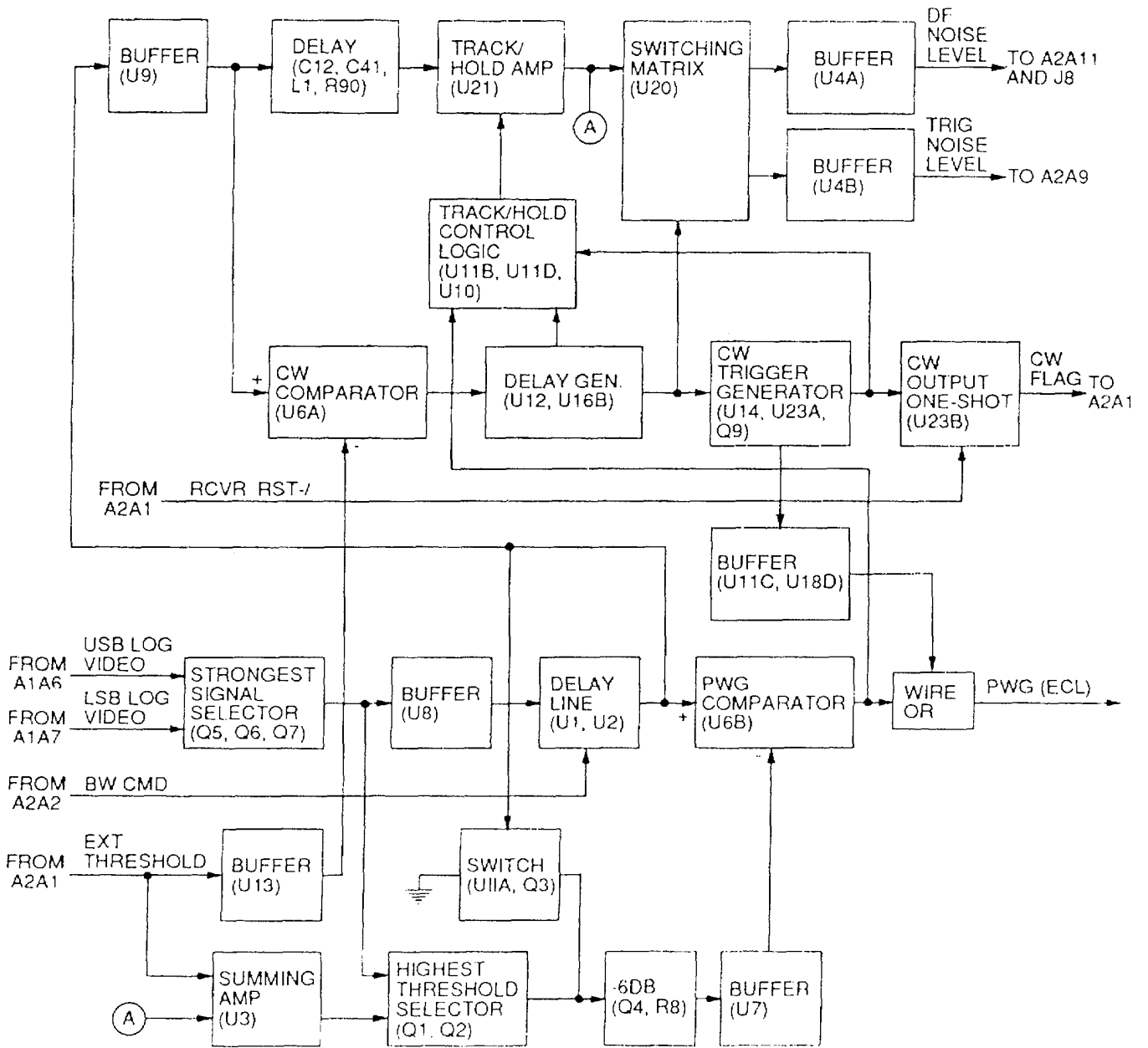
(2) Outputs.

- PWG (ECL)
- CW FLAG
- DF NOISE LEVEL
- FRU T/H \$
- FRU T/H \*
- PWG \$
- PWG \*
- T/H \$
- T/H \*
- TRIG NOISE LEVEL

(3) Signal Processing.

- Refer to the threshold detector and gate generator (A2A3) block diagram (part 1). The strongest signal is selected by the strongest signal selector circuitry comprised of Q5, A6, and O7. The output of this circuitry is buffered by emitter follower Q5 and buffer amplifier U8, whose output is applied to the input of delay line U2. U1, an analog switch circuit controlled by the Bw CMD input, selects either 30 nsec of delay (wide detection bandwidth) or the full 150nsec (narrow bandwidth). This delay is necessary to allow for system synchronization and settling of the filters in the threshold voltage circuits.
- The delayed signal is applied to PWG comparator U6B and unity gain buffer U9. The output of U9 is applied to the CW comparator U6A and, through a lowpass filter, to the track-and-hold circuit which supplies samples of noise or signal levels to the noise level outputs and the PWG threshold circuitry.

1-13. DETAILED OPERATION - Continued I



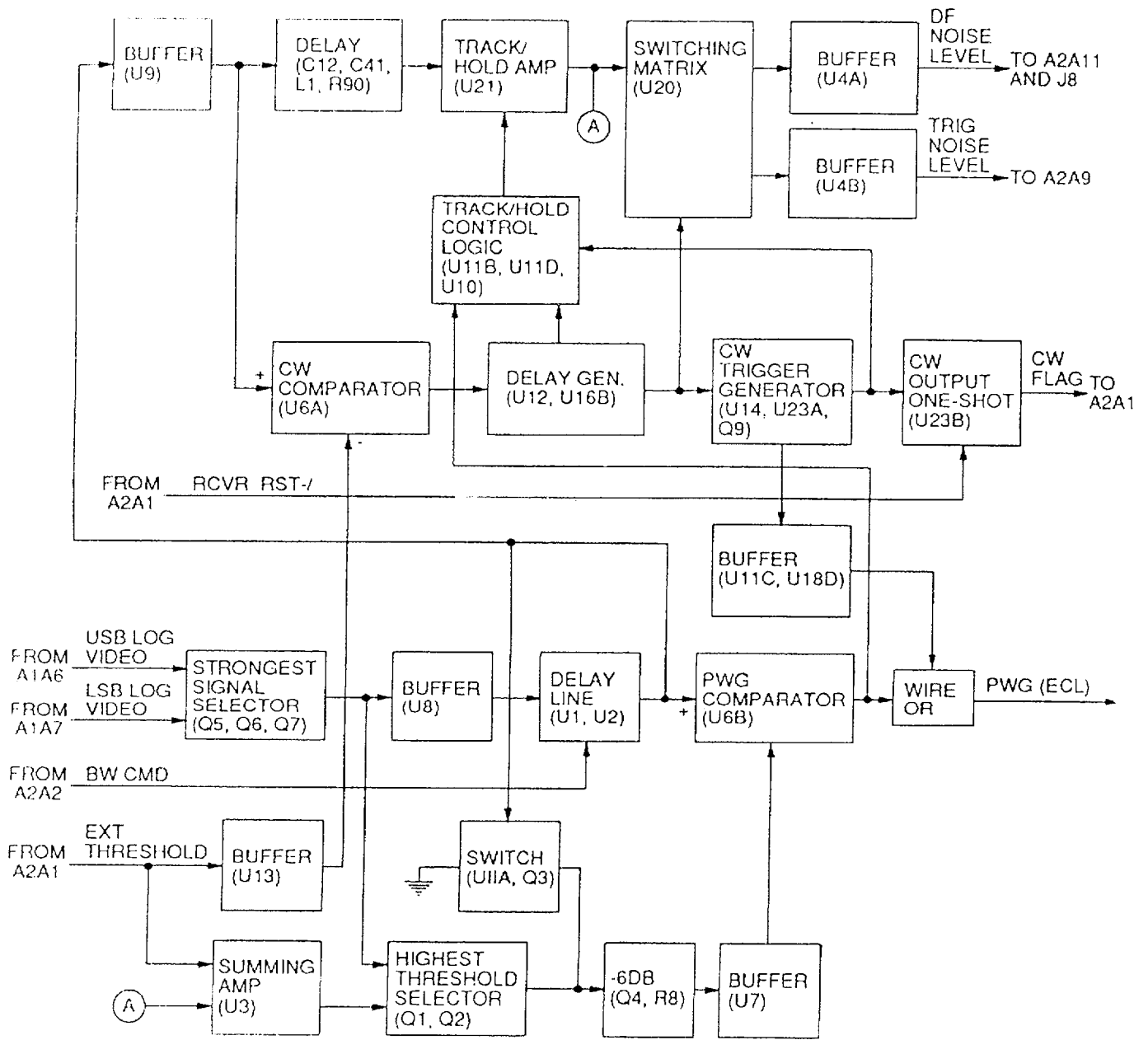
THRESHOLD DETECTOR AND GATE GENERATOR (A2A3) BLOCK DIAGRAM (PART 1)

## 1-13. DETAILED OPERATION - Continued

- The PWG (ECL) and CW signals interact to time the analog outputs at DF NOISE LEVEL through buffer U4A and TRIG NOISE LEVEL through buffer U4B. These two signals come from the same source' the trigger channel with the strongest signal. When the threshold detector and gate generator determines that a CW signal is being received, switching matrix U20 receives a control signal from the track/hold amp U21. The signal causes U20 to replace the noise level output voltages by fixed DC voltages.
- Normally these outputs track the strongest video input noise from the trigger channels, with a scale factor of 0.34 times the input voltage. However, during the first 100 usec of a received pulse (until it has been classified as a CW signal) these outputs are held at the value which the video input noise had just before the PWG comparator detected a signal. The noise level outputs return to tracking receiver noise level after the received signal has passed. These switching actions are controlled by the track/hold control logic circuitry comprised of U11B, U11D, and U10.
- The CW threshold is derived from the analog EXT THRESH input. U13, a dual op-amp, scales the input by a factor of 0.25 and adds a 0.0 to 2.5 volt offset.
- As with the CW comparator threshold, the PWG comparator threshold starts by scaling and offsetting EXT THRESH. A sample of the receive noise voltage is then added and the resultant is lowpass filtered to remove frequency components above approximately 725 kHz. This all occurs in U3.
- The receive noise voltage is derived from the same track-and-hold circuitry as the noise level output signals except that after 100 usec (a CW signal is being received), a sample of the signal voltage replaces the noise voltage. This causes the PWG comparator threshold to be greater than the received signal level, thus signals derived from PWG will be ended.
- After adding the noise (or signal) offset to the threshold voltage, the (modified) threshold voltage is compared to the signal level, and the greater value is selected to send to the PWG comparator threshold input. The highest threshold selector, comprised of Q1 and Q2, does this. This analog value is held until RCVR RST. /, acting through switch U11A, Q3, restores the PWG threshold to its (EXT THRESH) + (noise floor) 6 dB ) value. This is done to create different comparison thresholds for the rising and falling edges of received pulses.
- The next operation on the threshold voltage is adding another offset, calibrated to represent exactly 6.0 dB of received signal level. This is done by using U4 as a current source and subtracting the voltage that current induces in resistor R8 from the threshold voltage. U7, a unity gain buffer, prevents circuit loading from disturbing the accuracy of the PWG threshold voltage.
- Prior to receiving a pulse the PWG comparison threshold is set by EXT THRESH. the receiver noise floor, and the -6 dB factor. A pulse which exceeds the noise floor by whatever dB value is represented by (EXT THRESH -6 dB) will trigger PWG. It will also cause a change in the PWG comparison threshold to its own (signal level 6 dB). Thus, the falling edge of PWG will occur as the received pulse crosses its own 6 dB point. This facilitates the AQL system's requirement to measure pulse widths at their -6 dB points.



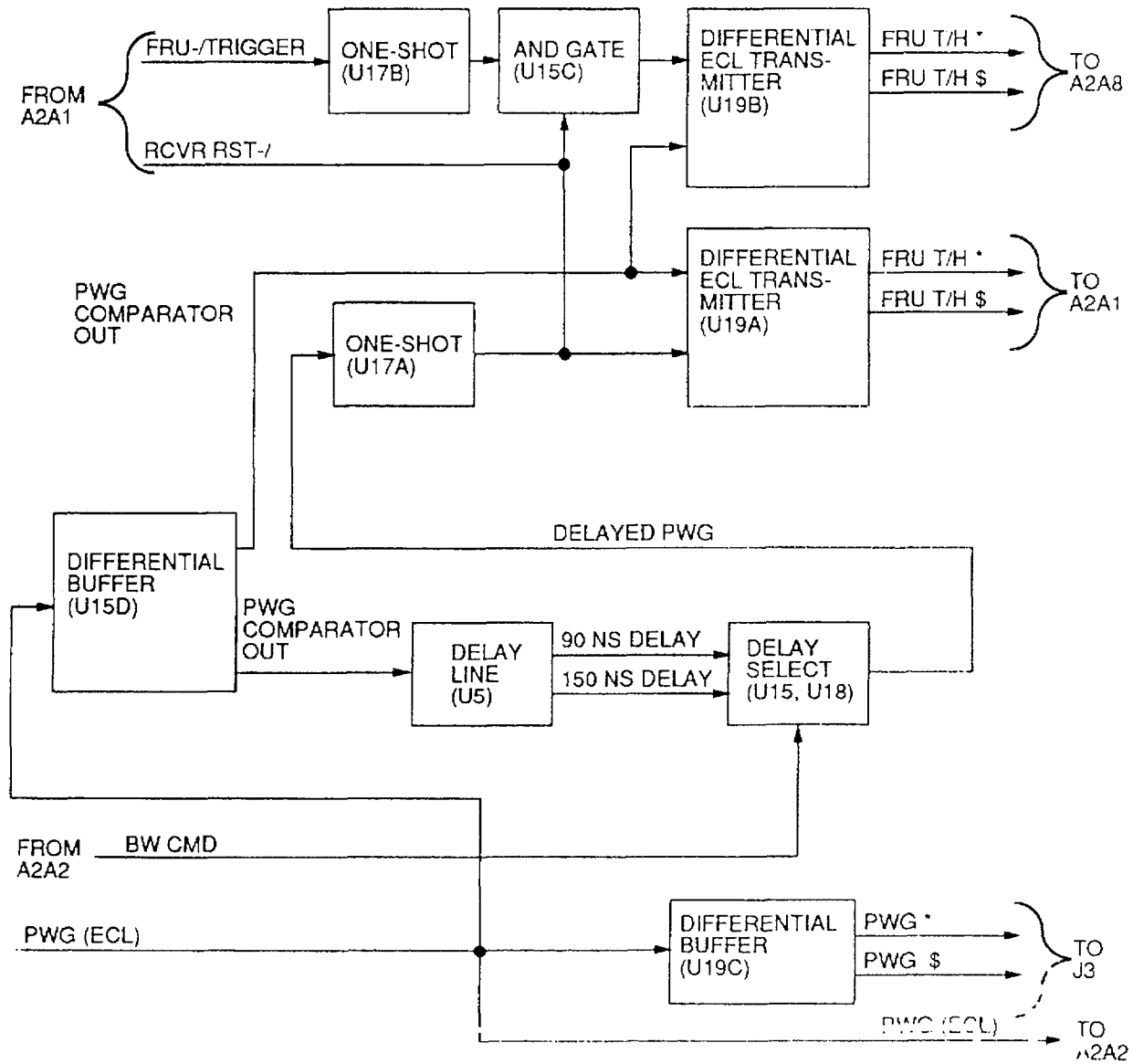
1-13. DETAILED OPERATION- Continued



THRESHOLD DETECTOR AND GATE GENERATOR (A2A3) BLOCK DIAGRAM (PART 1)

## 1-13 DETAILED OPERATION - Continued

- After the pulse passes, RCVR RST. / returns the PWG threshold to ((EXT THRESH) + (noise floor) 6 dB). If the pulse persists long enough to be characterized as CW, PWG (and derivative signals) are ended by raising the PWG comparison threshold above the received signal level. The threshold detector and gate generator can receive a pulse at the same time it is receiving a CW signal, provided the pulse level exceeds the CW level by an amount corresponding to EXT THRESH.
- While PWG and the sample-and-hold signals derived from it pertain to pulsed receive signals, a different chain of analog and logic devices creates CW FLAG when the received signal is not pulsed.
- The process begins similarly to the PWG signal with a fast ECL comparator, U6A. The comparator "-" input receives the (analog) CW threshold voltage while the "+" input gets video from the detected receive signal. The comparator output is buffered and converted to TTL format by delay generator U12, U16B.
- To this point, all received signals whether pulsed or not are processed in the same manner. The output of U16B in the delay generator starts an analog timing circuit in comparator U12. A pulse shorter than 100 usec (representing a non-CW signal) will prevent any output from the delay generator circuitry. Once the delay generator determines a CW signal has been received, there are four additional timing operations before CW FLAG is actually generated.
- The indication of a CW signal at the delay generator output initiates operation of the CW trigger generator comprised of U14, U23A, and O3. This circuitry sets the repeat times of CW FLAG, produced by U23B, determining its duty cycle. The CW FLAG output pulse width is 100 usec but the pulse may be cut short by RCVR RST. /. Also, CW FLAG occurs every 1500 usec after CW is first identified, and every 1000 usec after that.
- In addition to triggering CW FLAG, the CW trigger generator impresses a 450 nsec wide pulse on the PWG (ECL) line through buffer U11C, U18D, wired-OR with the PWG comparator output. This will hold the PWG comparator output line high. The operation of the dynamic threshold for PWG (ECL) will terminate PWG (ECL) on a long pulse before the pulse has actually ended.
- PWG comparator U6B "+" input receives trigger channel log video and the "-" input receives the dynamic threshold signal. The comparator output goes high whenever the trigger channel signal level exceeds the threshold, unless the threshold detector and gate generator detects a CW signal, in which case buffer U11C, U18D, wire-OR with the PWG comparator output, also holds the comparator output line high.
- Refer to the threshold detector and gate generator (A2A3) block diagram (part 2). The PWG comparator output is applied to U19C which buffers the PWG comparator output and converts it to differential ECL form. known as PWG\* and PWG\$.
- The PWG comparator output is also buffered by U15D, whose output is a differential signal. The positive portion of the differential signal is applied to delay line U5, which has two selectable delays.

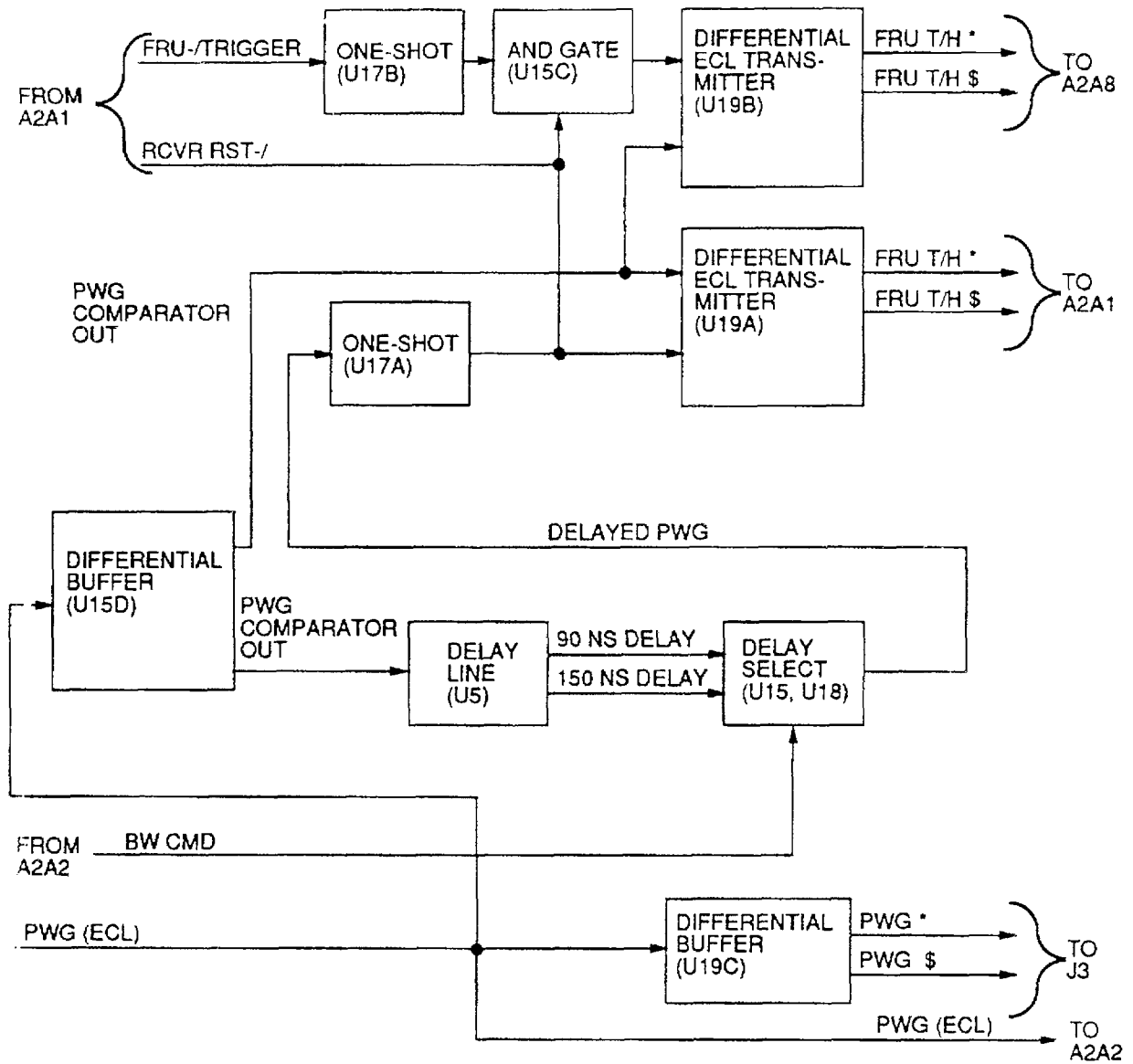


THRESHOLD DETECTOR AND GATE GENERATOR (A2A3) BLOCK DIAGRAM (PART 2)

**1-13. DETAILED OPERATION - Continued**

- The track/hold signals (T/H and FRU T/H) are created by passing the inverted PWG comparator outputs through ECL NOR gates used as transmission gates \* BW CMD is applied to delay select circuitry U15, U18 to select either the 90 nsec (wide detection bandwidth) or 150 nsec (narrow detection bandwidth) delay. The delayed PWG triggers one-shot U17A.
- The one-shot pulse would normally last for 425 usec except that RCVR RST ./ comes from the interface circuit card assembly (CCA) when PWG ends, or about 650 nsec after PWG starts, whichever is later. This unconditionally terminates the one-shot pulse The T/H transmission gate only passes the portion of the PWG pulse which occurs prior to the one-shot's being triggered (first 90 nsec of PWG during wideband operation or 150 nsec during narrowband).
- FRU T/H is similarly created, but allows for retriggering by FRU ./TRIGGER during a PWG Pulse. As with the initial triggering by PWG, FRU ./TRIGGER triggers one-shot U1 7B, whose output controls the passage of the PWG signal to the FRU T/H output. The initial pulse at FRU T/H will be 90 or 150 nsec wide (depending on selected detection bandwidth) while the retrigger pulse initiated by FRU ./TRIGGER starts at the leading edge of FRU ./TRIGGER and continues for the duration of PWG, or usec, whichever occurs first.

1-13. DETAILED OPERATION - Continued



THRESHOLD DETECTOR AND GATE GENERATOR (A2A3) BLOCK DIAGRAM (PART 2)

**1-13. DETAILED OPERATION - Continued**

u. Confirm Logic (A2A2). Refer to the confirm logic assembly (A2A2) block diagram and the signal logic and input/output circuits block diagram. The confirm logic assembly monitors frequency and amplitude parameters of received signals to verify that a received pulse has the characteristic of a valid signal. The confirm logic assembly indicates received signal validity through signals synchronized with PWG, and used by the IFP and other portions of the AQL system.

**(1) Inputs.**

- 150 MHZ FINE FRU (1)
- 150 MHZ FINE FRU (Q)
- BW CMD
- 150 MHZ COARSE FRU
- OUT-OF-BAND
- BIT 33
- BIT 3!
- PWG (ECL)
- DF LOG AMP
- USB FRU
- USB LOG AMP
- LSB FRU
- LSB LOG AMP

**(2) Outputs.**

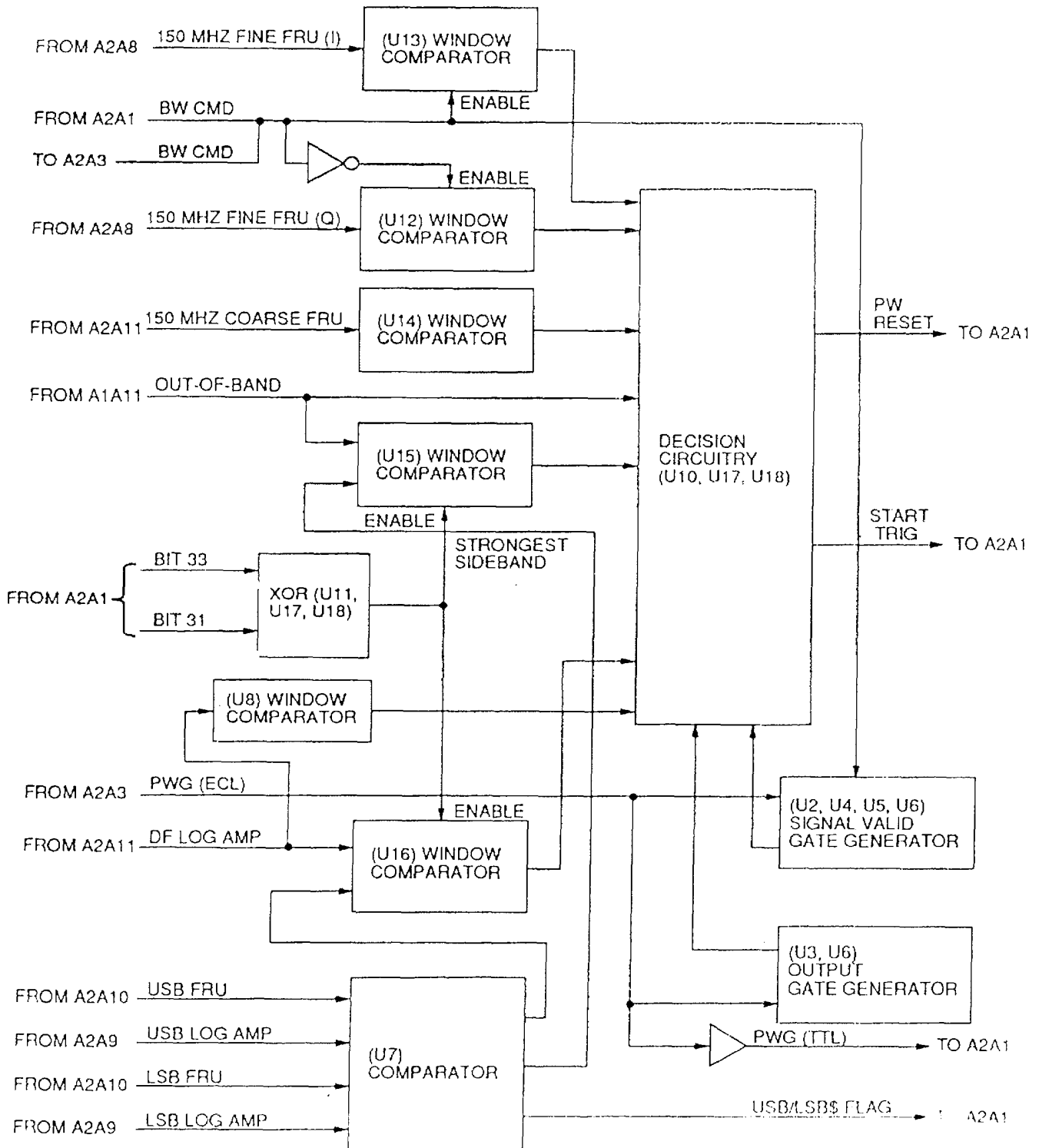
- PW RESET
- START TRIG
- PWG (TTL)
- USB?LSB \$ FLAG

**(3) Signal Processing.****NOTE**

A dollar sign (\$) placed after a signal name indicates a logic low level or a negative sense ECL line. An asterisk (\*) placed after a signal name indicates a positive sense ECL line.

- When active, START TRIG and PW RESET are logical complements (inverse) of each other. They are active only from 400 to 600 nsec after a high appears on PWG (ECL). During this interval, a high on START TRIG indicates a valid received signal, while a high on PW RESET indicates an invalid pulse. Outside this active signal, while a high on PW RESET indicates an invalid pulse. Outside this active interval both signals are always low.
- The confirm logic assembly creates START TRIG and PW RESET by monitoring seven conditions, any one of which could indicate that the received pulse is invalid U10, U17, and U18 form a decision circuitry function with these seven logic signals plus two timing strobe pulses as input.

1-13. DETAILED OPERATION - Continued



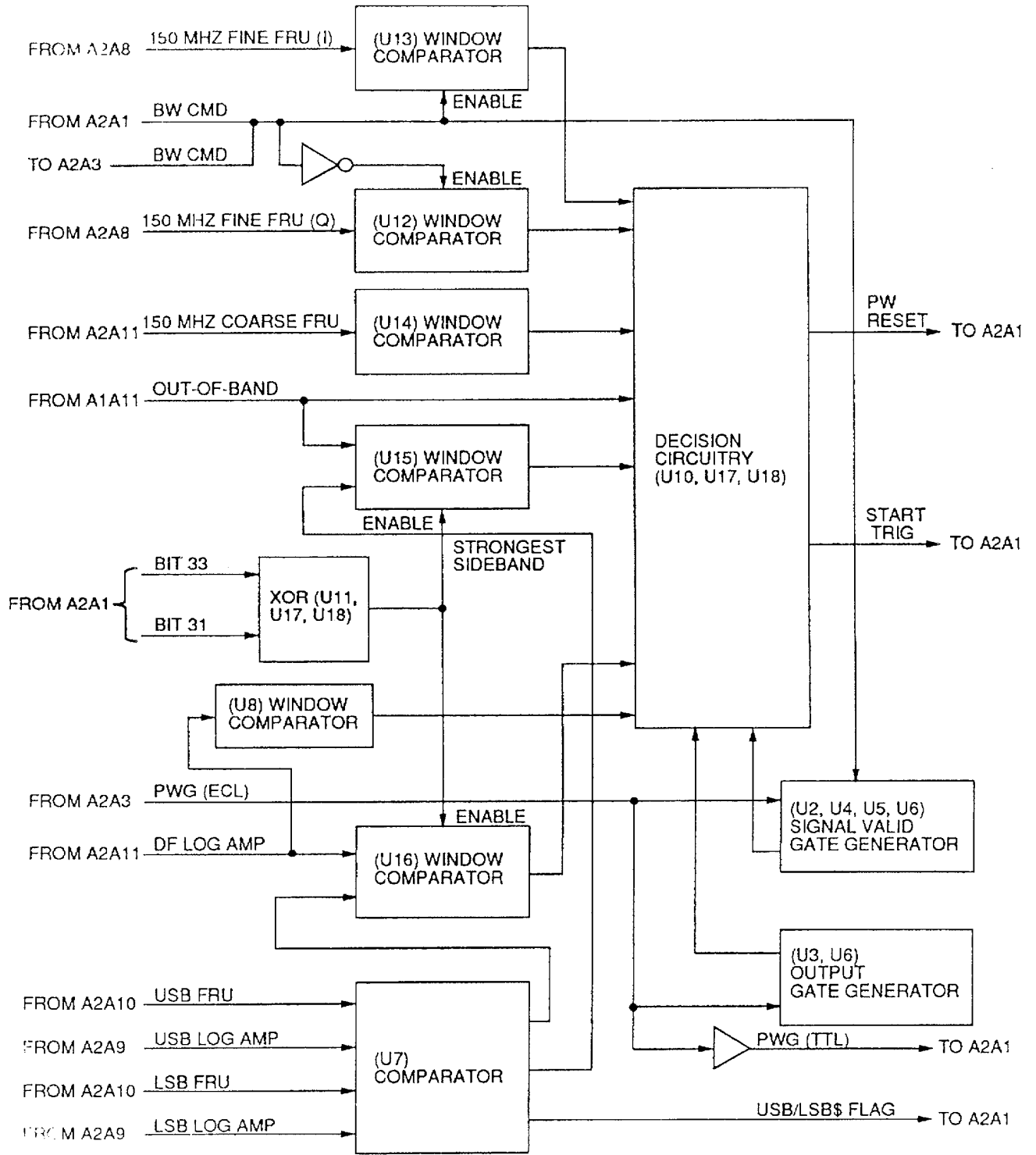
CONFIRM LOGIC ASSEMBLY (A2A2) BLOCK DIAGRAM1-71

**1-13. DETAILED OPERATION - Continued**

- One of the seven signals evaluated is the logic signal OUT-OF-BAND from the FRU converter assembly. OUT-OF-BAND is high when the measured frequency of a received signal is outside the passband of the frequency channel to which AQL is currently tuned.
- The remaining six signal-not-valid indications are generated by the confirm logic assembly using window comparators. The outputs of these window comparators are logic highs when their analog input is outside certain limits, for example, measured frequency being either above or below the range in which the AQL can accurately measure it.
- Window comparator U8 monitors DF LOG AMP (150 MHz) signal-to-noise (S/N) ratio as measured by the 150 MHz log amplitude signal. If this signal is greater than 2.63 volts (approximately 77 dB) or less than 0.125 volts (approximately 10 dB), PW RESET causes processing to be inhibited. Too strong a signal may lead to measurement errors from receiver overload conditions; too weak a signal cannot be accurately processed due to the accompanying noise.
- Window comparator U14 monitors received signal frequency as measured by the 150 MHz COARSE FRU. This signal must be greater than 2.09 volts (approximately 166 MHz) or less than 0.62 volts (approximately 134 MHz) to inhibit processing. Signals beyond these limits are outside the widest receiver passband.
- Window comparator U12 monitors received signal frequency as measured by the 150 MHz FINE FRU (Q) channel. This signal must be greater than 2.25 volts (greater than approximately 167 MHz or less than approximately 134 MHz) to inhibit processing. U12 is disabled, indicating a valid received signal, when the BW SELECT line is in the high (5 MHz) state.
- When BW SELECT is in the high (5 MHz) state, window comparator U13 is enabled and monitors 150 MHz FINE FRU (I). This signal must be greater than 1.85 volts (approximately 154 MHz) or less than 0.82 volts (approximately 146 MHz) to inhibit processing. Signals beyond these limits are outside the narrow receiver passband and cannot be accurately processed.
- The 150 MHz COARSE FRU signal from the strongest sideband is compared to 150 MHz COARSE FRU by window comparator U15. If the indicated frequencies are different by more than 12 MHz, the received signal is not valid. This test is disabled when either BIT 31 or BIT 33 (but not both) is high. This comparator is active, however, when no BIT signals are on or when both channels are excited by BIT signals.
- Window comparator U16 compares the log amplitude of the signal from the strongest sideband to the log amplitude of the 150 MHz signal (DF LOG AMP). If the indicated levels are more than 490 mV (about 13 dB) different, the received signal is not valid. This test is disabled under the same conditions as the previous test: either BIT 31 or BIT 33 (not both) is active. A signal received within the valid passband of the df channel will be no more than 13 dB down the response curve of one trigger channel or the other, so any greater difference in amplitudes indicates an invalid signal.



1-13 DETAILED OPERATION -Continued

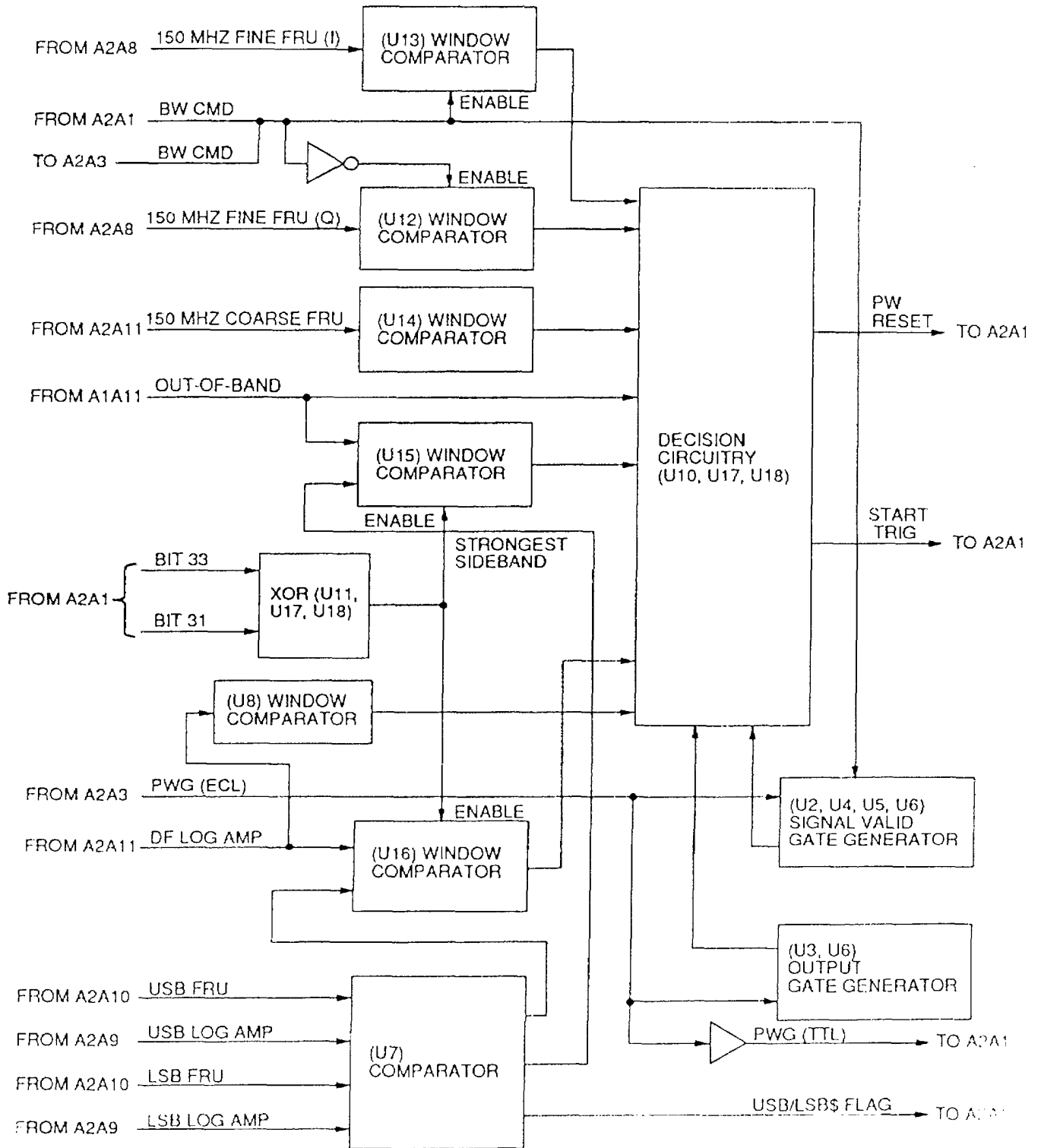


CONFIRM LOGIC ASSEMBLY (A2A2) BLOCK DIAGRAM

**1-13. DETAILED OPERATION - Continued**

- Comparator U7 determines which of the trigger channel signals (USB or LSB) is stronger by simply comparing their respective log amplitudes (USB LOG AMP and LSB LOG AMP). One output of the comparator is USB/LSB\$ FLAG. A high on that signal indicates the receiver was triggered by the USB trigger channel, a low indicates the receiver was triggered by the LSB channel. The other output of U7 operates switch U9, sending the amplitude or FRU signal of the triggering sideband to the appropriate window comparators for signal validation as described above.
- The confirm logic uses PWG to create two redundant timing signals which accomplish the same result: a signal-not-valid strobe and an output enabling pulse. The output enabling pulse is 200nsec wide and comes from the output gate generator. It is delayed for 400 nsec after PWG goes high to allow the analog signals being monitored to settle on their final values before received signal validity is determined.
- The signal valid strobe comes from the signal valid gate generator. Since it is a negative-going pulse, it guarantees that the output of the decision circuitry is held in a high (signal not valid) state except during the pulse interval. This strobe pulse is 700 nsec wide and begins 40 nsec after PWG goes high if the receiver is in its wideband mode, or 275 nsec after PWG in the narrowband mode. These delays permit the various analog signals being monitored to settle to their final values before received signal validity is determined.
- The confirm logic assembly also generates a copy of the PWG signal in TTL format, PWG (TTL).

1-13 DETAILED OPERATION -Continued



CONFIRM LOGIC ASSEMBLY (A2A2) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION- Continued

- v. Phase Reversal Detector (A2A4). Refer to the phase reversal detector (A2A4) block diagram and the signal logic and input/output circuits block diagram. The phase reversal detector is a specialized analog processing circuit used to identify received signals exhibiting rapid changes in received electrical phase or frequency. Rapid changes in signal frequency, as expressed by instantaneous levels of 150 MHz FINE FRU (I) and 150 MHz FINE FRU (Q), cause the phase reversal detector to send a pulse to the digital processing section of the AQL system. An instantaneous change in phase of a band-limited signal cannot be distinguished from a sudden, short jump to another frequency followed by a return to the original frequency. The 150 MHz fine FRU detects the instantaneous frequency of received mission signals. The phase reversal detector looks for sudden changes in received signal frequency (phase) as shown by rapid changes in the 150 MHz FINE FRU (I) and (Q) output voltages. To avoid triggering by noise, the frequency rate-of-change must exceed approximately 35 MHz per microsecond and the rate of change must be sustained for at least 20 nsec.

(1) Inputs.

- 150 MHz FINE FRU (I)
- 150 MHz FINE FRU (Q)

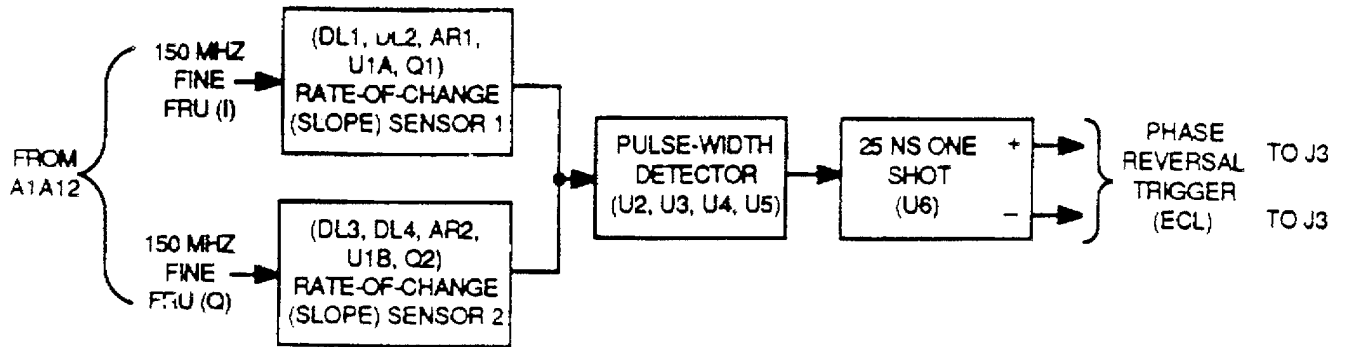
(2) Outputs.

- PHASE REVERSAL TRIGGER (ECL)

(3) Signal Processing.

- Two identical rate-of-change sensor circuits are used by the phase reversal detector, one for the FINE FRU (I) signal and one for the FINE FRU (Q) signal. These circuits sense the frequency rate of change and duration, and are each constructed from a delay line, a buffer amplifier, a calibrated voltage level shifter, and a comparator.
- The input from the fine FRU is applied to a rate-of-change (slope) sensor. The sensor output will go to a logic high when the input signal increases by more than the level shift (2.3 MHz) during the delay time (60 nsec). Both channels are monitored according to identical criteria and the results wired-OR together, so a rapid increase in frequency on either FRU channel will trigger the phase reversal detector.
- The next section is a pulse width detector which ensures that the detected frequency jump is sustained long enough to constitute a phase reversal and is not simply an indication of noise in the FRU circuitry. A special ECL module monitors the duration of pulses coming from the rate of change sensor, and passes those which persist for at least 25 nsec. The module does not respond to shorter pulse widths.
- The pulse coming out of the module must be delayed by 25 nsec while the module determines that the pulse is at least that long. Those which pass the pulse width discriminator trigger a 30 nsec one-shot. This one-shot in turn triggers a 25 nsec one-shot which generates the actual phase reversal output pulse, at approximately the time when the input signal frequency stops increasing at a high rate. The 30 nsec one-shot output also inhibits the operation of the pulse width detector, so the output phase reversal signal has at least a 25 nsec space between pulses.

1-13. DETAILED OPERATION - Continued



PHASE REVERSAL DETECTOR (A2A4) BLOCK DIAGRAM

**1-13. DETAILED OPERATION-** Continued

w. Interface Assembly (A2A1). Refer to the interface assembly (A2A1) block diagram and the signal logic and input/output circuits block diagram. The interface assembly buffers logic signals which enter or leave the IFP, converts the digital threshold data to analog form, and creates some timing and synchronization signals used by the IFP and other portions of the AQL system.

**NOTE**

A dollar sign (\$) placed after a signal name indicates a logic low level or a negative sense ECL line. An asterisk (\*) placed after a signal name indicates a positive sense ECL line.

(1) Inputs.

- T/H\*, T/H\$
- AO\* through A5\*
- \* AO\$ through A5\$
- BW CMD\*, BW CMD\$
- FRU RETRIG\*, FRU RETRIG\$
- BIT 31\*, BIT 32\*, BIT 33\*
- BIT 31\$, BIT 32\$, BIT 33\$
- PWG
- CW FLAG
- USB/LSB\$ FLAG
- START TRIG
- PW RST

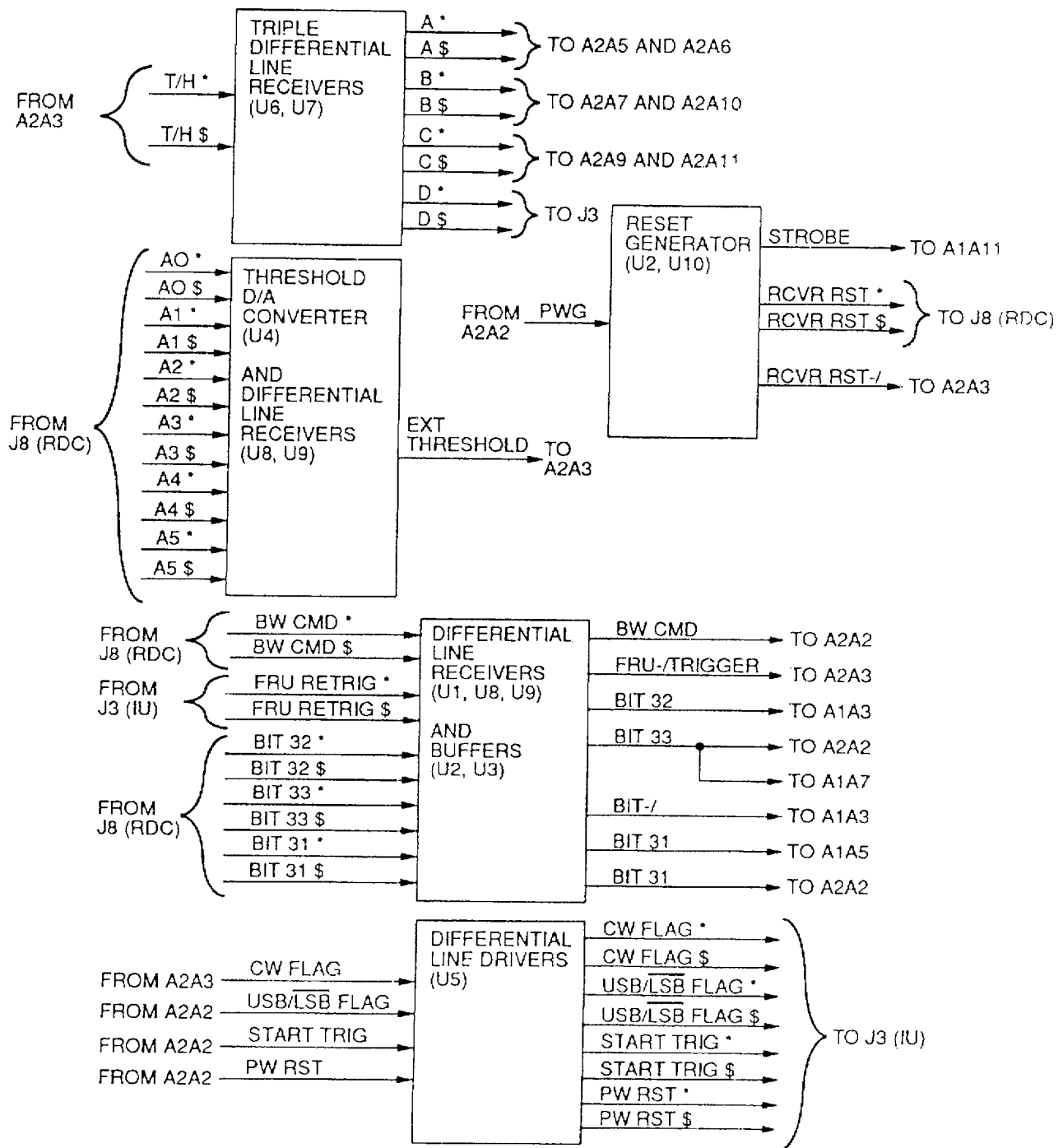
(2) Outputs.

- A\*, B\*, C\*, D\*
- A\$, B\$, C\$, D\$
- EXTTHRESHOLD
- BW CMD
- FRU ./TRIGGER
- BIT 31
- BIT32
- BIT33
- BIT ./
- STROBE
- RCVR RST \*, RCVR RST\$, RCVR RST.
- CW FLAG\*, CW FLAG\$
- USB/LSB\$ FLAG\*, USB/LSB\$ FLAG\$
- START TRIG\*, START TRIG\$
- PW RST\*, PW RST\$

(3) Signal Processing.

- Signals coming to the IFP from the RDC enter the interface assembly as differential signals. Differential line receivers (U1, U8, and U9) detect these signals and buffers (U2, U2) convert them to TTL format, and send them to various cards and modules in the IFP where they are used. These system-to-IFP signals include

1-13. DETAILED OPERATION - Continued



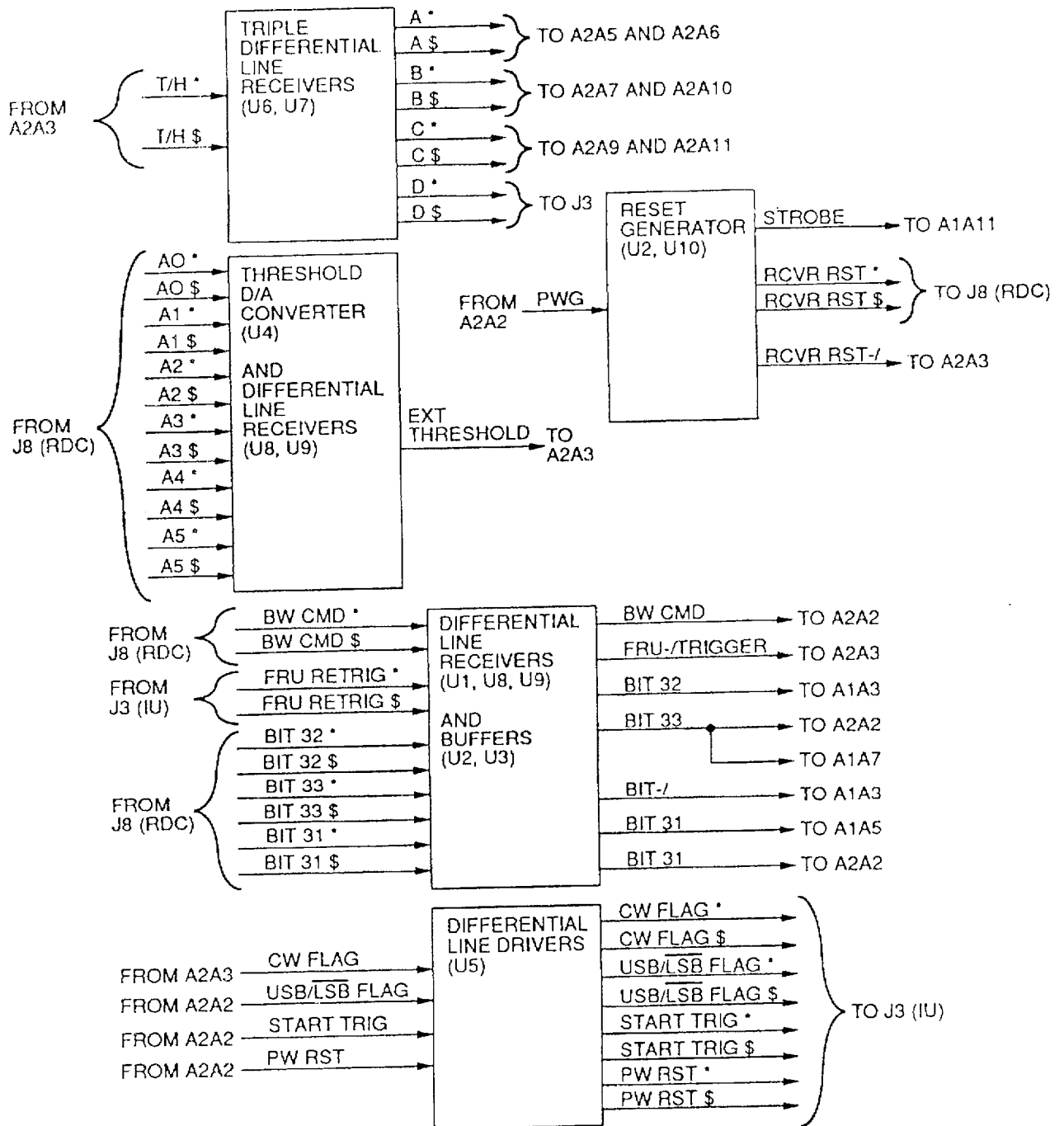
INTERFACE ASSEMBLY (A2A1) BLOCK DIAGRAM

## 1-13. DETAILED OPERATION - Continued

- The bandwidth selection command, BW CMD (logic low for wideband; logic high for narrowband).
- The FRU retrigger command, FRU RETRIG is received from the IU. The interface assembly inverts the sense of this signal and renames it FRU /TRIGGER. In this form a logic low initiates a new sample of the fine FRU frequency readout.
- BIT 31, the BIT command for the df channels. A logic high causes a BIT signal to be injected into the four df channels. This signal is split and further buffered to avoid excessive loading by the driven circuits within the IFP.
- BIT 33, the BIT command for the trigger channels. A logic high causes BIT signals to be injected into one of the trigger channels.
- BIT 32, the trigger channel BIT selection command. When BIT 33 is a logic high, a logic high on BIT 32 sends the BIT signal to the USB trigger channel while a logic low sends it to the LSB. Like BIT 31, this signal is split and further buffered to accommodate the loads it must drive.
- BIT ./ signal is low whenever any form of IFP BIT is requested. The BIT. / signal is used to enable the BIT signal oscillator.
- The processing signal threshold data, a six-bit digital word (A0 through A5) is converted to an analog voltage by the threshold digital-to-analog (D/A) converter and used in the threshold detector/gate generator.
- The interface assembly receives a differential ECL sample-and-hold signal (T/H) from the threshold detector/gate generator, splits it five ways and buffers each output. These signals operate the sample-and-hold amplifiers in the IFP, and one is SAMPLE CMD (D\*, D\$) sent to the RDC.
- Four TTL signals from the IFP are converted by the interface assembly to differential line signals for transmission to the IU. These signals are CW FLAG, USB/LSB FLAG, START TRIG and PW RST. CW FLAG is a logic high whenever the threshold detector/gate generator senses a CW signal. USB/LSB FLAG will be a logic high when the IFP has been triggered by a signal on the USB channel. START TRIG and PW RST are active only from 400 nsec to 600 nsec after PWG becomes a logic high. During this interval a logic high on START TRIG indicates a valid received signal, while a logic high on PW RST indicates an invalid pulse. Outside this active interval both signals are always logic lows.
- The interface assembly receives PWG, a TTL signal from the confirm logic and uses it to trigger a 650 nsec one-shot. The one-shot's output is OR'd with PWG in U2 to make STROBE, which is used by the FRU converter (A1A11). STROBE starts when PWG goes to a logic high, and remains high as long as PWG or 650 nsec, whichever is longer. Two signals are derived from the low-going edge of STROBE: RST is a 200 nsec wide, positive pulse which starts as STROBE ends. RST is sent to the RDC as RCVR RST\* and RCVR RST\$, a differential signal. RCVR RST./ is a negative-going TTL pulse with the same timing as RST, used by the threshold detector/gate generator and confirm logic assemblies.



1-13 DETAILED OPERATION - Continued



INTERFACE ASSEMBLY (A2A1) BLOCK DIAGRAM

CHAPTER 2

OPERATING INSTRUCTIONS

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Not Applicable.

**2-1/(2-2 BLANK)**

**CHAPTER 3**  
**OPERATOR MAINTENANCE**

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Not Applicable.

**CHAPTER 4**  
**ORGANIZATIONAL MAINTENANCE**

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Not Applicable.

## CHAPTER 5

## DIRECT SUPPORT MAINTENANCE

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**Section I. REPAIR PARTS, SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT**

**5-1. COMMON TOOLS AND EQUIPMENT**

For authorized common tools and equipment refer to the Modified Table of Organization and Equipment (MTOE) applicable to your unit.

**5-2. SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT**

Refer to Maintenance Allocation Chart (Appx B) and TM 11-5895-1284-23P

**5-3. REPAIR PARTS**

Repair parts are listed and illustrated in TM 11-5895-1284-23P.

**Section II. TROUBLESHOOTING**

**5-4. TEST EQUIPMENT REQUIRED**

- a Refer to paragraph(s) 5-1 and 5-2 and test setup diagram(s).
- b Locally fabricated jumper and cover (appx C).

**5-5. TEST CONNECTIONS**

- a On Electronic Systems Test Set (ESTS), set

<u>Switch</u>	<u>Set to</u>
IF FREQ MHZ	150.0
USB/LSB	LSB
SSB OFFSET	0
DVM SEL	VOLTS
AT1	30
AT2	0 or cf (para 5-6)
MOD/PW	CW
PW SET	full cw
TRIG SEL	ST TRIG/PW RST
EXT THRESH	OFF
EXT THRESH ADJ	full cw
SWEEP	OFF
BAND CMD	LB
BW CMD	30 MHz
BIT TEST	OFF
PHASE-DEG	0
PRF	10 KHz
DATA SELECT	B-CQ
POWER ON/OFF	ON

- b On VVM, set:

<u>Switch</u>	<u>Set to</u>
FREQ RANGE	100-200 MHz
AMPLITUDE	-30 dBm
METER OFFSET	0
PHASE RANGE	$\pm$ 6 Degrees

Connections made to test equipment are equivalent to 50-ohm terminations.

5-5. TEST CONNECTIONS - Continued

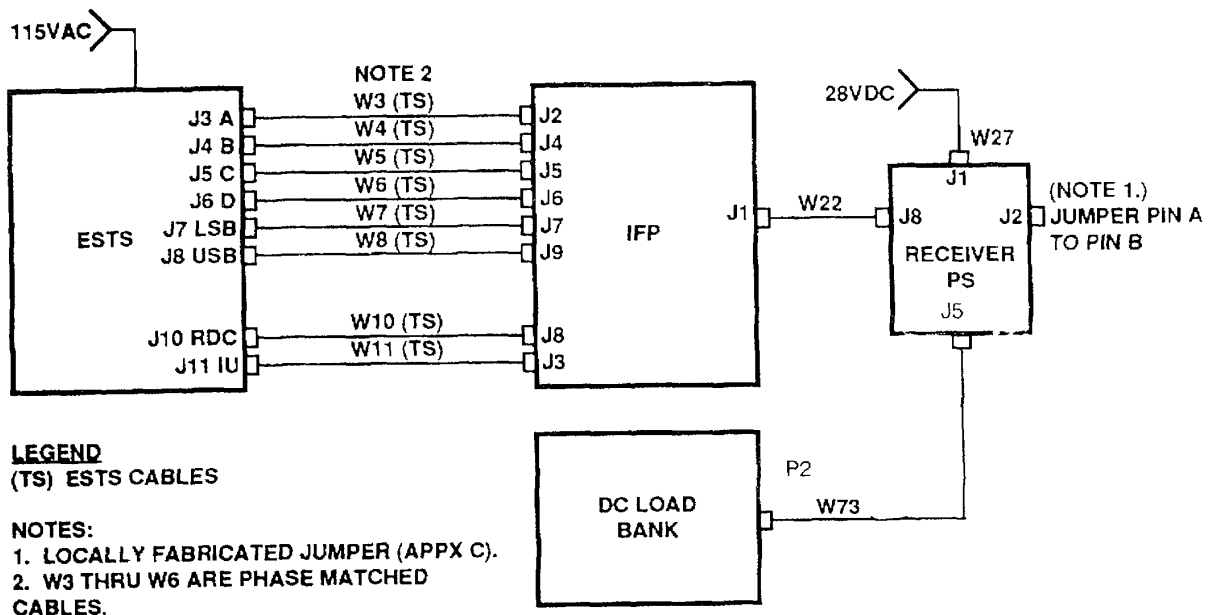


FIGURE 5-1. IFP INITIAL TEST SETUP

**NOTE**

IFP warm-up requirements are as follows:  
 Cover removed - 30 minutes  
 Alinement cover installed - 45 minutes

- c Connect test setup (fig. 5-1)
- d Turn on all test equipment. Set DC load bank to 0.2 + 0.1 amps.
- e Allow required warm-up time before proceeding
- f Calibrate test equipment (para 5-6).
- g Proceed to test procedure and fault isolation (para 5-7)



**5-6. TEST EQUIPMENT CALIBRATION**

**NOTE**

Test equipment calibration must be set and maintained throughout testing and troubleshooting.

Calibration factor (cf) obtained in this calibration procedure is used throughout testing and troubleshooting.

- a Apply power to vector voltmeter (VVM) and spectrum analyzer.
- b Disconnect W6 from IFP. Connect W6 to spectrum analyzer.
- c On ESTS, set:

<u>Switch</u>	<u>Set to</u>
AT2	0
AT1	30
IF FREQ MHz	150.0
MOD/PW	CW

- d Adjust ESTS AT2 for -30 +/- 0.5 dBm on spectrum analyzer.
- e Record AT2 dial setting for use as calibration factor (cf).

**NOTE**

More than one cf may be necessary. If spectrum analyzer readings are not within specifications, adjust AT2 to obtain specifications and note new cf and AT1 setting. Use appropriate cf for each AT1 setting throughout procedures.

- f Step through ESTS AT1 settings with ESTS AT2 set at the cf. Verify spectrum analyzer readings as follows:

<u>AT1</u>	<u>Power meter</u>
60	-60.0 ± 1.0 dBm
50	-50.0 ± 1.0 dBm
40	-40.0 ± 1.0 dBm
30	-30.0 ± 1.0 dBm

- g Set ESTS AT1 to 30. Record spectrum analyzer reading.
- h Set ESTS USB/LSB switch to LSB.
- i Set center frequency of spectrum analyzer to 120 MHz.

**5-6 TEST EQUIPMENT CALIBRATION - Continued**

- j Disconnect W7 from IFP.
- k Connect spectrum analyzer to the end of W7.
- l Amplitude must be within + 1.0 dB of step g.
- m Set ESTS USB/LSB switch to USB.
- n Set center frequency of spectrum analyzer to 180 MHz.
- o Disconnect W8 from IFP.
- p Connect spectrum analyzer to the end of W8.
- q Amplitude must be within + 1.0 dB of step g.
- r Connect VVM as shown in figure 5-2 view A. Make sure all cable connections are tight.
- s Set rf signal generator to 150.0 MHz. -10 dBm output.
- t Zero the VVM.
- u Remove power divider and connect adaptors to VVM probes as shown in figure 5-2, view B.
- v Remove W3 from IFP J2 (A) and connect VVM reference probe (channel A) to W3.
- w Remove W5 from IFP J5 (C) and connect VVM measuring probe (channel B
- x Remove W4 from ESTS J4 (B) and W6 from ESTS J6 (D). Connect 50 ohm loads to ESTS J4 and J6.
- y Record VVM phase reading.
- z Remove W3 from ESTS J3. Move 50 ohm load from ESTS J4 to ESTS J3. Disconnect W4 from IFP J4 and connect VVM channel A to W4. Record phase reading.
- aa The difference between the VVM phase reading here and the reading taken in step y must be less than 0.5 degree. Record the difference (step y - step z).
- ab Move 50 ohm load from ESTS J3 to ESTS J5. Connect W3 to ESTS J3. Connect VVM channel A to W3 and VVM channel B to W4.

**5- TEST EQUIPMENT CALIBRATION - Continued**

ac Zero the VVM.

ad Amplitude reading must be - 1.0 +1.0 dB.

ae Step ESTS PHASE/DEG switch and verify amplitude and phase as follows:

<u>PHASE/DEG</u>	<u>Amplitude</u>	<u>Phase</u>
+180	-1.0 ± 1.0 dB	0.0 ± 2.0 degrees
+135	-1.0 ± 1.0 dB	0.0 ± 2.0 degrees
+90	-1.0 ± 1.0 dB	0.0 ± 2.0 degrees
+45	-1.0 ± 1.0 dB	0.0 ± 2.0 degrees
-45	-1.0 ± 1.0 dB	0.0 ± 2.0 degrees
-90	-1.0 ± 1.0 dB	0.0 ± 2.0 degrees
-135	-1.0 ± 1.0 dB	0.0 ± 2.0 degrees
-180	-1.0 ± 1.0 dB	0.0 ± 2.0 degrees

af Reconnect W5 and W6 to ESTS J5 and J6, respectively. Disconnect W5 from IFP.

ag Connect VVM Channel B to end of W5.

5-6 TEST EQUIPMENT CALIBRATION - Continued

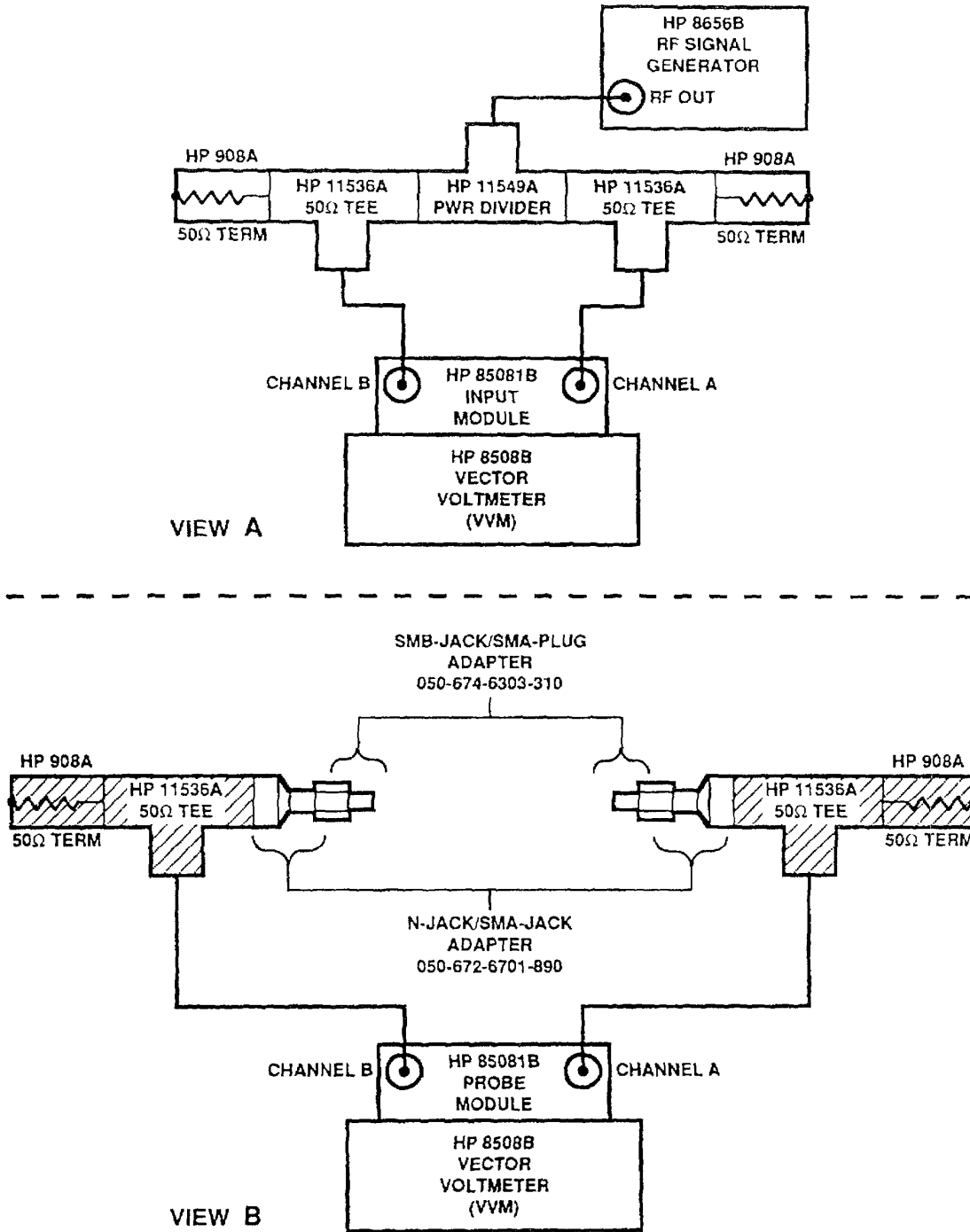


FIGURE 5-2 CALIBRATION SETUP

**5-6 TEST EQUIPMENT CALIBRATION - Continued**

ah Set ESTS PHASE/DEG switch to 0.

ai Amplitude reading must be  $-1.0 \pm 1.0$  dB. Phase reading must be  $0.0 \pm 0.5$  degree.

aj Step ESTS PHASE/DEG switch and verify amplitude and phase as follows:

<u>PHASE/DEG</u>	<u>Amplitude</u>	<u>Phase</u>
+180	$-1.0 + 1.0$ dB	$+180.0 + 2.0^\circ$
+135	$-1.0 \pm 1.0$ dB	$+135.0 \pm 2.0^\circ$
+90	$-1.0 + 1.0$ dB	$+90.0 - 2.0^\circ$
+45	$-1.0 + 1.0$ dB	$+45.0 \pm 2.0^\circ$
-45	$-1.0 + 1.0$ dB	$-45.0 + 2.0^\circ$
-90	$-1.0 + 1.0$ dB	$-90.0 + 2.0^\circ$
-135	$-1.0 \pm 1.0$ dB	$-135.0 + 2.0^\circ$
-180	$-1.0 \pm 1.0$ dB	$-180.0 + 2.0^\circ$

ak Move VVM channel B to the end of W6.

al Set ESTS PHASE/DEG switch to 0.

am Amplitude reading must be  $-1.0 \pm 1.0$  dB. Phase reading must be  $0.0 \pm 0.5$  degree.

an Step ESTS PHASE/DEG switch and verify amplitude and phase as follows.

<u>PHASE/DEG</u>	<u>Amplitude</u>	<u>Phase</u>
+180	$-1.0 + 1.0$ dB	$+180.0 + 2.0^\circ$
+135	$-1.0 + 1.0$ dB	$+135.0 + 2.0^\circ$
+90	$-1.0 + 1.0$ dB	$+90.0 + 2.0^\circ$
+45	$-1.0 + 1.0$ dB	$+45.0 + 2.0^\circ$
-45	$-1.0 \pm 1.0$ dB	$-45.0 + 2.0^\circ$
-90	$-1.0 \pm 1.0$ dB	$-90.0 \pm 2.0^\circ$
-135	$-1.0 + 1.0$ dB	$-135.0 + 2.0^\circ$
-180	$-1.0 \pm 1.0$ dB	$-180.0 + 2.0^\circ$

ao If the above cannot be met, rearrange cables W3 (TS) through W6 (TS) until the conditions can be met, replace cable set, or send ESTS for calibration.

ap Calibration complete. Restore ESTS connections as in figure 5-1.

**5-7 TEST PROCEDURES AND FAULT ISOLATION**

- a Use following procedure. The procedure is arranged in four columns.
- (1) Column (1). Contains step number. Do not skip steps unless ACTION column (4) directs otherwise.
  - (2) Column (2). Contains test operation to be performed.
  - (3) Column (3). Contains normal indication to be observed when procedure has been performed.
  - (4) Column (4). Prescribes corrective action.

**WARNING**

Whenever possible, shut off the power source before beginning work inside unit to prevent electrical shock.

**NOTE**

If repeating test procedure, be sure test setup (para 5-5) and calibrations (para 5-6) are correct before proceeding.

5-7 TEST PROCEDURES AND FAULT ISOLATION

STEP	PROCEDURE INDICATIONS	ACTION	
<b>PART I. TEST PROCEDURE</b>			
<b>A. BIT MODE TEST</b>			
<b>NOTE</b>			
All switches, indicators, and test points are on ESTS unless stated otherwise			
TTL and ECL logic levels stated in this procedure are defined as follows:			
Vdc			
TTL low = 0.0 to +1.0 high = +2.4 to + 5.5			
ECL low = -1.85 to - 1.63 high= - .81 to - .98			
1	Connect frequency counter to IFP connector J10.		
2	Set AT1 dial to 60.		
3	Set BIT TEST switch to USB.		
4	Read frequency counter	150.00 - 0.01 MHz	If not, replace AI A3 (para 5-31).
5	Disconnect frequency counter.		
6	Connect VVM CH A to IFP connector J1 0.		
7	Read VVM	-26.5 + 3.5 dBm	If not, replace A1A3 (para 5-31).
8	Observe LEDs	Only ST TRIG, CW and USB light	If not, go to step 133.
9	Set BIT TEST switch to LSB.		
10	Disconnect VVM.		
11	Connect frequency counter to IFP connector J1 0.		

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
12	Read frequency counter	150.00 + 0.01 MHz	If not, replace A1A3 (para 5-31).
13	Disconnect frequency counter.		
14	Connect VVM CH A to IFP connector J10.		
15	Read VVM	-26.5 + 3.5 dBm	If not, replace A1A3 (para 5-31).
16	Disconnect VVM.		
17	Observe LEDs	Only ST TRIG, CW, and LSB light	If not, go to step 133.
18	Turn DATA SELECT switch to each of the following settings At each setting read ESTS DVM		<p>a. If FRUQ fails, go to step 43.                      b. If FRUI fails, go to step 55.                      c. If LOG fails, go to step 32.                      d. Any other failure, go to step</p>
21	<u>Setting</u>	<u>ESTS DVM</u>	
	B-CQ	2.70 ± 0.30	
	B-CI	<1.44	
	A-CQ	2.7 + 0.30	
	A-CI	<1.44	
	A-DQ	2.70 + 0.30	
	A-DI	<1.44	
	FRUQ	<1.44	
	FRUI	2.70 + 0.30	
	LOG	2.53 + 0.49	
20	19 Connect o-scope CH 1 to ESTS PW GATE test point. Read ECL positive going pulse on o-scope display	PW: 500 + 20 ns PRI: 1000 + 50 us	<p>a. If not, replace A2A1 (para 5-32).                      b. If replacing A2A1 does not correct fault, replace A2A3 (para 5-32).                      c. If fault persists, send IFP to higher level maintenance.</p>



5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
<b>B. PHASE TRACKING 150 MHz/-30 DBm CW</b>			
21	On ESTS, set: Switch      Set to		
22	BIT TEST   OFF AT1          30 Observe LEDs	Only ST TRIG, CW, and LSB light	If not, go to step 133.
23	Set DATA SELECT switch to B-CQ.		
24	Turn PHASE-DEG switch to each of the following settings At each setting read ESTS DVM		a. If reading is within + 0.16 to + 0.21 tolerance, aline module (para 5-8) indicated by DATA SELECT switch position:
	Setting	ESTS DVM	
	-180	2.70 + 0.15	Position    Module B-CQ    A2A7 A-CQ    A2A5 A-DQ    A2A6
	-135	1.35 + 0.15	
	- 90	<1.26	
	- 45	1.35 + 0.15	
	0	2.70 ± 0.15	
	+ 45	4.05 + 0.15	
	+ 90	>4.14	
	+135	4.05 t 0.15	
	+180	2.70 + 0.15	b. If reading exceeds +/- 0.21 tolerance, go to step indicated by DATA SELECT switch position: Position    Step B-CQ    176 A-CQ    180 A-DQ    184 As specified.
25	Set DATA SELECT switch to A-CQ. Repeat step 24.	As specified	

5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
26	Set DATA SELECT switch to A-DQ. Repeat step 24.	As specified	As specified.
27	Set DATA SELECT switch to B-CI.		
28	Turn PHASE-DEG switch to each of following settings. At each setting read ESTS DVM	<u>ESTS</u>	<p>a. If reading is within + 0.16 to + 0.21 tolerance, aline module (para 5-8) indicated by DATA SELECT switch position:</p> <p><u>Position</u> <u>Module</u></p> <p>B-CI A2A7 A-CI A2A5 A-DI A2A6</p>
	<u>Setting</u>	>4.14	<p>b. If reading exceeds + 0.21 tolerance, go to step indicated by DATA SELECT switch position:</p> <p><u>Position</u> <u>Step</u></p> <p>B-CI 188 A-CI 192 A-DI 196</p>
	-180	4.05 + 0.15	
	-135	2.70 + 0.15	
	- 90	1.35 + 0.15	
	- 45	<1.26	
	0	1.35 + 0.15	
	+ 45	2.70 + 0.15	
	+ 90	4.05 + 0.15	
	+135	>4.14	
	+180		
29	Set DATA SELECT switch to A-CI. Repeat step 28.	As specified	As specified.
30	Set DATA SELECT switch to A-DI. Repeat step 28.	As specified	As specified.
31	Observe LEDs	Only ST TRIG, CW, and LSB light.	If not, go to step 133.

5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION																								
<b>C. LOG AMPLITUDE VS. DYNAMIC RANGE</b>																										
32	<p>On ESTS, set:</p> <table border="0"> <tr> <td><u>Switch</u></td> <td>Set to</td> </tr> <tr> <td>AT1</td> <td>0</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>EXT THRESH</td> <td>ON</td> </tr> <tr> <td>USB/LSB</td> <td>LSB</td> </tr> <tr> <td>DATA SELECT</td> <td>LOG</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>EXT THRESH</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> </table>	<u>Switch</u>	Set to	AT1	0	MOD/PW	CW	EXT THRESH	ON	USB/LSB	LSB	DATA SELECT	LOG	PHASE-DEG	0	DVM SEL	EXT THRESH	BIT TEST	OFF							
<u>Switch</u>	Set to																									
AT1	0																									
MOD/PW	CW																									
EXT THRESH	ON																									
USB/LSB	LSB																									
DATA SELECT	LOG																									
PHASE-DEG	0																									
DVM SEL	EXT THRESH																									
BIT TEST	OFF																									
33	<p>Adjust EXT THRESH ADJ control for -0.15 on ESTS DVM.</p>																									
34	<p>Set DVM SEL switch to volts.</p>	<p><b>NOTE</b> Step 35 will be repeated to test CW and 600 ns/200 ns pulses.</p>																								
35	<p>Set following switches to each of following settings. At each setting read ESTS DVM.</p>	<p>a. If incorrect in CW and pulse, go to step 202.</p> <p>b. If incorrect in 600 ns or 200 ns pulse, perform alinements in para 5-11 and 5-27.</p>																								
	<table border="0"> <tr> <td><u>EXTTHRESH</u></td> <td><u>AT1</u></td> </tr> <tr> <td>ON</td> <td>0</td> </tr> <tr> <td>OFF</td> <td>10</td> </tr> <tr> <td>OFF</td> <td>20</td> </tr> <tr> <td>OFF</td> <td>30</td> </tr> <tr> <td>OFF</td> <td>40</td> </tr> <tr> <td>OFF</td> <td>50</td> </tr> <tr> <td>OFF</td> <td>60</td> </tr> </table>	<u>EXTTHRESH</u>	<u>AT1</u>	ON	0	OFF	10	OFF	20	OFF	30	OFF	40	OFF	50	OFF	60	<table border="0"> <tr> <td><u>ESTS DVM</u></td> </tr> <tr> <td>5.00 + 0.23</td> </tr> <tr> <td>4.25 + 0.23</td> </tr> <tr> <td>3.50 + 0.23</td> </tr> <tr> <td>2.75 - 0.23</td> </tr> <tr> <td>2.00 + 0.23</td> </tr> <tr> <td>1.25 + 0.23</td> </tr> <tr> <td>0.501 0.23</td> </tr> </table>	<u>ESTS DVM</u>	5.00 + 0.23	4.25 + 0.23	3.50 + 0.23	2.75 - 0.23	2.00 + 0.23	1.25 + 0.23	0.501 0.23
<u>EXTTHRESH</u>	<u>AT1</u>																									
ON	0																									
OFF	10																									
OFF	20																									
OFF	30																									
OFF	40																									
OFF	50																									
OFF	60																									
<u>ESTS DVM</u>																										
5.00 + 0.23																										
4.25 + 0.23																										
3.50 + 0.23																										
2.75 - 0.23																										
2.00 + 0.23																										
1.25 + 0.23																										
0.501 0.23																										

5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION															
36	Set MODIPW switch to 600 ns. Repeat step 35.	200 + 10 ns pulse.															
37	Disconnect W3 from IFP and connect it to o-scope CH 1.																
38	Set AT 1 dial to 0.																
39	Adjust PW SET control. Read o-scope.																
40	Disconnect W3 from o-scope.																
41	Connect W3 to IFP connector J2.	D. FRUQ-30 dBm															
42	Repeat step 35.																
43	On ESTS, set:	NOTE															
	<table border="0"> <thead> <tr> <th>Switch</th> <th>Set to</th> </tr> </thead> <tbody> <tr> <td>IF FREQ MHz</td> <td>135.0</td> </tr> <tr> <td>AT 1</td> <td>30</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>DATA SELECT FRUQ</td> <td></td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> </tbody> </table>		Switch	Set to	IF FREQ MHz	135.0	AT 1	30	MOD/PW	CW	DATA SELECT FRUQ		PHASE-DEG	0	PW SET	full cw	BIT TEST
Switch	Set to																
IF FREQ MHz	135.0																
AT 1	30																
MOD/PW	CW																
DATA SELECT FRUQ																	
PHASE-DEG	0																
PW SET	full cw																
BIT TEST	OFF																
	Acceptable reading tolerances for IF FREQ MHz switch positions in step 44 are as follows:	<p>11 of 12 readings must be within + 0.42            9 of 12 readings must be within + 0.27            7 of 12 readings must be within + 0.21</p>															

5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
44	Turn IF FREO MHz switch through following settings At each setting, read and record ESTS DVM indication.		a. If any reading exceeds tolerance, aline A2A8 (para 5-8).  b. If fault persists, go to step
211.	<u>Setting</u>	<u>ESTS DVM</u>	
	135.0	4.05	
	137.0	3.51	
	139.0	2.97	
	141.0	2.43	
	143.0	1.89	
	145.0	1.35	
	155.0	1.35	
	157.0	1.89	
	159.0	2.43	
	161.0	2.97	
	163.0	3.51	
	165.0	4.05	
45	Set MOD/PW switch to 600 ns	As specified	As specified.
	Repeat step 44.		
46	On ESTS, set:		
	Switch                      Set to		
	IF FREQ MHz              150.0		
	MOD/PW                      CW		
47	Read ESTS DVM	< 0.95	If not, go to step 211.
48	Set MOD/PW to 600 ns	< 0.95	If not, go to step 211.
	Read ESTS DVM.		
49	Disconnect W3 from IFP and connect it to o-scope CH 1.		
50	Set AT1 dial to 0.		
51	Adjust PW SET control. Read o-scope.	200 + 10 ns pulse	
52	Disconnect W3 from o-scope and connect it to IFP connector J2.		

5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION															
53 54	Set AT1 dial to 30. Read ESTS DVM	< 0.95	If not, go to step 211.														
55	On ESTS, set: Switch                      Set to  IF FREQ MHz              145.0 MOD/PW                      CW PW SET                      full cw DATA SELECT              FRUI BIT TEST                      OFF	<b>E. FRUI -30 dBm</b>															
	<b>NOTE</b>																
	Acceptable reading tolerance for IF FREQ MHz switch positions in step 56 are as follows:																
	5 of 6 readings must be within + 0.42																
	4 of 6 readings must be within - 0.27																
	3 of 6 readings must be within - 0.21																
56	Turn IF FREQ MHz switch through following settings At each setting read and record ESTS DVM indication.		a. If any reading exceeds tolerance, aline A2A8 (para 5-8).														
	<table border="0" style="width: 100%;"> <thead> <tr> <th style="text-align: left;"><u>Setting</u></th> <th style="text-align: left;"><u>ESTS DVM</u></th> </tr> </thead> <tbody> <tr><td>145.0</td><td>4.05</td></tr> <tr><td>147.0</td><td>3.51</td></tr> <tr><td>149.0</td><td>2.97</td></tr> <tr><td>151.0</td><td>2.43</td></tr> <tr><td>153.0</td><td>1.87</td></tr> <tr><td>155.0</td><td>1.35</td></tr> </tbody> </table>	<u>Setting</u>	<u>ESTS DVM</u>	145.0	4.05	147.0	3.51	149.0	2.97	151.0	2.43	153.0	1.87	155.0	1.35		b. If fault persists, go to step 216.
<u>Setting</u>	<u>ESTS DVM</u>																
145.0	4.05																
147.0	3.51																
149.0	2.97																
151.0	2.43																
153.0	1.87																
155.0	1.35																
57	Set MOD/PW switch to 600 ns. Repeat step 56.	As specified	As specified.														

5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION																					
58	<p>Set MOD/PW switch to CW</p> <p>Read ESTS DVM for following IF FREQ MHz switch positions</p> <table border="0"> <tr> <td><u>Setting</u></td> <td><u>ESTS DVM</u></td> </tr> <tr> <td>135.0</td> <td>&gt; 3.64</td> </tr> <tr> <td>140.0</td> <td>&gt; 4.44</td> </tr> <tr> <td>160.0</td> <td>&lt; 0.95</td> </tr> <tr> <td>165.0</td> <td>&lt; 1.75</td> </tr> </table>	<u>Setting</u>	<u>ESTS DVM</u>	135.0	> 3.64	140.0	> 4.44	160.0	< 0.95	165.0	< 1.75		<p>a. If not, aline A2A8 (para 5-8).</p> <p>b. If fault persists, go to step 216.</p>										
<u>Setting</u>	<u>ESTS DVM</u>																						
135.0	> 3.64																						
140.0	> 4.44																						
160.0	< 0.95																						
165.0	< 1.75																						
59	<p>Set MOD/PW switch to 600 ns. Repeat step 58.</p>	As specified	As specified.																				
60	<p>Disconnect W3 from IFP and connect it to o-scope CH 1.</p>																						
61	<p>Set AT1 dial to 0.</p>																						
62	<p>Adjust PW SET control. Read o-scope.</p>	200 + 10 ns pulse																					
63	<p>Disconnect W3 from o-scope and connect it to IFP connector J2.</p>																						
64	<p>Set AT1 dial to 30.</p>																						
65	<p>Set IF FREQ MHz switch to 150.0. Read ESTS DVM.</p>	2.70 + 0.30	<p>a. If not, aline A2A8 (para 5-8)</p> <p>b. If fault persists, go to step 216.</p>																				
<b>F. EXTERNAL THRESHOLD @ 150.0 MHz</b>																							
66	<p>On ESTS, set:</p> <table border="0"> <tr> <td><u>Switch</u></td> <td><u>Set to</u></td> </tr> <tr> <td>USB/LSB</td> <td>LSB</td> </tr> <tr> <td>EXTTHRESH</td> <td>OFF</td> </tr> <tr> <td>AT1</td> <td>60</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>DVM SEL</td> <td>EXT THRESH</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>full cw</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	USB/LSB	LSB	EXTTHRESH	OFF	AT1	60	AT2	cf	DVM SEL	EXT THRESH	EXT THRESH		ADJ	full cw	MOD/PW	CW	PHASE-DEG	0		
<u>Switch</u>	<u>Set to</u>																						
USB/LSB	LSB																						
EXTTHRESH	OFF																						
AT1	60																						
AT2	cf																						
DVM SEL	EXT THRESH																						
EXT THRESH																							
ADJ	full cw																						
MOD/PW	CW																						
PHASE-DEG	0																						

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

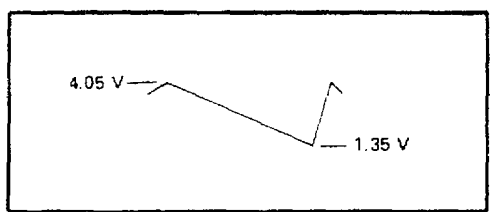
STEP	PROCEDURE INDICATIONS	ACTION	
67	Increase AT2 dial setting until ST TRIG and PW RST lights go out.	ST TRIG and PW RST lights go out	If not, go to step 69.
68	Step AT1 dial through following settings. At each setting adjust EXT THRESH ADJ ccw until both ST TRIG and PW RST lights go out. Read ESTS DVM.	<u>ESTS DVM</u>	
	<u>EXT THRESH</u> <u>AT1</u>		
	ON                      50	-0.10 + 0.04	
	ON                      40	-0.20 i 0.04	
	ON                      30	-0.30 + 0.04	
	ON                      20	-0.40 + 0.04	
	ON                      10	-0.50 + 0.04	
	ON                      0	-0.60 + 0.04	
69	On ESTS, set:  Switch              Set to  USB/LSB          USB EXTTHRESH      OFF AT1                  60 AT2                  cf DVM SEL          EXTTHRESH EXT THRESH ADJ                  full cw		
70	Increase AT2 dial setting until ST TRIG and PW RST lights go out.	ST TRIG and PW RST lights go out	If not, go to step 71.



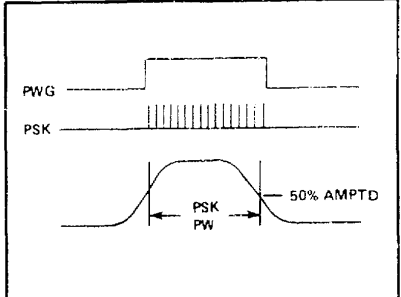
5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION																					
71	<p>Step AT1 dial through following settings. At each setting adjust EXT THRESH ADJ ccw until both ST TRIG and PW RST lights go out Read ESTS DVM</p> <table border="0"> <thead> <tr> <th><u>EXT THRESH</u></th> <th><u>AT1</u></th> <th><u>ESTS DVM</u></th> </tr> </thead> <tbody> <tr> <td>ON</td> <td>50</td> <td>-0.10 + 0.04</td> </tr> <tr> <td>ON</td> <td>40</td> <td>-0.20 + 0.04</td> </tr> <tr> <td>ON</td> <td>30</td> <td>-0.30 ± 0.04</td> </tr> <tr> <td>ON</td> <td>20</td> <td>-0.40 + 0.04</td> </tr> <tr> <td>ON</td> <td>10</td> <td>-0.50 + 0.04</td> </tr> <tr> <td>ON</td> <td>0</td> <td>-0.60 + 0.04</td> </tr> </tbody> </table>	<u>EXT THRESH</u>	<u>AT1</u>	<u>ESTS DVM</u>	ON	50	-0.10 + 0.04	ON	40	-0.20 + 0.04	ON	30	-0.30 ± 0.04	ON	20	-0.40 + 0.04	ON	10	-0.50 + 0.04	ON	0	-0.60 + 0.04	<p>a. If steps 67 through 71 are incorrect, replace A2A1 (para 5-32).</p> <p>b. If replacing A2A1 does not correct fault, replace A2A3 (para 5-32).</p> <p>c. If only steps 67 and/or 68 incorrect, replace A1A7 (para 5-31).</p> <p>d. If only steps 70 and/or 71 incorrect, replace A1A6 (para 5-31).</p> <p>e. If fault persists, send IFP to higher level maintenance.</p>
<u>EXT THRESH</u>	<u>AT1</u>	<u>ESTS DVM</u>																					
ON	50	-0.10 + 0.04																					
ON	40	-0.20 + 0.04																					
ON	30	-0.30 ± 0.04																					
ON	20	-0.40 + 0.04																					
ON	10	-0.50 + 0.04																					
ON	0	-0.60 + 0.04																					
<b>G. CHIRP</b>																							
72	<p>On ESTS, set:</p> <table border="0"> <thead> <tr> <th><u>Switch</u></th> <th><u>Set to</u></th> </tr> </thead> <tbody> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>DATA SELECT</td> <td>FRUI</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>IF FREQ MHz</td> <td>145.0</td> </tr> <tr> <td>MOD/PW</td> <td>CHIRP</td> </tr> <tr> <td>USB/LSB</td> <td>LSB</td> </tr> <tr> <td>EXTTHRESH</td> <td>OFF</td> </tr> </tbody> </table>	<u>Switch</u>	<u>Set to</u>	AT2	cf	AT1	30	DATA SELECT	FRUI	DVM SEL	VOLTS	IF FREQ MHz	145.0	MOD/PW	CHIRP	USB/LSB	LSB	EXTTHRESH	OFF				
<u>Switch</u>	<u>Set to</u>																						
AT2	cf																						
AT1	30																						
DATA SELECT	FRUI																						
DVM SEL	VOLTS																						
IF FREQ MHz	145.0																						
MOD/PW	CHIRP																						
USB/LSB	LSB																						
EXTTHRESH	OFF																						
73	<p>Connect o-scope:</p> <table border="0"> <thead> <tr> <th><u>Probe</u></th> <th><u>ESTS test point</u></th> </tr> </thead> <tbody> <tr> <td>CH 2</td> <td>DATA</td> </tr> <tr> <td>EXT TRIG</td> <td>PRF OUT</td> </tr> </tbody> </table>	<u>Probe</u>	<u>ESTS test point</u>	CH 2	DATA	EXT TRIG	PRF OUT																
<u>Probe</u>	<u>ESTS test point</u>																						
CH 2	DATA																						
EXT TRIG	PRF OUT																						

5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
74	On o-scope, set:  Switch                      Set to  Time base                      5 us/div CH 2 (vertical)                      1 v/div (dc) Trigger                      EXT		
75	Adjust o-scope trigger level, as required to observe waveform.		Waveform Slightly curved downward ramp  Peak: 4.05 - 0.56 V  Base: 1.35 ± 0.74 V
<b>H. PHASE SHIFT KEYING - PSK</b>			
76	On ESTS, set: <u>Switch</u> <u>Set to</u>		
77	IF FREQ MHz                      145.0 MOD/PW                      PSK Connect o-scope: <u>Probe</u> <u>ESTS test point</u>		
78	CH 1                      PWG CH 2                      PSK EXT TRIG                      PRF OUT On o-scope, set: <u>Switch</u> <u>Set to</u>  Trigger                      EXT Vert Mode                      ALT		

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION
79	<p>Read o-scope CH 1 and CH 2 waveforms.</p> <p>Measure PSK PW from 50% amplitude points of displayed pulse.</p>	<p style="text-align: center;"><b>NOTE</b></p> <div style="text-align: center;">  </div> <p><u>Waveforms</u></p> <p>PSK pulses only occur during PWG high:</p> <p>PSK PRI: 1.0 + 0.1 us</p> <p>PSK PW: 20.0 L 10.0 ns</p> <p>PSK pls amptd: 1.0 * 0.1 Vp-p</p> <p>a. If not, replace A2A4 (para 5-32).</p> <p>b. If fault persists, send IFP to higher level maintenance.</p>
		5-23

5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION												
<b>I. AMPLITUDE DIFFERENCE @ 150.0 MHz</b>														
80	<p>On ESTS, set:</p> <table border="0"> <tr> <td><u>Switch</u></td> <td><u>Set to</u></td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>USB/LSB</td> <td>LSB</td> </tr> <tr> <td>IF FREQ MHz</td> <td>150.0</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	MOD/PW	CW	AT1	30	AT2	cf	USB/LSB	LSB	IF FREQ MHz	150.0	
<u>Switch</u>	<u>Set to</u>													
MOD/PW	CW													
AT1	30													
AT2	cf													
USB/LSB	LSB													
IF FREQ MHz	150.0													
81	Change test setup (fig. 5-3).													
82	Set external signal generator for 150.0 MHz at 0 dBm.													
83	Set external attenuator for 30 dB in.													
84	Disconnect W6 from IFP and connect it to VVM.													
85	Adjust external signal generator for -30 dBm indication on VVM.													
86	Disconnect W6 from VVM and connect it to IFP CONNECTOR J6.													
<b>NOTE</b>														
In steps 87 and 89 equal intensity may not be achieved; it is acceptable if one or the other LEDs flickers.														
87	Increase step attenuator setting until ST TRIG and PW RST LEDs are lit with approximately equal intensity.													

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

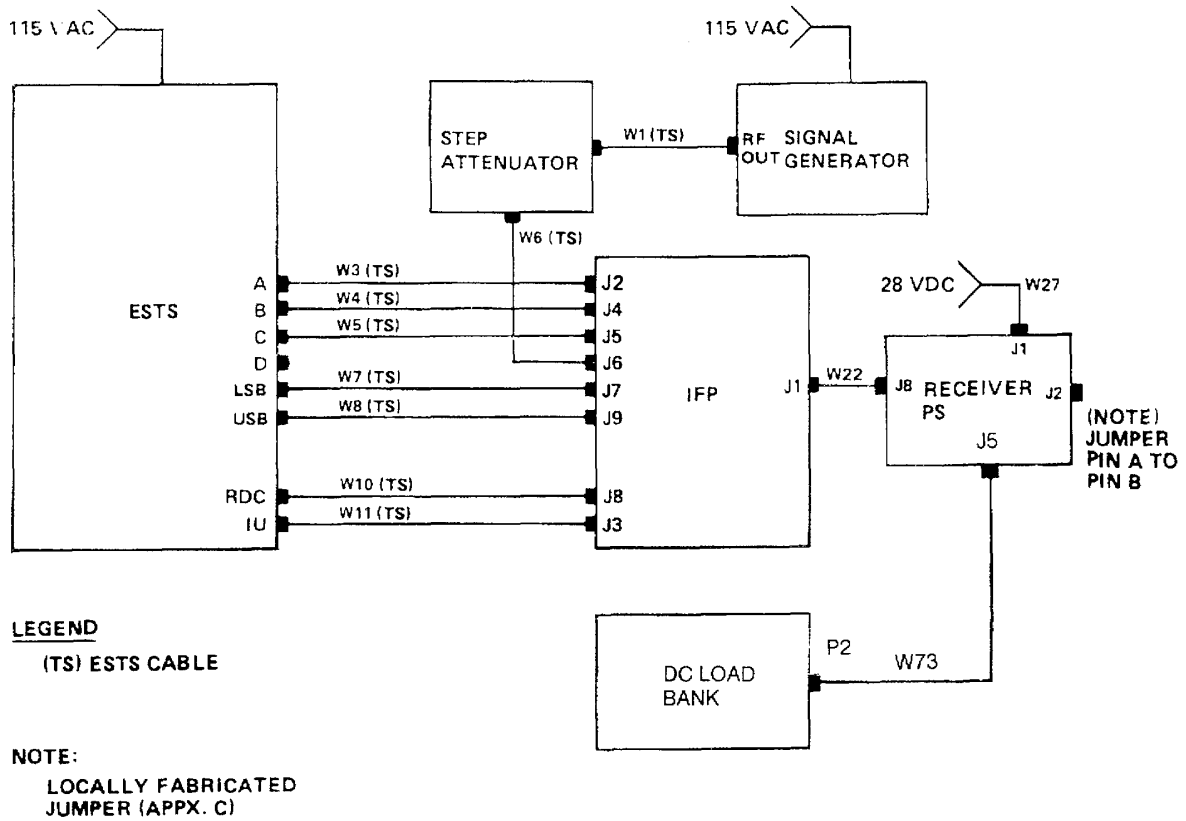


FIGURE 5-3. AMPLITUDE DIFFERENCE TEST SETUP

5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION															
88	Read step attenuator setting	43.0 + 3.0 dB	a. If setting exceeds + 4.0 to + 6.0 tolerance, aline A2A9 (para 5-8).  b. If setting exceeds + 6.0 tolerance, replace A2A2 (para 5-32). c. If fault persists, send IFP to higher level maintenance.														
89	Reduce step attenuator setting until ST TRIG and PW RST LEDs are lit with approximately equal intensity.	17.0 + 3.0 dB	a. If setting exceeds + 4.0 to + 6.0 tolerance, aline A2A9 (para 5-8).  b. If setting exceeds + 6.0 tolerance, replace A2A2 (para 5-32).  c. If fault persists, send IFP to higher level maintenance.														
90	Read step attenuator setting	17.0 + 3.0 dB	a. If setting exceeds + 4.0 to + 6.0 tolerance, aline A2A9 (para 5-8).  b. If setting exceeds + 6.0 tolerance, replace A2A2 (para 5-32).  c. If fault persists, send IFP to higher level maintenance.														
91	Set USB/LSB switch to USB. Repeat steps 83 through 90.	<b>J. BANDWIDTH</b>															
92	Repeat test setup (fig. 5-1)																
93	On ESTS, set:																
	<table border="0"> <thead> <tr> <th><u>Switch</u></th> <th><u>Set to</u></th> </tr> </thead> <tbody> <tr> <td>IF FREQ MHz</td> <td>150.0</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>USB/LSB</td> <td>USB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> </tbody> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHz	150.0	AT1	30	AT2	cf	USB/LSB	USB	BW CMD	30 MHz	MOD/PW	CW	5-26	
<u>Switch</u>	<u>Set to</u>																
IF FREQ MHz	150.0																
AT1	30																
AT2	cf																
USB/LSB	USB																
BW CMD	30 MHz																
MOD/PW	CW																

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

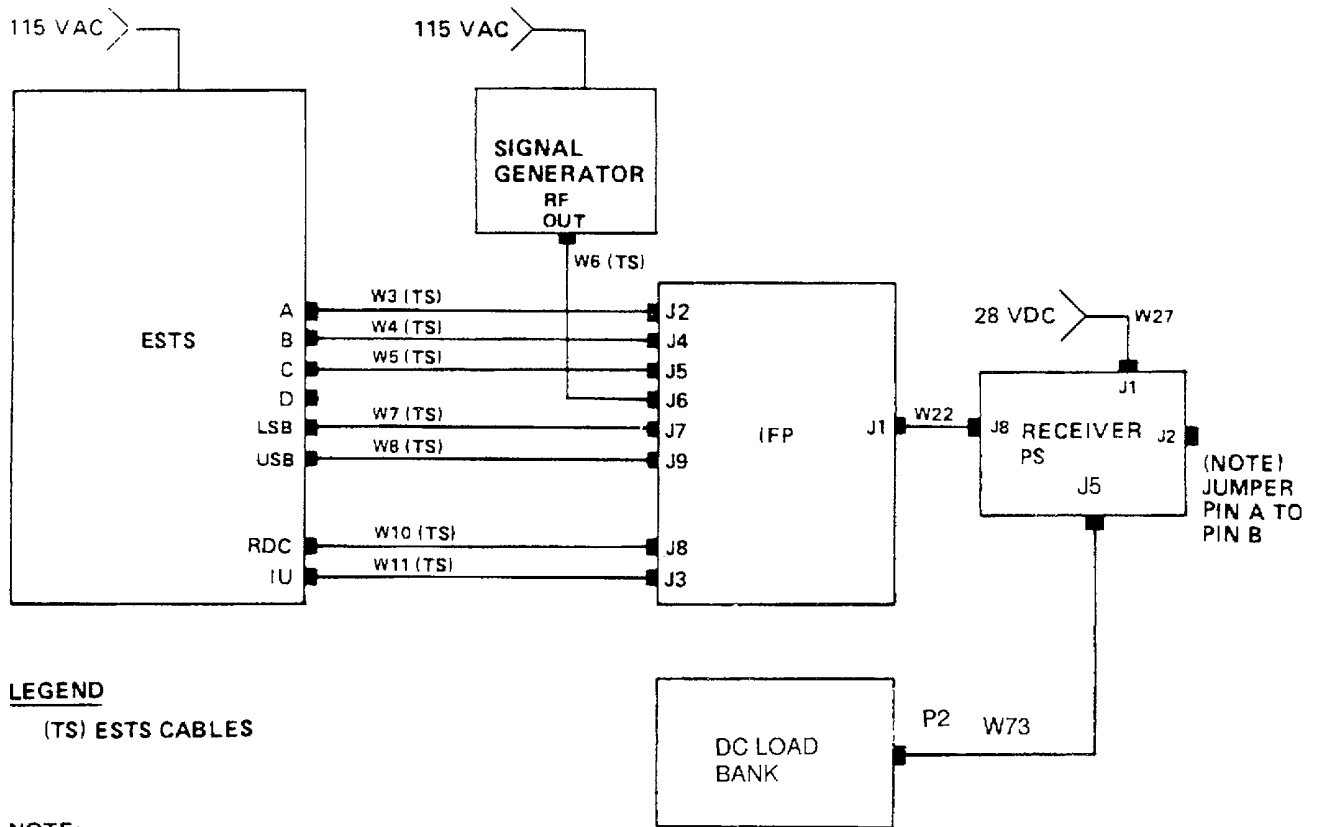
STEP	PROCEDURE INDICATIONS	ACTION	
94	Increase IF FREQ MHz switch setting in 0.1 MHz steps, until ST TRIG and PW RST LEDs are lit approximately equal intensity.		
95	Read IF FREQ MHz switch setting	166.0 - 1.0	<p>a. If setting exceeds D 1.1 to <math>\pm 3.0</math> MHz tolerance, aline A2A11 (para 5-8).</p> <p>b. If fault persists, go to step 220.</p>
96	Decrease IF FREQ MHz switch setting in 0.1 MHz steps, until ST TRIG and PW RST LEDs are lit with approximately equal intensity.		
97	Read IF FREQ MHz switch setting	134.0 - 1.0	<p>a. If setting exceeds + 1.1 to <math>\pm 3.0</math> MHz tolerance, aline A2A11 (para 5-8).</p> <p>b. If fault persists, go to step 220.</p>
98	On ESTS, set: <u>Switch</u> <u>Set to</u>		
99	IF FREQ MHz              150.0 BW CMD                      5 MHz		
99	Increase IF FREQ MHz switch setting in 0.1 MHz steps, until ST TRIG and PW RST LEDs are lit with approximately equal intensity.		
100	Read IF FREQ MHz switch setting	153.5 + 1.0	<p>a. If setting exceeds - 1.1 to + 3.0 MHz tolerance, aline A2A11 (para 5-8).</p> <p>b. If fault persists, go to step 220.</p>

5-7 TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
101	Decrease IF FREQ MHz switch setting in 0.1 MHz steps, until ST TRIG and PW RST LEDs are lit with approximately equal intensity.		
102	Read IF FREQ MHz switch setting	146.5 t 1.0	<p>a. If setting exceeds + 1.1 to ± 3.0 MHz tolerance, aline A2A11 (para 5-8).</p> <p>b. If fault persists, go to step 220.</p>
<b>K. FRU DIFFERENCE DF @ 150.0 MHz @ 30 dBm</b>			
103	On ESTS, set:		
	Switch                      Set to		
	USB/LSB                      USB		
	IF FREQ MHz                      150.0		
	BW CMD                      30 MHz		
104	Change test setup (fig. 5-4).		
105	Set external signal generator for 150.0 MHz at -30.0 dBm.		
106	Decrease signal generator frequency until ST TRIG and PW RST LEDs are lit with equal intensity.		
107	Read signal generator frequency setting	136.0 to 138.0 MHz (para 5-8).	<p>a. If not, aline A2A10</p> <p>b. If fault persists, go to step 234.</p>
108	Increase signal generator frequency until ST TRIG and PW RST LEDs are lit with equal intensity.		
109	Read signal generator frequency setting	162.0 MHz (para. 5-8).	<p>a. If not, aline A2A10</p> <p>b. If fault persists, go to step 234.</p>



5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued I



**LEGEND**

(TS) ESTS CABLES

**NOTE:**

LOCALLY FABRICATED  
JUMPER (APPX. C)

FIGURE 5-4. FRU DIFFERENCE TEST SETUP

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION															
110.	Set USB.LSB switch to LSB.																
111.	Repeat steps 105 through 109.	As specified.	As specified.														
<b>L. OUTPUT LEVEL AND PULSE WIDTH</b>																	
112.	Change test setup (fig. 5-1).																
113.	On ESTS, set:  <table border="0" style="width: 100%;"> <thead> <tr> <th style="text-align: left;"><u>Switch</u></th> <th style="text-align: left;"><u>Set to</u></th> </tr> </thead> <tbody> <tr> <td>IF FREQ MHz</td> <td>150.0</td> </tr> <tr> <td>AT1</td> <td>0</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MOD/PW</td> <td>600ns</td> </tr> <tr> <td>PRF</td> <td>500 kHz</td> </tr> <tr> <td>USB/LSB</td> <td>LSB</td> </tr> </tbody> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHz	150.0	AT1	0	AT2	cf	MOD/PW	600ns	PRF	500 kHz	USB/LSB	LSB		
<u>Switch</u>	<u>Set to</u>																
IF FREQ MHz	150.0																
AT1	0																
AT2	cf																
MOD/PW	600ns																
PRF	500 kHz																
USB/LSB	LSB																
114.	Observe LEDs.	ST TRIG, PULSE, and LSB light	If not, go to step 133.														
115.	Disconnect W3 from IFP and connect it to o-scope CH 1.																
116.	Adjust PW SET control o-scope.	Read 250 +/- ns pulse															
117.	Disconnect W3 from o-scope and connect it to IFP connector J2.																
118.	Set AT1 dial to 30.																
119.	Connect o-scope CH 2 to following test points test point read o-scope.  <table border="0" style="width: 100%;"> <thead> <tr> <th style="text-align: left;"><u>Test point</u></th> <th style="text-align: left;"><u>Display</u></th> </tr> </thead> <tbody> <tr> <td>PW GATE</td> <td>250 ± 40 ns (ECL) pulse</td> </tr> <tr> <td>ST TRIG</td> <td>200 ± 25 ns (TTL) pulse</td> </tr> </tbody> </table>	<u>Test point</u>	<u>Display</u>	PW GATE	250 ± 40 ns (ECL) pulse	ST TRIG	200 ± 25 ns (TTL) pulse		a. If not, replace A2A3 At each(para 5-32).  b. If replacing A2A3 does not correct fault, replace A2A1 (para 5-32).  c. If fault persists, send IFP to higher level maintenance.								
<u>Test point</u>	<u>Display</u>																
PW GATE	250 ± 40 ns (ECL) pulse																
ST TRIG	200 ± 25 ns (TTL) pulse																
120.	Set IF FREQ MHz switch to 130.0																

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
121.	Connect o-scope CH 2 to PW RST test point		
122.	Read o-scope.	200 ± 25 ns (TTL) pulse	
123.	Connect o-scope CH 2 to USB/LSB test point.		<p><u>a.</u> If not, replace A2A3 (para 5-32).</p> <p><u>b.</u> If replacing A2A3 does not correct fault, replace A2A1 (para 5-32).</p> <p><u>c.</u> If fault persists, send IFP to higher level maintenance.</p>
124.	<p>Set USB/LSB switch to</p> <p>following settings. At each setting read o-scope.</p> <p>USB LSB</p>	<p>TTL high TTL low</p>	<p><u>a.</u> If not, aline A2A9 (para 5-8).</p> <p><u>b.</u> If alinement does not correct fault, replace A2A2 (para 5-32).</p> <p><u>c.</u> If replacing A2A2 does not correct fault, replace A2A1 (para 5-32).</p> <p><u>d.</u> If fault persists, send IFP to higher level maintenance.</p>
125.	Connect o-scope CH 2 to CW test point.		
126.	Set MOD/PW to CW		
127.	Read o-scope.	0.85 ± 0.3 (TTL) pulse	<p><u>a.</u> If not, replace A2A1 (para 5-32).</p> <p><u>b.</u> If replacing A2A1 does not correct fault, replace A2A3 (para 5-32).</p> <p><u>c.</u> If fault persists, send IFP to higher level maintenance.</p>

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
<b>M. MAXIMUM PULSE WIDTH</b>			
128.	On ESTS, set: <u>Switch</u> <u>Set to</u>  MOD/PW                      100us PRF                              1 kHz PW SET                         full ccw		
129.	Sync o-scope CH 1, positive. Connect o-scope: <u>Probe</u> <u>Test point</u>  CH 1                            PWG CH2                             CW		
130.	Slowly turn PW SET clockwise until CH 2 pulse appears on o-scope.		
131.	Measure CH 1 pulse width.	100 + 10 us (TTL) pulse	<u>a.</u> If not, replace A2A1 (para 5-32).  <u>b.</u> If replacing A2A1 does not correct fault, replace A2A3 (para 5-32).  <u>c.</u> If fault persists, send IFP to higher level maintenance.
132.	Test procedure complete:  <u>a.</u> Remove power from test equipment.  <u>b.</u> Remove IFP from test setup.  <u>c.</u> If covers removed, install side covers (para 5-30).		

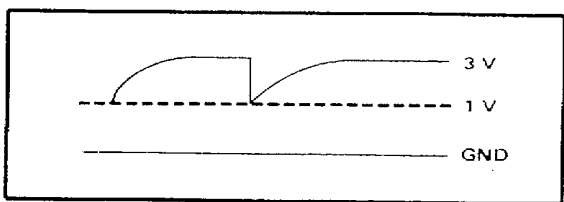
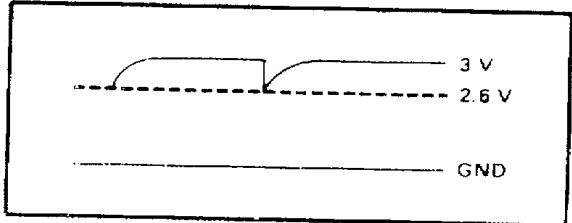
5-7. TEST PROCEDURES AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION												
<b>PART II. FAULT ISOLATION</b>														
<b>A. LED FAULT</b>														
133.	For following LED errors: <u>a.</u> All LEDs failed. <u>b.</u> ST TRIG LED failed (PW RST LED lit). <u>c.</u> CW/PULSE LEDs failed. <u>d.</u> USB/LSB LEDs failed	Go to step 134. Go to step 144.  Go to step 164. Go to step 165.												
134.	Remove side covers (para 5-23).													
135.	Using FO-3, check voltage between following test points and E3 (GND):	<u>Vdc</u>  E2 = +15.0 ± 0.15 E4 = -15.0 ± 0.15 E1 = + 5.5 ± 0.10 E5 = - 5.5 ± 0.10	If not, send IFP to higher level maintenance.											
136.	Remove A2A3 (para 5-32).													
137.	Install A2A3 on extender.													
138.	Install extender in IFP A2A3 slot.													
139.	On ESTS, set:  <table border="0" style="width: 100%;"> <tr> <td style="text-align: left;"><u>Switch</u></td> <td style="text-align: left;"><u>Set to</u></td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>MOD/PW</td> <td>600 ns</td> </tr> <tr> <td>USB/LSB</td> <td>USB</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	AT1	30	MOD/PW	600 ns	USB/LSB	USB	PW SET	full cw	BIT TEST	OFF	
<u>Switch</u>	<u>Set to</u>													
AT1	30													
MOD/PW	600 ns													
USB/LSB	USB													
PW SET	full cw													
BIT TEST	OFF													

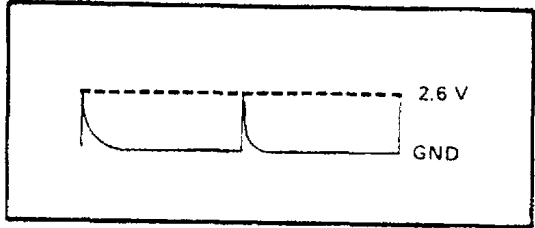
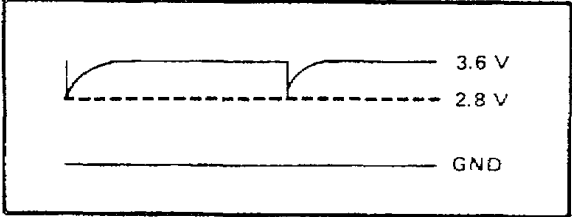
5-7. TEST PROCEDURES AND FAULT ISOLATION-Continued

STEP	PROCEDURE INDICATIONS	ACTION											
140.	Connect o-scope to A2A3 R11. Read o-scope.	PW: 600 + 100 ns  Amptd: +1.14 - 0.25 Vd	<p>a. If not, replace A1A6 (para 5-31).</p> <p>b. If replacing A1A6 does not correct fault, send IFP to higher level maintenance.</p> <p>c. If correct, go to step 141.</p>										
141.	Set USB/LSB switch to LSB.												
142.	Connect o-scope to A2A3 R10.												
143. (para	Read o-scope.	PW:  600 ± 100 ns  Amptd: 14 + 0.25 Vdc	<p>a. If not, replace A1A7 5-31).</p> <p>b. If replacing A1A7 does not correct fault, send IFP to higher level maintenance.</p> <p>c. If correct, replace A2A3 (para 5-32).</p> <p>d. If replacing A2A3 does not correct fault, send IFP to higher level maintenance.</p>										
144.	On ESTS, set: <table border="0" style="width: 100%;"> <tr> <td style="width: 60%;"><u>Switch</u></td> <td style="width: 40%;"><u>Set to</u></td> </tr> <tr> <td>USB/LSB</td> <td>USB</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	USB/LSB	USB	AT1	30	MOD/PW	CW	BIT TEST	OFF		
<u>Switch</u>	<u>Set to</u>												
USB/LSB	USB												
AT1	30												
MOD/PW	CW												
BIT TEST	OFF												
145.	Connect o-scope CH 1 to A2A2 TP3. Read o-scope.	200 ± 50 ns (TTL) pulse	<p>a. If correct, replace A2A1 (para 5-32).</p> <p>b. If fault persists, send IFP to higher level maintenance.</p>										
146.	While observing ST TRIG LED, repeatedly toggle USB/LSB switch between USB and LSB.	ST TRIG LED lit	<p>a. If not for both USB and LSB, go to step 147.</p> <p>b. If only USB incorrect, go to step 156.</p> <p>c. If only LSB incorrect, go to step 160.</p>										

5-7. TEST PROCEDURES AND FAULT ISOLATION -Continued

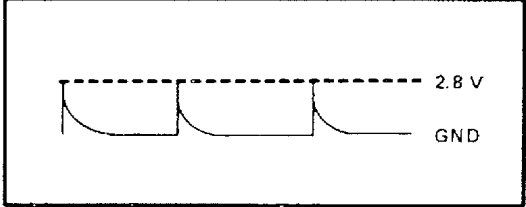
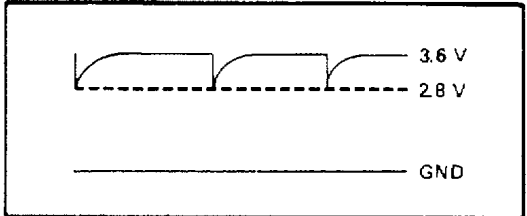
STEP	PROCEDURE INDICATIONS	ACTION	
147.	Connect o-scope CH 1 to A2A2 TP2. Read o-scope.	TTL low	If not, go to step 152.
148.	Connect o-scope CH 1 to A2A2 TP9. Read o-scope.	TTL negative pulse 70 us wide with 1.0 ms period.	If not, go to step 154.
149.	Connect o-scope CH 1 to A2A2 TP10. Read o-scope.	TTL low	If not, go to step 154.
150.	Connect o-scope CH 1 to A2A2 TP12. Read o-scope.	TTL low	If not, go to step 155.
151.	Connect o-scope CH 1 to A2A2 TP13. Read o-scope.	TTL low	<p>a. If not, go to step 155.</p> <p>b. If correct, replace A2A2 (para 5-32).</p> <p>c. If fault persists, send IFP to higher level maintenance.</p>
152.	Connect o-scope CH 1 to A2A8 TP1. Read o-scope.		If not, go to step 43.
153.	Connect o-scope CH 1 to A2A8 TP2. Read o-scope.		<p>a. If not, go to step 55.</p> <p>b. If correct, replace A2A2 (para 5-32).</p> <p>c. If fault persists, send IFP to higher level maintenance.</p>

5-7. TEST PROCEDURES AND FAULT ISOLATION -Continued

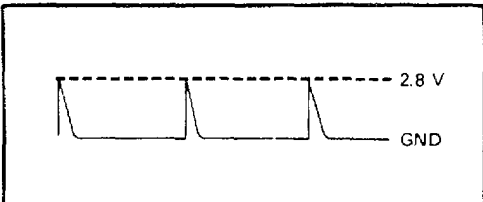
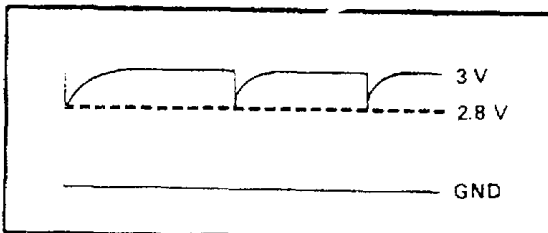
STEP	PROCEDURE INDICATIONS	ACTION	
154.	Connect o-scope CH 1 to A2A11 TP2. Read o-scope.		 <p>a. If not, go to step 32.</p> <p>b. If correct, replace A2A2 (para 5-32).</p> <p>c. If fault persists, send I FP to higher level maintenance.</p>
155.	Connect o-scope CH 1 to A2A11 TP1. Read o-scope.		 <p>a. If not, go to step 92.</p> <p>b. If correct, replace A2A2 (para 5-32).</p> <p>c. If fault persists, send IFP to higher level maintenance.</p>
156.	Connect o-scope CH 1 to A2A2 TP10. Read o-scope.	TTL low	If not, go to step 158.
157.	Connect o-scope CH 1 to A2A2 TP13. Read o-scope.	TTL low	<p>a. If not, go to step 159.</p> <p>b. If correct, replace A2A2 (para 5-32).</p> <p>c. If fault persists, send IFP to higher level maintenance.</p>



5-7. TEST PROCEDURES AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
158.	Connect o-scope CH 1 to A2A9 TP2. Read o-scope.		<p>a. If not, go to step 250.</p> <p>b. If correct, replace A2A2 (para 5-32).</p> <p>c. If fault persists, send IFP to higher level maintenance.</p>
159.	Connect o-scope CH 1 to A2A10 TP2. Read o-scope.		<p>a. If not, go to step 163.</p> <p>b. If correct, replace A2A2 (para 5-32).</p> <p>c. If fault persists, send IFP to higher level maintenance.</p>
160.	Connect o-scope CH 1 to A2A2 TP10. Read o-scope.	TTL low	If not, go to step 162.
161.	Connect o-scope CH 1 to A2A2 TP13. Read o-scope.	TTL low	<p>a. If not, go to step 163.</p> <p>b. If correct, replace A2A2 (para 5-32).</p> <p>c. If fault persists, send IFP to higher level maintenance.</p>

5-7. TEST PROCEDURES AND FAULT ISOLATION-Continued

STEP	PROCEDURE INDICATIONS	ACTION	
162.	Connect o-scope CH 1 to A2A9 TP3. Read o-scope.		 <p> <u>a.</u> If not, go to step 250.  <u>b.</u> If correct, replace A2A2 (para 5-32).  <u>c.</u> If fault persists, send IFP to higher level maintenance.                 </p>
163.	Connect o-scope CH 1 to A2A10 TPI. Read o-scope.		 <p> <u>a.</u> If not, go to step 103.  <u>b.</u> If correct, replace A2A2 (para 5-32).  <u>c.</u> If fault persists, send IFP to higher level maintenance.                 </p>
164.	Set MOD/PW switch to CW.	CW LED lit	<p> <u>a.</u> If not, replace A2A1 (para 5-32).  <u>b.</u> If replacing A2A1 does not correct fault, replace A2A3 (para 5-32).  <u>c.</u> If fault persists, send IFP to higher level maintenance.                 </p>



5-7. TEST PROCEDURES AND FAULT ISOLATION -Continued

STEP	PROCEDURE INDICATIONS	ACTION	
173.	Set USB/LSB to LSB.		
174.	Connect o-scope to A2A9 R61.		
175.	Read o-scope.	Amptd: $+1.14 \pm 0.25$ Vdc5-24).	<p>a. If not, replace A1A7 (para 5-32).</p> <p>b. If fault persists, send IFP to higher level maintenance.</p> <p>c. If correct, replace A2A9 (para 5-32).</p> <p>d. If fault persists, send IFP to higher level maintenance.</p>
<b>B. PHASE TRACKING FAULT</b>			
176.	Remove A1A13 (para 5-26).		
177.	Connect VVM:		
	Probe	Connector	
	A	J82	
	B	J83	
178.	Using 50-ohm terminations, terminate J84, J81, and J79.		
179.	Read VVM" phase and amplitude for following PHASE-DEG switch settings:		a. If any incorrect, replace A1A1, A1A2, A1A4, and A1A5 (para 5-31).
	Setting	<u>VVM</u>	b. If all correct, replace A2A7 (para 5-32).
	0	$-90 \pm 12.0$ degrees	c. If replacing A2A7 does
not	0	CH A $+7.0 \pm 2.0$ dBm	correct fault, replace A1A13 (para 5-33).
	0	CH" B $\pm 7.0 \pm 2.0$ dBm	d. If fault persists, send IFP to higher level maintenance.
	-90	$0.0 \pm 12.0$ degrees	
	-90	CH A $+7.0 \pm 2.0$ dBm	
	-90	CH B $+7.0 \pm 2.0$ dBm	

5-7. TEST PROCEDURES AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
180.	Remove A1A13 (para 5-26).		
181.	Connect VVM: <u>Probe</u> <u>Connector</u>  A                              J81 B                              J80		
182.	Using 50-ohm terminations, terminate J79, J82, and J84.		
183.	Read VVM" phase and amplitude for following PHASE-DEG switch settings:  <u>Setting</u>  0  0  0  -90  -90  -90	<u>VVM</u>  -90 ± 12.0 degrees  CH A +7.0 + 2.0 dBm  CH" B +7.0 + 2.0 dBm  0.0 + 12.0 degrees  CH A +7.0 + 2.0 dBm  CH B +7.0 + 2.0 dBm	a. If any incorrect, replace A1A1, A1A2, A1A4, and A1A5 (para 5-31).  b. If all correct, replace A2A7 (para 5-32).  c. If replacing A2A7 does not correct fault, replace A1A13 (para 5-33).  d. If fault persists, send IFP to higher level maintenance.
184.	Remove A1A12 and A1A13 (para 5-26).		
185.	Connect VVM <u>Probe</u> <u>Connector</u>  A                              J70 B                              J71		
186.	Using 50-ohm termination, terminate J72 and J80.		

5-7. TEST PROCEDURES AND FAULT ISOLATION -Continued

STEP	PROCEDURE INDICATIONS	ACTION																			
187.	<p>Read VVM" phase and amplitude for following PHASE--DEG switch settings:</p> <table border="0"> <tr> <td style="text-align: center;"><u>Setting</u></td> <td style="text-align: center;"><u>VVM</u></td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">-90 ± 2.0 degrees</td> </tr> <tr> <td style="text-align: center;">not</td> <td></td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">CH A + 7.0 ± 2.0 dBm</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">CH" B +7.0 ± 2.0 dBm</td> </tr> <tr> <td style="text-align: center;">IFP</td> <td></td> </tr> <tr> <td style="text-align: center;">-90</td> <td style="text-align: center;">0.0 ± 12.0 degrees</td> </tr> <tr> <td style="text-align: center;">-90</td> <td style="text-align: center;">CH A +7.0 ± 2.0 dBm</td> </tr> <tr> <td style="text-align: center;">-90</td> <td style="text-align: center;">CH B +7.0 ± 2.0 dBm</td> </tr> </table>	<u>Setting</u>	<u>VVM</u>	0	-90 ± 2.0 degrees	not		0	CH A + 7.0 ± 2.0 dBm	0	CH" B +7.0 ± 2.0 dBm	IFP		-90	0.0 ± 12.0 degrees	-90	CH A +7.0 ± 2.0 dBm	-90	CH B +7.0 ± 2.0 dBm		<p>a. If any incorrect, replace A1A1, A1A2, A A4, and A1A5 (para 5-31).</p> <p>b. If all correct, replace A2A7 (para 5-32).</p> <p>c. If replacing A2A7 does correct fault, replace A1A13 (para 5-33).</p> <p>d. If fault persists, send to higher level maintenance.</p>
<u>Setting</u>	<u>VVM</u>																				
0	-90 ± 2.0 degrees																				
not																					
0	CH A + 7.0 ± 2.0 dBm																				
0	CH" B +7.0 ± 2.0 dBm																				
IFP																					
-90	0.0 ± 12.0 degrees																				
-90	CH A +7.0 ± 2.0 dBm																				
-90	CH B +7.0 ± 2.0 dBm																				
188.	Remove A1A13 (para 5-26).																				
189.	<p>Connect VVM:</p> <table border="0"> <tr> <td style="text-align: center;"><u>Probe</u></td> <td style="text-align: center;"><u>Connector</u></td> </tr> <tr> <td style="text-align: center;">A</td> <td style="text-align: center;">J84</td> </tr> <tr> <td style="text-align: center;">B</td> <td style="text-align: center;">J83</td> </tr> </table>	<u>Probe</u>	<u>Connector</u>	A	J84	B	J83														
<u>Probe</u>	<u>Connector</u>																				
A	J84																				
B	J83																				
190.	Using 50-ohm terminators, terminate J79, J81, and J82.																				
191	<p>Read VVM" phase and amplitude for following PHASE--DEG switch settings:</p> <table border="0"> <tr> <td style="text-align: center;"><u>Setting</u></td> <td style="text-align: center;"><u>VVM</u></td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">-90 ± 12.0 degrees</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">CH A + 7.0 ± 2.0 dBm</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">CH" B + 7.0 ± 2.0 dBm</td> </tr> <tr> <td style="text-align: center;">-90</td> <td style="text-align: center;">0.0 ± 12.0 degrees</td> </tr> <tr> <td style="text-align: center;">-90</td> <td style="text-align: center;">CH A +7.0 ± 2.0 dBm</td> </tr> <tr> <td style="text-align: center;">-90</td> <td style="text-align: center;">CH B +7.0 ± 2.0 dBm</td> </tr> </table>	<u>Setting</u>	<u>VVM</u>	0	-90 ± 12.0 degrees	0	CH A + 7.0 ± 2.0 dBm	0	CH" B + 7.0 ± 2.0 dBm	-90	0.0 ± 12.0 degrees	-90	CH A +7.0 ± 2.0 dBm	-90	CH B +7.0 ± 2.0 dBm		<p>a. If any incorrect, replace A1A1, A1A2, A1A4, and A1A5 (para 5-31).</p> <p>b. If all correct, replace A2A7 (para 5-32).</p> <p>c. If replacing A2A7 does not correct fault, replace A1A13 (para 5-33).</p> <p>d. If fault persists, send IFP to higher level maintenance.</p>				
<u>Setting</u>	<u>VVM</u>																				
0	-90 ± 12.0 degrees																				
0	CH A + 7.0 ± 2.0 dBm																				
0	CH" B + 7.0 ± 2.0 dBm																				
-90	0.0 ± 12.0 degrees																				
-90	CH A +7.0 ± 2.0 dBm																				
-90	CH B +7.0 ± 2.0 dBm																				

5-7. TEST PROCEDURES AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
192.	Remove A1A13 (para 5-26).		
193.	Connect VVM: <u>Probe</u> <u>Connector</u>  A                              J79 B                              J80		
194.	Using 50-ohm terminations, terminate J81, J82, and J84.		
195.	Read VVM" phase and amplitude for following PHASE -DEG switch settings:  <u>Setting</u> 0 0 0 -90 -90 -90	<u>VVM</u>  -90 ± 12.0 degrees  CH A +7.0 ± 2.0 dBm  CH" B +7.0 ± 2.0 dBm  0.0 ± 12.0 degrees  CH A +7.0 ± 2.0 dBm  CH B +7.0 ± 2.0 dBm	a. If any incorrect, replace A1A1, A1A2, A1A4, and A1A5 (para 5-31).  b. If all correct, replace A2A7 (para 5-32).  c. If replacing A2A7 does not correct fault, replace A1A13 (para 5-33).  d. If fault persists, send IFP to higher level maintenance.
196.	Remove A1A12 and A1A13 (para 5-26).		
197.	Connect VVM: <u>Probe</u> <u>Connector</u>  A                              J71 B                              J72		
198.	Using 50-ohm terminations, terminate J70 and J80.		
		5-43	

5-7. TEST PROCEDURES AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION															
199.	<p>Read VVM" phase and amplitude for following PHASE-DEG switch settings:</p> <table border="0"> <tr> <td style="text-align: center;">Setting</td> <td style="text-align: center;"><u>VVM</u></td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">-90 - 12.0 degrees</td> </tr> <tr> <td style="text-align: center;">not A1A13</td> <td style="text-align: center;">CH A +7.0 - 2.0 dBm</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">CH" B +7.0 1 2.0 dBm</td> </tr> <tr> <td style="text-align: center;">-90 maintenance.</td> <td style="text-align: center;">0.0 + 12.0 degrees</td> </tr> <tr> <td style="text-align: center;">-90</td> <td style="text-align: center;">CH A +7.0 + 2.0 dBm</td> </tr> <tr> <td style="text-align: center;">-90</td> <td style="text-align: center;">CH B +7.0 + 2.0 dBm</td> </tr> </table>	Setting	<u>VVM</u>	0	-90 - 12.0 degrees	not A1A13	CH A +7.0 - 2.0 dBm	0	CH" B +7.0 1 2.0 dBm	-90 maintenance.	0.0 + 12.0 degrees	-90	CH A +7.0 + 2.0 dBm	-90	CH B +7.0 + 2.0 dBm		<p>a. If any incorrect, replace A1A1, A1A2, A1A4, and A1A5 (para 5-31).</p> <p>b. If all correct, replace A2A7 (para 5-32).</p> <p>c. If replacing A2A7 does correct fault, replace (para 5-33).</p> <p>d. If fault persists, send IFP to higher level</p>
Setting	<u>VVM</u>																
0	-90 - 12.0 degrees																
not A1A13	CH A +7.0 - 2.0 dBm																
0	CH" B +7.0 1 2.0 dBm																
-90 maintenance.	0.0 + 12.0 degrees																
-90	CH A +7.0 + 2.0 dBm																
-90	CH B +7.0 + 2.0 dBm																
200.	Remove 50-ohm terminations and VVM probes.																
201.	Install A2A12 and A1A13 (para 5-26).																
<b>C. LOG AMPLITUDE VS. DYNAMIC RANGE FAULT</b>																	
202.	Remove A2A11 (para 5-32).																
203.	Place A2A11 on extender.																
204.	Install extender in IFP A2A11 slot.																
205.	Connect o-scope CH 1 to R49.																
206.	Set MOD/PW switch to CW.																



5-7. TEST PROCEDURES AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION																			
207.	Read o-scope for following AT1 dial settings:(para 5-32).		a.If correct, replace A2A11																		
	<table border="0"> <tr> <td style="text-align: center;">Setting</td> <td></td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Scope display (Vdc)</td> </tr> <tr> <td style="text-align: center;">10</td> <td style="text-align: center;">1.98 + 0.10</td> </tr> <tr> <td style="text-align: center;">20</td> <td style="text-align: center;">1.70 ± 0.10</td> </tr> <tr> <td style="text-align: center;">30</td> <td style="text-align: center;">1.42 ± 0.10</td> </tr> <tr> <td style="text-align: center;">40</td> <td style="text-align: center;">1.14 ± 0.10</td> </tr> <tr> <td style="text-align: center;">50</td> <td style="text-align: center;">0.86 ± 0.10</td> </tr> <tr> <td style="text-align: center;">60</td> <td style="text-align: center;">0.58 ± 0.10</td> </tr> <tr> <td style="text-align: center;">60</td> <td style="text-align: center;">0.30 ± 0.10</td> </tr> </table>	Setting		0	Scope display (Vdc)	10	1.98 + 0.10	20	1.70 ± 0.10	30	1.42 ± 0.10	40	1.14 ± 0.10	50	0.86 ± 0.10	60	0.58 ± 0.10	60	0.30 ± 0.10		b.If not, replace A1A9 (para 5-31). c. If replacing A1A9 does not correct fault, replace A1A1, A1A2, A1A4 and A1A5 (para 5-31). d.If fault persists, send IFP to higher level maintenance.
Setting																					
0	Scope display (Vdc)																				
10	1.98 + 0.10																				
20	1.70 ± 0.10																				
30	1.42 ± 0.10																				
40	1.14 ± 0.10																				
50	0.86 ± 0.10																				
60	0.58 ± 0.10																				
60	0.30 ± 0.10																				
208.	Disconnect o-scope.																				
209.	Remove A1A11 and extender from IFP.																				
210.	Install A2A11 (para 5-32).																				
<b>D. FRUQ dBm FAULT</b>																					
211.	Remove A1A12 and A1A13 (para 5-33).																				
212.	Connect VVM: <table border="0"> <tr> <td style="text-align: center;"><u>Probe</u></td> <td style="text-align: center;"><u>Connector</u></td> </tr> <tr> <td style="text-align: center;">A</td> <td style="text-align: center;">J68</td> </tr> <tr> <td style="text-align: center;">B</td> <td style="text-align: center;">J67</td> </tr> </table>	<u>Probe</u>	<u>Connector</u>	A	J68	B	J67														
<u>Probe</u>	<u>Connector</u>																				
A	J68																				
B	J67																				
213.	Using 50-ohm termination, terminate J69.																				
214.	Set MOD/PW switch to CW.																				
5-45																					

5-7. TEST PROCEDURES AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION															
215.  not	<p>Read VVM phase and amplitude for following IF FREQ MHz switch positions:</p> <table border="0" style="width: 100%;"> <tr> <td style="text-align: center;"><u>Setting</u></td> <td style="text-align: center;"><u>VVM</u></td> </tr> <tr> <td style="text-align: center;">140.0</td> <td style="text-align: center;">-90.0 ± 12.0 degrees</td> </tr> <tr> <td style="text-align: center;">140.0</td> <td style="text-align: center;">CH A +4.0 ± 3.0 dBm</td> </tr> <tr> <td style="text-align: center;">140.0</td> <td style="text-align: center;">CH B +4.0 ± 3.0 dBm</td> </tr> <tr> <td style="text-align: center;">150.0</td> <td style="text-align: center;">0.0 ± 12.0 degrees</td> </tr> <tr> <td style="text-align: center;">150.0</td> <td style="text-align: center;">CH A +4.0 ± 3.0 dBm</td> </tr> <tr> <td style="text-align: center;">maintenance. 150.0</td> <td style="text-align: center;">CH B +4.0 ± 3.0 dBm</td> </tr> </table>	<u>Setting</u>	<u>VVM</u>	140.0	-90.0 ± 12.0 degrees	140.0	CH A +4.0 ± 3.0 dBm	140.0	CH B +4.0 ± 3.0 dBm	150.0	0.0 ± 12.0 degrees	150.0	CH A +4.0 ± 3.0 dBm	maintenance. 150.0	CH B +4.0 ± 3.0 dBm		<p>a. If correct, replace A2A8 (para 5-32).</p> <p>b. If replacing A2A8 does not correct fault, replace A1A12 (para 5-33).</p> <p>c. If any incorrect, replace A1A11 (para 5-31).</p> <p>d. If replacing A1A11 does not correct fault, replace A1A10.</p> <p>e. If fault persists, send IFP to higher level</p>
<u>Setting</u>	<u>VVM</u>																
140.0	-90.0 ± 12.0 degrees																
140.0	CH A +4.0 ± 3.0 dBm																
140.0	CH B +4.0 ± 3.0 dBm																
150.0	0.0 ± 12.0 degrees																
150.0	CH A +4.0 ± 3.0 dBm																
maintenance. 150.0	CH B +4.0 ± 3.0 dBm																
<b>E. FRUI -30 dBm FAULT</b>																	
216.	Remove A1A12 and A1A13 (para 5-33).																
217.	<p>Connect VVM:</p> <table border="0" style="width: 100%;"> <tr> <td style="text-align: center;"><u>Probe</u></td> <td style="text-align: center;"><u>Connector</u></td> </tr> <tr> <td style="text-align: center;">A</td> <td style="text-align: center;">J68</td> </tr> <tr> <td style="text-align: center;">B</td> <td style="text-align: center;">J69</td> </tr> </table>	<u>Probe</u>	<u>Connector</u>	A	J68	B	J69										
<u>Probe</u>	<u>Connector</u>																
A	J68																
B	J69																
218.	Using 50-ohm termination terminate J67.	<b>5-46</b>															

5-7. TEST PROCEDURES AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION															
219.	<p>Read VVM phase and amplitude for following IF FREQ MHz switch positions:</p> <table border="0"> <tr> <td style="text-align: center;"><u>Setting</u></td> <td style="text-align: center;"><u>VVM</u></td> </tr> <tr> <td style="text-align: center;">150.0</td> <td style="text-align: center;">-90.0 ± 12.0 degrees</td> </tr> <tr> <td style="text-align: center;">150.0</td> <td style="text-align: center;">CHA +4.0 ± 3.0 dBm</td> </tr> <tr> <td style="text-align: center;">150.0</td> <td style="text-align: center;">CH B +4.0 ± 3.0 dBm</td> </tr> <tr> <td style="text-align: center;">160.0</td> <td style="text-align: center;">0.0 ± 12.0 degrees</td> </tr> <tr> <td style="text-align: center;">160.0</td> <td style="text-align: center;">CH A +4.0 ± 3.0 dBm</td> </tr> <tr> <td style="text-align: center;">160.0</td> <td style="text-align: center;">CH B +4.0 ± 3.0 dBm</td> </tr> </table>	<u>Setting</u>	<u>VVM</u>	150.0	-90.0 ± 12.0 degrees	150.0	CHA +4.0 ± 3.0 dBm	150.0	CH B +4.0 ± 3.0 dBm	160.0	0.0 ± 12.0 degrees	160.0	CH A +4.0 ± 3.0 dBm	160.0	CH B +4.0 ± 3.0 dBm		<p>a. If correct, replace A2A8 (para 5-32).</p> <p>b. If replacing A2A8 does not correct fault, replace A1 A12 (para 5-33).</p> <p>c. If any incorrect, replace A1A11 (para5-31).</p> <p>d. If replacing A1A11 does not correct fault, replace A1 A10 (para 5-31).</p> <p>e. If fault persists, send IFP to higher level maintenance.</p>
<u>Setting</u>	<u>VVM</u>																
150.0	-90.0 ± 12.0 degrees																
150.0	CHA +4.0 ± 3.0 dBm																
150.0	CH B +4.0 ± 3.0 dBm																
160.0	0.0 ± 12.0 degrees																
160.0	CH A +4.0 ± 3.0 dBm																
160.0	CH B +4.0 ± 3.0 dBm																
220.	Remove A1A8 (para 5-31).																
221.	Connect VVM probe A to J43.																
222.	Read VVM CH A.	+4.0 ± 3.0 dBm	a. If not, go to step 223.														
			b. If correct, go to step 229.														
223.	Remove A1A11 (para 5-31).																
224.	Connect VVM probe A to J64.																
225.	Read VVM CH A	+7.0 ± 2.0 dBm	a. If not, go to step 226.														
			b. If correct, replace A1A11 (para 5-31).														
			c. If fault persists, send IFP to higher level maintenance.														
226.	Remove A1A9 (para 5-31)																
227.	Connect VVM probe A to J51.																
228.	Read VVM CH A.	-25.0 ± 5.0 dBm	a. If not, replace A1A1, A1A2, A1A4, and A1A5 (para 5-31).														
			b. If correct, replace A1A9 (para 5-31).														
			c. If fault persists, send IFP to higher level maintenance.														

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
229.	Install A1A8 (para 5-31).		
230.	Place A2A11 on extender.		
231.	Install extender in IFP A2A11 slot.		
232.	Connect o-scope CH1 to A2A11 R41.		
233.	Set IF FREQ MHz switch to following settings. At each setting read o-scope		a. If both readings are incorrect, replace A1 A8 (para 5-31).
	<u>IF FREQ MHz</u>	<u>Display (mVdc)</u>	b. If replacing A1A8 does not correct fault, replace A1A10 (para 5-31).
	140.0	-400 ± 200	c. If both readings are correct, replace A2A11 (para 5-32).
	160.0	+400 ± 200	d. If replacing A2A11 does not correct fault, replace A2A2 (para 5-32).
IFP			e. If fault persists, send
maintenance			to higher level

**G. FRU DIFFERENCE DF @ 150.0 MHz 30 dBm FAULT**

234.	Remove A1 A8 (para 5-31).		
235.	Set USB/LSB switch to USB.		
236.	Connect VVM probe A to J47.		
237.	Read VVM CH A.	+7.0 ± 2.0 dBm	If not, replace A1A6 (para 5-31).
238.	Connect VVM probe A to J36.		
239.	Set USB/LSB switch to LSB. Read VVM CH A. para 5-31).	+7.0 ± 2.0 dBm	If not, replace A1A7 (para
240.	Install A1A8 (para 5-31).		
241.	Remove A2A10 (para 5-32).		
242.	Install A2A10 on extender.		
243.	Install extender in IFP A2A10 slot.		

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
244.	Connect o-scope CH 1 to A2A10 R37.		
245.	Set USB/LSB switch to USB.		
246.	Set IF FREQ MHz switch to following settings. At each setting read o-scope.		<u>a.</u> If correct, replace A2A10 (para 5-32).
	<u>IF FREQ MHz</u>	<u>Display (mVdc)</u>	<u>b.</u> If replacing A1A8 does not correct fault, replace
	140.0 160.0	-400 + 200A1A2 (para 5-31). +400 + 200	<u>c.</u> If both readings are correct, replace A2A8 (para 5-32). <u>d.</u> If replacing A2A8 does not correct fault, replace A2A10 (para 5-32). <u>e.</u> If fault persists, send IFP to higher level maintenance.
247.	Set USB/LSB switch to LSB.		
248.	Connect o-scope CH 1 to A2A10 R24.		
249.	Repeat step 246.	As specified	As specified.
<b>H. TRIGGER AMPLITUDE FAILURE</b>			
250.	Remove A2A9 (para 5-32).		
251.	Place A2A9 on extender.		
252.	Install extender if IFP A2A9 slot.		
253.	Connect o-scope CH 1 to test point for sideband failure: <u>Test point</u> <u>Failure</u>		
	R54                                      USB R61                                      LSB		

5-7. TEST PROCEDURE AND FAULT ISOLATION - Continued

STEP	PROCEDURE INDICATIONS	ACTION																																					
254.	Set MOD/PW switch to CW.																																						
255.	Read o-scope for following AT1 dial settings:(para 5-32).  <table border="0" style="margin-left: 40px;"> <tr> <td style="text-align: right;">Setting</td> <td></td> </tr> <tr> <td style="text-align: right;">0</td> <td></td> </tr> <tr> <td style="text-align: right;">10</td> <td></td> </tr> <tr> <td style="text-align: right;">20</td> <td></td> </tr> <tr> <td style="text-align: right;">30</td> <td></td> </tr> <tr> <td style="text-align: right;">40</td> <td></td> </tr> <tr> <td style="text-align: right;">50</td> <td></td> </tr> <tr> <td style="text-align: right;">60</td> <td></td> </tr> </table>	Setting		0		10		20		30		40		50		60		Scope display (Vdc)  <table border="0" style="margin-left: 40px;"> <tr> <td></td> <td style="text-align: center;"><math>1.98 \pm 0.20</math></td> </tr> <tr> <td></td> <td style="text-align: center;"><math>1.70 \pm 0.20</math></td> </tr> <tr> <td></td> <td style="text-align: center;"><math>1.42 \pm 0.20</math></td> </tr> <tr> <td></td> <td style="text-align: center;"><math>1.14 \pm 0.20</math></td> </tr> <tr> <td></td> <td style="text-align: center;"><math>0.86 \pm 0.20</math></td> </tr> <tr> <td></td> <td style="text-align: center;"><math>0.58 \pm 0.20</math></td> </tr> <tr> <td></td> <td style="text-align: center;"><math>0.30 \pm 0.20</math></td> </tr> </table>		$1.98 \pm 0.20$		$1.70 \pm 0.20$		$1.42 \pm 0.20$		$1.14 \pm 0.20$		$0.86 \pm 0.20$		$0.58 \pm 0.20$		$0.30 \pm 0.20$	a. If correct, replace A2A9  b. If not, replace module for sideband failure:  <table border="0" style="margin-left: 40px;"> <tr> <td style="text-align: right;"><u>Failure</u></td> <td style="text-align: left;"><u>Module</u></td> </tr> <tr> <td style="text-align: right;">USB</td> <td style="text-align: left;">A1A6</td> </tr> <tr> <td style="text-align: right;">LSB</td> <td style="text-align: left;">A1A7</td> </tr> </table> (para 5-31).  c. If fault persists, send IFP to higher level maintenance.	<u>Failure</u>	<u>Module</u>	USB	A1A6	LSB	A1A7
Setting																																							
0																																							
10																																							
20																																							
30																																							
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<u>Failure</u>	<u>Module</u>																																						
USB	A1A6																																						
LSB	A1A7																																						
256.	Disconnect o-scope.																																						
257.	Remove A2A9 and extender from IFP.																																						
258.	Install A2A9 (para 5-32).																																						

**5-8. ALINEMENT SETUP |**a. Initial Conditions

- (1) Remove side covers (para 5-30).
- (2) Repeat test setup (para 5-5) and test equipment calibration (para 5-6).

**NOTES**

Reinstall any removed modules or circuit cards before attempting an alinement.

Adjustments are to be made only on assembly called out in the specific procedure.

Adjustments made when a card is extended may require fine tuning when the card is reinstalled in the IFP.

Ensure assemblies are securely mounted.

IFP warm-up requirements are as follows:

Cold start 15 minutes

Warm start 2-5 minutes

Replace assembly and retest as soon as LRU fails to meet required standard.

TTL and ECL logic levels stated in these procedures are defined as follows:

Vdc

TTL low = 0.0 to 1.0

high = +2.4 to +5.5

ECL low = -2/0 to -0.98

high = 0.0 to - 0.5

Refer to FO-2 for adjustment location

Refer to FO-3 for test point location.

Refer to FO-4 for block diagram.

**5-8. ALINEMENT SETUP -Continued**

b. Perform alinement indicated In sequence for replaced item:

**NOTE**

Fault isolation may call for performance of an alinement as a corrective action. Alinements performed as part of a fault isolation must be repeated In addition to the specific alinements required for items replaced below.

Item replaced	Alinement required (para reference)
A1A1, A1A2, A1A4, and A1A5	5-18, 5-19, 5-20
A1A6	5-10, 5-12, 5-13, 5-11, 5-16
A1A7	5-10, 5-12, 5-13, 5-11, 5-16
A1A8	5-22, 5-15, 5-27
A1A9	5-10, 5-12, 5-13, 5-23
A1A11	5-22, 5-15
A1A12	5-19, 5-20
A1A13	5-19, 5-20
A2A2	5-10, 5-22, 5-27
A2A3	5-10, 5-12, 5-13, 5-15, 5-16, 5-22, 5-27
A2A5	5-20
A2A6	5-20
A2A7	5-20
A2A8	5-21
A2A9	5-16
A2A10	5-22, 5-27
A2A11	5-15, 5-16
A1A10	5-19, 5-20, 5-22, 5-27, 5-15



**5-9. CONFIRM LOGIC VOLTAGE REFERENCE A2A2**

STEP	PROCEDURE INDICATIONS	ACTION	
1.	Connect DVM to A2A2TP14 (+) and A2A2TP1 (GND).	$+12 \pm 0.05$ Vdc	Replace A2A2 (para 5-32).

5-10. LOG AMPLITUDE ALINEMENT - CW A1A6, A1A7, A1A9

STEP	PROCEDURE INDICATIONS	ACTION																																												
<b>NOTE</b>																																														
If alinement cannot be successfully completed, replace A1A6, A1A7, or A1A9, as required (para 5-31). Repeat alinement procedure (para 5-8). If fault persists, send IFP to higher level maintenance.																																														
<b>A1A9</b>																																														
1.	Connect test equipment (fig 5-1).																																													
2.	On ESTS, set: <table style="margin-left: 20px; border: none;"> <tr> <td style="padding-right: 20px;"><u>Switch</u></td> <td><u>Set to</u></td> </tr> <tr> <td>POWER</td> <td>OFF</td> </tr> <tr> <td>IF FREQ MHz</td> <td>150.0</td> </tr> <tr> <td>USB/LSB</td> <td>USB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>60</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>PW SET</td> <td>Full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/PW</td> </tr> <tr> <td></td> <td>RST</td> </tr> <tr> <td>EXTTHRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>Full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PHASE DEG</td> <td>0</td> </tr> <tr> <td>PRF</td> <td>10 KHz</td> </tr> <tr> <td>DATA SELECT</td> <td>B-CQ</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	POWER	OFF	IF FREQ MHz	150.0	USB/LSB	USB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	60	AT2	cf	MOD/PW	CW	PW SET	Full cw	TRIG SEL	ST TRIG/PW		RST	EXTTHRESH	OFF	EXT THRESH		ADJ	Full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PHASE DEG	0	PRF	10 KHz	DATA SELECT	B-CQ	
<u>Switch</u>	<u>Set to</u>																																													
POWER	OFF																																													
IF FREQ MHz	150.0																																													
USB/LSB	USB																																													
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PW SET	Full cw																																													
TRIG SEL	ST TRIG/PW																																													
	RST																																													
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EXT THRESH																																														
ADJ	Full cw																																													
SWEEP	OFF																																													
BAND CMD	LB																																													
BW CMD	30 MHz																																													
BIT TEST	OFF																																													
PHASE DEG	0																																													
PRF	10 KHz																																													
DATA SELECT	B-CQ																																													
3.	Ensure power is off on power supply.																																													
4.	Remove A2A3 (para 5-32).																																													
5.	Connect ac voltmeter and DVM to IFP connector A2XA3-A (DF) as shown in figure 5-5.																																													
6.	Set DVM to measure dc volts, 2 Vdc range.																																													
<b>5-54</b>																																														

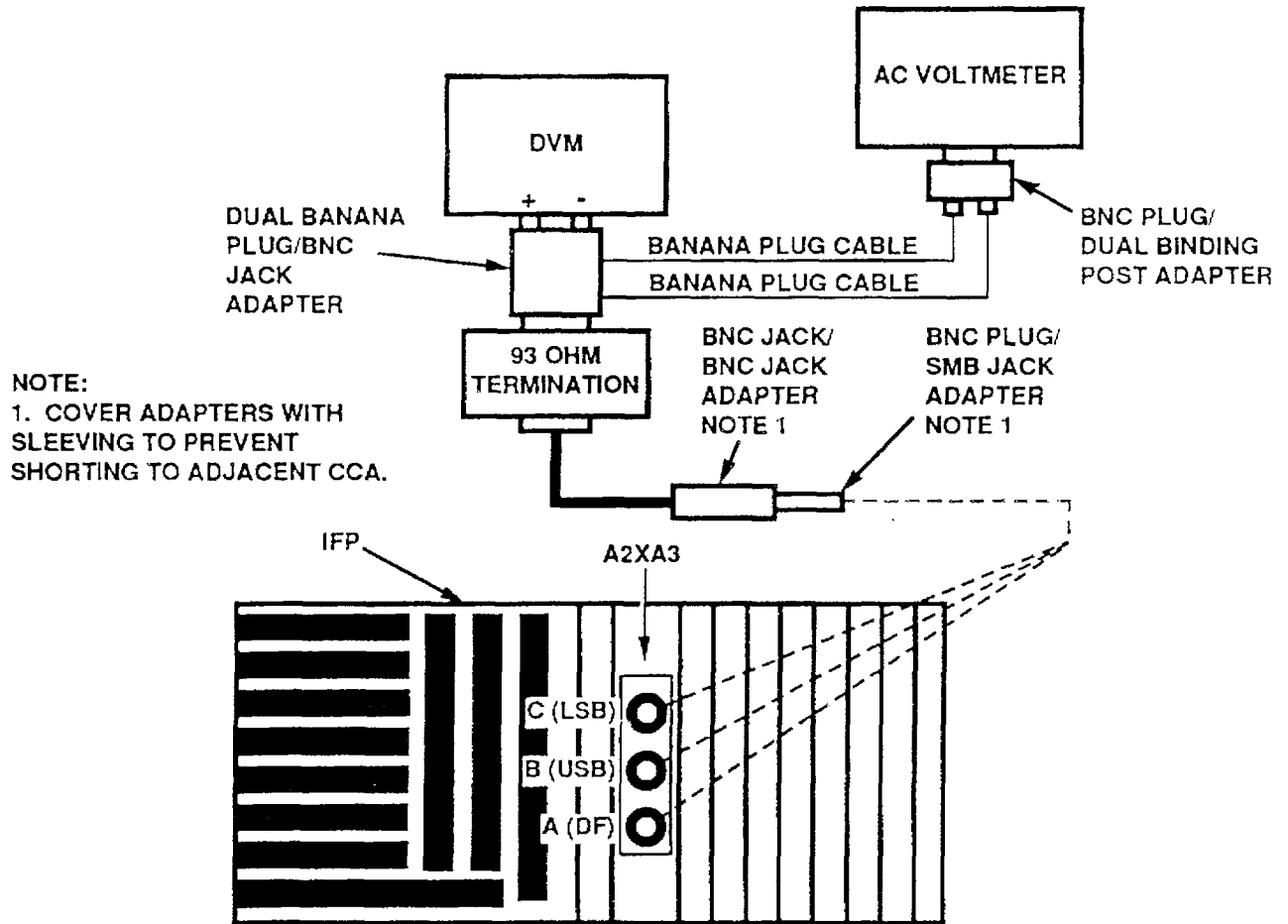


FIGURE 5-5. METER HOOKUP

**NOTE**

Ensure equipment warms up at least 30 minutes before making adjustments.

5-10. LOG AMPLITUDE ALINEMENT - CW A1A6, A1A7, A1A9- Continued

STEP	PROCEDURE INDICATIONS	ACTION	
8.	Turn on power supplies. Set ESTS POWER switch to ON.		
9.	Disconnect W6 from the IFP.		
10.	Adjust A1A9R48	Peak voltage on ac voltmeter	Adjust A1A9R21 to electrical mid range as indicated on DVM, and repeat this step.
11.	Connect W6 to IFP J6.	310 ± 5 mVdc on DVM	Adjust A1A9R36.
<p><b>NOTE</b> To prevent misalignment, the dc output must be more negative than -25 mVdc.</p>			
12.	Disconnect W6 from the IFP	-25 to -50 mVdc on DVM	Adjust A1A9R48: verify reading on ac voltmeter does not change more than +/- 10 mVac during adjustment.
13.	Connect W6 to IFP J6.		
14.	Set ESTS AT1 to 10.	1690 ± 5 mVdc on DVM	Adjust A1A9R21.
15.	A1A9R36, A1A9R48, and A1A9R21 interact. Set ESTS AT1 to 60 and repeat steps 11 through 14 until no adjustments are necessary.	As specified	
16.	Set ESTS AT1 to the following positions and verify voltages on DVM, ± 25 mVdc, except where noted:		
<p style="text-align: center;"><u>AT1</u></p> <p style="text-align: center;">60 50 40 30 20 10 0</p>		<p style="text-align: center;"><u>DVM</u></p> <p style="text-align: center;">310 ± 5 mVdc 586 862 1138 1414 1690 ± 5 mVdc 1966</p>	
<p><b>NOTE</b> To prevent misalignment, the dc output must be more negative than -25 mVdc.</p>			

5-10. LOG AMPLITUDE ALINEMENT-CW A1A6, A1A7, A1A9- Continued

STEP	PROCEDURE INDICATIONS	ACTION																	
17.	Disconnect W6 from the IFP.	-25 to -50 mVdc on DVM																	
18.	Record DVM reading.																		
<b>A1A6</b>																			
19.	Connect ac voltmeter and DVM to IFP connector A2XA3-B (USB) as shown fig. 5-5.																		
20.	Set ESTS AT1 to 60.																		
21.	Disconnect W8 from the IFP.																		
22.	Adjust A1A6R48.	Peak voltage on ac voltmeter	Adjust A1A6R21 to electrical mid range, as indicated on DVM, and repeat this step.																
23.	Connect W8 to IFP J9.	310 ± 5 mVdc on DVM	Adjust A1A6R36.																
<b>NOTE</b>																			
To prevent misalignment, the do output must be more negative than -25 mVdc.																			
24.	Disconnect W8 from the IFP.	-25 to -50 mVdc on DVM	Adjust A1A6R48; verify reading on ac voltmeter does 10 mVac during																
adjustment.	not change more than ±																		
25.	Connect W8 to IFP J9.																		
26.	Set ESTS AT1 to 10.	1690 ± 5 mVdc on DVM	Adjust A1A6R21.																
27.	A1A6R48, A1A6R36, and A1A6R21 interact. Set ESTS AT1 to 60 and repeat steps 23 through 26 until no adjustments are necessary.	As specified																	
28.	Set ESTS AT1 to the following positions and verify voltages on DVM + 25 mVdc except where noted.																		
<table border="0"> <tr> <td style="text-align: center;"><u>AT1</u></td> </tr> <tr> <td style="text-align: center;">60</td> </tr> <tr> <td style="text-align: center;">50</td> </tr> <tr> <td style="text-align: center;">40</td> </tr> <tr> <td style="text-align: center;">30</td> </tr> <tr> <td style="text-align: center;">20</td> </tr> <tr> <td style="text-align: center;">10</td> </tr> <tr> <td style="text-align: center;">0</td> </tr> </table>		<u>AT1</u>	60	50	40	30	20	10	0	<table border="0"> <tr> <td style="text-align: center;"><u>DVM</u></td> </tr> <tr> <td style="text-align: center;">310 ± 5 mVdc</td> </tr> <tr> <td style="text-align: center;">586</td> </tr> <tr> <td style="text-align: center;">862</td> </tr> <tr> <td style="text-align: center;">1138</td> </tr> <tr> <td style="text-align: center;">1414</td> </tr> <tr> <td style="text-align: center;">1690 ± 5 mVdc</td> </tr> <tr> <td style="text-align: center;">1966</td> </tr> </table>	<u>DVM</u>	310 ± 5 mVdc	586	862	1138	1414	1690 ± 5 mVdc	1966	
<u>AT1</u>																			
60																			
50																			
40																			
30																			
20																			
10																			
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586																			
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1138																			
1414																			
1690 ± 5 mVdc																			
1966																			

5-10. LOG AMPLITUDE ALINEMENT - CW A1A6, A1A7, A1A9- Continued

STEP	PROCEDURE INDICATIONS	ACTION	
<b>NOTE</b>			
To prevent misalignment, the dc output must be more negative than -25 mVdc.			
29.	Disconnect W6 from the IFP.	-25 to -50 mVdc on DVM	
30. A1A7	Record DVM reading.		
31.	On ESTS, set USB/LSB switch to LSB and AT1 to 60.		
32.	Connect ac voltmeter and DVM to IFP connector A2XA3-C (LSB) as shown in fig. 5-5.		
33.	Disconnect W7 from the IFP.		
34.	Adjust A1A7R48; observe ac voltmeter.	Peak voltage on ac volt Meter	Adjust A1A7R21 to electrical mid range, as indicated on DVM, and repeat this step.
35.	Connect W7 to IFP J7.	310 ± 5 mVdc on DVM	Adjust A1A7R36.
<b>NOTE</b>			
To prevent misalignment, the dc output must be more negative than -25 mVdc.			
36.	Disconnect W7 from the IFP.  not change more	-25 to -50 mVdc on DVM	Adjust A1A7R48; verify reading on ac voltmeter does  than + 10 mVac during adjustment.
37.	Connect W7 to IFP J7.		
38.	Set ESTS AT1 to 10.	1690 ± 5 mVdc on DVM	Adjust A1 A7R21.
39.	A1A7R48, A1A7R36, and A1A7R21 interact. Set ESTS AT1 to 60 and repeat steps 35 through 38 until no adjustments are necessary.	As specified	
<b>5-58</b>			

**5-10. LOG AMPLITUDE ALINEMENT -CW A1A6, A1A7, A1A9- Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
40.	Set ESTS AT1 to the following positions and verify voltages on DVM $\pm 25$ mVdc except where noted <u>AT1</u> 60 50 40 30 20 10 0	<u>DVM</u> 310 $\pm 5$ mVdc 586 862 1138 1414 1690 $\pm 5$ mVdc 1966	
<p style="text-align: center;"><b>NOTE</b></p> <p style="text-align: center;">To prevent misalignment, the dc output must be more negative than -25 mVdc.</p>			
41. 42. 43.	Disconnect W7 from the IFP. Record DVM reading. Compare readings recorded in steps 18, 30, and 42.	-25 to -50 mVdc on DVM  Steps 30 and 42 will be within 10 mVdc of each other and both will be less negative than step 18	
44.	Turn power supplies off. Set ESTS POWER switch OFF.		
45.	Install A2A3 (para 5-32).		

**5-11. TRIGGER LOG AMPLITUDE BALANCE - PULSE A2A3**

STEP	PROCEDURE INDICATIONS	ACTION	
------	-----------------------	--------	--

**NOTE**

If alinement cannot be successfully completed, replace A2A3 (para 5-32). Repeat alinement procedure (para 5-8). If fault persists, send IFP to higher level maintenance.

- |    |                                   |  |  |
|----|-----------------------------------|--|--|
| 1. | Connect test equipment (fig 5-1). |  |  |
|----|-----------------------------------|--|--|

**NOTE**

Ensure equipment warms up at least 30 minutes before making adjustments.

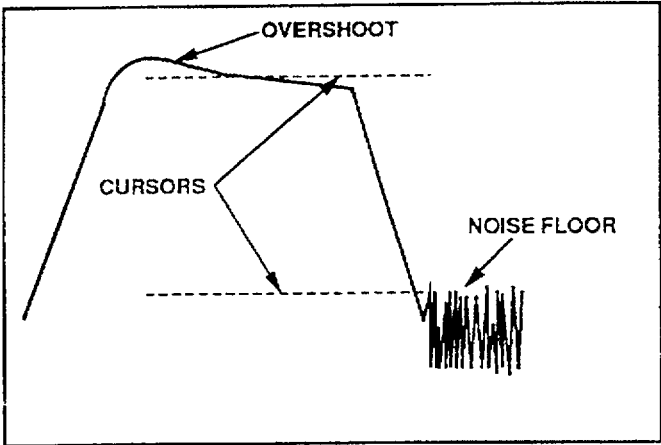
- |    |   |  |  |
|----|---|--|--|
| 2. | On ESTS, set:<br>Switch                    Set to<br>IF FREQ MHz            150.0<br>USB/LSB                LSB<br>SSB OFFSET            0<br>DVM SEL                VOLTS<br>AT1                      50<br>AT2                      cf<br>MOD/PW                600 nS<br>PW SET                 full cw<br>TRIG SEL               ST TRIG/<br>PW RST<br>EXT THRESHOFF<br>EXT THRESH<br>ADJ                      Full cw<br>SWEEP                  OFF<br>BAND CMD              LB<br>BW CMD                30 MHz<br>BIT TEST                OFF<br>PHASE-DEG            0<br>PRF                      10 KHz<br>DATA SELECT        B-CQ<br>POWER                 ON |  |  |
|----|---|--|--|

- |    |   |  |  |
|----|---|--|--|
| 3. | Connect o-scope to A2A3TP1 and A2A3TP2 (GND). Trigger on PRF OUT at J2 of ESTS. |  |  |
|----|---|--|--|



5-11. TRIGGER LOG AMPLITUDE BALANCE - PULSE A2A3 - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
4.	Set o-scope cursors to the peak signal level and the noise floor.		
5. 4	Set ESTS USB/LSB switch to USB. A1A7).	Peak amplitude will be within $\pm 10$ mV of step  Noise floor level will be within + 10 mV of step 4	a. Perform para 5-10, steps 21 through end (A1A6,  b. Repeat this paragraph.



**5-12.PULSE THRESHOLD ALINEMENT A2A3**

STEP	PROCEDURE INDICATIONS	ACTION																																													
		<b>NOTE</b>																																													
	If alinement cannot be successfully completed, replace A2A3 (para 5-32). Repeat alinement procedure (para 5-8). If fault persists, send IFP to higher level maintenance.																																														
1.	Connect test equipment (fig 5-1).																																														
		<b>NOTE</b>																																													
	Ensure equipment warms up at least 30 minutes before making adjustments.																																														
2.	On ESTS, set: <table border="0" style="width: 100%;"> <tr> <td style="text-align: left;"><u>Switch</u></td> <td style="text-align: left;"><u>Set to</u></td> </tr> <tr> <td>IF FREQ MHz</td> <td>150.0</td> </tr> <tr> <td>USB/LSB</td> <td>USB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>10</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MOD/PW</td> <td>600 nS</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/</td> </tr> <tr> <td>PW RST</td> <td></td> </tr> <tr> <td>EXTTHRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>Full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>PRF</td> <td>10 KHz</td> </tr> <tr> <td>DATA SELECT</td> <td>B-CQ</td> </tr> <tr> <td>POWER</td> <td>ON</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHz	150.0	USB/LSB	USB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	10	AT2	cf	MOD/PW	600 nS	PW SET	full cw	TRIG SEL	ST TRIG/	PW RST		EXTTHRESH	OFF	EXT THRESH		ADJ	Full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PHASE-DEG	0	PRF	10 KHz	DATA SELECT	B-CQ	POWER	ON		
<u>Switch</u>	<u>Set to</u>																																														
IF FREQ MHz	150.0																																														
USB/LSB	USB																																														
SSB OFFSET	0																																														
DVM SEL	VOLTS																																														
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MOD/PW	600 nS																																														
PW SET	full cw																																														
TRIG SEL	ST TRIG/																																														
PW RST																																															
EXTTHRESH	OFF																																														
EXT THRESH																																															
ADJ	Full cw																																														
SWEEP	OFF																																														
BAND CMD	LB																																														
BW CMD	30 MHz																																														
BIT TEST	OFF																																														
PHASE-DEG	0																																														
PRF	10 KHz																																														
DATA SELECT	B-CQ																																														
POWER	ON																																														
3.	Connect o-scope to PWG and PWG GND (GND) test points on ESTS. Trigger on PRF OUT at J2 of ESTS.	Pulse will be positive ECL pulse greater than 600 nSec in width																																													
4.	Set ESTS AT1 to 60.	Clean pulse (present 100%	Adjust A2A3R1 8. of the time)																																												

**5-12.PULSE THRESHOLD ALINEMENT A2A3 - Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
5.	Set ESTS USB/LSB switch	Clean pulse	Adjust A2A3R 18. to LSB.
6.	Switch ESTS USB/LSB switch between USB and LSB positions.	Very clean pulse in both positions	
7.	Set ESTS USB/LSB switch to USB.		
8.	Set ESTS AT1 from 10 to 50.	Clean pulse	Adjust A2A3R 18.
<p><b>NOTE</b></p> <p>At ESTS AT1 setting of 60, PWG must be as clean as possible in both USB and LSB. Do not sacrifice the clean PWG signal at settings between 10 and 50 to obtain a clean signal at 60.</p>			
9.	Set ESTS AT1 to 60.	Clean pulse	Adjust A2A3R18.
10.	Repeat steps 8 and 9 until no adjustment is necessary.		
11.	Set ESTS USB/LSB switch to LSB.		
12.	Set ESTS AT1 from 10 to 50.	Clean pulse	Adjust A2A3R18.
<p><b>NOTE</b></p> <p>At ESTS AT1 setting of 60, PWG must be as clean as possible in both USB and LSB. Do not sacrifice the clean PWG signal at settings between 10 and 50 to obtain a clean signal at 60.</p>			
13.	Set ESTS AT1 to 60.	Clean pulse	Adjust A2A3R18.
14.	Set ESTS AT2 from cf to cf +3.	PWG pulses will reduce to approximately 50% in occurrence somewhere between cf and cf + 3.	Repeat steps 4 through 14.
15.	Set ESTS AT2 from cf to cf +6. Note the AT2 setting where pulse (PWG) disappears.	Pulse will disappear with AT2 between cf + 3 and cf + 6	

**5-12. PULSE THRESHOLD ALINEMENT A2A3 - Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
16.	Set ESTS DVM SEL to EXT THRESH.		
17.	Adjust ESTS EXT THRESH-HOLD ADJ.	-0.15 on ESTS panel meter	
18.	Set ESTS ATI to .		
19.	Switch ESTS EXT THRESH between ON and OFF.	The pulse (PWG) cleans up when switch is ON	

**5-13. CW THRESHOLD ALINEMENT A2A3**

STEP	PROCEDURE INDICATIONS	ACTION
	<b>NOTE</b>	
	If alinement cannot be successfully completed, replace A2A3 (para 5-32). Repeat alinement procedure (para 5-8). If fault persists, send IFP to higher level maintenance.	
1.	Connect test equipment (fig. 5-1).	
	<b>NOTE</b>	
	Ensure equipment warms up at least 30 minutes before making adjustments.	
2.	On ESTS, set: Switch                      Set to  IF FREQ MHz              150.0 USB/LSB                    USB SSB OFFSET                0 DVM SEL                    VOLTS AT1                          10 AT2                          cf MOD/PW                    CW PW SET                      full cw TRIG SEL                   ST TRIG/ PW RST EXT THRESHOFF EXT THRESH ADJ                          Full cw SWEEP                      OFF BAND CMD                  LB BW CMD                    30 MHz BIT TEST                    OFF PHASE-DEG                0 PRF                          10 KHz DATA SELECT              A-CQ POWER                      ON	
3.	Connect o-scope to PWG and PWG GND (GND) test points on ESTS. Trigger on PWG. will be 1000 +/- 100 uSec	Pulse will be positive 500 +/- 50 nSec ECL pulse; pulse repetition interval  5-65

**5-13. CW THRESHOLD ALINEMENT A2A3 - Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
4.	Set ESTS AT1 to 60.	Clean pulse (present 100% the time)	Adjust A2A3R17 for same of indication as step 3.
5.	Set ESTS USB/LSB switch to LSB.	Clean pulse	Adjust A2A3R17.
6.	Switch ESTS USB/LSB between USB and LSB.	Verify clean pulse in both positions	
7.	Set ESTS USB/LSB switch to LSB.		
8.	Set ESTS AT1 from 10 to 50.	Clean pulse	Adjust A2A3R17.
<p><b>NOTE</b></p> <p>At ESTS AT1 setting of 60, PWG must be as clean as possible in both USB and LSB. Do not sacrifice the clean PWG signal at settings between 10 and 50 to obtain a clean signal at 60.</p>			
9.	Set ESTS AT1 to 60. Clean pulse	Adjust A2A3R17.	
10.	Repeat steps 8 and 9 until no adjustment is necessary.		
11.	Set ESTS AT1 to 60.	Clean pulse	
12.	Set ESTS AT2 from of to cf +3.	PWG pulses will reduce approximately 50% in occurrence between cf and cf + 3	Repeat steps 4 through 12.
13.	Set ESTS AT2 from cf to cf + 6. Note AT2 level where PWG disappears.	PWG will disappear between cf + 3 and cf + 6	

**5-14. DF/TRIGGER LOG AMPLITUDE NOISE FLOOR ALINEMENT A2A3**

STEP	PROCEDURE INDICATIONS	ACTION																																												
<b>NOTE</b>																																														
<p>If alinement cannot be successfully completed, replace A2A3 (para 5-32). Repeat alinement procedure (para 5-8). If fault persists, send IFP to higher level maintenance.</p>																																														
1.	<p>Connect test equipment (fig 5-1).</p>																																													
<b>NOTE</b>																																														
<p>Ensure equipment warms up at least 30 minutes before making adjustments.</p>																																														
2.	<p>On ESTS, set:</p> <table border="0"> <thead> <tr> <th><u>Switch</u></th> <th><u>Set to</u></th> </tr> </thead> <tbody> <tr> <td>IF FREQ MHz</td> <td>150.0</td> </tr> <tr> <td>USB/LSB</td> <td>LSB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>AT2</td> <td>of</td> </tr> <tr> <td>MOD/PW</td> <td>600 nS</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/</td> </tr> <tr> <td>PW RST</td> <td></td> </tr> <tr> <td>EXT THRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>Full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>PRF</td> <td>10 KHz</td> </tr> <tr> <td>DATA SELECT</td> <td>A-CQ</td> </tr> <tr> <td>POWER</td> <td>OFF</td> </tr> </tbody> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHz	150.0	USB/LSB	LSB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	30	AT2	of	MOD/PW	600 nS	PW SET	full cw	TRIG SEL	ST TRIG/	PW RST		EXT THRESH	OFF	EXT THRESH		ADJ	Full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PHASE-DEG	0	PRF	10 KHz	DATA SELECT	A-CQ	POWER	OFF	
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DATA SELECT	A-CQ																																													
POWER	OFF																																													
3.	<p>Place A2A3 on extender.</p>																																													
4.	<p>Connect o-scope to A2A3TP6, A2A3TP7, and A2A3TP2 (GND).</p>																																													
<b>5-67</b>																																														

**5-14. OFFTRIGGER LOG AMPLITUDE NOISE FLOOR ALINEMENT A2A3 - Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
<b>NOTE</b>			
O-scope 20 MHZ BW LIMIT can be used to clean up the signals.			
5.	Trigger on PRF OUT at J2 of ESTS. Set o-scope channels for 50 mV/div. Reference both channels to the same zero line.	Traces overlay each other within $\pm 5$ mV	Adjust A2A3R105.
6.	Set o-scope cursor to peak of A2A3TP6 signal.		
7.	Trigger o-scope off A2A3TP6.		
8.	Set ESTS MOD/PW switch to CW.	A2A3TP6 signal is within $\pm 5$ mV of cursor; A2A3TP7 signal is within $\pm 5$ mV of cursor.	Adjust A2A3R52 (TP6) Adjust A2A3R100 (TP7).
9.	Switch ESTS MOD/PW switch between 600 nSec and CW.	Verify readings of step 8	Repeat step 8.
10.	Turn ESTS POWER switch OFF. Turn power supply OFF.		
11.	Remove A2A3 and extender from IFP.		
12.	Install A2A3 (para 5-32).		
13.	Turn on power to power supply. Turn ESTS POWER switch ON.		
14.	Repeat this para with A2A3 installed to verify settings.		



**5-15. DF LOG AMPLITUDE SAMPLE AND HOLD ALINEMENT - CW/PULSE A2A11**

STEP	PROCEDURE INDICATIONS	ACTION																																					
<b>NOTE</b>																																							
<p>If alinement cannot be successfully completed, replace A2A1 1 (para 5-32). Repeat alinement procedure (para 5-8). If fault persists, send IFP to higher level maintenance.</p>																																							
1.	Connect test equipment (fig. 5-1).																																						
<b>NOTE</b>																																							
<p>Ensure equipment warms up at least 30 minutes before making adjustments.</p>																																							
2.	<p>On ESTS, set:</p> <table border="0"> <thead> <tr> <th><u>Switch</u></th> <th><u>Set to</u></th> </tr> </thead> <tbody> <tr><td>IF FREQ MHz</td><td>150.0</td></tr> <tr><td>USB/LSB</td><td>LSB</td></tr> <tr><td>SSB OFFSET</td><td>0</td></tr> <tr><td>DVM SEL</td><td>EXT THRESH</td></tr> <tr><td>AT2</td><td>cf</td></tr> <tr><td>MOD/PW</td><td>CW</td></tr> <tr><td>PW SET</td><td>full cw</td></tr> <tr><td>TRIG SEL</td><td>ST TRIG/</td></tr> <tr><td>PW RST</td><td></td></tr> <tr><td>EXTTHRESH</td><td>ON</td></tr> <tr><td>BAND CMD</td><td>LB</td></tr> <tr><td>BW CMD</td><td>30 MHz</td></tr> <tr><td>BIT TEST</td><td>OFF</td></tr> <tr><td>PHASE-DEG</td><td>0</td></tr> <tr><td>PRF</td><td>10 KHz</td></tr> <tr><td>DATA SELECT</td><td>LOG</td></tr> <tr><td>POWER</td><td>ON</td></tr> </tbody> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHz	150.0	USB/LSB	LSB	SSB OFFSET	0	DVM SEL	EXT THRESH	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIG/	PW RST		EXTTHRESH	ON	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PHASE-DEG	0	PRF	10 KHz	DATA SELECT	LOG	POWER	ON		
<u>Switch</u>	<u>Set to</u>																																						
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BW CMD	30 MHz																																						
BIT TEST	OFF																																						
PHASE-DEG	0																																						
PRF	10 KHz																																						
DATA SELECT	LOG																																						
POWER	ON																																						
3.	Set EXT THRESH ADJ.	-0.15 on ESTS DVM																																					
<b>NOTE</b>																																							
<p>Ensure EXT THRESH ADJ is not disturbed through the end of this paragraph.</p>																																							

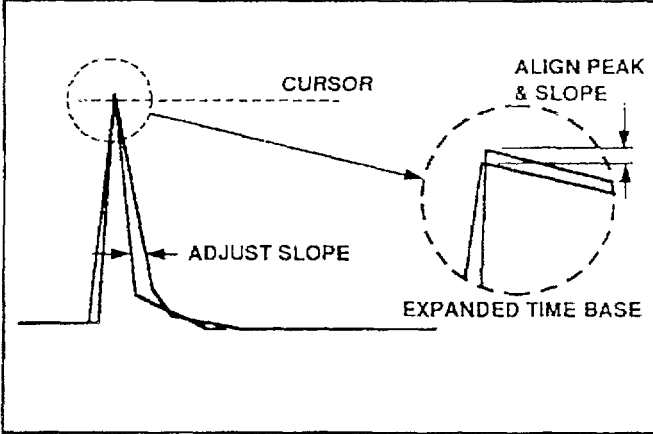
**5-15.DF LOG AMPLITUDE SAMPLE AND HOLD ALINEMENT - CWIPULSE A2A11 - Continued**

STEP	PROCEDURE INDICATIONS	ACTION
4.	On ESTS, set DVM SEL to VOLTS and EXT THRESH to OFF.	
5.	Set ESTS AT1 to 50.	
6.	Adjust A2A11 R5+1.25 + 0.02 on ESTS DVM	
7.	Set ESTS AT1 to 10.	
8.	Adjust A2A11 R4.+4.25 0.02 on ESTS DVM	
9.	A2A11 R5 and A2A11R4 interact. Repeat steps 5 through 8 until no adjustments are necessary.	As specified.
<b>NOTE</b>		
In the following steps for AT1 setting of 0, set ESTS EXT THRESH switch to ON.		
10.	Set ESTS AT1 to the following positions and verify voltages on ESTS DVM + 0.050.	
	<u>AT1</u>	<u>ESTS DVM</u>
	60	0.500
	50	1.250
	40	2.000
	30	2.750
	20	3.500
	10	4.250
	0	5.000
11.	Set ESTS USB/LSB switch to USB.	
12.	Repeat step 10.As specified.	
13.	Set ESTS MOD/PW switch to 600 nSec.	
14.	Repeat step 10.As specified	
15.	Set ESTS USB/LSB switch to LSB.	
16.	Repeat step 10.As specified.	
		<b>5-70</b>

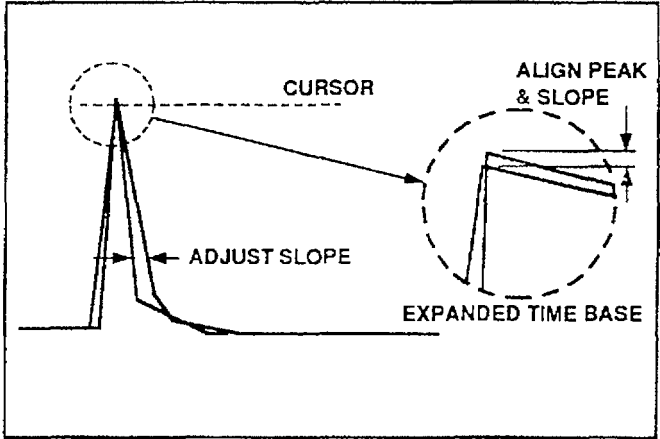
**5-16. DF/TRIGGER LOG AMPLITUDE BALANCE ALINEMENT A2A9**

STEP	PROCEDURE INDICATIONS	ACTION																																											
	<b>NOTE</b>																																												
	If alinement cannot be successfully completed, replace A2A9 (para 5-32). Repeat alinement procedure (para 5-8). If fault persists, send IFP to higher level maintenance.																																												
1.	Connect test equipment (fig. 5-1).																																												
	<b>NOTE</b>																																												
	Ensure equipment warms up at least 30 minutes before making adjustments.																																												
2.	On ESTS, set: <table border="0" style="width: 100%;"> <thead> <tr> <th style="text-align: left;"><u>Switch</u></th> <th style="text-align: left;"><u>Set to</u></th> </tr> </thead> <tbody> <tr><td>IF FREQ MHz</td><td>150.0</td></tr> <tr><td>USB/LSB</td><td>USB</td></tr> <tr><td>SSB OFFSET</td><td>0</td></tr> <tr><td>DVM SEL</td><td>VOLTS</td></tr> <tr><td>AT1</td><td>50</td></tr> <tr><td>AT2</td><td>cf</td></tr> <tr><td>MOD/PW</td><td>CW</td></tr> <tr><td>PW SET</td><td>full cw</td></tr> <tr><td>TRIG SEL</td><td>ST TRIG/</td></tr> <tr><td>PW RST</td><td></td></tr> <tr><td>EXT THRESH</td><td>OFF</td></tr> <tr><td>EXT THRESH</td><td></td></tr> <tr><td>ADJ</td><td>fully cw</td></tr> <tr><td>BAND CMD</td><td>LB</td></tr> <tr><td>BW CMD</td><td>30 MHz</td></tr> <tr><td>BIT TEST</td><td>OFF</td></tr> <tr><td>PHASE-DEG</td><td>0</td></tr> <tr><td>PRF</td><td>10 KHz</td></tr> <tr><td>DATA SELECT A-CQ</td><td></td></tr> <tr><td>POWERON</td><td></td></tr> </tbody> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHz	150.0	USB/LSB	USB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	50	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIG/	PW RST		EXT THRESH	OFF	EXT THRESH		ADJ	fully cw	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PHASE-DEG	0	PRF	10 KHz	DATA SELECT A-CQ		POWERON			
<u>Switch</u>	<u>Set to</u>																																												
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PRF	10 KHz																																												
DATA SELECT A-CQ																																													
POWERON																																													
3.	Connect o-scope to A2A11TP2, A2A9TP2, and A2A11TP3 (GND). Trigger on A2A11TP2.																																												
	<b>5-71</b>																																												

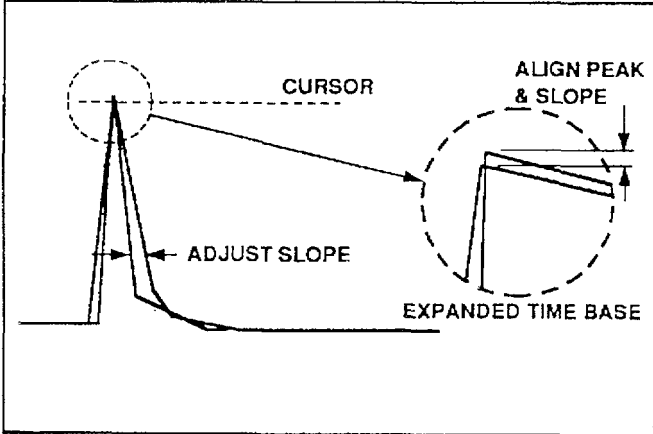
5-16.DF/TRIGGER LOG AMPLITUDE BALANCE ALINEMENT A2A9 - Continued

STEP	PROCEDURE INDICATIONS	ACTION
4.	Set o-scope channels for 200 mV/div. Reference both channels to the same zero line. Set o-scope time base for 200 uSec/div. Set both channels for dc coupling.	
5.	Set ESTS AT1 to 50.	
<p><b>NOTE</b></p> <p>The o-scope 20 MHZ BW LIMIT may be used to clean up the signals. Expand the time base as required to verify the full amplitude of the signal is displayed.</p>		
6.	Adjust A2A9R7. shown.	<p>Superimpose the traces as</p> 
7.	Set ESTS AT1 to 10.	
8.	Adjust o-scope VOLTS/DIV to see full trace.	

5-16.DFITRIGGER LOG AMPLITUDE BALANCE ALINEMENT A2A9 - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
9.	Adjust A2A9R13.	<p>Superimpose the traces as shown</p> 	
10.	A2A9R7 and A2A9R13 interact. Repeat steps 5 through 9 until adjustment is not necessary. Use o-scope time base to expand signal to find best results.	As specified	
11.	Using o-scope, monitor the signal at A2A11TP2 and A2A9TP3 with respect to A2A11TP3 (GND). Trigger on A2A11TP2.		
12.	Set ESTS USB/LSB switch to LSB.		
13.	Set ESTS AT1 to 50.		
<p><b>NOTE</b></p> <p>The o-scope 20 MHZ BW LIMIT may be used to clean up the signals. Expand the time base as required to verify the full amplitude of the signal is displayed.</p>			

5-16. DFITRIGGER LOG AMPLITUDE BALANCE ALINEMENT A2A9-Continued

STEP	PROCEDURE INDICATIONS	ACTION
14.	Adjust A2A9R26. Superimpose the traces as shown	
15.	Set ESTS AT1 to 10.	
16.	Adjust A2A9R19. Superimpose the traces.	
17.	A2A9R26 and A2A9R19 interact. Repeat steps 13 through 16 until adjustment is not necessary. Use o-scope time base to expand signal to find best results.	

**5-17. INPUT DF CHANNEL AMPLITUDE CHECK -CW A1A1, A1A2, A1A4, A1A5**

STEP	PROCEDURE INDICATIONS	ACTION																																										
<b>NOTE</b>																																												
<p>If alinement cannot be successfully completed, replace AI A1, A1A2, A1A4, and A1A5 (phase matched sets) (para 5-31). Repeat alinement procedure (para 5-8). If fault persists, send IFP to higher level maintenance.</p>																																												
1.	<p>Connect test equipment (fig. 5-1).</p>																																											
2.	<p>On ESTS, set:</p> <table border="0"> <thead> <tr> <th><u>Switch</u></th> <th><u>Set to</u></th> </tr> </thead> <tbody> <tr> <td>IF FREQ MHz</td> <td>150.0</td> </tr> <tr> <td>USB/LSB</td> <td>'LSB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/</td> </tr> <tr> <td>PW RST</td> <td></td> </tr> <tr> <td>EXTTHRESHOFF</td> <td></td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>fully cw</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>PRF</td> <td>10 KHz</td> </tr> <tr> <td>DATA SELECT</td> <td>B-CQ</td> </tr> <tr> <td>POWER</td> <td>OFF</td> </tr> </tbody> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHz	150.0	USB/LSB	'LSB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	30	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIG/	PW RST		EXTTHRESHOFF		EXT THRESH		ADJ	fully cw	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PHASE-DEG	0	PRF	10 KHz	DATA SELECT	B-CQ	POWER	OFF	
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PRF	10 KHz																																											
DATA SELECT	B-CQ																																											
POWER	OFF																																											
3.	<p>Turn power supply off.</p>																																											
4.	<p>Remove A1A12 and A1A13 (para 5-33).</p>																																											
<b>NOTE</b>																																												
<p>In steps that follow, J67 through J72 and J79 through J84 must always be terminated either by the rf power meter or 50 ohm terminations. Swap 50 ohm terminations as required.</p>																																												
<b>5-75</b>																																												

**5-17. INPUT DF CHANNEL AMPLITUDE CHECK -CW A1A1, A1A2, A1A4, A1A5-Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
5.	Install 50 ohm terminations on J68 through J72 and J79 through J84.		
6.	Calibrate rf power meter (para 5-6).		
7.	Connect rf power meter to J67.		
<b>NOTE</b>			
Ensure equipment warms up at least 30 minutes before making adjustments.			
8.	Turn on power supply. Set ESTS POWER switch to OFF.		
9.	Measure power at J67 on IFP.	+7 + 2.0 dBm	
10.	Step ESTS AT1 from 60 to 0. settings.	+7 + 2.0 dBm at all	
11.	Measure power at J68. 50 ohm terminations as required	Move+5 + 2.5 dBm maintenance.	Send IFP to higher level
12.	Measure power at J89 through J72. Move 50 ohm terminations as required	+7 . 2.0 dBm at all connectors	Send IFP to higher level maintenance.
13.	Measure power at J79 through J84. Move 50 ohm as required.	+7 z 2.0 dBm at all connectors	Send IFP to higher level maintenance.



**5-18. INPUT DF CHANNEL PHASE ALINEMENT AA1, A1A2, A1A4, A1A5**

STEP	PROCEDURE INDICATIONS	ACTION																																													
<b>NOTE</b>																																															
<p>If alinement cannot be successfully completed, replace A1A1, A1A2, A1A4, and A1A5 (phase matched sets) (para 5-24). Repeat alinement procedure (para 5-8). If fault persists, send IFP to higher level maintenance.</p>																																															
1.	Connect test equipment (fig. 5-1).																																														
2.	<p>On ESTS, set:</p> <table border="0"> <thead> <tr> <th><u>Switch</u></th> <th><u>Set to</u></th> </tr> </thead> <tbody> <tr><td>IF FREQ MHz</td><td>150.0</td></tr> <tr><td>USB/LSB</td><td>LSB</td></tr> <tr><td>SSB OFFSET</td><td>0</td></tr> <tr><td>DVM SEL</td><td>VOLTS</td></tr> <tr><td>AT1</td><td>30</td></tr> <tr><td>AT2</td><td>cf</td></tr> <tr><td>MOD/PW</td><td>CW</td></tr> <tr><td>PW SET</td><td>full cw</td></tr> <tr><td>TRIG SEL</td><td>ST TRIG/</td></tr> <tr><td>PW RST</td><td></td></tr> <tr><td>EXT THRESHOFF</td><td></td></tr> <tr><td>EXT THRESH</td><td></td></tr> <tr><td>ADJ</td><td>fully cw</td></tr> <tr><td>SWEEP</td><td>OFF</td></tr> <tr><td>BAND CMD</td><td>LB</td></tr> <tr><td>BW CMD</td><td>30 MHz</td></tr> <tr><td>BIT TEST</td><td>OFF</td></tr> <tr><td>PHASE-DEG</td><td>0</td></tr> <tr><td>PRF</td><td>10 KHz</td></tr> <tr><td>DATA SELECT</td><td>B-CQ</td></tr> <tr><td>POWER</td><td>OFF</td></tr> </tbody> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHz	150.0	USB/LSB	LSB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	30	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIG/	PW RST		EXT THRESHOFF		EXT THRESH		ADJ	fully cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PHASE-DEG	0	PRF	10 KHz	DATA SELECT	B-CQ	POWER	OFF		
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POWER	OFF																																														
3.	Turn power supply power off.																																														
4.	Remove A1A12 and A1A13 (para 5-33).																																														
<b>NOTE</b>																																															
<p>In steps that follow, J67 through J72 and J79 through J84 must always be terminated either by the VVM probes or 50 ohm terminations. Swap 50 ohm terminations as required.</p>																																															
5-77																																															

**5-18 INPUT DF CHANNEL PHASE ALINEMENT A1A1, A1A2, A1A4, A1A5- Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
5.	Install 50 ohm terminations on J67 through J70, J72, J79, and J81 through J84.		
<b>NOTE</b>			
Ensure equipment warms up at least 30 minutes before making adjustments.			
5.	Turn on power supply. Set		
6.	ESTS POWER switch to ON.		
7.	Zero the VVM using J1 as		
7.	reference.		
8.	Connect VVM channel A to	Phase will be $0.0 \pm 2.00$	a. Replace A1A1, A1A2, J71
8.	and channel B to J80, A1A4, and A1A5.		
9.	Set A1A1 C3, A1 A2C3,		
9.	A1A4C3, and A1A5C3 to		
9.	center of adjustment range.		
10.	Connect VVM channel A to	Phase of $+90 \pm 0.10$	Adjust A1A5C3.
10.	J71 and channel B to J70.		
11.	Connect VVM channel A to	Phase will be $0.0 \pm 4.00$	If tolerances can not be met, adjust A1A1C3 a few degrees and repeat procedure from step 10.
11.	J71 and channel B to J72.		
12.	Record phase value on VVM.		
13.	Adjust A1 A5C3.	Phase reading half of what was recorded in step 12	
13.			
14.	Connect VVM channel A to	Phase of $+90 \pm 0.1$	Adjust A1A4C3.
14.	J80 and channel B to J81.		
15.	Connect VVM channel A to	Phase will be $0.0 \pm 4.00$	If tolerances can not be met, adjust A1 A1C3 a few degrees and repeat procedure from step 10.
15.	J80 and channel B to J79.		
16.	Record phase value on VVM.		
17.	Adjust A1 A4C3.	Phase reading half of what was recorded in step 16	
17.			

**5-18 INPUT DF CHANNEL PHASE ALINEMENT A1A1, A1A2, A1A4, A1A5- Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
18.	Connect VVM channel A to J83 and channel B to J82.	Phase of $+90 \pm 0.1^\circ$	Adjust A1A2C3.
19.	Connect VVM channel A to J83 and channel B to J84.	Phase will be $0.0 + 4.00$	If tolerances can not be met, adjust A1A1C3 a few degrees and repeat procedure from step 10.
20.	Record phase value on VVM.		
21.	Adjust A1A2C3.	Phase reading half of what was recorded in step 20	If tolerances can not be met adjust A1 A1 C3 a few degrees and repeat procedure from step 10.
22.	Connect VVM channel A to J68 and channel B to J67.		
23.	Zero the VVM.		
24.	Connect VVM channel A to J68 and channel B to J69.	Phase will be $-90.0 + 4.00$	<p>a. Replace A1A10.</p> <p>b. Send IFP to higher level maintenance.</p>

**5-19. PHASE DETECTOR BALANCE-CW - PHASE/FINE FRU A1A12, A1A13**

STEP	PROCEDURE INDICATIONS	ACTION																																												
<b>NOTE</b>																																														
<p>If alinement cannot be successfully completed, replace A1A12 or A1A13 (para 5-32). Repeat alinement procedure (para 5-8). If fault persists, send IFP to higher level maintenance.</p>																																														
1.	<p>Connect test equipment (fig. 5-1).</p>																																													
2.	<p>On ESTS, set:</p> <table border="0"> <thead> <tr> <th><u>Switch</u></th> <th><u>Set to</u></th> </tr> </thead> <tbody> <tr> <td>IF FREQ MHz</td> <td>150.0</td> </tr> <tr> <td>USB/LSB</td> <td>LSB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/</td> </tr> <tr> <td>PW RST</td> <td></td> </tr> <tr> <td>EXT THRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>PRF</td> <td>10 KHz</td> </tr> <tr> <td>DATA SELECT A-CQ</td> <td></td> </tr> <tr> <td>POWEROFF</td> <td></td> </tr> </tbody> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHz	150.0	USB/LSB	LSB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	30	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIG/	PW RST		EXT THRESH	OFF	EXT THRESH		ADJ	full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PHASE-DEG	0	PRF	10 KHz	DATA SELECT A-CQ		POWEROFF		
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POWEROFF																																														
3.	<p>Turn power supply power off.</p>																																													
4.	<p>Remove A1A12 and A1A13 (para 5-33). Remove covers from A1A12 and A1A13 (para 5-30).</p>																																													
5.	<p>Remove A2A5, A2A6, A2A7, and A2A8 (para 5-32).</p>																																													
6.	<p>.Install A1A13 (para 5-33).</p>																																													
		<b>5-80</b>																																												

15-19. PHASE DETECTOR BALANCE -CW- PHASE/FINE FRU A1A12, A1A13-Continued

STEP	PROCEDURE INDICATIONS	ACTION
<b>NOTE</b>		
Ensure equipment warms up at least 30 minutes before making adjustments.		
7.	Turn on power supply. Set ESTS POWER switch to ON.	
8.	Set ESTS PHASE-DEG switch to -90.	
9.	Connect DVM to A2XA5-A as shown in fig. 5-6.	Record DVM reading

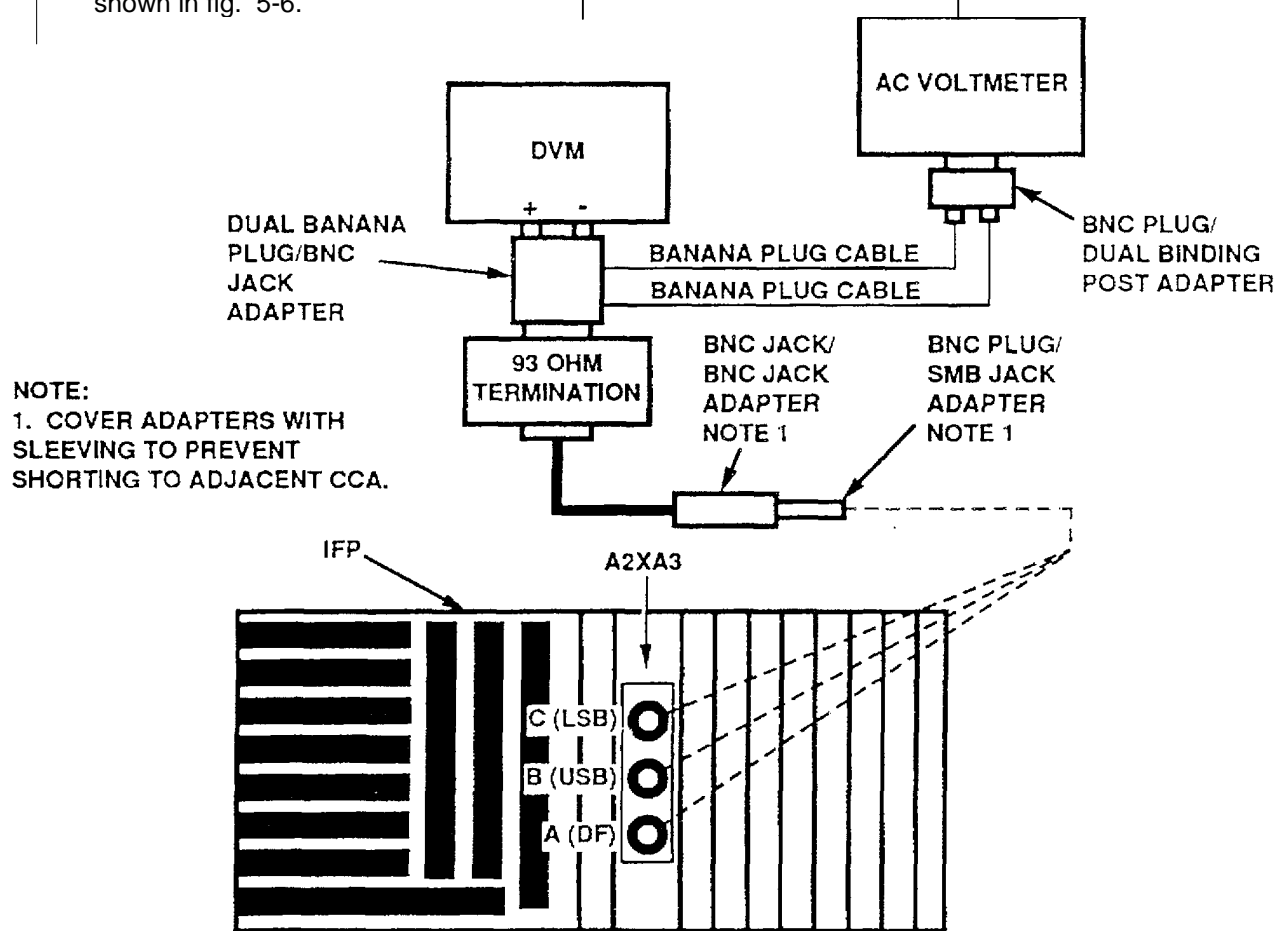


FIGURE 5-6. METER HOOKUP

5-19. PHASE DETECTOR BALANCE -CW- PHASE/FINE FRU A1A12, A1A13-Continued

STEP	PROCEDURE INDICATIONS	ACTION	
10.	Set ESTS PHASE-DEG switch to +90. step 9	DVM reading will be within + 0.01 Vdc of	Adjust A1A13A2C19.
11. through 11.	Switch ESTS PHASE-DEG switch between +90 and -90.	DVM readings will be within + 0.01 Vdc of each other	<u>a.</u> Adjust A1A1C3. <u>b.</u> Repeat steps 8
12.	Connect DVM to A2XA5-C.		
13.	Set ESTS PHASE-DEC switch to -180.		
14.	Record DVM reading.		
15.	Set ESTS PHASE-DEG switch to 0.	DVM reading will be within <u>+0.01</u> Vdc of step 14	Adjust A1A13A2C22.
16.	Switch ESTS PHASE-DEG switch between -180 and 0.	DVM reading will be within <u>+0.01</u> Vdc of each other	<u>a.</u> Adjust AI AC3. <u>b.</u> Repeat steps 8 through 16.
17.	Connect DVM to A2XA7-A		
18.	Set ESTS PHASE-DEG switch to -90.		
19.	Record DVM reading.		
20.	Set ESTS PHASE-DEG switch to +90.	DVM reading will be within <u>± 0.01</u> Vdc of step 19.	Adjust A1A13A1C22.
21.	Switch ESTS PHASE-DEG switch between +90 and -90.	DVM readings will be within + 0.01 Vdc of each other	<u>a.</u> Adjust A1A2C3. <u>b.</u> Repeat steps 18 through
21.			
22.	Connect DVM to A2XA7-C.		
23.	Set ESTS PHASE-DEG switch to -180.		
24.	Record DVM reading.		
25.	Set ESTS PHASE-DEG switch to 0.	DVM reading will be within <u>+ 0.01</u> Vdc of step 24.	Adjust A1 A1 3A1 C19.
26.	Switch ESTS PHASE-DEG switch between -180 and 0.	DVM readings will be within + 0.01 Vdc of each other.	<u>a.</u> Adjust A1 A2C3. <u>b.</u> Repeat steps 18 through 26.
27.	Turn off power supply. Set ESTS POWER switch to OFF.		

**+5-19. PHASE DETECTOR BALANCE - CW- PHASE/FINE FRU A1A12, A1A13- Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
28.	Remove A1 AI 3 (para 5-33). Install A1 A12 (para 5-33).		
29.	Turn on power supply. Set ESTS Power switch to ON.		
30.	Connect DVM to A2XA6-A.		
31.	Set ESTS PHASE-DEG switch to -90.		
32.	Record DVM reading.		
33.	Set ESTS PHASE-DEG switch to +90.	DVM reading will be within - 0.01 Vdc of step 32	Adjust A1AI 2A2C23.
34.	Switch ESTS PHASE-DEG switch between +90 and - 90.	DVM reading will be within + 0.01 Vdc of each other.	<u>a.</u> Adjust A1A5C3. <u>b.</u> Repeat entire alinement procedure.
35.	Connect DVM to A2XA6-C.		
36.	Set ESTS PHASE-DEG switch to -180.		
37.	Record DVM reading.		
38.	Set ESTS PHASE-DEG switch to 0.	DVM reading will be within - 0.01 Vdc of step 37	Adjust A1A12A2C26.
39.	Switch ESTS PHASE-DEG switch between -180 and 0.	DVM reading will be within + 0.01 Vdc of each other.	<u>a.</u> Adjust A1A5C3. <u>b.</u> Repeat entire alinement procedure.
40.	Connect DVM to A2XA8-C.		
41.	Set ESTS PHASE-DEG switch to 0. Set ESTS IF FREQ MHZ switch to 140.0		
42.	Record DVM reading.		
43.	Set ESTS IF FREQ MHZ switch to 160.0_0.01 Vdc of step 42.	DVM reading will be within	Adjust A1 A1 2A1 C26.
44.	Switch ESTS IF FREQ MHZ switch between 140.0 and 160.0.	DVM readings will be within + 0.01 Vdc of each other.	
45.	Connect DVM to A2XA8-A.		
46.	Set ESTS IF FREQ MHZ switch to 150.0.		
47.	Record DVM reading		

**5-19. PHASE DETECTOR BALANCE -CW- PHASE/FINE FRU A1A12, A1A13-Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
48.	Set ESTS IF FREQ MHZ switch to 170.0	DVM reading will be within $\pm 0.05$ Vdc of step 47.	Adjust A1A12A1C23.
49.	Switch ESTS IF FREQ MHZ switch between 150.0 and 170.0.	DVM readings will be within $\pm 0.05$ Vdc of each other	
50.	Turn off power supply. Set ESTS POWER switch to OFF.		
51.	Remove A1 A12 (para 5-33).		
52.	Install covers on A1 A12 and A1A13 (para 5-30).		
53.	Install A1A12, A1A13, and left hand cover to IFP (para 5-33).		
54.	Install A2A5, A2A6, A2A7, and A2A8 in IFP (para 5-32).		



**5-20. PHASE CHANNEL SAMPLE AND HOLD ALINEMENT - CW A2A5, A2A6, A2A7**

STEP	PROCEDURE INDICATIONS	ACTION
1.	Connect test equipment (fig. 5-1).  Ensure equipment warms up at least 30 minutes before making adjustments.	<p style="text-align: center;"><b>NOTE</b></p>
2.	On ESTS, et: Switch                      Set to IF FREQ MHz            150.0 USB/LSB                 USB SSBOFFSET              0 DVM SEL                 VOLTS AT1                       30 AT2                       cf MOD/PW                 CW PW SET                  full cw TRIG SEL                ST TRIG/ PW RST EXT THRESH OFF EXT THRESH ADJ                      full cw SWEEP                   OFF BAND CMD               LB BW CMD                 30 MHz BIT TEST                OFF PRF                      10 KHz DATA SELECT          A-CI POWER                  ON	
3.	Set ESTS PHASE-DEG switch to -45.	
4.	Adjust A2A5R5.	+1.35 ± 0.02 Vdc on ESTS DVM
5.	Set ESTS PHASE-DEG switch to -135.	
6.	Adjust A2A5R4.	+4.05 ± 0.02 Vdc on ESTS DVM
7.	A2A5R5 and A2A5R4 interact. Repeat steps 3 through 6 until no adjustment is necessary.	

**5-20. PHASE CHANNEL SAMPLE AND HOLD ALINEMENT - CW A2A5, A2A6, A2A7-** Continued

STEP	PROCEDURE INDICATIONS	ACTION	
8.	Set ESTS DATA SELECT switch to A-CQ.		
9.	Set ESTS PHASE-DEG switch to -45	+1.35 ± 0.02 Vdc on ESTS DVM	Adjust A2A5R2.
10.	Set ESTS PHASE-DEG switch to +45	+4.05 0.02 Vdc on	Adjust A2A5R3.
11.	A2A5R2 and A2A5R3 interact. Repeat steps 9 and 10 until no adjustment is necessary.		
12.	Set ESTS DATA SELECT switch to A-DI.		
13.	Set ESTS PHASE-DEG switch to -45.	+1.35 + 0.02 Vdc on ESTS DVM	Adjust A2A6R5.
14.	Set ESTS PHASE-DEG switch to -135	+4.05 + 0.02 Vc's on ESTS DVM	Adjust A2A6R4.
15.	A2A6R5 and A2A6R4 interact. Repeat steps 13 and 14 until no adjustment is necessary.		
16.	Set ESTS DATA SELECT switch to A-DQ.		
17.	Set ESTS PHASE-DEG switch to -45.	+1.35 -t 0.02 Vdc on ESTS DVM	Adjust A2A6R2.
18.	Set ESTS PHASE-DEG switch to +45.	+4.05 + 0.02 Vdc on ESTS DVM	Adjust A2A6R3.
19.	A2A6R2 and A2A6R3 interact. Repeat steps 17 and 18 until no adjustment is necessary.		
20.	Set ESTS DATA SELECT switch to B-CI.		
21.	Set ESTS PHASE-DEG switch to -45	+1.35 + 0.02 Vdc on ESTS DVM	Adjust A2A7R5.
22.	Set ESTS PHASE-DEG switch to -135.	+4.05 + 0.02 Vdc on	Adjust A2A7R4.
23.	A2A7R5 and A2A7R4 interact. Repeat steps 21 and 22 until no adjustment is necessary.		

**5-20. PHASE CHANNEL SAMPLE AND HOLD ALINEMENT -CW A2A5, A2A6, A2A7- Continued**

STEP	PROCEDURE INDICATIONS	ACTION	
24.	Set ESTS DATA SELECT switch to B-CQ.		
25.	Set ESTS PHASE-DEG switch to -45	+1.35 + 0.02 Vdc on ESTS DVM	Adjust A2A7R2.
26.	Set ESTS PHASE-DEG switch to +45 ESTS DVM	+4.05 + 0.02 Vdc on	Adjust A2A7R3.
27.	A2A7R2 and A2A7R3 interact. Repeat steps 25 and 26 until no adjustment is necessary.		

**5-21. FINE FRU SAMPLE AND HOLD ALINEMENT - CW A2A8**

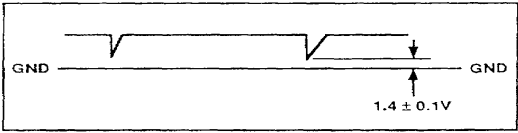
STEP	PROCEDURE INDICATIONS	ACTION																																											
1.	Connect test equipment (fig. 5-1).																																												
<b>NOTE</b>																																													
Ensure equipment warms up at least 30 minutes before making adjustments.																																													
2.	<p>On ESTS, set:</p> <table border="0"> <tr> <td><u>Switch</u></td> <td><u>Set to</u></td> </tr> <tr> <td>USB/LSB</td> <td>USB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>10</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/</td> </tr> <tr> <td>PW RST</td> <td></td> </tr> <tr> <td>EXTTHRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>PRF</td> <td>10 KHz</td> </tr> <tr> <td>DATA SELECT</td> <td>FRUQ</td> </tr> <tr> <td>POWER</td> <td>ON</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	USB/LSB	USB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	10	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIG/	PW RST		EXTTHRESH	OFF	EXT THRESH		ADJ	full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PHASE-DEG	0	PRF	10 KHz	DATA SELECT	FRUQ	POWER	ON		
<u>Switch</u>	<u>Set to</u>																																												
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PRF	10 KHz																																												
DATA SELECT	FRUQ																																												
POWER	ON																																												
3.	Set ESTS IF FREQ MHZ switch to 145.0	+1.35 t 0.02 Vdc on ESTS DVM	Adjust A2A8R2.																																										
4.	Set ESTS IF FREQ MHZ switch to 135.0	+4.05 ± 0.02 Vdc on ESTS DVM	Adjust A2A8R3.																																										
5.	A2A8R2 and A2A8R3 interact. Repeat steps 3 and 4 until no adjustment is necessary.																																												
6.	Set ESTS DATA SELECT switch to FRUI.																																												
7.	Set ESTS IF FREQ MHZ switch to 155.0	+1.35 t 0.02 Vdc on ESTS DVM	Adjust A2A8R5																																										

**5-21. FINE FRU SAMPLE AND HOLD ALINEMENT - CW A2A8 - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION
8.	Set ESTS IF FREQ MHZ switch to 145.0	+4.05 t 0.02 Vdc on ESTS DVM	Adjust A2A8R4.
9	A2A8R5 and A2A8R4 interact. Repeat steps 7 and 8 until no adjustment is necessary.		

**5-22. COURSE FRU SAMPLE AND HOLD ALINEMENT - CW A2A10, A2A11**

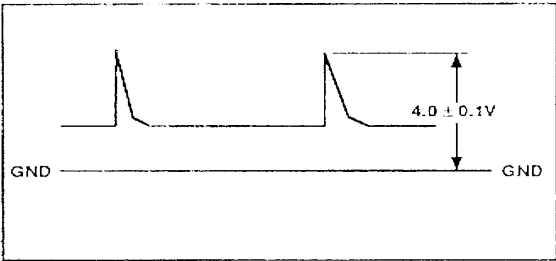
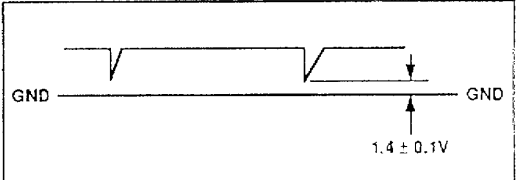
STEP	PROCEDURE	INDICATIONS	ACTION																																							
1.	Connect test equipment (fig. 5-1).	<p><b>NOTE</b></p> <p>Ensure equipment warms up at least 30 minutes before making adjustments.</p>																																								
2.	<p>On ESTS, set:</p> <table border="0"> <tr> <td><u>Switch</u></td> <td><u>Set to</u></td> </tr> <tr> <td>USB/LSB</td> <td>USB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/ PW RST</td> </tr> <tr> <td>EXTTHRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>PRF</td> <td>10 KHz</td> </tr> <tr> <td>DATA SELECT</td> <td>LOG</td> </tr> <tr> <td>POWER</td> <td>ON</td> </tr> </table>		<u>Switch</u>	<u>Set to</u>	USB/LSB	USB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	30	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIG/ PW RST	EXTTHRESH	OFF	EXT THRESH		ADJ	full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PHASE-DEG	0	PRF	10 KHz	DATA SELECT	LOG	POWER	ON
<u>Switch</u>	<u>Set to</u>																																									
USB/LSB	USB																																									
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DATA SELECT	LOG																																									
POWER	ON																																									
3.	Connect o-scope to A2A1 OTP2 and A2A1 OTP3 (GND).																																									
4.	Set ESTS IF FREQ MHZ switch to 135.0.	1.4 + 0.1 volts peak as shown	Adjust A2A1 OR5.																																							
5.	Read o-scope.																																									



5-22. COURSE FRU SAMPLE AND HOLD ALINEMENT - CW A2A10, A2A11 - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
6.	Set ESTS IF FREQ MHZ switch to 165.0.		
7.	Read o-scope.	+4.0 + 0.1 volts peak as shown	Adjust A2A10R4.
8.	A2A1 OR5 and A2A10R4 interact. Repeat steps 4 through 7 until no adjustment is necessary.		
9.	Set ESTS USB/LSB switch to LSB.		
10.	Connect o-scope to A2A10TP1 and A2A10TP3 (GND).		
11.	Set ESTS IF FREQ MHZ switch to 135.0.		
12.	Read o-scope.	+1.4 ± 0.1 volts peak as shown.	Adjust A2A10R2.
13.	Set ESTS IF FREQ MHZ switch to 165.0.		

5-22. COURSE FRU SAMPLE AND HOLD ALINEMENT - CW A2A10, A2A11 - Continued

STEP	PROCEDURE INDICATIONS	ACTION	
14.	Read o-scope.	+4.0 - 0.1 volts peak as shown	Adjust A2A10OR3. 
15.	Repeat steps 11 through 14 until no adjustment is necessary.		
16.	Set ESTS USB/LSB switch to USB.		
17.	Connect o-scope to A2A11TP1 and A2A11TP3 (GND).		
18.	Set ESTS IF FREQ switch to 135.0.		
19.	Read o-scope.	+1.4 - 0.1 volts peak as shown	Adjust A2A11R2. 
20.	Set ESTS IF FREQ MHZ switch to 165.0.		



5-22. COURSE FRU SAMPLE AND HOLD ALINEMENT -CW A2A10, A2A11 - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
21.	Read o-scope.	+4.0 + 0.1 volts peak as shown	Adjust A1 A11 R3.
<p>The diagram shows an oscilloscope trace within a rectangular frame. A horizontal line at the bottom is labeled 'GND' at both ends. The waveform consists of two identical pulses. Each pulse starts with a sharp vertical rise to a peak, followed by a gradual decay back to the baseline. A vertical double-headed arrow on the right side of the second pulse indicates the peak-to-ground voltage, which is labeled as <math>4.0 \pm 0.1V</math>.</p>			
22.	A2A11 R2 and A2A11 R3 interact. Repeat steps 18 through 21 until no adjustment is necessary.		

**5-23. FINAL PHASE CHANNEL ALINEMENT- CW**

STEP	PROCEDURE	INDICATIONS	ACTION																																										
1.	Connect test equipment (fig. 5-1).																																												
2.	Install alinement cover in place of right side cover (para 5-30).																																												
<b>NOTE</b>																																													
Ensure equipment warms up at least 45 minutes before making adjustments.																																													
3.	<p>On ESTS, set:</p> <table border="0" style="width: 100%;"> <tr> <td style="text-align: left;"><u>Switch</u></td> <td style="text-align: left;"><u>Set to</u></td> </tr> <tr> <td>IF FREQ MHZ</td> <td>150</td> </tr> <tr> <td>USB/LSB</td> <td>USB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>AT2</td> <td>cf.</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/</td> </tr> <tr> <td>PW RST</td> <td></td> </tr> <tr> <td>EXTTHRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PRF</td> <td>10 kHz</td> </tr> <tr> <td>DATA SELECT</td> <td>LOG</td> </tr> <tr> <td>POWER</td> <td>ON</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHZ	150	USB/LSB	USB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	30	AT2	cf.	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIG/	PW RST		EXTTHRESH	OFF	EXT THRESH		ADJ	full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	BIT TEST	OFF	PRF	10 kHz	DATA SELECT	LOG	POWER	ON		
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4.	Set ESTS DATA SELECT SWITCH TO A-CI.																																												
5.	Set ESTS PHASE-DEG switch to -90.																																												
6.	Record ESTS DVM reading.																																												
7.	Set ESTS PHASE-DEG switch to +90.	Reading will be within	Adjust A1A4C3. + 0.03 Vdc of step 6																																										

**5-23. FINAL PHASE CHANNEL ALINEMENT - CW - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION
8.	Set ESTS DATA SELECT switch to A-CQ.		
9.	Set ESTS PHASE-DEG switch to -180.		
10.	Record ESTS DVM reading.		
11.	Set ESTS PHASE-DEG switch to 0.	Reading will be within + 0.03 Vdc of step 10	<p><u>a.</u> Adjust AI A4C3 to split the difference between A-C1 and A-CQ.</p>
12.	Set ESTS DATA SELECT switch to A-DI.		<p><u>b.</u> Repeat steps 4 through 11.</p>
13.	Set ESTS PHASE-DEG switch to -90.		
14.	Record ESTS DVM reading.		
15.	Set ESTS PHASE-DEG switch to +90.	Reading will be within + 0.03 Vdc of step 14	<p><u>a.</u> Adjust A1A5C3</p>
16.	Set ESTS DATA SELECT switch to A-DQ.		
17.	Set ESTS PHASE-DEG switch to -180.		
18.	Record ESTS DVM reading.		
19.	Set ESTS PHASE-DEG switch to 0.	Reading will be within + 0.03 Vdc of step 18	<p><u>a.</u> Adjust A1A5C3 to split the difference between A-D1 and A-DQ.</p>
20.	Set ESTS DATA SELECT switch to B-CI.		<p><u>b.</u> Repeat steps 12 through 19.</p>
21.	Set ESTS PHASE-DEG switch to -90.		
22.	Record ESTS DVM reading.		
23.	Set ESTS PHASE-DEG switch to +90.	Reading will be within + 0.03 Vdc of step 22	<p><u>a.</u> Adjust A1A2C3.</p>
24.	Set ESTS DATA SELECT switch to B-CQ.		
25.	Set ESTS PHASE-DEG switch to -180.		

**5-23. FINAL PHASE CHANNEL ALINEMENT - CW - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION
26. 27.	Record ESTS DVM reading Set ESTS PHASE-DEG switch to 0.	Reading will be within $\pm 0.03$ Vdc of step 26	<p>a. Adjust A1A2C3 to split the difference between B-CI and B-CQ.</p> <p>b. Repeat steps 20 through 27.</p>
28.	Set ESTS DATA SELECT switch to A-CI.		
29.	Set ESTS PHASE-DEG switch to -45.	+1.35 $\pm$ 0.02 Vdc on ESTS DVM	Adjust A2A5R5.
30.	Set ESTS PHASE-DEG switch to -135.	+4.05 $\pm$ 0.02 Vdc on ESTS DVM	Adjust A2A5R4.
31.	A2A5R5 and A2A5R4 interact. Repeat steps 29 and 30 as required until no adjustment is necessary.		
32.	Set ESTS DATA SELECT switch to A-CQ.		
33.	Set ESTS PHASE-DEG switch to -45.	+1.35 $\pm$ 0.02 Vdc. 1 ESTS DV'	Adjust A2A5R2.
34.	Set ESTS PHASE-DEG switch to +45.	+4.05 $\pm$ .J2 Vdc on ESTS DVM	Adjust A2A5R3.
35.	A2A5R2 and A2A5R3 interact. Repeat steps 33 and 34 until no adjustment is necessary.		
36.	Set ESTS DATA SELECT switch to A-DI.		
37.	Set ESTS PHASE-DEG switch to -45.	+1.35 $\pm$ 0.02 Vdc on ESTS DVM	Adjust A2A6R5.
38.	Set ESTS PHASE-DEG switch to -135.	+4.05 $\pm$ 0.02 Vdc on ESTS DVM	Adjust A2A6R4.
39.	A2A6R4 and A2A6R5 interact. Repeat steps 37 and 38 as required until no adjustment is necessary.		
40.	Set ESTS DATA SELECT switch to B-CQ.		

**5-23. FINAL PHASE CHANNEL ALINEMENT - CW - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION																				
41.	<p>Set ESTS PHASE-DEG switch to the following positions and verify the ESTS DVM readings + 0.04 Vdc, except as indicated</p> <table border="0"> <thead> <tr> <th style="text-align: center;"><u>Phase</u></th> <th style="text-align: center;"><u>ESTS DVM</u></th> </tr> </thead> <tbody> <tr><td style="text-align: center;">-180</td><td style="text-align: center;">2.70</td></tr> <tr><td style="text-align: center;">-135</td><td style="text-align: center;">1.35</td></tr> <tr><td style="text-align: center;">-90</td><td style="text-align: center;">&lt;1.26</td></tr> <tr><td style="text-align: center;">-45</td><td style="text-align: center;">1.35</td></tr> <tr><td style="text-align: center;">0</td><td style="text-align: center;">2.70</td></tr> <tr><td style="text-align: center;">+45</td><td style="text-align: center;">4.05</td></tr> <tr><td style="text-align: center;">+90</td><td style="text-align: center;">&gt;4.14</td></tr> <tr><td style="text-align: center;">+135</td><td style="text-align: center;">4.05</td></tr> <tr><td style="text-align: center;">+180</td><td style="text-align: center;">2.70</td></tr> </tbody> </table>	<u>Phase</u>	<u>ESTS DVM</u>	-180	2.70	-135	1.35	-90	<1.26	-45	1.35	0	2.70	+45	4.05	+90	>4.14	+135	4.05	+180	2.70		
<u>Phase</u>	<u>ESTS DVM</u>																						
-180	2.70																						
-135	1.35																						
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-45	1.35																						
0	2.70																						
+45	4.05																						
+90	>4.14																						
+135	4.05																						
+180	2.70																						
42.	Set ESTS DATA SELECT switch to A-CQ																						
43.	Repeat step 41.	As specified.																					
44.	Set ESTS DATA-SELECT switch to A-DQ.																						
45.	Repeat Step 41	As specified.																					
46.	Set ESTS DATA SELECT switch to B-CI.																						
47.	<p>Set ESTS PHASE-DEC switch to the following positions and verify the ESTS DVM readings _ 0.04 Vdc, except as indicated</p> <table border="0"> <thead> <tr> <th style="text-align: center;"><u>Phase</u></th> <th style="text-align: center;"><u>ESTS DVM</u></th> </tr> </thead> <tbody> <tr><td style="text-align: center;">-180</td><td style="text-align: center;">&gt;4.14</td></tr> <tr><td style="text-align: center;">-135</td><td style="text-align: center;">4.05</td></tr> <tr><td style="text-align: center;">-90</td><td style="text-align: center;">2.70</td></tr> <tr><td style="text-align: center;">-45</td><td style="text-align: center;">1.35</td></tr> <tr><td style="text-align: center;">0</td><td style="text-align: center;">&lt;1.26</td></tr> <tr><td style="text-align: center;">+45</td><td style="text-align: center;">1.35</td></tr> <tr><td style="text-align: center;">+90</td><td style="text-align: center;">2.70</td></tr> <tr><td style="text-align: center;">+135</td><td style="text-align: center;">4.05</td></tr> <tr><td style="text-align: center;">+180</td><td style="text-align: center;">&gt;4.14</td></tr> </tbody> </table>	<u>Phase</u>	<u>ESTS DVM</u>	-180	>4.14	-135	4.05	-90	2.70	-45	1.35	0	<1.26	+45	1.35	+90	2.70	+135	4.05	+180	>4.14		
<u>Phase</u>	<u>ESTS DVM</u>																						
-180	>4.14																						
-135	4.05																						
-90	2.70																						
-45	1.35																						
0	<1.26																						
+45	1.35																						
+90	2.70																						
+135	4.05																						
+180	>4.14																						
48.	Set ESTS DATA SELECT switch to A-CI.																						

**5-23. FINAL PHASE CHANNEL ALINEMENT - CW - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION
49.	Repeat step 47.	As specified	
50.	Set ESTS DATA SELECT switch to A-DI.		
51.	Repeat step 47.	As specified	
52.	Set ESTS DATA SELECT switch to A-DQ.		
53.	Set ESTS PHASE-DEG switch to -45.	+1.35 ± 0.02 Vdc on ESTS DVM	Adjust A2A6R2.
54.	Set ESTS PHASE-DEG switch to +45.	+4.05 ± 0.02 Vdc on ESTS DVM	Adjust A2A6R3.
55.	A2A6R2 and A2A6R3 interact. Repeat steps 53 and 54 as required until no adjustment is necessary.		
56.	Set ESTS PHASE-DEG switch to the following positions and verify the ESTS DVM readings +/- 0.04 Vdc, except as indicated.		
	<u>Phase</u>	<u>ESTS DVM</u>	
	-180	2.70	
	-135	1.35	
	-90	<1.26	
	-45	1.35	
	0	2.70	
	+45	4.05	
	+90	>4.14	
	+135	4.05	
	+180	2.70	
57.	Set ESTS DATA SELECT switch to B-CI.		
58.	Set ESTS PHASE-DEG switch to -45.	+1.35 ± 0.02 Vdc on ESTS DVM	Adjust A2A7R5.
59.	Set ESTS PHASE-DEG switch to +45.	+4.05 ± 0.02 Vdc on ESTS DVM	Adjust A2A7R4.
60.	A2A7R4 and A2A7R5 interact. Repeat steps 58 and 59 as required until no adjustment is necessary.		
		<b>5-98</b>	

**5-23. FINAL PHASE CHANNEL ALINEMENT - CW - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION
61.	Set ESTS PHASE-DEG switch to the following positions and verify the ESTS DVM readings + 0.04 Vdc, except as indicated	<u>ESTS DVM</u>	
	<u>Phase</u>		
	-180	>4.14	
	-135	4.05	
	-90	2.70	
	-45	1.35	
	0	<1.26	
	+45	1.35	
	+90	2.70	
	+135	4.05	
	+180	>4.14	
62.	Set ESTS DATA SELECT switch to B-CQ		
63.	Set ESTS PHASE-DEG switch to -45.	+1.35 + 0.02 Vdc on ESTS DVM	Adjust A2A7R2.
64.	Set ESTS PHASE-DEG switch to +45. ESTS DVM	+4.05 + 0.02 Vdc on	Adjust A2A7R3.
65.	A2A7R2 and A2A7R3 interact. Repeat steps 63 and 64 as required until no adjustment is necessary.		
66.	Set ESTS PHASE-DEG switch to the following positions and verify the ESTS DVM readings ±0.04 Vdc, except as indicated	<u>ESTS DVM</u>	
	<u>Phase</u>		
	-180	2.70	
	-135	1.35	
	-90	<1.26	
	-45	1.35	
	0	2.70	
	+45	4.05	
	+90	>4.14	
	+135	4.05	
	+180	2.70	
		<b>5-99</b>	

**5-24. FINAL FRU CHANNEL ALINEMENT - CW**

STEP	PROCEDURE	INDICATIONS	ACTION																																										
1. 2.	Connect test equipment (fig. 5-1). Install alinement cover in place of right side cover (para 5-30).																																												
	<b>NOTE</b>																																												
	Ensure equipment warms up at least 45 minutes before making adjustments.																																												
3.	On ESTS, set:  <table border="0" style="width: 100%;"> <thead> <tr> <th style="text-align: left;"><u>Switch</u></th> <th style="text-align: left;"><u>Set to</u></th> </tr> </thead> <tbody> <tr><td>USB/LSB</td><td>LSB</td></tr> <tr><td>SSB OFFSET</td><td>0</td></tr> <tr><td>DVM SEL</td><td>VOLTS</td></tr> <tr><td>AT1</td><td>10</td></tr> <tr><td>AT2</td><td>cf</td></tr> <tr><td>MOD/PW</td><td>CW</td></tr> <tr><td>PW SET</td><td>full cw</td></tr> <tr><td>TRIG SEL</td><td>ST TRIGI</td></tr> <tr><td>PW RST</td><td></td></tr> <tr><td>EXTTHRESH</td><td>OFF</td></tr> <tr><td>EXT THRESH</td><td></td></tr> <tr><td>ADJ</td><td>full cw</td></tr> <tr><td>SWEEP</td><td>OFF</td></tr> <tr><td>BAND CMD</td><td>LB</td></tr> <tr><td>BW CMD</td><td>30 MHz</td></tr> <tr><td>PHASE-DEG</td><td>0</td></tr> <tr><td>BIT TEST</td><td>OFF</td></tr> <tr><td>PRF</td><td>10 KHz</td></tr> <tr><td>DATA SELECT</td><td>FRUQ</td></tr> <tr><td>POWER</td><td>ON</td></tr> </tbody> </table>	<u>Switch</u>	<u>Set to</u>	USB/LSB	LSB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	10	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIGI	PW RST		EXTTHRESH	OFF	EXT THRESH		ADJ	full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	PHASE-DEG	0	BIT TEST	OFF	PRF	10 KHz	DATA SELECT	FRUQ	POWER	ON		
<u>Switch</u>	<u>Set to</u>																																												
USB/LSB	LSB																																												
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BIT TEST	OFF																																												
PRF	10 KHz																																												
DATA SELECT	FRUQ																																												
POWER	ON																																												
4.	Set ESTS IF FREQ MHZ switch to 145.0.	+1.35 _ 0.02 Vdc on ESTS DVM	Adjust A2A8R2.																																										
5.	Set ESTS IF FREQ MHZ switch to 135.0.	+4.05 + 0.02 Vdc on ESTS DVM	Adjust A2A8R3.																																										
6.	A2A8R2 and A2A8R3 interact. Repeat steps 4 and 5 as required until no adjustment is necessary.																																												
		<b>5-100</b>																																											



**5-24. FINAL FRU CHANNEL ALINEMENT - CW - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION
7.	Set ESTS IF FREQ MHZ switch to the following positions and verify the ESTS DVM readings $\pm 0.02$ Vdc, except as indicated.	<u>ESTS DVM</u>	
	<u>Frequency</u>		
	135.0	4.05	
	140.0	2.70	
	145.0	1.35	
	150.0	<0.95	
	155.0	1.35	
	160.0	2.70	
	165.0	4.04	
8.	Set ESTS DATA SELECT switch to FRUI.		
9.	Set ESTS IF FREQ MHZ switch to 155.0.	+1.35 $\pm 0.02$ Vdc on ESTS DVM	Adjust A2A8R5.
10.	Set ESTS IF FREQ MHZ switch to 145.0.	+4.05 $\pm 0.02$ Vdc on ESTS DVM	Adjust A2A8R4.
11.	A2A8R4 and A2A8R5 interact. Repeat steps 9 and 10 as required until no adjustment is necessary.		
12.	Set ESTS IF FREQ MHZ switch to the following positions and verify the ESTS DVM readings $\pm 0.02$ Vdc, except as indicated.	<u>ESTS DVM</u>	
	<u>Frequency</u>		
	135.0	>3.40	
	140.0	>4.44	
	145.0	4.05	
	150.0	2.70	
	155.0	1.35	
	160.0	<0.95	
	165.0	<1.75	
		<b>5-101</b>	

**5-25. FINAL DF LOG AMPLITUDE ALINEMENT - CW**

STEP	PROCEDURE	INDICATIONS	ACTION																																								
1.	Connect test equipment (fig. 5-1).																																										
2.	Install alinement cover in place of right side cover (para 5-30).																																										
<b>NOTE</b>																																											
Ensure equipment warms up at least 45 minutes before making adjustments.																																											
3.	<p>On ESTS, set:</p> <table border="0"> <tr> <td><u>Switch</u></td> <td><u>Set to</u></td> </tr> <tr> <td>IF FREQ MHZ</td> <td>150.0</td> </tr> <tr> <td>USB/LSB</td> <td>LSB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/ PW RST</td> </tr> <tr> <td>EXTTHRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PRF</td> <td>10 KHz</td> </tr> <tr> <td>DATA SELECT</td> <td>LOG</td> </tr> <tr> <td>POWER</td> <td>ON</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHZ	150.0	USB/LSB	LSB	SSB OFFSET	0	DVM SEL	VOLTS	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIG/ PW RST	EXTTHRESH	OFF	EXT THRESH		ADJ	full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	PHASE-DEG	0	BIT TEST	OFF	PRF	10 KHz	DATA SELECT	LOG	POWER	ON		
<u>Switch</u>	<u>Set to</u>																																										
IF FREQ MHZ	150.0																																										
USB/LSB	LSB																																										
SSB OFFSET	0																																										
DVM SEL	VOLTS																																										
AT2	cf																																										
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BAND CMD	LB																																										
BW CMD	30 MHz																																										
PHASE-DEG	0																																										
BIT TEST	OFF																																										
PRF	10 KHz																																										
DATA SELECT	LOG																																										
POWER	ON																																										
4.	Set ESTS AT1 to 50.	+1.25 + 0.02 Vdc on ESTS DVM	Adjust A2A11 R5.																																								
5.	Set ESTS AT1 to 10.		Adjust A2A11R4.																																								
6.	A2A11 R4 and A2A11 R5 interact. Repeat steps 4 and 5 as required until no adjustment is necessary.																																										
<b>5-102</b>																																											

**5-25. FINAL DF LOG AMPLITUDE ALINEMENT - CW - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION
7.	<p>Set ESTS AT1 to the following positions and verify the ESTS DVM readings + 0.02 Vdc.</p> <p style="text-align: center;"><u>AT1</u></p> <p style="text-align: center;">60 50 40 30 20 10 0</p>	<p style="text-align: center;"><u>ESTS DVM</u></p> <p style="text-align: center;">0.50 1.25 2.00 2.75 3.50 4.25 5.00</p>	
8.	<p>Set ESTS USB/LSB switch to USB.</p>		
9.	<p>Repeat step 7</p>	<p>As specified.</p>	

**5-26. CONFIRM LOGIC DF/TRIGGER LOG AMPLITUDE BALANCE - CW**

STEP	PROCEDURE	INDICATIONS	ACTION																																																																																				
1. 2.	Connect test equipment (fig. 5-1). Install alignment cover in place of right side cover (para 5-30)																																																																																						
	<p style="text-align: center;"><b>NOTE</b></p> Ensure equipment warms up at least 45 minutes before making adjustments.																																																																																						
3.	On ESTS, set: <table border="0" style="width: 100%;"> <tr> <td style="width: 15%;"><u>Switch</u></td> <td style="width: 10%;"></td> <td style="width: 15%;"><u>Set to</u></td> <td></td> </tr> <tr> <td>IF FREQ MHZ</td> <td></td> <td>150.0</td> <td></td> </tr> <tr> <td>USB/LSB</td> <td></td> <td>USB</td> <td></td> </tr> <tr> <td>SSB OFFSET</td> <td></td> <td>0</td> <td></td> </tr> <tr> <td>DVM SEL</td> <td></td> <td>VOLTS</td> <td></td> </tr> <tr> <td>AT1</td> <td></td> <td>30</td> <td></td> </tr> <tr> <td>AT2</td> <td></td> <td>cf</td> <td></td> </tr> <tr> <td>MOD/PW</td> <td></td> <td>CW</td> <td></td> </tr> <tr> <td>PW SET</td> <td></td> <td>full cw</td> <td></td> </tr> <tr> <td>TRIG SEL</td> <td></td> <td>ST TRIG/ PW RST</td> <td></td> </tr> <tr> <td>EXTTHRESH</td> <td></td> <td>OFF</td> <td></td> </tr> <tr> <td>EXT THRESH</td> <td></td> <td></td> <td></td> </tr> <tr> <td>ADJ</td> <td></td> <td>full cw</td> <td></td> </tr> <tr> <td>SWEEP</td> <td></td> <td>OFF</td> <td></td> </tr> <tr> <td>BAND CMD</td> <td></td> <td>LB</td> <td></td> </tr> <tr> <td>BW CMD</td> <td></td> <td>30 MHz</td> <td></td> </tr> <tr> <td>PHASE-DEG</td> <td></td> <td>0</td> <td></td> </tr> <tr> <td>BIT TEST</td> <td></td> <td>OFF</td> <td></td> </tr> <tr> <td>PRF</td> <td></td> <td>10 KHz</td> <td></td> </tr> <tr> <td>DATA SELECT</td> <td></td> <td>LOG</td> <td></td> </tr> <tr> <td>POWER</td> <td></td> <td>ON</td> <td></td> </tr> </table>	<u>Switch</u>		<u>Set to</u>		IF FREQ MHZ		150.0		USB/LSB		USB		SSB OFFSET		0		DVM SEL		VOLTS		AT1		30		AT2		cf		MOD/PW		CW		PW SET		full cw		TRIG SEL		ST TRIG/ PW RST		EXTTHRESH		OFF		EXT THRESH				ADJ		full cw		SWEEP		OFF		BAND CMD		LB		BW CMD		30 MHz		PHASE-DEG		0		BIT TEST		OFF		PRF		10 KHz		DATA SELECT		LOG		POWER		ON			
<u>Switch</u>		<u>Set to</u>																																																																																					
IF FREQ MHZ		150.0																																																																																					
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PRF		10 KHz																																																																																					
DATA SELECT		LOG																																																																																					
POWER		ON																																																																																					
4.	Disconnect W6 from ESTS and IFP. Connect W6 between rf output of signal generator and VVM.																																																																																						
5.	Set rf signal generator to 150.0 + 0.05 MHz.																																																																																						
6.	Adjust output level of signal generator for $-30 \pm 0.5$ dBm on VVM.																																																																																						
		<b>5-104</b>																																																																																					

**5-26. CONFIRM LOGIC DF/TRIGGER LOG AMPLITUDE BALANCE - CW - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION
7.	Compare the VVM dBm reading with the generator power output reading.	The readings will be within + 2 dB of each other; record difference	
8.	Disconnect W6 from the VVM and connect it to IFP J6.		
9.	Decrease generator output until ESTS ST TRIG lamp goes out. step 7.	Generator output will be -43 dBm minus the difference recorded in	Adjust A2A9R7 to obtain correct results.
10.	Set generator output to -30 dBm.	ESTS ST TRIG lamp will be on	
11.	Increase generator output until ESTS ST TRIG lamp goes out.	Generator output will be -17 dBm minus the difference recorded in step 7.	Adjust A2A9R7 to obtain correct results.
12.	Set generator output to -30 dBm.	ESTS ST TRIG lamp will on	
13.	Repeat steps 9 through 12 until no adjustment is necessary.	As specified	
14.	Set ESTS USB/LSB switch to LSB.		
15.	Set generator output to -30 dBm.	ESTS ST TRIG lamp will be on	Adjust A2A9R26 to obtain correct results.
16.	Repeat steps 9 through 12 as required.	As specified correct results.	Adjust A2A9R26 to obtain

**5-27. CONFIRM LOGIC DF/TRIGGER COARSE FRU BALANCE - CW**

STEP	PROCEDURE	INDICATIONS	ACTION																																								
1.	Connect test equipment (fig. 5-1).																																										
2.	Install alinement cover in place of right side cover (para 5-30).																																										
<b>NOTE</b>																																											
Ensure equipment warms up at least 45 minutes before making adjustments.																																											
3.	<p>On ESTS, set:</p> <table border="0" style="width: 100%;"> <tr> <td style="width: 50%;"><u>Switch</u></td> <td style="width: 50%;"><u>Set to</u></td> </tr> <tr> <td>USB/LSB</td> <td>USB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/ PW RST</td> </tr> <tr> <td>EXT THRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>RW CMD</td> <td>30 MHz</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PRFI</td> <td>10 kHz</td> </tr> <tr> <td>DATA SELECT</td> <td>LOG</td> </tr> <tr> <td>POWER</td> <td>ON</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	USB/LSB	USB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	30	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIG/ PW RST	EXT THRESH	OFF	EXT THRESH		ADJ	full cw	SWEEP	OFF	BAND CMD	LB	RW CMD	30 MHz	PHASE-DEG	0	BIT TEST	OFF	PRFI	10 kHz	DATA SELECT	LOG	POWER	ON		
<u>Switch</u>	<u>Set to</u>																																										
USB/LSB	USB																																										
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RW CMD	30 MHz																																										
PHASE-DEG	0																																										
BIT TEST	OFF																																										
PRFI	10 kHz																																										
DATA SELECT	LOG																																										
POWER	ON																																										
4.	Set ESTS IF FREQ MHZ switch to 166.0.																																										
5.	Observe ESTS ST TRIG and PW RST lamps.	Both will be glowing with equal intensity	Adjust A2A11 R3 for equal intensity on lamps.																																								
6.	Set ESITS IF FREQ MHZ switch to 134.0.																																										
7.	Observe ESTS ST TRIG and PW RST lamps.	Both will be glowing with equal intensity	Adjust A2A11 R2 for equal intensity on lamps.																																								
<b>5-106</b>																																											

**5-27. CONFIRM LOGIC DFITRIGGER COARSE FRU BALANCE - CW - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION
8.	A2A11 R3 and A2A11 R2 interact. Repeat steps 4 through 7 as required until no adjustment is necessary.		
9.	Set ESTS IF FREQ MHZ switch to 150.0.		
10.	Disconnect W6 from ESTS. Connect to output of rf signal generator.		
11.	Set generator for 150.0 ± 0.5 MHz, -30 ± 2 dBm.		
12.	Decrease frequency of generator until ESTS ST TRIG and PW RST lamps glow with equal intensity.	Frequency will be lower than 138 MHz	Adjust A2A1 OR5 for equal intensity on lamps.
13.	Increase frequency of generator beyond 150 MHz until ESTS ST TRIG and PW RST lamps glow with equal intensity.	Frequency will be higher than 162 MHz	Adjust A2A10OR4 for equal intensity on lamps.
14.	Repeat steps 11 through 13 as required until no adjustment is necessary.	As specified	
15.	Set ESTS USB/LSB switch to LSB.		
16.	Repeat steps 11 through 13 as required adjusting A2A10R2 (138 MHz) and A2A10R3 (162 MHz) until no adjustment is necessary.	As specified	

**5-28. OUTOF-BAND ALINEMENT-CW**

STEP	PROCEDURE	INDICATIONS	ACTION																																										
1.	Connect test equipment (fig. 5-1).																																												
2.	Install alignment cover in place of right side cover (para 5-30).																																												
	<p><b>NOTE</b></p> <p>Ensure equipment warms up at least 45 minutes before making adjustments.</p>																																												
3.	<p>On ESTS, set:</p> <table border="0"> <tr> <td><u>Switch</u></td> <td><u>Set to</u></td> </tr> <tr> <td>IF FREQ MHZ</td> <td>150.0</td> </tr> <tr> <td>USB/LSB</td> <td>LSB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MODIPW</td> <td>CW</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIG/ PW RST</td> </tr> <tr> <td>EXTTHRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>BIT TEST</td> <td>OFF</td> </tr> <tr> <td>PRF</td> <td>10 KHz</td> </tr> <tr> <td>DATA SELECT</td> <td>LOG</td> </tr> <tr> <td>POWER</td> <td>ON</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHZ	150.0	USB/LSB	LSB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	30	AT2	cf	MODIPW	CW	PW SET	full cw	TRIG SEL	ST TRIG/ PW RST	EXTTHRESH	OFF	EXT THRESH		ADJ	full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	PHASE-DEG	0	BIT TEST	OFF	PRF	10 KHz	DATA SELECT	LOG	POWER	ON		
<u>Switch</u>	<u>Set to</u>																																												
IF FREQ MHZ	150.0																																												
USB/LSB	LSB																																												
SSB OFFSET	0																																												
DVM SEL	VOLTS																																												
AT1	30																																												
AT2	cf																																												
MODIPW	CW																																												
PW SET	full cw																																												
TRIG SEL	ST TRIG/ PW RST																																												
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PHASE-DEG	0																																												
BIT TEST	OFF																																												
PRF	10 KHz																																												
DATA SELECT	LOG																																												
POWER	ON																																												
4.	Disconnect W8 from ESTS and IFP. Connect W8 between rf signal generator output and VVM input.																																												
5.	Set generator to 180 +/- 0.05 1,Hz. Adjust generator output for -30 + 0.5 dBm on VVM.	Difference between VVM reading and generator output will be less than 1 dB; record difference.																																											
	<b>5-108</b>																																												



**5-28. OUT-OF-BAND ALINEMENT - CW - Continued**

STEP	PROCEDURE	INDICATIONS	ACTION
6.	Disconnect W8 from VVM. Connect W8 to IFP J9.	ESTS ST TRIG lamp will go out	
7.	Decrease generator output until ST TRIG lamp goes on. difference recorded in step 5 $\pm$ 2.5 dB	Generator output will be -37 dBm minus the	Adjust A1A11 R5 to obtain proper results.
8.	Set generator output to - 30 dBm.	ESTS ST TRIG lamp will be off	
9.	Increase generator output until ST TRIG lamp goes on. difference recorded in step 5 $\pm$ 2.5 dB	Generator output will be -23 dBm minus the	Adjust A1 A11 R5 to obtain proper results.
10.	Set generator output to - 30 dBm.	ESTS ST TRIG lamp will be off	
11.	Repeat steps 7 through 10 as required until no adjustment is necessary.		

**5-29. BIT OSCILLATOR ALINEMENT**

STEP	PROCEDURE	INDICATIONS	ACTION																																												
1.	Connect test equipment (fig. 5-1).																																														
2.	Install alinement cover in place of right side cover (para 5-30).																																														
<b>NOTE</b>																																															
Ensure equipment warms up at least 45 minutes before making adjustments.																																															
3.	<p>On ESTS, set:</p> <table border="0"> <tr> <td><u>Switch</u></td> <td><u>Set to</u></td> </tr> <tr> <td>IF FREQ MHZ</td> <td>150.0</td> </tr> <tr> <td>USB/LSB</td> <td>LSB</td> </tr> <tr> <td>SSB OFFSET</td> <td>0</td> </tr> <tr> <td>DVM SEL</td> <td>VOLTS</td> </tr> <tr> <td>AT1</td> <td>30</td> </tr> <tr> <td>AT2</td> <td>cf</td> </tr> <tr> <td>MOD/PW</td> <td>CW</td> </tr> <tr> <td>PW SET</td> <td>full cw</td> </tr> <tr> <td>TRIG SEL</td> <td>ST TRIGI</td> </tr> <tr> <td></td> <td>PW RST</td> </tr> <tr> <td>EXTTHRESH</td> <td>OFF</td> </tr> <tr> <td>EXT THRESH</td> <td></td> </tr> <tr> <td>ADJ</td> <td>full cw</td> </tr> <tr> <td>SWEEP</td> <td>OFF</td> </tr> <tr> <td>BAND CMD</td> <td>LB</td> </tr> <tr> <td>BW CMD</td> <td>30 MHz</td> </tr> <tr> <td>PHASE-DEG</td> <td>0</td> </tr> <tr> <td>BIT TEST</td> <td>LSB</td> </tr> <tr> <td>PRF</td> <td>10 kHz</td> </tr> <tr> <td>DATA SELECT</td> <td>LOG</td> </tr> <tr> <td>POWER</td> <td>ON</td> </tr> </table>	<u>Switch</u>	<u>Set to</u>	IF FREQ MHZ	150.0	USB/LSB	LSB	SSB OFFSET	0	DVM SEL	VOLTS	AT1	30	AT2	cf	MOD/PW	CW	PW SET	full cw	TRIG SEL	ST TRIGI		PW RST	EXTTHRESH	OFF	EXT THRESH		ADJ	full cw	SWEEP	OFF	BAND CMD	LB	BW CMD	30 MHz	PHASE-DEG	0	BIT TEST	LSB	PRF	10 kHz	DATA SELECT	LOG	POWER	ON		
<u>Switch</u>	<u>Set to</u>																																														
IF FREQ MHZ	150.0																																														
USB/LSB	LSB																																														
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EXTTHRESH	OFF																																														
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BAND CMD	LB																																														
BW CMD	30 MHz																																														
PHASE-DEG	0																																														
BIT TEST	LSB																																														
PRF	10 kHz																																														
DATA SELECT	LOG																																														
POWER	ON																																														
4.	Connect frequency counter to IFP J10.	150.0 = 0.01 MHz	Adjust A1 A3Y1 to obtain proper results.																																												
5.	Disconnect frequency counter from IFP. Connect rf power meter to IFP J10.	-24 + 3.5 dBm																																													
		<b>5-110</b>																																													

5-29. BIT OSCILLATOR ALINEMENT - Continued

STEP	PROCEDURE	INDICATIONS	ACTION
6.	<p>Set the ESTS DATA SELECT switch to the following positions and verify the voltages given.</p> <p style="text-align: center;"><u>DATA SELECT</u></p> <p>B-CQ                      A-CQ                      A-DQ                      B-CI                      A-CI                      A-DI                      FRUI                      FRUQ                      LOG</p>	<p style="text-align: center;"><u>Meter</u></p> <p>2.70 + 0.24                      2.70 ± 0.24                      2.70 + 0.24                      &lt;1.44                      &lt;1.44                      &lt;1.44                      2.7 ± 0.20                      &lt;1.44                      2.53 + 0.49</p>	<p>a. Replace A1A3.</p> <p>b. Send IFP to higher level maintenance.</p>

## Section III. MAINTENANCE

## 5-30. SIDE COVERS

## NOTE

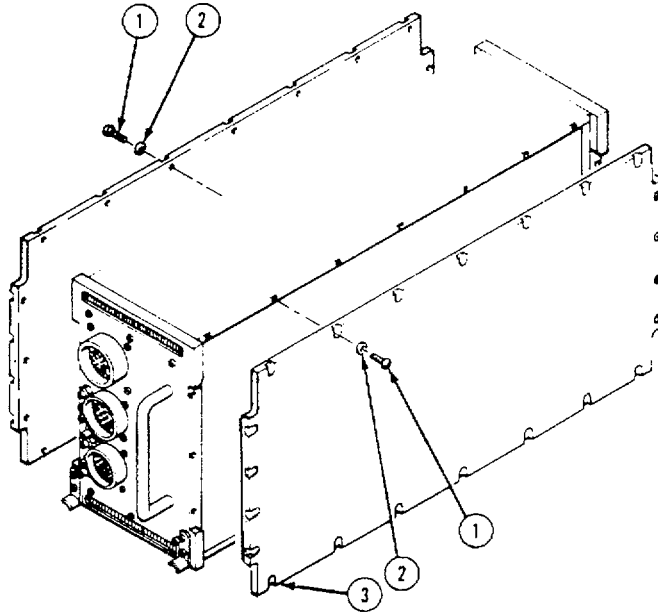
Procedure is the same for right and left cover.

- a. Preliminary Procedure. Turn power off.
- b. Removal.

## NOTE

If helicoil is stripped, replace helicoil insert (para 5-27).

- (1) Remove 22 screws (1) and washers (2).
- (2) Remove cover (3).



- c. Installation.
  - (1) Place cover (3) in installed position.
  - (2) Install 22 screws (1) and washers (2).
- d. Follow-on Procedure. Perform test (para 5-5, 5-6, 5-7).

**5-31. MODULE A1A1 THROUGH A1A11****NOTE**

Procedure is the same for modules A1A1 through A1A11, except where noted.

**a. Preliminary Procedures.**

- (1) Turn power off.
- (2) Remove right side cover (para 5-30).

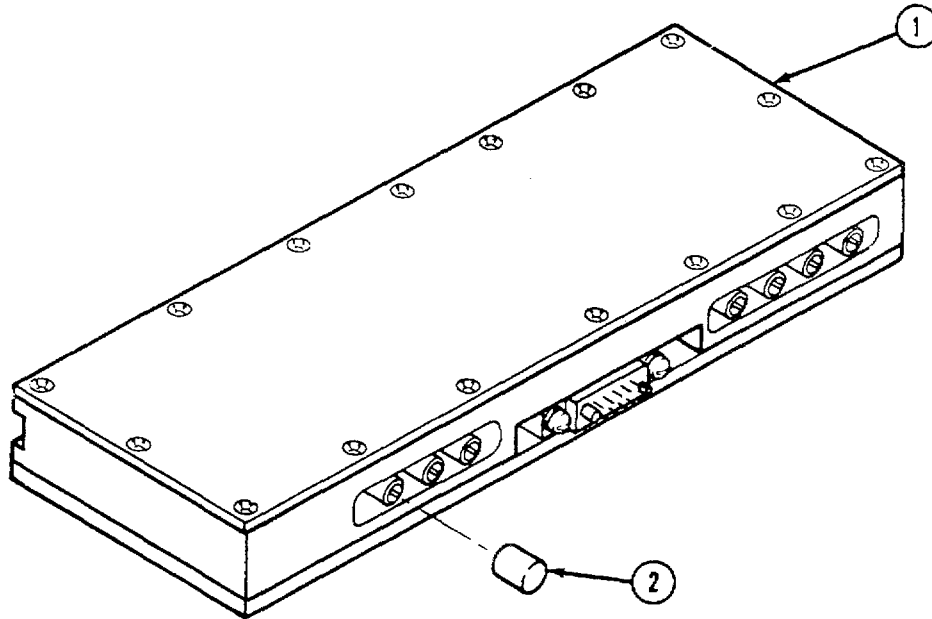
**b. Removal.****CAUTION**

Do not touch center adjustment screw on A1A3 when removing modules. Altering this factory adjustment may harm IFP performance.

- (1) Loosen two captive screws (1).
- (2) Remove module (2).

**5-31. MODULE AA1 THROUGH A1A11 - Continued**

- (3) If replacement module (1), note and record location of terminations (2) on module to aid in installation.
- (4) Remove terminations (2) from module (1).

**c. Installation.****NOTES**

If terminations were not removed from module, go to step (2).

Module termination locations are indicated in FO-4.

- (1) Install terminations (2) on module (1) as recorded during removal procedure.

**5-31. MODULE A1A1 THROUGH A1A1 - Continued****CAUTION**

Ensure that backplane connector is not blocked or terminations on A1A1, A1A2, A1A4, A1A5, and A1A11 may damage nearby connector backshells.

**NOTE**

It may be necessary to remove modules A1A12 and A1A13 (para 5-26) in order to clear blocked backplane connector.

(2) Carefully place module (2) in installed position.

(3) Tighten two captive screws (1).

d. Follow-on Procedures.

(1) If removed, install module A1A12, and A1A13 (para 5-33).

(2) Perform alinement (para 5-8) or test procedure (para 5-7), as required.

(3) Install right side cover (para 5-30).

**5-32. CIRCUIT CARD A2A1 THROUGH A2A11****NOTE**

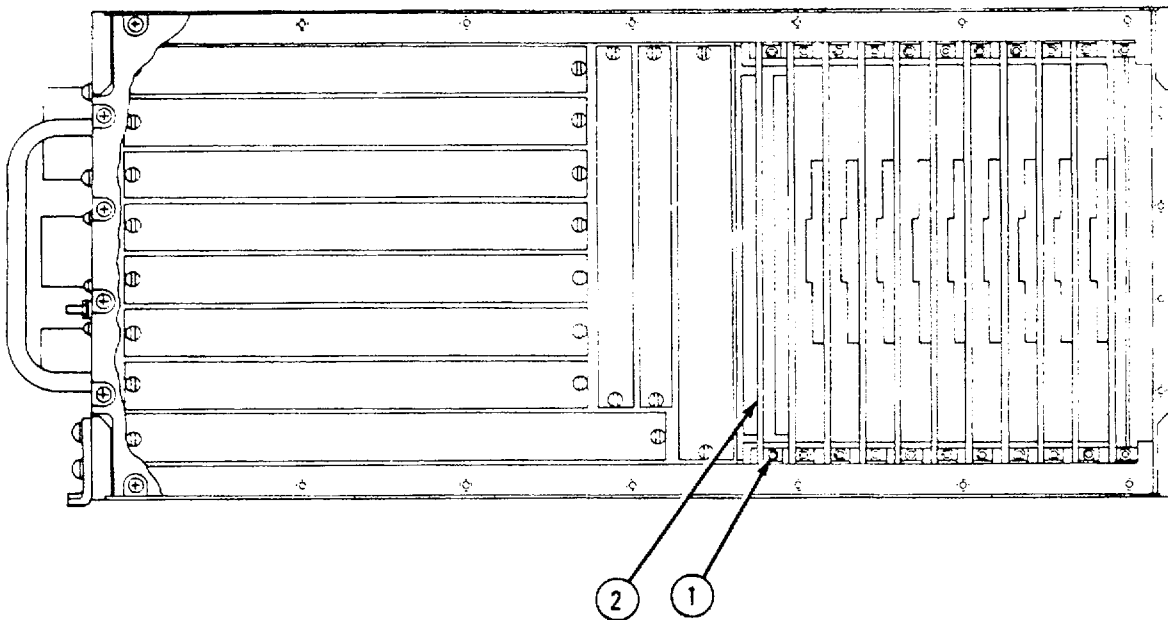
Procedure is same for circuit cards A2A1 through A2A11.

**a. Preliminary Procedures.**

- (1) Turn power off.
- (2) Remove right side cover (para 5-30).

**b. Removal.**

- (1) Loosen captive screws (1).
- (2) Using card extractor, remove circuit card (2).

**c. Installation.**

- (1) Place circuit card (2) in installed position.
- (2) Tighten two captive screws (1).

**d. Follow-on Procedures.**

- (1) Perform alinement (para 5-8) or test procedure (para 5-7), as required.
- (2) Install right side cover (para 5-30).



**5-33. MODULE A1A12 AND A1A13****NOTE**

Procedure is same for module A1A12 and A1A13.

a. Preliminary Procedures.

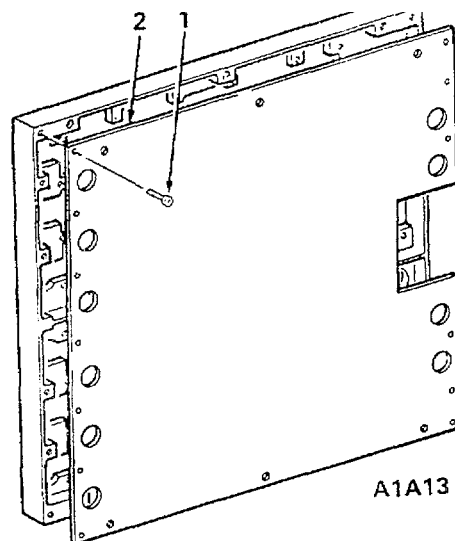
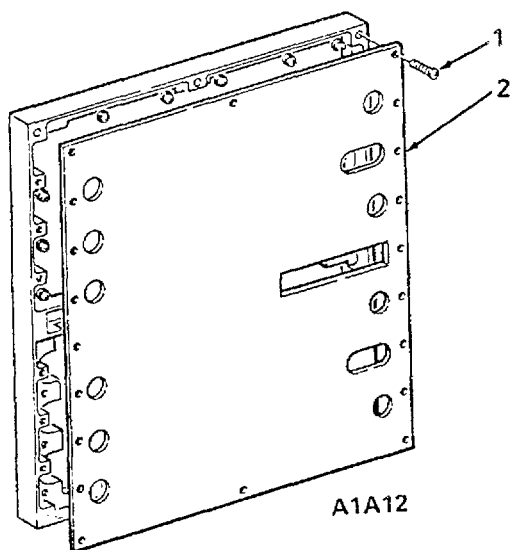
- (1) Turn power off.
- (2) Remove left side cover (para 5-30).

b. Removal.

- (1) Remove six screws (1).
- (2) Using circuit card extender, remove module A1A12 (3) and A1A13 (2).

**5-33. MODULE A1A12 AND A1A13- Continued****c. Disassembly**

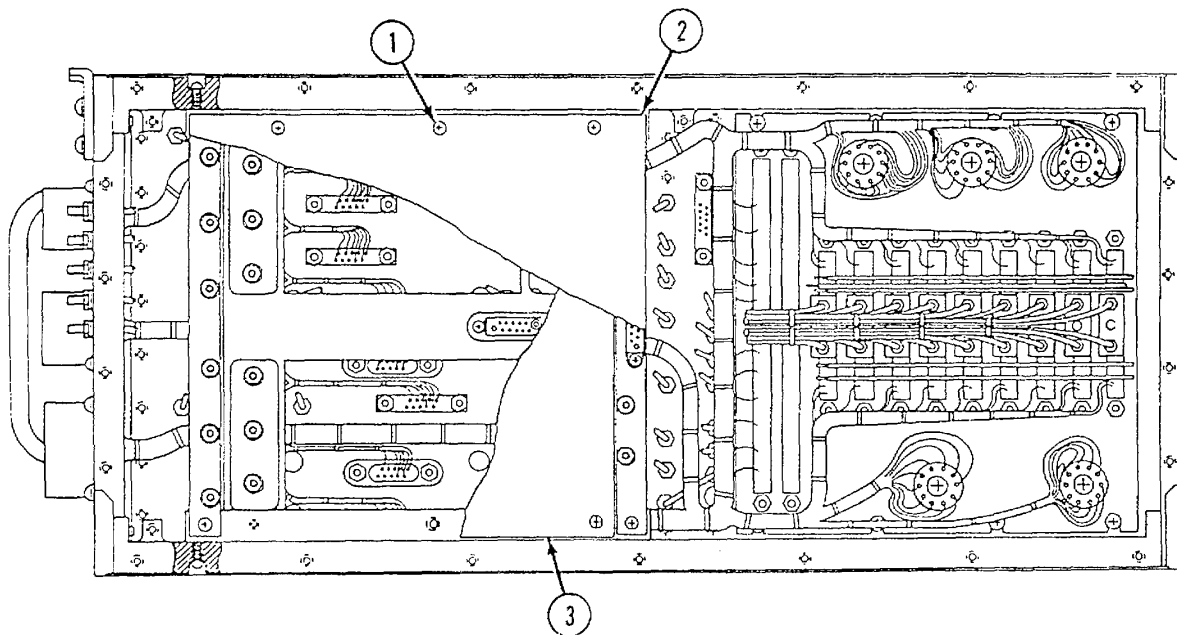
- (1) Disassemble module A1A12 by removing 14 screws (1) and removing cover (2).
- (2) Disassembly module A1A13 by removing 13 screws (1) and removing cover (2).

**d. Assembly**

- (1) Assembly module A1A12 by installing cover (2) and securing using 14 screws (1).
- (2) Assemble module A1A13 by installing cover (2) and securing using 13 screws (1).

**5-33. MODULE A1A12 AND A1A13-Continued****e. Installation.**

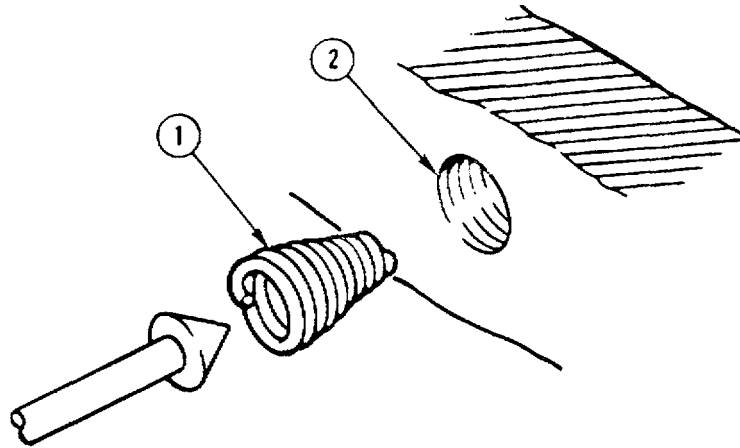
- (1) Place module A1A13 (2) and A1A12 (3) in installed position.
- (2) Install six screws (1). Torque to 6-8 inch/pounds.

**f. Follow-on Procedures.**

- (1) Perform alignment (para 5-8) or test procedure (para 5-7), as required.
- (2) Install left side cover (para 5-30).

**5-34 HELICOIL INSERTS**a. Removal.

- (1) Using removal tool, press and turn insert (1) counterclockwise.
- (2) Remove insert (1). If insert cannot be removed, go to step (3).
- (3) Using scribe, pry top thread of insert (1) away from housing hole (2).
- (4) Using needle-nose pliers, turn insert (1) counterclockwise.
- (5) Remove insert (1).



**5-34. HELICOIL INSERTS - Continued**b. Installation.**WARNING**

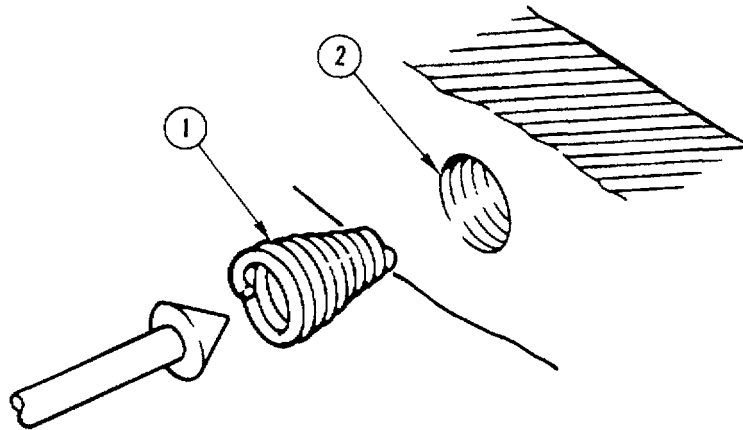
Isopropyl alcohol is flammable and moderately toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate.

- (1) Using pipe cleaner or swab, and isopropyl alcohol, clean housing hole (2).
- (2) Place new insert (1) on insertion tool.

**WARNING**

Zinc chromate dust primer is highly toxic to eyes, skin, and respiratory tract. Eye and skin protection required. Good general ventilation is normally adequate.

- (3) Coat insert (1) with zinc chromate dust primer.

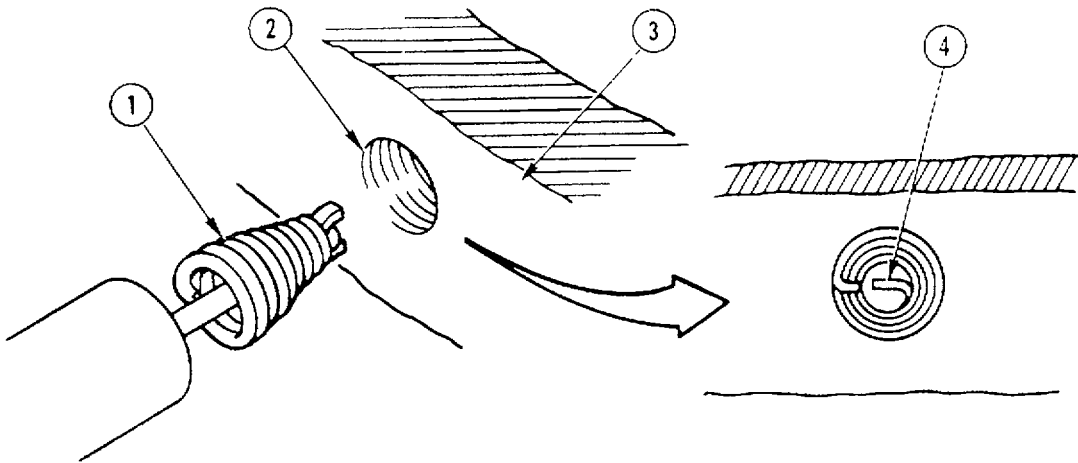


## 5-34. HELICOIL INSERTS - Continued

## NOTE

Top thread of insert should be below housing surface between  $1/4$  and  $1 - 1/2$  turns.

- (4) Using insertion tool, install insert (1) in housing hole (2) as follows:
  - (a) Aline insert threads with hole threads.
  - (b) Press insertion tool outer housing against hole housing (3).
  - (c) Turn insertion tool clockwise to thread insert into hole within limits given.
- (5) Ensure insert (1) is between  $1/4$  and  $1 - 1/2$  turns below housing surface.
  - (a) If insert is installed within limits given, go to step (6).
  - (b) If insert is not installed within limits given, replace insert.
- (6) Using tang removal tool, press and remove insert tang (4) from bottom of insert (1)
- (7) Allow zinc chromate dust primer one hour to cure.



- c. Follow-on Procedure. Install side cover (para 5-30).

**Section IV. PREPARATION FOR STORAGE OR SHIPMENT****5-35. STORAGE FACILITIES**

- a. Security of the stored equipment is required. The area used for storage must protect the equipment from being stolen.
- b. The equipment in storage must be protected from the weather. Covered storage is required.

**5-36. PROCEDURES**

- a. The equipment to be stored must be in good working order. Perform an operational check on the equipment prior to storage (para 5-7).
- b. When putting the equipment into administrative storage (1-45 days) use a storage area that is accessible. Equipment in administrative storage must be able to be removed from storage and put into operation on 24 hour notice.

**APPENDIX A  
REFERENCES**

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**A-1. SCOPE**

This appendix lists all forms, field manuals, technical manuals, and miscellaneous publications referenced in this manual. Only those publications available to, and required by the user are listed.

**A-2. FORMS**

Recommended Changes to Publications .....	DA Form 2028,
and Blank Forms .....	DA Form 2028-2
Report of Discrepancy (ROD) .....	SF 364
Discrepancy in Shipment Report (DISREP) .....	SF 361
Quality Deficiency Report   SF 368	

**A-3. FIELD MANUALS**

First Aid and Safety .....	FM 21-11
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**A-4. TECHNICAL MANUALS**

Operator's, Organizational, and Direct .....	TM 11-5821-332-13
Support Maintenance Manual for	
Airborne Relay Facility AN/ARW-83(V)6	
Operator's, Organizational, and Direct Support.....	TM 11-5895-1280-13
. Maintenance manual for Power Supply,	
. Receiver PP-8184/U	
Organizational and Direct Support .....	TM 11-5895-1284-23P
. Repair Parts and Special Tools	
. List for Processor, Intermediate	
. Frequency CV-4008/U	
Operator's, Organizational, and Direct .....	TM 11-6625-3149-13
. Support Maintenance Manual for	
. Test Set, Electronic System TS-42391U	

**A-5. MISCELLANEOUS PUBLICATIONS**

The Army Maintenance Management System .....	DA Pam 738-750
Consolidated Index of Army Publication.....	DA Pam 25-30
and Blank Forms	
Procedures for Destruction of Electronics .....	TM 750-244-2
Materiel to Prevent Enemy Use (Electronics Command)	



**APPENDIX B  
MAINTENANCE ALLOCATION CHART (MAC)**

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**Section I. INTRODUCTION**

**B-1. The Army Maintenance System Mac**

a. This introduction (Section I) provides a general explanation of all maintenance levels under the standard Army Maintenance System concept.

b. The Maintenance Allocation Chart (MAC) in section II designates overall authority and responsibility for the performance of maintenance functions on the identified end item or component. The application of the maintenance functions to the end item or component will be consistent with the capacities and capabilities of the designated maintenance levels, which are shown on the MAC in Column (4) as:

Unit - Includes 2 subcolumns, C (operator/crew) and O (unit) maintenance.

Direct Support - Includes an F subcolumn.

General Support - includes an H subcolumn.

Depot - includes a D subcolumn.

c. Section III lists the tools and test equipment (both special tools and common tools sets) required for each maintenance function as referenced from section II.

d. Section IV contains supplemental instructions and explanatory notes for a particular maintenance function.

**B-2. Maintenance Function**

Maintenance functions will be limited to and defined as follows:

a. *Inspect.* To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination (e.g. by sight, sound, or feel).

b. *Test.* To verify serviceability by measuring the mechanical, pneumatic, hydraulic, or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. *Service.* Operations required periodically to keep an item in proper operating condition, i.e., to clean (includes decontaminate, when required), to preserve, to drain, to paint, or to replenish fuel, lubricants, chemical fluids, or gases.

d. *Adjust.* To maintain, or regulate within prescribed limits, by bringing into proper position, or by setting the operating characteristics to specified parameters.

e. *Align.* To adjust specified variable elements of an item to bring about optimum or desired performance.

f. *Calibrate.* To determine and cause corrections to be made or to be adjusted on instruments or test measuring, and diagnostic equipment used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. *Remove/Install.* To remove and install the same item when required to perform service or other maintenance functions. Install may be the act of emplacing, or fixing into position a spare, repair part, or module (component or assembly) in a manner to allow the proper functioning of an equipment or system.

h. *Replace.* To remove an unserviceable item and install a serviceable counterpart in its place. "Replace" is authorized by the MAC and assigned maintenance level is shown as the 3rd position of the SMR code.

i. *Repair.* The application of maintenance services<sup>1</sup> including fault location/troubleshooting,<sup>2</sup> removal/installation, and disassembly/assembly<sup>3</sup> procedures, and maintenance actions<sup>4</sup> to identify troubles and restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.

j. *Overhaul.* That maintenance effort (service/action) prescribed to restore an item to a completely serviceable/operational condition as required by maintenance standards in appropriate technical publications

1. Services - Inspect, test, service, adjust, align, calibrate, and/or replace.

2. Fault location/troubleshooting - The process of investigation and detecting the cause of equipment malfunctioning; the act of isolating a fault within a system or unit under test (UUT).

3. Disassembly/assembly - The step-by-step breakdown (taking apart) of a spare/functional group coded item to the level of its least component, that is assigned an SMR code for the level of maintenance under consideration (i.e., identified as maintenance significant).

4. Actions - Welding, grinding, riveting, straightening, facing, machining, and/or resurfacing.

(i.e. DMWR. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. *Rebuilt.* Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (e.g., hours,/miles) considered in classifying Army equipments/components.

**B-3. Explanation of Columns in the Mac, Section II**

a. *Column 1, Group Number.* Column 1 lists functional group code numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. *Column 2, Component/Assembly.* Column 2 contains the item names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. *Column 3, Maintenance functions.* Column 3 lists the functions to be performed on the item listed in Column 2. (For detailed explanation of these functions, see paragraph B2).

d. *Column 4, Maintenance Level.* Column 4 specifies each level of maintenance authorized to perform each function listed in Column 3 by indicating work-time required (expressed as manhours in whole hours or decimals) in the appropriate subcolumn. This work-time figure represents the active time required to perform that maintenance function at the indicated level of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance levels, appropriate work-time figures will be shown for each level. The work-time figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time (including any necessary disassembly/assembly time), troubleshooting/fault isolation time, and quality assurance time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. The symbol designations for the various maintenance levels are as follows:

- C .....Operator or crew maintenance
- O .....Unit maintenance
- F .....Direct Support maintenance
- L .....Specialized Repair Activity (SRA)5
- H .....General support maintenance
- D .....Depot maintenance

e. *Column 5, Tools and Equipment.* Column 5 specifies, by code, those common tool sets (not individual tools), common TMDE, and special tools, test, special TMDE, and special support equipment required to perform the designated function.

f. *Column 6, Remarks.* When applicable, this column contains a letter code, in alphabetical order, which is keyed to the remarks in Section IV.

**B-4. Explanation of Columns in Tool and Test Equipment Requirements, Section III.**

a. *Column 1, Reference Code* The tool and test equipment reference code correlates with a code used in the MAC. Section 11, Column 5.

b. *Column 2, Maintenance Level.* The lowest level of maintenance authorized to use the tool or test equipment.

c. *Column 3, Nomenclature.* Name or identification of the tool or test equipment.

d. *Column 4, National Stock Number.* The National Stock Number of the tool or test equipment.

e. *Column 5, tool Number.* The manufacturer's part number.

**B-5. Explanation of Columns in Remarks, Section IV.**

a. *Column 1, Reference Code* The code recorded in Column 6, Section II.

b. *Column 2, Remarks.* This column lists information pertinent to the maintenance functions being performed as indicated in the MAC, Section II.

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5. This maintenance level is not included in Section II, column (4) of the Maintenance Allocation Chart. Functions to this level of maintenance are identified by a work-time figure in the "H" column of Section II, column (4), and an associated reference code used in the Remarks Code Column (6) This code is keyed to Section IV, Remarks, and the SRA complete repair application is explained there.

**Section II. MAINTENANCE ALLOCATION CHART  
FOR  
PROCESSOR, INTERMEDIATE FREQUENCY  
CV-4008/U**

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL					(5) TOOLS AND EQUIPMENT REF CODE	(6) REMARKS CODE	
			UNIT		DIRECT SUPPORT	GENERAL SUPPORT	DEPOT			
			C	O	F	H	D			
00	PROCESSOR, INTER- MEDIATE FREQUENCY CV-4008/U C5116261	INSPECT		0.2				2	A	
				0.3				2, 10, 11		
		TEST ALINE			1.3			10.0	18	B
								6.0	2, 3, 4, 5, 6, 9, 12, 13, 15,	
		ADJUST							2, 3, 4, 5, 6, 9, 12, 13, 15	C
		REPAIR		0.2					2,3,16	
01	MODULE ASSEMBLY, CONVERTER - CONVE RTERE- FREQUENCY RESOLV-  ING UNIT (A1A11) C5090563	REPAIR			0.3			18	D. E	
		REPAIR					0.6	1,2, 3		
		REPAIR REPLACE		0.1				2		
		INSPECT			0.1				18	
		TEST					2.0		2, 3, 4, 5, 6, 9 12	
		ADJUST							6, 9, 12, 13,15	
02	MODULE ASSEMBLY, BUILT IN TEST (A1A3) C5116581	ADJUST25						2, 3, 4, 5, 13, 15	0.5	
		REPAIR			0.1			2,3,16 18		
		REPLACE							18	
		INSPECT TEST			0.1			3.0	2, 3,4, 5, 6, 9, 12, 13, 15	
		REPAIR					0.5		13,1 2,3,16	
		REPLACE			0.1				18	

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL					(5) TOOLS AND EQUIPMENT REF CODE	(6) REMARKS CODE
			UNIT		DIRECT SUPPORT	GENERAL SUPPORT	DEPOT		
			C	O	F	H	D		
03	CIRCUIT CARD ASSEMBLY, DUAL SAMPLE/HOLD AMPLI- TITUDE (A2A9) C5116592	INSPECT			0.1			18	
		TEST					3.0	2, 3, 4, 5, 12, 13, 12, 13, 14, 15	
		ADJUST						2, 3, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15	
		REPAIR					0.5	1, 3	
		REPLACE			0.1			18	
04	CIRCUIT CARD ASSEMBLY, DUAL ASSEMBLY, DUAL SAMPLE/HOLD PHASE (A2A5, A2A6, A2A7, A2A8) C5116596	INSPECT	0.1	18					
		TEST					3.0	2, 3, 4, 5, 2, 3, 4, 5, 12, 3, 14, 15	
		ADJUST					3.0	2, 3, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15	
		REPAIR					0.5	13	
		REPLACE			0.1			18	
05	CIRCUIT CARD ASSEMBLY, DUAL SAMPLE/HOLD FREQ- UNCY RESOLVING UNIT (A2A10) C5116600	INSPECT			0.1			18	
		TEST					3.0	2, 3, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15,	
		TEST							
		ADJUST						2, 3, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15	
		REPAIR REPAIR					0.5	1, 3	
		REPLACE			0.1		18		

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL					(5) TOOLS AND EQUIPMENT REF CODE	(6) REMARKS CODE
			UNIT		DIRECT SUPPORT	GENERAL SUPPORT	DEPOT		
			C	O	F	H	D		
06	CIRCUIT CARD ASSEMBLY, DUAL SAMPLE/HOLD AMPLITUDE FREQUEN- CY RESOLVING UNIT (A2A1 1)	INSPECT TEST			0.1			18 2, 3, 4,5,	
		ADJUST					3.0	12, 13, 14, 15	
		REPAIR REPAIR					0.5	2, 3, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15 1,3	
		REPLACE			0.1			18	
07	CIRCUIT CARD ASSEMBLY, INTER- FACE (A2A1) C509566	INSPECT TEST			0.1			18 2, 3, 4 5 6,7,8,9, 12,13,	
		REPAIR REPLACE			0.1		0.5	14,15 1,3 18	
08	MODULE, QUAD PHASE DETECTOR A (A1 A12) C5116630	INSPECT TEST			0.1			18 2,3, 4, 5, 6,7,8,9, 12,13,15	
		REPAIR					0.3	2,3,16	
		REPLACE			0.1			18	
0801	CIRCUIT CARD ASSEMBLY, DUAL PHASE DETECTOR A (A1, A2) C5116558	INSPECT TEST					01 2.5	2 2, 3, 4, 5, 6, 7 8, 9 12,13, 14,15	
		REPAIR REPLACE					0.5	1,3 2,16	

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL					(5) TOOLS AND EQUIPMENT REF CODE	(6) REMARKS CODE	
			UNIT		DIRECT SUPPORT	GENERAL SUPPORT	DEPOT			
			C	O	F	H	D			
09	MODULE, QUAD PHASE DETECTOR B (AIAI3) C5116610	INSPECT TEST			0.1			2.5	18 2, 3, 4, 5, 6, 7 8 9 12, 13, 14, 15	
		REPAIR REPLACE			0.1			0.3	2,3,16 18	
0901	CIRCUIT CARD ASSEMBLY, DUAL PHASE DETECTOR B (A1, A2) C5116575	INSPECT TEST						0.1 2.5	2 2, 3, 4, 5, 6,7,8,9, 12, 13, 14,15	
		REPAIR						0.5 0.1	1,3	
		REPLACE							2,16	
10	MATCHED SET, MODULE ASSEMBLY,	INSPECT TEST			0.1			3.0	18 2, 3, 4, 5,	
		ADJUST						3.0 3.0	2,3,4,5, 6, 7, 8, 9, 12,13, 15	
		REPLACE			0.1				18	
11	MODULE ASSEMBLY 150 MHZ IF LIMITER/ LOGIC (AIA9) C5116637	INSPECT TEST			0.1			2.5	18 2 3 4 5 6, 7, 8, 9 12, 13, 15	
		REPAIR01						0.3	2,3, 16 18	
		REPLACE								
1101	MICRODULESTRIP ASSEM- BLY, 150 MHZ IF LIMIT- ER/ LOGIC AMPLIFIER (A1) C5116569	INSPECT TEST						0.1 2.5	2 2, 3, 4, 5, 6, 7 8, 9 12, 13, 14, 15	
		REPAIR REPLACE						04	1, 3 2,16	
			<b>B-6</b>							

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL					(5) TOOLS AND EQUIPMENT REF CODE	(6) REMARKS CODE
			UNIT		DIRECT SUPPORT	GENERAL SUPPORT	DEPOT		
			C	O	F	H	D		
12	MODULE ASSEMBLY, 180 MHZ, IF (AI A6) C5116641	INSPECT TEST	0.1	18					
		REPAIR					0.3	6, 7, 8, 9, 12, 13, 15 2, 3, 16 18	
		REPLACE			0.1				
1201	MICRO-STRIP SUBAS- SEMBLY, 180 MHZ LIMIT- ER/LOGIC AMPLIFIER (A1) C5116526	INSPECT TEST					0.1 2.5	2 2 3 4 5 7, 8 9 6, 13,14, 15	
		REPAIR					0.4	1,3	
		REPLACE					0.1	2,16	
13	MODULE ASSEMBLY, 120MHZ IF (A11A7) C5116645	INSPECT TEST			0.1		2.5	18 2, 3, 4, 5, 6,7,8,9, 12, 13, 15	
		REPAIR					0.3	2, 3, 16	
		REPLACE			0.1			18	
1301	MICRO-STRIP SUBAS- SEMBLY, 120 MHZ LIMIT- ER/LOGIC AMPLIFIER (A1) C5116528	INSPECT TEST					0.1 2.5	2 2, 3, 4, 5 6, 9, 12,13, 14,15	
		REPAIR					0.4	1,3	
		REPLACE					0.1	2,16	
14	MODULE ASSEMBLY, FEQUENCY RESOLVING UNIT (A1A8) C5116649	INSPECT TEST			0.1		3.0	18 2, 3, 4, 5, 6 7 8 9 12,13, 15 2, 3, 16	
		REPAIR REPLACE			01			18	

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL					(5) TOOLS AND EQUIPMENT REF CODE	(6) REMARKS CODE
			UNIT		DIRECT SUPPORT	GENERAL SUPPORT	DEPOT		
			C	O	F	H	D		
1401	MICRO-STRIP SUBASSEMBLY, 180 MHZ COARSE FREQUENCY RESOLVING UNIT (A3) C5116578	INSPECT TEST					0.1 3.0	2 2, 3, 4, 5, 6, 7, 8, 9 12, 13, 14, 15	
		REPAIR REPLACE					0.3 0.1	1,3 2,16	
1402	MICRO-STRIP SUBASSEMBLY, 120 MHZ COARSE FREQUENCY RESOLVING UNIT (A1) C5116701	INSPECT TEST					0.1 3.0	2 2,3,4,5, 6,7,8, 9, 12 13 14, 15	
		REPAIR REPLACE					0.4 0.1	1, 3 2, 16	
1403	MICRO-STRIP SUBASSEMBLY, 150 MHZ COARSE FREQUENCY RESOLVING UNIT (A2)C5116705	INSPECT TEST					0.1 30	18 2, 3, 4, 5, 6, 7, 8, 9 12,1 3 14,15	
		REPAIR REPLACE					0.4 0.1	1,3 18	
15	CIRCUIT CARD ASSEMBLY, CONFIRM LOGIC (A2A2) C5090540	INSPECT TEST					0.1 2.5	18 2, 3, 4, 5, 6, 7, 8, 12, 13, 14,15	
		REPAIR REPLACE			0.1		0.5	1,3  18	



(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL					(5) TOOLS AND EQUIPMENT REF CODE	(6) REMARKS CODE	
			UNIT		DIRECT SUPPORT	GENERAL SUPPORT	DEPOT			
			C	O	F	H	D			
16	CIRCUIT CARD ASSEMBLY, PHASE REVERSAL DETECTOR (A2A4) C5116720	INSPECT TEST			0.1			2.5	18 2, 3, 4, 5, 6, 7, 8,  9,12, 13, 14, 15	
		REPAIR REPLACE			0.1			04	1,3 18	
17	CIRCUIT CARD ASSEMBLY, THRESHOLD DEGENERATOR (A2A3) C5090543	INSPECT TEST			0.1			2.5	18 2, 3, 4, 5, 12, 13, 14,15	
		ADJUST						2.5	2, 3, 4, 5, 6, 7, 8, 9, 12,13, 14,15	
		REPAIR REPLACE			0.1			0.5	1, 3 18	
18	MOUNTING PLATE ASSEMBLY (A1) C5117922	INSPECT REPAIR REPLACE			0.1 0.8 0.3			18 18 18		
19	CONNECTOR PLATEASSEMBLY (A2) C5116697	INSPECT REPAIR REPLACE			0.1 1.0 0.6			18 18 18		
20	COAX CABLE ASSEMBLIES W1 THRU W57	INSPECT TEST REPAIR REPLACE			0.1 0.2 0.8 0.2			18 18 18 18		

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**SECTION III. TOOL AND TEST EQUIPMENT REQUIREMENTS  
FOR  
PROCESSOR, INTERMEDIATE FREQUENCY  
CV-4008/U**

<b>TOOL OR TEST EQUIPMENT REF CODE</b>	<b>MAINTENANCE CATEGORY</b>	<b>NOMENCLATURE</b>	<b>NATIONAL/NATO STOCK NUMBER</b>	<b>TOOL NUMBER</b>
01	D	TOOL KIT, ELECTRONIC EQUIPMENT REPAIR	5108-00-339-3150	8001-0018
02	0, D	TOOL KIT, ELECTRONIC EQUIPMENT TK-105/G	5180-00-610-8177	
03	D	MULTIMETER, DIGITAL AN/USM-486(U)	6625-01-145-2430	8050A-5011
04	D	ANALYZER, SPECTRUM AN/USM-489(V)1	6625-01-079-9495	492-01-02-03-21
05	D	POWER SUPPLY, RECEIVER PP-8184/U	5895-01-253-3997	C5116264
06	D	TEST SET, ELECTRONIC SYSTEMS TS-4239/U	6625-01-2609326	C5116271
07	D	EXTENDER CARD, TWENTY PIN		C5116738
08	D	EXTENDER CARD, NINETY PIN		C5116742
09	D	TERMINATOR, 50 OHM		C5118444
10	0	MISSION TEST EQUIPMENT		C5117754
11	0	TAPE, LINE REPLACEABLE UNIT DIAGNOSTICS		5034-2934-01
12	F, D	VOLTMETER, VECTOR ME-512/U	6625-00-929-1897	8405A
13	F, D	OSCILLOSCOPE, 400 MHZ	6625-01-015-6562	OS-266 (P)IU
14	D	TEST SYSTEM		ST-3000
15	D	COMPUTER, DIGITAL		C5090294
16	D	TORQUE LIMITING SET		MMCARR 5716A13 C5090586
17	D	REPAIR KIT, INSERT-SCREW THREAD		
18	F	GENERAL SUPPORT MAINTENANCE FACILITY		
19	D	EXTRACTOR, CIRCUIT CARD		C5090586
20	D	CABLE ADAPTER, VOLTMETER, VECTOR		LOMFG
21	D	TEST CABLE, POWER SUPPLY		LOMFG
22	D	TOOL, INSERTION/EXTRACTION		4916A
23	D	TEST CABLE, SPECTRUM ANALYZER		LOMFG
24	D	CABLE ADAPTER, DIGITAL MULTIMETER		LOMFG
25	F, D	PROBE, PASSIVE 10X	6625-01459-2436	P6063B
26	D	AMPLIFIER, WIDE BAND	6625-00-506-1121	7A19

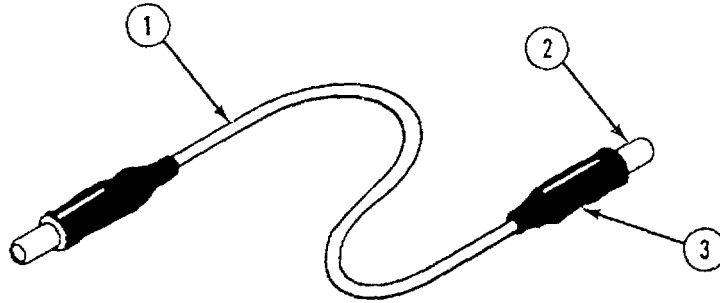
**B-111(B-12 BLANK)**

**SECTION IV. REMARKS**

REFERENCE CODE	REMARKS																																																																																
A	ORGANIZATIONAL MAINTENANCE LEVEL ACCOMPLISHES SYSTEM TESTS USING BIT, MISSION TEST EQUIPMENT, AND CONTINUITY TESTS OF CABLES.																																																																																
B	DIRECT SUPPORT MAINTENANCE LEVEL ACCOMPLISHES THOSE TESTS REQUIRED TO LOCATE FAULTY MODULES, COMPONENTS, WIRING AND CABLE PROBLEMS.																																																																																
C	ORGANIZATIONAL MAINTENANCE LEVEL ACCOMPLISHES REPAIR BY REPLACEMENT OF LAMPS, FUSES, KNOBS, FILTERS, CABLE ASSEMBLIES, SELECTED CARDS, AND BLACK BOXES DETECTED BY BIT AND MISSION TEST EQUIPMENT.																																																																																
D	DIRECT SUPPORT MAINTENANCE LEVEL PROVIDES ORGANIZATIONAL MAINTENANCE ASSISTANCE AS REQUIRED AND REPAIR OF CHASSIS/FRAME BY REPLACEMENT OF METERS, SWITCHES, CONNECTORS AND OTHER CHASSIS AND FRONT PANEL MOUNTED PIECE PARTS AND SELECTED MODULES/CIRCUIT CARDS AND CABLE ASSEMBLIES REPAIR/REPLACEMENT																																																																																
E	DIRECT SUPPORT MAINTENANCE LEVEL REPAIRS MINOR DAMAGE TO LRU CHASSIS AND COVERS BY STRAIGHTENING, SANDING, AND SPOT PAINTING																																																																																
F	THE FOUR 150 MHz IF MODULE ASSEMBLIES, PN C5116633, ARE PHASE MATCHED AND MUST BE REPLACED AS A SET.																																																																																
G	THE DELAY LINE MODULE, PN C5116727 IS NOT REPAIRABLE AND SHOULD B CONSIDERED AS A THROW AWAY ITEM.																																																																																
H	<p>CABLE ASSEMBLIES THE FOLLOWING LISTS OF SETS OF CABLES MUST BE REMOVED AND REPLACED AS SETS. THEY ARE CUT AND TRIMMED FOR PHASE TRACKING; THEREFORE, IF ONE CALBE IS BAD, THE SET MUST BE REPLACES WITH A NEW PHASE MATCHED SET, IT IS A DEPOT LEVEL TASK. THE SETS FOLLOW:</p> <table> <tbody> <tr> <td>SET 1</td> <td>W3, C5116662</td> <td>SET5</td> <td>W2</td> <td>C5116661</td> </tr> <tr> <td></td> <td>W20 C5116679</td> <td></td> <td>W6</td> <td>C5116665</td> </tr> <tr> <td></td> <td>W21 C5116680</td> <td></td> <td>W11</td> <td>C5116670</td> </tr> <tr> <td></td> <td>W12 C5116671</td> <td></td> <td></td> <td></td> </tr> <tr> <td>SET2</td> <td>W4, C5116663</td> <td>SET 6,</td> <td>W42</td> <td>C5117905</td> </tr> <tr> <td></td> <td>W14 C5116673</td> <td></td> <td>W43</td> <td>C5117906</td> </tr> <tr> <td></td> <td>W16 C5116675</td> <td></td> <td>W44</td> <td>C5117907</td> </tr> <tr> <td></td> <td>W45 C5117908</td> <td></td> <td></td> <td></td> </tr> <tr> <td>SET 3</td> <td>W7, C5116666</td> <td>SET 7</td> <td>W31,</td> <td>C5116691</td> </tr> <tr> <td></td> <td>W15 C5116674</td> <td></td> <td>W32,</td> <td>C5116692</td> </tr> <tr> <td></td> <td>W17, C5116676</td> <td></td> <td>W35,</td> <td>C5116695</td> </tr> <tr> <td></td> <td>W36 C5116695</td> <td></td> <td></td> <td></td> </tr> <tr> <td>SET 4</td> <td>W1, C5116660</td> <td></td> <td>W39,</td> <td>C5117902</td> </tr> <tr> <td></td> <td>W5, C5116664</td> <td></td> <td>W40</td> <td>C5117903</td> </tr> <tr> <td></td> <td>W13, C5116672</td> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td>W18, C5116677</td> <td></td> <td></td> <td></td> </tr> </tbody> </table>	SET 1	W3, C5116662	SET5	W2	C5116661		W20 C5116679		W6	C5116665		W21 C5116680		W11	C5116670		W12 C5116671				SET2	W4, C5116663	SET 6,	W42	C5117905		W14 C5116673		W43	C5117906		W16 C5116675		W44	C5117907		W45 C5117908				SET 3	W7, C5116666	SET 7	W31,	C5116691		W15 C5116674		W32,	C5116692		W17, C5116676		W35,	C5116695		W36 C5116695				SET 4	W1, C5116660		W39,	C5117902		W5, C5116664		W40	C5117903		W13, C5116672					W18, C5116677			
SET 1	W3, C5116662	SET5	W2	C5116661																																																																													
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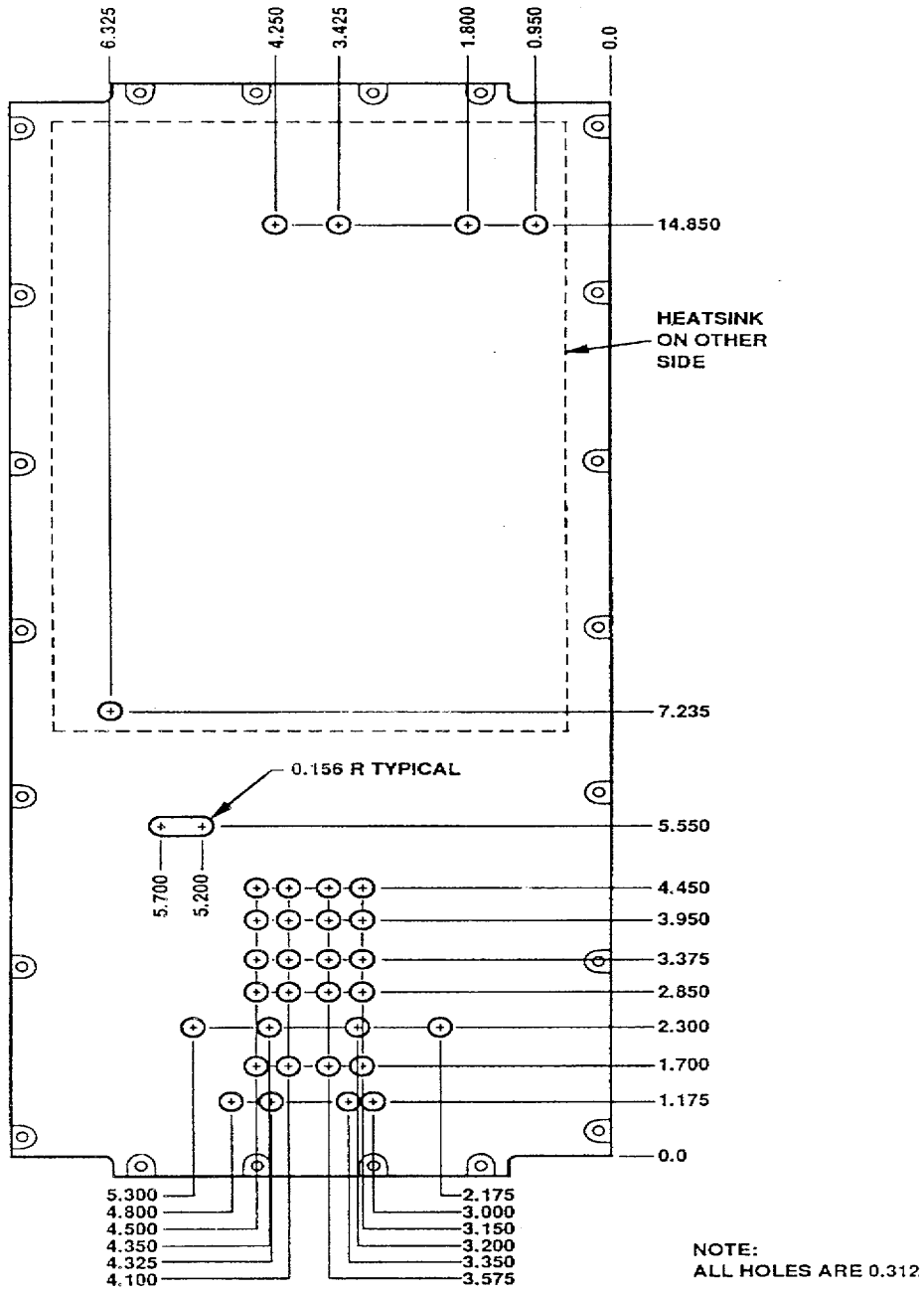
**APPENDIX C  
ILLUSTRATED LIST OF MANUFACTURED ITEMS**

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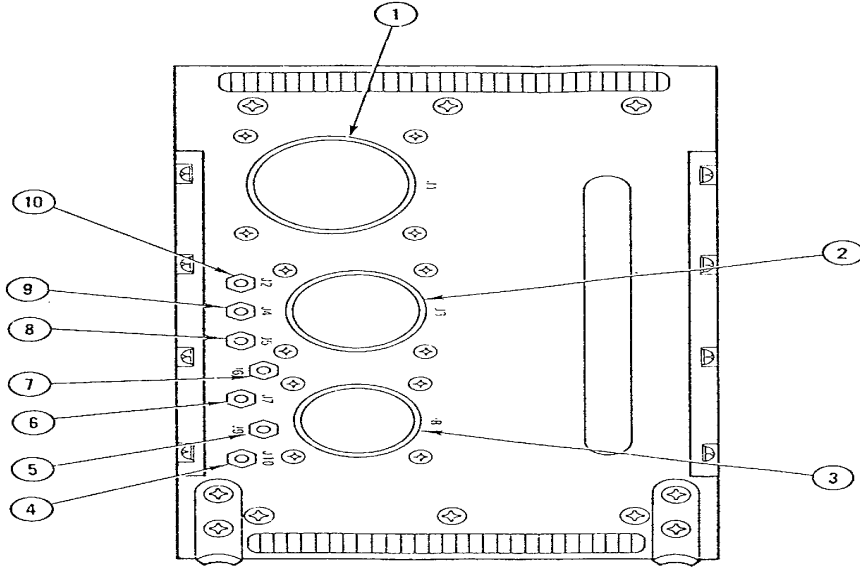


	<b>PART NUMBER</b>	<b>ITEM</b>	<b>QUANTITY</b>
1	20 AWG	WIRE, WHITE	6 INCHES
2	MS2749 - 20	PIN, CONNECTOR	2
3	M23053/5 - 101 - 0	SLEEVING INSULATION	AR

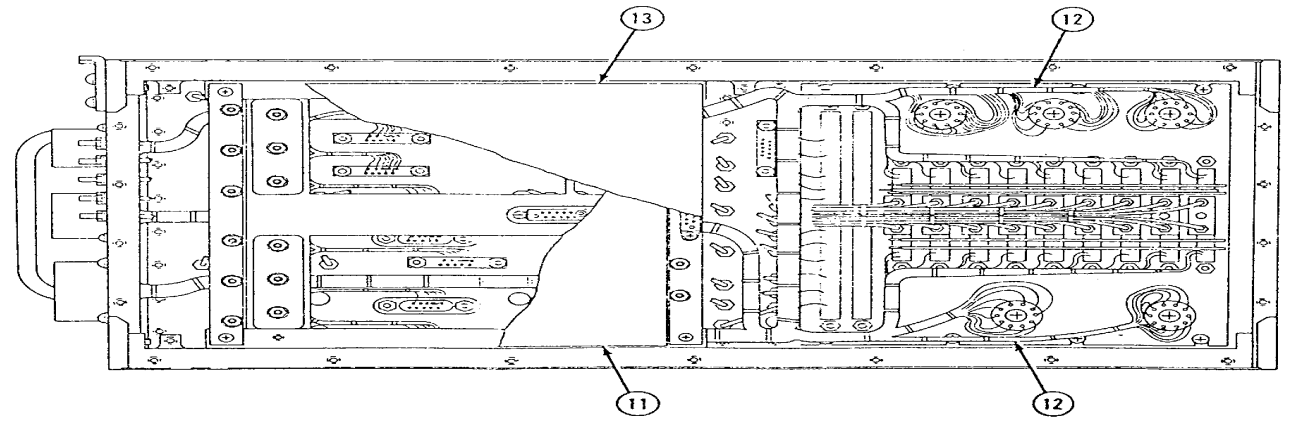
ALINEMENT COVER



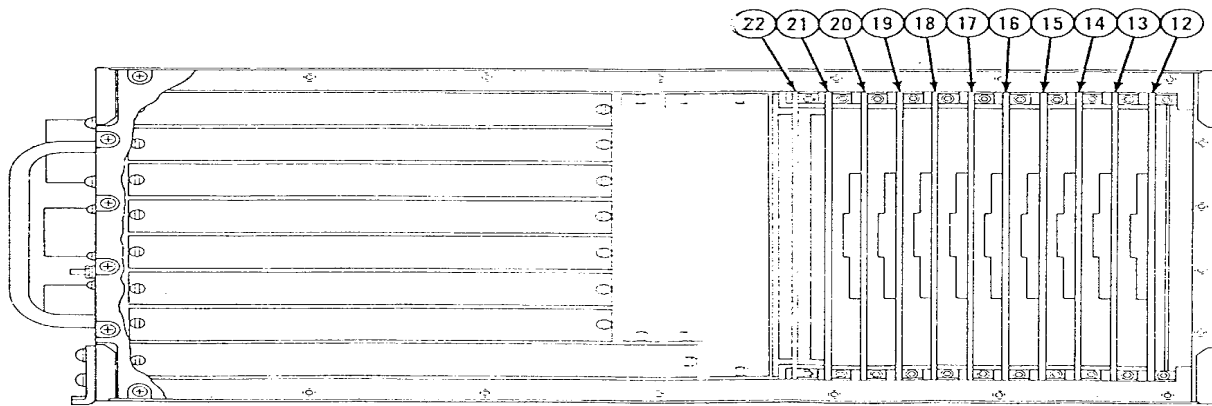
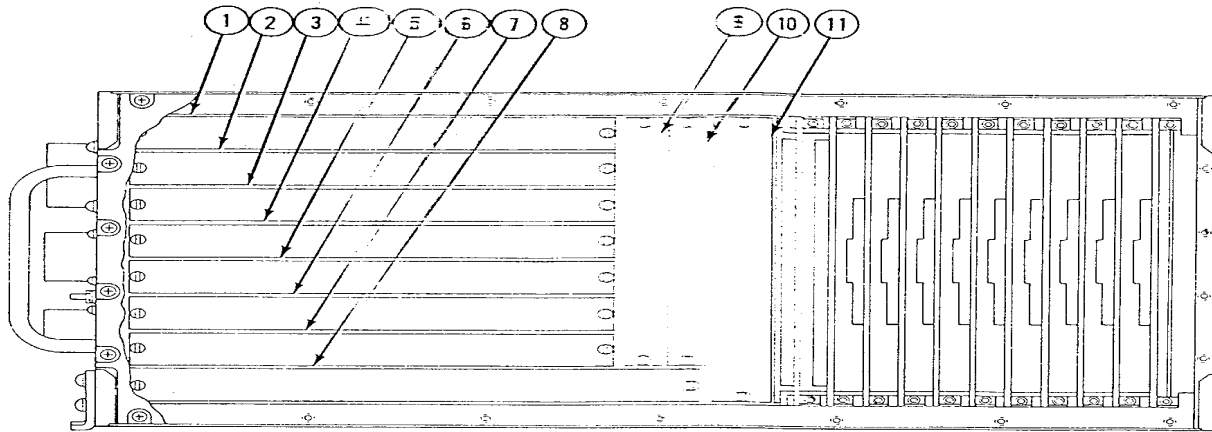
	PART NO.	ITEM	QUANTITY
1	C5117923	COVER	1



LEGEND		
REFERENCE DESIGNATION	COMPONENTS	KEY
J1	CONNECTOR POWER INPUT	1
J2	CONNECTOR CH A IF INPUT	10
J3	CONNECTOR IU I/O	2
J4	CONNECTOR CH B IF INPUT	9
J5	CONNECTOR CH C IF INPUT	8
J6	CONNECTOR CH D IF INPUT	7
J7	CONNECTOR LSB IF INPUT	6
J8	CONNECTOR RDC I/O	3
J9	CONNECTOR USB IF INPUT	5
J10	CONNECTOR BIT IF INPUT	4
A1A12	MODULE ASSEMBLY, QUAD PHASE DETECTOR A	11
A1A13	MODULE ASSEMBLY, QUAD PHASE DETECTOR B	13
W15	WIRE HARNESS	12



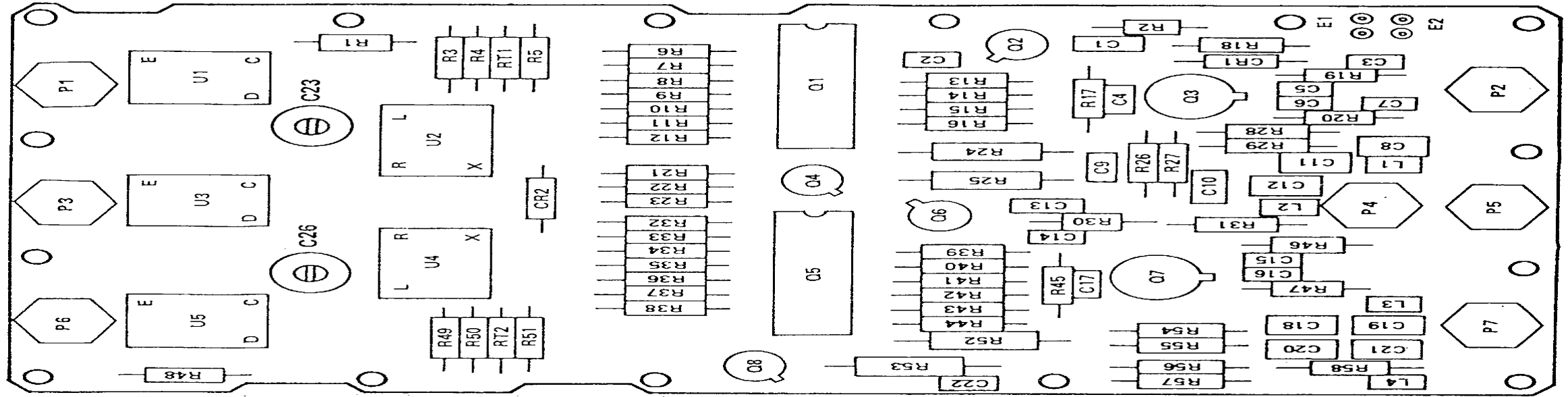
FO-1 Component Locations (Sheet 1 of 2)



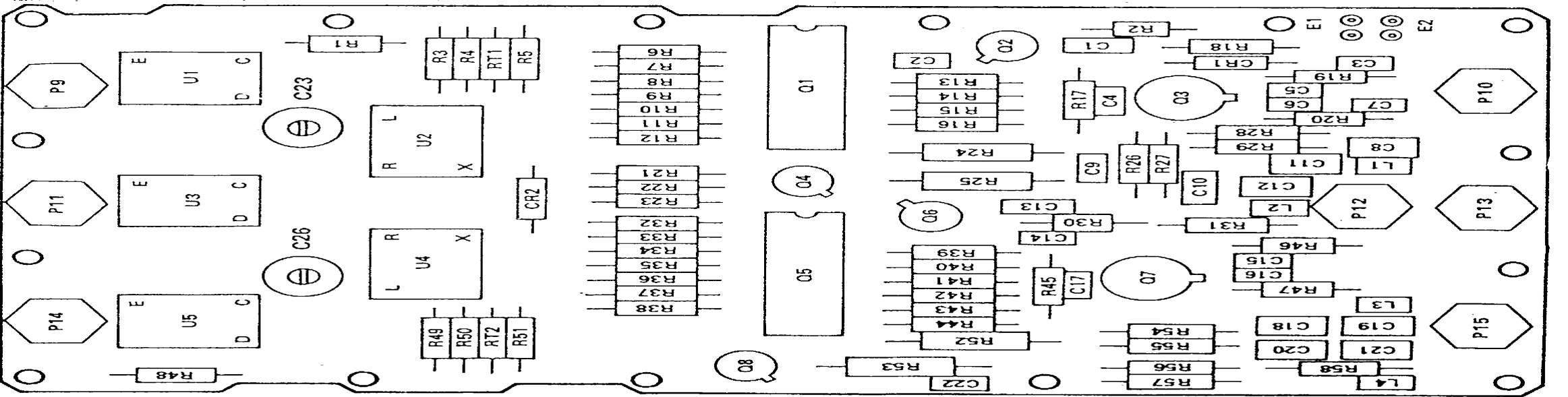
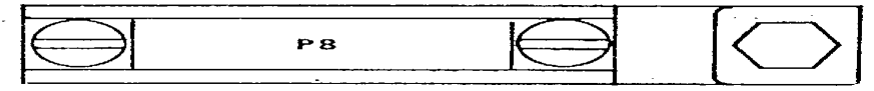
LEGEND

REFERENCE DESIGNATION	COMPONENTS	KEY
A1A1	150 MHz MODULE	1
A1A2	150 MHz MODULE	2
A1A3	BIT ASSEMBLY	3
A1A4	150 MHz MODULE	4
A1A5	150 MHz MODULE	5
A1A6	120 MHz IF MODULE	7
A1A7	180 MHz IF MODULE	6
A1A8	FRU MODULE	8
A1A9	150 MHz IF LIMITER/LOG MODULE	9
A1A10	DELAY LINE MODULE	10
A1A11	FRU-CONVERTER MODULE	11
A2A1	INTERFACE CCA	22
A2A2	CONFIRM LOGIC CCA	21
A2A3	THRESHOLD DETECTOR / GATE GENERATOR CCA	20
A2A4	PHASE REVERSAL DETECTOR CCA	19
A2A5	DUAL SAMPLE/HOLD PHASE CIRCUIT CARD ASSEMBLY	18
A2A6	DUAL SAMPLE/HOLD PHASE CIRCUIT CARD ASSEMBLY	17
A2A7	DUAL SAMPLE/HOLD PHASE CIRCUIT CARD ASSEMBLY	16
A2A8	DUAL SAMPLE/HOLD PHASE CIRCUIT CARD ASSEMBLY	15
A2A9	DUAL SAMPLE/HOLD AMPLITUDE CIRCUIT CARD ASSEMBLY	14
A2A10	DUAL SAMPLE/HOLD FRU CIRCUIT CARD ASSEMBLY	13
A2A11	DUAL SAMPLE/HOLD AMPLITUDE/FRU CIRCUIT CARD ASSEMBLY	12

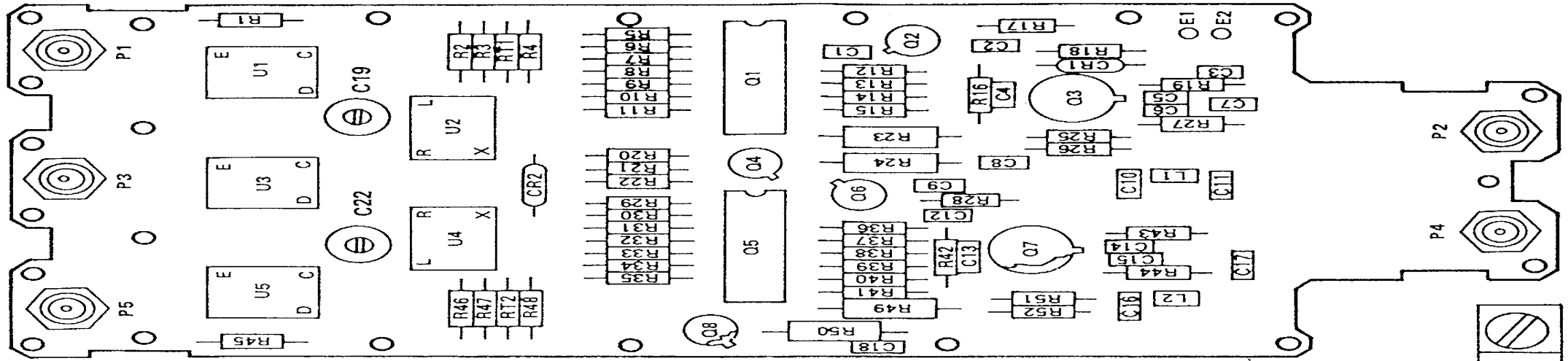
FO-1 Component Locations (Sheet 2 of 2)



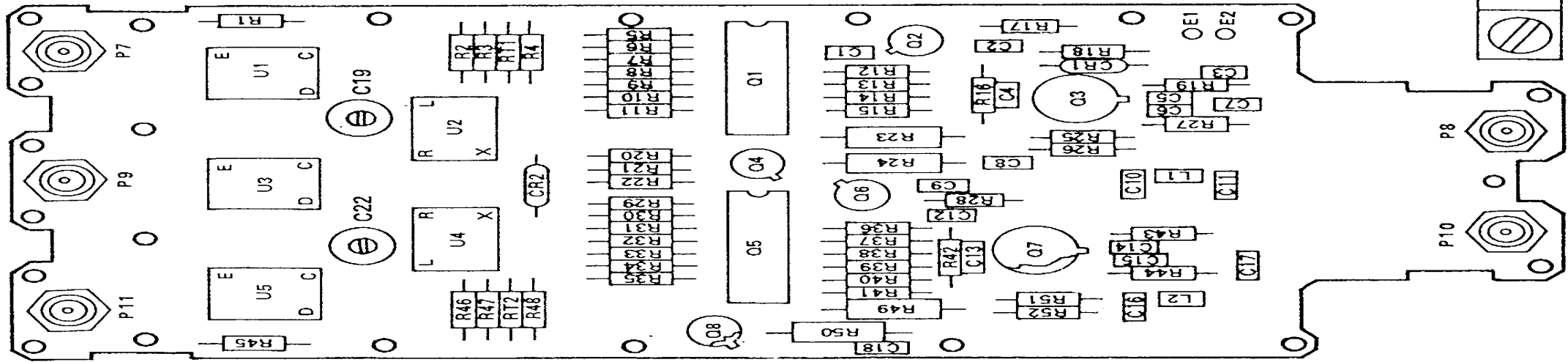
A1A12A2



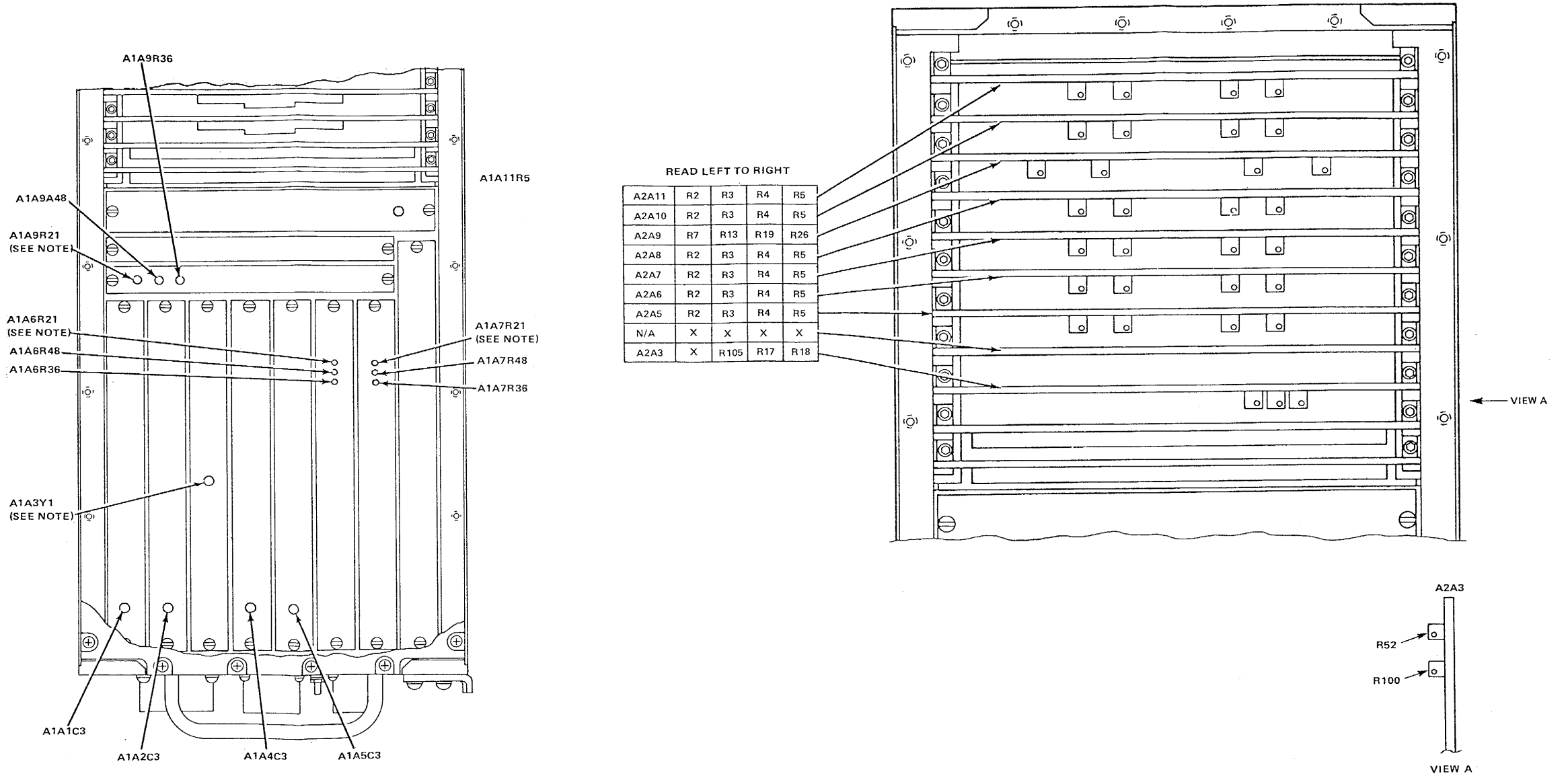




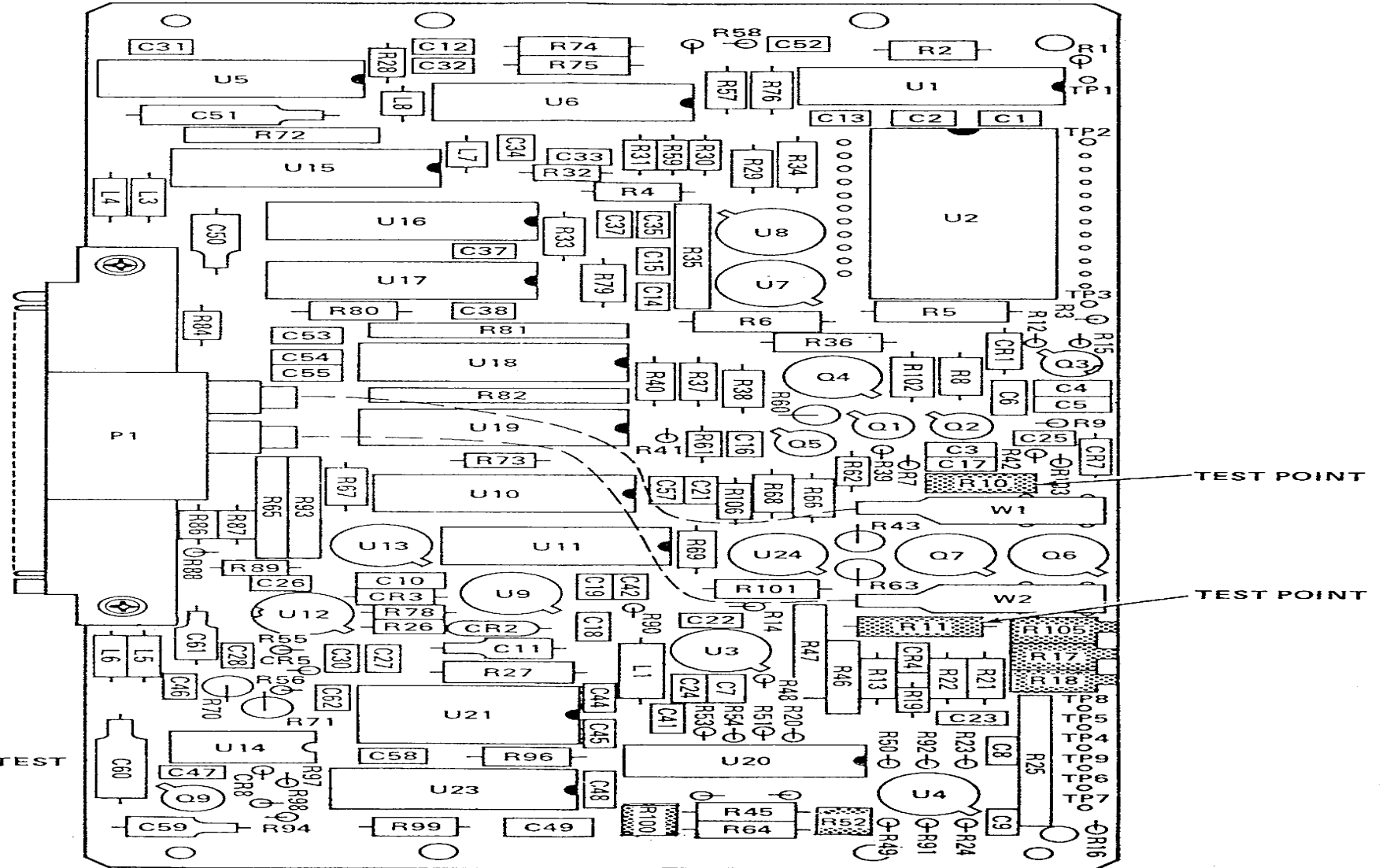
A1A13A2



A1A13A1

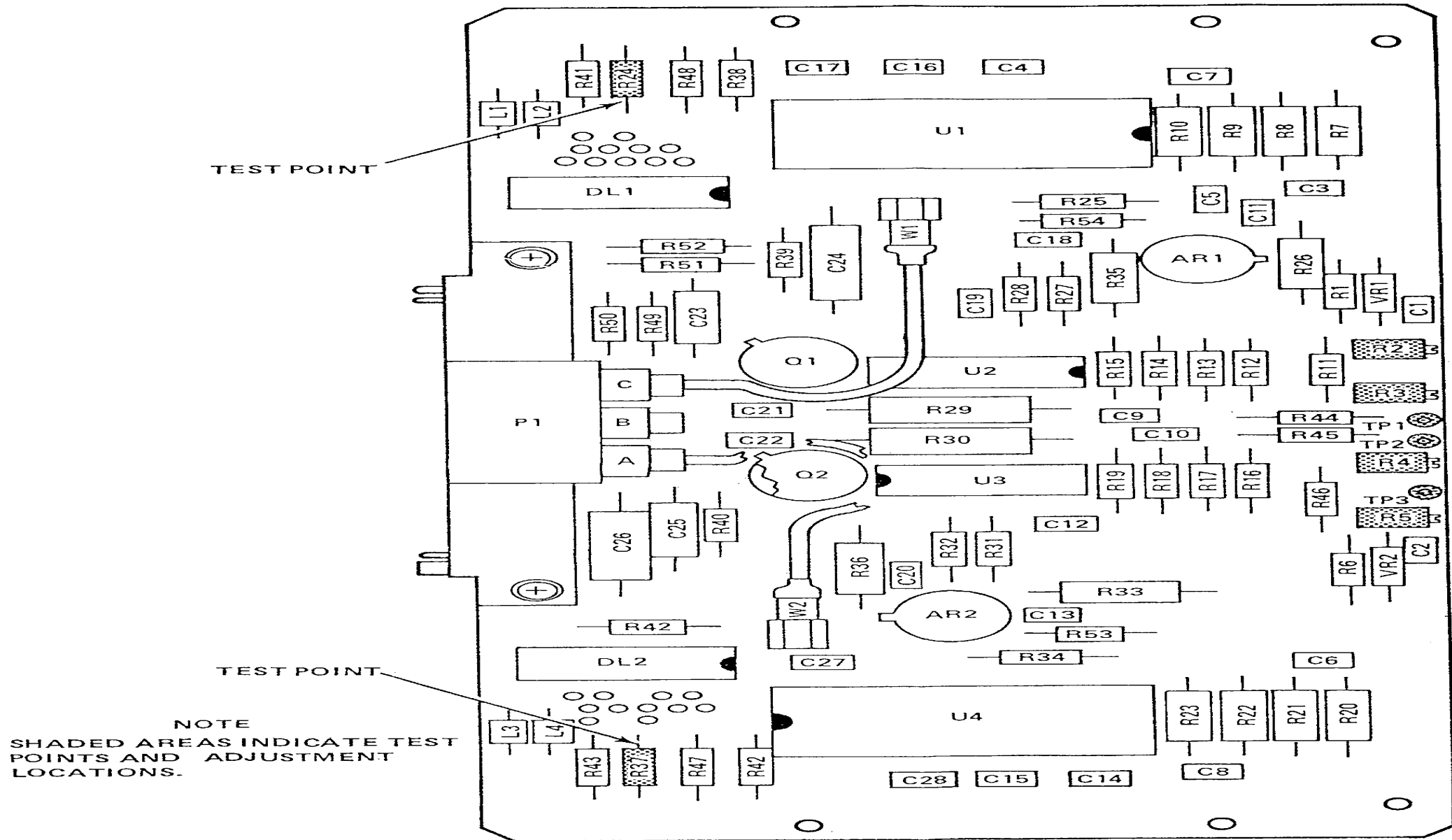


FO-2 Adjustment Locations (Sheet 3 of 3)

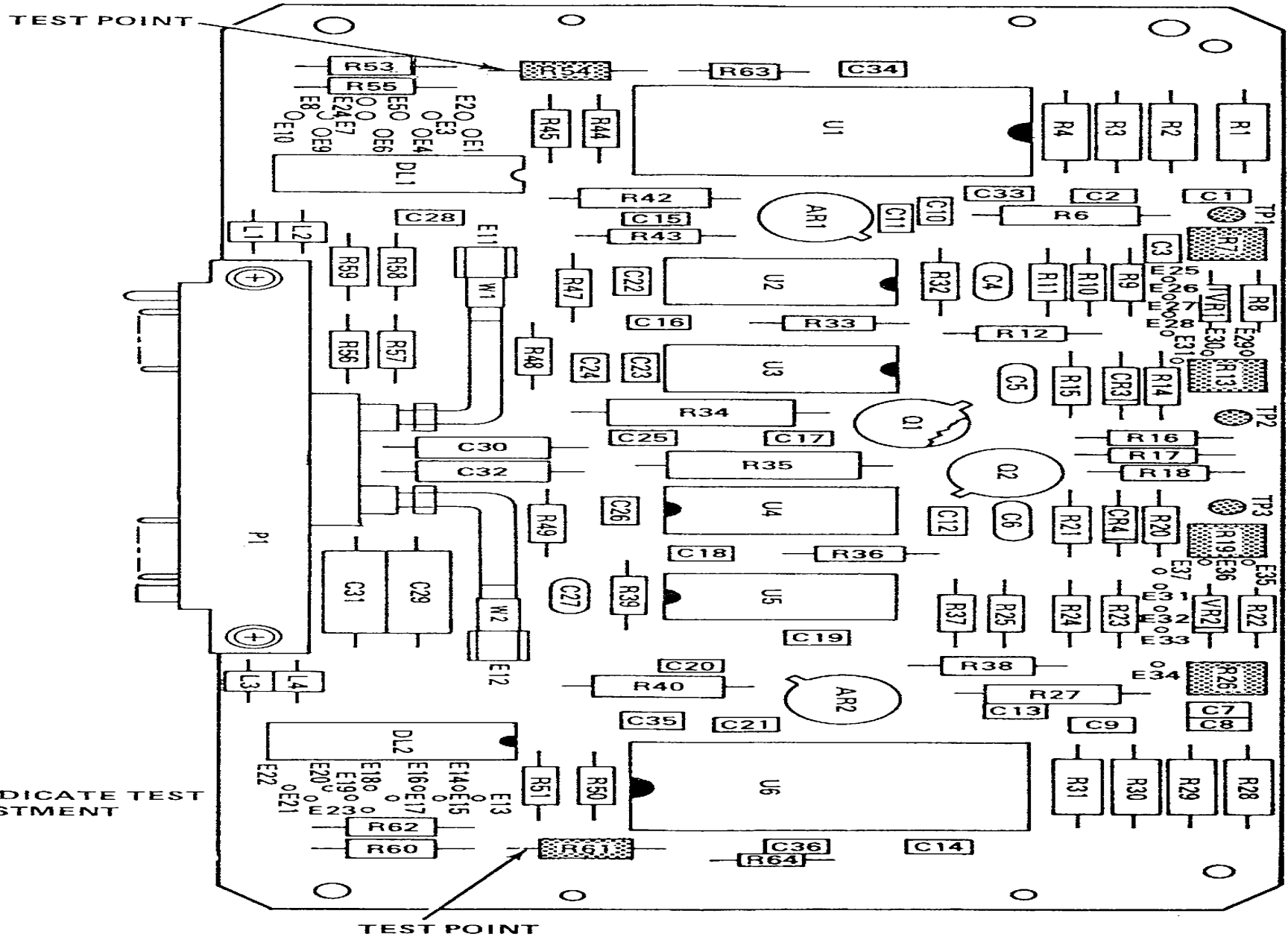


NOTE  
 SHADED AREAS INDICATE TEST  
 POINTS AND ADJUSTMENT  
 LOCATIONS.

FO-3. Test Points and Measurements (circuit Card A2A3)  
 Sheet 1 of 5)

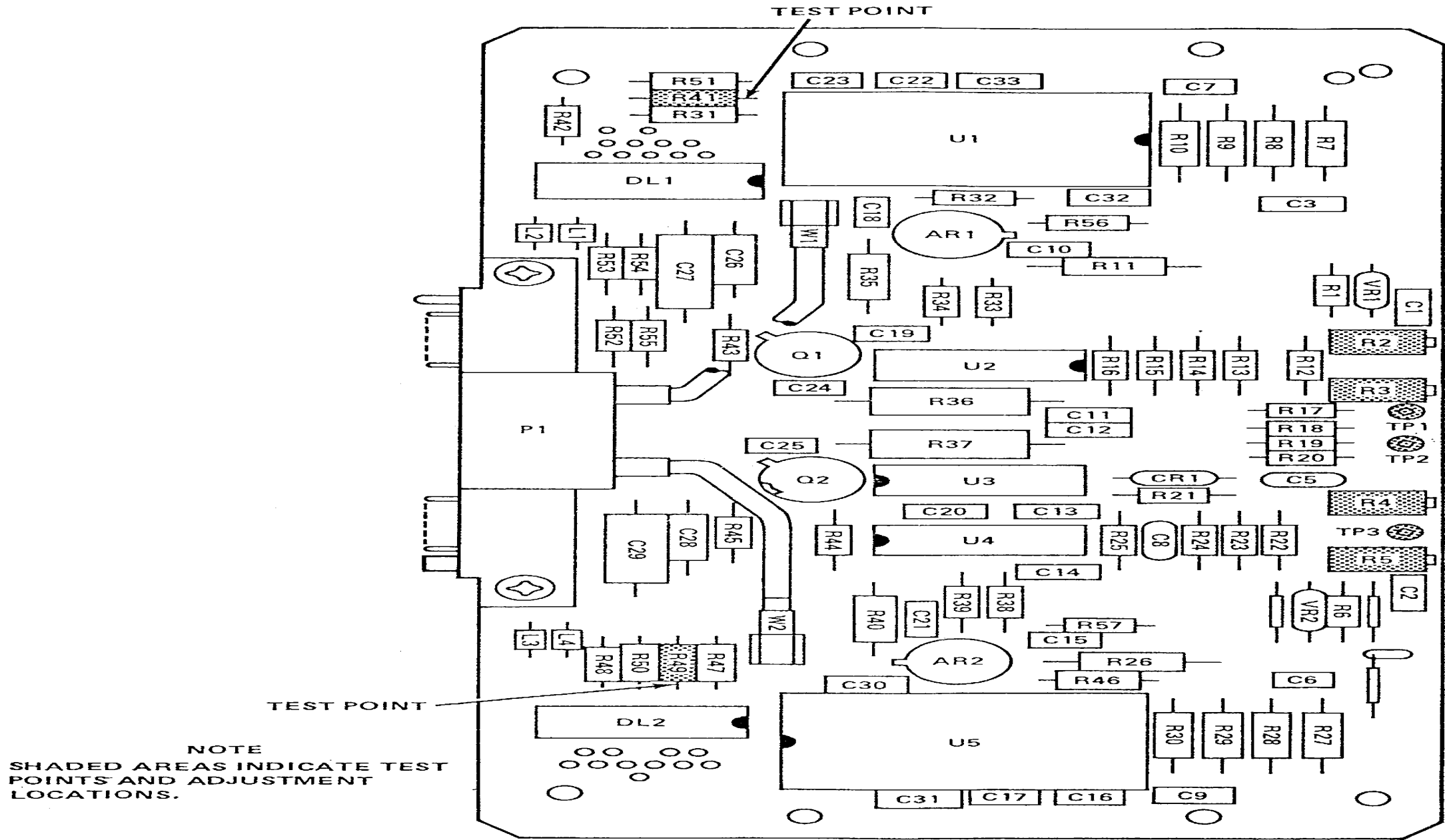


FO-3. Test Points and Measurements (Circuit Cars A2A5, A2A6, A2A7, A2A8, A2A10) (Sheet 2 of 5)



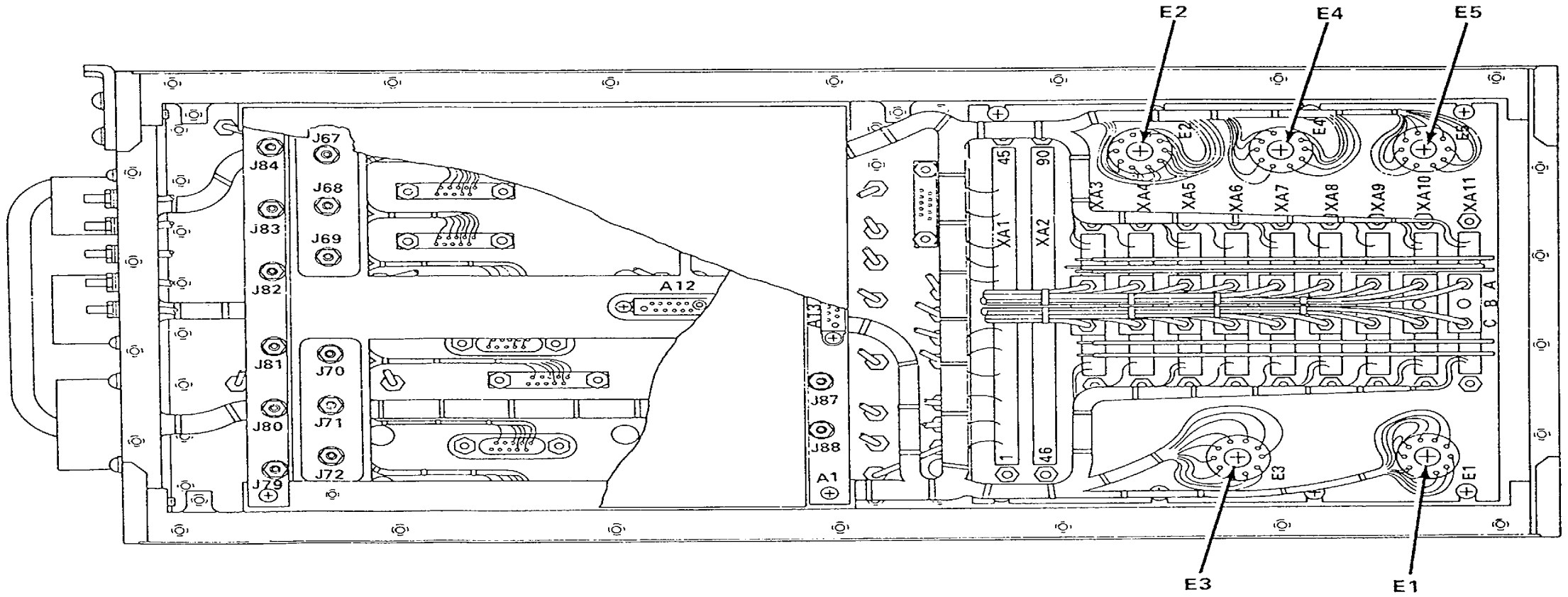
NOTE  
 SHADED AREAS INDICATE TEST  
 POINTS AND ADJUSTMENT  
 LOCATIONS.

FO-3. Test Points and Measurements (Circuit Card A2A9) (Sheet 3 of 5)

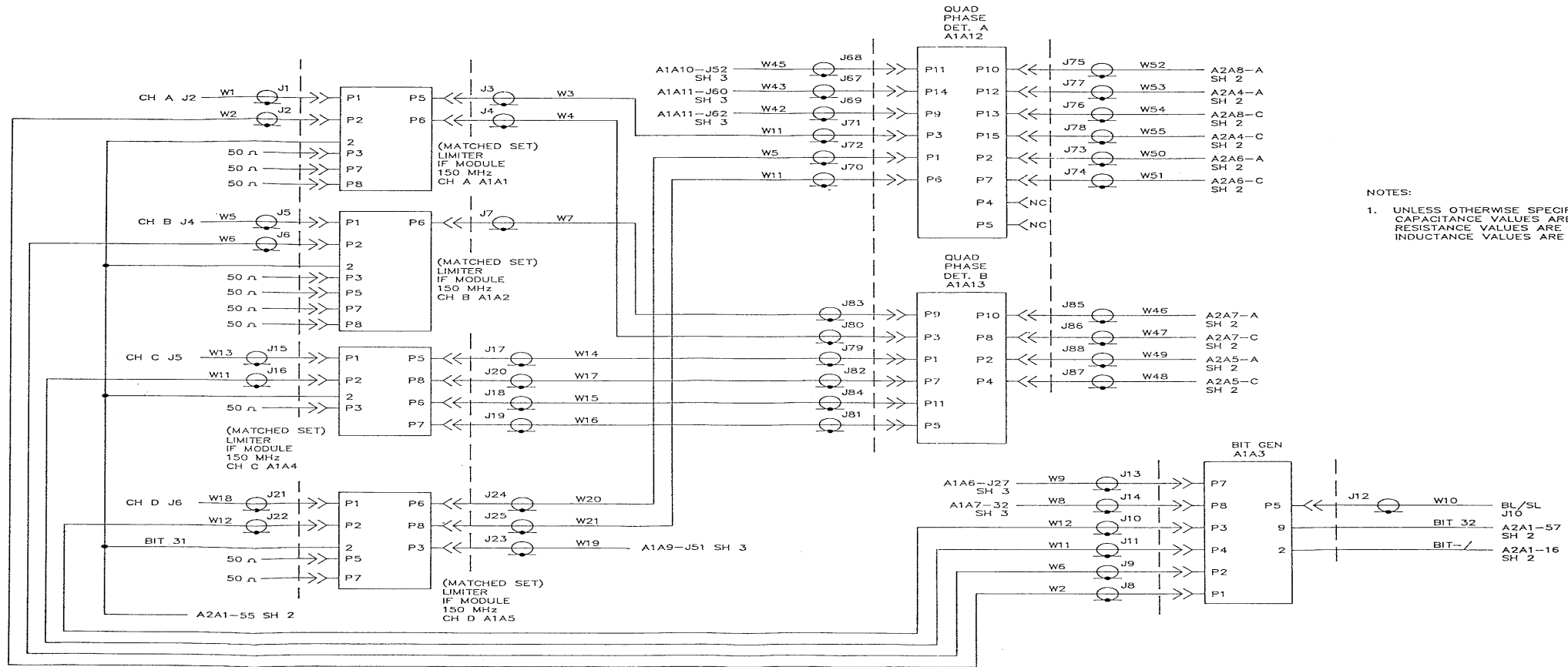


**NOTE**  
 SHADED AREAS INDICATE TEST POINTS AND ADJUSTMENT LOCATIONS.

FO-3. Test Points and Measurements (Circuit Card A2A11) (Sheet 4 of 5)



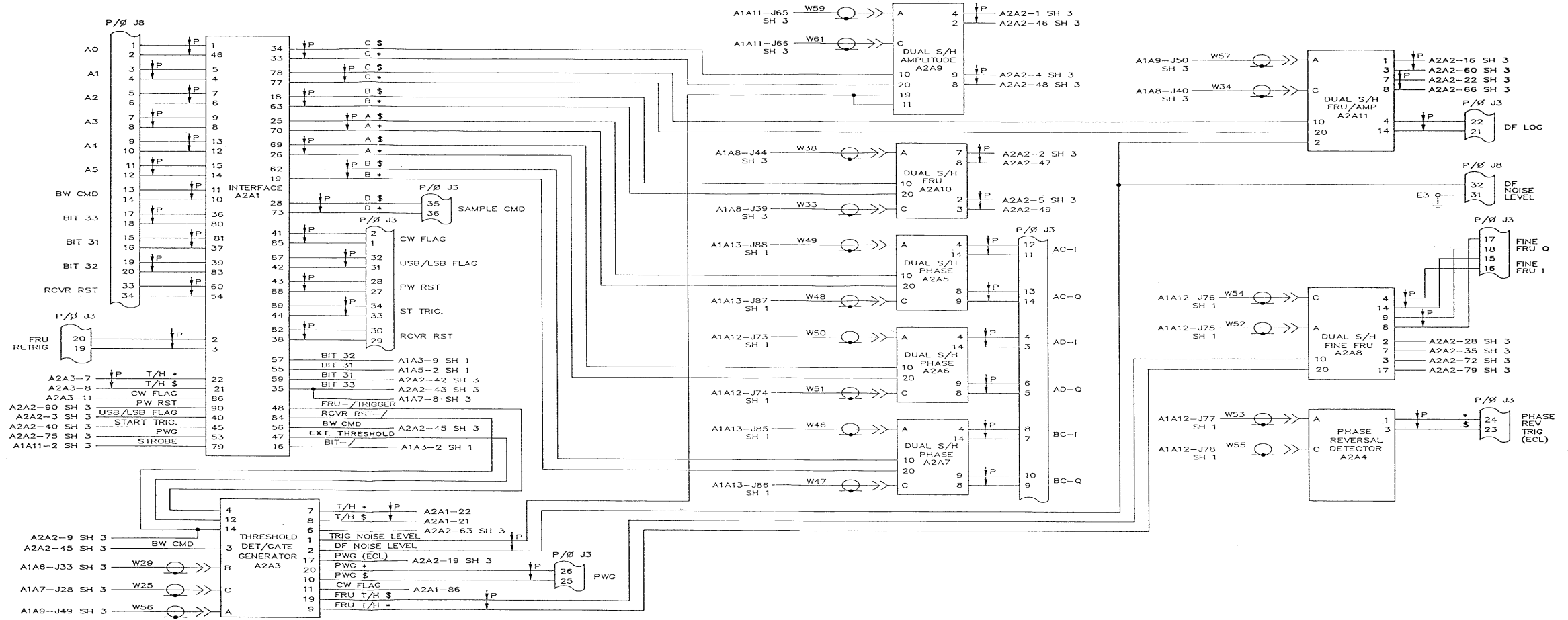
FO-3. Test Points and Measurements (Sheet 5 of 5)



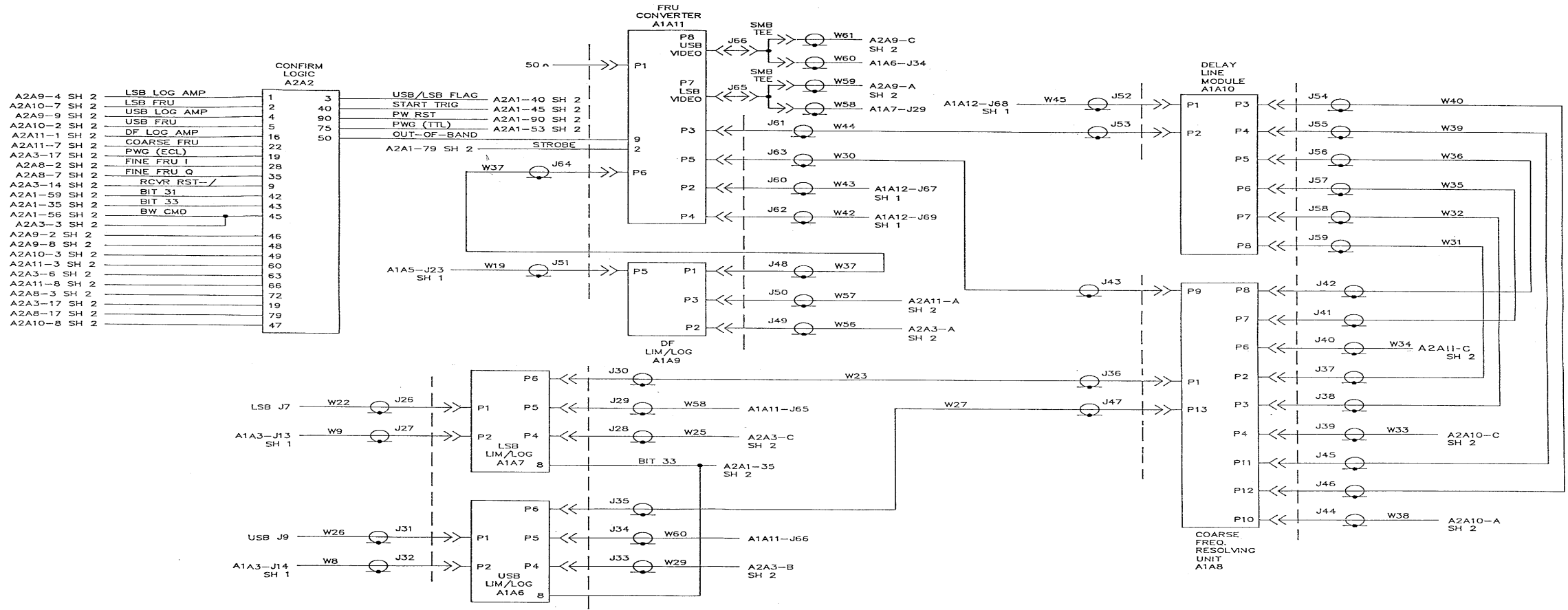
NOTES:  
 1. UNLESS OTHERWISE SPECIFIED:  
 CAPACITANCE VALUES ARE IN MICROFARADS.  
 RESISTANCE VALUES ARE IN OHMS.  
 INDUCTANCE VALUES ARE IN MICROHENRIES.

FO-4. IFP Block Diagram (Sheet 1 of 3)





FO-4. IFP Block Diagram (Sheet 2 of 3)



FO-4. IFP Block Diagram (Sheet 3 of 3)

By Order of the Secretary of the Army:

GORDON R. SULLIVAN  
General, United States Army  
Chief of Staff

Official:

MILTON H. HAMILTON  
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# THE METRIC SYSTEM AND EQUIVALENTS

## WEIGHT MEASURE

1 Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches  
 1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches  
 1 Kilometer = 1000 Meters = 0.621 Miles

## WEIGHTS

1 Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces  
 1 Kilogram = 1000 Grams = 2.2 lb.  
 1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

## LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces  
 1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

## SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches  
 1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet  
 1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

## CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches  
 1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

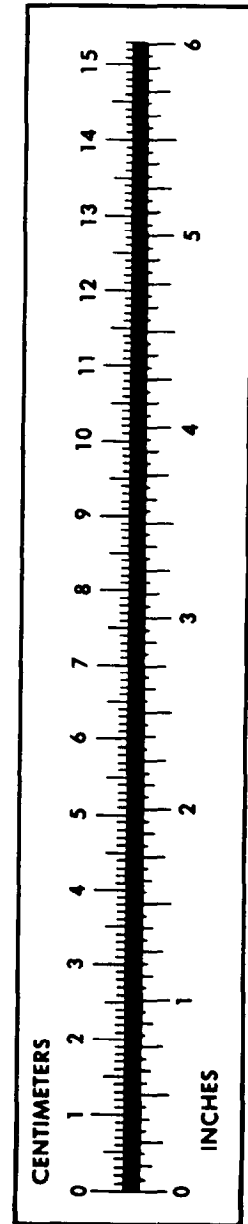
## TEMPERATURE

$5/9(^{\circ}\text{F} - 32) = ^{\circ}\text{C}$   
 212° Fahrenheit is equivalent to 100° Celsius  
 90° Fahrenheit is equivalent to 32.2° Celsius  
 32° Fahrenheit is equivalent to 0° Celsius  
 $9/5^{\circ}\text{C} + 32 = ^{\circ}\text{F}$

## APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
its	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
ometers per Liter	Miles per Gallon	2.354
ometers per Hour	Miles per Hour	0.621



**PIN: 072314-000**